NEC Electronics Inc.

NEC

MEMORY PRODUCTS

1986 DATA BOOK

NEC Electronics Inc.

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1986
MEMORY
DATA BOOK

April 1986
NECEL-000154
Stock No. 600100

NEC

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GENERAL INFORMATION

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Section 1 — General Information

Introduction

This catalog provides you with details about NEC's total memory product line, which is the broadest in the industry today. NEC memories not only give you a wider selection of device types, they also allow you to choose from various configurations and process technologies within a specific type of device. The variety of NEC memories gives you greater design alternatives and the ability to choose the part that truly fits your product.

The catalog is divided into sections for each of our major memory groups: ASMs, DRAM Modules, DRAMs, XRAMs, MOS SRAMs, ECL RAMs, EPROMs, Masked ROMs, Bipolar PROMs, and Packaging Information. The selection guides include detailed specifications and packaging information. In Section 2 of this catalog, you will find a description of the quality and reliability procedures that have enabled NEC to reach the highest quality standard currently available.

Memory Product Overview

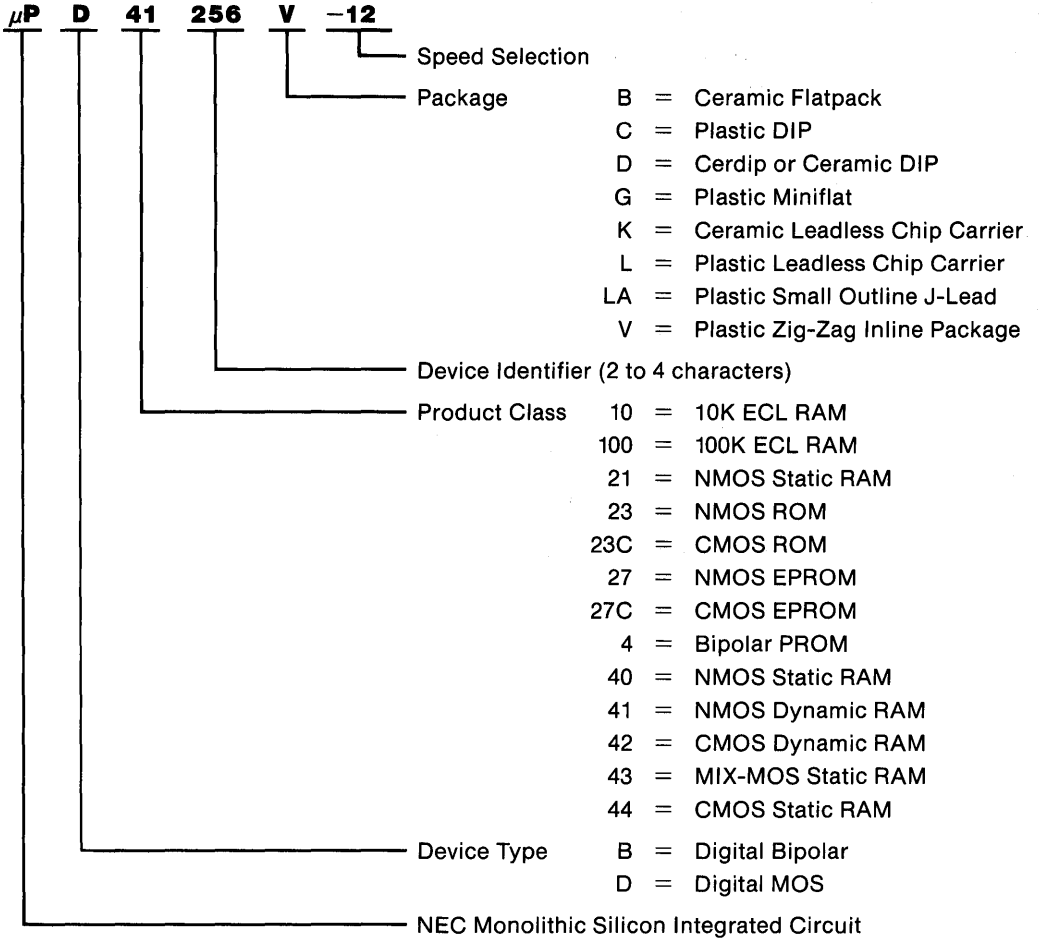
		RAM					EPROM			
Density	Application Specific	Module	Dynamic	XRAM	MOS Static	ECL	UV	OTP	ROM	Bipolar PROM
1K						μPB10422 μPB100422				
4K					μPD2147A μPD2149	μPB10470 μPB10474 μPB100470 μPB100474				μPB426
8K	μPD41101 μPD41102									
16K					μPD446 μPD449 μPD4016 μPD4311 μPD4314					μPB429
64K			μPD4164 μPD4265 μPD41416	μPD4168	μPD4361 μPD4362 μPD4364 μPD4464		μPD2764 μPD27C64	μPD2764 μPD27C64	μPD2364A μPD2364E μPD23C64E	
128K							μPD27128	μPD27128	μPD23128E μPD23C128E	
256K	μPD41221 μPD41264		μPD41256 μPD41257 μPD41464	μPD42832	μPD43256		μPD27256 μPD27C256 μPD27C256A	μPD27C256 μPD27C256A	μPD23C256E	
512K							μPD27C512			
1M		MC-41256A4 MC-41256A5 MC-411000A1	μPD411000 μPD411001 μPD414256				μPD27C1024		μPD23C1000	
2M		MC-41256A8 MC-41256A9							μPD23C2000	

Alphanumeric Index

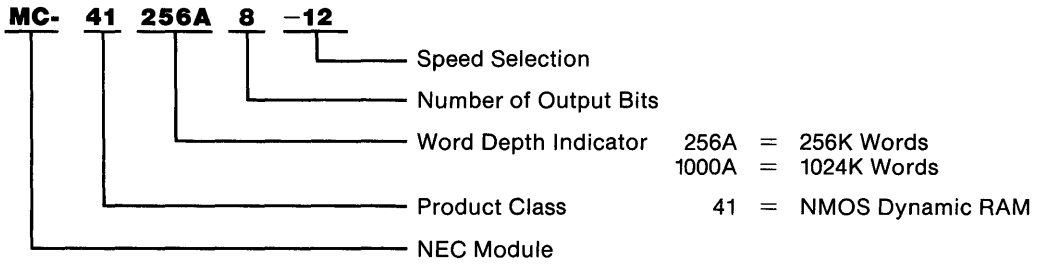
Alphanumeric Index (cont)

MEMORY PART NUMBER GUIDE

Monolithic



Module



Advanced Memory Products

Several products were in development but not yet announced at the time of printing this Data Book. In order to help the customers of NEC Electronics with their product planning and to extend the useful life of this Data Book, some of these new products are outlined below.

Application-Specific Memories

The industry-leading Video RAM is the μPD41264. In 1986 the focus for this device will be on new higher-performance versions and also denser packaging options and lower power consumption.

Other application specific memories in development are targeted for graphics, data communications, and other specialized memory requirements.

Dynamic RAM Modules

More module-based products will be announced in 1986 based on dynamic RAM and other memory technologies.

Dynamic RAMs

NEC Electronics will continue to build on its leadership position in this product category with new devices (1 M DRAMs) and enhanced performance versions of previously announced devices. Key product developments are centered around higher density, lower power, and faster access times. There are also product development trends toward higher density packaging and alternate memory organizations (x 4, x 8).

XRAMs

Higher-density products are in development in this unique product family. These products will be CMOS for low power and ease of use.

Static RAMs

1986 will be a year of many new announcements in this product family. There will be an emphasis on faster speed and lower power for the industry leader in density, the μPD43256, a 32K x 8 Mix-MOS Static RAM. In both the MOS and the ECL product families from NEC Electronics, several new high-speed products will be announced in 1986, including a 256K Mix-Mos Static RAM and a 16K ECL RAM; and there will be new speed options available on existing devices, such as the μPD4364, μPD4464, and μPD43256. In addition, NEC Electronics will continue to focus on the other needs of its customers, particularly in the areas of high-density surface mount packaging and wide memory organization (x 4, x 8).

Non-volatile Memories

In this product family, too, the emphasis will be on advanced packaging, such as for the μPD27C256AK/G (32K x 8 CMOS EPROM), and advanced products such as the μPD28C64 (8K x 8 EEPROM), OTP EPROMs, the μPD27C1024 (64K x 16 CMOS EPROM), and the μPD23C2000 (128K x 16 or 256K x 8 CMOS ROM).

Application-Specific Memory Selection Guide

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW)		Package	Pins
						Standby	Active		
μPD41101-3	910 x 8	NMOS	27	34	+5	—	495	C	24
μPD41101-2			27	34(R)/69(W)					
μPD41101-1			49	69					
μPD41102-3	1135 x 8	NMOS	21	28	+5	—	495	C	24
μPD41102-2			21	28(R)/56(W)					
μPD41102-1			40	56					
μPD41221-70	224K x 1	NMOS	55	70	+5	83	385	C	14
μPD41221-90			75	90					
μPD41264-12	64K x 4 with	NMOS	120 Port A 40 Port B	220 Port A 40 Port B	+5	66	853	C	24
μPD41264-15	dual ports		150 Port A 60 Port B	270 Port A 60 Port B			715		

Note:

Package: C = Plastic DIP

Dynamic RAM Module Selection Guide

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW)		Package	Pins
						Standby	Active		
MC-41256A4-12	256K x 4	NMOS	120	220	+5	110	1826	A/C	22
MC-41256A4-15			150	260			1540		
MC-41256A5-12	256K x 5	NMOS	120	220	+5	138	2283	A/C	24
MC-41256A5-15			150	260			1925		
MC-41256A8-12	256K x 8	NMOS	120	220	+5	220	3652	A/B	30
MC-41256A8-15			150	260			3080		
MC-41256A9-12	256K x 9	NMOS	120	220	+5	248	4109	A/B	30
MC-41256A9-15			150	260			3465		
MC-411000A1-12	1M x 1	NMOS	120	220	+5	110	539	A/C	22
MC-411000A1-15			150	260			468		

Note:

Package: A = Single Inline Memory Module (SIMM), Leaded, Glass-Epoxy Substrate; B = SIMM, Socket Mounted; C = SIMM, Leaded, Ceramic Substrate

Dynamic RAM Selection Guide

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW)		Package	Pins
						Standby	Active		
μPD4164-10	64K x 1	NMOS	100	200	+5	28	330	C	16
μPD4164-12			120	230			303		
μPD4164-15			150	260			275		
μPD4164-20			200	330			248		
μPD4265-20	64K x 1	CMOS	200	335	+5	2.8	193	C	16
μPD4265-25			250	410			165		
μPD41256-12	256K x 1	NMOS	120	220	+5	28	457	C/L/V	C = 16,
μPD41256-15			150	260			385		L = 18,
μPD41256-20			200	330			330		V = 16
μPD41257-15	256K x 1	NMOS	150	270	+5	28	385	C/L	C = 16,
μPD41257-20			200	335			330		L = 18
μPD41416-12	26K x 4	NMOS	120	220	+5	28	303	C	18
μPD41416-15			150	260			275		
μPD41416-20			200	330			248		
μPD41464-10	64K x 4	NMOS	100	200	+5	28	440	C/L	18
μPD41464-12			120	220			413		
μPD41464-15			150	260			385		
μPD411000-10	1M x 1	MNOS	100	200	+5	28	550	C/LA	C = 18,
μPD411000-12			120	220			495		LA = 26/20
μPD411000-15			150	260			440		
μPD411001-10	1M x 1	NMOS	100	200	+5	28	550	C/LA	C = 18,
μPD411001-12			120	220			495		LA = 26/20
μPD411001-15			150	260			440		
μPD414256-10	256K x 4	NMOS	100	200	+5	28	550	C/LA	C = 20,
μPD414256-12			120	220			495		LA = 26/20
μPD414256-15			150	260			440		

Note:

Package: C = Plastic DIP; L = Plastic Leaded Chip Carrier; V = Zig-zag Inline Package; LA = Small Outline J-Lead Package

XRAM Selection Guide

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW)		Package	Pins
						Standby	Active		
μPD4168-12	8K x 8	NMOS	120	220	+5	28	358	C	28
μPD4168-15			150	260			330		
μPD4168-20			200	330			303		
μPD42832-10	32K x 8	CMOS	100	160	+5	2.8	330	C/G	28
μPD42832-12			120	190			275		
μPD42832-15			150	235			220		

Note:

Package: C = Plastic DIP; G = Plastic Miniflat Package

MOS Static RAM Selection Guide

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW)		Package	Pins
						Standby	Active		
μPD446-3	2K x 8	CMOS	150	150	+5	0.055*	209	C/G	24
μPD446-2			200	200			165		
μPD446-1			250	250			143		
μPD446			450	450			99		
μPD449-3	2K x 8	CMOS	150	150	+5	0.055*	209	C	24
μPD449-2			200	200			165		
μPD449-1			250	250			143		
μPD449			450	450			99		
μPD2147A-25	4K x 1	NMOS	25	25	+5	110	880	D	18
μPD2147A-35			35	35					
μPD2147A-45			45	45					
μPD2149-2	1K x 4	NMOS	35	35	+5	—	990	D	18
μPD2149-1			45	45					
μPD2149			55	55					
μPD4016-5	2K x 8	NMOS	120	120	+5	83	330	C	24
μPD4016-3			150	150					
μPD4016-2			200	200					
μPD4016-1			250	250					
μPD4311-35	16K x 1	Mix-MOS	35	35	+5	11	440	C	20
μPD4311-45			45	45					
μPD4311-55			55	55					
μPD4314-35	4K x 4	Mix-MOS	35	35	+5	11	440	C	20
μPD4314-45			45	45					
μPD4314-55			55	55					
μPD4361-40	64K x 1	Mix-MOS	40	40	+5	11	660	K	22
μPD4361-45			45	45				C/K	
μPD4361-55			55	55				C/K	
μPD4361-70			70	70				C	
μPD4362-45	16K x 4	Mix-MOS	45	45	+5	11	495	C	22
μPD4362-55			55	55					
μPD4362-70			70	70					
μPD4364-12	8K x 8	Mix-MOS	120	120	+5	11/0.55/0.055	220	C/G	28
μPD4364-15			150	150			220		
μPD4364-20			200	200			193		
μPD4464-15	8K x 8	CMOS	150	150	+5	0.055/0.0055	220	C/G	28
μPD4464-20			200	200			193		
μPD43256-10	32K x 8	Mix-MOS	100	100	+5	11/0.55	385	C/G	28
μPD43256-12			120	120					
μPD43256-15			150	150					

Note:

Package: C = Plastic DIP; G = Plastic Miniflat Package; D = Cerdip; K = Ceramic Leadless Chip Carrier (LCC)

* Lower power version available; refer to the data sheet for more detail.

ECL RAM Selection Guide

Device	Organization	Process	Address Access Time (ns)	Chip Select Access Time (ns)	Supply Voltage	Maximum Power Dissipation (mW)	Package	Pins
μPB10422-7	256 x 4	10K	7	5*	−5.2	1144	D	24
μPB10422-10			10	5*				
μPB10470-10	4K x 1	10K	10	6	−5.2	1144	D	18
μPB10470-15			15	8				
μPB10474-8	1K x 4	10K	8	5	−5.2	1144	D	24
μPB10474-10			10	6				
μPB10474-15			15	8				
μPB100422-7	256 x 4	100K	7	5*	−4.5	990	B/D	24
μPB100422-10			10	5*				
μPB100470-10	4K x 1	100K	10	6	−4.5	990	D	18
μPB100470-15			15	8				
μPB100474-4.5	1K x 4	100K	4.5	4	−4.5	2025	K	24
μPB100474-6			6	4		2025	B/K	
μPB100474-8			8	5		990	B/D	
μPB100474-10			10	6		990	B/D	
μPB100474-15			15	8		990	B/D	

Note:

Package: D = Ceramic DIP; B = Ceramic Flat Package; K = Ceramic Leadless Chip Carrier (LCC)

* Block Select Access Time (ns).

EPROM Selection Guide

Device	Organization	Process	Access Time (ns)	Programming Option	Supply Voltage	Maximum Power Dissipation (mW)		Package	Pins
						Standby	Active		
μPD2764-2	8K x 8	NMOS	200	UV	+5	210	499	D	28
μPD2764			250	UV/OTP				C/D	
μPD2764-3			300	UV/OTP				C/D	
μPD2764-4			450	UV/OTP				C/D	
μPD27128-2	16K x 8	NMOS	200	UV	+5	210	604	D	28
μPD27128			250	UV/OTP				C/D	
μPD27128-3			300	UV/OTP				C/D	
μPD27128-4			450	UV/OTP				C/D	
μPD27256	32K x 8	NMOS	250	UV	+5	210	604	D	28
μPD27256-3			300						
μPD27C64-20	8K x 8	CMOS	200	UV	+5	0.55	165	D	28
μPD27C64-25			250	UV/OTP				C/D	
μPD27C64-30			300	UV/OTP				C/D	
μPD27C256-15	32K x 8	CMOS	150	UV	+5	0.55	165	D	28
μPD27C256-20			200	UV/OTP				C/D	
μPD27C256-25			250	UV/OTP				C/D	
μPD27C256A-12	32K x 8	CMOS	120	UV	+5*	0.55	165	D/K	28
μPD27C256A-15			150	UV/OTP				C/D/G/K	(except K = 32)
μPD27C256A-20			200	UV/OTP				C/D/G/K	
μPD27C512-15	64K x 8	CMOS	150	UV	+5*	0.55	165	D	28
μPD27C512-20			200						
μPD27C512-25			250						
μPD27C1024-15	64K x 16	CMOS	150	UV	+5*	0.55	275	D	40
μPD27C1024-20			200						
μPD27C1024-25			250						

Note:

Package: C = Plastic DIP for OTP (One Time Programmable) EPROMs; G = Plastic Miniflat Package for OTP;
D = Ceramic DIP with quartz window; K = Ceramic Leadless Chip Carrier with quartz window

*Programming voltage = 12.5 ± 0.3 V

Mask-Programmable ROM Selection Guide

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Operation	Maximum Power Dissipation (mW)* Standby	Active	Package	Pins
μPD2364A-1 μPD2364A	8K x 8	NMOS	150 200	150 200	Static	83	385	C	24
μPD2364E-1 μPD2364E	8K x 8	NMOS	200 250	200 250	Static	105	420	C	28
μPD23128E	16K x 8	NMOS	250	250	Static	138	495	C	28
μPD23C64E-1 μPD23C64E	8K x 8	CMOS	150 200	150 200	Static	0.165	165 138	C	28
μPD23C128E-1 μPD23C128E	16K x 8	CMOS	150 200	150 200	Static	0.165	165 138	C	28
μPD23C256E-1 μPD23C256E	32K x 8	CMOS	150 200	150 200	Static	0.165	165 138	C/G	28
μPD23C1000-1 μPD23C1000	128K x 8	CMOS	200 250	200 250	Static	0.55	220	C	28
μPD23C2000	128K x 16 or 256K x 8	CMOS	250	250	Static	0.55	220	C	40

Note:

Package: C = Plastic DIP; G = Plastic Miniflat Package

* Supply voltage = +5 V for all ROMs.

Bipolar PROM Selection Guide

Device	Organization	Process	Address Access Time (ns)	Chip Select Access Time (ns)	Supply Voltage	Maximum Power Dissipation (mW)	Package	Pins
μPB426-3	1K x 4	TTL	35	25	+5	826	C/D	18
μPB426-2			50	30				
μPB426-1			60	40				
μPB426			70	45				
μPB429-3	2K x 8	TTL	45	30	+5	880	C/D	24
μPB429-2			50	30				
μPB429-1			60	40				
μPB429			70	50				

Note:

Package: C = Plastic DIP; D = Ceramic DIP

NEC

QUALITY AND RELIABILITY

2

Section 2 — Quality and Reliability

Introduction

NEC has adopted Total Quality Control (TQC) to ensure the highest quality and reliability of its state-of-the-art memory products. With TQC, excellence is built into the product at every phase of production.

As large-scale integration reaches higher density levels, simple quality inspections cannot ensure adequate levels of excellence. Only with TQC during every stage of production, can NEC maintain its total product superiority in the semiconductor industry.

Approaches to Total Quality Control

Total Quality Control enables early detection of possible failures in memory products, so that problems in design may be prevented. Immediate action can then be taken before a problem occurs.

At NEC, all employees are involved with the concept and methodology of TQC. This quality insurance policy is an integral part of the entire organization.

NEC's research and development constantly strives to achieve higher standards. This ongoing process reduces extensive failure analysis and corrective actions taken as preventative measures.

Our goals are to upgrade quality standards and to further improve the superior product that has become synonymous with the NEC name.

Implementations of Distributed Quality Control

Building excellence into a product requires the earliest possible detection of failure in each phase. Immediate action is taken to remove the cause of failure. Because fixed-station quality inspection often precludes the ability to take immediate action, it is necessary to perform quality control functions at each step — especially at the conceptual stage.

Here are the significant stages

- ☐ Product development
- ☐ Wafer processing
- ☐ Assembly
- ☐ Electrical testing and screening
- ☐ Pre-inventory inspection
- ☐ Reliability assurance test

Product Development

The product development phase includes product conception, review of the device proposal, organization and physical element design, engineering evaluations, and transfer of the product to manufacturing.

In every step of the product development phase, quality and reliability requirements **must** be satisfied. Utilizing the TQC approach has shortened the product development cycles by two to three months. Building superiority into the product cannot be sacrificed — TQC is a way of life at NEC.

Wafer Fabrication Process Flow

The in-process quality inspections (frequency) that occurs at the wafer fabrication stage are as follows:

Flow	Process	Typical Item	Frequency
▽	(Wafers)		
		Dimension	Every lot
□	Incoming inspection	Resistivity	Every lot
		Appearance	Every lot
▽	(Masks)		
□	Incoming inspection		
○	Photo lithography	Alignment accuracy	Every lot
		Etching accuracy	Every lot
○	Difuse and oxidize	Oxide thickness	Every lot
		Sheet resistivity	Every lot
○	Metalize	Aluminum thickness	Every run
		Electrical parameters	Every lot
○	Passivation	CVD thickness	Every run
○	Wafer sort	Electrical characteristics	100% chips
○	Dicing		
□	Chip visual	Appearance	100% chips
▽	To assembly		

Note: The wafer fabrication steps repeated in the actual flow, which complies with our manufacturing specification, are eliminated in this diagram.

Assembly Process Flow of Plastic Memories

The in-process quality inspections (frequency) that are done during the assembly process are as follows:

Flow	Process	Typical Item	Frequency
	Chip		
	(Lead frame, solder)		
	Incoming inspection		
	Chip mounting	Appearance	Every lot
	(Fine Wire)		
	Incoming inspection		
	Wire bonding	Bond strength	Every shift
	Pre-seal visual	Appearance	100% IC's
	(Molding compound)		
	Incoming inspection		
	Molding	Appearance	100% IC's
	Thermal aging		
	Plating		
	Plating inspection	Appearance	Every lot
		Solderability	Every day
		Thickness	Every day
	Lead cut and bending		
	Marking	Marking permanency	Every run
	To test		

Electrical Testing and Screening

Electrical testing and infant mortality screening are performed at this stage. The flow chart below depicts the process.

Flow	Process	Frequency
	Assembly	
	1st electrical test	100%
	Burn-in	100%
	2nd electrical test	100%
	PDA	
	Pre-inventory inspection	Every lot
	Reliability assurance test	Every lot or every month
	Warehouse/finished goods	
	Customer	

In the first electrical test, DC parameters are tested, in accordance with electrical specifications, on 100% of each lot. This prescreen performance is completed prior to the infant mortality testing. 100% burn-in, as an integral part of the standard production process, is the most significant preventative measure NEC has implemented.

In the second electrical test, AC functional as well as DC parameter tests are performed. If the percentage of defective units exceeds a set limit, the lot is subject to an additional burn-in. During this second burn-in, the defective units undergo a failure analysis. The results of this analysis are then fed back into the process for corrective action.

Pre-Inventory Inspection

Prior to warehouse storage, lots are subject to an incoming inspection according to the following sampling plan:

- ☐ Electrical Test — DC parameters LTPD 3%
  Function test LTPD 3%
- ☐ Appearance — LTPD 3%

Reliability Assurance Test

The reliability assurance tests performed by NEC consist of high temperature operating life (HTOL), high temperature humidity life (HTSL), high humidity storage life (HHSL), and high humidity operating life (HHOL). In addition, various environmental and mechanical tests are also performed. Table 1 shows test conditions of various life tests, environmental tests, and mechanical tests performed on samples taken from similar process families on a monthly basis.

Table 1.

Test Item	Symbol	MIL-STD 883B Method, Condition	Remarks
High temperature operating life	HTOL	1005D (T_A = 125°C) V_{DD} as specified	Note 1
High temperature storage life	HTSL	1008 (T_A = 150°C)	Note 1
High humidity operating life	HHOL	T_A = 85°C at 85% RH V_{DD} as specified	Note 1
High humidity storage life	HHSL	T_A = 85°C at 85% RH	Note 1
Pressure cooker test	PCT	125°C (2.5 atm)	Note 1
Lead Fatigue	C3	2004B2	Broken lead is considered to be a reject
Solderability	C4	T_A = 230°C, 5 sec Use resin base flux	Less than 95% coverage is considered to be a reject
Soldering heat	C6	260°C, 10 sec w/out flux — Note 2	Note 1
Temperature cycle	C6	1010C; 10 cycles; −65°C to 150°C	Note 1
Thermal shock	C6	1011A; 15 cycles 0°C to 100°C	Note 1

Notes: 1. Electrical test per data sheet is performed. Devices that exceed these data sheet limits are considered to be rejects.
2. MIL-STD-750A Method 2031.

Summary

Building quality and reliability into products is the most efficient way to ensure product excellence. NEC's TQC process steps form a consolidated quality control system and guarantees a superior product.

The introduction of 100% burn-in and the performance of monthly reliability assurance tests, have established a singularly high standard of excellence for NEC's large-scale integrated circuits.

With total commitment to Total Quality Control, NEC is committed to producing superior products. Through continuous research and development, extensive failure analysis and process improvements, NEC continues to set and maintain the highest standards of quality and reliability.

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APPLICATION-SPECIFIC MEMORIES

3

Section 3 — Application-Specific Memories

μPD41101
910 x 8-BIT FIFO MEMORY

PRELIMINARY INFORMATION

Description

This device is a 910-word by 8-bit first-in first-out biport memory fabricated with the N-channel silicon gate process. The device helps to create an NTSC flicker-free television picture (noninterlace conversion) by providing intermediate storage and very high speed read and write operations.

The μPD41101 can also be used as a digital delay line. The delay length is variable from 10 to 910 bits.

Features

- ☐ 910-word x 8-bit organization
- ☐ FIFO (first-in first-out) biport memory
- ☐ Suitable for NTSC, $4f_{SC}$ digital television systems
- ☐ Asynchronous and simultaneous read/write operations
- ☐ Can be used as a 1H (910-bit) delay line
- ☐ TTL compatible
- ☐ Three-state outputs
- ☐ Single 5 V ± 10% power supply
- ☐ 24-pin, 300 mil DIP package

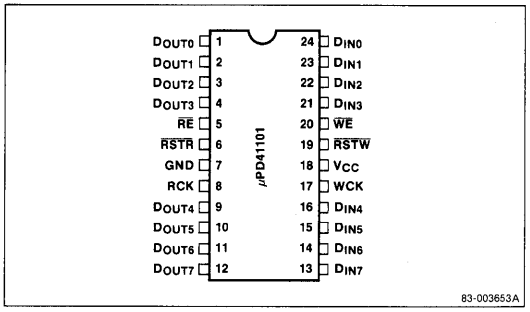
Performance Ranges

Device	Read Cycle Time (Min)	Read Access Time (Max)	Write Cycle Time (Min)
μPD41101-3	34 ns	27 ns	34 ns
μPD41101-2	34 ns	27 ns	69 ns
μPD41101-1	69 ns	49 ns	69 ns

Pin Identification

No.	Symbol	Function
1-4, 9-12	D_{OUT0}-D_{OUT7}	Read data outputs
5	$\overline{RE}$	Read enable input
6	$\overline{RSTR}$	Read address reset input
7	GND	Ground
8	RCK	Read clock input
13-16, 21-24	D_{IN0}-D_{IN7}	Write data inputs
17	WCK	Write clock input
18	V_{CC}	5 V power supply
19	$\overline{RSTW}$	Write address reset input
20	$\overline{WE}$	Write enable input

Pin Configuration



Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]

In a digital television application, the digital composite signal, luminance, chrominance, etc., information is written into these inputs.

D_{OUT0}-D_{OUT7} [Data Outputs]

These tri-state outputs are used to access the stored information. In a simple digital delay line application, a minimum delay of 10 clock cycles is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ [Write Address Reset Input]

Bringing this signal to a low level resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ [Read Address Reset Input]

Strobed by the rising edge of RCK, this signal resets the internal read address to 0.

$\overline{WE}$ [Write Enable Input]

This input controls write operations. If $\overline{WE}$ is at a low level, all write operations proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ [Read Enable Input]

This signal is similar to $\overline{WE}$ but controls read operations. If $\overline{RE}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK [Write Clock Input]

All write operations are performed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 909 to 0 and begin increasing again.

RCK [Read Clock Input]

All read operations are performed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts the internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 909 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram

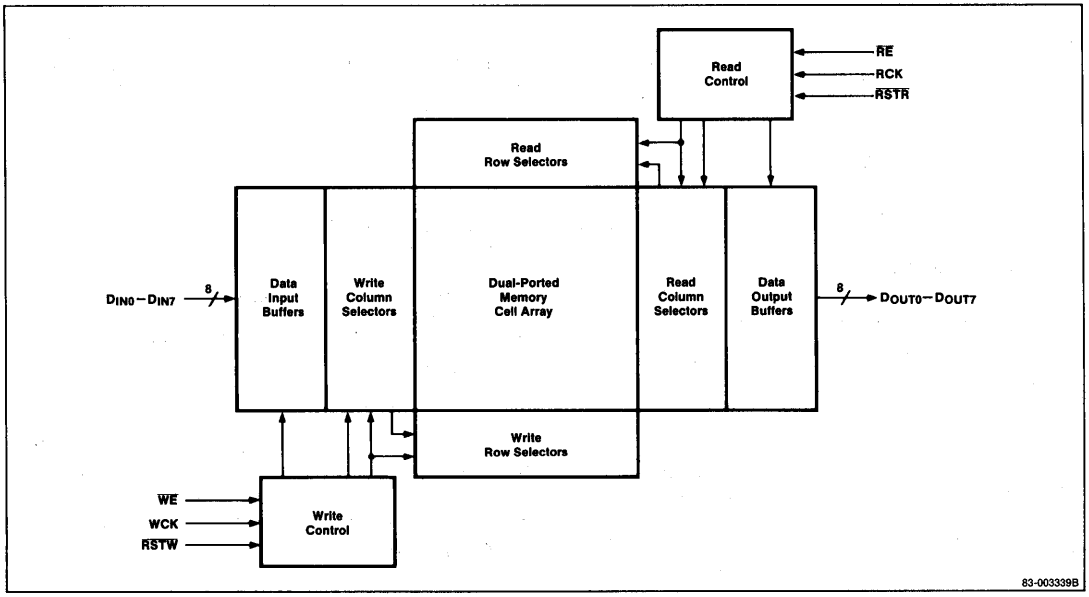
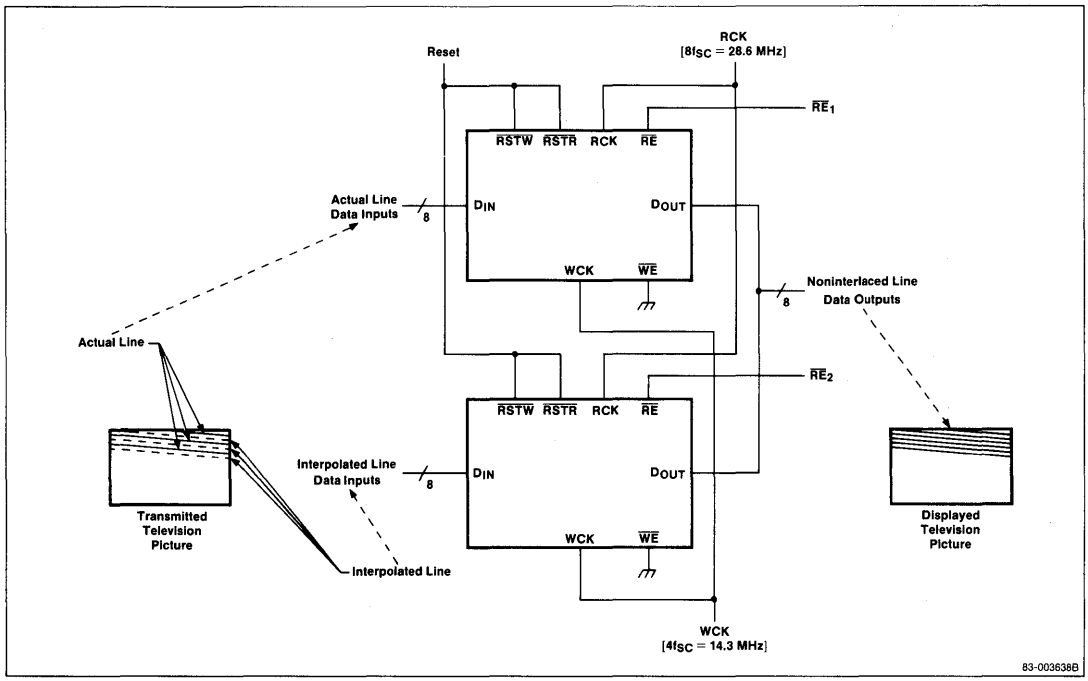


Figure 1. Connection for Noninterlace Conversion



Recommended DC Operating Conditions

$T_A = -20$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Ground	GND	0	0	0	V	
Input voltage high	V_{IH}	2.4		5.5	V	
Input voltage low	V_{IL}	−1.5		0.8	V	

Capacitance

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, $\overline{RCK}$, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Note:
(1) These parameters are sampled and not 100% tested.

DC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Write/Read cycle operating current	I_{CC}			90	mA	
Input leakage current	I_I	−10		10	μA	$V_I = 0$ to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} is disabled; $V_O = 0$ to 5.5 V
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -1$ mA
Output voltage low	V_{OL}			0.4	V	$I_{OL} = 2$ mA

Note:
(1) All voltages are referenced to ground.

AC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Symbol	Parameter	Limits μPD41101-3 Min	Limits μPD41101-3 Max	Limits μPD41101-2 Min	Limits μPD41101-2 Max	Limits μPD41101-1 Min	Limits μPD41101-1 Max	Unit	Test Conditions
t_{WCK}	Write clock cycle time	34	1090	69	1090	69	1090	ns	
t_{WCW}	WCK pulse width	14		25		25		ns	
t_{WCP}	WCK precharge time	14		25		25		ns	
t_{RCK}	Read clock cycle time	34	1090	34	1090	69	1090	ns	
t_{RCW}	RCK pulse width	14		14		25		ns	
t_{RCP}	RCK precharge time	14		14		25		ns	
t_{AC}	Access time		27		27		49	ns	
t_{ACR}	Access time after a reset cycle		49		49		49	ns	
t_{OH}	Output hold time	5		5		5		ns	
t_{OHR}	Output hold time after a reset cycle	5		5		5		ns	(Note 7)
t_{LZ}	Output active time	5	27	5	27	5	49	ns	(Note 4)
t_{HZ}	Output disable time	5	27	5	27	5	49	ns	(Note 4)
t_{DS}	Data-in set-up time	14		18		18		ns	
t_{DH}	Data-in hold time	5		5		5		ns	
t_{RS}	Reset active set-up time	14		14		20		ns	(Note 8)
t_{RH}	Reset active hold time	5		5		5		ns	(Note 8)
t_{RN1}	Reset inactive hold time	5		5		5		ns	(Note 9)
t_{RN2}	Reset inactive set-up time	14		14		20		ns	(Note 9)
t_{WES}	Write enable set-up time	14		20		20		ns	(Note 10)
t_{WEH}	Write enable hold time	5		5		5		ns	(Note 10)
t_{WEN1}	Write enable high delay from WCK	5		5		5		ns	(Note 11)
t_{WEN2}	Write enable low delay to WCK	14		20		20		ns	(Note 11)
t_{RES}	Read enable set-up time	14		14		20		ns	(Note 10)
t_{REH}	Read enable hold time	5		5		5		ns	(Note 10)
t_{REN1}	Read enable high delay from RCK	5		5		5		ns	(Note 11)
t_{REN2}	Read enable low delay to RCK	14		14		20		ns	(Note 11)
t_{WEW}	Write disable pulse width	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_{REW}	Read disable pulse width	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_{RSTW}	Write reset time	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_{RSTR}	Read reset time	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_T	Transition time	3	35	3	35	3	35	ns	

Note:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume $t_T = 5$ ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ± 200 mv from the steady state voltage with the load specified in figure 4. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

AC Characteristics (cont)

Note [cont]:

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the next equations in 1 line cycle operation:
$t_{WEW} + t_{RSTW} + 910t_{WCK} \leq 1$ ms
$t_{REW} + t_{RSTR} + 910t_{RCK} \leq 1$ ms

(7) This parameter has meaning when $t_{RCK} \geq t_{ACR}$ (max).

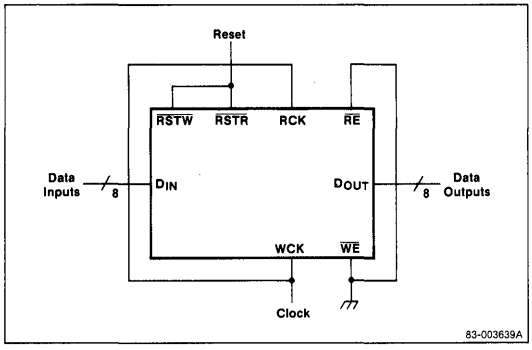
(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

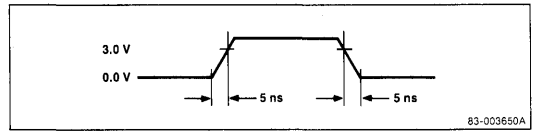
(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 2. Connection for a 1H (910 Bit) Delay Line



AC Input Timing Reference Waveform



AC Output Timing Reference Waveform

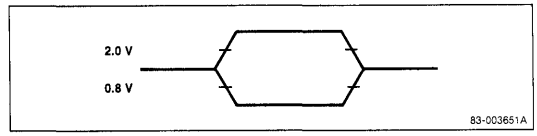


Figure 3. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

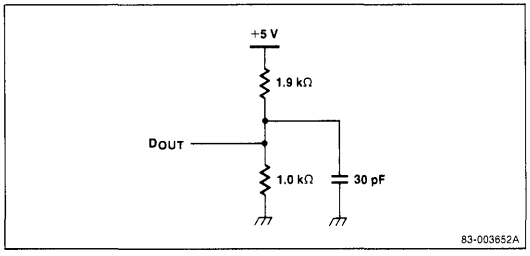
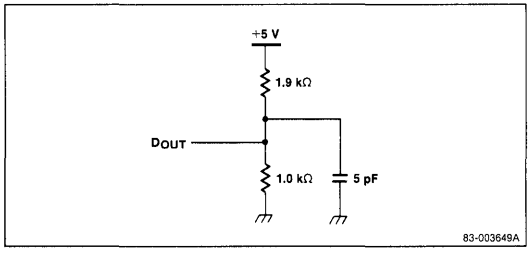
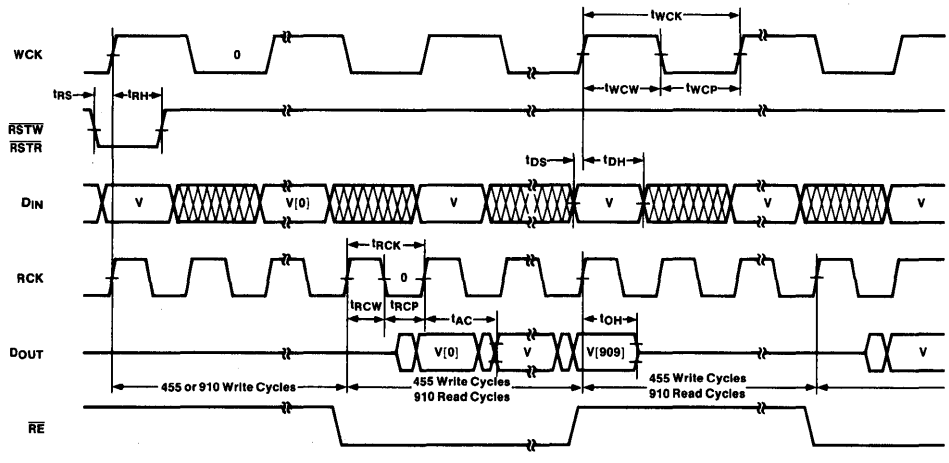


Figure 4. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

Basic Timing for Noninterlace Conversion



Note:

[1] $\overline{WE} = V_{IL}$.

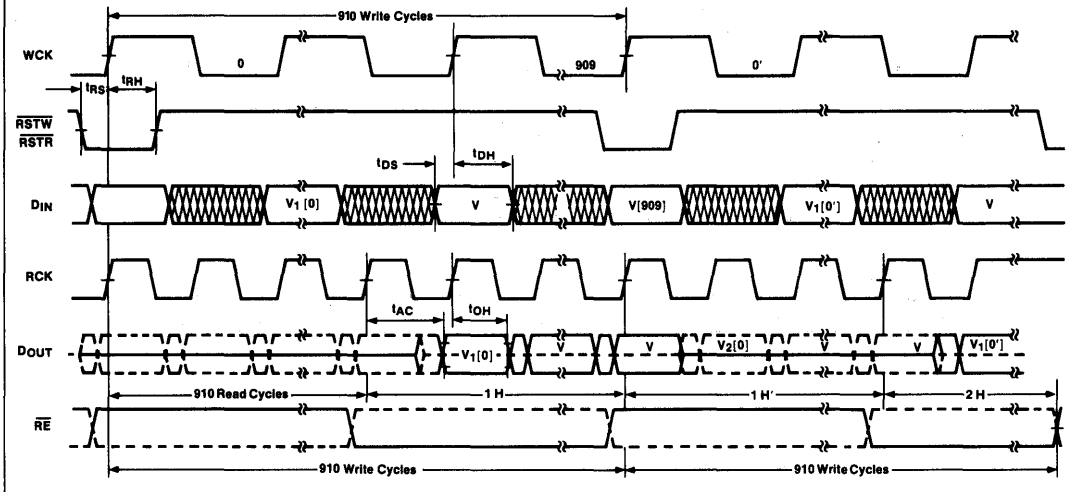
[2] V = Valid Data.

[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

83-003655B

Timing Waveforms (cont)

Application Timing for Noninterlace Conversion



Note:

[1] $\overline{WE} = V_{IL}$.

[2] V = Valid Data.

[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

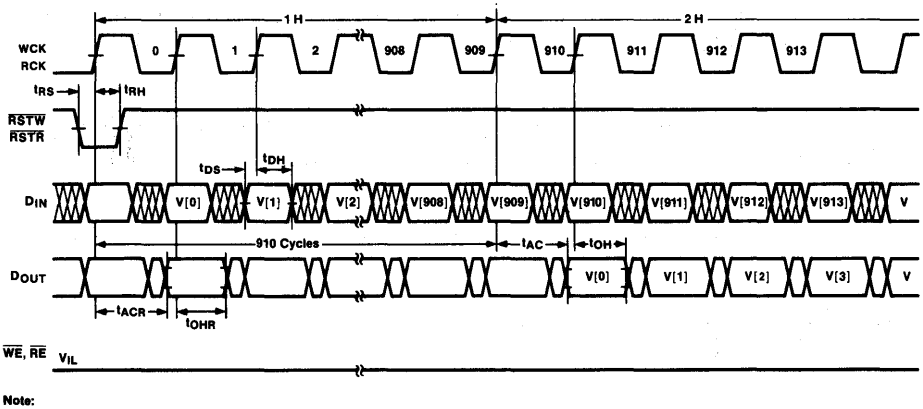
[4] 1H = the first "actual line" of 910 words. 1H' = the first [normally] interpolated line of 910 words. See Figure 1.

[5] See Figure 1. D_{IN} above represents the scan line input to one of the two μPD41101s. D_{OUT} and $\overline{RE}$ above represent the combined output and the complementary $\overline{RE}$ inputs for both devices. The signals for one μPD41101 are drawn as solid lines; the signals for the second μPD41101, as dashed lines.

[6] Reset pulses can be applied to $\overline{RSTW}$ and $\overline{RSTR}$ at regular intervals to remove any effects due to jitter in the system clock.

83-003656C

910-Bit Delay Line



Note:

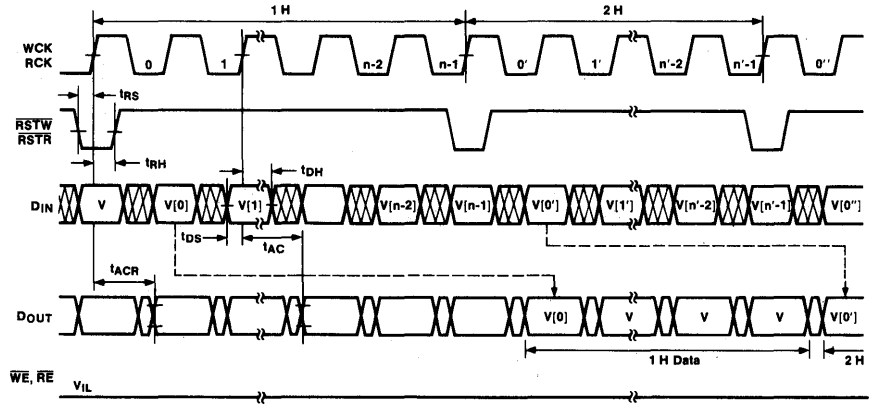
[1] V = Valid Data.

[2] 1H = the first group of 910 bits. 2H = the second group of 910 bits.

83-003657B

Timing Waveforms (cont)

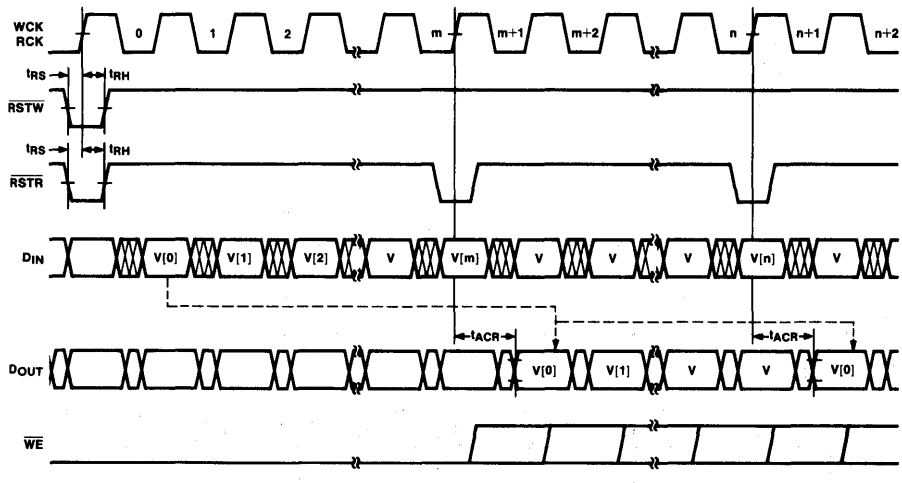
n-Bit Delay Line



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n bits.

83-003643B

Re-Read Operation

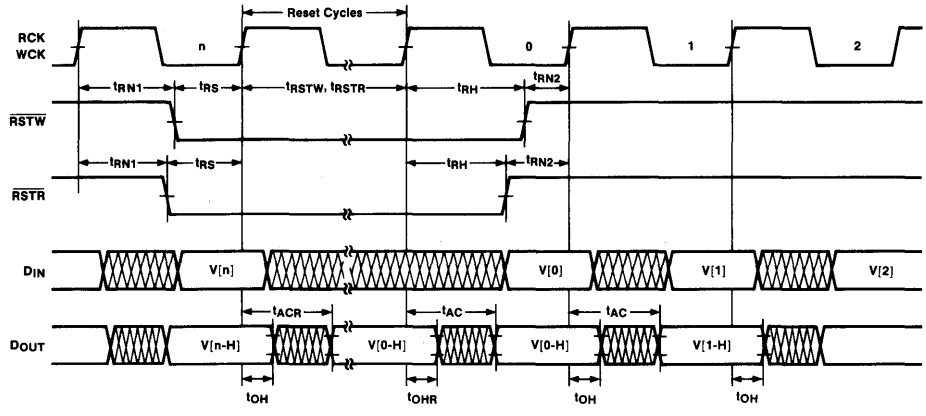


Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

Timing Waveforms (cont)

Read or Write Reset



Note:

[1] $\overline{WE} = \overline{RE} = V_{IL}$.

[2] V = Valid Data.

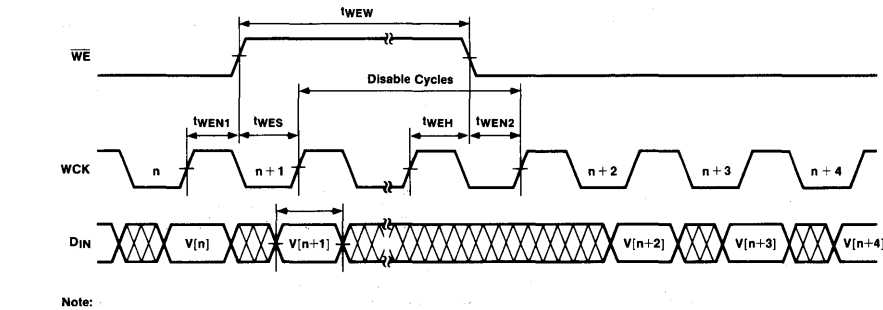
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

[4] H = 910 cycles.

[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83-003645B

Write Disable



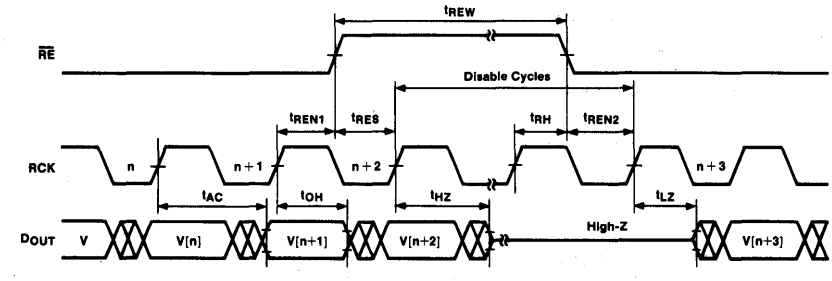
Note:

[1] V = Valid Data.

83-003723B

Timing Waveforms (cont)

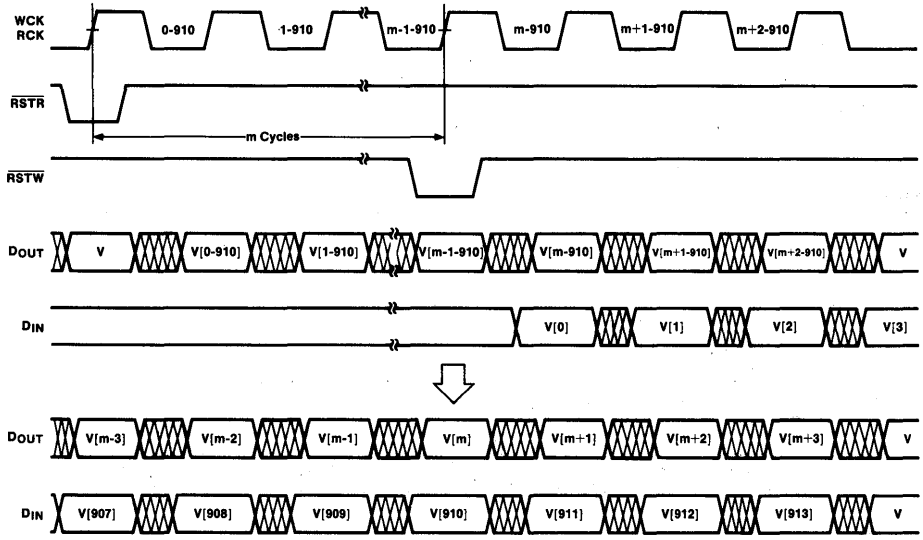
Read Disable



Note:
[1] V = Valid Data.

83-003646B

(910-m)-Bit Delay Line, No. 1

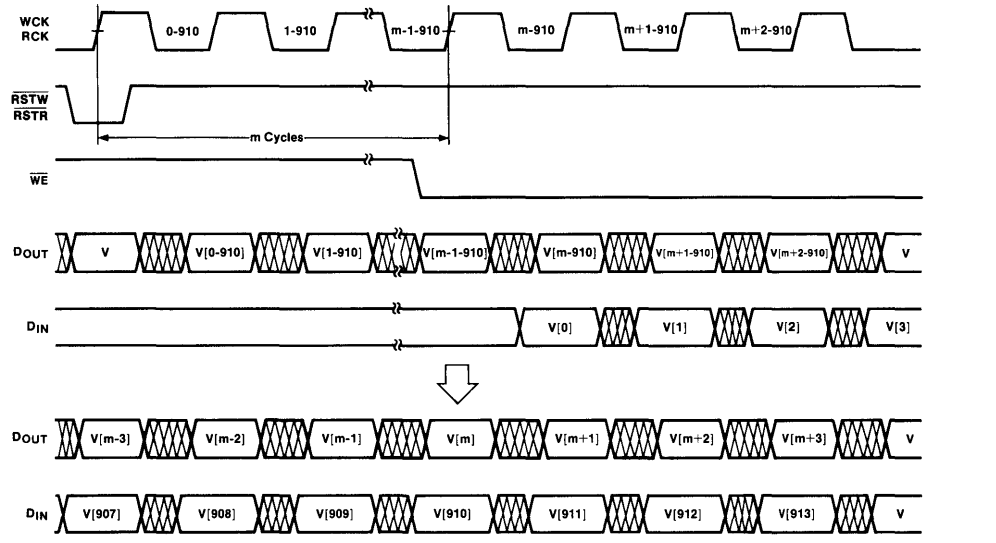


Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.

83-003658B

Timing Waveform (cont)

(910-m)-Bit Delay Line, No. 2



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

83-003659B

3

μPD41102
1135 x 8-BIT FIFO MEMORY

PRELIMINARY INFORMATION

Description

This device is a 1135-word by 8-bit first-in first-out biport memory fabricated with the N-channel silicon gate process. The device helps to create a PAL flicker-free television picture (noninterlace conversion) by providing intermediate storage and very high speed read and write operations.

The μPD41102 can also be used as a digital delay line. The delay length is variable from 12 to 1135 bits.

Features

- ☐ 1135-word x 8-bit organization
- ☐ FIFO (first-in first-out) biport memory
- ☐ Suitable for PAL, $4f_{SC}$ digital television systems
- ☐ Asynchronous and simultaneous read/write operations
- ☐ Can be used as a 1H (1135-bit) delay line
- ☐ TTL compatible
- ☐ Three-state outputs
- ☐ Single 5 V ± 10% power supply
- ☐ 24-pin, 300 mil DIP package

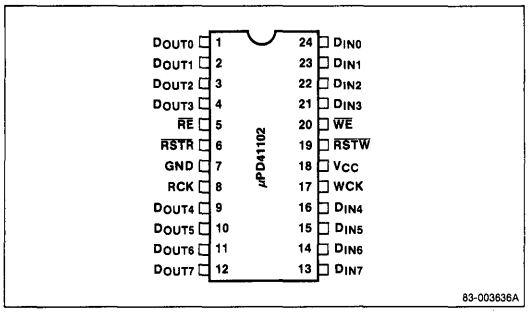
Performance Ranges

Device	Read Cycle Time (Min)	Read Access Time (Max)	Write Cycle Time (Min)
μPD41102-3	28 ns	21 ns	28 ns
μPD41102-2	28 ns	21 ns	56 ns
μPD41102-1	56 ns	40 ns	56 ns

Pin Identification

No.	Symbol	Function
1-4, 9-12	D_{OUT0}-D_{OUT7}	Read data outputs
5	$\overline{RE}$	Read enable input
6	$\overline{RSTR}$	Read address reset input
7	GND	Ground
8	RCK	Read clock input
13-16, 21-24	D_{IN0}-D_{IN7}	Write data inputs
17	WCK	Write clock input
18	V_{CC}	5 V power supply
19	$\overline{RSTW}$	Write address reset input
20	$\overline{WE}$	Write enable input

Pin Configuration



Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]

In a digital television application, the digital composite signal, luminance, chrominance, etc., information is written into these inputs.

D_{OUT0}-D_{OUT7} [Data Outputs]

These tri-state outputs are used to access the stored information. In a simple digital delay line application, a minimum delay of 12 clock cycles is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ [Write Address Reset Input]

Bringing this signal to a low level resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ [Read Address Reset Input]

Strobed by the rising edge of RCK, this signal resets the internal read address to 0.

$\overline{WE}$ [Write Enable Input]

This input controls write operations. If $\overline{WE}$ is at a low level, all write operations proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ [Read Enable Input]

This signal is similar to $\overline{WE}$ but controls read operations. If $\overline{RE}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK [Write Clock Input]

All write operations are performed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 1134 to 0 and begin increasing again.

RCK [Read Clock Input]

All read operations are performed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts the internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 1134 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram

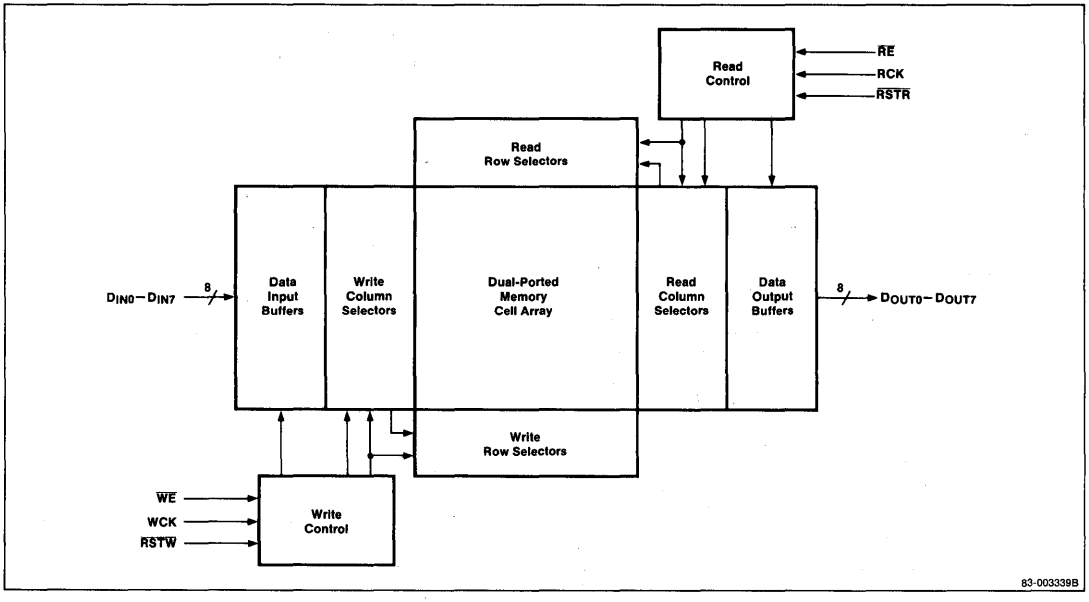
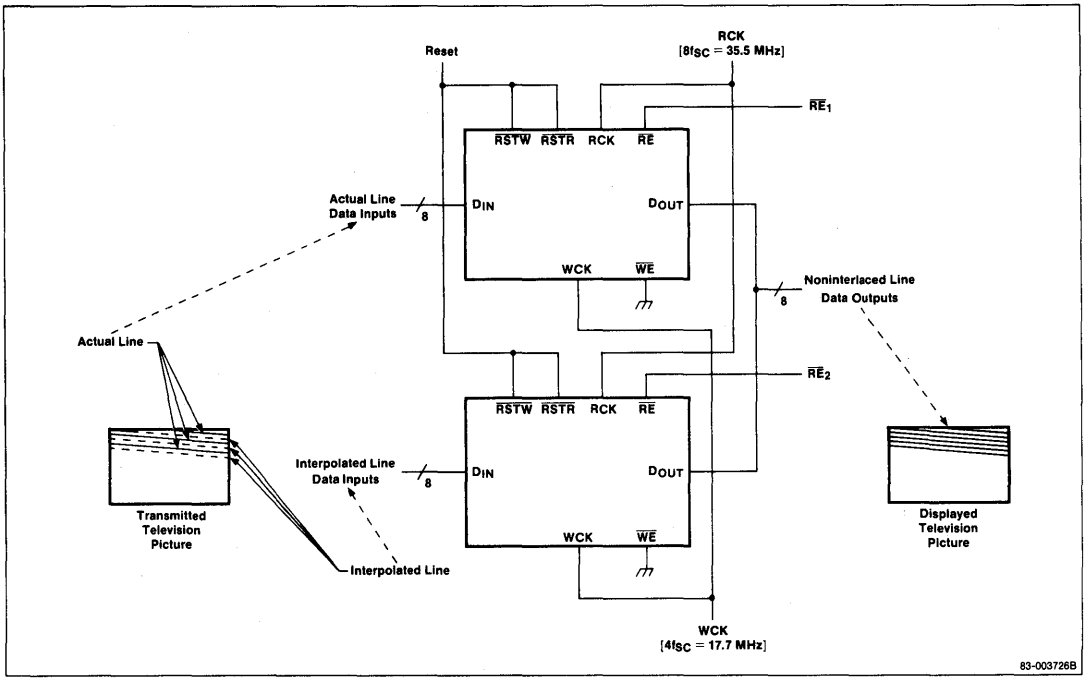


Figure 1. Connection for Noninterlace Conversion



3

Recommended DC Operating Conditions

$T_A = -20$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Ground	GND	0	0	0	V	
Input voltage high	V_{IH}	2.4		5.5	V	
Input voltage low	V_{IL}	−1.5		0.8	V	

Capacitance

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Note:
(1) These parameters are sampled and not 100% tested.

DC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Write/Read cycle operating current	I_{CC}			90	mA	
Input leakage current	I_I	−10		10	μA	$V_I = 0$ to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} is disabled; $V_O = 0$ to 5.5 V
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -1$ mA
Output voltage low	V_{OL}			0.4	V	$I_{OL} = 2$ mA

Note:
(1) All voltages are referenced to ground.

AC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Symbol	Parameter	Limits μPD41102-3 Min	Limits μPD41102-3 Max	Limits μPD41102-2 Min	Limits μPD41102-2 Max	Limits μPD41102-1 Min	Limits μPD41102-1 Max	Unit	Test Conditions
t_{WCK}	Write clock cycle time	28	880	56	880	56	880	ns	
t_{WCW}	WCK pulse width	12		20		20		ns	
t_{WCP}	WCK precharge time	12		20		20		ns	
t_{RCK}	Read clock cycle time	28	880	28	880	56	880	ns	
t_{RCW}	RCK pulse width	12		12		20		ns	
t_{RCP}	RCK precharge time	12		12		20		ns	
t_{AC}	Access time		21		21		40	ns	
t_{ACR}	Access time after a reset cycle		40		40		40	ns	
t_{OH}	Output hold time	5		5		5		ns	
t_{OHR}	Output hold time after a reset cycle	5		5		5		ns	(Note 7)
t_{LZ}	Output active time	5	21	5	21	5	40	ns	(Note 4)
t_{HZ}	Output disable time	5	21	5	21	5	40	ns	(Note 4)
t_{DS}	Data-in set-up time	12		15		15		ns	
t_{DH}	Data-in hold time	5		5		5		ns	
t_{RS}	Reset active set-up time	12		12		20		ns	(Note 8)
t_{RH}	Reset active hold time	5		5		5		ns	(Note 8)
t_{RN1}	Reset inactive hold time	5		5		5		ns	(Note 9)
t_{RN2}	Reset inactive set-up time	12		12		20		ns	(Note 9)
t_{WES}	Write enable set-up time	12		20		20		ns	(Note 10)
t_{WEH}	Write enable hold time	5		5		5		ns	(Note 10)
t_{WEN1}	Write enable high delay from WCK	5		5		5		ns	(Note 11)
t_{WEN2}	Write enable low delay to WCK	12		20		20		ns	(Note 11)
t_{RES}	Read enable set-up time	12		12		20		ns	(Note 10)
t_{REH}	Read enable hold time	5		5		5		ns	(Note 10)
t_{REN1}	Read enable high delay from RCK	5		5		5		ns	(Note 11)
t_{REN2}	Read enable low delay to RCK	12		12		20		ns	(Note 11)
t_{WEW}	Write disable pulse width	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_{REW}	Read disable pulse width	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_{RSTW}	Write reset time	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_{RSTR}	Read reset time	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
t_T	Transition time	3	35	3	35	3	35	ns	

Note:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume $t_T = 5$ ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ± 200 mv from the steady state voltage with the load specified in figure 4. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

AC Characteristic (cont)

Note [cont]:

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the next equations in 1 line cycle operation:
$t_{WEW} + t_{RSTW} + 1135t_{WCK} \leq 1$ ms
$t_{REW} + t_{RSTR} + 1135t_{RCK} \leq 1$ ms

(7) This parameter has meaning when $t_{RCK} \geq t_{ACR}$ (max).

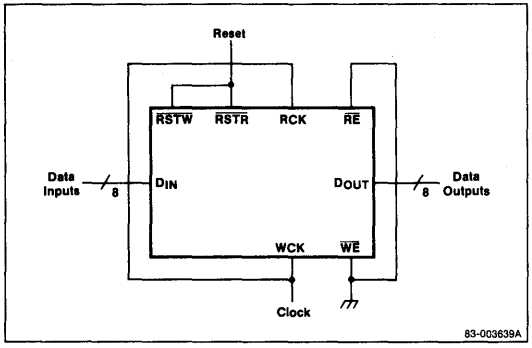
(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

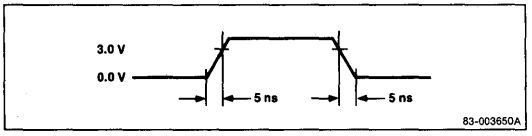
(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 2. Connection for a 1H (1135-Bit) Delay Line



AC Input Timing Reference Waveform



AC Output Timing Reference Waveform

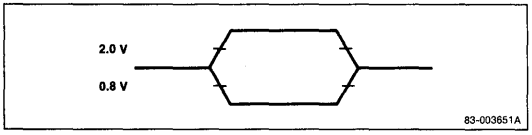


Figure 3. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

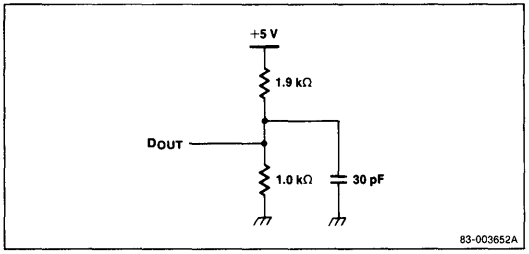
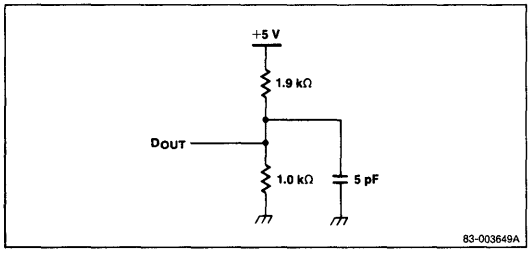
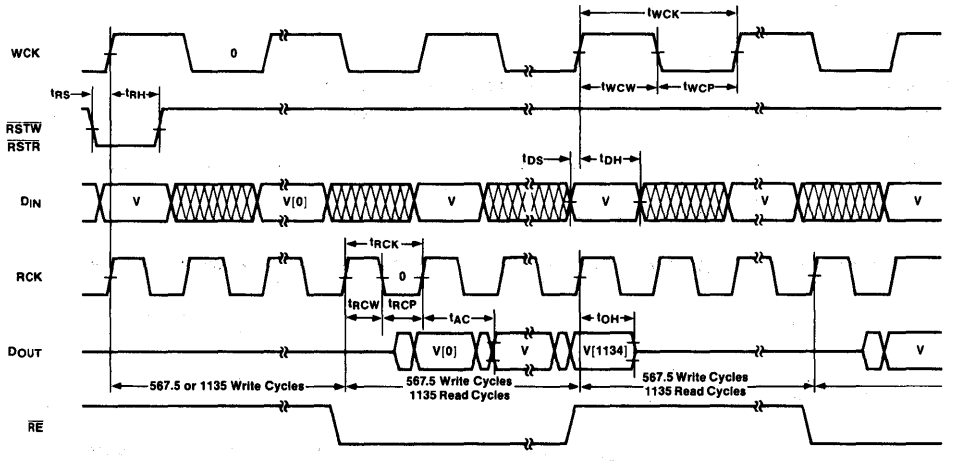


Figure 4. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms (cont)

Basic Timing for Noninterlace Conversion



Note:

[1] $\overline{WE} = V_{IL}$.

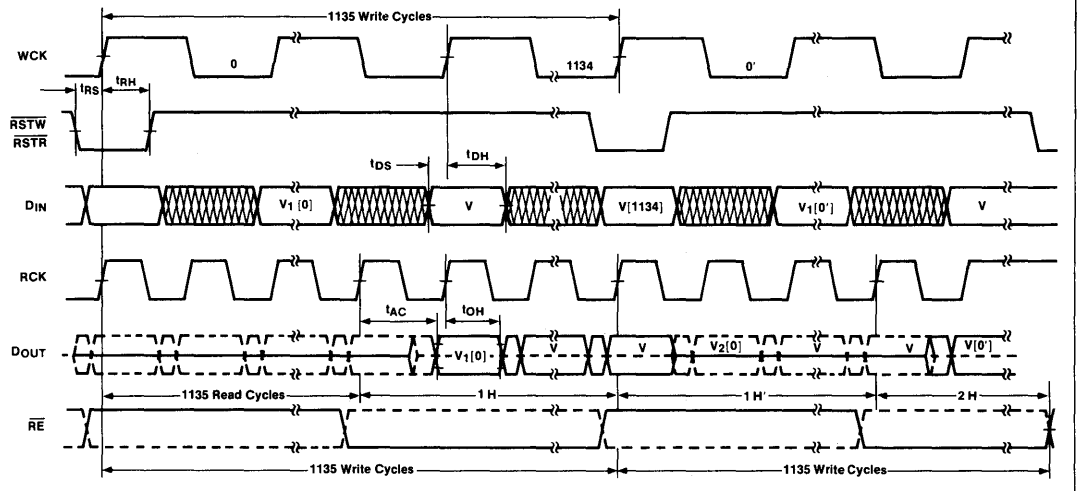
[2] V = Valid Data.

[3] For compatibility with PAL standards the WCK frequency is approximately 17.7 MHz. RCK cycles at twice this frequency, 35.5 MHz.

83-003640B

Timing Waveforms (cont)

Application Timing for Noninterlace Conversion



Note:

[1] $\overline{WE} = V_{IL}$.

[2] V = Valid Data.

[3] For compatibility with PAL standards the WCK frequency is approximately 17.7 MHz. RCK cycles at twice this frequency, 35.5 MHz.

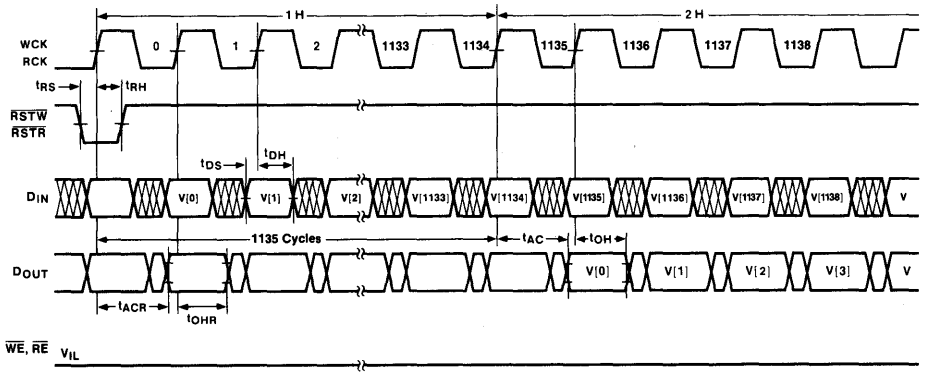
[4] 1H = the first "actual line" of 1135 words. 1H' = the first [normally] interpolated line of 1135 words. See Figure 1.

[5] See Figure 1. D_{IN} above represents the scan line input to one of the two μPD41102s. D_{OUT} and $\overline{RE}$ above represent the combined output and the complementary $\overline{RE}$ inputs for both devices. The signals for one μPD41102 are drawn as solid lines; the signals for the second μPD41102, as dashed lines.

[6] Reset pulses can be applied to $\overline{RSTW}$ and $\overline{RSTR}$ at regular intervals to remove any effects due to jitter in the system clock.

83-003641C

1135-Bit Delay Line



Note:

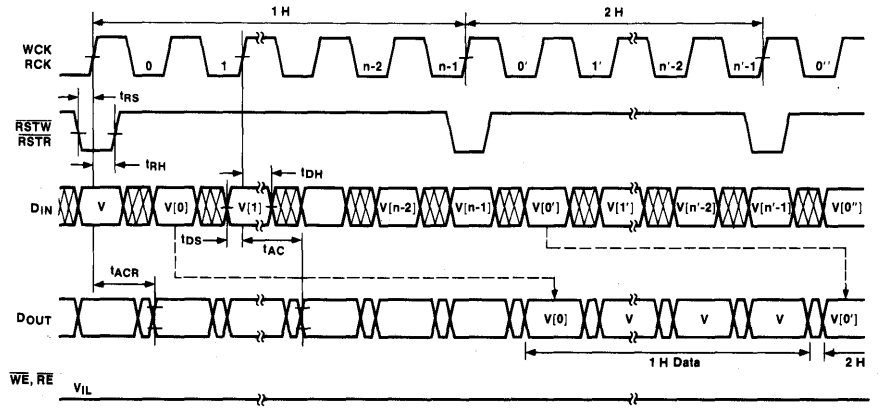
[1] V = Valid Data.

[2] 1H = the first group of 1135 bits. 2H = the second group of 1135 bits.

83-003642B

Timing Waveforms (cont)

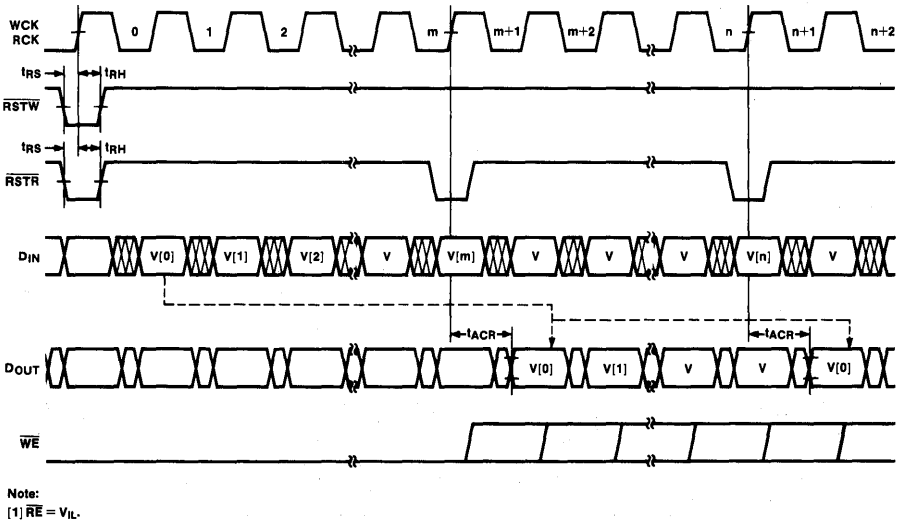
n-Bit Delay Line



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n bits.

83-003643B

Re-Read Operation

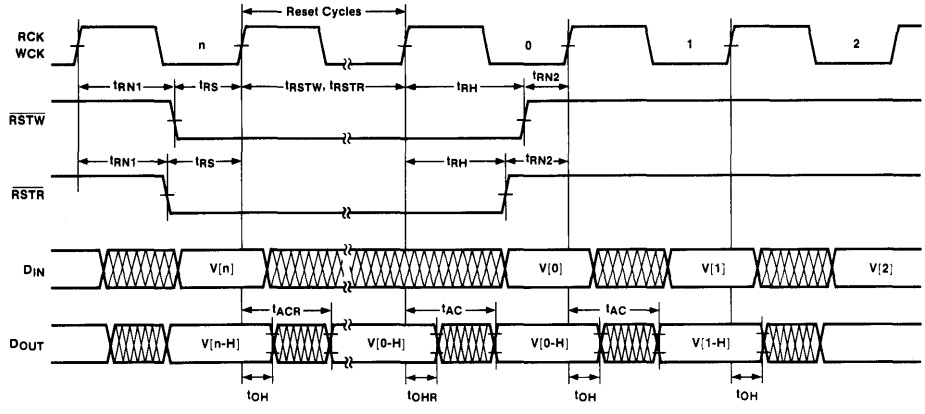


Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

Timing Waveforms (cont)

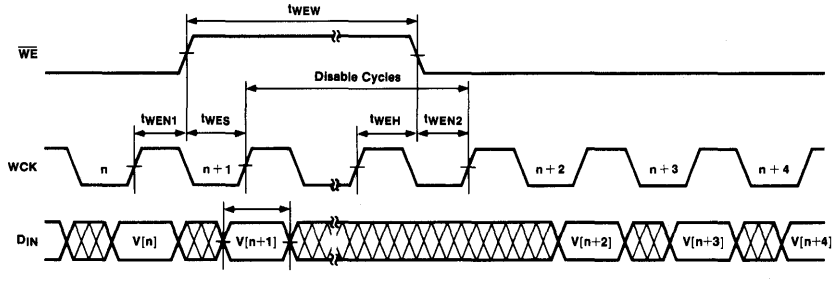
Read or Write Reset



Note:
[1] $\overline{WE} = \overline{RE} = V_{IL}$
[2] V = Valid Data.
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.
[4] H = 1135 cycles.
[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83-003727B

Write Disable

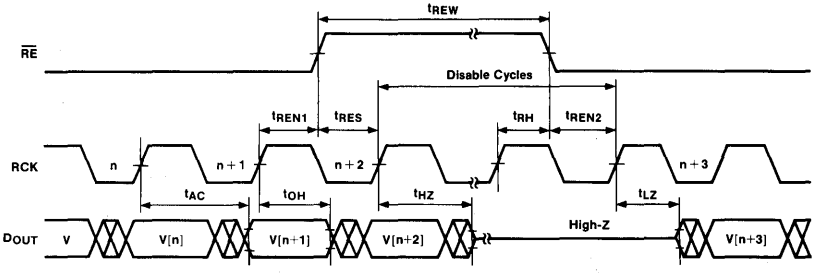


Note:
[1] V = Valid Data.

83-003723B

Timing Waveforms (cont)

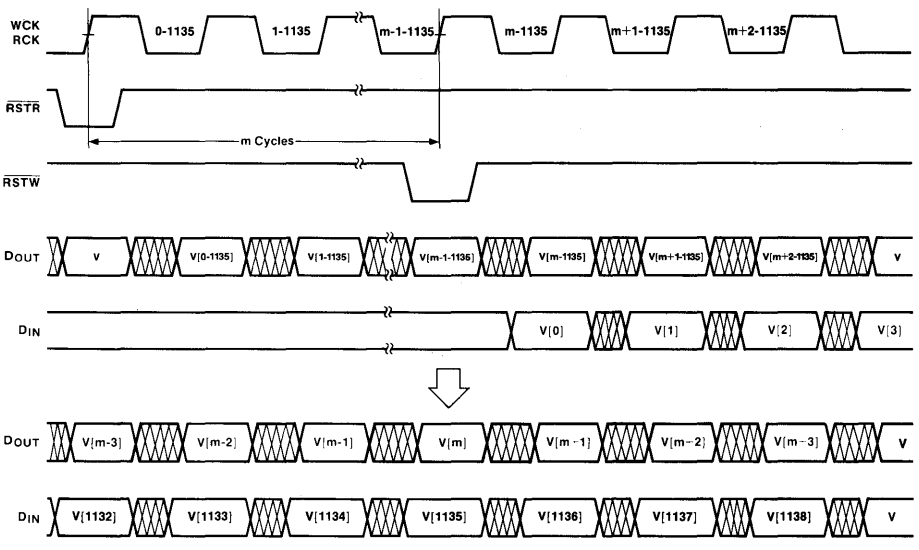
Read Disable



Note:
[1] V = Valid Data.

83-003646B

(1135-m)-Bit Delay Line, No. 1

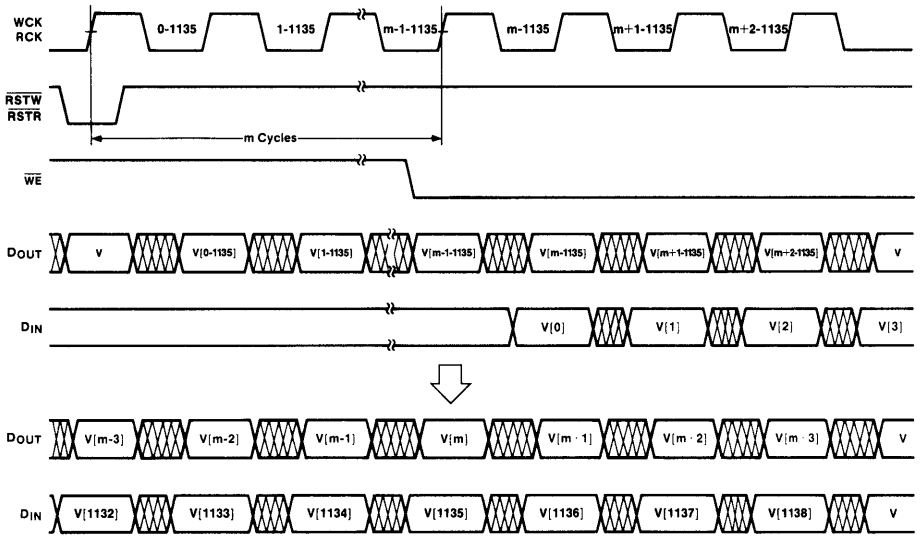


Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.

83-003647B

Timing Waveforms (cont)

(1135-m)-Bit Delay Line, No. 2



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

83-003648B

3

μPD41221
224,000-BIT
SERIAL-ACCESS NMOS RAM

Revision 1

Description

The NEC μPD41221 is a 224,000-bit serial-access memory that uses the same technology as standard N-channel MOS dynamic RAMs. The dynamic circuit technology based on the one transistor memory cell is combined with the double polysilicon NMOS process technology.

The μPD41221 is well-suited for use as a field memory for television systems. The memory array, organized as 320 rows by 700 columns, is a size that can satisfy almost all requirements for NTSC and PAL. Memory operation is based on one horizontal scanning period (1H). A serial read or write operation is executed on a row within 1H.

The operation sequence within 1H is as follows:
(1) The row location is specified by $\overline{RCR}$ (reset to row 0), $\overline{INC}$ (+1 increment), or $\overline{DEC}$ (−1 decrement).

(2) A data transfer cycle (from the row to the data register) is selected by $\overline{RAS}$ active with $\overline{WE}$ high.

(3) $\overline{SC}$ causes a serial write or read operation between the data input/output and the data register from column 0 to any column location up to 700.

(4) $\overline{REF}$ (refresh control) executes internal automatic refresh asynchronously with serial operation.

(5) A data restore cycle (from the data register to the row selected) is selected by $\overline{RAS}$ active with $\overline{WE}$ low.

Address pins are eliminated because serial address functions are built into the chip. SYN, an open-drain output, is in the low-impedance state from the 608th $\overline{SC}$ cycle to the beginning of the data restore cycle, allowing system designers to generate a horizontal sync signal.

The μPD41221 data register stores memory data on one word line. A fast serial read or write is executed between the data input/output and the data register. During the serial operation, data refresh cycles for the memory array can be performed asynchronously.

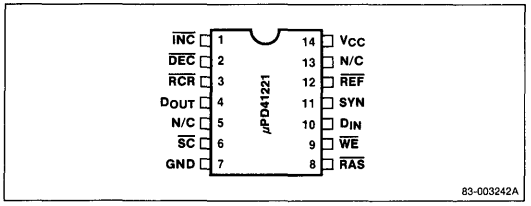
Features

- ☐ 224,000 × 1 serial-access memory
- ☐ Screen size memory array suitable for NTSC and PAL
- ☐ +5 V ± 10% single power supply
- ☐ On-chip substrate bias generator
- ☐ Two key functional blocks:
  320-row by 700-column memory array
  700-bit data register
- ☐ Full serial operation with line pointer control
- ☐ Variable serial cycle numbers up to column bit size
- ☐ Input data appears on data output in serial write cycle
- ☐ Dual (refresh/serial) operation
- ☐ Refresh cycle: 320 cycles/2 ms
- ☐ Power dissipation:
  -Active: 385 mW (max)
  -Standby: 82.5 mW (max)
- ☐ All inputs TTL-compatible
- ☐ Three-state HCMOS-compatible output
- ☐ Output data caused by negative $\overline{SC}$ transition is maintained up to next $\overline{SC}$ or $\overline{RAS}$ negative transition

Performance Ranges

Device	$\overline{SC}$ Cycle Time	Access Time from $\overline{SC}$	Serial Read Cycle Current	Serial Write Cycle Current
μPD41221-70	70 ns	55 ns	55 mA	55 mA
μPD41221-90	90 ns	75 ns	45 mA	45 mA

Pin Configuration

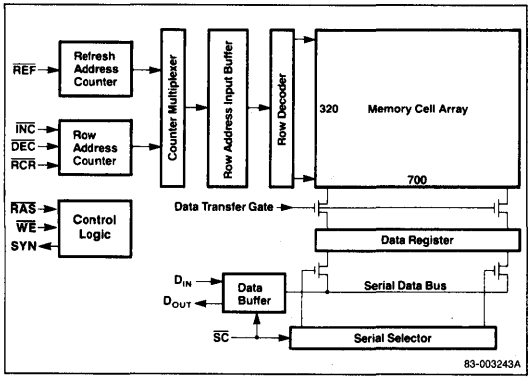


3

Pin Identification

No.	Symbol	Function
1	$\overline{INC}$	Row counter increment
2	$\overline{DEC}$	Row counter decrement
3	$\overline{RCR}$	Row counter reset
4	D_{OUT}	Data out
5, 13	NC	No connection
6	$\overline{SC}$	Serial control
7	GND	Ground
8	$\overline{RAS}$	Row address strobe
9	$\overline{WE}$	Write enable
10	D_{IN}	Data in
11	SYN	Sync acknowledge
12	$\overline{REF}$	Refresh control
14	V_{CC}	+5 V ± 10% power supply

Block Diagram



Absolute Maximum Ratings

Supply voltage on V_{CC} relative to GND, V_{CC}	−1.0 to +7.0 V
Supply voltage on inputs relative to GND, V_I	−1.0 to +7.0 V
Supply voltage on outputs relative to GND, V_O	−1.0 to +7.0 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{CC} = 5$ V, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance ($\overline{RAS}$, $\overline{REF}$, $\overline{SC}$, $\overline{WE}$, D_{IN}, $\overline{RCR}$, $\overline{INC}$, $\overline{DEC}$)	C_I			10	pF	GND = 0 V
Output capacitance (D_{OUT}, SYN)	C_O			10	pF	GND = 0 V

DC Characteristics

$T_A = -10$ to +55°C; $V_{CC} = 5.0$ V ± 10%; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Input voltage, high	V_{IH}	2.4		5.5	V	
Output voltage, low	V_{OL}	0		0.2 V_{CC}	V	$I_{OL} = 20\ \mu A$
Output voltage, high	V_{OH}	0.7 V_{CC}		V_{CC}	V	$I_{OH} = -20\ \mu A$
Input leakage current	I_I	−10		10	μA	$V_{IN} = 0$ V to 5.5 V; all other pins = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled, $V_{OUT} = 0$ V to 5.5 V
Standby current	I_{CC1}			15	mA	$I_O = 0$ mA (D_{OUT}, SYN); $\overline{RAS}$, $\overline{SC}$, $\overline{REF}$, $\overline{INC}$, $\overline{DEC}$, and $\overline{RCR} = V_{IH}$

Power Supply Current Characteristics

$T_A = -10$ to $+55°C$, $V_{CC} = 5.0\,V \pm 10\%$, GND = 0 V

Parameter	Symbol	Limits μPD41221-70 Min	Typ	Max	Limits μPD41221-90 Min	Typ	Max	Unit	Test Conditions
Data transfer cycle current	I_{CC2}			45			45	mA	$t_{RC} = t_{RC}$ min
Data restore cycle current	I_{CC3}			40			40	mA	$t_{RC} = t_{RC}$ min
$\overline{REF}$ refresh cycle current	I_{CC4}			40			40	mA	$t_{FC} = t_{FC}$ min
Serial read cycle current	I_{CC5}			55			45	mA	$t_{SC} = t_{SC}$ min
Serial write cycle current	I_{CC6}			55			45	mA	$t_{SC} = t_{SC}$ min
Row counter reset cycle current	I_{CC7}			20			20	mA	Minimum timing
Row counter increment cycle current	I_{CC8}			20			20	mA	Minimum timing
Row counter decrement cycle current	I_{CC9}			20			20	mA	Minimum timing

Note:
(1) An initial pause of 2 ms is required after power-up, followed by any eight cycles of $\overline{RAS}$ or $\overline{REF}$ before achieving proper device operation.

3

AC Characteristics

$T_A = -10$ to $+55°C$, $V_{CC} = 5.0\,V \pm 10\%$, GND = 0 V

Parameter	Symbol	Limits μPD41221-70 Min	Max	Limits μPD41221-90 Min	Max	Unit	Test Conditions
$\overline{RAS}$ cycle time	t_{RC}	710		710		ns	
$\overline{RAS}$ pulse width	t_{RAS}	500	2000	500	2000	ns	
$\overline{RAS}$ precharge time	t_{RP}	200		200		ns	
$\overline{RAS}$ to $\overline{REF}$ delay time	t_{RFD}	200		200		ns	
$\overline{RAS}$ to $\overline{SC}$ delay time	t_{RSD}	300		300		ns	
Read setup time before $\overline{RAS}$ low	t_{RRS}	0		0		ns	
Read hold time after $\overline{RAS}$ high	t_{RRH}	20		20		ns	
$\overline{REF}$ precharge time before $\overline{RAS}$ low	t_{FRP}	200		200		ns	
$\overline{SC}$ precharge time before $\overline{RAS}$ low	t_{SRP}	200		200		ns	
$\overline{WE}$ setup time before $\overline{RAS}$ low	t_{WRS}	0		0		ns	
$\overline{WE}$ hold time after $\overline{RAS}$ low	t_{WRH}	50		50		ns	
Output disable time from $\overline{RAS}$ low	t_{RSZ}	0	400	0	400	ns	(Note 1)
$\overline{REF}$ cycle time	t_{FC}	710		710		ns	
$\overline{REF}$ pulse width	t_{REF}	500		500		ns	
$\overline{REF}$ precharge time	t_{FP}	200		200		ns	
$\overline{SC}$ cycle time	t_{SC}	70		90		ns	
$\overline{SC}$ pulse width	t_{SA}	25	2000	35	2000	ns	
$\overline{SC}$ precharge time	t_{SP}	25	2000	35	2000	ns	
$\overline{WE}$ setup time before $\overline{SC}$ low	t_{WSS}	0		0		ns	
$\overline{WE}$ hold time after $\overline{SC}$ low	t_{WSH}	25		35		ns	
Read setup time before $\overline{SC}$ low	t_{RSS}	0		0		ns	
Read hold time after $\overline{SC}$ high	t_{RSH}	20		30		ns	
Data input setup time before $\overline{SC}$ low	t_{DSS}	0		0		ns	
Data input hold time after $\overline{SC}$ low	t_{DSH}	25		35		ns	
Access time from $\overline{SC}$	t_{SAC}		55		75	ns	

AC Characteristics (cont)

$T_A = -10$ to $+55°C$, $V_{CC} = 5.0\,V \pm 10\%$, GND = 0 V

Parameter	Symbol	Limits μPD41221-70 Min	Limits μPD41221-70 Max	Limits μPD41221-90 Min	Limits μPD41221-90 Max	Unit	Test Conditions
Output disable time from $\overline{SC}$ low	t_{SCZ}	5	40	5	60	ns	(Note 1)
$\overline{RAS}$ to $\overline{RCR}$ delay time	t_{RRD}	200		200		ns	
$\overline{RAS}$ to $\overline{INC}$ delay time	t_{RID}	200		200		ns	
$\overline{RAS}$ to $\overline{DEC}$ delay time	t_{RDD}	200		200		ns	
$\overline{RCR}$ pulse width	t_{RCR}	100	2000	100	2000	ns	
$\overline{INC}$ pulse width	t_{INC}	100	2000	100	2000	ns	
$\overline{DEC}$ pulse width	t_{DEC}	100	2000	100	2000	ns	
Time between $\overline{RCR}$ and $\overline{INC}$	t_{RIP}	100		100		ns	
Time between $\overline{INC}$ and $\overline{DEC}$	t_{IDP}	100		100		ns	
Time between $\overline{RCR}$ and $\overline{DEC}$	t_{RDP}	100		100		ns	
$\overline{RCR}$ precharge time before $\overline{RAS}$ low	t_{RRP}	100		100		ns	
$\overline{INC}$ precharge time before $\overline{RAS}$ low	t_{IRP}	100		100		ns	
$\overline{DEC}$ precharge time before $\overline{RAS}$ low	t_{DRP}	100		100		ns	
SYN response time after 608th $\overline{SC}$	t_{SYA}		200		200	ns	
SYN recovery time after $\overline{RAS}$ low	t_{SYR}	0	1400	0	1400	ns	
Refresh interval	t_{REF}		2		2	ms	
$\overline{RAS}$ precharge (serial operation)	t_{RPS}		2		2	ms	
Serial data output valid	t_{SOV}		2		2	ms	
Transition time	t_T	3	35	3	35	ns	

Note:

(1) t_{SCZ} and t_{RSZ} define the times at which the output achieves the open-circuit condition and are not referenced to output voltage levels. The duration of the output voltage level depends on the time constant of the load. See input and output timing waveforms and figures 1 and 2.

(2) Timing measurements assume $t_T = 5$ ns.

(3) V_{IH} (min) and V_{IL} (max) are the reference levels for measuring the timing of input signals and t_T.

Figure 1. Loading Conditions Test Circuit for SYN

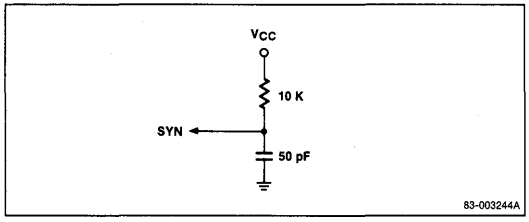
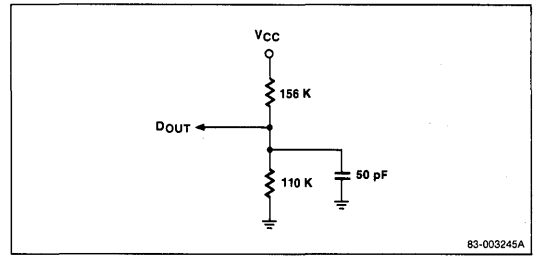
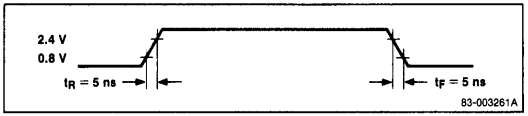


Figure 2. Loading Conditions Test Circuit for D_{OUT}

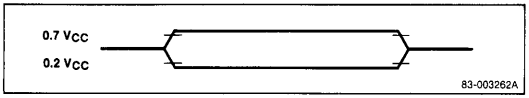


Timing Waveforms

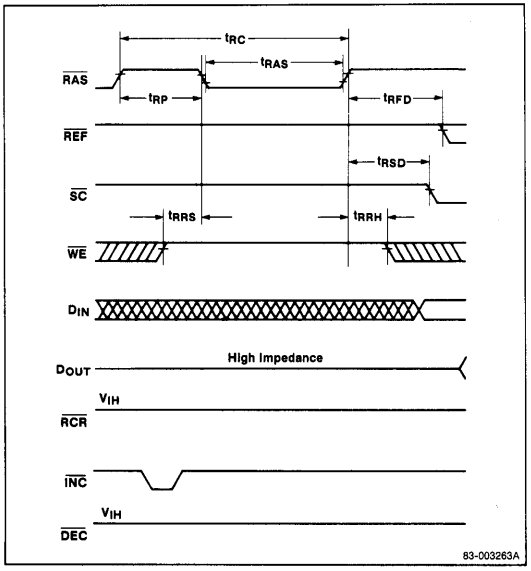
Input Timing



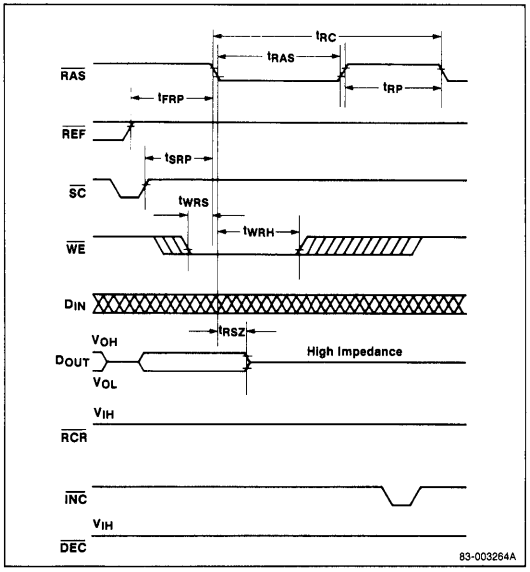
Output Timing



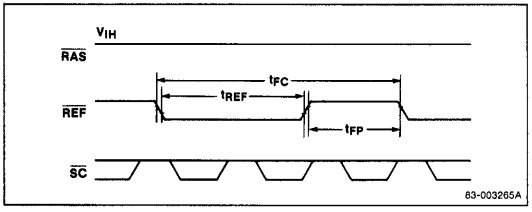
Data Transfer Cycle



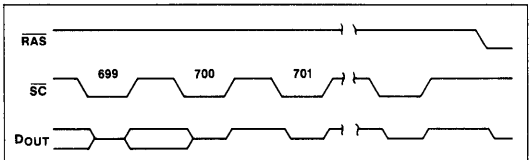
Data Restore Cycle



REF Refresh Cycle



Serial Read Data Output Control



Note:

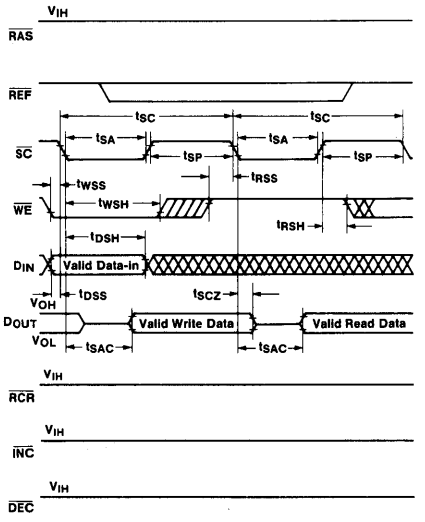
[1] SC count starts from location 0.

[2] V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

83-003269A

Timing Waveforms (cont)

Serial Read and Write Cycles



Note:

[1] V_{IH} [min] and V_{IL} [max] are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

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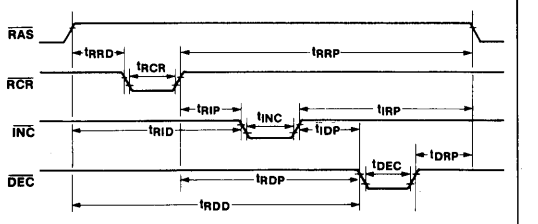
Row Counter Cycle

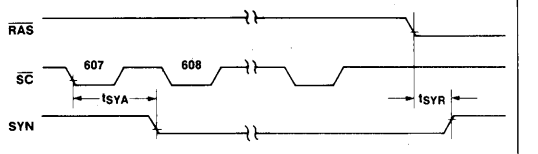


Note:

[1] V_{IH} [min] and V_{IL} [max] are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

83-003267A

Sync Acknowledge



Note:

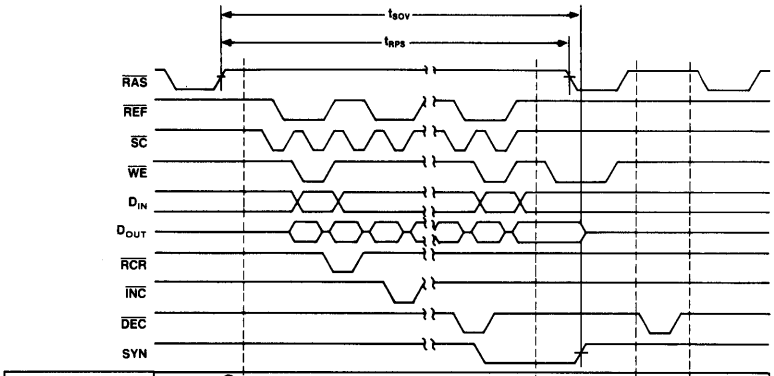
[1] SC count starts from location 0.

[2] V_{IH} [min] and V_{IL} [max] are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

83-003268A

Timing Waveforms (cont)

Total Timing Scheme



Data Transfer	O																		O
Data Restore														O					
REF Refresh								O								O			
Serial Write								O											
Serial Read								O											
Row Counter Reset								O						O		O			
Row Counter Increment								O						O		O			
Row Counter Decrement								O						O		O			

Note:

[1] In this table a "O" indicates that the operation is available using the timing shown above.

83-003270B

3

μPD41264
262,144-BIT DUAL PORT DYNAMIC NMOS RAM

Revision 2

Description

The NEC μPD41264 is a 262-144-bit Dual Port Memory equipped with a 64K × 4 dynamic RAM port and a 256 × 4 serial read port. The RAM port looks exactly like the NEC standard 64K × 4 dynamic RAM, μPD41464. The serial read port is connected to an internal 1024-bit data register through a 256 × 4 serial read output control and makes the memory look as if it were organized as 256 words of 1024 bits, each of which is read out serially 4 bits at a time.

The μPD41264 features full asynchronous dual access capability except when transferring memory cell data from a selected word line of the RAM array to the data register. To perform the data transfer, a special timing cycle using a transfer clock is necessary for the RAM port. On the other hand, the serial read port can operate without any change even during the data transfer period. Following the data transfer clock transition, the serial read output changes from an old line to a new line. The serial read start location on the new line is addressable in the data transfer cycle.

The RAM has a write-per-bit capability in addition to the conventional operation modes. Out of 4 data bits, individually selected bits can be written.

The μPD41264 utilizes a double poly layer, N-channel, silicon gate process which provides high storage cell density, high performance, and high reliability.

Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles or normal read or write cycles on the 256 address combination of A_0 through A_7 during a 4ms period. An automatic internal refresh is also available, using hidden refresh or $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry. Note that the transfer of a row of data from the memory array to the data register also refreshes that row.

All inputs and outputs, including clocks, are TTL-compatible. All address lines and data-in are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The μPD41264 is packaged in a 24-pin, dual-in-line, plastic package and is guaranteed for operation from 0°C to +70°C. Packages are designed for insertion in mounting-hole rows on 400-mil (10.16mm) centers.

Features

- ☐ Combination of three key functional blocks
  1. 64K × 4 dynamic RAM
  2. 1024-bit data register
  3. 256 × 4 serial read output control
- ☐ Two data ports: one random access port, one serial read port
- ☐ Data transfer from RAM to data register
- ☐ Fast serial read output from data register: up to 40ns
- ☐ Dual port accessibility except data transfer
- ☐ Address start of serial read follows data transfer

Features (cont)

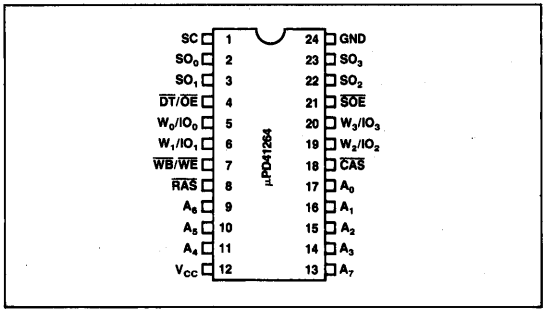
- ☐ Possible data transfer also in parallel with serial read
  - Real time data transfer
- ☐ Single +5V ± 10% power supply
- ☐ On-chip substrate bias generated
- ☐ RAM port based on 64K x 4 specifications
  - 2 main clocks: $\overline{RAS}$, $\overline{CAS}$, multiplexed address inputs
  - Common data input and output using 3-state output
  - $\overline{OE}$ allows direct connection of IO and address lines to simplify system design
  - Refresh: 256 cycles/4ms
  - Read, early write, late write, read-write/read-modify write, $\overline{RAS}$-only refresh, and page mode capability
  - $\overline{CAS}$ before $\overline{RAS}$: automatic internal refresh using on-chip refresh address counter
  - $\overline{CAS}$-controlled output allows hidden refresh
  - Write-per-bit capability regarding 4 IO bits -Write bit select multiplexed on IO_0-IO_3
- ☐ Activation with $\overline{RAS}$ causes data transfer
  - Same $\overline{RAS}$ cycle time as RAM operation
  - Row address inputs specify a word line transferred to data register
  - Column address inputs specify start location of following serial read
  - $\overline{DT}$ low-to-high transition transfers 1024 bits of data on the word line to the data register, and the start location to serial read control
  - Serial port can either operate during real time data transfer or be in a standby state
- ☐ SC performs fast serial read operation of 256 x 4 organization
  - $\overline{SOE}$ presents serial data on SO_0 – SO_3
  - $\overline{SOE}$ allows direct connection of multiple serial outputs for extension of data length
- ☐ Speed and power performance

		μPD41264-12		μPD41264-15	
RAM Port					
Access Time	t_{RAC}	120ns	max	150ns	max
	t_{CAC}	60ns	max	75ns	max
	t_{OEA}	30ns	max	40ns	max
Cycle Time	t_{RC}	220ns	min	270ns	min
Serial Port					
Access Time		40ns	max	60ns	max
Cycle Time		40ns	min	60ns	min
Dissipation Power					
Both Ports Operating		853mW	max	715mW	max
Both Ports Standby		66mW	max	66mW	max

- ☐ All inputs, outputs, and clocks fully TTL-compatible
- ☐ 3-state outputs for both random and serial access
- ☐ Double poly layer, N-channel, silicon gate technology
- ☐ 24-pin plastic DIP with 400 mil width

3

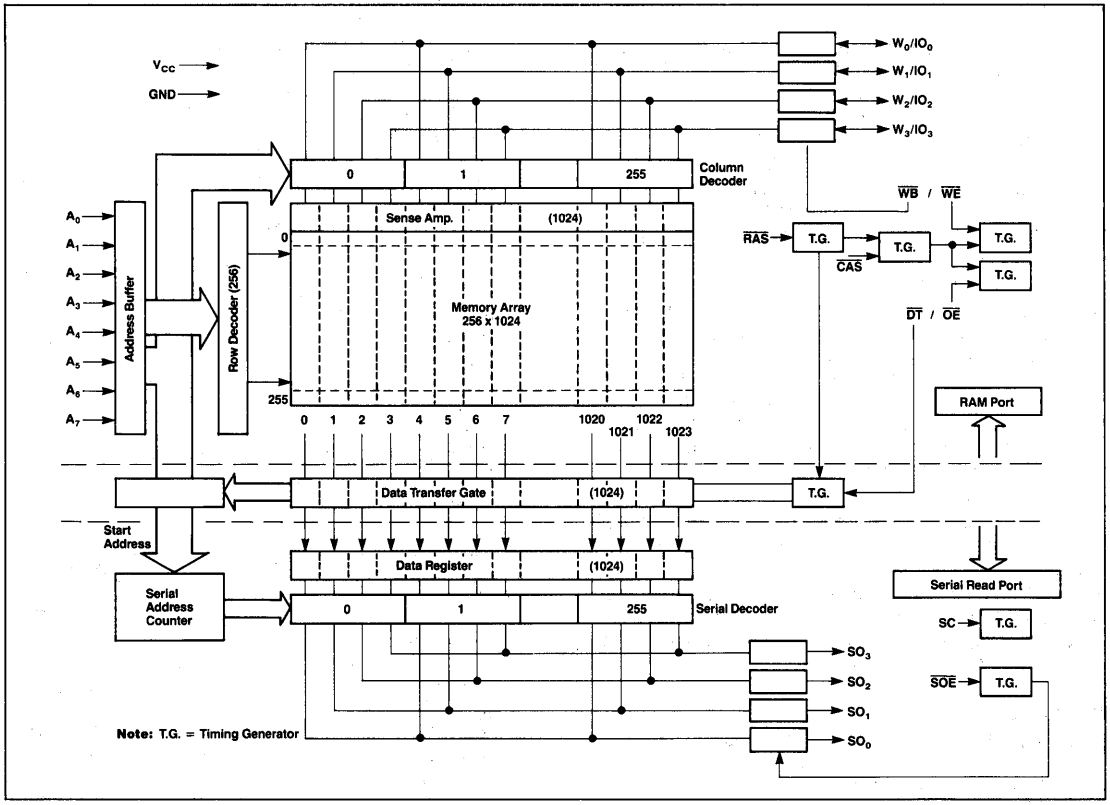
Pin Configuration



Pin Identification

Pin No.	Symbol	I/O	Description
1	SC	Input	Serial Control
2, 3, 22, 23	SO_0–SO_3	Output	Serial Read Outputs
4	$\overline{DT}/\overline{OE}$	Input	Data Transfer/Output Enable
5, 6, 19, 20	W_0–W_3	Input	Write Select in Write-per-Bit
	IO_0–IO_3	Input/Output	Data Inputs and Outputs
7	$\overline{WB}/\overline{WE}$	Input	Write-per-Bit/Write Enable
8	$\overline{RAS}$	Input	Row Address Strobe
9–11, 13–17	A_0–A_7	Input	Address Inputs
12	V_{CC}		+5V Power Supply
18	$\overline{CAS}$	Input	Column Address Strobe
21	$\overline{SOE}$	Input	Serial Output Enable
24	GND		Ground

Block Diagram



Device Operation

Overall description

As already shown the μPD41264 consists of the RAM port and the serial read port. The RAM port performs both standard dynamic RAM operation modes and the data transfer operation. All these operations are based on the conventional $\overline{RAS}/\overline{CAS}$ timing cycle. In the data transfer cycle the data in each memory cell on the selected word line is transferred to the corresponding data register through a data transfer gate at the same time. The serial read port shows the data of the data register in serial order. The RAM port and the serial read port can operate asynchronously, except during the data transfer period because the data transfer gate is turned on.

Addressing

The 262,144-bit memory array is arranged in a 256-row by 1024-column matrix. Each of 4 data bits in the RAM port corresponds to 65,536 memory cells. Therefore, 16 address bits are required to decode 1 memory cell location. Eight row address bits are set up on pins A_0 through A_7 and latched onto the chip by $\overline{RAS}$. Then the 8 column address bits are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable. When $\overline{RAS}$ is activated, 1024 cells on the selected word line are sensed simultaneously. The sense amplifier automatically restores the data. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers. Through 1 of 256 column decoders, 4 memory cells on the word line are connected to 4 data buses, respectively.

In the data transfer cycle 8 row address bits are used to select 1 of the 256 possible rows involved in the transfer of data to the data registers. Eight column address bits are assigned to select the 1 out of 256 serial decoders that corresponds to the start location of the following serial read cycle.

In the serial read port, when SC is activated, 4 data bits in the 1024 data registers are transferred to 4 serial data buses, respectively, and read out. By activating SC repeatedly, the serial read operation starting from the location specified in the data transfer cycle is performed within the 1024 bits in the data register.

RAM port operation

An operation in the RAM port begins with a negative transition of $\overline{RAS}$. $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths as specified in the timing table. These minimum pulse widths must be maintained for proper device operation and data integrity. A cycle once begun must be within specifications. The following functions are multiplexed pins in the RAM port to reduce the number of pins.

1. $\overline{DT}/\overline{OE}$
2. $\overline{WB}/\overline{WE}$
3. W_i/IO_i (i = 0, 1, 2, 3)

$\overline{OE}$, $\overline{WE}$ and IO_i are all based on the same functional concepts as in conventional RAMs. $\overline{DT}$, $\overline{WB}$ and W_i are all inputs to be applied with set-up and hold times referenced

RAM port operation (cont)

to the $\overline{RAS}$ negative transition in the same way as row address inputs. The $\overline{DT}$ level determines whether a cycle is a RAM operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i specifies data bits to be written in the write cycles with the write-per-bit capability. In the following explanation these multiplexed pins are described as, for example, $\overline{DT}(/\overline{OE})$, depending on the function then being used.

To use the μPD41264 in the random access mode, $\overline{DT}$ $(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}$ $(/\overline{OE})$ high disconnects the 1024-bit data register from the corresponding 1024 digit lines of the memory array. On the other hand, to perform the data transfer cycle, $\overline{DT}$ $(/\overline{OE})$ must be low as $\overline{RAS}$ falls. The 1024 data transfer gates are opened and a data transfer will occur from one of the memory rows to the data register.

Read Cycle. A read cycle is performed by activating a $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and maintaining $(\overline{WB}/)\overline{WE}$ high during the $\overline{CAS}$ active time. The data pin $(W_i/)$ IO_i (i = 0, 1, 2, 3) remains in a high-impedance state until valid data appears at the output at access time. Device access time, t_{ACC}, is the longest of the following three calculated intervals:

1. $t_{ACC} = t_{RAC}$
2. t_{ACC} = $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
3. t_{ACC} = $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access time from $\overline{RAS}$, t_{RAC}, access time from $\overline{CAS}$, t_{CAC}, and access time from $\overline{OE}$, t_{OEA}, are device parameters. $\overline{RAS}$ to $\overline{CAS}$ delay and $\overline{RAS}$ to $\overline{OE}$ delay are system-dependent timing parameters.

The output becomes valid after the access time has elapsed and remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state.

Write Cycle. A write cycle is performed by bringing $(\overline{WB}/)\overline{WE}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $(\overline{WB}/)\overline{WE}$ strobes data on $(W_i/)IO_i$ into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}(/\overline{WE})$ must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping $W_i(/IO_i)$ high with set-up and hold times referenced to the $\overline{RAS}$ negative transition.

For those data bits of $W_i(/IO_i)$ that are kept low as $\overline{RAS}$ falls, the write operation is inhibited on the chip. If $\overline{WB}(/\overline{WE})$ is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Early Write Cycle. An early write cycle is performed by bringing $(\overline{WB}/)\overline{WE}$ low before $\overline{CAS}$. The data is strobed in by $\overline{CAS}$ with set-up and hold times referenced to this signal. The output remains in the high-impedance state for the entire cycle. $(\overline{DT}/)\overline{OE}$ must meet $\overline{DT}$ high set-up and hold times as $\overline{RAS}$ falls but otherwise does not affect any circuit operation during the $\overline{CAS}$ active period.

3

Read-Write/Read-Modify-Write [RW/RMW] Cycle. An RW/RMW cycle is performed by bringing (WB/)WE low with RAS and CAS low. (W_I/)IO_I shows read data at access time. After that, with preparation for the coming write operation, (W_I/)IO_I is returned to the high-impedance state by (DT/)OE going high. The data to be written is strobed in by (WB/)WE with set-up and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of (DT/)OE which can be activated just after (WB/)WE falls, even when (WB/)WE is brought low after CAS.

Refresh Cycle. A cycle at each of the 256 row addresses (A_0 through A_7) will refresh all storage cells. Any operation cycle performed in the RAM port (i.e., read, write, refresh, or data transfer) refreshes the 1024 bits selected by the RAS addresses or an on-chip refresh address counter.

RAS-only Refresh. A cycle with RAS-only active refreshes the memory. CAS is maintained high during the RAS active period to keep (W_I/)IO_I in the high-impedance state. This is the recommended refresh mode, especially when the memory system consists of multiple rows of memory devices. The data outputs may be OR-tied with no bus contention when RAS-only refresh cycles are performed.

CAS before RAS Refresh. The μPD41264 has an internal refresh function. When CAS is low as RAS falls, the on-chip control circuitry works so that the refresh operation is performed for row addresses specified by the refresh address counter. In this cycle the circuit operation based on CAS is maintained in a reset state. When the internal refresh operation is completed, an increment in the refresh address counter is automatically performed with preparation for the next CAS before RAS cycle.

Hidden Refresh. A hidden refresh accomplishes a refresh cycle following a read cycle without disturbing the read data output. Once valid, the data output is controlled by CAS and OE. After the read cycle, CAS is held low while RAS goes high for precharge. A RAS-only cycle is then performed and the data output remains valid. The refresh operation itself is just the same as the CAS before RAS refresh. Therefore, the internal refresh operation is repeated with the valid data output.

Page Mode Cycle. Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. This is done by maintaining RAS low while successive CAS cycles are performed. Page mode operation allows a faster data transfer rate as RAS addresses are maintained internally and do not have to be reapplied. During this operation, read, write and RW/RMW cycles are possible. Note that the write-per-bit control specified in the entry write cycle is maintained through the following page write cycle.

Data Transfer Cycle. A data transfer cycle is performed by bringing DT (/OE) low as RAS falls. As described previously, 1 of the 256 rows involved in the data transfer and the start location of the following serial read cycle in the serial read port are specified by address inputs. DT (/OE) must be low for a specified time from RAS and CAS so that the data transfer condition may be satisfied. The DT low-to-high transition causes two transfer operations through the data transfer gates: column address buffer outputs to serial address counters and memory cell data amplified on digit lines to the data register. RAS and CAS must be low during these data transfer operations to keep the transferred data in the RAM port.

Serial read port operation

The serial read port operation is used only to read out serially the data in the data registers starting from a specified location. The entire operation therefore follows the data transfer cycle. Data stored in the serial register will remain valid for a minimum of 4 ms after the data transfer cycle. The only condition under which the serial read port must synchronize with the RAM port is when the DT(/OE) positive transition must occur within a specified period in an SC cycle. Except for this SC cycle, the serial read port can operate asynchronously with the RAM port. The data output will appear at SO_I after an access time of t_{SCA} from SC high only when SOE is maintained low. The SC cycle which includes the DT(/OE) positive transition shows old data in the data register; the following SC cycles show new data transferred to the data register serially and in a looped manner. The serial data output is maintained until the next SC is activated. SOE controls the impedance of the serial output allowing multiplexing of more than one bank of μPD41264 memories into the same external circuitry. When SOE is at a low-logic level, SO_I will be enabled and the proper data read out. When SOE is at a high-logic level, SO_I will be disabled and be in the high-impedance state.

Absolute Maximum Ratings*

Supply Voltage on Any Pin Except V_{CC} Relative to GND, V_{R1}	−1.0V to +7.0V
Supply Voltage on V_{CC} Relative to GND, V_{R2}	−1.0V to +7.0V
Operating Temperature, T_{OPR}	0°C to +70°C
Storage Temperature, T_{STG}	−55°C to +125°C
Short-circuit Output Current, I_{OS}	50mA
Power Dissipation, P_D	1.5W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0°C to +70°C

Recommended Operating Conditions

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Supply Voltage	GND		0		V	
High-level Input Voltage	V_{IH}	2.4		5.5	V	
Low-level Input Voltage	V_{IL}	−1.0		0.8	V	

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Input/Output Electrical Characteristics

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{IL}	−10		10	μA	V_{IN} = 0V to 5.5V; all other pins not under test = 0V
Output Leakage Current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) is disabled; V_{OUT} = 0V to 5.5V
RAM Port High-level Output Voltage	$V_{OH(R)}$	2.4		V_{CC}	V	$I_{OH(R)}$ = −2mA
RAM Port Low-level Output Voltage	$V_{OL(R)}$	0		0.4	V	$I_{OL(R)}$ = 4.2mA
Serial Read Port High-level Output Voltage	$V_{OH(S)}$	2.4		V_{CC}	V	$I_{OH(S)}$ = −2mA
Serial Read Port Low-level Output Voltage	$V_{OL(S)}$	0		0.4	V	$I_{OL(S)}$ = 4.2mA

Operation modes which define power supply currents for each port are described in the following table.

Power Supply Current

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Port	Symbol	Operating Conditions
RAM	RW	Read or write cycle, $\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC}(min)
RAM	STB	Standby, $\overline{RAS}$ = V_{IH}, D_{OUT} = high impedance
RAM	ROR	$\overline{RAS}$-only refresh, $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} (min)
RAM	PAGE	Page mode operation, $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = t_{PC} (min)
RAM	CBR	$\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ low as $\overline{RAS}$ falls, t_{RC} = t_{RC} (min)
RAM	DTR	Data transfer cycle, $\overline{DT}$ low as $\overline{RAS}$ falls, t_{RC} = t_{RC} (min)
Serial Read	STB	Standby, SC = $\overline{SOE}$ = V_{IH}
Serial Read	ACT	Serial read cycle, $\overline{SOE}$ = V_{IL}, SC cycling, t_{SCC} = t_{SCC} (min)

T_A = 0°C to +70°C; V_{CC} = 5.0V ±10%; GND = 0V

Port			Limits μPD41264-12			μPD41264-15				Test
RAM	Serial Read	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Conditions
RW	STB	I_{CC1}			95			85	mA	①
STB	STB	I_{CC2}			12			12	mA	①
ROR	STB	I_{CC3}			75			65	mA	①
PAGE	STB	I_{CC4}			65			55	mA	①
CBR	STB	I_{CC5}			75			65	mA	①
DTR	STB	I_{CC6}			120			100	mA	①
RW	ACT	I_{CC7}			155			130	mA	①
STB	ACT	I_{CC8}			60			45	mA	①
ROR	ACT	I_{CC9}			135			110	mA	①
PAGE	ACT	I_{CC10}			125			100	mA	①
CBR	ACT	I_{CC11}			135			110	mA	①
DTR	ACT	I_{CC12}			180			145	mA	①

Note: ① No load on IO_i and SO_i. Except for I_{CC2}, real values depend on output loading and cycle rates.

Capacitance

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 10%; GND = 0V; f = 1MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance, Address Inputs (A_0 to A_7)	$C_{I(A)}$			5	pF	
Input Capacitance, Data Transfer/Output Enable	$C_{I(DT/OE)}$			6	pF	
Input/Output Capacitance, Write Select/RAM Data IO	$C_{IO(W/IO)}$			7	pF	
Input Capacitance, Write-per-Bit/Write Enable	$C_{I(WB/WE)}$			8	pF	
Input Capacitance, Row Address Strobe	$C_{I(RAS)}$			8	pF	
Input Capacitance, Column Address Strobe	$C_{I(CAS)}$			8	pF	
Input Capacitance, Serial Output Enable	$C_{I(SOE)}$			6	pF	
Output Capacitance, Serial Read Output	$C_{O(SO)}$			7	pF	
Input Capacitance, Serial Control	$C_{I(SC)}$			8	pF	

AC Input/Output Timing Waveforms

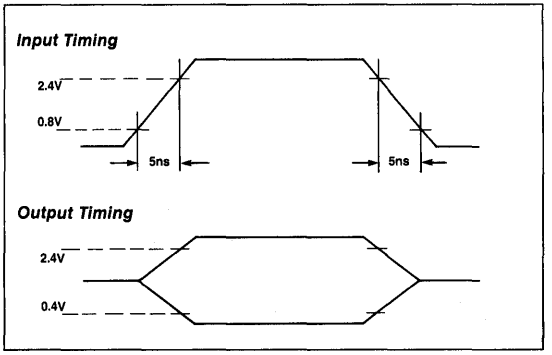


Figure 1. Output Loading, RAM Port

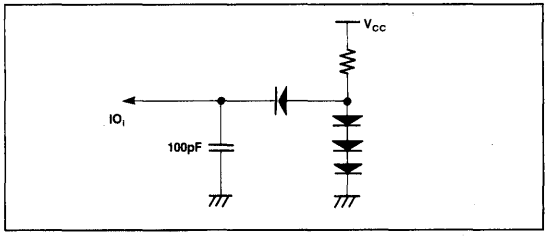
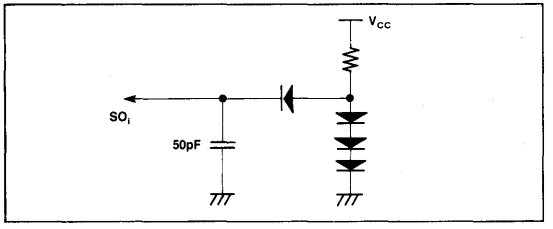


Figure 2. Output Loading, Serial Read Port



AC Characteristics ①②

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Switching Characteristics ③

No. ④	Parameter	Symbol	Limits 41264-12 Min	41264-12 Max	41264-15 Min	41264-15 Max	Unit	Test Conditions
4	Access Time from $\overline{RAS}$	t_{RAC}		120		150	ns	⑤
5	Access Time from $\overline{CAS}$	t_{CAC}		60		75	ns	⑥
36	Access Time from $\overline{OE}$	t_{OEA}		30		40	ns	
57	Serial Output Access Time from SC	t_{SCA}		40		60	ns	⑧
55	Serial Output Access Time from $\overline{SOE}$	t_{SOA}		35		50	ns	⑧
6	Output Disable Time from $\overline{CAS}$ High	t_{OFF}	0	30	0	40	ns	⑦
39	Output Disable Time from $\overline{OE}$ High	t_{OEZ}	0	30	0	40	ns	⑦
50	Serial Output Disable Time from $\overline{SOE}$ High	t_{SOZ}	0	30	0	40	ns	⑦

Notes:
① See AC input/output timing waveforms.
② See Figures 1 and 2.
③ An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
④ No. equals a number attached to each parameter in the timing waveforms.
⑤ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value given in the table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
⑥ Assumes that $t_{RCD} \geq t_{RCD}$ (max).
⑦ An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.
⑧ Data in the serial output register remains valid for 4 ms (min) after a data transfer cycle.

AC Characteristics (Cont.) ①②

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Timing Requirements ③

No. ④	Parameter	Symbol	Limits 41264-12 Min	41264-12 Max	41264-15 Min	41264-15 Max	Unit	Test Conditions
1	Random Read or Write Cycle Time	t_{RC}	220		270		ns	
2	Read-Write/Read-Modify-Write Cycle	t_{RWC}	300		355		ns	
3	Page Mode Cycle Time	t_{PC}	120		145		ns	
7	Transition Time (rise and fall)	t_T	3	50	3	50	ns	
8	$\overline{RAS}$ Precharge Time	t_{RP}	90		100		ns	
9	$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	ns	
10	$\overline{RAS}$ Hold Time	t_{RSH}	60		75		ns	
11	$\overline{CAS}$ Precharge Time (non-page mode)	t_{CPN}	25		30		ns	
12	$\overline{CAS}$ Precharge Time (page mode only)	t_{CP}	50		60		ns	
13	$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	ns	
14	$\overline{CAS}$ Hold Time	t_{CSH}	120		150		ns	
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	30	75	ns	⑤
16	$\overline{CAS}$ High to $\overline{RAS}$ Low Precharge Time	t_{CRP}	10		10		ns	
17	Row Address Set-up Time	t_{ASR}	0		0		ns	
18	Row Address Hold Time	t_{RAH}	15		20		ns	
19	Column Address Set-up Time	t_{ASC}	0		0		ns	
20	Column Address Hold Time	t_{CAH}	20		25		ns	
21	Column Address Hold Time after $\overline{RAS}$ Low	t_{AR}	80		100		ns	
22	Read Command Set-up Time	t_{RCS}	0		0		ns	
23	Read Command Hold Time after $\overline{RAS}$ High	t_{RRH}	20		20		ns	⑥

AC Characteristics (Cont.) ①②

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Timing Requirements ③

No. ④	Parameter	Symbol	Limits 41264-12 Min	41264-12 Max	41264-15 Min	41264-15 Max	Unit	Test Conditions
24	Read Command Hold Time after CAS High	t_{RCH}	0		0		ns	⑥
25	Write Command Set-up Time	t_{WCS}	0		0		ns	⑦
26	Write Command Hold Time	t_{WCH}	35		45		ns	
27	Write Command Hold Time after $\overline{RAS}$ Low	t_{WCR}	95		120		ns	
28	Write Command Pulse Width	t_{WP}	35		45		ns	
29	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40		45		ns	
30	Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40		45		ns	
31	Data in Set-up Time	t_{DS}	0		0		ns	⑧
32	Data in Hold Time	t_{DH}	35		45		ns	⑧
33	Data in Hold Time after $\overline{RAS}$ Low	t_{DHR}	95		120		ns	
34	$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	100		120		ns	⑦
35	$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	160		195		ns	⑦
37	$\overline{OE}$ High to Data in Set-up Delay	t_{OED}	35		40		ns	
38	$\overline{OE}$ High Hold Time after $\overline{WE}$ Low	t_{OEH}	30		40		ns	
40	$\overline{CAS}$ before $\overline{RAS}$ Refresh Set-up Time	t_{CSR}	10		10		ns	
41	$\overline{CAS}$ before $\overline{RAS}$ Refresh Hold Time	t_{CHR}	25		30		ns	
42	$\overline{RAS}$ High to $\overline{CAS}$ Low Precharge Time	t_{RPC}	0		0		ns	
43	Refresh Time Interval	t_{REF}		4		4	ms	
44	$\overline{DT}$ Low Set-up Time	t_{DLS}	0		0		ns	
45	$\overline{DT}$ Low Hold Time after $\overline{RAS}$ Low	t_{RDH}	100		130		ns	
46	$\overline{DT}$ Low Hold Time after $\overline{CAS}$ Low	t_{CDH}	40		55		ns	
47	SC High to $\overline{DT}$ High Delay	t_{SDD}	10		20		ns	
48	SC Low Hold Time after $\overline{DT}$ High	t_{SDH}	10		20		ns	
49	$\overline{OE}$ Pulse Width	t_{OE}	35		40		ns	
51	Serial Clock Cycle Time	t_{SCC}	40	50000	60	50000	ns	
52	SC Pulse Width	t_{SCH}	10		20		ns	
53	SC Precharge Time	t_{SCL}	10		20		ns	
54	$\overline{SOE}$ Low to Serial Output Set-up Delay	t_{SOO}	5		5		ns	
56	Serial Output Hold Time after SC High	t_{SOH}	10		10		ns	
58	$\overline{DT}$ High Set-up Time	t_{DHS}	0		0		ns	
59	$\overline{DT}$ High Hold Time	t_{DHH}	20		25		ns	
60	$\overline{DT}$ High to $\overline{RAS}$ High Delay	t_{DTR}	10		10		ns	
61	$\overline{DT}$ High to $\overline{CAS}$ High Delay	t_{DTC}	10		10		ns	
62	$\overline{OE}$ to $\overline{RAS}$ Inactive Set-up Time	t_{OES}	10		10		ns	
64	Write-per-Bit Set-up Time	t_{WBS}	0		0		ns	
65	Write-per-Bit Hold Time	t_{WBH}	20		25		ns	
66	Write Bit Selection Set-up Time	t_{WS}	0		0		ns	

AC Characteristics (Cont.) ①②

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 10%; GND = 0V

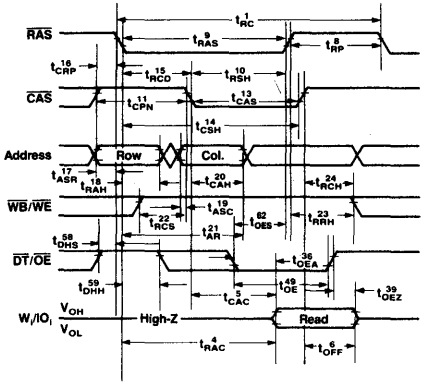
Timing Requirements ③

No. ④	Parameter	Symbol	Limits 41264-12 Min	41264-12 Max	41264-15 Min	41264-15 Max	Unit	Test Conditions
67	Write Bit Selection Hold Time	t_{WH}	20		25		ns	
68	$\overline{SOE}$ Pulse Width	t_{SOE}	15		20		ns	
69	$\overline{SOE}$ Precharge Time	t_{SOP}	15		20		ns	
70	$\overline{DT}$ High Hold Time After $\overline{RAS}$ High	t_{DTH}	20		25		ns	

Notes:
① See input/output timing waveforms.
② See Figures 1 and 2.
③ V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.
④ No. equals a number attached to each parameter in the timing waveforms.
⑤ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
⑥ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
⑦ t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until CAS goes back to V_{IH}) is indeterminate.
⑧ These parameters are referenced to CAS leading edge in early write cycles and to (WB/) WE leading edge in delayed write or read-modify-write cycles.

Timing Waveforms

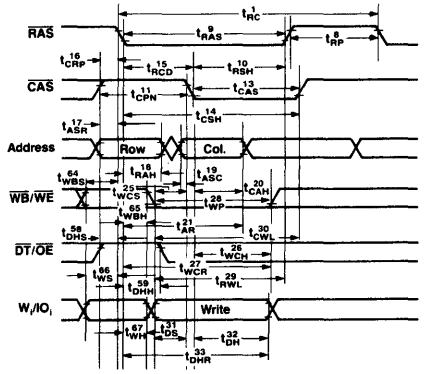
Read Cycle



Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

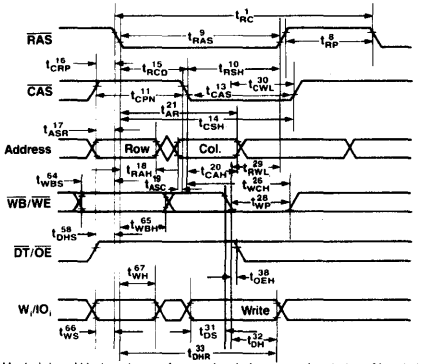
Timing Waveforms (cont)

Early Write Cycle



Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

Late Write Cycle



Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

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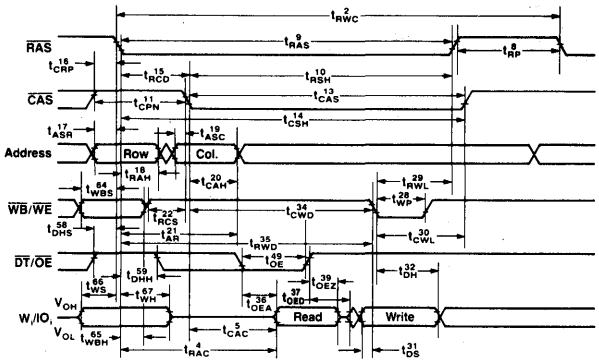
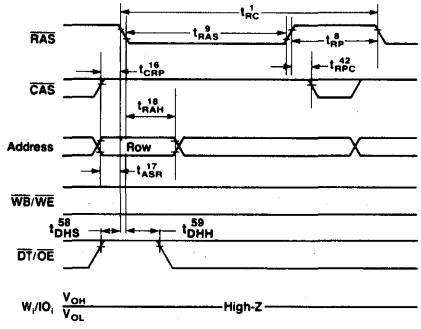
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycles



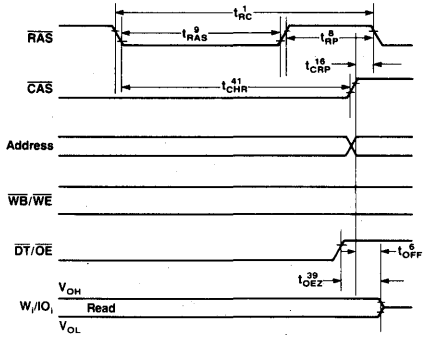
Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

RAS-only Refresh



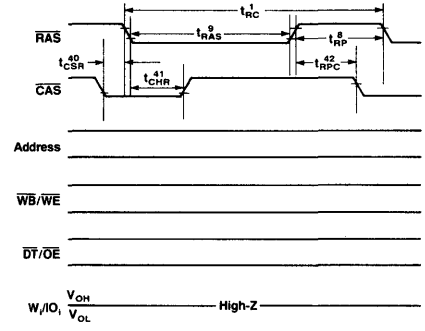
Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

Hidden Refresh



Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

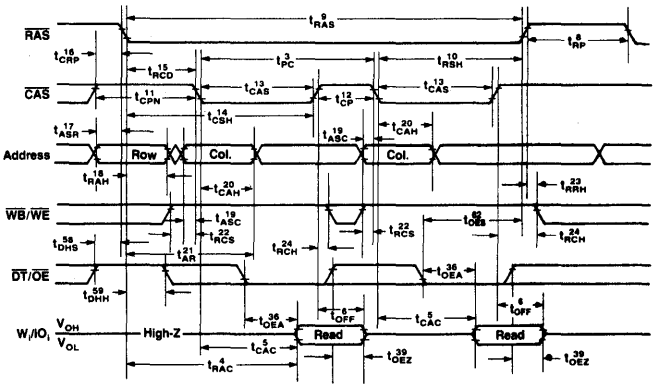
CAS before RAS Refresh



Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

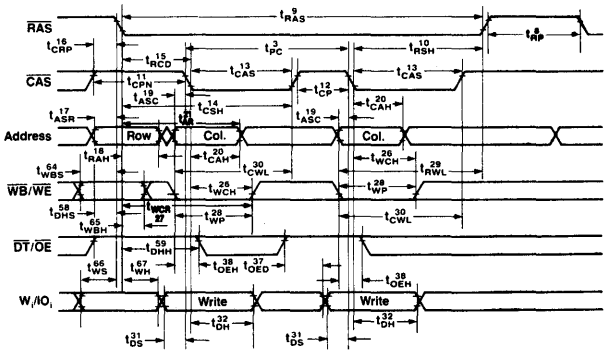
Timing Waveforms (cont)

Page Mode Read Cycle



Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

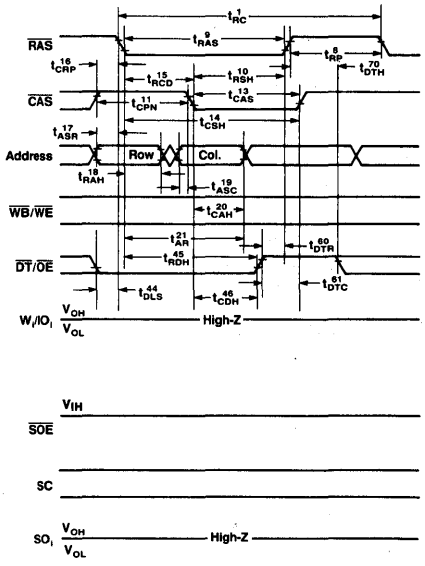
Page Mode Write Cycle



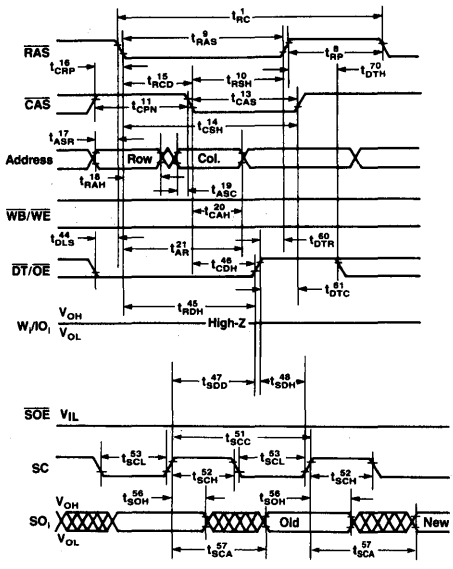
Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

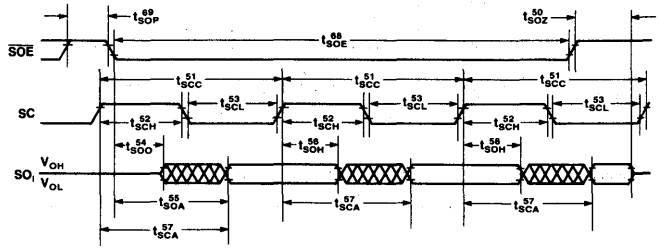
Timing Waveforms (cont)

Data Transfer Cycle (Port B Standby)



Data Transfer Cycle (Port B Active)





Note: V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

NEC Electronics Inc.

APPLICATION NOTE 32
μPD41221
SERIAL ACCESS MEMORY WITH CUSTOMIZED ARRAY SIZE

Introduction

This article introduces a new 320-row x 700-bit-field memory device. Originally designed for the television market, this device will find its way into many applications which require storing data in a raster format. NMOS DRAM technology, a 14-pin plastic DIP package and a unique row-pointer addressing scheme offer a low-cost device for smaller system size. The array size can be customized to meet customer applications. See figure 1.

The television business is driven by picture quality, which is an important attribute in the consumer decision-making process. High-definition television (HDTV) is usually direct broadcast transmission of 1125 line resolution. Higher picture quality can also be achieved by using the current NTSC standard and improving the image at the receiver end. It is for this market that the μPD41221 has immediate application. Because VCRs, CATV, video processing and special effects equipment use similar components, the μPD41221 finds many applications in this family of products.

In the associated industry of teletext, system price keeps terminals out of the average consumer's home.

This article shows how the frame buffer memory can reduce component cost and simplify system design. The inevitable success of this product could allow an inexpensive terminal (using tv as the monitor) to be given to the subscriber for only a monthly service charge.

The personal computer business is maturing and stablizing and two or three companies are becoming the de facto standards. With standardization comes opportunities to develop add-on PC products. Playing a dominant role in this market are the image grabber and video digital signal processing option packages. The μPD41221 finds many and varied applications in this business segment. Before studying various applications, let us look at the device architecture and operation.

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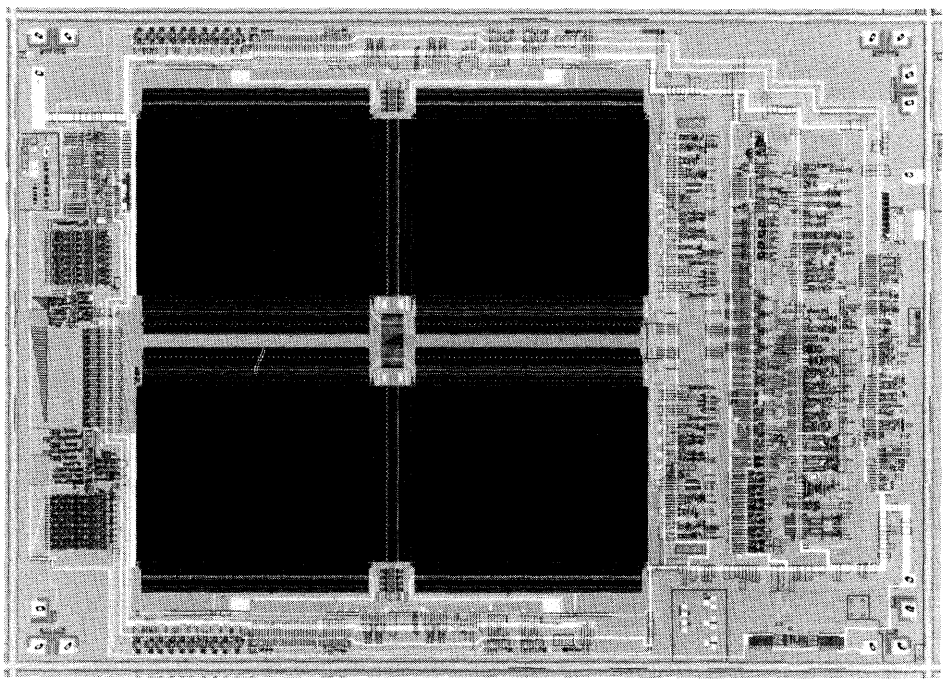
Figure 1. μPD41221C Die Photo



83-001551A

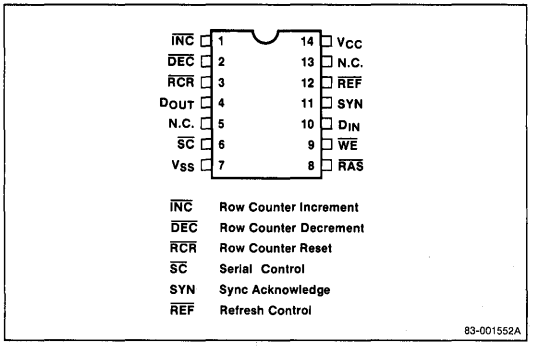
Device Definition

NEC has produced a field memory to fit most tv specifications (see table 1). This device is manufactured at low cost using 256K DRAM NMOS technology. Produced on the same lines as the 256K DRAM, the storage cells are similar, while peripheral circuits differ from those of the standard DRAM.

The device is line-addressable with the three signals $\overline{INC}/\overline{DEC}/\overline{RCR}$, and therefore allows packaging in a 14-pin dual in-line package. See figure 2.

This serial memory operates by sequential readout of each bit (column) in a row. Rows correspond to scan lines on the tv screen. The correspondence between bits in the memory and points on the screen is achieved by analog-to-digital conversion of the composite video signal which has been sampled at three times the frequency of the subcarrier signal. Seven outputs of the A/D converter are then stored in the serial memory.

Figure 2. 41221 Pinout



As seen in table 1, the μPD41221 can meet most tv standards and, by minor photomask modifications, can be customized to any size.

Table 1. Field Memory Specification for TV Standards

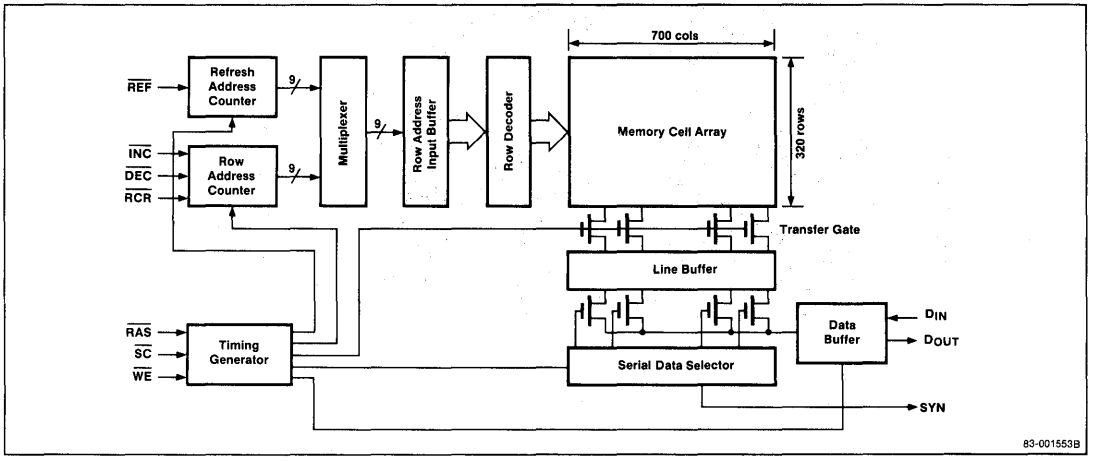
TV Standard	Sampling Rate	Memory Size	Rate
NTSC	$4f_{SC}$	263 x 910	69 ns
	$3f_{SC}$	263 x 682	93 ns
	$2.5f_{SC}$	263 x 569	112 ns
PAL	$4f_{SC}$	313 x 1135	56 ns
	$3f_{SC}$	313 x 851	75 ns
	$2.5f_{SC}$	313 x 709	90 ns

Internal Device Description

Organization

The memory array is similar to a standard DRAM containing a balanced bit line, 1/2C dummy cell and sense amplifier. A single-transistor transfer gate allows the level on the bit-line pairs to flow through and be latched in the line buffer (see figures 3 and 4). A four-phase dynamic shift register provides the appropriately timed column decode to cause a transfer from the line buffer to the serial data bus (read operation). The write operation is simply a reverse of the read, taking the data from the serial I/O and latching it in the line buffer.

Figure 3. Block Diagram



Unique Serial Read and Write Function

An initial pause of 2 ms is required after power up. After this pause it is recommended that 8 cycles of $\overline{REF}$, $\overline{INC}$, $\overline{DEC}$, $\overline{RCR}$, and $\overline{RAS}$ be performed. The total number of dummy cycles required is 40 cycles.

$8 \times (\overline{RAS} + \overline{REF} + \overline{INC} + \overline{DEC} + \overline{RCR}) = 40$ cycles

This requirement is invisible to the CRT user since a few seconds are required for the CRT to heat up.

The timing consistent with CRT operation is broken down into two time zones: (1) display time and (2) horizontal retrace time. See figure 6. Row selection can occur at any time but the row-selection pulse must be completed 100 ns before the data-transfer cycle. The negative transition of $\overline{RAS}$ starts a chain of internal clocks which precharge the bit lines, enable the sense amplifiers and turn on the transfer gates allowing the data to flow through and be latched in the line buffer (figure 4). A minimum of 710 ns is required to complete the data transfer operation, which occurs during the horizontal retrace time.

200 ns after $\overline{RAS}$ goes high, the serial clock can become active, beginning the serial-write, serial-read cycle for the display time. Refer to figure 5 for the following discussion of the line buffer and shift register. Data has been latched in the line buffer, which is actually two 176 column buffers (column 0-351) and two 174 column buffers (columns 352-699). Each line buffer pair has a shift register which provides the column decode enable, transferring data to the serial I/O pair. The I/O pairs are connected to four differential input selectors. I/O_0 and I/O_1 are tied to a serial bus which is driven from either the read selector or write selector. I/O_2 and I/O_3 are tied to a second set of read and write selectors.

During a read ($\overline{WE}$ high), one enabled read selector receives and amplifies the differential signal and inputs it to the data-out buffer. $\overline{WE}$ going low initiates a write operation by enabling the appropriate write and read selector driving the serial bus and resetting the decoded flip-flop in the line buffer.

Note: During a write operation the read selector is also active so that data also appears at data out, delayed by one serial access. The alternating reads and writes within the same operation is an unique feature not found in other DRAMs.

Data Restore

After 700 $\overline{SC}$ serial clock cycles, the output does not wrap around but switches unconditionally to a high state following the next $\overline{SC}$ low transition and remains high for any number of additional clocks (read cycle). For a write cycle the output follows the input. At the completion of the serial read or write, an internal clock signal, RAS1, has been active from the beginning of the data-transfer cycle throughout the serial read/write cycle. Due to leakage, the level of this signal begins to decay and may affect stored data. For this reason it is recommended that a data-restore cycle be performed after each period of serial read/write operation. Of course, the data-transfer operation performs a full refresh. It is the relatively long time period of maintaining RAS1 for the full scan line which creates the need for the data-restore cycle.

The data-restore cycle is achieved by bringing $\overline{WE}$ and then $\overline{RAS}$ low 200 ns after the last $\overline{SC}$ and $\overline{REF}$ clock. Data restore precharges the bit line and enables the sense amplifier, thus restoring all 700 cells for the previously selected row.

Refresh

The $\overline{REF}$ operation is executed by an on-chip refresh counter which is incremented by each refresh cycle. Nine address bits from the counter are multiplexed and sent to the row-address buffer and decoder which enables the selected row. The row selection process also generates internal row clock signals, and the full refresh functions occurs.

Figure 4. Basic Schematics of Sense-Amp. and Line Buffer

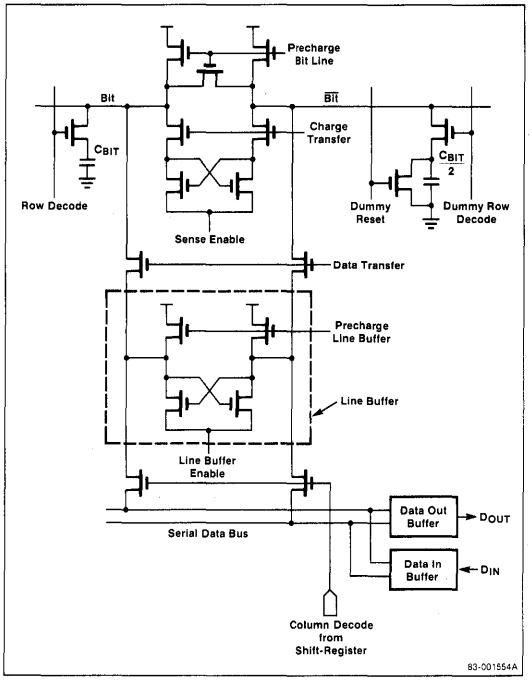


Figure 5. Basic Schematics of Shift Register

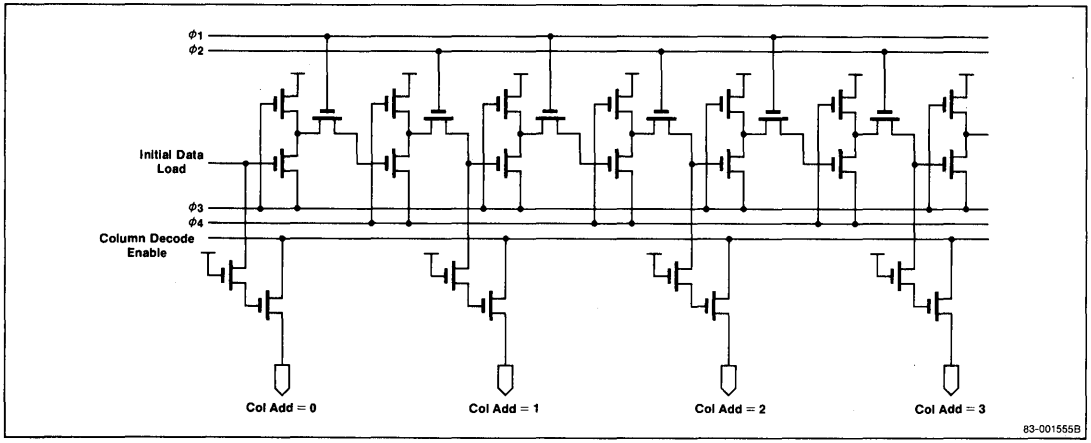
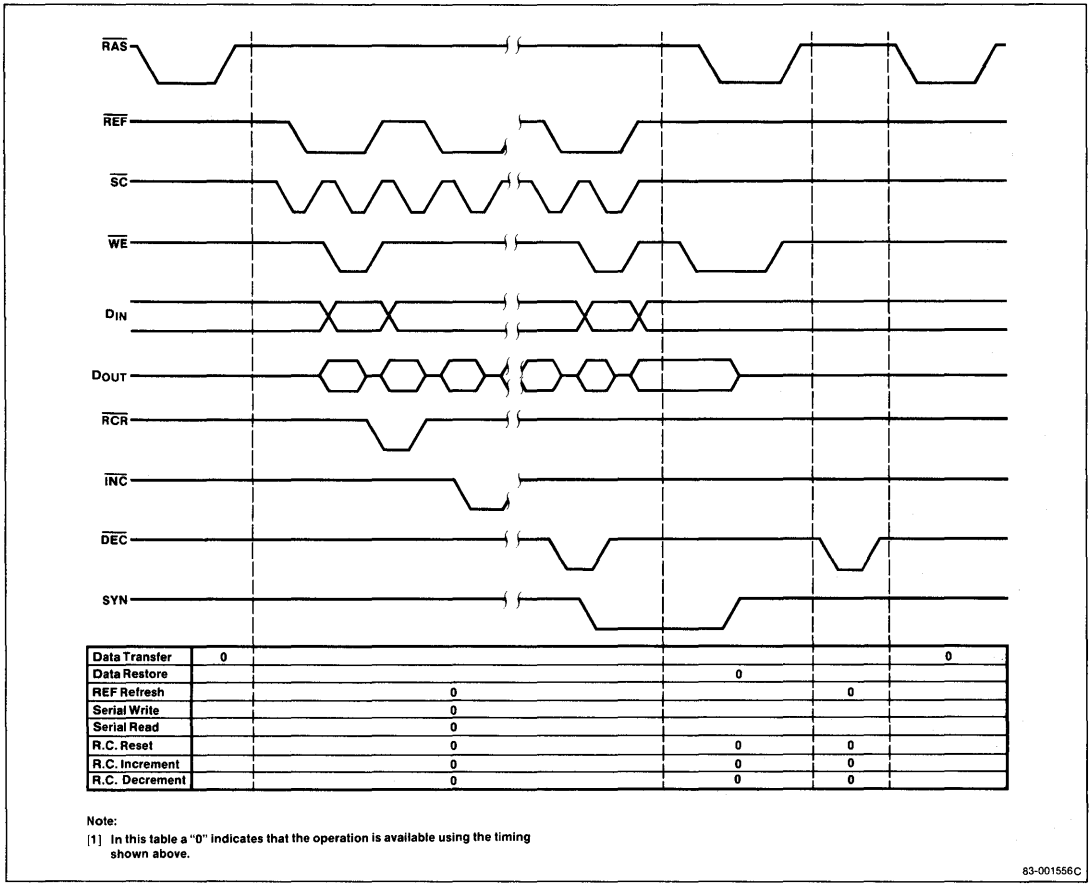


Figure 6. μPD41221 Timing Diagram



Data Transfer	0				0
Data Restore			0		
REF Refresh		0		0	
Serial Write		0			
Serial Read		0			
R.C. Reset		0	0	0	
R.C. Increment		0	0	0	
R.C. Decrement		0	0	0	

Note:

[1] In this table a "0" indicates that the operation is available using the timing shown above.

In an interlaced or non-interlaced CRT application, all 320 scan lines are read and restored every 16.6 or 33.3 milliseconds (one frame time). Obviously, this violates the 320 cycle/2 ms requirements. The $\overline{REF}$ input (pin 12) provides a method of supplying approximately 90 refresh pulses per scan line (refresh cycle = 710 ns) thus easily providing the 320 cycles within 4 scan lines.

One refresh scheme is simply to use a convenient clock (200 kHz to 1 MHz) from the system time-base generator. Gating this clock on and off with the horizontal synchronous pulse would ensure a $\overline{REF}$ refresh during the serial read/write time. Pin 12 refresh can be performed during, and asynchronously with, the serial read/write operation. Refresh can also be performed during horizontal retrace but not during a data-restore cycle or during a data-transfer operation.

Row Address Selection

The $\overline{INC}$, $\overline{DEC}$, and $\overline{RCR}$ signals modify the row-address counter. After incrementing, decrementing, or resetting the counter, the multiplexer inputs the 9 bits to the row-address buffer and decoder. This row selection can be initiated during the horizontal retrace or during video time, as shown in figure 6. The previous row address remains valid through any further video time and a data-restore cycle. The new row-decode and sense-amp operation does not begin until the falling edge of $\overline{RAS}$ begins the DT cycle.

Some Application Examples

Improved Picture Quality Through Progressive Scan Technique

The NTSC 1/30-of-a-second 525-line picture frame is broken down into two 262 1/2-line fields displayed in 1/60 of a second. This approach uses the current transmitted bandwidth but requires twice the scan rate in the television system. Today large tvs have spacing between lines and the visible line structure degrades picture resolution. The introduction of digital frame stores now makes possible the sequential or progressive scan technique.

With this technique the first or odd field is stored in the μPD41221. After scan conversion to double the line rate, each line of the even field is displayed. The stored odd field is read out of serial memory at double the normal line rate and is time-sequenced after each even line (see figure 7). All 525 lines are scanned in sequence rather than interlaced. Line flicker is thus eliminated and there is a perceived increase in vertical resolution.

Sequential Scan Television

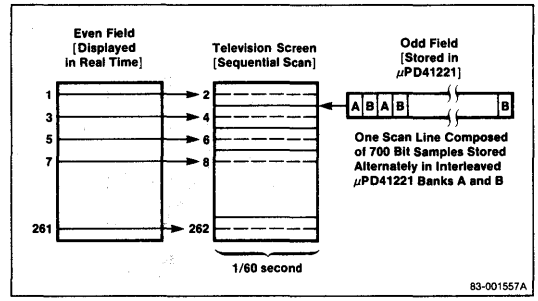
The system in figure 8 is representative of how the sequential scan technique might be implemented for the 25-inch home tv market. A dynamic comb filter separates the luminescence (Y) from the color or chroma signal (I & Q). An A/D conversion is performed on each component at three times the bandwidth of each sampled signal. A field separator discriminates the odd and even fields. The odd lines are stored in two banks of seven μPD41221 chips. The even lines can be displayed in real time, delayed by one horizontal time and scanned at twice the normal rate.

As mentioned before, all 525 lines are displayed in 16.67 ms, which results in 32 μs per line. Displaying 700 samples in 32 μs requires an access time of 45 ns per sample necessitating two banks of memory and a memory interlacing scheme shown in figure 7. The chroma I and Q signals can be multiplexed and only one bank of serial memory is required.

Image Freeze and Transmission

The personal computer in the automated office environment has many purposes, not the least of which is intercompany communications. Electronic mail is a great asset to the office but the ability to transmit images as well as text will open exciting new markets. Providing a means for people to view the same object even though they are thousands of miles apart will have a major impact on productivity while reducing costly travel.

Figure 7. Sequential Scan Technique



The diagram in figure 9 shows a freeze-frame transmission option for the IBM Personal Computer. Two of the five I/O system bus card slots are utilized. Since the image data is transmitted over telephone lines, a modem and the synchronous data line adapter are required. The frame grabber would occupy a second card slot and would contain the μPD41221 devices, A/D and D/A converters, and the required memory timing and control circuits. The number of serial memories used is dependent on such factors as screen resolution, number of colors, text overlay, etc. A high-speed line buffer is used to store one scan line of information.

While the tv camera analog signal is sampled and stored in the frame buffer it is simultaneously displayed on the monitor. (Displaying the frame as it is written in memory is possible because data-in appears at data out during a write cycle.) A scan line of data is transferred to the line buffer where it awaits a DMA transfer cycle. Now in system memory the data can be compressed prior to being transmitted over the telephone lines. Once received the compressed signal is decompressed and displayed on the monitor.

Figure 8. T.V. Employing Sequential Scan Technique with NEC's μPD41221

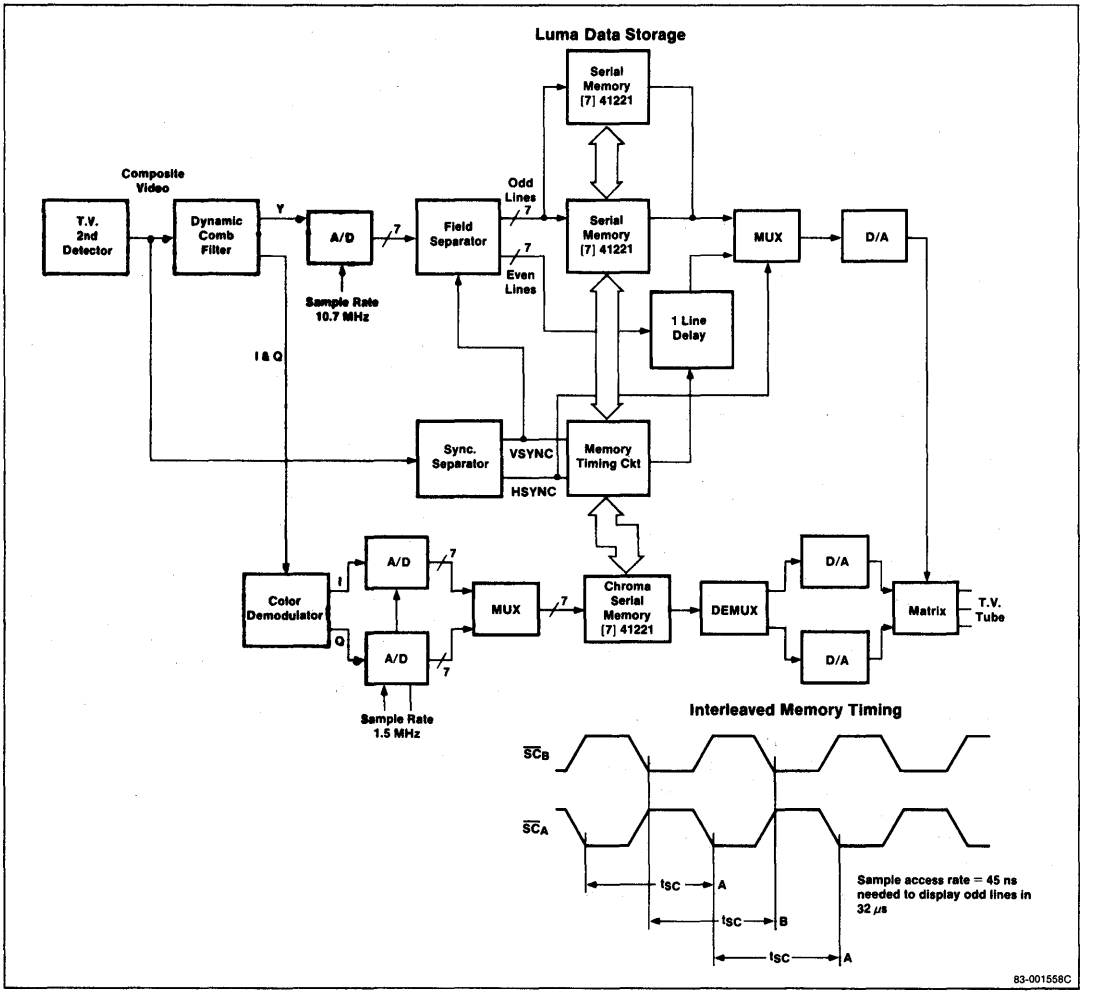
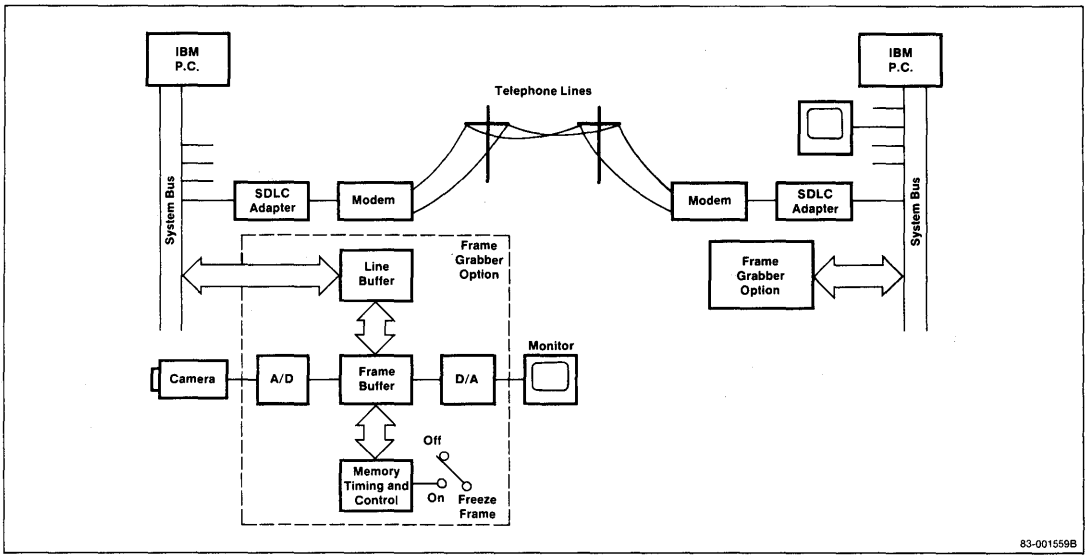


Figure 9. Image Freeze and Transmission System



μPD41221 vs Standard DRAMs for TV Applications

For tv applications the DRAM is an awkward fit. Achieving the higher access rates requires using three RAMs in parallel combined with a high-speed shift register. The serial-parallel and parallel-serial conversion coupled with the complex logic and control circuits makes this technique a poor alternative. Interleaving page-mode cycles or use of static-column devices also adds circuit complexity and increases system cost. The use of DRAMs is also likely to require the addition of a CRT controller and/or DRAM controller.

Memory-timing circuitry for the system shown in figure 9 is relatively simple compared to that required using DRAMs. The logic diagram in figure 10 is an example of how the memory timing might be designed for the frame grabber section of the image freeze and transmission system. The momentary on/off switch S1 (write/read control) in the on position initiates the data transfer, serial write and data-restore cycle storing one frame of information. When S1 is in the off position the frame buffer operates in the read and refresh mode, continuing to update the display.

After the horizontal and vertical sync pulses are stripped from the composite video, these signals are used by flip-flops U3 and U5 to generate the timing for the μPD41221. These signals control the field memory so that data restore and data transfer are performed during the horizontal retrace period. Serial data is read from or written to the field memory starting in the blanking period and continuing through the display period. The timing diagram for this system is shown in figure 11.

The counter U4 is used to generate the basic horizontal scan timing. The leading edge of the HSYNC releases the counter U4. Counter U4 counts the 2 MHz clock and decoder U6 generates $\overline{RAS}$ and $\overline{WE}$ for the data transfer and data restore functions. Outputs of the 74LS42 (1 through 4) are used for this purpose. $\overline{INC}$ and $\overline{RCR}$, which control the row addresses, are generated by decoder output 6. Decoder output 7 resets the counter, and data reading or writing begins. The $\overline{SC}$ signal is generated from the 3fSC clock. During the read and write time, the $\overline{REF}$ signal (generated by halving the 2 MHz clock) is available to perform memory-cell refresh.

With the momentary switch S1 in the normally off position, the $\overline{WE}$ signal is held high to allow the complete read out of the field memory. To store one field, $\overline{WE}$ is held low during the serial write time. This operation is controlled by counter U5. When switch S1 is pushed on, the memory is placed in the input mode. With all outputs high the counter loads on the next edge of the vertical sync setting QA low. QA controls the $\overline{WE}$ signal to set the one field write mode.

There are no addresses to be generated, no multiplexing, no latches and refresh ($\overline{REF}$) is provided by the 2 MHz output of U1. Using the 41221C, the control circuitry is reduced to about ten standard TTL logic ICs. This logic could be implemented in a gate array of about 250 gates.

Figure 10. Memory Timing and Control Chart

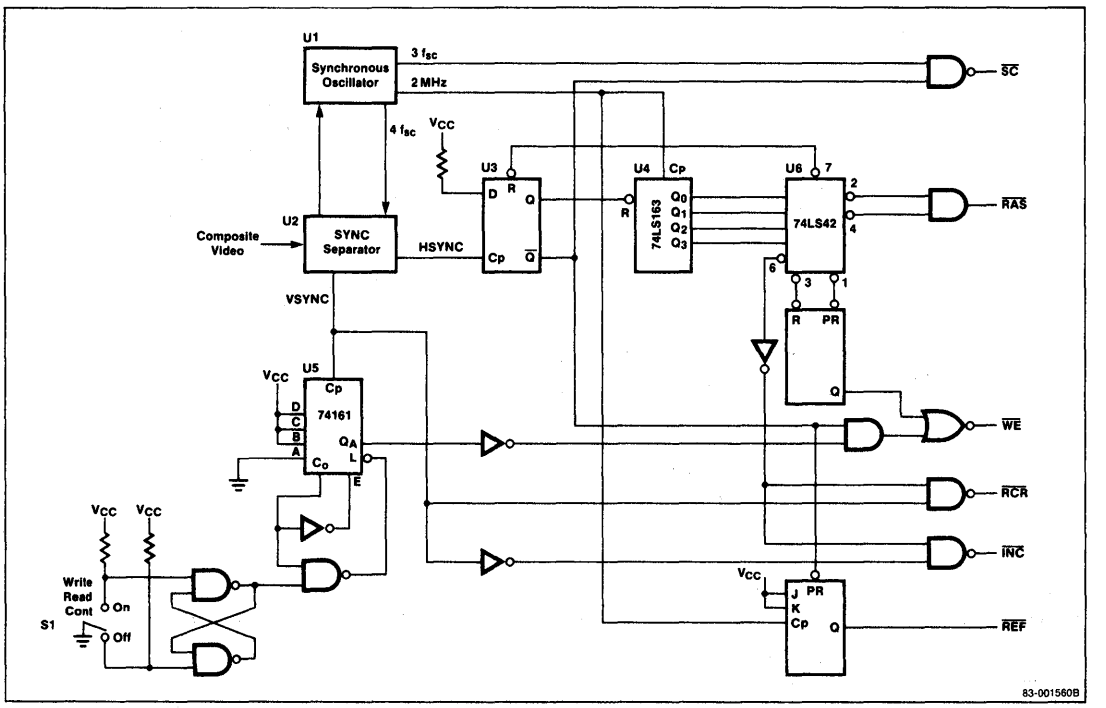
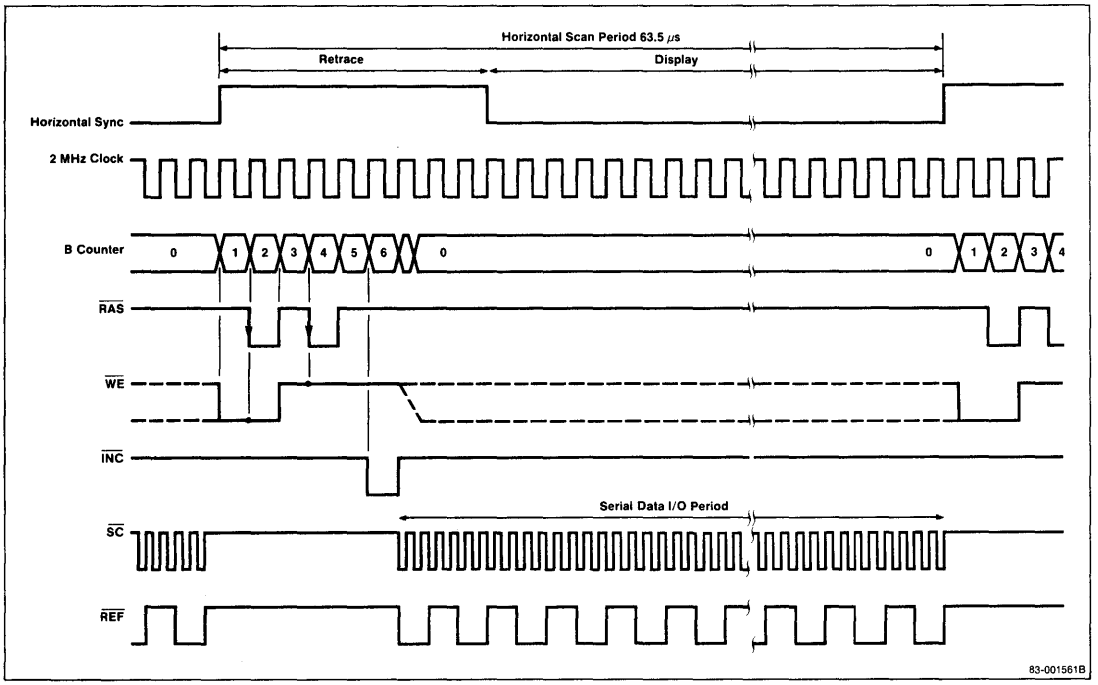


Figure 11. System Timing



A Peek at the Future

The new automated office and consumer applications will require the recording and transmissions of printed documents and photographic images. This facsimile-type transmission will demand low cost systems. Application-specific memories will play a major role in reducing the cost of these systems.

The cost advantages of NMOS DRAM mass production technology can now be applied to consumer products. In defining new devices, NEC is evaluating all operating parameters: speed, power, configuration and special on-chip circuits to best fit these new and emerging products. For example, field memory devices with capacities of 1 megabits could be used with high-performance systems requiring four times the sampling rate.

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APPLICATION NOTE 33 μPD41264 VRAM AND μPD7220A SYSTEM IMPLEMENTATION

Introduction

This application note describes the function of NEC's μPD41264 dual-ported memory and illustrates a graphics system that uses the μPD7220A Graphics Display Controller (GDC) and the μPD41264, operating in flash drawing mode. The first part describes the memory and the second part describes the system, with information on interfacing the video memory to the GDC and generating system timing.

μPD41264 Video RAM

Two real ports in a single piece of silicon is an exciting alternative to the use of standard memories and large quantities of TTL interface logic. NEC introduced the μPD41264 video memory at the 1985 International Solid State Circuit Conference (ISSCC). It combines a standard 64K x 4 DRAM with a high-speed 256 x 4 serial port. In this application, the serial port is referred to as port B and the random access port is referred to as port A.

The μPD41264 uses a double-poly-layer N-channel silicon gate process to provide high density, high performance, and high reliability. The 24-pin 400 mil DIP package is made possible by multiplexing two functions on a single terminal ($\overline{DT}/\overline{OE}$).

Data Transfer Operation

The data transfer (DT) operation (figure 1) is initiated when $\overline{DT}/\overline{OE}$ is low before $\overline{RAS}$ goes low. The operation begins as in a standard DRAM; $\overline{RAS}$ strobes row-address information into the row-address buffer and the information is sent to the row decoder to select a word line. Cell data is then transferred to the bit line and amplified. The transfer from the memory cell to the data register occurs on the positive edge of $\overline{DT}/\overline{OE}$. 1024 bits of data are sent through the enabled data transfer gates and into the data registers. The data registers then contain the new data, which is immediately ready for the serial port. The DRAM (port A) remains in tri-state during this data transfer cycle.

In non-$\overline{DT}$ cycles, $\overline{DT}/\overline{OE}$ is held high, disconnecting the data registers from the memory array. The data transfer gates are disabled or turned off, allowing both ports to operate asynchronously. During this time, the CPU can access port A while port B updates the display. In this mode, port A operates as a standard RAM device, making an $\overline{OE}$-controlled write possible.

Port B Operation

While the DT cycle proceeds, the SC clock provides video clock rate timing to a serial selector which shifts data out each pin (SO_0 to SO_3). This activity is independent of the RAM port except during a data-transfer cycle.

This is the only time interval when the RAM port and serial port do not work independently. The serial port reads out data serially from the registers starting at a specified location. Data appears at SO_i after an access time of t_{SCA}, referenced from the high transition of SC. With the speed of the SC clock, the data-valid time is short, making it difficult to latch the data into an external shift register. To solve this problem, the μPD41264 holds or latches the data until the next SC cycle.

The $\overline{SOE}$ signal must be low during a serial-shift cycle. When this pin is high, port B is in a high-impedance state. The $\overline{SOE}$ pin allows you to combine multiple chips in parallel.

Once the DT cycle occurs, 1024 bits of data are transferred from the cell array to the data register, which is now ready to send new data to the serial port. In this cycle, eight bits of column address are latched in the address buffer and sent to an 8-bit counter. This counter specifies the starting location of the serial selector in the data register. After setting this pointer, the 8-bit counter increments once for each SC clock cycle and wraps around like a ring counter after 256 SC clock cycles. This technique allows you to exchange new data for old "on the fly" in real time without interruption.

This real time operation requires that DT and SC be synchronized to ensure a continuous stream of valid data. The rising edge of $\overline{DT}/\overline{OE}$ must maintain a t_{SDD} (setup time) and t_{SDH} (hold time) with respect to the SC clock. This data register update timing is significant because it removes the restriction of waiting for the horizontal-blanking time before passing new pixel updates to the shift register.

Write-Per-Bit Operation

Graphics applications often require changing only selected pixels while surrounding pixels remain unchanged. In a single-memory plane, when you change pixel data for vector generation, the only bits that change are the vector bits. Multiple-plane write-per-bit applications include changing text over a constant image or, in a CAD system, changing only one layer of

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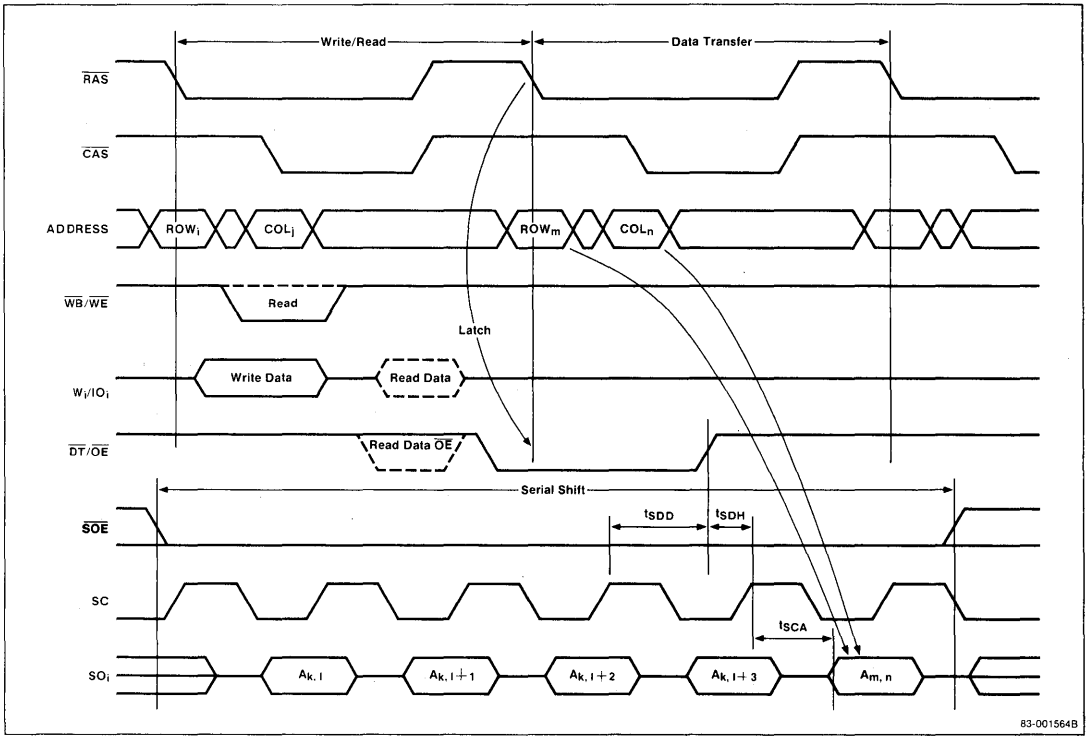
Figure 1. Timing Chart in a Data Transfer Cycle



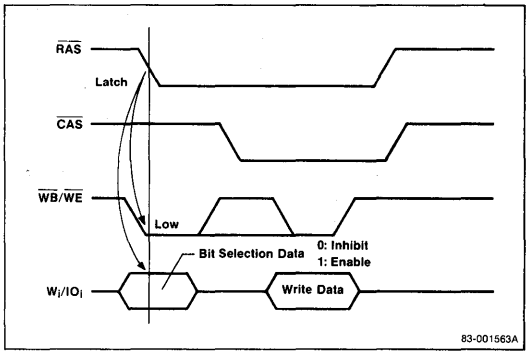
a VLSI chip. Standard DRAMs require two cycles or a read/modify/write cycle for this process. First, all four bits are read out; then the CPU modifies the data and rewrites it.

The μPD41264 can selectively access any one or combination of four bits. Latch the write-per-bit (WB) mode by bringing $\overline{WB}/\overline{WE}$ low before $\overline{RAS}$ goes low (figure 2). The bit selection or mask information is multiplexed on the common I/O terminal W_0/IO_0-W_3/IO_3. If the bit selection data is a logical 1, the common I/O terminal is enabled and new write data updates the frame buffer. A logical 0 inhibits the write and leaves the pixel unchanged.

If you perform a read/modify/write cycle, old mask data remains latched as long as $\overline{RAS}$ is held low. In a non-WB mode, this pin acts as a standard write enable, simultaneously writing all four bits.

Discussions with video systems houses reveal that competitive pressures are driving performance improvement. The independent clocking of the DRAM and serial port allows random access to occur simultaneously with shifting out video data. Asynchronous operation provides the CPU with almost 100% access to the frame buffer. Video RAMs allow the system designer to use his creativity to make the best use of the DRAM update time.

Figure 2. Write-Per-Bit Function Timing



The μPD7220A/μPD41264 Graphics System

Figure 3 shows a block diagram of a μPD7220A-based graphics system. The display memory is made up of four μPD41264s to form a 16-bit-wide memory plane. The multiplexed input and output lines are directly connected to the μPD7220A address/data bus. The data bits in the μPD41264 data register are loaded into the 8-bit shift register through the four serial output lines. The timing-controller logic generates the signals required to synchronize all the blocks within this system.

Use of the μPD7220A

The μPD7220A interacts with the display memory in display cycles and drawing cycles. (Refer to the Data Sheet and the Design Manual for the μPD7220A for detailed discussion on the use of these features and others mentioned later in this application note.) Display cycles are made up of two 2xWCLK cycles (2xWCLK is the input clock to the μPD7220A). A display address is output during the first cycle and the data is available at the end of the second cycle. Drawing cycles are made up of four 2xWCLK cycles. A drawing address is output during the first cycle and the μPD7220A reads the data from the display memory in the third cycle. It modifies and outputs the data at the end of the fourth cycle.

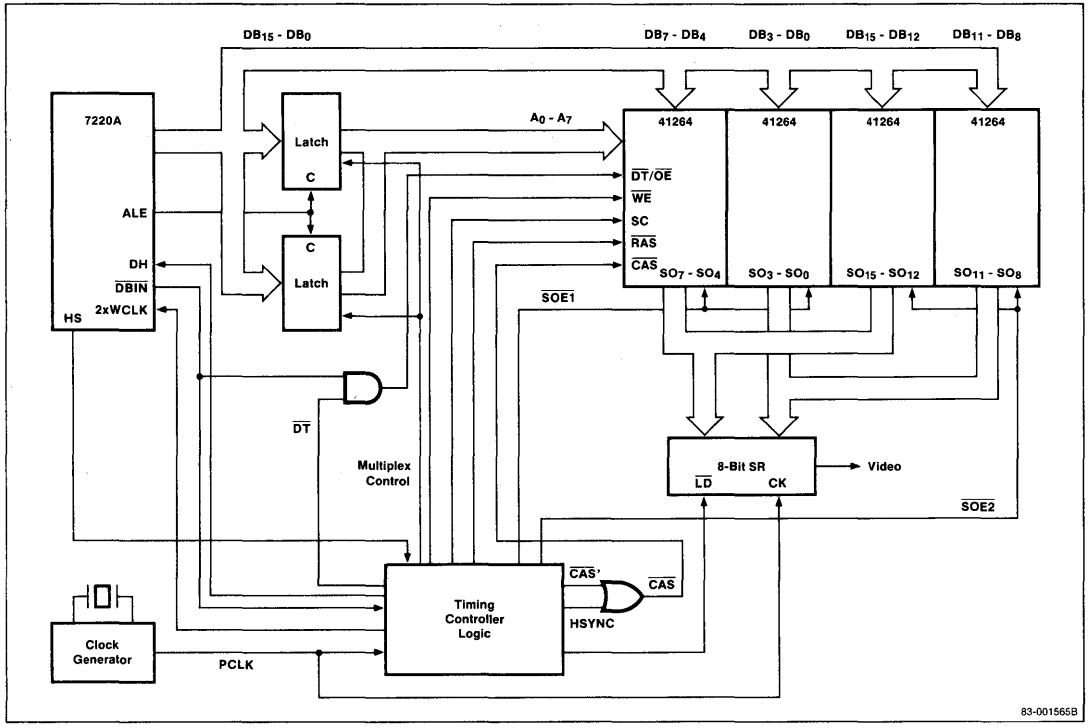
Drawing and display cycles are output in flashless and flash modes. In flashless mode, the drawing cycles are generated only during the horizontal and vertical blanking periods, and display cycles are performed during the active video time. This means that there are no display disturbances, but the update time is brief (15 - 20% of the total video time).

Flash mode allows drawing cycles to be generated at all times. Display cycles are output only when no drawing operation is in progress, or when the drawing hold (DH) pin of the μPD7220A is held high for four 2xWCLK cycles. This mode increases the update rate by four or five times, but makes display interruptions more likely.

The drawing hold function allows the μPD7220A to interface to the μPD41264 VRAMs. The μPD7220A can then operate in flash mode.

3

Figure 3. System Block Diagram



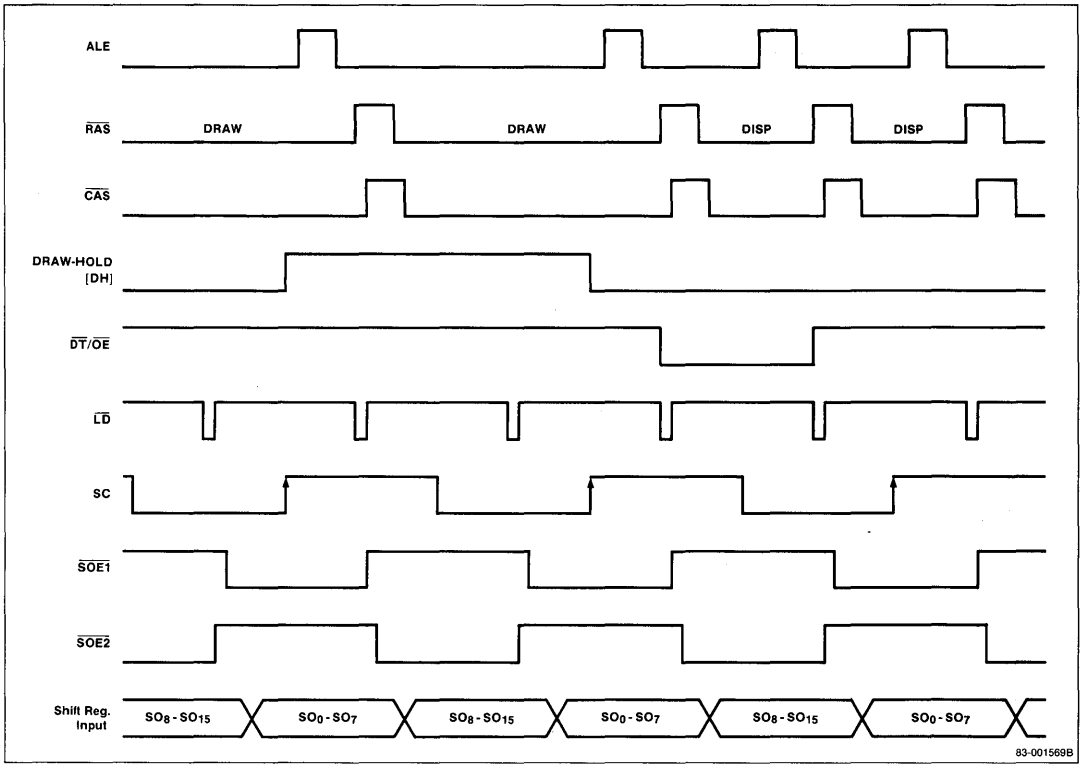
System Interface to the VRAMs

As shown in figure 3, the 8-bit shift register input data lines are connected to the serial data outputs of the four μPD41264s. The serial output enable signals ($\overline{SOE1}$ and $\overline{SOE2}$) input to the μPD41264s become active one at a time. This loads the shift register twice in one SC cycle. The SO_7-SO_0 data bits are loaded into the shift register after the rising edge of the SC clock. The shift register is emptied before the first half of the cycle ends. Then, the SO_{15}-SO_8 data bits are loaded at the middle of the cycle after the falling edge of SC occurs. This method of memory bank switching eliminates the need for an extra 8-bit shift register. Because 16 bits overall are shifted out during an SC cycle, the value of the serial clock frequency is one-sixteenth of the pixel clock (SC = 1/16 x PCLK).

The serial output enable ($\overline{SOE}$) input signal enables the serial output buffers of the μPD41264. There is a delay between the time that $\overline{SOE}$ goes active and when the serial data bits become valid. The signal transitions of $\overline{SOE1}$ and $\overline{SOE2}$ should not coincide with the SC clock to prevent data contention while switching memory banks. If the SC clock period is too short, this time delay may not be tolerated, preventing memory bank switching. In this case, you should use an extra 8-bit shift register.

The falling edge of the ALE signal latches the 16-bit address from the μPD7220A into the tri-state latches. The timing diagram in figure 4 shows how the ALE signal is delayed to construct the $\overline{RAS}$ signal. Delaying the $\overline{RAS}$ signal by a few PCLK cycles generates the $\overline{CAS}$ signal.

Figure 4. Timing for Memory Cycles



System Operation

This system uses three memory cycles: $\overline{RAS}$-only refresh cycle, read/modify/write cycle, and data-transfer cycle. The μPD7220A can perform the dynamic memory refresh if this is programmed in its RESET command. The lower 8-bit address lines (AD_7 - AD_0) of the μPD7220A are connected to its internal 8-bit refresh address counter. This counter is enabled during horizontal sync and its output is available on the falling edge of the ALE signal. Therefore, $\overline{CAS}$ and horizontal sync should be gated so that the $\overline{CAS}$ cycle does not occur during this period. A refresh cycle is accomplished with the row address coming from the AD_7-AD_0 lines during the $\overline{RAS}$ cycle. The number of refresh cycles depends on the width of the horizontal sync (programmable in the μPD7220A).

A drawing cycle in the μPD7220A is basically an RMW cycle. The external logic uses the $\overline{DBIN}$ signal to control the data bus output direction. This signal is used to control the $\overline{DT}/\overline{OE}$ inputs of the μPD41264s. When low, data is output from the memories so that the μPD7220A can read it. The $\overline{DBIN}$ signal also generates the $\overline{WE}$ (write enable) signal. This is accomplished by delaying $\overline{DBIN}$ by one and one-half 2xWCLK cycles and ORing the result with the 2xWCLK signal (see figure 5).

Setting the image bit and GD bit to one increments the display address every other display cycle. This mode allows you to double the μPD7220 clock rate while maintaining the occurrence of display addresses as in normal mode, thus doubling the drawing speed. This is shown in figure 6. DAD represents the display address.

A data-transfer cycle is the same as a read cycle except that the $\overline{DT}/\overline{OE}$ input signals of the μPD41264s must be low before $\overline{RAS}$ occurs. The external logic should generate a draw hold (DH) signal to the μPD7220A before generating this cycle. The DH signal must be high for four 2xWCLK cycles so that the μPD7220A can complete the current drawing cycle. After the DH signal goes from high to low, the μPD7220A generates two consecutive display cycles. The external logic can then use these display cycles to perform a data-transfer cycle. Figure 4 also shows the timing for this event.

The rate at which data-transfer cycles occur depends on the mapping of the display memory. If the mapping is such that the screen width is equal to the actual width of the display memory (in μPD7220A terms, this is referred to as the pitch parameter), a data-transfer cycle is generated every 256 SCLK cycles. Depending on the horizontal pixel resolution, the data-transfer cycle could take place during a raster-scan period. If so, you should perform a real-time data transfer.

If the screen width is less than the display memory width, generate a data transfer cycle during every horizontal retrace period to put data for the next horizontal line into the data registers of the μPD41264s.

Conclusion

So far, graphics systems based on the μPD7220A and regular dynamic memories have not been able to take full advantage of the μPD7220A's drawing speed; mainly because most systems use the μPD7220A in flashless drawing mode to avoid display disturbances. However, the advent of the μPD41264 makes it possible to use the flash drawing mode, increasing the drawing rate to four or five times the rate of systems using regular dynamic memories.

The key to this increased drawing rate is the dual data ports integrated into the μPD41264. The μPD7220A can communicate with port A to update the display memory at the same time that port B is being used to update the video display.

Figure 5. Timing for Drawing Cycles

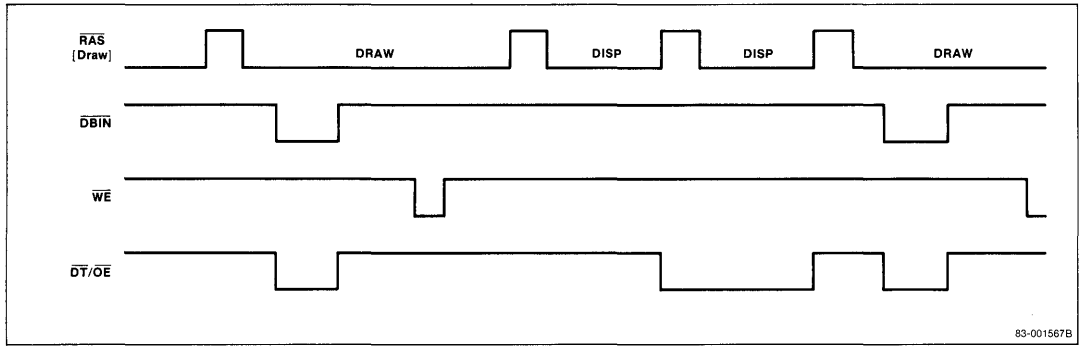
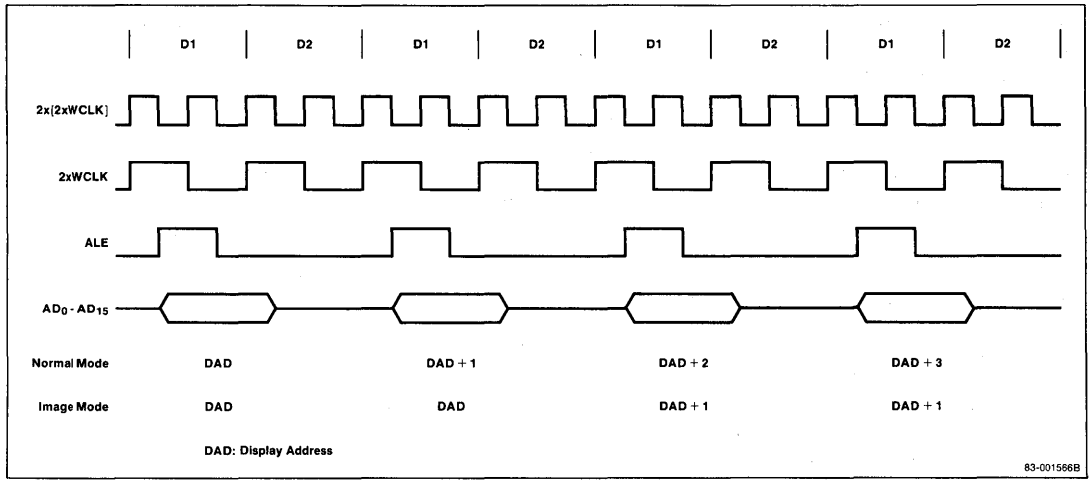


Figure 6. Image Mode and Normal Mode



APPLICATION NOTE 34
μPD41264
262,144-BIT DUAL-PORT DYNAMIC NMOS RAM

Development of a 256K-Bit Dual-Port Memory for Frame Buffering with Capability of Uninterrupted Serial Output

by Satoru Kobayashi, NEC Inc., Memory Technology Headquarters

NEC Inc. has developed a 64K x 4-bit dual-port dynamic memory chip with a key design emphasis on its ease of use in frame buffering for bit-mapped displays. The commercial part number is μPD41264. While it is accessed randomly, the memory is capable of displaying data output in a serial mode at the maximum rate of 25 MHz. In addition to this, as basic features, it has three new functions. They include the function to internally transfer data into the data registers designated for serial output while performing the output function of the display data. To accomplish the intended functions and performance level, the manufacturing technology has been kept the same as the existing one, while the circuit designs were modified. When this memory is used, updating the displayed data becomes several times faster than conventional methods

The advancement in semiconductor technology has been significant since the beginning of the 1970s. In the field of integrated circuitry, various types of technological innovations were made with the goal of higher density in integration, lower power dissipation, and lower costs.

Among such innovations, most notable changes occurred in the MOS dynamic memory. First, with the advent of the 1K-bit dynamic memory, the traditional magnetic core was replaced by semiconductor memory. Since then its capacity has been increasing by a factor of four every 2 to 3 years. At present the 256K-bit products are prevalent in the marketplace, and it appears as if sometime in 1985 specimens of 1M-bit memory might appear.

Product Diversification Started with 64K-Bit Products

The transition has been characterized by the increase in chip memory capacity; about the time the 64K-bit products appeared, product diversification started. Not only did we see improvements in the basic functions aimed at a decrease in access time and a reduction in power dissipation, but we also started seeing products with functions making them easy to use by increasing the tolerances in their critical timings, new refreshing methods, etc. At the same time, specialized memories dedicated to specific applications started appearing along with the 64K-bit products.[7, 11-13]

For instance, in addition to the conventional page mode, new high-speed access modes such as the nibble mode, static column mode, and ripple mode were introduced.[3, 4, 9] Then there were peripheral CMOS-type dynamic RAMs that combined the CMOS technology in peripheral circuits for the specific purpose of lowering power consumption. Moreover, to improve the ease of use, CAS-before-RAS refresh and self-refresh were introduced as additional functions plus functions to moderate the timing criticality in the areas of RAS time-out in static column mode and time-out during write.

Owing to these improvements in functionality and performance, the burden on users designing their systems was reduced. It should be noted, however, that these improvements were made with the anticipation of primary use as the main memory of large-scale mainframe computers. They were not developed for use in small systems, which have seen a dramatic rise in popularity in recent years. For this reason, they were not the kinds of functions that were necessarily easy to use from the viewpoint of small system designers.

Demands Are Increasing for Display Memories To Be Used in Small Systems

During the latter half of the 1970s, microprocessors began to be used in various types of electronic equipment. At the same time, a demand for memories was created for small systems such as personal computers, word processors, computer terminals, work stations, and CAD/CAM systems. Along with the rise in popularity of microprocessors, the unit price per bit of dynamic RAMs came down dramatically. The falling prices spurred a drastic increase in the volume of dynamic RAMs used in small systems. As a result, the ratio of their use is now reversed between small and large systems.

The application of RAMs in small systems can largely be divided into main memory and display memory. The main difference between small and large systems is that in small systems the ratio of RAMs used as display memories for storing character and graphic data is extremely large. The size of display memories per system ranges from several tens of kilobytes to as many as several megabytes, whereby the trend shows that the size has become equivalent to or larger than that of the main memory itself. It is expected that the demands for RAMs for display memories will continue to grow. There are speculations based on actual usage

that within 2 to 3 years as much as 30 to 40 percent of dynamic memories will be used for display purposes. Among display memories, frame buffers for bit-mapped displays will see a dramatic market expansion.

As Memory Capacity Increases, Conventional Chips Become More Difficult To Use.

Some aspects of the traditional standard chips render them difficult to use as frame buffers. Worse yet, as memory capacity increases from 256 kilobits to 1 megabit, problems stemming from difficulties associated with their use will become much more serious.

First, in the area of x1-bit patterns, which have traditionally made up the main type of RAMs, if the capacity increases, there will be situations in which the length of a word is too deep. At present, the capability for display resolution is generally in the range between 256 x 192 and 1280 x 1024 pixels. For instance, when a 256K-bit memory is used in a small-scale 256 x 192 pixel display, five planes can fit into one chip. It is difficult not to waste memory cells; the peripheral circuits tend to get large. Although there are specimens of x4-bit and x8-bit pattern memories, their main applications are for main memories in small systems. When they are used for frame buffers, and if the memory capacity requirement per chip is increased by a factor of four, then there is a tendency that this setup would spur demands for the word length also to be expanded by a factor of four. But if this is to be done, the number of pins needed would increase and the package size would become large, hence diminishing the advantage of a large capacity memory.

The memory cycle time is also a problem. For instance, in a display of 1280 x 1024 pixels, the display data are sent to the CRT at a speed of about 9.3 nanoseconds per pixel.[5] This is significantly shorter than the cycle time of conventional dynamic RAMs. For the purpose of mitigating the speed difference, the user must resort to a technique of taking out the data in parallel from a number of dynamic RAMs and converting the data into a serialized stream. For this, either parallel-to-serial conversion registers are used or a technique is used to enable the dynamic RAMs in a time-sliced synchronization schedule. Either way would result in bloated peripheral circuitry while the number of connection lines would increase on the printed circuit board. This, in turn, would become a burden during the PC board designing phase. As a result, even though it makes a large capacity memory possible, actual use in a system is difficult.

The basic function of a frame buffer is to send display to the CRT at a designated speed. The performance level of a system is determined by the efficiency with which the processor can refresh the display data while continuing this basic function. A frame buffer requires two access ports.[10] But a conventional standard dynamic RAM has been characterized as being a single-port memory, namely, containing only one set each of data input/output terminals and address input terminals. While the display data are being output to the CRT, this type cannot concurrently allow the processor to perform the memory access. There is only one remedy to this: introduce the time-slicing scheme so as to use it as a pseudo-dual-port memory.

There are primarily two methods of time-sliced access to a frame buffer. One is to permit CPU access to it only during the blanking phase of the display, while CPU access during the data display phase is restricted to sending display data to the CRT. This would invariably reduce the access efficiency of the processor to 20-30 percent. Another method is the cycle-steal method wherein the timing intervals are so minutely divided as to allow the processor access to the memory even during the display phase. As compared to the first method, the operational efficiency is improved; however, it requires complex high-speed peripheral circuits.

As pointed out in the foregoing, conventional standard dynamic RAMs are difficult to use for frame buffers. In principle, it is possible to assemble a large capacity memory into a frame buffer so long as it can function at a high rate of speed. Moreover, it is possible that, as replacements to the traditional page memory, techniques will be developed to use this type of memory in such high-speed access modes as the nibble mode, static column mode, and ripple mode.[5, 9] But for this type of memory to be used in such modes, additional externally attached circuits are needed between it and the microprocessor. If it is a single-port memory, building a frame buffer out of it becomes more difficult as its memory capacity becomes larger.

A Dual-Port Memory Solves Frame Buffering

Of various memories used for displays, we judged that the most adequate solution for a memory chip to be used for frame buffering was a genuine dual-port memory. Hence, we started our development efforts accordingly. The results were the dual-port dynamic memory (μPD41264), about which we published details in February 1985.[1, 6, 8]

As illustrated in figure 1, it is equipped with a 64K x 4-bit random access port, and a 256 x 4-bit serial access port. The serial port consists of four 256-bit data registers, each allowing serial output at the maximum rate of 25 megabits/second. This serial port can be used as a dedicated port for sending display data to the CRT. When a 4-bit parallel-serial converter is externally attached to it, it can send display data to the CRT at 100 megabits/ second.

The random access port does not have to get involved in display data output to the CRT except for timing the internal transfer of 1024-bit data blocks from the memory cell arrays. Using this memory chip, there is no need to resort to a cycle stealing technique to increase the access efficiency of the processor; in fact it can obtain nearly 100 percent efficiency.

In addition to the foregoing, we also devised measures to keep the memory cell usage efficiency rate near 100 percent regardless of what type of pixel configuration the display may consist of. The design intent was to allow it to accommodate a wide range of uses as a frame buffering memory, from low-resolution to high-resolution displays.

Dedicated Memories Deployed As the Market Determines

As for dynamic memories, we have entered a period when dedicated memories should be developed for a specific application, focusing on the functions and performance level it calls for so long as the market size is large enough. As we mentioned before, the area in which the memory demands will see a dramatic increase in the near future is display memories. We have classified the display memory field in figure 2. We divided the field into computer, television, telecommunications, and hybrid application groups, and established a basic goal of developing dedicated memories best suited to each application group. We have already commercialized a dedicated product (μPD41221C)[2] for television and telecommunication applications. This product was designed as a field memory for television and VTR applications by allowing high-speed serial input/output cycles. Since it is specialized for applications that do not require direct data manipulation by the processor, no random access function was provided. This allowed the chip to be packaged as a 14-pin DIP. The dual-port memory chip that we are introducing as a product this time is aimed at the computer applications group.

Functions Added for Frame Buffer Applications

The functional block diagram of the dual-port memory that we developed as a product this time is illustrated in figure 3. In addition to the 64K x 4-bit dynamic RAMs, we added a circuit that creates a serial port. The latter can internally transfer in one cycle a line of 1024 data bits from the memory cell array to a 256 x 4-bit register. Interfacing with the internal data transfer are the data transfer gates, which consist of 1024 transistor arrays. This setup makes it possible to serially output the data stored in the data registers by means of a selector and an output buffer. Its maximum output speed is 25 megabits/second.

Instead of shift registers, the serial-port registers were made of circuits that allow selective output of data from the data registers via a selector. Because of this design, it was possible to realize the pointer-control function to start serial output from any array address immediately following an internal data transfer.

The package is a 24-pin plastic DIP (figure 4). Because of the serial-port circuit, the width of the chip grew. For this reason, a 10.2-mm (400-mil) wide package was required. The terminals that are provided in the package but missing from the conventional standard-type RAMs are the serial clock (SC) terminal that controls the

Figure 1. Basic Configuration of a Dual-Port Dynamic Memory

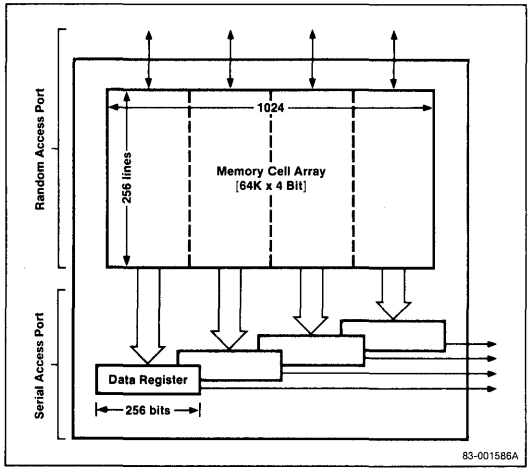
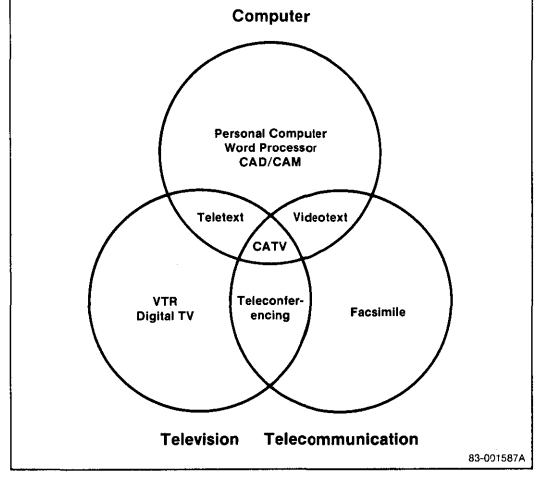


Figure 2. Application Fields of Display Memories



serial port, the serial output enable ($\overline{SOE}$) terminal, and the serial data output terminals (SO_0-SO_3), a total of six terminals. In addition, a data transfer control clock ($\overline{DT}$) for internal data transfer to the serial ports, a write per bit control signal ($\overline{WB}$), which became a necessity for the newly created functions, and the mask data input signals (W_0-W_3) were added as new features. However, to keep the increase in pins to a minimum, these were piggy-backed onto the conventional signal terminals.

Table 1 summarizes the primary timing characteristics of the μPD41264-12 product. With regard to refresh function, it requires 256 refresh cycles in 4 ms, the same as conventional dynamic RAMs. Since a refresh address counter has been provided internally, it is possible to allow the CAS-before-RAS refresh function. The input-output signals are handled entirely at the TTL level. In addition to the μPD41264-12, we also provided another product (μPD41264-15) with a maximum RAS access speed of 150 ns.

Figure 5 shows the source current waveform. When two ports are active simultaneously, current is 190 mA maximum. When ports are idle, current is 15 mA maximum.

Table 1. μPD41264-12 Timing Characteristics

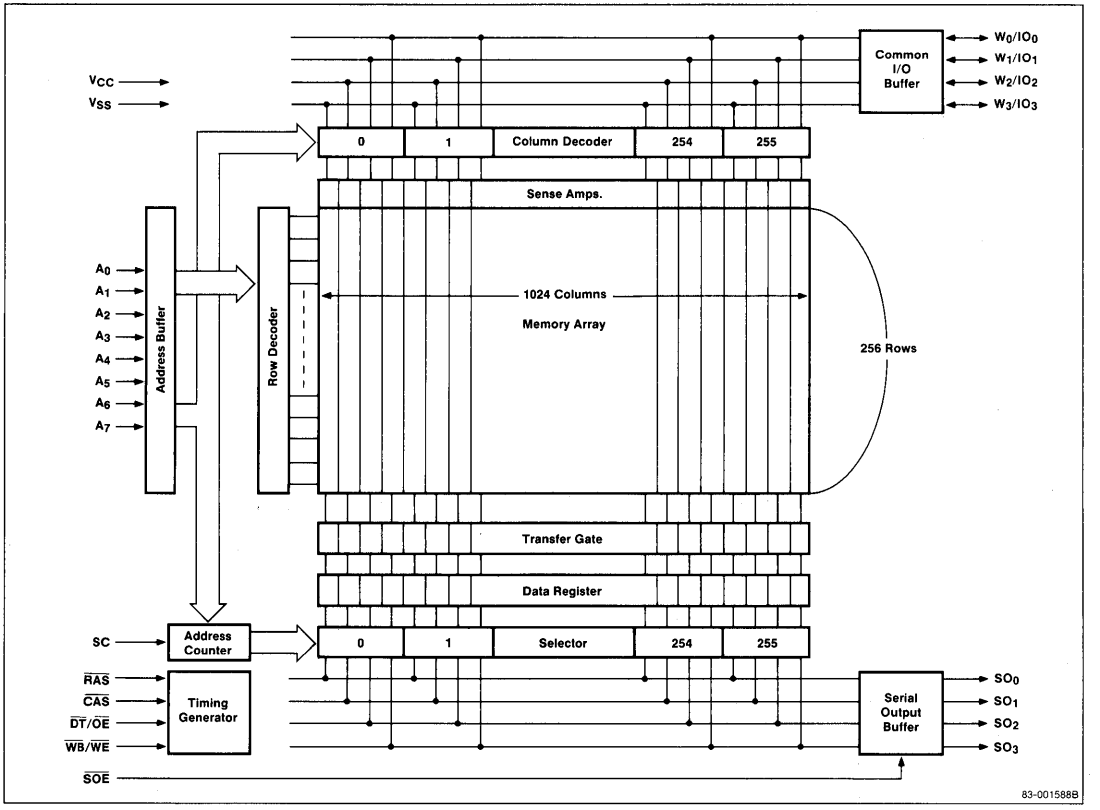
RAS access time	120 ns max
CAS access time	60 ns max
OE access time	35 ns max
RAS cycle time	230 ns max
Serial access time	40 ns max
Serial cycle time	40 ns min
SOE access time	35 ns max
Refresh	256 cycle/4 ms

Note:

(1) The cycle time in page mode is 120 ns minimum.

(2) In addition to RAS-only refresh, it is also furnished with the CAS-before-RAS refresh function.

Figure 3. Block Diagram of the Functional Interior



Three Functions Added for Ease of Use

We added three new functions to make the dual-port memory easy to use. One is the write-per-bit function, a new write mode for the random port. When this mode is used, of the 4-bit cells that can be selected during a random access mode by means of the row and column address specifications, it is possible to update the contents of any given cell in one RAS cycle. Although the cell is of a 4-bit pattern, write access is possible on a bit basis. In the areas of graphic pattern processing, there are times when the processor accesses the frame buffer(s) on bit-based units. This is a new function to address such demands.

By addition of two functions we call the pointer control function and the real-time data transfer function, we made it easy to use the serial port. When the pointer control function is used, horizontal scrolling of dots is made simpler. When the real-time data transfer function is used, it becomes possible to stop the waste of memory cells by flexibly adjusting to the display pixel patterns.

Serial Output Continues During Internal Data Transfers

Figure 6 shows timing control during internal data transfer. Just like the ordinary random access cycle, the internal data transfer cycle also begins with a timing of the falling $\overline{RAS}$ signal. Which cycle the timing belongs to is determined by the level of the data transfer control clock ($\overline{DT}$). Hence, when $\overline{DT}$ is kept at a high level during timing of the falling $\overline{RAS}$ signal, it means an ordinary random access cycle. Conversely, when the $\overline{DT}$ level is low, it means a data transfer cycle.

In the example of figure 6, a row address M is specified during the data transfer cycle. By means of this, the contents of row M are newly transferred into a data register and then output serially from the serial port. The actual operation of how the data in row M is read from the serial port is illustrated in figure 6. First, the $\overline{DT}$ signal is restored to a high level during the data transfer cycle; then data readout begins with the very first start-up timing of the SC clock.

Similarly, in order to update the contents of the data register(s), it is necessary to set up data transfer cycles using the random port control signals. During this period, only the random port is disabled from performing the ordinary random access function. However, as shown in figure 6, the functioning of the serial port can be continued without interruption. As described above, we provided a function to perform the internal data transfer while continuing the serial output. This we named the real-time data transfer function.

To accomplish the foregoing objectives, we provided only one timing rule between the SC signal, which is used by the serial port during data transfer cycles, and the data transfer clock, which is the signal from the random port side. They are shown in figure 6 as t_{SDD} and t_{SDH}. To accomplish the real-time data transfer, we introduced the restriction that both t_{SDD} and t_{SDH} be kept above 10 ns. As a method of meeting this requirement, we recommend a technique of synchronizing the timings between the start-up of $\overline{DT}$ during the data transfer cycle and the falling of SC. Since one phase period of SC is a minimum of 40 ns, even when the serial port is utilized at its maximum speed, this would allow a margin of about 10 ns for the start-up timing of $\overline{DT}$.

Owing to this real-time data transfer function, it is possible during the display to perform the internal data transfers needed to update the data within the data register(s). For this reason, it is possible to relate the data equal to one horizontal line to a plural number of lines within the memory. As a result, regardless of the pixel configuration of the display, it became possible to

Figure 4. Pin Configuration, 24-Pin Plastic DIP

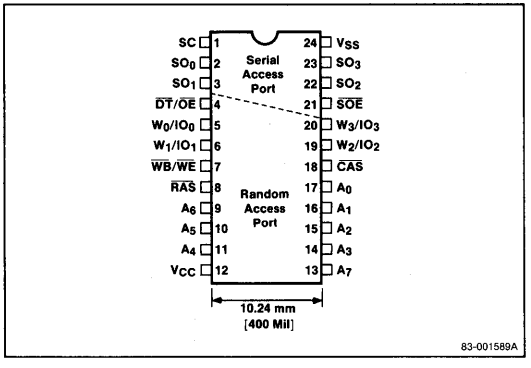
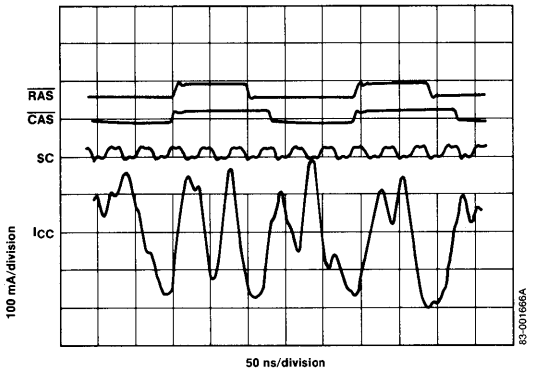


Figure 5. Source Current Waveform



make the usage efficiency of the memories making up the frame buffer(s) very close to 100 percent. It should be noted that during a data transfer cycle, the data output pin of the random port turns into a high-impedance state.

Although it is true that by virtue of the real-time data transfer function, the memory assignment can be accomplished freely regardless of the pixel configuration of a given display image, it is necessary to be careful of the refresh of the internal data register(s).

Because the serial port also consists of dynamic circuits, it is necessary to repeat the internal data transfers within a cycle period of 4 ms. During a vertical interlacing period of the display, it is always necessary to perform the internal data transfer prior to the beginning of display.

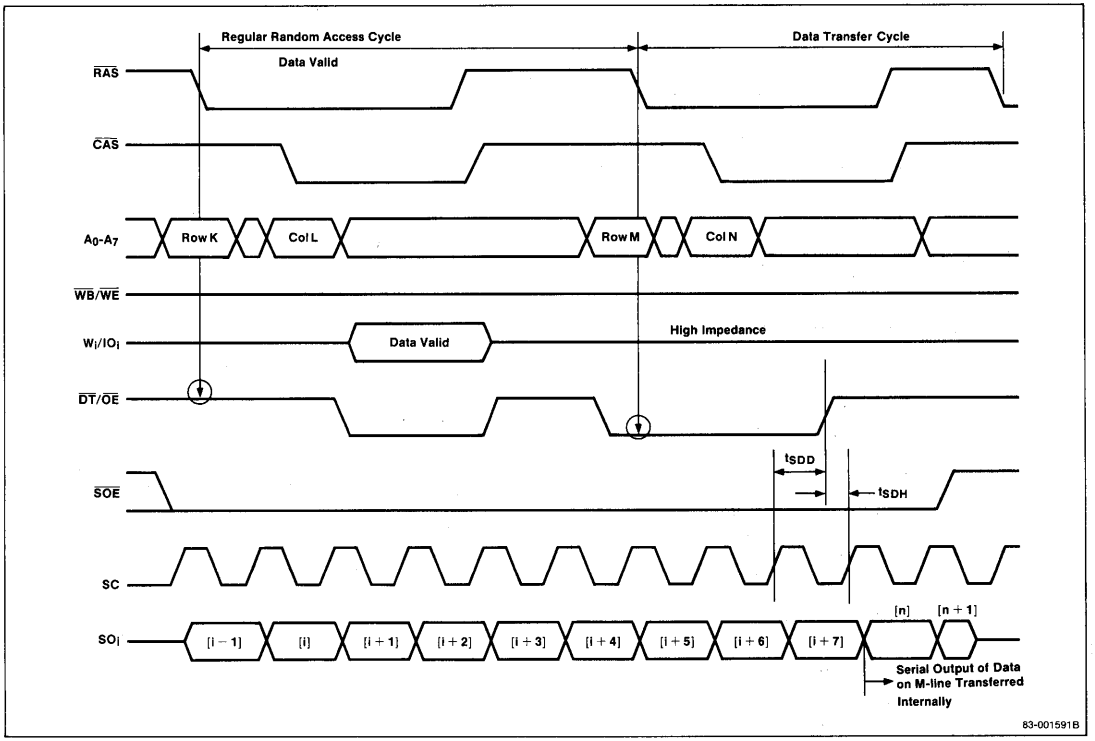
Pointer Control Function

As shown in figure 3, the serial readout port consists of the 256 x 4-bit data registers and the selector that serially selects and outputs their contents. Using such a design configuration, we made it possible to freely select the address of the data register from which to start the readout after the completion of internal data transfer(s). We call this the pointer control function.

In the timing example of figure 6, the column address N is specified by means of the $\overline{CAS}$ signal at the time of the internal data transfer. Its value determines the starting address of the data register. As shown in figure 6, it is after the $\overline{DT}$ signal is restored to the higher level during the data transfer cycle that the data in row M column N is read out by the first SC clock. Using this function, it is relatively easy to accomplish the horizontal dot scrolls.

A serial counter governs the pointer control function as shown in figure 3. This 8-bit counter counts the SC signals, and its output becomes the address of the selector, thereby serially selecting the contents of the data registers. By furnishing this counter with a control preset function and by assigning a predetermined value to it as the column address at the time of internal data transfer, we enabled it to perform the aforementioned function of determining the starting address of the selected data register. Note that the serial address counter directly counts the SC signals and that its action is not designed to be stopped by means of a serial output enable $\overline{SOE}$ signal.

Figure 6. Internal Data Transfer Timing



Write-per-Bit Function Timing

The write-per-bit function is a new random access function by which any specific memory cell can be rewritten on a bit basis in one RAS cycle, even though its design is 4-bit based.

Figure 7 shows the timing aspects of the write-per-bit function. During the falling phase of the $\overline{RAS}$ signal, if the $\overline{WB}/\overline{WE}$ signal is high level, it is the ordinary access mode, the same as conventional memories. If the $\overline{WB}/\overline{WE}$ signal level is kept low during the $\overline{RAS}$ signal falling phase, the access mode becomes the write-per-bit mode. In write-per-bit mode, to determine which of the 4-bit data terminals is to be write-enabled, mask data are input to the W_i/IO_i terminal during the $\overline{RAS}$ signal falling phase. When the level of the mask data is high, the terminal is write-enabled whereas when it is low the terminal is write-inhibited.

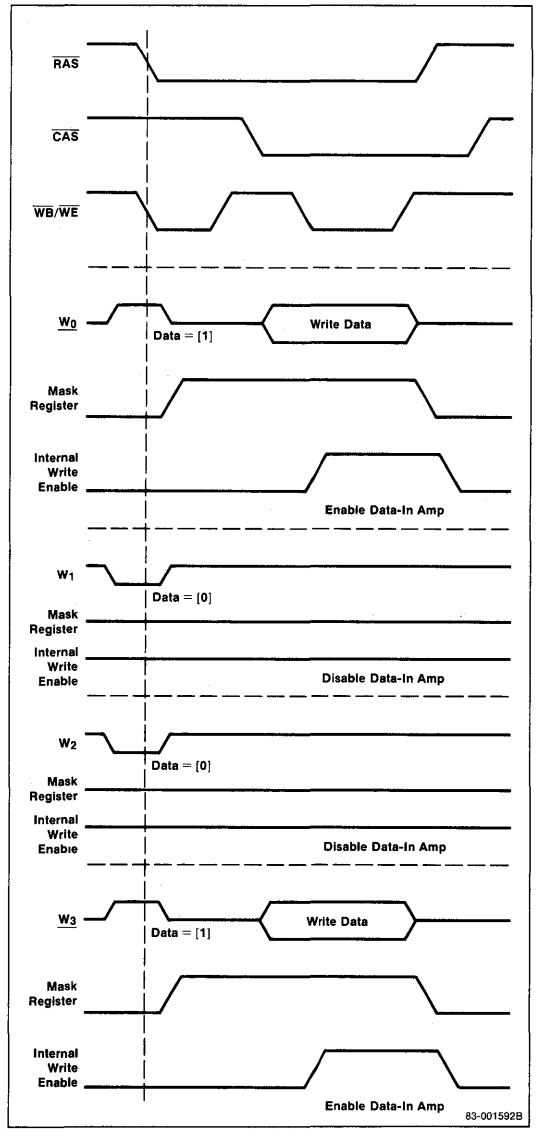
The foregoing function was accomplished by furnishing one internal circuit to determine the level of the $\overline{WB}/\overline{WE}$ signals during the $\overline{RAS}$ signal falling phase, and another to latch the determination as the mask data. This mask-data latch circuit is reset each time by means of the RAS clock. For this reason, it is necessary that the mask data be reset each time the RAS cycle takes place. In page mode, the mask data is set up in the very first RAS/CAS cycle when the mode shifts to page mode and the same value is retained so long as page mode continues. In page mode, it is not possible to update the mask data in each and every CAS cycle.

New Functions and Performance at Low Cost

When we set about developing the new memory chip, one important prerequisite was to keep the production cost as low as possible. Our market research revealed that no matter how outstanding the functions and performance, unless we keep the price at 1.2 to 1.5 times that of the conventional standard 256K-bit RAM chips, the new chip would not be accepted by a large number of users.

To achieve high access speed, there were efforts to bring in CMOS technology, which was already adopted in RAMs with static column mode.[3] At present, however, we judged that the way to realize a low-cost memory chip is undisputedly that of NMOS circuits. Consequently, we opted to adopt directly the process technology of NEC's traditional standard 256K-bit dynamic RAMs (see table 2). Since we can use the existing production line without modification, productivity can be kept at the same level as standard dynamic RAMs. If process conditions were altered, they could bring about factors that would raise costs, such as an increase in the number of masks or degradation in the flow of production lines. Against the background of such constraints, we realized the functions and performance of the new memory chip only by revising the design technology of the peripheral circuits while retaining the existing dynamic RAM as a core structure.

Figure 7. Write-per-Bit Function Timing



Chip Layout

The layout of the new memory chip is shown in figure 8. The rectangular circuit block at the left side was added for this chip. The remaining section is basically identical to the existing 64K x 4-bit dynamic RAM chip. It is characterized by a folding bit-line structure and its sense amplifier block was placed in the periphery. The row decoder, which selects bit lines, was placed in the center. The data registers, selector, and the serial I/O bus, which together compose the serial port, had to be placed close to the memory cell array.

The I/O bus and the row decoder of the random access port must be connected to the pair of bit lines connecting to the sense amplifier. Moreover, the data registers and the selector of the serial port must also be connected. While giving design priority to the serial port, which operates at a high rate of speed, we placed the row decoder in the central part of the gate arrays, a little bit separated from the sense amplifier. The serial port's circuits were placed in the outer rim of the gate arrays adjacent to the sense amplifier. Since the high-speed operating serial port becomes a major source of noise, by placing it at an outer rim we can expect to reduce the probability of transients.

Since we cannot avoid an increase in the surface displacement of the chip, the restriction in packaging was particularly severe in the shorter sides of the chip package. To prevent an increase there, dimensions of the memory cells in terms of the width and length ratio were slightly altered from that of conventional 64K x 4-bit RAMs (6 x 10 μm). The cell capacity remained the same.

Data Registers

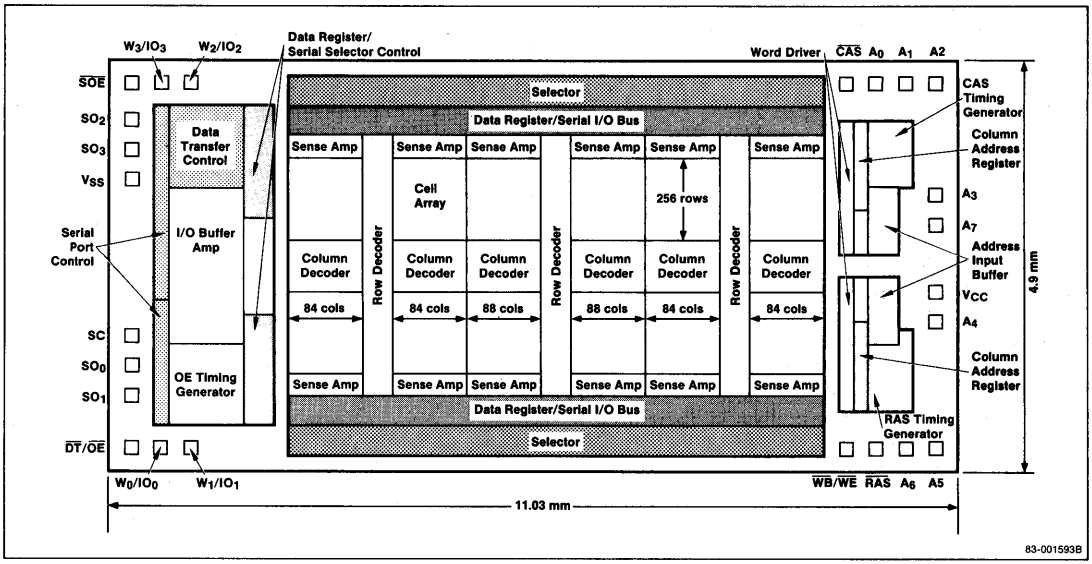
Figure 9 illustrates the architecture of circuits from the data I/O terminal of the random port I/O_i and the output terminal of the serial port SO_i to the sense amplifiers.

The two boxed-in sections indicate the data registers, which are connected to individual sense amplifiers. A set of 256 such circuits make up a serial output terminal.

The bit-line signals, which were amplified by the sense amplifiers, are sent to the serial port and the random access port. The real-time data transfer was accomplished by bypassing the data registers and providing the relay channel to send the signals amplified by the sense amplifiers directly to the serial output terminals.

The functioning of the random port is similar to that of conventional dynamic RAMs. For the serial port, the data registers read in data from the memory cells during the internal data transfer cycle and they retain the data until the next data transfer cycle. Next, the output from the data registers becomes the input to the differential amplifiers attached individually to each register. The differential amplifiers are given the enable state by means of output signals from their selector, which then sends signals to the differential amplifiers

Figure 8. Layout of the Dual-Port Memory Chip



connected to the serial output terminal. A set of 256 data registers and differential amplifiers is connected individually to each serial I/O bus depicted in figure 9. The output signals from the selector serially cause them to become enabled, hence causing the data to appear serially from the serial output terminal.

As shown in figure 9, for the data registers we adopted differential amplifiers consisting of MOS transistor pairs. Because we minimized the burden capacity of each bit-line, which would increase when the data registers were connected, the operational tolerances of the sense amplifiers did not diminish.

For the purpose of amplifying the contents of the data registers selected by the selector and to send them to the serial output terminal, static-type differential amplifiers were connected vertically. Since they operate at such a high speed as the maximum 25 MHz, no dynamic circuit can be used in this area. Hence the circuits used in the n-MOS static RAMs were adopted without modification.

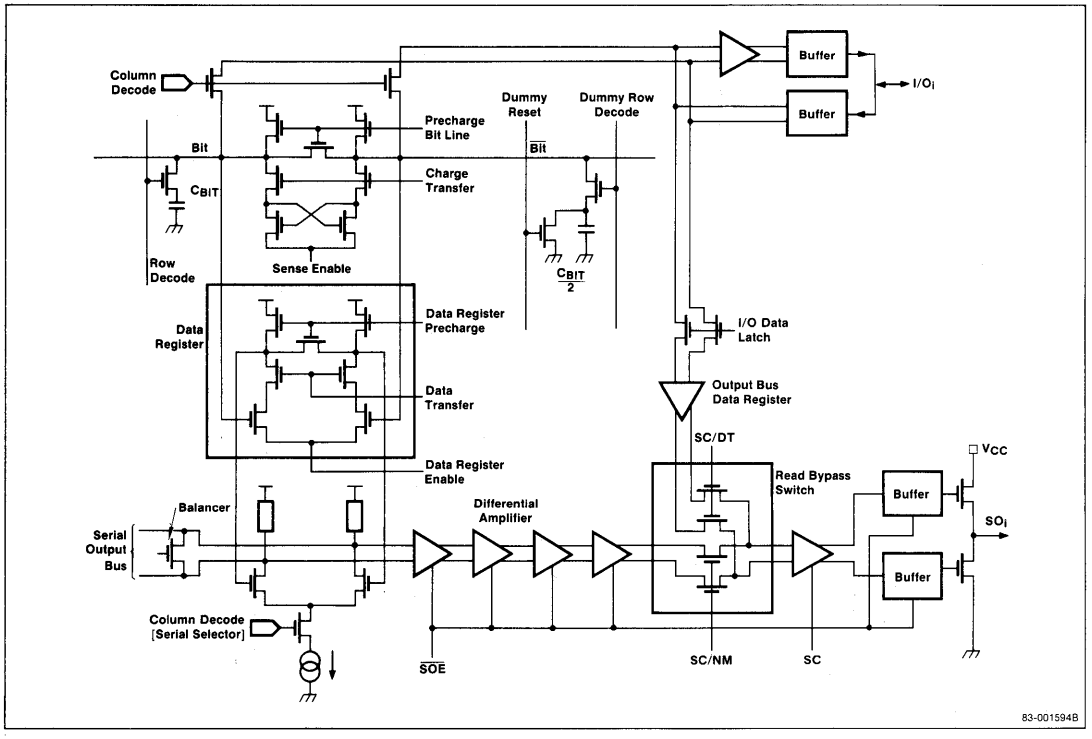
The serial port, which operates at high speed, was placed in the periphery.

Table 2. Processing Technology of the Dual-Port Memory

Polycrystalline Si gate	n-MOS process
n-MOS channel length	1.7 μm
Thickness of gate oxide Memory cell area Peripheral area	 16 nm* 40 nm
Memory cell structure	n-MOS transistor capacitor
Memory cell area	60 μm^2 [6 x 10 μm]
Chip dimensions	4.94 x 11.03 mm
Pre-charge level of bit-line	V_{CC}
Word-line level	Boosted level (higher than V_{CC}
Substrate bias generator	Internally provided

*Converted in terms of SiO_2.

Figure 9. Data Register Circuits



Internal Data Transfer Cycle

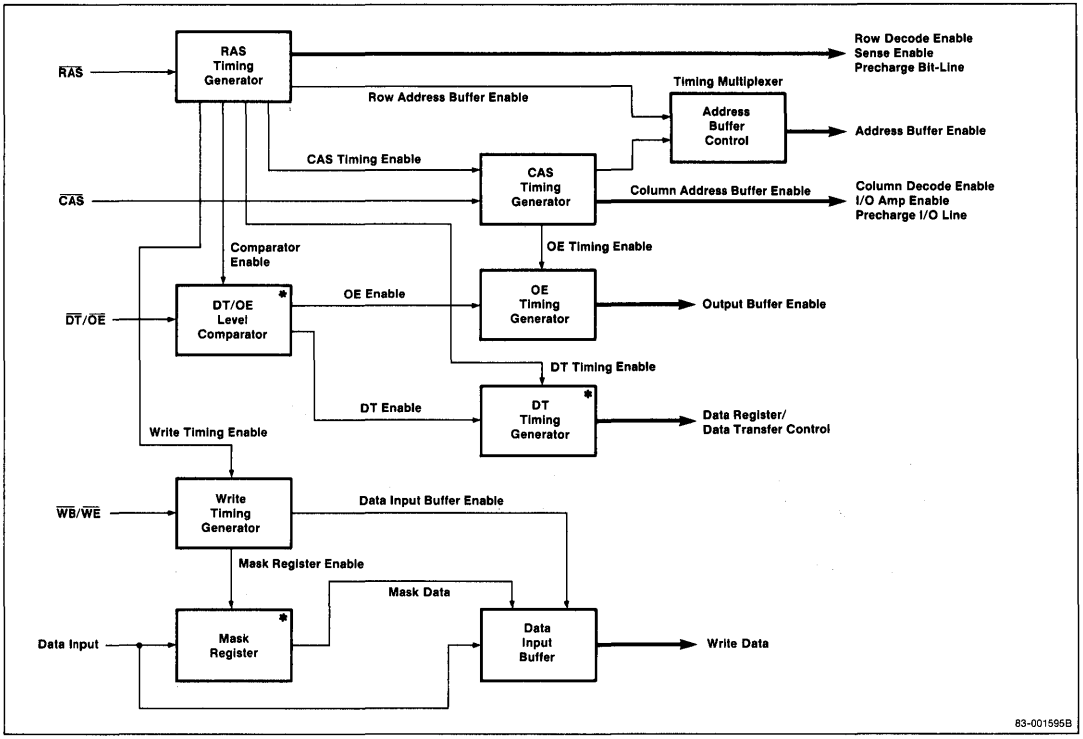
The area in figure 9 that required a significant amount of our efforts was the signal relay channel we built for the purpose of sending directly to the serial output ports the data ordinarily directed to the random port (see the right-hand side of the same figure). By bypassing the data registers, and thus taking the output from the sense amplifiers directly to the serial port, it became possible to accomplish the real-time data transfer. The internal data transfer begins with the start-up of the $\overline{DT}$ signal timing. To accomplish the real-time data transfer, the first data must be output within 10 ns of this $\overline{DT}$ start-up timing (figure 6). This operation cannot be done by ordinary procedures using the data registers. For this reason, as illustrated in figure 9, we furnished bypass channels, which were designed to output only the start-up data after the completion of the internal data transfer. In the bus architecture, as compared to ordinary access cycles, the contents of the memory cells are amplified, and they can be determined by specifying the row and column addresses. Although the data output terminal on the random port side is set to high-impedance mode during internal data transfer, its operation is identical to the ordinary readout cycles until it reaches the output buffer phase.

Figure 10 is a block diagram of the circuit to generate the timing signals for controlling the random port. The three asterisked blocks have been newly added. The DT/OE level comparator checks levels of the $\overline{DT}/\overline{OE}$ signals at the time of the $\overline{RAS}$ ascent to determine whether the data transfer or ordinary cycle is being invoked. The DT timing generator creates the internal timing signals to be used for data transfer cycles. The mask register retains mask data for write-per-bit operation.

Figure 11 shows timing of the main internal signals of the internal data transfer cycle. In order to invoke the data transfer cycle, first the $\overline{DT}/\overline{OE}$ signals are kept at a low level prior to the falling $\overline{RAS}$. Also it is necessary to keep the $\overline{DT}/\overline{OE}$ signals at a low level for at least 90 ns after the falling $\overline{RAS}$.

The DT/OE level comparator circuit shown in figure 10 detects that the $\overline{DT}/\overline{OE}$ signal level is low during the falling $\overline{RAS}$, and when the address buffer latches on the

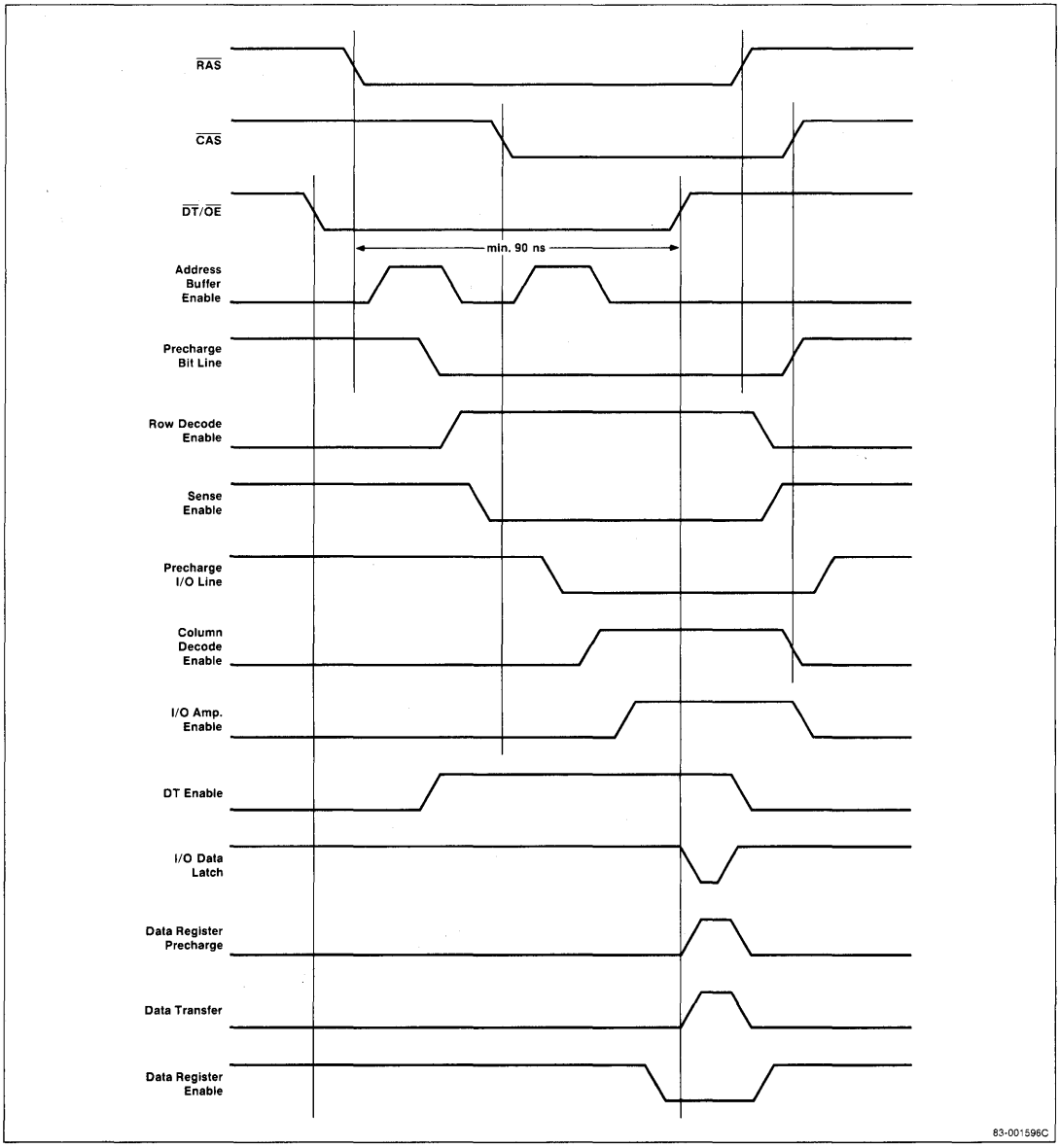
Figure 10. Block Diagram of the Timing Generator Circuit Controlling the Random Port



column address and settles its cycle action, the circuit emits the DT enable signal. Receiving this, the DT timing generator is enabled. In addition, the DT/OE level comparator controls the OE enable signals and hence turns the data output terminal of the random port into a high-impedance state. During this internal data transfer cycle, write-access to the random port becomes inhibited.

To actually transfer the data internally, the three types of internal signals that operate on the data registers are put under control (figure 9). The timing mechanism pertaining to these signals is illustrated in figure 11.

Figure 11. Timing of the Main Signals Involved in the Internal Data Transfer Cycle



First, a little before the signal to enable the I/O bus amplifier, which amplifies the signal level of the random port's I/O bus, signals are sent to enable the data registers, leaving the data registers activated beforehand. After this, when the $\overline{DT}/\overline{OE}$ signals are started up, the data register precharge signals and the data transfer signals are generated internally. This leads to intake of data by the data registers from the bit-lines. In this manner, the internal data transfer is carried out by means of the start-up timing of the $\overline{DT}/\overline{OE}$ signals.

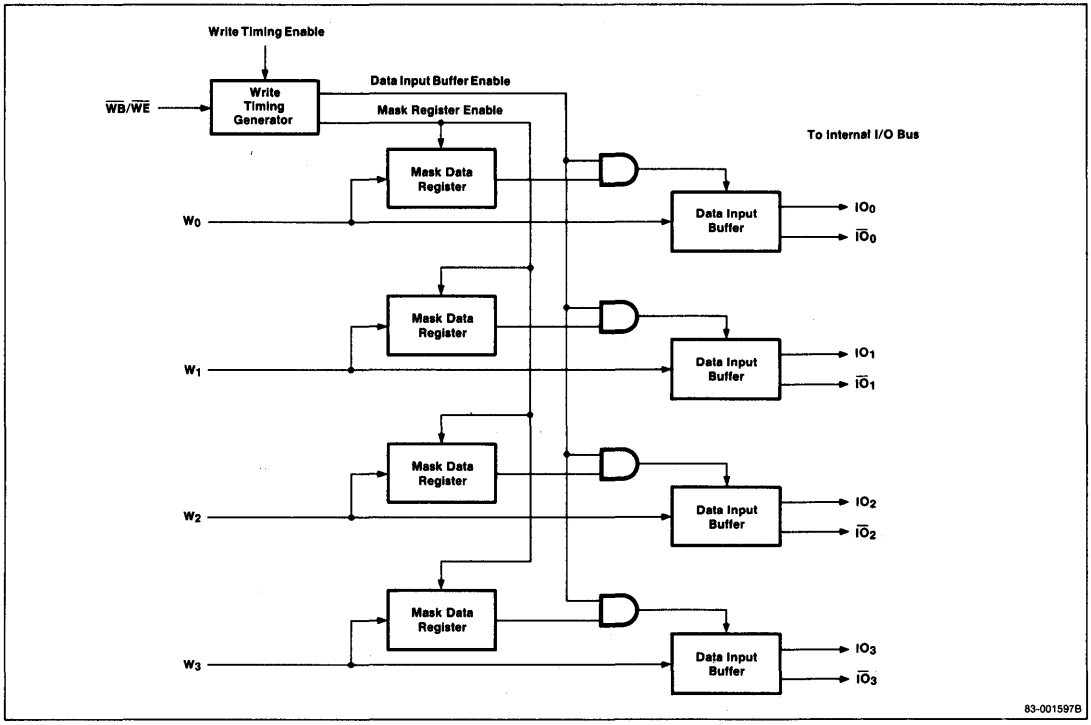
In the meantime, to accomplish the real-time data transfer function, it is necessary to guide the start-up data after data transfer through the bypass circuit as shown in figure 9. This is controlled by the output data latch signal, timing of which is shown in figure 11. This signal is also generated by means of the start-up timing of $\overline{DT}/\overline{OE}$. Using this signal, the start-up data are supplemented when they are sent to the I/O bus data registers shown in figure 9.

Write-per-Bit Circuit

Figure 12 shows a block diagram of the internal circuit that accomplishes the write-per-bit function. Its operational principle is a simple one. If the $\overline{WB}/\overline{WE}$ signal is at a low level at the time of the $\overline{RAS}$ descent, then the mask data registers are enabled and each of them latches its input signal W_i according to its own timing. The output from each mask data register controls its own data input buffer and determines whether or not to take in the data at the next write timing.

Initially, we were not thinking about this function. We assumed that the random port should be an identical design to that of conventional RAMs and proceeded with our overall design accordingly. However, when we queried our users, domestic and abroad, they asked that a write mask capability be provided. Since then we have received strong requests saying that in graphic application fields in particular this function is a necessity. Hence, as our response we added this write-per-bit function.

Figure 12. Internal Circuit of the Write-per-Bit Function



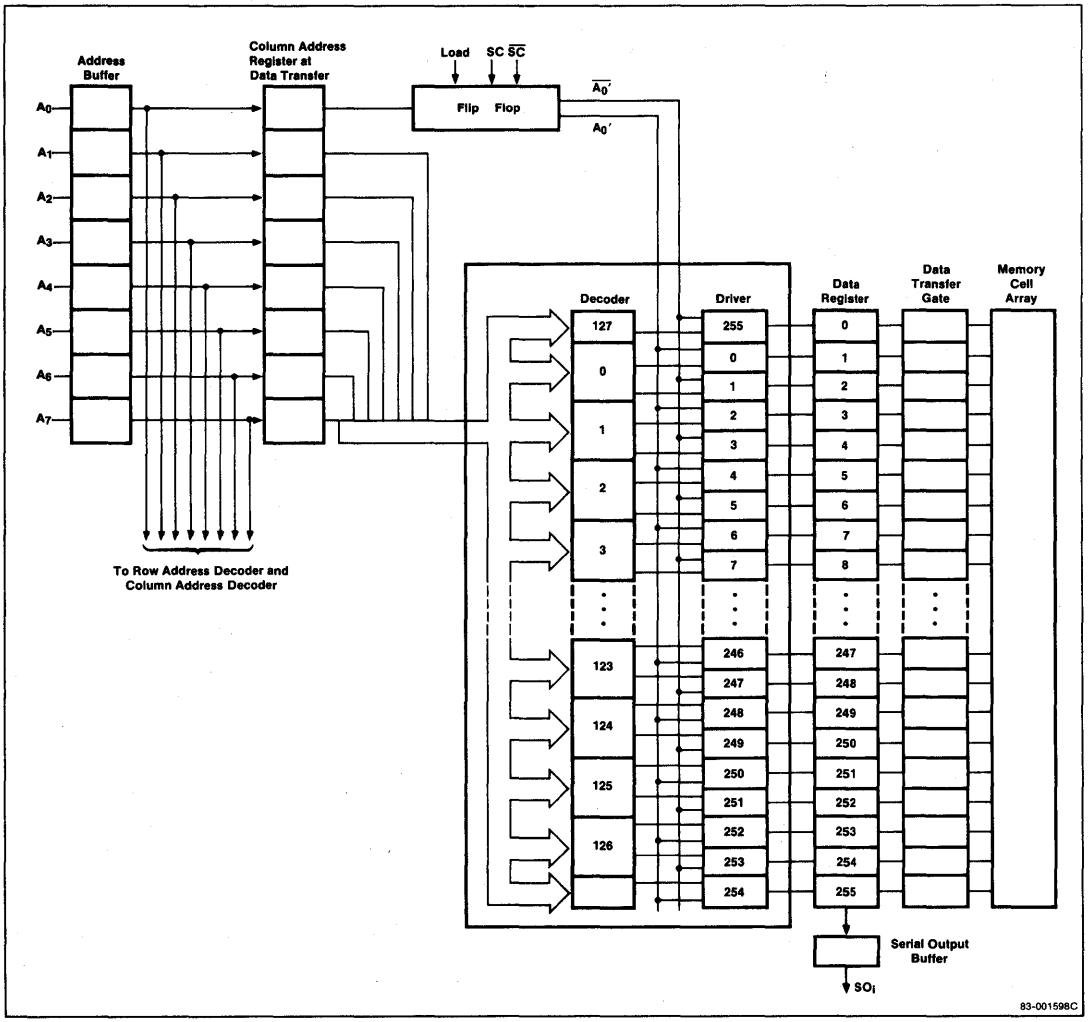
Pointer Control Function

Figure 13 is a block diagram of the internal circuit that accomplishes the pointer control function. Up to now, we have explained the serialized data output in terms of a combined functioning of the counter and a selector serially selecting the contents of the data registers. Functionally, this explanation is not wrong; however, in reality it is more contrived as shown in figure 13.

As a matter of fact, no counter is used. The row address is latched to the data transfer cycle and then decoded. As a result, of the 256 drivers shown in figure 13, only one is enabled and the contents of the corresponding data register are sent out to the serial output terminal. The decoder of figure 13 no longer gets involved in the subsequent serial operations. When the SC clock signal is received, the 256 drivers get serially enabled in a ring-register fashion and send out the data serially.

If a selector consists of a counter and a decoder, its power dissipation level gets high. This is because to operate the decoder at the maximum speed of 25 MHz, a static circuit must be adopted. Let us explain figure 13 somewhat more in detail. First, in the internal data transfer cycle, the row address is taken into the

Figure 13. Block Diagram of the Pointer Control Function



address register. Of the register outputs, A_1-A_7 get into the decoder, but A_0 only sets up staging the flip-flop for the next register action cycle. The two drivers are paired as a set and the output from the decoder enables only one such pair. The output of the flip-flop (A_0' and $\overline{A_0'}$) further selects only one pair.

The 256 drivers in figure 13 are joined together. When the SC clock signal is input, after selecting one driver using the decoder during the data transfer cycle, the drivers at the next level become enabled in a serially cascading manner. The A_0' and $\overline{A_0'}$ signals drive this mechanism.

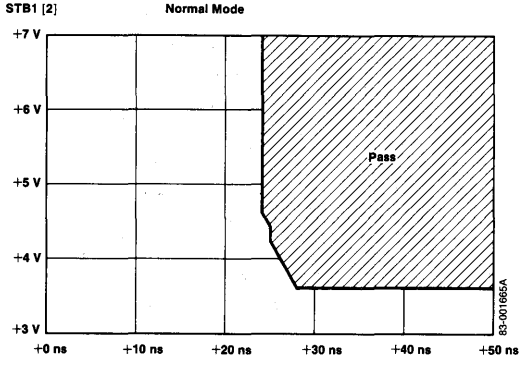
The flip-flopping output between A_0' and $\overline{A_0'}$ is controlled by the toggling operation of the falling SC clock.

As seen in figure 13, the addresses of the drivers and those of the data registers are offset by one for each of their combinations. This is because to operate them at a high rate of speed, the action of the selector and the amplification of the serial data are pipelined. By doing it this way, it was possible to take the access time of the serial port down to 25 ns in actual measurement (see figure 14).

The contents of the data register corresponding to an enabled driver appear in the serial port. For the purpose of accomplishing the pointer control function, the row address of the data transfer is input to enable a specific driver. Each of the drivers is connected together, serially enabled by the SC signals.

As explained previously, the flip-flop action is accomplished by the falling SC signals. As shown in figure 13, the output signal of the selector (that is, the driver's output in figure 13) stays more or less constant prior to start-up of the SC signal of the next cycle. In the circuit of figure 9, in the start-up timing of the SC signal, the differential amplifier attached to a particular data register is already set up in enable state. As a result, the access time measured from the start-up timing of the SC signal includes only the operational time needed to amplify the signals from the serial output bus shown in figure 9.

Figure 14. Measured Serial Output Port Access Time ($T_A = 25°C$)



Going back to figure 9, let us examine the operations of the section that amplifies and outputs data from the serial output bus. For the serial bus, a transistor or balancer is used as in static RAMs. This transistor becomes on-state when the SC signal stays at a low level, hence short-circuiting the two bus-lines. In order to speedily amplify new signals, the bus-lines need to be electrically charged to the same voltage beforehand. Simultaneously with the start-up of the SC signal, this transistor becomes off-state and the contents of the data register selected by the selector get amplified.

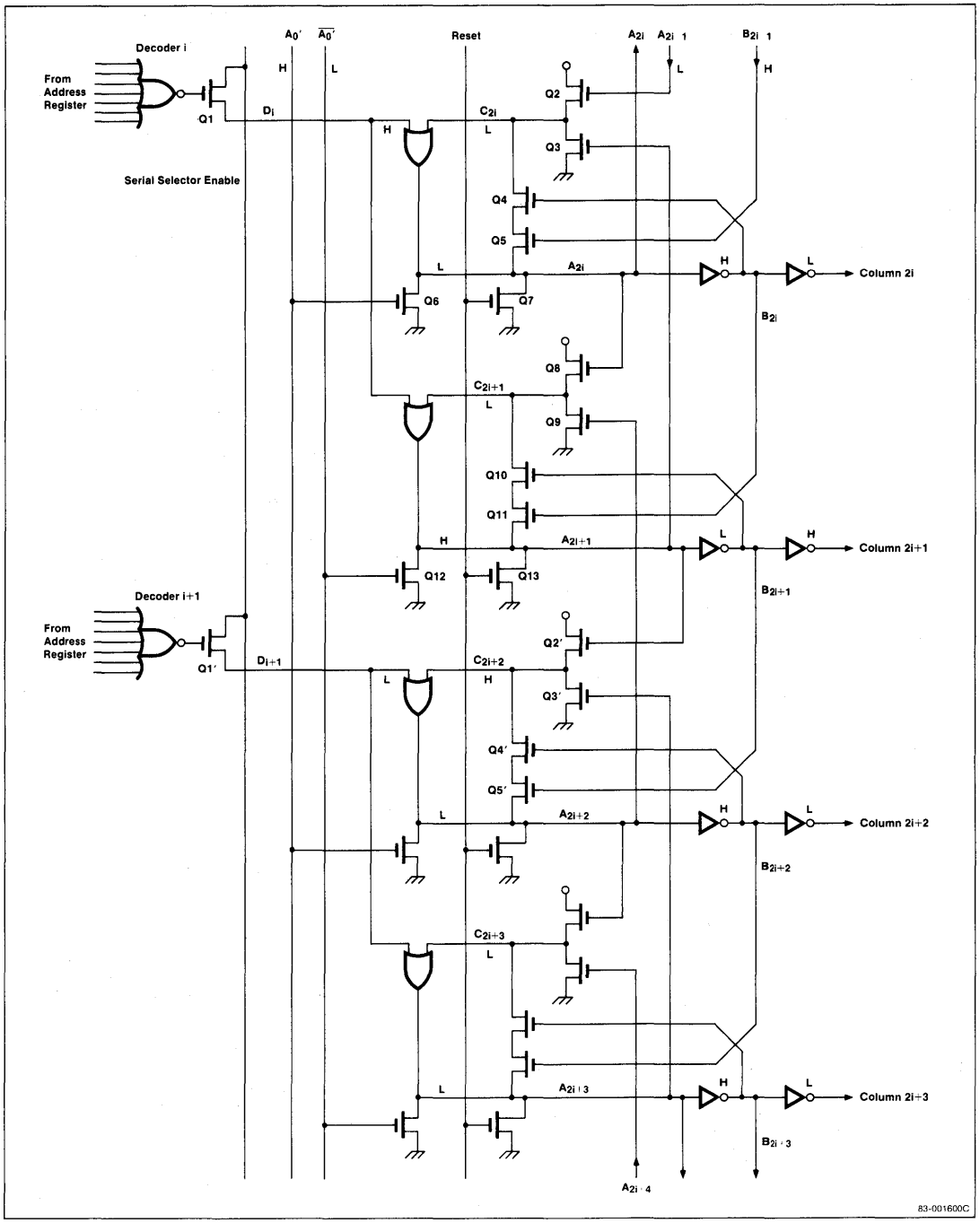
With regard to the switch to change over the readout channels, any one of the gates is "on" during the period the SC signal is at a high level. Both the SC/NM and SC/DT signals, which drive the switch, are the signals generated by the SC clock. The SC/DT signal is a signal consisting of only the SC pulse to access the beginning data after the internal data transfer. By contrast, the SC/NM signal consists of only those pulses taken from the SC clock that coincide with the SC/DT. This means that in ordinary serial cycles, the contents of the data registers are sent to the differential amplifiers in the beginning stage of the output buffer while the SC signals remain at a high level. It is only when the beginning data is accessed that the contents of the bypass channel are connected to the output terminal. In the differential amplifiers of the beginning stage of the output buffer, the $\overline{SC}$ signals, which are the inverted SC signals, are input as the enable signals. As a result, while the SC signals stay at a low level and all the changeover switches for the readout channels are "off," the previously mentioned data are kept at the output terminal.

Selector in the Pointer Control Function

In the data transfer cycles, the selector circuit of figure 13 reads in a new row address and activates the decoder circuit. For this reason, it takes longer than an ordinary selector operation. Even so, since we adopted the previously mentioned circuit design, we could leave some margin of tolerance in the selector's operation time during this phase. Because the internal serial I/O bus is shut off from the output terminal during this phase, unpredictable data cannot appear on the output terminal.

The details of the selector, consisting of decoders and drivers, are in figure 15. The figure is an excerpt showing only a portion of the 128 decoders and 256 drivers.

Figure 15. Selector Circuit Diagram



Let us start our explanation with operation of the internal data transfer cycle. Assume as given that the row address of this cycle causes the decoder (i) to be selected and that the least significant bit of the row address (A_0') is at a high level (H). First, when the $\overline{DT}$ signal of the data transfer cycle restores to H, a pulse with positive polarity is generated as a reset signal. As a result, Q7, Q13, etc. turn on and all the outputs are reset to a low level (L). After this, when a pulse with positive polarity is generated as the selector enabling signal, because the output from the decoder (i) is at H, node D_i is charged via Q1 and becomes H. The remaining 127 nodes will not get charged, since their corresponding decoders are at L. At this time, since A_0' is H, Q6 turns on and column 2i remains at L. In the meantime, since $\overline{A_0'}$ is at L, Q12 is off and column 2i+1 becomes H.

This means that immediately after the internal data transfer, only the output from driver 2i+1 becomes H. This amounts to the same operation explained in conjunction with figure 13. In figure 15, we added the signal levels at each of the locations during this phase. In this state, node C_{2i+1} is at H. This is because Q2' is on whereas Q3' is off. All nodes of the other driver circuits corresponding to C_{2i+2} are at L.

When the next SC clock signal is input from this state, column 2i+1 becomes L and column 2i+2 in turn should become H. When the SC clock is input, the flip-flop shown in figure 13 reverses and A_0' of figure 15 becomes L and $\overline{A_0'}$ becomes H. As a result, Q12 turns on, the stray capacitance at node A_{2i+1} is discharged, and column 2i+1 becomes L. In the meantime, Q5' turns off and the stray capacitance charge at node C_{2i+2} goes through the OR circuit, charging node A_{2i+2} into H level and causing column 2i+2 to become H. Similarly, when the next SC clock signal is input, column 2i+2 gets into L level, and column 2i+3 becomes H. Each time the SC clock signal is input and the flip-flop changes state, the output from the drivers changes into H in a chained series.

CPU Access to the Frame Buffer

In designing a frame buffer for graphic displays, the question of how to distribute the CPU access cycles and the data output cycles to the CRT becomes one of the keys in the system design. Typically, the conventional standard product or the single-port RAM is used. To avoid display flickers, we must resort to either the method of allowing the CPU access only during the blanking period, or the so-called cycle-stealing method. Either one of them brings about limitations in the access efficiency for the CPU. In many systems this constituted the bottleneck and the speed of refreshing the display data could not be increased. Moreover, timing their peripheral circuits would become complex.

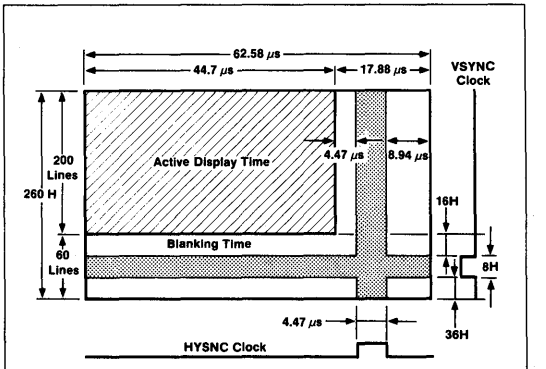
If our dual-port memory is used, it becomes possible to allow the CPU random access while display data are being output to the CRT. And the operational efficiency of the CPU is freed from the restriction of the frame buffer(s). Not only does the system design get simplified, but also, even when the display specifications are changed, it is possible for the memory's peripheral circuits to respond to the changes more easily.

There is a broad range of applications for the dual-port memory. It can be used as a general-purpose product for frame buffers ranging from low-resolution to high-resolution displays. Let us introduce here three kinds of systems utilizing this memory. First, we will describe in detail a system with a display of 320 x 200 pixels. Next, we will introduce a section that will become the key to assembling frame buffers for a 640 x 456 pixel display using one of NEC's graphic display controllers. Finally, we will describe a technique to be applied to a high-resolution display of 1280 x 1024 pixels.

A 320 x 200 Pixel Graphic Display System

Our first example is a demonstration circuit applied to a 320 x 200 pixel color graphic display system. Using the dual-port memory as the frame buffer, we created a board to directly connect to the RGB input terminal of the color display for NEC's PC-8001A personal computer.

Figure 16. Specifications of the 320 x 200 Pixel Graphic Display



Note:
[1] Horizontal display time = 44.7 μs [320 pixels]
Pixel rate = 44.7 μs/320 = 139.7 ns [7.158 MHz]
[2] Pixels in horizontal blank = 17.88 μs x 1000/139.7 ns = 128
[3] Total pixels in horizontal line = 320 + 128 = 448
[4] Pixel is derived from 2-bit P/S converter
[5] SC clock rate is one-half pixel clock rate
SC clock rate = CRTC clock rate = 3.58 MHz

83-001601A

Figure 16 shows the display specification of the PC-8001A. Since the horizontal display period is 44.7 μs, in order to display 320 pixels on one scan line, the pixel rate is 139.7 ns.

In the demonstration circuit design, the frame buffer to match such a display specification called for the mapping scheme shown in figure 17. For each corresponding RGB plane, a data bus for the 8-bit based CPU was provided. This means that in one CPU cycle, 2 bits are accessed in each RGB plane.

For the memory capacity of the frame buffer, 320 pixels x 200 pixels x 3 planes means 24,000 bytes are required. If the real-time data transfer function of the dual-port memory is used, the frame buffer can be contained within this minimum memory capacity. However, in our current configuration, we came up with the mapping scheme shown in figure 17B. That is, we used two dual-port memories and the high-order 4 bits and low-order 4 bits of the CPU data bus were connected to the respective random ports. Then, we corresponded each horizontal scanning beam to a row of the memory. This resulted in an unused residue of memories as shown in figure 17B.

It should be noted that the main emphasis of this experimental assembly was to verify the faster refresh speed of the displayed data. For this reason, our design specification was to make the internal data transfer take place only during the horizontal blanking periods and allowed the memory usage efficiency to stay less than optimum. Nevertheless, the 14K bytes of unused memory cells (worth 56 rows) were effectively utilized as part of the program area to be used by the CPU.

Block Diagram. Figure 18 is a block diagram of the demonstration circuit. For the PC-8001A color display, the horizontal sync signal (HSYNC) and the vertical sync signal (VSYNC) are synchronized with the RGB video output signals. Without receiving any external restrictions, the CPU (Z80A) executes the program written in the PROM.

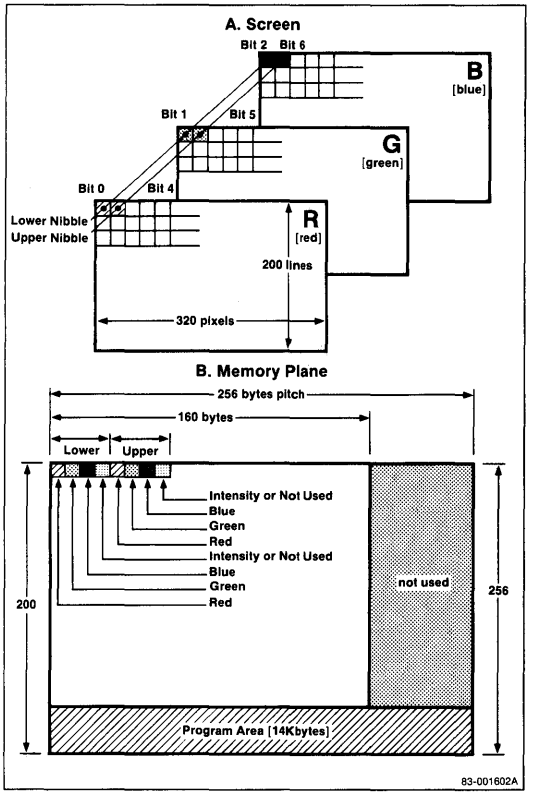
Although a CRT controller (6845) was used, it was merely a generator of the horizontal sync, vertical sync, and blanking signals. The timing generator and controller at the lower left side of figure 18 was made out of a standard TTL-type IC. The address output from the controller becomes the row address used by the dual-port memory when it internally transfers data. This address and the address sent from the CPU are multiplexed and applied to the address input of the dual-port memory, which is the frame buffer. The multiplexer also performs the time-slice selection for row and column addresses.

The frame buffer in figure 17 consists of two 256K-bit dual-port memories. The setup makes it possible to connect their random-access ports directly to the data bus of the CPU. If a single-port memory were used, a cumbersome switching circuit would be needed. The output from the frame buffer goes into three 2-bit parallel-serial converter circuits, one for each of the RGB planes, and their outputs become the video signals. For refreshing the dual-port memories, the CAS-before-RAS refresh was used. This refresh is executed during a CPU's instruction fetch cycle.

From the display specification of figure 16, the PIXEL clock that operates the parallel-serial converter circuit is 7.16 MHz. From this we can determine the frequency of the SC clock, which operates the serial port of the dual-port memory, to be 3.58 MHz. The frequency of the clock used in the 6845 CRT controller is identical. However, the timing control circuit controls the SC clock in such a way that it is stopped during the blanking period. Although there is a residual moment

3

Figure 17. Memory Mapping Scheme



of time left during the blanking period, between completion of internal data transfer by the dual-port memory and the beginning of the display, this is because the serial port is stopped during that time span. For the purpose of generating the foregoing clocking signals, a 14.318-MHz quartz oscillator was used. One advantage of a system using the dual-port memory is the ability to select the CPU clock independent of the display specifications. However, to keep the circuit simple, we chose the CPU clock also to be at 3.58 MHz.

Connection Diagram. A detailed connection diagram of our demonstration system and a photograph of its board are shown in figures 19 and 20. In addition to the CPU (Z80A), the CRT controller (6845), the PROM (27128), the two dual-port memories (41264s), the assembled unit included 25 standard TTL-type ICs. Table 3 summarizes the value settings given to the internal registers of the CRT controller. Following is a brief explanation for operation of the circuit shown in figure 19.

As can be surmised from figure 19, the timing control block of figure 18 is divided largely into four circuits: clock signal generator, DT/OE signal generator, SC clock generator, and address generation counter for data transfer.

Of these, the clock signal generator produces the clock signals needed by each of the others from a 14.318-MHz original clock oscillator. It provides 3.58-MHz clock signals to the CPU, the CRT controller, and the SC clock generator, while it outputs the 7.17-MHz PIXEL clock signals to the parallel-serial converter circuit. The $\overline{RAS}$ and $\overline{CAS}$ signals of the dual-port memory are also generated by this circuit. The $\overline{RAS}$ signal is created by adding the $\overline{MREQ}$ signal from the CPU and the $\overline{DT}$ signal from the DT/OE signal generator. To create the CAS timing of the CAS-before-RAS refresh, the $\overline{M1}$ signal from the CPU is also input. The selection signal for the multiplexer circuit to select the row and column addresses in a time-sliced fashion is also generated by means of this circuit (i.e., the A input for each multiplexer IC).

Figure 18. Block Diagram of the Circuit for a 320 x 200 Pixel Graphic Display

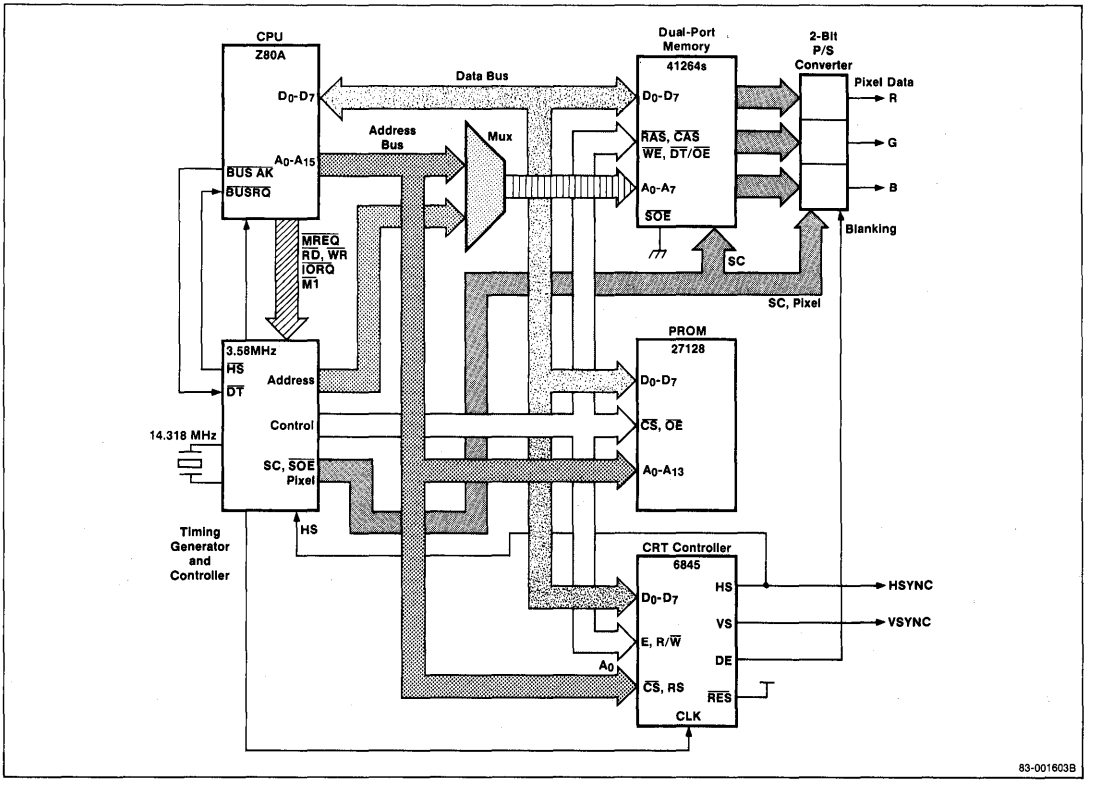
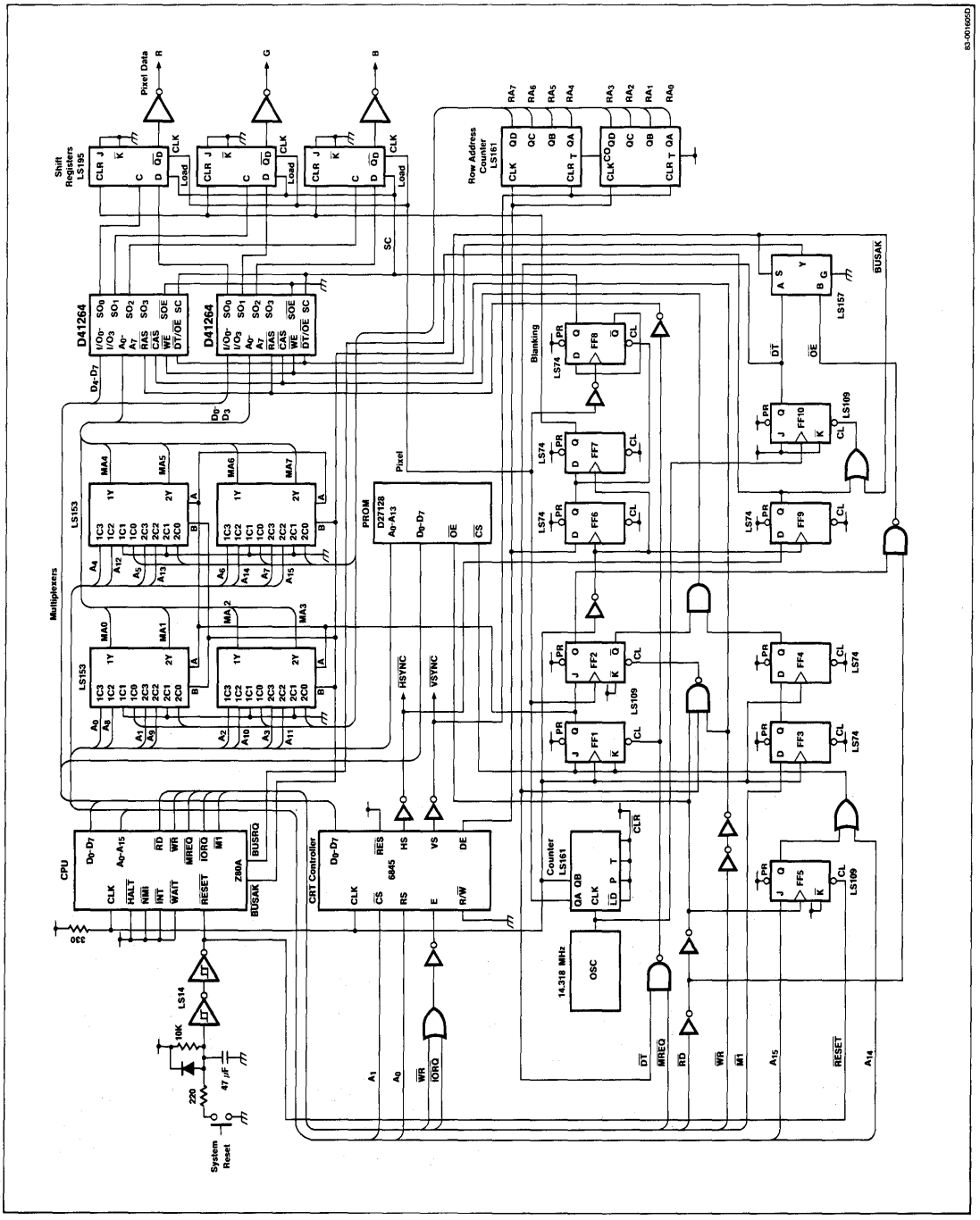


Figure 19. Connection Diagram of the 320 x 200 Pixel Graphic Display



With regard to the generator circuit of the SC clock, the 3.58-MHz clock signal from the clock generator circuit is controlled so that it is kept at a low level during the blanking period, and then is sent out to the frame buffer and the parallel-serial converter circuit.

For the circuit of our discussion here, to prevent the CPU from having access to the internal data transfer cycle of the dual-port memory, we adopted a method of inputting the $\overline{\text{BUSRQ}}$ signals to the CPU prior to each cycle. The DT/OE signal generator circuit of figure 19 produces this signal.

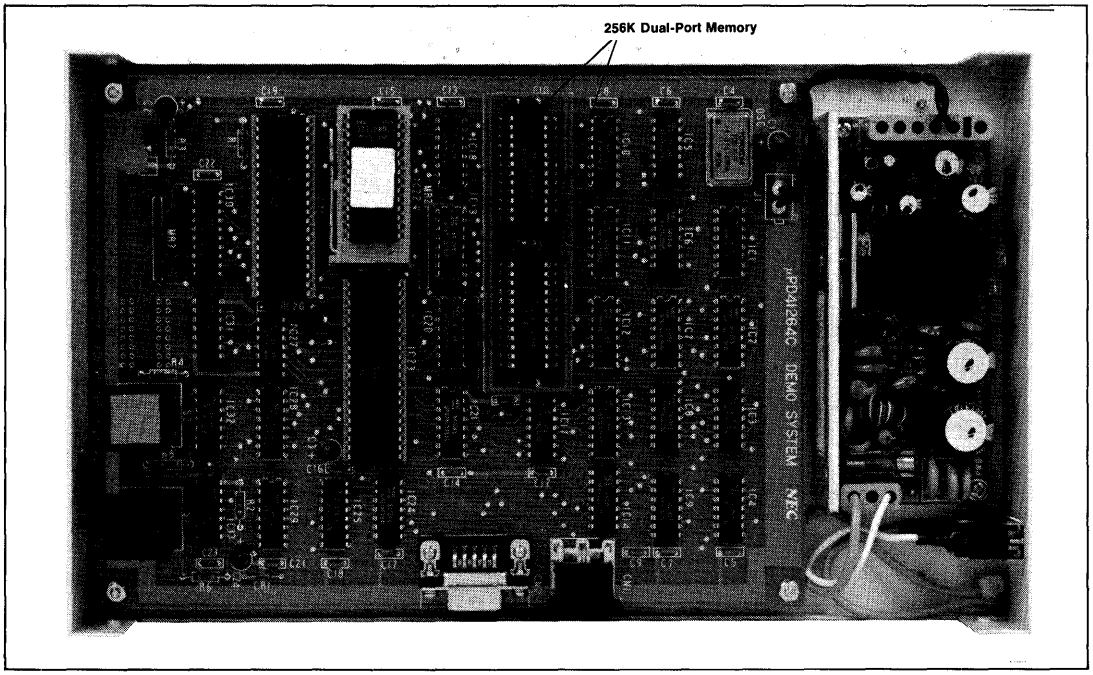
The $\overline{\text{BUSRQ}}$ signal was produced from the HSYNC signal generated by the CRT controller. When this signal is input into the CPU, the CPU returns the $\overline{\text{BUSAK}}$ signal. The DT/OE signal generator receives this signal and generates the $\overline{\text{DT}}$ signal that controls the internal data transfer.

The $\overline{\text{DT}}$ signal and the $\overline{\text{OE}}$ signal of the CPU access cycle are switched around by the selector in the final stage, and hence the $\overline{\text{DT}}/\overline{\text{OE}}$ input signal of the dual-port memory is created.

Table 3. Value Settings of CRT Controller (6845) Internal Registers

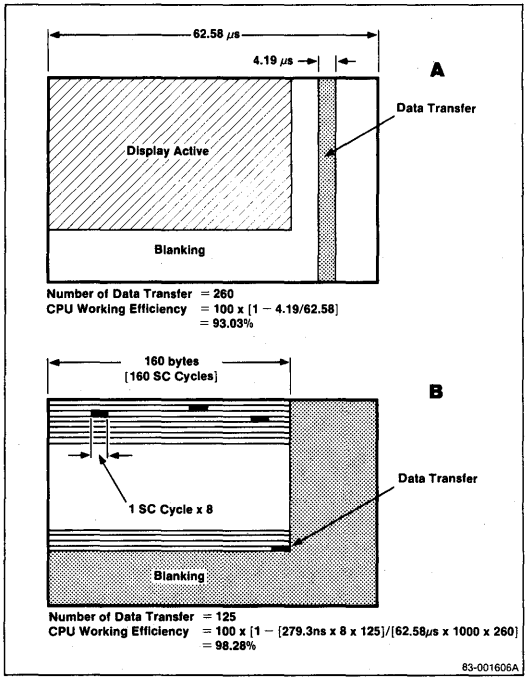
Register Number	Register Name	Setting Spec.	Set Value
R0	Number of all horizontal characters	224 characters/1H	223 = DFH
R1	Number of horizontally displayed characters	160 characters	160 = A0H
R2	Horizontally synchronous positions	180 characters	180 = 1B4H
R3	Width of horizontally synchronous pulses	15 characters	15 = 0FH
R4	Number of all vertical characters	128 rows/1V	127 = 7FH
R5	Total raster adjust horizontal characters	4 scan lines	4 = 04H
R6	Number of vertically displayed characters	100 rows	100 = 64H
R7	Vertically synchronous positions	108 rows	108 = 6CH
R8	Interlace mode	Non-interlaced	0 = 00H
R9	Maximum raster address	2 scan lines	1 = 01H
R10-R17			0 = 00H

Figure 20. Photograph of the 320 x 200 Pixel Graphic Display System Board



The row address generator counter for data transfer creates the row address for internal data transfer of the dual-port memory shown in figure 19. In this experiment, the row address of the memory was made to correspond to a horizontal scanning line of the display on a one-to-one basis and the data transfer cycle is executed during the horizontal blanking period. For this reason, the circuit of this section was simplified.

Figure 21. CPU Access Efficiency



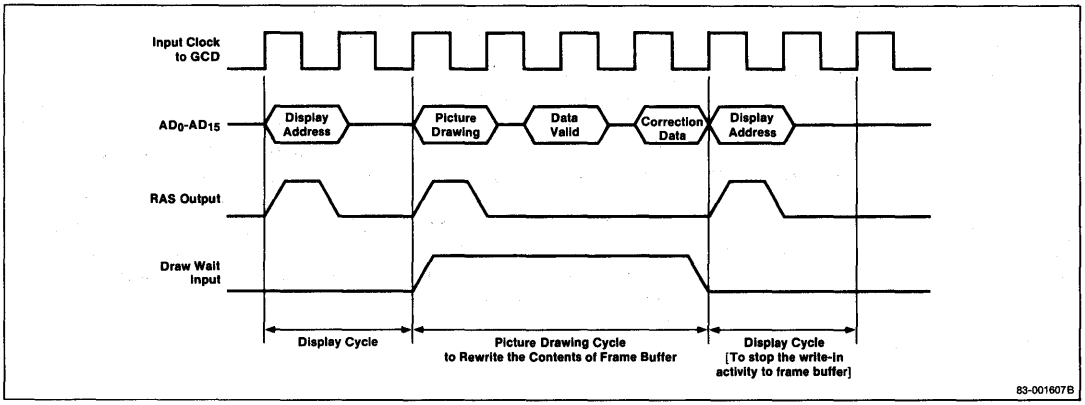
The address generator circuit for the data transfer counts the blanking signal DE, which is output from the CRT controller. The row address counters are cleared by $\overline{\text{VSYNC}}$ and their outputs sent to the multiplexer.

The multiplexer circuit of figure 19 selects the address of the dual-port memory. There are two functions involved. One is the function to select the row and column addresses in a time-sliced fashion. In this case, the function is controlled by an output from the clock signal generator circuit to the selection A input of the multiplexer ICs. The other function selects the CPU's address bus during ordinary CPU access cycles, but selects the transfer address during internal data transfer cycles. As we explained previously in connection with the DT/OE signal generator circuit, the $\overline{\text{BUSAK}}$ signal from the CPU controls this function via the selection B input to the multiplexer ICs. It should be noted that the multiplexer C1 inputs, which become the row address in internal data transfer cycles, are always low level in the demonstration circuit. If an output port is added to allow the CPU to control C1, it should become a simple task to accomplish the horizontal dot scrolling function.

Even with our demonstration circuit, in which we tried to keep the peripheral circuits as simple as possible, we could achieve an efficiency of 93.3 percent (figure 21A). If the real-time data transfer function is used effectively, it is possible to make the efficiency 98.28 percent (figure 21B).

If a signal as shown in figure 22 is input to the Draw-Wait terminal, the next cycle always becomes a display cycle. Even when the GDC is executing a graphic drawing cycle and updating the contents of the frame buffers, so long as such a signal is input from the outside, it is possible to force an interrupt in the access to frame buffers. Subsequently, the dual-port memory can execute the internal data transfer in the next cycle.

Figure 22. Draw-Wait Function Timing Diagram



Access Efficiency. Let us calculate the efficiency with which the CPU accesses the frame buffers in our demonstration circuit. As shown in figure 21A, the circuit always executes one data transfer cycle during one horizontal scanning period, including the vertical blanking period. From the figure we derive that the time ratio for the CPU to access the frame buffers is 93.30%. This value cannot be attained by means of a conventional single-port RAM.

If we can effectively use the real-time data transfer function, this value can be made even higher. As shown in figure 21B, if one row of the dual-port memory is corresponded to a display without waste, it is possible to reduce the number of data transfers for each frame to 125. If the circuit is designed so that the amount of time required for one cycle of data transfer is eight times that of the SC clock cycle, then using the calculation technique shown in figure 21B, the efficiency of the CPU access becomes 98.28%.

640 x 456 Pixel Graphic Display System

Next, we shall introduce an application example of a medium resolution system with 640 x 456 pixel display capability. For this we used an improved version of NEC's graphic display controller (GDC), μPD7220A.[14]

Draw-Wait. The improved version of the GDC was made into a product before the dual-port memory, but their development periods overlapped. For this reason, we could at least incorporate one function into the improved version of the GDC that would work in concert with the dual-port memory. This function is the Draw-Wait function. We provided a terminal (Draw-Wait) for temporarily halting externally the graphic drawing function of the GDC during its execution. In order to prevent an increase in the number of terminal ends, we piggy-backed this function with the existing light-pen input terminal. When the GDC is initialized, it is possible to decide whether this terminal is to be used for the light-pen input or the Draw-Wait input.

Referring to figure 22, when the terminal is used for the Draw-Wait input, an external signal is generated that is in sync with the GDC clock cycle and able to remain at a high level during at least four clock cycles. When the signal goes low, the GDC operates in a display cycle. This means that when the GDC executes a graphic drawing cycle and is updating the contents of the frame buffers, if an external signal is sent to the GDC (figure 22), in the next cycle the GDC halts the operation to update the frame buffers. It is possible to utilize this timing for the internal data transfer of the dual-port memory. In such an instance, it is also possible to utilize the display address output from the GDC as the pointer control address.

Flashing/Flashless Drawing Modes. Before we introduce the application example that combines the GDC and the dual-port memory, a brief explanation is in order for the graphic drawing mode of the GDC. The graphic drawing mode is divided into flashing mode and flashless mode. The flashless mode allows the graphic drawing action of the GDC only during the blanking period, whereas in the flashing mode graphic drawing can be performed even during display. Although the speed for screen display update increases in the flashing mode, in circuits using existing single-port RAMs as their frame buffers, the display is bound to incur flickering (flashing).

If the dual-port memory is used for the frame buffers, even when the GDC is in the flashing mode, there is no flickering in the display. It becomes possible to bring the drawing efficiency of the GDC close to 100 percent while keeping the display from being corrupted by flickers.

Graphic Drawing Speed. With an improved version of the GDC as the controller, and a circuit corresponding to a 640 x 456 pixel display, we examined the effect of improvements in aspects such as graphic drawing speed. The specifications of our demonstration board made it interchangeable with NEC's graphic memory board N5200 Model 05 (APC).

The N5200 Model 05 (APC) uses a 64K x 1-bit single-port RAM (μPD4164). By combining 16 such chips into a plane, and by internally assembling three planes, we made it possible to produce eight different colors at a time. Since the memory capacity of one plane is 1 megabit, the display area consisting of 640 x 456 pixels is extracted from the plane and displayed. When the dual-port memory is used in a configuration, its design architecture results in the diagram in figure 23. There, one plane consists of four chips. The random port can be directly connected to the GDC's bus. The serial port can be directly connected to the parallel-serial converter circuit. The $\overline{DT}/\overline{OE}$, SC, and $\overline{SOE}$ signals that control the dual-port memory are generated by a control circuit.

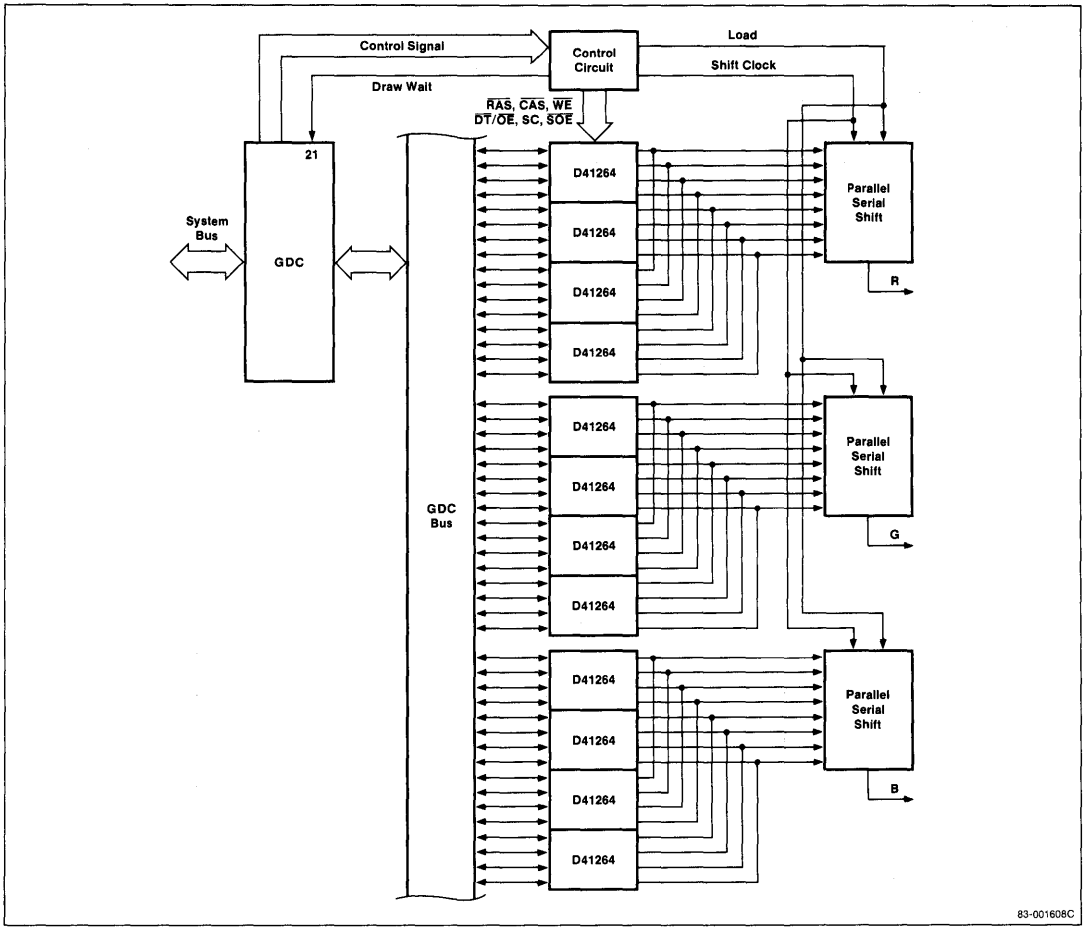
For the parallel-to-serial converter circuits, we managed with an 8-bit circuit for each plane. This was accomplished by dividing the memory chips composing a plane into two groups, and then flip-flopping the serial output enable signal $\overline{SOE}$ as the input to each group. If four kinds of $\overline{SOE}$ signals, each offset in phase by 45 degrees were generated, it would also be possible to make the parallel-to-serial conversion circuit as a 4-bit circuit.

Since the frame buffer for each plane consists of four chips, it is possible to store 4,096 bits (256 x 4 x 4) of data in the data registers within one cycle of internal data transfer. If memory and display were matched in such a way that all data in the data registers is sent to the CRT as display data, because there are 640 horizontal pixels, internal data transfer would need to be performed at an approximate rate of once per 6.4 scanning lines.

For the purpose of externally interrupting the graphic drawing operation during the period of internal data transfer of the dual-port memory, we used the Draw-Wait function of the GDC. The GDC is an improved version and operated in flashing mode.

The GDC is capable of independently establishing the virtual width of the display memory and the number of display pixels during one horizontal scanning period

Figure 23. Block Diagram of the 640 x 256 Pixel Graphic Display



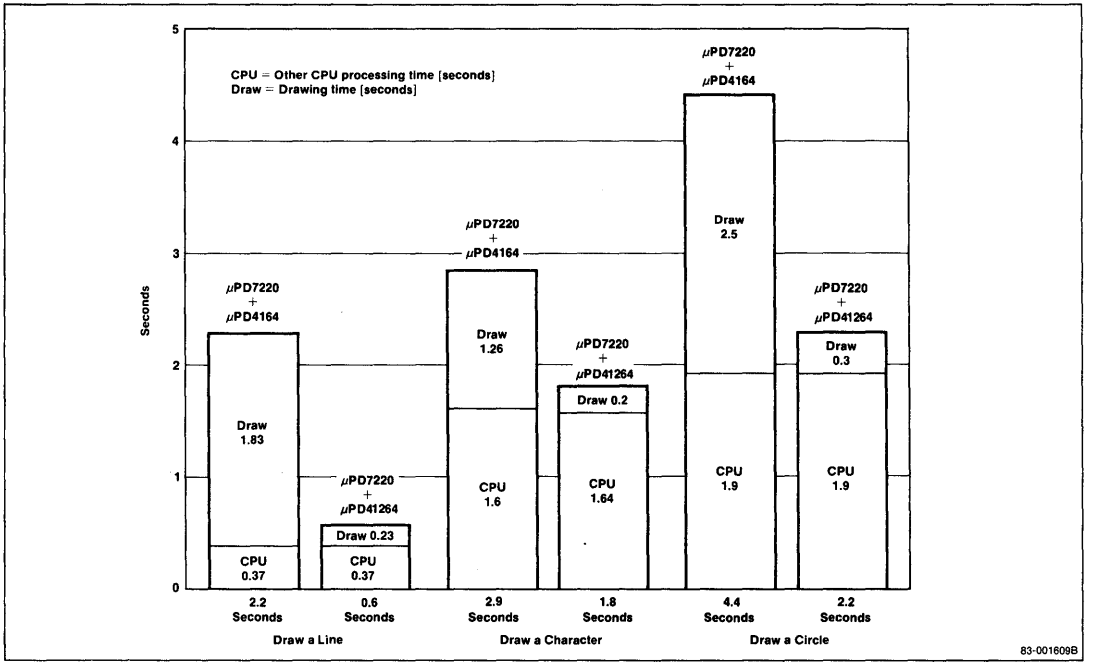
on the basis of the number of characters. There are two different cases for our consideration. In the first case, width of the memory is made larger than the number of horizontally displayed pixels. If this is done, horizontal scrolling becomes possible only by offsetting the addresses for the memory readout. Only the parts to be displayed are sent to the CRT from the contents of the data registers while the data transfer needs to be done each time a horizontal blanking period comes around.

In the second case, the width of the memory is matched against the number of horizontal pixels. This allows all data stored in the data registers to be sent to the CRT as display data. During horizontal blanking periods, the SC clock is halted, and hence the data output is halted. Timing signals will also be generated to continue internal data transfer during the display period.

By connecting the demonstration board to the N5200, we examined the results of improvement. In the N5200 Model 05 (APC), we used an 8086 microprocessor as the CPU, with the operating speed set at 5 MHz. Here, the GDC was operated in the flashless mode with a 2.5-MHz clock. Since the demonstration circuit operates the GDC in flashing mode, it is possible to update the contents of the frame buffers at a speed approximately four times as fast. Moreover, we set the GDC's clock at 5 MHz. Considering all these factors, the update speed in our demonstration circuit should be approximately eight times as fast as in traditional circuits.

Figure 24 compares processing time of a system using the existing N5200 and one using our demonstration circuit. Software to display simple lines, characters, and circles is based on graphic software GSX from Digital Research Inc. As shown in figure 24, the results reduced the total amount of time to only one-half or so. But this is because the CPU processing time for other than accesses to the frame buffers is very long. If we separate graphic drawing time from other processing time, the drawing time was shortened to between 1/6 and 1/8.

Figure 24. Comparison of Graphic Drawing Times



1280 x 1024 Pixel Graphic Display System

Finally, as an application in high-resolution display, we introduce an example of assembling the frame buffers corresponding to 1280 x 1024 pixel displays.

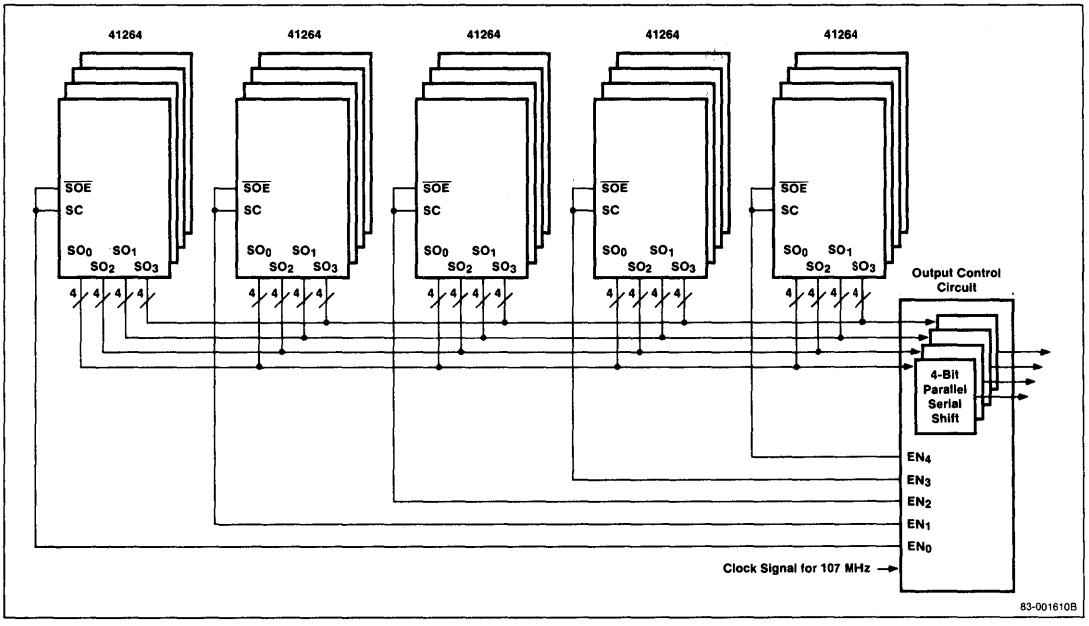
In this case, one plane consists of five packets of the dual-port memory. In order to assemble the buffer memory for four planes, 20 packets of the dual-port memory were used and they were divided into five banks, from the CPU's view. Figure 25 shows this.

For the 1280 x 1024 pixel display, it is necessary to send the display data at a cycle time of about 9.3 ns for each pixel. This means that the clock frequency cycle will be 107 MHz. In the example of figure 25, this data output requirement was accomplished by means of a 4-bit parallel-serial converter circuit for each plane. The EN_0-EN_4 symbols signify the enable signals of a 186-ns period, each with a phase offset. Using these signals, the serial port of each bank is enabled serially, hence loading the data in the 4-bit parallel-serial converter circuits. Since the serialization cycle time of the dual-port memory is 40 ns minimum, this leaves room for tolerances of other related timings. This is not the case with the traditional single-port RAMs.

In this design, it is possible to assemble the buffer memories for four planes. The parallel-to-serial converter circuits for the high-speed output of data into the display can be accomplished by a 4-bit circuit for each plane.

3

Figure 25. Frame Buffer for a 1280 x 1024 Pixel Graphic Display



Number of Product Types Will Increase

The new dual-port memory resolves almost all the problems that graphic systems designers have faced for many years. We are convinced that the three functions—real-time data transfer, pointer control, and write-per-bit—will become standard for any dual-port memory in first-generation frame buffers.[6]

Since the initial announcement, we have received much feedback from users. We have requests for even newer design specifications pertaining to power consumption, packaging, new functions, and so on.

The serial port we introduced this time adopted a static circuit. There is no denying that its power consumption level is high. In order to reduce this level, it is necessary for us to investigate new circuit technologies or introduction of the CMOS process.

The package for this product is 400 mils (10.2 mm) wide, which makes it large in comparison with traditional RAMs. Some users expressed their strong desire for a 300-mil (7.6-mm) package. For this we would need to investigate ways to introduce the processing technology used in the 1-megabit dynamic RAM, which will appear in the near future as a commercial product, and to make the packaging smaller. The idea of containing it within a PLCC is also one of our subjects for future investigation.

As new functions, we can name the serial input function as the first. This makes it possible to directly input signals from TV cameras and scanners. We can also think of its applications in the communications field. We encountered a considerable number of requests stating that even without the serial input capability, a function to simply transfer additional data internally from the data registers to the memory cell array is needed. This would make it possible to clear the memory quickly. It appears in the CAD/CAM field that this function will be a required feature. It should be noted that for the purpose of merely clearing the memory quickly, there are other techniques that should also be considered. In addition, we can think of incorporating into the chip the logical and arithmetic functions for data. In the current trend in graphic processing, the so-called raster operation function appears to be becoming standard. The arithmetic function we refer to corresponds to this trend.

It is imminent that 1-megabit dynamic RAMs will be introduced as commercial products. It should be in 1985 when each firm will introduce samples. This may spur diversification in the types of memory products. Not only in x4-bit configuration, but also in x8-bit and x16-bit configurations, we will see commercialization of the dual-port memory. For the purpose of increasing the speed of random access ports, there should be attempts made to adopt static column and/or ripple modes in such products.

Acknowledgment

In acknowledgment, we would like to mention that the dual-port memory was developed by the joint efforts of many people, headed by Mr. Shoji Ishimoto. For the creation of this paper, we received advice on many occasions from them. We would like to express our deep sense of appreciation to all those who were involved.

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NEC

DYNAMIC RAM MODULES

4

Section 4 — Dynamic RAM Modules

NEC Electronics Inc.

MC-41256A4
262,144 x 4-BIT
DYNAMIC NMOS RAM MODULE

PRELIMINARY INFORMATON

Description

The MC-41256A4 is a 262,144-word by 4-bit NMOS dynamic RAM module, designed to operate from a single +5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

The MC-41256A4 operates like four μPD41256 standard 256K DRAMs. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes four μPD41256s in PLCC packages and two power supply decoupling capacitors.

SIMM is a trade mark of Wang Laboratories.

Features

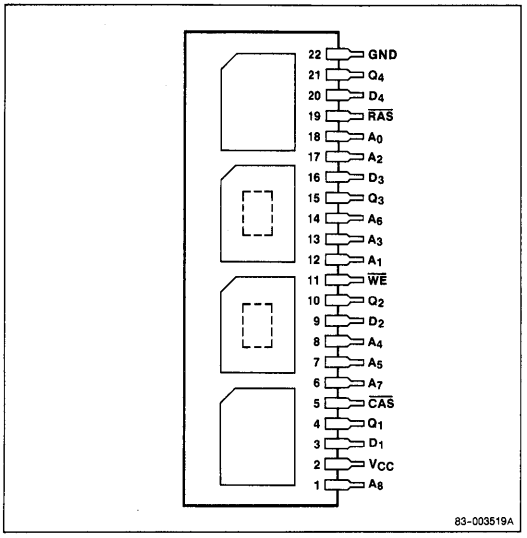
- ☐ 262,144-word by 4-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 22-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates four 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 110 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

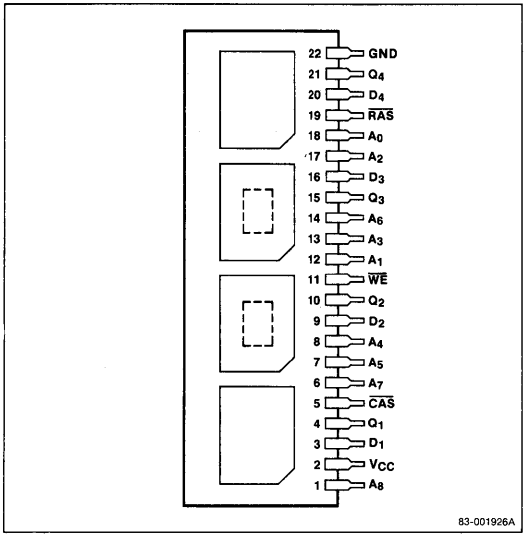
Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-41256A4-12	120 ns	220 ns	120 ns
MC-41256A4-15	150 ns	260 ns	145 ns

Pin Configuration

22-Pin SIMM, MC-41256A4A
(Glass-epoxy Substrate)



22-Pin SIMM, MC-41256A4C
(Ceramic Substrate)



4

Pin Identification

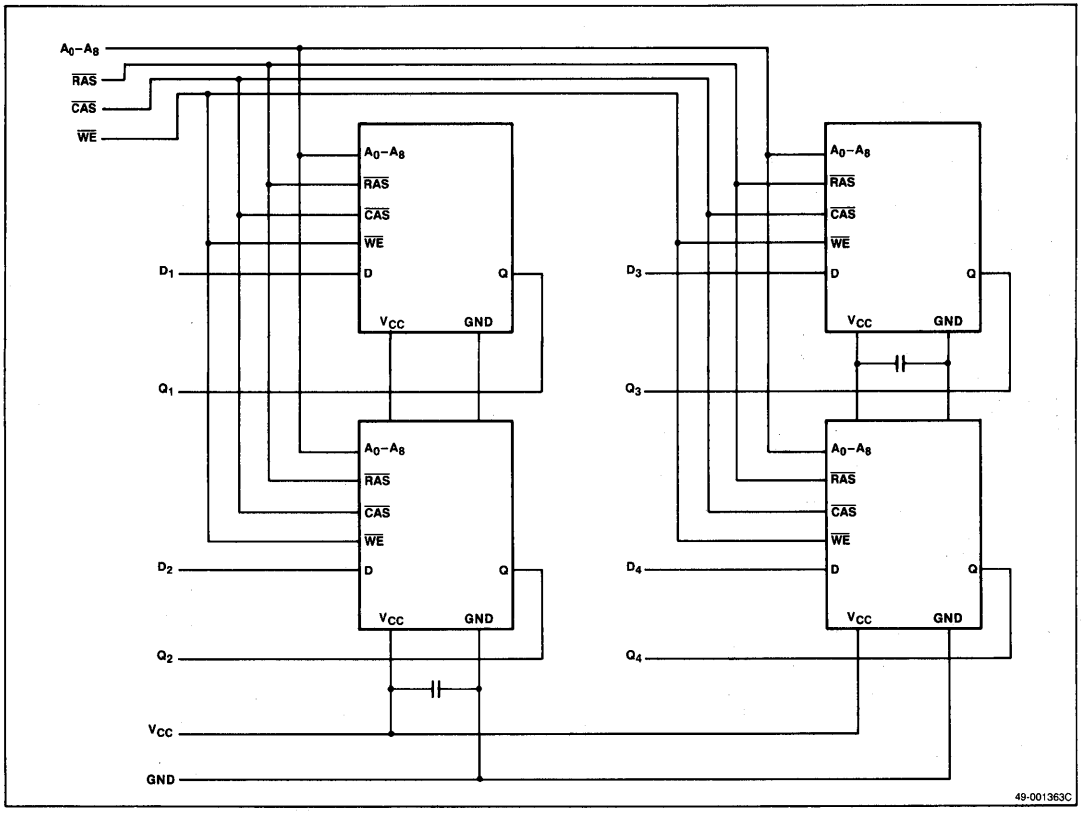
No.	Symbol	Function
1, 6-8, 12-14, 17, 18	A_0-A_8	Address inputs
2	V_{CC}	Power supply (+5.0 V)
3, 9, 16, 20	D_1-D_4	Data inputs
4, 10, 15, 21	Q_1-Q_4	Data outputs
5	$\overline{CAS}$	Column address strobe
11	$\overline{WE}$	Write enable
19	$\overline{RAS}$	Row address strobe
22	GND	Ground

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +85°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	4.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			40	pF	A_0-A_8
Input capacitance	C_{IR}			50	pF	$\overline{RAS}$, $\overline{WE}$
Input capacitance	C_{IC}			50	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}			15	pF	D_1-D_4, Q_1-Q_4 (Note 1)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			20.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−40		40	μA	For A_0-A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Data input leakage current	$I_{IL(D)}$	−10		10	μA	For D_1-D_4; V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A4-12 Min	Max	MC-41256A4-15 Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		332		280	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min (Note 5)
Operating current, refresh mode, average	I_{CC3}		260		212	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min (Note 5)
Operating current, page mode, average	I_{CC4}		180		140	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		270		225	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IL}, t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	

4

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A4-12 Min	MC-41256A4-12 Max	MC-41256A4-15 Min	MC-41256A4-15 Max	Unit	Test Conditions
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 16)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

AC Characteristics (cont)

Note [cont]:

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

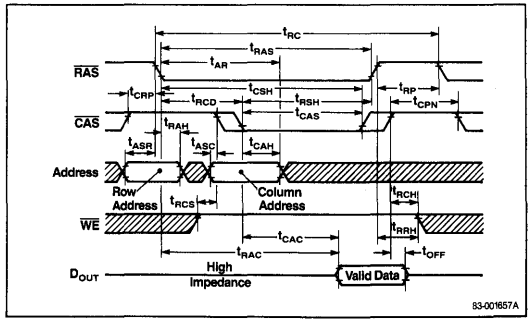
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

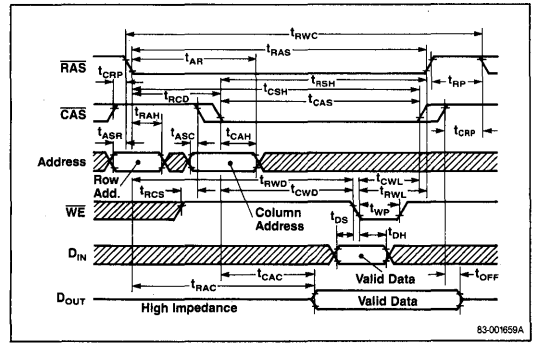
(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

Timing Waveforms

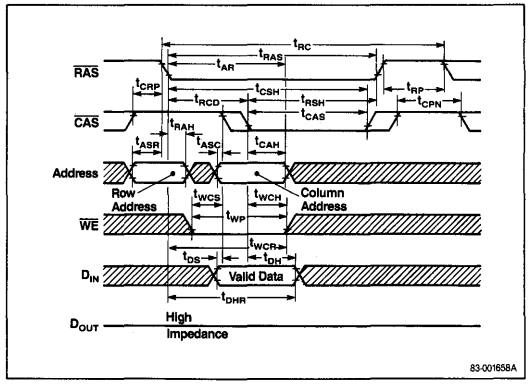
Read Cycle



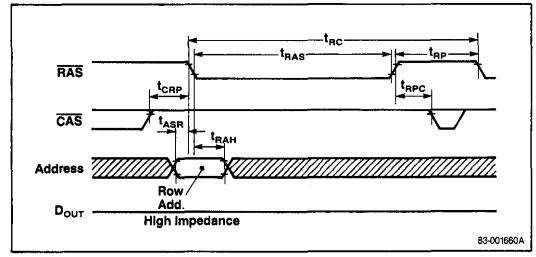
Read-Write/Read-Modify-Write Cycle



Write Cycle (Early Write)



RAS-Only Refresh Cycle



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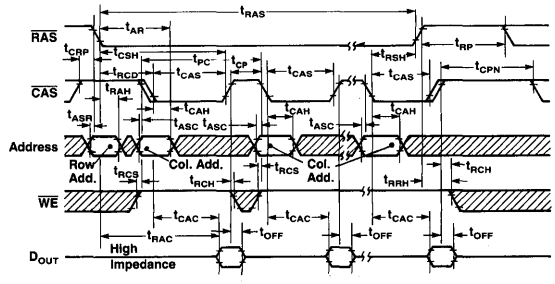
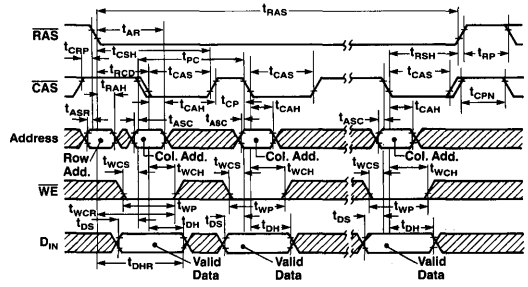
Timing Waveforms (cont)

Page Mode Read Cycle



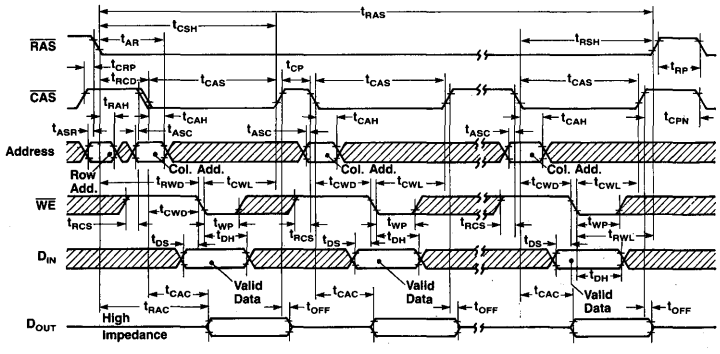
83-001661B

Page Mode Write Cycle (Early Write)



83-001662B

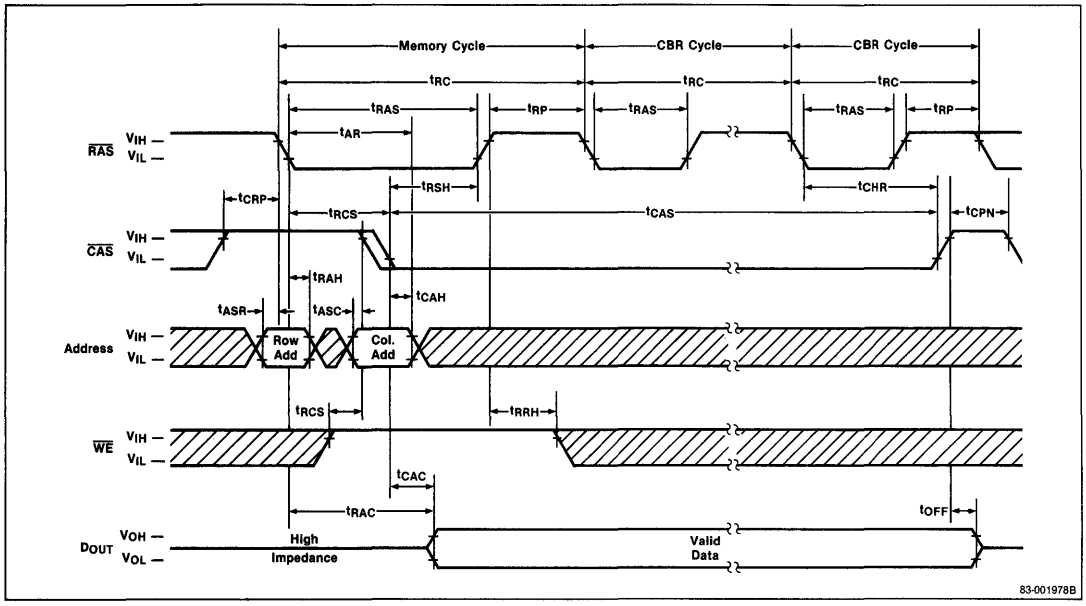
Page Mode Read-Write/Read-Modify-Write Cycle



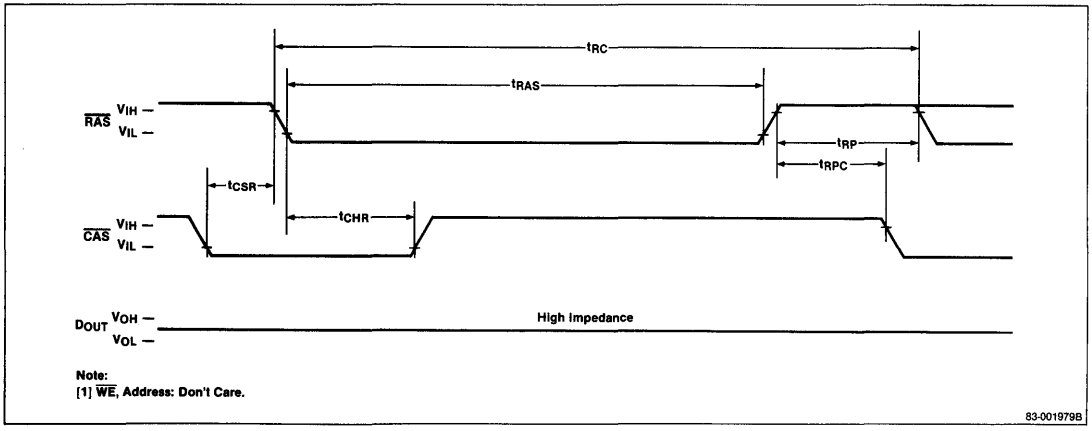
83-001664B

Timing Waveforms (cont)

Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

4

NEC

NEC Electronics Inc.

MC-41256A5
262,144 x 5-BIT
DYNAMIC NMOS RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-41256A5 is a 262,144-word by 5-bit NMOS dynamic RAM module, designed to operate from a single +5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

The MC-41256A5 operates like five μPD41256 standard 256K DRAMs. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes five μPD41256s in PLCC packages and two power supply decoupling capacitors.

SIMM is a trade mark of Wang Laboratories.

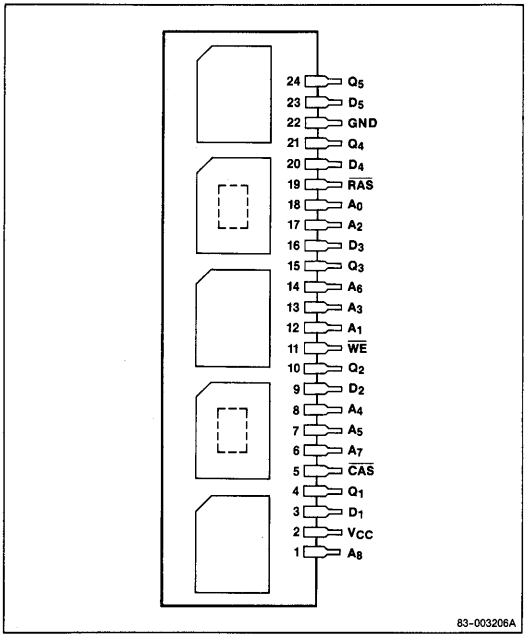
Features

- ☐ 262,144-word by 5-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 24-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates five 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 138 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-41256A5-12	120 ns	220 ns	120 ns
MC-41256A5-15	150 ns	260 ns	145 ns

Pin Configuration

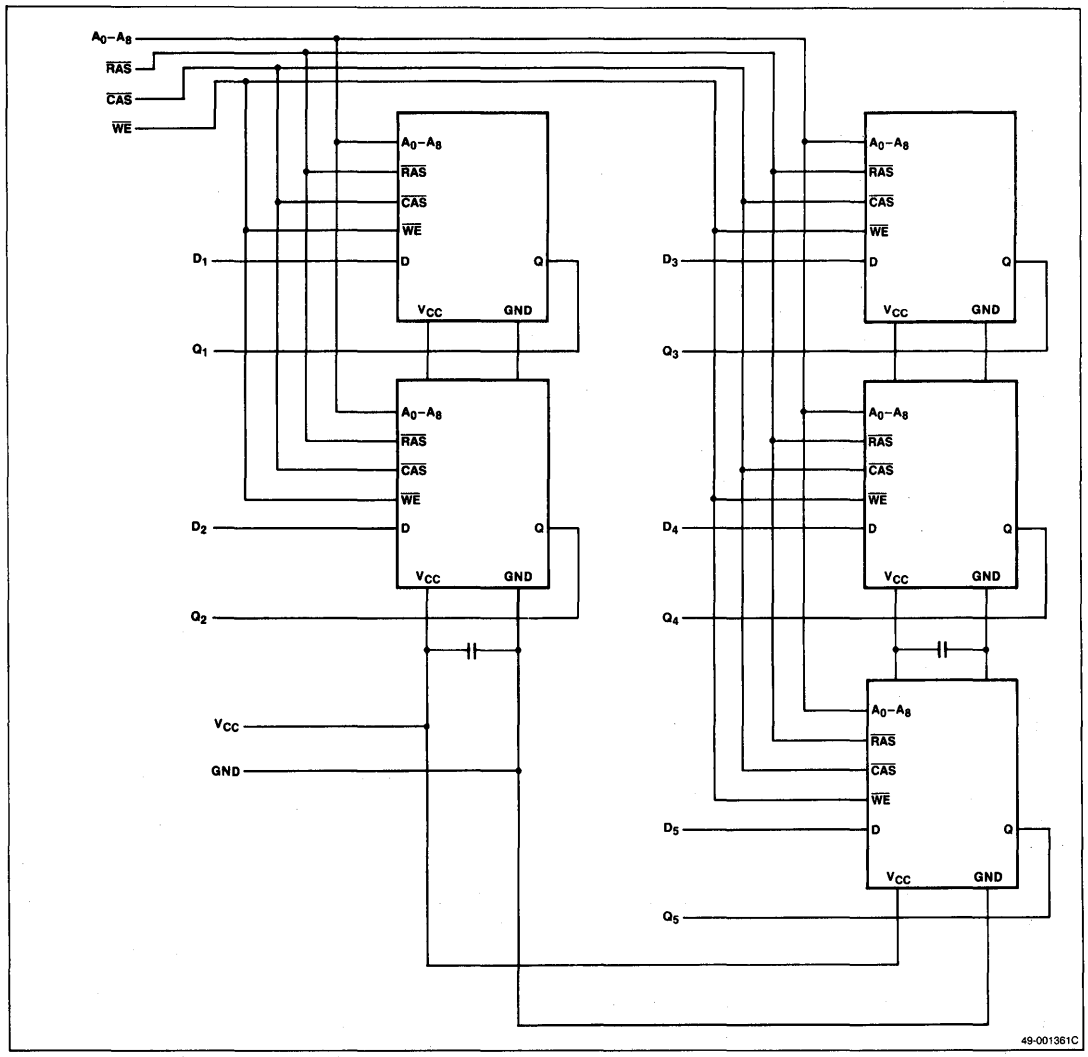


Pin Identification

No.	Symbol	Function
1, 6-8, 12-14, 17, 18	A_0-A_8	Address inputs
2	V_{CC}	Power supply (+5.0 V)
3, 9, 16, 20, 23	D_1-D_5	Data inputs
4, 10, 15, 21, 24	Q_1-Q_5	Data outputs
5	$\overline{CAS}$	Column address strobe
11	$\overline{WE}$	Write enable
19	$\overline{RAS}$	Row address strobe
22	GND	Ground

4

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +85°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	5.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			45	pF	A_0-A_8
Input capacitance	C_{IR}			55	pF	$\overline{RAS}$, $\overline{WE}$
Input capacitance	C_{IC}			55	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}			15	pF	D_1-D_5, Q_1-Q_5 (Note 1)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			25.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−50		50	μA	For A_0-A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Data input leakage current	$I_{IL(D)}$	−10		10	μA	For D_1-D_5; V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A5-12 Min	MC-41256A5-12 Max	MC-41256A5-15 Min	MC-41256A5-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		415		350	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh mode, average	I_{CC3}		325		265	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page mode, average	I_{CC4}		225		175	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		340		280	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IL}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	

AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	MC-41256A5-12 Min	MC-41256A5-12 Max	MC-41256A5-15 Min	MC-41256A5-15 Max	Unit	Test Conditions
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 16)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

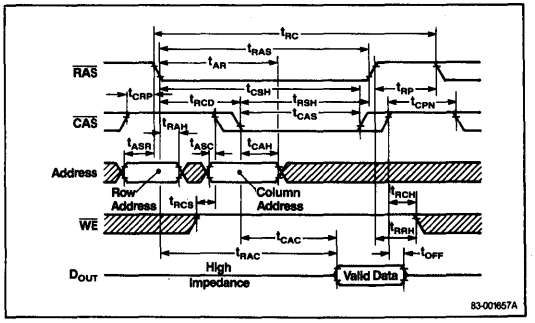
(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

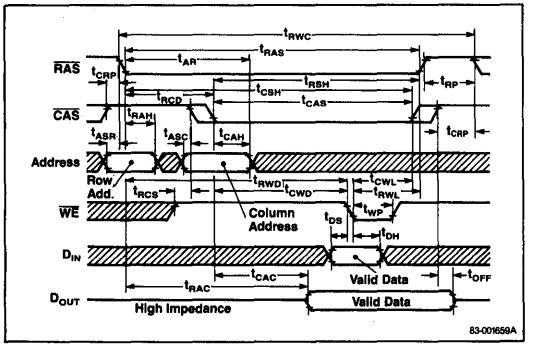
4

Timing Waveforms

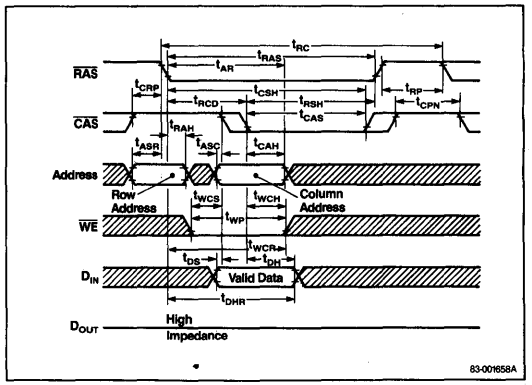
Read Cycle



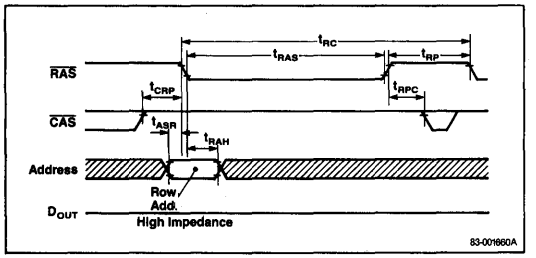
Read-Write/Read-Modify-Write Cycle



Write Cycle (Early Write)

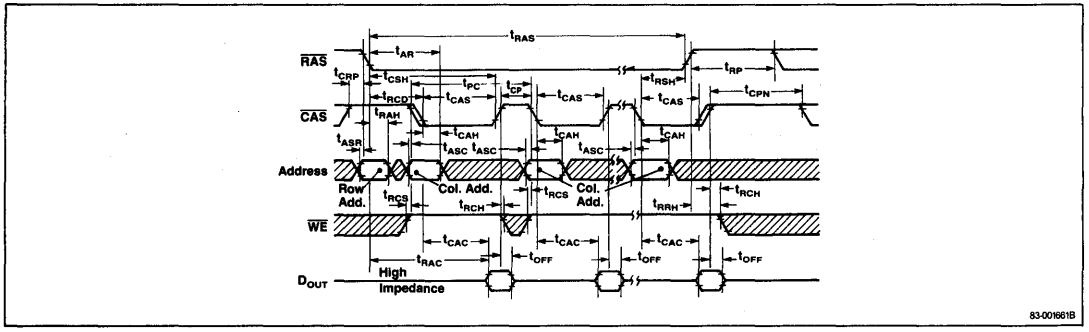


RAS-Only Refresh Cycle

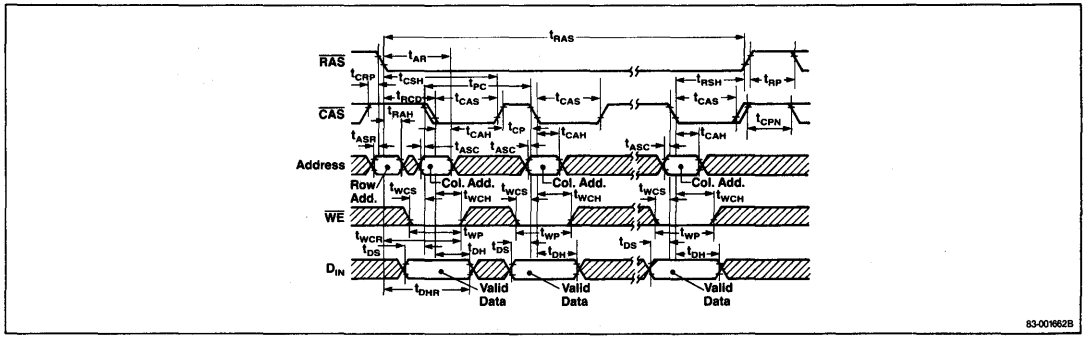


Timing Waveforms (cont)

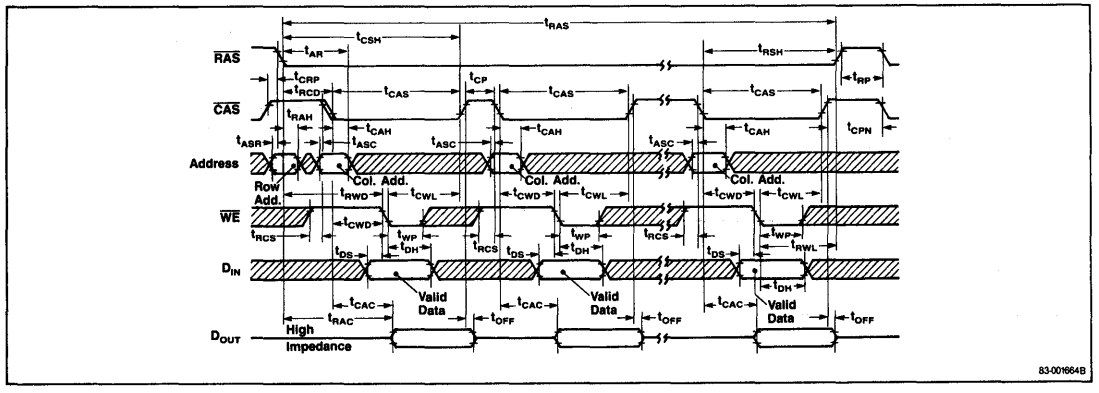
Page Mode Read Cycle



Page Mode Write Cycle (Early Write)

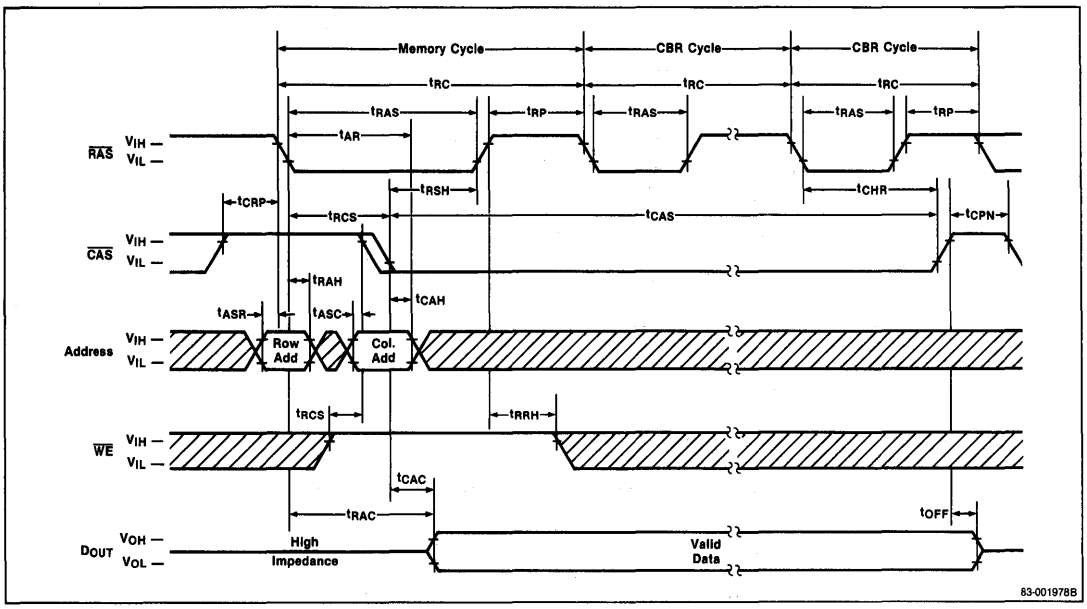


Page Mode Read-Write/Read-Modify-Write Cycle

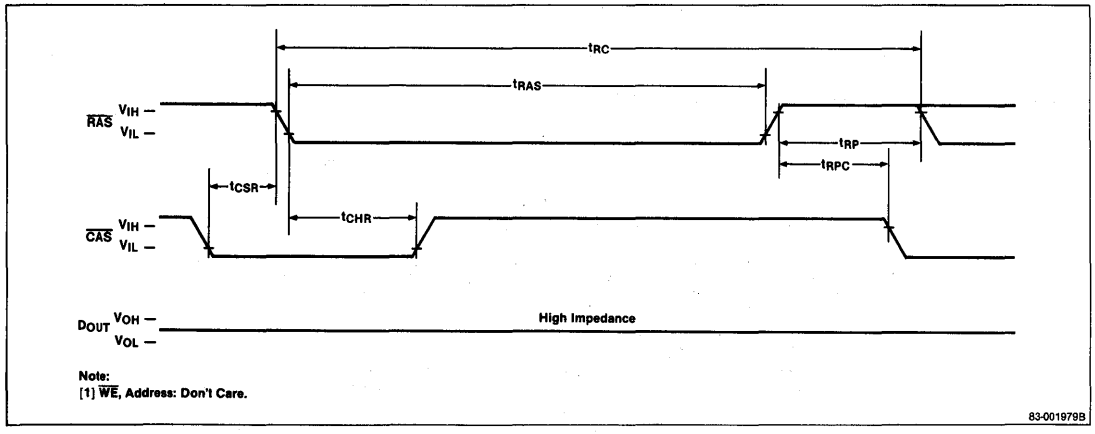


Timing Waveforms (cont)

Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



NEC
NEC Electronics Inc.

MC-41256A8
262,144 x 8-BIT
DYNAMIC NMOS RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-41256A8 is a 262,144-word by 8-bit NMOS dynamic RAM module, designed to operate from a single +5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

The MC-41256A8 operates like eight μPD41256 standard 256K DRAMs. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes eight μPD41256s in PLCC packages and eight power supply decoupling capacitors.

SIMM is a trade mark of Wang Laboratories.

Features

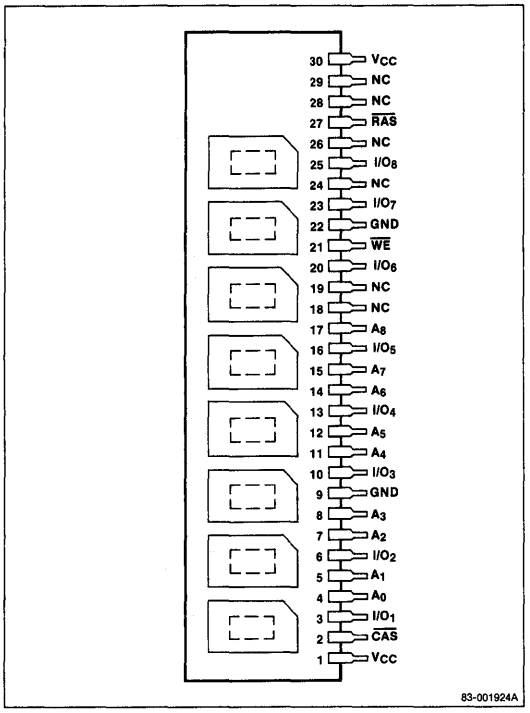
- ☐ 262,144-word by 8-bit organization
- ☐ Single +5V ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates eight 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 220 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-41256A8-12	120 ns	220 ns	120 ns
MC-41256A8-15	150 ns	260 ns	145 ns

Pin Configurations

30-Pin SIMM, MC-41256A8A



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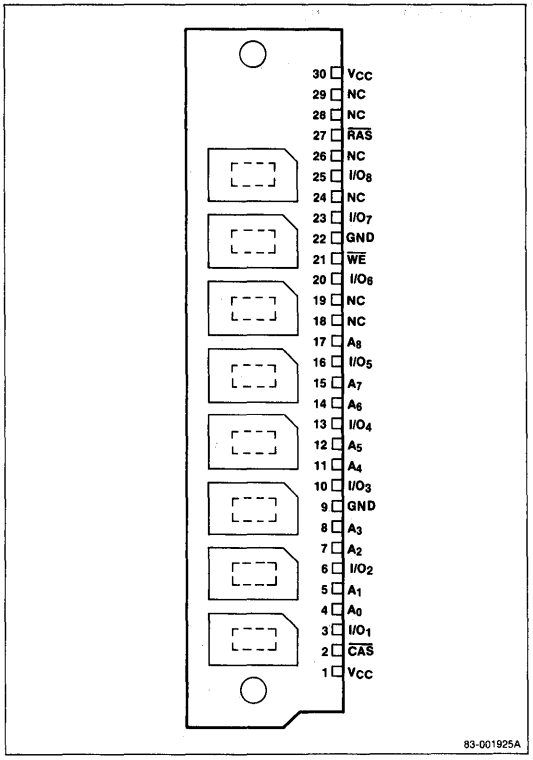
Pin Configurations (cont)

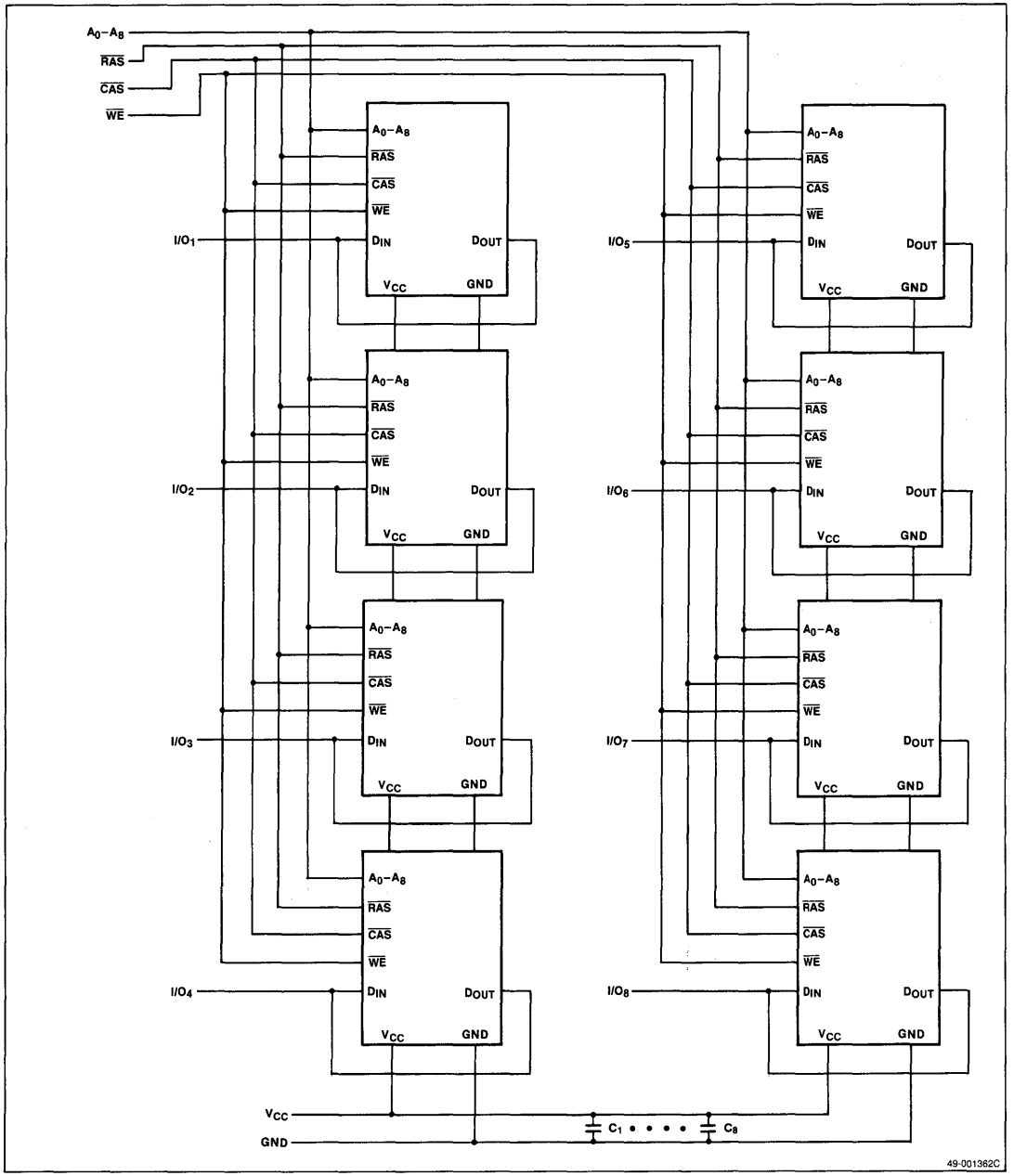
30-Pin SIMM, MC-41256A8B



Pin Identification

No.	Symbol	Function
1, 30	V_{CC}	Power supply (+5.0 V)
2	$\overline{CAS}$	Column address strobe
3, 6, 10, 13 16, 20, 23, 35	I/O_1-I/O_8	Common data inputs/outputs
4, 5, 7, 8, 11, 12, 14, 15, 17	A_0-A_8	Address inputs
9, 22	GND	Ground
18, 19, 24, 26 28, 29	NC	No connection
21	$\overline{WE}$	Write enable
27	$\overline{RAS}$	Row address strobe

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70 °C
Storage temperature, T_{STG}	−55 to +85 °C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 0 to +70 °C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			55	pF	A_0-A_8
Input capacitance	C_{IR}			70	pF	$\overline{RAS}$, $\overline{WE}$
Input capacitance	C_{IC}			70	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}			17	pF	I/O_1-I/O_8 (Note 1)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

DC Characteristics

T_A = 0 to +70 °C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			40.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−80		80	μA	V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−20		20	μA	D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A8-12 Min	MC-41256A8-12 Max	MC-41256A8-15 Min	MC-41256A8-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		664		560	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh mode, average	I_{CC3}		520		425	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page mode, average	I_{CC4}		360		280	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		545		450	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IL}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A8-12		MC-41256A8-15		Unit	Test Conditions
		Min	Max	Min	Max		
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 15)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 15)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

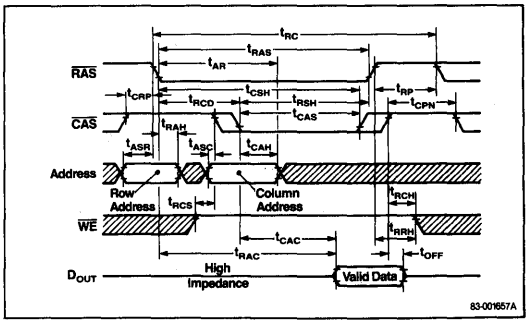
(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$.

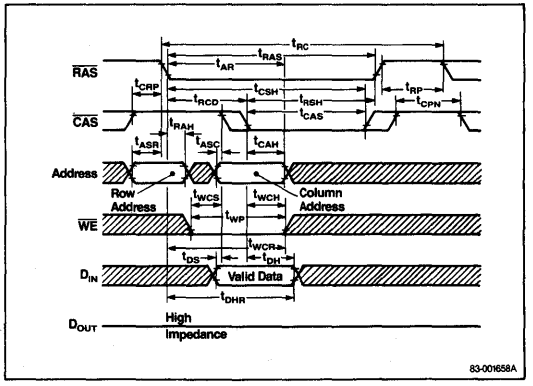
(15) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

Timing Waveforms

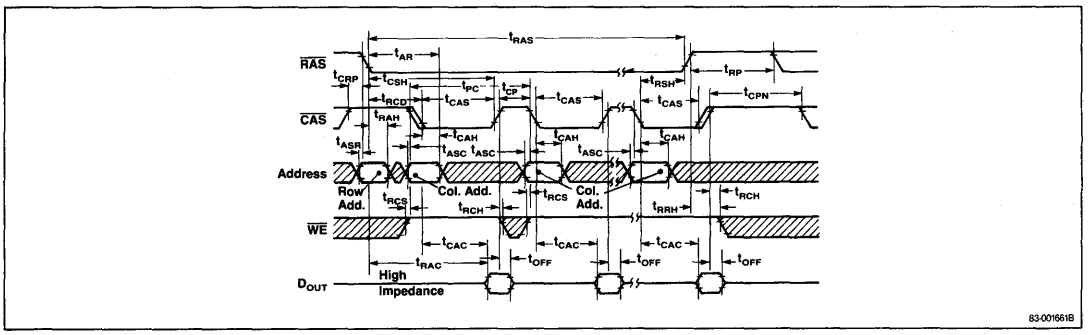
Read Cycle



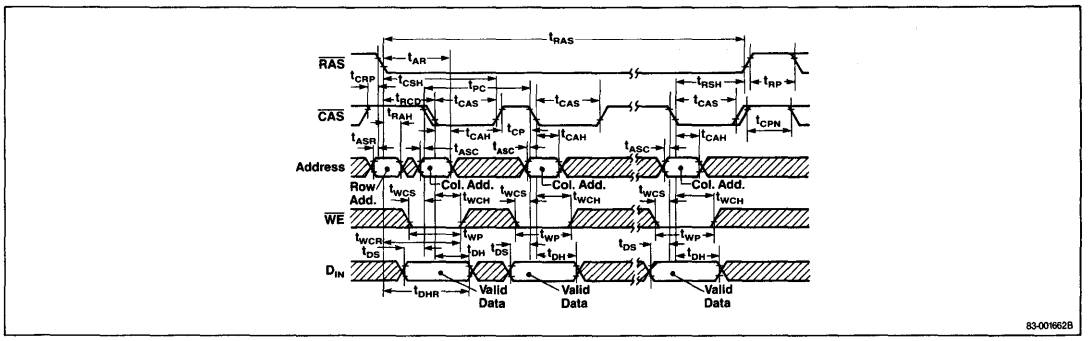
Write Cycle (Early Write)



Page Mode Read Cycle



Page Mode Write Cycle (Early Write)



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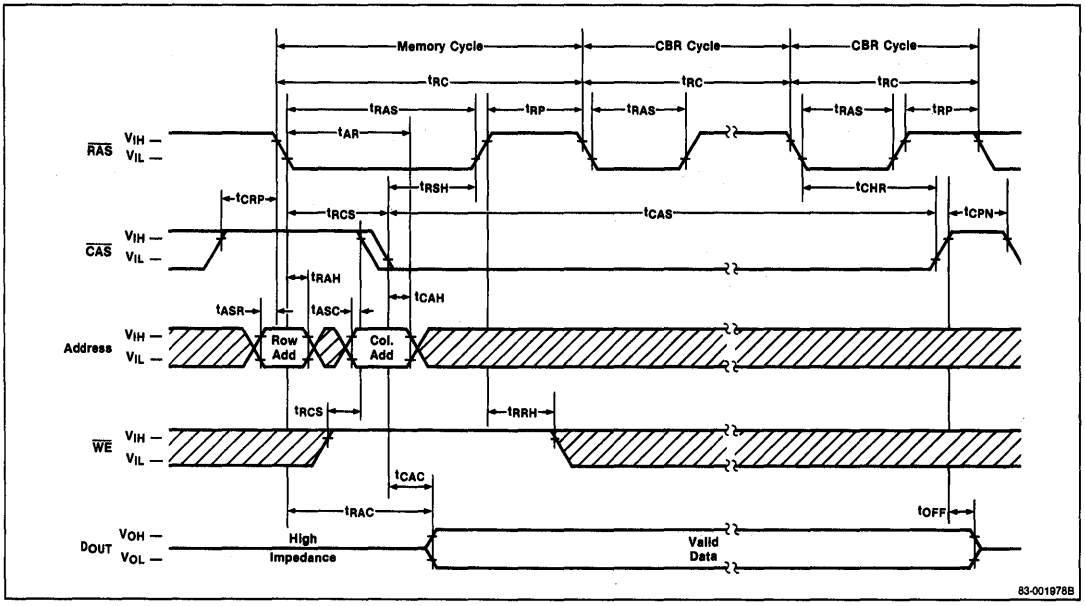
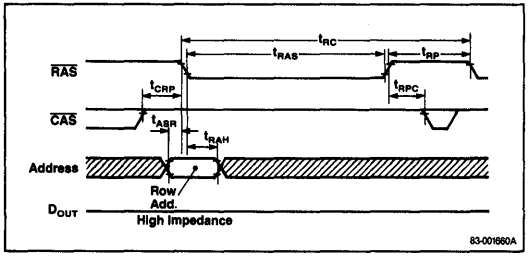
Timing Waveforms (cont)

Hidden Refresh Cycle

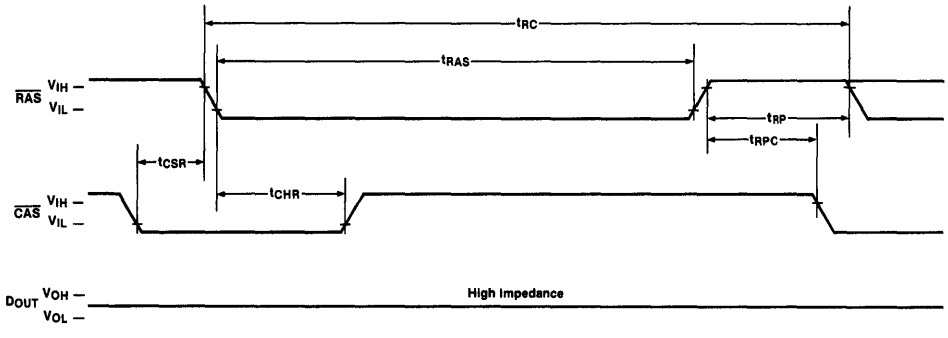


$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

83-001979B

NEC
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MC-41256A9
262,144 x 9-BIT
DYNAMIC NMOS RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-41256A9 is a 262,144-word by 9-bit NMOS dynamic RAM module, designed to operate from a single +5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

The MC-41256A9 operates like eight μPD41256 standard 256K DRAMs with a parity bit. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes nine μPD41256s in PLCC packages and nine power supply decoupling capacitors.

SIMM is a trade mark of Wang Laboratories.

Features

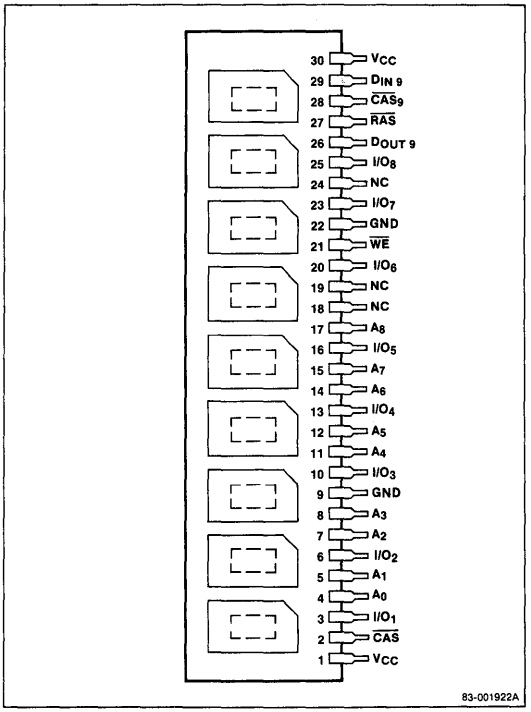
- ☐ 262,144-word by 9-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates nine 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 248 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-41256A9-12	120 ns	220 ns	120 ns
MC-41256A9-15	150 ns	260 ns	145 ns

Pin Configurations

30-Pin SIMM, MC-41256A9A



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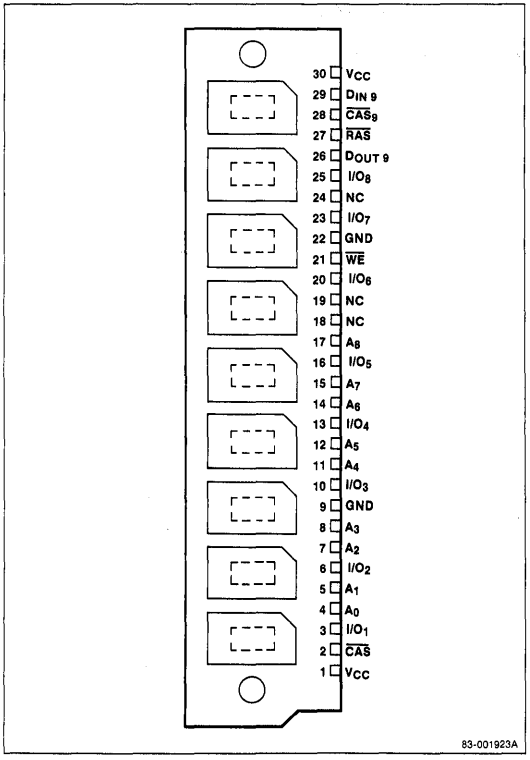
Pin Configurations (cont)

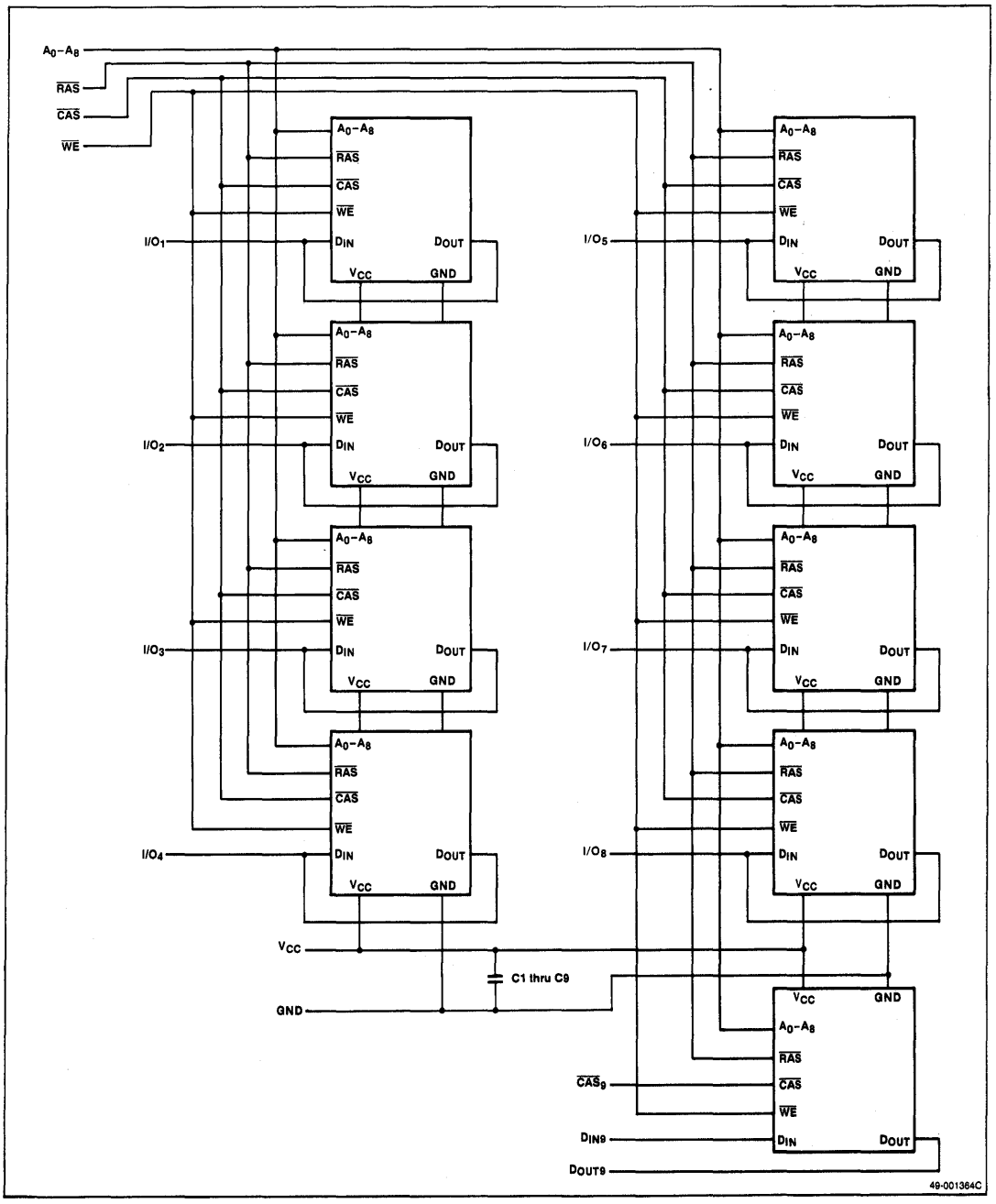
30-Pin SIMM, MC-41256A9B



Pin Identification

No.	Symbol	Function
1, 30	V_{CC}	Power supply (+5.0 V)
2	$\overline{CAS}$	Column address strobe
3, 6, 10, 13, 16, 20, 23, 25	I/O_1-I/O_8	Common data inputs/outputs
4, 5, 7, 8, 11, 12, 14, 15, 17	A_0-A_8	Address inputs
9, 22	GND	Ground
18, 19, 24	NC	No connection
21	$\overline{WE}$	Write enable
26	$D_{OUT\ 9}$	Data output 9
27	$\overline{RAS}$	Row address strobe
28	$\overline{CAS_9}$	Column address strobe for data output 9
29	$D_{IN\ 9}$	Data input 9

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +85°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			60	pF	A_0-A_8
Input capacitance	C_{IR}			75	pF	$\overline{RAS}$, $\overline{WE}$
Input capacitance	C_{IC}			70	pF	$\overline{CAS}$
Input capacitance	$C_{IC\,9}$			13	pF	$\overline{CAS}_9$
Input capacitance	$C_{IN\,9}$			17	pF	$D_{IN\,9}$
Input/output capacitance	C_{IO}			17	pF	I/O_1-I/O_8 (Note 1)
Output capacitance	$C_{OUT\,9}$			12	pF	$D_{OUT\,9}$ (Note 2)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

(2) $\overline{CAS}_9$ = V_{IH} to disable $D_{OUT\,9}$

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			45.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−90		90	μA	For A_0-A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Input leakage current	$I_{IL\,9}$	−10		10	μA	For $\overline{CAS}_9$, $D_{IN\,9}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−20		20	μA	For I/O_1-I/O_8; D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output leakage current	$I_{OL\,9}$	−10		10	μA	For $D_{OUT\,9}$; $D_{OUT\,9}$ disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	MC-41256A9-12 Min	MC-41256A9-12 Max	MC-41256A9-15 Min	MC-41256A9-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		747		630	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh mode, average	I_{CC3}		585		475	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page mode, average	I_{CC4}		405		315	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		610		505	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IL}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Notes 6, 17)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	

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AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-41256A9-12 Min	MC-41256A9-12 Max	MC-41256A9-15 Min	MC-41256A9-15 Max	Unit	Test Conditions
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15, 17)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15, 17)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15, 17)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 16)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

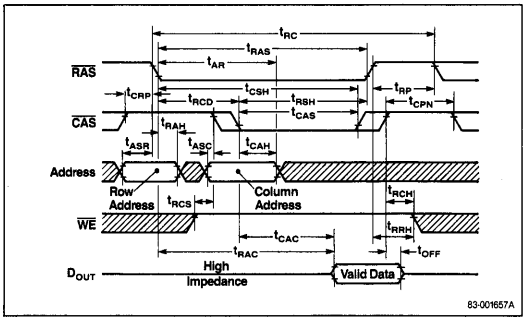
(15) For $D_{OUT\,9}$, t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\,9}$ (at access time and until $\overline{CAS}_9$ returns to V_{IH}) is indeterminate.

(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

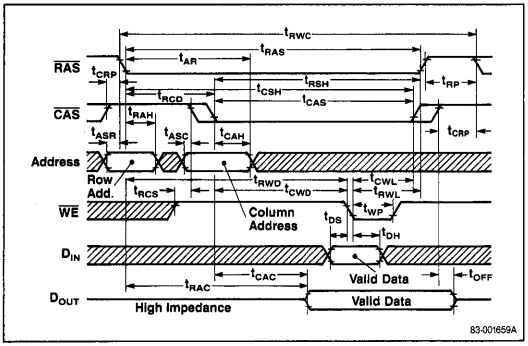
(17) Read-write/read-modify-write operation can be performed only by the PLCC controlled by $\overline{CAS}_9$ because of its separate data input and output terminals.

Timing Waveforms

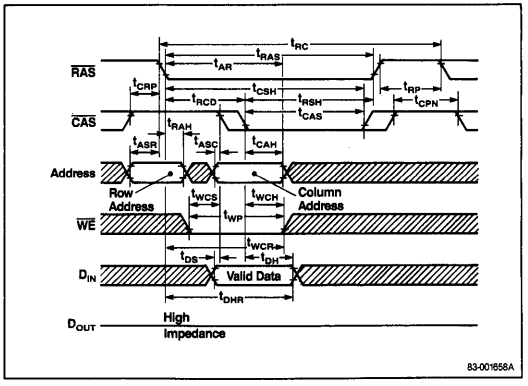
Read Cycle



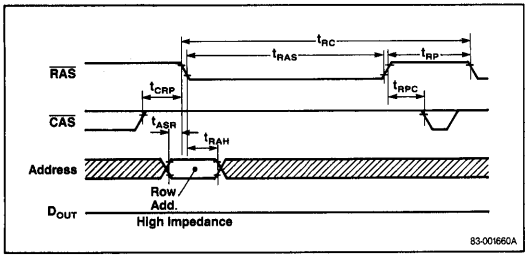
Read-Write/Read-Modify-Write Cycle (D_{OUT} only)



Write Cycle (Early Write)



RAS-Only Refresh Cycle



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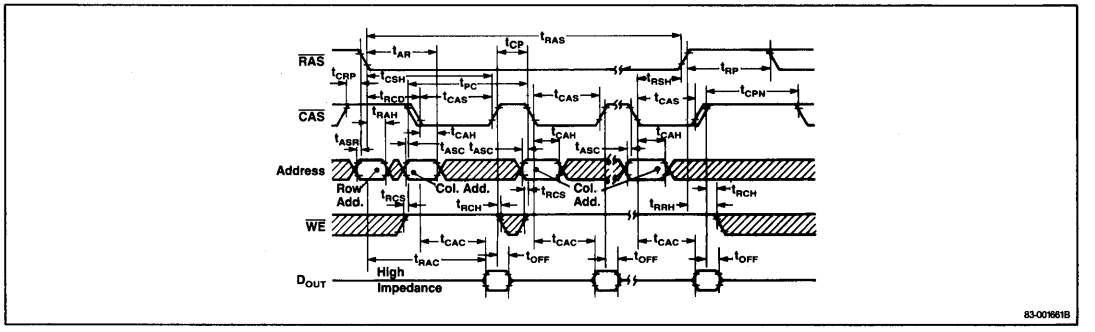
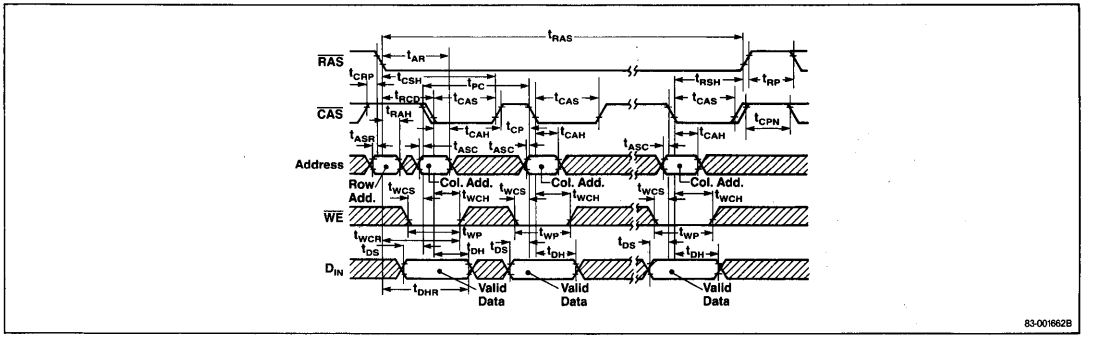
Timing Waveforms (cont)

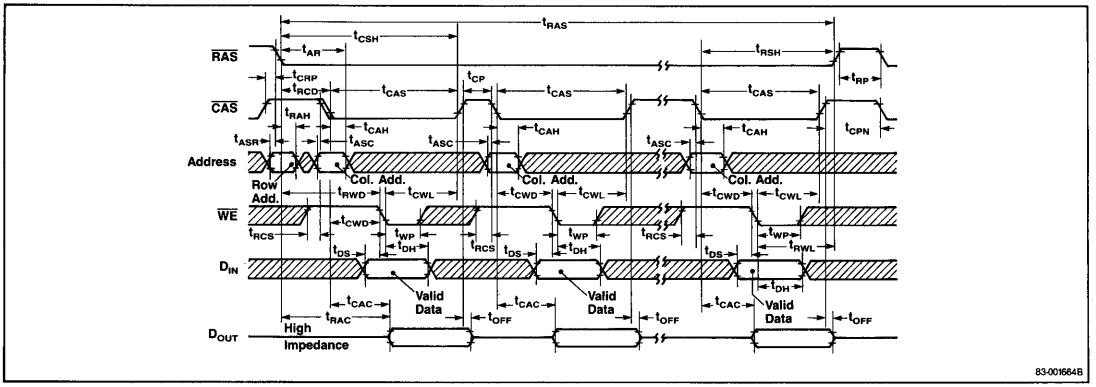
Page Mode Read Cycle



Page Mode Write Cycle (Early Write)

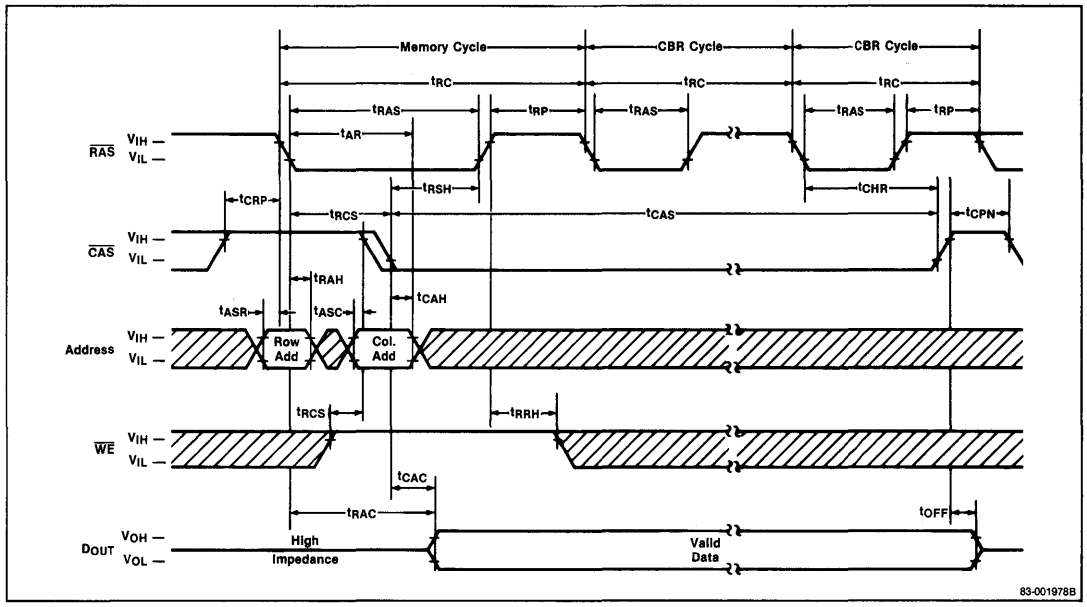


Page Mode Read-Write/Read-Modify-Write Cycle (D_{OUT} only)

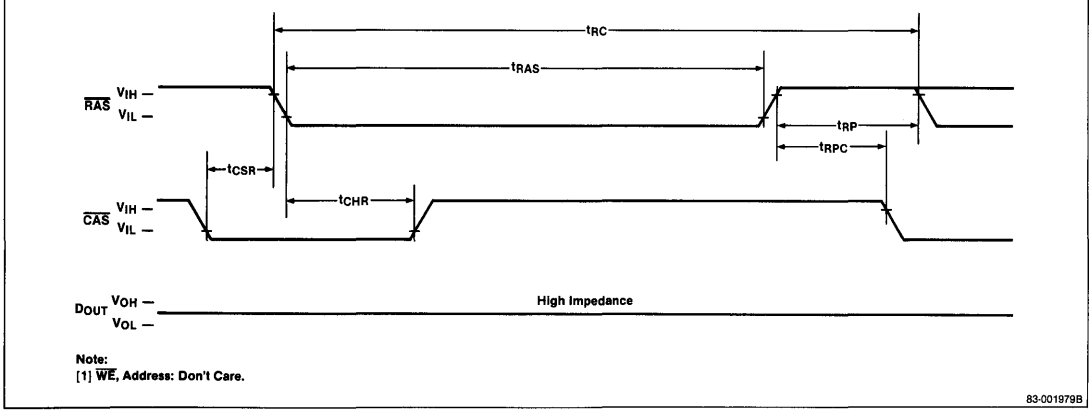


Timing Waveforms (cont)

Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

NEC

NEC Electronics Inc.

MC-411000A1
1,048,576 x 1-BIT
DYNAMIC NMOS RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-411000A1 is a 1,048,576-word by 1-bit NMOS dynamic RAM module, designed to operate from a single +5 V power supply. Advanced dynamic circuitry, including a single-transistor storage cell, sense amplifiers, multiplexed address buffers, and flexible refresh controls provide good system operating margins.

Separate data input and data output pins from four μPD41256s are controlled by individual $\overline{RAS}$ pins and common $\overline{CAS}$ and $\overline{WE}$. Data pins are connected in parallel to provide single input and single output terminals. Refresh is accomplished on each of the four μPD41256s by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4 ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes four μPD41256s in PLCC packages and two power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

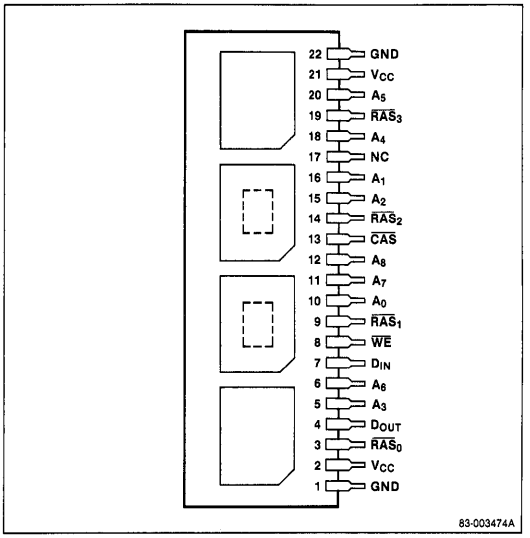
Features

- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 22-pin Single Inline Memory Module (SIMM) package
- ☐ Incorporates four 256K dynamic RAMs in high-density PLCC packaging (μPD41256L)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 110 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page mode capability

Performance Ranges

Device	Max Access Time	Read or Write Cycle Time	Page Mode Cycle Time
MC-411000A1-12	120 ns	220 ns	120 ns
MC-411000A1-15	150 ns	260 ns	145 ns

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 22	GND	Ground
2, 21	V_{CC}	Power supply (+5.0 V)
3, 9, 14, 19	$\overline{RAS_0}$-$\overline{RAS_3}$	Row address strobes
4	D_{OUT}	Data output
5, 6, 10-12, 15, 16, 18, 20	A_0-A_8	Address inputs
7	D_{IN}	Data input
8	$\overline{WE}$	Write enable
13	$\overline{CAS}$	Column address strobe
17	NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +85°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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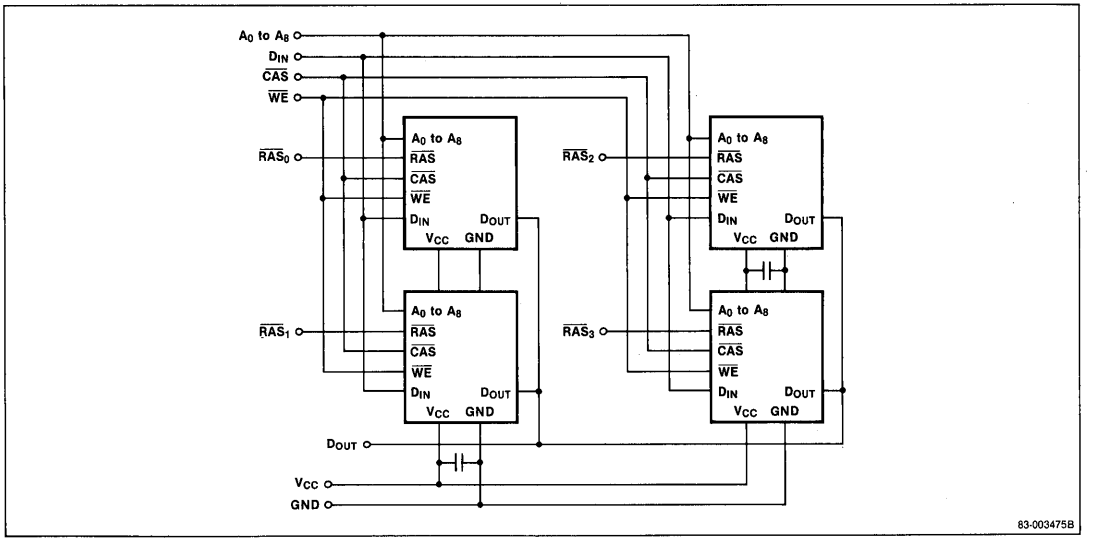
Block Diagram



Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IA}			40	pF	A_0-A_8, D_{IN}
Input capacitance	C_{IR}			15	pF	$\overline{RAS}_0$-$\overline{RAS}_3$
Input capacitance	C_{IW}			50	pF	$\overline{WE}$
Input capacitance	C_{IC}			50	pF	$\overline{CAS}$
Output capacitance	C_{OUT}			50	pF	D_{OUT} (Note 1)

Note:

(1) $\overline{CAS}$ = V_{IH} to disable D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			20.0	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = High-Z
Input leakage current	I_{IL}	−40		40	μA	For A_0-A_8, D_{IN}, $\overline{CAS}$, $\overline{WE}$; V_{IN} = 0 to 5.5 V; other pins = 0 V
Input leakage current, $\overline{RAS}$ input	$I_{IL\ (RAS)}$	−10		10	μA	V_{IN} = 0 to 5.5 V; untested $\overline{RAS}$ pins = V_{IH}; other pins = 0 V
Output leakage current	I_{OL}	−40		40	μA	D_{OUT} disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits MC-411000A1-12 Min	Limits MC-411000A1-12 Max	Limits MC-411000A1-15 Min	Limits MC-411000A1-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		98		85	mA	One $\overline{RAS}$ input and $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min, other three $\overline{RAS}$ inputs = V_{IH} (Note 5)
Operating current, refresh mode, average	I_{CC3}		80		68	mA	One $\overline{RAS}$ input cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min, other three $\overline{RAS}$ inputs = V_{IH} (Note 5)
Operating current, page mode, average	I_{CC4}		60		50	mA	One $\overline{RAS}$ input = V_{IL}, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min, other three $\overline{RAS}$ inputs = V_{IH} (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		83		71	mA	One $\overline{RAS}$ input cycling, $\overline{CAS} = V_{IL}$, $t_{RC} = t_{RC}$ min, other three $\overline{RAS}$ inputs = V_{IH} (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	

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AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits MC-411000A1-12 Min	Limits MC-411000A1-12 Max	Limits MC-411000A1-15 Min	Limits MC-411000A1-15 Max	Unit	Test Conditions
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	(Note 16)

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles on each $\overline{RAS}$ input before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

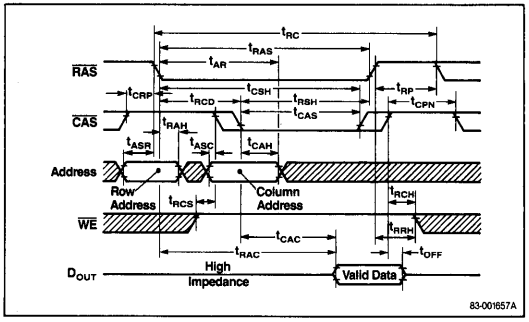
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

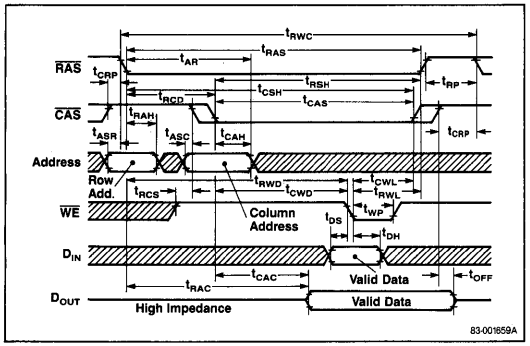
(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified. Refresh operations can be performed on all four μPD41256Ls simultaneously by the use of $\overline{CAS}$ before $\overline{RAS}$ refresh cycles or $\overline{RAS}$-only refresh cycles. All other operations require that only one of the $\overline{RAS_0}$-$\overline{RAS_3}$ inputs is in the active state.

Timing Waveforms

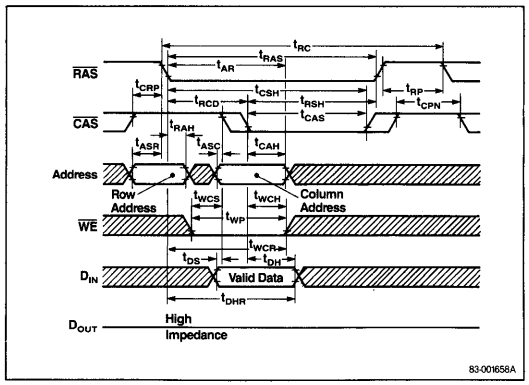
Read Cycle



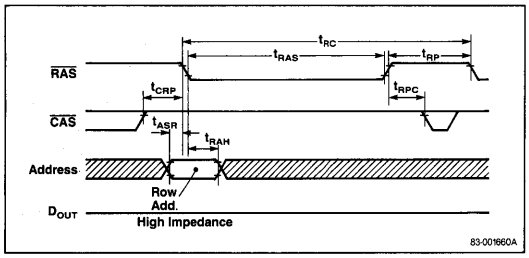
Read-Write/Read-Modify-Write Cycle



Write Cycle (Early Write)



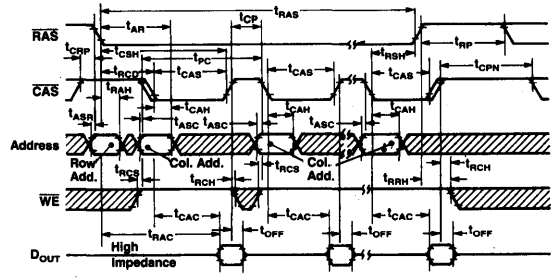
RAS-Only Refresh Cycle



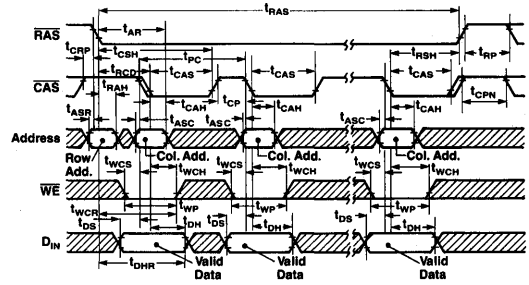
4

Timing Waveforms (cont)

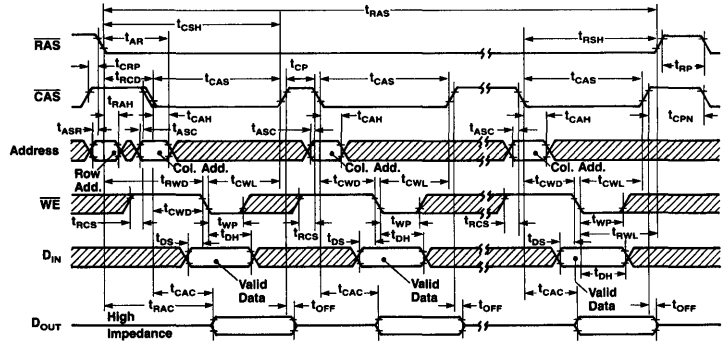
Page Mode Read Cycle



Page Mode Write Cycle (Early Write)

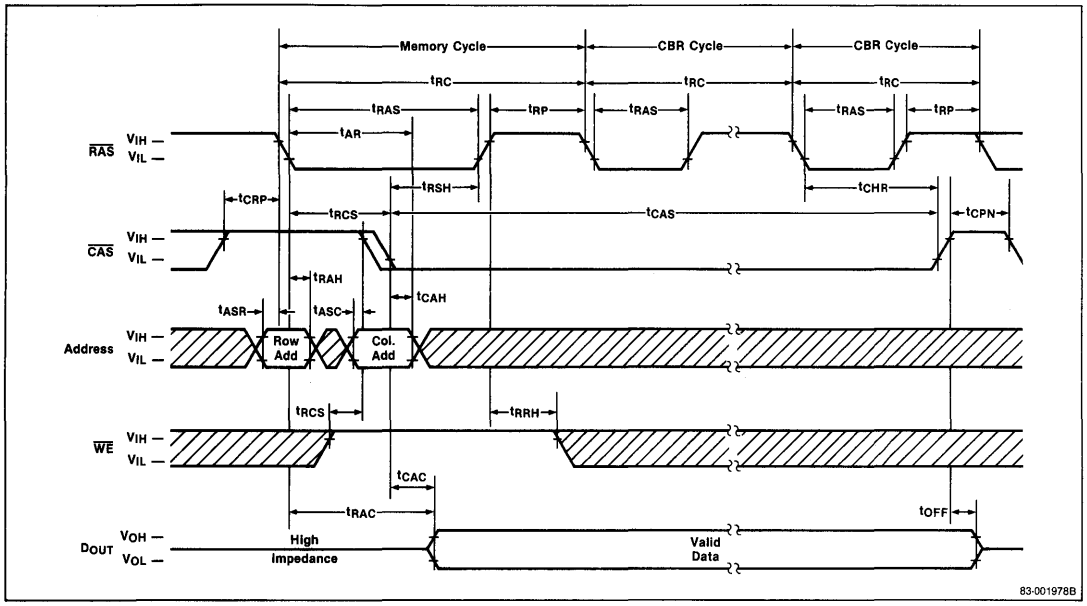


Page Mode Read-Write/Read-Modify-Write Cycle

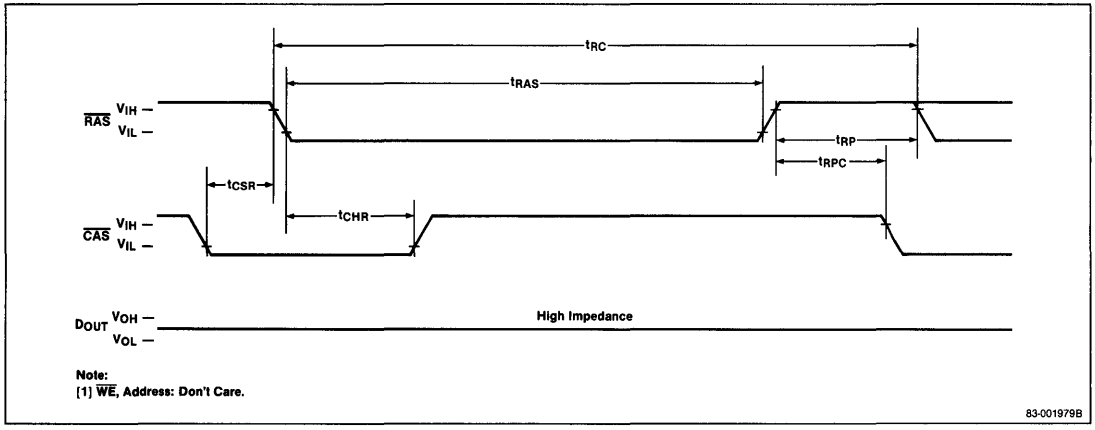


Timing Waveforms (cont)

Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

NEC

DYNAMIC RAMs 5

Section 5 — Dynamic RAMs

μPD4164
65,536 x 1-BIT
DYNAMIC NMOS RAM

Revision 4

Description

The NEC μPD4164 is a 65,536-word by 1-bit dynamic N-channel MOS Random-access Memory (RAM) designed to operate from a single +5V power supply. The negative-voltage substrate bias is internally generated providing both automatic and transparent operation.

The μPD4164 utilizes a three-poly, N-channel, silicon-gate process which provides high storage cell density, high performance, and high reliability.

The μPD4164 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 512 sense amplifiers, which assure that power dissipation is minimized. Refresh characteristics have been chosen to maximize yield at a low cost to the user while maintaining compatibility between dynamic RAM generations.

The μPD4164 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data-out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The μPD4164 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128-address combinations of A_0 through A_6 during a 2ms period.

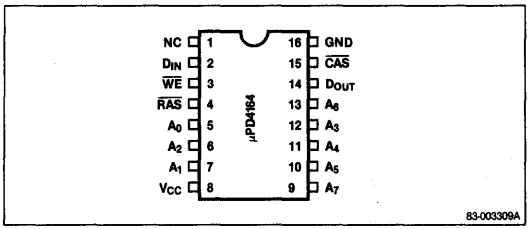
Multiplexed address inputs permit the μPD4164 to be packaged in the standard 16-pin dual-in-line package. The 16-pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

Features

- ☐ 65,536 x 1-bit organization
- ☐ High memory density
- ☐ Multiplexed address inputs
- ☐ Single +5V power supply
- ☐ On-chip substrate bias generator
- ☐ Low power dissipation: 27.5mW max (standby) (μPD4164-10); 330mW.(active); 27.5mW (standby)
- ☐ Three-state, TTL-compatible, nonlatched output
- ☐ Read, write, read-write, read-modify-write, $\overline{RAS}$-only refresh, and page mode capability
- ☐ All inputs TTL-compatible, and low input capacitance
- ☐ 128 refresh cycles (A_0–A_6 pins for refresh address)
- ☐ $\overline{CAS}$-controlled output allows hidden refresh
- ☐ Available in a plastic 16-pin package
- ☐ 4 performance ranges:

Device	Access Time	R/W Cycle	RMW Cycle
μPD4164-10	100ns	200ns	230ns
μPD4164-12	120ns	230ns	245ns
μPD4164-15	150ns	260ns	280ns
μPD4164-20	200ns	330ns	345ns

Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	NC	No connection
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
5–7, 9–13	A_0–A_7	Address inputs
8	V_{CC}	+5V power supply
14	D_{OUT}	Data output
15	$\overline{CAS}$	Column address strobe
16	GND	Ground

Absolute Maximum Ratings*

Operating Temperature, T_{OPR}	0°C to +70°C
Storage Temperature, T_{STG} (Plastic Package)	−55°C to +125°C
Supply Voltages On Any Pin except V_{CC}	−1V to +7V①
Supply Voltage, V_{CC}	−0.5V to +7V①
Short-circuit Output Current	50mA
Power Dissipation, P_D	1W

Note: ① Relative to GND.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DC Characteristics

T_A = 0°C to +70°C ①; V_{CC} = +5V ± 10%; GND = 0V

Parameter	Symbol		Limits Min	Typ	Max	Unit	Test Conditions
Supply Voltage	V_{CC}		4.5	5.0	5.5	V	All voltages referenced to GND
	GND		0	0	0	V	
High-level Input Voltage, ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	V_{IHC}		2.4		5.5	V	
High-level Input Voltage, All Inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	V_{IH}		2.4		5.5	V	
Low-level Input Voltage, All Inputs	V_{IL}		−1.0		0.8	V	
Operating Current Average Power Supply Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = t_{RC} (min)	I_{CC1}	μPD4164-20			45	mA	②
		μPD4164-15			50		
		μPD4164-12			55		
		μPD4164-10			60		
Standby Current Power Supply Standby Current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High-impedance)	I_{CC2}				5.0	mA	
Refresh Current Average Power Supply Current, Refresh Mode; $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = t_{RC} (min)	I_{CC3}	μPD4164-20			35	mA	②
		μPD4164-15			40		
		μPD4164-12			45		
		μPD4164-10			45		
Page Mode Current Average Power Supply Current, Page Mode Operation $\overline{RAS}$ = V_{IL}; $\overline{CAS}$ Cycling t_{PC} = t_{PC} (min)	I_{CC4}	μPD4164-20			35	mA	②
		μPD4164-15			40		
		μPD4164-12			45		
		μPD4164-10			45		
Input Leakage Current (any input); V_{IN} = 0V to +5.5V; All Other Pins Not Under Test = 0V	$I_{I(L)}$		−10		10	μA	
Output Leakage Current D_{OUT} is Disabled, V_{OUT} = 0V to +5.5V	$I_{O(L)}$		−10		10	μA	
Output Levels High-level Output Voltage (I_{OUT} = 5mA)	V_{OH}		2.4		V_{CC}	V	
Low-level Output Voltage (I_{OUT} = 4.2mA)	V_{OL}		0		0.4	V	

Notes: ① T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met.

② I_{CC1}, I_{CC3} and I_{CC4} depend on output loading and cycle rates. Specified rates are obtained with the output open.

Capacitance

T_A = 0°C to +70°C; V_{CC} = +5V ± 10%; GND = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance (A_0–A_7), D_{IN}	C_{I1}			5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}			8	pF	
Output Capacitance $D_{(OUT)}$	C_O			7	pF	

AC Characteristics

T_A = 0°C to +70°C ①; V_{CC} = +5V ± 10%; GND = 0V ② ③ ④

Parameter	Symbol	Limits 4164-20 Min	4164-20 Max	4164-15 Min	4164-15 Max	4164-12 Min	4164-12 Max	4164-10 Min	4164-10 Max	Unit	Notes
Random Read or Write Cycle Time	t_{RC}	330		260		230		200		ns	⑤
Read-write Cycle Time	t_{RWC}	345		280		245		230		ns	⑤
Page Mode Cycle Time	t_{PC}	190		145		130		110		ns	⑤
Access Time from $\overline{RAS}$	t_{RAC}		200		150		120		100	ns	⑥ ⑦
Access Time from $\overline{CAS}$	t_{CAC}		100		75		60		50	ns	⑦ ⑧
Output Buffer Turn-off Delay	t_{OFF}	0	50	0	40	0	35	0	30	ns	⑨
Transition Times (rise and fall)	t_T	3	50	3	50	3	35	3	35	ns	④
$\overline{RAS}$ Precharge Time	t_{RP}	120		100		90		90		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	.2	10	.15	10	.12	10	.1	10	μs	
$\overline{RAS}$ Hold Time	t_{RSH}	100		75		60		50		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	.1	10	.075	10	.06	10	.05	10	μs	
$\overline{CAS}$ Hold Time	t_{CSH}	200		150		120		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	30	100	25	75	25	60	20	50	ns	⑩
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		0		0		ns	
$\overline{CAS}$ Precharge Time	t_{CPN}	30		25		25		20		ns	
$\overline{CAS}$ Precharge Time (for page mode cycle only)	t_{CP}	80		60		60		50		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	0		0		0		0		ns	
Row Address Set-up Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	20		15		15		10		ns	
Column Address Set-up Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	30		25		20		15		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	130		100		80		65		ns	
Read Command Set-up Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	25		20		20		20		ns	⑪

AC Characteristics (Cont.)

T_A = 0°C to +70°C ①; V_{CC} = +5V ± 10%; GND = 0V ② ③ ④

Parameter	Symbol	Limits 4164-20 Min	4164-20 Max	4164-15 Min	4164-15 Max	4164-12 Min	4164-12 Max	4164-10 Min	4164-10 Max	Unit	Notes
Read Command Hold Time	t_{RCH}	0		0		0		0		ns	⑪
Write Command Hold Time	t_{WCH}	55		45		35		30		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	155		120		95		80		ns	
Write Command Pulse Width	t_{WP}	55		45		35		30		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	55		45		40		35		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	55		45		40		35		ns	
Data-in Set-up Time	t_{DS}	0		0		0		0		ns	⑫
Data-in Hold Time	t_{DH}	55		45		35		30		ns	⑫
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	155		120		95		80		ns	
Refresh Period	t_{REF}		2		2		2		2	ms	
Write Command Set-up Time	t_{WCS}	−10		−10		−10		0		ns	⑬
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	55		45		40		40		ns	⑬
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	130		120		100		90		ns	⑬

Notes: ① T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.

② An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

③ AC measurements assume t_T = 5ns.

④ V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

⑤ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle times at which proper operation over the full temperature range (T_A = 0°C to +70°C) is assured.

⑥ Assumes that $t_{RCS} \leq t_{RCD}$ (max). If t_{RCS} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

⑦ Measured with a load equivalent to 2 TTL loads and 100pF.

⑧ Assumes that $t_{RCD} \geq t_{RCD}$ (max).

⑨ t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

⑩ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.

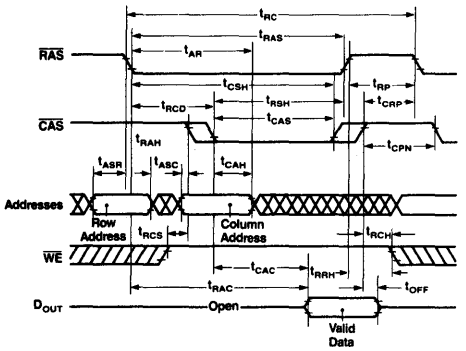
⑪ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

⑫ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

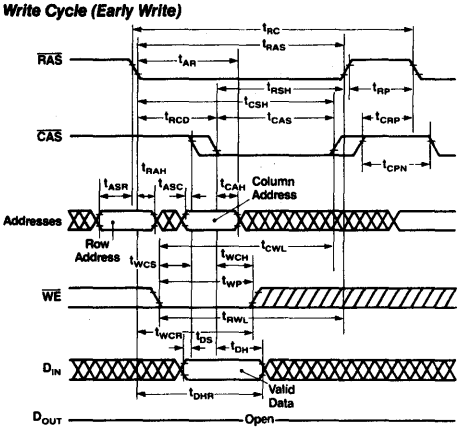
⑬ t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read-write, and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions is met the condition of the data-out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

Timing Waveforms

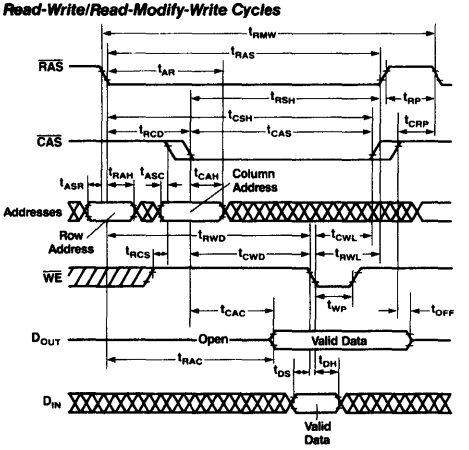
Read Cycle



Write Cycle (Early Write)



Read-Write/Read-Modify-Write Cycles



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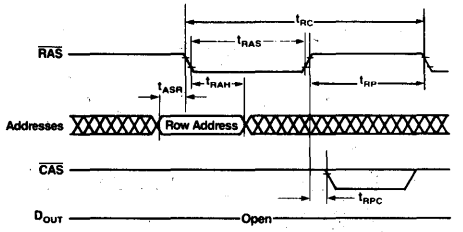
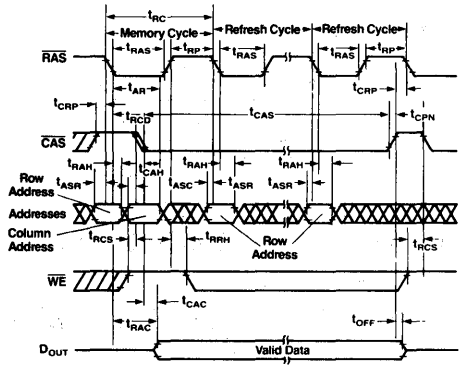
Timing Waveforms (Cont.)

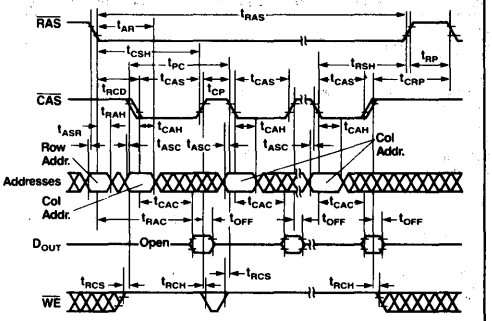
$\overline{RAS}$-only Refresh Cycle



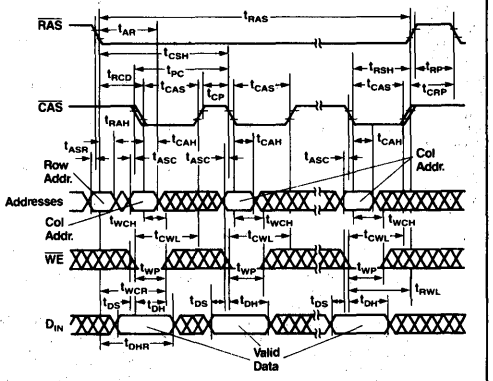
Hidden Refresh Cycle



Page Mode Read Cycle



Page Mode Write Cycle



μPD4265
65,536 x 1-BIT
DYNAMIC CMOS RAM

Revision 1

Description

The NEC μPD4265 is a 65,536-word by 1-bit dynamic CMOS Random Access Memory (RAM) designed to operate from a single +5 V power supply. The negative voltage substrate bias is generated internally providing automatic and transparent operation.
The unique construction of the μPD4265 allows for an extremely low standby power device that incorporates three user-selected, self-refresh standby modes. The device can accomplish $\overline{RAS}$-only refresh. Also, by utilizing the pin 1 refresh function, it can perform automatic pulsed refresh or hidden auto pulsed refresh which makes use of the internal refresh address generator.

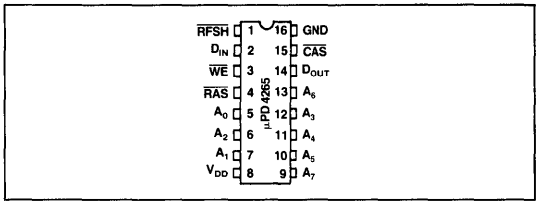
Features

- ☐ 65,536-word x 1-bit organization
- ☐ High memory density: 16-pin plastic DIP
- ☐ Single +5V ± 10% power supply
- ☐ Control on pin 1 for automatic and self refresh
- ☐ Multiplexed address inputs
- ☐ Fully TTL-compatible including clocks
- ☐ Three-state output
- ☐ Read, write, RMW, $\overline{RAS}$-only refresh, page mode, latched pulse, pulse and self-refresh capabilities
- ☐ $\overline{CAS}$-controlled output allows hidden refresh
- ☐ 2 performance ranges:

Device	t_{RAC}	t_{CAC}	t_{RC}	Power
μPD4265C-20	200ns	100ns	335ns	193mW
μPD4265C-25	250ns	125ns	410ns	165mW

- ☐ Cycle time: R/W, 335ns min
- ☐ Low power dissipation
  - 35mA max (operating)
  - 1.0mA max (standby, $\overline{RAS} = \overline{CAS} = V_{IH}$)
  - 0.5mA max (standby, $\overline{RAS} = \overline{CAS} = V_{DD}$)
  - 200μA max (self-refresh 1, T_A = 0°C to +70°C)
  - 100μA max (self-refresh 2, T_A = 0°C to +45°C)
  - 50μA max (self-refresh 3, T_A = 0°C to +25°C) (According to Figure 1.)
- ☐ 128 refresh cycles

Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	$\overline{RFSH}$	Refresh
2	D_{IN}	Data-in
3	$\overline{WE}$	Write Enable
4	$\overline{RAS}$	Row Address Strobe
5–7, 9–13	$A_0 - A_7$	Address Inputs
5–7, 10–13	$A_0 - A_6$	Refresh Addresses
8	V_{DD}	+5V Power Supply
14	D_{OUT}	Data-out
15	$\overline{CAS}$	Column Address Strobe
16	GND	Ground

Absolute Maximum Ratings*

Voltage on any Pin Relative to Ground, $V_{I/O}$	−1.0V to +7.0V
Operating Temperature, T_{OPT} (Ambient)	0°C to +70°C
Storage Temperature, T_{STG} (Ambient)	−55°C to +125°C
Short-circuit Output Current, I_{OS}	50mA
Power Dissipation, P_D	1W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C; f = 1MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address, Data-in	C_{I1}			5	pF	
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$	C_{I2}			8	pF	
Output	C_O			7	pF	

5

DC Characteristics

T_A = 0°C to +70°C; V_{DD} = 5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply Voltage	V_{DD}	4.5	5.0	5.5	V	All Voltages Referenced to Ground
High-level Input Voltage	V_{IH}	2.4		5.5	V	
Low-level Input Voltage	V_{IL}	−1.0		0.8	V	
V_{DD} Supply Current Standby	I_{DD2}			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}
Standby (Output-enable)	I_{DD5}			1.0	mA	$\overline{RAS}$ = V_{IH}
Standby	I_{DD6}			0.5	mA	$\overline{RAS}$ = $\overline{CAS}$ = V_{DD}
Self-refresh 1 (T_A = 0°C to +70°C)	I_{DD8}			200	μA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}; $\overline{WE}$ = V_{IH}
Self-refresh 2 (T_A = 0°C to +45°C)	I_{DD9}			100	μA	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}; $\overline{WE}$ = V_{IL}
Self-refresh 3	I_{DD10}			①		$\overline{CAS}$ = GND; $\overline{RAS}$ = V_{IH}; $\overline{WE}$ = V_{DD}/GND
Input Leakage Current	$I_{I(L)}$	−10		10	μA	
Output Leakage Current	$I_{O(L)}$	−10		10	μA	
Output Low Voltage	V_{OL}	0		0.4	V	I_{OL} = 4.2mA
Output High Voltage	V_{OH}	2.4		V_{DD}		I_{OH} = −5mA

Note: ① According to Figure 1.

AC Characteristics

T_A = 0°C to +70°C; V_{DD} = 5V ± 10%

Read, Write, RMW, $\overline{RAS}$-only Refresh Cycles

Parameter	Symbol	Limits 4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
V_{DD} Operating Current	I_{DD1}		35		30	mA	
V_{DD} $\overline{RAS}$-only Refresh Current	I_{DD3}		30		25	mA	
V_{DD} Page Current	I_{DD4}		20		17	mA	
Random Read or Write Cycle Time	t_{RC}	335		410		ns	
Read, Write Cycle Time	t_{RWC}	370		465		ns	
Access Time from $\overline{RAS}$	t_{RAC}		200		250	ns	
Access Time from $\overline{CAS}$	t_{CAC}		100		125	ns	
Output Buffer Turn-off Delay	t_{OFF}	0	50	0	60	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	60	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	120		150		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	200	10000	250	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100		125		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	10000	125	10000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	200		250		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	30	100	35	125	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	0		0		ns	
$\overline{CAS}$ Precharge Time, (Nonpage Cycles)	t_{CPN}	30		35		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	0		0		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	20		25		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	55		65		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	155		190		ns	
Read Command Set-up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	25		30		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	
Write Command Hold Time	t_{WCH}	55		65		ns	

AC Characteristics (Cont.)

T_A = 0°C to +70°C; V_{DD} = 5V ± 10%

Read, Write, RMW, $\overline{RAS}$-only Refresh Cycles

Parameter	Symbol	Limits 4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	155		190		ns	
Write Command Pulse Width	t_{WP}	55		65		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	55		65		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	55		65		ns	
Data-in Set-up Time	t_{DS}	0		0		ns	
Data-in Hold Time	t_{DH}	55		65		ns	
Data-in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	155		190		ns	
Refresh Period	t_{REF}		2		2	ns	
$\overline{WE}$ Command Set-up Time	t_{WCS}	−10		−10		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	80		100		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	180		235		ns	

Page Mode Cycle

Parameter	Symbol	Limits 4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
Read or Write Cycle Time	t_{PC}	190		260		ns	
Read Modify Write Cycle Time	t_{CPM}	230		280		ns	
$\overline{CAS}$ Precharge Time	t_{CP}	80		100		ns	
$\overline{RAS}$ Pulse Width	t_{RPM}	200	10000	250	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	100	10000	125	10000	ns	

Pulse Refresh Cycle (Latched Pulse Refresh)

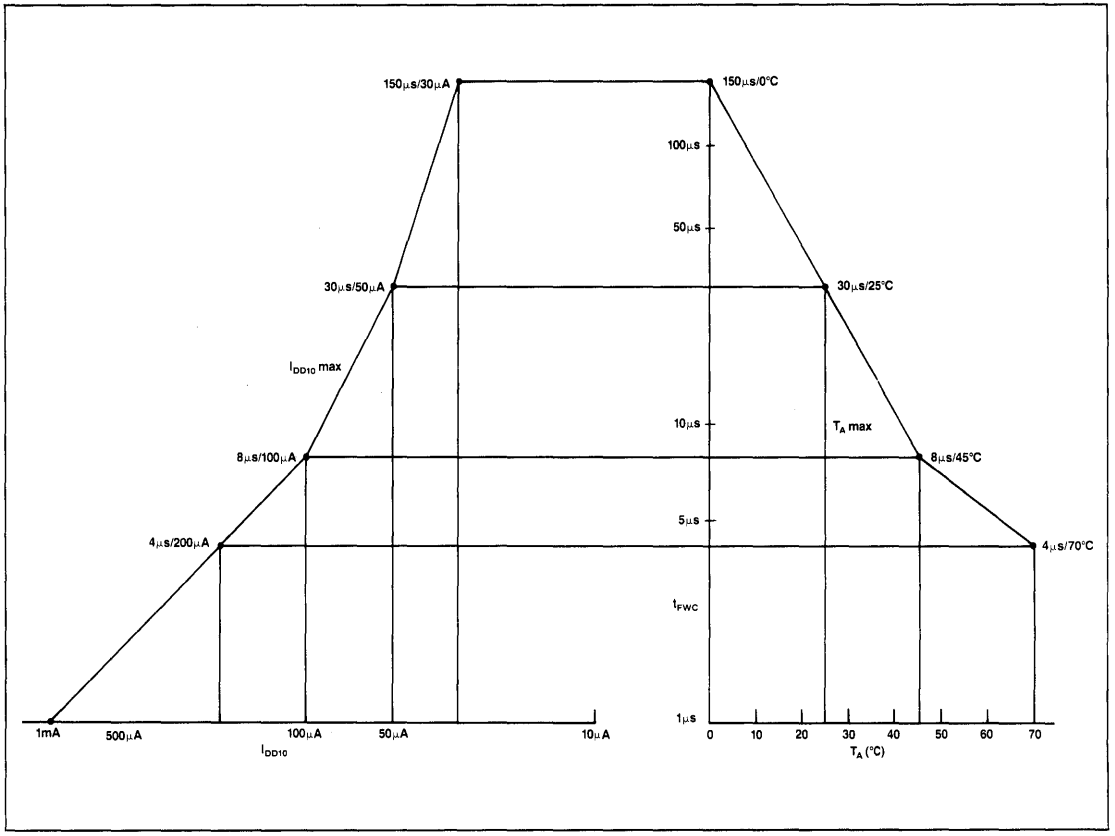
Parameter	Symbol	Limits 4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
V_{DD} Pulse Refresh Current	I_{DD7}		25		20	mA	
Pulse Refresh Cycle Time	t_{FC}	335		410		ns	
$\overline{RAS}$ to $\overline{RFSH}$ Delay	t_{RFD}	120		150		ns	
$\overline{RFSH}$ Pulse Width	t_{FAS}	80	1000	80	1000	ns	
$\overline{RFSH}$ Precharge Time	t_{FP}	120		120		ns	
$\overline{RFSH}$ to $\overline{RAS}$ Delay	t_{FSR}	30		30		ns	
$\overline{RFSH}$ before $\overline{RAS}$ Set-up Time	t_{FBR}	365		445		ns	
$\overline{RAS}$ to $\overline{RFSH}$ Delay (Latched Pulse)	t_{FRD}	80		80		ns	
$\overline{RAS}$ to $\overline{RFSH}$ Set-up (Latched Pulse)	t_{RFS}	455		560		ns	

Self-refresh Cycle

Parameter	Symbol	Limits 4265-20 Min	4265-20 Max	4265-25 Min	4265-25 Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{RFSH}$ Delay	t_{RFD}	120		150		ns	
$\overline{RFSH}$ Pulse Width	t_{FAS}	8000		8000		ns	
$\overline{RFSH}$ to $\overline{RAS}$ Delay	t_{FRS}	365		445		ns	
$\overline{RAS}$ Hold Time	t_{FRH}	8000		8000		ns	
$\overline{RAS}$ to $\overline{RFSH}$ Set-up Time	t_{RSF}	0		0		ns	
$\overline{RFSH}$ to $\overline{CAS}$ Delay	t_{FCD}	0	1000	0	1000	ns	
$\overline{RFSH}$ to $\overline{WE}$ Delay	t_{FWD}	0	1000	0	1000	ns	
$\overline{RFSH}$ to $\overline{CAS}$ Set-up Time	t_{FCS}	0		0		ns	
$\overline{RFSH}$ to $\overline{WE}$ Set-up Time	t_{FWS}	0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ Set-up Time	t_{FWCS}	0		0		ns	
$\overline{WE}$ Pulse Width	t_{FWP}	1		1		μs	
$\overline{WE}$ Pulse Cycle Time	t_{FWC}		①		①	μs	

Note: ① According to Figure 1.

Figure 1. I_{DD10} vs. t_{FWC} vs. T_A



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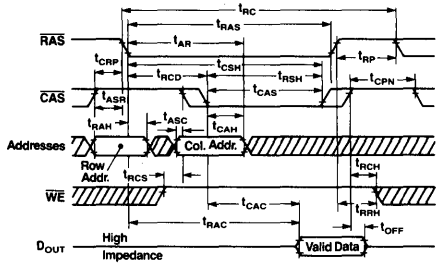
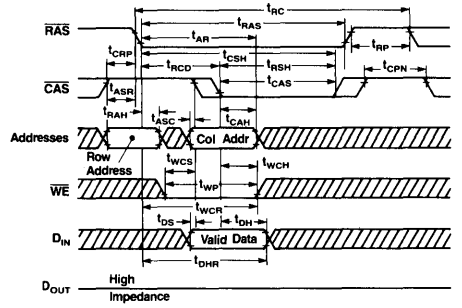
Timing Waveforms

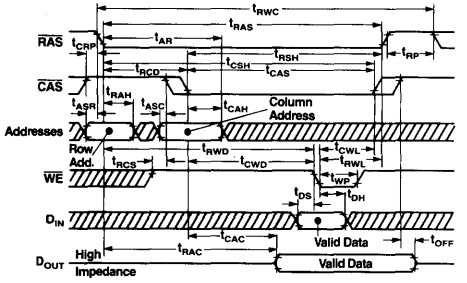
Read Cycle



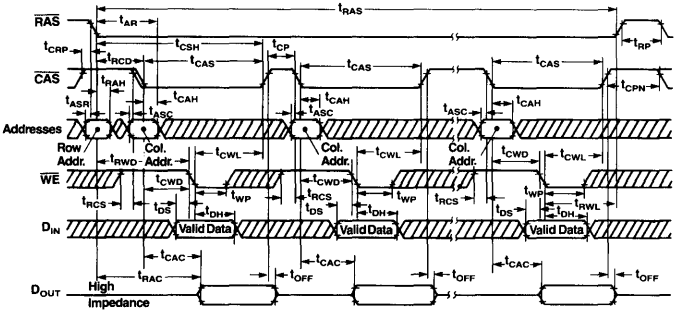
Write Cycle (Early Write)



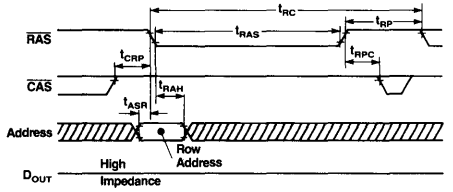
Read-Write/Read-Modify-Write Cycles



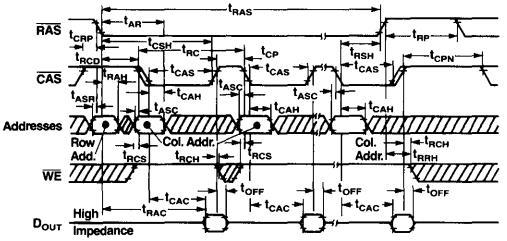
Page Mode Read-Write/Read-Modify-Write Cycles



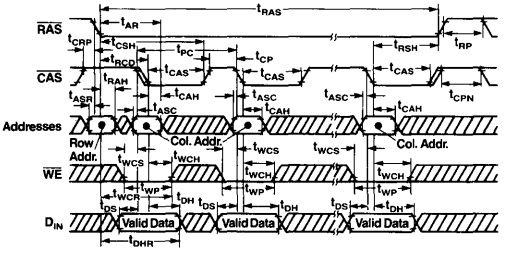
RAS-only Refresh Cycle



Page Mode Read Cycle



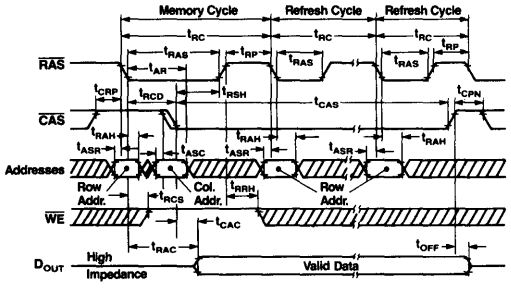
Page Mode Write Cycle (Early Write)



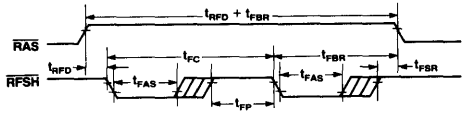
Page Mode Read-Write/Read-Modify-Write Cycles

Timing Waveforms (Cont.)

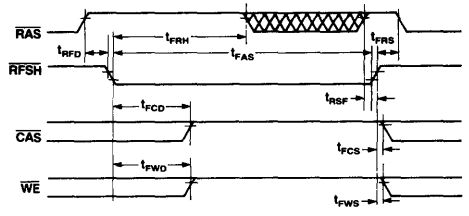
Hidden Refresh Cycle



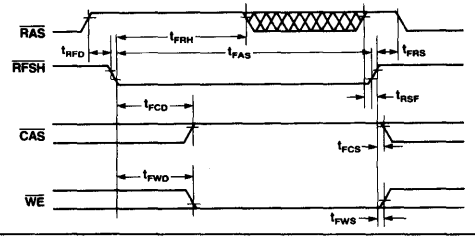
Pulse Refresh Cycle



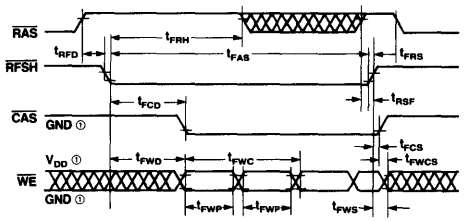
Self-refresh Cycle 1



Self-refresh Cycle 2

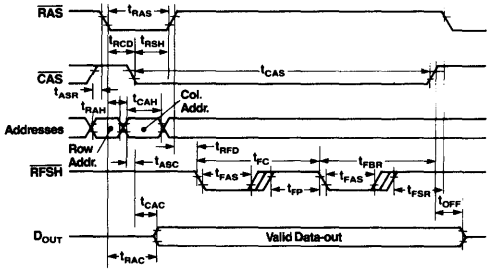


Self-refresh Cycle 3

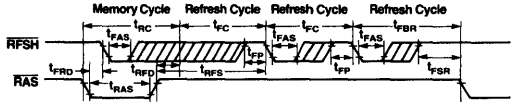


Note: ① Needs CMOS level.

Hidden Automatic Pulse Refresh Cycle



Latched Pulse Refresh Cycle



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μPD41256
262,144 x 1-BIT
DYNAMIC NMOS RAM

Revision 1

Description

The μPD41256 is a 262,144-word by 1-bit dynamic N-channel MOS RAM designed to operate from a single +5 V power supply. The negative voltage substrate bias is automatically generated internally.

The μPD41256 offers a direct upgrade from the 64K μPD4164 achieving a four-fold increase in bit density at the board level.

The μPD41256 utilizes double poly layer N-channel silicon-gate processing which provides for high storage cell density, high performance, and high reliability.

The μPD41256 utilizes a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 1024 sense amplifiers, which ensures that power dissipation is minimized.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output then is returned to the high impedance state by returning the $\overline{CAS}$ to the high state. The μPD41256 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A_0-A_7, during a 4 ms period.

Features

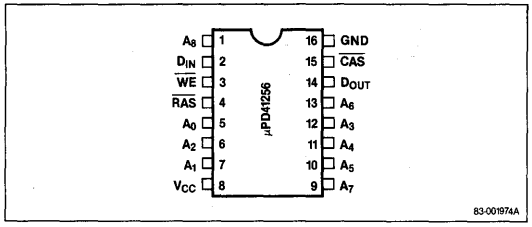
- ☐ 262,144 × 1-bit organization
- ☐ High density packaging: DIP, PLCC, ZIP
- ☐ Multiplexed address inputs
- ☐ Single +5 V, ±10% power supply
- ☐ On-chip substrate bias generator
- ☐ Low power dissipation: 28 mW standby (max)
- ☐ Nonlatched output is three-state, TTL-compatible
- ☐ All inputs TTL-compatible, and low input capacitance
- ☐ 256 refresh cycles (A_0-A_7 pins for refresh address)
- ☐ Page mode operation
- ☐ $\overline{RAS}$-only refresh, hidden refresh, and $\overline{CAS}$ before $\overline{RAS}$ refresh cycles (see Note 16)

Performance Ranges

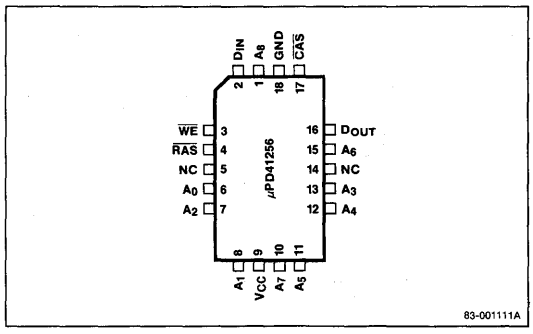
Device	Access Time (Max)	R/W Cycle (Min)	RMW Cycle (Min)
μPD41256-12	120 ns	220 ns	265 ns
μPD41256-15	150 ns	260 ns	310 ns
μPD41256-20	200 ns	330 ns	390 ns

Pin Configurations

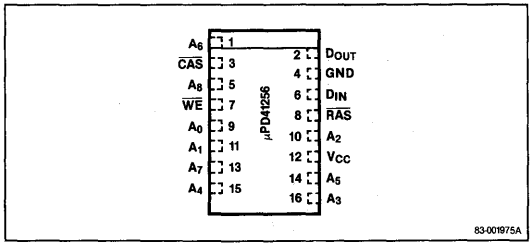
16-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



16-Pin Plastic Zig-Zag Inline Package (ZIP)



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Pin Indentification

Plastic DIP

No.	Symbol	Function
1, 5–7, 9–13	A_0–A_8	Address inputs
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable input
4	$\overline{RAS}$	Row address strobe
8	V_{CC}	+5 V power supply input
14	D_{OUT}	Data output
15	$\overline{CAS}$	Column address strobe input
16	GND	Ground

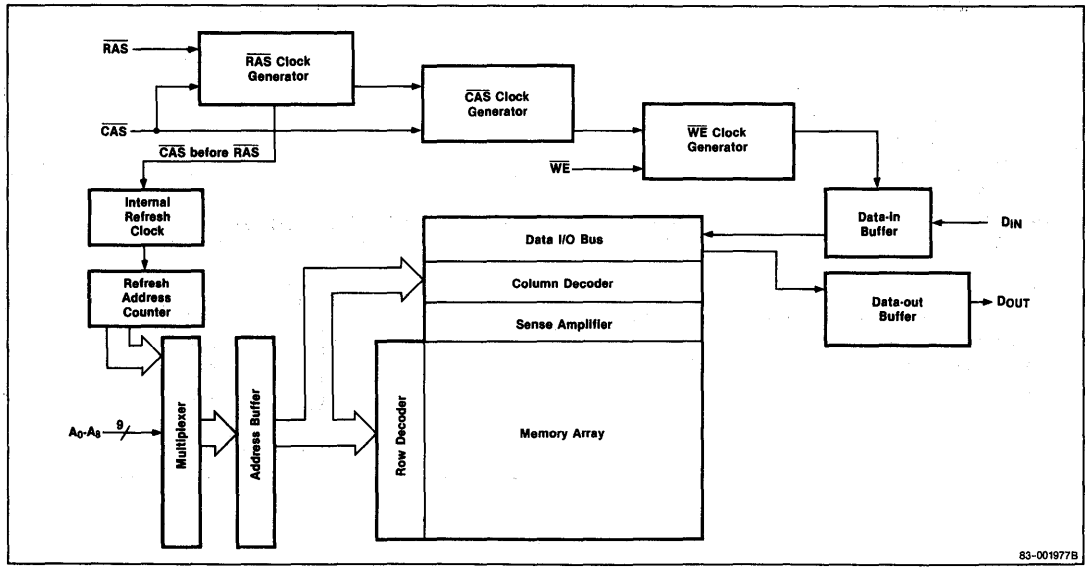
Plastic PLCC

No.	Symbol	Function
1, 6-8 10-13, 15	A_0–A_8	Address inputs
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable input
4	$\overline{RAS}$	Row address strobe
5, 14	NC	No connection
9	V_{CC}	+5 V power supply input
16	D_{OUT}	Data output
17	$\overline{CAS}$	Column address strobe input
18	GND	Ground

Plastic ZIP

No.	Symbol	Function
1, 5, 9–11, 13–16	A_0–A_8	Address inputs
2	D_{OUT}	Data output
3	$\overline{CAS}$	Column address strobe input
4	GND	Ground
6	D_{IN}	Data input
7	$\overline{WE}$	Write enable input
8	$\overline{RAS}$	Row address strobe
12	V_{CC}	+5 V power supply input

Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	−1.0 V to +7.0 V
Operating temperature, T_A (ambient)	0 to 70°C
Storage temperature, T_{STG}	−55 to 150°C
Power dissipation, P_D	1 W
Short-circuit output current, I_{OS}	50 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = 5\,V \pm 10\%$, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Standby supply current	I_{CC2}			5.0	mA	$\overline{RAS} = V_{IH}$, D_{OUT} = High impedance
Input leakage current	$I_{I(L)}$	−10		10	μA	$V_{IN} = 0$ V to 5.5 V, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, $V_{OUT} = 0$ V to 5.5 V
Output voltage low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Output voltage high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Supply voltage	GND	0	0	0	V	
Input voltage low	V_{IL}	−1.0		0.8	V	
Input voltage high	V_{IH}	2.4		5.5	V	

Capacitance

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\,V \pm 10\%$, f = 1.0 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{I1}			5	pF	A_0–A_8, D_{IN}
Input capacitance	C_{I2}			8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_{OUT}			7	pF	D_{OUT}

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AC Characteristics (Notes 2, 3, 4)

$0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$ (Note 1)

Parameter	Symbol	Limits μPD41256-12 Min	Limits μPD41256-12 Max	Limits μPD41256-15 Min	Limits μPD41256-15 Max	Limits μPD41256-20 Min	Limits μPD41256-20 Max	Unit	Test Conditions
Operating supply current, average	I_{CC1}		83		70		60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min, (Note 5)
Operating supply current, refresh mode, average	I_{CC3}		65		55		50	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min, (Note 5)
Operating supply current, page mode operation, average	I_{CC4}		60		55		50	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min, (Note 5)
Random read or write cycle time	t_{RC}	220		260		330		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		390		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		190		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		120		150		200	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75		100	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	30	0	35	0	45	ns	(Note 10)
Transition time, rise and fall	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	100	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		200		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	30	100	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	25		25		30		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	50		60		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
ROW address setup time	t_{ASR}	0		0		0		ns	
ROW address hold time	t_{RAH}	15		15		20		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	20		25		30		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		130		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		25		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		50		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		150		ns	
Write command pulse width	t_{WP}	20		25		30		ns	

AC Characteristics (Notes 2, 3, 4) (cont)

$0°C \leq T_A \leq 70°C$, $V_{CC} = 5\,V \pm 10\%$ (Note 1)

Parameter	Symbol	Limits μPD41256-12 Min	Limits μPD41256-12 Max	Limits μPD41256-15 Min	Limits μPD41256-15 Max	Limits μPD41256-20 Min	Limits μPD41256-20 Max	Unit	Test Conditions
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		55		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		55		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		50		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		150		ns	
Refresh period	t_{REF}		4		4		4	ms	
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		100		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		200		ns	(Note 15)
$\overline{CAS}$ set-up time for CBR refresh	t_{CSR}	10		10		10		ns	(Note 16)
$\overline{CAS}$ hold time for CBR refresh	t_{CHR}	30		30		35		ns	(Note 16)

Notes:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3} and I_{CC4} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_A = 0°C$ to $70°C$) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

(12) t_{CRP} requirement should be applicable for RAS/CAS cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to WE leading edge in delayed Write or Read-Modify-Write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a Read-Write and the data output will contain data read from the selected cell. If nither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

(16) P process code products do not have the $\overline{CAS}$-Before-$\overline{RAS}$ Refresh feature. DIP products with process codes L or F and PLCC products with process code E have the CBR feature. On DIP products with process code P, the external address inputs are required in Hidden Refresh cycles and the address timing must satisfy t_{ASR} and t_{RAH}, which are specified with respect to the $\overline{RAS}$ falling edge.

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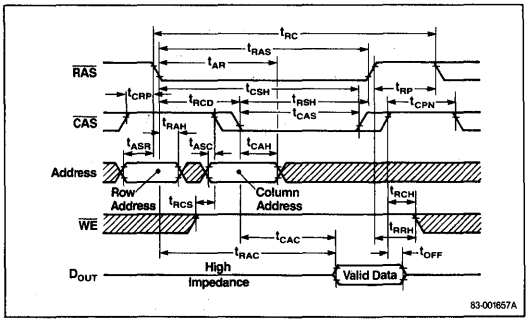
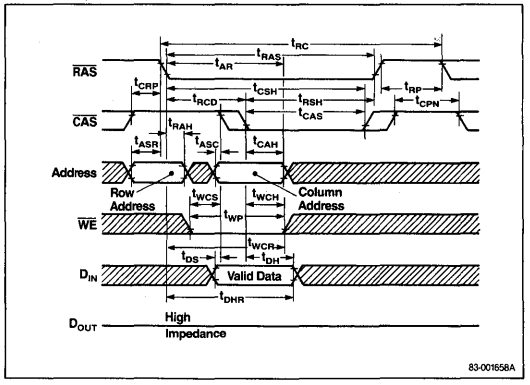
Timing Waveforms

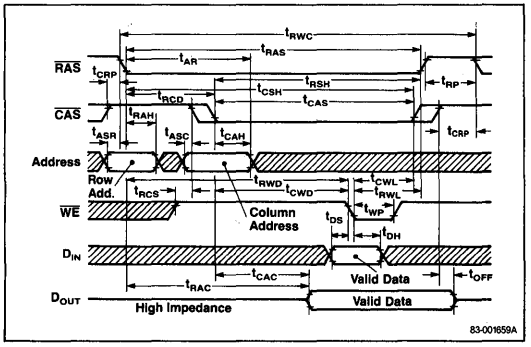
Read Cycle



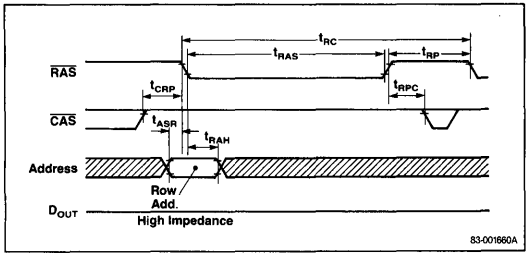
Write Cycle (Early Write)



Read-Write/Read-Modify-Write Cycle

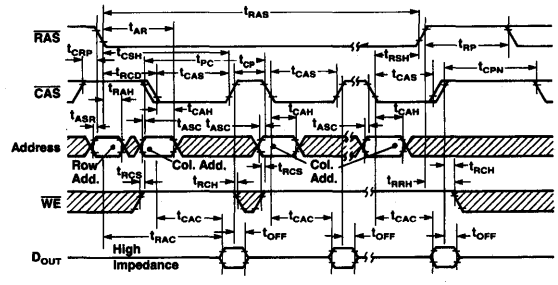


"RAS-Only" Refresh Cycle



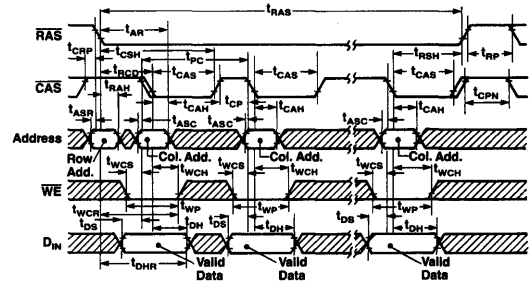
Timing Waveforms (cont)

Page Mode Read Cycle



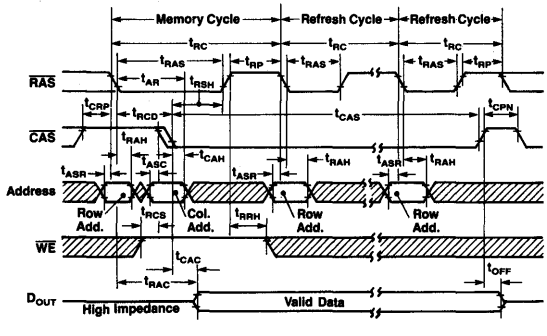
83-001661B

Page Mode Write Cycle (Early Write)



83-001662B

Hidden Refresh Cycle (Process Code P) (Note 16)



83-001663B

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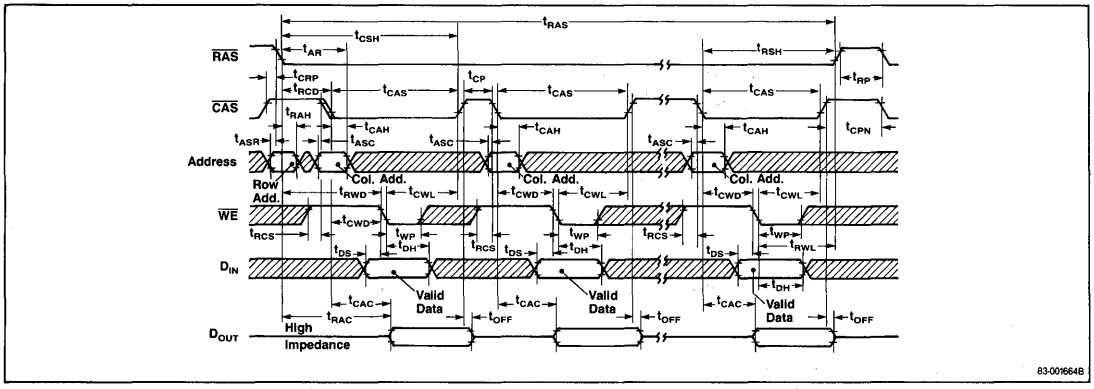
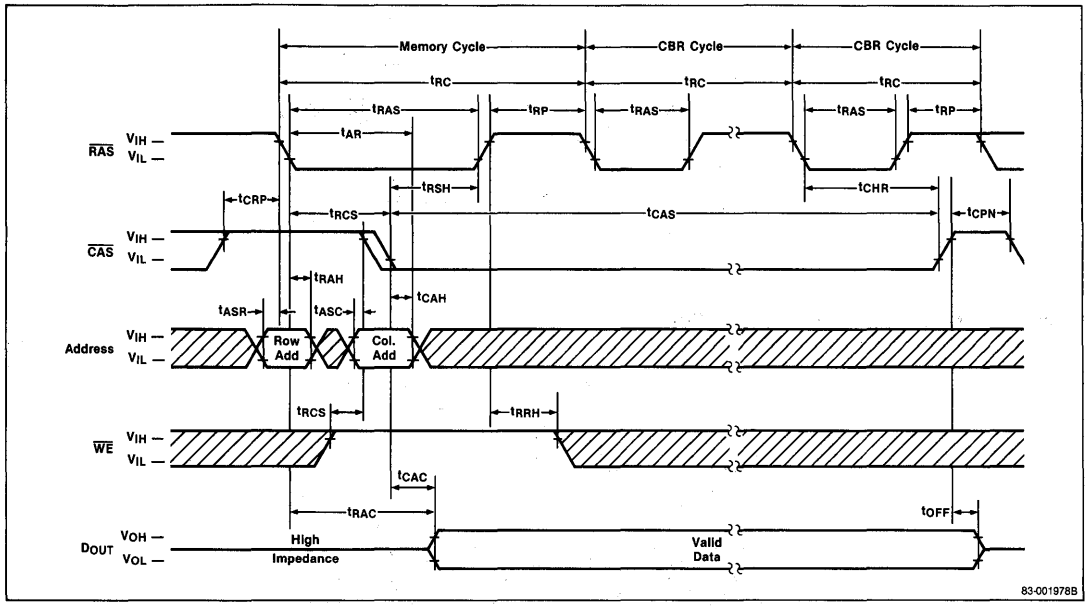
Timing Waveforms (cont)

Page Mode Read-Write/Read-Modify-Write Cycle

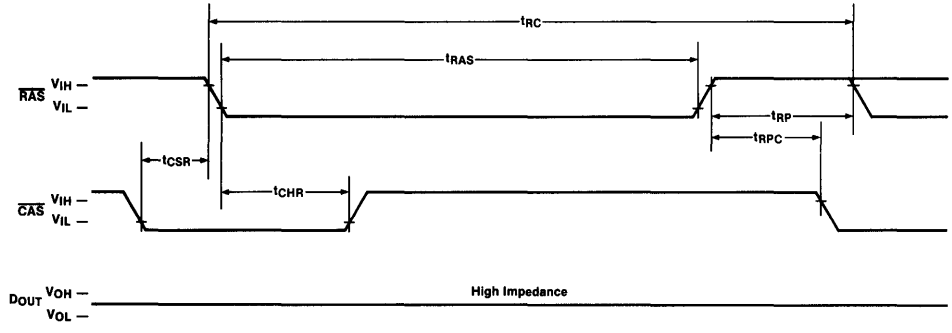


Hidden Refresh Cycle (Process Code L, F, E) (Note 16)



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (Process Code L, F, E) (Note 16)



Note:
[1] $\overline{WE}$, Address: Don't Care.

83-001979B

μPD41257
262,144 x 1-BIT
DYNAMIC NMOS RAM

Revision 1

Description

The NEC μPD41257 is a 262,144-word by 1-bit dynamic N-channel MOS random-access memory (RAM) designed to operate from a single +5 V power supply. The negative voltage substrate bias is automatically generated internally.

The μPD41257 utilizes double polylayer N-channel silicon gate processing which provides for high storage cell density, high performance, and high reliability.

The device also utilizes a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 1024 sense amplifiers, which ensures that power dissipation is minimized.

The three-state output is controlled by $\overline{CAS}$ independently of $\overline{RAS}$. The device is capable of nibble mode operation on either read or write cycles by cycling $\overline{CAS}$.

Refresh is accomplished by utilizing a $\overline{CAS}$ before $\overline{RAS}$ cycle that will enable the internal generation of the refresh address. Refresh can also be accomplished using $\overline{RAS}$-only refresh, hidden refresh, or normal read or write cycles on the 256 address combinations of A_0-A_7, during a 4 ms period.

Features

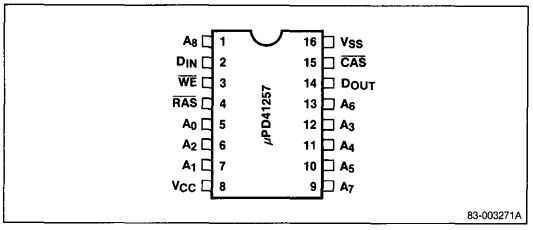
- ☐ 262,144-word x 1-bit organization
- ☐ High density plastic DIP and PLCC packaging
- ☐ Multiplexed address inputs
- ☐ Single +5 V ± 10% power supply
- ☐ Nibble mode on read or write or read-modify-write cycles
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Low power dissipation:
  −28 mW max (standby)
  −385 mW max (active, t_{RC} = 270 ns)
- ☐ Non-latched output, three-state, TTL-compatible
- ☐ All inputs TTL-compatible, and low input capacitance
- ☐ 256-cycle, 4 ms refresh (A_0-A_7 pins for refresh address)

Performance Ranges

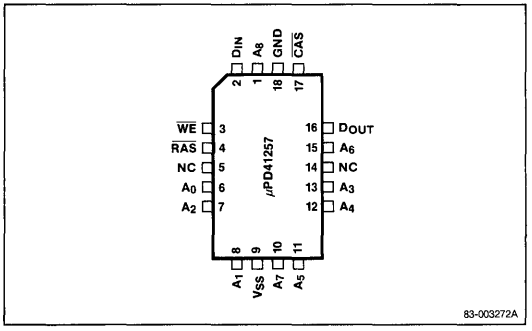
Device	Access Time	R/W Cycle	RMW Cycle
μPD41257-15	150 ns	270 ns	310 ns
μPD41257-20	200 ns	335 ns	390 ns

Pin Configurations

Plastic DIP



Plastic Leaded Chip Carrier (PLCC)



Pin Identification

Plastic DIP

No.	Symbol	Function
1, 5-7, 9-13	A_0-A_8	Address inputs
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
8	V_{CC}	Power supply (+5.0 V)
14	D_{OUT}	Data output
15	$\overline{CAS}$	Column address strobe
16	V_{SS}	Ground

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Pin Identification (cont)

PLCC

No.	Symbol	Function
1, 6-8, 10-13, 15	A_0-A_8	Address inputs
2	D_{IN}	Data input
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
5, 14	NC	No connection
9	V_{CC}	Power supply (+5.0 V)
16	D_{OUT}	Data output
17	$\overline{CAS}$	Column address strobe
18	V_{SS}	Ground

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	−1.0 to +7.0 V
Operating temperature, T_A	0 to +70°C
Storage temperature, T_{STG}	−55 to +150°C
Short-circuit output current	50 mA
Power Dissipation, P_D	1 W

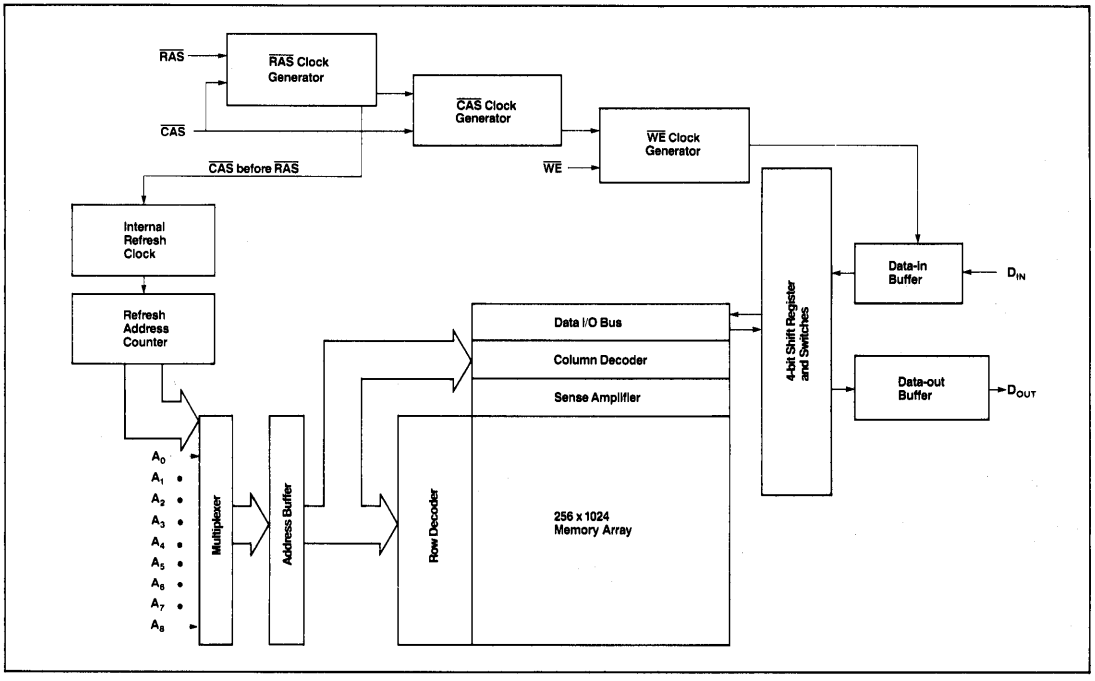
Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{I1}			5	pF	A_0-A_8, D_{IN}
Input capacitance	C_{I2}			8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O			7	pF	D_{OUT}

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%; V_{SS} = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Power supply standby current	I_{CC2}			5	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = high impedance
Input leakage current	$I_{I(L)}$	−10		10	μA	Any input V_{IN} = 0 V to V_{CC}, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, V_{OUT} = 0 to 5.5 V
Output high (logic 1) voltage	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA
Output low (logic 0) voltage	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) voltage, all inputs	V_{IH}	2.4		5.5	V	
Input low (logic 0) voltage, all inputs	V_{IL}	−1.0		0.8	V	

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD41257-15 Min	Max	μPD41257-20 Min	Max	Unit	Test Conditions
Standard Operation							
Average power supply operating current	I_{CC1}		70		60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min (Note 5)
Average power supply current, refresh mode	I_{CC3}		60		55	mA	RAS cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	270		335		ns	(Note 6)
Read-write cycle time	t_{RWC}	310		390		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		150		200	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		75		100	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	40	0	50	ns	(Note 10)
Transition time (rise and fall)	t_T	3	35	3	50	ns	(Note 4)
RAS precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	75		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	75	10,000	100	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	150		200		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	30	75	35	100	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0		0		ns	(Note 12)
$\overline{CAS}$ precharge time	t_{CPN}	30		35		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address set-up time	t_{ASR}	0		0		ns	

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AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	Limits μPD41257-15 Min	Limits μPD41257-15 Max	Limits μPD41257-20 Min	Limits μPD41257-20 Max	Unit	Test Conditions
Row address hold time	t_{RAH}	20		25		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	45		55		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	120		155		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		25		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	120		155		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	45		55		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	45		55		ns	
Data-in set-up time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	45		55		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	120		155		ns	
Refresh period	t_{REF}		4		4	ms	
$\overline{WE}$ command set-up time	t_{WCS}	0		0		ns	(Note 15)
CAS to $\overline{WE}$ delay	t_{CWD}	75		100		ns	(Note 15)
RAS to $\overline{WE}$ delay	t_{RWD}	150		200		ns	(Note 15)
Nibble Mode Operation							
Average power supply current, nibble mode operation	I_{CC6}		27		27	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{NC} = t_{NC}$ min (Note 5)
Nibble mode cycle time	t_{NC}	70		100		ns	(Note 6)
Nibble mode access time	t_{NAC}		35		50	ns	(Note 7)
Nibble mode precharge time	t_{NP}	25		40		ns	
Nibble mode $\overline{WE}$ pulse width	t_{NWP}	30		40		ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NAS}	35		50		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD41257-15 Min	Limits μPD41257-15 Max	Limits μPD41257-20 Min	Limits μPD41257-20 Max	Unit	Test Conditions
Nibble mode RAS hold time	t_{NRSH}	35		50		ns	
Nibble mode CAS to $\overline{WE}$ delay	t_{NCWD}	35		50		ns	
Nibble mode $\overline{WE}$ to $\overline{CAS}$ lead time	t_{NCWL}	35		50		ns	
CAS Before RAS Refresh Operation							
Average power supply current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode	I_{CC4}		60		55	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IL}, t_{RC} = t_{RC} min (Note 5)
$\overline{CAS}$ set-up time for CAS before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		30		ns	

Note:

(1) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(2) AC measurements assume t_T = 5 ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(4) All voltages referenced to V_{SS}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

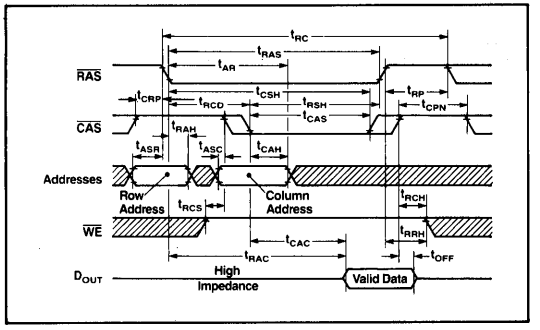
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output pin will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pins(at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

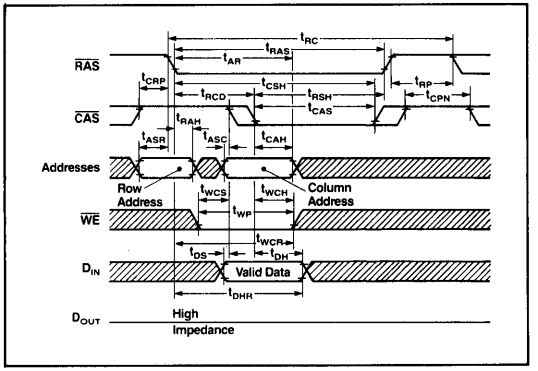
5

Timing Waveforms

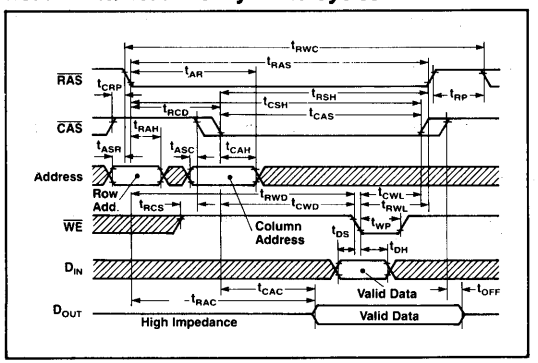
Read Cycle



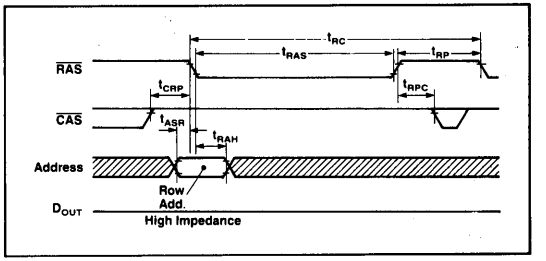
Write Cycle (Early Write)



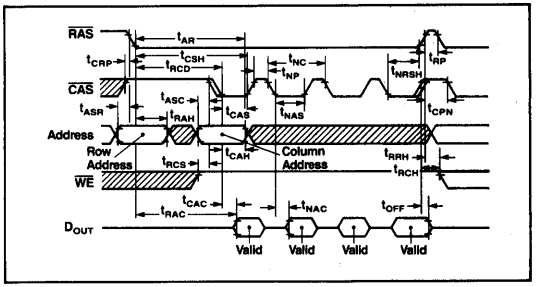
Read-Write/Read-Modify-Write Cycles



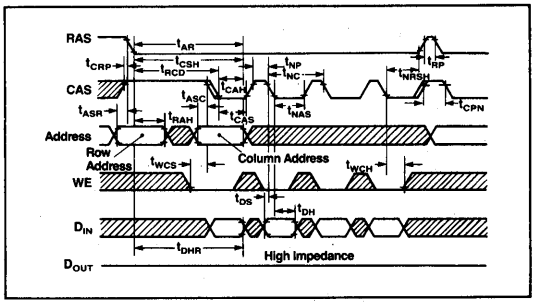
RAS-Only Refresh Cycle



Nibble Mode Read Cycle

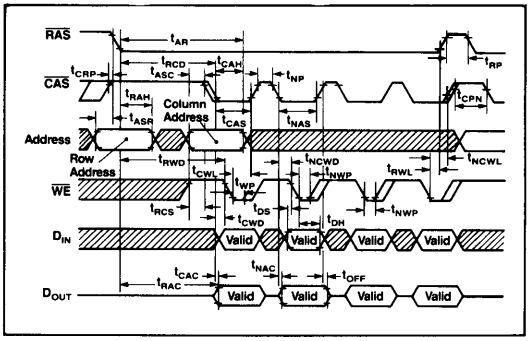


Nibble Mode Write Cycle

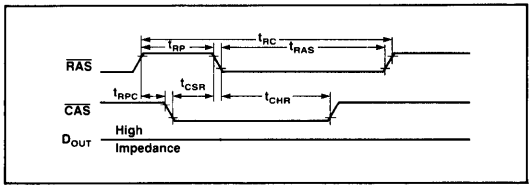


Timing Waveforms (cont)

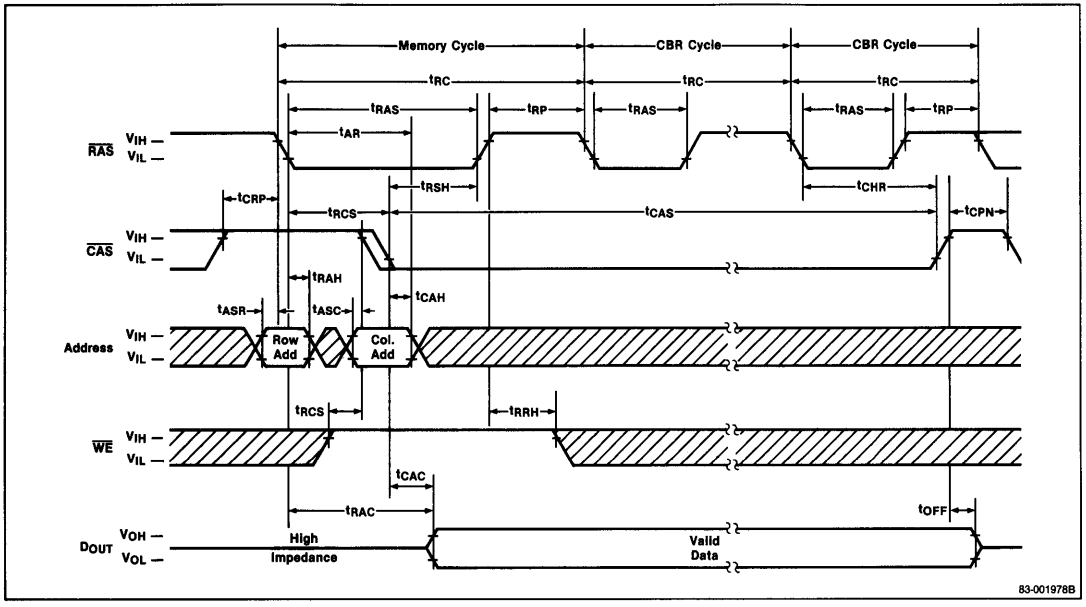
Nibble Mode Read-Modify-Write Cycle



CAS Before RAS Refresh Cycle



Hidden Refresh Cycle



5

μPD41416
16,384 x 4-BIT DYNAMIC NMOS RAM

Revision 2

Description

The μPD41416 is a 16,384-word by 4-bit dynamic N-channel MOS RAM designed to operate from a single +5 V power supply. The negative voltage substrate bias is internally generated; its operation is both automatic and transparent. The μPD41416 utilizes a double-polylayer, N-channel, silicon gate process which provides high storage cell density, high performance, and high reliability.

The μPD41416 uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation. Refresh is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0-A_6 during the refresh period of 2 milliseconds.

Multiplexed address inputs permit the μPD41416 to be packaged in a standard 18-pin dual-in-line package for high system bit density.

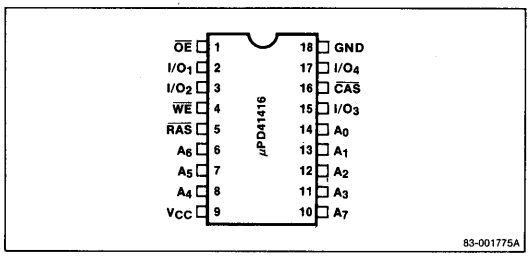
Features

- ☐ 16,384-word × 4-bit organization
- ☐ Single +5 V power supply ±10%
- ☐ Standard 18-pin plastic package
- ☐ $\overline{CAS}$, $\overline{OE}$ or early write mode to control D_{OUT} buffer impedance
- ☐ Low power dissipation,
  - —Active (t_{RC} = min): 303 mW
  - —Standby: 28 mW
- ☐ Read, write, read-write, read-modify-write. $\overline{RAS}$-only refresh, hidden refresh, and page mode capabilities
- ☐ 128 refresh cycles during 2 ms period

Performance Ranges

Device	t_{RAC}	t_{CAC}	t_{OEA}
μPD41416-12	120 ns	60 ns	30 ns
μPD41416-15	150 ns	75 ns	40 ns
μPD41416-20	200 ns	100 ns	50 ns

Pin Configuration



Pin Identification

No.	Symbol	Function
1	$\overline{OE}$	Output enable
2-3, 15, 17	I/O_1-I/O_4	Data input/output
4	$\overline{WE}$	Write enable
5	$\overline{RAS}$	Row address strobe
6-8, 10-14	A_0-A_7	Address inputs: A_0-A_5 = Column address inputs A_0-A_6 = Refresh address A_0-A_7 = Row address inputs
9	V_{CC}	+5 V power supply
16	$\overline{CAS}$	Column address strobe
18	GND	Ground

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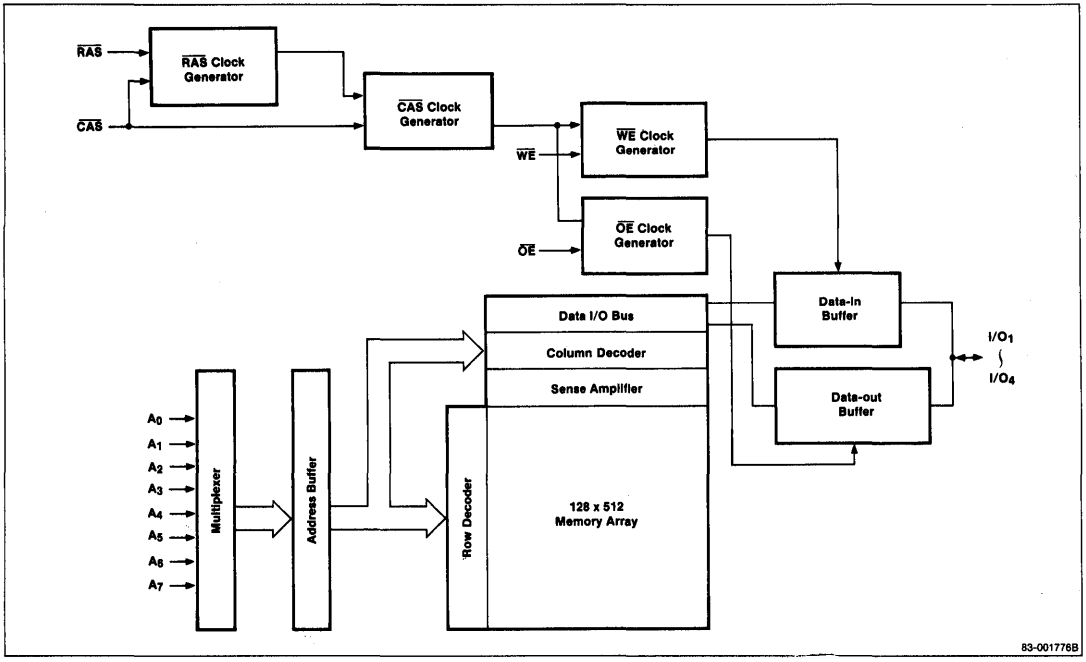
Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 V to +7.0 V
Storage temperature, T_{STG}	−55°C to 125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\,V \pm 10\%$; $f = 1.0\,MHz$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance, address inputs	C_{I1}			5	pF	
Input capacitance, strobe inputs	C_{I2}			8	pF	
Input/output capacitance, data ports	$C_{I/O}$			7	pF	

DC Characteristics

$T_A = 0°C$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage, high	V_{CC}	4.5	5.0	5.5	V	
Supply voltage, low	GND	0	0	0	V	
Standby supply current	I_{CC2}			5.0	mA	$\overline{RAS} = V_{IH}$, D_{OUT} = High impedance
Input leakage current	$I_{I(L)}$	−10		10	μA	$0\,V \leq V_{IN} \leq V_{CC}$, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, $0\,V \leq V_{OUT} \leq +5.5\,V$
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2\,mA$
Output voltage, high	V_{OH}	2.4			V	$I_{OUT} = -2\,mA$
Input voltage, low	V_{IL}	−1.0		0.8	V	
Input voltage, high	V_{IH}	2.4		5.5	V	

AC Characteristics (Notes 2, 3, 4)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\,V \pm 10\%$ (Note 1)

Parameter	Symbol	Limits μPD41416-12 Min	Limits μPD41416-12 Max	Limits μPD41416-15 Min	Limits μPD41416-15 Max	Limits μPD41416-20 Min	Limits μPD41416-20 Max	Unit	Test Conditions
Operating supply current, average	I_{CC1}		55		50		45	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min, (Note 5)
Operating supply current, refresh mode, average	I_{CC3}		45		40		35	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min, (Note 5)
Operating supply current, page mode operation, average	I_{CC4}		45		40		35	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min, (Note 5)
Random read or write cycle time	t_{RC}	220		260		330		ns	(Note 6)
Read-write cycle time	t_{RWC}	300		355		445		ns	(Note 6)
Page mode cycle time	t_{PC}	120		145		180		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		120		150		200	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75		100	ns	(Notes 7, 9)
Output turn-off delay from $\overline{CAS}$	t_{OFF}	0	30	0	40	0	50	ns	(Note 10)
Transition time, rise and fall	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}		90		100		120	ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	100	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		200		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	30	100	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0		0		0		ns	(Note 12)
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	25		25		30		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	50		60		70		ns	
$\overline{RAS}$ precharge, $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	15		15		20		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	20		25		30		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		130		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	35		45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95		120		155		ns	
Write command pulse width	t_{WP}	35		45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		55		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		55		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)

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AC Characteristics (Notes 2, 3, 4) (cont)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0\,V \pm 10\%$ (Note 1)

Parameter	Symbol	Limits μPD41416-12 Min	Limits μPD41416-12 Max	Limits μPD41416-15 Min	Limits μPD41416-15 Max	Limits μPD41416-20 Min	Limits μPD41416-20 Max	Unit	Test Conditions
Data-in hold time	t_{DH}	35		45		55		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	95		120		155		ns	
Refresh period	t_{REF}		2		2		2	ms	
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	95		120		155		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	155		195		255		ns	
Access time from $\overline{OE}$	t_{OEA}	30		40		50		ns	
Data delay time	t_{OED}	30		40		50		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turn-off delay from $\overline{OE}$	t_{OEZ}	0	30	0	40	0	50	ns	(Note 10)

Notes:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3} and I_{CC4} depend on output loading and cycle rates. Specified values are obtained with the outputs open.

(6) The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_A = 0°C$ to $70°C$) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

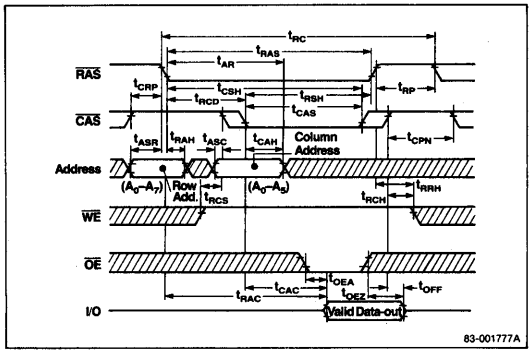
(12) t_{CRP} requirement should be applicable for $\overline{RAS}$, $\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

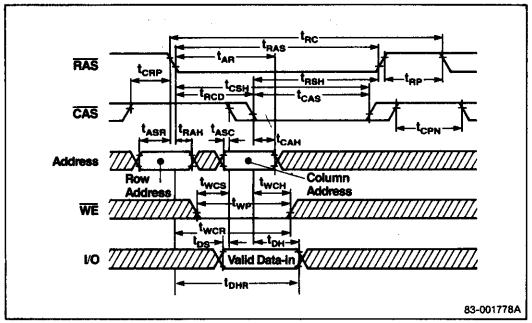
(14) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

Timing Waveforms

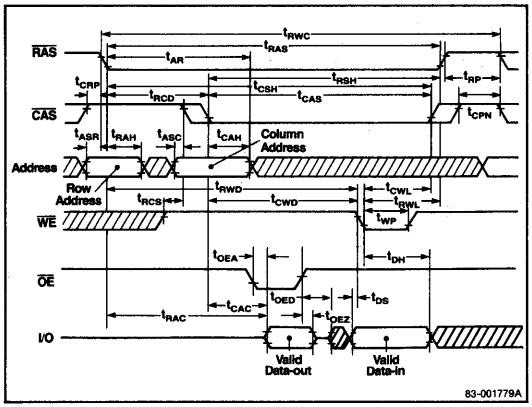
Read Cycle



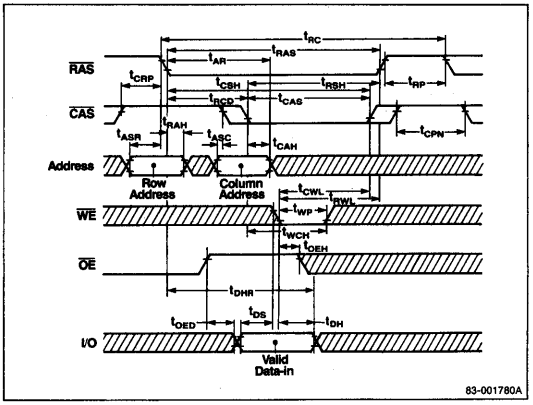
Write Cycle (Early Write)



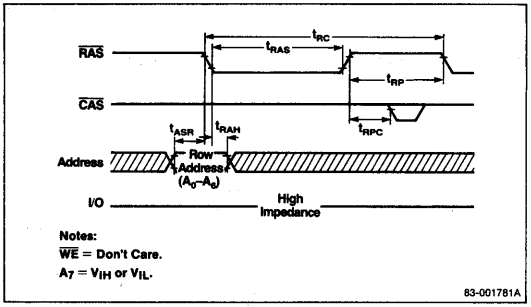
Read-Write/Read-Modify-Write Cycle



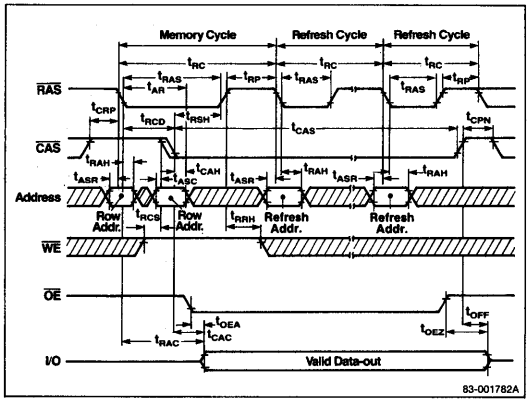
OE-Controlled Write Cycle



"RAS-Only" Refresh Cycle



Hidden Refresh Cycle



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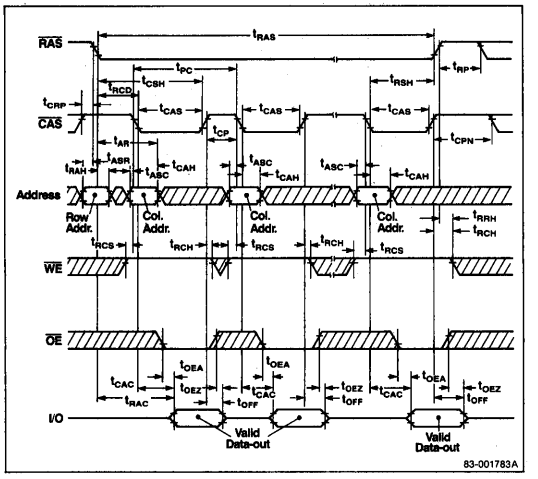
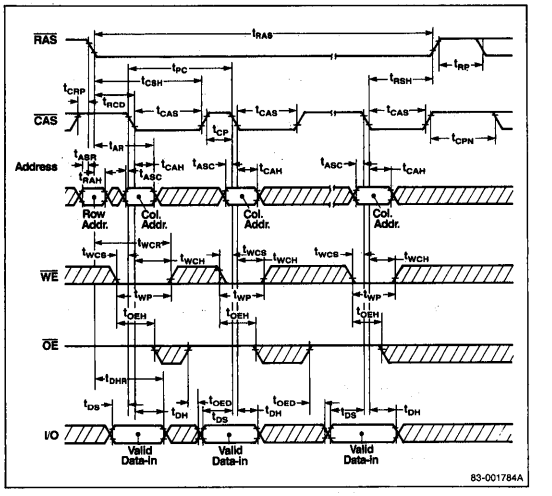
Timing Waveforms (cont)

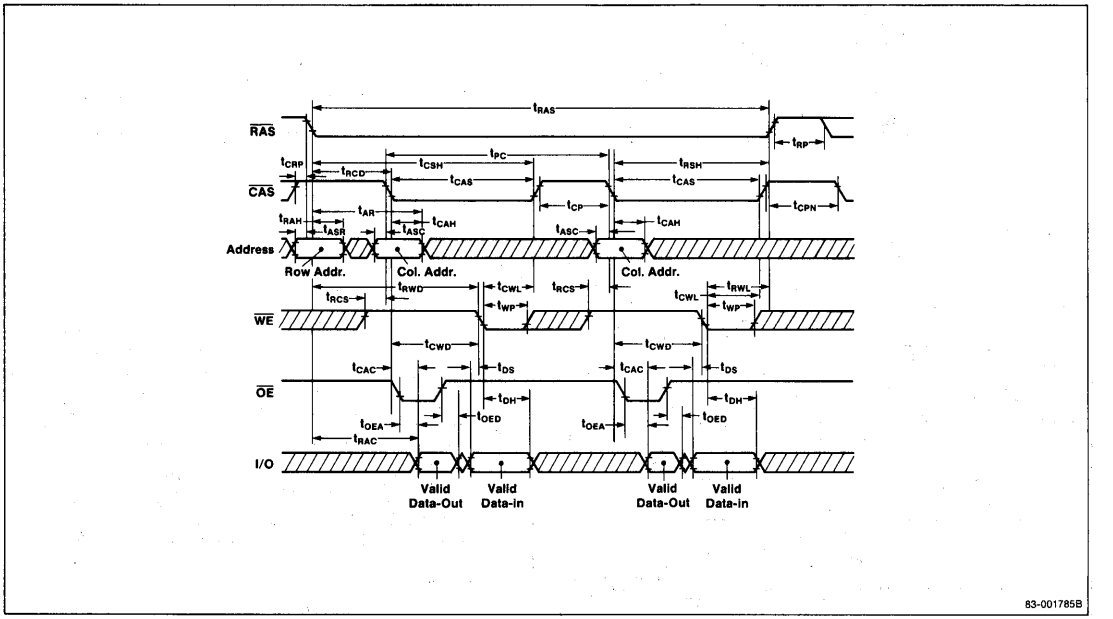
Page Mode Read Cycle



Page Mode Write Cycle (Early Write)



Page Mode Read-Write/Read-Modify-Write Cycle



μPD41464
65,536 x 4-BIT
DYNAMIC NMOS RAM

Revision 1

Description

The μPD41464 is a 65,536-word by 4-bit dynamic N-channel MOS random access memory (RAM) designed to operate from a single +5 V power supply. The negative voltage substrate bias is generated internally; its operation is automatic and transparent. The μPD41464 utilizes double polylayer N-channel silicon gate processing which provides high storage cell density, high performance, and high reliability. The device also uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation.

The three-state I/O is controlled by $\overline{CAS}$ independently of $\overline{RAS}$. After a valid read or hidden refresh cycle, data is held on the I/O by holding $\overline{CAS}$ low. The data I/O is returned to the high-impedance state by returning $\overline{CAS}$ high. The μPD41464 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh is accomplished by using $\overline{CAS}$ before $\overline{RAS}$ cycles, enabling the internal generation of the refresh address. Refresh can also be accomplished by using $\overline{RAS}$-only refresh or normal read or write cycles on the 256 address combinations of A_0-A_7 during the 4 ms refresh period.

Features

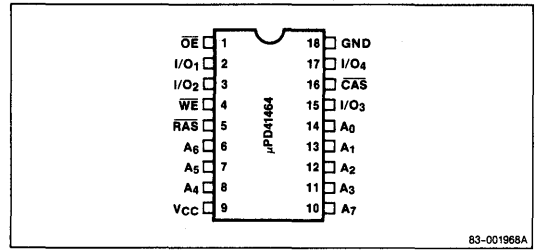
- ☐ 65,536-word by 4-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 18-pin DIP and PLCC packages
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Low power dissipation:
  - — 28 mW (standby)
  - — 440 mW (active, $t_{RC} = t_{RC}$ min)
- ☐ Non-latched TTL-compatible I/O
- ☐ Low input capacitance
- ☐ 256 refresh cycles during 4 ms period

Performance Ranges

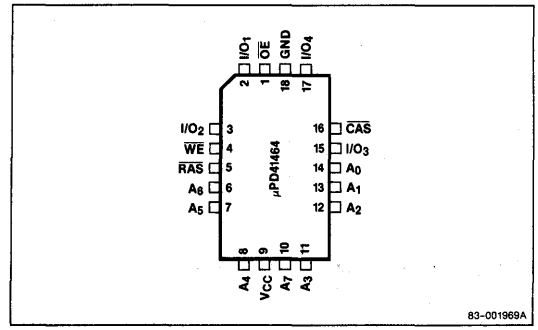
Device	t_{RAC}	t_{CAC}	t_{OEA}	I_{CC1}
μPD41464-10	100 ns	50 ns	25 ns	80 mA
μPD41464-12	120 ns	60 ns	30 ns	75 mA
μPD41464-15	150 ns	75 ns	40 ns	70 mA

Pin Configurations

18-Pin DIP



18-Pin PLCC



Pin Identification

No.	Symbol	Function
1	$\overline{OE}$	Output enable
2, 3, 15, 17	I/O_1-I/O_4	Data I/O
4	$\overline{WE}$	Write enable
5	$\overline{RAS}$	Row address strobe
6-8, 10-14	A_0-A_7	Address inputs
9	V_{CC}	Power supply
16	$\overline{CAS}$	Column address strobe
18	GND	Ground

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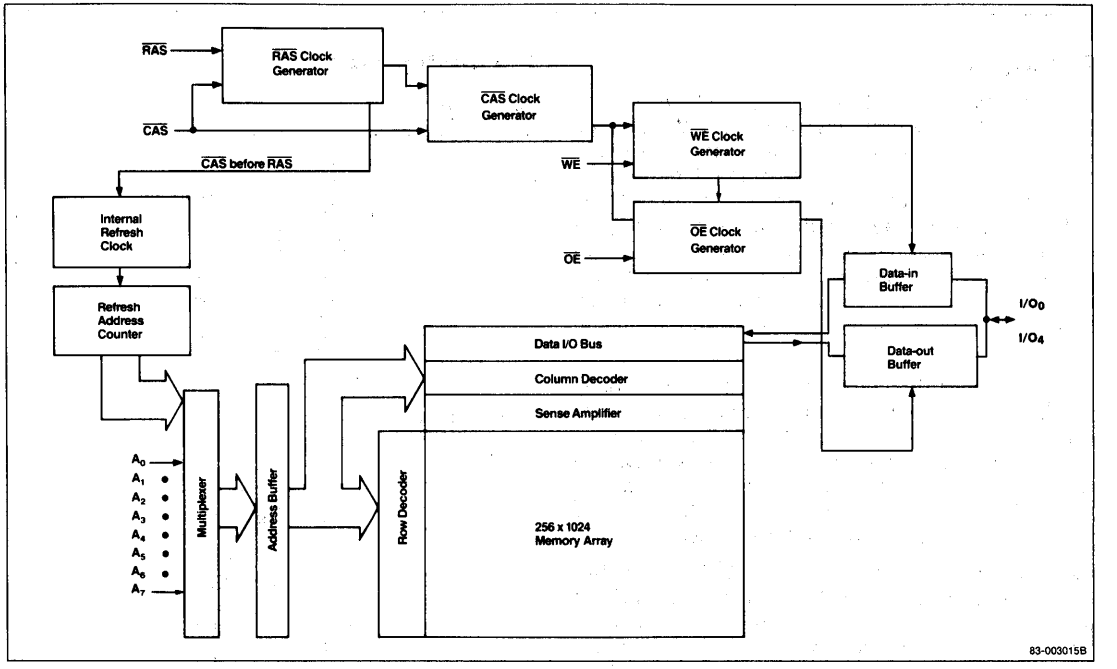
Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25$ °C, f = 1 MHz

		Limits				Test
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Input capacitance	C_{I1}			5	pF	A_0-A_7
Input capacitance	C_{I2}			8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O			7	pF	I/O_1-I/O_4

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input high voltage	V_{IH}	2.4		5.5	V	Referenced to GND
Input low voltage	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			5.0	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	I/O is High-Z, $V_{I/O}$ = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OL} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	μPD41464-10 Min	Max	μPD41464-12 Min	Max	μPD41464-15 Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		80		75		70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh mode, average	I_{CC3}		65		60		55	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page mode, average	I_{CC4}		55		50		45	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		70		65		60	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IL}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	200		220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	270		300		355		ns	(Note 6)
Page mode cycle time	t_{PC}	100		120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	40	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 3)
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to CAS delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to RAS precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	40		50		60		ns	

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AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	μPD41464-10		μPD41464-12		μPD41464-15		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	25		30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		90		115		ns	
Write command pulse width	t_{WP}	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	35		40		45		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	25		30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	75		90		115		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		195		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	80		95		120		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		25		30		40	ns	
Data delay time	t_{OED}	25		30		40		ns	
OE command hold time	t_{OEH}	0		0		0		ns	
Output turn-off delay from $\overline{OE}$	t_{OEZ}	0	25	0	30	0	40	ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	20		25		30		ns	

Note:

(1) An initial pause of 100 μs ($\overline{RAS}$ inactive) is required after power-up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved.

(2) AC measurements assume $t_T = 5$ ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

(4) All voltages referenced to GND.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. For lot code K of μPD41464-15, t_{RC} min must be 270 ns and I_{CC3} = 60 mA.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured. For lot code K of μPD41464-15, t_{RC} min must be 270 ns.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

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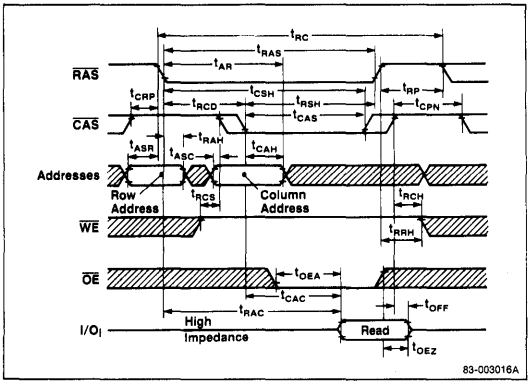
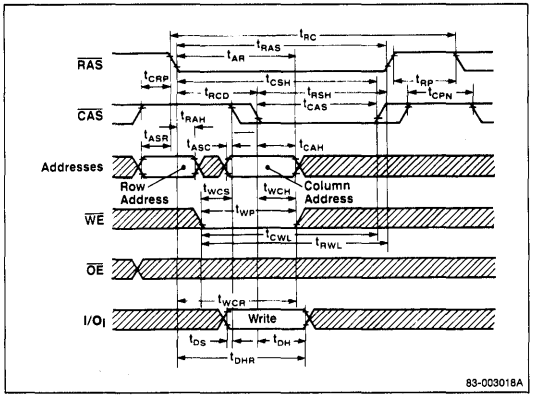
Timing Waveforms

Read Cycle

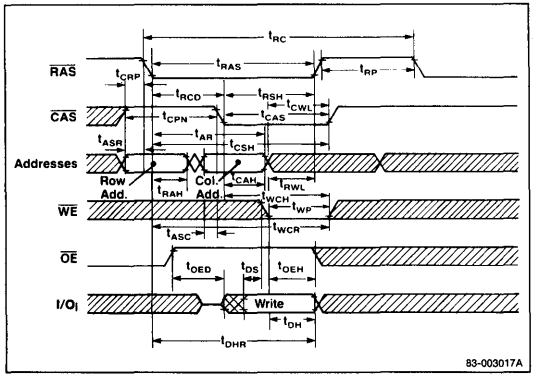


Write Cycle (Early Write)

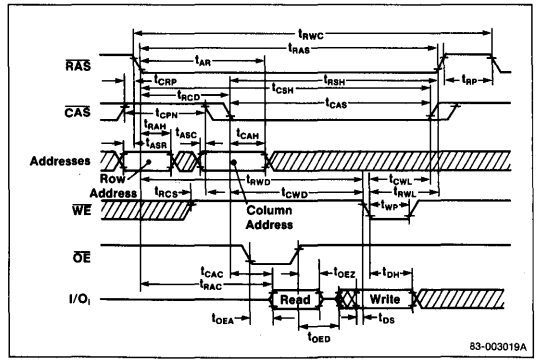


Timing Waveforms (cont)

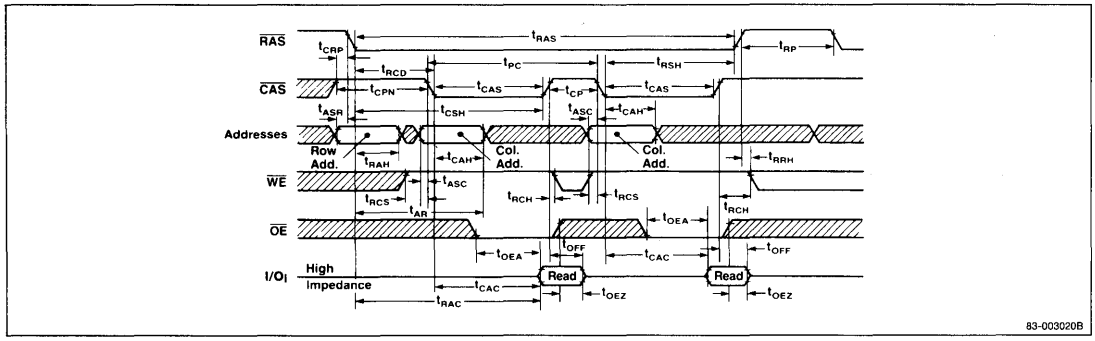
$\overline{OE}$-Controlled Write Cycle



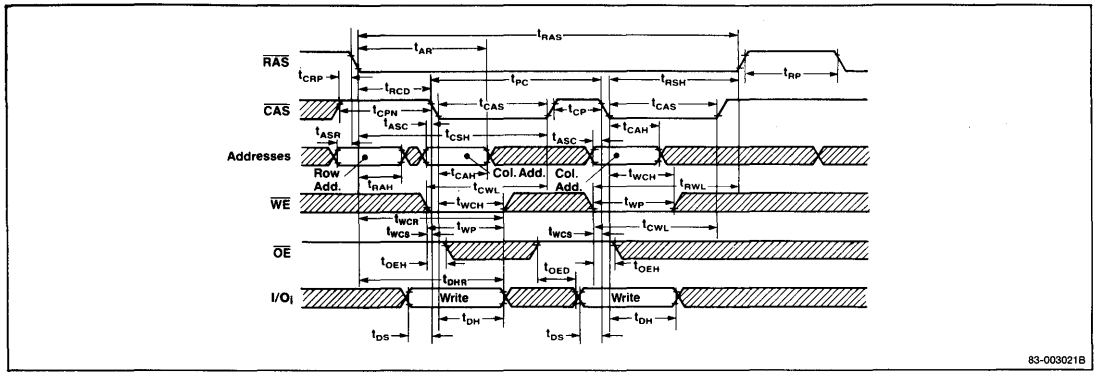
Read-Write/Read-Modify-Write Cycle



Page Mode Read Cycle

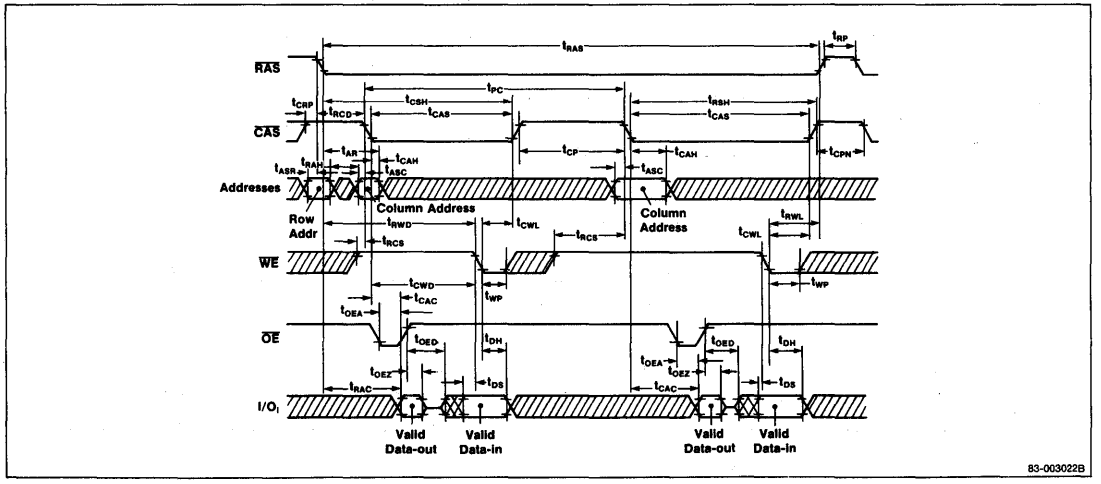


Page Mode Write Cycle (Early Write)

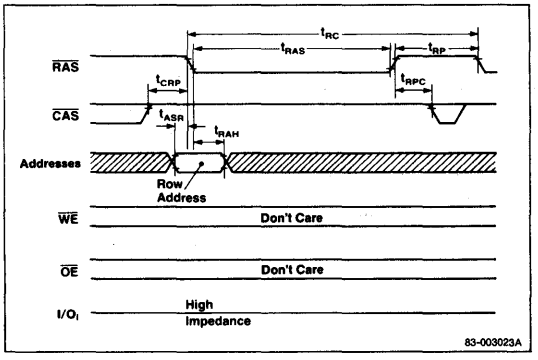


Timing Waveforms (cont)

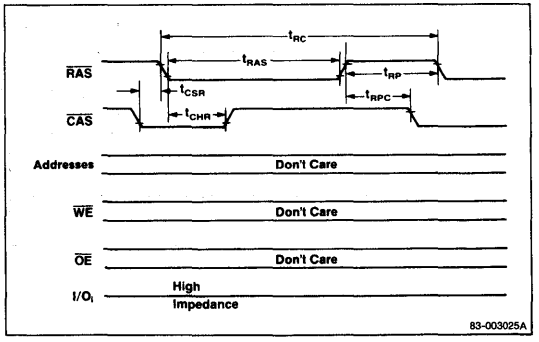
Page Mode Read-Write/Read-Modify-Write Cycle



RAS-Only Refresh Cycle



CAS Before RAS Refresh Cycle



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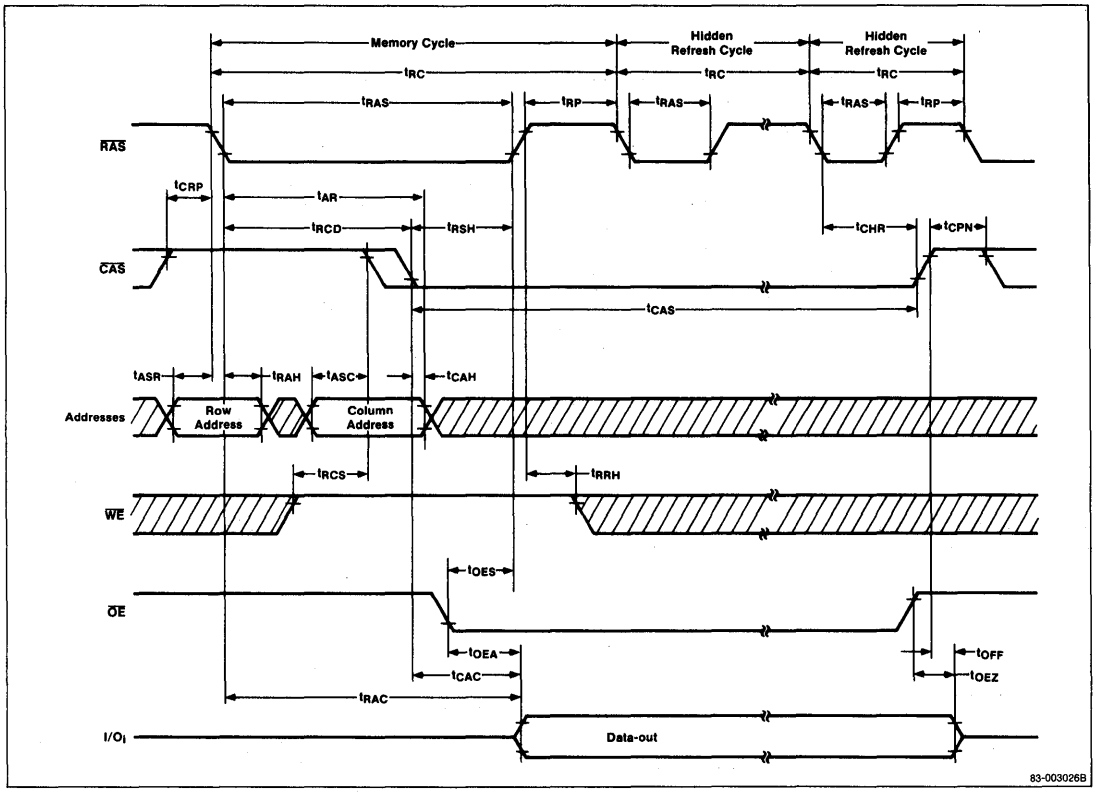
Timing Waveforms (cont)

Hidden Refresh Cycle



μPD411000
1,048,576 x 1-BIT
DYNAMIC NMOS RAM

PRELIMINARY INFORMATION

Description

The μPD411000 is a page mode version 1,048,576-word by 1-bit dynamic N-channel MOS random access memory (RAM). It is designed to operate from a single +5 V power supply. The negative voltage substrate bias is automatically generated internally. The μPD411000 utilizes advanced double-level polycide technology. The use of trench capacitors minimizes silicon area while providing high storage cell density, high performance, and high reliability. The device uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation.

The three-state output is controlled by $\overline{CAS}$ independently of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to the high-impedance state by returning $\overline{CAS}$ high. Hidden refresh allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh may be accomplished by using a $\overline{CAS}$ before $\overline{RAS}$ cycle, enabling the internal generation of the refresh address. Refresh can also be accomplished by using $\overline{RAS}$-only refresh or by a normal read or write cycle on the 512 address combinations of A_0-A_8 during the 8 ms refresh period.

Features

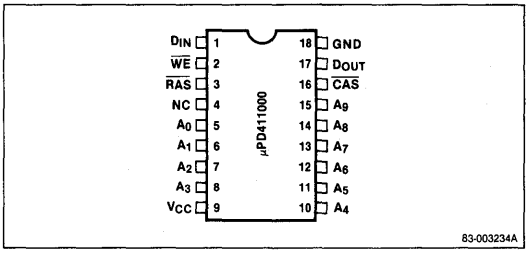
- ☐ 1,048,576-word by 1-bit organization
- ☐ Page mode operation
- ☐ High density 18-pin plastic DIP (μPD411000C) or 26/20-pin plastic SOJ (μPD411000LA)
- ☐ Single +5 V ±10% power supply
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Low power dissipation:
  — 28 mW standby (max)
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Non-latched TTL-compatible three-state output
- ☐ Low input capacitance
- ☐ TTL-compatible inputs
- ☐ 512 refresh cycles during 8 ms period

Performance Ranges

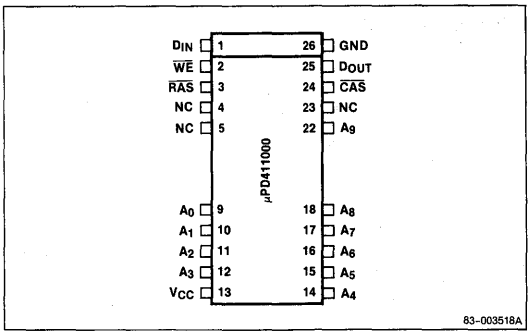
Device	Row Access Time (Max)	R/W Cycle (Min)	RMW Cycle (Min)	Page Mode Cycle (Min)
μPD411000-10	100 ns	200 ns	270 ns	100 ns
μPD411000-12	120 ns	220 ns	300 ns	120 ns
μPD411000-15	150 ns	260 ns	355 ns	145 ns

Pin Configurations

18-Pin Plastic DIP



26/20-Pin SOJ



Pin Identification

Plastic DIP

No.	Symbol	Function
1	D_{IN}	Data input
2	$\overline{WE}$	Write enable
3	$\overline{RAS}$	Row address strobe
4	NC	No connection
5-8, 10-15	A_0-A_9	Address inputs
9	V_{CC}	Power supply
16	$\overline{CAS}$	Column address strobe
17	D_{OUT}	Data output
18	GND	Ground

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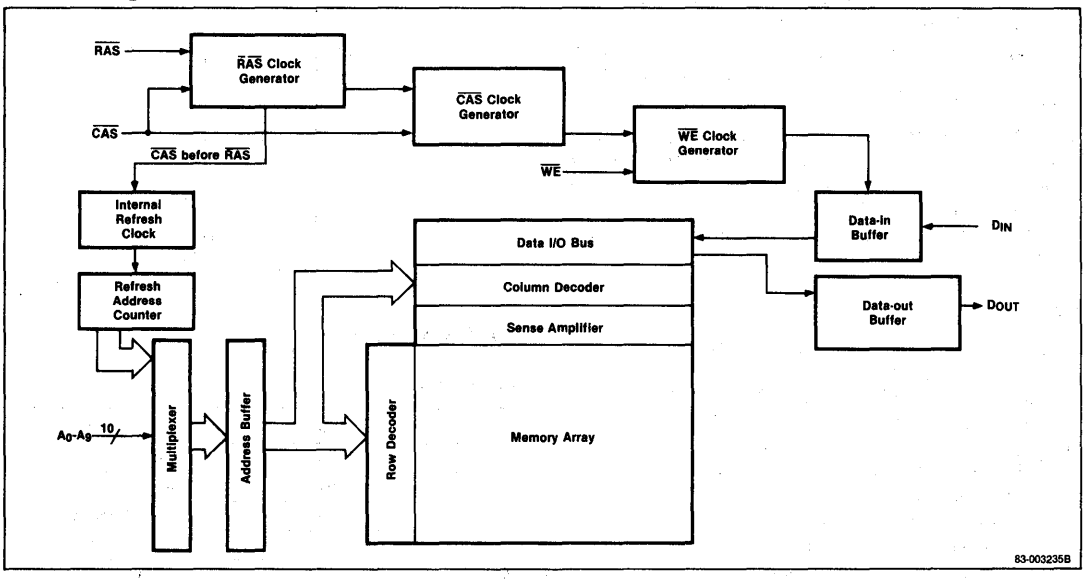
Pin Identification (cont)

Plastic SOJ

No.	Symbol	Function
1	D_{IN}	Data input
2	$\overline{WE}$	Write enable
3	$\overline{RAS}$	Row address strobe
4, 5, 23	NC	No connection
6-8, 19-21	—	No external lead
9-12, 14-18, 22	A_0-A_9	Address inputs
13	V_{CC}	Power supply
24	$\overline{CAS}$	Column address strobe
25	D_{OUT}	Data output
26	GND	Ground

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short circuit output current	50 mA
Power dissipation, P_D	1 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, f = 1 MHz

Parameter	Symbol	Max	Unit	Test Conditions
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
Input capacitance	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_D	7	pF	D_{OUT}

DC Characteristics

$T_A = 0$ to +70°C; $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input high voltage	V_{IH}	2.4		5.5	V	Referenced to GND
Input low voltage	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			5.0	mA	$\overline{RAS} = V_{IH}$, D_{OUT} = Hi-Z
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OL} = 4.2 mA
Ouput high voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −5 mA

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD411000-10 Min	Limits μPD411000-10 Max	Limits μPD411000-12 Min	Limits μPD411000-12 Max	Limits μPD411000-15 Min	Limits μPD411000-15 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		100		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh mode, average	I_{CC3}		85		75		65	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page mode operation, average	I_{CC4}		85		75		65	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC6}		90		80		70	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	200		220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	270		300		355		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	40	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	20		25		30		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	25		30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		90		115		ns	
Write command pulse width	t_{WP}	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	35		40		45		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD411000-10 Min	Max	μPD411000-12 Min	Max	μPD411000-15 Min	Max	Unit	Test Conditions
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	25		30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	75		90		115		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	100		120		150		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	50		60		75		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	20		25		30		ns	
Page cycle time	t_{PC}	100		120		145		ns	(Note 6)
$\overline{CAS}$ precharge time, page cycle	t_{CP}	40		50		60		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

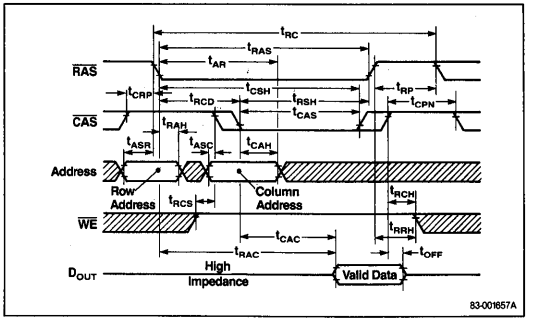
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

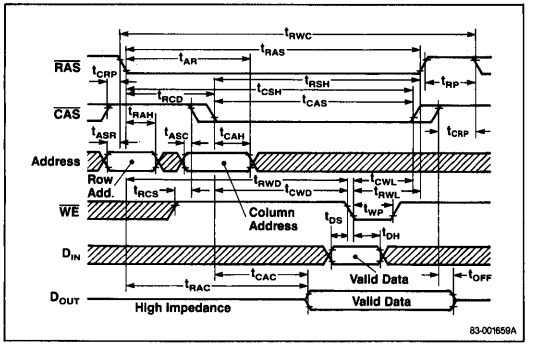
5

Timing Waveforms

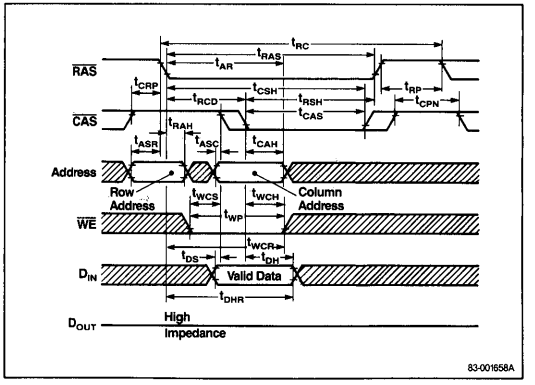
Read Cycle



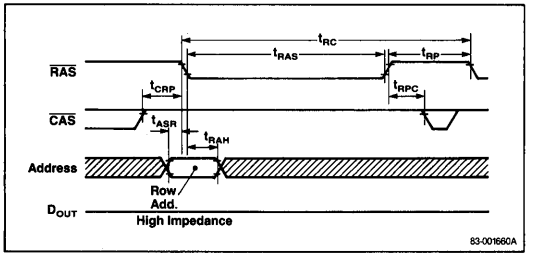
Read-Write/Read-Modify-Write Cycle



Write Cycle (Early Write)

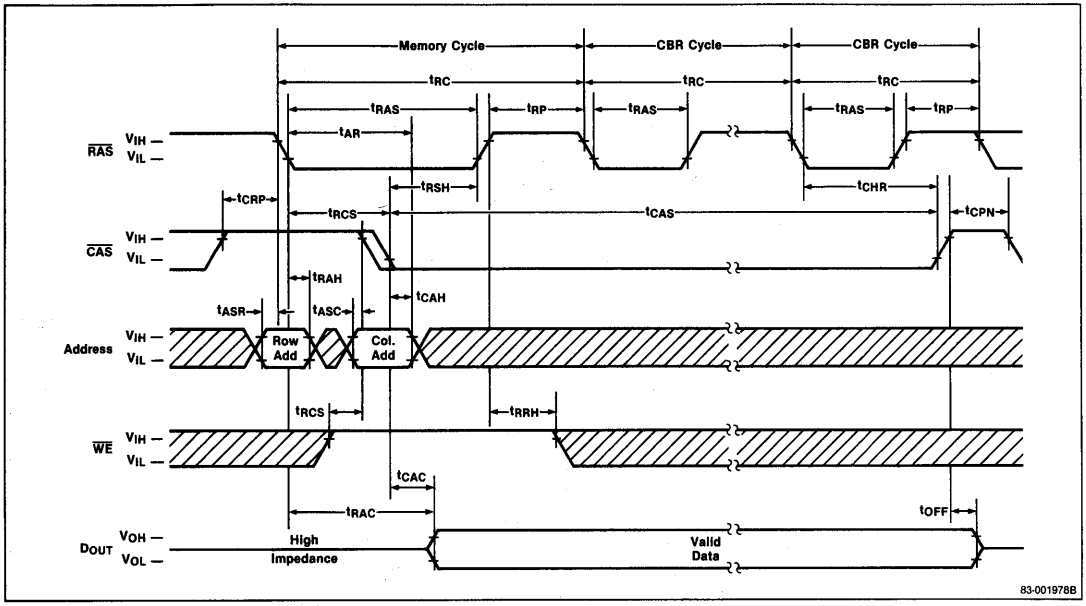


RAS-Only Refresh Cycle

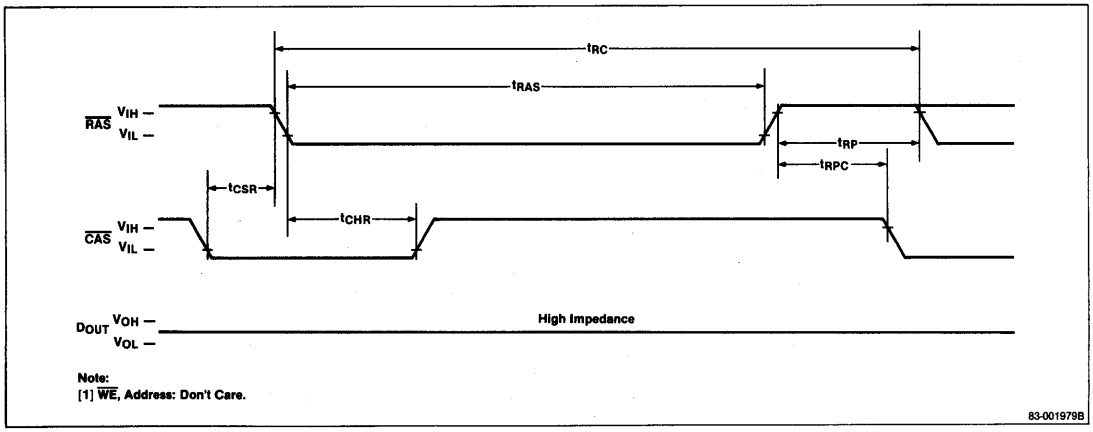


Timing Waveforms (cont)

Hidden Refresh Cycle



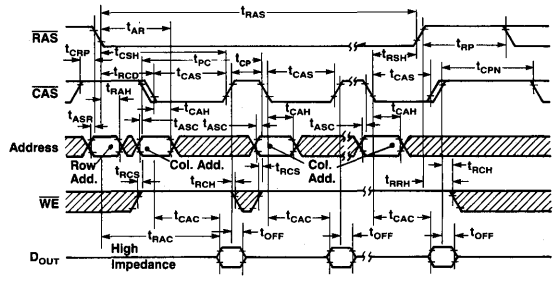
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



5

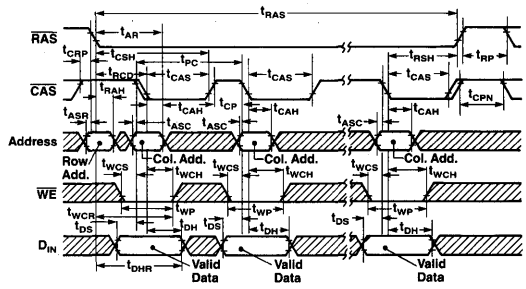
Timing Waveforms (cont)

Page Mode Read Cycle



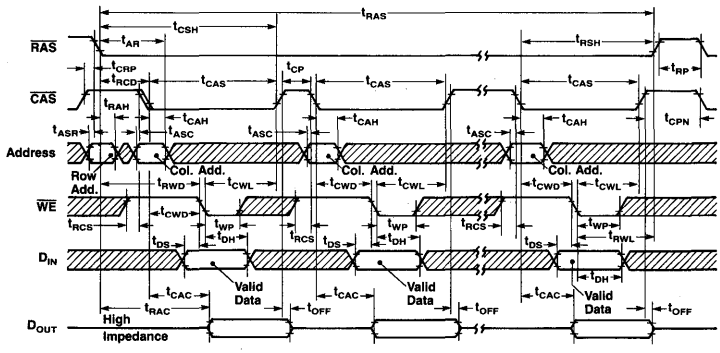
83-001661B

Page Mode Write Cycle (Early Write)



83-001662B

Page Mode Read-Write/Read-Modify-Write Cycle



83-001664B

μPD411001
1,048,576 x 1-BIT
DYNAMIC NMOS RAM

PRELIMINARY INFORMATION

Description

The μPD411001 is a nibble mode version 1,048,576-word by 1-bit dynamic N-channel MOS random access memory (RAM). It is designed to operate from a single +5 V power supply. The negative voltage substrate bias is automatically generated internally. The μPD411001 utilizes advanced double-level polycide technology. The use of trench capacitors minimizes silicon area while providing high storage cell density, high performance, and high reliability. The device uses a single transistor dynamic storage cell and advanced dynamic circuitry throughout, ensuring minimum power dissipation.

The three-state output is controlled by $\overline{CAS}$ independently of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to the high-impedance state by returning $\overline{CAS}$ high. Hidden refresh allows $\overline{CAS}$ to be held low to maintain output data while RAS is used to execute $\overline{RAS}$-only refresh cycles.

Refresh may be accomplished by using a $\overline{CAS}$ before $\overline{RAS}$ cycle, enabling the internal generation of the refresh address. Refresh can also be accomplished by using $\overline{RAS}$-only refresh or by normal read or write cycles on the 512 address combinations of A_0-A_8 during the 8 ms refresh period.

Features

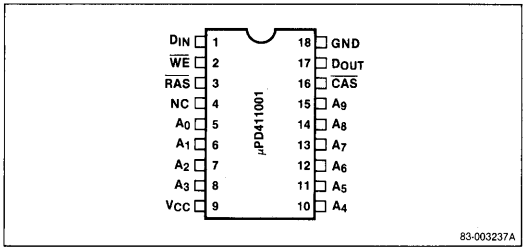
- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Nibble mode operation
- ☐ High density 18-pin plastic DIP (μPD411001C) or 26/20-pin SOJ (μPD411001LA)
- ☐ Low power dissipation:
  — 28 mW standby (max)
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Non-latched TTL-compatible three-state output
- ☐ Low input capacitance
- ☐ TTL-compatible inputs
- ☐ 512 refresh cycles during 8 ms period

Performance Ranges

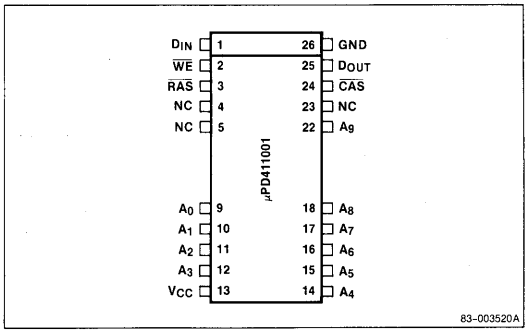
Device	Row Access Time (max)	Read/Write Cycle (min)	RMW Cycle (min)	Nibble Mode Access Time (max)
μPD411001-10	100 ns	200 ns	270 ns	25 ns
μPD411001-12	120 ns	220 ns	300 ns	30 ns
μPD411001-15	150 ns	260 ns	355 ns	35 ns

Pin Configurations

18-Pin Plastic DIP



26/20-Pin Plastic SOJ



Pin Identification

Plastic DIP

No.	Symbol	Function
1	D_{IN}	Data input
2	$\overline{WE}$	Write enable
3	$\overline{RAS}$	Row address strobe
4	NC	No connection
5-8, 10-15	A_0-A_9	Address inputs
9	V_{CC}	Power supply
16	$\overline{CAS}$	Column address strobe
17	D_{OUT}	Data output
18	GND	Ground

5

Pin Identification (cont)

Plastic SOJ

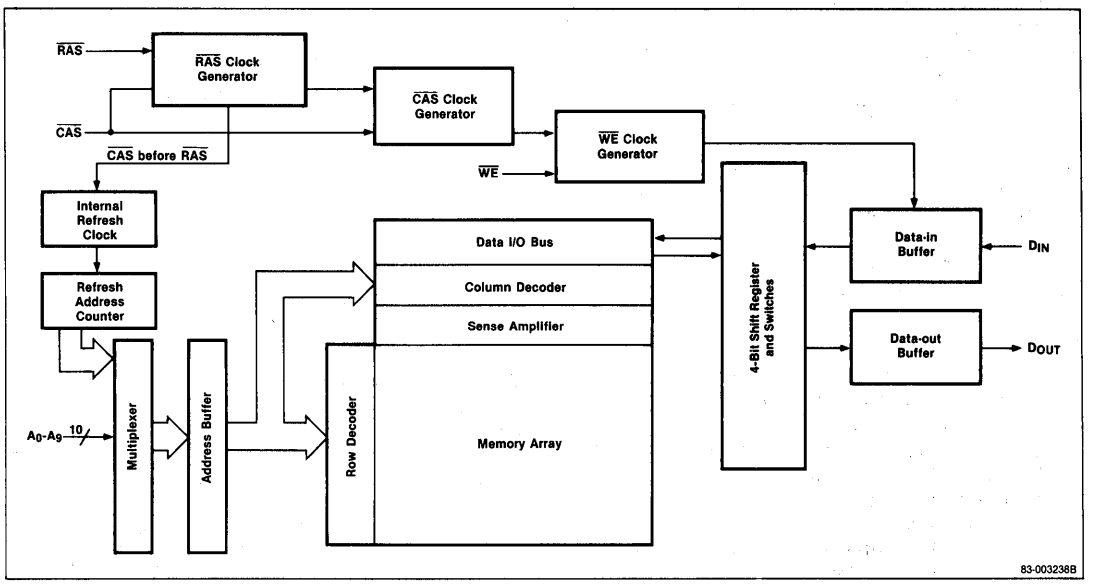
No.	Symbol	Function
1,2,24,25	I/O, $-I/O_4$	Data I/O
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
5	NC	No connection
6-8,19-21	—	No external lead
9-12,14-18,22	A_0-A_9	Address inputs
13	V_{CC}	Power supply
22	OE	Output enable
23	$\overline{CAS}$	Column address strobe
26	GND	Ground

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short circuit output current	50 mA
Power dissipation, P_D	1 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input high voltage	V_{IH}	2.4		5.5	V	Referenced to GND
Input low voltage	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			5.0	mA	$\overline{RAS} = V_{IH}$, D_{OUT} = Hi-Z
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, V_{OUT} = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	I_{OL} = 4.2 mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −5 mA

Capacitance

T_A = 25°C, f = 1 MHz

Parameter	Symbol	Max	Unit	Test Conditions
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
Input capacitance	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_D	7	pF	D_{OUT}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD411001-10 Min	Max	μPD411001-12 Min	Max	μPD411001-15 Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		100		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh mode, average	I_{CC3}		85		75		65	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, nibble mode operation, average	I_{CC5}		40		35		30	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{NC} = t_{NC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC6}		90		80		70	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	200		220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	270		300		355		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$, non-nibble cycle	t_{CAC}		50		60		75	ns	(Notes 7, 9)
Access time from $\overline{CAS}$, nibble mode cycle	t_{NAC}		25		30		35	ns	(Note 7)
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	40	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{RAS}$ hold time (nibble mode)	t_{NRSH}	25		30		35		ns	
$\overline{CAS}$ pulse width, non-nibble mode	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	

5

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD411001-10 Min	Max	μPD411001-12 Min	Max	μPD411001-15 Min	Max	Unit	Test Conditions
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time	t_{NP}	20		25		30		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	25		30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		90		115		ns	
Write command pulse width	t_{WP}	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		ns	
Write command to $\overline{CAS}$ lead time, non-nibble cycle	t_{CWL}	35		40		45		ns	
Write command to $\overline{CAS}$ lead time, nibble mode cycle	t_{NCWL}	25		30		35		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	25		30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	75		90		115		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	100		120		150		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay, non-nibble cycle	t_{CWD}	50		60		75		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay, nibble mode cycle	t_{NCWD}	25		30		35		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		10		ns	

AC Characteristics (cont)

T_A = 0 to +70 °C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD411001-10 Min	Limits μPD411001-10 Max	Limits μPD411001-12 Min	Limits μPD411001-12 Max	Limits μPD411001-15 Min	Limits μPD411001-15 Max	Unit	Test Conditions
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	20		25		30		ns	
Nibble mode cycle time	t_{NC}	55		65		75		ns	(Note 6)
$\overline{CAS}$ pulse width, nibble mode cycle	t_{NAS}	25	10000	30	10000	35	10000	ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8

Note:

(1) All voltages referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC5}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

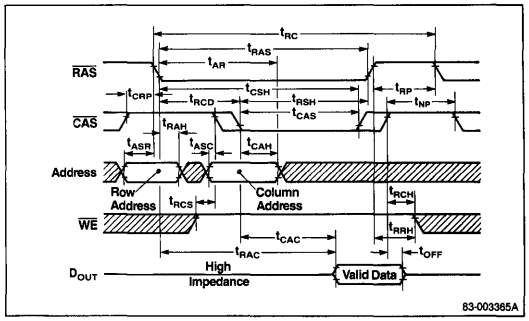
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{NCWD} are restrictive operating parameters in read-write/read-modify-write and nibble mode read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write or nibble mode early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If $t_{NCWD} \geq t_{NCWD}$ (min), the cycle is a nibble mode read-write cycle and the data output will contain data read from the selected cell. If none of the above conditions are met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

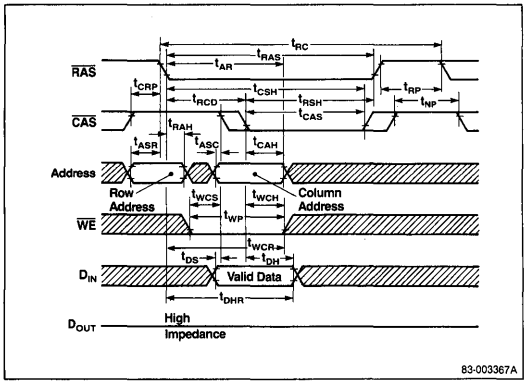
5

Timing Waveforms

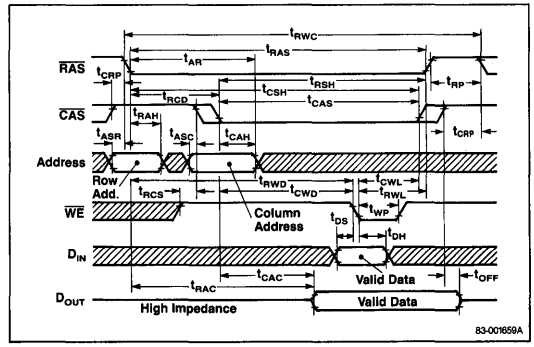
Read Cycle



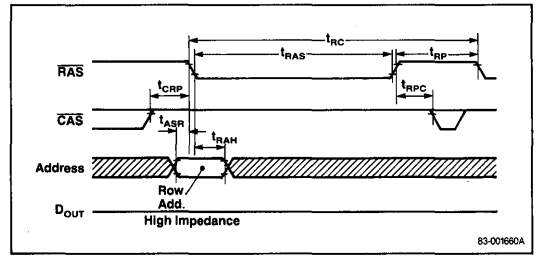
Write Cycle (Early Write)



Read-Write/Read-Modify-Write Cycle

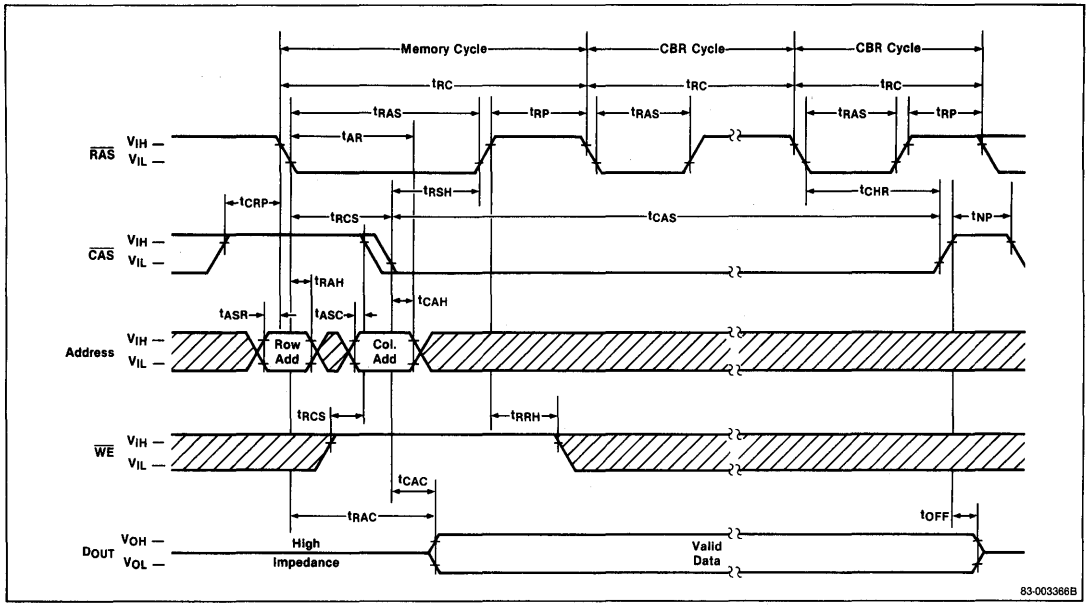


RAS-Only Refresh Cycle

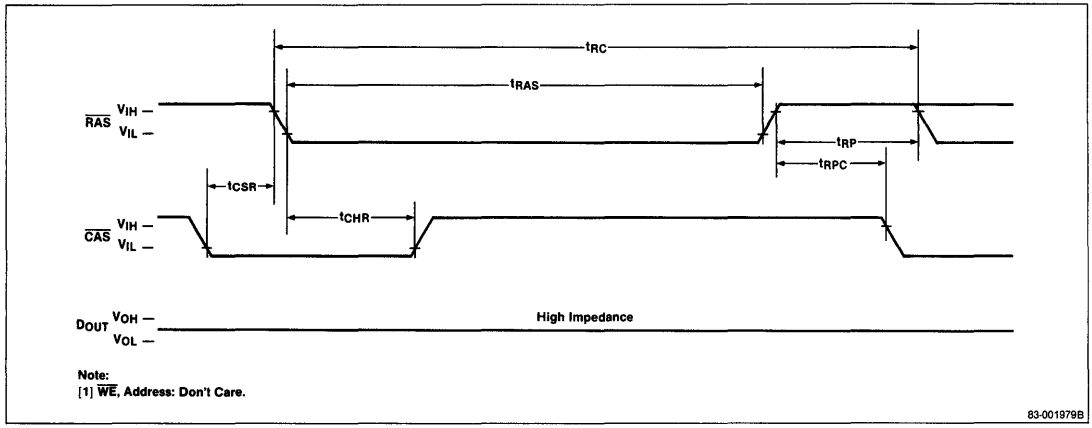


Timing Waveforms (cont)

Hidden Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

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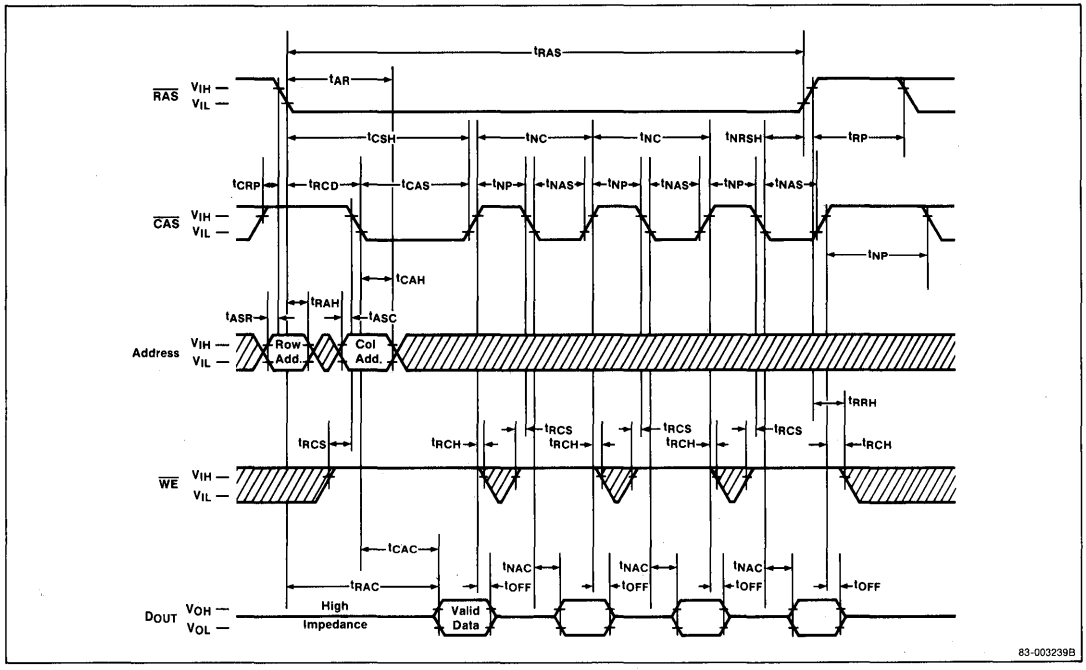
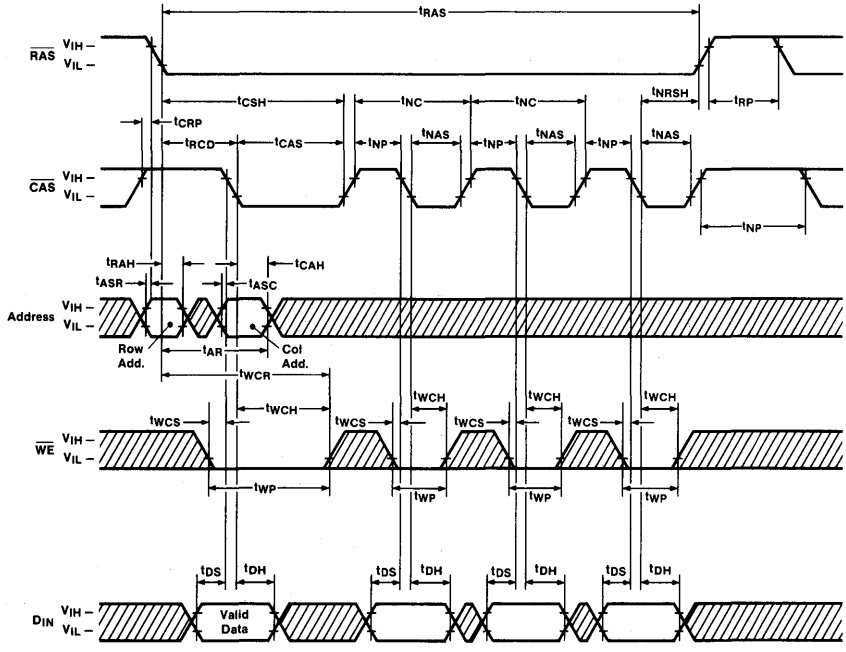
Timing Waveforms (cont)

Nibble Mode Read Cycle



Timing Waveforms (cont)

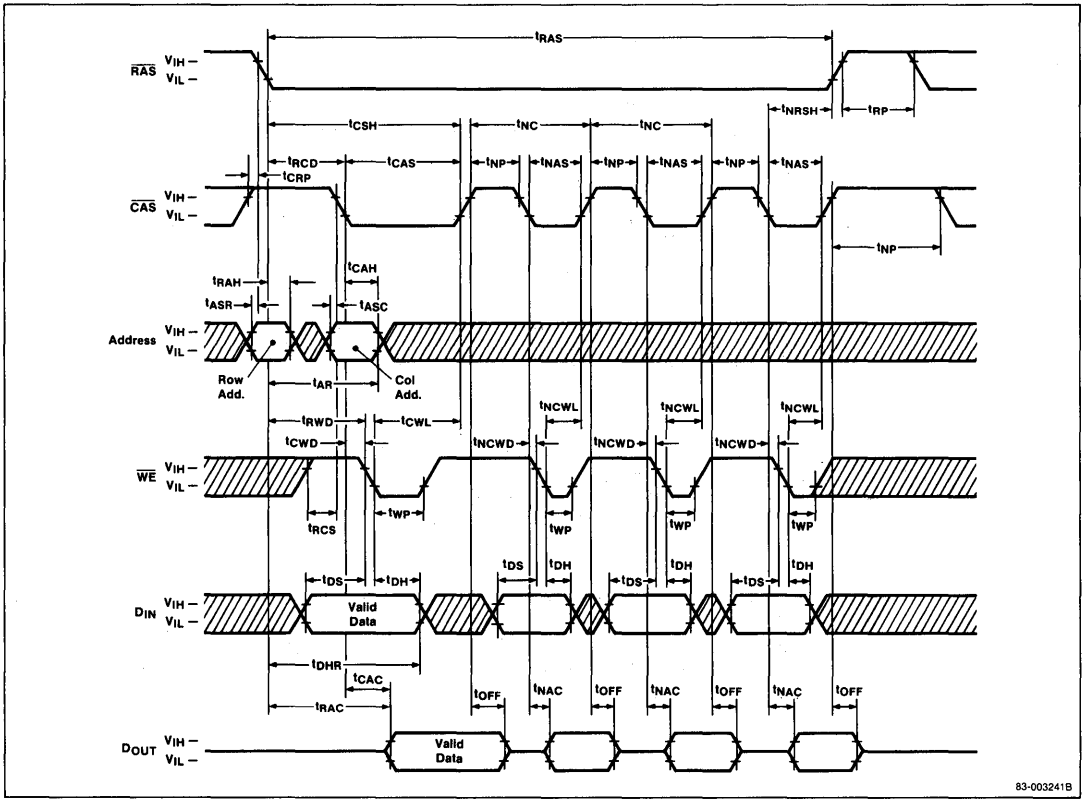
Nibble Mode Write Cycle (Early Write)



5

Timing Waveforms (cont)

Nibble Mode Read-Write/Read-Modify-Write Cycle



μPD414256
262,144 x 4-BIT
DYNAMIC NMOS RAM

PRELIMINARY INFORMATION

Description

The μPD414256 is a 262,144-word by 4-bit dynamic N-channel MOS random access memory (RAM) designed to operate from a single +5 V power supply. The negative voltage substrate bias is generated internally; its operation is automatic and transparent. The μPD414256 utilizes advanced double-level polycide technology. The use of trench capacitors minimizes silicon area while providing high storage cell density, high performance, and high reliability. The device uses advanced dynamic circuity throughout, ensuring minimum power dissipation.

The three-state I/O pins are controlled by $\overline{CAS}$ independently of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the I/O pins by holding $\overline{CAS}$ low. The data I/O pins are returned to the high-impedance state by returning $\overline{CAS}$ high. The μPD414256 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh is accomplished by using a $\overline{CAS}$ before $\overline{RAS}$ cycle, enabling the internal generation of the refresh address. Refresh can also be accomplished by using $\overline{RAS}$-only refresh or a normal read or write cycle on the 512 address combination of A_0-A_8 during the 8 ms refresh period.

Features

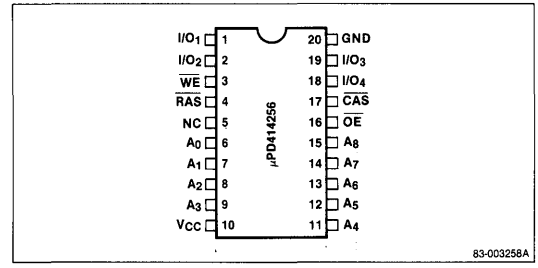
- ☐ 262,144-word by 4-bit organization
- ☐ Page mode operation
- ☐ High density 20-pin plastic DIP (μPD414256C) or 26/20-pin plastic SOJ (μPD414256LA)
- ☐ Single +5 V ±10% power supply
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Low power dissipation:
  - — 28 mW standby (max)
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Non-latched TTL-compatible I/O
- ☐ Low input capacitance
- ☐ TTL-compatible inputs
- ☐ 512 refresh cycles during 8 ms period

Performance Ranges

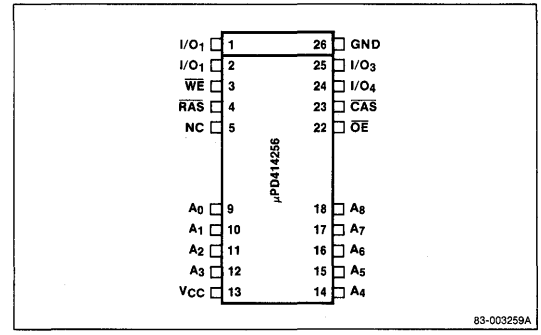
Device	Row Access Time (Max)	R/W Cycle (Min)	RMW Cycle (Min)	OE Access Time (Max)
μPD414256-10	100 ns	200 ns	270 ns	25 ns
μPD414256-12	120 ns	220 ns	300 ns	30 ns
μPD414256-15	150 ns	260 ns	355 ns	40 ns

Pin Configurations

20-Pin Plastic DIP



26/20-Pin SOJ



Pin Identification

Plastic DIP

No.	Symbol	Function
1, 2, 18, 19	I/O_1-I/O_4	Data I/O
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
5	NC	No connection
6-9, 11-15	A_0-A_8	Address inputs
10	V_{CC}	Power supply
16	$\overline{OE}$	Output enable
17	$\overline{CAS}$	Column address strobe
20	GND	Ground

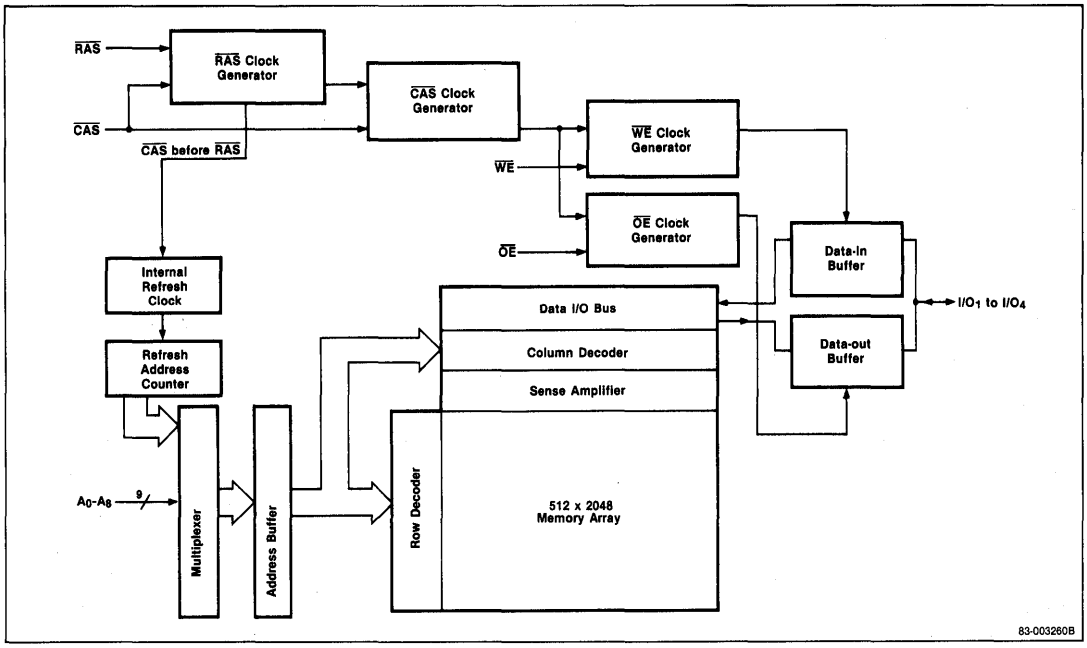
5

Pin Identification (cont)

Plastic SOJ

No.	Symbol	Function
1, 2, 24, 25	I/O_1-I/O_4	Data I/O
3	$\overline{WE}$	Write enable
4	$\overline{RAS}$	Row address strobe
5	NC	No connection
6-8, 19-21	—	No external lead
9-12, 14-18	A_0-A_8	Address inputs
13	V_{CC}	Power supply
22	$\overline{OE}$	Output enable
23	$\overline{CAS}$	Column address strobe
26	GND	Ground

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Short circuit output current	50 mA
Power dissipation, P_D	1 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25$ °C, f = 1 MHz

Parameter	Symbol	Max	Unit	Test Conditions
Input capacitance	C_{I1}	5	pF	Address
Input capacitance	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_D	7	pF	Input/output

DC Characteristics

$T_A = 0$ to +70 °C; $V_{CC} = 5$ V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input high voltage	V_{IH}	2.4		5.5	V	Referenced to GND
Input low voltage	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			5.0	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} 0 to 5.5 V, all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	I/O = High-Z, $V_{I/O}$ = 0 to 5.5 V
Output low voltage	V_{OL}	0		0.4	V	$I_{OL} = 4.2$ mA
Output high voltage	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -5$ mA

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AC Characteristics

T_A = 0 to +70 °C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD414256-10 Min	Limits μPD414256-10 Max	Limits μPD414256-12 Min	Limits μPD414256-12 Max	Limits μPD414256-15 Min	Limits μPD414256-15 Max	Unit	Tests Conditions
Operating current, average	I_{CC1}		100		90		90	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh mode, average	I_{CC3}		85		75		65	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page mode, average	I_{CC4}		85		75		65	mA	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling, $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode, average	I_{CC5}		90		80		70	mA	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IL}$, $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	200		220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	270		300		355		ns	(Note 6)
Page mode cycle time	t_{PC}	100		120		145		ns	(Note 6)
Refresh period	t_{REF}		8		8		8	ms	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	(Notes 7, 9)
Output buffer turn-off delay	t_{OFF}	0	25	0	30	0	40	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	20		25		30		ns	
$\overline{CAS}$ precharge time, page mode	t_{CP}	40		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	25		30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		90		115		ns	
Write command pulse width	t_{WP}	15		20		25		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ± 10%

Parameter	Symbol	Limits μPD414256-10 Min	Max	μPD414256-12 Min	Max	μPD414256-15 Min	Max	Unit	Test Conditions
Write command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	35		40		45		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	25		30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	75		90		115		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		195		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	80		95		120		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		25		30		40	ns	
Data delay time	t_{OED}	25		30		40		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turn-off delay from $\overline{OE}$	t_{OEZ}	0	25	0	30	0	40	ns	(Note 10)
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	20		25		30		ns	

Note:

(1) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(2) AC measurements assume t_T = 5 ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(4) All voltages referenced to GND.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

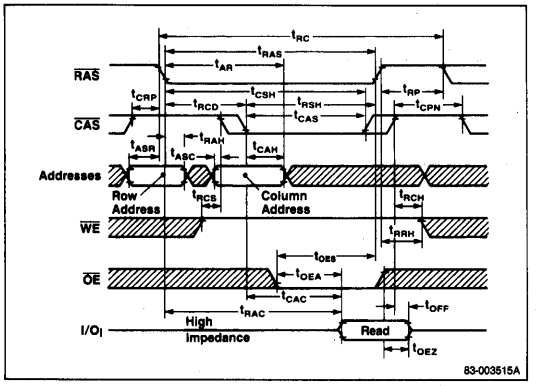
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

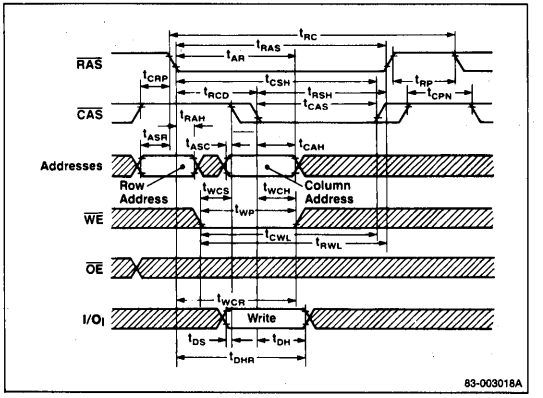
5

Timing Waveforms

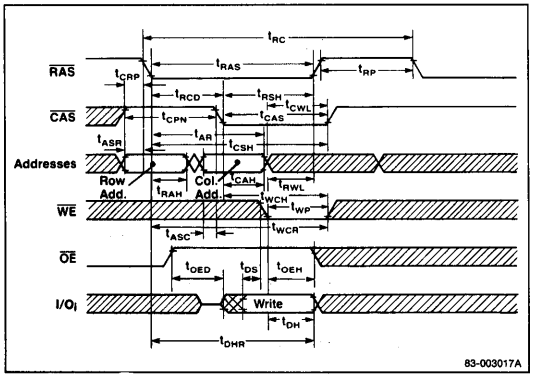
Read Cycle



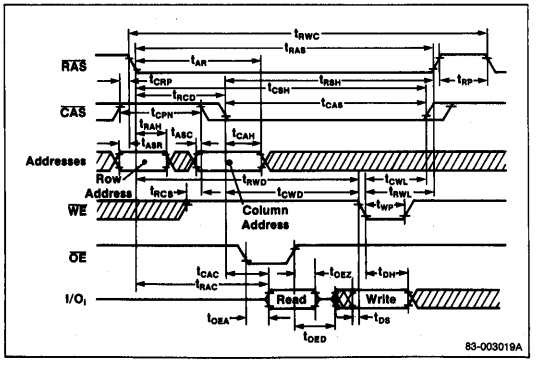
Write Cycle (Early Write)



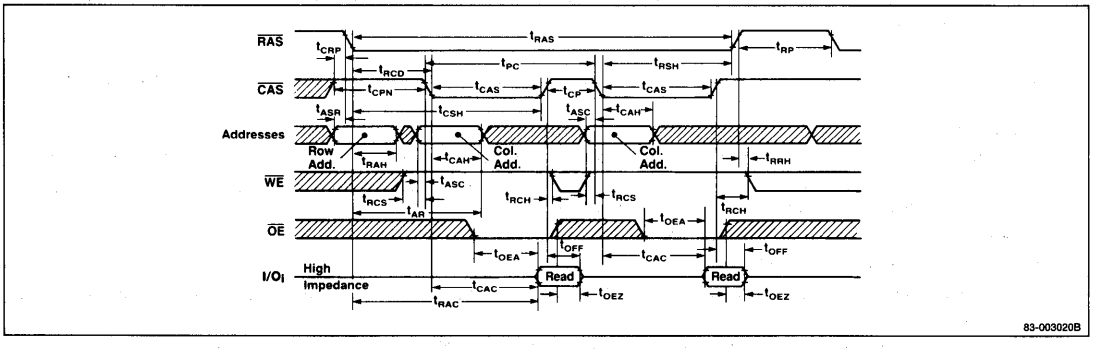
OE-Controlled Write Cycle



Read-Write/Read-Modify-Write Cycle

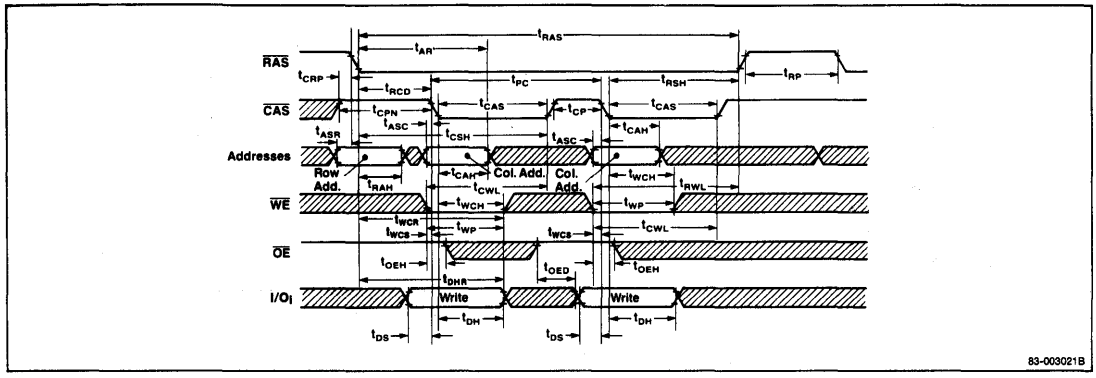


Page Mode Read Cycle

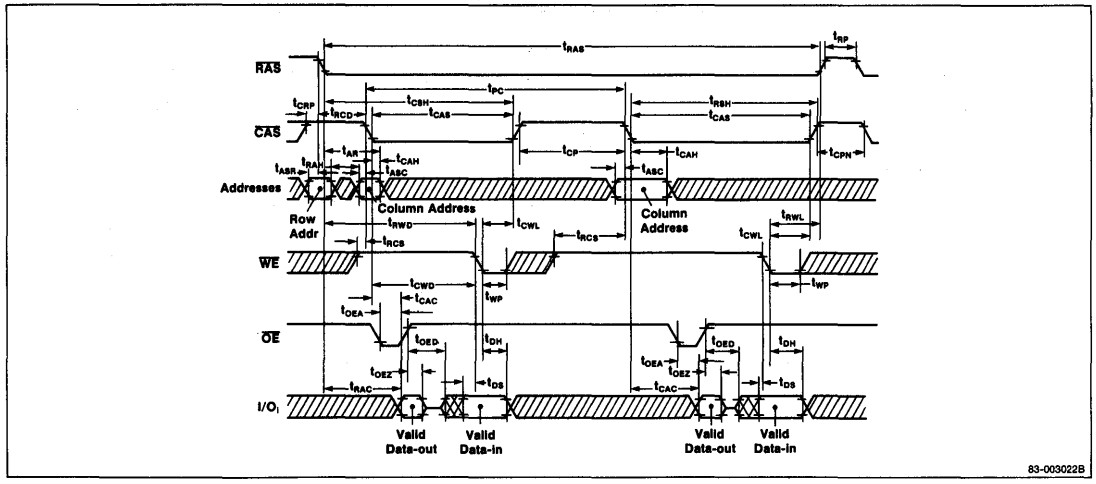


Timing Waveforms (cont)

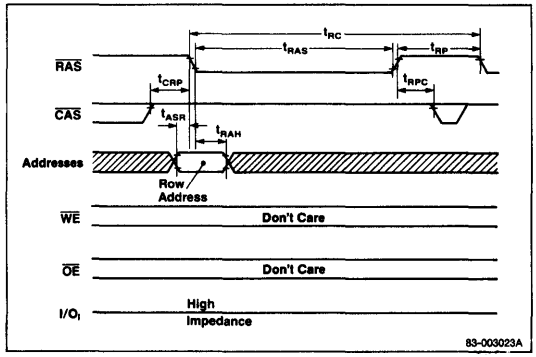
Page Mode Write Cycle (Early Write)



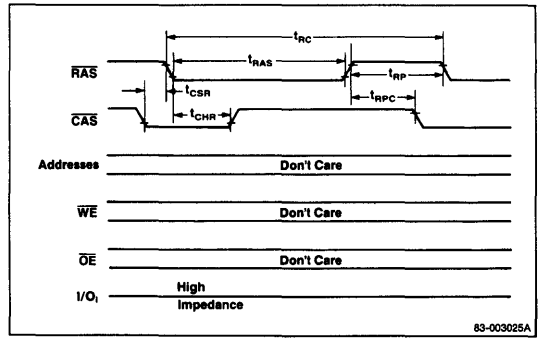
Page Mode Read-Write/Read-Modify-Write Cycle



RAS-Only Refresh Cycle

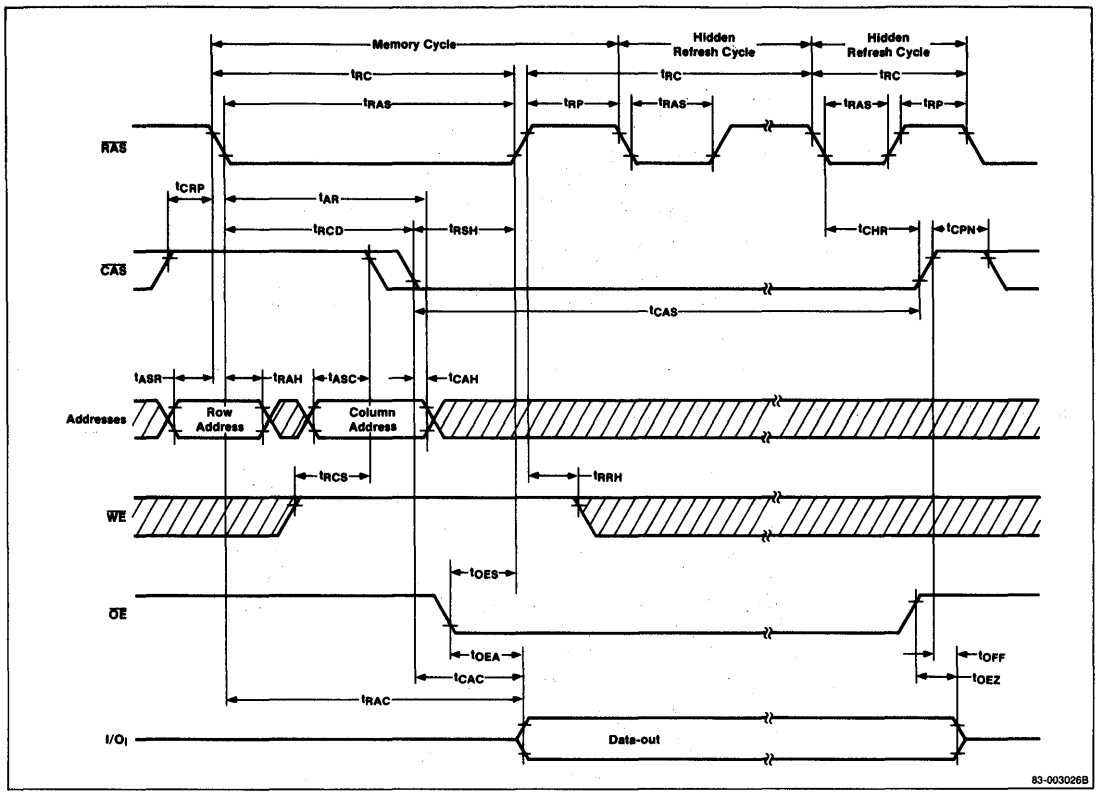


CAS before RAS Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



NEC

XRAMs 6

Section 6 — XRAMS

μPD4168
8,192 x 8-BIT NMOS XRAM

Revision 1

Description

The NEC μPD4168 is an 8,192 word by 8-bit NMOS XRAM designed to operate from a single +5 V power supply. The NEC μPD4168 is termed an XRAM because it incorporates some of the best features of both SRAMs (Non-multiplexed addresses, simple interface requirements) and DRAMs (the one-transistor core cell provides high density at low cost). The negative voltage substrate bias is internally generated and provides automatic and transparent operation.

The incorporation of an internal refresh address counter and refresh multiplexer allows the user to select one of three refresh modes. The self-refresh mode provides transparent refresh without system overhead. Internal latches for address, data, and chip select allow for use in systems incorporating multiplexed address/data buses.

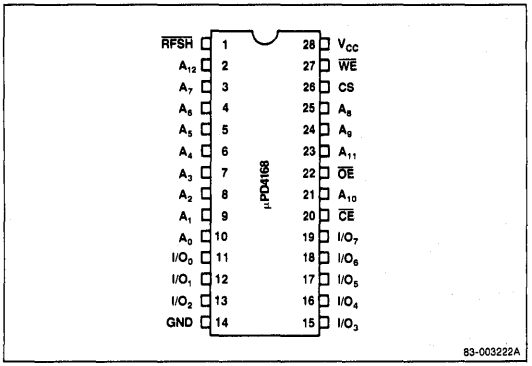
Features

- ☐ 8,192 words by 8-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ On-chip substrate bias generator
- ☐ Fast access times
- ☐ Low power dissipation:
  28 mW max-Standby
  19 mW max-Self refresh
- ☐ TTL-compatible
- ☐ 28-pin SRAM/ROM/EPROM compatible package
- ☐ Built-in refresh multiplexer and refresh address counter
- ☐ Power-down self-refresh mode
- ☐ Automatic precharge allows cycle time to be independent of system skews
- ☐ Latched address, CS, and $\overline{OE}$ functions allow use on multiplexed address/data bus
- ☐ Read, early write, late write, external refresh, pulse refresh, and self-refresh cycles

Performance Ranges

Device	t_{CEA}	t_{OEA}	t_C	I_{CC1}
μPD4168C-12	120 ns	45 ns	220 ns	65 mA
μPD4168C-15	150 ns	55 ns	260 ns	60 mA
μPD4168C-20	200 ns	70 ns	330 ns	55 mA

Pin Configuration



Pin Identification

No.	Symbol	Function
1	$\overline{RFSH}$	Internal refresh
2-10, 21, 23-25	A_0-A_{12}	Address inputs
11-13, 15-19	I/O_0-I/O_7	Data in/out
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	$\overline{OE}$	Output enable
26	CS	Chip select
27	$\overline{WE}$	Write enable
28	V_{CC}	+5 V power supply

Pin Functions

$\overline{RFSH}$ (Refresh Input)

A built-in refresh control circuit enables this input. Two refresh modes are available: pulse refresh, using the $\overline{RFSH}$ input as a clock input, and power-down self-refresh, using the $\overline{RFSH}$ input as logic level input. $\overline{RFSH}$ is high (inactive) during normal read and write cycles.

A_0-A_{12} (Address Inputs)

The μPD4168 requires 13 address inputs to select a word of data. Because these address inputs are internally read onto the chip at the falling edge of a $\overline{CE}$ clock pulse, the $\overline{CE}$ clock determines their address setup and hold times. Inputs A_0-A_6 perform external refresh.

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I/O_0-I/O_7 (Data Inputs/Outputs)

Common I/O pins require $\overline{WE}$ and $\overline{OE}$ to control data. The $\overline{CE}$ clock and $\overline{WE}$ determine the data setup and hold times (t_{DSC}, t_{DHC}, t_{DSW}, t_{DHW}) for these pins during a memory write cycle; $\overline{OE}$ determines the access time (t_{OEA}) during a read cycle.

GND (Ground)

All voltages are referenced to GND.

$\overline{CE}$ (Chip Enable)

The chip enable clock initiates read/write cycles and external refresh cycles. It allows addresses, CS, and (during an early write cycle) data inputs to be internally read onto the chip.

$\overline{OE}$ (Output Enable)

$\overline{OE}$ controls the output timing for I/O_0-I/O_7. Access time (t_{CEA}, t_{OEA}) is determined by the $\overline{CE}$ clock or by the $\overline{OE}$ input, according to $\overline{OE}$ input timing.

CS (Chip Select)

When CS is high (active) while the $\overline{CE}$ clock is enabled, the μPD4168 can perform read/write operations. If CS is latched low (inactive) while the $\overline{CE}$ clock is enabled, I/O_0-I/O_7 remain in the high-impedance state, regardless of the status of $\overline{WE}$ and $\overline{OE}$.

$\overline{WE}$ (Write Enable)

$\overline{WE}$ controls read/write operations. $\overline{WE}$ input timing determines whether a write cycle is an early write or a late write.

V_{CC} (Power Supply)

+5 V power supply.

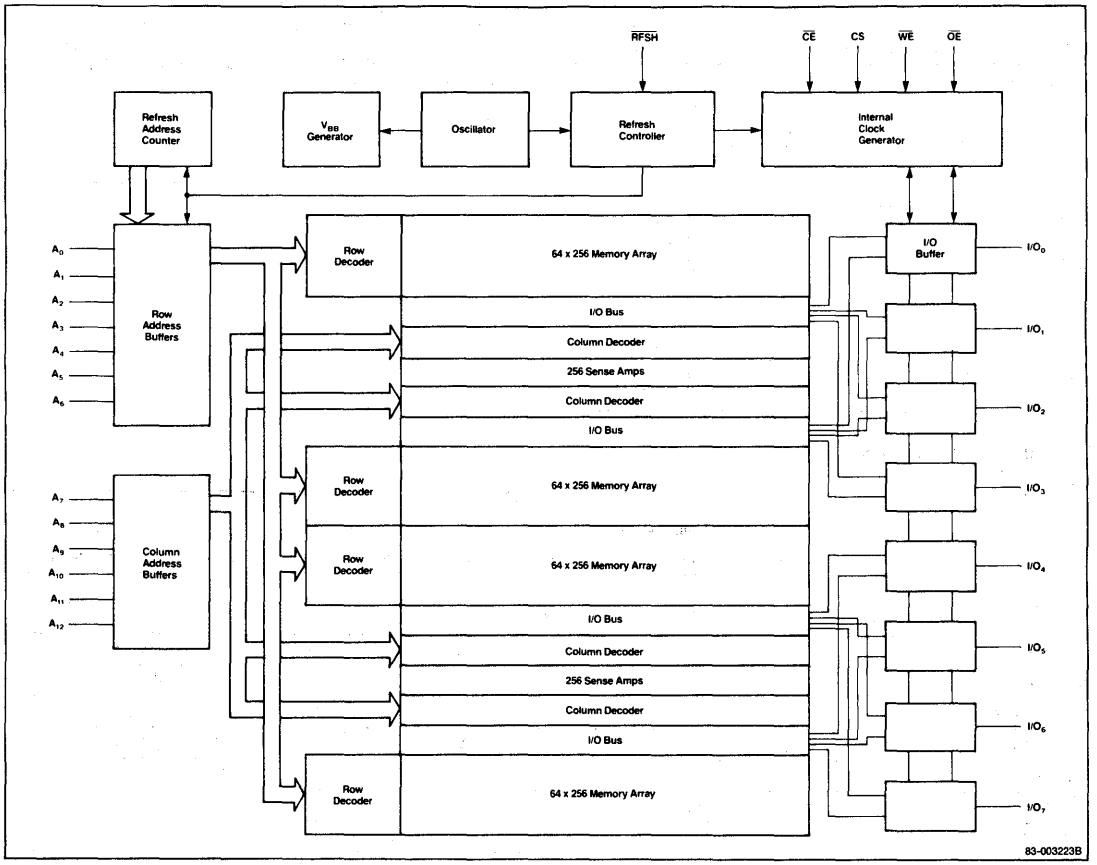
μPD4168 Functional Modes

Mode	$\overline{RFSH}$	$\overline{CE}$	CS	$\overline{WE}$	$\overline{OE}$	I/O	Comments
Read cycle	H	C′	H	H	L	Data out	$\overline{OE}$: low logic level or clock pulse
Early write	H	C′	H	L	H	Data in	
Late Write	H	C′	H	C′	H	Data in	
External refresh	H	C′	H	H	H	High-Z	
	H	C′	L	X	X	High-Z	Standby
Pulse refresh	C′	H	X	X	X	High-Z	
	C′	C′	H	H	H	High-Z	After external refresh cycle
	C′	C′	H	H	L	(Note 1)	After read cycle
	C′	C′	H	L	H	Data in	After early write cycle
	C′	C′	H	C′	H	Data in	After late write cycle
Power down self-refresh	L	H	X	X	X	High-Z	
Standby	H	H	X	X	X	High-Z	

H = V_{IH}, L = V_{IL}, C′ = negative edge of clock pulse, X = V_{IH} or V_{IL}

Note:
(1) Depends on previous cycle

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to +70°C; $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input voltage, low	V_{IL}	−1.0		0.8	V	Referenced to GND
Input voltage, high	V_{IH}	2.4		5.5	V	Referenced to GND
Output voltage, low	V_{OL}	0		0.4	V	$I_{OL} = 2$ mA

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DC Characteristics (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -1$ mA
Average V_{CC} supply current, active	I_{CC1}			65	mA	$t_C = 220$ ns
				60	mA	$t_C = 260$ ns
				55	mA	$t_C = 330$ ns
Standby current	I_{CC2}			5	mA	$\overline{CE} \geq V_{IH}$ min, $\overline{RFSH} \geq V_{IH}$ min
Self-refresh average current	I_{CC3}			3.5	mA	$\overline{RFSH} \leq V_{IL}$ max
Input leakage current	$I_{I(L)}$	−10		10	μA	$V_{IN} = 0$ to 5.5 V; others = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	$V_{OUT} = 0$ to 5.5 V; D_{OUT} = High-Z

Capacitance

$T_A = 0$ to +70°C, $V_{CC} = 5.0$ V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			10	pF	f = 1 MHz
Data I/O capacitance	$C_{I/O}$			10	pF	f = 1 MHz

AC Characteristics

$T_A = 0$ to +70°C, $V_{CC} = 5$ V ±10%

Parameter	Symbol	Limits μPD4168-12 Min	Max	μPD4168-15 Min	Max	μPD4168-20 Min	Max	Unit	Test Conditions
Average V_{CC} supply current, active	I_{CC1}		65		60		55	mA	$t_C = t_C$ (min)
Read, write, or refresh cycle time	t_C	220		260		330		ns	
Access time from $\overline{CE}$	t_{CEA}		120		150		200	ns	(Note 5)
Data off time from $\overline{CE}$	t_{CEZ}		30		35		45	ns	(Note 6)
Access time from $\overline{OE}$	t_{OEA}		45		55		70	ns	(Note 5)
Data off time from $\overline{OE}$	t_{OEZ}		30		35		45	ns	(Note 6)
$\overline{CE}$ pulse width	t_{CE}	120	10000	150	10000	200	10000	ns	
$\overline{CE}$ precharge time	t_P	90		100		120		ns	
Address setup time to $\overline{CE}$	t_{ASC}	0		0		0		ns	
Address hold time from $\overline{CE}$	t_{AHC}	35		45		55		ns	
CS setup time to $\overline{CE}$	t_{CSC}	0		0		0		ns	
CS hold time from $\overline{CE}$	t_{CHC}	35		45		55		ns	
Data setup time to $\overline{CE}$, early write	t_{DSC}	−10		−10		−10		ns	
Data hold time from $\overline{CE}$, early write	t_{DHC}	90		100		120		ns	
Data setup time to $\overline{WE}$, late write	t_{DSW}	0		0		0		ns	
Data hold time from $\overline{WE}$, late write	t_{DHW}	50		60		70		ns	
$\overline{WE}$ setup time to $\overline{CE}$, early write	t_{WSC}	−30		−30		−30		ns	(Note 7)
$\overline{WE}$ hold time from $\overline{CE}$, early write	t_{WHC}	90		100		125		ns	
$\overline{WE}$ pulse duration	t_{WD}	60		70		90		ns	
$\overline{CE}$ hold time from $\overline{WE}$, late write	t_{CHW}	90		105		135		ns	
$\overline{WE}$ setup time to $\overline{CE}$, read cycle	t_{RCS}	0		0		0		ns	
$\overline{WE}$ hold time from $\overline{CE}$, read cycle	t_{RCH}	0		0		0		ns	
$\overline{CE}$ hold time from $\overline{OE}$, read cycle	t_{CHO}	45		55		70		ns	
$\overline{OE}$ setup time to $\overline{CE}$, write cycle	t_{OES}	0		0		0		ns	
$\overline{OE}$ hold time from $\overline{CE}$, write cycle	t_{OEH}	0		0		0		ns	

AC Characteristics (cont)

$T_A = 0$ to $+70°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits μPD4168-12 Min	Limits μPD4168-12 Max	Limits μPD4168-15 Min	Limits μPD4168-15 Max	Limits μPD4168-20 Min	Limits μPD4168-20 Max	Unit	Test Conditions
$\overline{CE}$ delay to $\overline{RFSH}$, pulse refresh	t_{CRD}	50		65		80		ns	
$\overline{RFSH}$ pulse width, pulse refresh	t_{RDP}	50	4000	65	4000	80	4000	ns	
$\overline{RFSH}$ recovery time, pulse refresh	t_{RPR}	90		100		120		ns	
$\overline{RFSH}$ pulse width, self refresh	t_{RDS}	40		40		40		μs	(Note 8)
$\overline{RFSH}$ recovery time, self refresh	t_{RSR}	2		2		2		μs	
$\overline{CE}$ hold time from $\overline{RFSH}$, self refresh	t_{CSH}	40		40		40		μs	
$\overline{CE}$ setup time to $\overline{RFSH}$, self refresh	t_{CSS}	35		40		50		ns	
Transition time, rise and fall	t_T	3	50	3	50	3	50	ns	(Note 4)
Refresh period	t_{REF}		2		2		2	ms	
$\overline{RFSH}$ precharge time	t_{RP}	90		100		120		ns	
$\overline{OE}$ lead time to refresh cycle	t_{OEL}	170		210		260		ns	
$\overline{WE}$ lead time to refresh cycle	t_{WEL}	170		210		260		ns	
$\overline{RFSH}$ setup time to $\overline{CE}$	t_{RC}	280		320		410		ns	

Note:

(1) All voltages referenced to GND (0 V).

(2) An initial pause of 2 ms is required after power up, followed by any 8 $\overline{CE}$ cycles and 64 $\overline{RFSH}$ cycles before proper device operation is achieved. Read, write, and external refresh cycles may be used as $\overline{CE}$ dummy cycles for initialization. The 64 refresh dummy cycles can be performed before or after the 8 $\overline{CE}$ dummy cycles. Both dummy cycles must be within AC parameters. See figure 1, below.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring input signal timing. Transition times are measured between V_{IH} and V_{IL}.

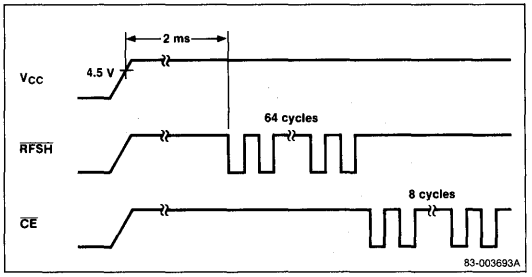
(5) Load = 2 TTL loads and 50 pF.

(6) t_{CEZ} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

(7) $t_{WSC} \leq t_{WSC}$ (min), the cycle is a late write cycle.

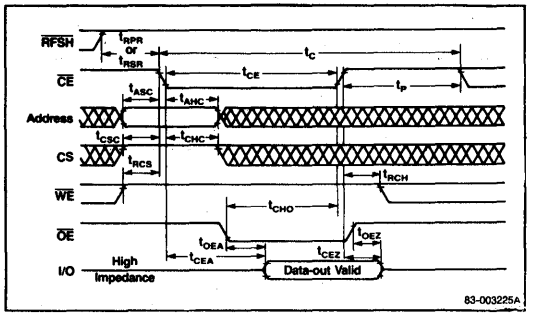
(8) A power down self-refresh cycle is initiated when the $\overline{RFSH}$ input is active low for a period of 40 μs. The refresh interval is about 15.6 μs.

Figure 1. Power-up Dummy Cycles

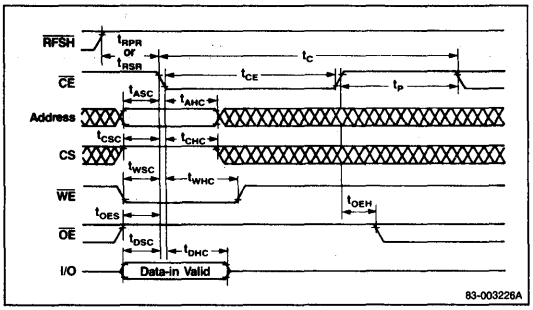


Timing Waveforms

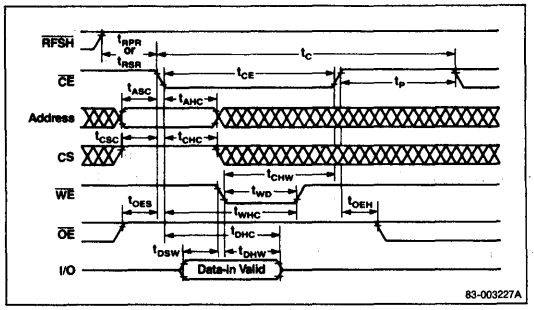
Read Cycle



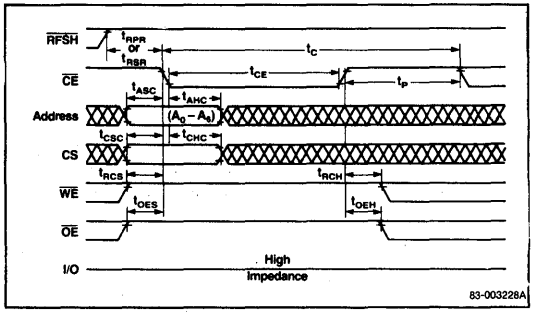
Early Write Cycle



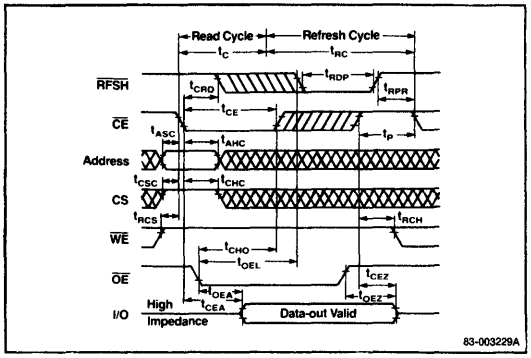
Late Write Cycle



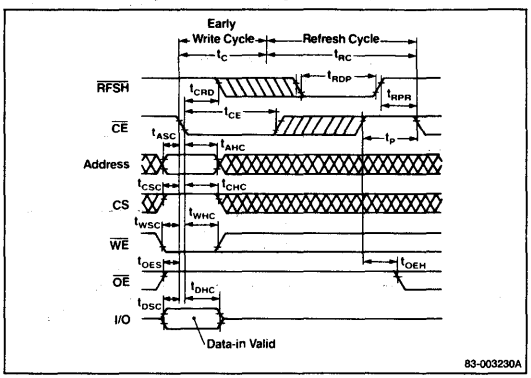
External Refresh Cycle



Pulse Refresh Cycle after Read Cycle Complete

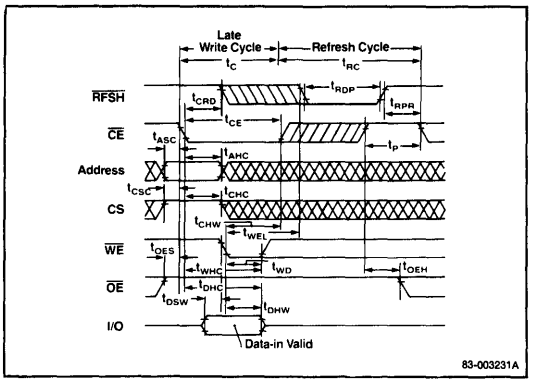


Pulse Refresh Cycle after Early Write Cycle Complete

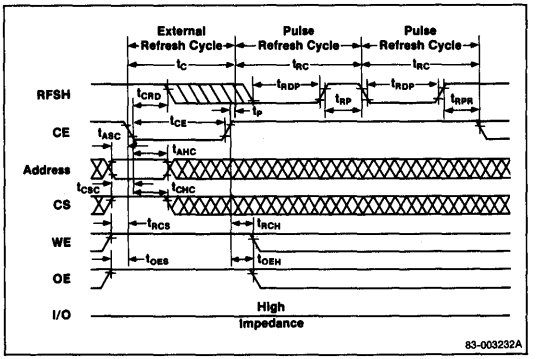


Timing Waveforms (cont)

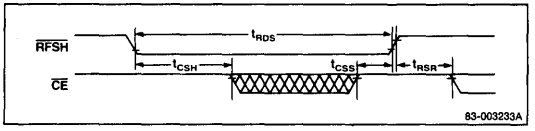
Pulse Refresh Cycle after Late Write Cycle Complete



Pulse Refresh Cycle after External Refresh Cycle Complete



Power-down Self Refresh



6

μPD42832
32,768 x 8-BIT CMOS XRAM

PRELIMINARY INFORMATION

Description

The NEC μPD42832 is a 32,768-word by 8-bit CMOS XRAM, designed to operate from a single +5V power supply. The NEC μPD42832 is termed an XRAM because it incorporates some of the best features of both SRAMs (non-multiplexed addresses, simple interface requirements) and DRAMs (the one-transistor core cell provides high density at low cost). Advanced circuitry, including sense amplifiers, provides wide operating margins and low power dissipation while maintaining high performance.

The incorporation of an internal refresh address counter and refresh multiplexer allows selection of one of three refresh modes. The self-refresh mode provides transparent refresh without system overhead.

The pulse refresh mode utilizes the internal refresh address counter; external refresh cycles use the 256 address combinations of A_0-A_7.

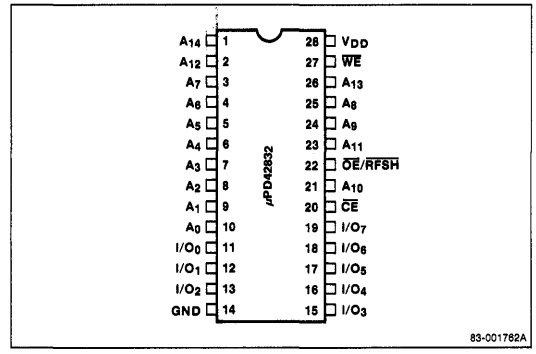
Features

- ☐ 32,768-word by 8-bit organization
- ☐ Single +5 V ±10% power supply
- ☐ TTL/CMOS-compatible
- ☐ Low power dissipation:
  1.0 mA (standby, $\overline{CE} = \overline{OE}/\overline{RFSH} = V_{IH}$)
  0.5 mA (standby, $\overline{CE} = \overline{OE}/\overline{RFSH} = V_{DD}$)
  100 μA (self-refresh, μPD42832-L)
- ☐ Available cycle types:
  Memory cycles: read, write, read/modify/write
  Refresh cycles: external refresh, pulse refresh, self-refresh
- ☐ 28-pin ROM-compatible plastic DIP (μPD42832C)
- ☐ 28-pin plastic miniflat package (μPD42832G)

Performance Ranges

Device	Access Time	Cycle Time	Power Supply	
			Active	Standby
μPD42832-10	100 ns	160 ns	60 mA	0.5 mA
μPD42832-12	120 ns	190 ns	50 mA	0.5 mA
μPD42832-15	150 ns	235 ns	40 mA	0.5 mA

Pin Configuration



Pin Identification

No.	Symbol	Function
1-10, 21, 23-26	A_0-A_{14}	Address inputs
11-13, 15-19	I/O_0-I/O_7	Data inputs/outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	$\overline{OE}/\overline{RFSH}$	Output enable/Refresh
27	$\overline{WE}$	Write enable
28	V_{DD}	+5 V power supply

Absolute Maximum Ratings

Voltage on any pin (except V_{DD})	−1.0 V to +7.0 V
Supply voltage, V_{DD}	−1.0 V to +7.0 V
Short circuit output current, I_O	50 mA
Power dissipation, P_D	1 W
Operating temperature, T_{OPR}	0°C to +70°C
Storage temperature, T_{STG}	−55°C to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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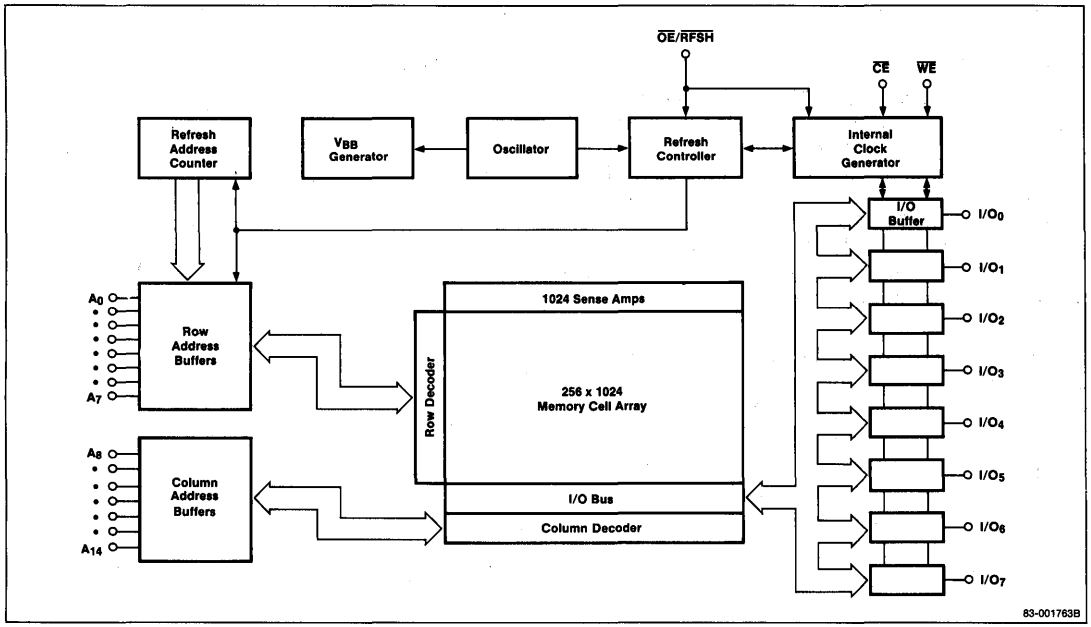
Block Diagram



DC Characteristics

$T_A = 0$ to $+70°C$; $V_{DD} = 5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{DD}	4.5	5.0	5.5	V	
Input high voltage	V_{IH}	2.4		5.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	
Standby current	I_{DD2}			1.0	mA	$\overline{CE} = \overline{OE}/\overline{RFSH} = V_{IH}$
Standby current	I_{DD2}			0.5	mA	$\overline{CE} = \overline{OE}/\overline{RFSH} = V_{DD}$
Self refresh	I_{DD3}			(1)	mA	$\overline{OE}/\overline{RFSH} = 0$ V, $\overline{CE} = V_{DD}$
Input leakage current	$I_{I(L)}$	−10		10	μA	$V_{IN} = 0$ to 5.5 V, all other pins not under test = 0 V
I/O leakage current	$I_{O(L)}$	−10		10	μA	I/O = High-Z, $V_{OUT} = 0$ to 5.5 V
Output high voltage	V_{OH}	2.4		V_{DD}	V	$I_{OH} = -1.0$ mA
Output low voltage	V_{OL}	0		0.4	V	$I_{OL} = 4.0$ mA

Note:

(1) μPD42832C-10/12/15, μPD42832G-10/12/15: $I_{DD3} = 1.5$ mA;
μPD42832C-10L/12L/15L, μPD42832G-10L/12L/15L:
$I_{DD3} = 0.1$ mA;

Capacitance

$T_A = 25°C$, $f = 1$ MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit
I/O capacitance	$C_{I/O}$			10	pF
Input capacitance	C_I			7	pF

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}/\overline{RFSH}$	I/O PIN
Standby	High	X	High	High-Z
Refresh	High	X	Low	High-Z
Read	Low	High	Low	D_{OUT}
External refresh	Low	High	High	High-Z
Write	Low	Low	High	D_{IN}

AC Characteristics

$T_A = 0°C$ to $+70°C$; $V_{DD} = 5.0\ V \pm 10\%$

Parameter	Symbol	μPD42832-10 Min	μPD42832-10 Max	μPD42832-12 Min	μPD42832-12 Max	μPD42832-15 Min	μPD42832-15 Max	Unit
Operating current(1)	I_{DD1}		60		50		40	mA
Refresh current(2)	I_{DD4}		60		50		40	mA
Pulse refresh current(3)	I_{DD5}		60		50		40	mA
Random read or write cycle time	t_{RC}	160		190		235		ns
$\overline{CE}$ access time	t_{CEA}		100		120		150	ns
Chip disable to output in high-Z	t_{CHZ}	0	30	0	35	0	40	ns
$\overline{OE}$ access time	t_{OEA}		30		35		40	ns
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	0	40	ns
$\overline{CE}$ to output in low-Z	t_{CLZ}	10		10		10		ns
$\overline{OE}$ to output in low-Z	t_{OLZ}	5		5		5		ns
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns
$\overline{CE}$ precharge time	t_P	50		60		75		ns
$\overline{CE}$ pulse width	t_{CE}	100	10000	120	10000	150	10000	ns
Address setup time before $\overline{CE}$ low	t_{ASC}	0		0		0		ns
Address hold time after $\overline{CE}$ low	t_{AHC}	25		30		40		ns
$\overline{OE}$ hold time after $\overline{CE}$ low	t_{OHC}	0		0		0		ns
$\overline{OE}$ setup time before $\overline{CE}$ low	t_{OSC}	10		10		10		ns
Read command setup time before $\overline{CE}$ low	t_{RCS}	0		0		0		ns
Read command hold time after $\overline{CE}$ high	t_{RCH}	0		0		0		ns
Write command hold time after $\overline{CE}$ low	t_{WCH}	70		85		105		ns
Write command pulse width	t_{WP}	70		85		105		ns
Write command to $\overline{CE}$ lead time	t_{CWL}	70		85		105		ns
Data setup time before $\overline{WE}$ high	t_{DSW}	60		75		95		ns
Data hold time after $\overline{WE}$ high	t_{DHW}	0		0		0		ns
Data setup time before $\overline{CE}$ high	t_{DSC}	60		75		95		ns
Data hold time after $\overline{CE}$ high	t_{DHC}	0		0		0		ns
$\overline{WE}$ to output in high-Z	t_{WHZ}	0	30	0	35	0	40	ns
Output active from end of write	t_{WLZ}	10		10		10		ns
Read/Write cycle time	t_{RWC}	250		295		365		ns
$\overline{CE}$ to $\overline{RFSH}$ delay time	t_{RFD}	50		60		75		ns
$\overline{RFSH}$ pulse width in pulse refresh	t_{FAP}	80	1000	80	1000	80	1000	ns
$\overline{RFSH}$ precharge time	t_{FP}	30		30		30		ns
Pulse refresh cycle time	t_{FC}	160		190		235		ns
$\overline{RFSH}$ to $\overline{CE}$ setup time after pulse refresh	t_{FCE}	190		225		275		ns
$\overline{RFSH}$ to $\overline{CE}$ delay time after pulse refresh	t_{FSR}	80		95		115		ns
$\overline{RFSH}$ pulse width in self refresh	t_{FAS}	8000		8000		8000		ns
$\overline{RFSH}$ to $\overline{CE}$ delay after self refresh	t_{FRS}	190		225		275		ns
Refresh period	t_{REF}		4		4		4	ms

Note: (1) $t_{RC} = t_{RC}$ (min); $I_O = 0$ mA (2) $t_{RC} = t_{RC}$ (min); $\overline{OE}/\overline{RFSH} = \overline{WE} = V_{IH}$ (3) $t_{FC} = t_{FC}$ (min); $\overline{CE} = V_{IH}$

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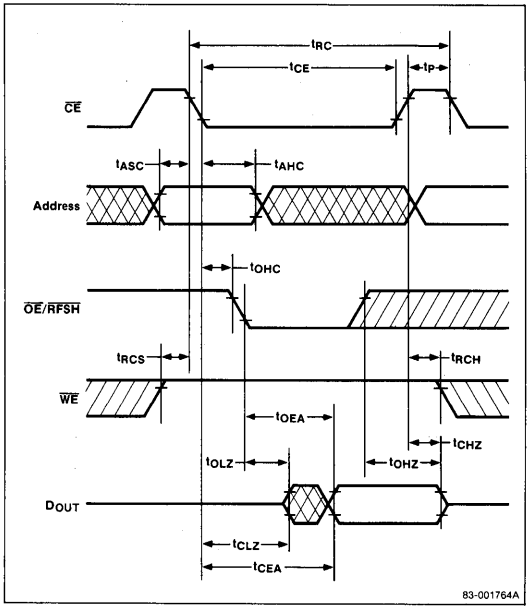
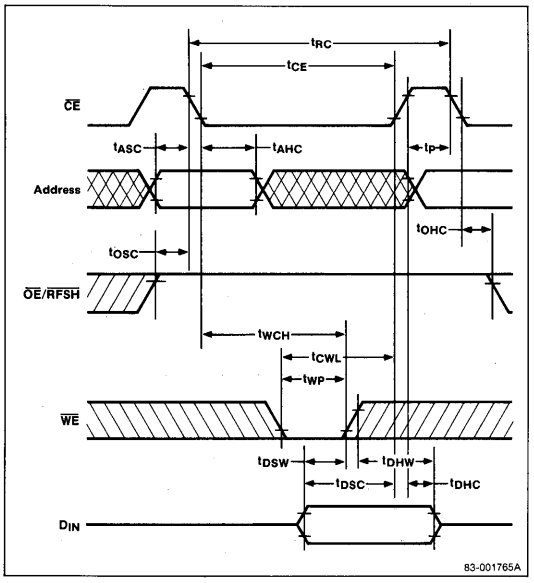
Timing Waveforms

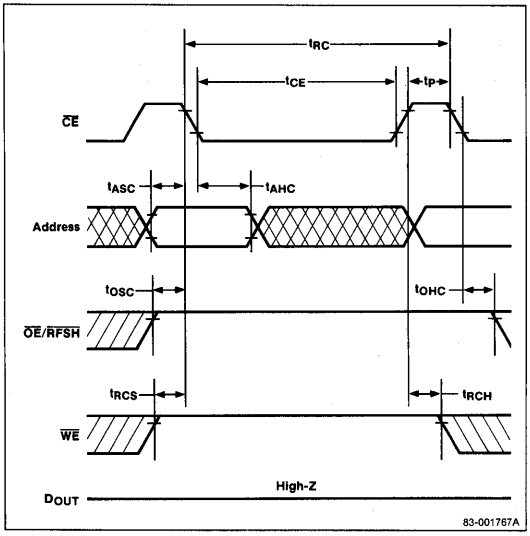
Read Cycle



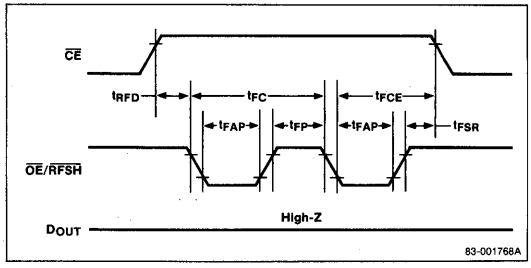
Write Cycle



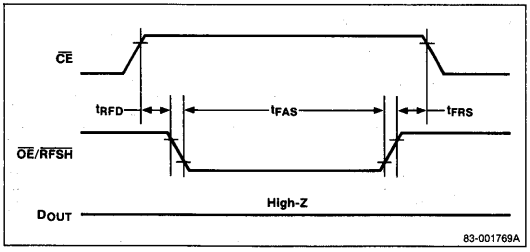
External Refresh Cycle



Pulse Refresh Cycle

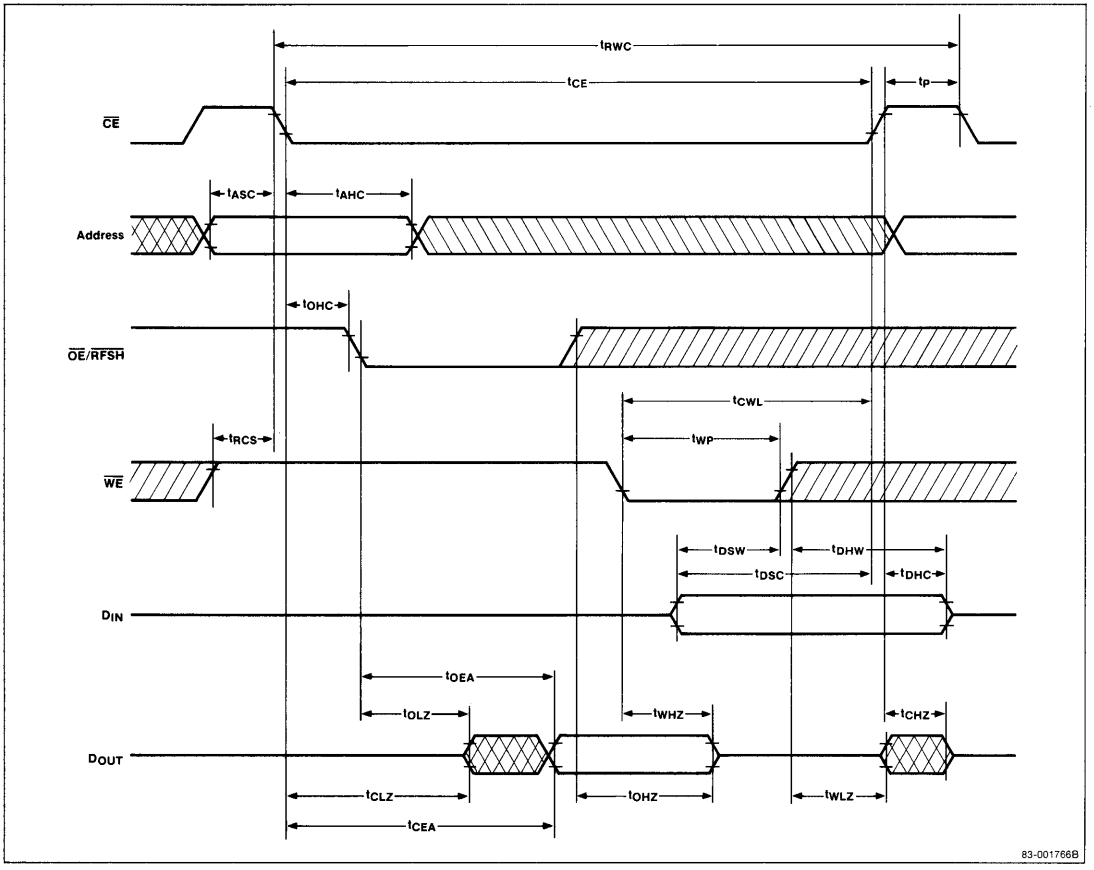


Self Refresh Cycle



Timing Waveform (cont)

Read/Modify/Write Cycle



6

NEC

MOS STATIC RAMs

7

Section 7 — MOS Static RAM

μPD446
2,048 x 8-BIT STATIC CMOS RAM

Revision 3

Description

The μPD446 is a high-speed, low-power, 2048-word by 8-bit static CMOS RAM fabricated with advanced silicon-gate CMOS technology. A unique circuitry technique makes the μPD446 a very low operating power device which requires no clock or refreshing to operate. Minimum standby power current is drawn by this device when $\overline{CS}$ equals V_{CC} independently of the other input levels. Data retention is guaranteed at a power supply voltage as low as 2 V.

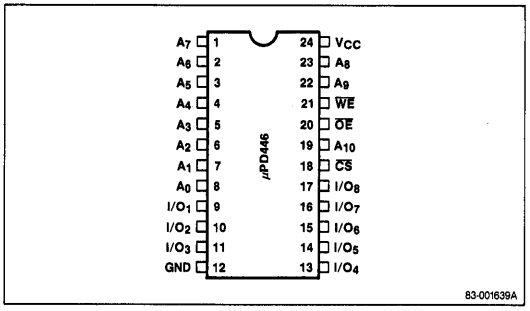
The μPD446 has a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

The μPD446 is also packaged in a miniflat package providing high density application.

Features

- ☐ Single +5 V supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL compatible — all inputs and outputs
- ☐ Common I/O using three-state output
- ☐ $\overline{OE}$ eliminates need for external bus buffers
- ☐ Max access/min cycle times down to 150 ns
- ☐ Low power dissipation
  - — Active: 38 mA max
  - — Standby: 10 μA max
- ☐ Data retention voltage: 2 V min
- ☐ Operating temperature range: −40°C to +85°C
- ☐ Standard 24-pin plastic package (μPD446C)
- ☐ Plug-in compatible with 16K EPROMs (μPD446C)
- ☐ Miniflat package for high density application (μPD446G)
- ☐ L version
  - — Standby current 1.0 μA max at 60°C for battery backup operation

Pin Configuration



Pin Identification

No.	Symbol	Function
1–8, 19, 22, 23	A_0–A_{10}	Address input
9–11, 13–17	I/O_1–I/O_8	Data input/output
18	$\overline{CS}$	Chip select
20	$\overline{OE}$	Output enable
21	$\overline{WE}$	Write enable
24	V_{CC}	Power (+5 V)
12	GND	GND

Performance Ranges

Device	Access Time (Max)	Cycle Time (Min)	Power Supply (Max) Active	Power Supply (Max) Standby
μPD446C-3, 446G-15	150 ns	150 ns	38 mA	(Note 1)
μPD446C-2, 446G-20	200 ns	200 ns	30 mA	(Note 1)
μPD446C-1, 446G-25	250 ns	250 ns	26 mA	(Note 1)
μPD446C, 446G-45	450 ns	450 ns	18 mA	(Note 1)

Note:

(1) μPD446C-L/-1L/-2L/-3L, μPD446G-45L/25L/20L/15L
T_A = 25°C, 0.2 μA
T_A = 60°C, 1.0 μA
T_A = 85°C, 10 μA

μPD446C/-1/-2/-3, μPD446G-45/25/20/15
T_A = 25°C, 1.0 μA
T_A = 60°C, 5.0 μA
T_A = 85°C, 10 μA

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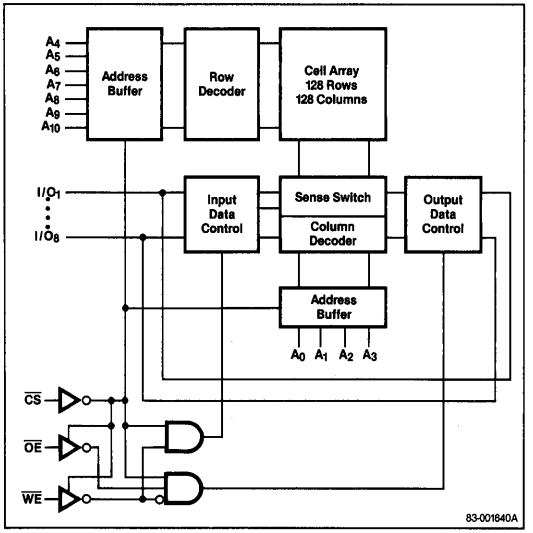
Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	7.0 V
Input voltage, V_{IN}	−0.3 to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.3 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−40 to 85°C
Storage temperature, T_{STG}	−55 to 125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_{IN}			6	pF	V_{IN} = 0 V
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O}$ = 0 V

Recommended DC Operating Conditions

T_A = −40 to +85°C

		Limits			
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage low	V_{IL}	−0.3		0.8	V
Input voltage high	V_{IH}	2.2		V_{CC} + 0.3	V

DC Characteristics

T_A = −40 to 85°C, V_{CC} = 5 V ± 10%

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input leakage current	I_{LI}			1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}			1	μA	$V_{I/O}$ = 0 V to V_{CC}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Operating supply current	I_{CCA1}		(1)	(1)	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 V min cycle
Operating supply current	I_{CCA2}		5	10	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 V DC current
Standby supply current	I_{CCS}		0.02	(2)	μA	$\overline{CS}$ = V_{CC} − 0.2 V, V_{IN} = 0 V to V_{CC}
Output voltage low	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output voltage high	V_{OH}	2.4			V	I_{OH} = −1.0 mA

Notes:

(1) μPD446C-3/3L, μPD446G-15/15L: 25 mA typ, 38 mA max
μPD446C-2/2L, μPD446G-20/20L: 20 mA typ, 30 mA max
μPD446C-1/1L, μPD446G-25/25L: 18 mA typ, 26 mA max
μPD446C/-L, μPD446G-45/45L: 12 mA typ, 18 mA max

(2) μPD446C-L/-1L/-2L/-3L, μPD446G-45L/25L/20L/15L
T_A = 25°C, 0.2 μA
T_A = 60°C, 1.0 μA
T_A = 85°C, 10 μA
μPD446C/-1/-2/-3, μPD446G-45/25/20/15
T_A = 25°C, 1.0 μA
T_A = 60°C, 5.0 μA
T_A = 85°C, 10 μA

AC Characteristics

$T_A = -40$ to 85°C, $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	μPD446C-3 μPD446G-15 Min	μPD446C-3 μPD446G-15 Max	μPD446C-2 μPD446G-20 Min	μPD446C-2 μPD446G-20 Max	μPD446C-1 μPD446G-25 Min	μPD446C-1 μPD446G-25 Max	μPD446C μPD446G-45 Min	μPD446C μPD446G-45 Max	Unit
Read Cycle										
Read cycle time	t_{RC}	150		200		250		450		ns
Address access time	t_{AA}		150		200		250		450	ns
Chip select access time	t_{ACS}		150		200		250		450	ns
Output enable to output valid	t_{OE}		75		100		120		150	ns
Output hold from address change	t_{OH}	15		15		15		15		ns
Chip select to output in Lo-Z	t_{CLZ}	10		10		10		10		ns
Output enable to output in Lo-Z	t_{OLZ}	5		5		5		5		ns
Chip deselect to output in Hi-Z	t_{CHZ}		50		60		80		100	ns
Output disable to output in Hi-Z	t_{OHZ}		50		60		80		100	ns
Write Cycle										
Write cycle time	t_{WC}	150		200		250		450		ns
Chip select to end of write	t_{CW}	120		150		180		210		ns
Address valid to end of write	t_{AW}	120		150		180		210		ns
Address setup time	t_{AS}	0		0		0		0		ns
Write pulse width	t_{WP}	90		120		150		180		ns
Write recovery time	t_{WR}	0		0		0		0		ns
Data valid to end of write	t_{DW}	50		60		80		100		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write enable to output in Hi-Z	t_{WHZ}		50		60		80		100	ns
Output active from end of write	t_{OW}	10		10		10		10		ns

AC Test Conditions

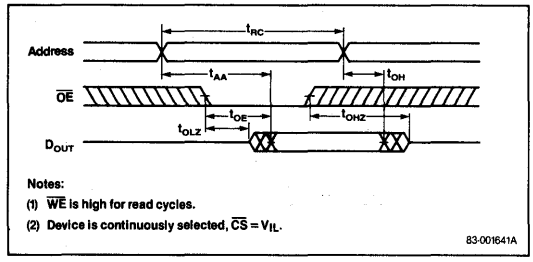
Input pulse levels	0.8 to 2.2 V
Input pulse rise and fall time	10 ns
Timing reference levels	1.5 V
Output load	1 TTL + 100 pF

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	I_{CC}
H	X	X	Not selected	Hi-Z	Standby
L	H	H	Not selected	Hi-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Timing Waveforms

Read Cycle No. 1



Notes:

(1) $\overline{WE}$ is high for read cycles.

(2) Device is continuously selected, $\overline{CS} = V_{IL}$.

83-001641A

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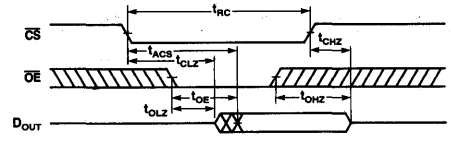
Timing Waveforms (cont)

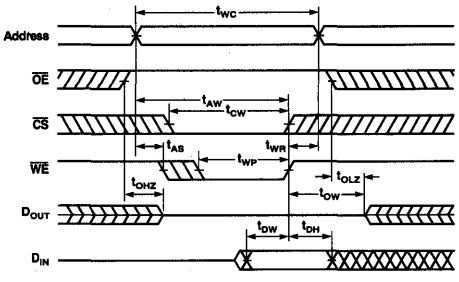
Read Cycle No. 2



Notes:
(1) $\overline{WE}$ is high for read cycles.
(2) Address valid prior to or coincident with $\overline{CS}$ transition low.

83-001642A

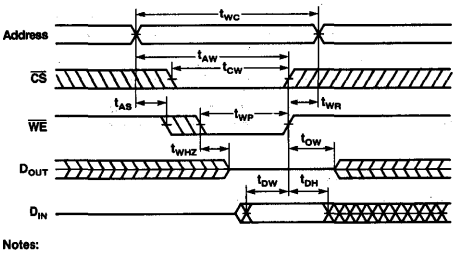
Write Cycle No. 1



Notes:
(1) $\overline{WE}$ must be high during all address transitions.
(2) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
(3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(4) If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, output buffers remain in a high impedance state.

83-001643A

Write Cycle No. 2



Notes:
(1) $\overline{WE}$ must be high during all address transitions.
(2) A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
(3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(4) If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, output buffers remain in a high impedance state.
(5) $\overline{OE}$ is continuously low.

83-001644A

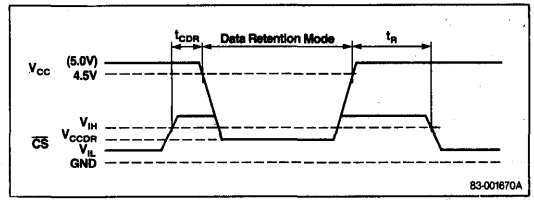
Low V_{CC} Data Retention Characteristics

$T_A = -40$ to 85°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0			V	V_{IN} = 0 V to V_{CC}, $\overline{CS}$ = V_{CC}
Data retention supply current	I_{CCDR}		0.01	(1)	μA	V_{IN} = 0 V to V_{CC}, $\overline{CS}$ = V_{CC}, V_{CC} = 3.0 V
Chip deselection to data retention mode	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Note:
(1) μPD446C-L/-1L/-2L/-3L, μPD446G-45L/25L/20L/15L
T_A = 25°C, 0.2 μA
T_A = 60°C, 1.0 μA
T_A = 85°C, 10 μA
μPD446C/-1/-2/-3, μPD446G-45/25/20/15
T_A = 25°C, 1.0 μA
T_A = 60°C, 5.0 μA
T_A = 85°C, 10 μA

Low V_{CC} Data Retention



83-001670A

μPD449
2,048 x 8-BIT STATIC CMOS RAM

Revision 4

Description

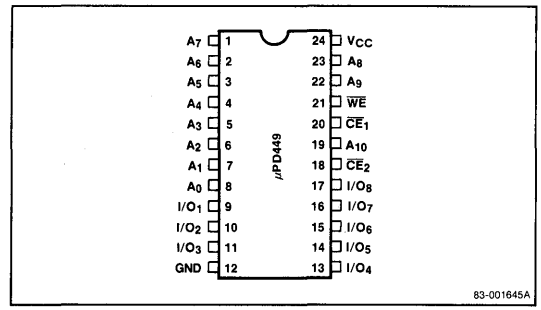
The μPD449 is a high-speed, low-power, 2048-word by 8-bit static CMOS RAM fabricated with advanced silicon-gate CMOS technology. A unique circuitry technique makes the μPD449 a very low operating power device which requires no clock or refreshing to operate. Since the device has two chip enable inputs, it is suited for battery backup applications. Minimum standby power current is drawn by this device when $\overline{CE}_1$ or $\overline{CE}_2$ equals V_{CC} independently of the other input levels. Data retention is guaranteed at a power supply voltage as low as 2 V.

The μPD449 has a standard 24-pin dual-in-line package and is plug-in compatible with 16K EPROMs.

Features

- ☐ Single +5 V supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL compatible — all inputs and outputs
- ☐ Common I/O using three-state output
- ☐ Two chip enable inputs for battery backup application
- ☐ Max access/min cycle times down to 150 ns
- ☐ Low power dissipation,
  - — Active: 38 mA max
  - — Standby: 10 μA max
- ☐ Data retention voltage: 2 V min
- ☐ Operating temperature range: −40 to +85°C
- ☐ Standard 24-pin plastic package
- ☐ Plug-in compatible with 16K EPROMs
- ☐ L version
  - — Standby current 1.0 μA max at 60°C for battery backup operation

Pin Configuration



Pin Identification

No.	Symbol	Function
1–8, 19, 22, 23	A_0–A_{10}	Address input
9–11, 13–17	I/O_1–I/O_8	Data input/output
20, 18	$\overline{CE}_1$, $\overline{CE}_2$	Chip enable input
21	$\overline{WE}$	Write enable input
24	V_{CC}	Power (+5 V)
12	GND	GND

Performance Ranges

Device	Access Time (Max)	Cycle Time (Min)	Power Supply (Max) Active	Standby
μPD449C-3	150 ns	150 ns	38 mA	(Note 1)
μPD449C-2	200 ns	200 ns	30 mA	(Note 1)
μPD449C-1	250 ns	250 ns	26 mA	(Note 1)
μPD449C	450 ns	450 ns	18 mA	(Note 1)

Note:
(1) μPD449C-L/-1L/-2L/-3L
T_A = 25°C, 0.2 μA
T_A = 60°C, 1.0 μA
T_A = 85°C, 10 μA
μPD449C/-1/-2/-3
T_A = 25°C, 1.0 μA
T_A = 60°C, 5.0 μA
T_A = 85°C, 10 μA

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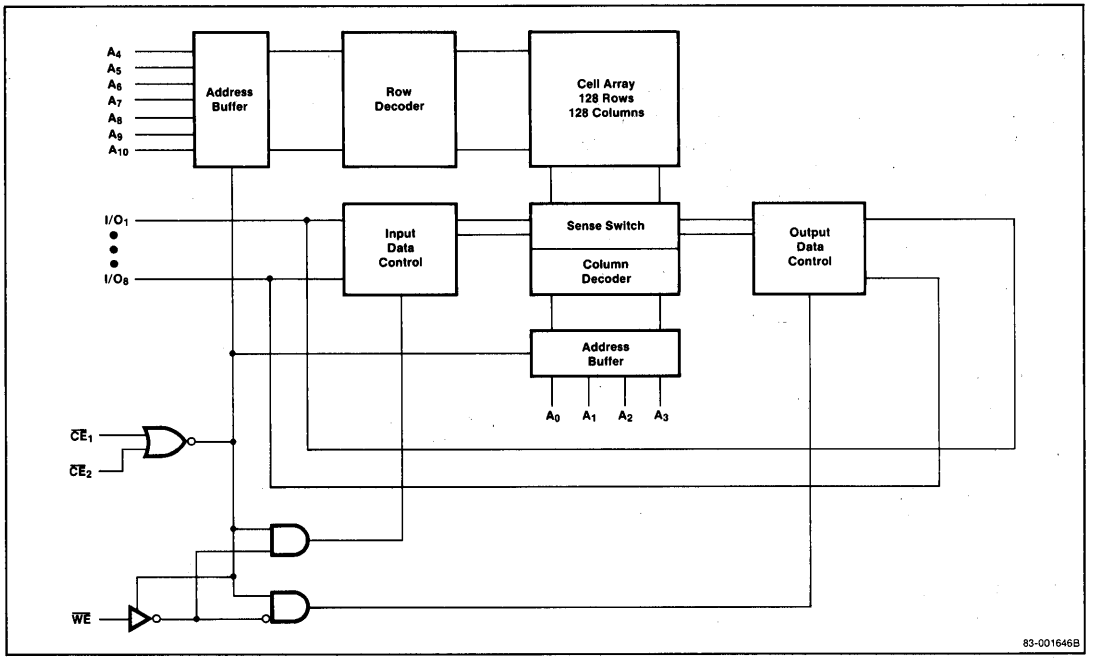
Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	7.0 V
Input voltage, V_{IN}	−0.3 to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.3 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−40 to +85°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	V_{IN} = 0 V
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O}$ = 0 V

Recommended DC Operating Conditions

T_A = −40 to +85°C

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage low	V_{IL}	−0.3		0.8	V
Input voltage high	V_{IH}	2.2		V_{CC} + 0.3	V

Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	MODE	I/O	I_{CC}
X	H	X	Not selected	Hi-Z	Standby
H	X	X	Not selected	Hi-Z	Standby
L	L	H	Read	D_{OUT}	Active
L	L	L	Write	D_{IN}	Active

AC Test Conditions

Input pulse levels	0.8 to 2.2 V
Input pulse rise and fall time	10 ns
Timing reference levels	1.5 V
Output load	1 TTL +100 pF

DC Characteristics

$T_A = -40$ to $+85°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}			1	μA	$V_{IN} = 0\,V$ to V_{CC}
I/O leakage current	I_{LO}			1	μA	$V_{I/O} = 0\,V$ to V_{CC}, $\overline{CE_1}$ or $\overline{CE_2} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}		(1)	(1)	mA	$\overline{CE_1}$ and $\overline{CE_2} = V_{IL}$, $I_{I/O} = 0$, min cycle
Operating supply current	I_{CCA2}		5	10	mA	$\overline{CE_1}$ and $\overline{CE_2} = V_{IL}$, $I_{I/O} = 0$ DC current
Standby supply current	I_{SB}		0.02	(2)	μA	$\overline{CE_1}$ or $\overline{CE_2} \geq V_{CC} - 0.2\,V$, other $\overline{CE}$ input $\leq 0.2\,V$ or $\geq V_{CC} - 0.2\,V$, $V_{IN} = 0\,V$ to V_{CC}

DC Characteristics (cont)

$T_A = -40$ to $+85°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage low	V_{OL}			0.4	V	$I_{OL} = 2.0\,mA$
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -1.0\,mA$

Notes:

(1) μPD449C-3/3L, 25 mA typ, 38 mA max
μPD449C-2/2L, 20 mA typ, 30 mA max
μPD449C-1/1L, 18 mA typ, 26 mA max
μPD449C/-L, 12 mA typ, 18 mA max

(2) μPD449C-L/-1L/-2L/-3L
$T_A = 25°C$, 0.2 μA max
$T_A = 60°C$, 1.0 μA max
$T_A = 85°C$, 10 μA max
μPD449C/-1/-2/-3
$T_A = 25°C$, 1.0 μA max
$T_A = 60°C$, 5.0 μA max
$T_A = 85°C$, 10 μA max

AC Characteristics

$T_A = -40$ to $+85°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	μPD449-3 Min	μPD449-3 Max	μPD449-2 Min	μPD449-2 Max	μPD449-1 Min	μPD449-1 Max	μPD449 Min	μPD449 Max	Unit
Read Cycle										
Read cycle time	t_{RC}	150		200		250		450		ns
Address access time	t_A		150		200		250		450	ns
Chip enable ($\overline{CE_1}$) to output valid	t_{CO1}		150		200		250		450	ns
Chip enable ($\overline{CE_2}$) to output valid	t_{CO2}		150		200		250		450	ns
Output hold from address change	t_{OH}	15		15		15		15		ns
Chip enable ($\overline{CE_1}$) to output in Lo-Z	t_{LZ1}	5		5		5		5		ns
Chip enable ($\overline{CE_2}$) to output in Lo-Z	t_{LZ2}	5		5		5		5		ns
Chip enable ($\overline{CE_1}$) to output in Hi-Z	t_{HZ1}		50		60		80		100	ns
Chip enable ($\overline{CE_2}$) to output in Hi-Z	t_{HZ2}		50		60		80		100	ns
Write Cycle										
Write cycle time	t_{WC}	150		200		250		450		ns
Chip enable ($\overline{CE_1}$) to end of write	t_{CW1}	120		150		180		210		ns
Chip enable ($\overline{CE_2}$) to end of write	t_{CW2}	120		150		180		210		ns
Address setup time	t_{AW}	0		0		0		0		ns
Write pulse width	t_{WP}	90		120		150		180		ns
Write recovery time	t_{WR}	0		0		0		0		ns
Data valid to end of write	t_{DW}	50		60		80		100		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write enable to output in Hi-Z	t_{WZ}		50		60		80		100	ns
Output active from end of write	t_{OW}	10		10		10		10		ns

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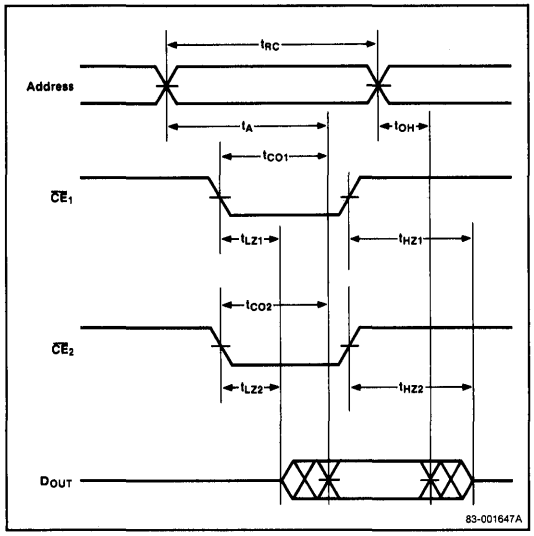
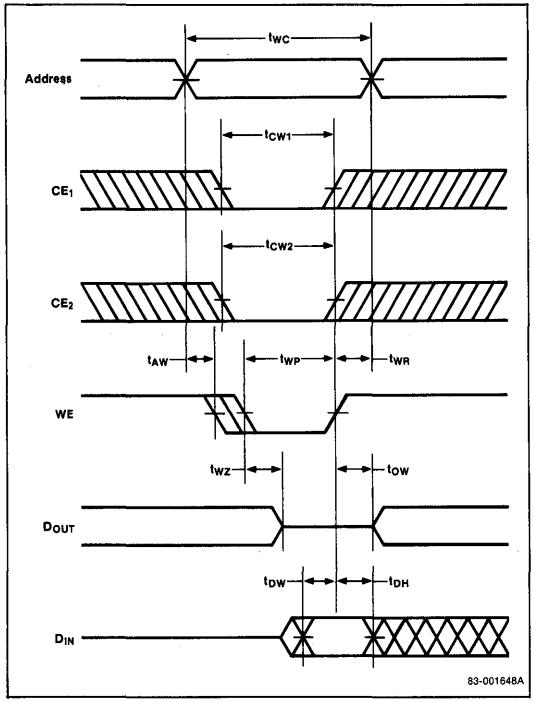
Timing Waveforms

Read Cycle (Address Access)



Write Cycle (Address Access)



Low V_{CC} Data Retention Characteristics

$T_A = -40$ to $+85°C$

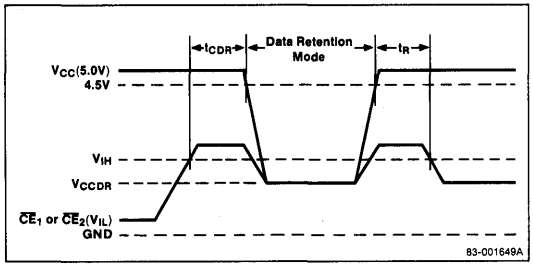
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0			V	V_{IN} = 0 V to V_{CC}, $\overline{CE}_1$ or $\overline{CE}_2 = V_{CC}$
Data retention supply current	I_{CCDR}		0.01	(1)	μA	V_{IN} = 0 V to V_{CC}, $\overline{CE}_1$ or $\overline{CE}_2 = V_{CC}$, other $\overline{CE}$ input = 0 V or V_{CC}, V_{IN} = 0 V to V_{CC}, V_{CC} = 3.0 V
Chip deselection to data retention mode	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Note:

(1) μPD449C-L/-1L/-2L/-3L
- $T_A = 25°C$, 0.2 μA max
- $T_A = 60°C$, 1.0 μA max
- $T_A = 85°C$, 10 μA max

μPD449C/-1/-2/-3
- $T_A = 25°C$, 1.0 μA max
- $T_A = 60°C$, 5.0 μA max
- $T_A = 85°C$, 10 μA max

Data Retention Timing Chart



μPD2147A
4,096 x 1-BIT
STATIC NMOS RAM

Revision 1

Description

The μPD2147A is a 4096-bit static Random Access Memory organized as 4096 words by 1 bit, using a scaled MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the μPD2147A — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are deselected.

The μPD2147A is placed in an 18-pin cerdip package configured with the industry standard 2147 pinout. It is directly TTL compatible in all respects: input, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

Features

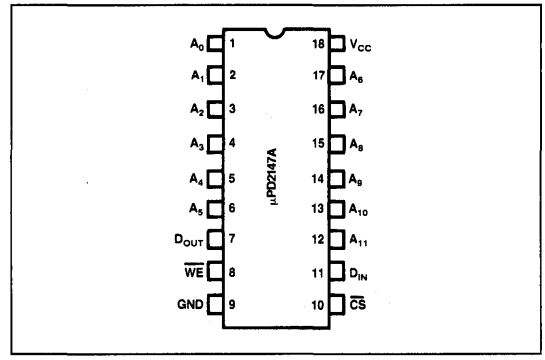
- ☐ Pinout, Function, and Power Compatible to Industry Standard 2147
- ☐ Scaled MOS Technology
- ☐ Completely Static Memory — No Clock or Timing Strobe Required
- ☐ Equal Access and Cycle Times
- ☐ Single +5V Supply
- ☐ Direct Performance Upgrade for 2147
- ☐ Automatic Power-Down
- ☐ High Density 18-Pin Package
- ☐ Directly TTL Compatible — All Input and Output
- ☐ Separate Data Input and Output
- ☐ Three-State Output
- ☐ 3 performance ranges:

Device	Max Access Time	Supply Current	
		Active	Standby
μPD2147A-25	25 ns	160 mA	20 mA
μPD2147A-35	35 ns	160 mA	20 mA
μPD2147A-45	45 ns	160 mA	20 mA

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

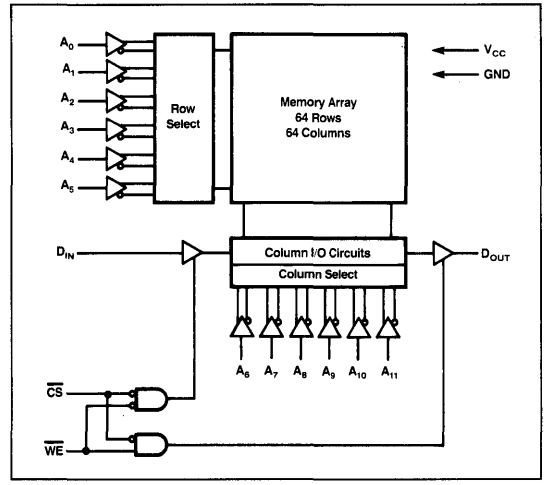
Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Function
1-6, 17-12	A_0-A_{11}	Address Inputs
7	D_{OUT}	Data Output
8	$\overline{WE}$	Write Enable
9	GND	Ground
10	$\overline{CS}$	Chip Select
11	D_{IN}	Data Input
18	V_{CC}	Power (+5V)

Block Diagram



7

Absolute Maximum Ratings*

Operating Temperature	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−3.5V to +7V ①
DC Output Current	20mA
Power Dissipation	1.2 W

Note: ① with respect to ground

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and Operating Characteristics

T_A = 0°C to +70°C; V_{CC} = +5V ± 10%①

Parameter	Symbol	Limits Min	Typ②	Max	Unit	Test Conditions
Input Load Current (All Input Pins)	I_{LI}		0.01	10	μA	V_{CC} = Max, V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}		0.01	10	μA	$\overline{CS}$ = V_{IH}, V_{CC} = Max, V_{OUT} = GND to V_{CC}
Operating Current	I_{CC}		120	150	mA	T_a = 25°C V_{CC} = Max, $\overline{CS}$ = V_{IL},
				160	mA	T_a = 0°C Output Open
Standby Current	I_{SB}		12	20	mA	V_{CC} = Min to Max, $\overline{CS}$ = V_{IH}
Peak Power-On Current	I_{PO}③		25	50	mA	V_{CC} = GND to V_{CC} = Min, $\overline{CS}$ = Lower to V_{CC} or V_{IH} Min
Input Low Voltage	V_{IL}	−3.0		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −4.0 mA
Output Short Circuit Current	I_{OS}			±130	mA	V_{OUT} = GND to V_{CC}

Notes: ① The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
② Typical limits are V_{CC} = 5V, T_a = +25°C, and specified loading.
③ A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 1

Capacitance

T_A = 25°C; f = 1.0 MHz①

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			6	pF	V_{OUT} = 0V

Note: ① This parameter is sampled and not 100% tested.

Figure 1. Loading Conditions Test Circuit

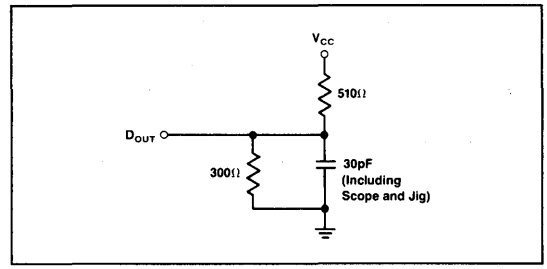
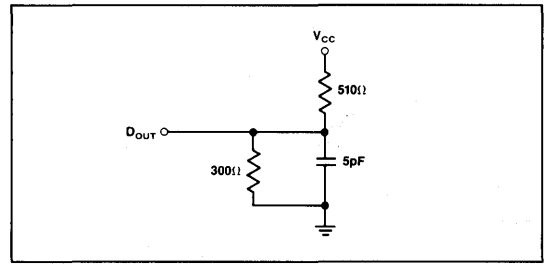


Figure 2. Input Pulse Test Circuit



AC Characteristics

Read Cycle

T_A = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

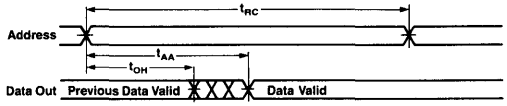
Parameter	Symbol	Limits μPD2147A-25 Min	Max	μPD2147A-35 Min	Max	μPD2147A-45 Min	Max	Unit	Test Conditions
Read Cycle Time	t_{RC}①	25		35		45		ns	
Address Access Time	t_{AA}		25		35		45	ns	
Chip Select Access Time	t_{ACS}		25		35		45	ns	
Output Hold From Address Change	t_{OH}	5		5		5		ns	
Chip Select to Output in Low Z	t_{LZ}②	5		5		5		ns	③
Chip Deselection to Output in High Z	t_{HZ}②	0	20	0	30	0	30	ns	④
Chip Selection to Power-Up Time	t_{PU}	0		0		0		ns	
Chip Selection to Power-Down Time	t_{PD}		20		20		20	ns	

Write Cycle

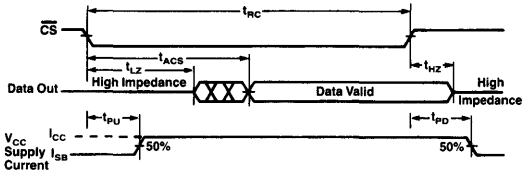
Parameter	Symbol	Limits μPD2147A-25 Min	Max	μPD2147A-35 Min	Max	μPD2147A-45 Min	Max	Unit	Test Conditions
Write Cycle Time②	t_{WC}	25		35		45		ns	
Chip Selection to End of Write	t_{CW}	25		35		45		ns	
Address Valid to End of Write	t_{AW}	25		35		45		ns	
Address Setup Time	t_{AS}	0		0		0		ns	
Write Pulse Width	t_{WP}	20		20		25		ns	
Write Recovery Time	t_{WR}	0		0		0		ns	
Data Valid to End of Write	t_{DW}	20		20		25		ns	
Data Hold Time	t_{DH}	10		10		10		ns	
Write Enabled to Output in High Z	t_{WZ}	0	15	0	20	0	25	ns	③
Output Active From End of Write	t_{OW}	0		0		0		ns	④

Timing Waveforms

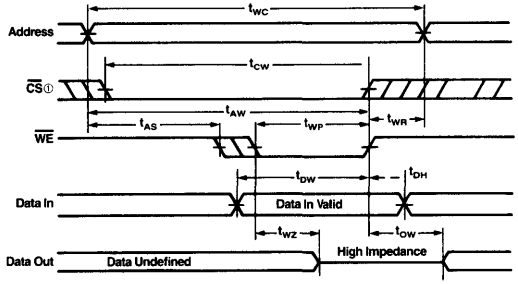
Read Cycle No. 1 ⑤⑥



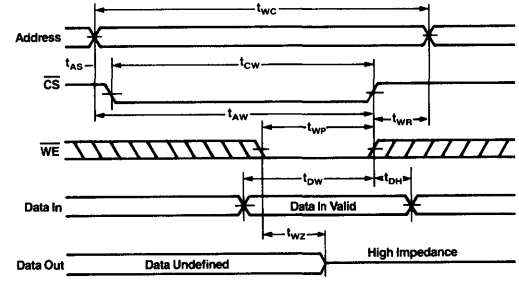
Read Cycle No. 2 ⑤⑦



Write Cycle No. 1 ($\overline{WE}$ Controlled) ⑤



Write Cycle No. 2 ($\overline{CS}$ Controlled) ⑤



Notes:
① All Read Cycle timings are referenced from the last valid address to the first transitioning address.
② At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min, both for a given device and from device to device.
③ Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
④ Transition is measured at V_{OL} + 200mV and V_{OH} − 200mV with specified loading in Figure 2.
⑤ $\overline{WE}$ is high for Read Cycles.
⑥ Device is continuously selected, $\overline{CS}$ = V_{IL}.
⑦ Addresses valid prior to or coincident with $\overline{CS}$ transition low.

Notes:
① If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
② All Write Cycle timings are referenced from the last valid address to the first transitioning address.
③ Transition is measured at V_{OL} + 200mV and V_{OH} − 200mV with specified loading in Figure 2.
④ Transition is measured ±200mV from steady state voltage with specified loading in Figure 2.
⑤ $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

7

μPD2149
1,024 x 4-Bit
STATIC NMOS RAM

Revision 1

Description

The μPD2149 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits. Using a scaled NMOS technology, it incorporates an innovative design approach which provides the ease-of-use features associated with non-clocked static memories.

The μPD2149 is encapsulated in an 18-pin ceramic package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5 V supply. The data is read out non-destructively and has the same polarity as the input data.

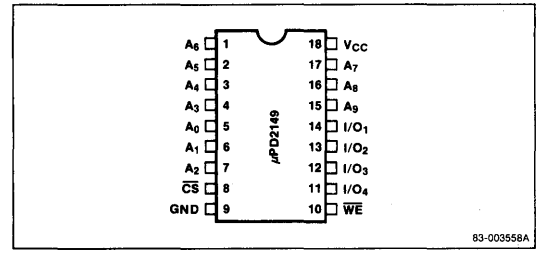
Features

- ☐ Completely static memory - no clock or timing strobe required
- ☐ Equal access and cycle times, faster chip select access
- ☐ Single +5 V supply
- ☐ High density 18-pin package
- ☐ Directly TTL compatible - all inputs and outputs
- ☐ Common input and output
- ☐ Three-state outputs
- ☐ Power dissipation: 180 mA max

Performance Ranges

Device	Address Access Time (Max)	$\overline{CS}$ Access Time (Max)
μPD2149-2	35 ns	15 ns
μPD2149-1	45 ns	20 ns
μPD2149	55 ns	25 ns

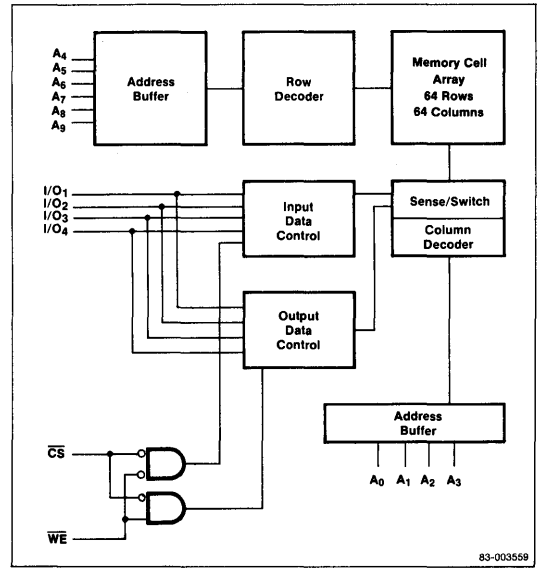
Pin Configuration



Pin Identification

No.	Symbol	Function
1-7, 15-17	A_0-A_9	Address inputs
8	$\overline{CS}$	Chip select input
9	GND	Ground
10	$\overline{WE}$	Write enable input
11-14	I/O_1-I/O_4	Data input/output
18	V_{CC}	+5 V Power supply

Block Diagram



7

Absolute Maximum Ratings

Operating temperature, T_{OPR}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +150°C
Voltage on any pin	−1.5 to +7.0 V
DC output current	20 mA
Power dissipation, P_D	1.2 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70°C; $V_{CC} = +5$ V ± 10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input leakage current	I_{LI}		+10	μA	V_{IN} = GND to V_{CC}
Output leakage current	I_{LO}		+50	μA	$\overline{CS} = V_{IH}$, V_{OUT} = GND to 4.5 V
Power supply current	I_{CC}		180	mA	$V_{IN} = V_{CC}$, I/O = open
Input low voltage	V_{IL}		0.8	V	
Input high voltage	V_{IH}	2.1	V_{CC}	V	
Output low voltage	V_{OL}		0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4		V	I_{OH} = −4 mA
Output short circuit current	I_{OS}		±200	mA	V_{OUT} = GND to V_{CC}

Note

(1) The operating temperature range is guaranteed with transverse air flow exceeding 400 feet per minute.

Capacitance

$T_A = 25$°C, f = 1 MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	V_{IN} = 0 V
Data output capacitance	C_{DOUT}			7	pF	V_{DOUT} = 0 V

Note

(1) These parameters are sampled and not 100% tested.

AC Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ± 10%

Parameter	Symbol	Limits μPD2149-2 Min	Limits μPD2149-2 Max	Limits μPD2149-1 Min	Limits μPD2149-1 Max	Limits μPD2149 Min	Limits μPD2149 Max	Unit	Test Conditions
Read Cycle									
Read cycle time	t_{RC}	35		45		55		ns	
Access time	t_A		35		45		55	ns	
Chip selection to output valid	t_{CO}		15		20		25	ns	
Chip selection to output active	t_{CX}	5		5		5		ns	(Note 4)
Output high-Z from deselection	t_{OTD}		10		15		20	ns	(Note 3)
Output hold from address change	t_{OH}	5		5		5		ns	
Write Cycle									
Write cycle time	t_{WC}	35		45		55		ns	
Chip selection to end of write	t_{CW}	30		40		50		ns	
Address valid to end of write	t_{AW}	30		40		50		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	30		35		40		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	20		20		20		ns	
Data hold time	t_{DH}	5		5		5		ns	
Write enabled to output in high-Z	t_{WZ}	0	10	0	15	0	20	ns	(Note 3)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 4)

Notes:

(1) AC test conditions:
Input pulse levels = GND to 3.0 V,
Input pulse rise and fall times = 5 ns,
Timing reference levels = 1.5 V. See figures 1 and 2 for output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with loading shown in figure 2.

(4) Transition is measured ±200 mV from steady state voltage with loading shown in figure 2.

Figure 1. Output Load

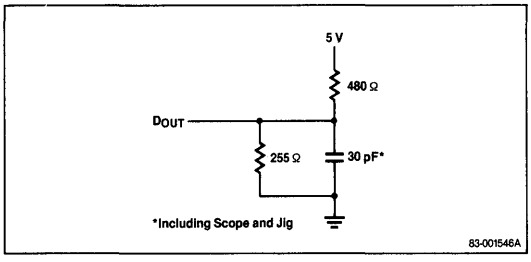
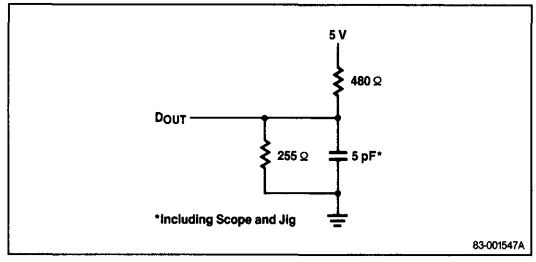


Figure 2. Output Load for t_{CX}, t_{OTD}, t_{WZ}, and t_{OW}



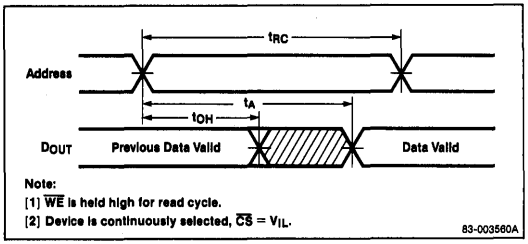
Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O
H	X	Not selected	Hi-Z
L	H	Read	D_{OUT}
L	L	Write	Hi-Z

7

Timing Waveforms

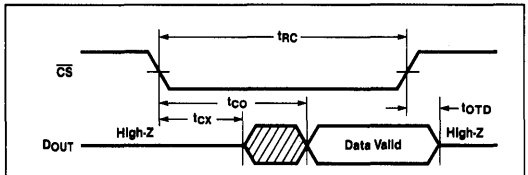
Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{WE}$ is held high for read cycle.
[2] Device is continuously selected, $\overline{CS}$ = V_{IL}.

83-003560A

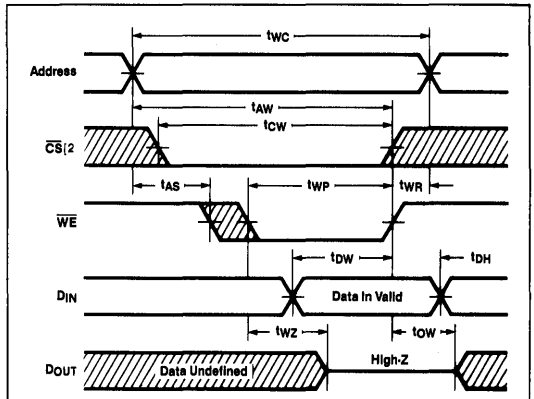
Read Cycle No. 2 (Chip Select Access)



Notes:
[1] $\overline{WE}$ is held high for read cycle.
[2] Address valid prior to or coincident with $\overline{CS}$ transition low.

83-003890A

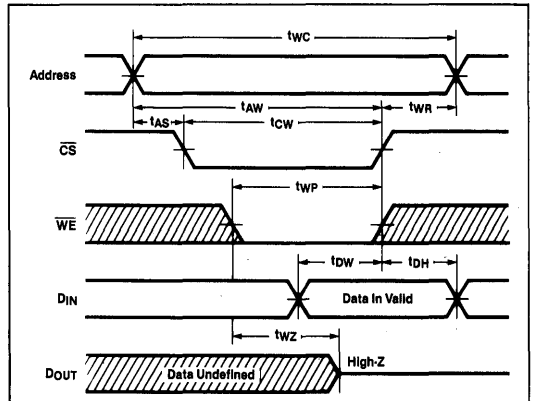
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in a high-impedance state.

83-001637A

Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: [1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-001549A

μPD4016
2,048 x 8-BIT
STATIC NMOS RAM

Revision 3

Description

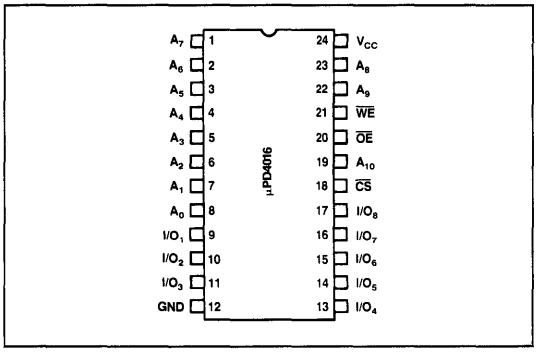
The μPD4016 is a 16,384-bit static Random-access Memory device organized as 2,048 words by 8 bits. Using a scaled NMOS technology, its design provides the ease-of-use features associated with nonclocked static memories. The μPD4016 has a three-state output and offers a standby mode with an attendant 75% savings in power consumption. It features equal access and cycle times and provides an output enable function that eliminates the need for external bus buffers. The μPD4016 is packaged in a 600-mil-wide standard 24-pin dual-in-line package which is plug-compatible with 16K EPROMS.

Features

- ☐ Scaled NMOS technology
- ☐ Completely static memory: no clock, no refresh
- ☐ Equal access and cycle times
- ☐ Single +5V power supply
- ☐ Automatic power-down
- ☐ All inputs and outputs directly TTL-compatible
- ☐ Common I/O capability
- ☐ $\overline{OE}$ eliminates need for external bus buffers
- ☐ Three-state outputs
- ☐ Plug-compatible with 16K 5V EPROMS (600 mil)
- ☐ Low power dissipation in standby mode
- ☐ Available in a standard 24-pin dual-in-line package (600-mil width)
- ☐ 4 performance ranges:

Device	Access Time	R/W Cycle Time	Power Supply Active	Power Supply Standby
μPD4016C-1	250ns	250ns	60mA	15mA
μPD4016C-2	200ns	200ns	60mA	15mA
μPD4016C-3	150ns	150ns	60mA	15mA
μPD4016C-5	120ns	120ns	60mA	15mA

Pin Configuration



Pin Identification

Pin No.	Symbol	Description
1–8, 22, 23	A_0–A_{10}	Address Inputs
9–11, 13–17	I/O_1–I/O_8	Data Input/Output
12	GND	Ground
18	$\overline{CS}$	Chip Select
20	$\overline{OE}$	Output Enable
21	$\overline{WE}$	Write Enable
24	V_{CC}	+5V Power Supply

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
H	X	X	Not Selected	High-Z	Standby
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
L	L	L	Write	D_{IN}	Active

Absolute Maximum Ratings*

Temperature Under Bias	−10°C to +85°C
Storage Temperature, T_{ST}	−55°C to +125°C
Voltage on any Pin with Respect to Ground	−1.5V to +7V
DC Output Current, I_O	20mA
Power Dissipation, P_D	1W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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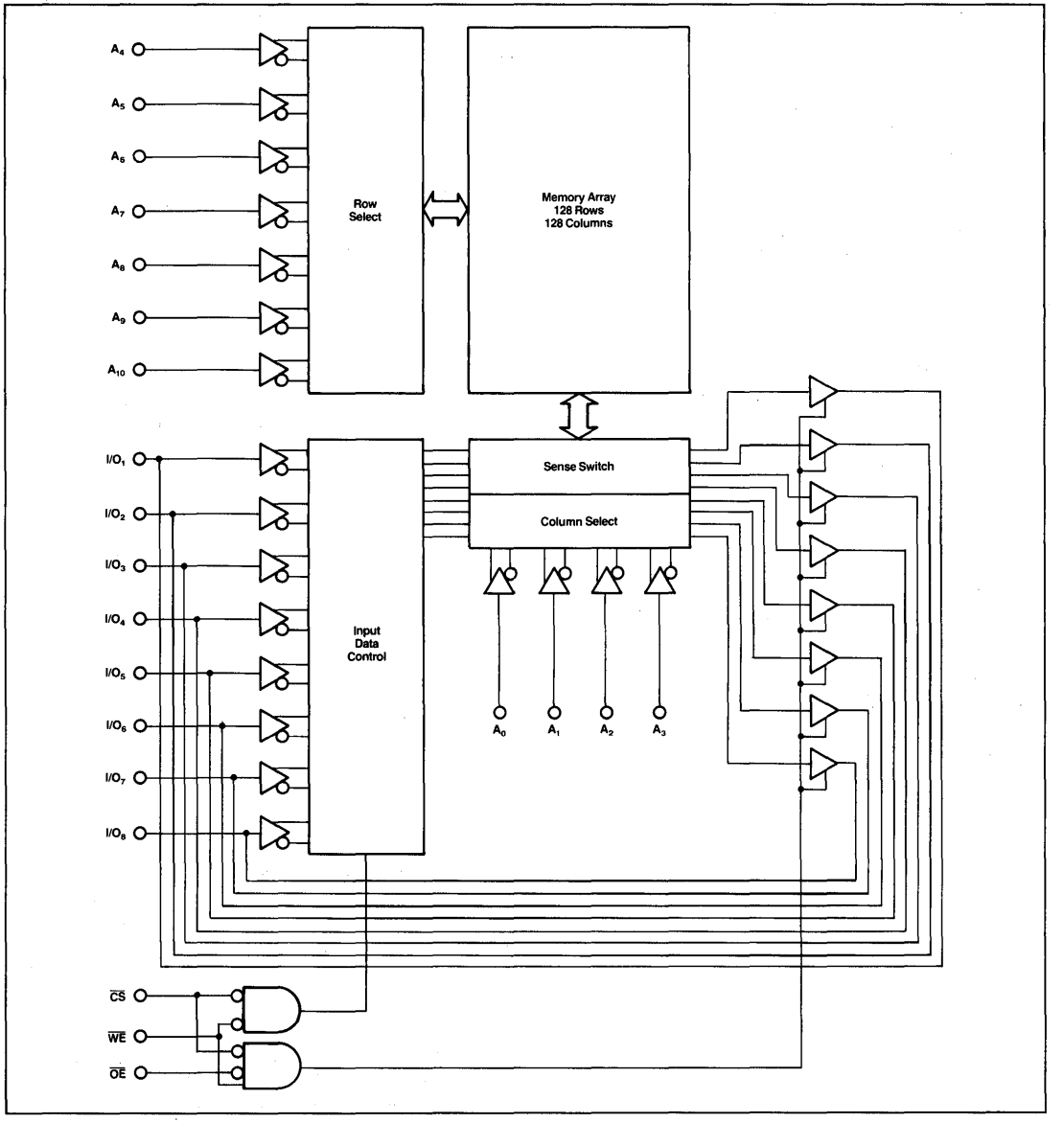
Block Diagram



Capacitance ①

T_A = 25°C; f = 1MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			5	pF	V_{IN} = 0V
I/O Capacitance	$C_{I/O}$			7	pF	$V_{I/O}$ = 0V

Note: ① This parameter is sampled and not 100% tested.

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = 5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions ①
Input Leakage Current	I_{LI}			10	μA	V_{CC} = Max V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}			10	μA	V_{CC} = Max; $\overline{CS}$ = V_{IH} V_{OUT} = GND to V_{CC}
Operating Current	I_{CC}			60	mA	V_{CC} = Max; $\overline{CS}$ = V_{IL} (outputs open)
Standby Current	I_{SB}			15	mA	V_{CC} = Min to Max; $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.5		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = 1mA
Output Short-circuit Current	I_{OS}		70		mA	V_{OUT} = GND to V_{CC}

Note: ① Input pulse levels: 0.8V to 2.2V
Input rise and fall times: 10ns
Input timing reference levels: 1.5V
Output timing reference levels: 1.5V

Figure 1. Loading Conditions Test Circuit

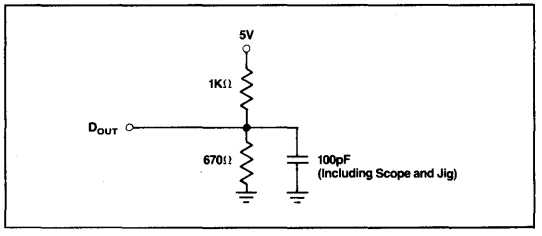
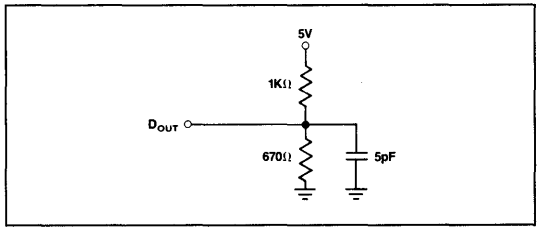


Figure 2. Input Pulse Test Circuit



AC Characteristics

T_A = 0°C to +70°C; V_{CC} = 5V ± 10%

Read Cycle

Parameter	Symbol	Limits ① 4016-5 Min	4016-5 Max	4016-3 Min	4016-3 Max	4016-2 Min	4016-2 Max	4016-1 Min	4016-1 Max	Unit	Notes
Read Cycle Time	t_{RC}	120		150		200		250		ns	②
Address Access Time	t_{AA}		120		150		200		250	ns	
Chip Select Access Time	t_{ACS}		120		150		200		250	ns	③
Output Hold from Address Change	t_{OH}	10		10		10		10		ns	
Chip Selection to Output in Low-Z	t_{LZ}	10		10		10		10		ns	④ ⑤
Chip Deselection to Output in High-Z	t_{HZ}		45		50		60		80	ns	④ ⑤
Output Enable to Output Valid	t_{OE}		50		70		90		110	ns	
Output Enable to Output in Low-Z	t_{OLZ}	10		10		10		10		ns	④ ⑤
Output Disable to Output in High-Z	t_{OHZ}		45		50		60		80	ns	④ ⑤
Chip Selection to Power-up Time	t_{PU}	0		0		0		0		ns	⑤
Chip Deselection to Power-down Time	t_{PD}		60		70		90		110	ns	⑤

Write Cycle

Parameter	Symbol	Limits ① 4016-5 Min	4016-5 Max	4016-3 Min	4016-3 Max	4016-2 Min	4016-2 Max	4016-1 Min	4016-1 Max	Unit	Notes
Write Cycle Time	t_{WC}	120		150		200		250		ns	
Chip Selection to End of Write	t_{CW}	90		120		160		200		ns	
Address Valid to End of Write	t_{AW}	80		90		120		150		ns	
Address Set-up Time	t_{AS}	0		0		0		0		ns	
Write Pulse Width	t_{WP}	70		80		100		130		ns	⑥
Write Recovery Time	t_{WR}	10		10		10		10		ns	
Data Valid to End of Write	t_{DW}	45		50		60		80		ns	
Data Hold Time	t_{DH}	0		0		0		0		ns	
Write Enabled to Output in High-Z	t_{WZ}		45		50		60		80	ns	⑤ ⑦
Output Active from End of Write	t_{OW}	10		10		10		10		ns	⑤ ⑦

Notes: ① See Part No. / Package Width table below.
② All read cycle timings are referenced from the last valid address to the first transition address.
③ Address valid prior to or coincident with $\overline{CS}$ transition low.
④ Transition is measured ± 200mV from steady-state voltage with specified load of Figure 1.
⑤ This parameter is sampled and not 100% tested.
⑥ If $\overline{CS}$ and $\overline{OE}$ are both low before write enabled, $t_{WP} = t_{WZ} + t_{OW}$.
⑦ Transition is measured ± 200mV from steady-state voltage with specified load of Figure 2.

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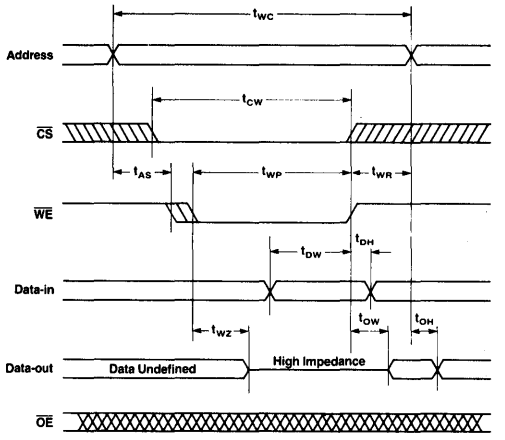
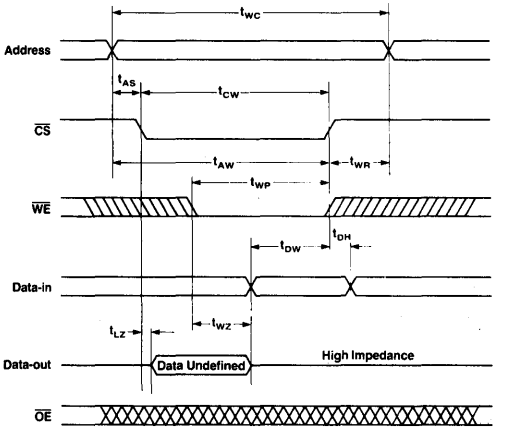
Timing Waveforms

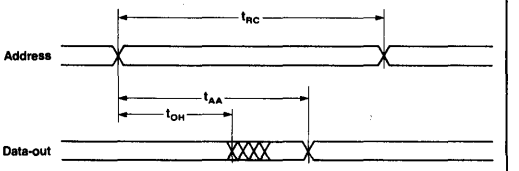
Write Cycle No. 1 ($\overline{WE}$ Controlled)



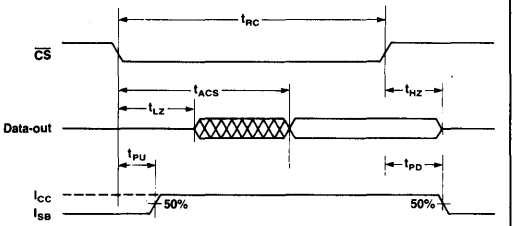
Write Cycle No. 2 ($\overline{CS}$ Controlled)



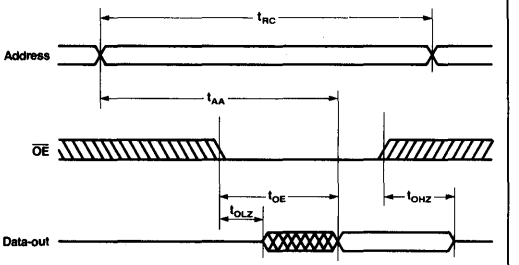
Read Cycle No. 1 ① ② ③



Read Cycle No. 2 ① ③ ④



Read Cycle No. 3 ① ②



Notes: ① $\overline{WE}$ is high for read cycles.
② Device is continuously selected, $\overline{CS}$ = V_{IL}.
③ $\overline{OE}$ = V_{IL}.
④ Address valid prior to or coincident with $\overline{CS}$ transition low.

μPD4311
16,384 x 1-BIT
STATIC MIX-MOS RAM

Description

The μPD4311 is a high-speed, low-power, 16,384-word by 1-bit static MIX-MOS RAM fabricated with a short-channel, silicon-gate MIX-MOS technology. The μPD4311 is a low standby power device using N-channel memory cells with polysilicon resistors. Additionally, an excellent circuitry technique achieves very high speed and low operating power. The μPD4311 requires no clock or refreshing to operate.

The μPD4311 is fully compatible with the μPD2167. It is packaged in a 20-pin plastic DIP with the standard 2167 pinout (μPD4311C) and a 20-pin Cerdip package (μPD4311D).

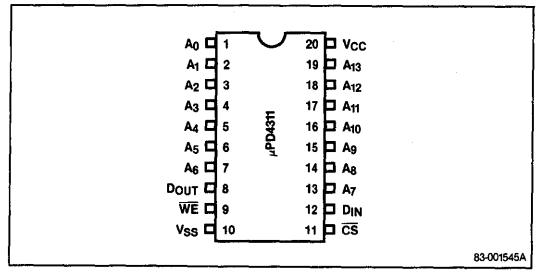
Features

- ☐ Single +5 V supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL-compatible — all inputs and outputs
- ☐ Separated data input and output
- ☐ Three-state output
- ☐ Standard 300 mil plastic DIP and Cerdip
- ☐ Compatible with μPD2167

Performance Ranges

Device	Access Time	Power Supply (Max)	
		Active	Standby
μPD4311C/D-35	35 ns	80	2 mA
μPD4311C/D-45	45 ns	80	2 mA
μPD4311C/D-55	55 ns	80	2 mA

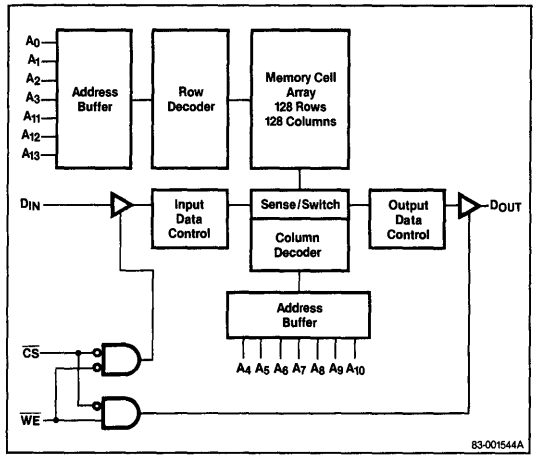
Pin Configuration



Pin Identification

No.	Symbol	Function
1–7, 13–19	A_0–A_{13}	Address input
12	D_{IN}	Data input
8	D_{OUT}	Data output
11	$\overline{CS}$	Chip select
9	$\overline{WE}$	Write enable
20	V_{CC}	+5 V power supply
10	V_{SS}	Ground

Block Diagram



7

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 V to +7.0 V
Input voltage, V_{IN}	−0.5 V [1] to +7.0 V
Output voltage, V_{OUT}	−0.5 V to +7.0 V
Operating temperature, T_{OPR}	0 to 70°C
Storage temperature, T_{STG}:	
−μPD4311C	−55 to 125°C
−μPD4311D	−65 to 150°C
Power dissipation, P_D	1.0 W

Note: [1] V_{IN} = −3.0 V min for 20 ns pulse.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz [Note 1]

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	V_{IN} = 0 V
Data output capacitance	C_{DOUT}			6	pF	V_{DOUT} = 0 V

Note: [1] This parameter is sampled and not 100% tested.

Recommended DC Operating Conditions

T_A = 0 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage low	V_{IL}	−0.5[1]		0.8	V
Input voltage high	V_{IH}	2.2		6.0	V

Note: [1] V_{IL} = −3.0 V min for 20 ns pulse.

DC Characteristics

T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}, V_{CC} = Max
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}, $\overline{CS}$ = V_{IH}, V_{CC} = Max
Operating supply current	I_{CC}			80	mA	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0 mA
Standby supply current	I_{SB}			15	mA	$\overline{CS}$ = V_{IH}
Standby supply current	I_{SB1}			2	mA	$\overline{CS}$ = V_{CC} − 0.2 V, V_{IN} < 0.2 V or > V_{CC} − 0.2 V
Output voltage low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics [Note 1]

$T_A = 0°C$ to $70°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits μPD4311-35 Min	Limits μPD4311-35 Max	Limits μPD4311-45 Min	Limits μPD4311-45 Max	Limits μPD4311-55 Min	Limits μPD4311-55 Max	Unit	Test Conditions
Read Cycle									
Read cycle time	t_{RC}	35		45		55		ns	[Note 2]
Address access time	t_{AA}		35		45		55	ns	
Chip select access time	t_{ACS}		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in Lo-Z	t_{LZ}	5		5		5		ns	[Note 3]
Chip deselect to output in Hi-Z	t_{HZ}	0	20	0	25	0	30	ns	[Note 4]
Chip select to power-up time	t_{PU}	0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	35	0	40	0	45	ns	
Write Cycle									
Write cycle time	t_{WC}	35		45		55		ns	[Note 2]
Chip select to end of write	t_{CW}	35		40		45		ns	
Address valid to end of write	t_{AW}	35		40		45		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	25		30		35		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	20		25		25		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in Hi-Z	t_{WZ}	0	20	0	25	0	30	ns	[Note 4]
Output active from end of write	t_{OW}	0		0		0		ns	[Note 3]

Notes: [1] AC test conditions:
Input pulse levels = GND to 3.0 V
Input pulse rise and fall times = 5 ns
Timing reference levels = 1.5 V. See figures 1 and 2 for output load.
[2] All read and write cycle timings are referenced from the last valid address to the first transitioning address.
[3] Transition is measured ±200 mV from steady state voltage with loading shown in figure 2.
[4] Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with loading shown in figure 2.

Truth Table

$\overline{CS}$	$\overline{WE}$	MODE	I/O	I_{CC}
H	X	Not selected	Hi-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	Hi-Z	Active

Figure 1. Output Load

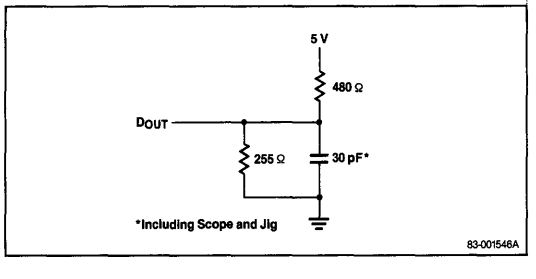
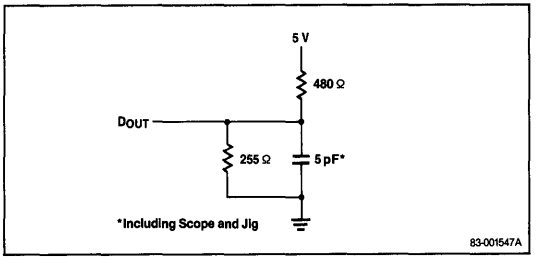


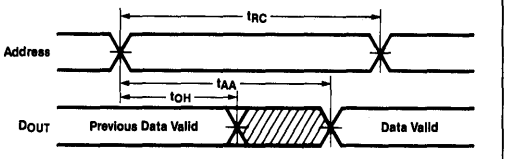
Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}



7

Timing Waveforms

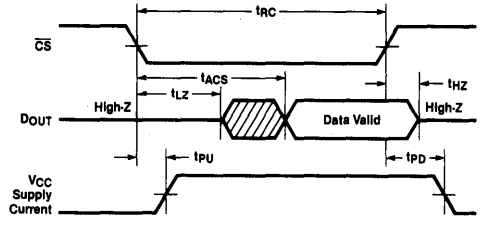
Read Cycle No. 1 (Address Access)



Notes: [1] WE is held high for read cycle.
[2] Device is continuously selected, $\overline{CS}$ + V_{IL}.

83-001636A

Read Cycle No.2 (Chip Select Access)

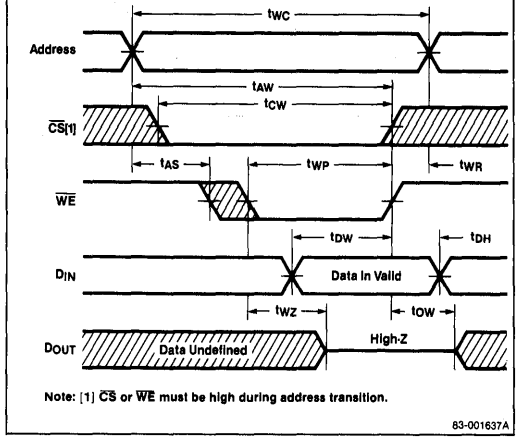


Notes: [1] $\overline{WE}$ is held high for read cycle.
[2] Address valid prior to or coincident with $\overline{CS}$ transition low.

83-001548A

Timing Waveforms (cont)

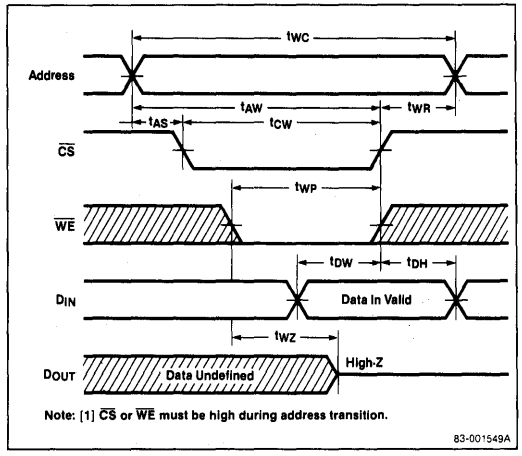
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note: [1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-001637A

Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: [1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-001549A

NEC Electronics Inc.

μPD4314
4,096 x 4-BIT
STATIC MIX-MOS RAM

PRELIMINARY INFORMATION

Revision 1

Description

The μPD4314 is a high-speed, low-power, 4,096-word by 4-bit static MIX-MOS RAM fabricated with a short-channel, silicon-gate MIX-MOS technology. The μPD4314 is a low standby power device using N-channel memory cells with polysilicon resistors. Additionally, a unique circuitry technique achieves very high speed and low operating power. The μPD4314 requires no clock or refreshing to operate.

The μPD4314 is packaged in a standard 20-pin plastic DIP.

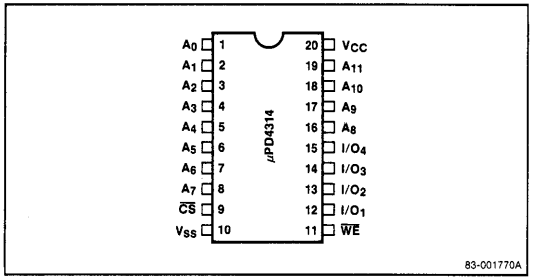
Features

- ☐ Single +5 V supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL compatible — all inputs and outputs
- ☐ Common I/O using three-state output
- ☐ Standard 300 mil 20-pin plastic DIP

Performance Ranges

Device	Access Time (Max)	Cycle Time (Min)	Power Supply (Max) Active	Standby
μPD4314C-35	35 ns	35 ns	80 mA	2 mA
μPD4314C-45	45 ns	45 ns	80 mA	2 mA
μPD4314C-55	55 ns	55 ns	80 mA	2 mA

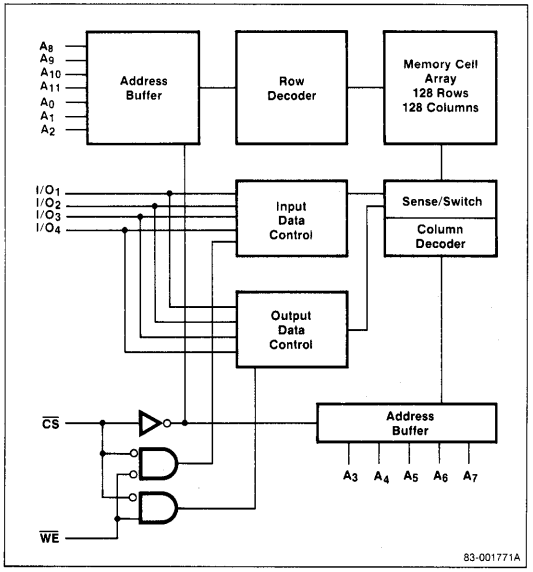
Pin Configuration



Pin Identification

No.	Symbol	Function
1-8, 16-19	A_0-A_{11}	Address input
12-15	I/O_1-I/O_4	Data input/output
9	$\overline{CS}$	Chip select input
11	$\overline{WE}$	Write enable input
20	V_{CC}	+5 V Power supply
10	V_{SS}	Ground

Block Diagram



7

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 V to +7.0 V
Input voltage, V_{IN}	−0.5 V [1] to +7.0 V
Output voltage, V_{OUT}	−0.5 V [1] to +7.0 V
Operating temperature, T_{OPR}	0 to 70°C
Storage temperature, T_{STG}	−55 to 125°C
Power dissipation, P_D	1.0 W

Note: [1] V_{IN} = −3.0 V for 20 ns max pulse

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

T_A = 0 to +70°C

		Limits			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage low	V_{IL}	−0.5[1]		0.8	V
Input voltage high	V_{IH}	2.2		V_{CC} + 0.3	V

Note: [1] V_{IL} = −3.0 V for 20 ns max pulse

DC Characteristics

T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}, V_{CC} = Max
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}, $\overline{CS}$ = V_{IH}, V_{CC} = Max
Operating supply current	I_{CC}		60	80	mA	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0 mA
Standby supply current	I_{SB}		6	20	mA	$\overline{CS}$ = V_{IH}
Standby supply current	I_{SB1}			2	mA	$\overline{CS}$ = V_{CC} − 0.2 V, V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Capacitance

T_A = 25°C, f = 1 MHz [Note 1]

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input capacitance	C_{IN}			5	pF	V_{IN} = 0 V
Data output capacitance	C_{DOUT}			7	pF	V_{DOUT} = 0 V

Note: [1] This parameter is sampled and not 100% tested.

AC Characteristics [Note 1]

T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%

		Limits							
		μPD4314-35		μPD4314-45		μPD4314-55			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Cycle									
Read cycle time	t_{RC}	35		45		55		ns	[Note 2]
Address access time	t_{AA}		35		45		55	ns	
Chip select access time	t_{ACS}		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in Lo-Z	t_{LZ}	5		5		5		ns	[Note 4]
Chip deselect to output in Hi-Z	t_{HZ}	0	20	0	25	0	30	ns	[Note 3]
Chip select to power-up time	t_{PU}	0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	35	0	45	0	55	ns	

Note: [1] AC test conditions:
Input pulse levels = GND to 3.0 V,
Input pulse rise and fall times = 5 ns,
Timing reference levels = 1.5 V. See figures 1 and 2 for output load.
[2] All read and write cycle timings are from the last valid address to the first transitioning address.
[3] Transition is measured at V_{OL} +200 mV and V_{OH} − 200 mV with loading shown in figure 2.
[4] Transition is measured ±200 mV from steady state voltage with loading shown in figure 2.

AC Characteristics [Note 1] (cont)

$T_A = 0°C$ to $70°C$, $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Limits μPD4314-35 Min	Limits μPD4314-35 Max	Limits μPD4314-45 Min	Limits μPD4314-45 Max	Limits μPD4314-55 Min	Limits μPD4314-55 Max	Unit	Test Conditions
Write Cycle									
Write cycle time	t_{WC}	35		45		55		ns	[Note 2]
Chip select to end of write	t_{CW}	35		40		45		ns	
Address valid to end of write	t_{AW}	35		40		45		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	30		40		50		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	20		25		30		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in Hi-Z	t_{WZ}	0	20	0	25	0	30	ns	[Note 3]
Output active from end of write	t_{OW}	0		0		0		ns	[Note 4]

Note: [1] AC test conditions:
Input pulse levels = GND to 3.0 V,
Input pulse rise and fall times = 5 ns,
Timing reference levels = 1.5 V. See figures 1 and 2 for output load.
[2] All read and write cycle timings are referenced from the last valid address to the first transitioning address.
[3] Transition is measured at $V_{OL} + 200$ mV and $V_{OH} - 200$ mV with loading shown in figure 2.
[4] Transition is measured ±200 mV from steady state voltage with loading shown in figure 2.

Figure 1. Output Load

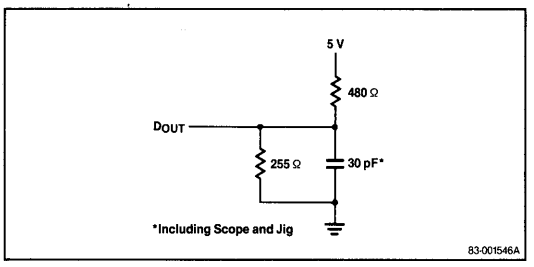
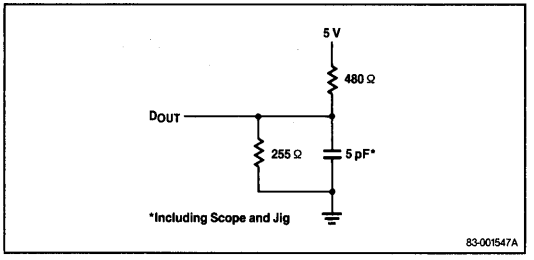


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW}



Truth Table

$\overline{CS}$	$\overline{WE}$	MODE	I/O	I_{CC}
H	X	Not selected	Hi-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	Hi-Z	Active

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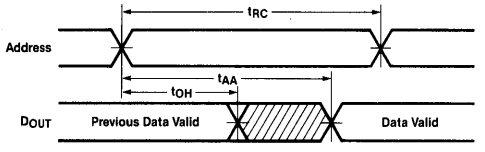
Timing Waveforms

Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{WE}$ is held high for read cycle.
[2] Device is continuously selected, $\overline{CS}$ = V_{IL}.

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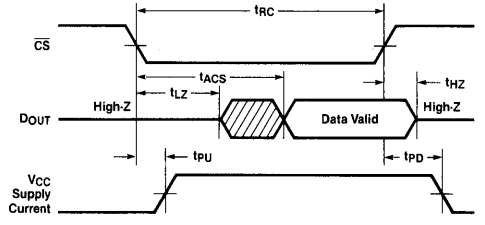
Read Cycle No. 2 (Chip Select Access)



Notes:
[1] $\overline{WE}$ is held high for read cycle.
[2] Address valid prior to or coincident with $\overline{CS}$ transition low.

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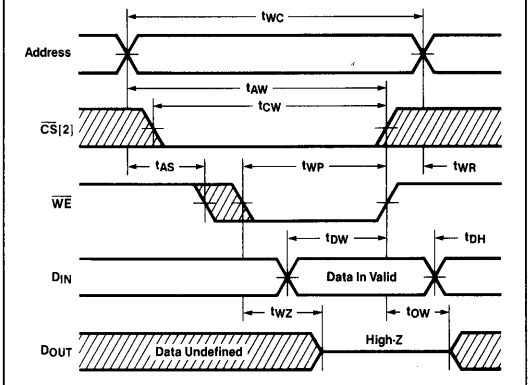
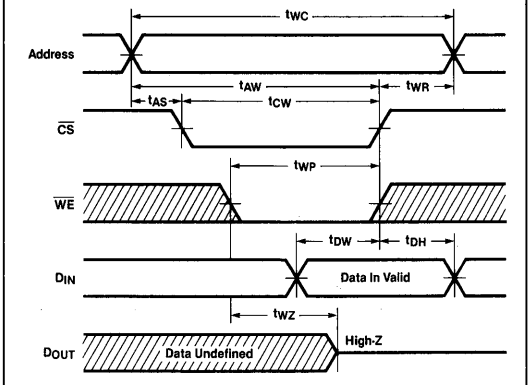
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in a high-impedance state.

83-001637A

Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: [1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-001549A

μPD4361
65,536 x 1-BIT
STATIC MIX-MOS RAM

Revision 1

Description

The μPD4361 is a high-speed, low-power, 65,536-words by 1-bit static MIX-MOS RAM fabricated with a short-channel, silicon-gate MIX-MOS process. It is a low standby power device using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors. Additionally, a unique circuitry technique achieves very high speed and low operating power. The uPD4361 requires no clock or refreshing to operate.

The μPD4361 is packaged in a 300 mil wide 22-pin plastic DIP (μPD4361C) and a 290 mil x 490 mil 22-pin ceramic leadless chip carrier (μPD4361K). The μPD4361 has two types of access times, address and chip select. In addition, the μPD4361C-L features a low-power data retention mode.

Features

- ☐ 65,536 x 1-bit organization
- ☐ Single +5 V supply
- ☐ Fully static operation—no clock or refreshing required
- ☐ All inputs and outputs TTL-compatible
- ☐ Separated data input and output
- ☐ Three-state output
- ☐ MIX-MOS process
- ☐ Data retention current of 50 μA max on the μPD4361C-L
- ☐ Standard 300 mil 22-pin plastic DIP and 290 mil x 490 mil ceramic LCC
- ☐ Standard JEDEC pin configurations

Performance Ranges

Device	Access Time	Power Supply (Max)	
		Active	Standby
μPD4361-40 (1)	40 ns	120 mA	2 mA
μPD4361-45	45 ns	120 mA	2 mA
μPD4361-55	55 ns	120 mA	2 mA
μPD4361-70 (2)	70 ns	120 mA	2 mA

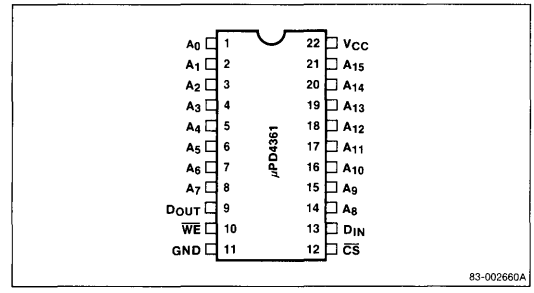
Note:

(1) μPD4361K only.

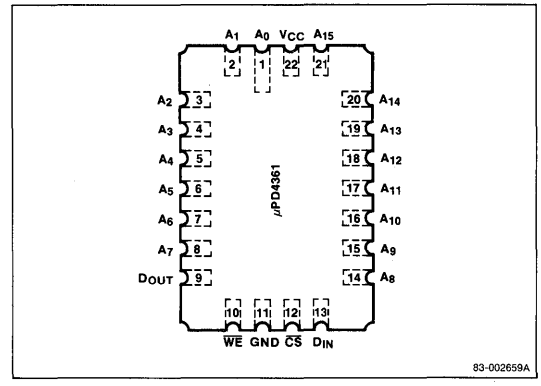
(2) μPD4361C-70/70L only.

Pin Configurations

22-Pin Plastic DIP



22-Pin Ceramic LCC



Pin Identification

No.	Symbol	Function
1-8, 14-21	A_0-A_{15}	Address inputs
9	D_{OUT}	Three-state data output
10	$\overline{WE}$	Write enable
11	GND	Ground
12	$\overline{CS}$	Chip select
13	D_{IN}	Data input
22	V_{CC}	Power supply

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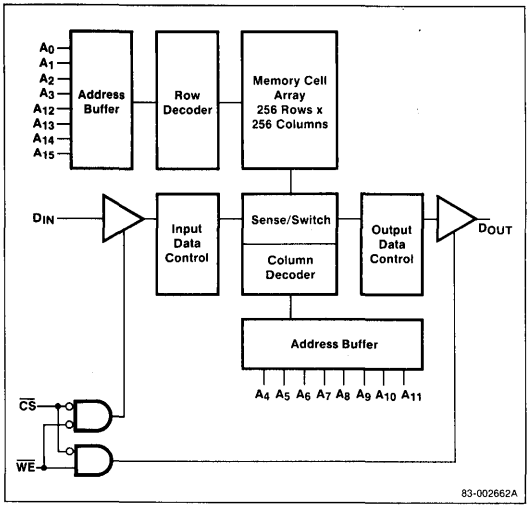
Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	Output	I_{CC}
H	X	Not selected	High-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	High-Z	Active

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to 7.0 V
Voltage on any pin, V_{IN}	−0.5 to 7.0 V (1)
Operating temperature, T_{OPR}	0 to +70°C (2)
Storage temperature, T_{STG}	−55 to +125°C (3)
Power dissipation, P_D	1.0 W

Note:

(1) −3.0 V for 20 ns pulse

(2) T_{OPR} for 4361K = −10 to +85°C

(3) T_{STG} for 4361K = −65 to +150°C

Comment: Exposing the device to stresses above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C; f = 1 MHz (1)

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_{IN}			5	pF	V_{IN} = 0 V
I/O capacitance	C_{DOUT}			7	pF	V_{DOUT} = 0 V

Note:

(1) This parameter is sampled and not 100% tested.

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = 5 V ±10%

		Limits							Test
		μPD4361C/C-L			μPD4361K				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V	
Input low voltage	V_{IL}	−0.5 (1)		0.8	−0.5 (1)		0.8	V	
Input high voltage	V_{IH}	2.2		6.0	2.2		6.0	V	
Input leakage current	I_{LI}	−2		2	−2		2	μA	V_{IN} = 0 V to V_{CC}, V_{CC} = max
Output leakage current	I_{LO}	−2		2	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}, V_{CC} = max
Operating supply current	I_{CC}			120			120	mA	$\overline{CS}$ = V_{IL}, I_{DOUT} = 0 mA
Standby supply current	I_{SB}			20			20	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2			2	mA	$\overline{CS}$ = V_{CC} − 0.2 V, V_{IN} < 0.2 V or > V_{CC} − 0.2 V
Output low voltage	V_{OL}			0.4			0.4	V	I_{OL} = 8.0 mA
Output high voltage	V_{OH}	2.4			2.4			V	I_{OH} = −4.0 mA

Note:

(1) −3.0 V for 20 ns pulse

AC Characteristics (Note 1)

$T_A = 0°C$ to $+70°C$; $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Limits								Unit
		μPD4361-40(2)		μPD4361-45		μPD4361-55		μPD4361-70(3)		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read cycle time	t_{RC} (4)	40		45		55		70		ns
Address access time	t_{AA}		40		45		55		70	ns
Chip select access time	t_{ACS}		40		45		55		70	ns
Output hold from address change	t_{OH}	5		5		5		5		ns
Chip select to output in Low-Z	t_{LZ} (6)	5		5		5		5		ns
Chip deselect to output in High-Z	t_{HZ} (5)	0	22	0	25	0	30	0	30	ns
Chip select to power-up time	t_{PU}	0		0		0		0		ns
Chip deselect to power-down time	t_{PD}	0	27	0	30	0	40	0	40	ns
Write Cycle										
Write cycle time	t_{WC} (4)	40		45		55		70		ns
Chip selection to end of write	t_{CW}	37		40		50		60		ns
Address valid to end of write	t_{AW}	37		40		50		60		ns
Address setup time	t_{AS}	0		0		0		0		ns
Write pulse width	t_{WP}	23		25		30		40		ns
Write recovery time	t_{WR}	0		0		0		0		ns
Data valid to end of write	t_{DW}	23		25		25		30		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write enabled to output in High-Z	t_{WZ} (5)	0	22	0	25	0	25	0	30	ns
Output active from end of write	t_{OW} (6)	0		0		0		0		ns

Note:

(1) AC test conditions: Input pulse levels = GND to 3.0 V; Input pulse rise and fall times = 5 ns; Timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) Available for μPD4361K only.

(3) Available for μPD4361C or μPD4361C-L only.

(4) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(5) Transition is measured at $V_{OL} + 200$ mV and $V_{OH} - 200$ mV with loading shown in figure 2.

(6) Transition is measured ±200 mV from steady state voltage with loading shown in figure 2.

Figure 1. Output Load

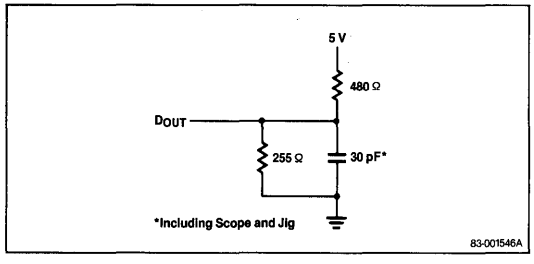
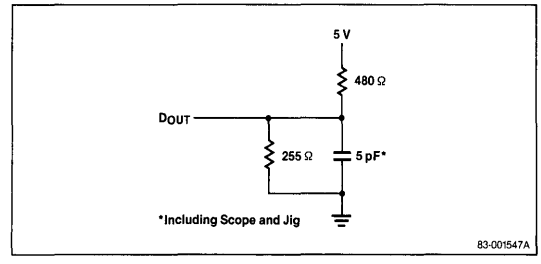


Figure 2. Output Load for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}



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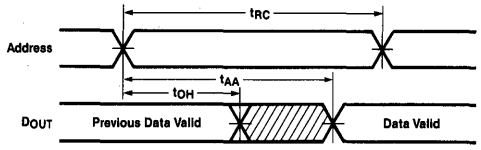
Timing Waveforms

Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{WE}$ is held high for read cycle.
[2] Device is continuously selected, $\overline{CS}$ = V_{IL}.

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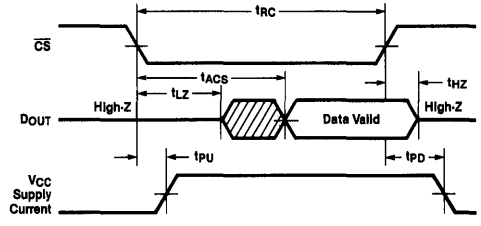
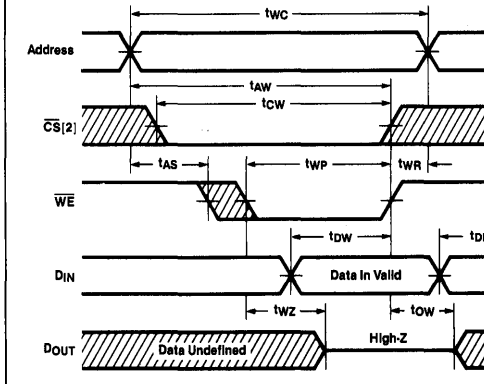
Read Cycle No. 2 (Chip Select Access)



Note: [1] $\overline{WE}$ is held high for read cycle.
[2] Address valid prior to or coincident with $\overline{CS}$ transition low.

83-001548A

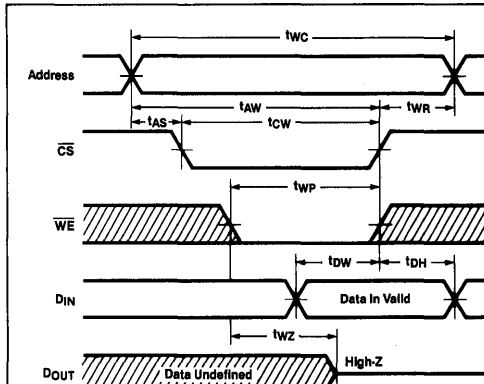
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in a high-impedance state.

83-001637A

Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: [1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-001549A

Low V_{CC} Data Retention Characteristics (Note 1)

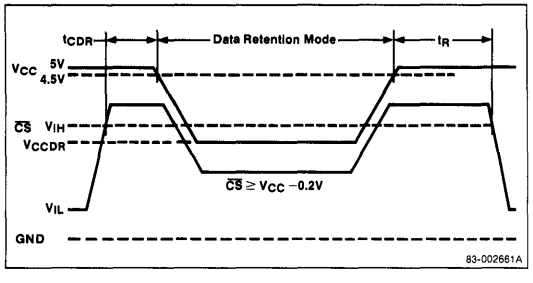
$T_A = 0°C$ to $70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $0 \text{ V} \leq V_{IN} \leq 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	$V_{CC} = 3.0$ V, $CS \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $0 \text{ V} \leq V_{IN} \leq 0.2$ V
Chip deselect to data retention time	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Note:

(1) For μPD4361C-L only.

Data Retention



μPD4362
16,384 x 4-BIT
STATIC MIX-MOS RAM

Description

The μPD4362 is a high-speed, low-power, 16,384-words by 4-bits static MIX-MOS RAM fabricated with a short-channel, silicon-gate MIX-MOS process. It is a low standby power device using N-channel memory cells with polysilicon resistors. Additionally, a unique circuitry technique achieves very high speed and low operating power. The μPD4362 requires no clock or refreshing to operate.

The μPD4362 is packaged in a standard 22-pin plastic DIP.

Features

- ☐ Single +5 V supply
- ☐ Fully static operation — no clock or refresh required
- ☐ All inputs and outputs TTL-compatible
- ☐ Common I/O capability
- ☐ Standard 300 mil 22-pin plastic DIP

Performance Ranges

Device	Access Time	Power Supply (Max) Active	Standby
μPD4362C-45	45 ns	90 mA	2 mA
μPD4362C-55	55 ns	90 mA	2 mA
μPD4362C-70	70 ns	90 mA	2 mA

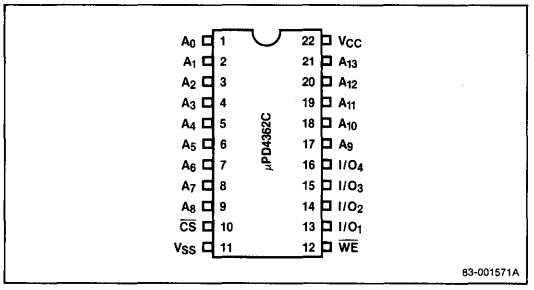
Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to 7.0 V
All input and ouput voltages, V_{IN}	−0.5 (1) to 7.0 V
Operating temperature, T_{OPR}	0°C to +70°C
Storage temperature, T_{STG}	−55°C to +125°C
Power dissipation, P_D	1.0 W

Note: (1) $V_{IN} = -3.0$ V for 20 ns pulse

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

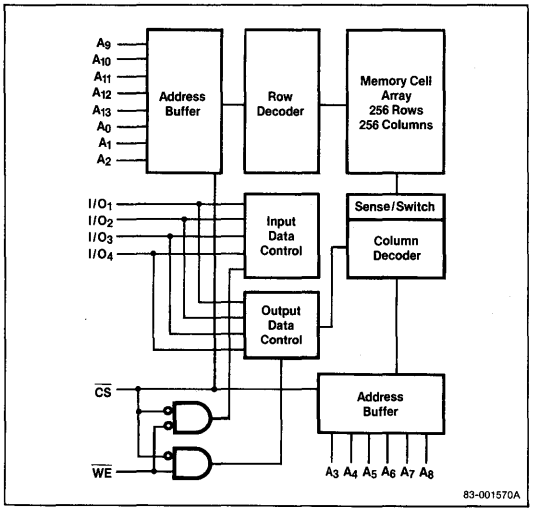
Pin Configuration



Pin Identification

No.	Symbol	Function
1-9, 17-21	$A_0 - A_{13}$	Address input
13-16	$I/O_1 - I/O_4$	Data input/output
10	$\overline{CS}$	Chip select
12	$\overline{WE}$	Write enable
22	V_{CC}	Power supply
11	V_{SS}	Ground

Block Diagram



7

Recommended DC Operating Conditions

$T_A = 0°C$ to $70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.5 (1)		0.8	V
Input high voltage	V_{IH}	2.2		$V_{CC} + 0.3$	V

Note: (1) $V_{IL} = -3.0$ V for 20 ns pulse

Capacitance

$T_A = 25°C$; $f = 1$ MHz (1)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	$V_{IN} = 0$ V
I/O capacitance	C_{DOUT}			7	pF	$V_{DOUT} = 0$ V

Note: (1) This parameter is sampled and not 100% tested.

DC Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = 5$ V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	$V_{IN} = 0$ - V_{CC}; V_{CC} = MAX
Output leakage current	I_{LO}	−2		2	μA	$V_{OUT} = 0$ - V_{CC}; $\overline{CS} = V_{IH}$, V_{CC} = MAX
Operating supply current	I_{CC}			90	mA	$\overline{CS} = V_{IL}$, $I_{DOUT} = 0$ mA
Standby supply current	I_{SB}			20	mA	$\overline{CS} = V_{IH}$
	I_{SB1}			2	mA	$\overline{CS} = V_{CC} - 0.2$ V; $V_{IN} < 0.2$ V or $> V_{CC} - 0.2$ V
Output low voltage	V_{OL}			0.4	V	$I_{OL} = 8.0$ mA
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -4.0$ mA

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	Not selected	High-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	High-Z	Active

AC Characteristics

$T_A = 0°C$ to $+70°C$; $V_{CC} = 5$ V ± 10%

Parameter	Symbol	Limits 4362-45 Min	Max	4362-55 Min	Max	4362-70 Min	Max	Unit
Read Cycle								
Read cycle time	t_{RC} (2)	45		55		70		ns
Address access time	t_{AA}		45		55		70	ns
Chip select access time	t_{ACS}		45		55		70	ns
Output hold from address change	t_{OH}	5		5		5		ns
Chip selection to output in low-Z	t_{LZ} (3)	5		5		5		ns
Chip deselection to output in high-Z	t_{HZ} (4)	0	25	0	25	0	30	ns
Chip selection to power-up time	t_{PU}	0		0		0		ns
Chip deselection to power-down time	t_{PD}	0	45	0	55	0	55	ns
Write Cycle								
Write cycle time	t_{WC} (2)	45		55		70		ns
Chip selection to end of write	t_{CW}	40		50		60		ns
Address valid to end of write	t_{AW}	40		50		60		ns
Address set-up time	t_{AS}	0		0		0		ns
Write pulse width	t_{WP}	40		50		60		ns
Write recovery time	t_{WR}	0		0		0		ns
Data valid to end of write	t_{DW}	20		25		30		ns
Data hold time	t_{DH}	0		0		0		ns
Write enabled to output in high-Z	t_{WZ} (4)	0	20	0	25	0	30	ns
Output active from end of write	t_{OW} (3)	0		0		0		ns

Note: (1) AC test conditions: input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured ±200 mV from steady state voltage with loading shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with loading shown in figure 2.

Figure 1. Output Load

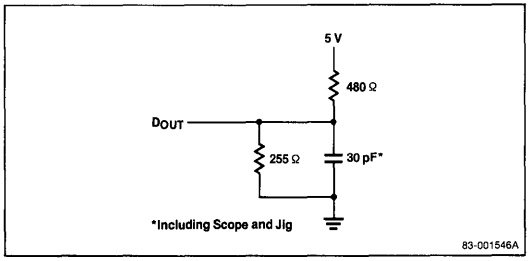
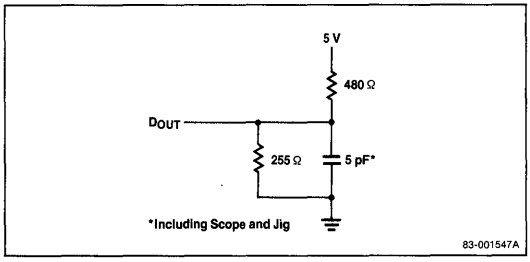
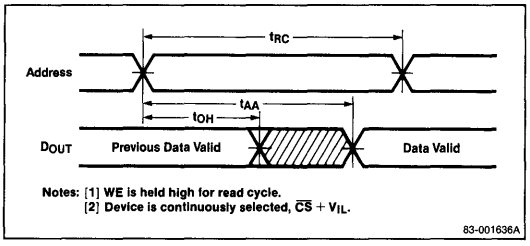


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW}

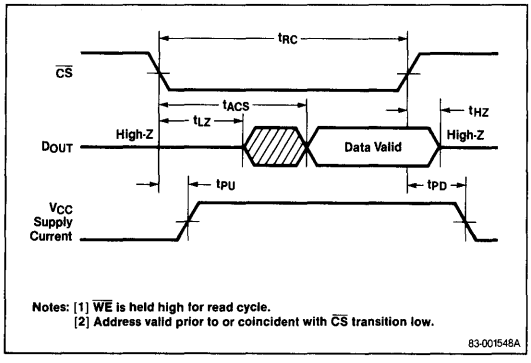


Timing Waveforms

Read Cycle No. 1 (Address Access)

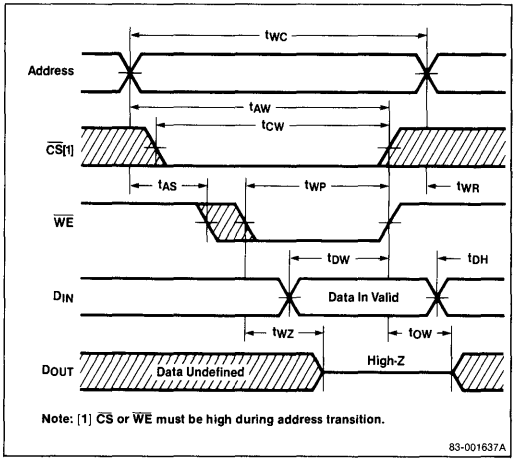


Read Cycle No. 2 (Chip Select Access)

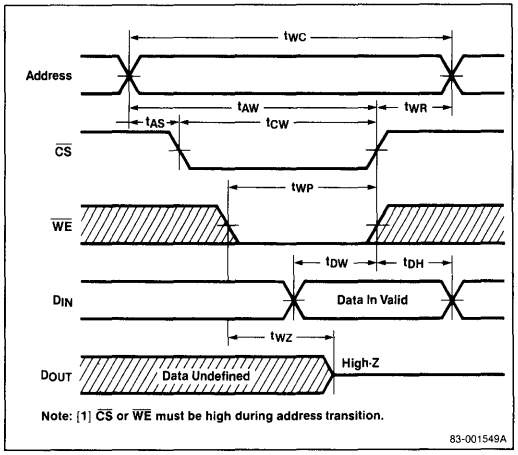


Timing Waveforms (cont)

Write Cycle No. 1 (WE Controlled)



Write Cycle No. 2 (CS Controlled)



7

μPD4364
8,192 x 8-BIT
STATIC MIX-MOS RAM

Revision 1

Description

The μPD4364 is a high-speed, low-power, 8,192-word by 8-bit static MIX-MOS RAM fabricated with advanced silicon-gate MIX-MOS technology. The μPD4364 is a low standby power device using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors. Furthermore, a unique circuitry technique makes the μPD4364 a very low operating power device which requires no clock or refreshing to operate.

Two chip enable inputs are provided for battery back-up application, and an output enable input is included for easy interface. Data retention is guaranteed at a power supply voltage as low as 2 V (μPD4364-12L/15L/20L and μPD4364-12LL/15LL/20LL).

The μPD4364 is packaged in standard 28-pin DIP and miniflat packages and is plug-in compatible with 2764-type EPROMs.

Features

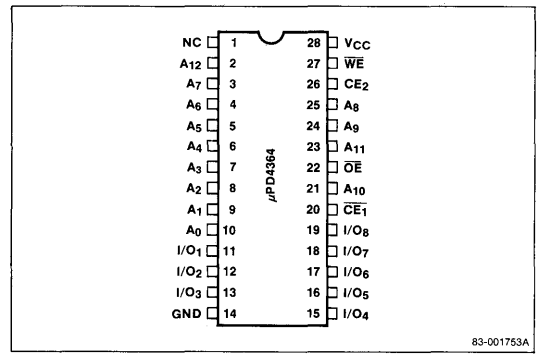
- ☐ Single +5 V power supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL compatible — all inputs and outputs
- ☐ Common I/O using three-state output
- ☐ Output enable and two chip enable inputs for easy application
- ☐ Data retention voltage
  - — μPD4364-12L/15L/20L: 2 V min
  - — μPD4364-12LL/15LL/20LL: 2 V min
- ☐ Standard 28-pin plastic DIP (μPD4364C)
- ☐ 28-pin miniflat (SOP) package (μPD4364G)
- ☐ Plug-in compatible with 2764-type EPROMs

Performance Ranges

Device	Access Time (Max)	Cycle Time (Min)	Power Supply (Max)	
			Active	Standby
μPD4364-12/12L/12LL	120 ns	120 ns	40 mA	(Note 1)
μPD4364-15/15L/15LL	150 ns	150 ns	40 mA	(Note 1)
μPD4364-20/20L/20LL	200 ns	200 ns	35 mA	(Note 1)

Note:
(1) μPD4364-12/15/20: 2 mA max;
μPD4364-12L/15L/20L: 100 μA max;
μPD4364-12LL/15LL/20LL: 50 μA max

Pin Configuration



Pin Identification

No.	Symbol	Function
1	NC	No connection
2–10, 21, 23–25	A_0–A_{12}	Address input
11–13, 15–19	I/O_1–I/O_8	Data input/output
14	GND	Ground
20	$\overline{CE_1}$	Chip enable input, active low
22	$\overline{OE}$	Output enable input
26	CE_2	Chip enable input, active high
27	$\overline{WE}$	Write enable input
28	V_{CC}	+5 V Power supply

Absolute Maximum Ratings

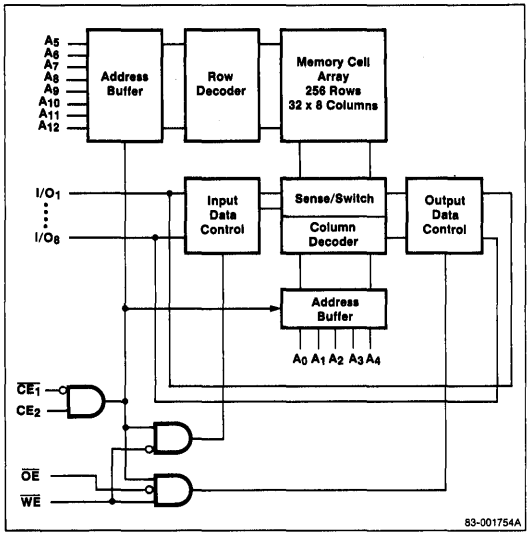
Power supply voltage, V_{CC}	−0.5 V (1) to +7.0 V
Input voltage, V_{IN}	−0.5 V (1) to V_{CC} +0.5 V
Output voltage, V_{OUT}	−0.5 V (1) to V_{CC} +0.5 V
Operating temperature, T_{OPR}	0 to 70°C
Storage temperature, T_{STG}	−55 to 125°C
Power dissipation, P_D	1.0 W

Note:
(1) −3.0 V min (Pulse width 50 ns max)

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7

Block Diagram



Capacitance

$T_A = 25°C$, f = 1.0 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	$V_{IN} = 0$ V
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O} = 0$ V

Recommended DC Operating Conditions

$T_A = 0$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage low	V_{IL}	−0.3(1)		0.8	V
Input voltage high	V_{IH}	2.2		$V_{CC}+0.5$	V

Note:
(1) −3.0 V min (Pulse width 50 ns max)

DC Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}			1	μA	$V_{IN} = 0$ V to V_{CC}
Output leakage current	I_{LO}			1	μA	$V_{I/O} = 0$ V to V_{CC}, $\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}			(1)	mA	$\overline{CE_1} = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$, Min cycle
Operating supply current	I_{CCA2}			15	mA	$\overline{CE_1} = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$, DC current
Standby supply current	I_{SB}			(2)	mA	$\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$
Standby supply current	I_{SB1}			(3)	mA	$\overline{CE_1} \geq V_{CC} - 0.2$ V, $CE_2 \geq V_{CC} - 0.2$ V
Standby supply current	I_{SB2}			(3)	mA	$CE_2 \leq 0.2$ V
Output voltage low	V_{OL}			0.4	V	$I_{OL} = 2.1$ mA
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -1.0$ mA

Notes:
(1) μPD4364-12/12L/12LL: 40 mA max; 20 mA typ
μPD4364-15/15L/15LL: 40 mA max; 18 mA typ
μPD4364-20/20L/20LL: 35 mA max; 14 mA typ

(2) μPD4364-12/15/20: 5 mA max
μPD4364-12L/15L/20L: 3 mA max
μPD4364-12LL/15LL/20LL: 3 mA max

(3) μPD4364-12/15/20: 2 mA max, 20 μA typ
μPD4364-12L/15L/20L: 100 μA max, 2 μA typ
μPD4364-12LL/15LL/20LL: 50 μA max, 2 μA typ

AC Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits μPD4364 -12/12L/12LL Min	Limits μPD4364 -12/12L/12LL Max	Limits μPD4364 -15/15L/15LL Min	Limits μPD4364 -15/15L/15LL Max	Limits μPD4364 -20/20L/20LL Min	Limits μPD4364 -20/20L/20LL Max	Unit	Test Conditions(1)
Read Cycle									
Read cycle time	t_{RC}	120		150		200		ns	
Address access time	t_{AA}		120		150		200	ns	
$\overline{CE}_1$ access time	t_{CO1}		120		150		200	ns	
CE_2 access time	t_{CO2}		120		150		200	ns	
Output enable to output valid	t_{OE}		60		70		100	ns	
Output hold from address change	t_{OH}	10		15		15		ns	
Chip enable ($\overline{CE}_1$) to output in Lo-Z	t_{LZ1}	10		15		15		ns	
Chip enable (CE_2) to output in Lo-Z	t_{LZ2}	10		15		15		ns	
Output enable to output in Lo-Z	t_{OLZ}	5		5		5		ns	
Chip enable ($\overline{CE}_1$) to output in Hi-Z	t_{HZ1}		40		50		100	ns	
Chip enable (CE_2) to output in Hi-Z	t_{HZ2}		40		50		100	ns	
Output enable to output in Hi-Z	t_{OHZ}		40		50		80	ns	
Write Cycle									
Write cycle time	t_{WC}	120		150		200		ns	
Chip enable ($\overline{CE}_1$) to end of write	t_{CW1}	85		100		180		ns	
Chip enable (CE_2) to end of write	t_{CW2}	85		100		180		ns	
Address valid to end of write	t_{AW}	85		100		180		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	70		90		140		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	50		60		80		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in Hi-Z	t_{WHZ}		40		50		100	ns	
Output active from end of write	t_{OW}	5		10		10		ns	

Note:

(1) Input pulse levels: 0.8 V to 2.4 V
Input pulse rise and fall times: 5 ns
Timing reference levels: 1.5 V
Output load: 1 TTL gate and $C_L = 100\,pF$

Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	MODE	I/O	I_{CC}
H	X	X	X	Not selected	Hi-Z	Standby
X	L	X	X	Not selected	Hi-Z	Standby
L	H	H	H	D_{OUT} disabled	Hi-Z	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

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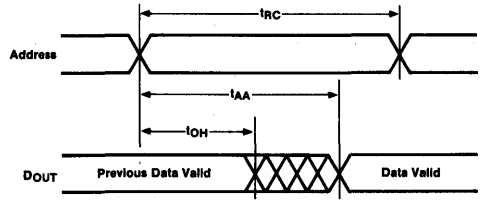
Timing Waveforms

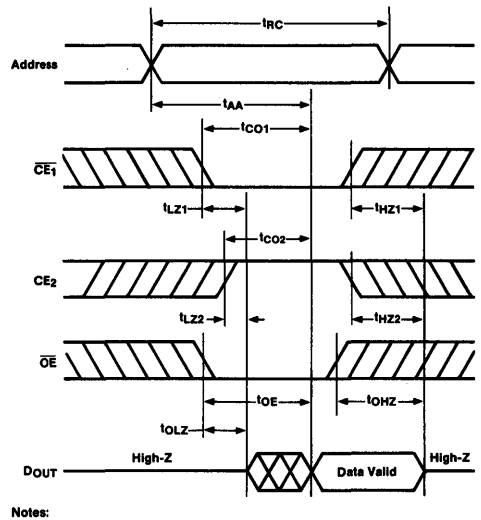
Read Cycle No. 1 (Address Access) (Notes 1, 2)



Notes:
(1) $\overline{WE}$ is high for read cycle.
(2) Device is continuously selected, $\overline{CE_1} = \overline{OE} = V_{IL}$, $CE_2 = V_{IH}$.

83-001755A

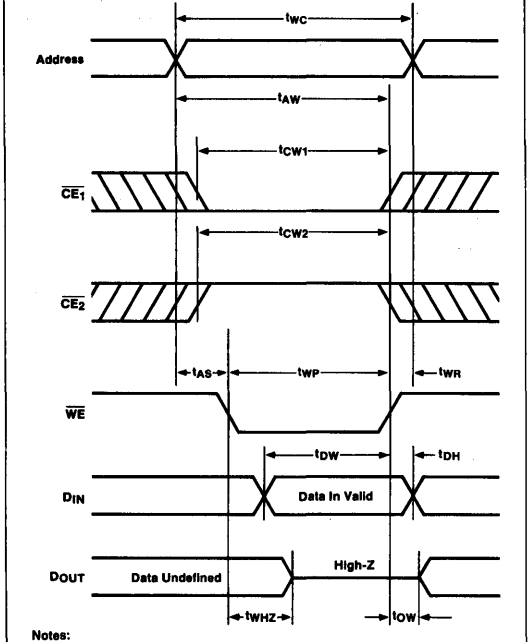
Read Cycle No. 2 (Chip Enable Access) (Notes 1, 2)



Notes:
(1) $\overline{WE}$ is high for read cycle.
(2) Address valid prior to or coincident with $\overline{CE_1}$ transition low, CE_2 transition high.

83-001756A

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Notes 1, 2, 3)

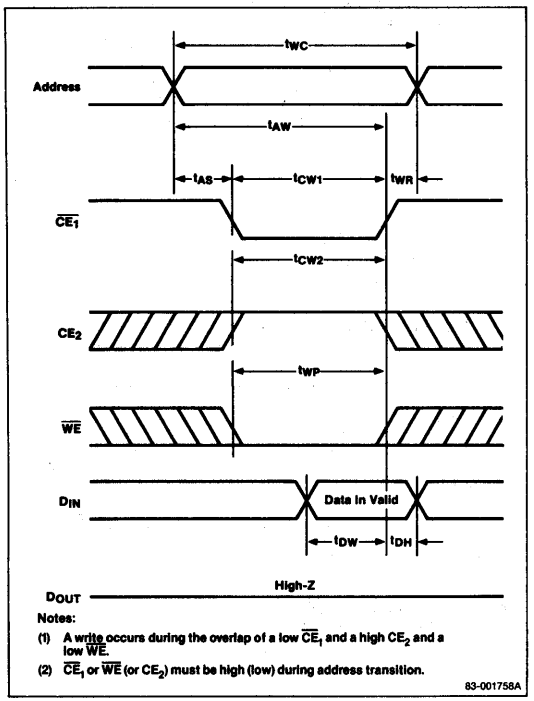


Notes:
(1) A write occurs during the overlap of a low $\overline{CE_1}$ and a high CE_2 and a low $\overline{WE}$.
(2) $\overline{CE_1}$ or $\overline{WE}$ (or CE_2) must be high (low) during address transition.
(3) If $\overline{OE}$ is high, I/O pins remain in a high impedance state.

83-001757A

Timing Waveforms (cont)

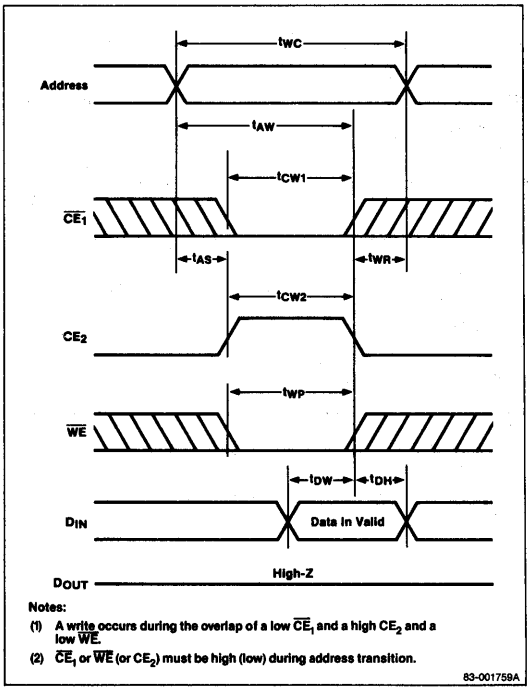
Write Cycle No. 2 ($\overline{CE}_1$ Controlled) (Notes 1, 2)



Notes:
(1) A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
(2) $\overline{CE}_1$ or $\overline{WE}$ (or CE_2) must be high (low) during address transition.

83-001758A

Write Cycle No. 3 (CE_2 Controlled) (Notes 1, 2)



Notes:
(1) A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
(2) $\overline{CE}_1$ or $\overline{WE}$ (or CE_2) must be high (low) during address transition.

83-001759A

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Low V_{CC} Data Retention Characteristics (Note 1)

$T_A = 0°C$ to $70°C$

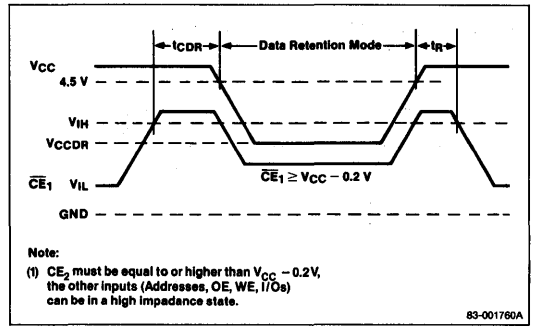
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2.0		5.5	V	$\overline{CE_1} \geq V_{CC} - 0.2$ V $CE_2 \geq V_{CC} - 0.2$ V
Data retention supply voltage	V_{CCDR2}	2.0		5.5	V	$CE_2 \leq 0.2$ V
Data retention supply current	I_{CCDR1}		1	(2)	μA	$V_{CC} = 3.0$ V $\overline{CE_1} \geq V_{CC} - 0.2$ V $CE_2 \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR2}		1	(2)	μA	$V_{CC} = 3.0$ V $CE_2 \leq 0.2$ V
Chip deselect to data retention time	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) For μPD4364-12L/12LL, μPD4364-15L/15LL, μPD4364-20L/20LL only

(2) μPD4364-12L/15L/20L: 50 μA max; 15 μA (0 to 40°C)
μPD4364-12LL/15LL/20LL: 20 μA max; 5 μA (0 to 40°C)

Data Retention ($\overline{CE_1}$ Controlled) (Note 1)

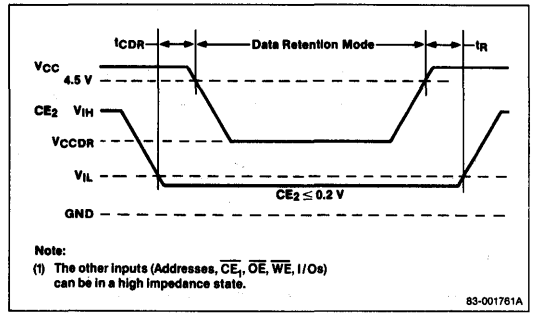


Note:

(1) CE_2 must be equal to or higher than $V_{CC} - 0.2$V, the other inputs (Addresses, OE, WE, I/Os) can be in a high impedance state.

83-001760A

Data Retention (CE_2 Controlled) (Note 1)



Note:

(1) The other inputs (Addresses, $\overline{CE_1}$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

83-001761A

μPD4464
8,192 x 8-BIT STATIC CMOS RAM

Revision 1

Description

The μPD4464 is a high-speed, low-power, 8,192-word by 8-bit static CMOS RAM fabricated with advanced silicon-gate CMOS technology. The μPD4464 is a very low standby power device using full CMOS memory cells with 6 transistors. Furthermore, a unique circuitry technique makes the μPD4464 a very low operating power device which requires no clock or refreshing to operate.

Two chip enable inputs are provided for battery backup application, and an output enable input is included for easy interface. Data retention is guaranteed at a power supply voltage as low as 2 V.

The μPD4464 is packaged in a standard 28-pin DIP and miniflat package and is plug-in compatible with 2764-type EPROMs.

Features

- ☐ Single +5 V power supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL compatible — all inputs and outputs
- ☐ Common I/O using three-state output
- ☐ Output enable and two chip enable inputs for easy application
- ☐ Data retention voltage: 2 V min
- ☐ Standard 28-pin plastic DIP (μPD4464C)
- ☐ 28-pin miniflat (SOP) package (μPD4464G)
- ☐ Plug-in compatible with 2764-type EPROMs
- ☐ Operating temperature range: – 40°C to 85°C

Performance Ranges

Device	Access Time (Max)	Cycle Time (Min)	Power Supply (Max) Active	Standby
μPD4464-15	150 ns	150 ns	40 mA	10 μA [1]
μPD4464-20	200 ns	200 ns	35 mA	10 μA [1]

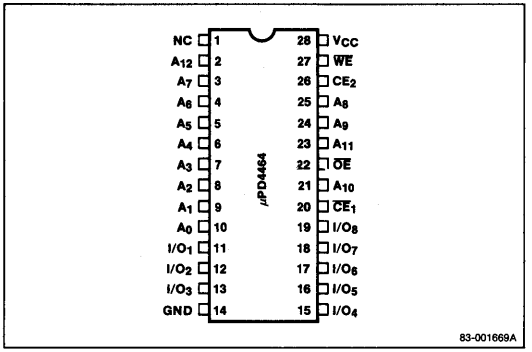
Note: [1] μPD4464-15L/20L: 1.0 μA max (– 40°C to 60°C)
0.2 μA max (– 40°C to 25°C)

Capacitance

$T_A = 25°C$, f = 1.0 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	$V_{IN} = 0$ V
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O} = 0$ V

Pin Configuration



Pin Identification

No	Symbol	Function
1	NC	No connection
2-10, 21, 25-27	A_0-A_{12}	Address input
11-13, 15-19	I/O_1-I/O_8	Data input/output
14	GND	Ground
20	$\overline{CE}_1$	Chip enable active low
22	$\overline{OE}$	Output enable
26	CE_2	Chip enable active high
27	$\overline{WE}$	Write enable
28	V_{CC}	+5 V power supply

Absolute Maximum Ratings

Power supply voltage, V_{CC}	–0.5 V (1) to +7.0 V
Input voltage, V_{IN}	–0.5 V (1) to V_{CC}+ 0.5 V
Output voltage, V_{OUT}	–0.5 V (1) to V_{CC}+ 0.5 V
Operating temperature, T_{OPR}	–40 to 85°C
Storage temperature, T_{STG}	–55 to 125°C
Power dissipation, P_D	1.0 W

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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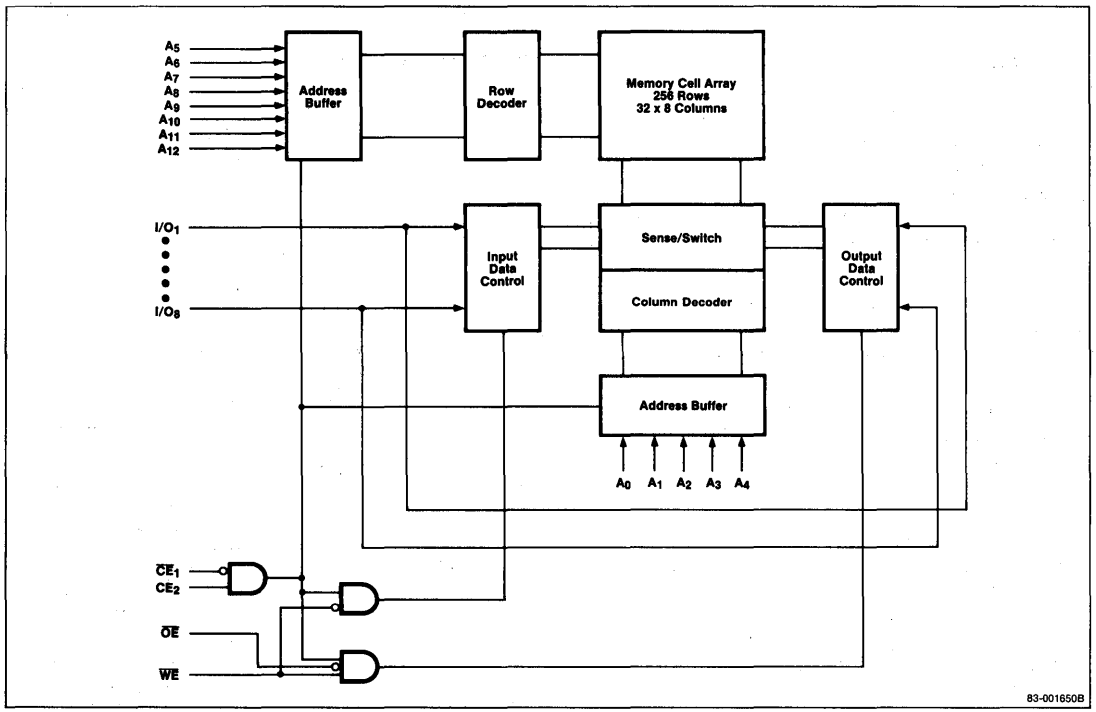
Block Diagram



Recommended DC Operating Conditions

$T_A = -40°C$ to $85°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage low	V_{IL}	−0.3[1]		0.8	V
Input voltage high	V_{IH}	2.2		$V_{CC}+0.5$	V

Note: [1] −3.0 V min (Pulse width 50 ns max)

DC Characteristics

$T_A = -40°C$ to $85°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}			1	μA	$V_{IN} = 0\,V$ to V_{CC}
I/O leakage current	I_{LO}			1	μA	$V_{I/O} = 0\,V$ to V_{CC} $\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}			[1]	mA	$\overline{CE_1} = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$, Min Cycle

DC Characteristics (cont)

$T_A = -40°C$ to $85°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Operating supply current	I_{CCA2}		5	15	mA	$\overline{CE_1} = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$ (DC current)
Standby supply current	I_{CCS1}		0.02	10[2]	μA	$\overline{CE_1} \geq V_{CC} - 0.2\,V$ $CE_2 \geq V_{CC} - 0.2\,V$
Standby supply current	I_{CCS2}		0.02	10[2]	μA	$CE_2 \leq 0.2\,V$
Output voltage low	V_{OL}			0.4	V	$I_{OL} = 2.1\,mA$
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -1.0\,mA$

Notes: [1] μPD4464-15/15L: 40 mA max
μPD4464-20/20L: 35 mA max
[2] μPD4464-15L/20L: 1.0 μA max (−40°C to 60°C)
0.2 μA max (−40°C to 25°C)

AC Characteristics

$T_A = -40°C$ to $85°C$, $V_{CC} = 5\,V \pm 10\%$

Parameter	Symbol	Limits μPD4464 -15 Min	Max	Limits μPD4464 -20 Min	Max	Unit	Test Conditions[1]
Read Cycle							
Read cycle time	t_{RC}	150		200		ns	
Address access time	t_{AA}		150		200	ns	
$\overline{CE}_1$ access time	t_{CO1}		150		200	ns	
CE_2 access time	t_{CO2}		150		200	ns	
Output enable to output valid	t_{OE}		75		100	ns	
Output hold from address change	t_{OH}	10		10		ns	
Chip enable ($\overline{CE}_1$) to output in Low-Z	t_{LZ1}	10		10		ns	
Chip enable (CE_2) to output in Low-Z	t_{LZ2}	10		10		ns	
Output enable to output in Low-Z	t_{OLZ}	5		5		ns	
Chip enable ($\overline{CE}_1$) to output in High-Z	t_{HZ1}		75		100	ns	
Chip enable (CE_2) to output in High-Z	t_{HZ2}		75		100	ns	
Output enable to output in High-Z	t_{OHZ}		60		80	ns	
Write Cycle							
Write cycle time	t_{WC}	150		200		ns	
Chip enable ($\overline{CE}_1$) to end of write	t_{CW1}	130		180		ns	
Chip enable (CE_2) to end of write	t_{CW2}	130		180		ns	
Address valid to end of write	t_{AW}	130		180		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	100		140		ns	
Write recovery time	t_{WR}	5		5		ns	
Data valid to end of write	t_{DW}	70		80		ns	
Data hold time	t_{DH}	5		5		ns	
Write enable to output in High-Z	t_{WHZ}		75		100	ns	
Output active from end of write	t_{OW}	10		10		ns	

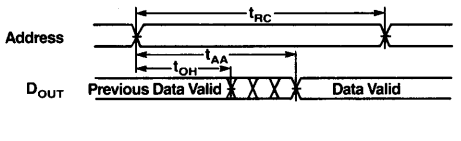
Note: [1] Input pulse levels: 0.8 V to 2.4 V
Input pulse rise and fall times: 5 ns
Timing reference levels: 1.5 V
Output load: 1 TTL gate and $C_L = 100$ pF

Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	MODE	I/O	I_{CC}
H	X	X	X	Not selected	Hi-Z	Standby
X	L	X	X	Not selected	Hi-Z	Standby
L	H	H	H	D_{OUT} disabled	Hi-Z	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

Timing Waveforms

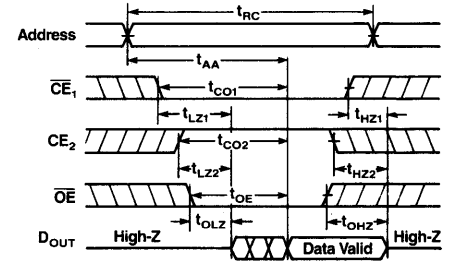
Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{WE}$ is high for read cycle.
[2] Device is continuously selected: $\overline{CE}_1 = \overline{OE} = V_{IL}$, $CE_2 = V_{IH}$.

83-001651A

Read Cycle No. 2 (Chip Enable Access)



Note:
[1] $\overline{WE}$ is high for read cycle.
[2] Address valid prior to or coincident with $\overline{CE}_1$ transition low and CE_2 transition high.

83-001652A

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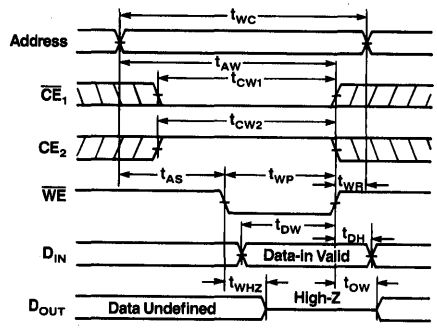
Timing Waveforms (cont)

Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note:

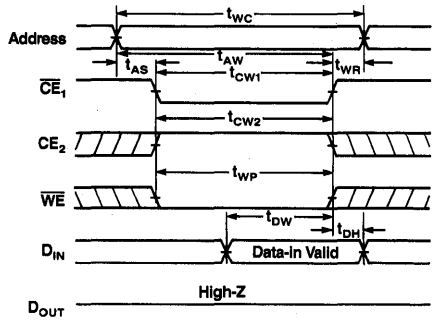
[1] A write occurs during a low $\overline{WE}$ and the overlap of a low $\overline{CE}_1$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.

83-001653A

Write Cycle No. 2 ($\overline{CE}_1$ Controlled)



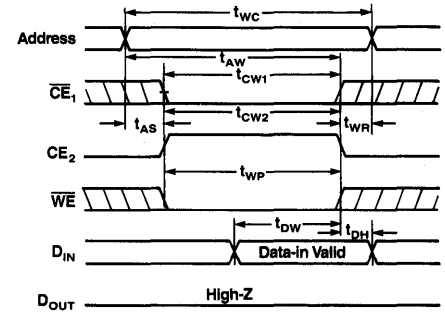
Note:

[1] A write occurs during a low $\overline{WE}$ and the overlap of a low $\overline{CE}_1$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

83-001654A

Write Cycle No. 3 (CE_2 Controlled)



Note:

[1] A write occurs during a low $\overline{WE}$ and the overlap of a low $\overline{CE}_1$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

83-001655A

Low V_{CC} Data Retention Characteristics

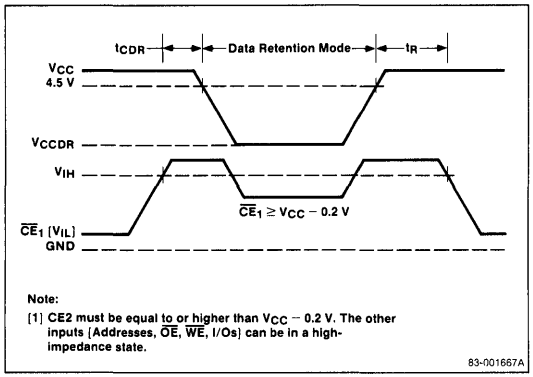
$T_A = -40°C$ to $85°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2.0		5.5	V	$\overline{CE}_1 \geq V_{CC} - 0.2\,V$ $CE_2 \geq V_{CC} - 0.2\,V$
Data retention supply voltage	V_{CCDR2}	2.0		5.5	V	$CE_2 \leq 0.2\,V$
Data retention supply current	I_{CCDR1}		0.01	10[1]	μA	$V_{CC} = 3.0\,V$ $\overline{CE}_1 \geq V_{CC} - 0.2\,V$ $CE_2 \geq V_{CC} - 0.2\,V$
Data retention supply current	I_{CCDR2}		0.01	10[1]	μA	$V_{CC} = 3.0\,V$ $CE_2 \leq 0.2\,V$
Chip deselect to data retention time	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Note: [1] μPD4464-15L/20L: 1.0 μA max (−40°C to 60°C)
0.2 μA max (−40°C to 25°C)

Timing Waveforms (cont)

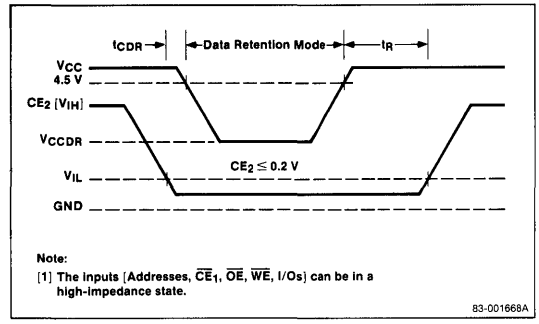
Data Retention ($\overline{CE}_1$ Controlled)



Note:
[1] CE2 must be equal to or higher than V_{CC} − 0.2 V. The other inputs [Addresses, $\overline{OE}$, $\overline{WE}$, I/Os] can be in a high-impedance state.

83-001667A

Data Retention (CE_2 Controlled)



Note:
[1] The inputs [Addresses, $\overline{CE}_1$, $\overline{OE}$, $\overline{WE}$, I/Os] can be in a high-impedance state.

83-001668A

7

μPD43256
32,768 x 8-BIT
STATIC MIX-MOS RAM

Revision 1

Description

The μPD43256 is a high-speed, low-power, 32,768-word by 8-bit static MIX-MOS RAM fabricated with advanced silicon-gate MIX-MOS technology. The μPD43256 is a low standby power device using n-channel memory cells with polysilicon resistors. Furthermore, a novel circuitry technique makes the μPD43256 a high-speed and low operating power device which requires no clock or refreshing to operate.

Minimum standby power is drawn by this device when $\overline{CS}$ is at a high level, independently of the other inputs' levels.

Data retention is guaranteed at a power supply voltage as low as 2 V (μPD43256-10L/12L/15L).

The μPD43256C is packaged in a standard 28-pin plastic dual-in-line package.

The μPD43256G is packaged in a standard 28-pin plastic miniflat (SOP) package.

Features

- ☐ Single +5 V supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL-compatible — all inputs and outputs
- ☐ Common I/O using three-state output
- ☐ One Chip Select and one Output Enable input for easy application
- ☐ Data retention voltage
  - — μPD43256-10L/12L/15L: 2 V min
- ☐ Standard 28-pin plastic DIP and miniflat (SOP) packages

Performance Ranges

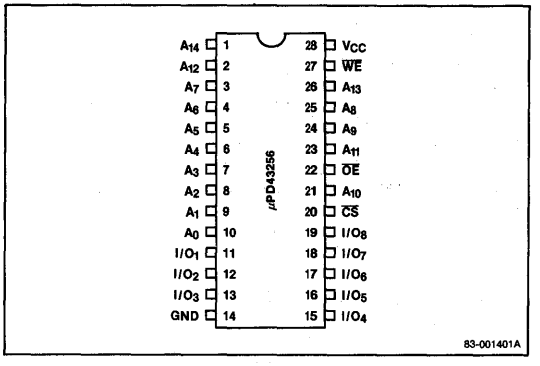
Device	Access Time	Cycle Time	Power Supply (Max) Active	Standby
μPD43256-10	100 ns	100 ns	70 mA	2 mA
μPD43256-12	120 ns	120 ns	70 mA	2 mA
μPD43256-15	150 ns	150 ns	70 mA	2 mA
μPD43256-10L	100 ns	100 ns	70 mA	100 μA
μPD43256-12L	120 ns	120 ns	70 mA	100 μA
μPD43256-15L	150 ns	150 ns	70 mA	100 μA

Capacitance

$T_A = 25°C$, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	$V_{IN} = 0$ V
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O} = 0$ V

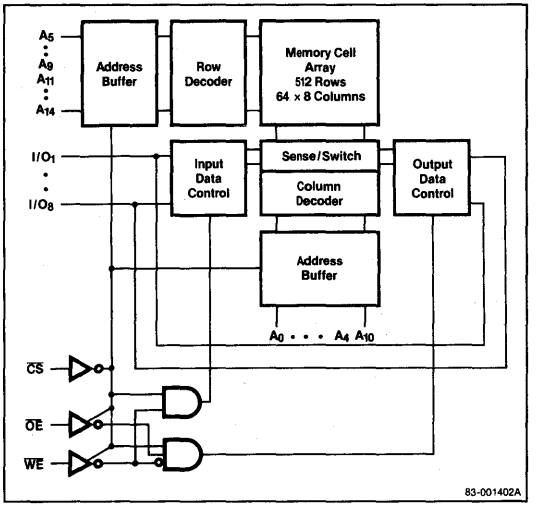
Pin Configuration



Pin Identification Table

No.	Symbol	Function
1-10, 21, 23-26	A_0-A_{14}	Address input
11-13, 15-19	I/O_1-I/O_8	Data input/output
14	GND	Ground
20	$\overline{CS}$	Chip select
22	$\overline{OE}$	Ouput enable
27	$\overline{WE}$	Write enable
28	V_{CC}	Power (+5 V)

Block Diagram



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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5[1] to 7.0 V
Input voltage, V_{IN}	−0.5[1] to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$	−0.5[1] to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to 70°C
Storage temperature, T_{STG}	−55 to 125°C
Power dissipation, P_D	1.0 W

Note: [1] −3.0 V min (pulse width 50 ns)

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

T_A = 0 to 70°C

		Limits			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.3[1]		0.8	V
Input high voltage	V_{IH}	2.2		V_{CC} + 0.5	V

Note: [1] −3.0 V min (pulse width 50 ns)

DC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 10%

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input leakage current	I_{LI}			1	μA	V_{IN} = 0 to V_{CC}
I/O leakage current	I_{LO}			1	μA	$V_{I/O}$ = 0 to V_{CC} $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Operating supply current	I_{CCA}		Note 1	70	mA	$\overline{CS} \leq V_{IL}$, Min Cycle $I_{I/O}$ = 0
Standby supply current	I_{SB}			Note 2	mA	$\overline{CS} \geq V_{IH}$
Standby supply current	I_{SB1}		Note 3	Note 3	mA	$\overline{CS} \geq V_{CC} - 0.2$ V
Output low voltage	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4			V	I_{OH} = −1.0 mA

Notes: [1] μPD43256-10/10L: 35 mA typ
μPD43256-12/12L: 30 mA typ
μPD43256-15/15L: 25 mA typ
[2] μPD43256-10/12/15: 5 mA max
μPD43256-10L/12L/15L: 3 mA max
[3] μPD43256-10/12/15: 20 μA typ, 2 mA max
μPD43256-10L/12L/15L: 2 μA typ, 100 μA max

AC Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 10%

		μPD43256 -10/10L		μPD43256 -12/12L		μPD43256 -15/15L		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read Cycle								
Read cycle time	t_{RC}	100		120		150		ns
Address access time	t_{AA}		100		120		150	ns
Chip select access time	t_{ACS}		100		120		150	ns
Output enable to output valid	t_{OE}		50		60		70	ns
Output hold from address change	t_{OH}	10		10		10		ns
Chip select to output in Lo-Z	t_{CLZ}	10		10		10		ns
Output enable to output in Lo-Z	t_{OLZ}	5		5		5		ns
Chip select to output in Hi-Z	t_{CHZ}		35		40		50	ns
Output enable to output in Hi-Z	t_{OHZ}		35		40		50	ns
Write Cycle								
Write cycle time	t_{WC}	100		120		150		ns
Chip select to end of write	t_{CW}	80		85		100		ns
Address valid to end of write	t_{AW}	80		85		100		ns
Address setup time	t_{AS}	0		0		0		ns
Write pulse width	t_{WP}	70		70		90		ns
Write recovery time	t_{WR}	5		5		5		ns
Data valid to end of write	t_{DW}	40		50		60		ns
Data hold time	t_{DH}	0		0		0		ns
Write enable to output in Hi-Z	t_{WHZ}		35		40		50	ns
Output active from end of write	t_{OW}	10		10		10		ns

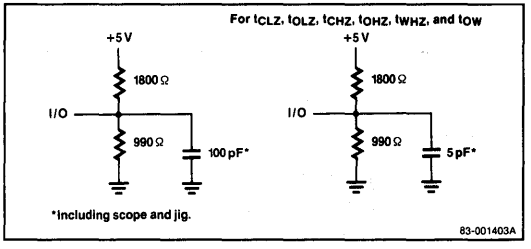
AC Test Conditions

Input pulse levels	0.8 to 2.2 V
Input pulse rise and fall time	5 ns
Timing reference levels	1.5 V

Truth Table

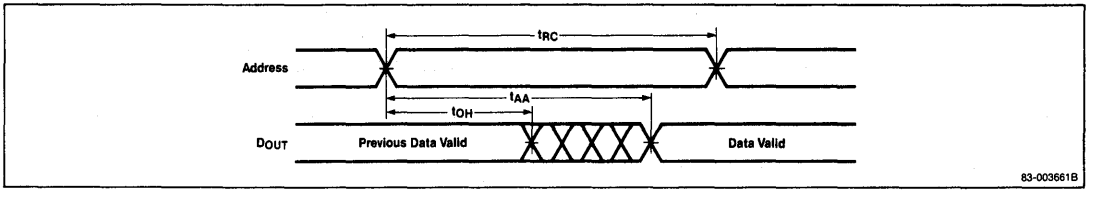
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	I_{CC}
H	X	X	Not selected	Hi-Z	Standby
L	H	H	Not selected	Hi-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

AC Test Circuits

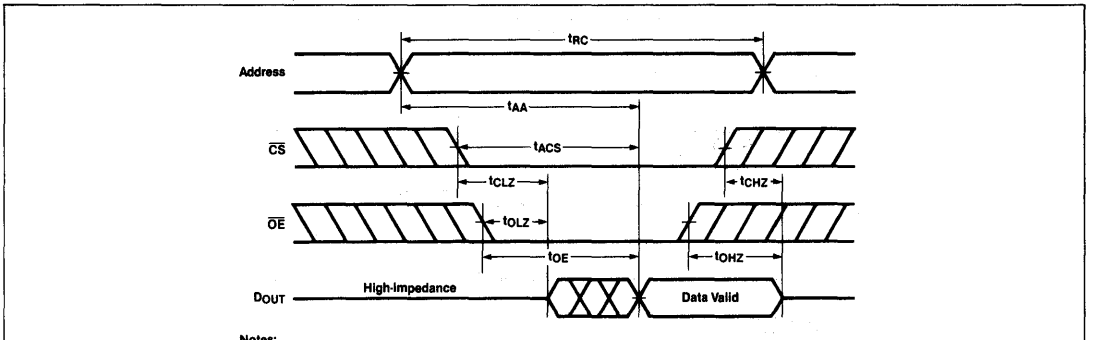


Timing Waveforms

Read Cycle No. 1 (Address Access) (Notes 1, 2)



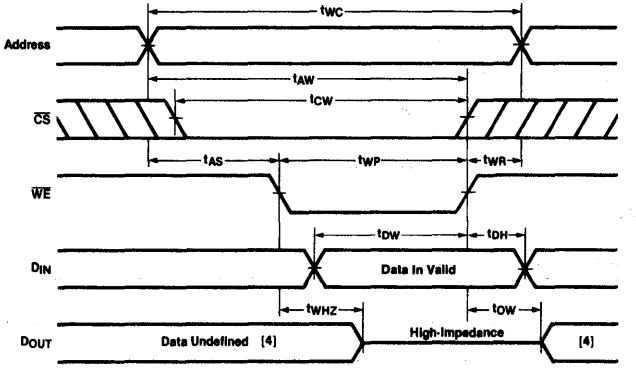
Read Cycle No. 2 (Chip Select Access) (Notes 1, 3)



Notes:
[1] $\overline{WE}$ is high for read cycle.
[2] Device is continuously selected, $\overline{CS} = \overline{OE} = V_{IL}$.
[3] Address valid prior to or coincident with $\overline{CS}$ transition low.

Timing Waveforms (Cont)

Write Cycle No. 1 ($\overline{WE}$ Controlled) (Notes 1, 2, 3)



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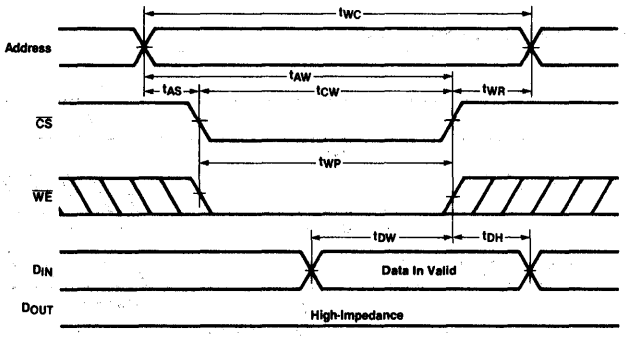
Write Cycle No. 2 ($\overline{CS}$ Controlled) (Notes 1, 2)



Notes:

[1] A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, I/O pins remain in a high-impedance state.

[4] During this period, I/O pins are in the output state, therefore input signals of opposite phase to the outputs must not be applied.

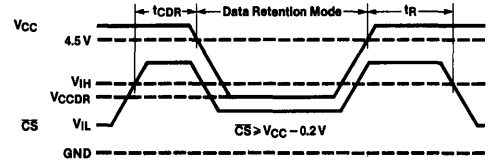
83-001405B

Low V_{CC} Data Retention Characteristics

T_A = 0 to 70°C for μPD43256-10L/12L/15L

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	V_{CC} = 3.0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
Chip deselection to data retention mode	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Data Retention Timing Chart



Note: 1. The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high-impedance state.

83-001406A

7

ECL RAMs

8

Section 8 — ECL RAMs

μPB10422
256 x 4-BIT
10K ECL RAM

Revision 1

Description

The NEC μPB10422 is a very high speed ECL 10K interface RAM. It is organized as 256 words by 4 bits with non-inverted open emitter outputs and low power consumption. Two fast access time versions are available: 7 ns max. (μPB10422-7) and 10 ns max. (μPB10422-10). The μPB10422 is available in a 400 mil 24-pin ceramic DIP.

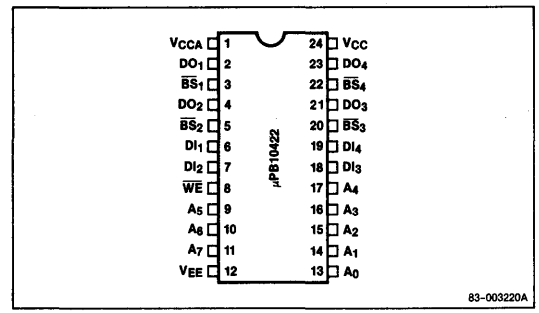
Features

- ☐ 256 word x 4-bit organization
- ☐ ECL 10K interface
- ☐ Non-inverted open emitter output
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in a 24-pin ceramic DIP

Performance Ranges

Device	Package	Access Time (Max)	Supply Current (Min)
μPB10422-7	24-pin ceramic DIP	7 ns	−220 mA
μPB10422-10	24-pin ceramic DIP	10 ns	−220 mA

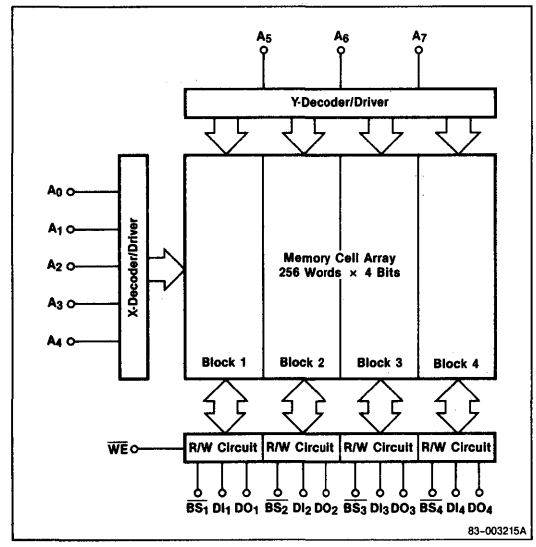
Pin Configuration



Pin Identification

No.	Symbol	Function
1	V_{CCA}	Power supply (output devices)
2, 4, 21, 23	DO_1-DO_4	Data outputs
3, 5, 20, 22	$\overline{BS}_1$-$\overline{BS}_4$	Block select inputs
6, 7, 18, 19	DI_1-DI_4	Data inputs
8	$\overline{WE}$	Write enable
9-11, 13-17	A_0-A_7	Addresses
12	V_{EE}	Power supply
24	V_{CC}	Power supply (current switches and bias driver)

Block Diagram



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Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	+0.5 to −7.0 V
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	+0.1 to −30 mA
Storage temperature, T_{STG}	−65 to +150°C
Under bias, T_{STG} (bias)	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to 75°C, V_{EE} = −5.2 V, output load = 50 Ω to −2 V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000	−840	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 0°C
		−960	−810	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 25°C
		−900	−720	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 75°C
Output voltage, low	V_{OL}	−1870	−1665	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 0°C
		−1850	−1650	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 25°C
		−1830	−1625	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020		mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 0°C
		−980		mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 25°C
		−920		mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 75°C
Output threshold voltage, low	V_{OLC}		−1645	mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 0°C
			−1630	mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 25°C
			−1605	mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 75°C
Input voltage, high	V_{IH}	−1145	−840	mV	For all inputs, T_A = 0°C
		−1105	−810	mV	For all inputs, T_A = 25°C
		−1045	−720	mV	For all inputs, T_A = 75°C
Input voltage, low	V_{IL}	−1870	−1490	mV	For all inputs, T_A = 0°C
		−1850	−1475	mV	For all inputs, T_A = 25°C
		−1830	−1450	mV	For all inputs, T_A = 75°C
Input current, high	I_{IH}		220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5	170	μA	BS_1-BS_4, $V_{IN} = V_{IL}$ min
		−50		μA	All others, $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−220		mA	All inputs and outputs open

Note:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Capacitance

Parameter	Symbol	Limits μPB10422-7 Min	Typ	Max	Limits μPB10422-10 Min	Typ	Max	Unit
Input capacitance	C_{IN}		4			4		pF
Output capacitance	C_{OUT}		5			5		pF

AC Characteristics

$T_A = 0$ to 75 °C, $V_{EE} = -5.2\ V \pm 5\%$

Parameter	Symbol	Limits μPB10422-7 Min	Typ	Max	Limits μPB10422-10 Min	Typ	Max	Unit
Read Mode								
Block select access time	t_{ABS}			5			5	ns
Block select recovery time	t_{RBS}			5			5	ns
Address access time	t_{AA}			7			10	ns
Write Mode								
Write pulse width	t_W	5			6			ns
Data setup time	t_{WSD}	1			2			ns
Data hold time	t_{WHD}	1			2			ns
Address setup time	t_{WSA}	1			2			ns
Address hold time	t_{WHA}	1			2			ns
Block select setup time	t_{WSBS}	1			2			ns
Block select hold time	t_{WHBS}	1			2			ns
Write disable time	t_{WS}			5			5	ns
Write recovery time	t_{WR}			6			9	ns
Output Rise and Fall Times								
Output rise time	t_R		2			2		ns
Output fall time	t_F		2			2		ns

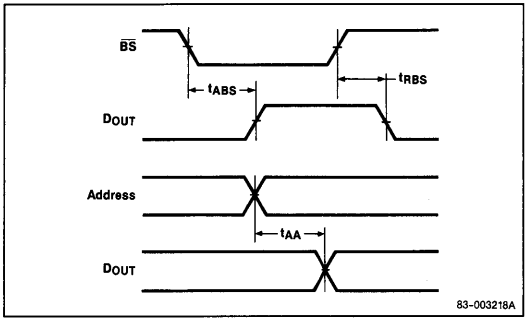
Note:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) All timing measurements are referenced to 50% input levels.

Timing Waveforms

Read Mode



Write Mode

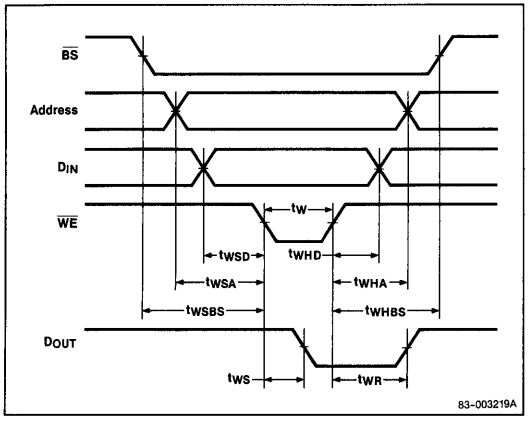


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Figure 1. Loading Conditions Test Circuit

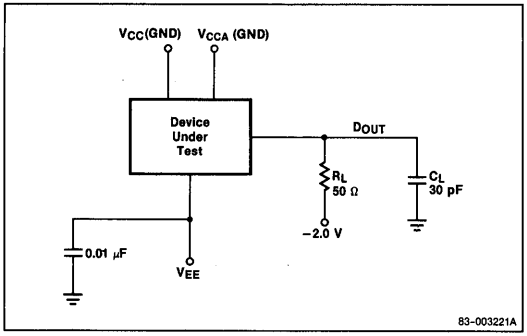
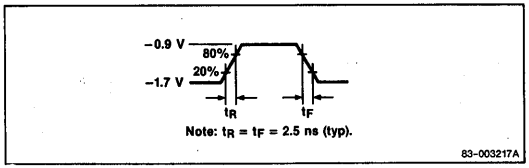


Figure 2. Input Pulse



Description

The NEC μPB10470 is a very high-speed ECL 100K interface Random-access Memory. The device is organized as 4K words by 1 bit, with an open emitter output (noninverted), and low power consumption. Two fast access time versions are available: 10ns max (μPB10470-10) and 15ns max (μPB10470-15).

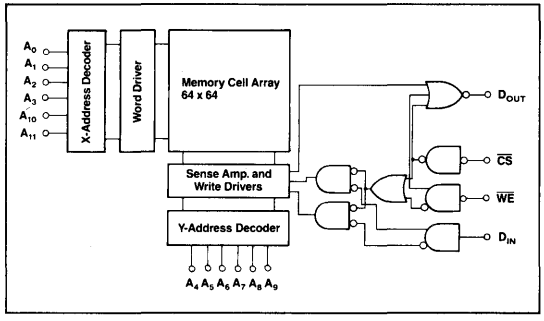
The μPB100470 is available in a hermetic, 300mil, 18-lead DIP.

Features

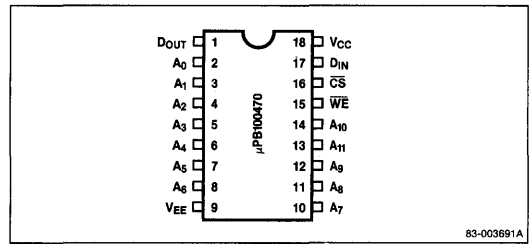
- ☐ 4K-word x 1-bit organization
- ☐ ECL 100K interface
- ☐ Open emitter output (noninverted)
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in 18-lead, 300mil, DIP and LCC
- ☐ 2 performance ranges:

Device	Package	Access Time	Power Consumption
μPB10470-10	DIP	10ns max	1.2W max
μPB10470-15	DIP	15ns max	1.2W max

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	D_{OUT}	Data Output
2–8, 10–14	A_0–A_{11}	Addresses
9	V_{EE}	Power Supply
15	$\overline{WE}$	Write Enable
16	$\overline{CS}$	Chip Enable
17	D_{IN}	Data Input
18	V_{CC}	Power Supply

Absolute Maximum Ratings*

Supply Voltage, V_{EE} to V_{CC}	+0.5V to −7.0V
Input Voltage, V_{IN}	+0.5V to V_{EE}
Output Current, I_{OUT}	+0.1mA to −30mA
Storage Temperature, T_{STG}	−65°C to +150°C
Under Bias, T_{STG} (Bias)	−55°C to +125°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

Parameter	Symbol	Limits 10470-10 Min	Typ	Max	Limits 10470-15 Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}		4			4		pF	
Output Capacitance	C_{OUT}		5			5		pF	

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DC Characteristics ①

T_A = 0°C to +75°C; V_{EE} = −5.2V; Output Load = 50Ω to −2V

Parameter	Symbol	T_A(°C)	Limits Min	Typ	Max	Unit	Test Conditions
Output Voltage	V_{OH}	0	−1000		−840	mV	V_{IN} = V_{IHA} or V_{ILB}
		+25	−960		−810		
		+75	−900		−720		
	V_{OL}	0	−1870		−1665		
		+25	−1850		−1650		
		+75	−1830		−1625		
Output Threshold Voltage	V_{OHC}	0	−1020			mV	V_{IN} = V_{IHB} or V_{ILA}
		+25	−980				
		+75	−920				
	V_{OLC}	0			−1645		
		+25			−1630		
		+75			−1605		
Input Voltage	V_{IH}	0	−1145		−840	mV	Guaranteed input voltage high for all inputs.
		+25	−1105		−810		
		+75	−1045		−720		
	V_{IL}	0	−1870		−1490		Guaranteed input voltage low for all inputs.
		+25	−1850		−1475		
		+75	−1830		−1450		
Input Current	I_{IH}	0 to +75			220	μA	V_{IN} = V_{IHA}
	I_{IL}	0 to +75		0.5	170		$\overline{CS}$
		0 to +75	−50				Others — V_{IN} = V_{ILB}
Supply Current	I_{EE}	0 to +75	−220			mA	All inputs and outputs are open.

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics ①

T_A = 0°C to +75°C; V_{EE} = −5.2V ± 5%

Read Mode

Parameter	Symbol	Limits 10470-10 Min	Typ	Max	10470-15 Min	Typ	Max	Unit	Test Conditions
Chip Select Access Time	t_{ACS}			6			8	ns	
Chip Select Recovery Time	t_{RCS}			6			8	ns	
Address Access Time	t_{AA}			10			15	ns	

Write Mode

Parameter	Symbol	Limits 10470-10 Min	Typ	Max	10470-15 Min	Typ	Max	Unit	Test Conditions
Write Pulse Width	t_W	10			15			ns	
Data Set-up Time	t_{WSD}	2			2			ns	
Data Hold Time	t_{WHD}	2			2			ns	
Address Set-up Time	t_{WSA}	3			3			ns	
Address Hold Time	t_{WHA}	2			2			ns	
Chip Select Set-up Time	t_{WSCS}	2			2			ns	
Chip Select Hold Time	t_{WHCS}	2			2			ns	
Write Disable Time	t_{WS}			6			8	ns	
Write Recovery Time	t_{WR}			10			10	ns	

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics (Cont.) ①

T_A = 0°C to +75°C; V_{EE} = −5.2V ± 5%

Output Rise and Fall Times

Parameter	Symbol	Limits 10470-10 Min	Typ	Max	10470-15 Min	Typ	Max	Unit	Test Conditions
Rise Time	t_R		2			2		ns	
Fall Time	t_F		2			2		ns	

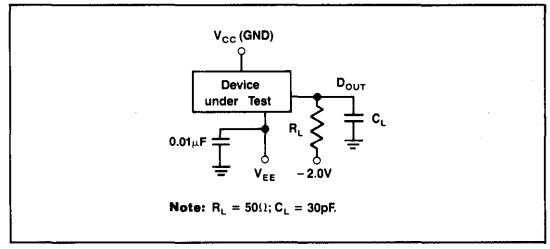
Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

Truth Table

Input $\overline{CS}$	Input $\overline{WE}$	Input D_{IN}	Output	Mode
H	X	X	L	Not Selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

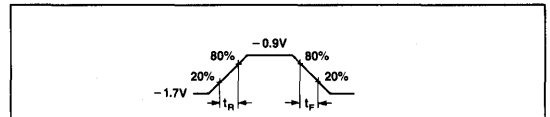
Note: X = Don't care.

Figure 1. Loading Conditions Test Circuit



Note: R_L = 50Ω; C_L = 30pF.

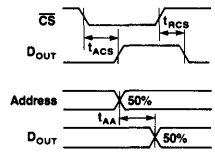
Figure 2. Input Pulse Test Circuit



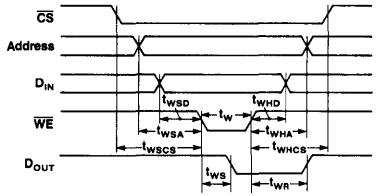
Note: t_R = t_F = 2.5ns (typ).

Timing Waveforms

Read Mode



Write Mode



8

μPB10474
1,024 x 4-BIT
10K ECL RAM

Revision 1

Description

The NEC μPB10474 is a very high speed ECL 10k interface random access memory (RAM). It is organized as 1,024 words by 4 bits with non-inverted open emitter outputs and low power consumption. Three access time versions are available: 8 ns max. (μPB10474-8), 10 ns max. (μPB10474-10), and 15 ns max. (μPB10474-15). The μPB10474 is available in a hermetic, 400 mil, 24-pin DIP.

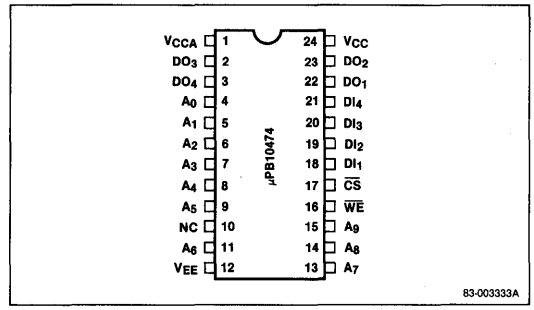
Features

- ☐ 1,024 word x 4-bit organization
- ☐ ECL 10k interface
- ☐ Non-inverted open emitter outputs
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in a 24-pin 400 mil DIP (μPB10474D)

Performance Ranges

Device	Package	Access Time (Max)	Supply Current (Min)
μPB10474-8	24-pin DIP	8 ns	−220 mA
μPB10474-10	24-pin DIP	10 ns	−220 mA
μPB10474-15	24-pin DIP	15 ns	−220 mA

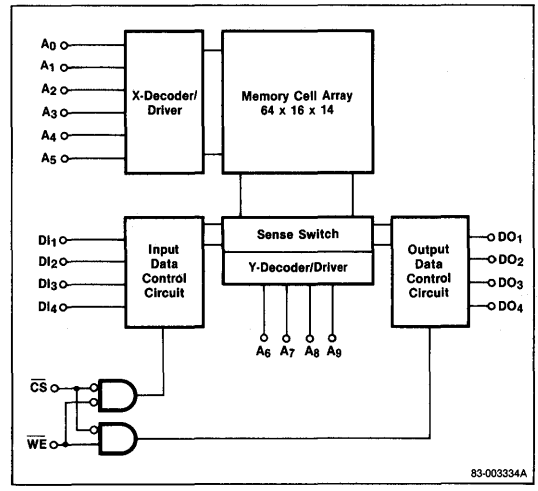
Pin Configuration



Pin Identification

No.	Symbol	Function
1	V_{CCA}	Power supply (output devices)
2, 3, 22, 23	DO_1-DO_4	Data outputs
4-9, 11, 13-15	A_0-A_9	Addresses
10	NC	No connection
12	V_{EE}	Power supply
16	$\overline{WE}$	Write enable
17	$\overline{CS}$	Chip select
18-21	DI_1-DI_4	Data inputs
24	V_{CC}	Power supply (current switches and bias driver)

Block Diagram



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Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	+0.5 to −7.0 V
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	+0.1 to −30 mA
Storage temperature, T_{STG}	−65 to +150°C
Under bias, $T_{STG(bias)}$	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}		4		pF	f = 1 MHz
Output capacitance	C_{OUT}		5		pF	f = 1 MHz

DC Characteristics

T_A = 0 to 75°C, V_{EE} = −5.2 V, output load = 50 Ω to −2 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 0°C
	V_{OH}	−960		−810	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 25°C
	V_{OH}	−900		−720	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 0°C
	V_{OL}	−1850		−1650	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 25°C
	V_{OL}	−1830		−1625	mV	$V_{IN} = V_{IH}$ max or V_{IL} min, T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 0°C
	V_{OHC}	−980			mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 25°C
	V_{OHC}	−920			mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 0°C
	V_{OLC}			−1630	mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 25°C
	V_{OLC}			−1605	mV	$V_{IN} = V_{IH}$ min or V_{IL} max, T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs, T_A = 0°C
	V_{IH}	−1105		−810	mV	For all inputs, T_A = 25°C
	V_{IH}	−1045		−720	mV	For all inputs, T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs, T_A = 0°C
	V_{IL}	−1850		−1475	mV	For all inputs, T_A = 25°C
	V_{IL}	−1830		−1450	mV	For all inputs, T_A = 75°C
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$; $V_{IN} = V_{IL}$ min
	I_{IL}	−50			μA	For all others; $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Note:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to 75°C, V_{EE} = −5.2 V ± 5%, output load = 50 Ω to −2 V

		Limits									
		μPB10474-8			μPB10474-10			μPB10474-15			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Read Mode											
Chip select access time	t_{ACS}			5			6			8	ns
Chip select recovery time	t_{RCS}			5			6			8	ns
Address access time	t_{AA}			8			10			15	ns
Write Mode											
Write pulse width	t_W	6			10			15			ns
Data setup time	t_{WSD}	1			2			2			ns
Data hold time	t_{WHD}	1			2			2			ns
Address setup time	t_{WSA}	1			3			3			ns
Address hold time	t_{WHA}	1			2			2			ns
Chip select setup time	t_{WSCS}	1			2			2			ns
Chip select hold time	t_{WHCS}	1			2			2			ns
Write disable time	t_{WS}			5			6			8	ns
Write recovery time	t_{WR}			8			10			10	ns
Output Rise and Fall Times											
Output rise time	t_R		2			2			2		ns
Output fall time	t_F		2			2			2		ns

Note:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Figure 1. Loading Conditions Test Circuit

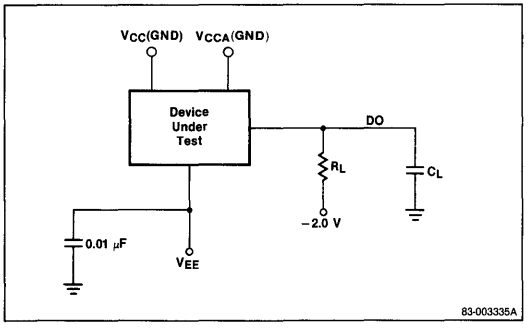
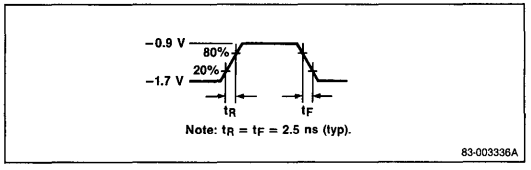


Figure 2. Input Pulse



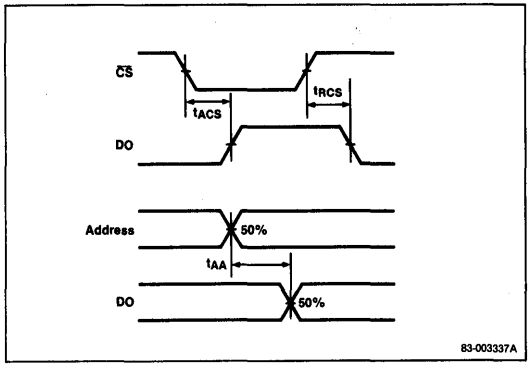
Truth Table

Input				
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not Selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

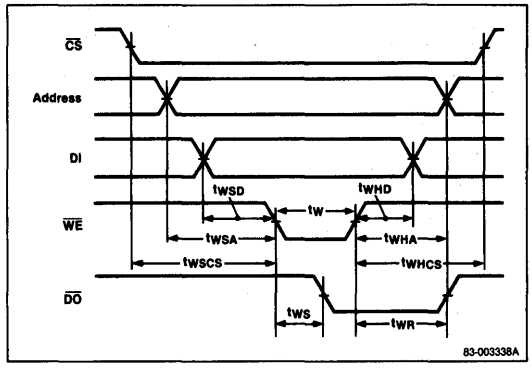
8

Timing Waveforms

Read Mode



Write Mode



μPB100422
256 x 4-BIT 100K ECL RAM

Revision 1

Description

The NEC μPB100422 is a very high speed ECL 100k interface RAM. It is organized as 256 words by 4 bits with a non-inverted open emitter output and low power consumption. Two fast access time versions are available: 7 ns max. (μPB100422-7) and 10 ns max. (μPB100422-10). The μPB100422 is available in a 400 mil 24-pin ceramic DIP or a 24-pin ceramic flatpack.

Features

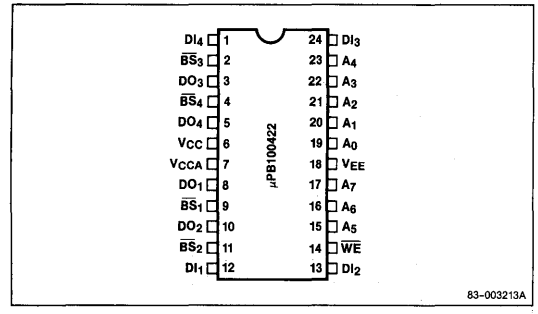
- ☐ 256 word x 4-bit organization
- ☐ ECL 100k interface
- ☐ Non-inverted open emitter output
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in a 24-pin 400 mil DIP or a 24-pin flatpack

Performance Ranges

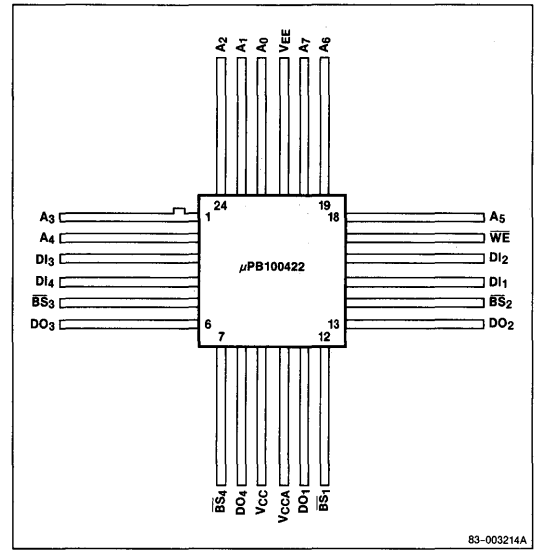
Device	Package	Access Time (Max)	Supply Current (Min)
μPB100422D-7	24-pin DIP	7 ns	−220 mA
μPB100422B-7	24-pin flat	7 ns	−220 mA
μPB100422D-10	24-pin DIP	10 ns	−220 mA
μPB100422B-10	24-pin flat	10 ns	−220 mA

Pin Configurations

24-Pin DIP



24-Pin Flatpack



8

Pin Identification

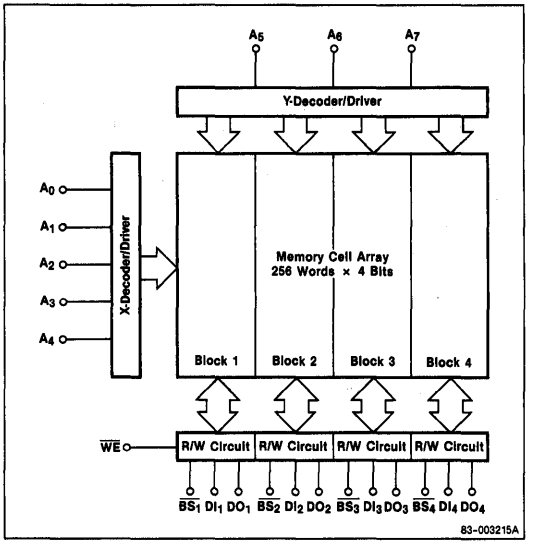
Ceramic DIP

No.	Symbol	Function
1, 12, 13, 24	DI_1-DI_4	Data inputs
2, 4, 9, 11	$\overline{BS}_1$-$\overline{BS}_4$	Block select inputs
3, 5, 8, 10	DO_1-DO_4	Data outputs
6	V_{CC}	Power supply (current switches and bias driver)
7	V_{CCA}	Power supply (output devices)
14	$\overline{WE}$	Write enable
15-17, 19-23	A_0-A_7	Addresses
18	V_{EE}	Power supply

Ceramic Flatpack

No.	Symbol	Function
1, 2, 18-20, 22-24	A_0-A_7	Addresses
3, 4, 15, 16	DI_1-DI_4	Data inputs
5, 7, 12, 14	$\overline{BS}_1$-$\overline{BS}_4$	Block select inputs
6, 8, 11, 13	DO_1-DO_4	Data outputs
9	V_{CC}	Power supply (current switches and bias driver)
10	V_{CCA}	Power supply (output devices)
17	$\overline{WE}$	Write enable
21	V_{EE}	Power supply

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	+0.5 to −7.0 V
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	+0.1 to −30 mA
Storage temperature, T_{STG}	−65 to +150°C
Under bias, $T_{STG(bias)}$	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

		Limits						
		μPB100422-7			μPB100422-10			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4			4		pF
Output capacitance	C_{OUT}		5			5		pF

DC Characteristics

T_A = 0 to 85°C, V_{EE} = −4.5 V, output load = 50 Ω to −2 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	For all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	For all inputs
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5		170	μA	$\overline{BS_1}$-$\overline{BS_4}$, $V_{IN} = V_{IL}$ min
	I_{IL}	−50			μA	All others, $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Note:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to 85°C, V_{EE} = −4.5 V ± 5%

Parameter	Symbol	Limits μPB100422-7 Min	Typ	Max	μPB100422-10 Min	Typ	Max	Unit
Read Mode								
Block select access time	t_{ABS}			5			5	ns
Block select recovery time	t_{RBS}			5			5	ns
Address access time	t_{AA}			7			10	ns
Write Mode								
Write pulse width	t_W	5			6			ns
Data setup time	t_{WSD}	1			2			ns
Data hold time	t_{WHD}	1			2			ns
Address setup time	t_{WSA}	1			2			ns
Address hold time	t_{WHA}	1			2			ns
Block select setup time	t_{WSBS}	1			2			ns
Block select hold time	t_{WHBS}	1			2			ns
Write disable time	t_{WS}			5			5	ns
Write recovery time	t_{WR}			6			9	ns

Parameter	Symbol	Limits μPB100422-7 Min	Typ	Max	μPB100422-10 Min	Typ	Max	Unit
Output Rise and Fall Times								
Output rise time	t_R		2			2		ns
Output fall time	t_F		2			2		ns

Note:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) All timing measurements are referenced to 50% input levels.

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Figure 1. Loading Conditions Test Circuit

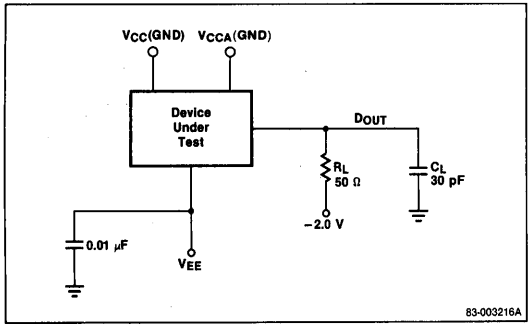
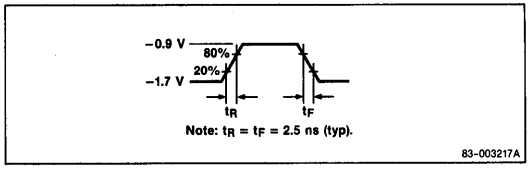
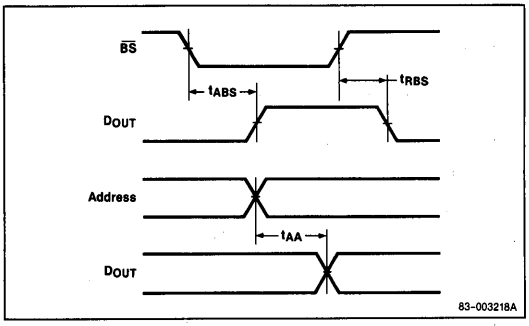


Figure 2. Input Pulse

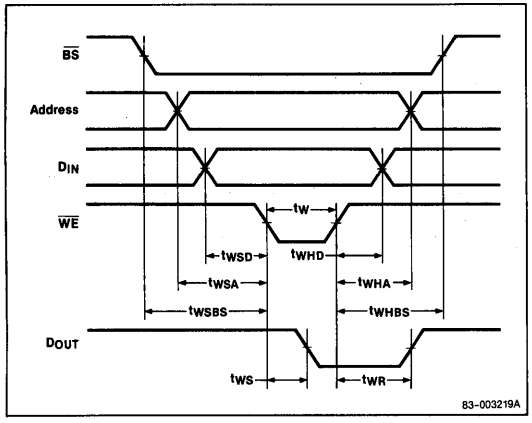


Timing Waveforms

Read Mode



Write Mode



Description

The NEC μPB100470 is a very high-speed ECL 100 K interface Random-access Memory with full voltage and temperature compensation. The device is organized as 4 K words by 1 bit, with an open emitter output (noninverted), and low power consumption. Two fast access time versions are available: 10 ns max (μPB100470-10) and 15 ns max (μPB100470-15).

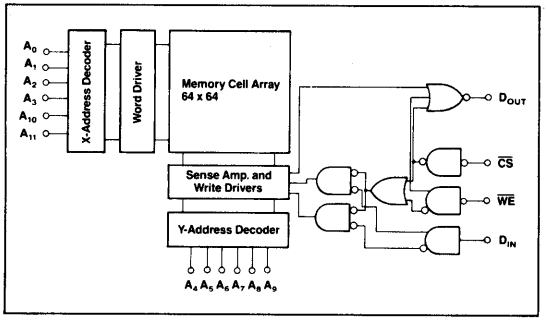
The μPB100470 is available in a hermetic, 300 mil, 18-lead DIP.

Features

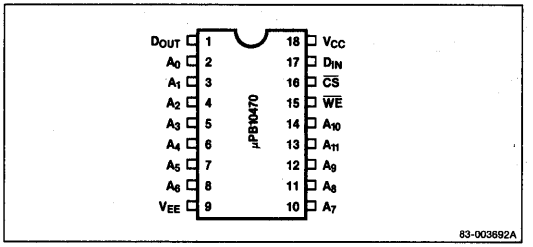
- ☐ 4K-word × 1-bit organization
- ☐ ECL 100K interface with full voltage and temperature compensation
- ☐ Open emitter output (noninverted)
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in 18-lead, 300 mil, DIP and LCC
- ☐ 4 performance ranges:

Device	Package	Access Time	Power Consumption
μPB100470-10	DIP	10ns max	1W max
μPB100470-15	DIP	15ns max	1W max

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	D_{OUT}	Data Output
2–8, 10–14	A_0–A_{11}	Addresses
9	V_{EE}	Power Supply
15	$\overline{WE}$	Write Enable
16	$\overline{CS}$	Chip Select
17	D_{IN}	Data Input
18	V_{CC}	Power Supply

Absolute Maximum Ratings*

Supply Voltage, V_{EE} to V_{CC}	+0.5V to −7.0V
Input Voltage, V_{IN}	+0.5V to V_{EE}
Output Current, I_{OUT}	+0.1mA to −30mA
Storage Temperature, T_{STG}	−65°C to +150°C
Under Bias, T_{STG} (Bias)	−55°C to +125°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

Parameter	Symbol	Limits 100470-10 Min	Typ	Max	100470-15 Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}		4			4		pF	
Output Capacitance	C_{OUT}		5			5		pF	

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DC Characteristics ①

T_A = 0°C to +85°C; V_{EE} = −4.5V; Output Load = 50Ω to −2V

Parameter	Symbol	T_A(°C)	Limits Min	Typ	Max	Unit	Test Conditions
Output Voltage	V_{OH}	0 to +85	−1025		−880	mV	$V_{IN} = V_{IHA}$ or V_{ILB}
	V_{OL}	0 to +85	−1810		−1620		
Output Threshold Voltage	V_{OHC}	0 to +85	−1035			mV	$V_{IN} = V_{IHB}$ or V_{ILA}
	V_{OLC}	0 to +85			−1610		
Input Voltage	V_{IH}	0 to +85	−1165		−880	mV	Guaranteed input voltage high for all inputs.
	V_{IL}	0 to +85	−1810		−1475		Guaranteed input voltage low for all inputs.
Input Current	I_{IH}	0 to +85			220	μA	$V_{IN} = V_{IHA}$
	I_{IL}	0 to +85	0.5		170		$\overline{CS}$
			−50				Others $V_{IN} = V_{ILB}$
Supply Current	I_{EE}	0 to +85	−220			mA	All inputs and outputs are open.

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics ①

T_A = 0°C to +85°C; V_{EE} = −4.5V ± 5%

Read Mode

Parameter	Symbol	Limits 100470-10 Min	Typ	Max	100470-15 Min	Typ	Max	Unit	Test Conditions
Chip Select Access Time	t_{ACS}			6			8	ns	
Chip Select Recovery Time	t_{RCS}			6			8	ns	
Address Access Time	t_{AA}			10			15	ns	

Write Mode

Parameter	Symbol	Limits 100470-10 Min	Typ	Max	100470-15 Min	Typ	Max	Unit	Test Conditions
Write Pulse Width	t_W	10			15			ns	
Data Set-up Time	t_{WSD}	2			2			ns	
Data Hold Time	t_{WHD}	2			2			ns	
Address Set-up Time	t_{WSA}	3			3			ns	
Address Hold Time	t_{WHA}	2			2			ns	
Chip Select Set-up Time	t_{WSCS}	2			2			ns	
Chip Select Hold Time	t_{WHCS}	2			2			ns	
Write Disable Time	t_{WS}			6			8	ns	
Write Recovery Time	t_{WR}			10			10	ns	

Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

AC Characteristics (Cont.) ①

T_A = 0°C to +85°C; V_{EE} = −4.5V ± 5%

Output Rise and Fall Times

Parameter	Symbol	Limits 100470-10 Min	Typ	Max	100470-15 Min	Typ	Max	Unit	Test Conditions
Rise Time	t_R		2			2		ns	
Fall Time	t_F		2			2		ns	

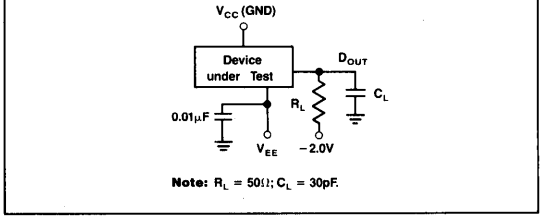
Note: ① The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow greater than 2.0m/sec maintained.

Truth Table

Input $\overline{CS}$	Input $\overline{WE}$	Input D_{IN}	Output	Mode
H	X	X	L	Not Selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

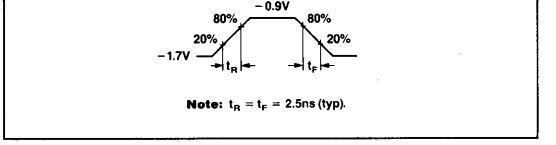
Note: X = Don't care.

Figure 1. Loading Conditions Test Circuit



Note: R_L = 50Ω; C_L = 30pF.

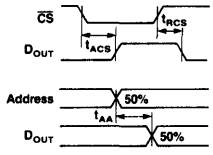
Figure 2. Input Pulse Test Circuit

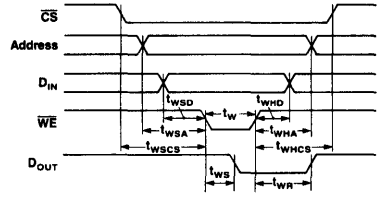


Note: $t_R = t_F$ = 2.5ns (typ).

Timing Waveforms

Read Mode





8

μPB100474
1,024 x 4-BIT
100K ECL RAM

Revision 1

Description

NEC's μPB100474 is a very high-speed ECL 100K interface random access memory. The μPB100474 is organized as 1K words by 4 bits with open emitter outputs (non-inverted). It is available in a hermetic DIP (μPB100474D), leadless chip carrier (LCC) (μPB100474K), or ceramic flatpack package (μPB100474B) version.

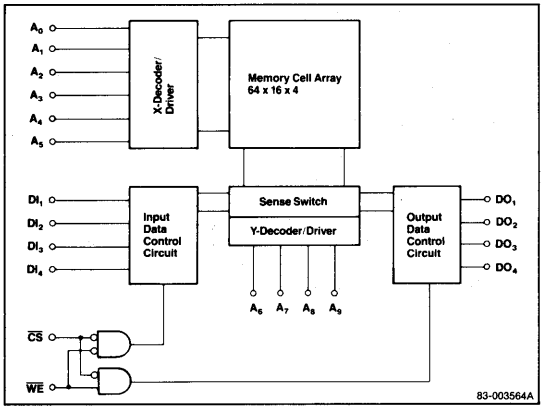
Features

- ☐ 1K-word bx 4-bit organization
- ☐ ECL 100K interface
- ☐ Full voltage and temperature compensation
- ☐ Open emitter outputs (non-inverted)
- ☐ Fast access times
- ☐ Available in DIP, LCC, and flatpack versions

Performance Ranges

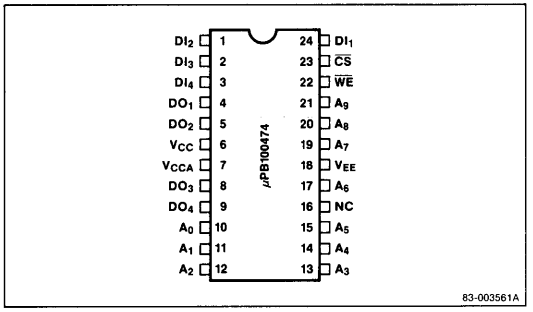
Device	Packages	Access Time (Max)	Supply Current (Min)
μPB100474-4.5	K	4.5 ns	−450 mA
μPB100474-6	B/K	6 ns	−450 mA
μPB100474-8	B/D	8 ns	−220 mA
μPB100474-10	B/D	10 ns	−220 mA
μPB100474-15	B/D	15 ns	−220 mA

Block Diagram

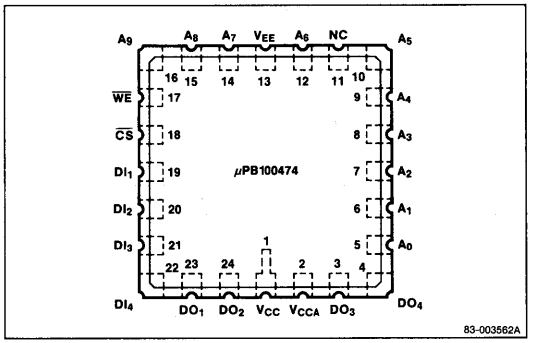


Pin Configurations

24-Pin Ceramic DIP



24-Pin Ceramic LCC



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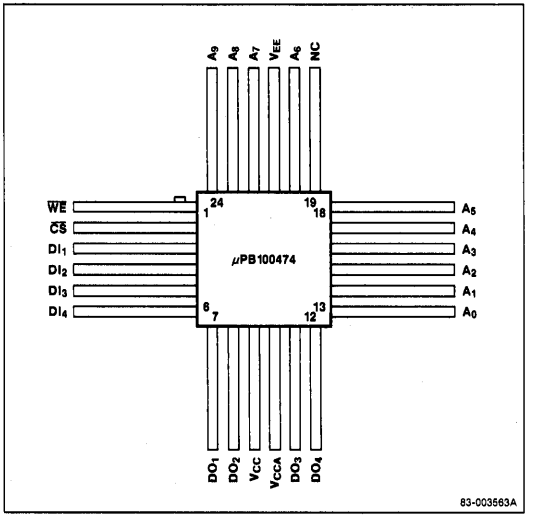
Pin Configurations (cont)

24-Pin Ceramic Flatpack



Pin Identification

Ceramic DIP

No.	Symbol	Function
1-3, 24	DI_1-DI_4	Data inputs
4, 5, 8, 9	DO_1-DO_4	Data outputs
6	V_{CC}	Power supply (current switches and bias driver)
7	V_{CCA}	Power supply (output devices)
10-15, 17, 19-21	A_0-A_9	Addresses
16	NC	No connection
18	V_{EE}	Power supply
22	$\overline{WE}$	Write enable
23	$\overline{CS}$	Chip select

Pin Identification (cont)

Ceramic LCC

No.	Symbol	Function
1	V_{CC}	Power supply (current switches and bias driver)
2	V_{CCA}	Power supply (output devices)
3, 4, 23, 24	DO_1-DO_4	Data outputs
5-10, 12, 14-16	A_0-A_9	Addresses
11	NC	No connection
13	V_{EE}	Power supply
17	$\overline{WE}$	Write enable
18	$\overline{CS}$	Chip select
19-22	DI_1-DI_4	Data inputs

Ceramic Flatpack

No.	Symbol	Function
1	$\overline{WE}$	Write enable
2	$\overline{CS}$	Chip select
3-6	DI_1-DI_4	Data inputs
7, 8, 11, 12	DO_1-DO_4	Data outputs
9	V_{CC}	Power supply (current switches and bias driver)
10	V_{CCA}	Power supply (output devices)
13-18, 20, 22-24	A_0-A_9	Addresses
19	NC	No connection
21	V_{EE}	Power supply

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	+0.5 to −7.0 V
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	+0.1 to −30 mA
Storage temperature, T_{STG}	−65 to +150°C
Under bias, T_{STG} (Bias)	−55 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; Output load = 50 Ω to −2 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage high	V_{OH}	−1025		−880	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output voltage low	V_{OL}	−1810		−1620	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output threshold voltage high	V_{OHC}	−1035			mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Output threshold voltage low	V_{OLC}			−1610	mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Input voltage high	V_{IH}	−1165		−880	mV	Guaranteed input voltage high for all inputs
Input voltage low	V_{IL}	−1810		−1475	mV	Guaranteed input voltage low for all inputs
Input current high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ max
Input current low	I_{IL}	0.5		170	μA	$\overline{CS}$, $V_{IN} = V_{IL}$ min
		−50			μA	Others, $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−450	−360		mA	t_{AA} = 4.5/6 ns, all inputs and outputs open (Note 2)
		−220	−160		mA	t_{AA} = 8/10/15 ns, all inputs and outputs open (Note 2)

Note:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

(2) For the μPB100474-4.5/6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90°C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10°C/W.

Truth Table

Input CS	WE	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Note:

X = Don't care.

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}		4		pF	
Output capacitance	C_{OUT}		5		pF	

Figure 1. Loading Conditions Test Circuit

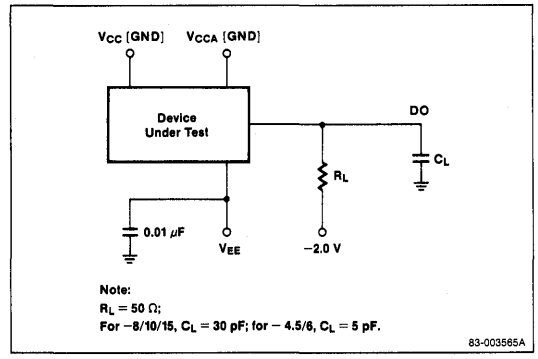
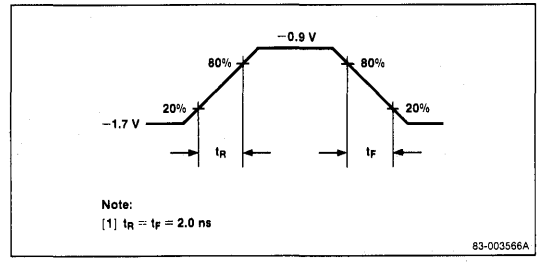


Figure 2. Input Pulse



8

AC Characteristics

T_A = 0 to +85 °C; V_{EE} = −4.5 V ±5%; Output load = 50 Ω to −2 V

		Limits															
		μPB100474-4.5			μPB100474-6			μPB100474-8			μPB100474-10			μPB100474-15			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Read Mode																	
Chip select access time	t_{ACS}			4			4			5			6			8	ns
Chip select recovery time	t_{RCS}			4			4			5			6			8	ns
Address access time	t_{AA}			4.5			6			8			10			15	ns
Write Mode																	
Write pulse width	t_W	4.5			6			6			10			15			ns
Data setup time	t_{WSD}	1			1			1			2			2			ns
Data hold time	t_{WHD}	1			1			1			2			2			ns
Address setup time	t_{WSA}	1			1			1			3			3			ns
Address hold time	t_{WHA}	2			2			1			2			2			ns
Chip select setup time	t_{WSCS}	1			1			1			2			2			ns
Chip select hold time	t_{WHCS}	1			1			1			2			2			ns
Write disable time	t_{WS}			4			4			5			6			8	ns
Write recovery time	t_{WR}			4.5			6			8			10			10	ns
Rise and Fall Times																	
Output rise time	t_R		2			2			2			2			2		ns
Output fall time	t_F		2			2			2			2			2		ns

Note:

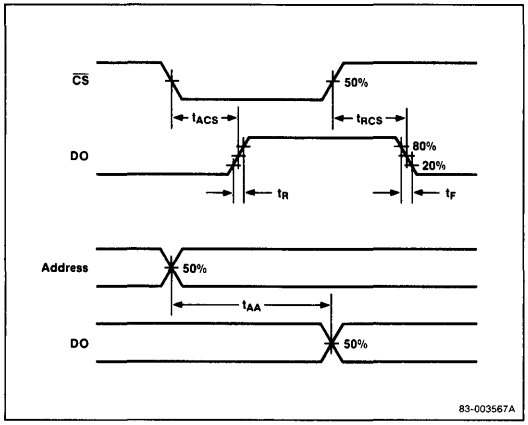
(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

(2) For the μPB100474-4.5/6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90 °C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10 °C/W.

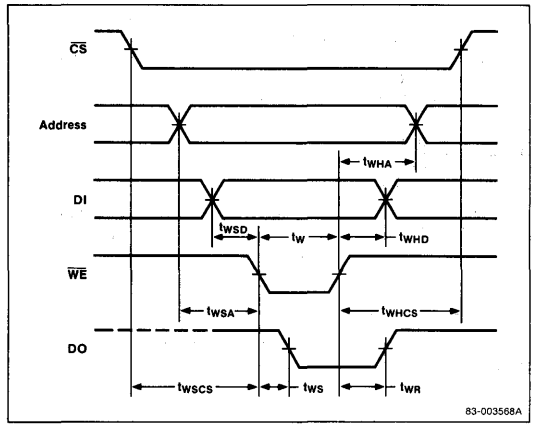
(3) See figures 1 and 2 for loading conditions and input pulse timing. For the μPB100474-4.5/6, C_L = 5 pF. For the μPB100474-8/10/15, C_L = 30 pF.

Timing Waveforms

Read Mode



Write Mode



UV and OTP EPROMs

9

Section 9 — UV and OTP EPROMs

NEC

NEC Electronics Inc.

μPD2764
8,192 x 8-BIT
NMOS UV/OTP EPROM

Revision 1

Description

The μPD2764 is a 65,536-bit (8,192 × 8-bit) electrically programmable read-only memory (EPROM). It operates from a single +5V supply making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with reduction in power consumption.

A distinctive feature of the μPD2764 is a separate output enable control ($\overline{OE}$) in addition to the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD2764 features conventional, simple one-pulse programming controlled by TTL-level signals as well as a high-speed programming mode. Total programming time for all 65,536 bits is 420 seconds for conventional mode, and typically 60 to 120 seconds for the high-speed mode.

The μPD2764 is available in a cerdip package with a quartz window as an ultraviolet (UV), erasable EPROM, or in a plastic package as a one-time-programmable (OTP), non-erasable EPROM.

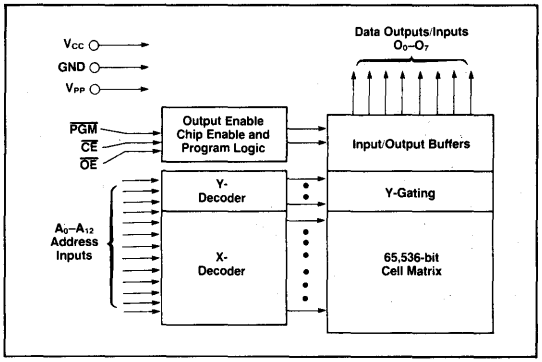
Features

- ☐ Ultraviolet erasable and electrically programmable
- ☐ Access time—200ns max
- ☐ Low power dissipation: 80mA max (active)
  25mA max (standby)
- ☐ High-speed programming mode
  (typical program time 60s to 120s)
- ☐ Programmable with single pulse
  (total program time 420s)
- ☐ Industry standard pinout (JEDEC approved)
- ☐ 4 performance ranges

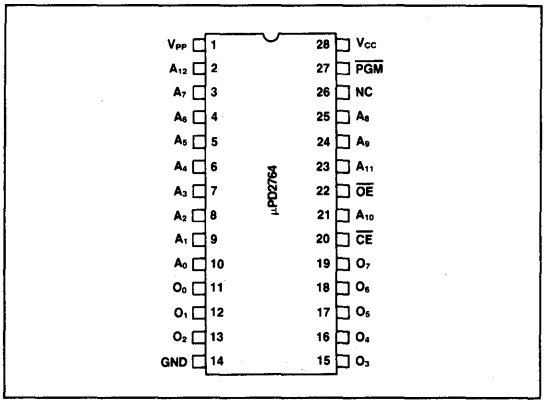
Device	Max Access Time	Max V_{CC} Supply Current	
		Active	Standby
μPD2764-2	200ns	80mA	25mA
μPD2764①	250ns	80mA	25mA
μPD2764-3①	300ns	80mA	25mA
μPD2764-4①	450ns	80mA	25mA

Note: ① Available as either UV or OTP.

Block Diagram



Pin Configuration



Pin Identification

A_0–A_{12}	Addresses
$\overline{OE}$	Output Enable
O_0–O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program
NC	No Connect

Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z

Note: X can be either V_{IL} or V_{IH}.

Absolute Maximum Ratings*

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.6V to +6.5V
Input Voltage	−0.6V to +6.5V
Supply Voltage V_{CC}	−0.6V to +6.5V
Supply Voltage V_{PP}	−0.6V to +22V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9

DC Characteristics

Read Mode and Standby Mode

T_A = 0°C to + 70°C; V_{CC} = +5V ± 5%; V_{PP} = V_{CC}

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Output Leakage Current	I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 5.25V
V_{CC} Current Standby	I_{CC1}			25	mA	$\overline{CE}$ = V_{IH}
V_{CC} Current Active	I_{CC2}			80	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{PP} Current	I_{PP1}			15	mA	V_{PP} = 5.25V

Note: V_{PP} may be connected directly to V_{CC} except during programming.

Program, Program Verify, and Program Inhibit Modes

T_A = 25°C ± 5°C; V_{CC}* = +5V ± 5%; V_{PP} = + 21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
V_{CC} Current	I_{CC2}			100	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

*V_{CC} = 6V ± 5% for high-speed programming.

AC Characteristics

Read Mode and Standby Mode

T_A = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits 2764-2 Min	2764-2 Max	2764 ① Min	2764 ① Max	2764-3 ① Min	2764-3 ① Max	2764-4 ① Min	2764-4 ① Max	Unit	Test Conditions
Address to Output Delay	t_{ACC}		200		250		300		450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		200		250		300		450	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$/V_{PP} to Data Output Delay	t_{OE}		70		100		120		120	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$/V_{PP} to Data Output Float Delay	t_{DF}	0	60	0	85	0	105	0	105	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold Time	t_{OH}	0		0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: ① Available as either UV or OTP.

Test Conditions—
Output Load: 1TTL gate and C_L = 100pF
Input Rise and Fall Times: 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Levels:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

Program, Program Verify, and Program Inhibit Modes

T_A = 25°C ± 5°C; V_{CC}* = +5V ± 5%; V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2			μs	Input Pulse Levels = 0.8V to 2.2V Input Timing Reference Level = 1.0V and 2.0V Output Timing Reference Level = 0.8V and 2V Input Rise and Fall Times: 20ns
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Chip Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from $\overline{OE}$	t_{OE}			150	ns	
Program Pulse Width*	t_{PW}	45	50	55	ms	
V_{PP} Setup Time	t_{VS}	2			μs	

*V_{CC} = 6V ± 5% and t_{PW} = 1 ms ± 5% for high-speed programming.

Capacitance

T_A = 25°C; f = 1MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	14	pF	V_{OUT} = 0V

Function

The μPD2764 operates from a single +5V power supply making it ideal for microprocessor applications.

The μPD2764 features a standby mode which reduces the power dissipation.

Operation

The five operation modes of the μPD2764 are listed in Table 1. In the read mode the only power supply required is a +5V supply. During programming all inputs are TTL levels except for V_{PP} which rises from V_{CC} level to 21V.

Read Mode

When $\overline{CE}$ and $\overline{OE}$ are at a low (0) level, Read is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD2764 is placed in a standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is also reduced.

Programming Modes

The μPD2764 can be programmed in two ways: (1) conventional programming mode, and (2) high-speed programming mode. In the conventional mode, basically a 50ms $\overline{PGM}$ pulse is applied to each bit location. The high-speed programming mode is similar to the Intelligent Programming Algorithm™, in which up to fifteen 1ms $\overline{PGM}$ pulses are applied to each bit location, followed by an additional 4ms $\overline{PGM}$ pulse for each number of 1ms pulse applied before. The high-speed programming mode reduces the programming time to 60s to 120s typical.

™: Intelligent Programming Algorithm is a registered trademark of Intel Corporation.

Conventional Programming Mode

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD2764 is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at +21V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially, or at random.

When multiple μPD2764s are connected in parallel except for $\overline{CE}$, individual μPD2764s can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD2764 to be programmed.

Programming of multiple μPD2764s in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

High-speed Programming Mode

In this mode, programming begins by addressing the first location, and applying valid data to the eight output pins (a low level TTL signal, 0, into the chosen bit location).

V_{CC} is then raised to 6V ± 0.25V followed by V_{PP} raised to 21V ± 0.5V. A $\overline{PGM}$ pulse of 1ms ± 5% is then applied in the same manner as described in the program mode timing diagram. The bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1ms $\overline{PGM}$ pulse is applied, to a maximum of fifteen times. If the bit gets programmed within fifteen efforts, another pulse of 4ms for each effort is applied and the next address is applied. If the bit does not get programmed in fifteen 1ms efforts, another $\overline{PGM}$ pulse of 60ms is applied and the bit verified. If the bit is not programmed at this stage, the device would be rejected as a program failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage, V_{CC} and V_{PP} pins are lowered to 5V ± 5% and all bytes are then verified again for programming.

Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at a high (1) level.

Programming Inhibit Mode

Programming multiple μPD2764s in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD2764s may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD2764 will inhibit it from being programmed.

Output Disable

The data outputs of two or more μPD2764s may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD2764s should be disabled by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the read line from the system control bus. These connections offer the lowest average power consumption.

Erasure Mode

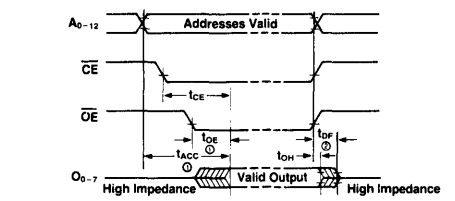
Erasure of the μPD2764 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD2764. Consequently, if the μPD2764 is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure. Opaque labels are supplied with every device.

The recommended erasure procedure for the μPD2764 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be not less than 15W-sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000μW/cm^2 power rating.

During erasure, the μPD2764 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Timing Waveforms

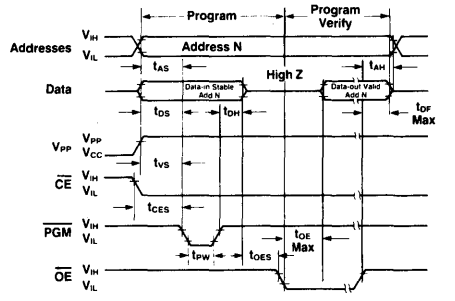
Read Mode



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Program Mode



μPD27128
16,384 x 8-BIT
NMOS UV/OTP EPROM

Revision 1

Description

The μPD27128 is a 131,072-bit (16,384 × 8) electrically programmable read-only memory (EPROM). It operates from a single +5V supply making it ideal for microprocessor applications. It features an output enable control and offers a standby mode with reduction in power consumption.

A distinctive feature of the μPD27128 is a separate output enable control ($\overline{OE}$) in addition to the chip enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple-bus microprocessor systems. The μPD27128 features conventional, simple one-pulse programming controlled by TTL-level signals as well as a high-speed programming mode. Total programming time for all 131,072 bits is 820 seconds for the conventional mode, and typically 120 seconds for the high-speed mode.

The μPD27128 is available in a cerdip package as an ultraviolet (UV), erasable EPROM, or in a plastic package as a one-time-programmable (OTP), non-erasable EPROM.

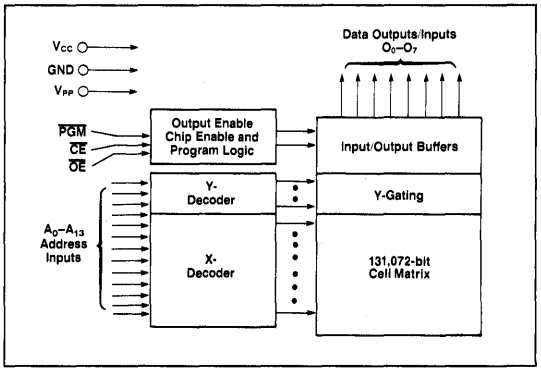
Features

- ☐ Ultraviolet erasable and electrically programmable
- ☐ Access time—200ns max
- ☐ Low power dissipation: 100mA max active current
  25mA max standby current
- ☐ High-speed programming mode
  (typical program time 120s)
- ☐ Programmable with single pulse
  (total program time 820s)
- ☐ Industry standard pinout (JEDEC approved)
- ☐ 4 performance ranges

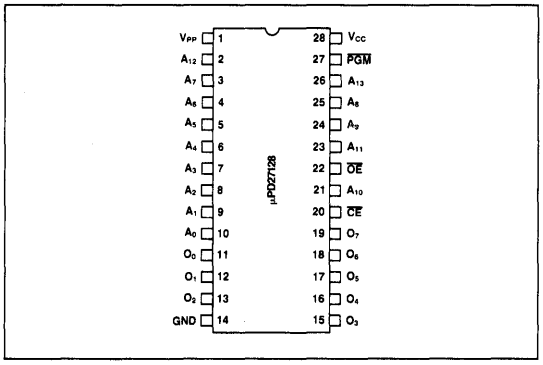
Device	Max Access Time	Max V_{CC} Supply Current	
		Active	Standby
μPD27128-2	200ns	100mA	25mA
μPD27128①	250ns	100mA	25mA
μPD27128-3①	300ns	100mA	25mA
μPD27128-4①	450ns	100mA	25mA

Note: ① Available as either UV or OTP.

Block Diagram



Pin Configuration



Pin Identification

A_0–A_{13}	Addresses
$\overline{OE}$	Output Enable
O_0–O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program

Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
High Speed Programming	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}

Note: X can be either V_{IL} or V_{IH}.

Absolute Maximum Ratings*

Operating Temperature	−10°C to +80°C
Storage Temperature	−65°C to +125°C
Output Voltage	−0.6V to 7.0V
Input Voltage	−0.6V to 7.0V
Supply Voltage V_{CC}	−0.6V to 7.0V
Supply Voltage V_{PP}	−0.6V to +22V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C; f = 1MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	14	pF	V_{OUT} = 0V

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DC Characteristics

Read Mode and Standby Mode

T_A = 0°C to + 70°C; V_{CC} = +5V ± 5%; V_{PP} = V_{CC}

Parameter		Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1mA
Input High Voltage		V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Output Leakage Current		I_{LO}			10	μA	V_{OUT} = 5.25V
Input Leakage Current		I_{LI}			10	μA	V_{IN} = 5.25V
V_{CC} Current	Standby	I_{CC1}			25	mA	$\overline{CE}$ = V_{IH}
	Active	I_{CC2}		60	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{PP} Current		I_{PP1}			15	mA	V_{PP} = 5.25V

Program, Program Verify, and Program Inhibit Modes

T_A = 25°C ± 5°C; V_{CC} ① = +5V ± 5%; V_{PP} = + 21V ± 0.5V

Parameter		Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage		V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage		V_{IL}	−0.1		0.8	V	
Input Leakage Current		I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output High Voltage		V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2.1mA
V_{CC} Current	Program Inhibit	I_{CC1}			25mA		$\overline{CE}$ = V_{IH}
	Program Verify	I_{CC2}			100mA		
V_{PP} Current	Program	I_{PP2}			30mA		$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
	Program Verify	I_{PP3}			15mA		$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}
	Program Inhibit	I_{PP4}			15mA		$\overline{CE}$ = V_{IH}

Note: ① V_{CC} = 6V ± 0.25V for high-speed programming.

AC Characteristics

Read Mode and Standby Mode

T_A = 0°C to +70°C; V_{CC} = +5V ± 5%; V_{PP} = V_{CC}

Parameter	Symbol	Limits 27128-2 Min	27128-2 Max	27128① Min	27128① Max	27128-3① Min	27128-3① Max	27128-4① Min	27128-4① Max	Unit	Test Conditions
Address to Output Delay	t_{ACC}		200		250		300		450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	t_{CE}		200		250		300		450	ns	$\overline{OE}$ = V_{IL}
Output Enable to Output Delay	t_{OE}		75		100		120		150	ns	$\overline{CE}$ = V_{IL}
Output Enable High to Output Delay	t_{DF}	0	60	0	85	0	105	0	130	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold Time	t_{OH}	0		0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: ① Available as either UV or OTP.

Test Conditions—
Output Load: See Fig. 1.
Input Rise and Fall Times: 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Levels:
Inputs: 0.8V and 2.0V
Outputs: 0.8V and 2.0V

AC Characteristics (Cont.)

Program, Program Verify, and Program Inhibit Modes

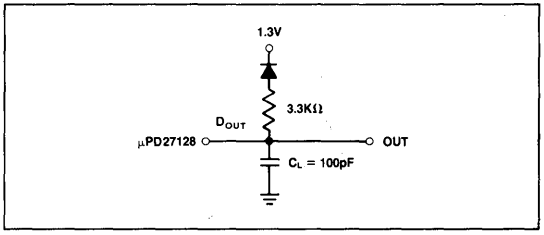
T_A = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2			μs	Input Pulse Levels = 0.45V to 2.4V Input Timing Reference Level = 0.8V and 2.0V Output Timing Reference Level = 0.8V and 2V Input Rise and Fall Times: 20ns
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	0			μs	
$\overline{CE}$ Setup Time	t_{CES}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Chip Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from $\overline{OE}$	t_{OE}			150	ns	
Program Pulse Width①	t_{PW}	45	50	55	ms	
V_{PP} Setup Time	t_{VS}	2			μs	

Note: ①V_{CC} = 6V ± 0.25V and t_{PW} = 1 ms ± 5% for high-speed programming.

Test Conditions—
Input Pulse Levels = 0.45V to 2.4V
Input Timing Reference Level = 0.8V and 2.0V
Output Timing Reference Level = 0.8V and 2V
Input Rise and Fall Times: 20ns

Figure 1. Loading Conditions Test Circuit



Function

The μPD27128 operates from a single +5V power supply making it ideal for microprocessor applications.

The μPD27128 features a standby mode which reduces the power dissipation.

Operation

The six operation modes of the μPD27128 are listed in Table 1. In the read mode the only power supply required is a +5V supply. During programming all inputs are TTL levels except for V_{PP} which rises from V_{CC} level to 21V.

Read Mode

When $\overline{CE}$ and $\overline{OE}$ are at a low (0) level, Read is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD27128 is placed in a standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input. The active power dissipation is also reduced.

Programming Modes

The μPD27128 can be programmed in two ways: (1) conventional programming mode, and (2) high-speed programming mode. In the conventional mode, basically a 50ms $\overline{PGM}$ pulse is applied to each bit location. The high-speed

programming mode is similar to the Intelligent Programming Algorithm™, in which up to fifteen 1ms $\overline{PGM}$ pulses are applied to each bit location, followed by an additional 4ms $\overline{PGM}$ pulse for each number of 1ms pulses applied before. The high-speed programming mode reduces the programming time to 120s typical.

Conventional Programming Mode

Programming begins with erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD27128 is placed in the programming mode by applying a low (0) level TTL signal to the $\overline{CE}$ and $\overline{PGM}$ with V_{PP} at +21V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially, or at random.

When multiple μPD27128s are connected in parallel except for $\overline{CE}$, individual μPD27128s can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD27128 to be programmed.

Programming of multiple μPD27128s in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

High-speed Programming Mode

In this mode, programming begins by addressing the first location, and valid data appearing at the eight output pins (a low level TTL signal, 0, into the chosen bit location).

V_{CC} is then raised to 6V ± 0.25V followed by V_{PP} raised to 21V ± 0.5V. A $\overline{PGM}$ pulse of 1ms ± 5% is then applied in the same manner as described in the program mode timing diagram. The bit is then verified and a program/no program decision is made. If the bit is not programmed, another 1ms $\overline{PGM}$ pulse is applied, to a maximum of fifteen times. If the bit gets programmed within fifteen efforts, another pulse of 4ms for each effort is applied and the next address is applied. If the bit does not get programmed in fifteen 1ms efforts, another $\overline{PGM}$ pulse of 60ms is applied and the bit verified. If the bit is not programmed at this stage, the device would be rejected as a program failure. If the bit is programmed, the next address is applied until all addresses are complete.

At this stage, V_{CC} and V_{PP} pins are lowered to 5V ± 5% and all bytes are then verified again for programming. This algorithm is compatible with that of the μPD2764.

Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at a high (1) level.

Programming Inhibit Mode

Programming multiple μPD27128s in parallel with different data is easier with the program inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$), all like inputs (including $\overline{OE}$) of the parallel μPD27128s may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ (or $\overline{PGM}$) input with V_{PP} at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD27128s will inhibit it from being programmed.

Output Disable

The data outputs of two or more μPD27128s may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD27128 should be disabled by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the read line from the system control bus. These connections offer the lowest average power consumption.

Erasure Mode

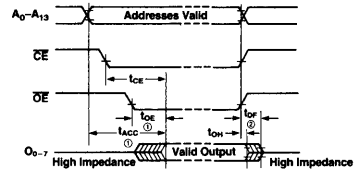
Erasure of the μPD27128 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD27128. Consequently, if the μPD27128 is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure. Opaque labels are supplied with every device.

The recommended erasure procedure for the μPD27128 is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be not less than 15W-sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000μW/cm^2 power rating.

During erasure, the μPD27128 should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Timing Waveforms

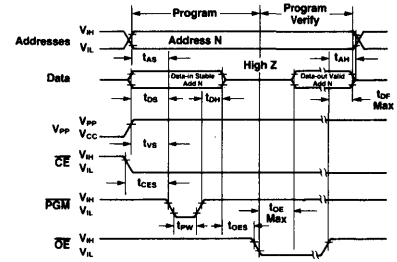
Read Mode



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Program Mode



μPD27256
32,768 x 8-BIT
NMOS UV EPROM

Revision 2

Description

The μPD27256 is a 262,144-bit electrically programmable read-only memory utilizing NMOS double-polysilicon technology. The device is organized as 32K words by 8 bits and operates from a single +5V ±5% power supply. All inputs and outputs are TTL-compatible. The μPD27256 has single location programming, three-state outputs and is pin-compatible with the 27C256 EPROM. It is available as a 28-pin DIP.

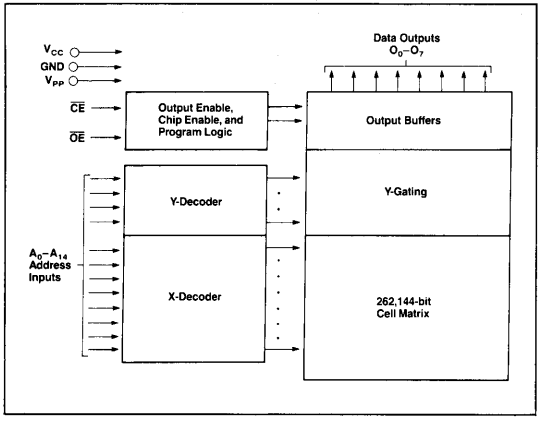
The μPD27256 is available in a cerdip package with a quartz window as an ultraviolet (UV), erasable EPROM.

Features

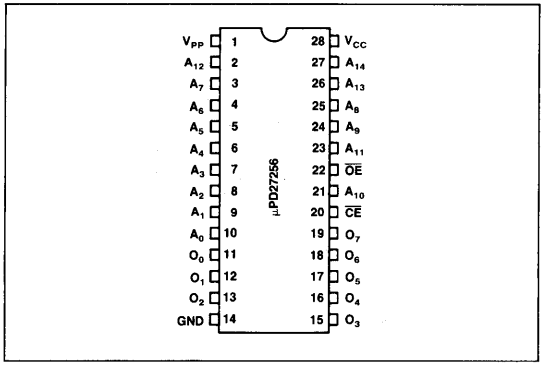
- ☐ 32K by 8 organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Access time — 200ns max
- ☐ Single location programming
- ☐ High-speed programming mode
- ☐ Low power dissipation: 100mA max (active)
  25mA max (standby)
- ☐ Input/output TTL-compatible for reading and programming
- ☐ Single +5V ±5% power supply
- ☐ Three-state outputs
- ☐ Pin-compatible with μPD27C256 EPROM
- ☐ NMOS double-polysilicon technology
- ☐ 28-pin DIP
- ☐ 3 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD27256	250ns	100mA	25mA
μPD27256-3	300ns	100mA	25mA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Description
1	V_{PP}	Program Voltage
2–10, 21, 23–27	A_0–A_{14}	Address Inputs
11–13, 15–19	O_0–O_7	Data Outputs
14	GND	Ground
20	$\overline{CE}$	Chip Enable
22	$\overline{OE}$	Output Enable
28	V_{CC}	+5V ±5% Power Supply

Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	V_{PP}	V_{CC}	High-Z

Note: X can be either V_{IL} or V_{IH}.

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Absolute Maximum Ratings*

Operating Temperature, T_{OPR}	−10°C to +80°C
Storage Temperature, T_{STG}	−65°C to +125°C
Output Voltage, V_{OH}	−0.6V to V_{CC} +6.5V
Input Voltage, V_{IH}	−0.6V to V_{CC} +6.5V
Supply Voltage, V_{CC}	−0.6V to +7V
Supply Voltage, V_{PP}	−0.6V to +22V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance ①

T_A = 25°C; f = 1MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	14	pF	V_{OUT} = 0V

Note: ① This parameter is sampled periodically.

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5V ±5%; V_{PP} = V_{CC}
Read and Standby Modes

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
Input High Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Output Leakage Current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}; V_{OUT} = 0 to V_{CC}
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
V_{CC} Current	I_{CC1}			25	mA	$\overline{CE}$ = V_{IH} (standby)
	I_{CC2}			100	mA	$\overline{CE}$ = V_{IL} (active)
V_{PP} Current	I_{PP1}			15	mA	V_{PP} = 5.25V

T_A = 25°C ± 5°C; V_{CC} = 6V ± 0.25V; V_{PP} = +21V ± 0.5V
Program, Program Verify, and Program Inhibit Modes

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC}+1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Output High Voltage	V_{OH}	2.4			V	V_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
V_{CC} Current	I_{CC2}			100	mA	
V_{PP} Current	I_{PP2}			30	mA	$\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}

AC Characteristics

T_A = 0°C to +70°C; V_{CC} = +5V ± 5%; V_{PP} = V_{CC}
Read and Standby Modes

Parameter	Symbol	Limits 27256 Min	27256 Max	27256-3 Min	27256-3 Max	Unit	Test Conditions ①
Address to Output Delay	t_{ACC}		250		300	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
CE to Output Delay	t_{CE}		250		300	ns	$\overline{CE}$ = V_{IL}
Output Enable to Output Delay	t_{OE}		100		120	ns	$\overline{CE}$ = V_{IL}
Output Enable High to Output Float	t_{DF}	0	85		105	ns	$\overline{CE}$ = V_{IL}
Address to Output Hold	t_{OH}	0		0		ns	$\overline{CE}$ = V_{IL}

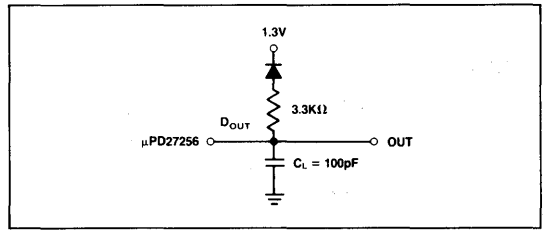
Notes: ① Output load: see Figure 1.
Input rise and fall times: 20ns.
Input pulse levels: 0.45V to 2.4V.
Input and output timing measurement reference levels: 0.8V and 2.0V.

T_A = 25°C ± 5°C; V_{CC} = +6V ± 0.25V; V_{PP} = 21V ± 0.5V
Program, Program Verify, and Program Inhibit Modes ① ②

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Set-up Time	t_{AS}	2			μs	
Data Set-up Time	t_{DS}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Address Hold Time	t_{AH}	2			μs	Input pulse levels = 0.45V to 2.4V
Chip Enable to Output Float Delay	t_{DF}			130	ns	Input and output timing reference levels = 0.8V and 2.0V
V_{CC} = Set-up Time	t_{VS}	2			μs	
Program Pulse Width	t_{PW}	0.95	1	1.05	ms	
$\overline{CE}$ Set-up Time	t_{CES}	2			μs	Input rise and fall times = 20ns
$\overline{OE}$ Set-up Time	t_{OES}	2			μs	
$\overline{OE}$ Hold Time ③	t_{OEH}	2			μs	
$\overline{OE}$ Recovery Time ③	t_{OR}	2			μs	
$\overline{CE}$ to Output Valid ③	t_{DV}			1	μs	

Notes: ① V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
② V_{CC} must be applied simultaneously or before V_{PP} and removed after V_{PP}.
③ These parameters are sampled periodically.

Figure 1. Loading Conditions Test Circuit



Programming Operation

High Speed Programming Mode

Begin programming by erasing all data; this places all bits in the high level (1) state. Enter data by programming a low level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the 8 output pins. Raise V_{CC} to +6 V ±.25 V; then raise V_{PP} to +21 V ±.5 V. Apply a 1 ms (±5%) program pulse to $\overline{CE}$ as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1 ms pulse to $\overline{CE}$ up to a maximum of 20 times. If the bit is programmed within 20 tries, apply an additional overprogram pulse of (1 x number of tries) ms and input the next address. If the bit is not programmed in 20 tries, reject the device as a program failure.

After all bits are programmed, lower both V_{CC} and V_{PP} to +5 V ±5% and verify all data again.

Programming Inhibit Mode

Use the programing inhibit mode to program multiple μPD27256s connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low level (0) TTL pulse to the $\overline{CE}$ input of the μPD27256 to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed data to determine that the data was correctly programmed. The program verification can be performed with the $\overline{CE}$ and $\overline{OE}$ at low levels (0).

Erasure

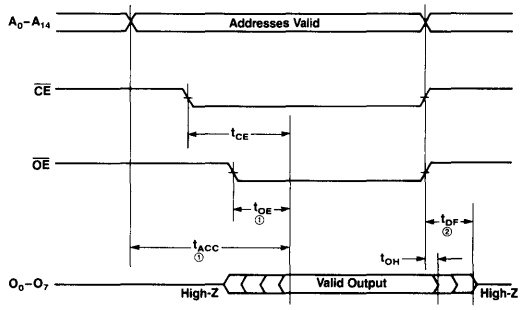
Erase data on the μPD27256 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254 nm ultraviolet rays. A lighting level of 15 W-sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity x exposure time.)

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27256 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

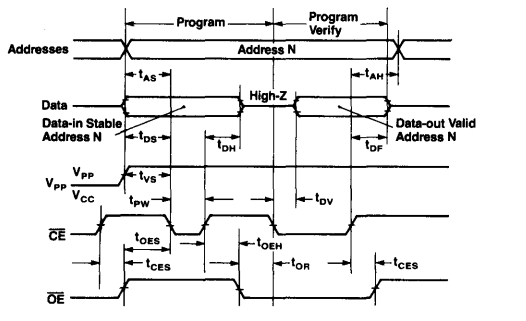
Timing Waveforms

Read Mode



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Program Mode



μPD27C64
8,192 x 8-BIT
CMOS UV/OTP EPROM

Revision 1

Description

The μPD27C64 is a 65,536-bit (8,192 × 8-bit) electrically programmable read-only memory (EPROM). It operates from a single +5 V power supply making it ideal for microprocessor applications. It is fabricated using an advanced CMOS process which saves substantial power in operating and standby modes.

A distinctive feature of the μPD27C64 is an output enable (OE) separate from the chip enable (CE). The OE control eliminates bus contention in multiple-bus microprocessor systems. The μPD27C64 features fast, simple, one-pulse programming controlled by TTL-level signals. A high-speed programming mode is also available.

The μPD27C64 is available in a cerdip package with a quartz window as an ultraviolet (UV), erasable EPROM, or in a plastic package as a one-time-programmable (OTP), non-erasable EPROM.

Features

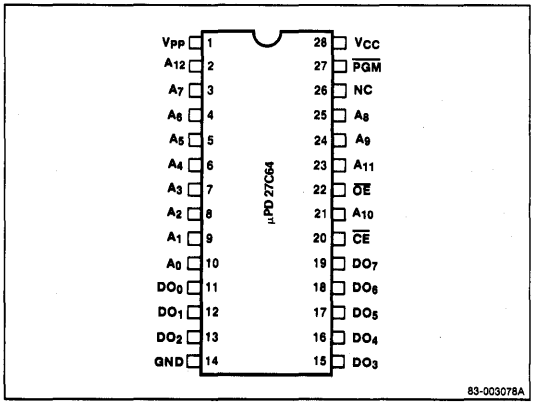
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Low supply current:
  - —30 mA (max) active current
  - —100 μA (max) standby current
- ☐ High-speed programming mode
- ☐ Single location programming
- ☐ Programmable with single pulse (total programming time is 420 sec in standard mode)
- ☐ Input/output TTL-compatible
- ☐ Single +5 V power supply
- ☐ Low power dissipation:
  - —33 mW/MHz (max) operating
  - —550 μW (max) standby
- ☐ μPD2764-compatible
- ☐ 28-pin DIP

Performance Ranges

Device	Access Time (Max)	Power Supply (Max) Active	Standby
μPD27C64-20	200 ns	30 mA	100 μA
μPD27C64-25(1)	250 ns	30 mA	100 μA
μPD27C64-30(1)	300 ns	30 mA	100 μA

Note:
(1) Available as either UV or OTP.

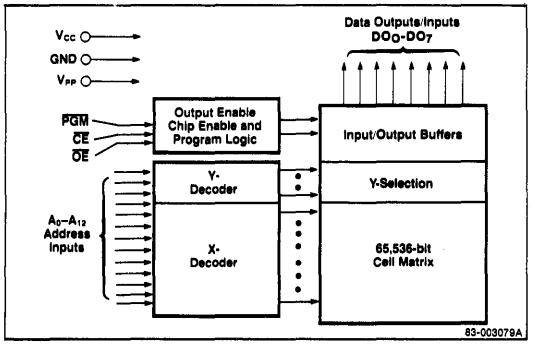
Pin Configuration



Pin Identification

No.	Symbol	Function
1	V_{PP}	Program voltage
2-10, 21, 23-25	A_0-A_{12}	Address inputs
11-13, 15-19	DO_0-DO_7	Data inputs/outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	$\overline{OE}$	Output enable
26	NC	No connection
27	$\overline{PGM}$	Program
28	V_{CC}	+5 V power supply

Block Diagram



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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.3 V to +7.0 V
Input voltage, V_{IN}	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10°C to +80°C
Storage temperature, T_{STG}	−65°C to +125°C
Program voltage, V_{PP}	−0.3 V to +22 V

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	$V_{IN} = 0$ V
Output capacitance	C_{OUT}			12	pF	$V_{OUT} = 0$ V

DC Characteristics

Read and Standby Modes

$T_A = 0°C$ to +70°C, $V_{CC} = +5$ V ± 10%, $V_{PP} = V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Input voltage, high	V_{IH}	2.0		$V_{CC}+0.3$	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output leakage current	I_{LO}			10	μA	$\overline{OE} = V_{IH}$, $V_{OUT} = 0$ V to V_{CC}
Input leakage current	I_{LI}			10	μA	$V_{IN} = 0$ V to V_{CC}
Operating supply current	I_{CCA1}			10	mA	$\overline{CE} = V_{IL}$, $V_{IN} = V_{IH}$
Operating supply current	I_{CCA2}			30	mA	f = 5 MHz, $I_{OUT} = 0$ mA
Standby supply current	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
Standby supply current	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$, $V_{IN} = 0$ V to V_{CC}
Program voltage current	I_{PP1}		1	100	μA	$V_{PP} = V_{CC} \pm 0.6$ V

Standard Programming, Program Verify, and Program Inhibit Modes

$T_A = 25°C \pm 5°C$, $V_{CC} = +5$ V ± 10%, $V_{PP} = +21$ V ± 0.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Input voltage, high	V_{IH}	2.0		$V_{CC}+0.3$	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Operating supply current	I_{CC2}			30	mA	
Program voltage current	I_{PP}			30	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

High-Speed Programming Mode

$T_A = 25°C \pm 5°C$, $V_{CC} = +6$ V ± 0.25 V, $V_{PP} = +21$ V ± 0.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Input voltage, high	V_{IH}	2.0		$V_{CC}+1$	V	
Input voltage, low	V_{IL}	−0.1		0.8	V	
Input leakage current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Operating supply current	I_{CC2}			30	mA	
Program voltage current	I_{PP}			30	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

AC Characteristics

Read and Standby Modes

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, $V_{PP} = V_{CC}$

Parameter	Symbol	Limits μPD27C64-20 Min	Limits μPD27C64-20 Max	Limits μPD27C64-25(1) Min	Limits μPD27C64-25(1) Max	Limits μPD27C64-30(1) Min	Limits μPD27C64-30(1) Max	Unit	Test Conditions(2)
Address to output delay	t_{ACC}		200		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		200		250		300	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ low to data output delay	t_{OE}	10	75	10	100	10	120	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to data output float delay	t_{DF}	0	60	0	85	0	105	ns	$\overline{CE} = V_{IL}$
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note:

(1) Available in either UV or OTP.

(2) Output load: see Loading Conditions Test Circuit. Input rise and fall times: 20 ns. Input pulse levels: 0.45 V to 2.4 V. Timing measurement reference levels:
Inputs: 0.8 V and 2.0 V
Outputs: 0.8 V and 2.0 V.

Standard Programming, Program Verify, and Program Inhibit Modes

$T_A = 25°C \pm 5°C$, $V_{CC} = +5V \pm 10\%$, $V_{PP} = +21V \pm 0.5V$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	(Notes 1, 2, 3)
Data setup time	t_{DS}	2			μs	(Notes 1, 2, 3)
Address hold time	t_{AH}	0			μs	(Notes 1, 2, 3)
Data hold time	t_{DH}	2			μs	(Notes 1, 2, 3)
Output enable to output float delay	t_{DF}	0		130	ns	(Notes 1, 2, 3)
Program supply setup time	t_{VS}	2			μs	(Notes 1, 2, 3)
Program pulse width	t_{PW}	20	50	55	ms	(Notes 1, 2, 3)
$\overline{CE}$ setup time	t_{CES}	2			μs	(Notes 1, 2, 3)
$\overline{OE}$ setup time	t_{OES}	2			μs	(Notes 1, 2, 3)
$\overline{OE}$ to data utilization delay	t_{OE}			150	ns	(Notes 1, 2, 3)

Note:

(1) Input pulse levels: $V_I = 0.45V$ to 2.4 V.

(2) Input and output timing reference levels = 0.8 V and 2.0 V.

(3) Input rise and fall times = 20 ns.

High-Speed Programming Mode

$T_A = 25°C \pm 5°C$, $V_{CC} = +6V \pm 0.25V$, $V_{PP} = +21V \pm 0.5V$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	(Notes 1, 2)
Data setup time	t_{DS}	2			μs	(Notes 1, 2)
Address hold time	t_{AH}	2			μs	(Notes 1, 2)
Data hold time	t_{DH}	2			μs	(Notes 1, 2)
Chip enable to output float delay	t_{DF}	0		130	ns	(Notes 1, 2)
Supply current setup time	t_{VCS}	2			μs	(Notes 1, 2)
Program setup time	t_{VPS}	2			μs	(Notes 1, 2)
Initial program pulse width	t_{PW}	0.95	1	1.05	ms	(Notes 1, 2)
Additional program pulse range	t_{OPW}	3.8		63	ms	(Notes 1, 2)
$\overline{CE}$ setup time	t_{CES}	2			μs	(Notes 1, 2)
$\overline{OE}$ setup time	t_{OES}	2			μs	(Notes 1, 2)
$\overline{OE}$ data utilization delay	t_{OE}			150	ns	(Notes 1, 2)

Note:

(1) Input pulse levels: $V_I = 0.45V$ to 2.4 V.

(2) Input and output timing reference levels = 0.8 V and 2.0 V.

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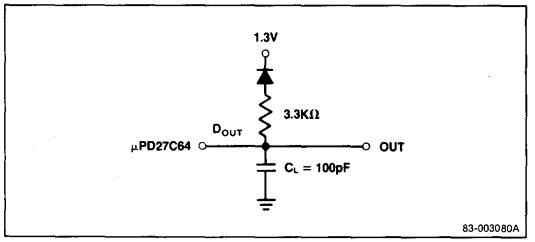
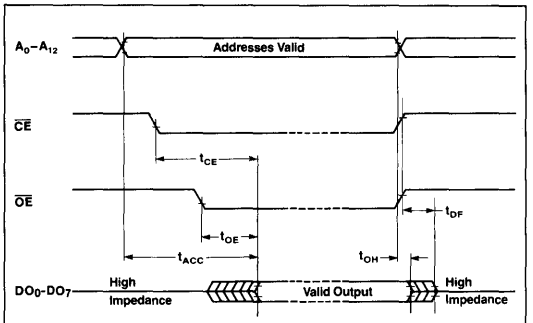
Figure 1. Loading Conditions Test Circuit



Timing Waveforms

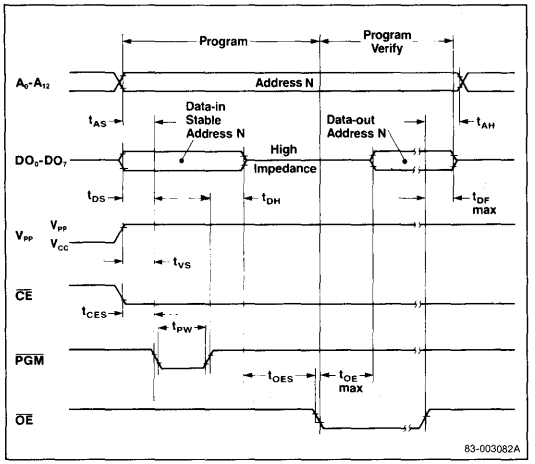
Read Mode



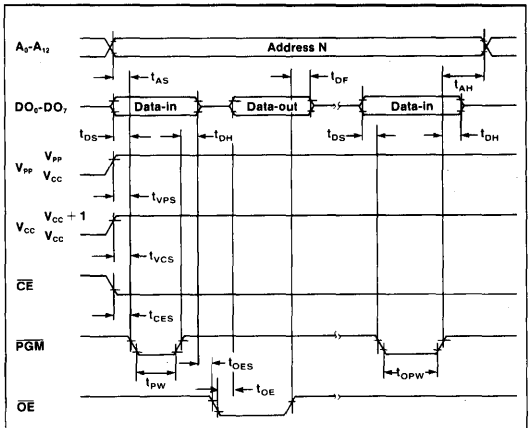
Note:
1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

83-003081A

Programming Mode



High-Speed Programming Mode



Note:
1. If a read is performed within the t_{ACC} range, the $\overline{OE}$ input lead time from $\overline{CE}$ fall time is $t_{ACC}-t_{OE}$ (max).
2. t_{DF} represents the time from the rise of $\overline{OE}$ or $\overline{CE}$, whichever rises to V_{IH} first.
3. Connect V_{CC} before V_{PP} and disconnect after V_{PP}.

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Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5 V	+5 V	Data output
Standby	V_{IH}	X	X	+5 V	+5 V	High impedance
Standard program	V_{IL}	X	V_{IL}	V_{PP}	+5 V	Data input
Program verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	+5 V	Data output
Program inhibit	V_{IH}	X	X	V_{PP}	+5 V	High impedance
High-speed programming	V_{IL}	X	V_{IL}	V_{PP}	+6 V	Data input

Note:
(1) X can be either V_{IL} or V_{IH}. (V_{IH} = TTL-level high input voltage, V_{IL} = TTL-level low input voltage)

Function

The μPD27C64 uses a single standard +5 V power supply (μPD8086, μPD8085, μPD8088). Furthermore, all the input/output terminals are TTL-level so that the total system can be simplified. For programming purposes, an additional +21 V power supply is required.

The μPD27C64 does not require any complex programming devices. Programming can be done while chips are mounted on a system board. A single TTL-level pulse (pulse duration 50 ms) is used to program any single address.

The μPD27C64 features a standby mode which reduces the power dissipation from the maximum active power dissipation of 165 mW to a maximum standby power dissipation of 550 μW. This results in a power savings of over 99% with no increase in access time.

Erasure

Data written on the μPD27C64 can be erased by light with a wavelength shorter than 400 nm. If it is exposed to direct sunlight or fluorescent light, programmed data may be erased. Therefore, in order to protect the programmed data, mask the window to prevent erasing by ultraviolet rays.

Data on the μPD27C64 is usually erased by 254 nm ultraviolet rays. The lighting level required to completely erase written data is 15 W-sec/cm^2 (min) (ultraviolet ray intensity × exposure time).

An ultraviolet lamp of 12,000 μW/cm^2 will take approximately 15 to 20 minutes. The distance between the lamp and μPD27C64 should be within 2.5 cm. The filter on the ultraviolet lamp should be removed for this operation. The program protect seal should also be removed from the window of the μPD27C64.

Operation

The six operation modes of the μPD27C64 are listed in the truth table. V_{CC} should be set to +5 V for each Read, Standby, Standard programming, Program verify, or Program inhibit mode. V_{CC} should be set to +6 V for the High-speed Programming mode. Control terminals $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$, and V_{PP} should be set according to the data in this table.

Read Mode

When $\overline{CE}$ and $\overline{OE}$ are at a low (0) level, Read is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The μPD27C64 is placed in a standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode the outputs are in a high-impedance state, independent of the $\overline{OE}$ input. The active power dissipation is reduced from 165 mW to 550 μW.

Programming Modes

The μPD27C64 can be programmed in two ways: (1) standard programming mode, and (2) high-speed programming mode. In the standard mode, basically a 50 ms $\overline{PGM}$ pulse is applied to each bit location. The high-speed programming mode is similar to the Intelligent Programming Algorithm® in which up to fifteen 1 ms $\overline{PGM}$ pulses are applied to each bit location, followed by an additional $\overline{PGM}$ pulse, of which the width is 4 ms for each number of 1 ms pulses applied before. The high-speed programming mode reduces the programming time to typically 60 s to 120 s.

Standard Programming Mode

Programming begins by erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The μPD27C64 is placed in the programming mode by applying a low (0) TTL-level program pulse to the $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at +21 V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially, or at random.

When multiple μPD27C64s are connected in parallel except for $\overline{CE}$, individual μPD27C64s can be programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ input of the desired μPD27C64 to be programmed.

Programming of multiple μPD27C64s in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{PGM}$ inputs.

High-speed Programming Mode

In this mode, programming begins by addressing the first location, and applying valid data to the eight output pins (a low-level TTL signal, 0, into the chosen bit location).

V_{CC} is then raised to 6 V ± 0.25 V followed by V_{PP} raised to 21 V ± 0.5 V. A $\overline{PGM}$ pulse of 1 ms ± 5% is then input in the same manner as described in the programming mode timing diagram. The bit is then verified and a program/no-program decision is made. If the bit is not yet programmed, another 1 ms $\overline{PGM}$ pulse is input, to a maximum of fifteen times. If the bit is programmed within fifteen efforts, another pulse of 4 ms for each effort is input and the next address is input. If the bit does not program within fifteen 1 ms efforts, another $\overline{PGM}$ pulse of 60 ms is input and the bit verified. If the bit is not programmed at this stage, the device would be rejected as a program failure. If the bit is programmed, the next address is input until all addresses are complete.

At this stage, V_{CC} and V_{PP} pins are lowered to 5 V ± 5% and all bytes are then verified again for programming.

® Intelligent Programming Algorithm is a registered trademark of Intel Corporation.

Program Inhibit Mode

Programming multiple μPD27C64s in parallel with different data is easier with the programming inhibit mode. Except for $\overline{CE}$ (or $\overline{PGM}$) all like inputs (including $\overline{OE}$) of the parallel μPD27C64s may be common. Programming is accomplished by applying a low (0) TTL-level program pulse to the $\overline{CE}$ and $\overline{PGM}$ inputs with V_{PP} at +21V. A high (1) level applied to the $\overline{CE}$ (or $\overline{PGM}$) of the other μPD27C64 will inhibit it from being programmed.

Program Verify Mode

A verify should be performed on the programmed bits to determine that the data was correctly programmed. The program verify can be performed with $\overline{CE}$ and $\overline{OE}$ at low (0) levels and $\overline{PGM}$ at a high (1) level.

Output Disable

The data outputs of two or more μPD27C64s may be wire-ORed together to the same data bus. In order to prevent bus contention problems between devices, all but the selected μPD27C64s should be disabled by raising the $\overline{CE}$ input to a TTL high. $\overline{OE}$ input should be made common to all devices and connected to the read line from the system control bus. These connections offer the lowest average power consumption.

μPD27C256
32,768 x 8-BIT
CMOS UV/OTP EPROM

Revision 1

Description

The μPD27C256 is a 262,144-bit ultraviolet erasable and electrically programmable read-only memory utilizing CMOS double-polysilicon technology. The device is organized as 32K words by 8 bits and operates from a single +5 V power supply. All inputs and outputs are TTL-compatible. The μPD27C256 has single location programming, three-state outputs and is pin-compatible with the 27256 EPROM. It is available as a 28-pin DIP.

The μPD27C256 is available in a cerdip package with a quartz window as an ultraviolet (UV) erasable EPROM, or in a plastic package as a one-time-programmable (OTP), non-erasable EPROM.

The μPD27C256 has a V_{PP} of 21 V.

Features

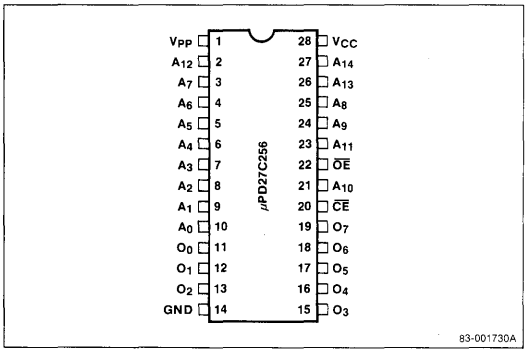
- ☐ 32K-word by 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Single location programming
- ☐ High-speed programming mode
- ☐ Low power dissipation:
  - 165 mW (active)
  - 550 μW (standby)
- ☐ Input/output TTL-compatible for reading and programming
- ☐ Single +5 V power supply
- ☐ JEDEC vendor identification mode
- ☐ Three-state outputs
- ☐ Pin-compatible with μPD27256 EPROM
- ☐ CMOS double-polysilicon technology
- ☐ 28-pin DIP

Performance Ranges

Device	Access Time (Max)	Power Supply (Max) Active	Standby
μPD27C256-15	150 ns	30 mA	100 μA
μPD27C256-20[1]	200 ns	30 mA	100 μA
μPD27C256-25[1]	250 ns	30 mA	100 μA

Note: [1] Available as either UV or OTP. OTP version is *preliminary*.

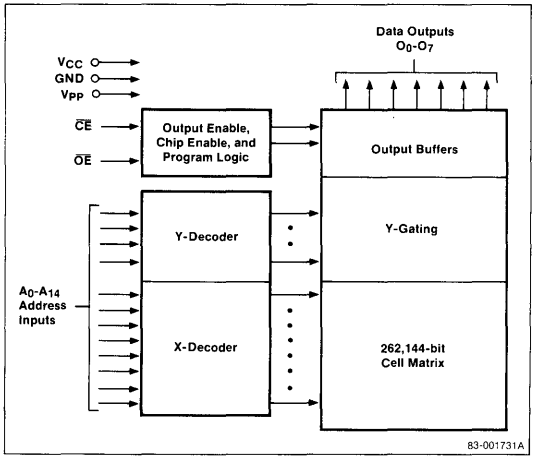
Pin Configuration



Pin Identification

No.	Symbol	Function
1	V_{PP}	Program voltage
2-10, 21, 23-27	A_0-A_{14}	Address inputs
11-13, 15-19	O_0-O_7	Data outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	$\overline{OE}$	Output enable
28	V_{CC}	+5 V power supply

Block Diagram



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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 V to +7.0 V
Input voltage, V_{IN}[1]	−0.6 V to V_{CC} + 0.6 V
Output voltage, V_{OUT}	−0.6 V to V_{CC} + 0.6 V
Operating temperature, T_{OPR}	−10°C to 80°C
Storage temperature, T_{STG}	−65°C to 125°C
Program voltage, V_{PP}	−0.6 V to +22 V
ID read voltage on pin 24, V_{ID}	−0.6 V to +13.5 V

Note: [1] V_{IN} = −3.0 V min for 20 ns pulse.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz [Note 1]

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}			12	pF	V_{OUT} = 0 V

Note: [1] This parameter is sampled and not 100% tested.

DC Characteristics

Read and Standby Modes

T_A = 0°C to +70°C, V_{CC} = +5 V ±10%(1); V_{PP} = V_{CC}

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC}+0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output leakage current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}, V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}
Operating supply current	I_{CCA2}			30	mA	5 MHz, I_{OUT} = 0 mA
Standby supply current	I_{SB1}			1	mA	$\overline{CE}$ = V_{IH}
Standby supply current	I_{SB2}			100	μA	$\overline{CE}$ = V_{CC}
Program voltage current	I_{PP1}			100	μA	V_{PP} = V_{CC}

Note: [1] For μPD27C256-15: V_{CC} = 5 V ±5%

Program, Program Verify, and Program Inhibit Modes

T_A = 25°C ±5°C, V_{CC} = +6 V ±0.25 V, V_{PP} = +21 V ±0.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC}+0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
ID read voltage	V_{ID}	11.5		12.5	V	
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP2}			30	mA	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}

AC Characteristics

Read and Standby Modes

$T_A = 0°C$ to $+70°C$, $V_{CC} = +5\ V \pm 10\%$(3); $V_{PP} = V_{CC}$

Parameter	Symbol	Limits μPD27C256-15 Min	Max	μPD27C256-20[1] Min	Max	μPD27C256-25[1] Min	Max	Unit	Test Conditions[2]
Address to output delay	t_{ACC}		150		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		150		200		250	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ low to data output delay	t_{OE}		75		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to data output float delay	t_{DF}		60		60		85	ns	$\overline{CE} = V_{IL}$
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Notes: [1] Available in either UV or OTP.
[2] Output load: see figure 1.
Input rise and fall times: 20 ns.
Input pulse levels: 0.45 V to 2.4 V.
Timing measurement reference levels:
Inputs: 0.8 V and 2.0 V
Outputs: 0.8 V and 2.0 V.
[3] For μPD27C256-15: $V_{CC} = 5\ V \pm 5\%$

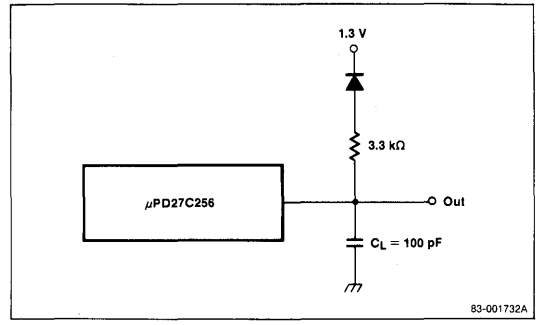
Program, Program Verify, and Program Inhibit Modes

$T_A = 25°C \pm 5°C$, $V_{CC} = +6\ V \pm 0.25\ V$, $V_{PP} = +21\ V \pm 0.5\ V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	[Notes 2, 3, 4]
Data setup time	t_{DS}	2			μs	[Notes 2, 3, 4]
Address hold time	t_{AH}	2			μs	[Notes 2, 3, 4]
Data hold time	t_{DH}	2			μs	[Notes 2, 3, 4]
Chip enable to output float delay	t_{DF}			130	ns	[Notes 2, 3, 4]
Supply current setup time	t_{VS}	2			μs	[Notes 2, 3, 4]
Program pulse width	t_{PW}	0.95	1	1.05	ms	[Notes 2, 3, 4]
$\overline{CE}$ setup time	t_{CES}	2			μs	[Notes 2, 3, 4]
$\overline{OE}$ setup time	t_{OES}	2			μs	[Notes 2, 3, 4]
$\overline{OE}$ hold time[1]	t_{OEH}	2			μs	[Notes 2, 3, 4]
$\overline{OE}$ recovery time[1]	t_{OR}	2			μs	[Notes 2, 3, 4]
$\overline{CE}$ to output valid	t_{DV}			1	μs	[Notes 2, 3, 4]

Notes: [1] $t_{OEH} + t_{OR} \geq 50\ \mu s$.
[2] Input pulse levels = 0.45 V to 2.4 V.
[3] Input and output timing reference levels = 0.8 V and 2.0 V.
[4] Input rise and fall times = 20 ns.

Figure 1. Loading Conditions Test Circuit



Truth Table

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	Hi-Z
ID read	V_{IL}	V_{IL}	V_{ID}	V_{CC}	V_{CC}	D_{OUT}

Note: [1] X can be either V_{IL} or V_{IH}.

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Programming Operation

High Speed Programming Mode

Begin programming by erasing all data; this places all bits in the high level (1) state. Enter data by programming a low level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the 8 output pins. Raise V_{CC} to +6 V ± 0.25 V; then raise V_{PP} to +21 V ± 0.5 V. Apply a 1 ms (±5%) program pulse to $\overline{CE}$ as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1 ms pulse to $\overline{CE}$ up to a maximum of 20 times. If the bit is programmed within 20 tries, apply an additional overprogram pulse of (1 × number of tries) ms and input the next address. If the bit is not programmed in 20 tries, reject the device as a program failure.

After all bits are programmed, lower both V_{CC} and V_{PP} to +5 V ± 5% and verify all data again.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C256s connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low level (0) TTL pulse to the $\overline{CE}$ input of the μPD27C256 to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed data to determine that the data was correctly programmed. The program verification can be performed with the $\overline{CE}$ and $\overline{OE}$ at low levels (0).

Erasure

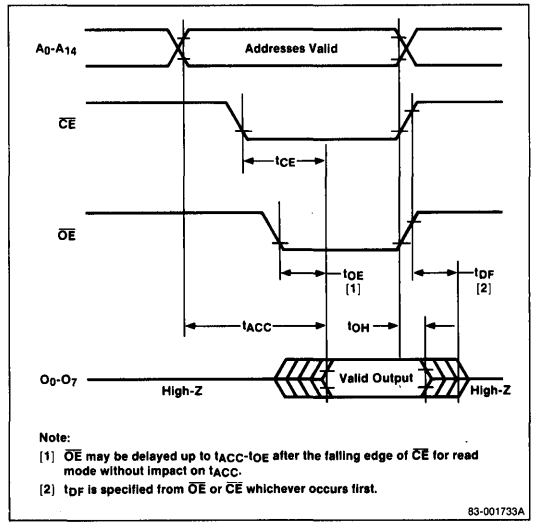
Erase data on the μPD27C256 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254 nm ultraviolet rays. A lighting level of 15 W-sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity × exposure time).

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C256 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

Timing Waveforms

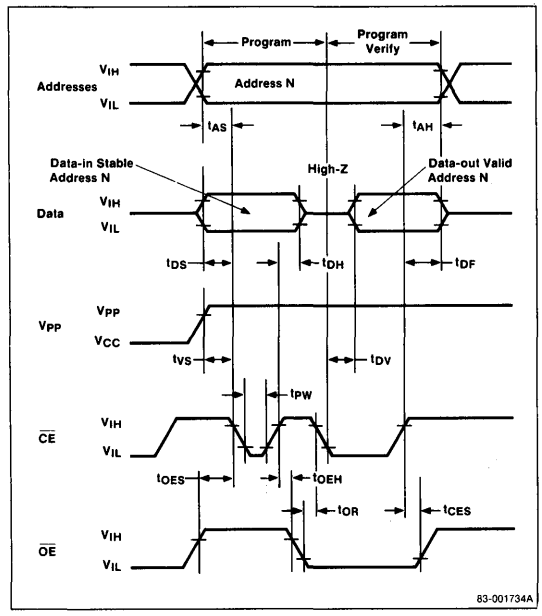
Read Mode



Note:
[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

83-001733A

Program Mode



83-001734A

μPD27C256A
32,768 x 8-BIT
CMOS UV/OTP EPROM

Description

The μPD27C256A is a 262,144-bit ultraviolet erasable and electrically programmable read-only memory utilizing CMOS double-polysilicon technology. The device is organized as 32K words by 8 bits and operates from a single +5 V power supply. All inputs and outputs are TTL-compatible. The μPD27C256A has single location programming, three-state outputs and is pin-compatible with the 27256 EPROM. It is available as a 28-pin DIP.

The μPD27C256A is available in a cerdip package with a quartz window as an ultraviolet (UV) erasable EPROM, or in a plastic package as a one-time-programmable (OTP) non-erasable EPROM. High density surface mount packages are available for both UV and OTP versions.

The μPD27C256A has a program voltage (V_{PP}) of 12.5 V.

Features

- ☐ 32K-word by 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Single location programming
- ☐ High-speed programming mode
- ☐ Low power dissipation,
  - —Active: 165 mW
  - —Standby: 550 μW
- ☐ Input/output TTL-compatible for reading and programming
- ☐ Single +5 V ± 10% power supply
- ☐ JEDEC vendor identification mode
- ☐ Three-state outputs
- ☐ Pin-compatible with μPD27256 EPROM
- ☐ CMOS double-polysilicon technology
- ☐ 28-pin DIP, plastic miniflat, or 32-pin ceramic LCC packages

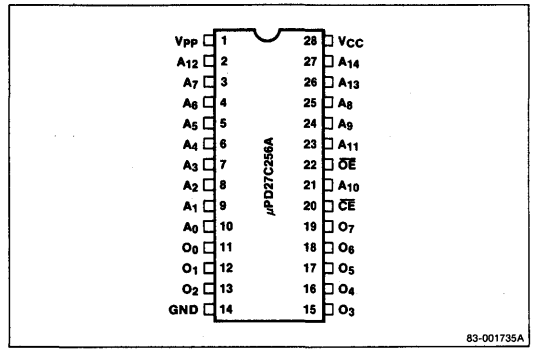
Performance Ranges

Device	Access Time (Max)	Power Supply (Max) Active	Standby
μPD27C256A-12	120 ns	30 mA	100 μA
μPD27C256A-15(1)	150 ns	30 mA	100 μA
μPD27C256A-20(1)	200 ns	30 mA	100 μA

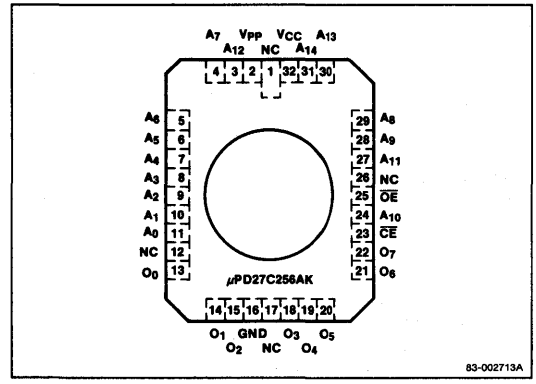
Note:
(1) Available as either UV or OTP. OTP version is *preliminary*.

Pin Configuration

28-Pin DIP, Plastic Miniflat



32-Pin Ceramic Leadless Chip Carrier (LCC)



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Pin Identification

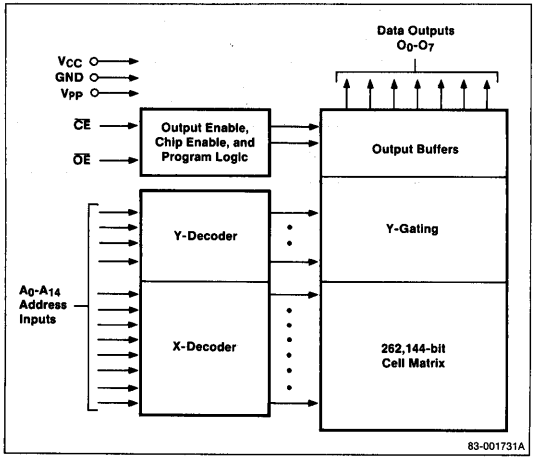
DIP and Plastic Miniflat

No.	Symbol	Function
1	V_{PP}	Program voltage
2-10, 21, 23-27	A_0-A_{14}	Address inputs
11-13, 15-19	O_0-O_7	Data outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	$\overline{OE}$	Output enable
28	V_{CC}	+5 V ±10% power supply

Ceramic LCC

No.	Symbol	Function
1, 12, 17, 26	NC	No connection
2	V_{PP}	Program voltage
3-11, 24, 27-31	A_0-A_{14}	Address inputs
13-15, 18-22	O_0-O_7	Data outputs
16	GND	Ground
23	$\overline{CE}$	Chip enable
25	$\overline{OE}$	Output enable
32	V_{CC}	+5 V ±10% power supply

Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 V to +7.0 V
Input voltage, V_{IN}(1)	−0.6 V to V_{CC} + 0.6 V
Output voltage, V_{OUT}	−0.6 V to V_{CC} + 0.6 V
Operating temperature, T_{OPR}	−10°C to 80°C
Storage temperature, T_{STG}	−65°C to 125°C
Program voltage, V_{PP}	−0.6 V to +13.0 V
ID read voltage on pin 24, V_{ID}	−0.6 V to +13.5 V

Note:
(1) V_{IN} = −3.0 V min for 20 ns pulse.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz (Note 1)

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_{IN}			6	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}			12	pF	V_{OUT} = 0 V

Note:
(1) This parameter is sampled and not 100% tested.

DC Characteristics

Read and Standby Modes

T_A = 0 to +70°C, V_{CC} = +5 V ±10%, V_{PP} = V_{CC}

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC}+0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output leakage current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}, V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}
Operating supply current	I_{CCA2}			30	mA	5 MHz, I_{OUT} = 0 mA
Standby supply current	I_{SB1}			1	mA	$\overline{CE}$ = V_{IH}
Standby supply current	I_{SB2}			100	μA	$\overline{CE}$ = V_{CC}
Program voltage current	I_{PP1}			100	μA	V_{PP} = V_{CC}

Program, Program Verify, and Program Inhibit Modes

T_A = 25°C ± 5°C, V_{CC} = +6 V ±0.25 V, V_{PP} = +12.5 V ±0.3 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC}+0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
ID read voltage	V_{ID}	11.5		12.5	V	
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP2}			30	mA	CE = V_{IL}, OE = V_{IH}

AC Characteristics

Read and Standby Modes

T_A = 0 to +70°C, V_{CC} = +5 V ±10%, V_{PP} = V_{CC}

Parameter	Symbol	Limits μPD27C256A-12 Min	Max	μPD27C256A-15(1) Min	Max	μPD27C256A-20(1) Min	Max	Unit	Test Conditions(2)
Address to output delay	t_{ACC}		120		150		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		120		150		200	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ low to data output delay	t_{OE}		60		75		75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to data output float delay	t_{DF}		50		60		60	ns	$\overline{CE}$ = V_{IL}
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Notes:

(1) Available in either UV or OTP.

(2) Output load: see figure 1.
Input rise and fall times: 20 ns.
Input pulse levels: 0.45 V to 2.4 V.
Timing measurement reference levels:
Inputs: 0.8 V and 2.0 V
Outputs: 0.8 V and 2.0 V.

9

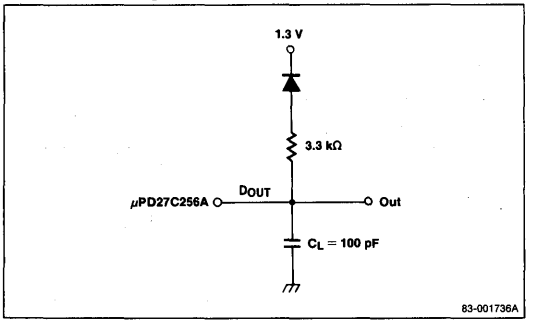
AC Characteristics (cont)

Program, Program Verify, and Program Inhibit Modes
$T_A = 25°C \pm 5°C$, $V_{CC} = +6\ V \pm 0.25\ V$, $V_{PP} = +12.5\ V \pm 0.3\ V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	(Notes 1, 2, 3)
Data setup time	t_{DS}	2			μs	(Notes 1, 2, 3)
Address hold time	t_{AH}	0			μs	(Notes 1, 2, 3)
Data hold time	t_{DH}	2			μs	(Notes 1, 2, 3)
Output enable to output float delay	t_{DF}			130	ns	(Notes 1, 2, 3)
V_{PP} setup time	t_{VPS}	2			μs	(Notes 1, 2, 3)
Program pulse width	t_{PW}	0.95	1	1.05	ms	(Notes 1, 2, 3)
V_{CC} setup time	t_{VCS}	2			μs	
OE setup time	t_{OES}	2			μs	(Notes 1, 2, 3)
Overprogram pulse width	t_{OPW}	0.95		21	ms	
Data valid from OE	t_{OE}			150	ns	

Notes:
(1) Input pulse levels = 0.45 V to 2.4 V.
(2) Input and output timing reference levels = 0.8 V and 2.0 V.
(3) Input rise and fall times = 20 ns.

Figure 1. Loading Conditions Test Circuit



Truth Table

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	Hi-Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	Hi-Z
ID read	V_{IL}	V_{IL}	V_{ID}	V_{CC}	V_{CC}	D_{OUT}

Note:
(1) X can be either V_{IL} or V_{IH}.

Programming Operation

High Speed Programming Mode

Begin programming by erasing all data; this places all bits in the high level (1) state. Enter data by programming a low level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the 8 output pins. Raise V_{CC} to $+6\ V \pm 0.25\ V$; then raise V_{PP} to $+12.5\ V \pm 0.3\ V$. Apply a 1 ms (±5%) program pulse to $\overline{CE}$ as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1 ms pulse to $\overline{CE}$ up to a maximum of 25 times. If the bit is programmed within 25 tries, apply an additional overprogram pulse of (3 × number of tries) ms and input the next address. If the bit is not programmed in 25 tries, reject the device as a program failure.

After all bits are programmed, lower both V_{CC} and V_{PP} to $+5\ V \pm 10\%$ and verify all data again.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C256As connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low level (0) TTL pulse to the $\overline{CE}$ input of the μPD27C256A to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed data to determine that the data was correctly programmed. The program verification can be performed with $\overline{OE}$ at a low level (0). To perform verification on multiple μPD27C256As connected in parallel, with a common $\overline{OE}$ input applied to all devices, first reduce V_{PP} to V_{CC}. Then the normal read mode can be used with a low level (0) applied to the $\overline{CE}$ input of the device to be verified. A high level (1) is applied to the $\overline{CE}$ input of all other devices.

Erasure

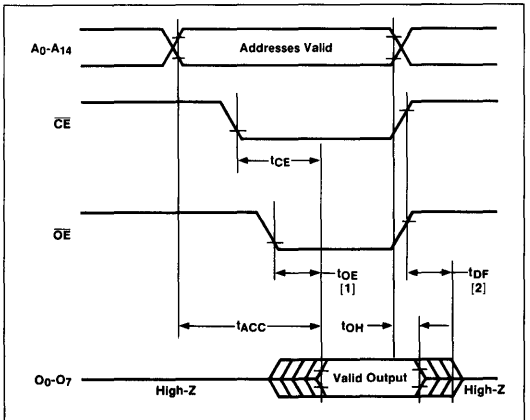
Erase data on the μPD27C256A by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254 nm ultraviolet rays. A lighting level of 15 W-sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity × exposure time).

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C256A within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

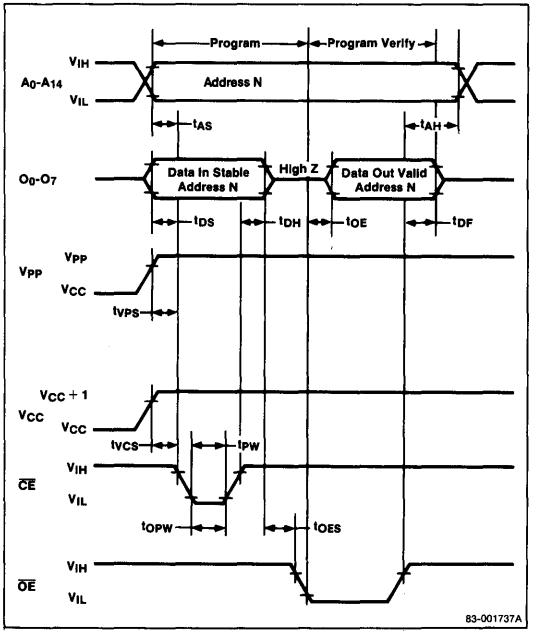
Timing Waveforms

Read Mode



Note:
[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

Program Mode



NEC
NEC Electronics Inc.

μPD27C512
65,536 x 8-BIT
CMOS UV EPROM

PRELIMINARY INFORMATION

Description

The μPD27C512 is a 524,288-bit ultraviolet erasable and electrically programmable ROM using an advanced CMOS process that produces a substantial power saving. The device is organized as 64K words by 8 bits and operates from a single +5 V power supply. All inputs and outputs are TTL-compatible. The device is available in a 28-pin cerdip package with a quartz window.

Features

- ☐ 64K x 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ High speed programming mode
- ☐ Low power dissipation:
  - — 30 mA max (active)
  - — 100 μA max (standby)
- ☐ TTL-compatible inputs and outputs
- ☐ Single +5 V power supply
- ☐ Three-state outputs
- ☐ Advanced CMOS technology
- ☐ 28-pin DIP

Performance Ranges

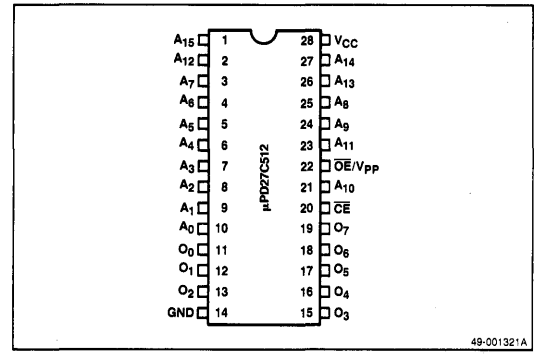
Device	Access Time	Power Supply	
		Active	Standby
μPD27C512D-15	150 ns	30 mA	100 μA
μPD27C512D-20	200 ns	30 mA	100 μA
μPD27C512D-25	250 ns	30 mA	100 μA

Absolute Maximum Ratings

Operating temperature, T_{OPR}	−10 to +80° C
Storage temperature, T_{STG}	−65 to +125 C
Output voltage, V_O	−0.6 to +7 V
Input voltage, V_I	−0.6 to +7 V
Input voltage, A_9	−0.6 to +13.5 V
Supply voltage, V_{CC}	−0.6 to +7 V
Supply voltage, V_{PP}	−0.6 to +13.5 V

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

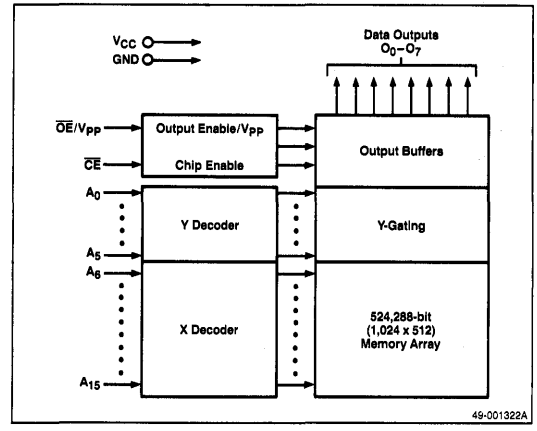
Pin Configuration



Pin Identification

No.	Symbol	Function
1-10, 21, 23-27	A_0-A_{15}	Address inputs
11-13, 15-19	O_0-O_7	Data outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
22	$\overline{OE}/V_{PP}$	Output enable/program voltage
28	V_{CC}	Power supply

Block Diagram



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Mode Selection

Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	+5 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	+5 V	High-Z
Standby	V_{IH}	X	+5 V	High-Z
Program	V_{IL}	V_{PP}	+6 V	D_{IN}
Program verify	V_{IL}	V_{IL}	+6 V	D_{OUT}
Program inhibit	V_{IH}	X	+6 V	High-Z

Note:

X can be V_{IL} or V_{IH}.

Capacitance

$T_A = 25°C$, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN1}		4	6	pF	$V_I = 0$ V
	C_{IN2}		12	20	pF	$\overline{OE}/V_{PP}$, $V_I = 0$ V
Output capacitance	C_{OUT}		8	12	pF	$V_O = 0$ V

DC Characteristics

Read and Standby Modes

$T_A = 0$ to +70°C, $V_{CC} = 5$ V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH}	2.0		$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	−0.3		0.8	V	
Output high voltage	V_{OH1}	2.4			V	$I_{OH} = -400$ μA
	V_{OH2}	$V_{CC} - 0.7$			V	$I_{OH} = -100$ μA
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output leakage current	I_{LO}			10	μA	$V_O = 0$ to V_{CC}, $\overline{OE} = V_{IH}$
Input leakage current	I_{LI}			10	μA	$V_I = 0$ to V_{CC}
V_{CC} current	I_{CCA1}			30	mA	$\overline{CE} = V_{IL}$, $V_I = V_{IH}$
(active)	I_{CCA2}			30	mA	f = 5 MHz, $I_{OUT} = 0$ mA
V_{CC} current	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
(standby)	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$, $V_I = 0$ to V_{CC}

Programming Modes

$T_A = 25 \pm 5°C$, $V_{CC} = 6.0$ V ± .25 V, $V_{PP} = 12.5$ V ±0.3 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH}	2.0		$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	$V_I = V_{IL}$ or V_{IH}
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -400$ μA
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
V_{PP} current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = V_{IH}$
V_{CC} current	I_{CC}			30	mA	

AC Characteristics

Read and Standby Modes

$T_A = 0$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Limits μPD27C512-15 Min	Limits μPD27C512-15 Max	Limits μPD27C512-20 Min	Limits μPD27C512-20 Max	Limits μPD27C512-25 Min	Limits μPD27C512-25 Max	Unit	Test Conditions
Address to output delay	t_{ACC}		150		200		250	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		150		200		250	ns	$\overline{OE}/V_{PP} = V_{IL}$
$\overline{OE}/V_{PP}$ to output delay	t_{OE}		75		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}/V_{PP}$ high to output float	t_{DF}	0	60	0	60	0	85	ns	$\overline{CE} = V_{IL}$
Output hold from address, $\overline{CE}$, or $\overline{OE}$, whichever transition occurs first	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

Note:

(1) Output load: see figure 1. Input rise and fall times ≤ 20 ns. Input pulse levels: 0.45 V and 2.4 V. Timing measurement reference levels:
Inputs = 0.8 V and 2.0 V
Outputs = 0.8 V and 2.0 V

Programming Modes

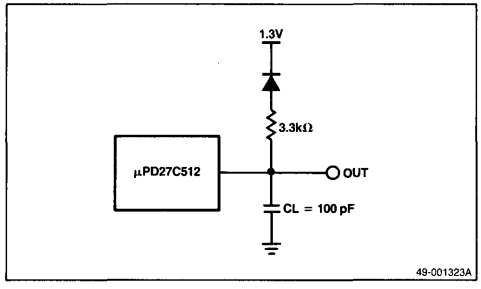
$T_A = 25 \pm 5°C$, $V_{CC} = 6.0\ V \pm .25\ V$, $V_{PP} = 12.5\ V \pm 0.3\ V$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{CE}$ to output float time	t_{DF}	0		130	ns	
V_{CC} setup time	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram pulse width	t_{OPW}	2.85		78.75	ms	
$\overline{CE}$ to output delay	t_{DV}			1	μs	$\overline{OE}/V_{PP} = V_{IL}$
$\overline{OE}/V_{PP}$ hold time	t_{OEH}	2			μs	(Note 1)
$\overline{OE}/V_{PP}$ recovery time	t_{VR}	2			μs	(Note 1)
$\overline{OE}/V_{PP}$ rise time	t_{PRT}	50			ns	

Note:

(1) $t_{OEH} + t_{VR} \geq 50\ \mu s$

Figure 1. Loading Conditions Test Circuit



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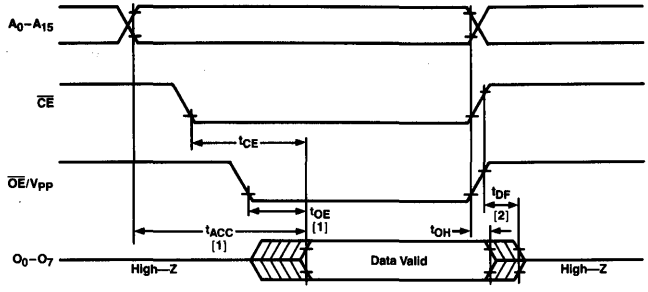
Timing Waveforms

Read Mode



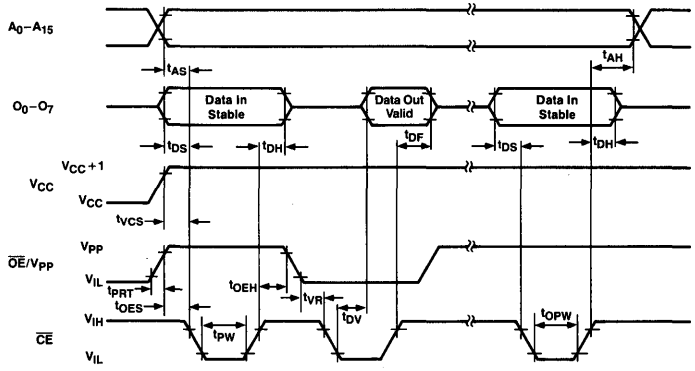
Note:

[1] $\overline{OE}/V_{PP}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ for read cycles without affecting t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first.

49-001324B

Programming Mode



Note:

[1] V_{CC} must be applied before or simultaneously with $\overline{OE}/V_{PP}$ and removed after or simultaneously with $\overline{OE}/V_{PP}$.

[2] V_{PP} must not be greater than +13 V, including overshoot.

49-001325B

Programming Operation

High-speed Programming Mode

Begin programming by erasing all data; this places all bits in the high level (1) state. Enter data by programming a low level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the 8 output pins. Raise V_{CC} to +6 V ± .25 V; then raise $\overline{OE}/V_{PP}$ to +12.5 V ± 0.3 V. Apply a 1 ms (± 5%) program pulse to CE as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1 ms pulse to $\overline{CE}$ up to a maximum of 25 times. If the bit is programmed within 25 tries, apply an additional overprogram pulse of (3 x number of tries) ms and input the next address. If the bit is not programmed in 25 tries, reject the device as a program failure.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C512s connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}/V_{PP}$) may be common. Program individual devices by applying a low level (0) TTL pulse to the $\overline{CE}$ input of the μPD27C512 to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed bits to determine that the data was correctly programmed. The program verification can be performed with $\overline{CE}$ and $\overline{OE}/V_{PP}$ at low levels (0).

Erasure

Erase data on the μPD27C512 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254 nm ultraviolet rays. A lighting level of 15 W-sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity x exposure time).

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C512 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

NEC
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μPD27C1024
65,536 x 16-BIT CMOS UV EPROM

PRELIMINARY INFORMATION

Description

The μPD27C1024 is a 1,048,576-bit ultraviolet erasable and electrically programmable ROM using an advanced CMOS process that produces a substantial power saving. The device is organized as 64K words by 16 bits and operates from a single +5 V ± 10% power supply. All inputs and outputs are TTL-compatible. The device is available in a 40-pin cerdip package with a quartz window.

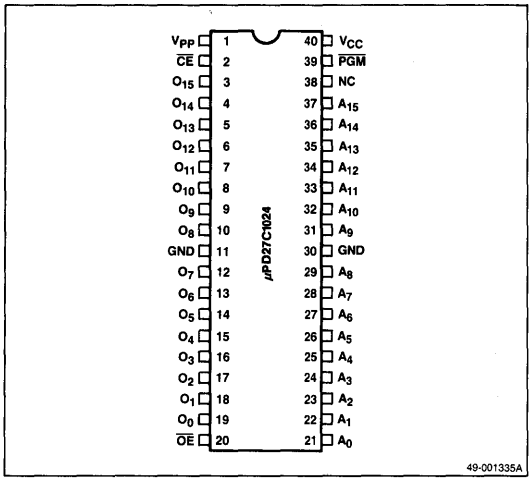
Features

- ☐ 64K x 16-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Very high speed programming mode
- ☐ Low power dissipation:
  - — 50 mA max (active)
  - — 100 μA max (standby)
- ☐ TTL-compatible inputs and outputs
- ☐ Single +5 V ± 10% power supply
- ☐ Three-state outputs
- ☐ Advanced CMOS technology
- ☐ 40-pin DIP

Performance Ranges

Device	Access Time	Power Supply (max)	
		Active	Standby
μPD27C1024D-15	150 ns	50 mA	100 μA
μPD27C1024D-20	200 ns	50 mA	100 μA
μPD27C1024D-25	250 ns	50 mA	100 μA

Pin Configuration



Pin Identification

No.	Symbol	Function
1	V_{PP}	Program voltage
2	$\overline{CE}$	Chip enable
3-10, 12-19	O_0-O_{15}	Data outputs
11, 30	GND	Ground
20	$\overline{OE}$	Output enable
21-29, 31-37	A_0-A_{15}	Address inputs
38	NC	No connection
39	$\overline{PGM}$	Program
40	V_{CC}	Power supply

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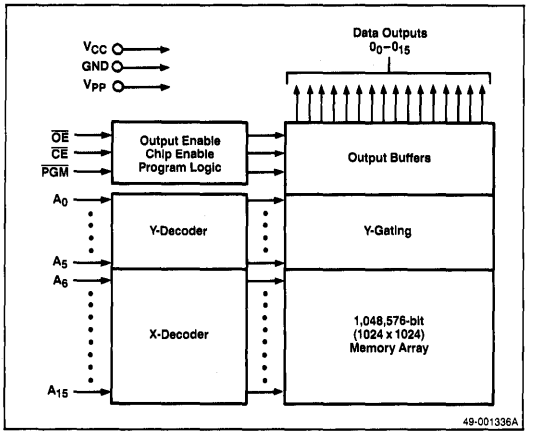
Block Diagram



Mode Selection

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5 V	+5 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	+5 V	+5 V	High-Z
Standby	V_{IH}	X	X	+5 V	+5 V	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6 V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6 V	D_{OUT}
Program inhibit	V_{IH}	X	X	+12.5 V	+6 V	High-Z

Note:

X can be V_{IL} or V_{IH}.

Absolute Maximum Ratings

Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C
Output voltage, V_O	−0.6 to +7 V
Input voltage, V_I	−0.6 to +7 V
Input voltage, A_9	−0.6 to +13.5 V
Supply voltage, V_{CC}	−0.6 to +7 V
Supply voltage, V_{PP}	−0.6 to +13.5 V

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}		4	6	pF	$V_I = 0$ V
Output capacitance	C_{OUT}		8	12	pF	$V_O = 0$ V

DC Characteristics

Read and Standby Modes

$T_A = 0$ to +70°C, $V_{CC} = 5$ V ± 10%, $V_{PP} = V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH}	2.0		$V_{CC}+0.3$	V	
Input low voltage	V_{IL}	−0.3		0.8	V	
Output high voltage	V_{OH1}	2.4			V	$I_{OH} = -400\ \mu A$
	V_{OH2}	$V_{CC}-0.7$			V	$I_{OH} = -100\ \mu A$
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output leakage current	I_{LO}			10	μA	$V_O = 0$ to V_{CC}, $\overline{OE} = V_{IH}$
Input leakage current	I_{LI}			10	μA	$V_I = 0$ to V_{CC}
V_{PP} current	I_{PP}		1	100	μA	$V_{PP} = V_{CC}$
V_{CC} current (active)	I_{CCA1}			30	mA	$\overline{CE} = V_{IL}$, $V_I = V_{IH}$
	I_{CCA2}			50	mA	f = 5 MHz, $I_{OUT} = 0$ mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$, $V_I = 0$ to V_{CC}

DC Characteristics (cont)

Programming Modes

$T_A = 25°C \pm 5°C$, $V_{CC} = 6.0\ V \pm .25\ V$, $V_{PP} = 12.5\ V \pm 0.3\ V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH}	2.0		$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	$V_I = V_{IL}$ or V_{IH}
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 2.1\ mA$
V_{PP} current	I_{PP}			100	μA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC} current	I_{CC}			30	mA	

AC Characteristics

Read and Standby Modes

$T_A = 0$ to $+70°C$, $V_{CC} = 5\ V \pm 10\%$, $V_{PP} = V_{CC}$

Parameter	Symbol	Limits μPD27C1024-15 Min	Max	μPD27C1024-20 Min	Max	μPD27C1024-25 Min	Max	Unit	Test Conditions
Address to output delay	t_{ACC}		150		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		150		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}		75		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float	t_{DF}	0	60	0	60	0	85	ns	$\overline{CE} = V_{IL}$
Output hold from address, $\overline{CE}$, or $\overline{OE}$, whichever transition occurs first	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note:

(1) Output load: see figure 1. Input rise and fall times ≤ 20 ns. Input pulse levels: 0.45 V and 2.4 V. Timing measurement reference levels:
Inputs = 0.8 V and 2.0 V
Outputs = 0.8 V and 2.0 V

Programming Modes

$T_A = 25°C \pm 5°C$, $V_{CC} = 6.0\ V \pm .25\ V$, $V_{PP} = 12.5\ V \pm 0.3\ V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	.095	0.1	0.105	ms	
Overprogram pulse width	t_{OPW}	0.38		0.42	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

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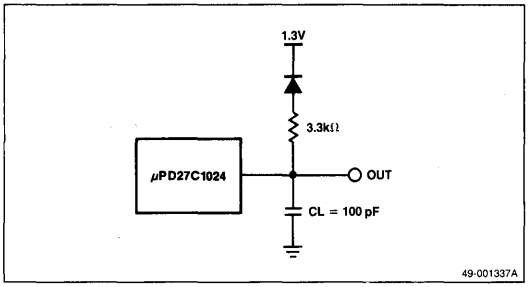
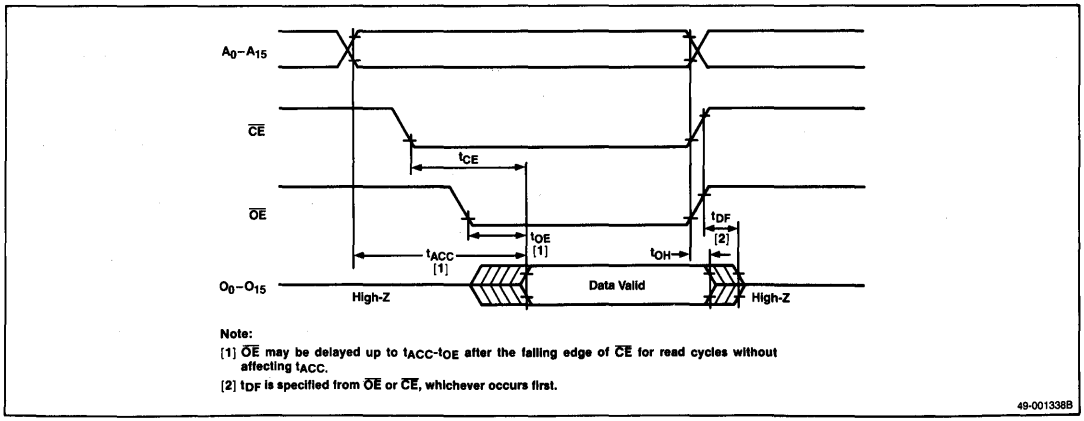
Figure 1. Loading Conditions Test Circuit



Timing Waveforms

Read Mode



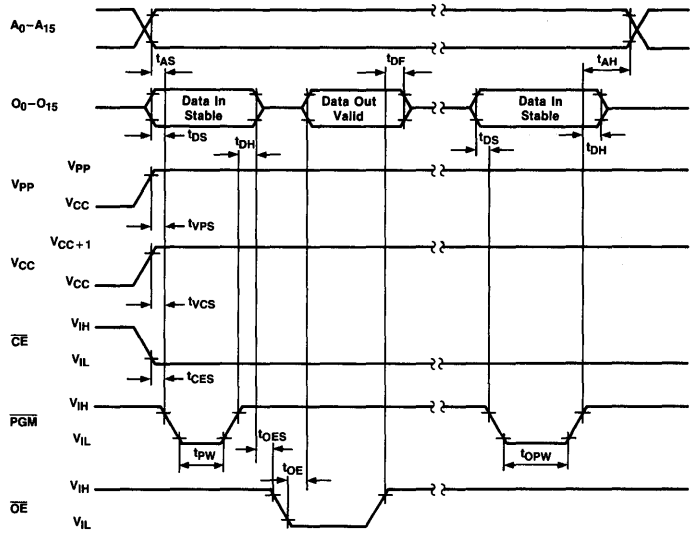
Note:

[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read cycles without affecting t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Timing Waveforms (cont)

Programming Mode



Note:

[1] V_{CC} must be applied before or simultaneously with V_{PP} and removed after or simultaneously with V_{PP}.

[2] V_{PP} must not be greater than +13 V, including overshoot.

49-001339B

Programming Operation

Very High-speed Programming Mode

Begin programming by erasing all data; this places all bits in the high level (1) state. Enter data by programming a low level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the 16 output pins. Raise V_{CC} to +6 V ± .25 V; then raise V_{PP} to +12.5 V ± 0.3 V. Apply a 0.1 ms (±5%) program pulse to $\overline{PGM}$ as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 0.1 ms pulse to $\overline{PGM}$ up to a maximum of 10 times. If the bit is programmed within 10 tries, apply an additional overprogram pulse of (0.4 x number of tries) ms. If the bit is not programmed in 10 tries, apply another pulse of 4 ms. If the bit is not programmed at this stage, reject the device as a program failure. If the bit is programmed, input the next address and repeat the programming procedure until all addresses are programmed.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C1024s connected in parallel. All like inputs (except $\overline{CE}$ or $\overline{PGM}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low level (0) TTL pulse to the $\overline{CE}$ input of the μPD27C1024 to be programmed. Applying a high level (1) to the $\overline{CE}$ or $\overline{PGM}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed bits to determine that the data was correctly programmed. The program verification can be performed with $\overline{CE}$ and $\overline{OE}$ at low levels (0) and $\overline{PGM}$ at a high level (1).

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Erasure

Erase data on the μPD27C1024 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254 nm ultraviolet rays. A lighting level of 15 W-sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity x exposure time).

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C1024 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

NEC

MASK-PROGRAMMABLE ROMs

10

Section 10 — Mask-Programmable ROMs

NEC
NEC Electronics Inc.

μPD2364A
8,192 x 8-BIT MASK-PROGRAMMABLE NMOS ROM

Revision 1

Description

The μPD2364A is a 65,536-bit Read-only Memory utilizing NMOS silicon gate technology. The device is static in operation, organized as 8,192 words by 8 bits and operates from a single +5V ± 10% power supply. The μPD2364A has three-state outputs. All inputs and outputs are fully TTL-compatible. The Output Enable/Chip Enable pin is mask-programmable and can be specified by selecting 1, 0 or don't-care data and standby mode. The μPD2364A is available in a plastic (μPD2364AC) 24-pin DIP. Pinout is compatible with Mostek MK36000®

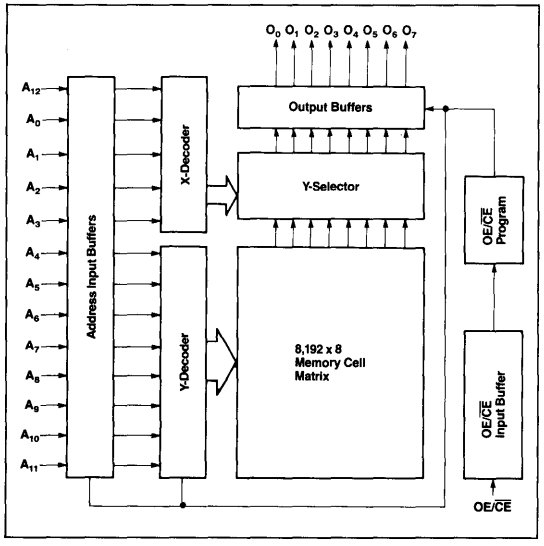
® = Registered trademark.

Features

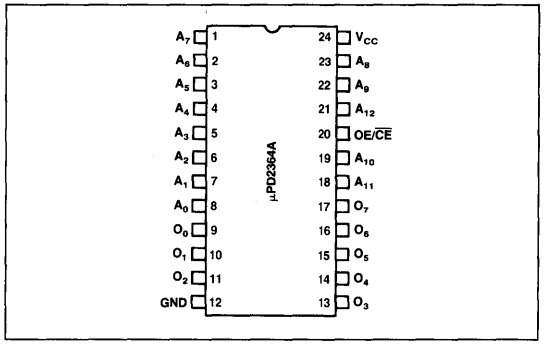
- ☐ 8,192-word by 8-bit organization
- ☐ I/O TTL-compatible
- ☐ Three-state outputs
- ☐ Single +5V ± 10% power supply
- ☐ Mask-programmable OE/$\overline{CE}$
- ☐ 24-pin plastic DIP
- ☐ 2 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD2364A	200ns	70mA	15mA
μPD2364A-1	150ns	70mA	15mA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Symbol	Description
1–8, 18–19, 21–23	A_0–A_{12}	Address Inputs
9–11, 13–17	O_0–O_7	Three-state Data Outputs
12	GND	Ground
20	OE/$\overline{CE}$	Mask-programmable Output Enable/Chip Enable ①
24	V_{CC}	+5V ± 10% Power Supply

Note: ① Pin 20 may be mask-programmed as an OE or a $\overline{CE}$ function. If it is defined as OE, it may be specified as active high (1), active low (0), or don't-care (X). If it is defined as $\overline{CE}$, it will be active low (0) and a high (1) for standby mode.

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Absolute Maximum Ratings*

Supply Voltage, V_{CC}	−0.5V to +7V
Input Voltage, V_I	−0.5V to +7V
Output Voltage, V_O	−0.5V to +7V
Operating Temperature, T_{OPR}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = −10°C to +70°C; V_{CC} = +5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10	pF	f = 1MHz
Output Capacitance	C_O			15	pF	f = 1MHz

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.0		V_{CC} + 1.0	V	
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +2.1mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+10	μA	$V_O = V_{CC}$ (chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (chip deselected)
Power Supply Current	I_{CC2}		40	70	mA	$\overline{CE} = V_{IL}$
	I_{CC1} ①		8	15	mA	$\overline{CE} = V_{IH}$ (standby mode)

Note: ① OE/$\overline{CE}$ = $\overline{CE}$.

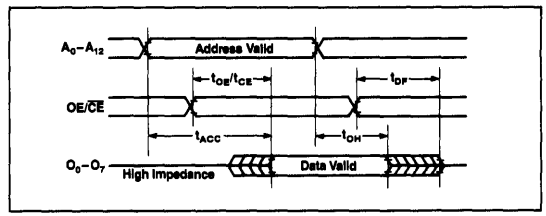
AC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5V ± 10%

Parameter	Symbol	Limits μPD2364A Min	μPD2364A Max	μPD2364A-1 Min	μPD2364A-1 Max	Unit	Test Conditions
Access Time	t_{ACC}		200		150	ns	Input Voltage: t_R, t_F = 20ns Timing Reference Levels: Input and Output = 0.8V and 2.0V Load = 1 TTL + 100pF
Chip Enable Access Time	t_{CE} ①		200		150	ns	
OE Output On Time	t_{OE} ②	10	100	10	100	ns	
Output Hold Time	t_{OH}	0		0		ns	
Output Disable Time	t_{DF}	0	90	0	90	ns	

Notes: ① OE/$\overline{CE}$ = $\overline{CE}$.
② OE/$\overline{CE}$ = $\overline{OE}$.

Timing Waveform



μPD2364E
8,192 x 8-BIT MASK-PROGRAMMABLE NMOS ROM

Revision 2

Description

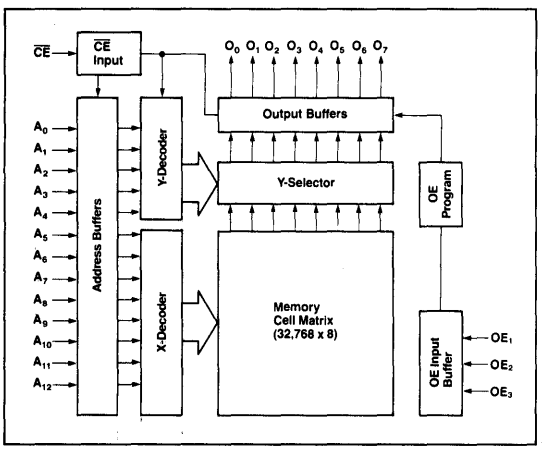
The μPD2364E is a 65,536-bit Read-only Memory utilizing NMOS silicon gate technology. The device is static in operation, organized as 8,192 words by 8 bits and operates from a single +5V power supply. The device has three-state outputs and all inputs and outputs are fully TTL-compatible. The chip select pins are mask-programmable and can be specified by selecting 1, 0, and Don't-care data. Pinout is compatible with 2764 EPROMs.

Features

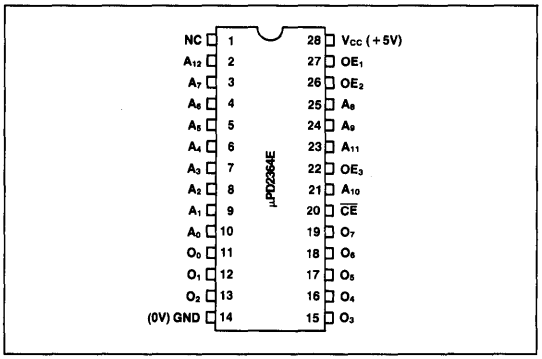
- ☐ All inputs and outputs are fully TTL-compatible
- ☐ Three-state outputs for direct bus compatibility
- ☐ Single +5V ± 5% power supply
- ☐ Three mask-programmable chip selects
- ☐ 2 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD2364E	250ns	80mA	20mA
μPD2364E-1	200ns	80mA	20mA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Function
1	NC	No Connection.
2–10, 21, 23–25	A_0–A_{12}	Address Inputs.
11–13, 15–19	O_0–O_7	Three-state Data Outputs.
14	GND	Ground.
20	$\overline{CE}$	Chip Enable.
22, 26–27	OE_1–OE_3	Mask-programmable Chip Selects.
28	V_{CC}	Single +5V Power Supply.

10

Absolute Maximum Ratings*

Supply Voltage, V_{CC}	−0.5V to +7V
Input Voltage, V_I	−0.5V to +7V
Output Voltage, V_O	−0.5V to +7V
Operating Temperature, T_{OPR}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = −10°C to +70°C

		Limits							
		μPD2364E			μPD2364E-1				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10			10	pF	f = 1MHz
Output Capacitance	C_O			15			15	pF	f = 1MHz

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5V ± 5%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.1		V_{CC} + 1.0	V	
Input Low Voltage	V_{IL}	−0.5		+0.7	V	
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +2.1mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+10	μA	$V_O = V_{CC}$, chip deselected
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V, chip deselected
Supply Voltage Current	I_{CC1}		45	80	mA	CE = V_{IL}
Supply Voltage Current	I_{CC2}		12	20	mA	CE = V_{IH}, standby mode

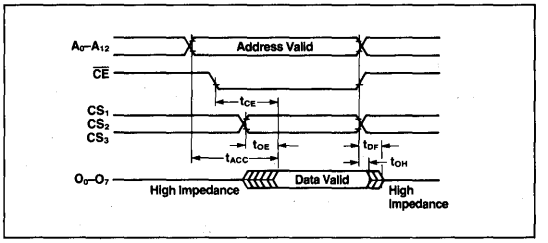
AC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5 ± 5%

		Limits							
		μPD2364E			μPD2364E-1				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions①
Access Time	t_{ACC}			250			200	ns	
Chip Enable Access Time	t_{CE}			250			200	ns	
OE_1 to OE_3 Output On Time	t_{OE}	10		110	10		100	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		100	0		90	ns	

Notes: ① Input rise and fall times (t_R, t_F): 20ns
Timing reference levels: Input and Output voltages = 0.8V and 2.0V
Load = 1 TTL + 100 pF

Timing Waveform



Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid address and the corresponding valid data out.

Output Hold Delay, t_{OH}

Output hold delay is the minimum time after an address change that the previous data remains valid.

Chip Enable Access Time, t_{CE}

The maximum time between application of a valid chip enable input and the corresponding valid outputs.

Output Enable Time, t_{OE}

Output enable time is the maximum delay between chip selects becoming true and output data becoming valid.

Output Disable Time, t_{DF}

Output disable time is the delay between chip selects or chip enable becoming false and output stages going to the high impedance state. t_{DF} is specified as CE or OE, whichever comes first.

Custom Programming Instructions

Bit pattern submittal options

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 2764 EPROM
2. Two programmed 2732 EPROMs

Bit pattern verification

For customer verification of the submitted bit pattern, several alternatives are also available. The following are those found to be most expeditious.

Customer Pattern Submitted Via	Verification Routine
1. One programmed 2764 EPROM	Customer sends NEC one additional erased 2764. NEC programs the spare 2764 with the data from the programmed 2764, and returns it to the customer for verification.
2. Two programmed 2732 EPROMs	Customer sends NEC two additional erased 2732s. NEC programs the spare 2732s with the data from the programmed EPROMs and returns them to the customer for verification.

μPD23128E
16,384 x 8-BIT MASK-PROGRAMMABLE NMOS ROM

Revision 1

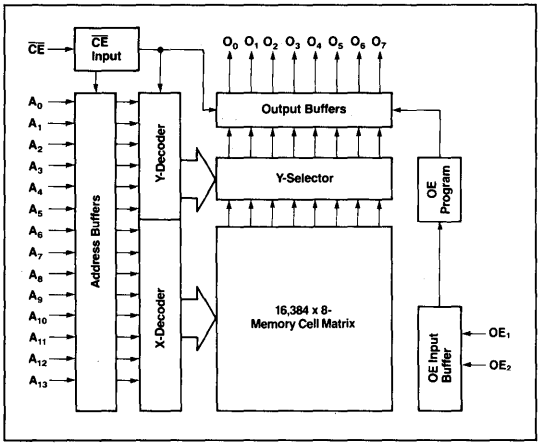
Description

The μPD23128E is a fully static 131,072-bit Read-only Memory, utilizing MOS N-channel silicon gate technology. The device is organized as 16,384 words by 8 bits and operates from a single +5V power supply. All inputs and outputs are fully TTL-compatible. The device has two programmable output enables that allow memory expansion without the use of external logic. Programming is accomplished during the fabrication process. Pinout is compatible with 27128 EPROMs.

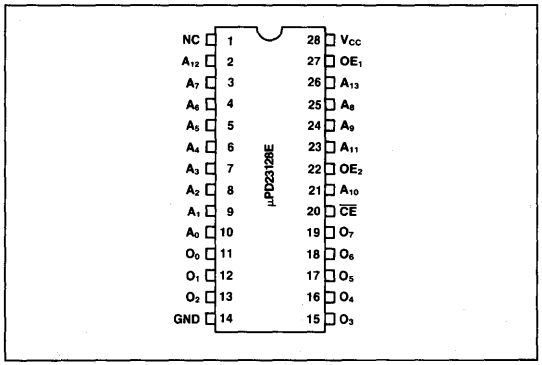
Features

- ☐ Fast access time: 250ns max
- ☐ All inputs and outputs fully TTL-compatible
- ☐ Three-state outputs for direct bus compatibility
- ☐ Single +5V ± 10% power supply
- ☐ Fully static operation
- ☐ Two programmable output enables for memory expansion
- ☐ Low-power standby mode

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	NC	No Connection.
2–10, 21, 23–26	A_0–A_{13}	Address Inputs.
11–13, 15–19	O_0–O_7	Three-state Data Outputs.
14	GND	Ground.
20	$\overline{CE}$	Chip Enable.
22, 27	OE_1, OE_2	Output Enables.
28	V_{CC}	Single +5V Power Supply.

10

Absolute Maximum Ratings*

Supply Voltage, V_{CC}	−0.5V to +7V
Input Voltage, V_I	−0.5V to +7V
Output Voltage, V_O	−0.5V to +7V
Operating Temperature, T_{OPT}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5V ± 10%

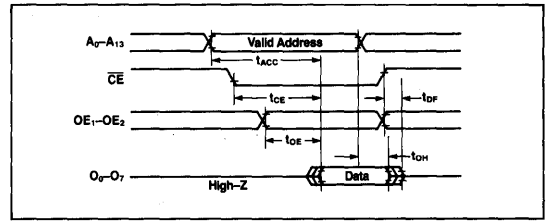
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.0		V_{CC} +1.0	V	
Input Low Voltage	V_{IL}	−0.5		+0.7	V	
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +3.2mA
Input Leakage High Current	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Low Current	I_{LIL}			−10	μA	V_I = 0V
Output Leakage High Current	I_{LOH}			+10	μA	$V_O = V_{CC}$, Chip deselected
Output Leakage Low Current	I_{LOL}			−10	μA	V_O = 0V, Chip deselected
Power Supply Current	I_{CC1}		50	90	mA	$\overline{CE} = V_{IL}$
	I_{CC2}		13	25	mA	$\overline{CE} = V_{IH}$, Standby mode

AC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address to Output Access Time	t_{ACC}			250	ns	
Chip Enable Access Time	t_{CE}			250	ns	
Output Enable Access Time	t_{OE}	10		100	ns	
Output Hold Time	t_{OH}	0			ns	
Output Disable Time	t_{DF}	0		100	ns	

Timing Waveform



Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid address and the corresponding valid data out.

Chip Enable Access Time, t_{CE}

The minimum time between application of a valid chip enable input and the corresponding valid outputs.

Output Enable Access Time, t_{OE}

The minimum time between application of valid output enable inputs and the corresponding valid outputs.

Output Hold Time, t_{OH}

Output hold time is the minimum time after an address change that the previous data remains valid.

Output Disable Time, t_{DF}

Output disable time is the delay between chip selects becoming false and output stages going to the high impedance state.

μPD23C64E
8,192 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Revision 1

Description

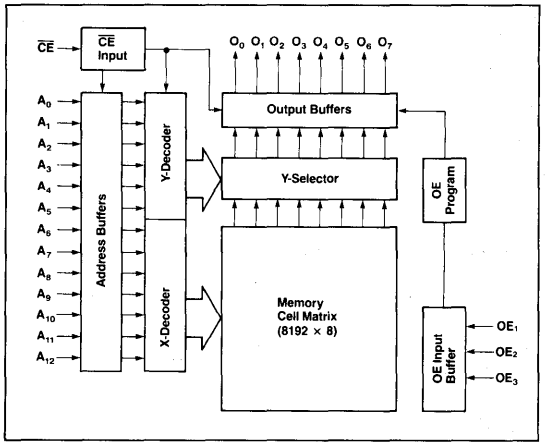
The μPD23C64E is a 65,536-bit Read-only Memory utilizing CMOS silicon gate technology. The device is static in operation, organized as 8,192 words by 8 bits andhas three-state outputs. All inputs and outputs are fully TTL-compatible. The output enable pins are mask-programmable and can be specified by selecting 1, 0, or don't-care data (see Table 1). The μPD23C64E is packaged in a plastic (μPD23C64EC) 28-pin DIP. Pinout is compatible with μPD2764 EPROMs.

Features

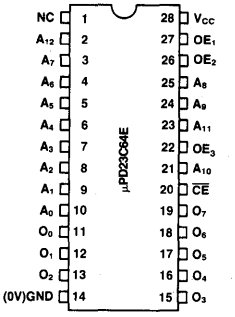
- ☐ 8,192-word x 8-bit organization
- ☐ I/O TTL-compatible
- ☐ Three-state outputs
- ☐ Single +2.5V to +6.0V power supply
- ☐ CMOS process technology
- ☐ Fully static operation
- ☐ Pinout compatible with μPD2764 EPROMs
- ☐ Plastic 28-pin DIP available
- ☐ 2 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD23C64E	200ns	25mA	30μA
μPD23C64E-1	150ns	30mA	30μA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Description
1	NC	No Connection
2–10, 21, 23–25	A_0–A_{12}	Address Inputs
11–13, 15–19	O_0–O_7	Data Outputs
14	GND	Ground
20	$\overline{CE}$	Chip Enable
22, 26–27	OE_1–OE_3	Output Enables ①
28	V_{CC}	Single +2.5V to +6.0V power supply

Note: ① The active levels of OE_1, OE_2 and OE_3 input can be specified by the values given in Table 1.

Table 1. OE_1–OE_3 Active Level Specifications

OE_1	OE_2	OE_3
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1
X	X	X

Note: ① X = Don't-care.

10

Absolute Maximum Ratings*

Supply Voltage, V_{CC}	−0.3V to +7V
Input Voltage, V_I	−0.3V to V_{CC} +0.3V
Output Voltage, V_O	−0.3V to V_{CC} +0.3V
Operating Temperature, T_{OPR}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = −10°C to +70°C; V_{CC} = +2.5V to 6.0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10	pF	f = 1MHz
Output Capacitance	C_O			15	pF	f = 1MHz

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.1		V_{CC} +0.3		
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = +3.2mA
Input Leakage Current High	I_{LIH}			10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			10	μA	$V_O = V_{CC}$ (chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (chip deselected)
Power Supply Current	I_{CC1}		13	25	mA	$\overline{CE} = V_{IL}$ 23C64E
			16	30	mA	23C64E-1
	I_{CC2}		0.2	1.5	mA	$\overline{CE} = V_{IH}$ (standby mode)
	I_{CC3}		0.2	30	μA	$\overline{CE} = V_{CC}$ −0.2V (standby mode)

DC Characteristics (Cont.)

T_A = −10°C to +70°C; V_{CC} = +2.5V + 6.0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	0.7 × V_{CC}		V_{CC} + 0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.18 × V_{CC}	V	
Output High Voltage	V_{OH}	0.75 × V_{CC}			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = +400μA
Input Leakage Current High	I_{LIH}			10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			10	μA	$V_O = V_{CC}$ (chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (chip deselected)
Power Supply Current	I_{CC1}		3	10	mA	V_{CC} = +3.0V ± 10% 23C64E
			7	18	mA	V_{CC} = +5.0V ± 10%
			3.5	10	mA	V_{CC} = +3.0V ± 10% 23C64E-1
			8	20	mA	V_{CC} = +5.0V ± 10%
	I_{CC3}		0.1	30	μA	V_{CC} = +3.0V ± 10% $\overline{CE} = V_{CC}$ −0.2V (standby mode)
			0.2	30	μA	V_{CC} = +5.0V ± 10%

AC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5.0V ± 10%

Parameter	Symbol	Limits 23C64E Min	Typ	Max	23C64E-1 Min	Typ	Max	Unit	Test Conditions①
Access Time	t_{ACC}			200			150	ns	
Chip Enable Access Time	t_{CE}			200			150	ns	
Output Enable Access Time	t_{OE}	10		100	10		100	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		90	0		90	ns	

Note: ① Input voltage, t_R, t_F = 20ns;
Input and output timing reference levels = 0.8V and 2.0V;
Load = 1 TTL + 100pF.

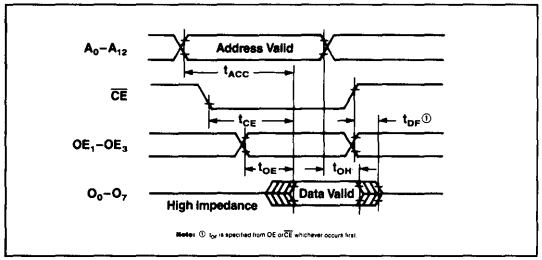
AC Characteristics (Cont.)

T_A = −10°C to +70°C; V_{CC} = +2.5V to +6.0V

Parameter	Symbol	Limits 23C64E Min	Typ	Max	23C64E-1 Min	Typ	Max	Unit	Test Conditions①
Access Time	t_{ACC}			600			450	ns	
Chip Enable Access Time	t_{CE}			600			450	ns	
Output Enable Access Time	t_{OE}			300			300	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		250	0		250	ns	

Note: ① Input and output voltage timing reference levels = $0.18V_{CC}$ and $0.7V_{CC}$;
Load = 150pF.

Timing Waveform



Note: ① t_{DF} is specified from OE or $\overline{CE}$ whichever occurs first.

Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid address and the corresponding valid data out.

Chip Enable Access Time, t_{CE}

The minimum time between application of a valid chip enable input and the corresponding valid outputs.

Output Enable Access Time, t_{OE}

The minimum time between application of a valid output enable input and the corresponding valid outputs.

Output Hold Delay, t_{OH}

Output hold delay is the minimum time after an address change that the previous data remains valid.

Output Disable Time, t_{DF}

Output disable time is the delay between chip selects becoming false and output stages going to the high impedance state.

10

NEC
NEC Electronics Inc.

μPD23C128E
16,384 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Revision 1

Description

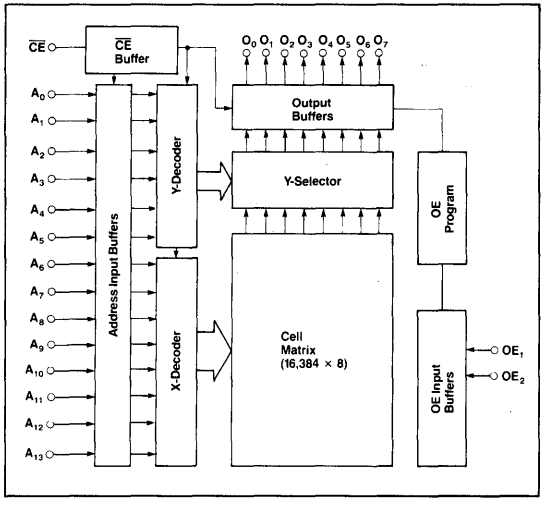
The μPD23C128E is a 131,072-bit Read-only Memory utilizing CMOS silicon gate technology. The device is static in operation, organized as 16,384 words by 8 bits, and has three-state outputs. All inputs and outputs are fully TTL-compatible. The output enable pins are mask-programmable and can be specified by selecting 1, 0, or Don't-care data (see Table 1). The μPD23C128E is packaged in a plastic (μPD23C128EC) 28-pin DIP. Pinout is compatible with μPD27128 EPROMs.

Features

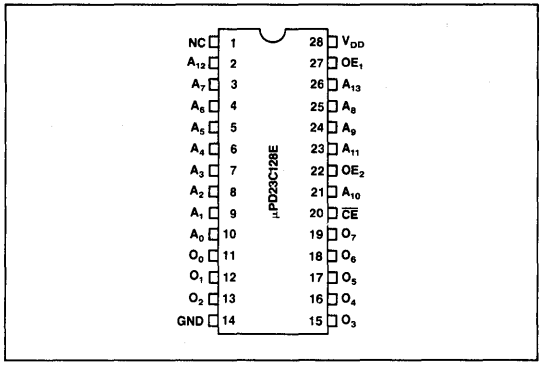
- ☐ 16,384-word × 8-bit organization
- ☐ I/O TTL-compatible
- ☐ Three-state outputs
- ☐ Single +2.5V to +6.0V power supply
- ☐ Plastic 28-pin DIP
- ☐ 2 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD23C128E	200ns	25mA	30μA
μPD23C128E-1	150ns	30mA	30μA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Description
1	NC	No Connection
2–10, 21, 23–26	A_0–A_{13}	Address Inputs
11–13, 15–19	O_0–O_7	Data Outputs
14	GND	Ground
20	$\overline{CE}$	Chip Enable
22, 27	OE_2, OE_1 ①	Output Enables
28	V_{DD}	+2.5V to +6.0V Power Supply

Note: ① Active level inputs are specified in Table 1.

Table 1. OE Input Active Level Specifications

OE_1	OE_2
0	0
1	0
0	1
1	1
x	x

Note: x = Don't care.

Absolute Maximum Ratings*

Operating Temperature, T_{OPR}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C
Supply Voltage, V_{DD}	−0.3V to +7V
Input Voltage, V_I	−0.3V to V_{DD} +0.3V
Output Voltage, V_O	−0.3V to V_{DD} +0.3V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Capacitance

T_A = −10°C to +70°C; V_{CC} = +2.5V to +6.0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10	pF	f = 1MHz
Output Capacitance	C_O			15	pF	f = 1MHz

DC Characteristics

T_A = −10°C to +70°C; V_{DD} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.2		V_{DD}+0.3		
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = +3.2mA
Input Leakage Current High	I_{LIH}			10	μA	$V_I = V_{DD}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			10	μA	$V_O = V_{DD}$ (Chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (Chip deselected)
Power Supply Current	I_{DD1}		13	25	mA	$\overline{CE} = V_{IL}$ μPD23C128E
			16	30	mA	μPD23C128E-1
	I_{DD2}		0.2	1.5	mA	$\overline{CE} = V_{IH}$ (Standby mode)
	I_{DD3}		0.2	30	μA	$\overline{CE} = V_{DD}$ − 0.2V (Standby mode)

T_A = −10°C to +70°C; V_{DD} = +2.5V to +6.0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	0.7 × V_{DD}		V_{DD} +0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.18 × V_{DD}	V	
Output High Voltage	V_{OH}	0.75 × V_{DD}			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = +400μA
Input Leakage Current High	I_{LIH}			10	μA	$V_I = V_{DD}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			10	μA	$V_O = V_{DD}$ (Chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (Chip deselected)
Power Supply Current	I_{DD1}		3	10	mA	V_{DD} = +3.0V ± 10% μPD23C128E
			7	18	mA	V_{DD} = +5.0V ± 10%
			3.5	10	mA	V_{DD} = +3.0 ± 10% μPD23C128E-1
			8	20	mA	V_{DD} = +5.0V ± 10%
	I_{DD3}		0.1	30	μA	V_{DD} = +3.0V ± 10% $\overline{CE} = V_{DD}$ − 0.2V
			0.2	30	μA	V_{DD} = +5.0V ± 10% (Standby mode)

AC Characteristics

T_A = −10°C to +70°C; V_{DD} = +5.0V ± 10%

Parameter	Symbol	Limits 23C128E Min	Typ	Max	23C128E-1 Min	Typ	Max	Unit	Test Conditions ①
Access Time	t_{ACC}			200			150	ns	
Chip Enable Access Time	t_{CE}			200			150	ns	
OE_1, OE_2 Output On Time	t_{OE}	10		100	10		100	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		90	0		90	ns	

Note: ① Input voltage, t_R, t_F = 20ns;
Input and output timing reference levels = 0.8V and 2.0V;
Output load = 1 TTL + 100pF.

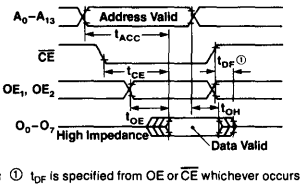
AC Characteristics (Cont.)

T_A = −10°C to +70°C; V_{DD} = +2.5V to +6.0V

Parameter	Symbol	Limits 23C128E Min	Typ	Max	23C128E-1 Min	Typ	Max	Unit	Test Conditions ①
Access Time	t_{ACC}			600			450	ns	
Chip Enable Access Time	t_{CE}			600			450	ns	
OE_1, OE_2 Output On Time	t_{OE}			300			300	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		250	0		250	ns	

Note: ① Input and output timing reference levels = 0.18V_{DD} and 0.7V_{DD};
Output load = 150pF.

Timing Waveform



Note: ① t_{DF} is specified from OE or $\overline{CE}$ whichever occurs first.

μPD23C256E
32,768 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Revision 1

Description

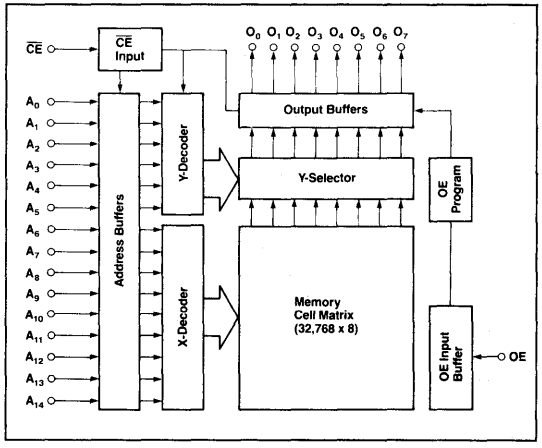
The μPD23C256E is a 262,144-bit Read-only Memory utilizing CMOS silicon gate technology. The device is static in operation, organized as 32,768 words by 8 bits, and has three-state outputs. All inputs and outputs are fully TTL-compatible. The Output Enable pin is mask-programmable and can be specified by selecting 1, 0, or don't-care data. The μPD23C256E is packaged in a 28-pin plastic (μPD23C256EC) DIP and a 28-pin miniflat package (μPD23C256EG). Pinout is compatible with μPD27256 EPROMs.

Features

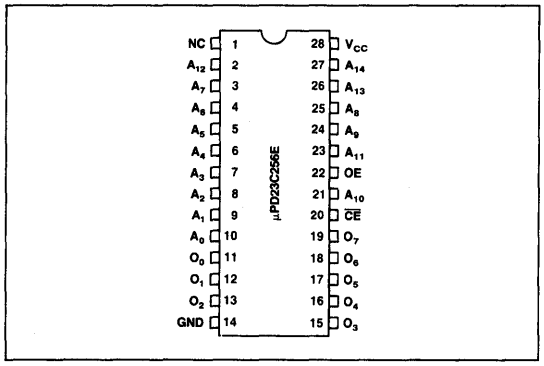
- ☐ 32,768-word by 8-bit organization
- ☐ I/O TTL-compatible
- ☐ Three-state output
- ☐ Single +2.5V to +6.0V power supply
- ☐ Available in plastic DIP and miniflat packages
- ☐ Low power consumption
  - Active: 40mA max
  - Standby: 30μA max
- ☐ 2 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD23C256E	200ns	25mA	30μA
μPD23C256E-1	150ns	30mA	30μA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Symbol	Description
1	NC	No Connection
2–10, 21, 23–27	A_0–A_{14}	Address Inputs
11–13, 15–19	O_0–O_7	Data Outputs
14	GND	Ground
20	$\overline{CE}$	Chip Enable
22	OE	Output Enable ①
28	V_{CC}	Single +2.5V to +6.0V Power Supply

Note: ① The active level of the OE input is specified by 0, 1, or x where x equals don't-care data.

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Absolute Maximum Ratings*

Supply Voltage, V_{CC}	−0.3V to +7V
Input Voltage, V_I	−0.3V to V_{CC} +0.3V
Output Voltage, V_O	−0.3V to V_{CC} +0.3V
Operating Temperature, T_{OPR}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = −10°C to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10	pF	f = 1MHz
Output Capacitance	C_O			15	pF	f = 1MHz

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = +3.2mA
Input Leakage Current High	I_{LIH}			10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			10	μA	$V_O = V_{CC}$ (Chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (Chip deselected)
Power Supply Current	I_{CC1}		14	25	mA	$\overline{CE} = V_{IL}$ μPD23C256E
			17	30	mA	μPD23C256E-1
	I_{CC2}		0.2	1.5	mA	$\overline{CE} = V_{IH}$ (Standby mode)
	I_{CC3}		0.2	30	μA	$\overline{CE} = V_{CC}$ − 0.2V (Standby mode)

DC Characteristics (Cont.)

T_A = −10°C to +70°C; V_{CC} = +2.5V to +6.0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	0.7 x V_{CC}		V_{CC} +0.3V	V	
Input Low Voltage	V_{IL}	−0.3		0.55	V	V_{CC} = 2.5V to 4.5V
		−0.3		0.8		V_{CC} = 4.5V to 6.0V
Output High Voltage	V_{OH}	0.75 V_{CC}			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = +400μA
Input Leakage Current High	I_{LIH}			10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			10	μA	$V_O = V_{CC}$ (Chip deselected)
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V (Chip deselected)
Power Supply Current	I_{CC1}		3	10	mA	V_{CC} = +3.0V ± 10% μPD23C256E
			6	18	mA	V_{CC} = +5.0V ± 10%
			3.5	10	mA	V_{CC} = +3.0V ± 10% μPD23C256E-1
			7	20	mA	V_{CC} = +5.0V ± 10%
	I_{CC3}		0.1	30	μA	V_{CC} = +3.0V ± 10% $\overline{CE} = V_{DD}$ − 0.2V
			0.2	30	μA	V_{CC} = +5.0V ± 10% (Standby mode)

AC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5.0V ± 10%

Parameter	Symbol	Limits 23C256E Min	Typ	Max	23C256E-1 Min	Typ	Max	Unit	Test Conditions ①
Access Time	t_{ACC}			200			150	ns	
Chip Enable Access Time	t_{CE}			200			150	ns	
Output Enable Access Time	t_{OE}	10		100	10		100	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		90	0		90	ns	②

Notes: ① Input voltage, t_R, t_F = 20ns; Input and output timing reference levels = 0.8V and 2.0V; Load = 1TTL + 100pF.
② t_{DF} is specified from $\overline{CE}$ or OE, whichever occurs first.

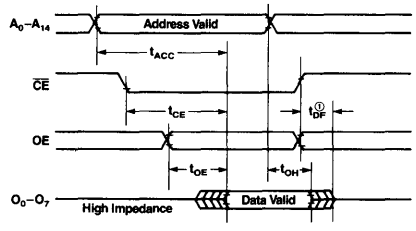
AC Characteristics (Cont.)

T_A = −10°C to +70°C; V_{CC} = +2.5V to +6.0V

Parameter	Symbol	Limits 23C256E Min	Typ	Max	23C256E-1 Min	Typ	Max	Unit	Test Conditions ①
Access Time	t_{ACC}			650			500	ns	
Chip Enable Access Time	t_{CE}			650			500	ns	
Output Enable Access Time	t_{OE}			300			300	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		250	0		250	ns	②

Notes: ① Input and output timing reference levels = V_{IL} and V_{IH}; Load = 150pF.
② t_{DF} is specified from $\overline{CE}$ or OE, whichever occurs first.

Timing Waveform



Note: ① t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid address and the corresponding valid data out.

Chip Enable Access Time, t_{CE}

The maximum time between application of a valid chip enable input and the corresponding valid outputs.

Output Enable Access Time, t_{OE}

The maximum time between application of a valid output enable input and the corresponding valid outputs.

Output Hold Time, t_{OH}

Output hold time is the minimum time after an address change that the previous data remains valid.

Output Disable Time, t_{DF}

Output disable time is the delay between chip selects becoming false and output stages going to the high-impedance state. t_{DF} is specified from $\overline{CE}$ or OE, whichever occurs first.

NEC Electronics Inc.

μPD23C1000
131,072 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The μPD23C1000 is a 1,048,576-bit ROM utilizing CMOS silicon gate technology. The device is static in operation and organized as 131,072 words by 8 bits. The device has three-state outputs and all inputs and outputs are fully TTL-compatible. The μPD23C1000 is available in a plastic (μPD23C1000C) 28-pin DIP.

Features

- ☐ 131,072 words by 8-bit organization
- ☐ Fast access time
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5 V power supply
- ☐ CMOS process technology
- ☐ Fully static operation
- ☐ Low power dissipation: 220 mW (active)
  550 μW (standby)

Performance Ranges

Device	Access Time (Max)	Power Supply (Max)	
		Active	Standby
μPD23C1000C-1	200 ns	40 mA	100 μA
μPD23C1000C	250 ns	40 mA	100 μA

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70 °C
Storage temperature, T_{STG}	−65 to +150 °C

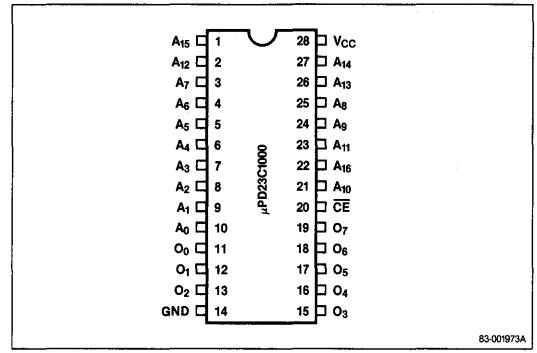
Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25 °C

Parameter	Symbol	Limits Min	Typ	Max	Units	Test Conditions
Input capacitance	C_I			10	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

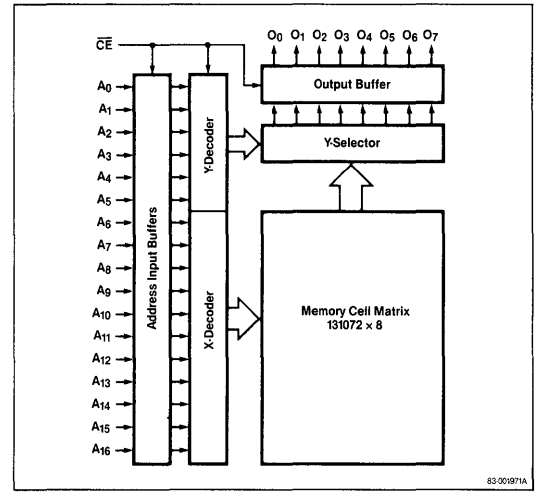
Pin Configuration



Pin Identification

No.	Symbol	Function
1-10, 21-27	A_0-A_{16}	Address inputs
11-13, 15-19	O_0-O_7	Data outputs
14	GND	Ground
20	$\overline{CE}$	Chip enable
28	V_{CC}	+5 V power supply

Block Diagram



10

DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH}	2.2		V_{CC} +0.3	V	
Input low voltage	V_{IL}	−0.3		0.8	V	
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output low voltage	V_{OL}			0.4	V	$I_{OL} = +3.2$ mA
Input leakage current high	I_{LIH}			10	μA	$V_I = V_{CC}$
Input leakage current low	I_{LIL}			−10	μA	$V_I = 0$ V
Output leakage current high	I_{LOH}			10	μA	$V_O = V_{CC}$, Chip deselected
Output leakage current low	I_{LOL}			−10	μA	$V_O = 0$ V, Chip deselected
Power supply current	I_{CC1}			40	mA	$\overline{CE} = V_{IL}$
Power supply current	I_{CC2}			1.5	mA	$\overline{CE} = V_{IH}$, Standby mode
Power supply current	I_{CC3}			100	μA	$\overline{CE} = V_{CC} - 0.2$ V, Standby mode

AC Characteristics (Note 1)

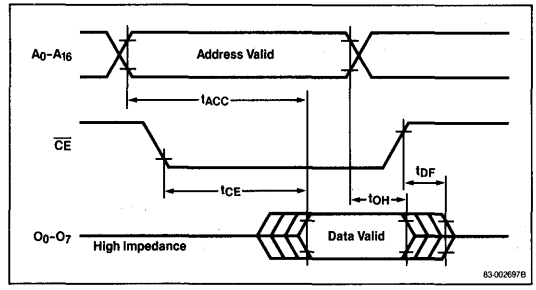
$T_A = -10°C$ to $+70°C$, $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	μPD23C1000-1 Min	μPD23C1000-1 Max	μPD23C1000 Min	μPD23C1000 Max	Unit
Address access time	t_{ACC}		200		250	ns
Chip enable access time	t_{CE}		200		250	ns
Output hold time	t_{OH}	0		0		ns
Output disable time	t_{DF}	0	60	0	60	ns

Note:

(1) AC test conditions: Input voltage rise and fall times = 20 ns; timing reference levels: inputs and outputs = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF

Timing Waveform



NEC
NEC Electronics Inc.

μPD23C2000
2,097,152-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The μPD23C2000 is a 2,097,152-bit ROM utilizing CMOS silicon gate technology. The device is static in operation and the organization is mask-programmable (word mode: 131,072 words by 16 bits; or byte mode: 262,144 words by 8 bits). The device has three-state outputs and all inputs and outputs are fully TTL-compatible. The Output Enable pin is mask-programmable and can be specified by selecting "1", "0" and "Don't Care" data. The μPD23C2000 is available in a plastic (μPD23C2000C) 40-pin DIP.

Features

- ☐ Programmable word organization
  131,072 words by 16 bits (Word mode)
  262,144 words by 8 bits (Byte mode)
- ☐ Fast access time: 250 ns
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5 V power supply
- ☐ CMOS process technology
- ☐ Fully static operation
- ☐ Low power dissipation: 220 mW (active)
  550 μW (standby)

Performance Range

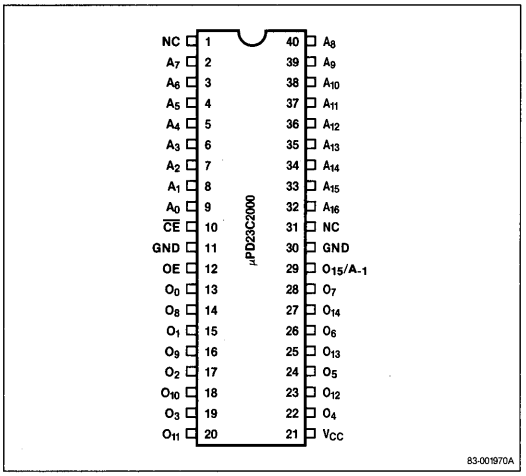
Device	Access Time (Max)	Power Supply (Max)	
		Active	Standby
μPD23C2000	250 ns	40 mA	100 μA

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{CC} +0.3 V
Output voltage, V_O	−0.3 V to V_{CC} +0.3 V
Operating temperature, T_{OPR}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



Pin Identification

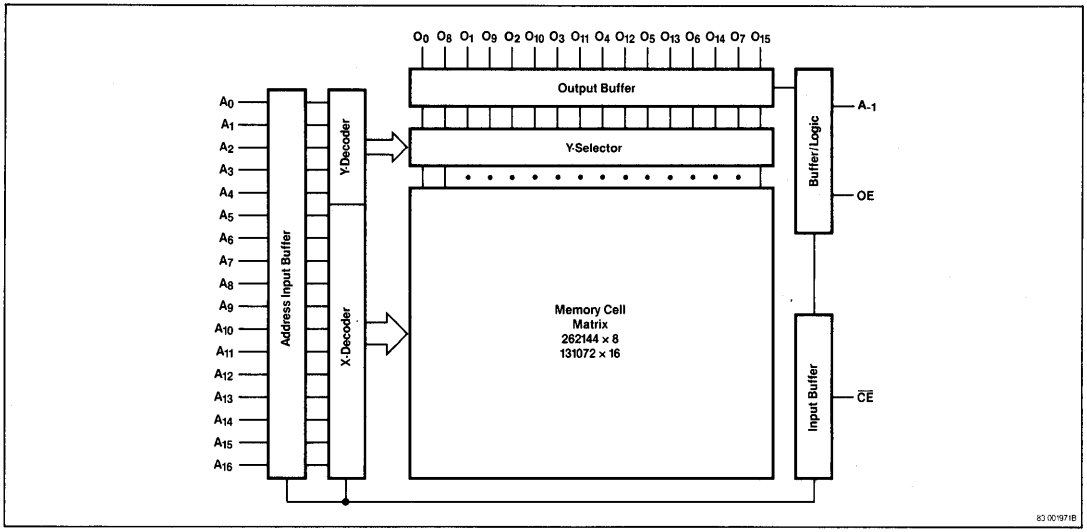
No.	Symbol	Function
1, 31	NC	No connection
2-9, 32-40	A_0-A_{16}	Address inputs
10	$\overline{CE}$	Chip enable
11, 30	GND	Ground
12	OE	Output enable
13-20, 22-28	O_0-O_{14}	Outputs
21	V_{CC}	+5 V power supply
29	O_{15}/A_{-1}	Output 15 (word mode)/LSB address (byte mode)

Capacitance

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C_I			10	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

10

Block Diagram



DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH}	2.2		V_{CC} +0.3	V	
Input low voltage	V_{IL}	−0.3		0.8	V	
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output low voltage	V_{OL}			0.4	V	$I_{OL} = +3.2$ mA
Input leakage current high	I_{LIH}			10	μA	$V_I = V_{CC}$
Input leakage current low	I_{LIL}			−10	μA	$V_I = 0$ V
Output leakage current high	I_{LOH}			10	μA	$V_O = V_{CC}$, Chip deselected
Output leakage current low	I_{LOL}			−10	μA	$V_O = 0$ V, Chip deselected
Power supply current	I_{CC1}			40	mA	$\overline{CE} = V_{IL}$
Power supply current	I_{CC2}			1.5	mA	$\overline{CE} = V_{IH}$, Standby mode
Power supply current	I_{CC3}			100	μA	$\overline{CE} = V_{CC} - 0.2$ V, Standby mode

AC Characteristics (Note 1)

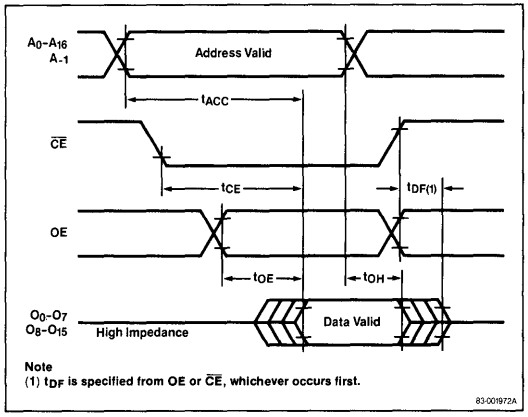
$T_A = -10°C$ to $+70°C$, $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit
Address access time	t_{ACC}			250	ns
Chip enable access time	t_{CE}			250	ns
Output enable access time	t_{OE}	10		110	ns
Output hold time	t_{OH}	0			ns
Output disable time	t_{DF}	0		70	ns

Note:

(1) AC test conditions: Input voltage rise and fall times = 20 ns; timing reference levels: inputs and outputs = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF

Timing Waveform



Note
(1) t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

10

NEC

BIPOLAR TTL PROMs **11**

Section 11 — Bipolar TTL PROMs

NEC

NEC Electronics Inc.

μPB426
1,024 x 4-BIT
BIPOLAR TTL PROM

Revision 1

Description

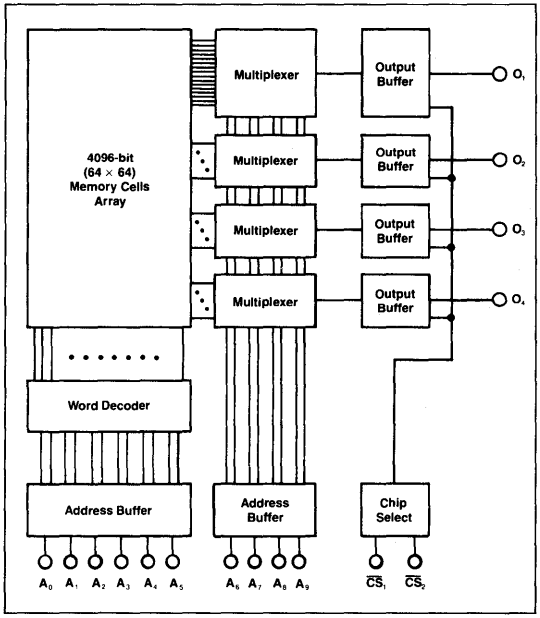
The μPB426 is a high-speed, electrically programmable, fully decoded 4096-bit TTL read-only memory. On-chip address decoding, two chip-select inputs and three-state outputs allow easy expansion of memory capacity. The μPB426 is fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

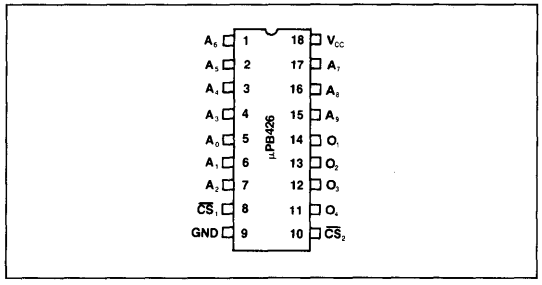
- ☐ A.I.M. (Avalanche Induced Migration), Shorted-junction technology
- ☐ ±10% V_{CC} Operation
- ☐ Two Chip Select inputs for memory expansion
- ☐ Three-state outputs (μPB426)
- ☐ Cerdip and plastic 18-lead dual in-line packages
- ☐ Fast programming time: 200 μs/bit typ.
- ☐ Compatible with: HM-7643, 82S137 types and equivalent devices
- ☐ 4 performance ranges:

Device	Address Access Time	Power Supply
μPB426	70ns	150mA
μPB426-1	60ns	150mA
μPB426-2	50ns	150mA
μPB426-3	35ns	150mA

Block Diagram



Pin Configuration



Pin Identification

A_0-A_9	Address Inputs
O_1-O_4	Data Outputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Selects
V_{CC}	Power (+5V)
GND	Ground

Operation

Programming

A logic one can be permanently programmed into a selected bit location by using a programmer. First, the desired word is selected by the ten address inputs in TTL levels. Either or both of the two chip select inputs must be at a logic one (high). Secondly, a train of high-current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then stopped.

Reading

To read the memory, both of the two chip select inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip select inputs are at logic one (high), all the ouputs will be floating.

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Absolute Maximum Ratings*

Operating Temperature	−25°C to + 75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V, V_{IN} = 2.5V

Characteristics	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}		8	pF
Output Capacitance	C_{OUT}		10	pF

DC Characteristics

T_A = 0°C to +75°C, V_{CC} = 4.50V to 5.50V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	V_I = 5.5V, V_{CC} = 5.5V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V, V_{CC} = 5.5V
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 16 mA, V_{CC} = 4.5V
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.5V, V_{CC} = 5.5V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O = 0.4V, V_{CC} = 5.5V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I = −18mA, V_{CC} = 4.5V
Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded, V_{CC} = 5.5V
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −2.4 mA
Output Short Circuit Current	$-I_{SC}$	15		60	mA	V_O = 0V

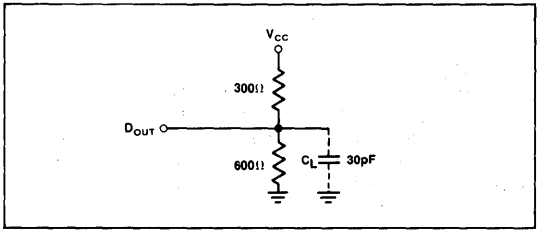
AC Characteristics

T_A = 0°C to +75°C, V_{CC} = 4.50V to 5.50V

Parameter	Symbol	μPB426-3 Min.	Max.	μPB426-2 Min.	Max.	μPB426-1 Min.	Max.	μPB426 Min.	Max.	Unit	Test Conditions
Address Access Time	t_{AA}		35		50		60		70	ns	
Chip Select Access Time	t_{ACS}		25		30		40		45	ns	①②③④
Chip Select Disable Time	t_{DCS}		25		30		40		45	ns	

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

Figure 1. Loading Conditions Test Circuit



Programming Specification

You must rigorously observe this specification in order to program the NEC Bipolar PROMS correctly. NEC will not accept responsibility for any device found to be defective if it was not programmed according to this specification.

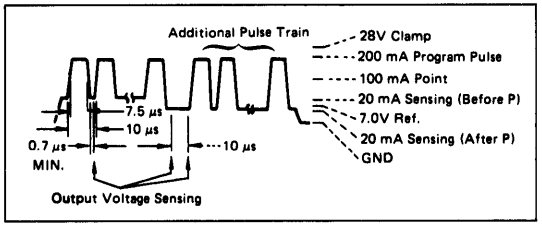
A typical programming operation is performed by sensing, programming, and sensing again to find out if the word to be programmed has reached the desired state. Either or both of the two chip enable inputs must be at a logic one (high).

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement ensures that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic one (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. The current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process continues until the selected bit is altered to the one state. You can tell that a bit is programmed when two successive sense readings, 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied, and the sense current is terminated.

Characteristic	Limit	Unit	Notes
Ambient Temperature	25 ± 5	°C	
Programming pulse			
Amplitude	200 ± 5%	mA	
Clamp voltage	28 + 0% − 2%	V	
Ramp rate (both in rise and in fall)	70 max.	V/μs	
Pulse width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty cycle	70% min.		
Sense current			
Amplitude	20 ± 0.5	mA	
Clamp voltage	28 + 0% − 2%	V	
Ramp rate	70 max.	V/μs	15V point/ 150Ω load.
Sense current interruption before and after address change	10 min.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum sensed voltage for programmed one	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 min.	μs	

Figure 2. Typical Output Voltage Waveform



Qualified Programming Equipment

Approved Manufacturer	Model No.	Personality Module	Socket Adaptors
Data I/O Issaquah, WA	5, 7, 9, 17, 19, 29A	919-1555	715-1305-5
Data I/O Issaquah, WA	Unipak II (950-0059-03C)	Family Code 72	Pinout Code 05
Minato Electronics Tokyo, Japan	1850/1870	7SP-4XXN	5SA-18P20
Kontron Redwood City, CA	MPP-80S	MOD 18C	SA4

μPB429
2,048 x 8-BIT
BIPOLAR TTL PROM

Revision 1

Description

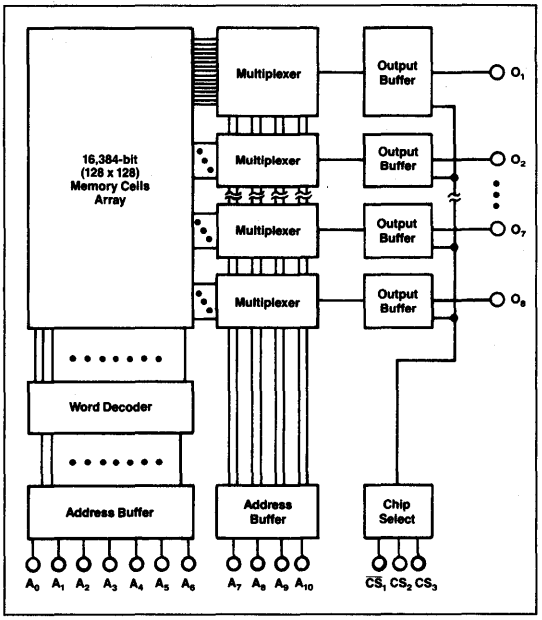
The μPB429 is a high-speed, electrically programmable, fully decoded 16384-bit TTL read-only memory. On-chip address decoding, three chip-select inputs and three-state outputs allow easy expansion of memory capacity. The μPB429 is fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

Features

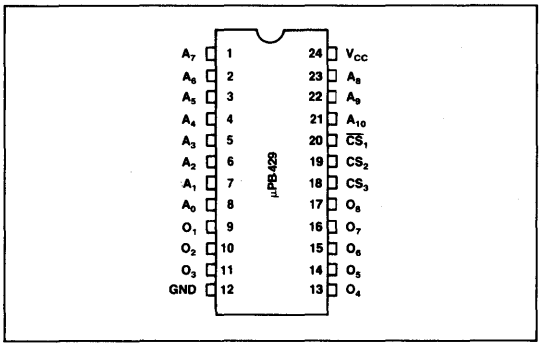
- ☐ A.I.M. (Avalanche Induced Migration), Shorted-junction technology
- ☐ ±10% V_{CC} Operation
- ☐ Three Chip Select inputs for memory expansion
- ☐ Three-state outputs (μPB429)
- ☐ Cerdip and plastic 24-lead dual in-line packages
- ☐ Fast programming time: 10 sec. max for all 16K bits
- ☐ Replaces: 82S191, HM76161, 3636 and equivalent devices
- ☐ 4 performance ranges:

Device	Address Access Time	Power Supply
μPB429	70ns	160mA
μPB429-1	60ns	160mA
μPB429-2	50ns	160mA
μPB429-3	45ns	160mA

Block Diagram



Pin Configuration



Pin Identification

A_0-A_{10}	Address Inputs
O_1-O_8	Data Outputs
$\overline{CS}_1$, CS_2, CS_3	Chip Selects
V_{CC}	Power (+5V)
GND	Ground

Operation

Programming

A logic one can be permanently programmed into a selected bit location by using a programmer. First, the desired word is selected by the eleven address inputs in TTL levels. Disenable the memory by proper application of logic levels on the chip selects. Secondly, a train of high-current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then stopped.

Reading

To read the memory, enable the device (i.e.; $\overline{CS}_1 = 0$, $CS_2 = CS_3 = 1$). The outputs then correspond to the data programmed in the selected words. When the chip is deselected, all the ouputs will be floating.

11

Absolute Maximum Ratings*

Operating Temperature	−25°C to + 75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V, V_{IN} = 2.5V

Characteristics	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}		8	pF
Output Capacitance	C_{OUT}		10	pF

DC Characteristics

T_A = 0°C to +75°C, V_{CC} = 4.50V to 5.50V

Parameter	Symbol	Limits Min.	Typ.	Max.	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	V_I = 5.5V, V_{CC} = 5.5V
Input Low Current	$-I_{IL}$			0.25	mA	V_I = 0.4V, V_{CC} = 5.5V
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 16 mA, V_{CC} = 4.5V
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.5V, V_{CC} = 5.5V
Output Leakage Current	$-I_{OFF2}$			40	μA	V_O = 0.4V, V_{CC} = 5.5V
Input Clamp Voltage	$-V_{IC}$			1.2	V	I_I = −18mA, V_{CC} = 4.5V
Power Supply Current	I_{CC}		100	160	mA	All Inputs Grounded, V_{CC} = 5.5V
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −2.4 mA
Output Short Circuit Current	$-I_{SC}$	20		70	mA	V_O = 0V

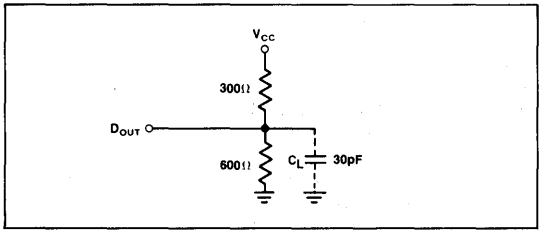
AC Characteristics

T_A = 0°C to +75°C, V_{CC} = 4.50V to 5.50V

Parameter	Symbol	μPB429-3 Min.	Max.	μPB429-2 Min.	Max.	μPB429-1 Min.	Max.	μPB429 Min.	Max.	Unit	Test Conditions
Address Access Time	t_{AA}		45		50		60		70	ns	
Chip Select Access Time	t_{ACS}		30		30		40		50	ns	①②③④
Chip Select Disable Time	t_{DCS}		30		30		40		50	ns	

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

Figure 1. Loading Conditions Test Circuit



Programming Specification

You must rigorously observe this specification in order to program the NEC Bipolar PROMS correctly. NEC will not accept responsibility for any device found to be defective if it was not programmed according to this specification.

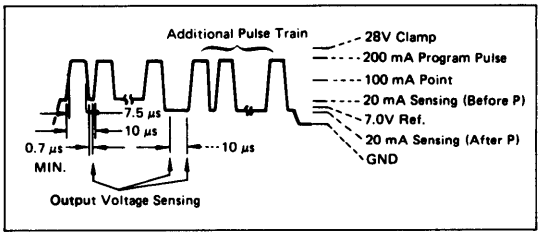
A typical programming operation is performed by sensing, programming, and sensing again to find out if the word to be programmed has reached the desired state. Disenable the memory by proper application of logic levels in the three chip selects.

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement ensures that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic one (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. The current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process continues until the selected bit is altered to the one state. You can tell that a bit is programmed when two successive sense readings, 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied, and the sense current is terminated.

Characteristic	Limit	Unit	Notes
Ambient Temperature	25 ± 5	°C	
Programming pulse			
Amplitude	200 ± 5%	mA	
Clamp voltage	28 + 0% − 2%	V	
Ramp rate (both in rise and in fall)	70 max.	V/μs	
Pulse width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty cycle	70% min.		
Sense current			
Amplitude	20 ± 0.5	mA	
Clamp voltage	28 + 0% − 2%	V	
Ramp rate	70 max.	V/μs	15V point/ 150Ω load.
Sense current interruption before and after address change	10 min.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum sensed voltage for programmed one	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 min.	μs	

Figure 2. Typical Output Voltage Waveform



Qualified Programming Equipment

Approved Manufacturer	Model No.	Personality Module	Socket Adaptors
Data I/O Issaquah, WA	5, 7, 9, 17, 19, 29A	919-1555	715-1628-2
Data I/O Issaquah, WA	Unipak II (950-0059-03C)	Family Code 72	Pinout Code 21
Minato Electronics Tokyo, Japan	1850/1870	7SP-4XXN	5SA-24P74
Kontron Redwood City, CA	MPP-805	MOD 18C	SA22

PACKAGING INFORMATION

Section 12 — Packaging Information

Package/Device Cross Reference

Package	Device
14-Pin Plastic DIP	μPD41221C
16-Pin Plastic DIP	μPD4164C μPD4265C
16-Pin Plastic DIP (300 mil, Semiwide Body)	μPD41256C (Process Code F)
16-Pin Plastic DIP (300 mil, Wide Body)	μPD41256C (Process Codes P and L) μPD41257C
16-Pin Plastic Zig-Zag Inline Package	μPD41256V
18-Pin Plastic DIP	μPD41416C μPB426C
18-Pin Plastic DIP (300 mil, Semiwide Body)	μPD41464C (Process Codes L and F)
18-Pin Plastic DIP (300 mil, Wide Body)	μPD41464C (Process Code K) μPD411000C μPD411001C
18-Pin Plastic Leadless Chip Carrier	μPD41256L μPD41257L μPD41464L
18-Pin Ceramic DIP (300 mil)	μPB10470D μPB100470D
18-Pin Cerdip (300 mil)	μPD2147AD μPD2149D μPB426D
20-Pin Plastic DIP (300 mil)	μPD4311C μPD4314C
20-Pin Plastic DIP (300 mil, Wide Body)	μPD414256C
22-Pin Plastic DIP (300 mil, Wide Body)	μPD4361C μPD4362C
22-Pin Ceramic LCC	μPD4361K
22-Pin SIMM, MC-41256A4A (Glass-epoxy Substrate)	MC-41256A4A
22-Pin SIMM, MC-411000A1A (Glass-epoxy Substrate)	MC-411000A1A
22-Pin SIMM, MC-41256A4C (Ceramic Substrate)	MC-41256A4C
22-Pin SIMM, MC-411000A1C (Ceramic Substrate)	MC-411000A1C
24-Pin Plastic DIP (300 mil)	μPD41101C μPD41102C
24-Pin Plastic DIP (400 mil)	μPD41264C
24-Pin Plastic DIP (600 mil)	μPD446C μPD449C μPD4016C μPD2364AC μPB429C
24-Pin Ceramic DIP (400 mil)	μPB10422D μPB10474D μPB100422D μPB100474D
24-Pin Cerdip (600 mil)	μPB429D
24-Pin Ceramic Flatpack	μPB100422B μPB100474B
24-Pin Plastic Miniflat	μPD446G
24-Pin Ceramic LCC	μPB100474K
24-Pin SIMM, MC-41256A5A (Glass-epoxy Substrate)	MC-41256A5A
24-Pin SIMM, MC-41256A5C (Ceramic Substrate)	MC-41256A5C
26/20-Pin Plastic SOJ	μPD411000LA μPD411001LA μPD414256LA
28-Pin Plastic DIP (600 mil)	μPD4168C μPD42832C μPD4364C μPD4464C μPD43256C μPD2764C μPD27128C μPD27C64C μPD27C256C

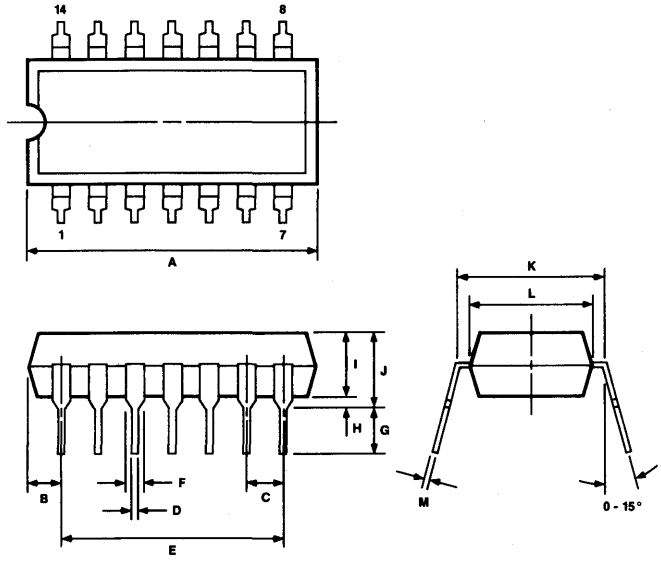
Package/Device Cross Reference (cont)

Package	Device
28-Pin Plastic DIP (600 mil) (cont)	μPD27C256AC μPD2364EC μPD23128EC μPD23C64EC μPD23C128EC μPD23C256EC μPD23C1000C
28-Pin Cerdip (600 mil)	μPD2764D μPD27128D μPD27C64D
28-Pin Cerdip (600 mil, Wide Body)	μPD27256D μPD27C256D μPD27C256AD μPD27C512D
28-Pin Plastic Miniflat	μPD42832G μPD4364G μPD4464G μPD43256G μPD27C256AG μPD23C256AG
30-Pin SIMM, MC-41256A8A (Glass-epoxy Substrate)	MC-41256A8A
30-Pin SIMM, MC-41256A9A (Glass-epoxy Substrate)	MC-41256A9A
30-Pin SIMM, MC-41256A8B (Glass-epoxy Substrate)	MC-41256A8B
30-Pin SIMM, MC-41256A9B (Glass-epoxy Substrate)	MC-41256A9B
32-Pin Ceramic LCC	μPD27C256AK
40-Pin Plastic DIP (600 mil)	μPD23C2000C
40-Pin Cerdip (600 mil, Wide Body)	μPD27C1024D

14-Pin Plastic DIP (400 mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	15.24	.600
F	1.2 min	.047 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$

Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.

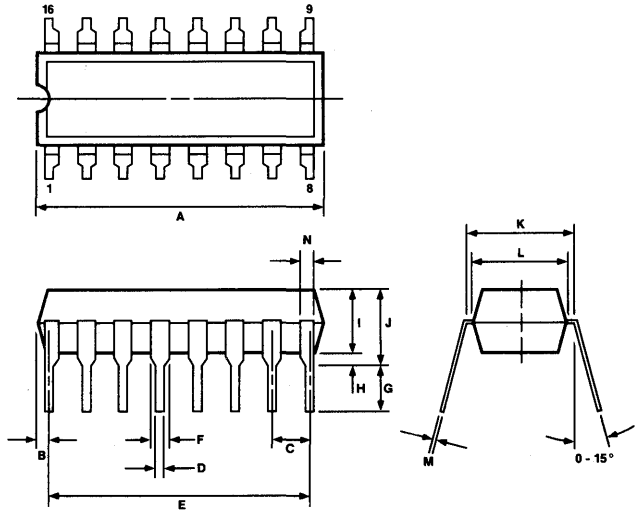


83-003576B

16-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	17.78	.700
F	1.2 min	.047 min
G	3.5 ± .03	.138 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.4	.252
M	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$
N	1.0 min	.039 min

Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.

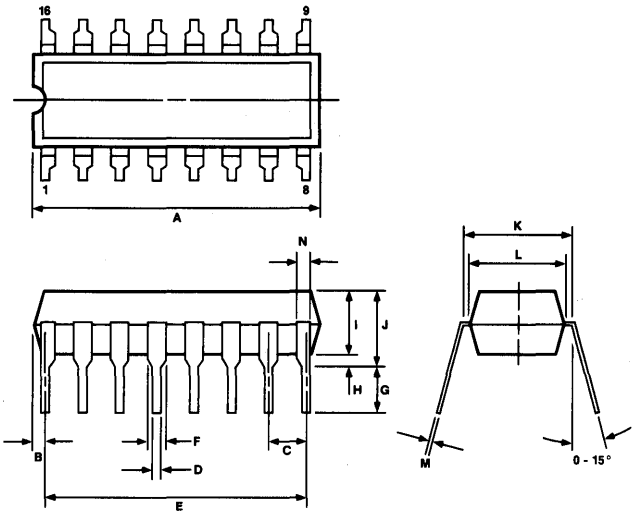


83-003584B

16-Pin Plastic DIP (300 mil, Semiwide Body)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	17.78	.700
F	1.2 min	.047 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.7	.264
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$
N	1.0 min	.039 min

Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.

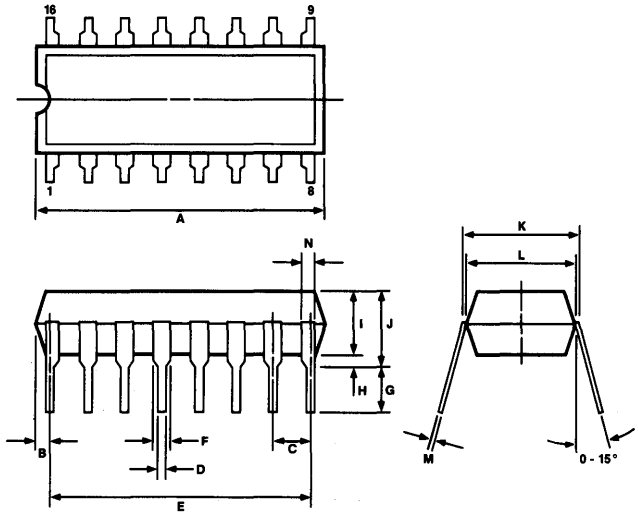


83-003634B

16-Pin Plastic DIP (300 mil, Wide Body)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	17.78	.700
F	1.2 min	.047 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.4	.291
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$
N	1.0 min	.039 min

Note:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.

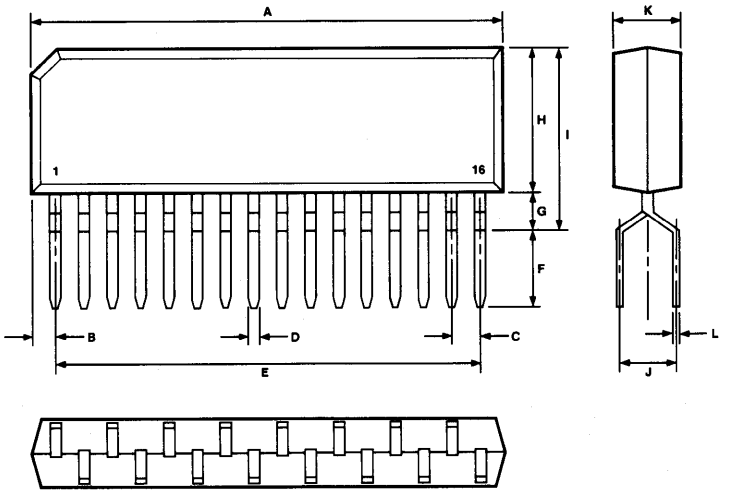


83-003580B

16-Pin Plastic ZIP

Item	Millimeters	Inches
A	21.59 max	.850 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	19.05	.750
F	3.5 ± .3	.138 ± .012
G	.9 min	.035 min
H	6.6	.260
I	8.3 max	.327 max
J	2.54 [TP]	.100 [TP]
K	2.8 ± .2	.110 ± .008
L	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$

Notes:
[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.

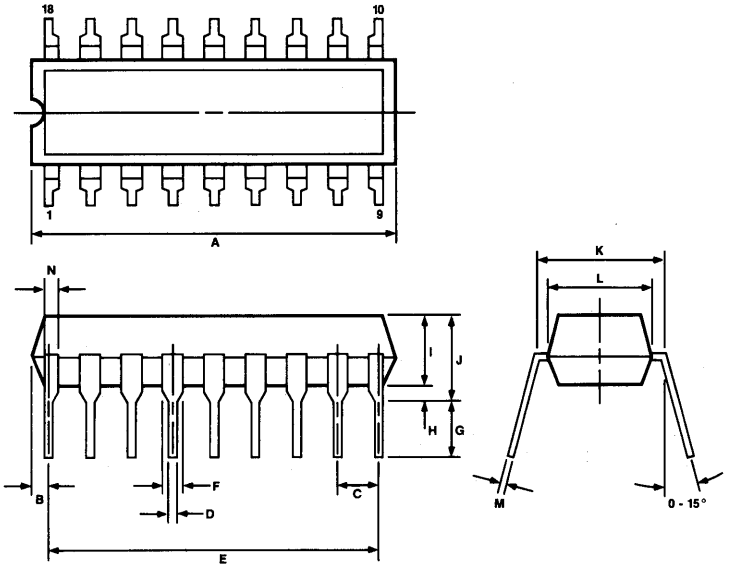


83-003585B

18-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	20.32	.800
F	1.2 min	.047 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$
N	1.0 min	.039 min

Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.



83-003630B

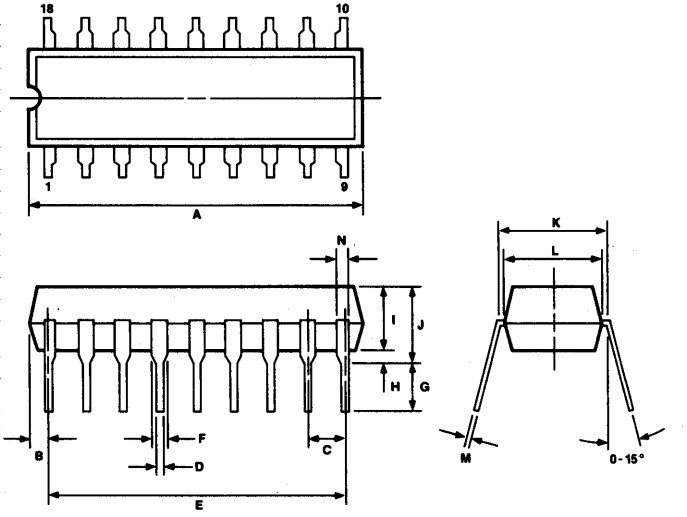
18-Pin Plastic DIP (300 mil, Semiwide Body)

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	20.32	.800
F	1.2 min	.047 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.7	.264
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$
N	1.0 min	.039 min

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003588B

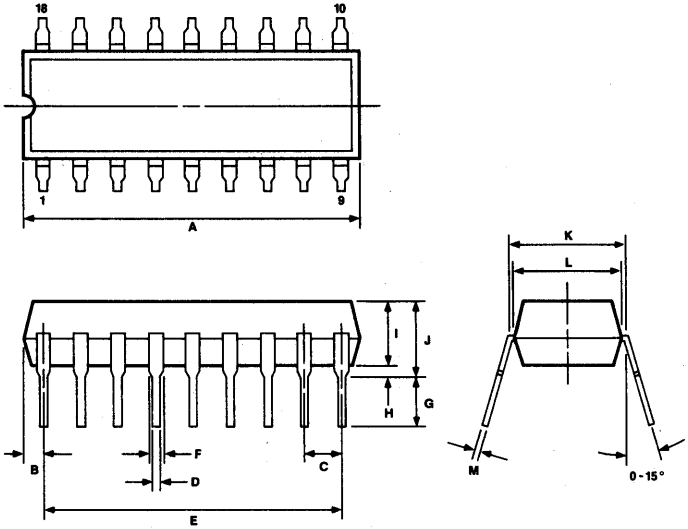
18-Pin Plastic DIP (300 mil, Wide Body)

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	20.32	.800
F	1.2 min	.047 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.35	.289
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

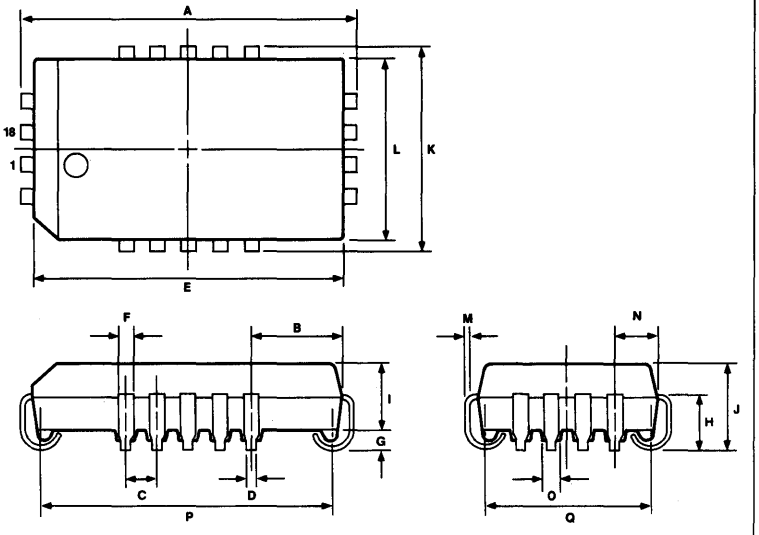
[2] Item "K" to center of leads when formed parallel.



83-003586B

18-Pin Plastic Leadless Chip Carrier

Item	Millimeters	Inches
A	13.4 ± .20	.528 ± .008
B	3.71 ± .15	.146 ± .006
C	1.27	.050
D	.40 ± .10	.016 ± .004
E	12.5	.492
F	.60	.024
G	.8 min	.031 min
H	2.40 ± .20	.094 ± .008
I	2.6	.102
J	3.50 ± .20	.138 ± .008
K	8.30 ± .20	.327 ± .008
L	7.40	.291
M	$.20^{+.10}_{-.05}$	$.008^{+.004}_{-.002}$
N	1.80 ± .20	.071 ± .008
O	.70	.028
P	11.68 ± .20	.460 ± .008
Q	6.6 ± .20	.260 ± .008



83-003581B

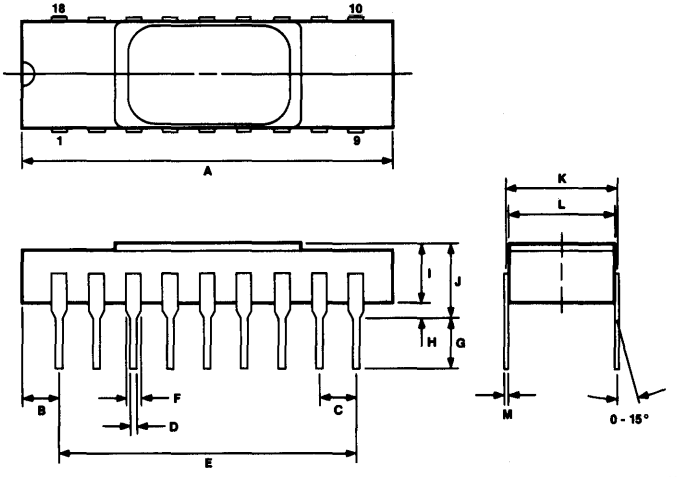
18-Pin Ceramic DIP (300 mil)

Item	Millimeters	Inches
A	25.40 max	1.000 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.46 ± .05	.018 ± .002
E	20.32	.800
F	1.25 min	.049 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.020 min
I	2.90	.114
J	4.57 max	.180 max
K	7.62 [TP]	.300 [TP]
L	7.32	.288
M	.25 ± .05	$.010^{+.002}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003628B

NEC

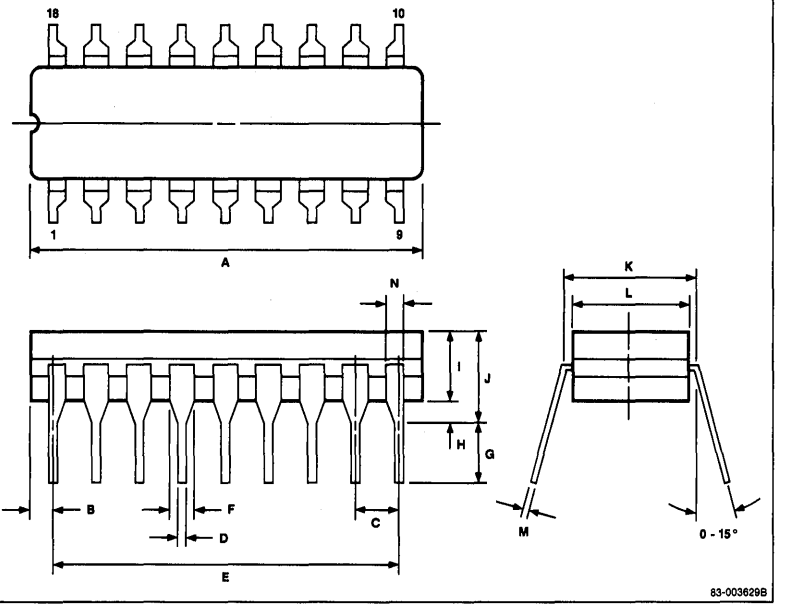
18-Pin Cerdip (300 mil)

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.46 ± .05	.018 ± .002
E	20.32	.800
F	1.42 min	.055 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.020 min
I	3.95	.156
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.60	.260
M	.25 ± .05	.010 $^{+.002}_{-.003}$
N	.89 min	.035 min

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003629B

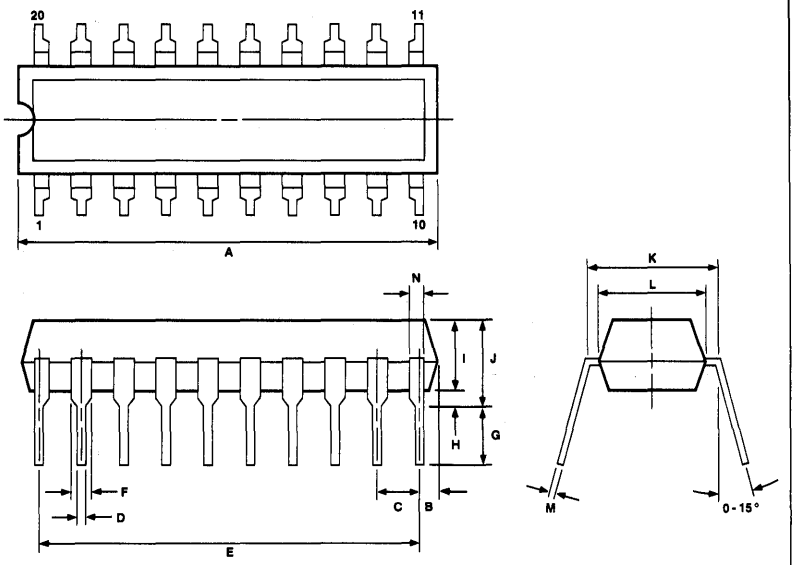
20-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	25.40 max	1.000 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	22.86	.900
F	1.1 min	.043 min
G	3.5 ± .30	.138 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$
N	.9 min	.035 min

Note:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

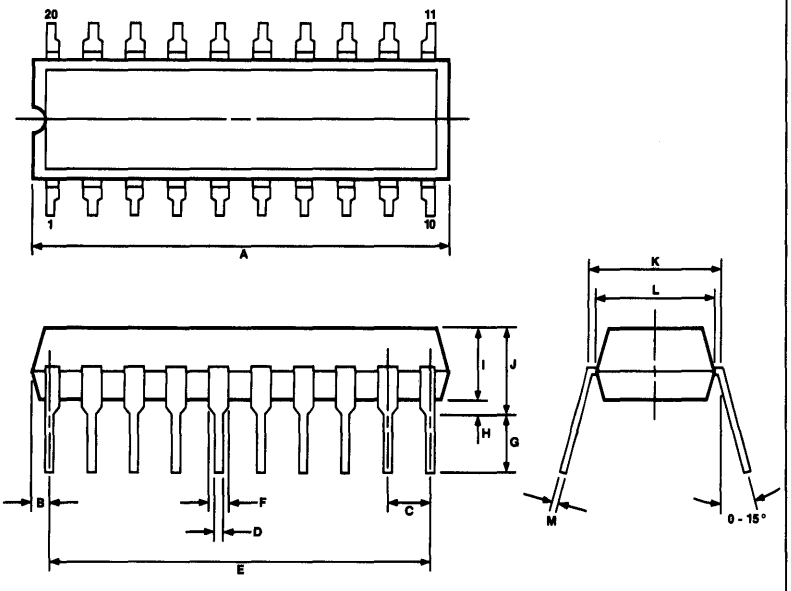


83-001491B

20-Pin Plastic DIP (300 mil, Wide Body)

Item	Millimeters	Inches
A	25.40 max	1.000 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	22.86	.900
F	1.2 min	.047 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.25	.285
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$

Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.

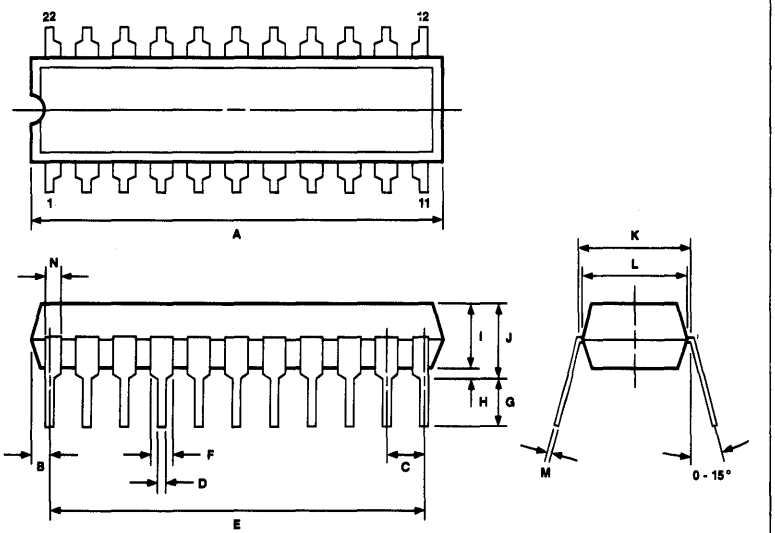


83-003626B

22-Pin Plastic DIP (300 mil, Wide Body)

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	25.40	1.000
F	1.2 min	.047 min
G	3.20 ± .30	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.40	.291
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$
N	.9 min	.035 min

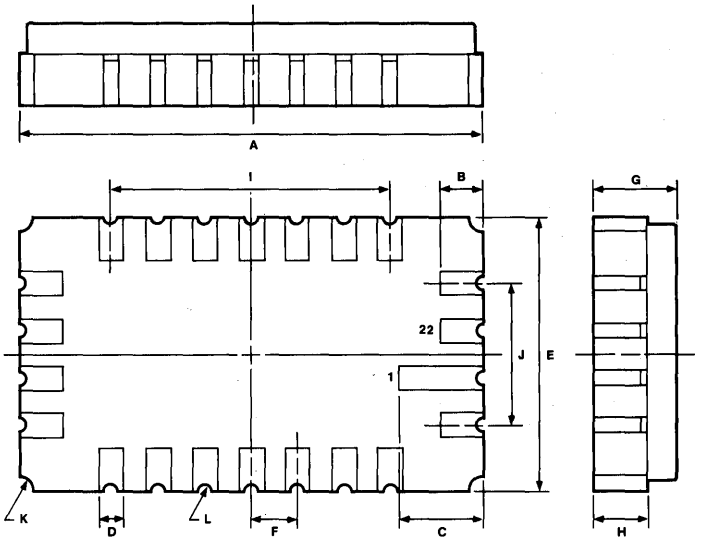
Note:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.



83-003577B

22-Pin Ceramic LCC

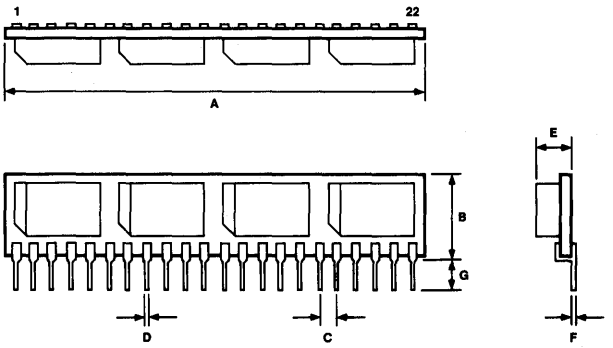
Item	Millimeters	Inches
A	12.45 ± .35	.490 ± .014
B	1.14	.045
C	2.29	.090
D	.64	.025
E	7.37 ± .35	.290 ± .014
F	1.27	.050
G	2.26 max	.089 max
H	1.40	.055
I	7.62	.300
J	3.81	.150
K	.3 rad	.012 rad
L	.2 rad	.008 rad



83-003578B

22-Pin SIMM, MC-41256A4A (Glass-epoxy Substrate)

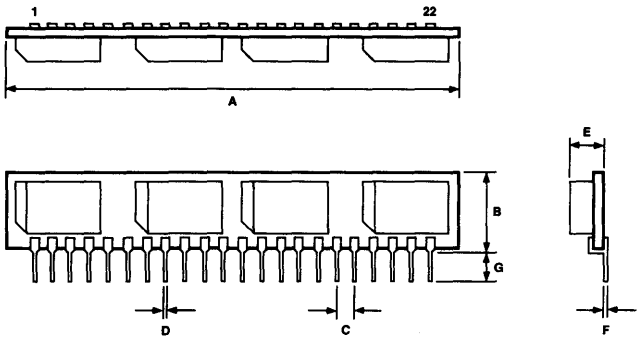
Item	Millimeters	Inches
A	56.52	2.225
B	11.43 max	.450 max
C	2.54	.100
D	.45	.018
E	5.30 max	.209 max
F	.25	.010
G	4.00	.157



83-003205B

22-Pin SIMM, MC-411000A1A (Glass-epoxy Substrate)

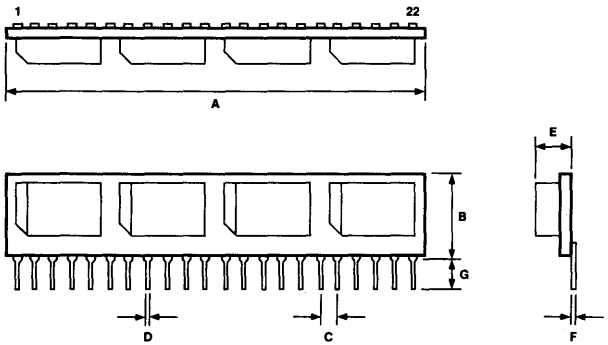
Item	Millimeters	Inches
A	61.0	2.40
B	10.92 max	.430 max
C	2.54	.100
D	.45	.018
E	5.30 max	.209 max
F	.25	.010
G	4.00	.157



83-003477B

22-Pin SIMM, MC-41256A4C (Ceramic Substrate)

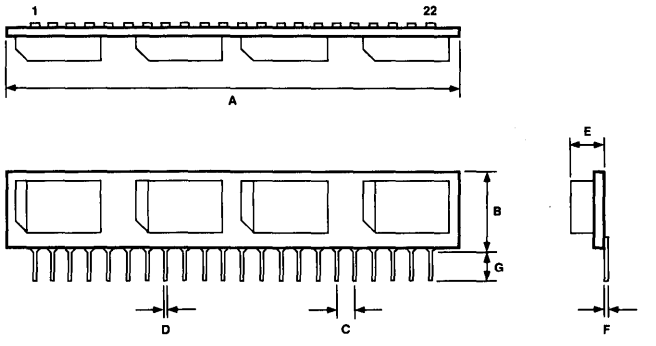
Item	Millimeters	Inches
A	56.52	2.225
B	9.70 max	.382 max
C	2.54	.100
D	.45	.018
E	5.08 max	.200 max
F	.25	.010
G	4.00	.157



83-003204B

22-Pin SIMM, MC-411000A1C (Ceramic Substrate)

Item	Millimeters	Inches
A	61.0	2.40
B	9.7 max	.382 max
C	2.54	.100
D	.45	.018
E	5.08 max	.200 max
F	.25	.010
G	4.00	.157



83-003476B

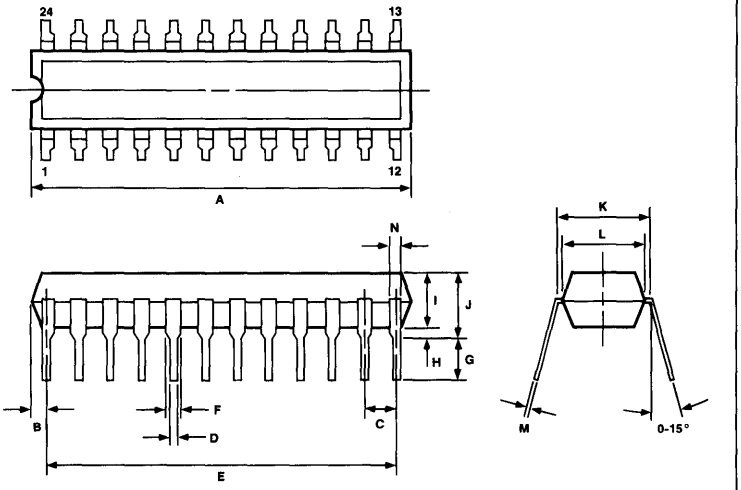
24-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	27.94	1.100
F	1.2 min	.047 min
G	3.50 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.4	.252
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$
N	1.0 min	.039 min

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003725B

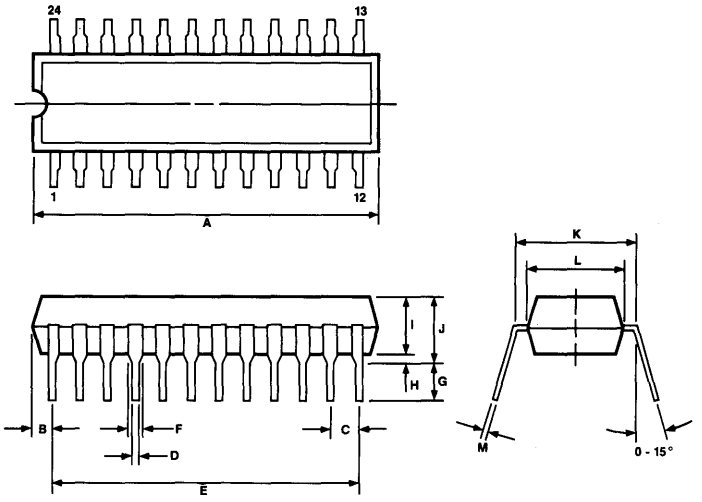
24-Pin Plastic DIP (400 mil)

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	27.94	1.100
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003627B

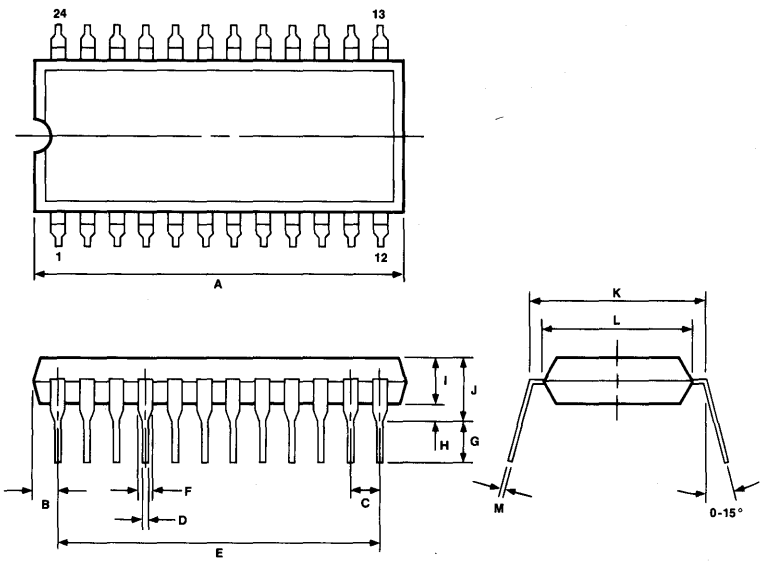
24-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	27.94	1.100
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

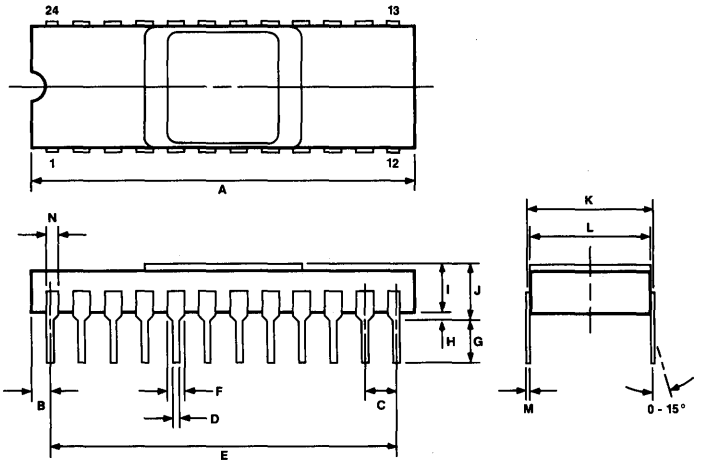


83-001950B

24-Pin Ceramic DIP (400 mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.46 ± .05	.018 ± .002
E	27.94	1.100
F	1.25 min	.049 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.020 min
I	2.74	.108
J	4.57 max	.180 max
K	10.16 [TP]	.400 [TP]
L	10.0	.394
M	.25 ± .05	.010 $^{+.002}_{-.003}$
N	1.0 min	.039 min

Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.

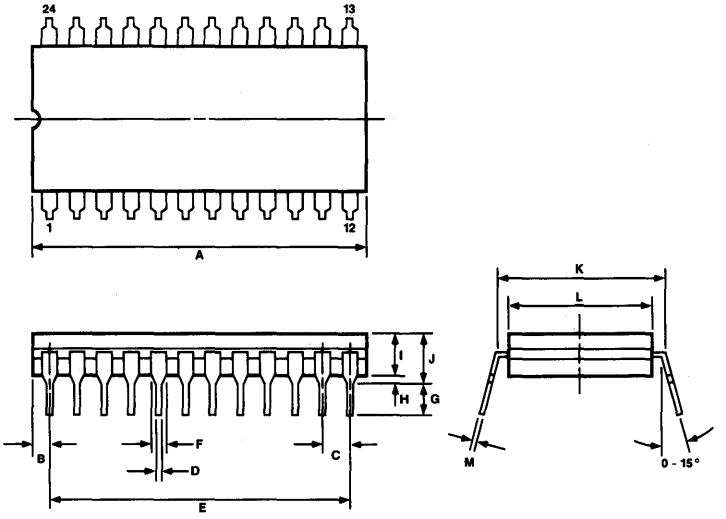


83-003549B

24-Pin Cerdip (600 mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .010	.020 $^{+.004}_{-.005}$
E	27.94	1.100
F	1.2 min	.047 min
G	3.0 ± .3	.118 ± .012
H	.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.21	.520
M	.25 ± .05	.010 $^{+.002}_{-.003}$

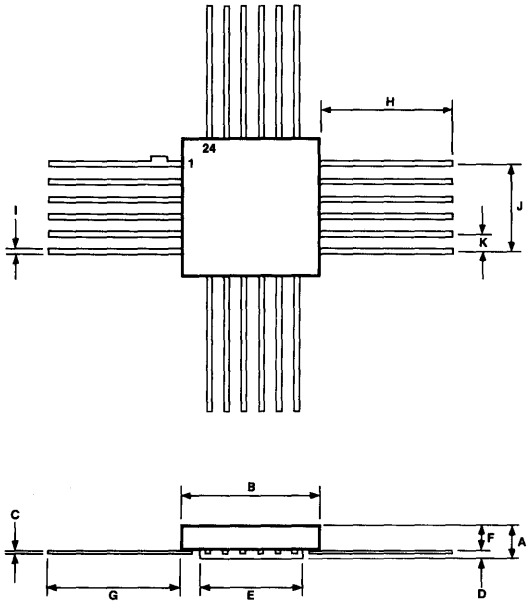
Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.



83-003633B

24-Pin Ceramic Flatpack

Item	Millimeters	Inches
A	2.6 max	.102 max
B	9.5	.374
C	.13	.005
D	.5	.020
E	6.9	.272
F	2.0	.079
G	8.9	.350
H	8.9	.350
I	.43	.017
J	6.35	.250
K	1.27	.050

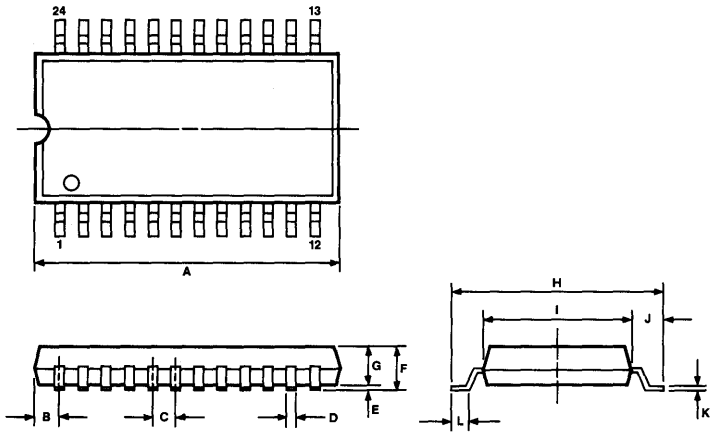


83-003583B

24-Pin Plastic Miniflat

Item	Millimeters	Inches
A	16.51 max	.650 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	$.40 \pm .10$	$.016^{+.004}_{-.005}$
E	$.1^{+.2}_{-.1}$	$.004^{+.008}_{-.004}$
F	2.5 max	.099 max
G	2.00	.079
H	$12.2 \pm .3$	$.480^{+.013}_{-.012}$
I	8.4	.331
J	1.9	.075
K	$.15^{+.10}_{-.05}$	$.006^{+.004}_{-.002}$
L	$.9 \pm .2$	$.035^{+.009}_{-.008}$

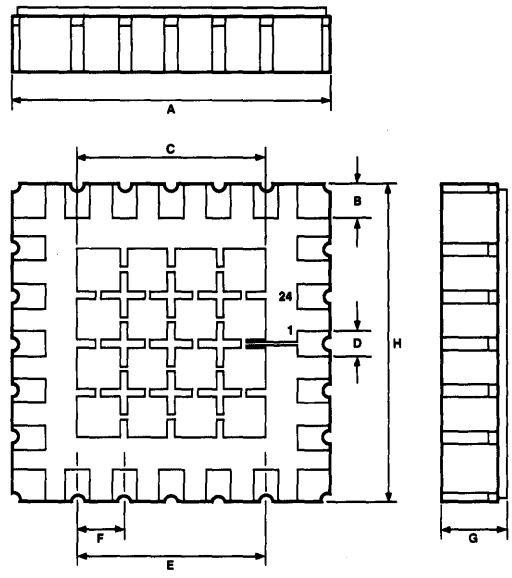
Notes:
[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.



83-002701B

24-Pin Ceramic LCC

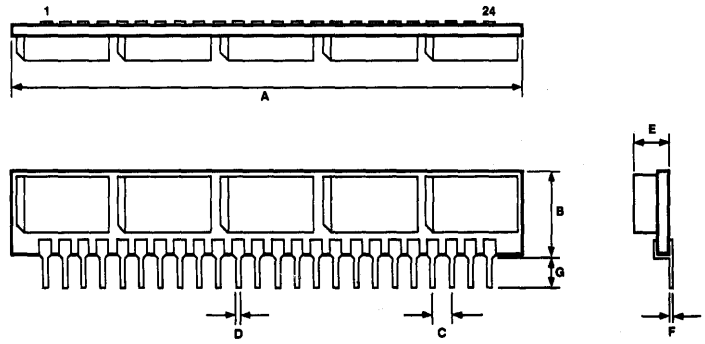
Item	Millimeters	Inches
A	8.51	.335
B	.89	.035
C	5.14	.202
D	.64	.025
E	5.08	.200
F	1.27	.050
G	1.76	.069
H	8.51	.335



83-003582B

24-Pin SIMM, MC-41256A5A (Glass-epoxy Substrate)

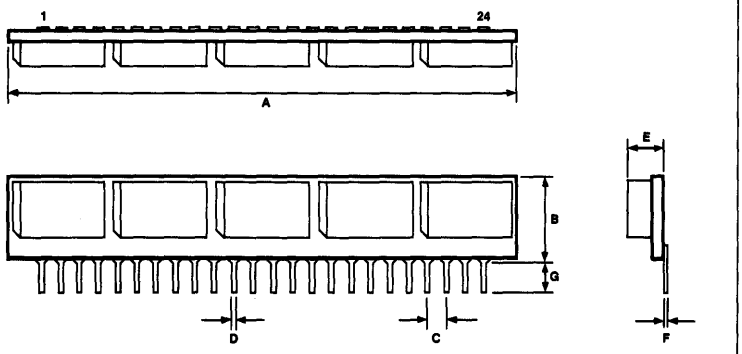
Item	Millimeters	Inches
A	68.60	2.70
B	11.40 max	.449 max
C	2.54	.100
D	.45	.018
E	5.30 max	.209 max
F	.25	.010
G	4.00	.157



83-003209B

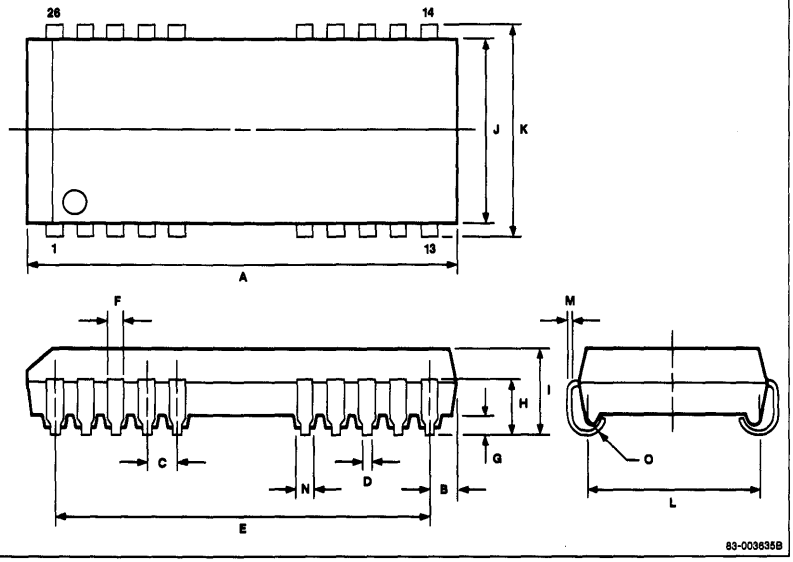
24-Pin SIMM, MC-41256A5C (Ceramic Substrate)

Item	Millimeters	Inches
A	66.60	2.70
B	9.70 max	.382 max
C	2.54	.100
D	.45	.018
E	5.08 max	.200 max
F	.25	.010
G	4.00	.157



26/20-Pin Plastic SOJ

Item	Millimeters	Inches
A	17.35 ± .25	.683 ± .010
B	1.08 ±.15	.043 ± .006
C	1.27	.050
D	.40 ± .10	.016 ± .004
E	15.24	.600
F	.80	.024
G	.8 min	.031 min
H	2.4 ± .2	.094 ± .008
I	3.5 ± .2	.138 ± .008
J	7.57	.298
K	8.47 ± .2	.333 ± .008
L	6.73 ± .2	.265 ± .008
M	$.20^{+.10}_{-.05}$	$.008^{+.004}_{-.002}$
N	.07	.028
O	.85 rad	.033 rad



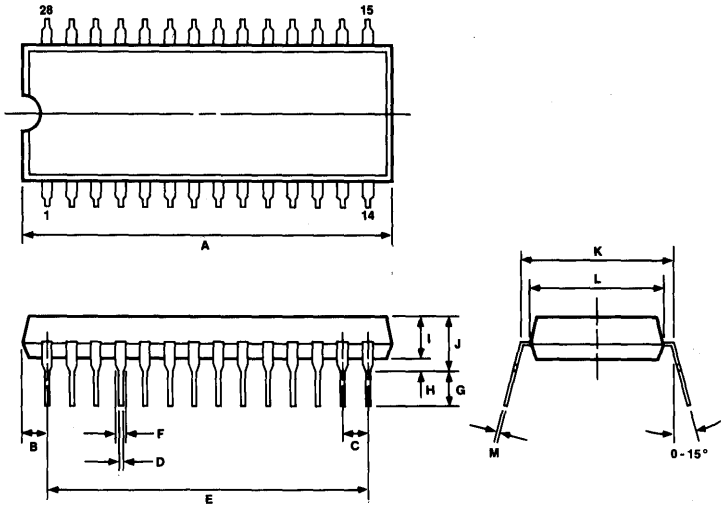
28-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	33.02	1.300
F	1.2 min	.047 min
G	3.6 ± .30	.142 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.20	.520
M	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-001675B

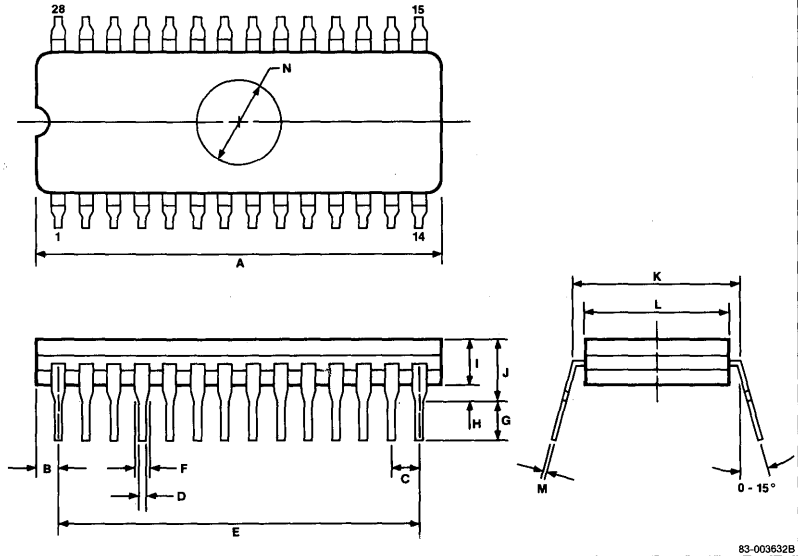
28-Pin Cerdip (600 mil)

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	33.02	1.300
F	1.2 min	.047 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.21	.520
M	.25 ± .05	$.010^{+.002}_{-.003}$
N	7.62 dia	.300 dia

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

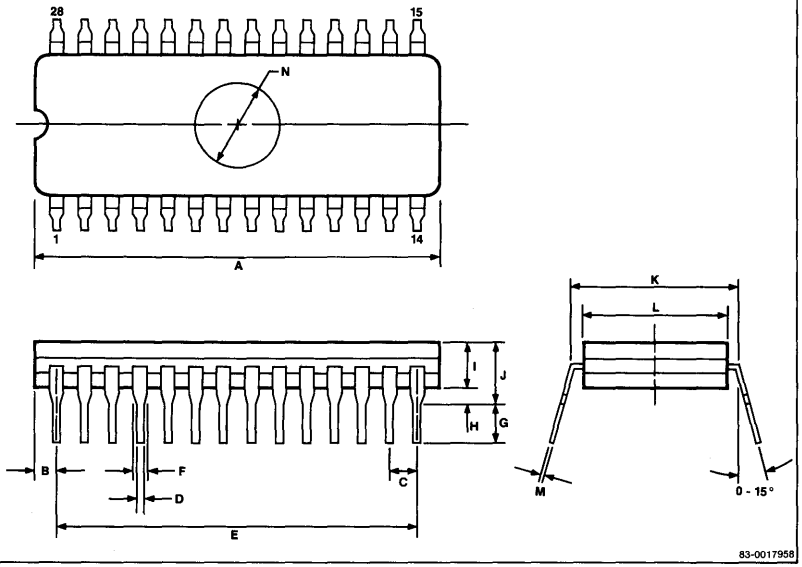


83-003632B

28-Pin Cerdip (600 mil, Wide Body)

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	33.02	1.300
F	1.2 min	.047 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	.25 ± .05	$.010^{+.002}_{-.003}$
N	8.89 dia	.350 dia

Notes:
[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.

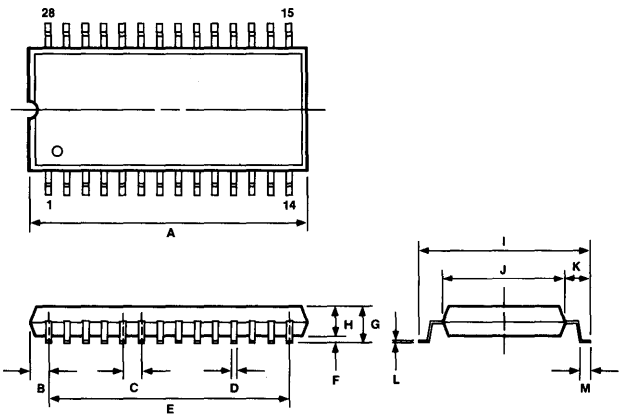


83-001795B

28-Pin Plastic Miniflat

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	.40 ± .10	$.016^{+.004}_{-.005}$
E	16.51	.650
F	$.1^{+.2}_{-.1}$	$.004^{+.008}_{-.004}$
G	2.5 max	.099 max
H	2.00	.079
I	11.8 ± .3	$.465^{+.012}_{-.013}$
J	8.4	.331
K	1.7	.067
L	$.15^{+.10}_{-.05}$	$.006^{+.004}_{-.002}$
M	.7 ± .2	$.028^{+.008}_{-.009}$

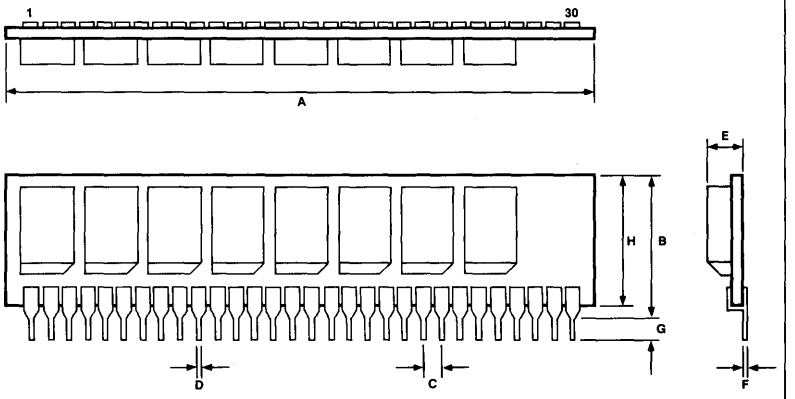
Note:
[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.



83-001676B

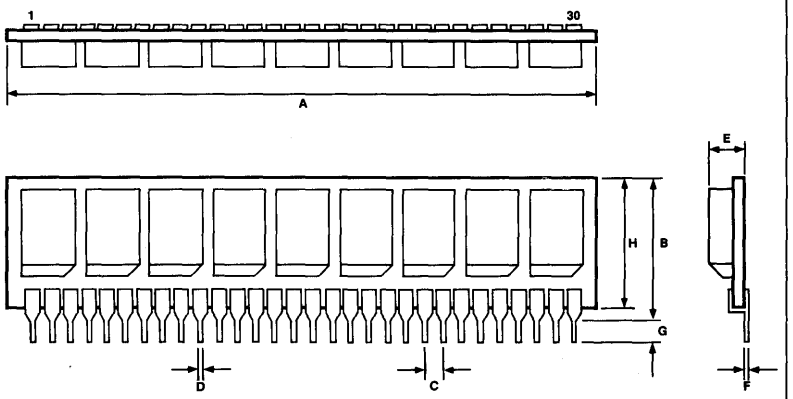
30-Pin SIMM, MC-41256A8A (Glass-epoxy Substrate)

Item	Millimeters	Inches
A	78.90	3.106
B	18.00 max	.709 max
C	2.54	.100
D	.45	.018
E	5.30 max	.209 max
F	.25	.010
G	4.00	.157
H	16.76	.660



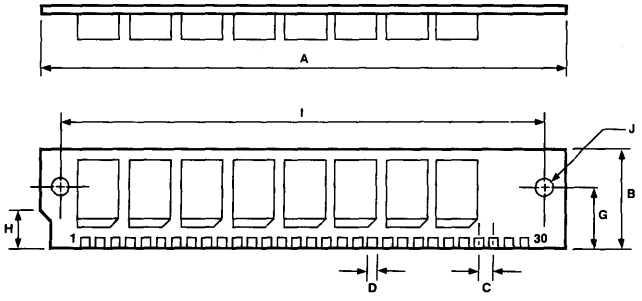
30-Pin SIMM, MC-41256A9A (Glass-epoxy Substrate)

Item	Millimeters	Inches
A	78.90	3.106
B	18.00 max	.709 max
C	2.54	.100
D	.45	.018
E	5.30 max	.209 max
F	.25	.010
G	4.00	.157
H	16.76	.660



30-Pin SIMM, MC-41256A8B (Glass-epoxy Substrate)

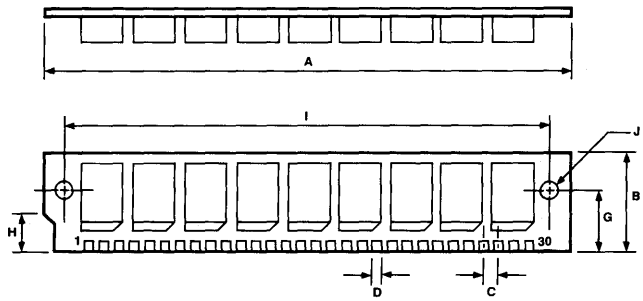
Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ± .08	.050 ± .0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



83-003210B

30-Pin SIMM, MC-41256A9B (Glass-epoxy Substrate)

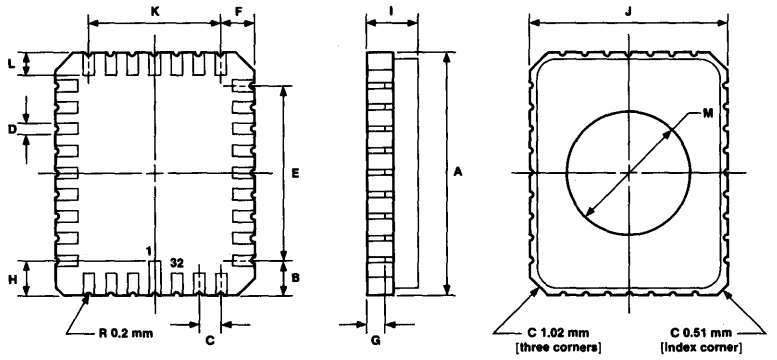
Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ± .08	.050 ± .0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



83-003212B

32-Pin Ceramic LCC

Item	Millimeters	Inches
A	13.97 ± 0.20	.55 ± .008
B	1.9	.075
C	1.27	.050
D	.64 ± .1	.025 ± .004
E	10.16	.400
F	1.9	.075
G	1.02	.040
H	2.17	.085
I	3.0 max	.120 max
J	11.43 ± .15	.450 ± .006
K	7.62	.300
L	1.27 ± .15	.050 ± .006
M	7.11 dia	.280 dia



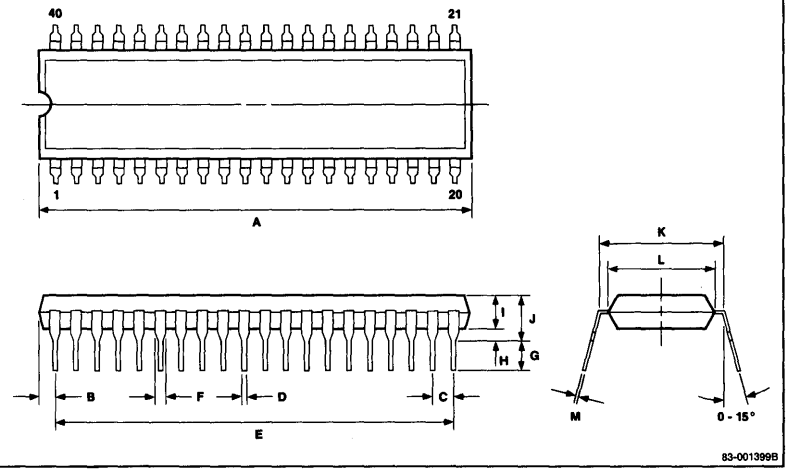
40-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	48.26	1.900
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



40-Pin Cerdip (600 mil, Wide Body)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	48.26	1.900
F	1.2 min	.047 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	.25 ± .05	$.010^{+.002}_{-.003}$
N	8.89 dia	.350 dia

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.