400042

National Semiconductor

INTERFACE: Data Transmission Databook

Special Interface
LVDS Technology
Line Drivers and Receivers

Introducing Low Voltage Differential Signaling (LVDS) Technology

INTERFACE: DATA TRANSMISSION

DATABOOK

1994 Edition

TIA/EIA-232 (RS-232)

TIA/EIA-422 and 423

TIA/EIA-485

Low Voltage Differential Signaling

Special Interface

General Purpose Line Drivers

General Purpose Receivers

Application Notes

Military Interface

Appendices and Physical Dimensions

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Introduction

Since its creation in 1973, National Semiconductor's Interface design and production teams have continuously produced technically advanced products unparalleled in the semiconductor industry.

Growing from a line of early drivers and receivers, which pioneered the introduction of the TRI-STATE® function, National Semiconductor's Data Transmission product line today is the most comprehensive available—with over 150 devices in a variety of product categories. These Interface devices support and complement National's VLSI product families.

Based on its advance design and process capabilities, National's Data Transmission product line includes:

- The industry's first CMOS TIA/EIA-232 (RS-232) Drivers and Receivers
- The industry's first CMOS TIA/EIA-422 (RS-422) Drivers and Receivers
- The industry's widest selection of TIA/EIA-485 (RS-485) Drivers, Receivers, Transceivers, and Repeaters
- The industry's first TIA/EIA-485 (RS-485) type Military Qualified (883) Transceivers, Drivers and Receivers
- The industry's first TIA/EIA-485 (RS-485) Quad Transceiver
- The industry's first TIA/EIA-485 (RS-485) BiCMOS Hex Transceiver
- The industry's first 3.3V powered RS-232 3 Driver X 5 Receiver Device for Laptop and Notebook Applications
- The industry's first LVDS—Low Voltage Differential Signaling Quad Drivers and Receivers for applications requiring ultra low power dissipation and switching rates exceeding 65 MHz

In addition to the detailed data transmission product datasheets, this databook includes the following documents to speed component selection and for technical reference: Selection Guides, Cross References, Package Drawings, and over 25 application notes devoted solely to the topic of Data Transmission.

For applications support or product information on National Semiconductor's Interface: Data Transmission Products, please contact the:

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The data sheet is printed for reference information only.

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***Boldface denotes new product Introduction and Application Notes.**

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Line Drivers and Receivers Selection Guide

The common purpose of transmission line drivers and receivers is to transmit data quickly and reliably through a variety of environments over electrically long distances. This task is complicated by the fact that externally introduced noise and ground shifts can severely degrade the data.

The connection between two elements in a system should be considered a transmission line if the transmitted signal takes longer than half its rise or fall time to travel from the driver to the receiver.

The Electronics Industry Association (EIA) and the Telecommunications Industry Association (TIA) have developed several standards to simplify the interface in data communications systems. Previously, EIA labeled the standards with the prefix "RS", which stood for recommended standard. This has been deleted and replaced with TIA/EIA, to help identify the standardizing organizations. The letter suffix represents the revision level of the standard. For example TIA/EIA-232-E denotes the fifth revision of RS-232.

All new and revised standards (EIA, EIA/TIA, and TIA/EIA) will adopt the new prefix nomenclature of TIA/EIA. Existing standards utilize the prefix that was current at the time the standard was balloted (approved). This includes the familiar RS, EIA, and EIA/TIA prefix. Looking forward, this selection guide adopts the TIA/EIA prefix for all TIA-EIA data transmission standards.

Single-Ended Data Transmission

In data processing systems today there are two basic means of communicating between components. One method is single-ended, which uses only one signal line for data transmission, and the other is differential, which uses two signal lines.

TIA/EIA-232-E (RS-232)

The first of these, "RS-232", was introduced in 1962 and has been widely used throughout the industry. TIA/EIA-232-E was developed for single-ended data transmission at relatively slow data rates (20 kbps) over short distances (typically up to ~50 ft.).

TIA/EIA-423-A (RS-423)

With the need to transmit data faster and over longer distances, TIA/EIA-423-A, a newer standard for single-ended applications, was established. TIA/EIA-423-A extends the maximum data rate to 100 kbps (up to 30 ft.) and the maximum distance to 4000 feet (up to 1 kbps). TIA/EIA-423-A also requires high impedance driver outputs with power off to not load the transmission line.

Differential Data Transmission

When transmitting at very high data rates, over long distances and through noisy environments, single-ended transmission is often inadequate. In these applications, differential data transmission offers superior performance. Differential transmission nullifies the effects of ground shifts and noise signals which appear as common mode voltages on the transmission line.

TIA/EIA-422-A (RS-422)

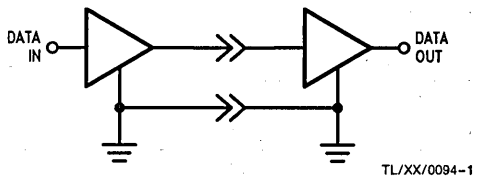
TIA/EIA-422-A was defined by the EIA for this purpose and allows data rates up to 10 Mbps (up to 40 ft.) and line lengths up to 4000 feet (up to 100 kbps).

Drivers designed to meet this standard are well suited for party-line type applications where only one driver is connected to, and transmits on, a bus and up to 10 receivers can receive the data. While a party-line type of application has many uses, TIA/EIA-422-A devices cannot be used to construct a truly multipoint bus. A multipoint bus consists of multiple drivers and receivers connected to a single bus, and any one of them can transmit or receive data.

TIA/EIA-485 (RS-485)

To meet the need for truly multipoint communications, the EIA established TIA/EIA-485 in 1983. TIA/EIA-485 meets all the requirements of TIA/EIA-422-A, but in addition, this new standard allows up to 32 drivers and 32 receivers to be connected to a single bus—thus allowing a truly multipoint bus to be constructed.

TIA/EIA-232-E Application



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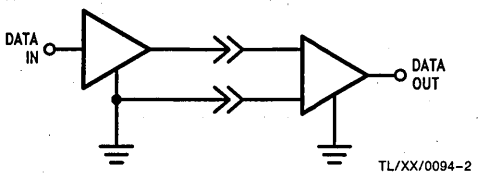
TIA/EIA-423-A Application



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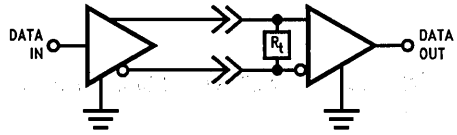
Differential Data Transmission (Continued)

TIA/EIA-422-A Application



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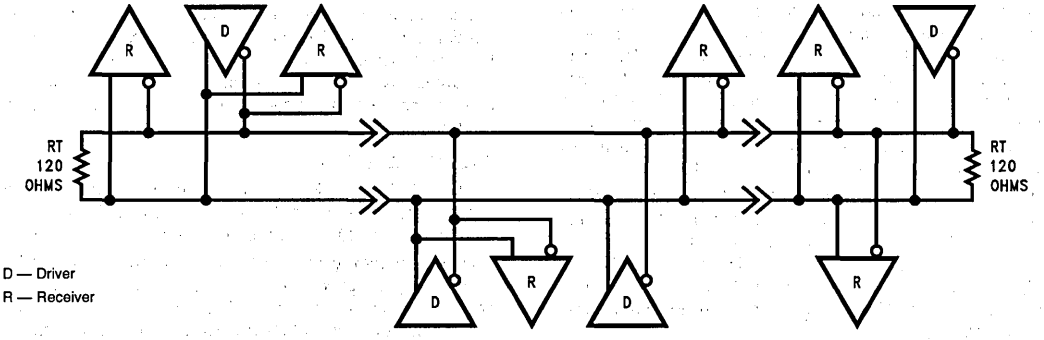
The key features of TIA/EIA-485:

- Implements a truly multipoint bus consisting of up to 32 drivers and 32 receivers (32 unit loads).
- An extended common-mode range for both drivers and receivers in TRI-STATE and with power off (−7V to +12V).
- Drivers can withstand bus contention and bus faults.

National Semiconductor produces a variety of drivers, receivers, and transceivers for these four very popular transmission standards and numerous other data transmission requirements.

Shown below is a table that highlights key aspects of the TIA/EIA Standards. More detailed comparisons can be found in the various application notes located in Section 8 of this databook.

TIA/EIA-485 Application



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Specification		TIA/EIA-232-E	TIA/EIA-423-A	TIA/EIA-422-A	TIA/EIA-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers Allowed on One Line		1 Driver, 1 Receiver	1 Driver, 10 Receivers	1 Driver, 10 Receivers	32 Drivers, 32 Receivers
Maximum Cable Length		~50 feet	4000 feet	4000 feet	4000 feet
Maximum Data Rate		20 kb/s	100 kb/s	10 Mb/s	10 Mb/s
Driver Output Maximum Voltage		±25V	±6V	−0.25V to +6V	−7V to +12V
Driver Output Signal Level	Loaded	±5V to ±15V	±3.6V	±2V	±1.5V
	Unloaded	±25V	±6V	±6V	±6V
Driver Load Impedance		3 kΩ to 7 kΩ	≥450Ω	100Ω	54Ω
Maximum Driver Output Current (High Impedance State)	Power On	——	——	——	±100 μA
	Power Off	±6.6 mA (±2V)	±100 μA	±100 μA	±100 μA
Slew Rate		30 V/μs max	Controls Provided	——	——
Receiver Input Voltage Range		±15V	±12V	−10V to +10V	−7V to +12V
Receiver Input Sensitivity		±3V	±200 mV	±200 mV	±200 mV
Receiver Input Resistance		3 kΩ to 7 kΩ	4 kΩ min	4 kΩ min	~ ≥ 12 kΩ

See TIA/EIA Standards for exact conditions. For reference, the "as published" nomenclature of the TIA/EIA Standards are listed below:

EIA/TIA-232-E-1991
EIA RS-422-A-1978
EIA RS-423-A-1978
EIA RS-485-1983
EIA/TIA-562-1989

TIA/EIA-232 UNBALANCED LINE DRIVERS

Device Number			Number of Drivers	Power Supplies V_{CC}/V_{EE} (V)	Max I_{CC} (mA)	Max I_{EE} (mA)	Typical I_O (mA)	Min V_O (V)	Typical Prop. Delay (ns)	Slew Rate Control	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military											
0°C to +70°C	−40°C to +85°C	−55°C to +125°C											
DS1488			4	±9 to ±15	25	−23	±6	±6/±9	230	External Cap.	N, J, M		1-63
DS14C88	DS14C88T		4	±5 to ±12	0.5	−0.06	±10	±3/±9	1500	Internal	N, J, M	Low Power CMOS	1-59
DS75150			2	±12	22	−20	±10	±5	60	External Cap.	N, M		1-74
		DS9616HM	3	±12	25	−25	—	±5	—	External Cap.	J, E		1-83

TIA/EIA-232 UNBALANCED RECEIVERS

Device Number			Number of Receivers	Power Supply V_{CC} (V)	Max I_{CC} (mA)	Typical Prop. Delay (ns)	Response Control	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military								
0°C to +70°C	−40°C to +85°C	−55°C to +125°C								
DS1489			4	5	26	28	External Cap.	N, J, M	Noise Filter, Adjustable Thresholds	1-70
DS1489A			4	5	26	28	External Cap.	N, M	Noise Filter, Adjustable Thresholds	1-70
DS14C89A	DS14C89AT		4	5	0.9/2.0	3500	Internal	N, J, M	Low Power CMOS Device	1-67
DS75154			4	5 or 12	35/40	22	—	N, M		1-78
		DS9627M	2	±12	18/−16		—	J		1-87

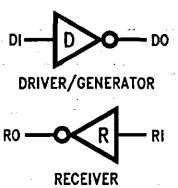
TIA/EIA-232 UNBALANCED LINE DRIVERS AND RECEIVERS (Continued)

Device Number		Number of Drivers	Number of Receivers	Number of External Caps	Nom. Cap. (μF)	Shutdown Mode	Rec. Output TRI-STATE	Power Supply (V)	Max I_{CC} (mA)	Packages	Page #
0°C to +70°C	−40°C to +85°C										
DS14C232C	DS14C232T	2	2	2	1.0	No	No	+5	3.0	M, N, WM	1-8
DS14C237	DS14C237T	5	3	4	1.0	No	No	+5	10	N, WM	1-17
DS14C238	DS14C238T	4	4	4	1.0	No	No	+5	10	N, WM	1-21
DS14C239	DS14C239T	3	5	2	1.0	No	Yes	+5, +7.5−+13.2	TBD	N, WM	1-26
DS14C241	DS14C241T	4	5	4	1.0	Yes	Yes	+5	10	WM	1-31
DS14C335	DS14C335T	3	5	4	0.47	Yes	No	3.3V	20	MSA	1-38
DS14C561*		4	5	4	1.0	Yes	Yes	3.3V	6	WM	1-54

Characteristics of an TIA/EIA-232-E Device:

DRIVER/GENERATOR:
Minimum driver high output voltage with 3 kΩ load — +5V
Minimum driver low output voltage with 3 kΩ load — −5V
Power off driver output resistance (V_O = ±2V) — ≥300Ω
Typical maximum data rate — 20 kb/s
Maximum driver slew rate — ≤30 V/μs
See TIA/EIA Standard TIA/EIA-232-E for exact conditions.

RECEIVERS:
Receiver input voltage range — ±15V
Receiver input sensitivity — ±3V
Receiver input resistance — >3 kΩ and <7 kΩ



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NEW DEVICES:

DS14185 TIA/EIA-232 3x5 Driver/Receiver (Page 1-3)
DS14C535 +5V Supply TIA/EIA-232 3x5 Driver/Receiver (Page 1-47)

***Note:** DS14C561 is 232 compatible only, and conforms to TIA/EIA-562.
See Datasheets for Complete Specifications.

TIA/EIA-422 BALANCED LINE DRIVERS

Device Number			Number of Drivers	Power Supply V_{CC} (V)	Min V_{OH} (V)	Rated I_{OH} (mA)	Max V_{OL} (V)	Rated I_{OL} (mA)	Max I_{CC} (mA)	Typ Prop. Delay (ns)	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military											
0°C to +70°C	−40°C to +85°C	−55°C to +125°C											
	DS26C31T	DS26C31M	4	5	2.5	−20	0.5	20	0.5	6	N, J, M, E, W	Low Power	2-10
DS26F31C		DS26F31M	4	5	2.5	−20	0.5	20	50	10	J, E, W		2-18
DS26LS31C		DS26LS31M	4	5	2.5	−20	0.5	20	60	10	N, J, M, W		2-21
DS3487			4	5	2.5	−20	0.5	48	80	10	N, M		2-61
	DS34C87T		4	5	2.5	−20	0.5	48	0.5	6	N, J, M	Low Power	2-52
DS34F87		DS35F87	4	5	2.5	−20	0.5	48	50	—	N, J		2-57
DS3691		DS1691A	2	5 or ±5	—	—	—	—	30	120	N, J, M, V	422 or 423	2-3
DS8921			1D/1R*	5	2.5	−20	0.5	20	35	10	N, M	Transceiver	2-83
DS8921A	DS8921AT		1D/1R*	5	2.5	−20	0.5	20	35	10	N, J, M	Low Skew	2-83
	DS89C21T		1D/1R*	5	3.8	−6	0.3	6	6	10	N, M	Low Power	2-88
DS8922			2D/2R*	5	2.5	−20	0.5	20	78	12	N, M	Dual Transceiver	2-93
DS8922A			2D/2R*	5	2.5	−20	0.5	20	78	12	N, M	Low Skew	2-93
DS8923			2D/2R*	5	2.5	−20	0.5	20	78	12	N, M	Dual Transceiver	2-93
DS8923A			2D/2R*	5	2.5	−20	0.5	20	78	12	N, M	Low Skew	2-93
DS9638C		DS9638M	2	5	2	−40	0.5	40	65	10	N, J, M		2-120

Characteristics of an TIA/EIA-422-A Line Driver:

Minimum driver output voltage with 100Ω test termination load — Greater than |2V| or 50% of unloaded output voltage

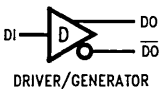
Driver output resistance — <100Ω

Driver output short circuit current (V_O = 0V) — ≤150 mA

Driver power off current (V_O = −250 mV to +6V) — ≤|100 μA|

Typical maximum data rate — 10 Mb/s

See TIA/EIA Standard TIA/EIA-422-A for exact conditions.



DRIVER/GENERATOR

TL/XX/0094-6

NEW DEVICE:

DS8925 LocalTalk™ Dual Driver/Triple Receiver (Page 2-103)

*This device includes both driver(s) and receiver(s).

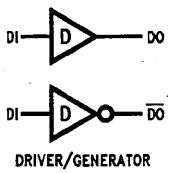
See Datasheets for Complete Specifications

TIA/EIA-423 UNBALANCED LINE DRIVERS

Device Number		Number of Drivers per Package	Power Supplies V_{CC}/V_{EE} (V)	Max Supply Current I_{CC}/I_{EE} (mA)	Min V_O (V)	Typical I_{OS} (mA)	Typical Prop. Delay (ns)	Slew Rate Control	Packages	Comments and Special Features	Page #
Commercial	Military										
0°C to +70°C	−55°C to +125°C										
DS3691	DS1691A	4	±5	30/−22	±4	±80	180	External Cap.	N, J, M, V	422 or 423	2-3
DS9636AC	DS9636A/M	2	±12	18/−18	±4	±60	—	External Res.	N, J	One Resistor Sets Slew Rate	2-111

Characteristics of an TIA/EIA-423-A line driver:

Minimum driver output voltage with 450Ω load — ≥|3.6V|
Driver output resistance — <50Ω
Driver output short circuit current (V_O = 0V) — ≤|150 mA|
Maximum driver output voltage — ±6V
Driver power off current (V_O = ±6V) — ≤|100 μA|
Typical maximum data rate — 100 kbps
See TIA/EIA Standard TIA/EIA-423-A for exact conditions.



DRIVER/GENERATOR

TL/XX/0094–7

NEW DEVICE:
DS8925 LocalTalk™ Dual Driver/Triple Receiver (Page 2-103)

See Datasheets for Complete Specifications

TIA/EIA-422 and TIA/EIA-423 BALANCED RECEIVERS

Device Number			Number of Receivers	Power Supply V_{CC} (V)	Max I_{CC} (mA)	Typ Prop. Delay (ns)	Max VCM (V)	Output Stage	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military									
0°C to +70°C	−40°C to +85°C	−55°C to +125°C									
	DS26C32AT	DS26C32AM	4	5	23/25	19	±14	TRI-STATE	N, J, M, W, E	Low Power CMOS Device	2-25
DS26F32C		DS26F32M	4	5	50	15	±25	TRI-STATE	W, J, E		2-32
DS26LS32C		DS26LS32M	4	5	70	17	±25	TRI-STATE	N, J, M, W		2-36
DS26LS32AC			4	5	70	23	±25	TRI-STATE	N, M	Failsafe Feature	2-36
	DS34C86T		4	5	23	19	±14	TRI-STATE	N, J, M	Low Power CMOS Device	2-39
DS34F86		DS35F86	4	5	50	15	±15	TRI-STATE	J		2-44
DS3486			4	5	85	19	±25	TRI-STATE	N, J, M		2-48
DS88C20		DS78C20	2	5 to 15	15/30	100	±25	Strobe	N, J	Response Control	2-64
DS88C120		DS78C120	2	5 to 15	15/30	100	±25	Strobe	N, J	Response Control, Failsafe	2-68
DS88LS120		DS78LS120	2	5	16	38	±25	Strobe	N, J, W		2-76
DS8921			1D/1R*	5	35	14	±10	—	N, M	Transceiver	2-83
DS8921A	DS8921AT		1D/1R*	5	35	14	±10	—	N, J, M	Low Skew Transceiver	2-83
	DS89C21T		1D/1R*	5	6	30	±14	—	N, M	Low Power	2-88
DS8922			2D/2R*	5	78	12	±10	TRI-STATE	N, M	Dual Transceiver	2-93
DS8922A			2D/2R*	5	78	12	±10	TRI-STATE	N, M	Low Skew Dual Transceiver	2-93
DS8923			2D/2R*	5	78	12	±10	TRI-STATE	N, M	Dual Transceiver	2-93
DS8923A			2D/2R*	5	78	12	±10	TRI-STATE	N, M	Low Skew Dual Transceiver	2-93
DS9637AC		DS9637AM	2	5	50	15	±15	—	N, J, M		2-115
DS9639AC			2	5	50	55	±15	—	N		2-124

Characteristics of an TIA/EIA-422-A / 423-A Receiver:

Receiver common mode voltage range — ±7V
Receiver sensitivity over ±10V common mode — ±200 mV
Maximum differential input voltage — ±12V
Minimum receiver input impedance — 4 kΩ

See TIA/EIA Standard TIA/EIA-422-A or TIA/EIA-423-A for exact conditions.

RECEIVER

TL/XX/0094–8

NEW DEVICE:

DS8925 LocalTalk™ Dual Driver/Triple Receiver (Page 2-103)

*This device includes both Driver(s) and Receiver(s).

See Datasheets for Complete Specifications

TIA/EIA-485 BALANCED LINE DRIVERS, RECEIVERS AND TRANSCEIVERS

Device Number			Number of Drivers	Number of Receivers	Max I_{CC} (mA)	Typ. Driver Prop. Delay (ns)	Typ. Receiver Prop. Delay (ns)	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military								
0°C to +70°C	−40°C to +85°C	−55°C to +125°C								
DS36F95		DS16F95	1	1	28	12	19	W, J, E	Low Power	3-18
DS3695	DS3695T		1	1	60	15	25	N, J		3-3
DS3696	DS3696T		1	1	60	15	25	N, J	Thermal Shutdown Reporting	3-3
DS3697			1	1	60	15	25	N	Repeater	3-3
DS3698			1	1	60	15	25	N	Repeater, Thermal Shutdown Reporting	3-3
DS3695A	DS3695AT		1	1	60	15	25	M	SOIC Package	3-12
DS3696A			1	1	60	15	25	M	SOIC Package, Thermal Shutdown Reporting	3-12
DS75176B	DS75176BT		1	1	55	17	32	N, M		3-79
DS96F172C		DS96F172M	4	0	50	12	—	N, W, J, E	Low Power, Common Enable	3-89
DS96F174C		DS96F174M	4	0	50	12	—	W, J, E	Low Power, Enable Pair	3-89
DS96172C			4	0	70	12	—	N, J	Common Enable	3-84
DS96174C			4	0	70	12	—	N, J	Enable Pair	3-84
DS96F173C		DS96F173M	0	4	50	—	15	W, J, E	Low Power, Common Enable	3-102
DS96F175C		DS96F175M	0	4	50	—	15	W, J, E	Low Power, Enable Pair	3-102
DS96173C			0	4	75	—	15	N, J		3-97
DS96175C			0	4	75	—	15	N, J		3-97
DS96176C			1	1	35	12	16	N, J		3-110
DS96177C			1	1	35	12	16	N	Repeater	3-120
DS36276			1	1	60	60	60	M, N	Failsafe RS-485 Compatible—**NEW**	3-28
	DS36277T		1	1	60	60	90	M, N	Dominant Mode RS-485 Compatible—**NEW**	3-40
DS36950			4	4	90	15	14	V	QUAD Transceiver, IPI Applications	3-52
DS36954			4	4	90	15	14	V	QUAD Transceiver, SCSI Applications	3-61
DS36BC956			6	6	—	—	—	MEA	HEX Transceiver—**NEW**	3-68

Characteristics of an TIA/EIA-485 Device:

RECEIVERS:

Receiver common mode voltage range — −7V to +12V

Receiver sensitivity over common mode range — ±200 mV

Typical receiver input impedance — 12 kΩ

See TIA/EIA Standard TIA/EIA-485 for exact conditions.

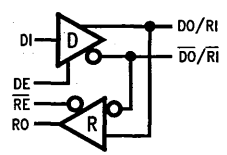
DRIVERS:

Minimum driver output voltage with 54Ω load — $\geq|1.5V|$

Driver output short circuit current (V_O = −7V to +12V) — $\leq|250$ mA$|$

Maximum driver output offset voltage — 3V

Typical maximum data rate — 10 Mb/s.



TYPICAL TRANSCEIVER

TL/XX/0094–9

See Datasheets for Complete Specifications

BALANCED AND UNBALANCED LINE DRIVERS

Standard	Device Number		Type of Driver	Number of Drivers	Power Supply V_{CC} (V)	Max I_{CC} (mA)	Output Stage	Output Voltage Min V_O (V)	Output Current I_O (mA)	Typical Prop. Delay (ns)	Packages	Page #
	Commercial	Military										
	0°C to +70°C	−55°C to +125°C										
188-114	DS3692	DS1692	Differential	2	5 or ±5	30/−22	TRI-STATE	±6	±20	190	N, J	6-3
—	DS75110A	DS55110A	Differential	2	±5	35/−50	TRI-STATE		±12	9	N, J, M	6-7
—	DS75113	DS55113	Differential	2	5	65	Note 2	3/0.2	±40	13	N, J, M	6-12
—	DS75114	DS9614M	Differential	2	5	50	Note 2	3/0.2	±40	15	N, J, W, E	6-19
—	DS75121		Single Ended	2	5	60	—	2.4	−100	11	N	6-24
IBM 360	DS75123		Single Ended	2	5	60	—	3.11	−100	12	N	6-26
—	DS8830	DS7830	Differential	2	5	18	—	1.8/0.5	±40	11	N, J, W	6-28
—	DS8831	DS7831	Note 1	2/4	5	90	TRI-STATE	1.8/0.5	±40	13	N, J, W	6-38
—	DS8832	DS7832	Note 1	2/4	5	90	TRI-STATE	1.8/0.5	±40	13	N, J, W	6-38
—	MM88C29	MM78C29	Single Ended	4	3 to 15						N, M, J, W	6-32
—	MM88C30	MM78C30	Differential	2	3 to 15						N, M, J, W	6-32

Note 1: Driver can be used in differential or single ended mode.

Note 2: Output features TRI-STATE, Choice of open collector or active pull-up.

See Datasheets for Complete Specifications

BALANCED AND UNBALANCED RECEIVERS

Standard	Device Number		Number of Receivers	Input Sensitivity (mV)	Power Supply V_{CC} (V)	Max I_{CC}/I_{EE} (mA)	Rated V_{CM} (V)	Typ. Prop. Delay (ns)	Packages	Output Stage	Comments and Special Features	Page #
	Commercial	Military										
	0°C to +70°C	−55°C to +125°C										
—	DS26LS33C	DS26LS33M	4	±500	5	80	±25	17	N, J, W	TRI-STATE	422/3 Type	2-36
—	DS26LS33AC		4	±500	5	80	±25	23	N	TRI-STATE	422/3 Type	2-36
—	DS3603	DS1603	2	±25	±5	40/−15	±3	17	N, J, W	TRI-STATE		7-3
—	DS3650		4	±25	±5	60/−30	±3	21	N, M	TRI-STATE		7-7
—	DS3652	DS1652	4	±25	±5	60/−30	±3	22	J, M	TRI-STATE	Note 1	7-7
—	DS75107/A	DS55107	2	±25	±5	30/−15	±3	17	N, J, M	Strobe		7-15
—	DS75108/A		2	±25	±5	30/−15	±3	19	N, M	Strobe	Note 1	7-15
—	DS75208		2	±10	±5	30/−15	±3		N, J	Strobe		7-15
—	DS75115	DS9615M	2	±500	5	50	±15	20	N, J, W, E	Strobe	Response Control	7-22
—		DS55122	3	—	5	72	6	20	J, W	Strobe		7-27
IBM 360	DS75124		3	—	5	72	7	20	N	Strobe		7-30
IBM 360/370	DS75129		8	—	5	53	7	18	N	Strobe		7-33
—	DS8820	DS7820	2	1000	5	10.2	±15	150	N, J, W	Strobe	Response Control	7-37
—	DS8820A	DS7820A	2	1000	5	10.2	±15	30	N, J, W	Strobe	Response Control	7-41
		DS9622M	2	—	5	22.9/−11.1	±15	50	J, W, E		Open Collector	7-46

Note 1: Open collector output stage.

See Datasheets for Complete Specifications

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Line Driver and Receiver Cross Reference Guide

The Line Driver and Receiver Cross Reference Guide is provided as an aid in identifying replacement part numbers. Direct replacements feature identical pin-outs and very similar electrical specifications. Similar replacements also feature the same pin-out, and similar electrical specifications. Consult the data sheets for recommended operating conditions and package availability. Before replacing a specific product, it is recommended to compare electrical, functional, and mechanical specifications. Interchangeability between devices is not guaranteed. Manufacturers' most current data sheets take precedence over this guide.

AMD to National		
Device	**Direct**	**Similar**
AM26LS30	DS3691	
AM26LS31	DS26LS31	
AM26LS32	DS26LS32A	
AM26LS33	DS26LS33A	
AM26LS32B		DS26F32
AM26LS34		DS96173

Motorola to National		
Device	**Direct**	**Similar**
AM26LS30	DS3691	
AM26LS31	DS26LS31	
AM26LS32		DS26LS32A
MC1488	DS1488	
MC1489	DS1489	
MC1489A	DS1489A	
MC3450	DS3650	
MC3452	DS3652	
MC3486	DS3486	
MC3487	DS3487	
MC3488	DS9636A	
MC55107		DS55107
MC55S110		DS55110A
MC75107	DS75107	
MC75108	DS75108	
MC75S110	DS75110A	
MC75129	DS75129	
MC8T13		DS55121
MC8T14		DS55122
MC8T24		DS75124
SN75172	DS96172C	
SN75173	DS96173C	
SN75174	DS96174C	
SN75175	DS96175C	
SN75176	DS75176B	
SN75177	DS96177C	

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Line Driver and Receiver Cross Reference Guide

Signetics to National		
Device	**Direct**	**Similar**
AM26LS30	DS3691	
AM26LS31	DS26LS31	
AM26LS32	DS26LS32A	
AM26LS33	DS26LS33A	
DS7820	DS7820	
DS7830	DS7830	
DS8820	DS8820	
DS8830	DS8830	
MC1488	DS1488	
MC1489	DS1489	
MC1489A	DS1489A	
8T13	DS75121	
8T14	DS55122	
8T23	DS75123	
8T24	DS75124	
8T129	DS75129	

TI to National		
Device	**Direct**	**Similar**
AM26LS31	DS26LS31	
AM26LS32A	DS26LS32A	
AM26LS33A	DS26LS33A	
MAX232	DS14C232	
MC3486	DS3486	
MC3487	DS3487	
SN55107B	DS55107	
SN55108B	DS55108	
SN55110A	DS55110A	
SN55113	DS55113	
SN55114	DS9614	
SN55115	DS9615	
SN55121	DS55121	
SN55122	DS55122	
SN55173		DS96F173M
SN55182	DS7820A	
SN55183	DS7830	
SN55ALS192		DS26C31M
SN55ALS194		DS35F87
SN55ALS195		DS35F86
SN65176B	DS75176BT	
SN65ALS176		DS75176BT
SN65C188	DS14C88T	
SN65C189A	DS14C89AT	
SN75107B	DS75107	
SN75108B	DS75108	
SN75110A	DS75110A	
SN75113	DS75113	
SN75114	DS75114	
SN75115	DS75115	
SN75121	DS75121	
SN75123	DS75123	
SN75124	DS75124	
SN75129	DS75129	
SN75146		DS9639A
SN75150	DS75150	
SN75154	DS75154	

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Line Driver and Receiver Cross Reference Guide

Texas Instruments to NSC		
Device	**Direct**	**Similar**
SN75172	DS96172C	
SN75173	DS96173C	
SN75174	DS96174C	
SN75175	DS96175C	
SN75176	DS96176C	
SN75176A	DS75176B	
SN75176B	DS75176B	
SN75177	DS96177C	
SN75177B	DS3697	
SN75182	DS8820A	
SN75183	DS8830	
SN75188	DS1488	
SN75189	DS1489	
SN75189A	DS1489A	
SN75ALS176	DS36F95	
SN75ALS191		DS9638
SN75ALS192		DS26C31C
SN75ALS193		DS26C32AC
SN75ALS194		DS34C87
SN75ALS195		DS34C86
SN75C188	DS14C88	
SN75C189A	DS14C89A	
SN75LBC241	DS14C241T	
SN75LV4737	DS14C335	
SN95176B	DS16F95	
TL3695	DS3695	
μA9636A	DS9636A	
μA9637A	DS9637A	
μA9638	DS9638	
μA9639	DS9639A	

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National/Fairchild Consolidation and Nomenclature Changes

Device Designation	Device Designation
Fairchild	National
μA1488DC	DS1488J
μA1488PC	DS1488N
μA1488SC	DS1488M
μA1489DC	DS1489J
μA1489PC	DS1489N
μA1489SC	DS1489M
μA1489APC	DS1489AN
μA26LS31DC	DS26LS31CJ
μA26LS31PC	DS26LS31CN
μA26LS32PC	DS26LS32ACN
μA3486DC	DS3486J
μA3486PC	DS3486N
μA3487PC	DS3487N
μA55107ADM	DS55107AJ
μA75107ADC	DS75107AJ
μA75107APC	DS75107AN
μA75107ASC	DS75107AM
μA75107BDC	DS75107J
μA75107BPC	DS75107N
μA75107BSC	DS75107M
μA75108BPC	DS75108N
μA75108BSC	DS75108M
μA75110APC	DS75110AN
μA75110ASC	DS75110AM
μA75150TC	DS75150N
μA75150SC	DS75150M
μA75154PC	DS75154N

*Contact Product Marketing

Device Designation	Device Designation
Fairchild	National
μA9614DM	*
μA9614PC	DS75114N
μA9615DM	*
μA9615PC	DS75115N
μA96172DC	DS96172CJ
μA96172PC	DS96172CN
μA96174DC	DS96174CJ
μA96174PC	DS96174CN
μA96173DC	DS96173CJ
μA96173PC	DS96173CN
μA96175DC	DS96175CJ
μA96175PC	DS96175CN
μA96176RC	DS96176CJ
μA96176TC	DS96176CN
μA96177TC	DS96177CN
μA9636ARM	DS9636AMJ
μA9636ARC	DS9636ACJ
μA9636ATC	DS9636ACN
μA9637ARM	DS9637AMJ
μA9637ARC	DS9637ACJ
μA9637ATC	DS9637ACN
μA9637ASC	DS9637ACM
μA9638RM	DS9638MJ
μA9638RC	DS9638CJ
μA9638TC	DS9638CN
μA9639ATC	DS9639ACN

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National/Fairchild Consolidation and Nomenclature Changes

Device Designation	Device Designation
MIL/AREO FSC	**MIL/AREO NSC**
μA55107ADMQB	DS55107AJ/883
μA55110ADMQB	DS55110AJ/883
μA9614DMQB	DS9614MJ/883
μA9614FMQB	DS9614MW/883
μA9614LMQB	DS9614ME/883
μA9615DMQB	DS9615MJ/883
μA9615FMQB	DS9615MW/883
μA9615LMQB	DS9615ME/883
μA9616HDMQB	DS9616HMJ/883
μA9616HLMQB	DS9616HME/883
μA9622DMQB	DS9622MJ/883
μA9622LMQB	DS9622ME/883
μA9622FMQB	DS9622MW/883
μA9627DMQB	DS9627MJ/883
μA9636ARMQB	DS9636AJ/883
μA9637ARMQB	DS9637AMJ/883
μA9638RMQB	DS9638MJ/883
μA55110ADMQM	SMD-8754701CA
μA9622DMQM	SMD-8752201CA
μA9622FMQM	SMD-8752201AA
μA9638RMQM	SMD-8754601PA

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Extended Temperature Range Devices

Line Drivers and Receivers

Commercial		Military	
−40°C to +85°C	−55°C to +125°C	883	MLS
DS14C88T	DS1691A	DS14C232	DS16F95
DS14C89AT	DS1692	DS1603	DS26C31M
DS14C232T	DS16F95	DS1652	DS26C32AM
DS14C237T	DS26F31M	DS1691A	DS26F31M
DS14C238T	DS26LS31M	DS16F95	DS26F32M
DS14C239T	DS26F32M	DS26C31M	DS26F33M
DS14C241T	DS26LS32M	DS26F31M	DS26LS31M
DS14C335T	DS26LS33M	DS26LS31M	DS26LS32AM
DS26C31T	DS35F86	DS26C32AM	DS26LS33M
DS26C32AT	DS35F87	DS26F32M	DS55115
DS34C86T	DS55107	DS26LS32M	DS78C120
DS34C87T	DS55107A	DS26LS33M	DS78LS120
DS3695T	DS55113	DS55107A	DS7820A
DS3695AT	DS7820	DS55110A	DS7820
DS3696T	DS7820A	DS55113	DS7830
DS36277T	DS78C20	DS55115	DS9615M
DS75176BT	DS9636AM	DS55122	DS9638M
DS8921AT	DS9637AM	DS7820	DS96F174M
DS89C21T	DS9638M	DS7820A	DS96F175M
MM88C29	DS96F172M	DS78C20	
MM88C30	DS96F173M	DS7830	
	DS96F174M	DS7831	
	DS96F175M	DS7832	
		DS78C120	
		DS78LS120	
		DS9614M	
		DS9615M	
		DS9616HM	
		DS9622M	
		DS9627M	
		DS9636A	
		DS9637AM	
		DS9638M	
		DS96F172M	
		DS96F173M	
		DS96F174M	
		DS96F175M	
		MM78C29	
		MM78C30	

Note 1: Package suffix is not shown, see Datasheet.

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New Additions to the Interface: Data Transmission Databook

Datasheets:

DS14C335	+3.3V Supply TIA/EIA-232 3 X 5 Driver/Receiver	RS-232
DS14C535	+5V Supply TIA/EIA-232 3 X 5 Driver/Receiver	RS-232
DS14185	TIA/EIA-232 3 X 5 Driver/Receiver	RS-232
DS89C21	Differential CMOS Line Driver and Receiver Pair	RS-422
DS8925	LocalTalk™ Dual Driver/Triple Receiver	RS-422/3
DS36276	Failsafe Multipoint Transceiver	~RS-485
DS36277	Dominant Mode Multipoint Transceiver	~RS-485
DS36BC956	Lower Power BiCMOS HEX Differential Transceiver	RS-485
DS90C031	LVDS Quad CMOS Differential Line Driver	LVDS
DS90C032	LVDS Quad CMOS Differential Line Receiver	LVDS
DS36001	Serial Link Input Output Device	

Application Notes:

AN-847	Failsafe Biasing of Differential Buses
AN-876	Inter-operation of the DS14C335 with +5V UARTs
AN-878	Increasing System ESD Tolerance for Line Drivers and Receivers used in RS-232 Interfaces
AN-903	A Comparison of Differential Termination Techniques
AN-904	An Introduction to the Differential SCSI Interface
AN-912	Common Data Transmission Parameters and their Definitions
AN-914	Understanding Power Requirements in RS-232 Applications
AN-915	Automotive Physical layer SAE J1708 and the DS36277
AN-916	A Practical Guide to Cable Selection
AN-917	Popular Connector Pin Assignments for Data Communication

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Application Note—Selection Guide

Application Note Number AN-XXX	Title	DTP Devices Referenced	TIA/EIA Standards Referenced
AN-22	Integrated Circuits for Digital Data Transmission	DS7830/DS8830, DS7820/DS8820	
AN-108	Transmission Line Characteristics	DS7820/DS8820	
AN-214	Transmission Line Drivers and Receivers for EIA Standards, RS-422 and RS-423	DS3691, DS88LS120	422 423
AN-216	Summary of Well Known Interface Standards		ALL
AN-336	Understanding Integrated Circuit Package Power Capabilities		
AN-409	Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard	DS3695/DS3696, DS3697/DS3698	485
AN-438	Low Power RS-232C Driver and Receiver in CMOS	DS14C88, DS14C89A	232
AN-450	Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability		
AN-454	Automotive Multiplex Wiring	DS75176B DS3695	485
AN-457	High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Programs	DS8921/A, DS8922/A, DS8923/A	422
AN-643	EMI/RFI Board Design		
AN-702	Build a Directional-Sensing Bidirectional Repeater	DS75176B, DS96175C	485
AN-759	Comparing EIA-485 and EIA-422-A Line Drivers and Receivers in Multipoint Applications		422 485
AN-805	Calculating Power Dissipation for Differential Line Drivers	DS26LS31, DS96F172	422 485
AN-806	Data Transmission Lines and Their Characteristics		
AN-807	Reflections: Computations and Waveforms		
AN-808	Long Transmission Lines and Data Signal Quality		
AN-847	FAILSAFE Biasing of Differential Buses	DS3695, DS96172, DS96F172	422 485
AN-876	Inter-Operation of the DS14C335 with +5V UARTs	DS14C335	232
AN-878	Increasing System ESD Tolerance for Line Drivers and Receivers used in RS-232 Interfaces	DS1488, DS1489A	232

Application Note—Selection Guide (Continued)

Application Note Number AN-XXX	Title	DTP Devices Referenced	TIA/EIA Standards Referenced
AN-903	A Comparison of Differential Termination Techniques		422 485
AN-904	An Introduction to the Differential SCSI Interface	DS36954 DS36BC956	485
AN-912	Common Data Transmission Parameters and their Definitions		All
AN-914	Understanding Power Requirements in RS-232 Applications	DS14C335	232 562
AN-915	Automotive Physical Layer SAE J1708 and the DS36277	DS36277 DS75176B	485
AN-916	A Practical Guide to Cable Selection		All
AN-917	Popular Connector Pin Assignments for Data Communication		All

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Cross Reference for Related Products

(Device Type/Family to National Databook Title)

Backplane Transceiver Logic (BTL)
TTL Bus Drivers
GPIB (IEEE-488) Transceivers
- HIGH PERFORMANCE BUS INTERFACE DESIGNER'S GUIDE

IBM Communications—3270
- IBM DATA COMMUNICATIONS HANDBOOK

ECL Line Drivers and Receivers
- F100K ECL LOGIC DATABOOK AND DESIGNER'S GUIDE

SCSI Controllers
- MASS STORAGE HANDBOOK

Standard Logic Line Drivers, Receivers, and Transceivers (244/245)
- ADVANCED BiCMOS LOGIC DATABOOK
- ALS/AS LOGIC DATABOOK
- CMOS LOGIC DATABOOK
- FACT™ ADVANCED CMOS LOGIC DATABOOK
- FAST® ADVANCED SCHOTTKY TTL LOGIC DATABOOK
- FAST® APPLICATIONS HANDBOOK

Display Drivers
- LINEAR APPLICATION SPECIFIC IC's DATABOOK

Peripheral Drivers
- POWER IC's DATABOOK

Section 1

TIA/EIA-232 (RS-232)

Section 1 Contents

National Semiconductor

ADVANCE INFORMATION

DS14185
TIA/EIA-232 3 Driver x 5 Receiver

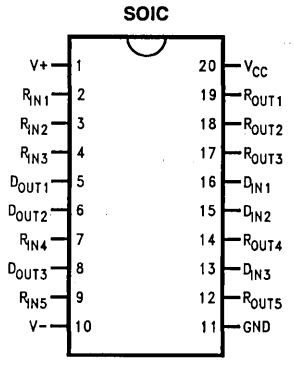
General Description

The DS14185 is a three driver, five receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device is constructed on a bipolar process. Driver slew rate control has been internalized to eliminate the need for external slew rate control capacitors.

Features

- Replaces one 1488 and two 1489's
- Conforms to TIA/EIA-232-E and V.28
- 3 drivers and 5 receivers
- ESD ≥ 2.5 kV
- Flow through pinout
- Failsafe receiver outputs
- 20-pin SOIC package
- Pin compatible with SN75C185

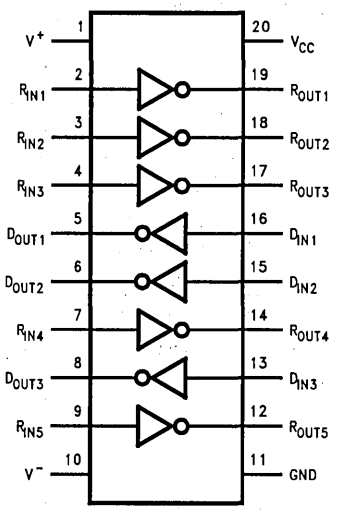
Connection Diagram



Pinout subject to change. TL/F/11938–1

Order Number DS14185M
See NS Package M20B

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+7V
Supply Voltage (V^+)	+15V
Supply Voltage (V^-)	−15V
Driver Input Voltage	0V to V_{CC}
Driver Output Voltage (Power Off)	±15V
Receiver Input Voltage	±25V
Receiver Output Voltage (R_{OUT})	0V to V_{CC}
Maximum Package Power Dissipation @ +25°C	
M Package	1488 mW
Derate M Package	11.9 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 4 seconds)	+260°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Supply Voltage (V^+)	+9.0	+12.0	+13.2	V
Supply Voltage (V^-)	−9.0	−12.0	−13.2	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
I_{CC}	V_{CC} Supply Current	No Load, All Inputs at +5V			18	33	mA
I^+	V^+ Supply Current	No load, All Inputs at 0.8V or +2V	$V^+ = 9V, V^- = -9V$		11.3	15	mA
			$V^+ = 13.2V, V^- = -13.2V$		14.3	21	mA
I^-	V^- Supply Current		$V^+ = 9V, V^- = -9V$		−9.8	−13	mA
			$V^+ = 13.2V, V^- = -13.2V$		−13.5	−19	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 5V$				10	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$				−1.3	mA
V_{OH}	High Level Output Voltage	$R_L = 3\,k\Omega, V_{IN} = 0.8V, V^+ = 9V, V^- = -9V$		6	7		V
		$R_L = 3\,k\Omega, V_{IN} = 0.8V, V^+ = +13.2V, V^- = -13.2V$		9	10.5		V
		$R_L = 7\,k\Omega, V_{IN} = 0.8V, V^+ = +13.2V, V^- = -13.2V$				13.2	V
V_{OL}	Low Level Output Voltage	$R_L = 3\,k\Omega, V_{IN} = 2V, V^+ = 9V, V^- = -9V$		−6	−6.8		V
		$R_L = 3\,k\Omega, V_{IN} = 2V, V^+ = +13.2V, V^- = -13.2V$		−9	−10.5		V
		$R_L = 7\,k\Omega, V_{IN} = 0.8V, V^+ = +13.2V, V^- = -13.2V$		−13.2			V
I_{OS}^+	Output High Short Circuit Current	$V_O = 0V, V_{IN} = 0.8V$		−6		−12	mA
I_{OS}^-	Output Low Short Circuit Current	$V_O = 0V, V_{IN} = 2.0V$		6		12	mA
R_O	Output Resistance	$-2V \le V_O \le +2V, V^+ = V^- = V_{CC} = 0V$		300			Ω
		$-2V \le V_O \le +2V, V^+ = V^- = V_{CC}$ = Open Ckt		300			Ω

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Note 2). (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS						
V_{TH}	Input High Threshold	$V_O \leq 0.4V$, $I_O = 3.2$ mA	1.55		2.4	V
V_{TL}	Input Low Threshold	$V_O \geq 2.5V$, $I_O = -0.5$ mA	0.65		1.35	V
R_{IN}	Input Resistance	$V_{IN} = \pm 3V$ to $\pm 15V$	3.0		7	kΩ
I_{IN}	Input Current	$V_{IN} = +15V$	3.6		8.3	mA
		$V_{IN} = +3V$	0.43		1	mA
		$V_{IN} = -15V$	−3.6		−8.3	mA
		$V_{IN} = -3V$	−0.43		−1	mA
V_{OH}	High Level Output Voltage (Note 7)	$I_{OH} = -0.5$ mA, $V_{IN} = -3V$	2.6			V
		$I_{OH} = -10$ μA, $V_{IN} = -3V$	4.0			V
		$I_{OH} = -0.5$ mA, V_{IN} = Open Circuit	2.6			
		$I_{OH} = -10$ μA, V_{IN} = Open Circuit	4.0			
V_{OL}	Low Level Output Voltage	$I_{OL} = 3.2$ mA, $V_{IN} = +3V$			0.4	V
I_{OSR}	Short Circuit Current	$V_O = 0V$, $V_{IN} = 0V$	−1.7		−4	mA

Switching Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 3$ kΩ, $C_L = 50$ pF (*Figures 1* and *2*)			2	μs
t_{PLH}	Propagation Delay Low to High	$R_L = 3$ kΩ, $C_L = 50$ pF (*Figures 1* and *2*)			2	μs
SR1	Output Slew Rate (Note 8)	$R_L = 3$ kΩ to 7 kΩ, $C_L = 50$ pF (*Figures 1* and *2*)	4		30	V/μs
SR2	Output Slew Rate (Note 8)	$R_L = 3$ kΩ to 7 kΩ, $C_L = 2500$ pF (*Figures 1* and *2*)	4		30	V/μs
RECEIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 1.5$ kΩ, $C_L = 15$ pF (includes fixture plus probe), (*Figures* 3 and *4*)			50	ns
t_{PLH}	Propagation Delay Low to High				85	ns
t_r	Rise Time				175	ns
t_f	Fall Time				20	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified. Minimum and maximum values are specified as an absolute value and the sign is used to indicate direction.

Note 3: All typicals are given for: $V_{CC} = +5.0V$, $V^+ = +12.0V$, $V^- = -12V$, $T_A = +25°C$.

Note 4: Only one driver output shorted at a time.

Note 5: Generator characteristics for driver input: f = 64 kHz (128 kbits/sec), $t_r = t_f < 10$ ns, $V_{IH} = 3V$, $V_{IL} = 0V$, duty cycle = 50%.

Note 6: Generator characteristics for receiver input: f = 64 kHz (128 kbits/sec), $t_r = t_f = 200$ ns, $V_{IH} = 5V$, $V_{IL} = -5V$, duty cycle = 50%.

Note 7: If receiver inputs are unconnected, receiver output is a logic high.

Note 8: Driver output slew rate is measured from the +3.0V to the −3.0V level on the output waveform. Inputs not under test are connected to V_{CC} or GND.

Parameter Measurement Information

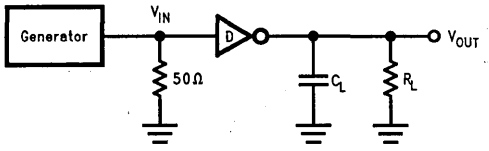

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FIGURE 1. Driver Propagation Delay and Transition Time Test Circuit (Note 5)

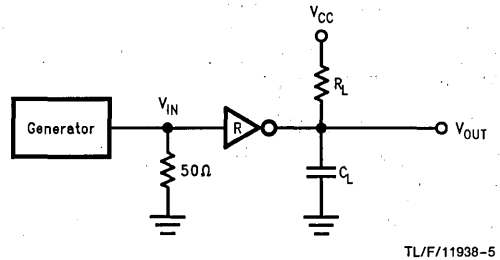

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FIGURE 3. Receiver Propagation Delay and Transition Time Test Circuit (Note 6)

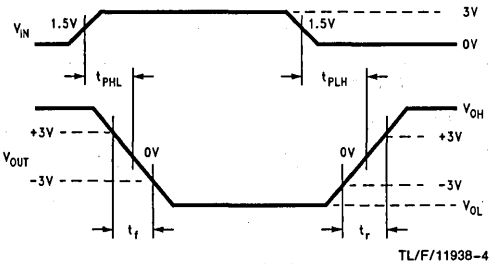

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FIGURE 2. Driver Propagation Delay and Transition Time Waveforms Slew Rate (SR) = 6V/(t_r or t_f)

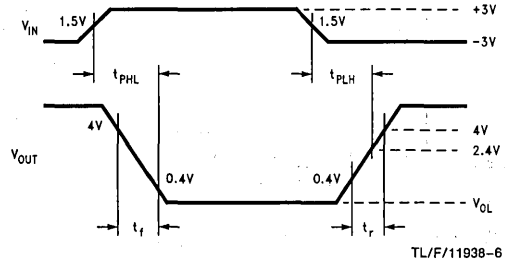

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FIGURE 4. Receiver Propagation Delay and Transition Time Waveform

Pin Descriptions

Pin #	Name	Description
13, 15, 16	D_{IN}	TTL Level Driver Inputs
5, 6, 8	D_{OUT}	Driver Output Pins
2, 3, 4, 7, 9	R_{IN}	Receiver Input Pins
12, 14, 17, 18, 19	R_{OUT}	Receiver Output Pins
11	GND	Ground
1	V^+	Positive Power Supply Pin ($+9.0 \leq V^+ \leq +13.2$)
10	V^-	Negative Power Supply Pin ($-9.0 \leq V^- \leq -13.2$)
20	V_{CC}	Positive Power Supply Pin ($+5V \pm 5\%$)

Application Information

In a typical Data Terminal Equipment (DTE) to Data Circuit Terminating Equipment (DCE) 9-pin de-facto interface implementation, 2 data lines and 6 control lines are required. The data lines are TXD and RXD. The control lines are RTS, DTR, DSRT, DCE, CTS, and RI.

The DS14185 is a 3 x 5 Driver/Receiver and offers a single chip solutuion for the DTE interface. As shown in *Figure 5*, this interface affords direct flow-thru interconnect. For a more conservative design, the user may wish to insert ground traces between the signal lines to minimize cross talk.

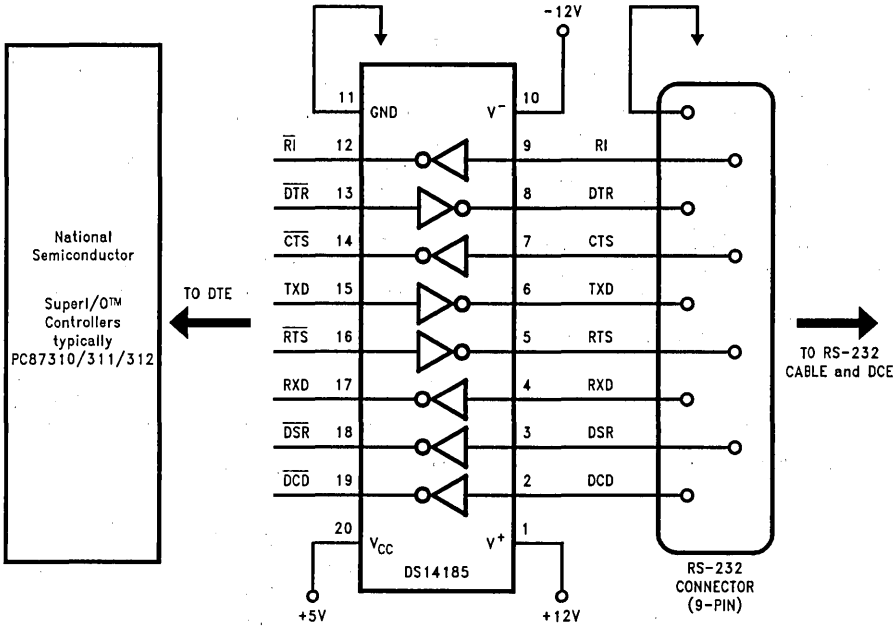

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FIGURE 5. Typical DTE Application

National Semiconductor

DS14C232
Low Power +5V Powered TIA/EIA-232 Dual Driver/Receiver

General Description

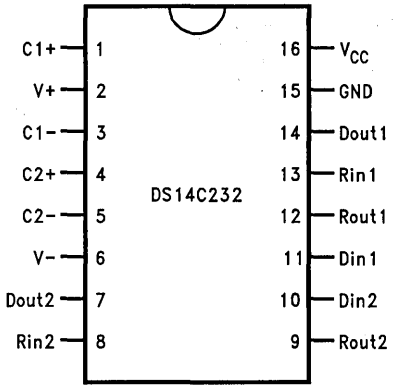
The DS14C232 is a low power dual driver/receiver featuring an onboard DC to DC converter, eliminating the need for ±12V power supplies. The device only requires a +5V power supply. I_{CC} is specified at 3.0 mA maximum, making the device ideal for battery and power conscious applications. The drivers' slew rate is set internally and the receivers feature internal noise filtering, eliminating the need for external slew rate and filter capacitors. The device is designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The driver inputs and receiver outputs are TTL and CMOS compatible. DS14C232C driver outputs and receiver inputs meet TIA/EIA-232-E (RS-232) and CCITT V.28 standards.

Features

- Pin compatible with industry standard MAX232, LT1081, ICL232 and TSC232
- Single +5V power supply
- Low power—I_{CC} 3.0 mA maximum
- DS14C232C meets TIA/EIA-232-E (RS-232) and CCITT V.28 standards
- CMOS technology
- Receiver Noise Filter
- Package efficiency—2 drivers and 2 receivers
- Available in Plastic DIP, Narrow and Wide SOIC packages
- TIA/EIA-232 compatible extended temperature range options:

DS14C232T	−40°C to +85°C
DS14C232	−55°C to +125°C

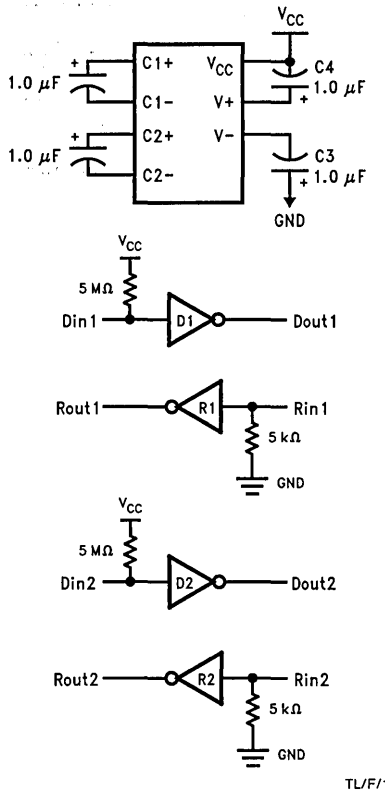
Connection Diagrams



TL/F/10744–1

Order Number DS14C232CN, DS14C232TN, DS14C232CM, DS14C232TM, DS14C232CWM or DS14C232TWM
See NS Package Number N16A, M16A or M16B

Functional Diagram



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Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately on the following pages.

Supply Voltage, V_{CC}	−0.3V to 6V
V^+ Pin	$(V_{CC} - 0.3)$V to +14V
V^- Pin	+0.3V to −14V
Driver Input Voltage	−0.3V to $(V_{CC} + 0.3)$V
Driver Output Voltage	$(V^+ + 0.3)$V to $(V^- - 0.3)$V
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to $(V_{CC} + 0.3)$V
Junction Temperature	+150°C
Maximum Package Power Dissipation @ 25°C (Note 6)	
N Package	1698 mW
M Package	1156 mW
WM Package	1376 mW
Short Circuit Duration, D_{OUT}	Continuous
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering, 4 sec.)	+260°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 2.5 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C232C	0	+70	°C
DS14C232T	−40	+85	°C

Electrical Characteristics Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DC TO DC CONVERTER CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 0.8V			9.0		V
V^-	Negative Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 2.0V			−8.5		V
I_{CC}	Supply (V_{CC}) Current	No Load			1.0	3.0	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq$ 2.0V		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq$ 0.8V		−10		+10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		5.0	8.0		V
V_{OL}	Low Level Output Voltage	R_L = 3 kΩ			−7.0	−5.0	V
I_{OS+}	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V	(Note 3)	−30	−15	−5.0	mA
I_{OS-}	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2V		5.0	11	30	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = 0V = GND		300			Ω
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage	V_{CC} = 5.0V			1.9	2.4	V
		V_{CC} = 5.0V ±10%			1.9	2.6	V
V_{TL}	Input Low Threshold Voltage			0.8	1.5		V
V_{HY}	Hysteresis	T_A = 0°C to +85°C		0.2	0.4	1.0	V
		T_A = −40°C to 0°C		0.1	0.4	1.0	V
R_{IN}	Input Resistance	T_A = 0°C to +85°C	−15V ≤ V_{IN} ≤ +15V	3.0	4.7	7.0	kΩ
		T_A = −40°C to 0°C (Note 8)		3.0	4.7	10	kΩ
I_{IN}	Input Current	V_{IN} = +15V	0°C to +85°C	+2.14	+3.75	+5.0	mA
		V_{IN} = +3V		+0.43	+0.64	+1.0	mA
		V_{IN} = −3V		−1.0	−0.64	−0.43	mA
		V_{IN} = −15V		−5.0	−3.75	−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −3.2 mA		3.5	4.5		V
		V_{IN} = −3V, I_O = −20 μA		4.0	4.9		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +3.2 mA			0.15	0.4	V

COMMERCIAL

Switching Characteristics Over recommended operating conditions, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay Low to High	$R_L = 3\ k\Omega$, $C_L = 50\ pF$	*Figure 1* and *Figure 2*		1.0	4.0	μs
t_{PHL}	Propagation Delay High to Low				1.0	4.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.1	1.0	μs
SR1	Output Slew Rate	$R_L = 3\ k\Omega$ to $7\ k\Omega$, $C_L = 50\ pF$	(Note 7)	4.0		30	V/μs
SR2	Output Slew Rate	$R_L = 3\ k\Omega$, $C_L = 2500\ pF$			4.5		V/μs
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay Low to High	Input Pulse Width > 10 μs, $C_L = 50\ pF$ *(Figures 3 and 4)*			2.9	6.5	μs
t_{PHL}	Propagation Delay High to Low				2.5	6.5	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.4	2.0	μs
t_{nw}	Noise Pulse Width Rejected	*(Figures 3 and 4)*	$T_A = 0°C$ to $+85°C$		0.7	0.5	μs
			$T_A = -40°C$ to $0°C$		0.7	0.3	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: I_{OS+} and I_{OS-} values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f = 200$ ns, $V_{IH} = 3V$, $V_{IL} = -3V$, f = 30 kHz.

Note 5: All typicals are given for $V_{CC} = 5.0V$.

Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: N Package 15.6 mW/°C, M Package 10.6 mW/°C and WM Package 12.7 mW/°C.

Note 7: Slew rate is defined as $\Delta V/\Delta t$, measured between ±3V level.

Note 8: TIA/EIA-232-E receiver input impedance maximum limit is 7 kΩ.

MIL-STD 883C

Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the RETS please contact your local National Semiconductor sales office or distributor.

Supply Voltage, V_{CC}	−0.3V to 6V
V^+ Pin	(V_{CC} − 0.3)V to +14V
V^- Pin	+0.3V to −14V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation @ 25°C (Note 8)	
J Package	1520 mW
E Package	2000 mW
Short Circuit Duration, D_{OUT}	Continuous
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering, 4 sec.)	+260°C
ESD Rating (HMB, 1.5 kΩ, 100 pF)	≥ 2.5 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C232	−55	+125	°C

Electrical Characteristics Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Max	Units
DEVICE CHARACTERISTICS (C1–C4 = 1.0 μF)						
I_{CC}	Supply (V_{CC}) Current	No Load			8.0	mA
DRIVER CHARACTERISTICS						
V_{IH}	High Level Input Voltage			2		V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$			100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$			100	μA
V_{OH}	High Level Output Voltage	$R_L = 3\ k\Omega$		5.0		V
V_{OL}	Low Level Output Voltage	$R_L = 3\ k\Omega$			−5.0	V
I_{OS+}	Output High Short Circuit Current	$V_O = 0V$	(Note 3)	−25		mA
I_{OS-}	Output Low Short Circuit Current	$V_O = 0V$			25	mA
R_O	Output Resistance	$-2V \leq V_O \leq +2V$, $T_A = 25°C$, $V_{CC} = 0V = GND$		300		Ω
RECEIVER CHARACTERISTICS (C1–C4 = 1.0 μF)						
V_{TH}	Input High Threshold Voltage				3.0	V
V_{TL}	Input Low Threshold Voltage			0.2		V
V_{HY}	Hysteresis	$T_A = 25°C, +125°C$		0.1	1.0	V
		$T_A = -55°C$		0.05	1.0	V
R_{IN}	Input Resistance	$V_{IN} = \pm 3V$ and $\pm 15V$, $T_A = 25°C$		3.0	7.0	kΩ
V_{OH}	High Level Output Voltage	$I_O = -3.2\ mA$		3.5		V
		$I_O = -20\ \mu A$		4.0		V
V_{OL}	Low Level Output Voltage	$I_O = +3.2\ mA$			0.4	V

MIL-STD-883C

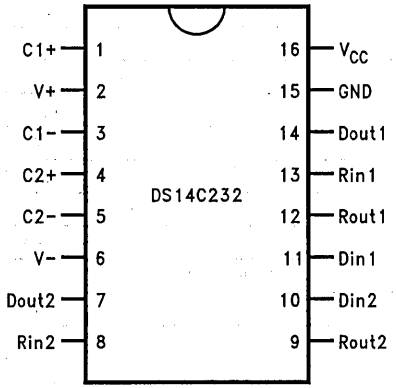
Switching Characteristics Over recommended operating conditions, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Units
DRIVER CHARACTERISTICS (C1–C4 = 1.0 μF)						
t_{PLH}	Propagation Delay Low to High	R_L = 3 kΩ, C_L = 50 pF	*Figures 1* and *2*		4.0	μs
t_{PHL}	Propagation Delay High to Low				4.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				1.0	μs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF	(Note 7)	1.5	30	V/μs
RECEIVER CHARACTERISTICS (C1–C4 = 1.0 μF)						
t_{PLH}	Propagation Delay Low to High	Input Pulse Width > 10 μs			8.0	μs
t_{PHL}	Propagation Delay High to Low	C_L = 50 pF			8.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$	*(Figures 3* and *4)*			2.0	μs

Note 8: Ratings apply to ambient temperature at +25°C. Above this temperature derate: J Package 12.2 mW/°C and E Package 13.3 mW/°C.

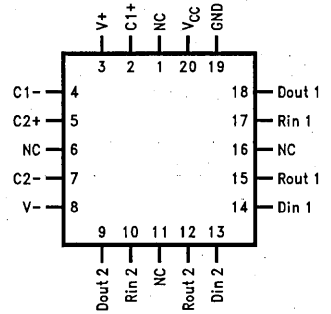
Connection Diagrams (Continued)

J Package
16-Lead Dual-In-line Package



TL/F/10744–1

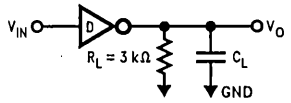
E Package
20-Lead Ceramic Leadless Chip Carrier



TL/F/10744–10

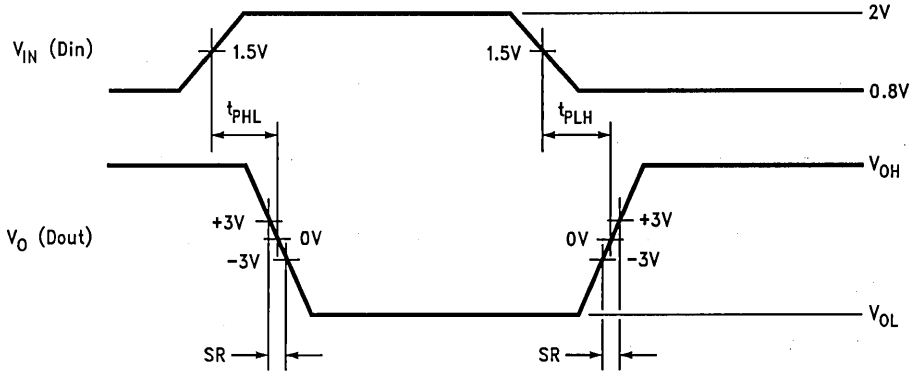
For Complete Military 883 Specifications
See RETS Data Sheet.
Order Number DS14C232J/883 or DS14C232E/883
See NS Package Number E20A or J16A

Parameter Measurement Information



TL/F/10744–3

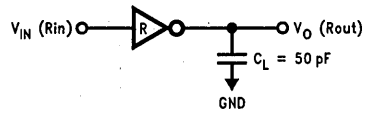
FIGURE 1. Driver Load Circuit



TL/F/10744–4

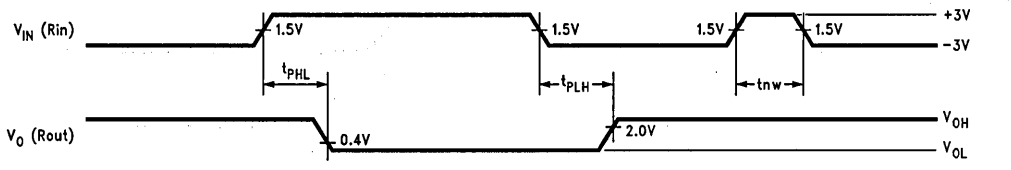
FIGURE 2. Driver Switching Waveform

Parameter Measurement Information (Continued)



TL/F/10744–5

FIGURE 3. Receiver Load Circuit



TL/F/10744–6

FIGURE 4. Receiver Propagation Delays and Noise Rejection (Note 4)

Pin Descriptions

V_{CC} (Pin 16)

Power supply pin for the device, +5V (±10%).

V+ (Pin 2)

Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4-1.0 μF (6.3V). Capacitor value should be larger than 1 μF. This supply is not intended to be loaded externally.

V− (Pin 6)

Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3-1.0 μF (16V). Capacitor value should be larger than 1 μF. This supply is not intended to be loaded externally.

C1+, C1− (Pins 1, 3)

External capacitor connection pins. Recommended capacitor: 1.0 μF (6.3V). Capacitor value should be larger than 1 μF.

C2+, C2− (Pins 4, 5)

External capacitor connection pins. Recommended capacitor: 1.0 μF (16V). Capacitor value should be greater than 1 μF.

$D_{IN}1$, $D_{IN}2$ (Pins 11, 10)

Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal active pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input HIGH. Output will be LOW for open inputs.

$D_{OUT}1$, $D_{OUT}2$ (Pins 14, 7)

Driver output pins conform to TIA/EIA-232-E levels.

$R_{IN}1$, $R_{IN}2$ (Pins 13, 8)

Receiver input pins accept TIA/EIA-232-E input voltages (±25V). Receivers feature a noise filter and guaranteed hysteresis of 100 mV. Unused receiver input pins may be left open. Internal input resistor 4.7 kΩ pulls input low, providing a failsafe high output.

$R_{OUT}1$, $R_{OUT}2$ (Pins 12, 9)

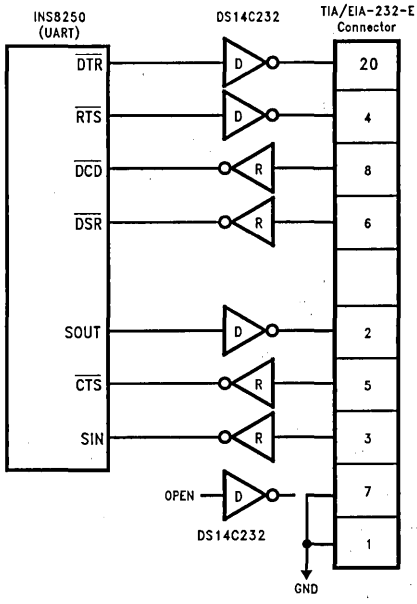
Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (Pin 15)

Ground Pin.

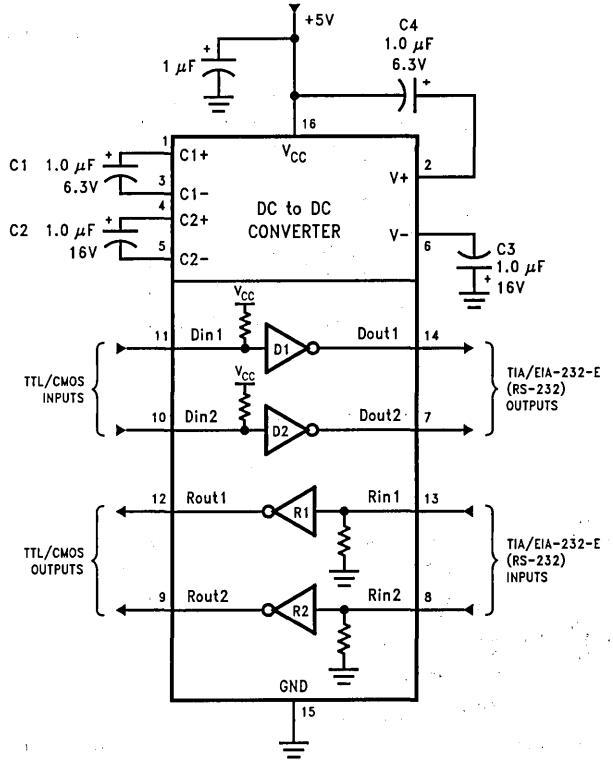
Typical Application Information

Application of DS14C232 and INS8250



TL/F/10744–7

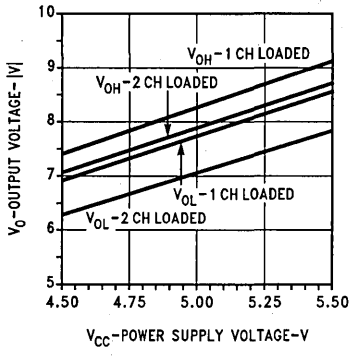
Typical Connection Diagram



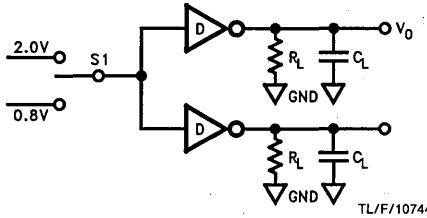
TL/F/10744–9

Typical Performance Characteristics

DRIVER V_{OH} & V_{OL} vs POWER SUPPLY VOLTAGE

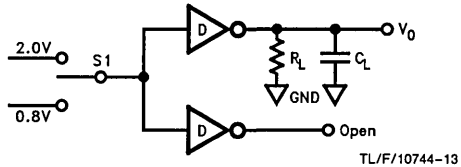


TL/F/10744-11



TL/F/10744-12

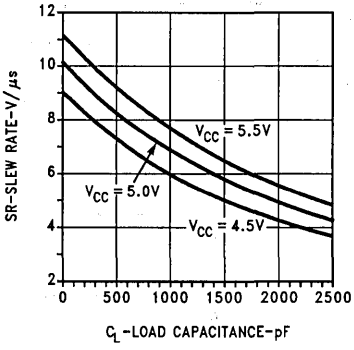
V_{CC} = 5.0V, R_L = 3 kΩ, C_L = 15 pF (includes jig and probe capacitance), C_P = 1 μF



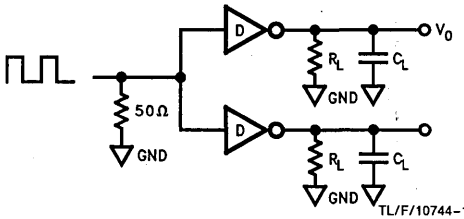
TL/F/10744-13

S1	V_O
2.0V	V_{OL}
0.8V	V_{OH}

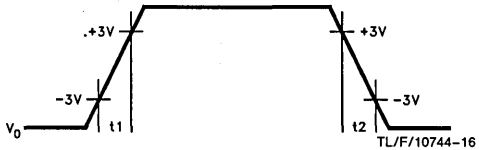
DRIVER SLEW RATE vs POWER SUPPLY VOLTAGE & LOAD CAPACITANCE



TL/F/10744-14



TL/F/10744-15



TL/F/10744-16

T_a = 25°C, R_L = 5 kΩ, C_P = 1 μF, f = 30 KHz

SR = 6V/t1 or 6V/t2, whichever is greater.

National Semiconductor

DS14C237
Single Supply TIA/EIA-232 5 x 3 Driver/Receiver

General Description

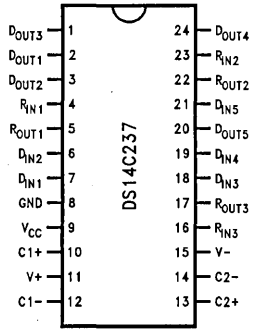
The DS14C237 is a five driver, three receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates ±12V supplies by employing an internal DC-DC converter to generate the necessary output levels from a single +5V supply. Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors.

One device is capable of implementing a complete nine pin interface. The combination of its extended operating temperature range and low power requirement makes this device an ideal choice for a wide variety of commercial, industrial, and battery powered applications.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC-DC converter
- Operates with single +5V supply
- Low power requirement—I_{CC} 10 mA max
- Internal driver slew rate control
- Receiver Noise Filtering
- Operates above 120 kbits/sec
- Direct replacement for MAX237
- Industrial temperature range option-DS14C237T (−40°C to +85°C)

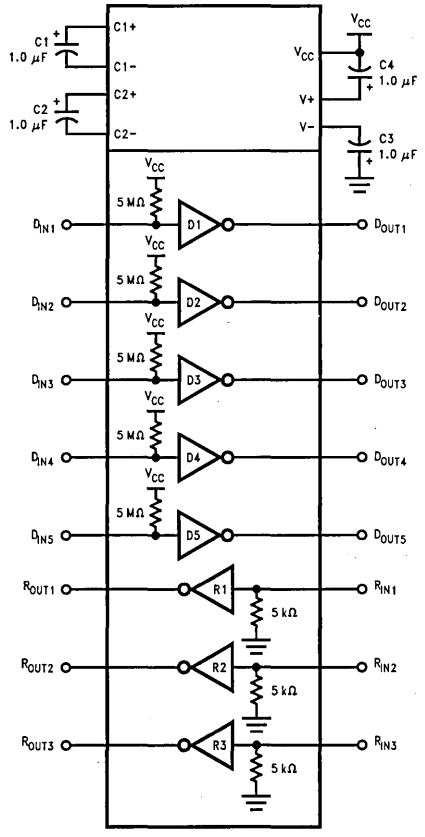
Connection Diagram



TL/F/11284–1

Order Number
DS14C237N, DS14C237WM,
DS14C237TN or DS14C237TWM
See NS Package Number M24B or N24A

Functional Diagram



TL/F/11284–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V+ Pin	(V_{CC} − 0.3V) to +15V
V− Pin	+0.3V to −15V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V+ + 0.3V) to (V− − 0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6)	
N Package	2400 mW
WM Package	1400 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temperature (T_A)			
DS14C237	0	+70	°C
DS14C237T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 0.8V			9.0		V
V^-	Negative Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 2.0V			−8.5		V
I_{CC}	Supply Current (V_{CC})	No Load			6.5	10	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.8V$		−10		10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		5.0	7.4		V
V_{OL}	Low Level Output Voltage				−6.3	−5.0	V
I_{OS}^+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V	(Note 3)	−30	−15	−5.0	mA
I_{OS}^-	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V		5.0	12	30	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V		300			Ω
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage				1.9	2.4	V
V_{TL}	Input Low Threshold Voltage			0.8	1.5		V
V_{HY}	Hysteresis			0.2	0.4	1.0	V
R_{IN}	Input Resistance			3.0	4.5	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V		2.14	3.8	5.0	mA
		V_{IN} = +3V		0.43	0.6	1.0	mA
		V_{IN} = −3V		−1.0	−0.6	−0.43	mA
		V_{IN} = −15V		−5.0	−3.8	−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −3.2 mA		3.5	4.5		V
		V_{IN} = −3V, I_O = −20 μA		4.0	4.9		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +3.2 mA			0.25	0.4	V

Switching Characteristics

Over recommended operating conditions, unless otherwise specified (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	R_L = 3 kΩ C_L = 50 pF *Figures 1* and *2*		0.7	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW			0.6	4.0	μs
t_{sk}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$			0.1	1.0	μs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF	4.0	15	30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF	3.0	5.0		V/μs
RECEIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	Input Pulse Width > 10 μs C_L = 50 pF *Figures 3* and *4*		2.0	6.5	μs
t_{PHL}	Propagation Delay HIGH to LOW			2.8	6.5	μs
t_{sk}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$			0.8	2.0	μs
t_{nw}	Noise Pulse Width Rejected			2.5	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

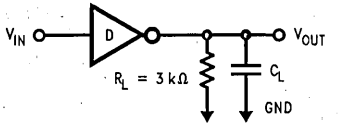
Note 3: $I_{OS}+$ and $I_{OS}-$ values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 64 kHz (128 kbits/sec). Drive AC Input Waveform for test purposes: $t_r = t_f \leq 10$ ns, V_{IH} = 3V, V_{IL} = 0V, f = 64 kHz (128 kbits/sec).

Note 5: All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

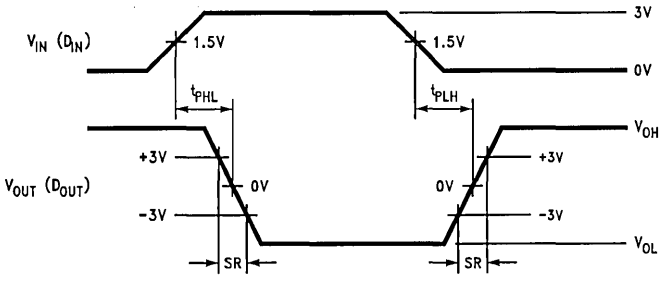
Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: N package 20 mW/°C and WM package 13.5 mW/°C.

Parameter Measurement Information



TL/F/11284–4

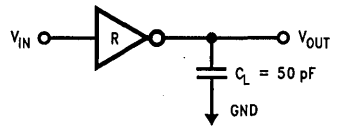
FIGURE 1. Driver Load Circuit



TL/F/11284–5

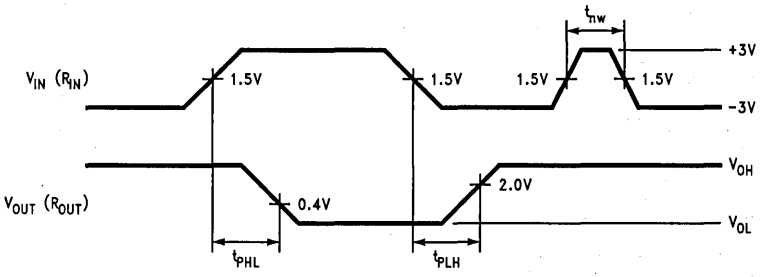
FIGURE 2. Driver Switching Waveform

Parameter Measurement Information (Continued)



TL/F/11284–6

FIGURE 3. Receiver Load Circuit



TL/F/11284–7

FIGURE 4. Receiver Propagation Delays and Noise Rejection

Pin Description

V_{CC} (Pin 9)—Power supply pin for the device, +5V (±10%).

V^+ (Pin 11)—Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4 = 1.0 μF (6.3V). This supply is not intended to be loaded externally.

V^- (Pin 15)—Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3 = 1.0 μF (16V). This supply is not intended to be loaded externally.

$C1^+$, $C1^-$ (Pins 10, 12)—External capacitor connection pins. Recommended capacitor—1.0 μF (6.3V).

$C2^+$, $C2^-$ (Pins 13, 14)—External capacitor connection pins. Recommended capacitor—1.0 μF (16V).

D_{IN} 1–5 (Pins 7, 6, 18, 19, 21)—Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input to V_{CC}. Output will be LOW for open inputs.

D_{OUT} 1–5 (Pins 2, 3, 1, 24, 20)—Driver output pins conform to TIA/EIA-232-E levels.

R_{IN1} 1–3 (Pins 4, 23, 16)—Receiver input pins accept TIA/EIA-232-E input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 200 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–3 (Pins 5, 22, 17)—Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (Pin 8)—Ground Pin.

National Semiconductor

DS14C238
Single Supply TIA/EIA-232 4 x 4 Driver/Receiver

General Description

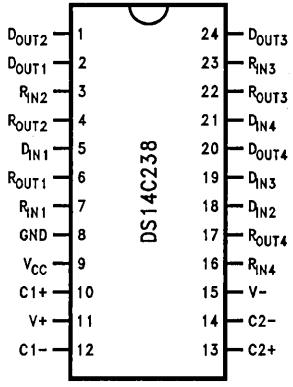
The DS14C238 is a four driver, four receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates ±12V supplies by employing an internal DC-DC converter to generate the necessary output levels from a single +5V supply. Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors.

The combination of its extended operating temperature range and low power requirement makes this device an ideal choice for a wide variety of commercial, industrial, and battery powered applications.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC-DC converter
- Operates with single +5V supply
- Low power requirement—I_{CC} 10 mA max
- Internal driver slew rate control
- Receiver noise filtering
- Operates above 120 kbits/sec
- Direct replacement for MAX238
- Industrial temperature range option—DS14C238T (−40°C to +85°C)

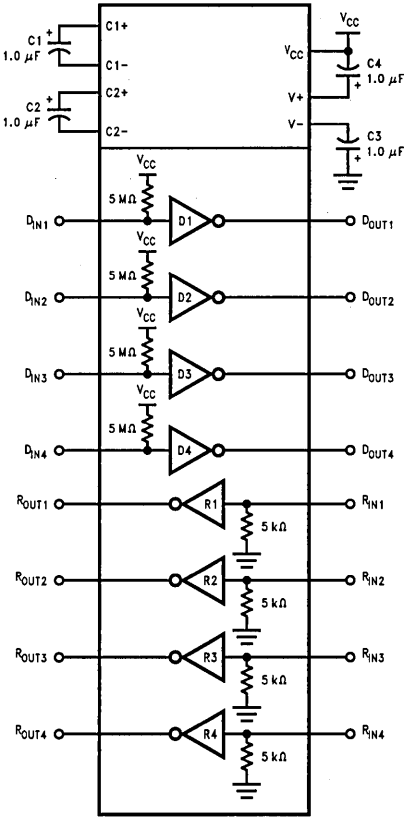
Connection Diagram



TL/F/11282–1

Order Number DS14C238N, DS14C238WM, DS14C238TN or DS14C238TWM
See NS Package Numbers M24B or N24A

Functional Diagram



TL/F/11282–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V+ Pin	(V_{CC} −0.3V) to +15V
V− Pin	+0.3V to −15V
Driver Input Voltage	−0.3V to (V_{CC} +0.3V)
Driver Output Voltage	(V+ +0.3V) to (V− −0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} +0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6)	
N Package	2400 mW
WM Package	1400 mW
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering, 4 Seconds)	+260°C
Short Circuit Duration (D_{OUT})	Continuous

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C238	0	+70	°C
DS14C238T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 0.8V			9.0		V
V−	Negative Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 2.0V			−8.0		V
I_{CC}	Supply Current (V_{CC})	No Load			7.0	10	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.8V$		−10		+10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		5.0	7.4		V
V_{OL}	Low Level Output Voltage				−6.3	−5.0	V
I_{OS}+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V	(Note 3)	−30	−15	−5.0	mA
I_{OS}−	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V		5.0	12	30	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V		300			Ω

Electrical Characteristics (Continued)

Over recommended operating conditions, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS						
V_{TH}	Input High Threshold Voltage			1.9	2.4	V
V_{TL}	Input Low Threshold Voltage		0.8	1.5		V
V_{HY}	Hysteresis		0.2	0.4	1.0	V
R_{IN}	Input Resistance		3.0	4.5	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V	2.14	3.8	5.0	mA
		V_{IN} = +3V	0.43	0.6	+1.0	mA
		V_{IN} = −3V	−1.0	−0.6	−0.43	mA
		V_{IN} = −15V	−5.0	−3.8	−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −3.2 mA	3.5	4.5		V
		V_{IN} = −3V, I_O = −20 μA	4.0	4.9		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +3.2 mA		0.25	0.4	V

Switching Characteristics

Over recommended operating conditions, unless otherwise specified. (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	R_L = 3 kΩ, C_L = 50 pF (*Figures 1* and *2*)		0.7	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW			0.6	4.0	μs
t_{sk}	Skew $\lvert t_{PLH}-t_{PHL} \rvert$			0.1	1.0	μs
SR1	Output Slew Rate	R_L = 3kΩ to 7 kΩ, C_L = 50 pF	4.0	15	30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF	3.0	5.0		V/μs
RECEIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	Input Pulse Width > 10 μs, C_L = 50 pF (*Figures 3* and *4*)		2.0	6.5	μs
t_{PHL}	Propagation Delay HIGH to LOW			2.8	6.5	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL} \rvert$			0.8	2.0	μs
t_{NW}	Noise Pulse Width Rejected			2.5	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

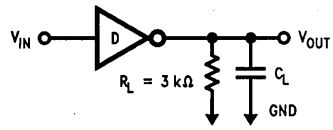
Note 3: I_{OS}+ and I_{OS}− values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 64 kHz (128 kbits/sec). Driver AC input waveform for test purposes: $t_r = t_f \leq$ 10 ns, V_{IH} = 3V, V_{IL} = 0V, f = 64 kHz (128 kbits/sec).

Note 5: All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

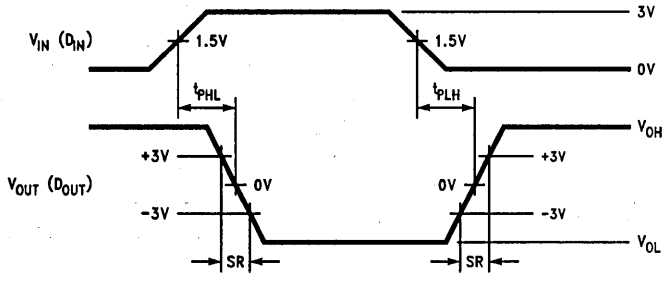
Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: N package 20 mW/°C and WM package 13.5 mW/°C.

Parameter Measurement Information



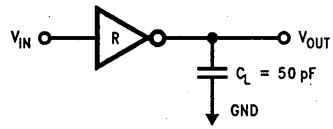
TL/F/11282–4

FIGURE 1. Driver Load Circuit



TL/F/11282–5

FIGURE 2. Driver Switching Waveform



TL/F/11282–6

FIGURE 3. Receiver Load Circuit

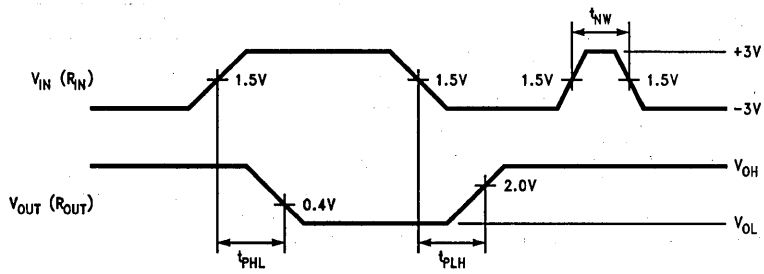


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FIGURE 4. Receiver Propagation Delays and Noise Rejection

Pin Descriptions

V_{CC} (pin 9)—Power supply pin for the device, +5V (±10%).

V+ (pin 11)—Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4 = 1.0 μF (6.3V). This supply is not intended to be loaded externally.

V− (pin 15)—Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3 = 1.0 μF (16V). This supply is not intended to be loaded externally.

C1+, C1− (pins 10 and 12)—External capacitor connection pins. Recommended capacitor – 1.0 μF (6.3V).

C2+, C2− (pins 13 and 14)—External Capacitor connection pins. Recommended capacitor – 1.0 μF (16V).

D_{IN} 1–5 (pins 7, 6, 8, 18, 19, and 21)—Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input to V_{CC}. Output will be LOW for open inputs.

D_{OUT} 1–5 (pins 2, 3, 1, 24, and 20)—Driver output pins conform to TIA/EIA-232-E levels.

R_{IN1} 1–3 (pins 4, 23, and 16)—Receiver input pins accept TIA/EIA-232-E input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 200 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–3 (pins 5, 22, and 17)—Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (pin 8)—Ground Pin.

National Semiconductor

DS14C239
Dual Supply TIA/EIA-232 3 x 5 Driver/Receiver

General Description

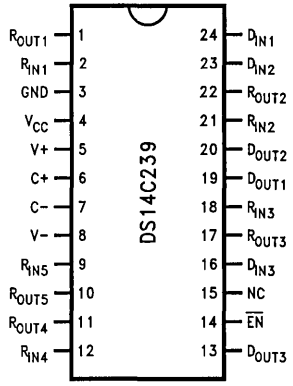
The DS14C239 is a three driver, five receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates −12V supply by employing an internal DC-DC converter to generate the necessary output levels from a single +5V supply and a positive voltage power supply (+7.5V to +13.2V). Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors. With the addition of TRI-STATE® receiver outputs, device power consumption is kept to a minimum.

The combination of its low power requirement and extended operating temperature range makes this device an ideal choice for a wide variety of commercial, industrial, and battery powered applications.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC-DC converter
- Low power requirement: I^+ = 10 mA max
  I_{CC} = 1 mA max
- Internal driver slew rate control
- Receiver Noise Filtering
- Operates above 120 kbits/sec
- TRI-STATE Receiver Outputs
- Direct replacement for MAX239
- Industrial temperature range option—DS14C239T (−40°C to +85°C)

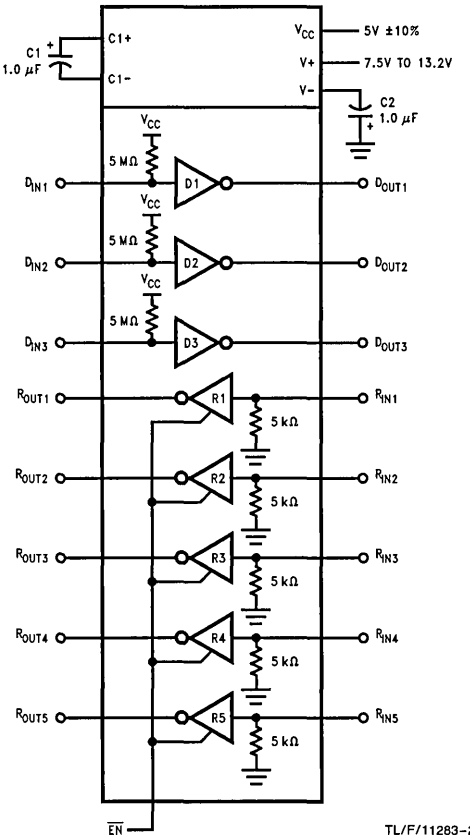
Connection Diagram



TL/F/11283–1

Order Number DS14C239N, DS14C239WM, DS14C239TN or DS14C239TWM
See NS Package Number M24B or N24A

Functional Diagram



TL/F/11283–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +15V
V^- Pin	+0.3V to −15V
Driver Input Voltage	− 0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6)	
N Package	2400 mW
WM Package	1400 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Supply Pin (V^+)	7.5	13.2	V
Operating Free Air Temp. (T_A)			
DS14C239	0	+70	°C
DS14C239T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DEVICE CHARACTERISTICS						
V^-	Negative Power Supply	R_L = 3 kΩ, C1, C2 = 1.0 μF, D_{IN} = 2.0V		−9.5		V
I^+	Supply Current (V^+)	No Load		4	10	mA
I_{CC}	Supply Current (V_{CC})	No Load		0.1	1.0	mA
DRIVER CHARACTERISTICS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$	−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.8V$	−10		+10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ	5.0	8.7		V
V_{OL}	Low Level Output Voltage			−8.0	−5.0	V
I_{OS}^+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V	−40	−20	−5.0	mA
I_{OS}^-	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V	5.0	16	40	mA
R_O	Output Resistance	$-2V \leq V_O \leq +2V$, $V_{CC} = V^+ = GND = 0V$	300			Ω
RECEIVER CHARACTERISTICS						
V_{TH}	Input High Threshold Voltage	T_A = 25°C		2	2.4	V
		T_A = −40°C to +85°C		2	2.6	V
V_{TL}	Input Low Threshold Voltage		0.8	1.5		V
V_{HY}	Hysteresis	T_A = 25°C	0.2	0.5	1.0	V
		T_A = −40°C to +85°C	0.1	0.5	1.0	V

Electrical Characteristics (Continued)

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Continued)							
R_{IN}	Input Resistance			3.0	4.5	7.0	kΩ
I_{IN}	Input Current	$V_{IN} = +15V$		2.14	3.8	5.0	mA
		$V_{IN} = +3V$		0.43	0.6	1.0	mA
		$V_{IN} = -3V$		−1.0	−0.6	−0.43	mA
		$V_{IN} = -15V$		−5.0	−3.8	−2.14	mA
V_{OH}	High Level Output Voltage	$V_{IN} = -3V$, $I_O = -3.2$ mA		3.5	4.5		V
		$V_{IN} = -3V$, $I_O = -20$ μA		4.0	4.9		V
V_{OL}	Low Level Output Voltage	$V_{IN} = +3V$, $I_O = +3.2$ mA			0.25	0.4	V
V_{IH}	High Level Input Voltage		$\overline{EN}$	2.4		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.4V$		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.8V$		−10		+10	μA
I_{OZ}	Output Leakage Current	$\overline{EN} = V_{CC}$, $0V \leq R_{OUT} \leq V_{CC}$		−10	0.1	+10	μA

Switching Characteristics

Over recommended operating conditions, unless otherwise specified (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	$R_L = 3$ kΩ, $C_L = 50$ pF (Figures 1 and 2)		0.7	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW			0.7	4.0	μs
t_{sk}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$			0	1.0	μs
SR1	Output Slew Rate	$R_L = 3$kΩ to 7 kΩ, $C_L = 50$ pF, $V^+ \leq 10.35V$	4.0	17	30	V/μs
SR2	Output Slew Rate	$R_L = 3$ kΩ, $C_L = 2500$ pF, $V^+ \leq 10.35V$	3.0	6.4		V/μs
RECEIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	Input Pulse Width > 10 μs, $C_L = 50$ pF (Figures 3 and 4)		2.1	6.5	μs
t_{PHL}	Propagation Delay HIGH to LOW			2.9	6.5	μs
t_{sk}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$			0.8	2.0	μs
t_{PLZ}		(Figures 5 and 7)		0.25	2.0	μs
t_{PZL}				0.70	2.0	μs
t_{PHZ}		(Figures 5 and 6)		0.25	2.0	μs
t_{PZH}				0.70	2.0	μs
t_{nw}	Noise Pulse Width Rejected	(Figures 3 and 4)		2.0	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

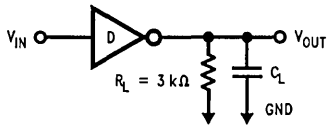
Note 3: I_{OS}^+ and I_{OS}^- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f = 200$ ns, $V_{IH} = 3V$, $V_{IL} = -3V$, f = 64 kHz (128 kbits/sec). Driver AC input waveform for test purposes: $t_r = t_f \leq 10$ ns, $V_{IH} = 3V$, $V_{IL} = 0V$, f = 64 kHz (128 kbits/sec).

Note 5: All typicals are given for $V_{CC} = 5.0V$ and $T_A = +25°C$, $V^+ = 10.35V$.

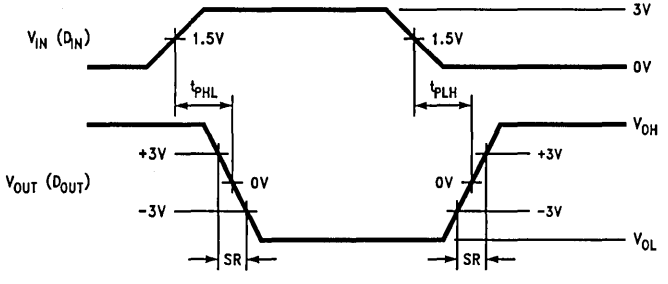
Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: N package 20 mW/°C and WM package 13.5 mW/°C.

Parameter Measurement Information



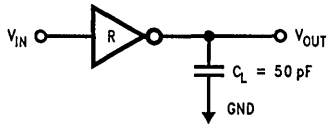
TL/F/11283–4

FIGURE 1. Driver Load Circuit



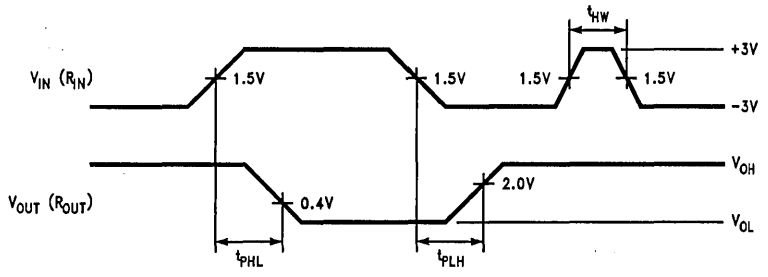
TL/F/11283–5

FIGURE 2. Driver Switching Waveform



TL/F/11283–6

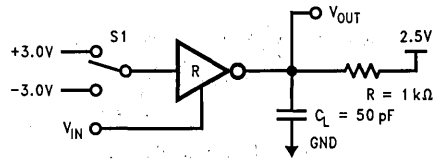
FIGURE 3. Receiver Load Circuit



TL/F/11283–7

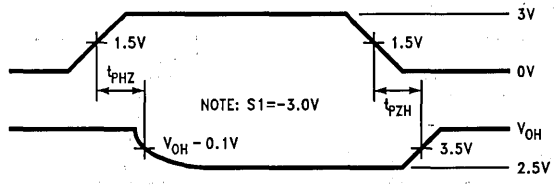
FIGURE 4. Receiver Propagation Delays and Noise Rejection

Parameter Measurement Information (Continued)



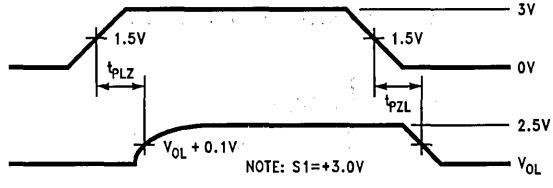
TL/F/11283–8

FIGURE 5. Receiver Disable Load Circuit



TL/F/11283–9

FIGURE 6. Receiver TRI-STATE Timing (t_{PHZ}, t_{PZH})



TL/F/11283–10

FIGURE 7. Receiver TRI-STATE Timing (t_{PLZ}, t_{PZL})

Pin Descriptions

V_{CC} (pin 4)—Power supply pin for the device, +5V (±10%).

V^+ (pin 5)—Positive supply for TIA/EIA-232-E drivers. Specified at 7.5V minimum and 13.2V maximum.

V^- (pin 8)—Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C2 = 1.0 μF (16V). This supply is not intended to be loaded externally.

C1+, C1− (pins 6, 7)—External capacitor connection pins. Recommended capacitor—1.0 μF (16V).

$\overline{EN}$ (pin 14)—Controls the Receiver output TRI-STATE Circuit. A High level on this pin will disable the Receiver Output.

D_{IN} 1–3 (pins 24, 23, 16)—Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input to V_{CC}. Output will be LOW for open inputs.

D_{OUT} 1–3 (pins 19, 20, 13)—Driver output pins conform to TIA/EIA-232-E levels.

R_{IN} 1–5 (pins 2, 21, 18, 12, 9)—Receiver input pins accept TIA/EIA-232-E input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 100 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–5 (pins 1, 22, 17, 11, 10)—Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (pin 3)—Ground pin.

National Semiconductor

DS14C241
Single Supply TIA/EIA-232 4 x 5 Driver/Receiver

General Description

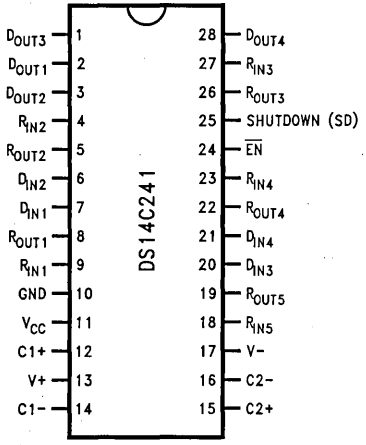
The DS14C241 is four driver, five receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates ±12V supplies by employing an internal DC–DC converter to generate the necessary output levels from a single +5V supply. Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors. With the addition of TRI-STATE® receiver outputs and a shutdown mode, device power consumption is kept to a minimum.

The combination of its low power requirement and extended operating temperature range makes this device an ideal choice for a wide variety of commercial, industrial, and battery powered applications

Features

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC–DC converter
- Operates with single +5V supply
- Low power requirement—I_{CC} 10 mA max
- Shutdown mode—I_{CX} 10 μA max
- Internal driver slew rate control
- Receiver noise filtering
- Operates above 120 kbits/sec
- TRI-STATE receiver outputs
- Direct replacement for MAX241
- Industrial temperature range option—DS14C241T (−40°C to +85°C)

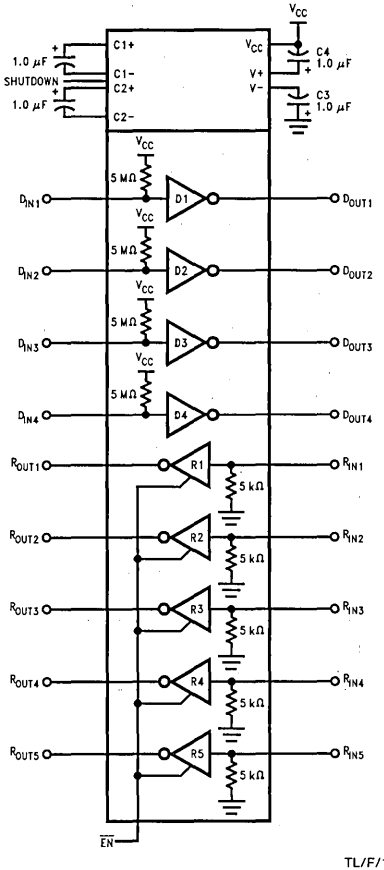
Connection Diagram



TL/F/11281–1

Order Number DS14C241WM or DS14C241TWM
See NS Package Number M28B

Functional Diagram



TL/F/11281–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V+ Pin	(V_{CC} − 0.3V) to +15V
V− Pin	+0.3V to −15V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V+ + 0.3V) to (V− − 0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6) WM Package	1520 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C241	0	+70	°C
DS14C241T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 0.8V			9.0		V
V^-	Negative Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 2.0V			−8.0		V
I_{CC}	Supply Current (V_{CC})	No Load			8.5	10	mA
I_{CX}	Supply Current Shutdown	R_L = 3 kΩ, SD = V_{CC}			1.0	10	μA
V_{IH}	High Level Enable Voltage		SD	2.4		V_{CC}	V
V_{IL}	Low Level Enable Voltage			GND		0.8	V
I_{IH}	High Level Enable Current			−10		+10	μA
I_{IL}	Low Level Enable Current			−10		+10	μA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage		D_{IN}	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.8V$		−10		+10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		5.0	7.5		V
V_{OL}	Low Level Output Voltage				−6.5	−5.0	V
I_{OS}^+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V		−30	−15	−5.0	mA
I_{OS}^-	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V		5.0	12	30	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V		300			Ω
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage				1.9	2.4	V
V_{TL}	Input Low Threshold Voltage			0.8	1.5		V
V_{HY}	Hysteresis			0.2	0.4	1.0	V
R_{IN}	Input Resistance			3.0	4.5	7.0	kΩ

Electrical Characteristics (Continued)

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Continued)							
I_{IN}	Input Current	$V_{IN} = +15V$		2.14	3.8	5.0	mA
		$V_{IN} = +3V$		0.43	0.6	1.0	mA
		$V_{IN} = -3V$		−1.0	−0.6	−0.43	mA
		$V_{IN} = -15V$		−5.0	−3.8	−2.14	mA
V_{OH}	High Level Output Voltage	$V_{IN} = -3V$, $I_O = -3.2$ mA		3.5	4.6		V
		$V_{IN} = -3V$, $I_O = -20$ μA		4.0	4.9		V
V_{OL}	Low Level Output Voltage	$V_{IN} = +3V$, $I_O = +3.2$ mA			0.25	0.4	V
V_{IH}	High Level Input Voltage		$\overline{EN}$	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.8V$		−10		+10	μA
I_{OZ}	Output Leakage Current	$\overline{EN} = V_{CC}$, $0V \leq R_{OUT} \leq V_{CC}$		−10		+10	μA

Switching Characteristics

Over recommended operating conditions, unless otherwise specified (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	$R_L = 3$ kΩ, $C_L = 50$ pF (*Figures 1* and *2*)			0.7	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW				0.6	4.0	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$				0.1	1.0	μs
SR1	Output Slew Rate	$R_L = 3$ kΩ to 7 kΩ, $C_L = 50$ pF		4.0	15	30	V/μs
SR2	Output Slew Rate	$R_L = 3$ kΩ, $C_L = 2500$ pF		3.0	5.0		V/μs
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	Input Pulse Width > 10 μs, $C_L = 50$ pF (*Figures 3* and *4*)			2.0	6.5	μs
t_{PHL}	Propagation Delay HIGH to LOW				2.8	6.5	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$				0.8	2.0	μs
t_{PLZ}		(*Figures 5* and *7*)			0.1	2.0	μs
t_{PZL}					0.6	2.0	μs
t_{PHZ}		(*Figures 5* and *6*)			0.2	2.0	μs
t_{PZH}					0.6	2.0	μs
t_{NW}	Noise Pulse Width Rejected	(*Figures 3* and *4*)			2.5	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

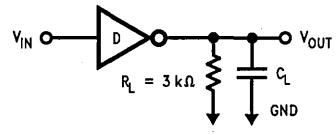
Note 3: I_{OS}^+ and I_{OS}^- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f = 200$ ns, $V_{IH} = 3V$, $V_{IL} = -3V$, f = 64 kHz (128 kbits/sec). Driver AC input waveform for test purposes: $t_r = t_f \leq 10$ ns, $V_{IH} = 3V$, $V_{IL} = 0V$, f = 64 kHz (128 kbits/sec).

Note 5: All typicals are given for $V_{CC} = 5.0V$ and $T_A = +25°C$.

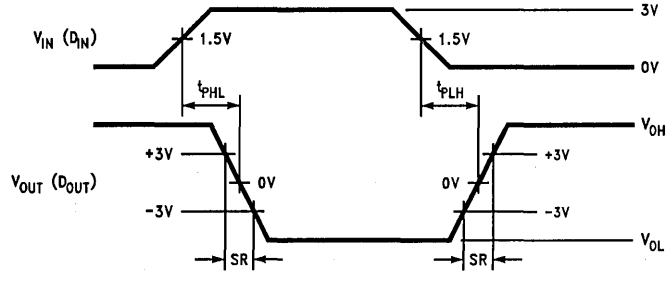
Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: WM package 14.3 mW/°C.

Parameter Measurement Information



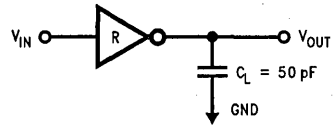
TL/F/11281–4

FIGURE 1. Driver Load Circuit



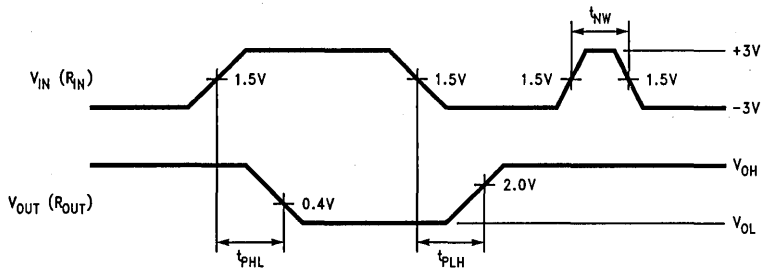
TL/F/11281–5

FIGURE 2. Driver Switching Waveform



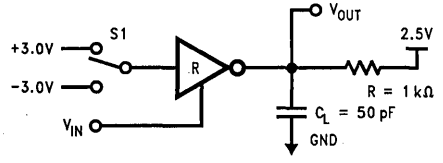
TL/F/11281–6

FIGURE 3. Receiver Load Circuit



TL/F/11281–7

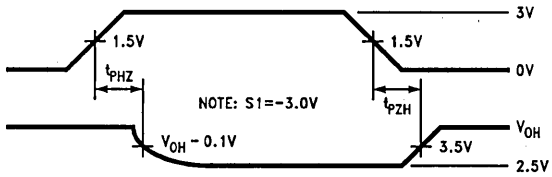
FIGURE 4. Receiver Propagation Delays and Noise Rejection



TL/F/11281–8

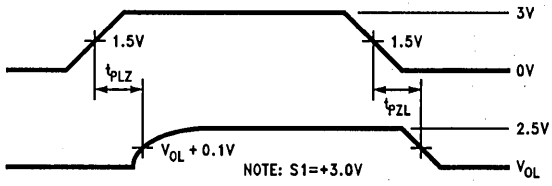
FIGURE 5. Receiver Disable Load Circuit

Parameter Measurement Information (Continued)



TL/F/11281-9

FIGURE 6. Receiver TRI-STATE Timing (t_{PHZ}, t_{PZH})



TL/F/11281-10

FIGURE 7. Receiver TRI-STATE Timing (t_{PLZ}, t_{PZL})

Pin Descriptions

V_{CC} (pin 11)—Power supply pin for the device, +5V (±10%).

V^+ (pin 13)—Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4 = 1.0 μF (6.3V). This supply is not intended to be loaded externally.

V^- (pin 17)—Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3 = 1.0 μF (16V). This supply is not intended to be loaded externally.

$C1^+$, $C1^-$ (pins 12 and 14)—External capacitor connection pins. Recommended capacitor—1.0 μF (6.3V).

$C2^+$, $C2^-$ (pins 15 and 16)—External capacitor connection pins. Recommended capacitor—1.0 μF (16V).

$\overline{EN}$ (pin 24)—Controls the Receiver output TRI-STATE Circuit. A HIGH level on this pin will disable the Receiver Output.

SHUTDOWN (SD) (pin 25)—A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 10 μA. Providing a low power state.

D_{IN} 1–4 (pins 7, 6, 20 and 21)—Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input to V_{CC}. Output will be LOW for open inputs.

D_{OUT} 1–4 (pins 2, 3, 1 and 28)—Driver output pins conform to TIA/EIA-232-E levels.

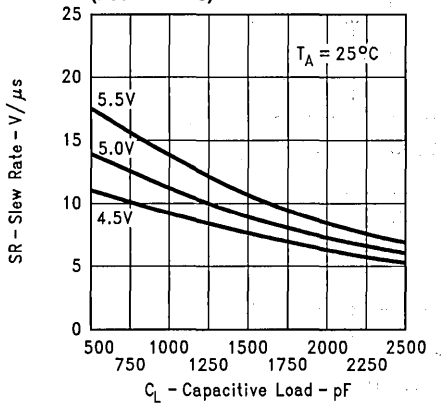
R_{IN} 1–5 (pins 9, 4, 27, 23 and 18)—Receiver input pins accept TIA/EIA-232-E input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 200 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–5 (pins 8, 5, 26, 22 and 19)—Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (pin 10)—Ground pin.

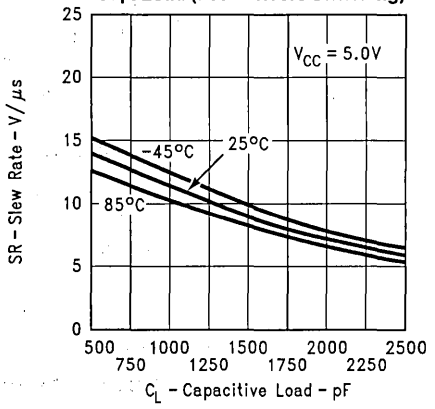
Typical Performance Characteristics

Slew Rate vs Cap. Load vs V_{CC} (Four Drivers)



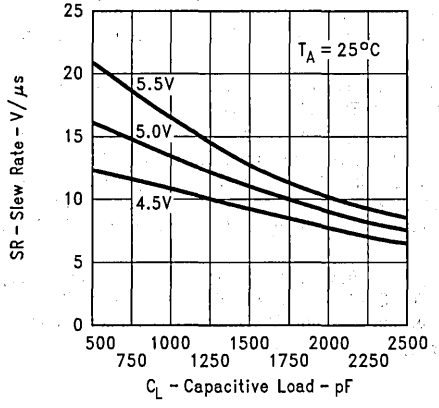
TL/F/11281–11

Slew Rate vs Temperature vs Cap. Load (Four Drivers Switching)



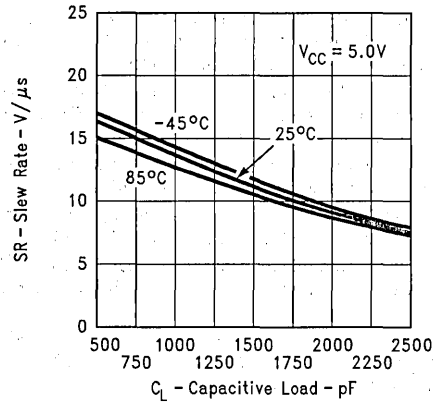
TL/F/11281–12

Slew Rate vs Cap. Load vs V_{CC} (One Driver)



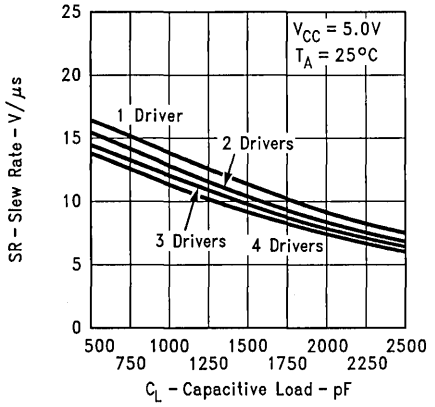
TL/F/11281–13

Slew Rate vs Temperature vs Cap. Load (One Driver Switching)



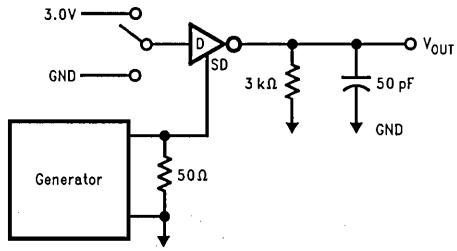
TL/F/11281–14

Driver Slew Rate vs Cap. Load vs Number of Drivers



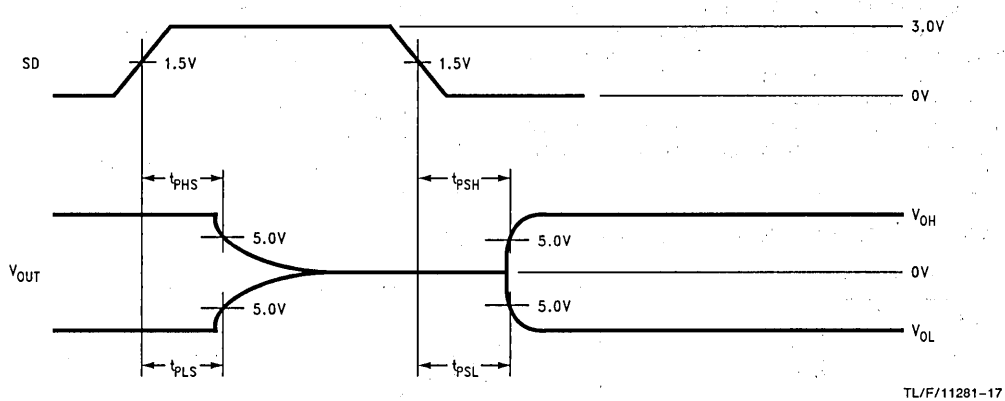
TL/F/11281–15

Typical Performance Characteristics (Continued)



TL/F/11281–16

FIGURE 8. Driver Shutdown (SD) Delay Test Circuit



TL/F/11281–17

FIGURE 9. Driver Shutdown (SD) Delay Timing Waveforms

Typical data only.

Symbol	Parameter	Conditions	Typ	Units
t_{PHS}	Propagation Delay High to SD	V_{CC} = 5V(Notes 7 and 8)	124	µs
t_{PLS}	Propagation Delay Low to SD	T_A = 25°C	110	µs
t_{PSH}	Propagation Delay SD to High		114	µs
t_{PSL}	Propagation Delay SD to Low		97	µs

Note 7: Sample size = 10 parts; 3 different datecodes.

Note 8: All drivers are loaded as shown in *Figure 8.*

National Semiconductor

DS14C335
+3.3V Supply TIA/EIA-232 3 x 5 Driver/Receiver

General Description

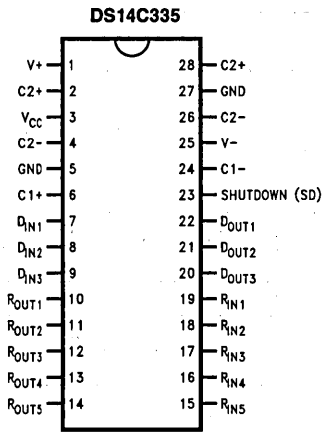
The DS14C335 is three driver, five receiver device which conforms to TIA/EIA-232-E and CCITT V.28 standard specifications. This device employs an internal DC-DC converter to generate the necessary output levels from a +3.3V power supply. A SHUTDOWN (SD) mode reduces the supply current to 10 μA maximum. In the SD mode, one receiver is active, allowing ring indicator (RI) to be monitored. PC Board space consumption is minimized by the availability of Shrink Small Outline Packaging (SSOP).

This device's low power requirement and small footprint makes it an ideal choice for Laptop and Notebook applications.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28 specifications
- Operates with single +3.3V power supply
- Low power requirement—I_{CC} 20 mA maximum
- SHUTDOWN mode—I_{CX} 10 μA maximum
- One Receiver (R5) active during SHUTDOWN
- Operates up to 128 kbps—Lap-Link® Compatible
- Flow through pinout
- 4V/μs minimum Slew Rate guaranteed
- Inter-operates with +5V UARTs
- Available in 28-lead SSOP EIAJ Type II package

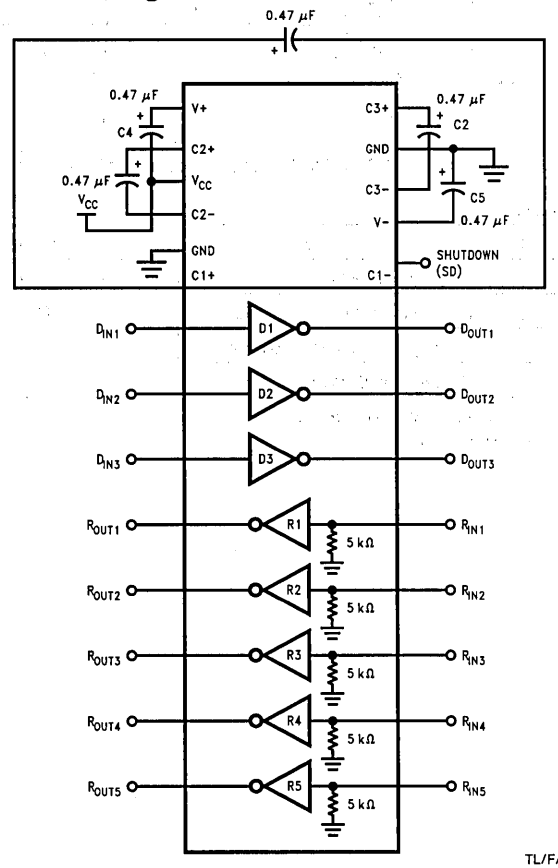
Connection Diagram



TL/F/11734-1

Order Number DS14C335MSA or DS14C335TMSA
See NS Package Number MSA28

Functional Diagram



TL/F/11734-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +14V
V^- Pin	+0.3V to −14V
Input Voltage (DIN, SD)	−0.3V to +5.5V
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous
Maximum Package Power Dissipation @ +25°C	
SSOP MSA Package	1286 mW
Derate MSA Package 10.3 mW/°C above +25C	
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 2.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
DC-DC Converter Capacitors (C1–C5)	0.47		µF
Operating Free Air Temperature (T_A)			
DS14C335	0	+70	°C
DS14C335T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DEVICE CHARACTERISTICS								
V^+	Positive Power Supply	No Load C1–C5 = 0.47 µF	D_{IN} = 0.8V			+9.3		V
V^-	Negative Power Supply		D_{IN} = 2.0V			−9.0		V
I_{CC}	Supply Current	No Load				11.5	20	mA
I_{CX}	SHUTDOWN Supply Current	R_L = 3 kΩ, SD = V_{CC}, 5.5V				1.0	10	µA
V_{IH}	High Level Enable Voltage			SD	2.0			V
V_{IL}	Low Level Enable Voltage				GND		0.8	V
I_{IH}	High Level Enable Current	2.0V ≤ V_{IN} ≤ 5.5V	0°C to +85°C				+2.0	µA
			−40°C to 0°C				+4.0	µA
I_{IL}	Low Level Enable Current	GND ≤ V_{IN} ≤ 0.8V			−2.0			µA
DRIVER CHARACTERISTICS								
V_{IH}	High Level Input Voltage		D_{IN}		2.0			V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	2.0V ≤ V_{IN} ≤ 5.5V					+1.0	µA
I_{IL}	Low Level Input Current	GND ≤ V_{IN} ≤ 0.8V			−1.0			µA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ			+5.0	+7.1		V
V_{OL}	Low Level Output Voltage					−6.3	−5.0	V
I_{OS+}	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V (Note 7)			−40	−16.5	−8	mA
I_{OS-}	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V (Note 7)			6	12.3	40	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V			300			Ω

Electrical Characteristics (Continued)

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Note 4)						
V_{TH}	Input High Threshold Voltage	R1–R5, SD = 0.8V		1.4	2.4	V
		R5, 2.0V ≤ SD ≤ 5.5V		2.0	2.8	V
V_{TL}	Input Low Threshold Voltage	R1–R5, SD = 0.8V	0.4	1.1		V
		R5, 2.0V ≤ SD ≤ 5.5V	0.1	0.5		V
V_{HY}	Hysteresis		50	300		mV
R_{IN}	Input Resistance	V_{IN} = ±3V to ±15V	3.0	3.8	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V	2.14		5.0	mA
		V_{IN} = +3V	0.43		1.0	mA
		V_{IN} = −3V	−1.0		−0.43	mA
		V_{IN} = −15V	−5.0		−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_{OH} = −1 mA	2.4	3.1		V
		V_{IN} = −3V, I_{OH} = −100 μA	2.8	3.28		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_{OL} = +2 mA		0.23	0.4	V

Switching Characteristics

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	R_L = 3 kΩ C_L = 50 pF (*Figures 1* and *2*)	0.1	0.6	1.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		0.1	0.6	1.0	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$			0	0.2	μs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF *(Figure 2)*	4	13	30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF *(Figure 2)*	4	10	30	V/μs
t_{PLS}	Propagation Delay LOW to SD	(*Figures 5* and *6*) R_L = 3 kΩ C_L = 50 pF		0.48		ms
t_{PSL}	Propagation Delay SD to LOW			1.88		ms
t_{PHS}	Propagation Delay HIGH to SD			0.62		ms
t_{PSH}	Propagation Delay SD to HIGH			1.03		ms
RECEIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	C_L = 50 pF (*Figures 3* and *4*)	0.1	0.4	1.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		0.1	0.6	1.0	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$			0.2	0.8	μs
t_{PLS}	Propagation Delay LOW to SD	(*Figures 7* and *8*) R_L = 1 kΩ C_L = 50 pF R1–R4 Only		0.13		μs
t_{PSL}	Propagation Delay SD to LOW			1.0		μs
t_{PHS}	Propagation Delay HIGH to SD			0.19		μs
t_{PSH}	Propagation Delay SD to HIGH			0.58		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

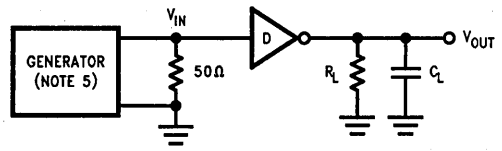
Note 4: Receiver characteristics are guaranteed for SD = 0.8V. When SD = 2.0V, receiver five (R5) is active and meets receiver parameters in SHUTDOWN (SD) mode, unless otherwise specified.

Note 5: Generator characteristics for driver input: f = 64 kHz (128 kbits/sec), $t_r = t_f < 10$ ns, V_{IH} = 3V, V_{IL} = 0V, duty cycle = 50%.

Note 6: Generator characteristics for receiver input: f = 64 kHz (128 kbits/sec), $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, duty cycle = 50%.

Note 7: Only one driver output shorted at a time.

Parameter Measurement Information



TL/F/11734–3

FIGURE 1. Driver Propagation Delay and Slew Rate Test Circuit

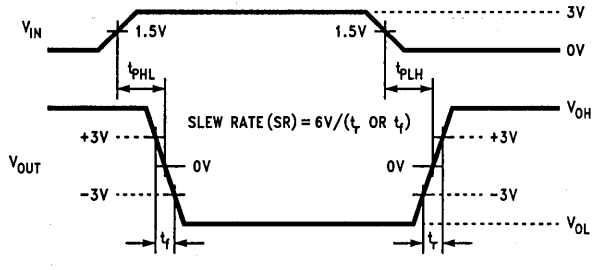


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FIGURE 2. Driver Propagation Delay and Slew Rate Timing

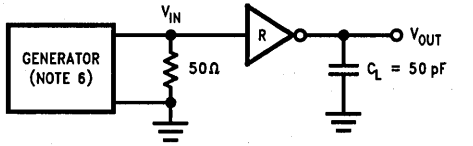

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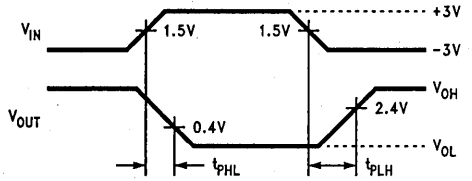
FIGURE 3. Receiver Propagation Delay Test Circuit



TL/F/11734–6

FIGURE 4. Receiver Propagation Delay Timing

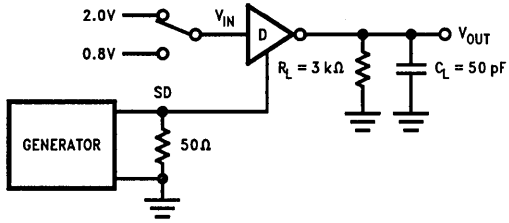


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FIGURE 5. Driver SHUTDOWN (SD) Delay Test Circuit

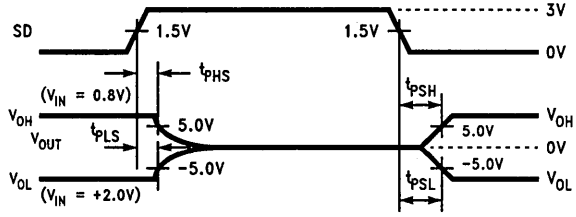

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FIGURE 6. Driver SHUTDOWN (SD) Delay Timing

Parameter Measurement Information (Continued)

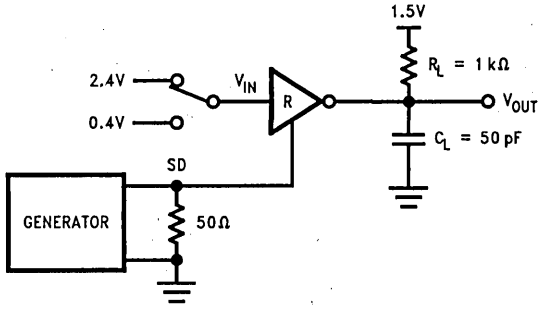

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FIGURE 7. Receiver SHUTDOWN (SD) Delay Test Circuit

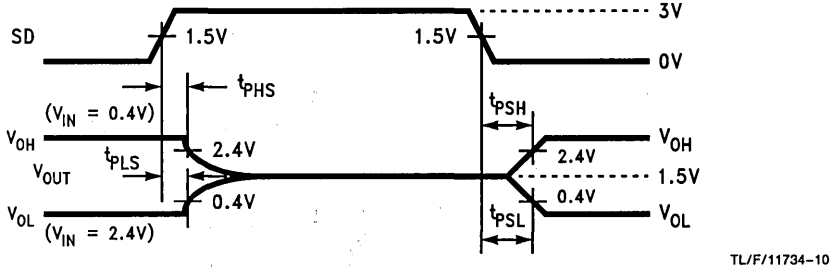

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FIGURE 8. Receiver SHUTDOWN (SD) Delay Timing

Pin Descriptions

V_{CC} (Pin 3). Power supply pin for the device, +3.3V (±0.3V).

V^+ (Pin 1). Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor—0.47 μF (16V). This supply is not intended to be loaded externally.

V^- (Pin 25). Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor—0.47 μF (16V). This supply is not intended to be loaded externally.

C1+, C1− (Pins 6, 24). External capacitor connection pins. Recommended capacitor—0.47 μF (6.3V).

C2+, C2− (Pins 2, 4). External capacitor connection pins. Recommended capacitor—0.47 μF (16V).

C3+, C3− (Pins 28, 26). External capacitor connection pins. Recommended capacitor—0.47 μF (6.3V).

SHUTDOWN (SD) (Pin 23). A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 10 μA, providing a low power state. In this mode receiver R5 remains active. The SD pin should be driven or tied low (GND) to disable the shutdown mode.

D_{IN} 1–3 (Pins 7, 8, 9). Driver input pins are JEDEC 3.3V standard compatible.

D_{OUT} 1–3 (Pins 22, 21, 20). Driver output pins conform to TIA/EIA-232 -E levels.

R_{IN} 1–5 (Pins 19, 18, 17, 16, 15). Receiver input pins accept TIA/EIA-232-E input voltages (±25V). Receivers guarantees hysteresis of TBD mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–5 (Pins 10, 11, 12, 13, 14). Receiver output pins are JEDEC 3.3V standard compatible.

GND (Pin 27). Ground Pin.

Application Information

9-Pin SERIAL PORT APPLICATION

In a typical Data Terminal Equipment (DTE) to Data Circuit-Terminating Equipment (DCE) 9-pin de-facto interface implementation, 2 data lines and 6 control lines are required. The data lines are TXD and RXD and the control lines are RTS, DTR, DSR, DCD, CTS and RI. The DS14C335 is a 3 x 5 Driver/Receiver and offers a single chip solution for the DTE interface as shown in *Figure 9*.

Ring Indicator (RI) is used to inform the DTE that an incoming call is coming from a remote DCE. When the DS14C335 is in SHUTDOWN (SD) mode, receiver five (R5) remains active and monitors RI circuit. This active receiver (R5) alerts the DTE to switch the DS14C335 from SHUTDOWN to active mode.

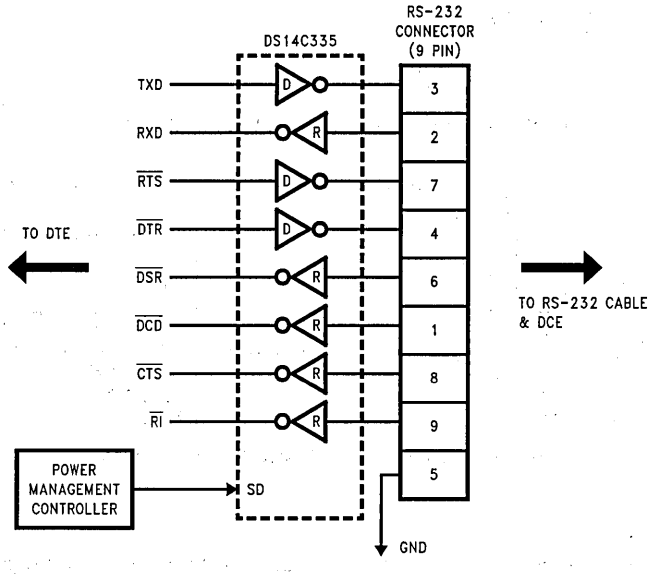

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FIGURE 9. Typical DTE Application

Application Information (Continued)

MOUSE DRIVING

The DS14C335 was tested for drive current under the following mouse driving conditions:

- Two driver outputs set at V_{OH} and their outputs were tied together (paralleled), sourcing current to supply the V+ terminal of the mouse electronics
- One driver output set at V_{OL} to sink the current from the V− terminal of the mouse electronics
- One receiver was used to accept data from the mouse
- Power Supply Voltage (V_{CC}): 3.0V to 3.6V

Completion of the testing (performed by National's Data Transmission Applications Group and a major PC manufacturer) concluded that the DS14C335 and it's DC-DC Convertor supplied adequate drive capability to power a typical PC mouse. The mouse tested was specified with the following conditions:

10 mA at +6V
5.0 mA at −6V

Since driver current is limited, it is recommended that newer lower power mice be specified for battery powered applications. Using older high power mice is wasteful of precious battery charge.

EXTERNAL DC-DC CONVERTOR COMPONENTS

The DS14C335 with it's unique DC-DC Convertor triples the power supply voltage (3.0V) to +9.3V and then inverts it to a −9V potential. This unique convertor **ONLY** requires 5 external surface mount 0.47 μF capacitors. The five identical components were chosen to simplify PCB layout and the procurement of components. The DS14C335's DC-DC Convertor also provides a larger signal swing (higher at RS-232 standard data rates) which translates to more noise margin for the rejection of ground potential differences, induced noise, and crosstalk compared to other DC-DC convertor schemes which only provide limited signal swing and limited noise margin.

DC-DC CONVERTOR CAPACITORS

The use of polarized capacitors is not required. However, if they are used, the polarity indicated in the DS14C335 Functional Diagram must be honored for proper operation. Surface mount capacitors or ceramic capacitors may be used, however, for optimal efficiency, capacitors with a low effective series resistance (ESR) should be used. Values in the low Ohms(Ω) is normally acceptable.

INTEROPERATION WITH +5V UARTs

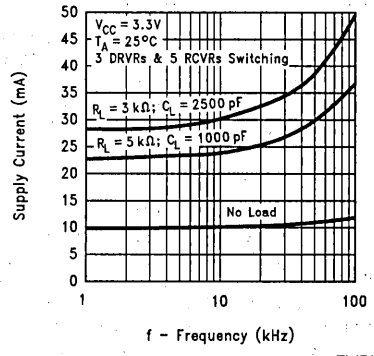
The DS14C335 provides full RS-232 driver output levels and a single chip solution for the popular 9-pin defacto serial port. This device may be used in either pure +3V applications or mixed power supplied +3V/+5V applications. The Driver Input (DIN) and ShutDown (SD) input pins can directly accept full +5V levels without the need for any external components. The Receiver Output (ROUT) is specified at 2.4V minimum while sourcing 1 mA. This level is compatible with standard TTL thresholds. For a complete discussion on "Interoperation of the DS14C335 with +5V UARTs" please see National Application Note AN-876.

POWER DISSIPATION IN REAL RS-232 APPLICATIONS

The DS14C335 DC-DC Convertor uses special circuitry that helps limit the increase in power supply current as frequency increases. A complete description of power dissipation and calculations for RS-232 applications can be found in National Application Note AN-914 titled "Understanding Power Requirements in RS-232 Applications". Typical performance curves are also located in this datasheet for quick reference.

Typical Performance Characteristics

Supply Current vs Frequency vs Driver Loads



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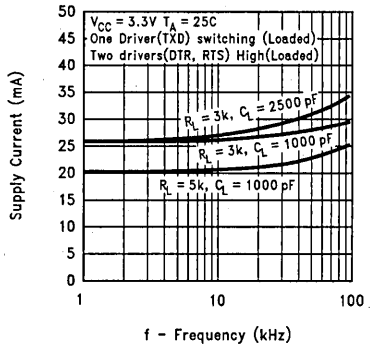
Supply Current vs Frequency vs Driver Loads



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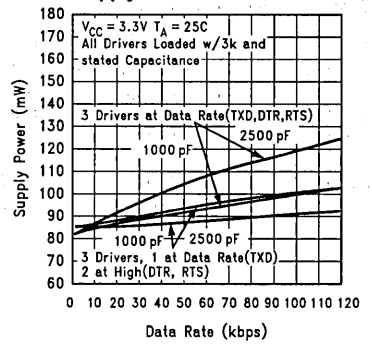
Supply Power vs Data Rate



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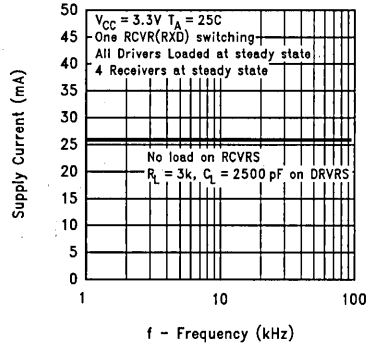
Supply Current vs Frequency (Receiver)



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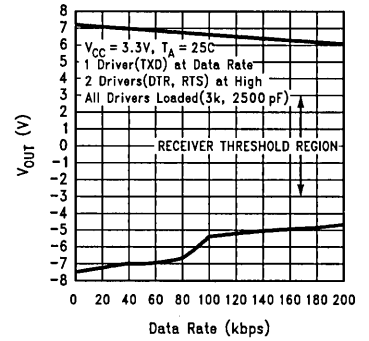
Driver Output vs Data Rate



TL/F/11734–16

National Semiconductor

ADVANCE INFORMATION

DS14C535
+5V Supply TIA/EIA-232 3 x 5 Driver/Receiver

General Description

The DS14C535 is three driver, five receiver device which conforms to TIA/EIA-232-E and CCITT V.28 standard specifications. This device employs an internal DC-DC converter to generate the necessary output levels from a +5V power supply. A SHUTDOWN (SD) mode reduces the supply current to 10 μA maximum. In the SD mode, one receiver is active, allowing ring indicator (RI) to be monitored. PC Board space consumption is minimized by the availability of Shrink Small Outline Packaging (SSOP).

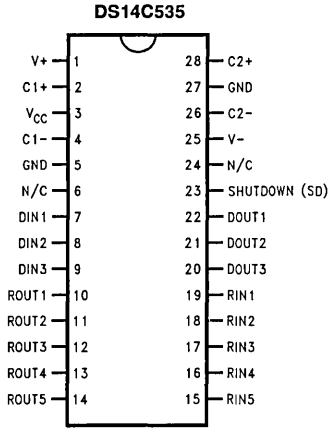
This device allows an easy migration path to the 3V DS14C335. The packages are the same. The N/C pins on the DS14C535 are not physically connected to the chip. Board layout for the DS14C335 will accommodate both devices.

This device's low power requirement and small footprint makes it an ideal choice for Laptop and Notebook applications.

Features

- Pin compatible with DS14C335
- Conforms to TIA/EIA-232-E and CCITT V.28 specifications
- Operates with single +5V power supply
- Low power requirement—I_{CC} 10 mA maximum
- SHUTDOWN mode—I_{CX} 10 μA maximum
- One Receiver (R5) active during SHUTDOWN
- Operates up to 128 kbps—Lap-Link® Compatible
- Flow through pinout
- 4V/μs minimum Slew Rate guaranteed
- Available in 28-lead SSOP EIAJ Type II package
- Only four 0.1 μF capacitors required for the DC-DC converter

Connection Diagram



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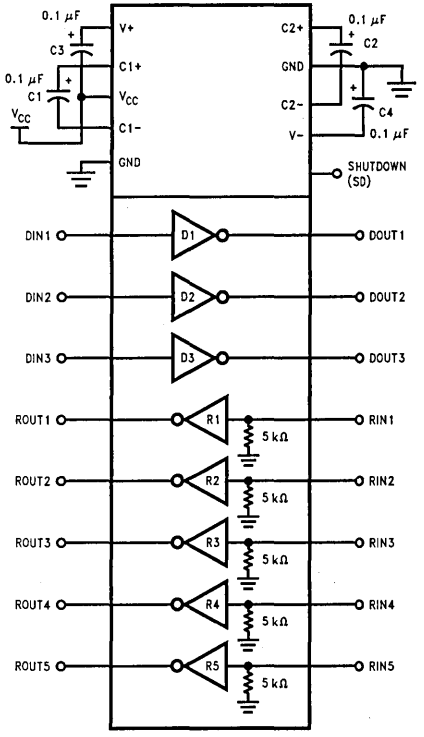
Order Number DS14C535MSA or DS14C535TMSA
See NS Package Number MSA28

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +14V
V^- Pin	+0.3V to −14V
Input Voltage (D_{IN}, SD)	−0.3V to +5.5V
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	Continuous
Maximum Package Power Dissipation @ +25°C	
SSOP MSA Package	1286 mW
Derate MSA Package 10.3 mW/°C above +25°C	
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 2.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Free Air Temperature (T_A)			
DS14C535	0	+70	°C
DS14C535T	−40	+85	°C

DC-DC Converter Capacitors (C1−C4)

Recommended range of values is 0.1 μF to 0.68 μF, ±20%. For more detail refer to application information section of this data sheet.

Electrical Characteristics

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DEVICE CHARACTERISTICS								
V^+	Positive Power Supply	No Load C1−C4 = 0.1 μF	D_{IN} = 0.8V			+9.3		V
V^-	Negative Power Supply		D_{IN} = 2.0V			−9.0		V
I_{CC}	Supply Current	No Load					10	mA
I_{CX}	SHUTDOWN Supply Current	R_L = 3 kΩ, SD = V_{CC}				1.0	10	μA
V_{IH}	High Level Enable Voltage			SD	2.0			V
V_{IL}	Low Level Enable Voltage				GND		0.8	V
I_{IH}	High Level Enable Current	2.0V ≤ V_{IN} ≤ 5.5V	0°C to +85°C				+2.0	μA
			−40°C to 0°C				+4.0	μA
I_{IL}	Low Level Enable Current	GND ≤ V_{IN} ≤ 0.8V			−2.0			μA
DRIVER CHARACTERISTICS								
V_{IH}	High Level Input Voltage		D_{IN}		2.0			V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	2.0V ≤ V_{IN} ≤ 5.5V					+1.0	μA
I_{IL}	Low Level Input Current	GND ≤ V_{IN} ≤ 0.8V			−1.0			μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ			+5.0	TBD		V
V_{OL}	Low Level Output Voltage					TBD	−5.0	V
I_{OS+}	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V (Note 7)			−40		−8	mA
I_{OS-}	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V (Note 7)			6		40	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V			300			Ω

Electrical Characteristics (Continued)

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Note 4)						
V_{TH}	Input High Threshold Voltage	R1–R5, SD = 0.8V		1.4	2.4	V
		R5, 2.0V ≤ SD ≤ 5.5V		2.0	2.8	V
V_{TL}	Input Low Threshold Voltage	R1–R5, SD = 0.8V	0.8	1.1		V
		R5, 2.0V ≤ SD ≤ 5.5V	0.1	0.5		V
V_{HY}	Hysteresis		0.2		1.0	V
R_{IN}	Input Resistance	V_{IN} = ±3V to ±15V	3.0	3.8	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V	2.14		5.0	mA
		V_{IN} = +3V	0.43		1.0	mA
		V_{IN} = −3V	−1.0		−0.43	mA
		V_{IN} = −15V	−5.0		−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_{OH} = −3.2 mA	3.5			V
		V_{IN} = −3V, I_{OH} = −20 μA	4.0			V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_{OL} = +3.2 mA		0.23	0.4	V

Switching Characteristics

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	R_L = 3 kΩ C_L = 50 pF (*Figures 1* and *2*)	0.1	0.6	1.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		0.1	0.6	1.0	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$			0	0.2	μs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF *(Figure 2)*	4	13	30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF *(Figure 2)*	4	10	30	V/μs
t_{PLS}	Propagation Delay LOW to SD	(*Figures 5* and *6*) R_L = 3 kΩ C_L = 50 pF		0.48		ms
t_{PSL}	Propagation Delay SD to LOW			1.88		ms
t_{PHS}	Propagation Delay HIGH to SD			0.62		ms
t_{PSH}	Propagation Delay SD to HIGH			1.03		ms
RECEIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	C_L = 50 pF (*Figures 3* and *4*)	0.1	0.4	1.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		0.1	0.6	1.0	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$			0.2	0.8	μs
t_{PLS}	Propagation Delay LOW to SD	(*Figures 7* and *8*) R_L = 1 kΩ C_L = 50 pF R1–R4 Only		0.13		μs
t_{PSL}	Propagation Delay SD to LOW			1.0		μs
t_{PHS}	Propagation Delay HIGH to SD			0.19		μs
t_{PSH}	Propagation Delay SD to HIGH			0.58		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

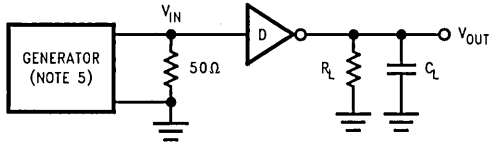
Note 4: Receiver characteristics are guaranteed for SD = 0.8V. When SD = 2.0V, receiver five (R5) is active and meets receiver parameters in SHUTDOWN (SD) mode, unless otherwise specified.

Note 5: Generator characteristics for driver input: f = 64 kHz (128 kbits/sec), $t_r = t_f < 10$ ns, V_{IH} = 3V, V_{IL} = 0V, duty cycle = 50%.

Note 6: Generator characteristics for receiver input: f = 64 kHz (128 kbits/sec), $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, duty cycle = 50%.

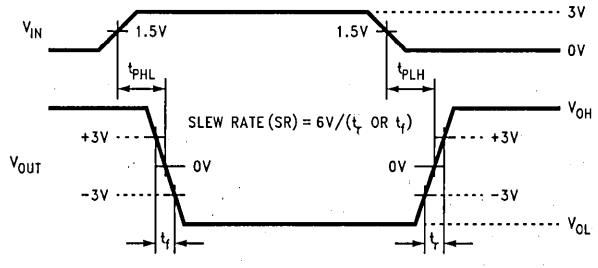
Note 7: Only one driver output shorted at a time.

Parameter Measurement Information



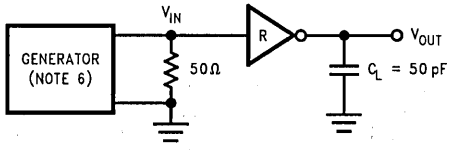
TL/F/11910–3

FIGURE 1. Driver Propagation Delay and Slew Rate Test Circuit



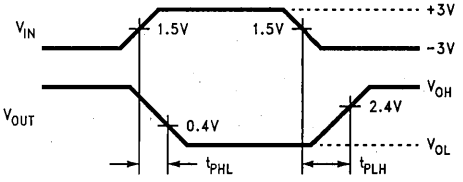
TL/F/11910–4

FIGURE 2. Driver Propagation Delay and Slew Rate Timing



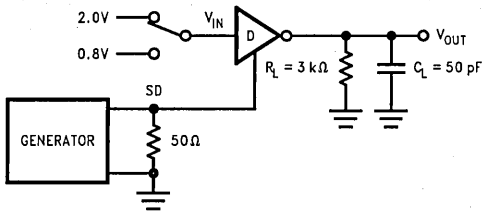
TL/F/11910–5

FIGURE 3. Receiver Propagation Delay Test Circuit



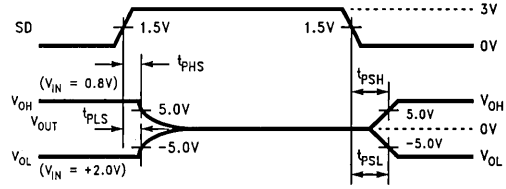
TL/F/11910–6

FIGURE 4. Receiver Propagation Delay Timing



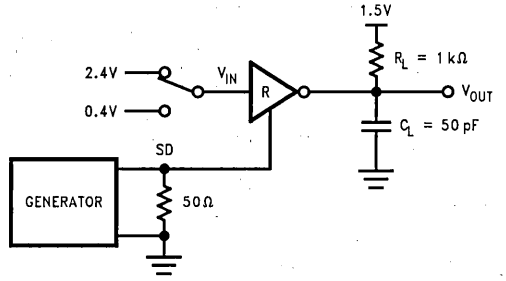
TL/F/11910–7

FIGURE 5. Driver SHUTDOWN (SD) Delay Test Circuit



TL/F/11910–8

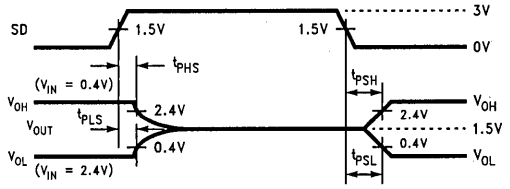
FIGURE 6. Driver SHUTDOWN (SD) Delay Timing



TL/F/11910–9

FIGURE 7. Receiver SHUTDOWN (SD) Delay Test Circuit

Parameter Measurement Information (Continued)



TL/F/11910–10

FIGURE 8. Receiver SHUTDOWN (SD) Delay Timing

Pin Descriptions

V_{CC} (Pin 3). Power supply pin for the device, +5V (±0.5V).

V^+ (Pin 1). Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor—0.1 μF (16V). This supply is not intended to be loaded externally.

V^- (Pin 25). Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor—0.1 μF (16V). This supply is not intended to be loaded externally.

C1+, C1− (Pins 2, 4). External capacitor connection pins.

C2+, C2− (Pins 28, 26). External capacitor connection pins.

SHUTDOWN (SD) (Pin 23). A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 10 μA, providing a low power state. In this mode receiver R5 remains active. The SD pin should be driven or tied low (GND) to disable the shutdown mode.

D_{IN} 1–3 (Pins 7, 8, 9). Driver input pins.

D_{OUT} 1–3 (Pins 22, 21, 20). Driver output pins conform to TIA/EIA-232 -E levels.

R_{IN} 1–5 (Pins 19, 18, 17, 16, 15). Receiver input pins accept TIA/EIA-232-E input voltages (±25V). Receivers guarantees hysteresis of TBD mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–5 (Pins 10, 11, 12, 13, 14). Receiver output pins.

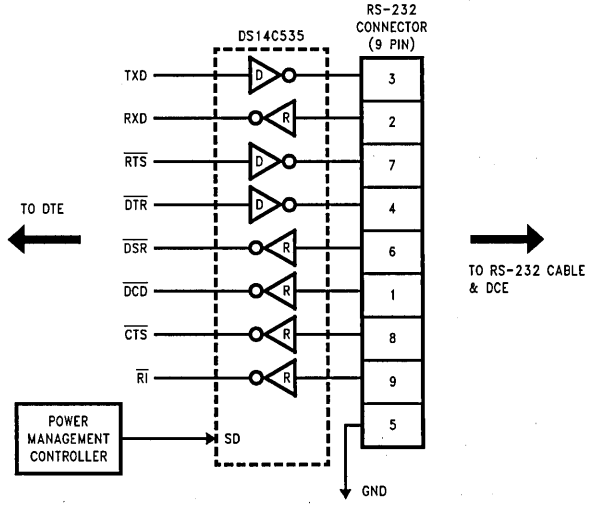
GND (Pin 27). Ground Pin.

Application Information

In a typical Data Terminal Equipment (DTE) to Data Circuit-Terminating Equipment (DCE) 9-pin de-facto interface implementation, 2 data lines and 6 control lines are required. The data lines are TXD and RXD and the control lines are RTS, DTR, DSR, DCD, CTS and RI. The DS14C535 is a 3 x 5 Driver/Receiver and offers a single chip solution for the DTE interface as shown in *Figure 9*.

Ring Indicator (RI) is used to inform the DTE that an incoming call is coming from a remote DCE. When the DS14C535 is in SHUTDOWN (SD) mode, receiver five (R5) remains active and monitors RI circuit. This active receiver (R5) alerts the DTE to switch the DS14C535 from SHUTDOWN to active mode.

To achieve minimum power consumption, the DS14C535 can be in SHUTDOWN mode and only activated when communications are needed.



TL/F/11910–11

FIGURE 9. Typical DTE Application

Application Information (Continued)

Capacitors:

Capacitors can be ceramic or tantalum. Standard surface mount in the range of 0.1 μF to 0.68 μF are readily available from several manufacturers. A minimum 30V rating is recommended. Contact manufacturers for specific detail on surface mounting and dielectrics. A partial list of manufacturers include:

Manufacturer	Phone Number
KEMET	803-963-6300
AVX	803-448-9411
MURATA-ERIE	800-831-9172

National Semiconductor

DS14C561
+3.3V-Powered 4 x 5 Driver/Receiver

General Description

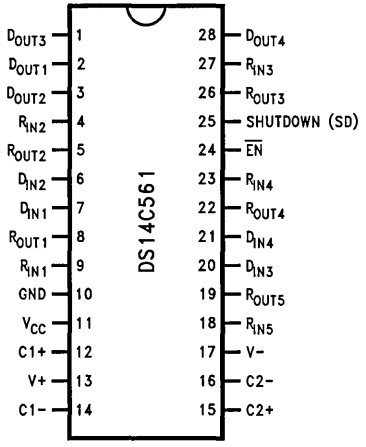
The DS14C561 is a +3.3V-powered device that conforms to the new TIA/EIA-562 standard. This standard provides a faster, lower-power alternative to TIA/EIA-232-E (RS-232) Interfaces, while guaranteeing interoperation with TIA/EIA-232-E Interfaces. The DS14C561 is guaranteed to operate with a minimum supply voltage of +3V, while maintaining the TIA/EIA-562 output signal levels ±3.7V.

The DS14C561 features an internal DC-DC converter, with four external 1.0 μF capacitors to double and invert +3.3V to ±6.6V. The device also offers a shutdown mode that reduces supply current to 100 μA, making the part ideal for use in battery-powered or power-conscious applications.

Features

- Conforms to TIA/EIA-562
- Full AC Specifications
- Internal DC-DC converter
- Operates with a single +3.3V supply
- Low power requirement I_{CC} 6 mA max
- Shutdown mode I_{CX} 100 μA max
- Operates over 64 kbits/sec
- Receiver noise filtering
- TRI-STATE® receiver outputs
- Pin compatible with MAX561

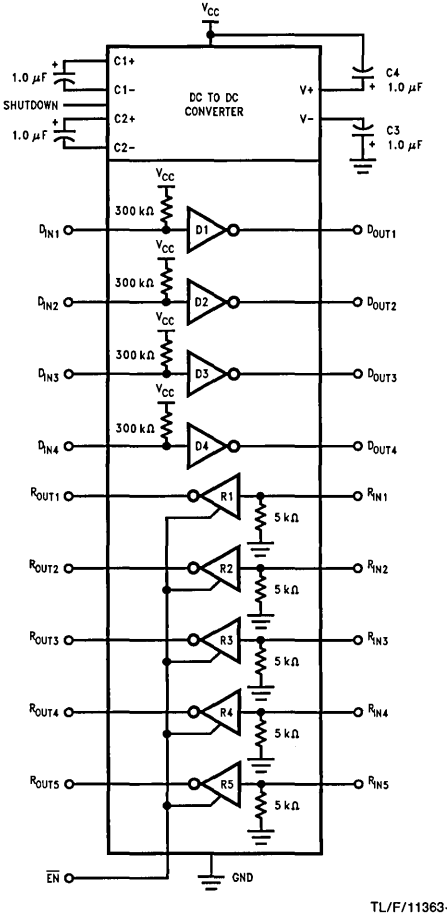
Connection Diagram



TL/F/11363–1

Order Number DS14C561WM
See NS Package Number M28B

Functional Diagram



TL/F/11363–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +14V
V^- Pin	+0.3V to −14V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6) Wide SOIC (WM) Package	1520 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Operating Free Air Temp. (T_A) DS14C561	0	+70	°C

Electrical Characteristics

V_{CC} = +3.3V ±0.3V, C1−C4 = 1 µF, T_A = 0°C to +70°C, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1−C4 = 1.0 µF	D_{IN} = 0.4V		6.0		V
V^-	Negative Power Supply		D_{IN} = 2.4V		−5.0		V
I_{CC}	Supply Current (V_{CC})	No Load			3.5	6.0	mA
I_{CX}	Supply Current Shutdown	R_L = 3 kΩ, SD = V_{CC}			20	100	µA
V_{IH}	High Level Enable Voltage		SD	2.0		V_{CC}	V
V_{IL}	Low Level Enable Voltage			GND		0.4	V
I_{IH}	High Level Enable Current			−10		+10	µA
I_{IL}	Low Level Enable Current			−10		+10	µA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage		D_{IN}	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.4	V
I_{IH}	High Level Input Current	$V_{IN} \geq$ 2.0V		−10		+10	µA
I_{IL}	Low Level Input Current	$V_{IN} \leq$ 0.4V		−10		+10	µA
		V_{IN} = 0V		−10		+10	µA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		3.7	5.0	13.2	V
V_{OL}	Low Level Output Voltage	3 Drivers Loaded		−13.2	−4.0	−3.7	V
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		3.7	4.8	13.2	V
V_{OL}	Low Level Output Voltage	4 Drivers Loaded, V_{CC} = +3.3V		−13.2	−4.2	−3.7	V
I_{OS}^+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.4V		−20	−10	−2	mA
I_{OS}^-	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V		2.0	8.0	20	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V		300			Ω
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage				1.3	2.0	V
V_{TL}	Input Low Threshold Voltage			0.4	1.0		V
V_{HY}	Hysteresis			0.05	0.3		V
R_{IN}	Input Resistance			3.0	4.5	7.0	kΩ

Electrical Characteristics (Continued)

V_{CC} = +3.3V ±0.3V, C1–C4 = 1 µF, T_A = 0°C to +70°C, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Continued)							
I_{IN}	Input Current	V_{IN} = +15V		2.14		5.0	mA
		V_{IN} = +3V		0.43		1.0	mA
		V_{IN} = −3V		−1.0		−0.43	mA
		V_{IN} = −15V		−5.0		−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −200 µA		2.6	3.0		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +1.6 mA			0.2	0.4	V
V_{IH}	High Level Input Voltage		$\overline{EN}$	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.4	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		+10	µA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.4V$		−10		+10	µA
I_{OZ}	Output Leakage Current	$\overline{EN}$ = V_{CC}, 0V ≤ R_{OUT} ≤ V_{CC}		−10		+10	µA

Switching Characteristics

V_{CC} = +3.3V ±0.3V, C1–C4 = 1 µF, T_A = 0°C to +70°C, unless otherwise specified (Note 4)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS								
t_{PLH}	Propagation Delay LOW to HIGH		R_L = 3 kΩ C_L = 50 pF (*Figures 1* and *2*)			1.0	4.0	µs
t_{PHL}	Propagation Delay HIGH to LOW					0.8	4.0	µs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$					0.2	1.0	µs
SR1	Output Slew Rate		R_L = 3 kΩ to 7 kΩ, C_L = 50 pF				30	V/µs
SR2	Output Slew Rate		R_L = 3 kΩ, C_L = 2500 pF, f = 10 kHz				30	V/µs
t_r, t_f	Output Rise, Fall Time (Note 7)	V_{CC} = 3.3V	R_L = 3 kΩ, C_L = 2500 pF, f = 10 kHz		0.2	2.7	3.1	µs
			R_L = 3 kΩ, C_L = 1000 pF, f = 32 kHz		0.2	1.7	2.1	µs
RECEIVER CHARACTERISTICS								
t_{PLH}	Propagation Delay LOW to HIGH		Input Pulse Width > 10 µs C_L = 150 pF (*Figures 3* and *4*)			3.7	9.0	µs
t_{PHL}	Propagation Delay HIGH to LOW					4.7	9.0	µs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$					1.0	3.0	µs
t_{PLZ}			(*Figures 5* and *7*)			0.2		µs
t_{PZL}						1.2		µs
t_{PHZ}			(*Figures 5* and *6*)			0.4		µs
t_{PZH}						1.2		µs
t_{NW}	Noise Pulse Width Rejected		(*Figures 3* and *4*)			4.0	1.0	µs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: I_{OS}^+ and I_{OS}^- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

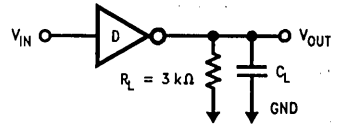
Note 4: Receiver AC input waveform for test purposes: t_r = t_f = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 32 kHz (64 kbits/sec). Driver AC input waveform for test purposes: t_r = t_f = ≤ 10 ns, V_{IH} = 3V, V_{IL} = 0V, f = 32 kHz (64 kbits/sec).

Note 5: All typicals are given for V_{CC} = 3.3V and T_A = +25°C.

Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: WM package 14.3 mW/°C..

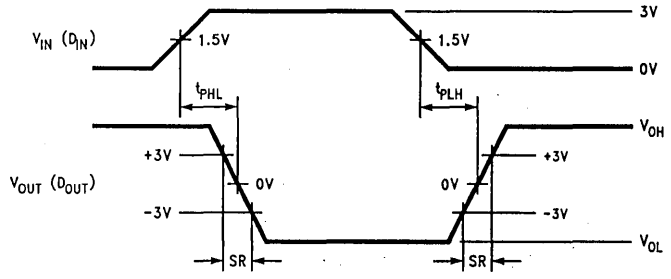
Note 7: Rise and Fall Times (t_r, t_f) are measured between the ±3.3V levels on the driver output. One output switching.

Parameter Measurement Information



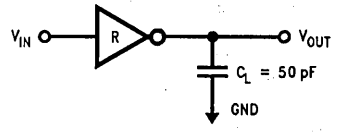
TL/F/11363-3

FIGURE 1. Driver Load Circuit



TL/F/11363-4

FIGURE 2. Driver Switching Waveform



TL/F/11363-5

FIGURE 3. Receiver Load Circuit

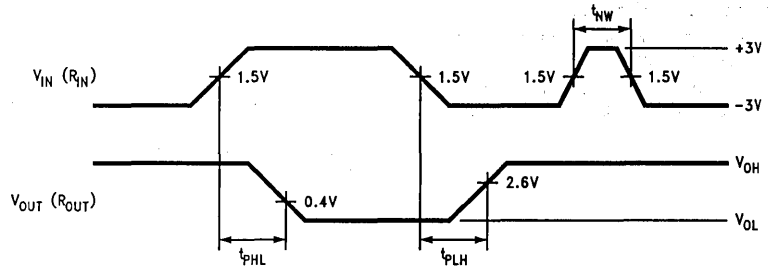


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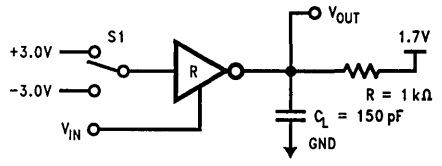
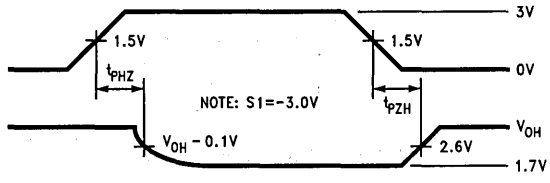
FIGURE 4. Receiver Propagation Delays and Noise Rejection



TL/F/11363-7

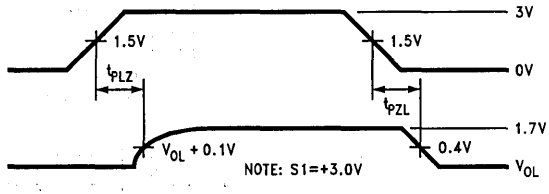
FIGURE 5. Receiver Disable Load Circuit

Parameter Measurement Information (Continued)



TL/F/11363-8

FIGURE 6. Receiver TRI-STATE® Delay Timing (t_{PHZ}, t_{PZH})



TL/F/11363-9

FIGURE 7. Receiver TRI-STATE® Delay Timing (t_{PLZ}, t_{PZL})

Pin Descriptions

V_{CC} (pin 11)—Power supply pin for the device, +3.3V ±0.3V.

V^+ (pin 13)—Positive supply for drivers. Recommended external capacitor: C4 = 1 μF. This supply is not intended to be loaded externally.

V^- (pin 17)—Negative supply for drivers. Recommended external capacitor: C3 = 1 μF. This supply is not intended to be loaded externally.

$C1^+$, $C1^-$ (pins 12 and 14)—External capacitor connection pins. Recommended capacitor: 1μF.

$C2^+$, $C2^-$ (pins 15 and 16)—External capacitor connection pins. Recommended capacitor: 1 μF.

$\overline{EN}$ (pin 24)—Controls the Receiver output TRI-STATE® Circuit. A HIGH level on this pin will disable the Receiver Output.

SHUTDOWN (SD) (pin 25)—A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 100 μA. Providing a low power state.

D_{IN} 1–4 (pins 7, 6, 20 and 21)—Inputs of unused drivers may be left open, an internal pull-up resistor pulls input to V_{CC}. Output will be LOW for open inputs. (300 kΩ minimum, typically 3.3 MΩ)

D_{OUT} 1–4 (pins 2, 3, 1 and 28)—Driver output pins conform to TIA/EIA-562 levels.

R_{IN} 1–5 (pins 9, 4, 27, 23 and 18)—Receiver input pins accept TIA/EIA-562 input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 50 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT}1–5 (pins 8, 5, 26, 22 and 19)—Receiver output pins generate a maximum V_{OL} of 0.4V given an I_O of 1.6 mA and a minimum V_{OH} of 2.6V given an I_O of −200 μA.

GND (pin 10)—Ground pin.

National Semiconductor

DS14C88/DS14C88T QUAD CMOS Line Driver

General Description

The DS14C88 and DS14C88T, pin-for-pin compatible to the DS1488/MC1488, are line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices translate standard TTL/CMOS logic levels to levels conforming to EIA-232-D and CCITT V.28 standards.

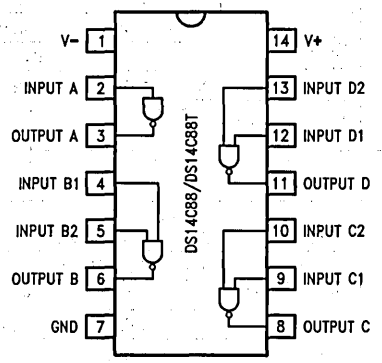
The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to its bipolar equivalents: 500 μA (DS14C88) versus 25 mA (DS1488).

The DS14C88/DS14C88T simplifies designs by eliminating the need for external slew rate control capacitors. Slew rate control in accordance with EIA-232D is provided on-chip, eliminating the output capacitors.

Features

- Meets EIA-232D and CCITT V.28 standards
- Industrial temperature range
  −40°C to +85°C—DS14C88T
- LOW power consumption
- Wide power supply range
  ±5V to ±12V
- Available in SOIC package

Connection Diagram



TL/F/11105–1

Order Number DS14C88N, DS14C88M, DS14C88TJ, DS14C88TN or DS14C88TM
See NS Package Number J14A, N14A or M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
- V^+ Pin: +13V
- V^- Pin: −13V

Driver Input Voltage: (V^+) +0.3V to GND −0.3V

Driver Output Voltage: $|(V^+) - V_O| \leq 30V$, $|(V^-) - V_O| \leq 30V$

Continuous Power Dissipation @ +25°C (Note 2)
- N Package: 1513 mW
- J Package: 1935 mW
- M Package: 1063 mW

Junction Temperature: +150°C

Lead Temperature (Soldering 4 seconds): +260°C

Storage Temperature Range: −65°C to +150°C

This Product does not meet 2000V ESD rating.

Recommended Operating Conditions

	Min	Max	Units
V^+ Supply (GND = 0V)	+4.5	+12.6	V
V^- Supply (GND = 0V)	−4.5	−12.6	V
Operating Free Air Temp. (T_A)			
DS14C88	0	+75	°C
DS14C88T	−40	+85	°C

Electrical Characteristics Over Recommended Operating Conditions, unless otherwise specified

Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_{IL}	Maximum Low Input Current	V_{IN} = GND					+10	μA
I_{IH}	Maximum High Input Current	$V_{IN} = V^+$			−10			μA
V_{IL}	Low Level Input Voltage	$V^+ \geq +7V, V^- \leq -7V$			GND		0.8	V
		$V^+ < +7V, V^- > -7V$			GND		0.6	V
V_{IH}	High Level Input Voltage				2.0		V^+	V
V_{OL}	Low Level Output Level	$V_{IN} = V_{IH}$, R_L = 3 kΩ or 7 kΩ	$V^+ = 4.5V, V^- = -4.5V$			−4.0	−3.0	V
			$V^+ = 9V, V^- = 9V$			−8.0	−6.5	V
			$V^+ = 12V, V^- = -12V$			−10.5	−9.0	V
V_{OH}	High Level Output Level	$V_{IN} = V_{IL}$, R_L = 3 kΩ or 7 kΩ	$V^+ = 4.5V, V^- = -4.5V$		3.0	4.0		V
			$V^+ = 9V, V^- = -9V$		6.5	8.0		V
			$V^+ = 12V, V^- = -12V$		9.0	10.5		V
I_{OS+}	High Level Output Short Circuit Current (Note 3)	V_{IN} = 0.8V, V_O = GND		$V^+ = +12V$, $V^- = -12V$	−45			mA
I_{OS-}	Low Level Output Short Circuit Current (Note 3)	V_{IN} = 2.0V, V_O = GND					+45	mA
R_{OUT}	Output Resistance	$V^+ = V^- = GND = 0V$, $-2V \leq V_O \leq +2V$ (Note 4) *(Figure 1)*			300			Ω
I_{CC+}	Positive Supply Current	$V_{IN} = V_{ILmax}$, R_L = OPEN	$V^+ = 4.5V, V^- = -4.5V$				10	μA
			$V^+ = 9V, V^- = -9V$				30	μA
			$V^+ = 12V, V^- = -12V$				60	μA
		$V_{IN} = V_{IHmin}$, R_L = OPEN	$V^+ = 4.5V, V^- = -4.5V$				50	μA
			$V^+ = 9V$, $V^- = -9V$	DS14C88			300	μA
				DS14C88T			400	μA
			$V^+ = 12V$, $V^- = -12V$	DS14C88			500	μA
				DS14C88T			700	μA
I_{CC-}	Negative Supply Current	$V_{IN} = V_{ILmax}$, R_L = OPEN	$V^+ = 4.5V$, $V^- = -4.5V$	DS14C88			−10	μA
				DS14C88T			−15	μA
			$V^+ = 9V$, $V^- = -9V$	DS14C88			−10	μA
				DS14C88T			−15	μA
			$V^+ = 12V$, $V^- = -12V$	DS14C88			−10	μA
				DS14C88T			−15	μA
		$V_{IN} = V_{IHmin}$, R_L = OPEN	$V^+ = 4.5V$, $V^- = -4.5V$	DS14C88			−30	μA
				DS14C88T			−45	μA
			$V^+ = 9V$, $V^- = -9V$	DS14C88			−30	μA
				DS14C88T			−45	μA
			$V^+ = 12V$, $V^- = -12V$	DS14C88			−60	μA
				DS14C88T			−80	μA

Switching Characteristics

Over Recommended Operating Conditions, unless otheriwse specified (*Figures 2* and *3*) (Notes 5 and 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Low to High	$V^+ = +4.5V, V^- = -4.5V$		1.5	6.0	μs
		$V^+ = +9.0V, V^- = -9.0V$		1.2	5.0	μs
		$V^+ = +12V, V^- = -12V$		1.2	4.0	μs
t_{PHL}	Propagation Delay High to Low	$V^+ = +4.5V, V^- = -4.5V$		1.5	6.0	μs
		$V^+ = +9.0V, V^- = -9.0V$		1.35	5.0	μs
		$V^+ = +12V, V^- = -12V$		1.3	4.0	μs
t_r	Rise Time (Note 7)		0.2	1.0		μs
t_f	Fall Time (Note 7)		0.2	1.0		μs
tsk	Typical Propagation Delay Skew	$V^+ = +4.5V, V^- = -4.5V$		250		ns
		$V^+ = +9.0V, V^- = -9.0V$		200		ns
		$V^+ = +12V, V^- = -12V$		150		ns
S_R	Output Slew Rate (Note 7)	$R_L = 3\ k\Omega$ to $7\ k\Omega$ $C_L = 15\ pF$ to $2500\ pF$			30	V/μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Derate N Package 12.1 mW/°C, J Package 12.9 mW/°C, and M Package 8.5 mW/°C above +25°C.

Note 3: I_{OS+} and I_{OS-} values are for one output at a time. If more than one output is shorted simultaneously, the device dissipation may be exceeded.

Note 4: Power supply (V^+, V^-) and GND pins are connected to ground for the Output Resistance Test (R_O).

Note 5: AC input test waveforms for test purposes: $t_r = t_f \leq 20$ ns, $V_{IH} = 2V$, $V_{IL} = 0.8V$ (0.6V at $V^+ = 4.5V$, $V^- = -4.5V$)

Note 6: Input rise and rall times must not exceed 5 μs.

Note 7: The output slew rate, rise time, and fall time are measured from the +3.0V to the −3.0V level on the output waveform.

Note 8: C_L include jig and probe capacitances.

Parameter Measure Information

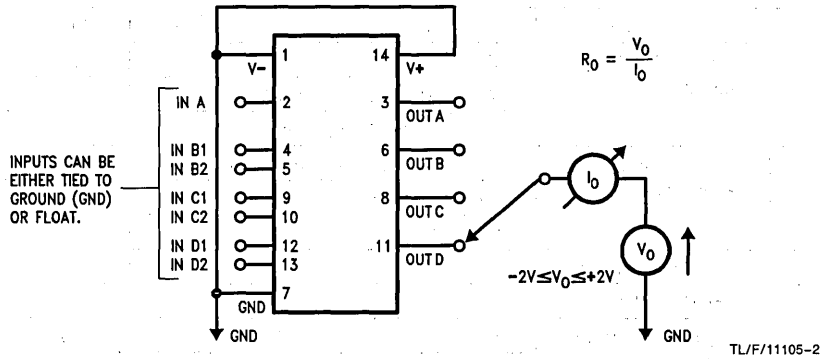


FIGURE 1. Output Resistance Test Circuit (Power-Off)

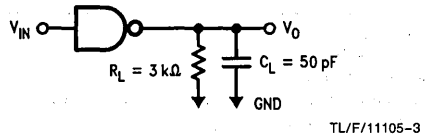


FIGURE 2. Driver Load Circuit (Note 8)

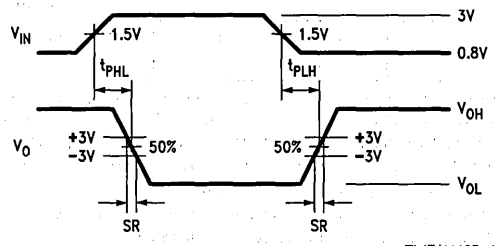


FIGURE 3. Driver Switching Waveform

Typical Application Information

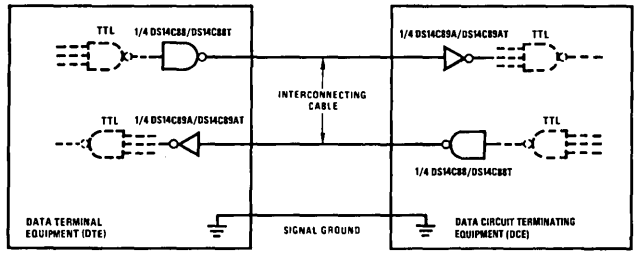


FIGURE 4. EIA-232D Data Transmission

National Semiconductor

DS1488 Quad Line Driver

General Description

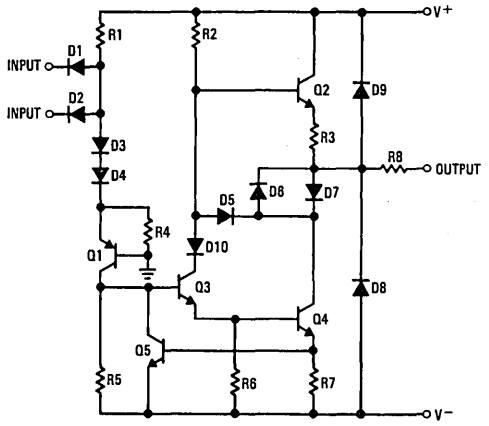
The DS1488 is a quad line driver which converts standard TTL input logic levels through one stage of inversion to output levels which meet EIA Standard RS-232D and CCITT Recommendation V.24.

Features

- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are TTL/LS compatible

Schematic and Connection Diagrams

1/4 Circuit



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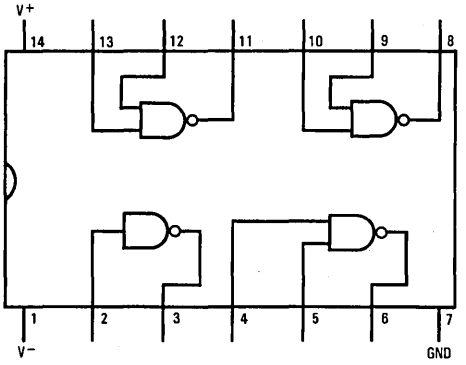
Dual-In-Line Package



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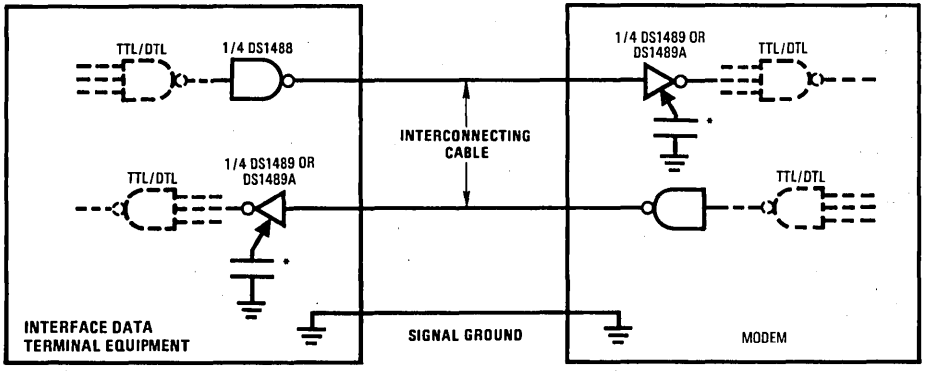
Top View

Order Number DS1488J, DS1488M or DS1488N
See NS Package Number J14A, M14A or N14A

Typical Applications

RS-232C Data Transmission



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*Optional for noise filtering

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
V^+	+15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \le V_{IN} \le 7.0V$
Output Voltage	±15V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded DIP Package	1280 mW
SO Package	974 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded DIP package 10.2 mW/°C above 25°C; derate SO package 7.8 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) $V_{CC}+ = 9V, V_{CC}- = -9V$ unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IL}	Logical "0" Input Current	$V_{IN} = 0V$			−1.0	−1.3	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = +5.0V$			0.005	10.0	µA
V_{OH}	High Level Output Voltage	$R_L = 3.0\ k\Omega$, $V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$	6.0	7.0		V
			$V^+ = 13.2V, V^- = -13.2V$	9.0	10.5		V
V_{OL}	Low Level Output Voltage	$R_L = 3.0\ k\Omega$, $V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$	−6.0	−6.8		V
			$V^+ = 13.2V, V^- = -13.2V$	−9.0	−10.5		V
$I_{OS}+$	High Level Output Short-Circuit Current	$V_{OUT} = 0V, V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
$I_{OS}-$	Low Level Output Short-Circuit Current	$V_{OUT} = 0V, V_{IN} = 1.9V$		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V, V_{OUT} = \pm 2V$		300			Ω
$I_{CC}+$	Positive Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$		15.0	20.0	mA
			$V^+ = 12V, V^- = -12V$		19.0	25.0	mA
			$V^+ = 15V, V^- = -15V$		25.0	34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$		4.5	6.0	mA
			$V^+ = 12V, V^- = -12V$		5.5	7.0	mA
			$V^+ = 15V, V^- = -15V$		8.0	12.0	mA
$I_{CC}-$	Negative Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$		−13.0	−17.0	mA
			$V^+ = 12V, V^- = -12V$		−18.0	−23.0	mA
			$V^+ = 15V, V^- = -15V$		−25.0	−34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$		−0.001	−0.015	mA
			$V^+ = 12V, V^- = -12V$		−0.001	−0.015	mA
			$V^+ = 15V, V^- = -15V$		−0.01	−2.5	mA
P_d	Power Dissipation	$V^+ = 9.0V, V^- = -9.0V$			252	333	mW
		$V^+ = 12V, V^- = -12V$			444	576	mW

Switching Characteristics ($V_{CC} = 9V, V_{EE} = -9V, T_A = 25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logical "1"	$R_L = 3.0\ k\Omega, C_L = 15\ pF, T_A = 25°C$		230	350	ns
t_{pd0}	Propagation Delay to a Logical "0"	$R_L = 3.0\ k\Omega, C_L = 15\ pF, T_A = 25°C$		70	175	ns
t_r	Rise Time	$R_L = 3.0\ k\Omega, C_L = 15\ pF, T_A = 25°C$		75	100	ns
t_f	Fall Time	$R_L = 3.0\ k\Omega, C_L = 15\ pF, T_A = 25°C$		40	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1488.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the DS1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}(\Delta T/\Delta V)$$

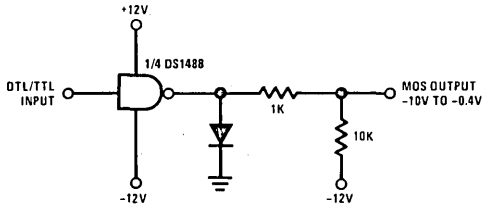
where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS-232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

See Typical Performance Characteristics.

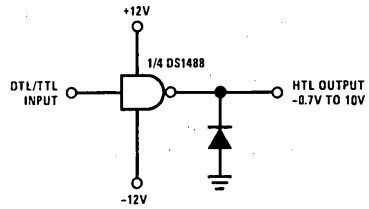
Typical Applications (Continued)

DTL/TTL-to-MOS Translator



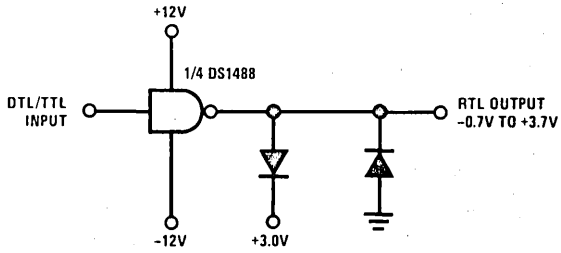
TL/F/5776–4

DTL/TTL-to-HTL Translator



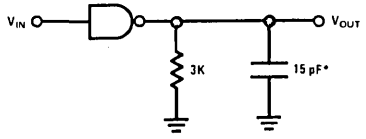
TL/F/5776–5

DTL/TTL-to-RTL Translator



TL/F/5776–6

AC Load Circuit and Switching Time Waveforms



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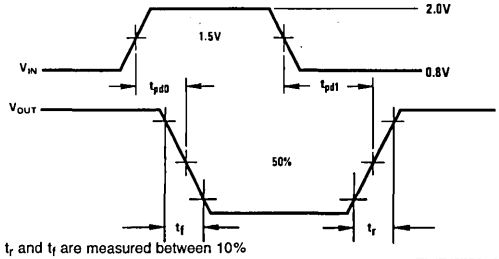
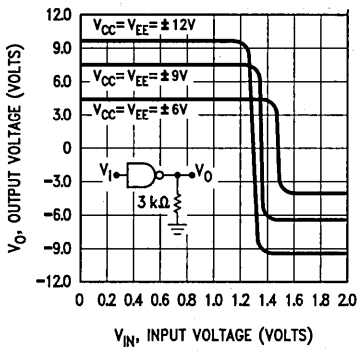
*C_L includes probe and jig capacitance.



t_r and t_f are measured between 10% and 90% of the output waveform.

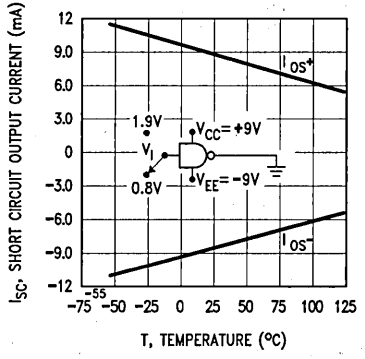
TL/F/5776–8

Typical Performance Characteristics T_A = +25°C unless otherwise noted



TL/F/5776–9

FIGURE 1. Transfer Characteristics vs Power Supply Voltage



TL/F/5776–10

FIGURE 2. Short-Circuit Output Current vs Temperature

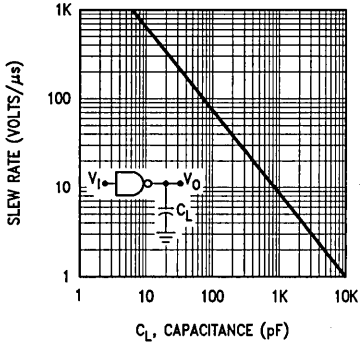


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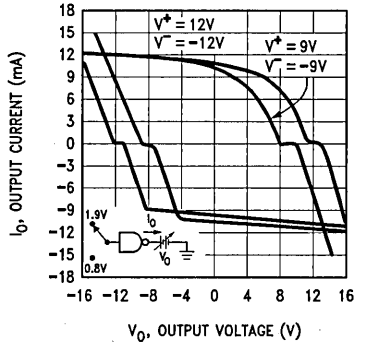
FIGURE 3. Output Slew Rate vs Load Capacitance



TL/F/5776–12

FIGURE 4. Output Voltage and Current-Limiting Characteristics

National Semiconductor

DS14C89A/DS14C89AT Quad CMOS Receiver

General Description

The DS14C89A/DS14C89AT, pin-for-pin compatible to the DS1489A/MC1489A, are receivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices translate levels conforming to EIA-232E and CCITT V.28 standards to TTL/CMOS logic levels.

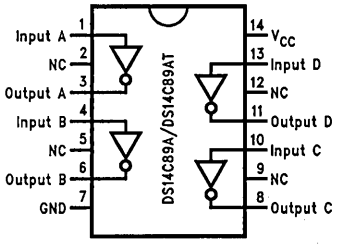
The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to their bipolar equivalents: 900 μA (DS14C89A) versus 26 mA (DS1489A).

The DS14C89A/DS14C89AT provide on chip noise filtering which eliminates the need for external response control filter capacitors. When replacing the DS1489A with the DS14C89A/DS14C89AT, the response control filter pins can be tied high, low, or not connected.

Features

- Meets EIA/TIA-232-E and CCITT V.28 Standards
- Industrial Temperature Range
  −40°C to +85°C–DS14C89AT
- LOW Power consumption
- On chip noise filter
- Available in SOIC Package

Connection Diagram



TL/F/11106–1

Order Number DS14C89AN, DS14C89AM, DS14C89ATJ, DS14C89ATN, DS14C89ATM
See NS Package Number J14A, M14A, N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC}	+6V
Input Voltage	−30V to +30V
Receiver Output Voltage	(V_{CC}) +0.3V to GND−0.3V
Junction Temperature	+150°C
Continuous Power Dissipation @ +25°C (Note 2)	
N Package	1513 mW
J Package	1935 mW
M Package	1063 mW
Lead Temp. (Soldering 4 seconds)	+260°C
Storage Temp. Range	−65°C to +150°C
ESD Rating ≥ 1.8 kV, Typically ≥ 2 kV (HMB, 1.5 kΩ, 100 pF)	

Recommended Operating Conditions

	Min	Max	Units
V_{CC} (GND = 0V)	+4.5	+5.5	V
Operating Free Air Temp. (T_A)			
DS14C89A	0	+75	°C
DS14C89AT	−40	+85	°C

Electrical Characteristics Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Input High Threshold				1.3		2.7	V
V_{TL}	Input Low Threshold				0.5		1.9	V
V_{HY}	Typical Input Hysteresis					1.0		V
I_{IN}	Input Current	V_{IN} = +25V	V_{CC} = +4.5V to +5.5V		3.6		8.3	mA
		V_{IN} = −25V			−3.6		−8.3	mA
		V_{IN} = +3V			0.43		1.0	mA
		V_{IN} = −3V			−0.43		−1.0	mA
		V_{IN} = +15V	V_{CC} = 0V (Power-Off) (Note 4)		2.14		5.0	mA
		V_{IN} = −15V			−2.14		−5.0	mA
		V_{IN} = +3V			0.43		1.0	mA
		V_{IN} = −3V			−0.43		−1.0	mA
V_{OH}	Output High Voltage	V_{IN} = V_{TL} (min)	I_{OUT} = −3.2 mA		2.8	4.0		V
			I_{OUT} = −20μA		3.5	4.7		V
V_{OL}	Output Low Voltage	V_{IN} = V_{TH} (max) I_{OUT} = +3.2 mA				0.15	0.4	V
I_{CC}	Supply Current	No Load V_{IN} = 2.7V or 0.5V		DS14C89A		0.5	900	μA
				DS14C89AT		0.5	2.0	mA

AC Electrical Characteristics

Over recommended operating conditions, unless otherwise specified, C_l = 50 pF (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Low to High	Input Pulse Width ≥ 10 μs		3.5	6.5	μs
t_{PHL}	Propagation Delay High to Low	Input Pulse Width ≥ 10 μs		3.2	6.5	μs
t_{SK}	Typical Propagation Delay Skew			400		ns
t_r	Output Rise Time			40	300	ns
t_f	Output Fall Time			40	300	ns
t_{nw}	Pulse Width assumed to be Noise				1.0	μs

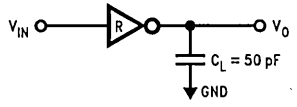
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Derate N Package 12.1 mW/°C, J Package 12.9 mW/°C, and M Package 8.5 mW/°C above +25°C.

Note 3: AC input waveforms for test purposes: t_r = t_f = 200 ns, V_{IH} = +3V, V_L = −3V, f = 20 KHz.

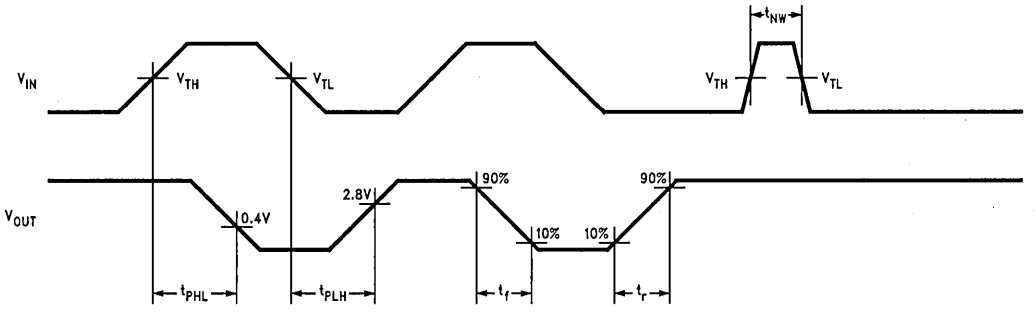
Note 4: Under the power-off supply conditions it is assumed that the power supply potential drops to zero (0V) and is replaced by a low impedance or short circuit to ground.

Parameter Measurement Information



TL/F/11106–2

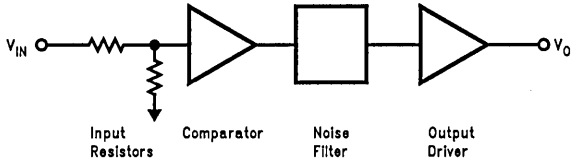
FIGURE 1: Receiver Load Circuit



TL/F/11106–3

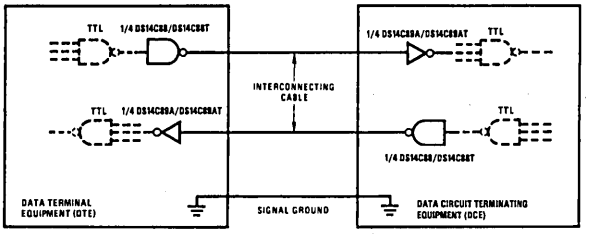
FIGURE 2: Receiver Switching Waveform (Note 3)

Typical Application Information



TL/F/11106–4

FIGURE 3. Receiver Block Diagram



TL/F/11106–5

FIGURE 4. EIA-232D Data Transmission

National Semiconductor

DS1489/DS1489A Quad Line Receiver

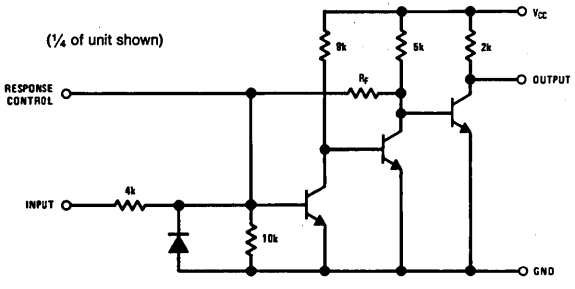
General Description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA Standard RS-232D. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements.

Features

- Four separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode: high output for open inputs
- Inputs withstand ±30V

Schematic and Connection Diagrams



DS1489: R_F = 10k
DS1489A: R_F = 2k

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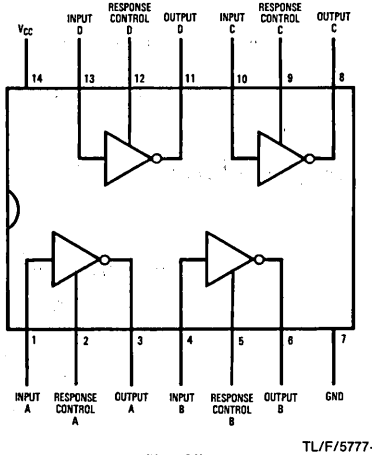
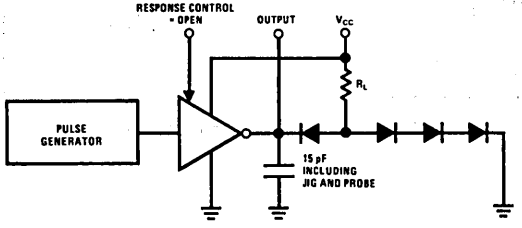
Dual-In-Line Package



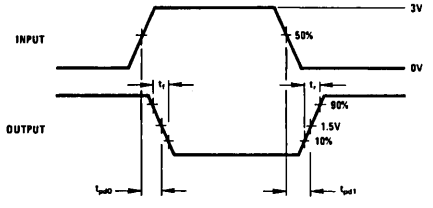
TL/F/5777–2

Top View
Order Number DS1489J, DS1489M, DS1489AM, DS1489N or DS1489AN
See NS Package Number J14A, M14A or N14A

AC Test Circuit and Voltage Waveforms



TL/F/5777–3



TL/F/5777–4

FIGURE 1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20 mA
Power Dissipation (Note 2)	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded DIP Package	1207 mW
SO Package	1042 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 9.7 mW/°C above 25°C; derate SO package 8.33 mW/°C above 25°C.

Electrical Characteristics (Notes 2, 3 and 4)

DS1489/DS1489A: The following apply for V_{CC} = 5.0V ±1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Input High Threshold Voltage	V_{OUT} ≤ 0.45V, I_{OUT} = 10 mA	DS1489	T_A = 25°C	1.0	1.25	1.5	V
					0.9		1.6	V
			DS1489A	T_A = 25°C	1.75	2.00	2.25	V
					1.55		2.40	V
V_{TL}	Input Low Threshold Voltage	V_{OUT} ≥ 2.5V, I_{OUT} = −0.5 mA		T_A = 25°C	0.75	1.00	1.25	V
					0.65		1.35	V
I_{IN}	Input Current	V_{IN} = +25V			+3.6	+5.6	+8.3	mA
		V_{IN} = −25V			−3.6	−5.6	−8.3	mA
		V_{IN} = +3V			+0.43	+0.53		mA
		V_{IN} = −3V			−0.43	−0.53		mA
V_{OH}	Output High Voltage	I_{OUT} = −0.5 mA	V_{IN} = 0.75V		2.6	3.8	5.0	V
			Input = Open		2.6	3.8	5.0	V
V_{OL}	Output Low Voltage	V_{IN} = 3.0V, I_{OUT} = 10 mA				0.33	0.45	V
I_{SC}	Output Short Circuit Current	V_{IN} = 0.75V				−3.0		mA
I_{CC}	Supply Current	V_{IN} = 5.0V				14	26	mA
P_d	Power Dissipation	V_{IN} = 5.0V				70	130	mW

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Input to Output "High" Propagation Delay	R_L = 3.9k, *(Figure 1)* (AC Test Circuit)		28	85	ns
t_{pd0}	Input to Output "Low" Propagation Delay	R_L = 390Ω, *(Figure 1)* (AC Test Circuit)		20	50	ns
t_r	Output Rise Time	R_L = 3.9k, *(Figure 1)* (AC Test Circuit)		110	175	ns
t_f	Output Fall Time	R_L = 390Ω, *(Figure 1)* (AC Test Circuit)		9	20	ns

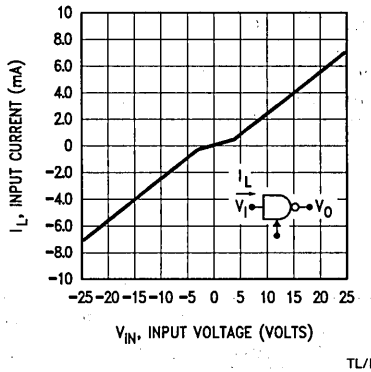
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1489 and DS1489A.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

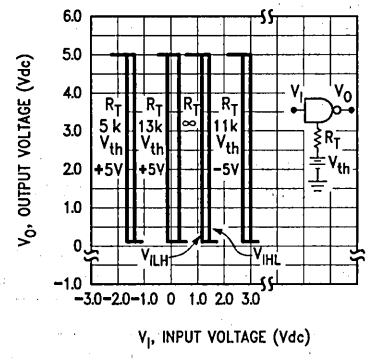
Note 4: These specifications apply for response control pin = open.

Typical Characteristics V_{CC} = 5.0V, T_A = +25°C unless otherwise noted



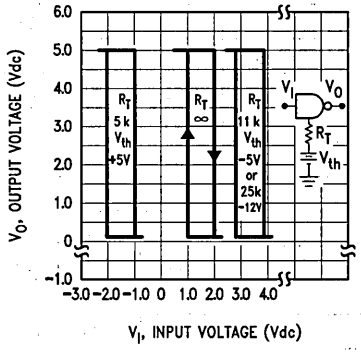
TL/F/5777–7

FIGURE 2. Input Current



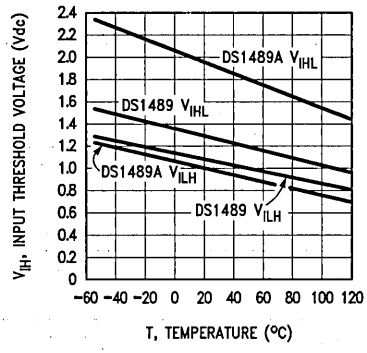
TL/F/5777–8

FIGURE 3. DS1489 Input Threshold Voltage Adjustment



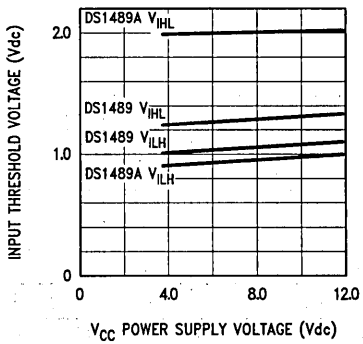
TL/F/5777–9

FIGURE 4. DS1489A Input Threshold Voltage Adjustment



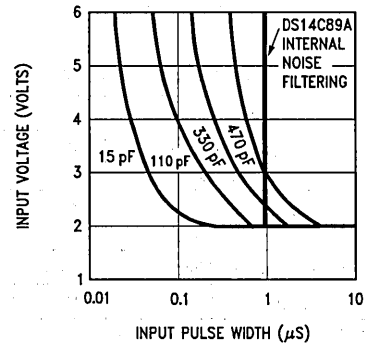
TL/F/5777–10

FIGURE 5. Input Threshold Voltage vs Temperature



TL/F/5777–11

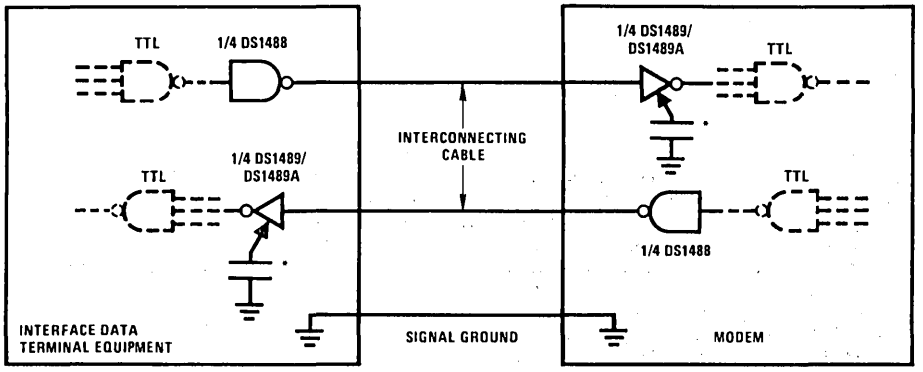
FIGURE 6. Input Threshold vs Power Supply Voltage



TL/F/5777–12

FIGURE 7. Noise Rejection vs Capacitance for DS1489A

Typical Application Information

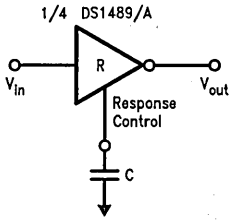


*Optional for noise filtering.

TL/F/5777–5

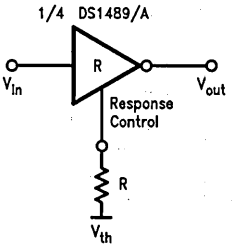
Applications Using the Response Control Pin

Noise Filter
(See *Figure 7*)



TL/F/5777–13

Threshold Shift
(See *Figures 3* and *4*)



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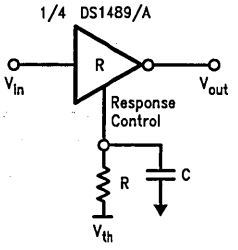
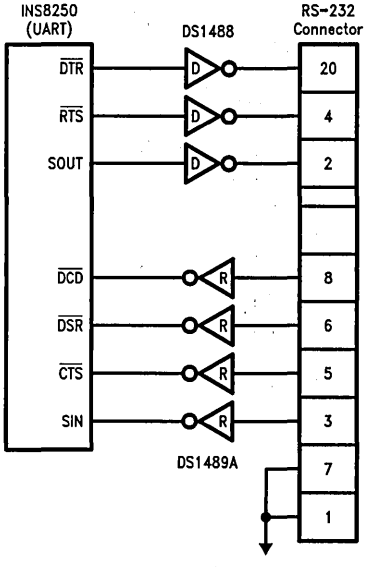
Noise Filter and Threshold Shift
(See *Figures 3, 4* and *7*)



TL/F/5777–15

Application of DS148, DS1489A and INS8250



TL/F/5777–16

National Semiconductor

DS75150 Dual Line Driver

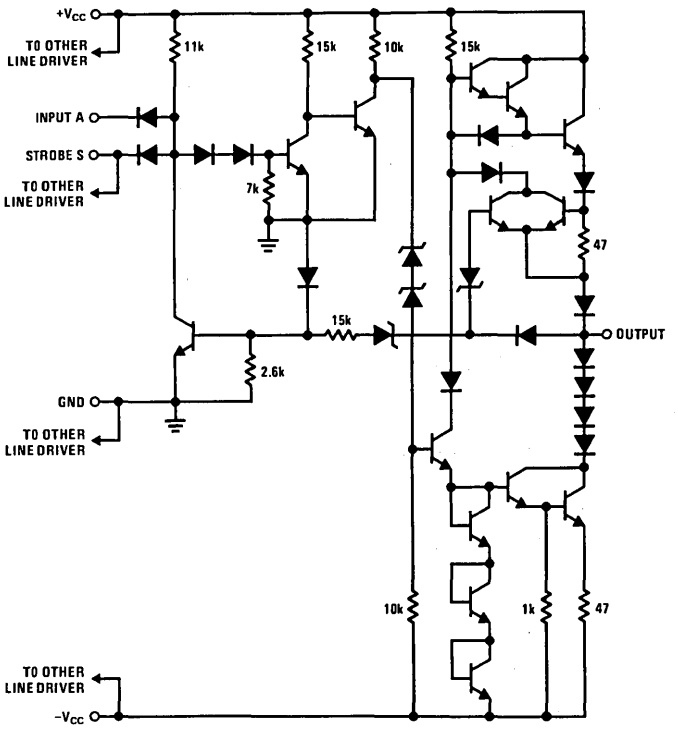
General Description

The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and LS families. Operation is from −12V and +12V power supplies.

Features

- Withstands sustained output short-circuit to any low impedance voltage between −25V and +25V
- 2 μs max transition time through the −3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and LS families
- Common strobe input
- Inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages ±12V

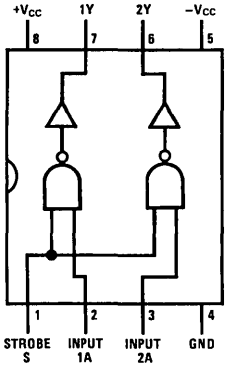
Schematic and Connection Diagrams



TL/F/5794–1

Component values shown are nominal.
1/2 of circuit shown

Dual-In-Line Package



TL/F/5794–2

Top View

Positive Logic C = $\overline{AS}$

Order Number
DS75150M or DS75150N
See NS Package Number
M08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $+V_{CC}$	15V
Supply Voltage $-V_{CC}$	15V
Input Voltage	15V
Applied Output Voltage	+25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded DIP Package	1022 mW
SO Package	655 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate molded DIP package 8.2 mW/°C above 25°C. Derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage ($+V_{CC}$)	10.8	13.2	V
Supply Voltage ($-V_{CC}$)	−10.8	−13.2	V
Input Voltage (V_I)	0	+5.5	V
Output Voltage (V_O)		±15	V
Operating Ambient Temperature Range (T_A)	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low-Level Input Voltage	*(Figure 2)*				0.8	V
V_{OH}	High-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −13.2V, V_{IL} = 0.8V, R_L = 3 kΩ to 7 kΩ *(Figure 2)*		5	8		V
V_{OL}	Low-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −10.8V, V_{IH} = 2V, R_L = 3 kΩ to 7 kΩ *(Figure 1)*			−8	−5	V
I_{IH}	High-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 2.4V, *(Figure 3)*	Data Input		1	10	μA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 2.4V, *(Figure 3)*	Strobe Input		2	20	μA
I_{IL}	Low-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0.4V, *(Figure 3)*	Data Input		−1	−1.6	mA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0.4V, *(Figure 3)*	Strobe Input		−2	−3.2	mA
I_{OS}	Short-Circuit Output Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, *(Figure 4)*, (Note 4)	V_O = 25V		2	5	mA
			V_O = −25V		−3	−6	mA
			V_O = 0V, V_I = 3V		15	30	mA
			V_O = 0V, V_I = 0V		−15	−30	mA
$+I_{CCH}$	Supply Current From $+V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			10	22	mA
$-I_{CCH}$	Supply Current From $-V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−1	−10	mA
$+I_{CCL}$	Supply Current From $+V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			8	17	mA
$-I_{CCL}$	Supply Current From $-V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−9	−20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75150. All typical values are T_A = 25°C and $+V_{CC}$ = 12V, $-V_{CC}$ = −12V.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

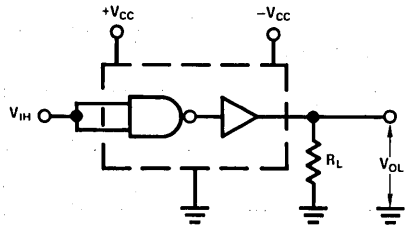
Note 4: Only one output at a time should be shorted.

Note 5: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5V is the maximum, the typical value is more-negative voltage.

AC Electrical Characteristics ($+V_{CC}$ = 12V, $-V_{CC}$ = −12V, T_A = 25°C)

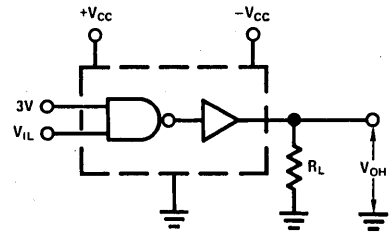
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.4	2	μs
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.5	2	μs
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		40		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		20		ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		60		ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		45		ns

DC Test Circuits



TL/F/5794–3

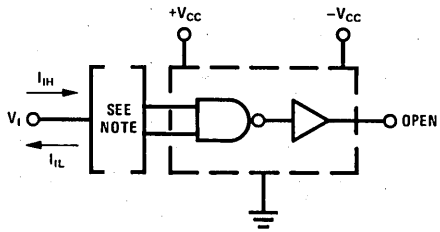
FIGURE 1. V_{IH}, V_{OL}



TL/F/5794–4

Each input is tested separately.

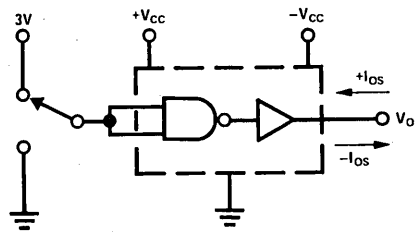
FIGURE 2. V_{IL}, V_{OH}



TL/F/5794–5

Note: When testing I_{IH}, the other input is at 3V; when testing I_{IL}, the other input is open.

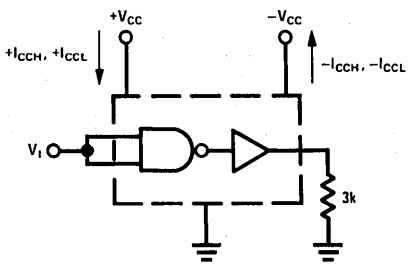
FIGURE 3. I_{IH}, I_{IL}



TL/F/5794–6

I_{OS} is tested for both input conditions at each of the specified output conditions.

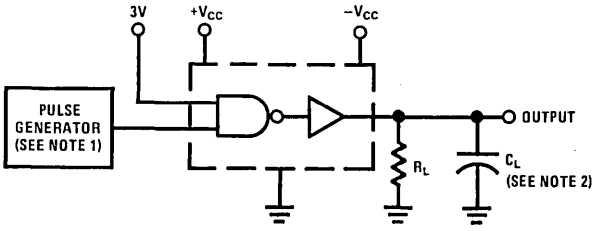
FIGURE 4. I_{OS}



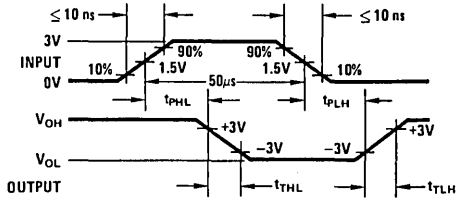
TL/F/5794–7

FIGURE 5. $I_{CCH}+$, $I_{CCH}-$, $I_{CCL}+$, $I_{CCL}-$

AC Test Circuit and Switching Waveforms



TL/F/5794–8



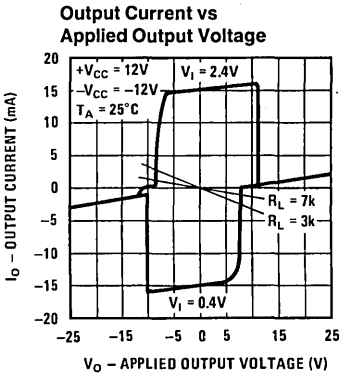
TL/F/5794–9

Note 1: The pulse generator has the following characterstics: duty cycle ≤ 50%, $Z_{OUT} \cong 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6

Typical Performance Characteristics



TL/F/5794–10

FIGURE 7

National Semiconductor

DS75154 Quad Line Receiver

General Description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and LS circuits when either supply voltage is used.

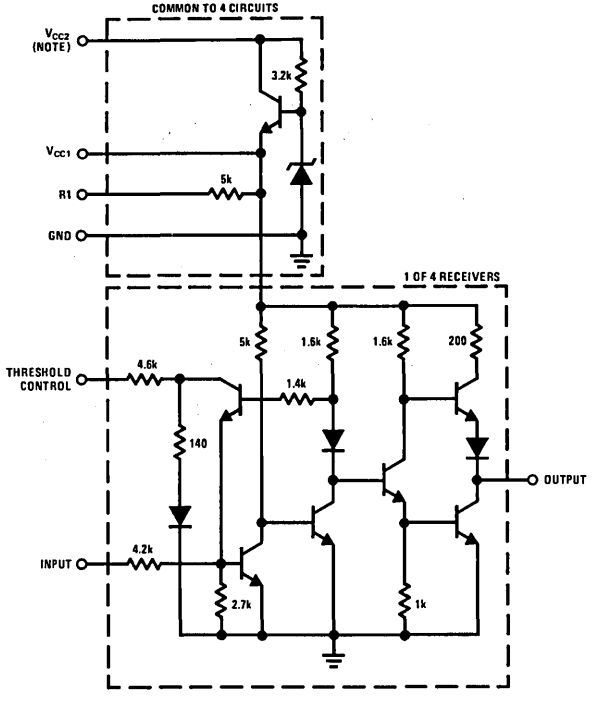
In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

Features

- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with TTL or LS
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

Schematic Diagram



TL/F/5795–1

Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Normal Supply Voltage (Pin 15), (V_{CC1})	7V
Alternate Supply Voltage (Pin 16), (V_{CC2})	14V
Input Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded DIP Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (Pin 15), (V_{CC1})	4.5	5.5	V
Alternate Supply Voltage (Pin 16), (V_{CC2})	10.8	13.2	V
Input Voltage		±15	V
Temperature, (T_A)	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 1)*		3			V
V_{IL}	Low-Level Input Voltage	*(Figure 1)*				−3	V
V_{T+}	Positive-Going Threshold Voltage	*(Figure 1)*	Normal Operation	0.8	2.2	3	V
			Fail-Safe Operation	0.8	2.2	3	V
V_{T-}	Negative-Going Threshold Voltage	*(Figure 1)*	Normal Operation	−3	−1.1	0	V
			Fail-Safe Operation	0.8	1.4	3	V
$V_{T+}-V_{T-}$	Hysteresis	*(Figure 1)*	Normal Operation	0.8	3.3	6	V
			Fail-Safe Operation	0	0.8	2.2	V
V_{OH}	High-Level Output Voltage	$I_{OH}=-400\ \mu A$, *(Figure 1)*		2.4	3.5		V
V_{OL}	Low-Level Output Voltage	$I_{OL}=16$ mA, *(Figure 1)*			0.23	0.4	V
r_I	Input Resistance	*(Figure 2)*	$\Delta V_I=-25V$ to $-14V$	3	5	7	kΩ
			$\Delta V_I=-14V$ to $-3V$	3	5	7	kΩ
			$\Delta V_I=-3V$ to $+3V$	3	6		kΩ
			$\Delta V_I=3V$ to 14V	3	5	7	kΩ
			$\Delta V_I=14V$ to 25V	3	5	7	kΩ
$V_{I(OPEN)}$	Open-Circuit Input Voltage	$I_I=0$, *(Figure 3)*		0	0.2	2	V
I_{OS}	Short-Circuit Output Current (Note 5)	$V_{CC1}=5.5V$, $V_I=-5V$, *(Figure 4)*		−10	−20	−40	mA
I_{CC1}	Supply Current From V_{CC1}	$V_{CC1}=5.5V$, $T_A=25°C$, *(Figure 5)*			20	35	mA
I_{CC2}	Supply Current From V_{CC2}	$V_{CC2}=13.2V$, $T_A=25°C$, *(Figure 5)*			23	40	mA

Switching Characteristics ($V_{CC1}=5V$, $T_A=25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		20		ns
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		9		ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75154. All typical values are for $T_A=25°C$ and $V_{CC1}=5V$.

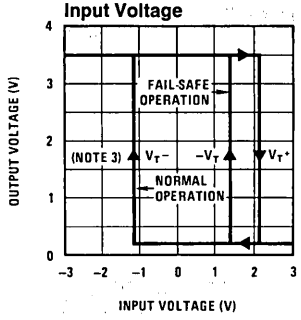
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3V is the maximum, the minimum limit is a more-negative voltage.

Note 5: Only one output at a time should be shorted.

Typical Performance Characteristics

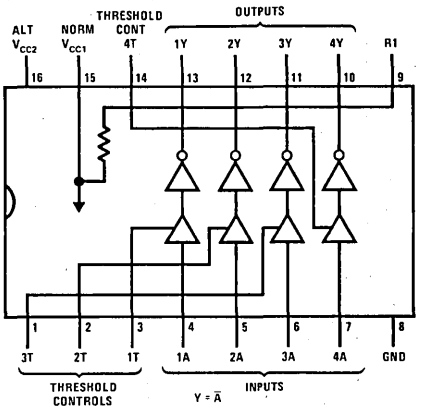
Output Voltage vs Input Voltage



TL/F/5795–10

Connection Diagram

Dual-In-Line Package

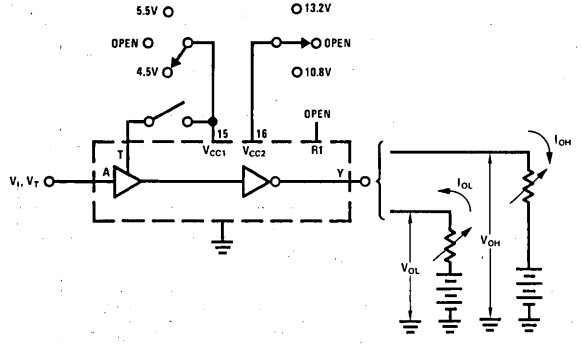


TL/F/5795–2

Top View

Order Number DS75154M or DS75154N
See NS Package Number M16A or N16A

DC Test Circuits and Truth Tables



TL/F/5795–3

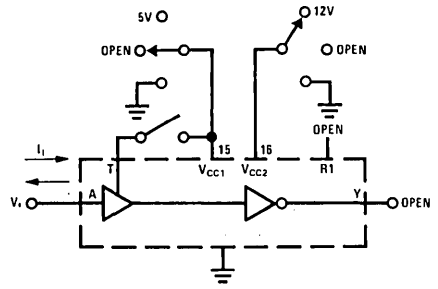
Test	Measure	A	T	Y	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open-Circuit Input (Fail-Safe)	V_{OH} V_{OH}	Open Open	Open Open	I_{OH} I_{OH}	4.5V Open	Open 10.8V
V_{T+} min, V_{T-} (Fail-Safe)	V_{OH} V_{OH}	0.8V 0.8V	Open Open	I_{OH} I_{OH}	5.5V Open	Open 13.2V
V_{T+} min (Normal)	V_{OH} V_{OH}	(Note 1) (Note 1)	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IL} max, V_{T-} min (Normal)	V_{OH} V_{OH}	−3V −3V	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IH} min, V_{T+} max, V_{T-} max (Fail-Safe)	V_{OL} V_{OL}	3V 3V	Open Open	I_{OL} I_{OL}	4.5V Open	Open 10.8V
V_{IH} min, V_{T+} max, (Normal)	V_{OL} V_{OL}	3V 3V	Pin 15 Pin 15	I_{OL} I_{OL}	4.5V and T T	Open 10.8V
V_{T-} max (Normal)	V_{OL} V_{OL}	(Note 2) (Note 2)	Pin 15 Pin 15	I_{OL} I_{OL}	5.5V and T T	Open 13.2V

Note 1: Momentarily apply −5V, then 0.8V.

Note 2: Momentarily apply 5V, then ground.

FIGURE 1. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}

DC Test Circuits and Truth Tables (Continued)

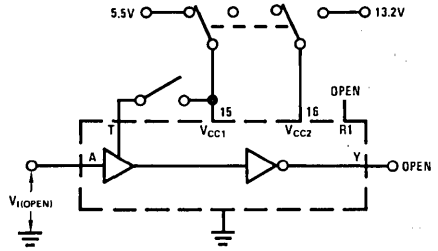


$r_I = \frac{\Delta V_I}{\Delta I_I}$

TL/F/5795–4

T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5V	Open
Open	Gnd	Open
Open	Open	Open
Pin 15	T and 5V	Open
Gnd	Gnd	Open
Open	Open	12V
Open	Open	Gnd
Pin 15	T	12V
Pin 15	T	Gnd
Pin 15	T	Open

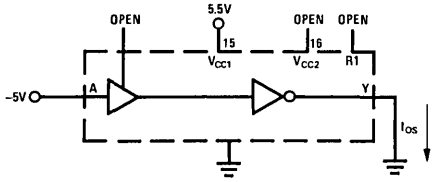
FIGURE 2. r_I



TL/F/5795–5

T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5.5V	Open
Pin 15	5.5V	Open
Open	Open	13.2V
Pin 15	T	13.2V

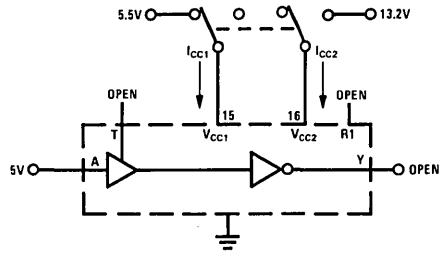
FIGURE 3. $V_{I(OPEN)}$



TL/F/5795–6

Each output is tested separately.

FIGURE 4. I_{OS}

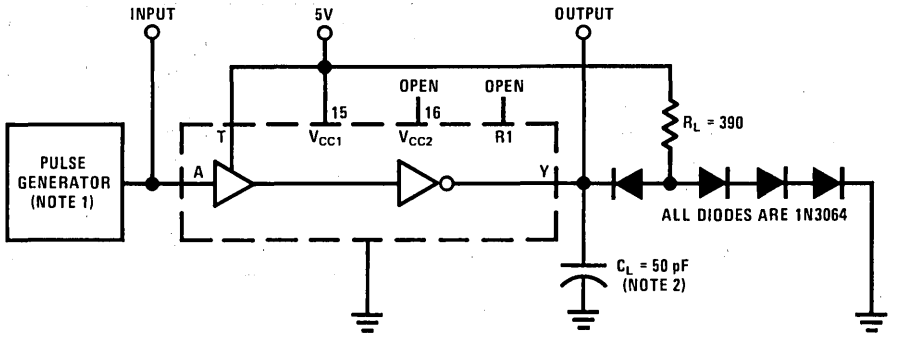


TL/F/5795–7

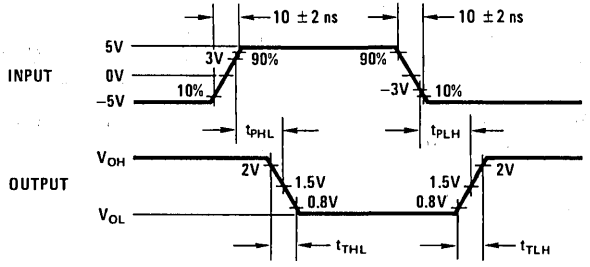
All four line receivers are tested simultaneously.

FIGURE 5. I_{CC}

AC Test Circuit and Switching Time Waveforms



TL/F/5795–8



TL/F/5795–9

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, $t_W = 200$ ns, duty cycle $\leq$ 20%.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6

National Semiconductor

DS9616H
Triple Line Driver

General Description

The DS9616H is a triple line driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24 and/or MIL-STD-188C. Each driver converts TTL/DTL logic levels to EIA/CCIT and/or MIL-STD-188C logic levels for transmission between data terminal equipment and data communications equipment. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH on the inhibit terminal interrupts signal transfer and forces the output to a V_{OL} (EIA/CCITT MARK) state.

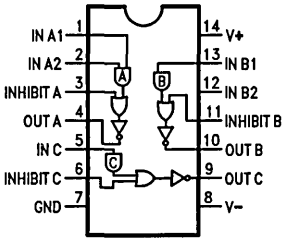
For the complementary function, see the DS9627MJ Dual EIA RS-232-C and MIL-STD-188C Line Receiver.

Features

- Internal slew rate limiting
- Meets EIA RS-232-C and CCITT V.24 and/or MIL-STD-188C
- Logic true inhibit function
- Output short circuit current-limiting
- Output voltage levels independent of supply voltages

Connection Diagrams

14-Lead DIP

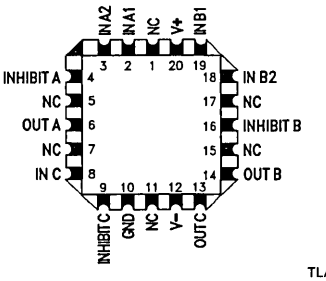


TL/F/10815–1

Top View

Order Number DS9616HMJ/883
See NS Package Number J14A

20-Terminal LCC



TL/F/10815–2

Top View

Order Number DS9616HME/883
See NS Package Number E20A

For Complete Military 883 Specifications, see RETS Data Sheet.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 4) DIP and CCP	400 mW
Supply Voltage	±15V
Input or Inhibit Voltage	−1.5V to +6.0V
Output Signal Voltage	±15V

Note 1: V_{IH} and V_{IL} are guaranteed by the V_{OH} and V_{OL} tests.

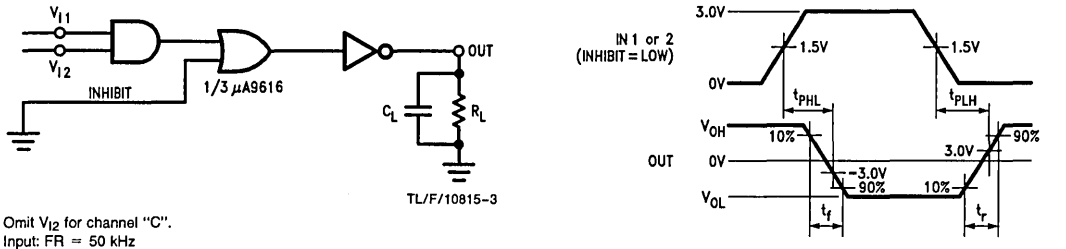
Note 2: All input and supply leads are grounded.

Note 3: An external capacitor may be needed to meet signal wave shaping requirements of MIL-STD-188C at the applicable modulation rate. No external capacitor is needed to meet RS-232-C.

Note 4: Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

DS9616HM
Electrical Characteristics $\pm 10.8V \leq V_{CC} \leq \pm 13.2V$, $R_L = 3.0\ k\Omega$, unless otherwise specified

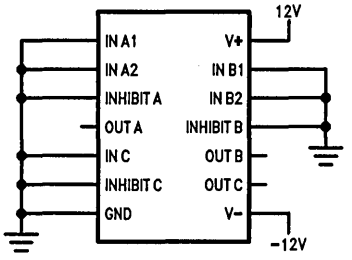
Symbol	Characteristic	Condition	Min	Max	Unit
V_{OH}	Output Voltage HIGH	V_{I1} and/or $V_{I2} = V_{INHIBIT} = 0.8V$	5.0	7.0	V
V_{OL}	Output Voltage LOW	$V_{I1} = V_{I2} = V_{INHIBIT} = 2.0V$	−7.0	−5.0	V
V_{OH} to V_{OL}	Output Voltage HIGH to Output Voltage LOW Magnitude Matching Error			±10	%
$I_{OS}+$	Positive Output Short Circuit Current	$R_L = 0\Omega$, V_{I1} and/or $V_{I2} = V_{INHIBIT} = 0.8V$	−45	−12	mA
$I_{OS}-$	Negative Output Short Circuit Current	$R_L = 0\Omega$, $V_{I1} = V_{I2} = V_{INHIBIT} = 2.0V$	12	60	mA
V_{IH}	Input Voltage HIGH (Note 1)		2.0		V
V_{IL}	Input Voltage LOW (Note 1)			0.8	V
I_{IH}	Input Current HIGH	$V_{I1} = V_{I2} = 2.4V$		40	μA
		$V_{I1} = V_{I2} = 5.5V$		1.0	mA
I_{IL}	Input Current LOW	$V_{I1} = V_{I2} = 0.4V$	−1.6		mA
$I+$	Positive Supply Current	$V_{I1} = V_{I2} = V_{INHIBIT} = 0.8V$		25	mA
		$V_{I1} = V_{I2} = V_{INHIBIT} = 2.0V$		15	mA
$I-$	Negative Supply Current	$V_{I1} = V_{I2} = V_{INHIBIT} = 0.8V$	−1.0		mA
		$V_{I1} = V_{I2} = V_{INHIBIT} = 2.0V$	−25		mA
R_O	Output Resistance, Power Off (Note 2)	$-2.0V \leq V_O \leq 0.5V$	300		Ω
SR+	Positive Slew Rate (Note 3)	$C_L = 2500\ pF$, $R_L = 3.0\ k\Omega$ (See *Figure 1*)	4.0	30	V/μs
			4.0	30	V/μs
SR−	Negative Slew Rate (Note 3)	$C_L = 2500\ pF$, $R_L = 3.0\ k\Omega$ (See *Figure 1*)	−30	−4.0	V/μs
			−30	−4.0	V/μs



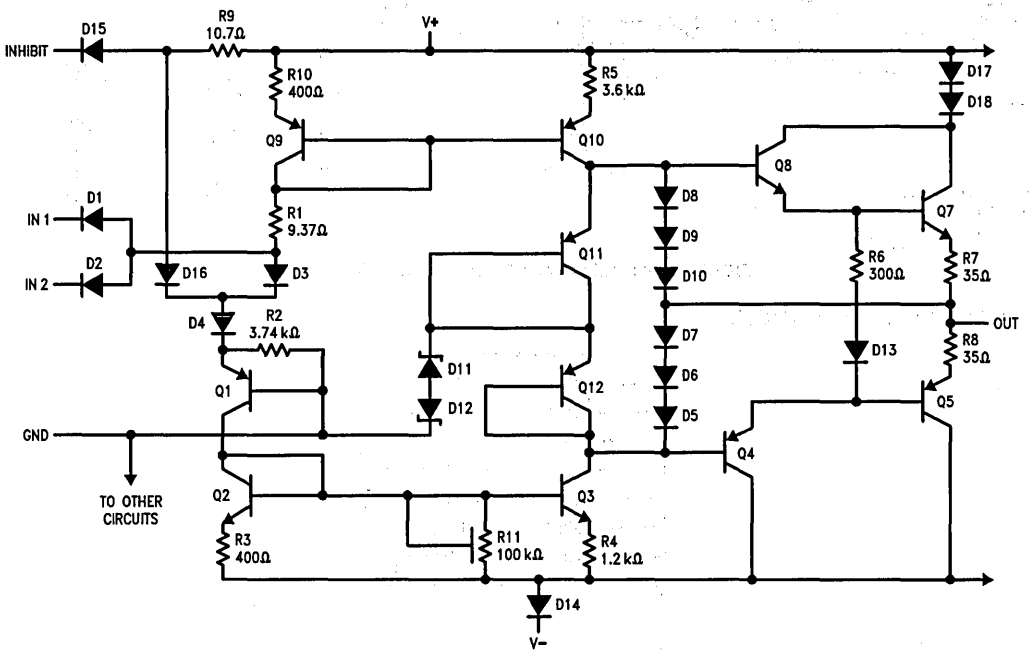
Omit V_{I2} for channel "C".
Input: FR = 50 kHz
Pulse Width = 10 μs
$t_r = t_f = 10 \pm 5.0$ ns

FIGURE 1. Switching Time Test Circuit and Waveforms

Primary Burn-In Circuit



Equivalent Circuit (⅓ of circuit)



TL/F/10815–6

National Semiconductor

DS9627 Dual Line Receiver

General Description

The DS9627 is a dual-line receiver which meets the electrical interface specifications of EIA RS-232C and MIL-STD-188C. The input circuitry accommodates ±25V input signals and the differential inputs allow user selection of either inverting or non-inverting logic for the receiver operation. The DS9627 provides both a selectable hysteresis range and selectable receiver input resistance. When pin 1 is tied to V^-, the typical switching points are at 2.6V and −2.6V, thus meeting RS-232-C requirements. When pin 1 is open, the typical switching points are at 50 μA and −50 μA, thus satisfying the requirements of MIL-STD-188C LOW level interface. Connecting the RA and/or RB pins to the (−) input yields an input impedance in the range of 3 kΩ to 7 kΩ and satisfies RS-232-C requirements; leaving RA and/or RB pins unconnected, the input resistance will be greater than 6 kΩ to satisfy MIL-STD-188C.

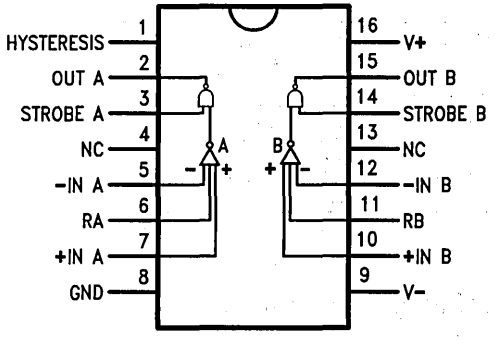
The output circuitry is TTL/DTL compatible and will allow "collector-dotting" to generate the wired-OR function. A TTL/DTL strobe is also provided for each receiver.

Features

- EIA RS-232-C input standards
- MIL-STD-188C input standards
- Variable hysteresis control
- High common mode rejection
- R control (5 kΩ or 10 kΩ)
- Wired-OR capability
- Choice of inverting and non-inverting inputs
- Outputs and strobe TTL compatible

Connection Diagram

16-Lead DIP



TL/F/9761–1

Top View

Order Number DS9627MJ/883
See NS Package Number J16A

For Complete Military 883 Specifications, see RETS Data Sheet.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Internal Power Dissipation (Note 5)	400 mW
V^+ to GND	0V to +15V
V^- to GND	0V to −15V
Input Voltage Referred to GND	±25V
Strobe to GND	−0.5V to +5.5V
Applied Output Voltage	−0.5V to +15V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)	−55	+125	°C

Electrical Characteristics

Hysteresis, −IN A, −IN B, RA and RB Open for MIL-STD-188C, unless otherwise specified (Notes 2 and 3)

Symbol	Characteristics	Conditions		Min	Max	Units
V_{OL}	Output Voltage LOW	$V^+ = 10.8V, V^- = -13.2V,$ $V_I^+ = 0.6V, I_{OL} = 6.4$ mA			0.4	V
V_{OH}	Output Voltage HIGH	$V^+ = 10.8V, V^- = -13.2V,$ $V_I^+ = 0.6V, I_{OH} = -0.5$ mA		2.4		V
I_{OS}	Output Short Circuit Current (Note 4)	$V^+ = 13.2V, V^- = -10.8V,$ $V_I^+ = 0.6V, V_O = 0V$		−3.0		mA
$I_{IH}(ST)$	Input Current HIGH (Strobe)	$V^+ = 10.8V,$ $V^- = -13.2V, V_I^+ = 0.6V$	$V_{ST} = 2.4V$		40	μA
			$V_{ST} = 5.5V$		1.0	mA
R_I	Input Resistance	$V^+ = 13.2V, V^- = -13.2V,$ $-3.0V \le V_I^+ \le 3.0V$		6.0		kΩ
I_{TH}^+	Positive Threshold Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V,$ $V_O = 2.4V$			100	μA
I_{TH}^-	Negative Threshold Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V,$ $V_O = 0.4V$		−100		μA
$V_{IL}(ST)$	Input Voltage LOW (Strobe)	$V_I^+ = -0.6V$			0.8	V
$V_{IH}(ST)$	Input Voltage HIGH (Strobe)	$V^+ = 13.2V, V^- = -10.8V,$ $V_I^+ = -0.6V$		2.0		V
I^+	Positive Supply Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V$ $V_I^+ = -0.6V$			18	mA
I^-	Negative Supply Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V$ $V_I^+ = 0.6V$		−16		mA

Electrical Characteristics

+IN A and −IN B connected to ground, RA and RB connected to −IN A and −IN B and Hysteresis connected to V^- for RS-232C, unless otherwise specified

Symbol	Characteristics	Conditions	Min	Max	Units
R_I	Input Resistance	$3.0V \le V_I \le 25V$	3.0	7.0	kΩ
		$-3.0V \le V_I \le -25V$	3.0	7.0	kΩ
V_I	Input Voltage		−2.0	2.0	V
V_{TH+}	Positive Threshold Voltage			3.0	V
V_{TH-}	Negative Threshold Voltage		−3.0		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range.

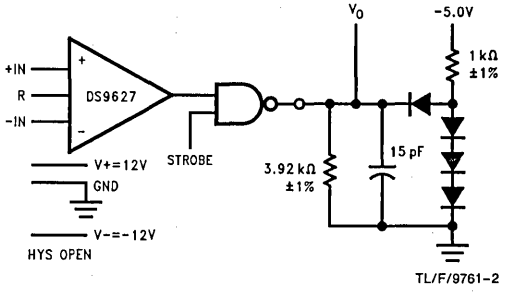
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

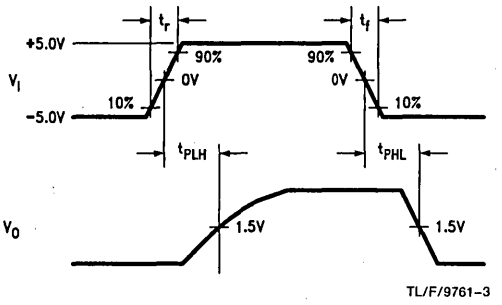
Note 5: Rating applies to ambient temperatures up to +125°C. Above 125°C ambient, derate linearity at 120°C/W.

Electrical Characteristics $V_{CC} = \pm 12V$ for MIL-STD-188C and RS-232C, $T_A = 25°C$

Symbol	Characteristics	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay to High Level	(See *Figure 1*)		250	ns
t_{PHL}	Propagation Delay to Low Level	(See *Figure 1*)		250	ns



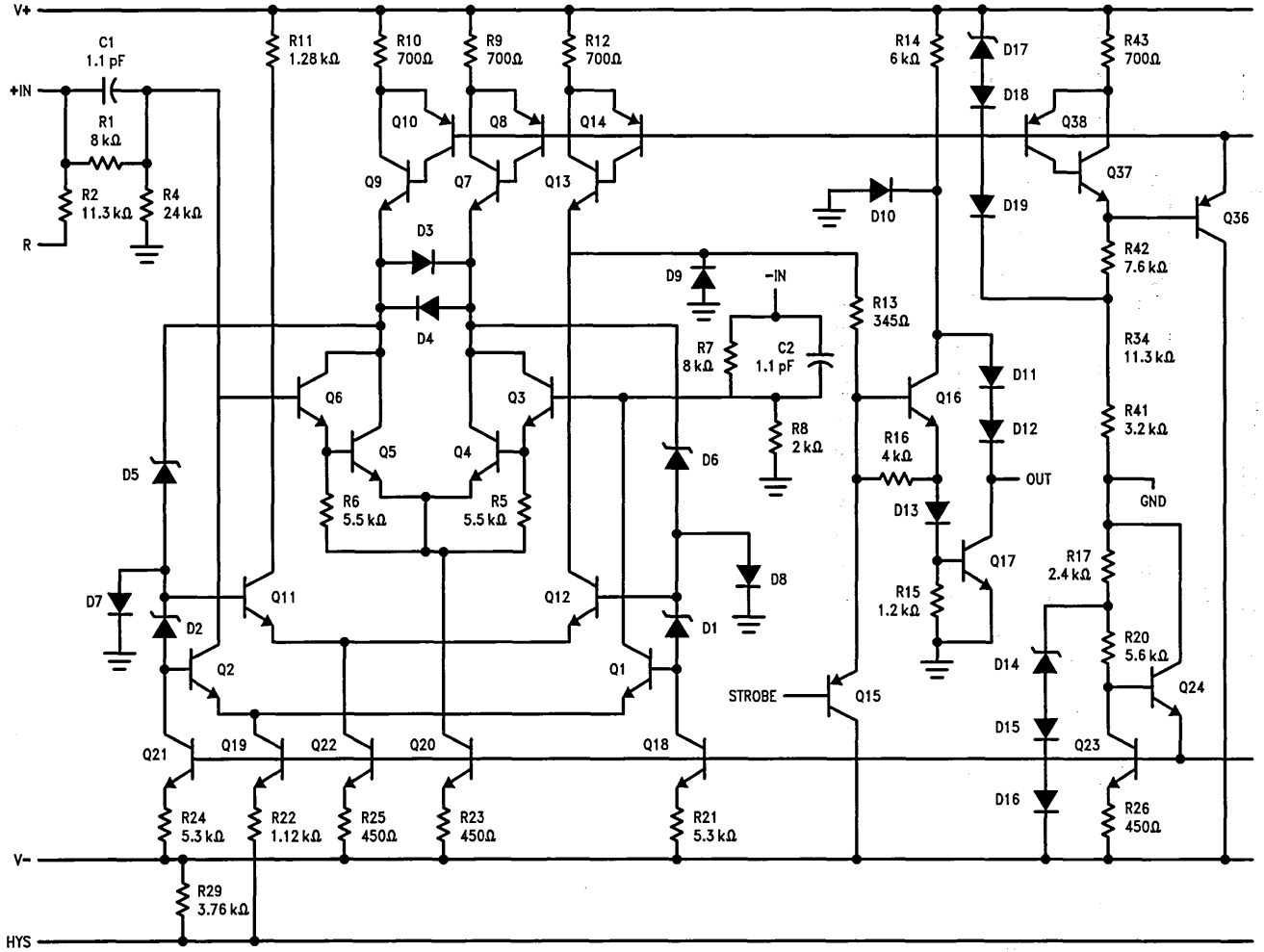
15 pF includes jig capacitance. All diodes are FD777 or equivalent.



PRR = 10 kHz
PW = 50 μs
$t_r = t_f = 5$ ns

FIGURE 1. Switching Time Test Circuit and Waveforms

Equivalent Circuit (½ of Circuit)



TL/F/9761–4

Section 2

TIA/EIA-422 and 423

Section 2 Contents

National Semiconductor

DS1691A/DS3691 (RS-422/RS-423) Line Drivers with TRI-STATE® Outputs

General Description

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the requirements of EIA standards RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 single-ended line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to slow the rise time for suppression of near end crosstalk to other receivers in the cable. Rise time capacitors are primarily intended for waveshaping output signals in the single-ended driver mode. Multipoint applications in differential mode with waveshaping capacitors is not allowed.

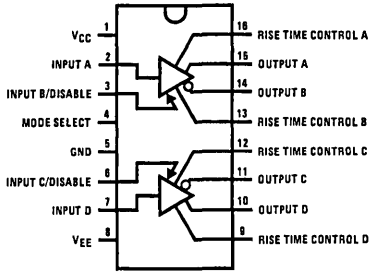
With the mode select pin low, the DS1691A/DS3691 are dual-differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE mode and 0V output unbalance when operated with ±5V supply.

Features

- Dual RS-422 line driver with mode pin low, or quad RS-423 line driver with mode pin high
- TRI-STATE outputs in RS-422 mode
- Short circuit protection for both source and sink outputs
- Outputs will not clamp line with power off or in TRI-STATE
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption
  - RS-422 I_{CC} = 9 mA/driver typ
  - RS-423 I_{CC} = 4.5 mA/driver typ
  - I_{EE} = 2.5 mA/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Pin compatible with AM26LS30

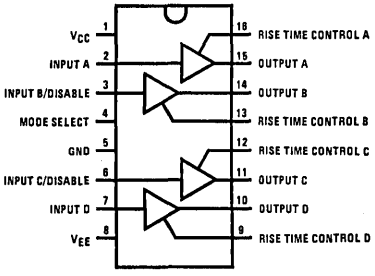
Connection Diagrams

With Mode Select LOW (RS-422 Connection)



Top View TL/F/5783–1

With Mode Select HIGH (RS-423 Connection)

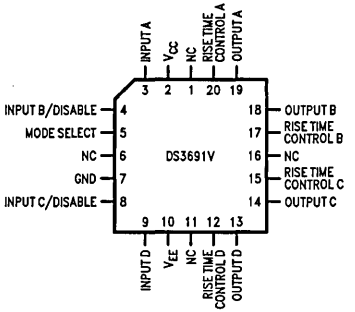


Top View TL/F/5783–2

Truth Table

Operation	Inputs			Outputs	
	Mode	A (D)	B (C)	A (D)	B (C)
RS-422	0	0	0	0	1
	0	0	1	TRI-STATE	TRI-STATE
	0	1	0	1	0
	0	1	1	TRI-STATE	TRI-STATE
RS-423	1	0	0	0	0
	1	0	1	0	1
	1	1	0	1	0
	1	1	1	1	1

Order Number DS1691AJ, DS3691J, DS3691M, DS3691N or DS3691V
See NS Package Number J16A, M16A, N16A or V20A
For Complete Military 883 Specifications, see RETS Data Sheet
Order Number DS1691AJ/883
See NS Package Number J16A



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to + 150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1691A			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3691			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1691A	−55	+125	°C
DS3691	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-422 CONNECTION, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	μA
		V_{IN} ≤ 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Differential Output Voltage $V_{A,B}$	R_L = ∞	V_{IN} = 2V		3.6	6.0	V
$\overline{V_O}$			V_{IN} = 0.8V		−3.6	−6.0	V
V_T	Differential Output Voltage $V_{A,B}$	R_L = 100Ω, V_{CC} ≥ 4.75V	V_{IN} = 2V	2	2.4		V
$\overline{V_T}$			V_{IN} = 0.8V	−2	−2.4		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	R_L = 100Ω, V_{CC} ≥ 4.75V		4.0	4.8		V
V_{CMR}	Output Voltage Common-Mode Range	$V_{DISABLE}$ = 2.4V		±10			V
I_{XA}	Output Leakage Current Power OFF	V_{CC} = 0V	V_{CMR} = 10V			100	μA
I_{XB}			V_{CMR} = −10V			−100	μA
I_{OX}	TRI-STATE Output Current	V_{CC} = Max, V_{EE} = 0V and −5V	V_{CMR} ≤ 10V			100	μA
			V_{CMR} ≥ −10V			−100	μA
I_{SA}	Output Short Circuit Current	V_{IN} = 0.4V	V_{OA} = 6V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA

AC Electrical Characteristics T_A = 25°C (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-422 CONNECTION, V_{CC} = 5V, MODE SELECT = 0.8V						
t_r	Output Rise Time	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_f	Output Fall Time	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		250	350	ns
t_{PZH}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		180	300	ns
t_{PLZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		180	300	ns
t_{PHZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		250	350	ns

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-423 CONNECTION, $\|V_{CC}\| = \|V_{EE}\|$, MODE SELECT ≥ 2V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	μA
		V_{IN} ≤ 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Output Voltage	R_L = ∞, (Note 6) V_{CC} ≥ 4.75V	V_{IN} = 2V	4.0	4.4	6.0	V
$\overline{V_O}$			V_{IN} = 0.4V	−4.0	−4.4	−6.0	V
V_T	Output Voltage	R_L = 450Ω V_{CC} ≥ 4.75V	V_{IN} = 2.4V	3.6	4.1		V
$\overline{V_T}$			V_{IN} = 0.4V	−3.6	−4.1		V
$\|V_T\| - \|\overline{V_T}\|$	Output Unbalance	$\|V_{CC}\| = \|V_{EE}\|$ = 4.75V, R_L = 450Ω			0.02	0.4	V
I_X^+	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = 6V		2	100	μA
I_X^-	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = −6V		−2	−100	μA
I_S^+	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
I_S^-	Output Short Circuit Current	V_O = 0V	V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, R_L = ∞			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, R_L = ∞			−10	−22	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1691A and across the 0°C to +70°C range for the DS3691. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

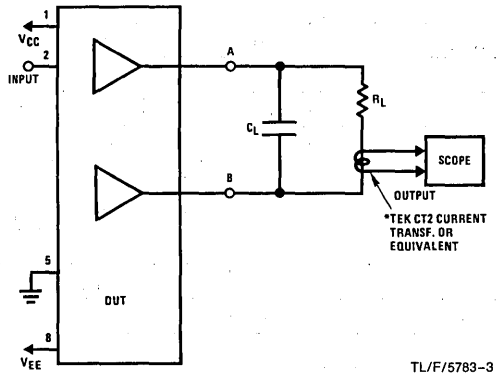
Note 5: Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

Note 6: At −55°C, the output voltage is +3.9V minimum and −3.9V minimum.

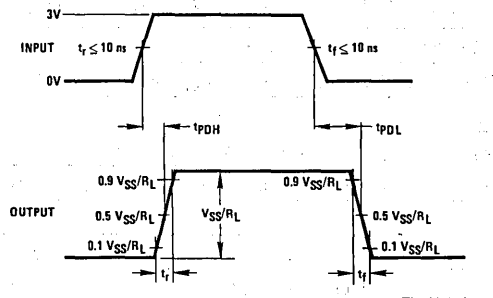
AC Electrical Characteristics T_A = 25°C (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-423 CONNECTION, V_{CC} = 5V, V_{EE} −5V, MODE SELECT = 2.4V						
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		μs
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		μs
t_{rc}	Rise Time Coefficient	R_L = 450Ω, C_L = 500 pF, C_C = 50 pF *(Figure 3)*		0.06		μs/pF
t_{PDH}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns
t_{PDL}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns

AC Test Circuits and Switching Time Waveforms

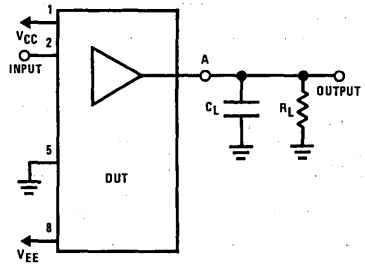


TL/F/5783–3

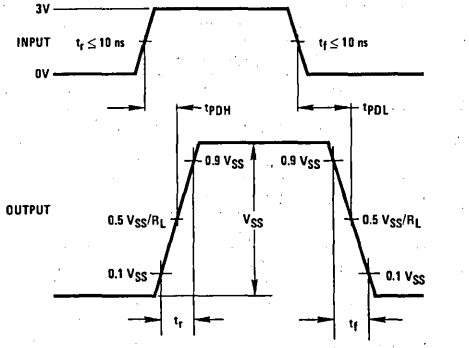


TL/F/5783–4

FIGURE 1. Differential Connection



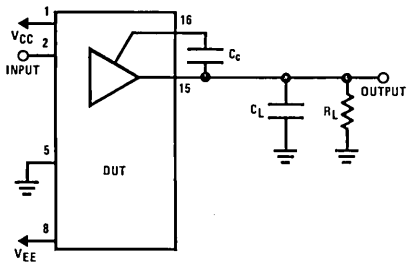
TL/F/5783–5



TL/F/5783–6

FIGURE 2. RS-423 Connection

AC Test Circuits and Switching Time Waveforms (Continued)



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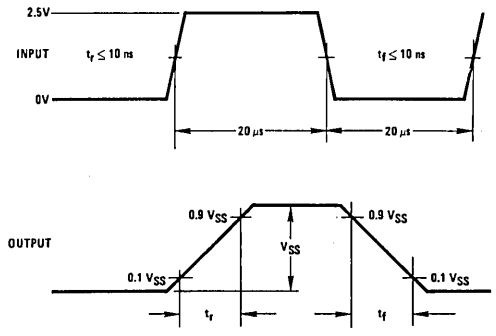

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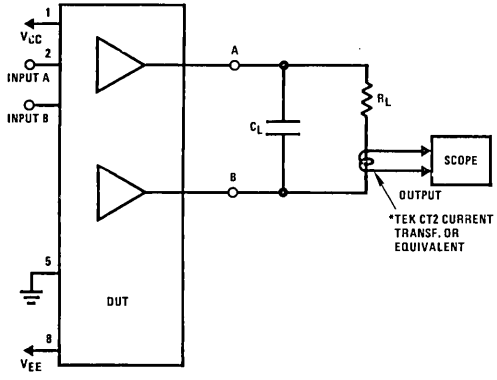
FIGURE 3. Rise Time Control for RS-423



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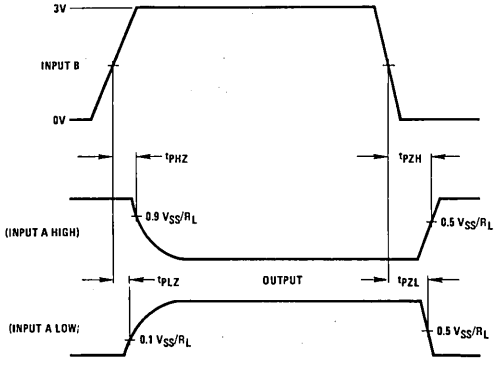

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FIGURE 4. TRI-STATE Delays

Switching Waveforms

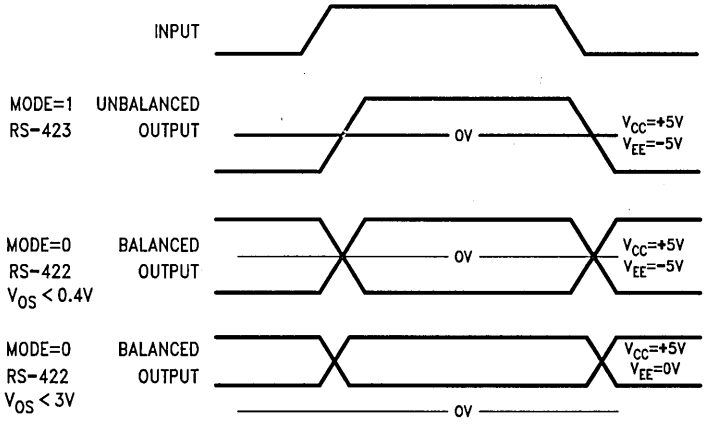

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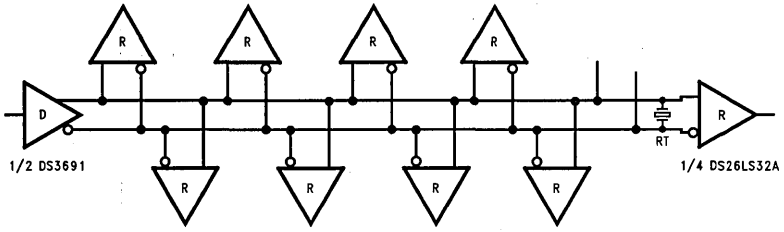
FIGURE 5. Typical Output Voltage

Typical Application Information

Fully Loaded RS-422 Interface



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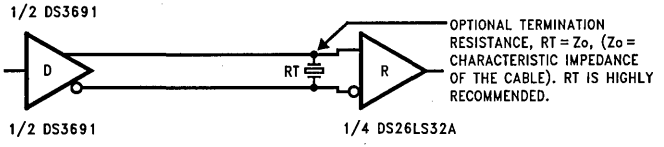
RS-422 Point to Point Application



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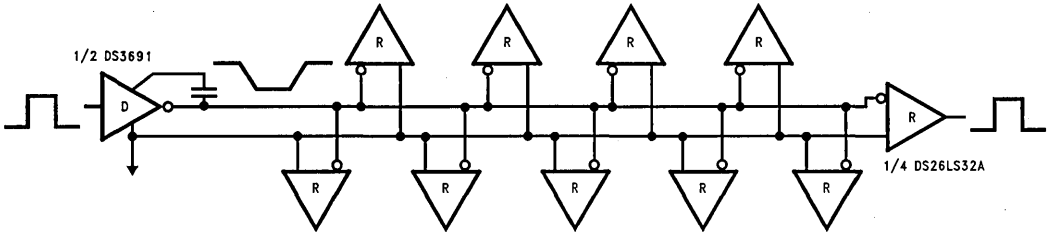
Fully Loaded RS-423 Interface



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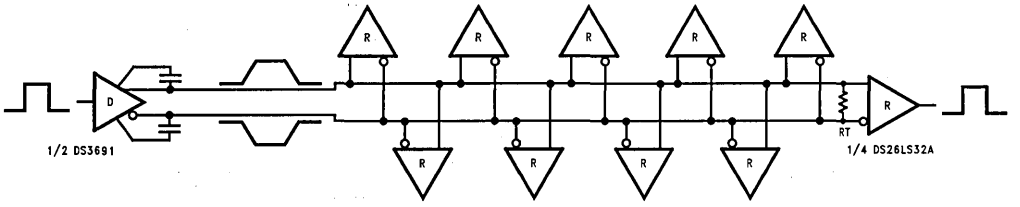
Differential Application with Rise Time Control



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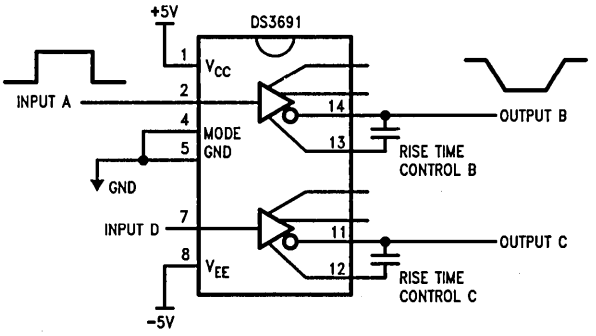
***Note:** Controlled edge allows longer stub lengths. Multiple Drivers are NOT allowed.

Typical Application Information (Continued)

Dual RS-423 Inverting Driver



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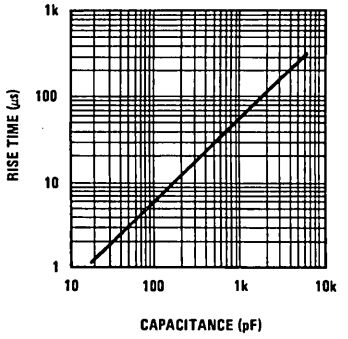
Typical Rise Time Control Characteristics (RS-423 Mode)

Rise Time vs External Capacitor



TL/F/5783–12

2

National Semiconductor

DS26C31T/DS26C31M
CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken (see Note 8). This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

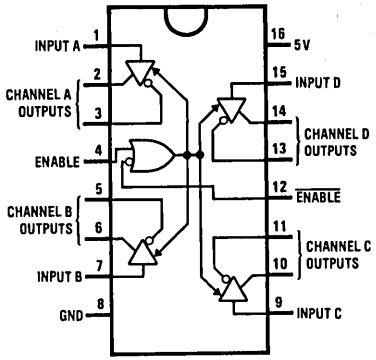
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs will not load line when V_{CC} = 0V
- DS26C31T meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount
- Mil-Std-883C compliant

Connection Diagrams

Dual-In-Line Package



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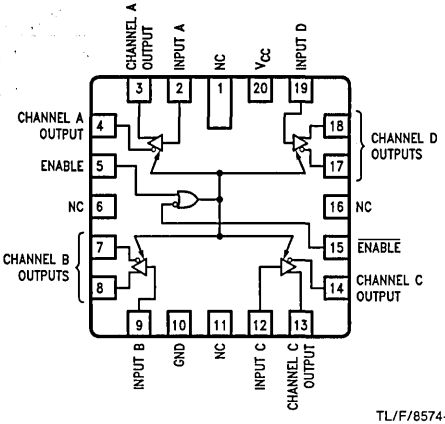
Top View

Order Number DS26C31TJ, DS26C31TM or DS26C31TN
See NS Package Number J16A, M16A or N16E

For Complete Military 883 Specifications, See RETS Data Sheet

Order Number DS26C31ME/883, DS26C31MJ/883 or DS26C31MW/883
See NS Package Number E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier (E)



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Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max. Power Dissipation (P_D) @25°C (Note 3)	
Ceramic "J" Pkg.	2419 mW
Plastic "N" Pkg.	1736 mW
SOIC "M" Pkg.	1226 mW
Ceramic "W" Pkg.	1182 mW
Ceramic "E" Pkg.	2134 mW
Lead Temperature (T_L) (Soldering, 4 sec.)	260°C

This device does not meet 2000V ESD Rating. (Note 13)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
DS26C31T	−40	+85	°C
DS26C31M	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA		2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 20 mA			0.3	0.5	V
V_T	Differential Output Voltage	R_L = 100Ω (Note 5)		2.0	3.1		V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference In Differential Output	R_L = 100Ω (Note 5)				0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100Ω (Note 5)			1.8	3.0	V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$	Difference In Common Mode Output	R_L = 100Ω (Note 5)				0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}				±1.0	μA
I_{CC}	Quiescent Supply Current (Note 6)	DS26C31T I_{OUT} = 0 μA	V_{IN} = V_{CC} or GND		200	500	μA
			V_{IN} = 2.4V or 0.5V (Note 6)		0.8	2.0	mA
		DS26C31M I_{OUT} = 0 μA	V_{IN} = V_{CC} or GND		200	500	μA
			V_{IN} = 2.4V or 0.5V (Note 6)		0.8	2.1	mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, ENABLE = V_{IL}, $\overline{\text{ENABLE}}$ = V_{IH}			±0.5	±5.0	μA

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{SC}	Output Short Circuit Current	V_{IN} = V_{CC} or GND (Notes 5, 7)		−30		−150	mA
I_{OFF}	Output Leakage Current Power Off (Note 5)	DS26C31T V_{CC} = 0V	V_{OUT} = 6V			100	μA
			V_{OUT} = −0.25V			−100	μA
		DS26C31M V_{CC} = 0V	V_{OUT} = 6V			100	μA
			V_{OUT} = 0V (Note 8)			−100	μA

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature derate N package at 13.89 mW/°C, J package 16.13 mW/°C, M package 9.80 mW/°C, E package 12.20 mW/°C, and W package 6.75 mW/°C.

Note 4: Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Note 8: The DS26C31M (−55°C to +125°C) is tested with V_{OUT} between +6V and 0V while RS-422A condition is +6V and −0.25V.

Switching Characteristics V_{CC} = 5V ±10%, t_r ≤ 6 ns, t_f ≤ 6 ns (*Figures 1, 2, 3* and *4*) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C31T	CS26C31M	
t_{PLH}, t_{PHL}	Propagation Delays Input to Output	S1 Open		6	11	14	ns
Skew	(Note 9)	S1 Open		0.5	2.0	3.0	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	14	ns
t_{PZH}	Output Enable Time	S1 Closed		11	19	22	ns
t_{PZL}	Output Enable Time	S1 Closed		13	21	28	ns
t_{PHZ}	Output Disable Time (Note 10)	S1 Closed		5	9	12	ns
t_{PLZ}	Output Disable Time (Note 10)	S1 Closed		7	11	14	ns
C_{PD}	Power Dissipation Capacitance (Note 11)			50			pF
C_{IN}	Input Capacitance			6			pF

Note 9: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 10: Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 11: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Comparison Table of Switching Characteristics into "LS-Type" Load

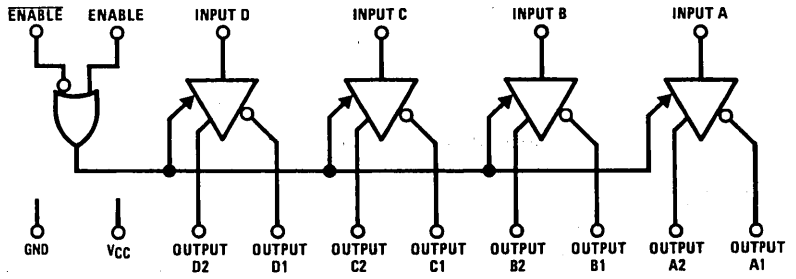
V_{CC} = 5V, T_A = 25°C, $t_r \leq 6$ ns, $t_f \leq 6$ ns (*Figures 2, 4, 5* and *6*) (Note 12)

Symbol	Parameter	Conditions	DS26C31T		DS26LS31C		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delays Input to Output	C_L = 30 pF S1 Closed S2 Closed	6	8	10	15	ns
Skew	(Note 9)	C_L = 30 pF S1 Closed S2 Closed	0.5	1.0	2.0	6.0	ns
t_{THL}, t_{TLH}	Differential Output Rise and Fall Times	C_L = 30 pF S1 Closed S2 Closed	4	6			ns
t_{PLZ}	Output Disable Time (Note 10)	C_L = 10 pF S1 Closed S2 Open	6	9	15	35	ns
t_{PHZ}	Output Disable Time (Note 10)	C_L = 10 pF S1 Open S2 Closed	4	7	15	25	ns
t_{PZL}	Output Enable Time	C_L = 30 pF S1 Closed S2 Open	14	20	20	30	ns
t_{PZH}	Output Enable Time	C_L = 30 pF S1 Open S2 Closed	11	17	20	30	ns

Note 12: This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or guaranteed.

Note 13: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥ 1500V
Outputs ≥ 1000V
EIAJ (0Ω, 200 pF) ≥ 350V

Logic Diagram



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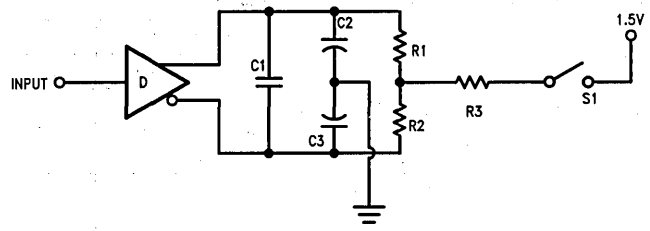
AC Test Circuit and Switching Time Waveforms



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Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

FIGURE 1. AC Test Circuit

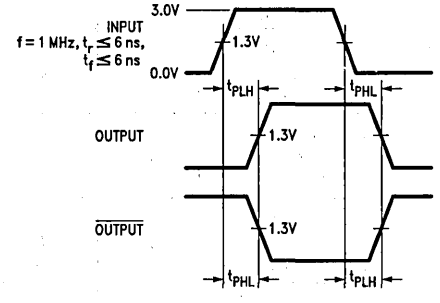

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FIGURE 2. Propagation Delays

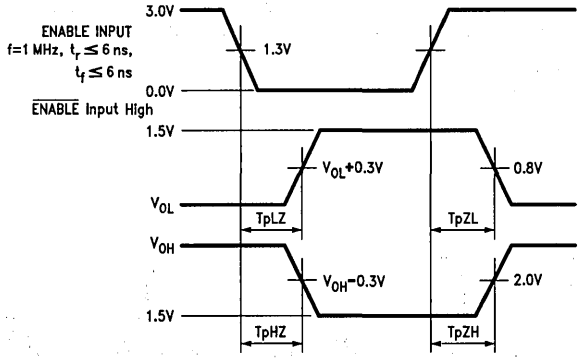

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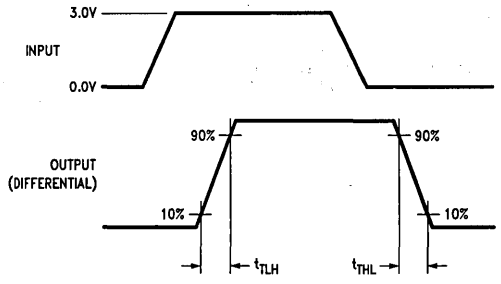
FIGURE 3. Enable and Disable Times



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Input pulse; f = 1 MHz, 50%; $t_r \leq 6$ ns, $t_f \leq 6$ ns

FIGURE 4. Differential Rise and Fall Times

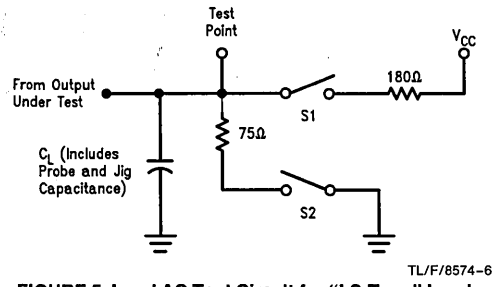

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FIGURE 5. Load AC Test Circuit for "LS-Type" Load

AC Test Circuit and Switching Time Waveforms (Continued)

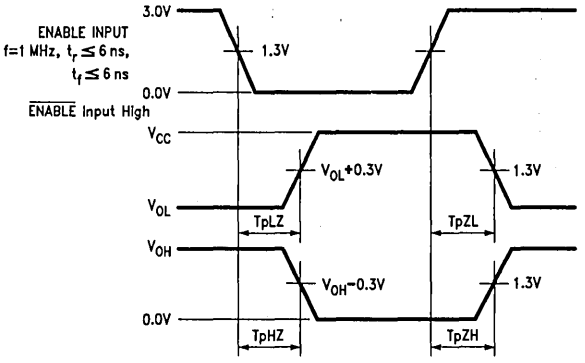

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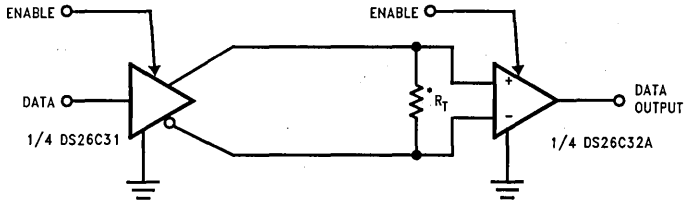
FIGURE 6. Enable and Disable Times for "LS-Type" Load

Typical Applications

Two-Wire Balanced System, RS-422



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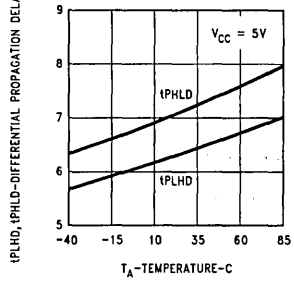
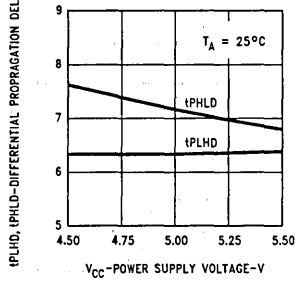
*R_T is optional although highly recommended to reduce reflection.

Typical Performance Characteristics

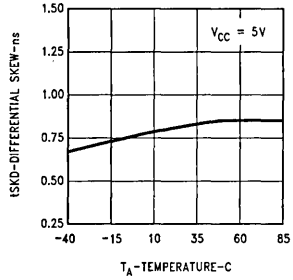
Differential Propagation Delay vs Temperature



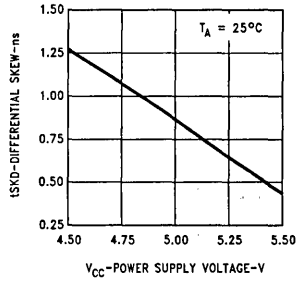
Differential Propagation Delay vs Power Supply Voltage



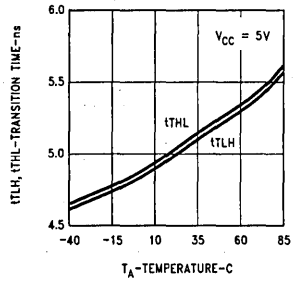
Differential Skew vs Temperature



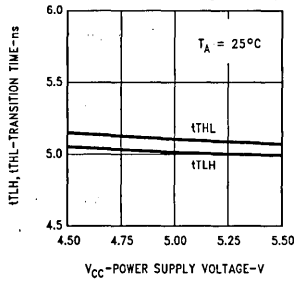
Differential Skew vs Power Supply Voltage



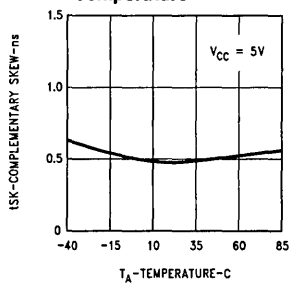
Differential Transition Time vs Temperature



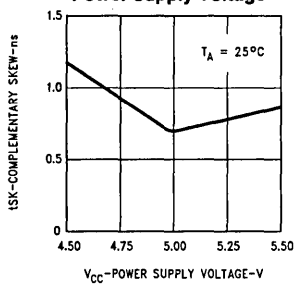
Differential Transition Time vs Power Supply Voltage



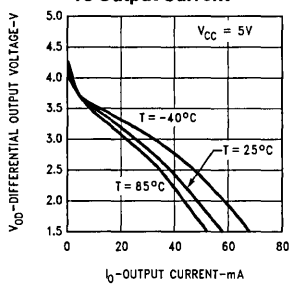
Complementary Skew vs Temperature



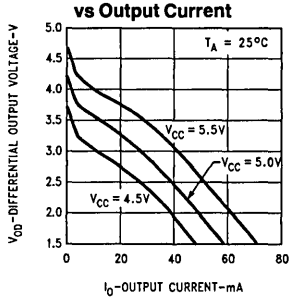
Complementary Skew vs Power Supply Voltage



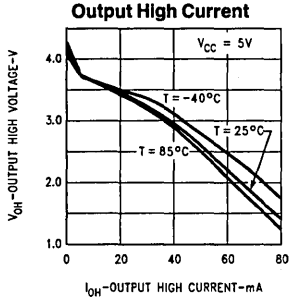
Differential Output Voltage vs Output Current



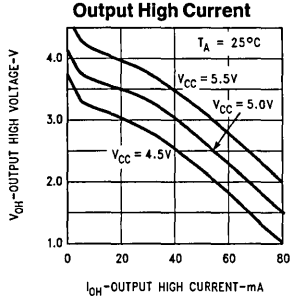
Differential Output Voltage vs Output Current



Output High Voltage vs Output High Current



Output High Voltage vs Output High Current



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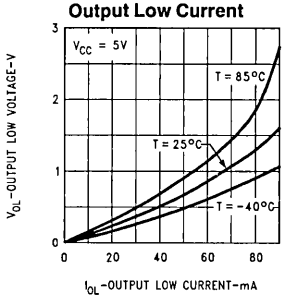
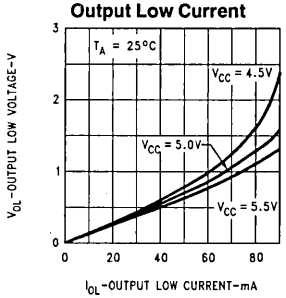
Typical Performance Characteristics (Continued)

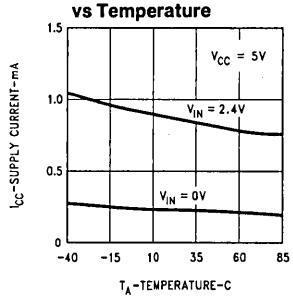
Output Low Voltage vs Output Low Current



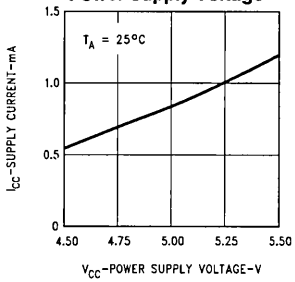
Output Low Voltage vs Output Low Current



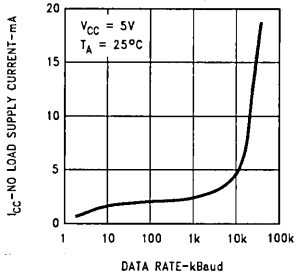
Supply Current vs Temperature



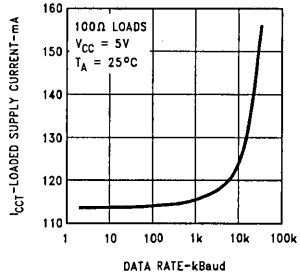
Supply Current vs Power Supply Voltage



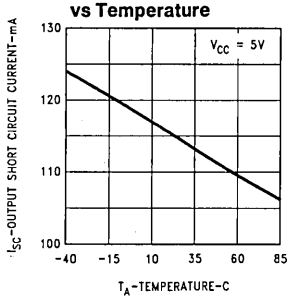
No Load Supply Current vs Data Rate



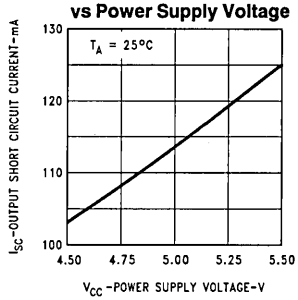
Loaded Supply Current vs Data Rate



Output Short Circuit Current vs Temperature



Output Short Circuit Current vs Power Supply Voltage



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2

National Semiconductor

DS26F31C/DS26F31M
Quad High Speed Differential Line Driver

General Description

The DS26F31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26F31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The DS26F31 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F31 features lower power, extended temperature range, and improved specifications.

The circuit provides an enable and disable function common to all four drivers. The DS26F31C/DS26F31M features TRI-STATE® outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

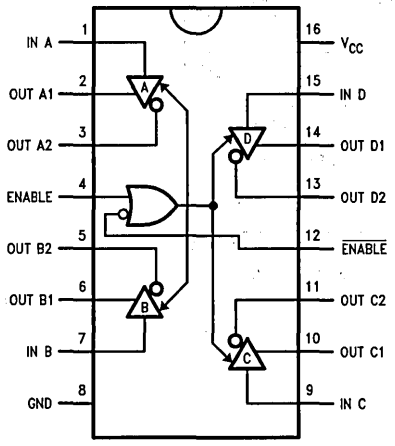
The DS26F31C/DS26F31M offers optimum performance when used with the DS26F32 Quad Differential Line Receiver.

Features

- Military temperature range
- Output skew—2.0 ns typical
- Input to output delay—10 ns
- Operation from single +5.0V supply
- 16-lead ceramic DIP Package
- Outputs won't load line when V_{CC} = 0V
- Output short circuit protection
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines

Connection and Logic Diagrams

16-Lead Dual-In-Line Package

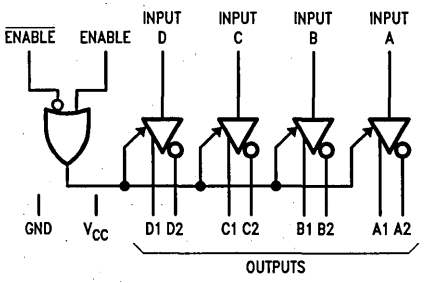


TL/F/9614-1

Top View

Order Number DS26F31CJ or DS26F31MJ
See NS Package Number J16A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS26F31ME/883, DS26F31MJ/883, or DS26F31MW/883
See NS Package Numbers E20A, J16A, or W16A



TL/F/9614-2

FIGURE 1. Logic Symbol

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Supply Voltage	7.0V
Input Voltage	7.0V
Output Voltage	5.5V

*Derate cavity package 10 mW/°C above 25°C.

Operating Range

DS26F31C	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS26F31M	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output Voltage HIGH	V_{CC} = Min, I_{OH} = −20 mA		2.5	3.2		V
V_{OL}	Output Voltage LOW	V_{CC} = Min, I_{OL} = 20 mA			0.32	0.5	V
V_{IH}	Input Voltage HIGH	V_{CC} = Min		2.0			V
V_{IL}	Input Voltage LOW	V_{CC} = Max				0.8	V
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4V			−0.10	−0.20	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.7V			0.5	20	μA
I_{IR}	Input Reverse Current	V_{CC} = Max, V_I = 7.0V			0.001	0.1	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.5V		0.5	20	μA
			V_O = 0.5V		0.5	−20	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−0.8	−1.5	V
I_{OS}	Output Short Circuit	V_{CC} = Max (Note 4)		−30	−60	−150	mA
I_{CCX}	Supply Current	V_{CC} = Max, All Outputs Disabled				50	mA
I_{CC}		V_{CC} = Max, All Outputs Enabled				40	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5, Note 6			10	15	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			10	15	ns
SKEW	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5, Note 6			2.0	4.5	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10 pF			23	32	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10 pF			15	25	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			20	30	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5			23	32	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS26F31M and across the 0°C to +70°C range for the DS26F31C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: C_L = 30 pF, V_I = 1.3V to V_O = 1.3V, V_{PULSE} = 0V to +3V (See AC Load Test Circuit for TRI-STATE Outputs).

Note 6: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Test Circuit and Timing Waveforms

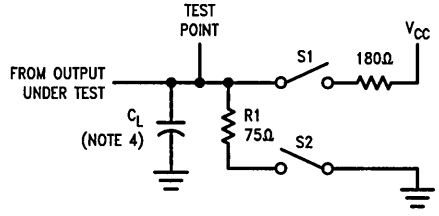


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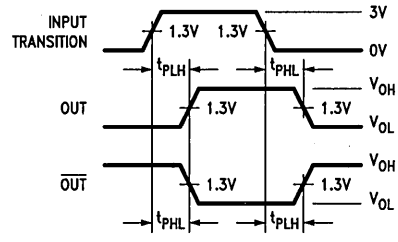
FIGURE 2. AC Load Test Circuit for TRI-STATE Outputs



TL/F/9614–4

FIGURE 3. Propagation Delay (Notes 1 and 3)

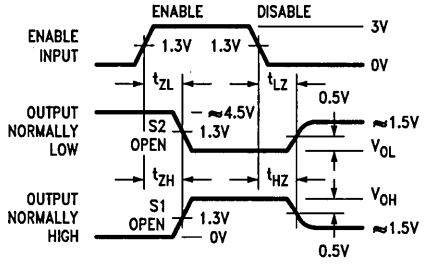


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FIGURE 4. Enable and Disable Times (Notes 2 and 3)

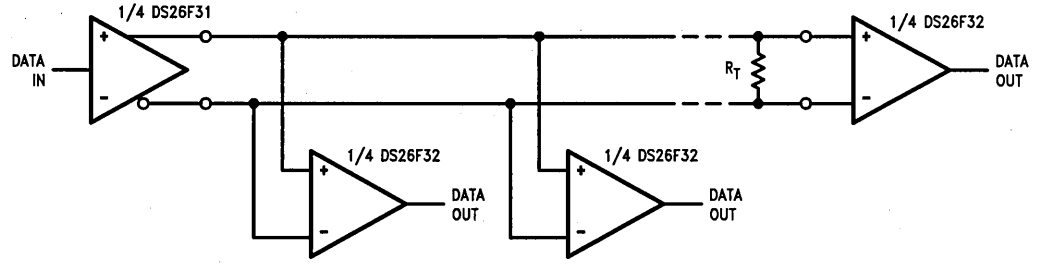
Note 1: Diagram shown for Enable Low. Switches S1 and S2 open.

Note 2: S1 and S2 of Load Circuit are closed except where shown.

Note 3: Pulse Generator for all Pulses: Rate ≤ 1.0 MHz, $Z_O = 50\Omega$, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns.

Note 4: C_L includes probe and jig capacitance.

Typical Application



TL/F/9614–6

FIGURE 5. Typical Application

National Semiconductor

DS26LS31C/DS26LS31M Quad High Speed Differential Line Driver

General Description

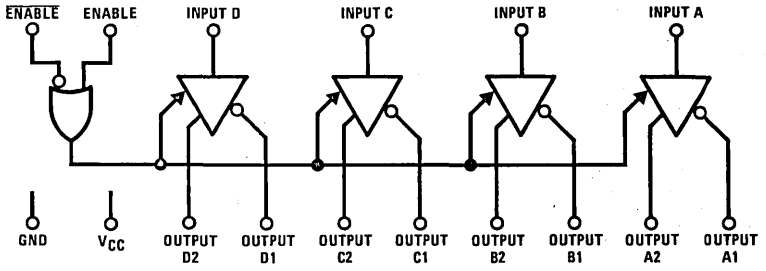
The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE® outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

Features

- Output skew—2.0 ns typical
- Input to output delay—10 ns typical
- Operation from single 5V supply
- Outputs won't load line when V_{CC} = 0V
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA Standard RS-422
- Pin compatible with AM26LS31
- Available in military and commercial temperature range

Logic and Connection Diagrams



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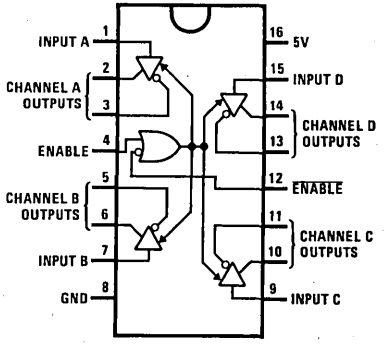
Dual-In-Line Package



TL/F/5778–2

Top View
Order Number DS26LS31CJ, DS26LS31CM, DS26LS31CN or DS26LS31MJ
See NS Package Number J16A, M16A or N16A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS26LS31MJ/883 or DS26LS31MW/883
See NS Package J16A or W16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5.5V
Output Voltage (Power OFF)	−0.25 to 6V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS26LS31M	4.5	5.5	V
DS26LS31	4.75	5.25	V
Temperature, T_A			
DS26LS31M	−55	+125	°C
DS26LS31	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = −20 mA	2.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4V		−40	−200	μA
I_{IH}	Input High Current	V_{IN} = 2.7V			20	μA
I_I	Input Reverse Current	V_{IN} = 7V			0.1	mA
I_O	TRI-STATE Output Current	V_O = 2.5V			20	μA
		V_O = 0.5V			−20	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.5	V
I_{SC}	Output Short-Circuit Current		−30		−150	mA
I_{CC}	Power Supply Current	All Outputs Disabled or Active		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Input to Output	C_L = 30 pF		10	15	ns
t_{PHL}	Input to Output	C_L = 30 pF		10	15	ns
Skew	Output to Output	C_L = 30 pF		2.0	6.0	ns
t_{LZ}	Enable to Output	C_L = 10 pF, S2 Open		15	35	ns
t_{HZ}	Enable to Output	C_L = 10 pF, S1 Open		15	25	ns
t_{ZL}	Enable to Output	C_L = 30 pF, S2 Open		20	30	ns
t_{ZH}	Enable to Output	C_L = 30 pF, S1 Open		20	30	ns

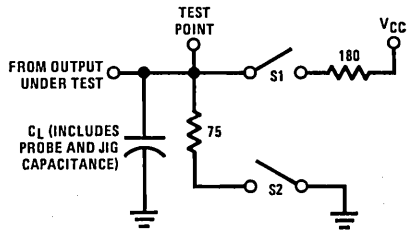
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS726LS31M and across the 0°C to +70°C range for the DS26LS31. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms



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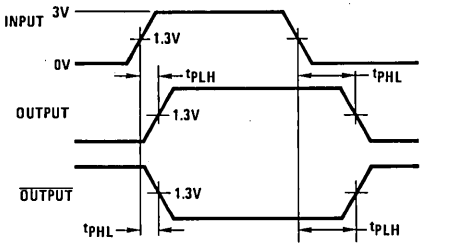
Note: S1 and S2 of load circuit are closed except where shown.

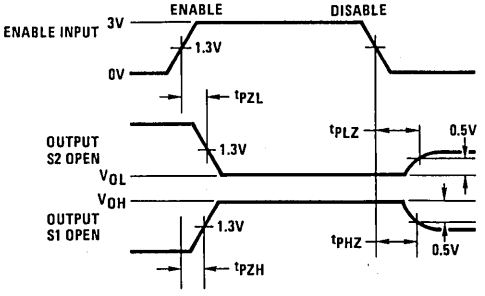
FIGURE 1. AC Test Circuit



TL/F/5778–4

f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

FIGURE 2. Propagation Delays



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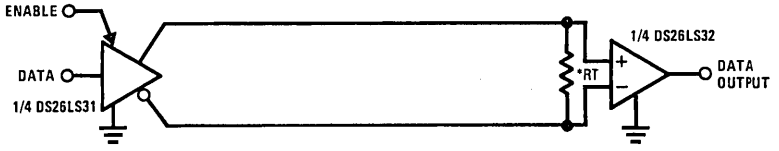
f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

FIGURE 3. Enable and Disable Times

Typical Applications

Two-Wire Balanced System, RS-422



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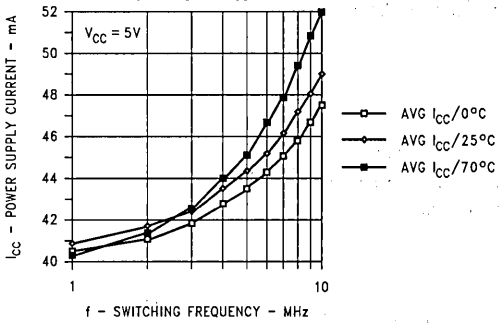
*R_T is optional although highly recommended to reduce reflection.

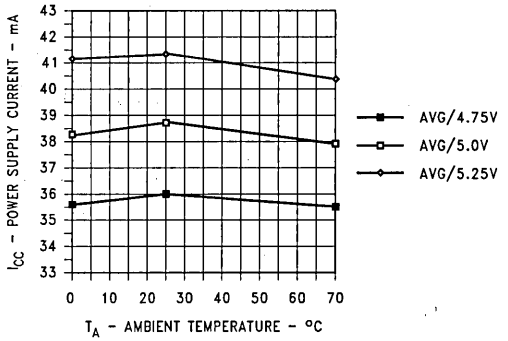
Typical Performance Characteristics

DS26LS31CN Unloaded I_C vs Frequency vs T_A



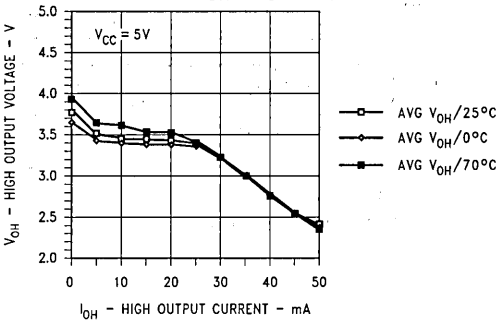
TL/F/5778–7

DS26LS31 I_{CC} vs V_{CC} vs T_A



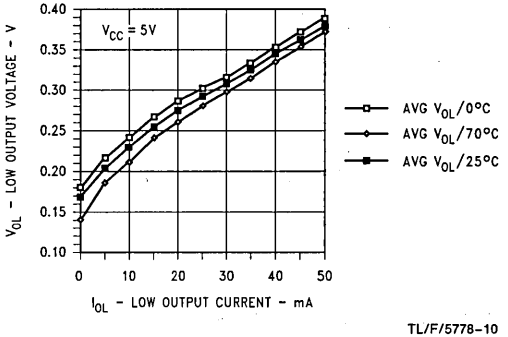
TL/F/5778–8

DS26LS31CN V_{OH} vs I_{OH} vs T_A



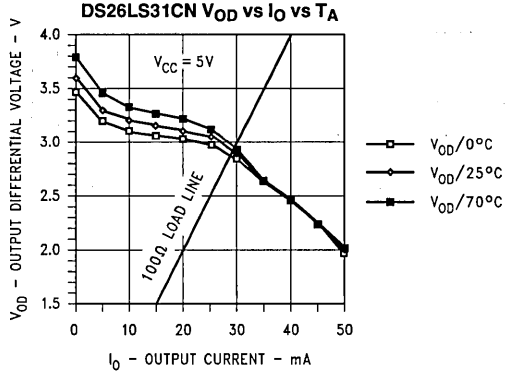
TL/F/5778–9

DS26LS31CN V_{OL} vs I_{OL} vs T_A



TL/F/5778–10

DS26LS31CN V_{OD} vs I_O vs T_A



TL/F/5778–11

National Semiconductor

DS26C32AT/DS26C32AM
Quad Differential Line Receiver

General Description

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

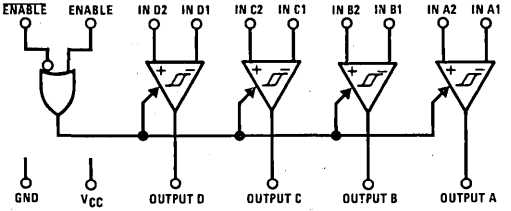
The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers, and features TRI-STATE® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

- CMOS design for low power
- ±0.2V sensitivity over input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses
- Available in Surface Mount
- Mil-Std-883C compliant

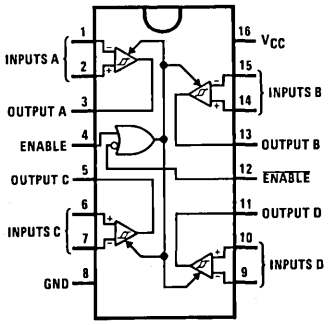
Logic Diagram



TL/F/8764–1

Connection Diagrams

Dual-In-Line Package



TL/F/8764–2

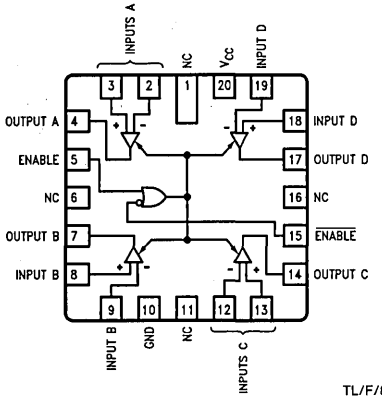
Top View

Order Number DS26C32ATJ, DS26C32ATM or DS26C32ATN
See NS Package J16A, M16A or N16E

For Complete Military 883 Specifications, See RETS Data Sheet.

Order Number DS26C32AME/883, DS26C32AMJ/883 or DS26C32AMW/883
See NS Package E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier



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Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq V_{TH}$ (Max)	H
		$V_{ID} \leq V_{TH}$ (Min)	L
		Open	H

Z = TRI-STATE

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Maximum Power Dissipation at 25°C (Note 5)	
Ceramic "J" Pkg.	2308 mW
Plastic "N" Pkg.	1645 mW
SOIC "M" Pkg.	1190 mW
Ceramic "E" Pkg.	2108 mW
Ceramic "W" Pkg.	1215 mW
Maximum Current Per Output	±25 mA

This device does not meet 2000V ESD rating. (Note 4)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)			
DS26C32AT	−40	+85	°C
DS26C32AM	−55	+125	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$		−200	35	+200	mV
R_{IN}	Input Resistance	V_{IN} = −7V, +7V (Other Input = GND)	DS26C32AT	5.0	6.8	10	kΩ
			DS26C32AM	4.5	6.8	11	kΩ
I_{IN}	Input Current	V_{IN} = +10V, Other Input = GND	DS26C32AT		+1.1	+1.5	mA
			DS26C32AM		+1.1	+1.8	mA
		V_{IN} = −10V, Other Input = GND	DS26C32AT		−2.0	−2.5	mA
			DS26C32AM		−2.0	−2.7	mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min, V_{DIFF} = +1V I_{OUT} = −6.0 mA		3.8	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max, V_{DIFF} = −1V I_{OUT} = 6.0 mA			0.2	0.3	V
V_{IH}	Minimum Enable High Input Level Voltage			2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage					0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, ENABLE = V_{IL}, $\overline{\text{ENABLE}}$ = V_{IH}			±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND				±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max, V_{DIF} = +1V	DS26C32AT		16	23	mA
			DS26C32AM		16	25	mA
V_{HYST}	Input Hysteresis	V_{CM} = 0V			60		mV

AC Electrical Characteristics V_{CC} = 5V ±10% (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C32AT	DS26C32AM	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		19	30	35	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		4	9	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	22	29	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	23	29	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply over recommended operating conditions. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥2000V
All other pins ≥1000V
EIAJ (0Ω, 200 pF) ≥350V

Note 5: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.16 mW/°C, J Package 15.38 mW/°C, M Package 9.52 mW/°C, E Package 12.04 mW/°C, and W package 6.94 mW/°C.

Comparison Table of Switching Characteristics into "LS-Type" Load

(*Figures 4, 5,* and *6*) (Note 6)

Symbol	Parameter	Conditions	DS26C32A	DS26LS32A	Units
			Typ	Typ	
t_{PLH}	Input to Output	C_L = 15 pF	17	23	ns
t_{PHL}			19	23	ns
t_{LZ}	ENABLE to Output	C_L = 5 pF	13	15	ns
t_{HZ}			12	20	ns
t_{ZL}	ENABLE to Output	C_L = 15 pF	13	14	ns
t_{ZH}			13	15	ns

Note 6: This table is provided for comparison purposes only. The values in this table for the DS26C32A reflect the performance of the device, but are not tested or guaranteed.

Test and Switching Waveforms

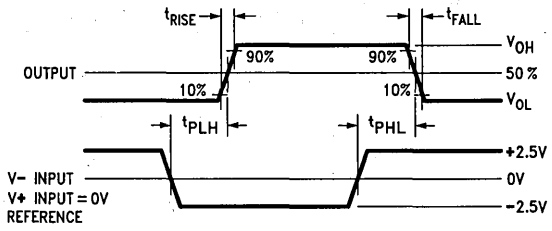

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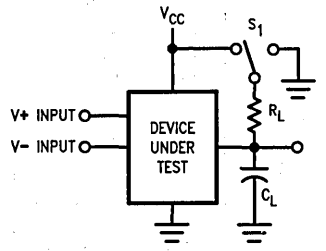
FIGURE 1. Propagation Delay



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C_L includes load and test jig capacitance.
S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S_1 = Gnd for t_{PZH} and t_{PHZ} measurements.

FIGURE 2. Test Circuit for TRI-STATE Output Tests

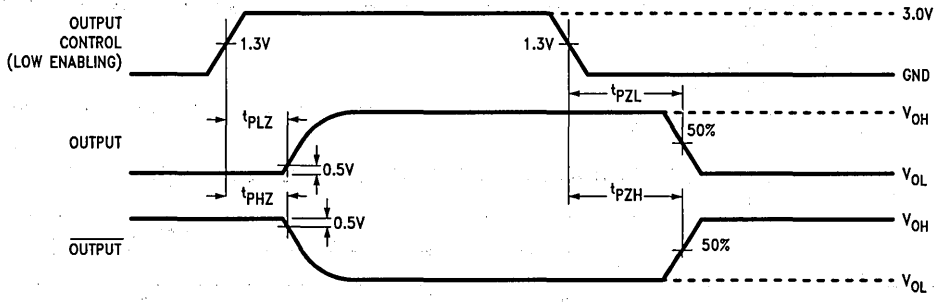

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FIGURE 3. TRI-STATE Output Enable and Disable Waveforms

AC Test Circuit and Switching Time Waveforms

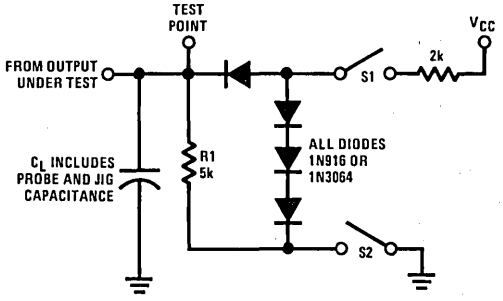

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FIGURE 4. Load Test Circuit for TRI-STATE Outputs for "LS-Type" Load

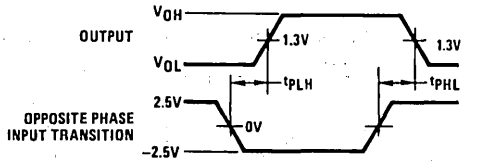

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FIGURE 5. Propagation Delay for "LS-Type" Load (Notes 7, 9)

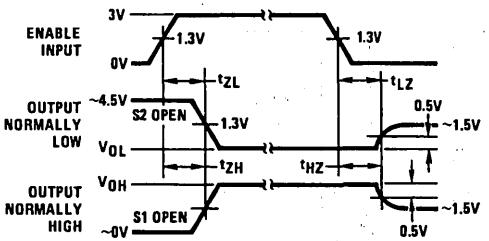

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FIGURE 6. Enable and Disable Times for "LS-Type" Load (Notes 8, 9)

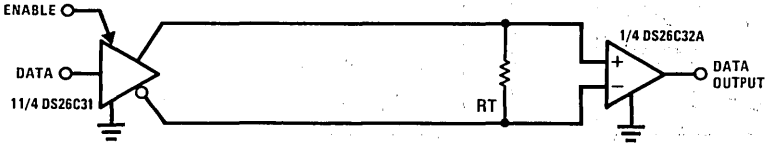
Note 7: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 8: S1 and S2 of load circuit are closed except where shown.

Note 9: Pulse generator for all pulses: Rate ≤ 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.

Typical Applications

Two-Wire Balanced Systems, RS-422



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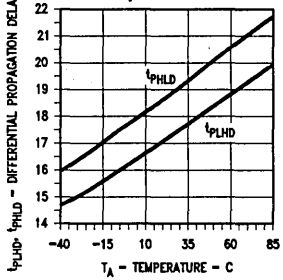
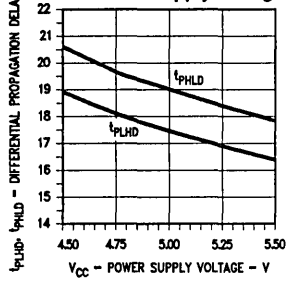
Typical Performance Characteristics

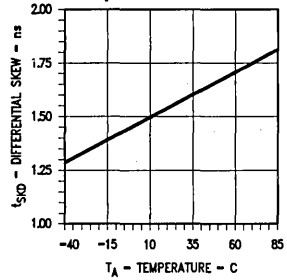
Differential Propagation Delay vs Temperature



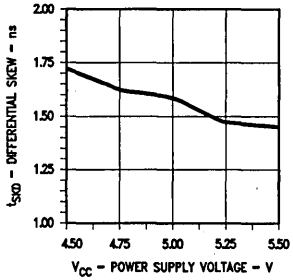
Differential Propagation Delay vs Power Supply Voltage



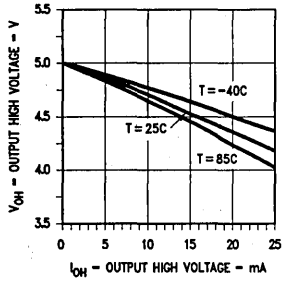
Differential Skew vs Temperature



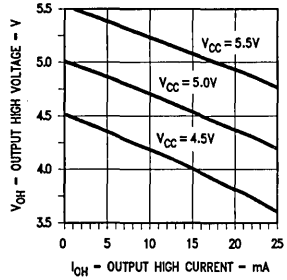
Differential Skew vs Power Supply Voltage



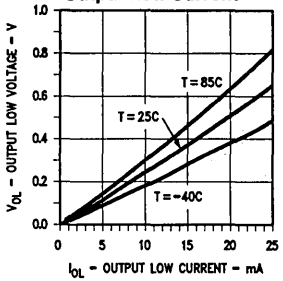
Output High Voltage vs Output High Current



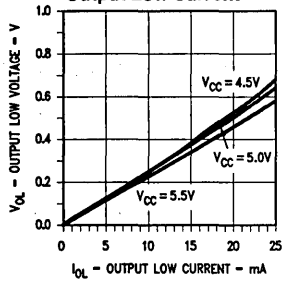
Output High Voltage vs Output High Current



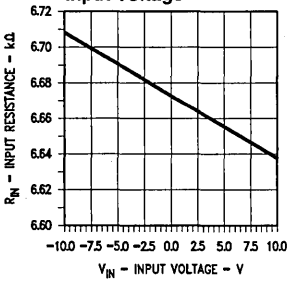
Output Low Voltage vs Output Low Current



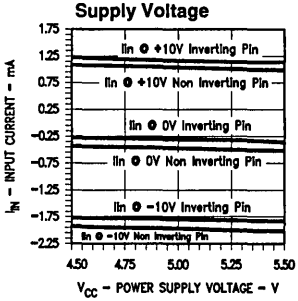
Output Low Voltage vs Output Low Current



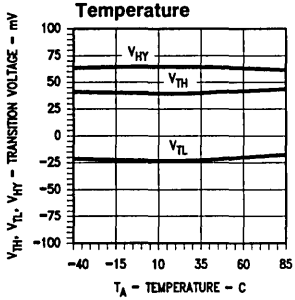
Input Resistance vs Input Voltage



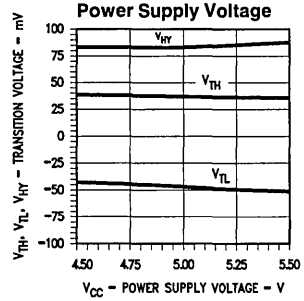
Input Current vs Power Supply Voltage



Hysteresis & Differential Transition Voltage vs Temperature



Hysteresis & Differential Transition Voltage vs Power Supply Voltage



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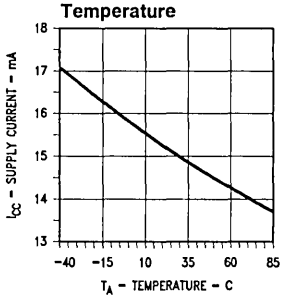
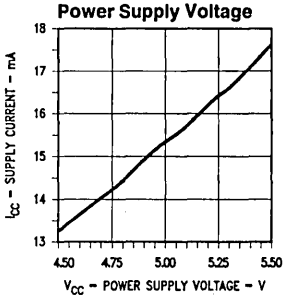
Typical Performance Characteristics (Continued)

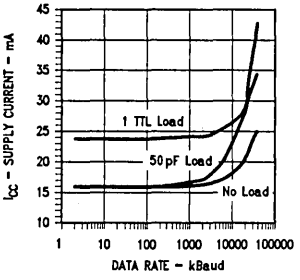
Supply Current vs Temperature



Disabled Supply Current vs Power Supply Voltage



Supply Current vs Data Rate



TL/F/8764–11

2

National Semiconductor

DS26F32C/DS26F32M
Quad Differential Line Receiver

General Description

The DS26F32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26F32 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F32 features lower power, extended temperature range, and improved specifications.

The device features an input sensitivity of 200 mV over the input common mode range of ±7.0V. The DS26F32 provides an enable function common to all four receivers and TRI-STATE® outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

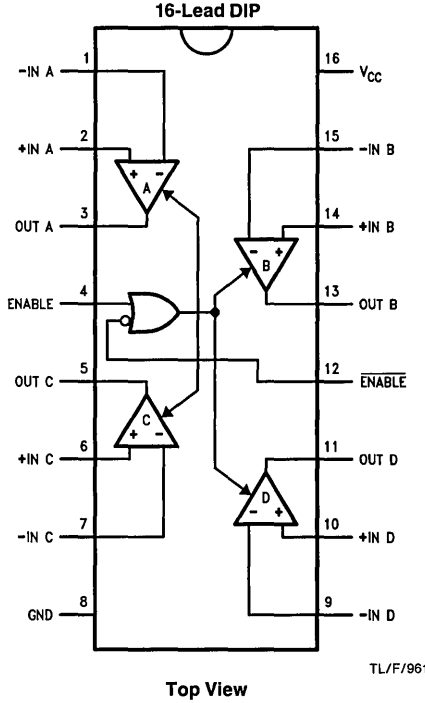
The DS26F32 offers optimum performance when used with the DS26F31 Quad Differential Line Driver.

Features

- Military temperature range
- Input voltage range of ±7.0V (differential or common mode) ±0.2V sensitivity over the input voltage range
- Meets all the requirements of EIA standards RS-422 and RS-423
- High input impedance (18k typical)
- 30 mV input hysteresis
- Operation from single +5.0V supply
- Input pull-down resistor prevents output oscillation on unused channels
- TRI-STATE outputs, with choice of complementary enables, for receiving directly onto a data bus
- Propagation delay 15 ns typical

Connection Diagram

16-Lead DIP



TL/F/9615–1

Top View

Function Table (Each Receiver)

Differential Inputs	Enables		Outputs
$V_{ID} = (V_{IN}+) - (V_{IN}-)$	E	$\overline{E}$	OUT
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	H	Z

H = High Level
L = Low Level
X = Immaterial

Order Number DS26F32CJ or DS26F32MJ
See NS Package Number J16A

For Complete Military 883 Specifications, see RETS Datasheet.

Order Number DS26F32ME/883, DS26F32MJ/883 or DS26F32MW/883

See NS Package Number E20A, J16A or W16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to + 175°C
Operating Temperature Range	
DS26F32M	−55°C to +125°C
DS26F32C	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Supply Voltage	7.0V
Common Mode Voltage Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7.0V
Output Sink Current	50 mA

*Derate cavity package 10 mW/°C above 25°C.

Operating Range

DS26F32C	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS26F32M	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V

Electrical Characteristics Over operating range, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$-7.0V \le V_{CM} \le +7.0V$, $V_O = V_{OL}$ or V_{OH}		−0.2	±0.06	+0.2	V
R_I	Input Resistance	$-15V \le V_{CM} \le +15V$, One Input AC Ground		14	18		kΩ
I_I	Input Current (under Test)	$V_I = +15V$, Other Input $-15V \le V_I \le +15V$				2.3	mA
		$V_I = -15V$, Other Input $-15V \le V_I \le +15V$				−2.8	
V_{OH}	Output Voltage HIGH	V_{CC} = Min, $\Delta V_I = +1.0V$, $V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\ \mu A$	0°C to +70°C	2.8	3.4		V
			−55°C to +125°C	2.5	3.4		
V_{OL}	Output Voltage LOW	V_{CC} = Min, $\Delta V_I = -1.0V$, $V_{\overline{ENABLE}} = 0.8V$	I_{OL} = 4.0 mA			0.4	V
			I_{OL} = 8.0 mA			0.45	
V_{IL}	Enable Voltage LOW					0.8	V
V_{IH}	Enable Voltage HIGH			2.0			V
V_{IC}	Enable Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	
I_{IL}	Enable Current LOW	V_I = 0.4V			−0.2	−0.36	mA
I_{IH}	Enable Current HIGH	V_I = 2.7V			0.5	10	μA
I_I	Enable Input High Current	V_I = 5.5V			1.0	50	μA
I_{OS}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4) $\Delta V_I = +1.0V$		−15	−50	−85	mA
I_{CC}	Supply Current	V_{CC} = Max, All V_I = GND, Outputs Disabled			30	50	mA
V_{HYST}	Input Hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V			30		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

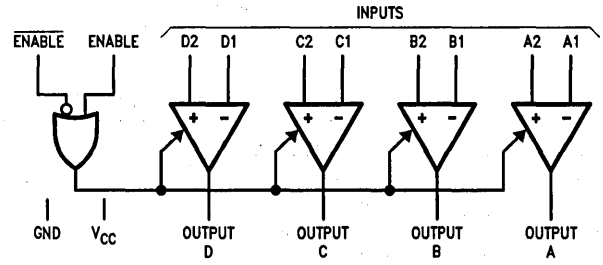
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS26F32M and across the 0°C to +70°C range for the DS26F32C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

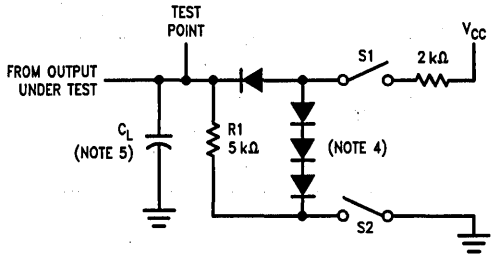
Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Input to Output	*Figures 2, 3*	C_L = 15 pF		15	22	ns
t_{PHL}	Input to Output				15	22	ns
t_{LZ}	Enable to Output	*Figures 2, 4*	C_L = 5 pF		14	18	ns
t_{HZ}	Enable to Output				15	20	ns
t_{ZL}	Enable to Output		C_L = 15 pF		13	18	ns
t_{ZH}	Enable to Output				12	16	ns



TL/F/9615–2

FIGURE 1. Logic Symbol



TL/F/9615–3

FIGURE 2. Load Test Circuit for Three-State Outputs

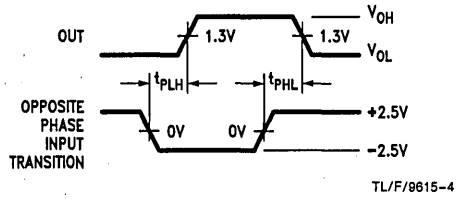


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FIGURE 3. Propagation Delay (Notes 1, 2 and 3)

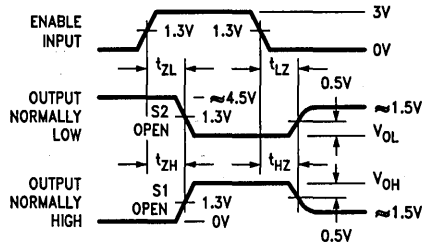

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FIGURE 4. Enable and Disable Times (Notes 1, 2 and 3)

Note 1: Diagram shown for $\overline{\text{ENABLE}}$ Low.

Note 2: S1 and S2 of Load Circuit are closed except where shown.

Note 3: Pulse Generator of all Pulses: Rate ≤ 1.0 MHz, Z_O = 50Ω, t_r ≤ 6.0 ns, t_f ≤ 6.0 ns.

Note 4: All diodes are IN916 or IN3064.

Note 5: C_L includes probe and jig capacitance.

Typical Application

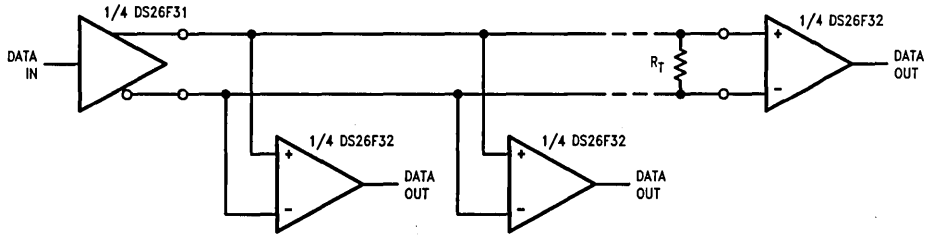

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FIGURE 5

National Semiconductor

DS26LS32C/DS26LS32M/DS26LS32AC/DS26LS33C/ DS26LS33M/DS26LS33AC Quad Differential Line Receivers

General Description

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of ±7V and the DS26LS33 and DS26LS33A have an input sensitivity of 500 mV over the input voltage range of ±15V.

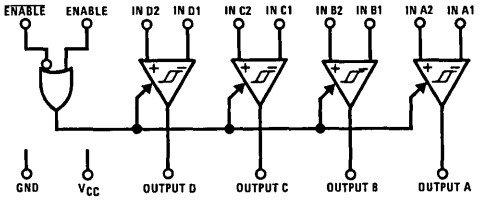
Both the DS26LS32A and DS26LS33A differ in function from the popular DS26LS32 and DS26LS33 in that input pull-up and pull-down resistors are included which prevent output oscillation on unused channels.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE® outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commerical operating temperature ranges.

Features

- High differential or common-mode input voltage ranges of ±7V on the DS26LS32 and DS26LS32A and ±15V on the DS26LS33 and DS26LS33A
- ±0.2V sensitivity over the input voltage range on the DS26LS32 and DS26LS32A, ±0.5V sensitivity on the DS26LS33 and DS26LS33A
- DS26LS32 and DS26LS32A meet all requirements of RS-422 and RS-423
- 6k minimum input impedance
- 100 mV input hysteresis on the DS26LS32 and DS26LS32A, 200 mV on the DS26LS33 and DS26LS33A
- Operation from a single 5V supply
- TRI-STATE outputs, with choice of complementary output enables for receiving directly onto a data bus

Logic Diagram



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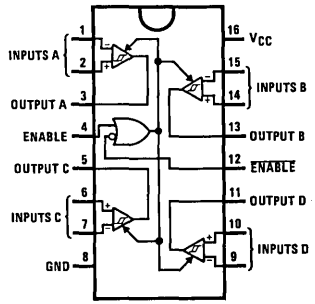
Connection Diagram

Dual-In-Line Package



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Top View

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0

HI-Z = TRI-STATE

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

Order Number DS26LS32CM, DS26LS32CN, DS26LS32MJ, DS26LS32ACM, DS26LS32ACN, DS26LS33CN, DS26LS33MJ or DS26LS33ACN
See NS Package Number J16A, M16A or N16A

For Complete Military 883 Specifications, See RETS Data Sheet.

Order Number DS26LS32MJ/883, DS26LS32MW/883, DS26LS33MJ/883, DS26LS33MW/883
See NS Package Number J16A or W16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Common-Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Dip Package	1362 mW
SO Package DS26LS32	1002 mW
DS26LS32A	1051 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C.

Derate SO Package 8.01 mW/°C for DS26LS32
8.41 mW/°C for DS26LS32A

Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS26LS32M, DS26LS33M (MIL)	4.5	5.5	V
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	4.75	5.25	V
Temperature, (T_A)			
DS26LS32M, DS26LS33M (MIL)	−55	+125	°C
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	0	+70	°C

Electrical Characteristics over the operating temperature range unless otherwise specified (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL}	DS26LS32, DS26LS32A, $-7V \le V_{CM} \le +7V$	−0.2	±0.07	0.2	V
			DS26LS33, DS26LS33A, $-15V \le V_{CM} + 15V$	−0.5	±0.14	0.5	V
R_{IN}	Input Resistance	$-15V \le V_{CM} \le +15V$ (One Input AC GND)		6.0	8.5		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = 15V$, Other Input $-15V \le V_{IN} \le +15V$				2.3	mA
		$V_{IN} = -15V$, Other Input $-15V \le V_{IN} \le +15V$				−2.8	mA
V_{OH}	Output High Voltage	V_{CC} = MIN, $\Delta V_{IN} = 1V$, $V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\ \mu A$	Commercial	2.7	4.2		V
			Military	2.5	4.2		V
V_{OL}	Output Low Voltage	V_{CC} = Min, $\Delta V_{IN} = -1V$, $V_{\overline{ENABLE}} = 0.8V$	I_{OL} = 4 mA			0.4	V
			I_{OL} = 8 mA			0.45	V
V_{IL}	Enable Low Voltage					0.8	V
V_{IH}	Enable High Voltage			2.0			V
V_I	Enable Clamp Voltage	V_{CC} = Min, $I_{IN} = -18$ mA				−1.5	V
I_O	OFF-State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	μA
I_{IL}	Enable Low Current	$V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Enable High Current	$V_{IN} = 2.7V$				20	μA
I_{SC}	Output Short-Circuit Current	$V_O = 0V$, V_{CC} = Max, $\Delta V_{IN} = 1V$		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled	DS26LS32, DS26LS32A		52	70	mA
			DS26LS33, DS26LS33A		57	80	mA
I_I	Input High Current	$V_{IN} = 5.5V$				100	μA
V_{HYST}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5V$, $V_{CM} = 0V$	DS26LS32, DS26S32A		100		mV
			DS26LS33, DS26LS33A		200		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, all currents out of device pins are shown as negative, all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 3: All typical values are $V_{CC} = 5V$, $T_A = 25°C$.

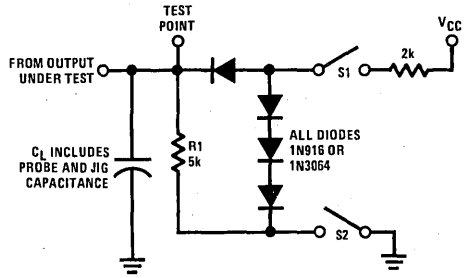
Note 4: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

Symbol	Parameter	Conditions	DS26LS32/DS26LS33			DS26LS32A/DS26LS33A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Input to Output	$C_L = 15$ pF		17	25		23	35	ns
t_{PHL}				17	25		23	35	ns
t_{LZ}	ENABLE to Output	$C_L = 5$ pF		20	30		15	22	ns
t_{HZ}				15	22		20	25	ns
t_{ZL}	ENABLE to Output	$C_L = 15$ pF		15	22		14	22	ns
t_{ZH}				15	22		15	22	ns

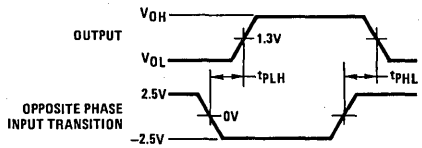
AC Test Circuit and Switching Time Waveforms

Load Test Circuit for TRI-STATE Outputs



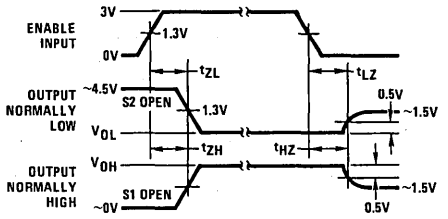
TL/F/5255–3

Propagation Delay (Notes 1 and 3)



TL/F/5255–4

Enable and Disable Times (Notes 2 and 3)



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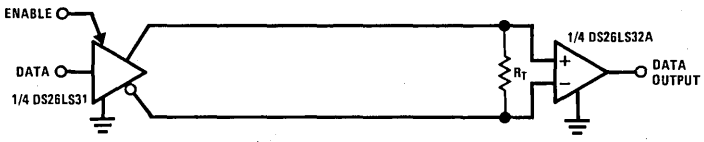
Note 1: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 2: S1 and S2 of load circuit are closed except where shown.

Note 3: Pulse generator for all pulses: Rate = 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 6$ ns; $t_f \leq 6.0$ ns.

Typical Applications

Two-Wire Balanced Interface—RS-422



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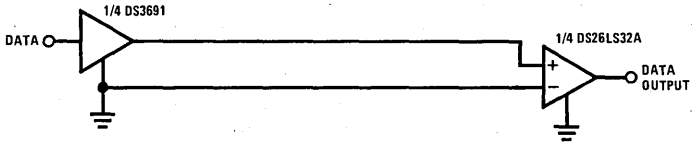
Single Wire with Driver Ground Reference—RS-423



TL/F/5255–7

National Semiconductor

DS34C86T
Quad CMOS Differential Line Receiver

General Description

The DS34C86T is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS34C86T has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Hysteresis is provided to improve noise margin and discourage output instability for slowly changing input waveforms.

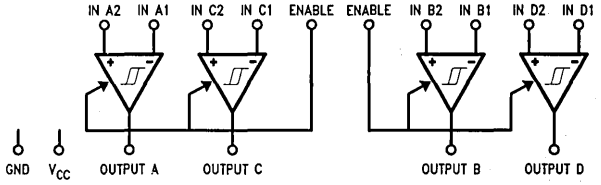
The DS34C86T features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

Separate enable pins allow independent control of receiver pairs. The TRI-STATE® outputs have 6 mA source and sink capability. The DS34C86T is pin compatible with the DS3486.

Features

- CMOS design for low power
- ±0.2V sensitivity over the input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for system bus compatibility
- Available in surface mount
- Open input Failsafe feature, output high for open input

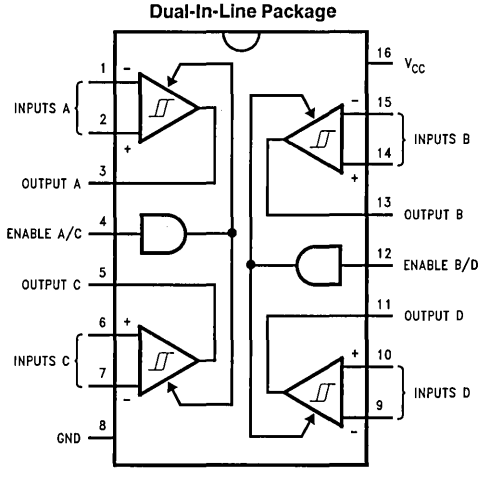
Logic Diagram



TL/F/8699–1

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS34C86TJ, DS34C86TM, and DS34C86TN
See NS Package Number J16A, M16A and N16E

Truth Table

Enable	Input	Output
L	X	Z
H	$V_{ID} \geq V_{TH}$ (Max)	H
H	$V_{ID} \leq V_{TH}$ (Min)	L
H	Open*	H

*Open, not terminated
Z = TRI-STATE

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec)	260°C
Maximum Power Dissipation at 25°C (Note 5)	
Ceramic "J" Package	2308 mW
Plastic "N" Package	1645 mW
SOIC Package	1190 mW
Current Per Output	±25 mA

This device does not meet 2000V ESD rating. (Note 4)

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	−200	35	+200	mV
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	5.0	6.8	10	kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +10V$, Other Input = GND $V_{IN} = -10V$, Other Input = GND		+1.1 −2.0	+1.5 −2.5	mA mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min., $V_{(DIFF)} = +1V$ $I_{OUT} = -6.0$ mA	3.8	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max., $V_{(DIFF)} = -1V$ I_{OUT} = 6.0 mA		0.2	0.3	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, TRI-STATE Control = V_{IL}		±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., $V_{(DIFF)} = +1V$		16	23	mA
V_{HYST}	Input Hysteresis	V_{CM} = 0V		60		mV

AC Electrical Characteristics V_{CC} = 5V ±10% (Note 3) (*Figures 1, 2,* and *3*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		19	30	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		4	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	18	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	21	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply across the operating temperature range.

All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: ESD Rating; HBM (1.5kΩ, 100 pF)
Inputs ≥ 2000V
All other pins ≥ 1000V
EIAJ (0Ω, 200 pF) ≥ 350V

Note 5: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.16 mW/°C, J Package 15.38 mW/°C and M Package 9.52 mW/°C.

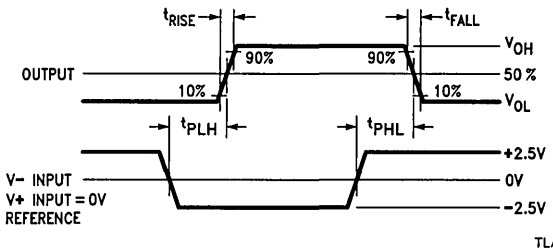
Comparison Table of Switching Characteristics into "LS-Type" Load

V_{CC} = 5V, T_A = 25°C (*Figures 4* and *5*) (Note 6)

Symbol	Parameter	DS34C86		DS3486		Units
		Typ	Max	Typ	Max	
$t_{PHL(D)}$	Propagation Delay Time Output High to Low	17		19		ns
$t_{PLH(D)}$	Propagation Delay Time Output Low to High	19		19		ns
t_{PLZ}	Output Low to TRI-STATE	13		23		ns
t_{PHZ}	Output High to TRI-STATE	12		25		ns
t_{PZH}	Output TRI-STATE to High	13		18		ns
t_{PZL}	Output TRI-STATE to Low	13		20		ns

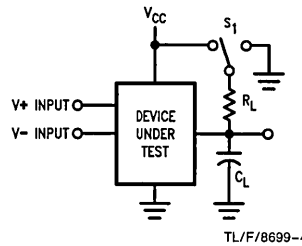
Note 6: This Table is provided for comparison purposes only. The values in this table for the DS34C86 reflect the performance of the device but are not tested or guaranteed.

Test and Switching Waveforms



TL/F/8699-3

FIGURE 1. Propagation Delays



TL/F/8699-4

C_L Includes load and test jig capacitance.
S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = GND for t_{PZH}, and t_{PHZ} measurements.

FIGURE 2. Test Circuit for TRI-STATE Output Tests

Test and Switching Waveforms (Continued)

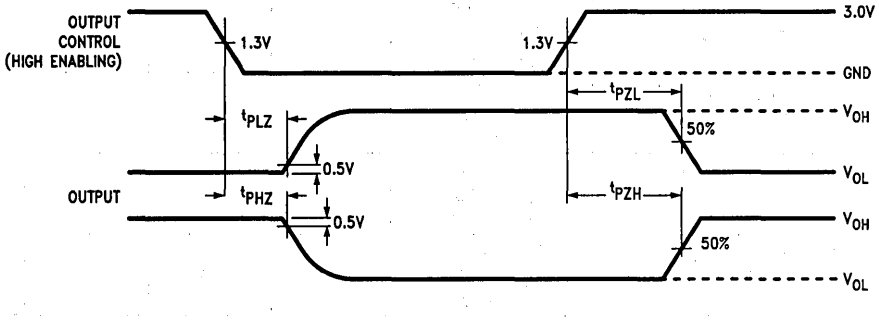
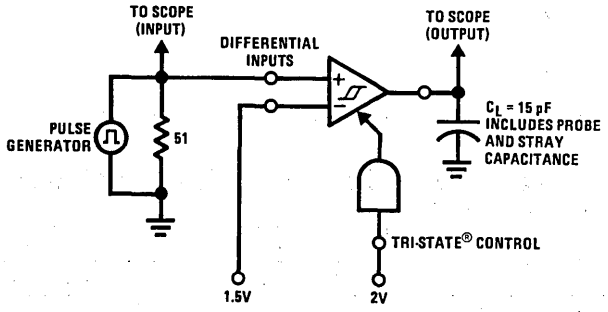
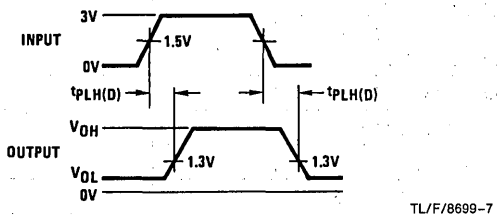


FIGURE 3. TRI-STATE Output Enable and Disable Waveforms

AC Test Circuits and Switching Time Waveforms

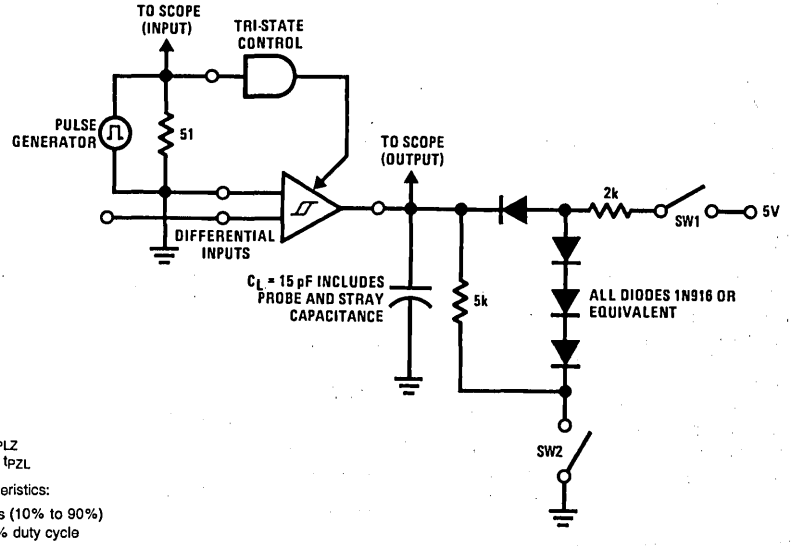




Input Pulse Characteristics:
$t_{TLH} = t_{THL} = 6$ ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

FIGURE 4. Propagation Delay Differential Input to Output for "LS-Type" Load

AC Test Circuits and Switching Time Waveforms (Continued)

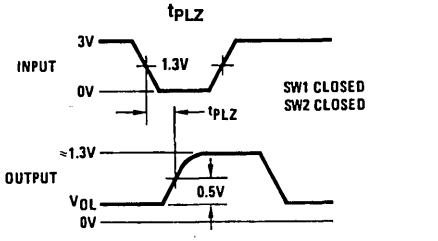


1.5V for t_{PHZ} and t_{PLZ}
−1.5V for t_{PLZ} and t_{PZL}

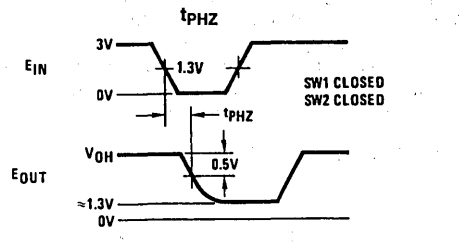
Input Pulse Characteristics:

$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

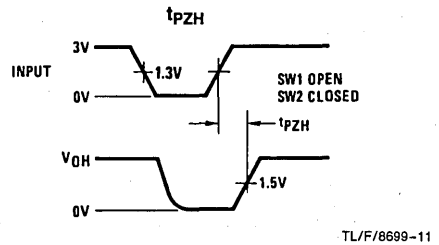
TL/F/8699-8



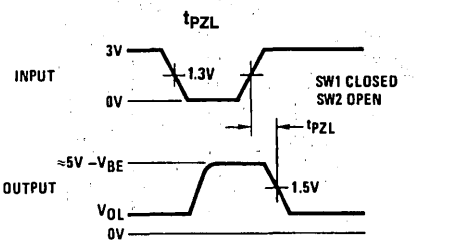
TL/F/8699-9



TL/F/8699-10



TL/F/8699-11



TL/F/8699-12

FIGURE 5. Propagation Delay TRI-STATE Control Unit to Output for "LS-Type" Load

National Semiconductor

DS34F86/DS35F86 RS-422/RS-423 Quad Line Receiver with TRI-STATE® Outputs

General Description

The DS34F86/DS35F86 RS-422/3 Quad Receiver features four independent receivers, which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible TRI-STATE structures which are forced to a high impedance state when the appropriate output control lead reaches a logic zero condition. A PNP device buffers each output control lead to assure minimum loading for either logic one or logic zero inputs. In addition each receiver has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

The DS34F86/DS35F86 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS34F86/DS35F86 features lower power, extended temperature range, and improved specifications.

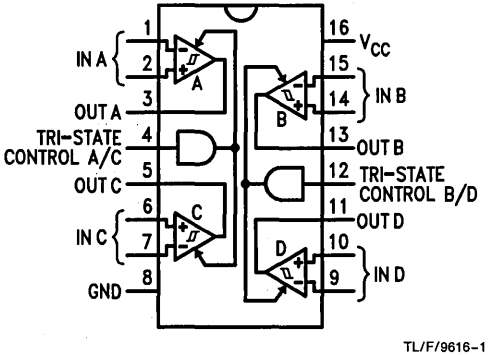
The DS34F86/DS35F86 offers optimum performance when used with the DS34F87/DS35F87 Quad Line Driver.

Features

- Military temperature range
- TRI-STATE outputs
- Fast propagation times (15 ns typical)
- TTL compatible
- 5.0V supply
- Lead compatible and interchangeable with MC3486 and DS3486

Connection Diagram

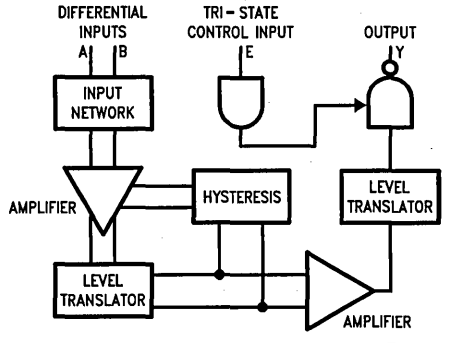
16-Lead DIP



TL/F/9616–1

Top View

Order Number DS34F86J or DS35F86J
See NS Package Number J16A



TL/F/9616–2

FIGURE 1. Block Diagram

Function Table (Each Receiver)

Differential Inputs $V_{ID} = (V_{IN}+) - (V_{IN}-)$	Enable E	Output OUT
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

H = High Level
L = Low Level
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
Ceramic DIP −65°C to +175°C

Operating Temperature Range
DS35F86 −55°C to +125°C
DS34F86 0°C to +70°C

Lead Temperature
Ceramic DIP (soldering, 60 seconds) 300°C

Maximum Power Dissipation* at 25°C
Cavity Package 1500 mW

Supply Voltage 8.0V

Input Voltage 8.0V

Input Common Mode Voltage ±15V

Input Differential Voltage ±25V

*Derate cavity package 10 mW/°C above 25°C.

Operating Conditions

DS34F86
Temperature 0°C to +70°C
Supply Voltage 4.75V to 5.25V

DS35F86
Temperature −55°C to +125°C
Supply Voltage 4.5V to 5.5V

Input Common Mode Voltage Range −7.0V to +7.0V

Input Differential Voltage Range 6V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2			V
V_{IL}	Input Voltage LOW					0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage (Note 6)	$-7V \le V_{CM} \le 7V$, $V_{IH} = 2V$	$V_O = V_{OH}$			0.2	V
			$V_O = V_{OL}$	−0.2			
I_{IB}	Input Bias Current	V_{CC} = 0V or 5.25V, Other inputs at 0V	$V_I = -10V$			−3.25	mA
			$V_I = -3V$			−1.50	
			$V_I = +3V$			+1.50	
			$V_I = +10V$			+3.25	
V_{OH}	Output Voltage HIGH (Note 5)	$-7V \le V_{CM} \le 7V$, $V_{IH} = 2V$, $I_O = -0.4$ mA, $V_{ID} = 0.4V$	0°C to +70°C	2.8			V
			−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	$-7V \le V_{CM} \le 7V$, $V_{IH} = 2V$	$I_O = 8$ mA, $V_{ID} = 0.4V$			0.5	V
I_{OZ}	Off State (High Impedance) Output Current	$V_{I(D)} = +3V$, $V_{IL} = 0.8V$, $V_O = 0.5V$				−10	μA
		$V_{I(D)} = -3V$, $V_{IL} = 0.8V$, $V_O = 2.7V$				10	
I_{OS}	Output Short Circuit Current (Note 4)	$V_{I(D)} = +3V$, $V_{IH} = 2V$, $V_O = 0V$		−15		−100	mA
I_{IL}	Input Current LOW (TRI-STATE Control)	$V_{IL} = 0.5V$				−100	μA
I_{IH}	Input Current HIGH (TRI-STATE Control)		$V_{IH} = 2.7V$			20	μA
			$V_{IH} = 5.25V$			40	
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)	$I_{IC} = -10$ mA				−1.5	V
I_{CC}	Supply Current	$V_{IL} = 0V$				50	mA

2

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS35F86 and across the 0°C to +70°C range for the DS34F86. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

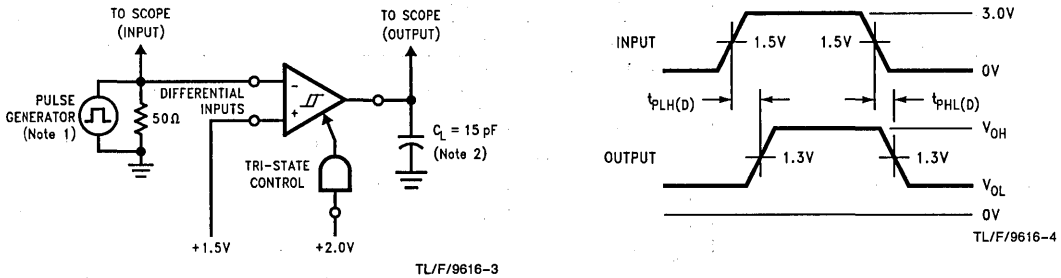
Note 5: Refer to EIA RS-422/3 for exact conditions. Input balance and V_{OH}/V_{OL} levels are tested simultaneously for worse case.

Note 6: Differential input threshold voltage and guaranteed output levels are tested simultaneously for worst case.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (Figures 2 & 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
$t_{PHL(D)}$	Propagation Delay Time Differential Inputs to Outputs	*Figure 2*		15	22	ns
$t_{PLH(D)}$				15	22	ns
t_{LZ}	Propagation Delay Time Controls to Outputs	C_L = 5 pF *Figure 3*		14	18	ns
t_{HZ}				15	20	ns
t_{ZH}		*Figure 3*		12	16	ns
t_{ZL}				13	18	ns

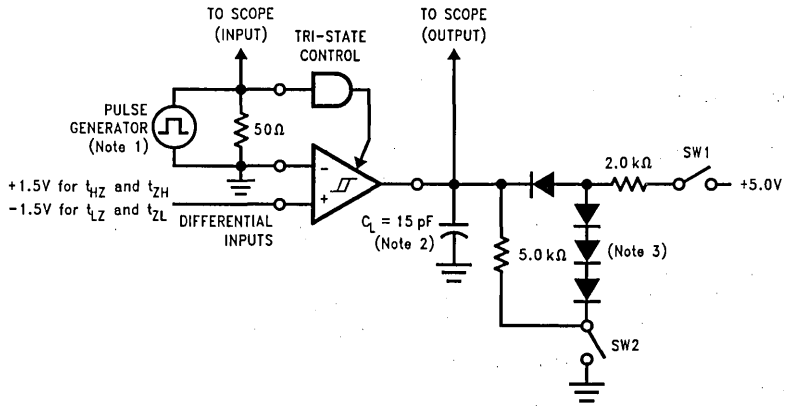
Parameter Measurement Information



TL/F/9616-3

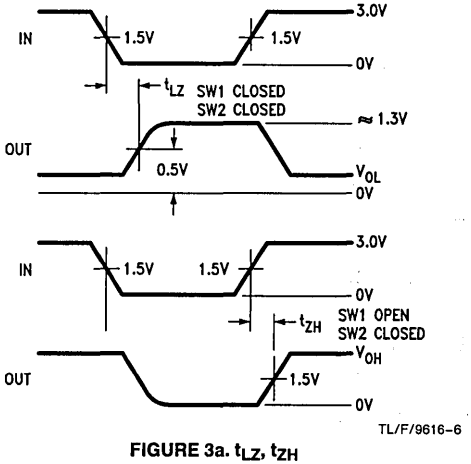
FIGURE 2. Propagation Delay Differential Input to Output

Parameter Measurement Information (Continued)



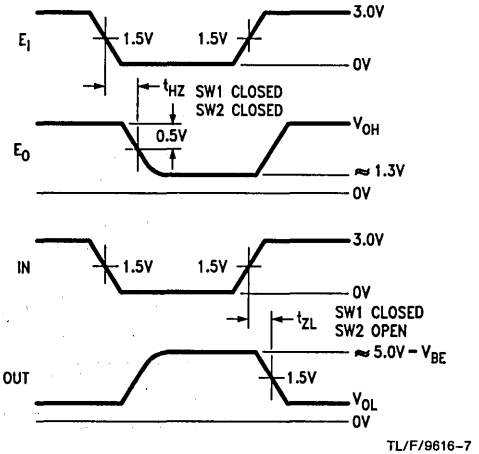
TL/F/9616–5

FIGURE 3. Propagation Delay TRI-STATE Control Input to Output



TL/F/9616–6

FIGURE 3a. t_{LZ}, t_{ZH}



TL/F/9616–7

FIGURE 3b. t_{HZ}, t_{ZL}

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_{TLH} = t_{THL}$ = 6.0 ns (10% to 90%), Z_O = 50Ω.

Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are IN916 or equivalent.

2

National Semiconductor

DS3486 Quad RS-422, RS-423 Line Receiver

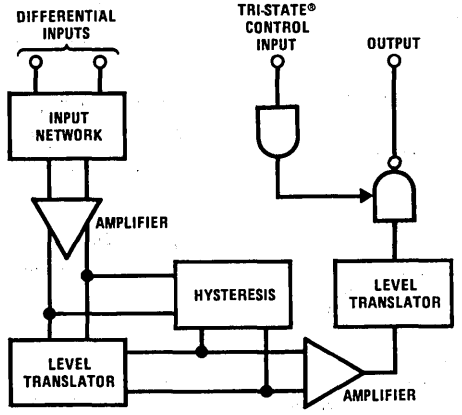
General Description

National's quad RS-422, RS-423 receiver features four independent receivers which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible, TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

Features

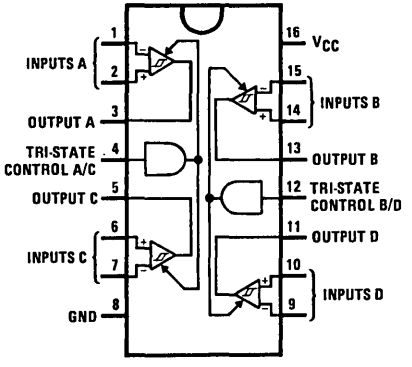
- Four independent receivers
- TRI-STATE outputs
- Internal hysteresis −140 mV (typ)
- Fast propagation times −19 ns (typ)
- TTL compatible outputs
- 5V supply
- Pin compatible and interchangeable with MC3486

Block and Connection Diagrams



TL/F/5779–1

Dual-In-Line Package



TL/F/5779–2

Top View

Order Number DS3486J, DS3486M or DS3486N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage, V_{CC}	8V
Input Common-Mode Voltage, V_{ICM}	±25V
Input Differential Voltage, V_{ID}	±25V
TRI-STATE Control Input Voltage, V_I	8V
Output Sink Current, I_O	50 mA
Storage Temperature, T_{STG}	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433mW
Molded Dip Package	1362 mW
SO Package	1002 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate Dip molded package 10.2 mW/°C above 25°C. Derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Power Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A	0	70	°C
Input Common-Mode Voltage Range, V_{ICR}	−7.0	7.0	V

Electrical Characteristics

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5V and V_{IC} = 0V. See Note 2.)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage—High Logic State (TRI-STATE Control)			2.0			V
V_{IL}	Input Voltage—Low Logic State (TRI-STATE Control)					0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage		$-7V \le V_{IC} \le 7V$, V_{IH} TRI-STATE = 2V $I_O = -0.4$ mA, $V_{OH} \ge 2.7V$		0.070	0.2	V
			I_O = 8 mA, $V_{OL} \ge 0.5V$		0.070	−0.2	V
$I_{IB(D)}$	Input Bias Current		V_{CC} = 0V or 5.25V, Other Inputs at 0V				
			$V_I = -10V$			−3.25	mA
			$V_I = -3V$			−1.50	mA
			V_I = 3V			1.50	mA
			V_I = 10V			3.25	mA
	Input Balance		$-7V \le V_{IC} \le 7V$, $V_{IH(3C)}$ = 2V, (Note 4)				
		V_{OH}	$I_O = -0.4$ mA, V_{ID} = 0.4V	2.7			V
		V_{OL}	I_O = 8 mA, $V_{ID} = -0.4V$			0.5	V
I_{OZ}	Output TRI-STATE Leakage Current		$V_{I(D)}$ = 3V, V_{IL} = 0.8V, V_{OL} = 0.5V			−40	μA
			$V_{I(D)} = -3V$, V_{IL} = 0.8V, V_{OH} = 2.7V			40	μA
I_{OS}	Output Short-Circuit Current		$V_{I(D)}$ = 3V, V_{IH} TRI-STATE = 2V, V_O = 0V, (Note 3)	−15		−100	mA
I_{IL}	Input Current—Low Logic State (TRI-STATE Control)		V_{IL} = 0.5V			−100	μA
I_{IH}	Input Current—High Logic State (TRI-STATE Control)		V_{IH} = 2.7V			20	μA
			V_{IH} = 5.25V			100	μA
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)		$I_{IN} = -10$ mA			−1.5	V
I_{CC}	Power Supply Current		All Inputs V_{IL} = 0V			85	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.

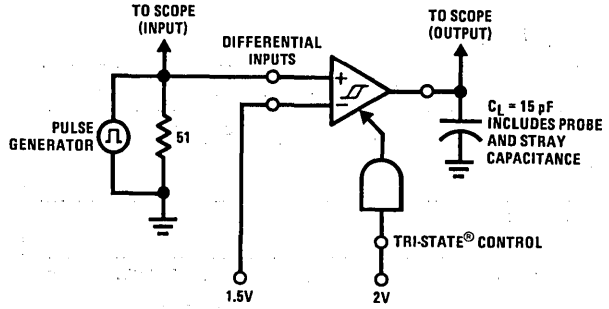
Note 3: Only one output at a time should be shorted.

Note 4: Refer to EIA RS-422/3 for exact conditions.

Switching Characteristics (Unless otherwise noted, V_{CC} = 5V and T_A = 25°C.)

Symbol	Parameter	Min	Typ	Max	Units
$t_{PHL(D)}$	Propagation Delay Time—Differential Inputs to Output Output High to Low		19	35	ns
$t_{PLH(D)}$	Output Low to High		19	30	ns
t_{PLZ}	TRI-STATE Control to Output Output Low to TRI-STATE		23	35	ns
t_{PHZ}	Output High to TRI-STATE		25	35	ns
t_{PZH}	Output TRI-STATE to High		18	30	ns
t_{PZL}	Output TRI-STATE to Low		20	30	ns

AC Test Circuits and Switching Time Waveforms



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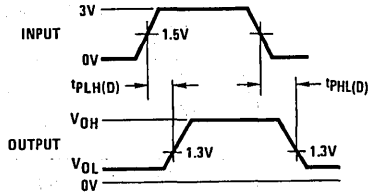
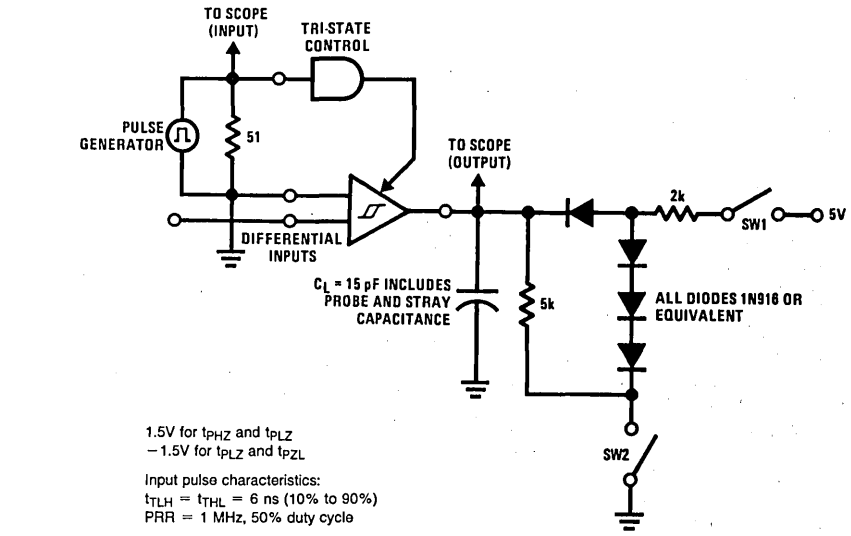


TL/F/5779–4

Input pulse characteristics:
$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

FIGURE 1. Propagation Delay Differential Input to Output

AC Test and Switching Time Waveforms (Continued)



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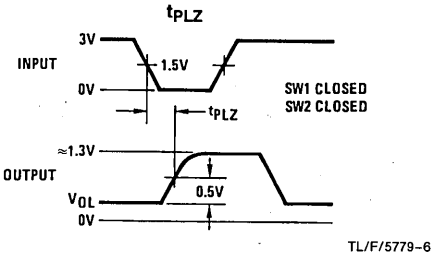
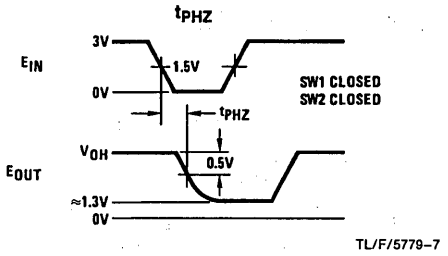


TL/F/5779–6



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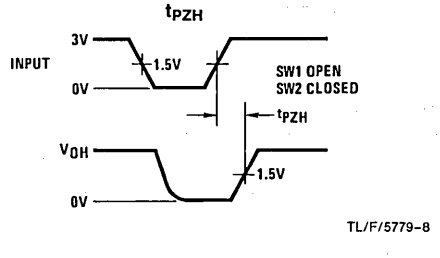

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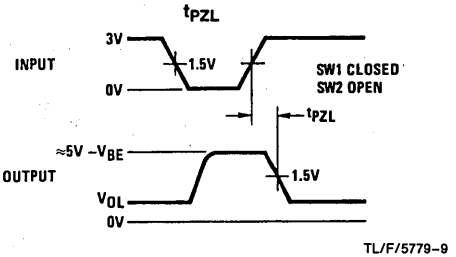


TL/F/5779–9

FIGURE 2. Propagation Delay TRI-STATE Control Input to Output

National Semiconductor

DS34C87T CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS34C87T is a quad differential line driver designed for digital data transmission over balanced lines. The DS34C87T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS34C87T accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. This device has separate enable circuitry for each pair of the four drivers. The DS34C87T is pin compatible to the DS3487T.

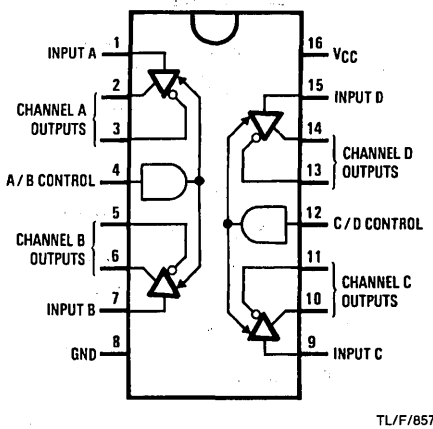
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount

Connection and Logic Diagrams

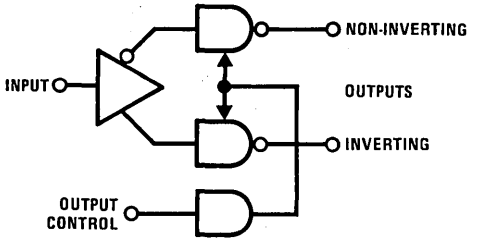
Dual-In-Line Package



TL/F/8576–1

Top View

Order Number DS34C87TJ, DS34C87TM or DS34C87TN
See NS Package Number J16A, M16A or N16E



TL/F/8576–2

Truth Table

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state X = Irrelevant
H = High logic state Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Maximum Power Dissipation (P_D) @ 25°C (Note 3)	
Ceramic "J" Package	2419 mW
Plastic "N" Package	1736 mW
SOIC Package	1226 mW
Lead Temperature (T_L) (Soldering 4 sec)	260°C

This device does not meet 2000V ESD rating. (Note 12)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
DS34C87T	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA	2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 48 mA		0.3	0.5	V
V_T	Differential Output Voltage	R_L = 100 Ω (Note 5)	2.0	3.1		V
$\lvert V_T\rvert - \lvert \overline{V}_T\rvert$	Difference In Differential Output	R_L = 100 Ω (Note 5)			0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100 Ω (Note 5)		2.0	3.0	V
$\lvert V_{OS} - \overline{V}_{OS}\rvert$	Difference In Common Mode Output	R_L = 100 Ω (Note 5)			0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}			±1.0	μA
I_{CC}	Quiescent Supply Current	I_{OUT} = 0 μA, V_{IN} = V_{CC} or GND V_{IN} = 2.4V or 0.5V (Note 6)		200 0.8	500 2.0	μA mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, Control = V_{IL}		±0.5	±5.0	μA
I_{SC}	Output Short Circuit Current	V_{IN} = V_{CC} or GND (Notes 5, 7)	−30		−150	mA
I_{OFF}	Power Off Output Leakage Current	V_{CC} = 0V (Note 5); V_{OUT} = 6V V_{OUT} = −0.25V			100 −100	μA μA

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.89 mW/°C, J Package 16.13 mW/°C, and M Package 9.80 mW/°C.

Note 4: Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V ±10%, t_r, t_f ≤ 6 ns (*Figures 1, 2, 3,* and *4*) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	S1 Open		6	11	ns
Skew	(Note 8)	S1 Open		0.5	3	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	ns
t_{PZH}	Output Enable Time	S1 Closed		12	25	ns
t_{PZL}	Output Enable Time	S1 Closed		13	26	ns
t_{PHZ}	Output Disable Time (Note 9)	S1 Closed		4	8	ns
t_{PLZ}	Output Disable Time (Note 9)	S1 Closed		6	12	ns
C_{PD}	Power Dissipation Capacitance (Note 10)			100		pF
C_{IN}	Input Capacitance			6		pF

Note 8: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 9: Output disable time is the delay from the control input being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 10: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V^2_{CC} f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Comparison Table of Switching Characteristics into "LS-Type" Load

V_{CC} = 5V, T_A = +25°C, t_r ≤ 6 ns, t_f ≤ 6 ns (*Figures 4, 5, 6, 7, 8* and *9*) (Note 11)

Symbol	Parameter	Conditions	DS34C87		DS3487		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output		6	10	10	15	ns
Skew	(Note 8)		1.5	2.0			ns
t_{THL}, t_{TLH}	Differential Output Rise and Fall Times		4	7	10	15	ns
t_{PHZ}	Output Disable Time (Note 9)	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	8	11	17	25	ns
t_{PLZ}	Output Disable Time (Note 9)	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	7	10	15	25	ns
t_{PZH}	Output Enable Time	C_L = 50 pF, R_L = ∞, S1 Open, S2 Closed	11	19	11	25	ns
t_{PZL}	Output Enable Time	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Open	14	21	15	25	ns

Note 11: This table is provided for comparison purposes only. The values in this table for the DS34C87 reflect the performance of the device but are not tested or guaranteed.

Note 12: ESD Rating: HBM (1.5 kΩ, 100 pF)

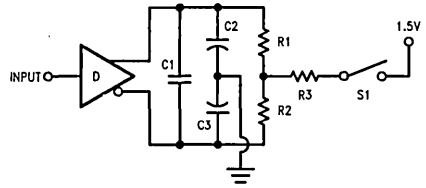
Inputs ≥ 1500V

Outputs ≥ 1000V

EIAJ (0Ω, 200 pF)

All Pins ≥ 350V

AC Test Circuit and Switching Time Waveforms



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Note: C1 = C2 = C3 = 40 pF (including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω

FIGURE 1. AC Test Circuit

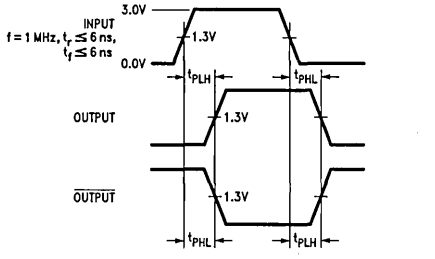

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FIGURE 2. Propagation Delays

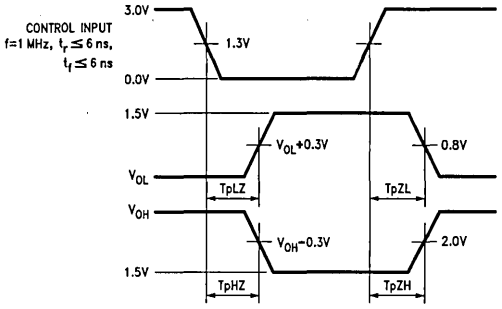

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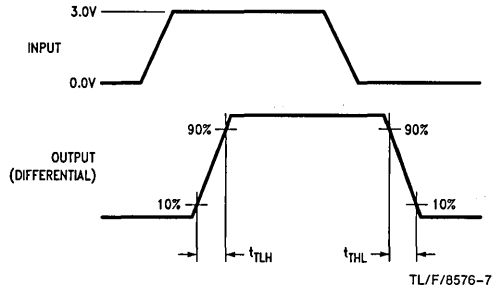
FIGURE 3. Enable and Disable Times



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Input pulse; f = 1 MHz, 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

FIGURE 4. Differential Rise and Fall Times

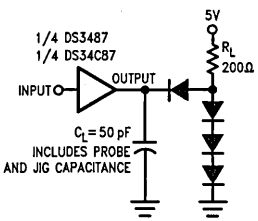

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FIGURE 5. Propagation Delays Test Circuit for "LS-Type" Load

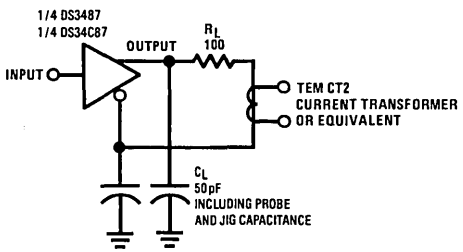

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FIGURE 6. Differential Rise and Fall Times Test Circuit for "LS-Type" Load

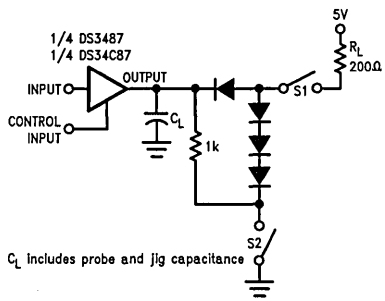

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FIGURE 7. Load Enable and Disable Times Test Circuit for "LS-Type" Load

AC Test Circuit and Switching Time Waveforms (Continued)

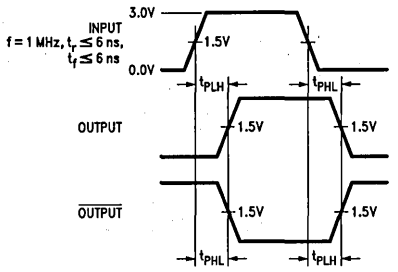

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FIGURE 8. Load Propagation Delays for "LS-Type" Load

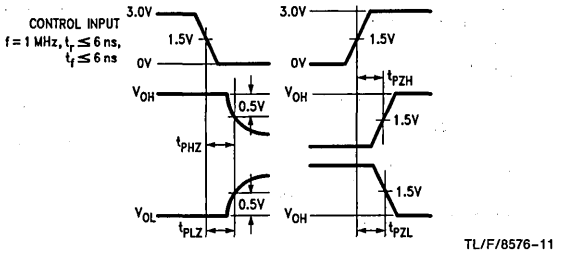

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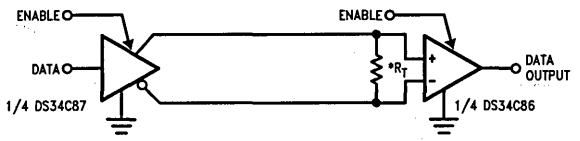
FIGURE 9. Load Enable and Disable Times for "LS-Type" Load

Typical Applications

Two-Wire Balanced System, RS-422



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*R_T is optional although highly recommended to reduce reflection.

National Semiconductor

DS34F87/DS35F87
RS-422 Quad Line Driver with TRI-STATE® Outputs

General Description

The DS34F87/DS35F87 RS-422 Quad Line Driver features four independent drivers which comply with EIA Standards for the electrical characteristics of balanced voltages digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control lead reaches a logic zero condition. All input leads are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power-up and power-down.

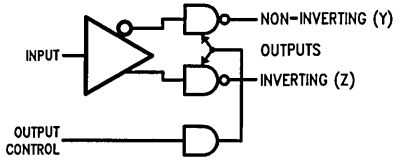
The DS34F87/DS35F87 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS34F87/DS35F87 features lower power, extended temperature range, and improved specifications.

The DS34F87/DS35F87 offers optimum performance when used with the DS34F86/DS35F86 Quad Line Receiver.

Features

- Military temperature range
- Four independent drivers
- TRI-STATE outputs
- PNP high impedance inputs
- Fast propagation time
- TTL compatible
- 5.0V supply
- Output rise and falls times less than 15 ns
- Lead compatible and interchangeable with MC3487 and DS3487

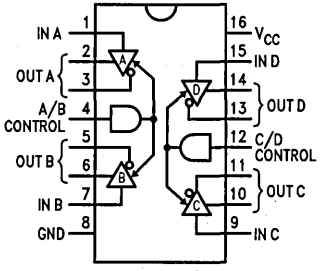
Block and Connection Diagrams



TL/F/9618–2

FIGURE 1

16-Lead DIP



TL/F/9618–1

Top View

Order Number DS34F87J, DS34F87N or DS35F87J
See NS Package Number J16A or N16A

Function Table (Each Driver)

Input	Enable	Output	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
Ceramic DIP −65°C to +175°C

Lead Temperature
Ceramic DIP (soldering, 60 sec.) 300°C

Supply Voltage 8.0V

Input Voltage 5.5V

Maximum Power Dissipation* at 25°C
Cavity Package 1500 mW

*Derate cavity package 10 mW/°C above 25°C.

Operating Range

DS34F87
Temperature 0°C to +70°C
Supply Voltage 4.75V to 5.25V

DS35F87
Temperature −55°C to +125°C
Supply Voltage 4.5V to 5.5V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Voltage LOW				0.8	V
V_{IH}	Input Voltage HIGH		2.0			V
I_{IL}	Input Current LOW	V_{IL} = 0.5V			−200	μA
I_{IH}	Input Current HIGH	V_{IH} = 2.7V			+50	μA
		V_{IH} = 5.5V			+100	
V_{IC}	Input Clamp Voltage	I_I = −18 mA			−1.5	V
V_{OL}	Output Voltage LOW	I_{OL} = 48 mA			0.5	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA	2.5			V
I_{OS}	Output Short Circuit Current (Note 4)	V_{IH} = 2.0V	−40		−140	mA
I_{OZ}	Output Leakage Current Hi-Z State	V_{IL} = 0.5V, V_{IL} (z) = 0.8V			±100	μA
		V_{IH} = 2.7V, V_{IL} (z) = 0.8V			±100	
$I_{OL(off)}$	Output Leakage Current Power Off	V_{OH} = 6.0V, V_{CC} = 0V			+100	μA
		V_{OL} = −0.25V, V_{CC} = 0V			−100	
V_{OS}-$\overline{V}_{OS}$	Output Offset Voltage Difference (Note 5)				±0.4	V
V_{OD}	Output Differential Voltage (Note 5)		2.0			V
ΔV_{OD}	Output Differential Voltage Change				±0.4	V
I_{CCX}	Supply Current	Control Leads Gnd			50	mA
I_{CC}		Control Leads 2.0V			40	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS35F87 and across the 0°C to +70°C range for the DS34F87. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA RS-422/3 for exact conditions.

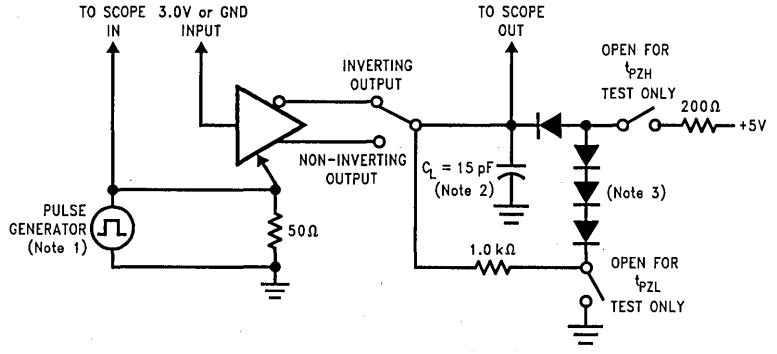
Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Times	High to Low Input			20	ns
t_{PLH}		Low to High Input			15	ns
t_{THL}	Output Transition Times—Differential	High to Low Input			15	ns
t_{TLH}		Low to High Input			15	ns
$t_{PHZ(E)}$	Propagation Delay Control to Output	R_L = 200, C_L = 50 pF			35	ns
$t_{PLZ(E)}$		R_L = 200, C_L = 50 pF			35	ns
$t_{PZH(E)}$		R_L = ∞, C_L = 50 pF			35	ns
$t_{PZL(E)}$		R_L = 200, C_L = 50 pF			35	ns
SKEW	Output to Output	Note 2			4.5	ns

Note 1: C_L = 50 pF, V_I = 1.5V to V_O = 1.5V, V_{PULSE} = 0V to +3.0V.

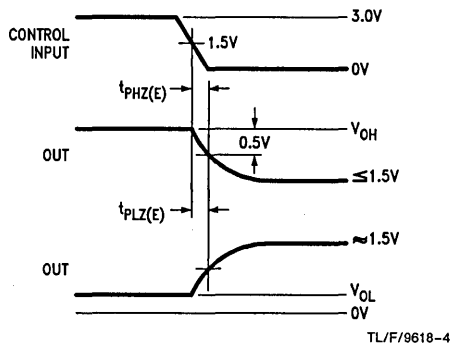
Note 2: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Parameter Measurement Information



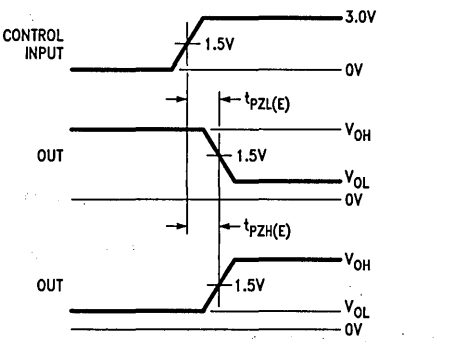
TL/F/9618-3

FIGURE 2. TRI-STATE Enable Test Circuit and Waveforms



TL/F/9618-4

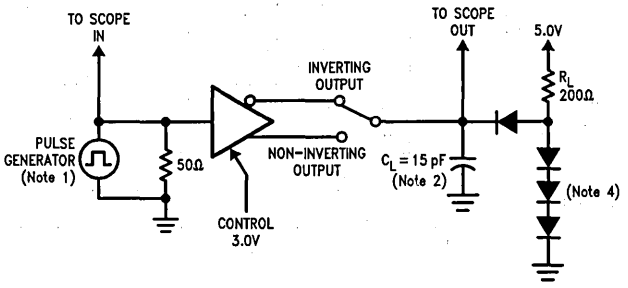
FIGURE 2a



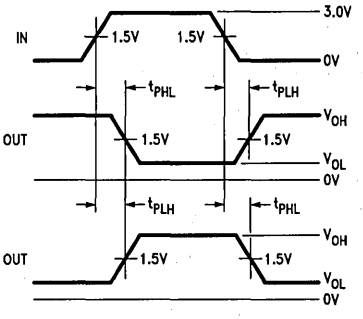
TL/F/9618-5

FIGURE 2b

Parameter Measurement Information (Continued)

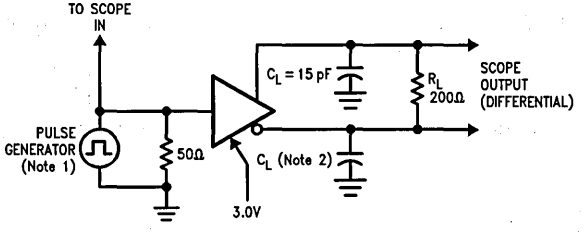


TL/F/9618-6

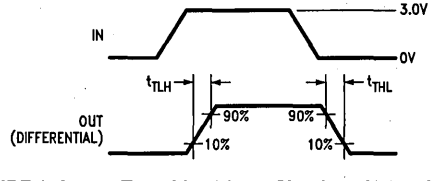


TL/F/9618-7

FIGURE 3. Propagation Delay Times Input to Output Waveforms and Test Circuit



TL/F/9618-8



TL/F/9618-9

FIGURE 4. Output Transition Times Circuit and Waveforms

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_{TLH} = t_{THL} \leq 5.0$ ns (10% to 90%), $Z_O = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are IN3064 or equivalent.

Note 4: All diodes are IN914 or equivalent.

National Semiconductor

DS3487 Quad TRI-STATE® Line Driver

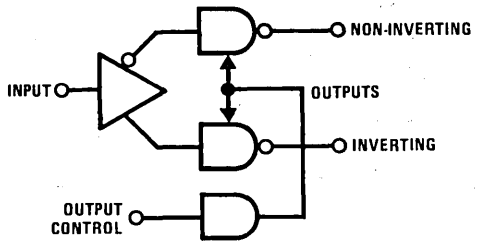
General Description

National's quad RS-422 driver features four independent drivers which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs.

Features

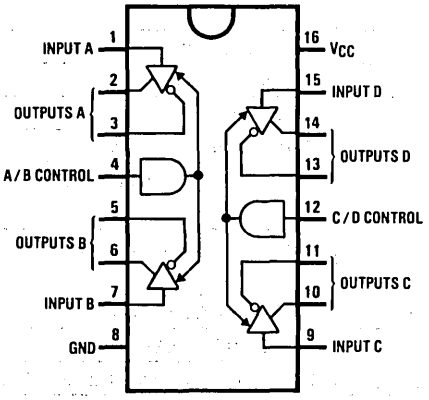
- Four independent drivers
- TRI-STATE outputs
- Fast propagation times (typ 10 ns)
- TTL compatible
- 5V supply
- Output rise and fall times less than 15 ns
- Pin compatible with DS8924 and MC3487

Block and Connection Diagrams



TL/F/5780–1

Dual-In-Line Package



TL/F/5780–2

Top View

Order Number DS3487M or DS3487N
See NS Package Number M16A or N16A

Truth Table

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded DIP Package	1476 mW
SO Package	1051 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate DIP molded package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS3487	4.75	5.25	V
Temperature (T_A)			
DS3487	0	+70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	V_{IL} = 0.5V				−200	μA
I_{IH}	Input High Current		V_{IH} = 2.7V			50	μA
			V_{IH} = 5.5V			100	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
V_{OL}	Output Low Voltage	I_{OL} = 48 mA				0.5	V
V_{OH}	Output High Voltage	I_{OH} = −20 mA		2.5			V
I_{OS}	Output Short-Circuit Current			−40		−140	mA
I_{OZ}	Output Leakage Current (TRI-STATE)		V_O = 0.5V			−100	μA
			V_O = 5.5V			100	μA
I_{OFF}	Output Leakage Current Power OFF	V_{CC} = 0V	V_O = 6V			100	μA
			V_O = −0.25V			−100	μA
$\lvert V_{OS}-\overline{V}_{OS}\rvert$	Difference in Output Offset Voltage					0.4	V
V_T	Differential Output Voltage			2.0			V
$\lvert V_T\rvert-\overline{V}_T\rvert$	Difference in Differential Output Voltage					0.4	V
I_{CC}	Power Supply Current		Active		50	80	mA
			TRI-STATE		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Input to Output			10	15	ns
t_{PLH}	Input to Output			10	15	ns
t_{THL}	Differential Fall Time			10	15	ns
t_{TLH}	Differential Rise Time			10	15	ns
t_{PHZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		17	25	ns
t_{PLZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		15	25	ns
t_{PZH}	Enable to Output	R_L = ∞, C_L = 50 pF, S1 Open		11	25	ns
t_{PZL}	Enable to Output	R_L = 200Ω, C_L = 50 pF, S2 Open		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

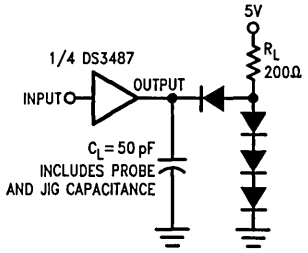
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3487. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive, all currents out of device pins as negative. All voltages are referenced to ground unless otherwise specified.

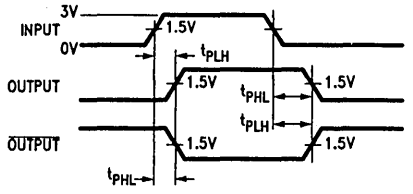
Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422, where applicable.

AC Test Circuits and Switching Time Waveforms



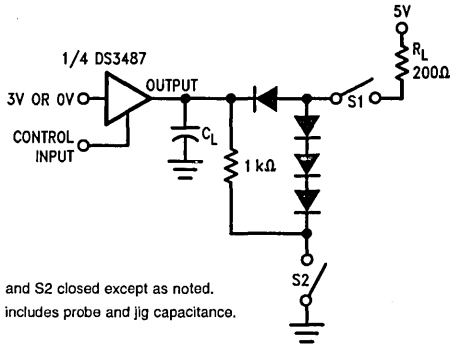
TL/F/5780-3



TL/F/5780-4

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

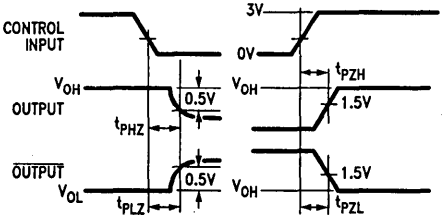
FIGURE 1. Propagation Delays



S1 and S2 closed except as noted.

C_L includes probe and jig capacitance.

TL/F/5780-5



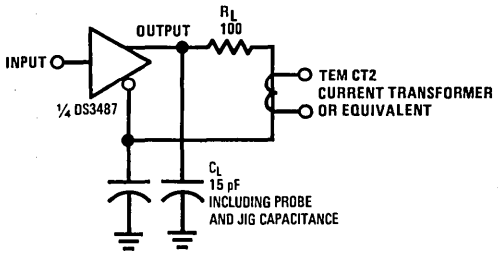
TL/F/5780-6

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

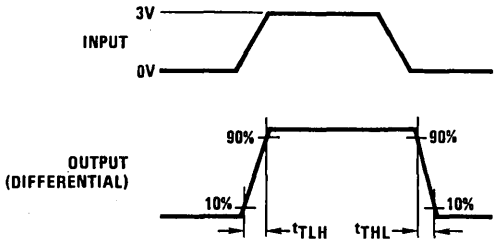
S1 = open for t_{PZH}

S2 = open for t_{PZL}

FIGURE 2. TRI-STATE Enable and Disable Delays



TL/F/5780-7



TL/F/5780-8

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 3. Differential Rise and Fall Times

National Semiconductor

DS78C20/DS88C20 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C20 and DS88C20 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver, and the pinout is identical.

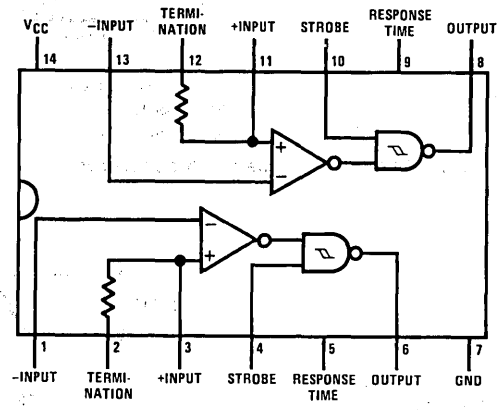
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180Ω terminating resistor, which may be used optionally on twisted pair lines. The DS78C20 is specified over a −55°C to +125°C operating temperature range, and the DS88C20 over a 0°C to +70°C range.

Features

- Meets requirements of EIA Standards RS-232-C RS-422 and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- ½ V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- DS7830/DS8830 or MM78C30/MM88C30 recommended driver

Connection Diagram

Dual-In-Line Package



TL/F/5798–1

Top View

Order Number DS78C20J or DS88C20N
See NS Package Numbers J14A or N14A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS78C20J/883
See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	18V
Common-Mode Voltage	±25V
Differential Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded Package	1280 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.1 mW/°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C20	−55	+125	°C
DS88C20	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	I_{OUT} = −200 μA, $V_{OUT} \geq V_{CC}$ −1.2V	−10V ≤ V_{CM} ≤ 10V		0.06	0.2	V
			−15V ≤ V_{CM} ≤ 15V		0.06	0.3	V
		I_{OUT} = 1.6 mA, $V_{OUT} \leq$ 0.5V	−10V ≤ V_{CM} ≤ 10V		−0.08	−0.2	V
			−15V ≤ V_{CM} ≤ 15V		−0.08	−0.3	V
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ 15V			5		kΩ
R_T	Line Termination Resistance	T_A = 25°C		100	180	300	Ω
I_{IND}	Data Input Current (Unterminated)	V_{CM} = 10V			2	3.1	mA
		V_{CM} = 0V			0	−0.5	mA
		V_{CM} = −10V			−2	−3.1	mA
V_{THB}	Input Balance	I_{OUT} = 200 μA, $V_{OUT} \geq$ V_{CC} −1.2V, R_S = 500Ω, (Note 5)	−7V ≤ V_{CM} ≤ 7V		0.1	0.4	V
		I_{OUT} = 1.6 mA, $V_{OUT} \leq$ 0.5V, R_S = 500Ω, (Note 5)	−7V ≤ V_{CM} ≤ 7V		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −200 μA, V_{DIFF} = 1V		V_{CC} − 1.2	V_{CC} − 0.75		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 1.6 mA, V_{DIFF} = −1V			0.25	0.5	V
I_{CC}	Power Supply Current	15V ≤ V_{CM} ≤ −15V, V_{DIFF} = −0.5V (Both Receivers)	V_{CC} = 5.5V		8	15	mA
			V_{CC} = 15V		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	V_{STROBE} = 15V, V_{DIFF} = 3V	V_{CC} = 15V		15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	V_{STROBE} = 0V, V_{DIFF} = −3V	V_{CC} = 15V		−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	I_{OUT} = 1.6 mA, $V_{OL} \leq$ 0.5V	V_{CC} = 5V	3.5	2.5		V
			V_{CC} = 10V	8.0	5.0		V
			V_{CC} = 15V	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	I_{OUT} = −200 μA, V_{OH} = V_{CC} −1.2V	V_{CC} = 5V		2.5	1.5	V
			V_{CC} = 10V		5.0	2.0	V
			V_{CC} = 15V		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 15V, V_{STROBE} = 0V, (Note 4)		−5	−20	−40	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	C_L = 50 pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	C_L = 50 pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	C_L = 50 pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	C_L = 50 pF		100	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C20 and across the 0°C to +70°C range for the DS88C20. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

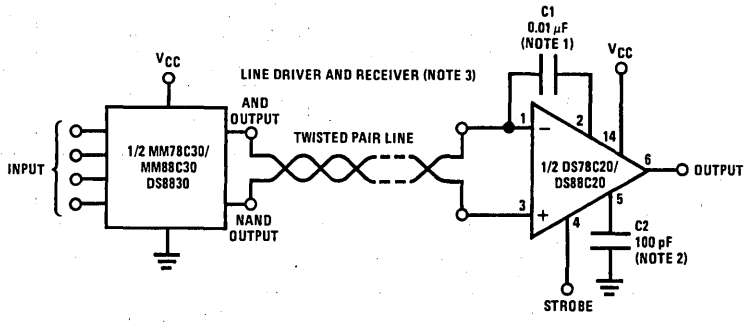
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA-RS-422 for exact conditions.

Typical Applications

RS-422/RS-423 Application



TL/F/5798–2

Note 1: (Optional internal termination resistor.)

a) Capacitor in series with internal line termination resistor, terminates the line and saves termination power. Exact value depends on line length.

b) Pin 1 connected to pin 2; terminates the line.

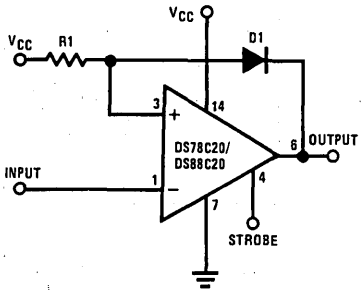
c) Pin 2 open; no internal line termination.

d) Transmission line may be terminated elsewhere or not at all.

Note 2: Optional to control response time.

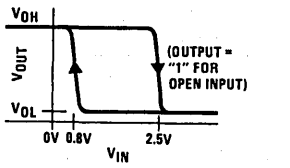
Note 3: V_{CC} 4.5V to 15V for the DS78C20. For further information on line drivers and line receivers, refer to applicaton notes AN-22, AN-83 and AN-108.

RS-232-C Application with Hysteresis



TL/F/5798–3

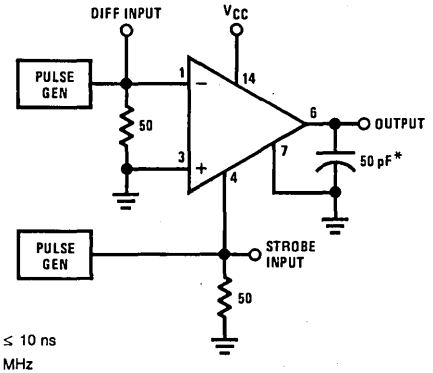
V_{CC}	R1 ±5%
5V	4,3 kΩ
10V	15 kΩ
15V	24 kΩ



TL/F/5798–4

For signals which require fail-safe or have slow rise and fall times, use R1 and D1 as shown above. Otherwise, the positive input (pin 3 or 11) may be connected to ground.

AC Test Circuit

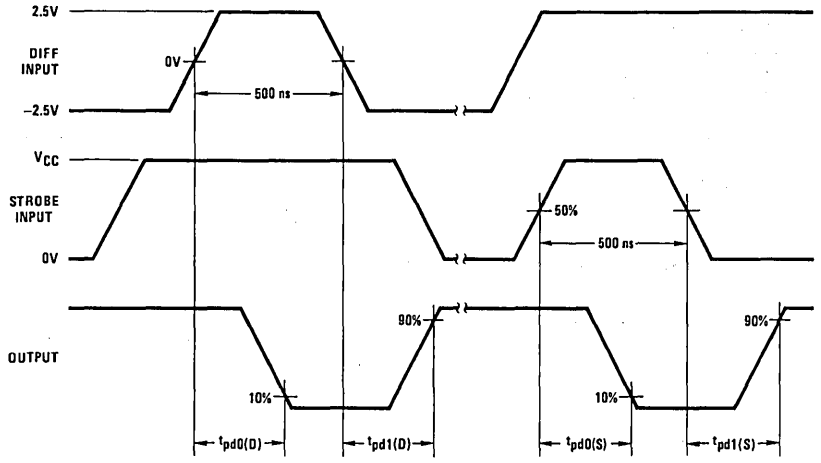


$t_r = t_f = \leq 10$ ns
PRR = 1 MHz

TL/F/5798–5

*Includes probe and jig capacitance

Switching Time Waveforms



TL/F/5798–6

National Semiconductor

DS78C120/DS88C120 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C120 and DS88C120 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

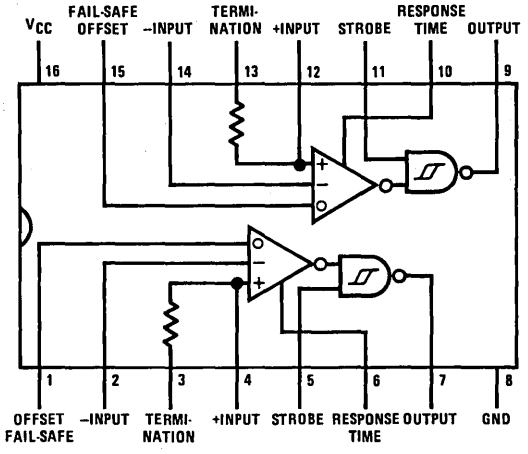
Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes a 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78C120 is specified over a −55°C to +125°C temperature range and the DS88C120 from 0°C to +70°C.

Features

- Full compatibility with EIA Standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



TL/F/5801–1

Top View

Order Number DS88C120N
See NS Package Number N16A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS78C120J/883
See NS Package Number J16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	18V
Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C120	−55	+125	°C
DS88C120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	$I_{OUT} = 1.6\ mA, V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
V_{TH}	Differential Threshold Voltage Fail-Safe	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.47	0.7	V
V_{TL}	Offset = 5V	$I_{OUT} = 1.6\ mA, V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$	0.2	0.42		V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V, 0V \leq V_{CC} \leq 15V$		4	5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
R_O	Offset Control Resistance	$T_A = 25°C$			56		kΩ
I_{IND}	Data Input Current (Unterminated)	$0V \leq V_{CC} \leq 15V$	$V_{CM} = 10V$		2	3.1	mA
			$V_{CM} = 0V$		0	−0.5	mA
			$V_{CM} = -10V$		−2	−3.1	mA
V_{THB}	Input Balance (Note 5)	$I_{OUT} = 200\ \mu A, V_{OUT} \geq V_{CC} - 1.2V, R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 1.6\ mA, V_{OUT} \leq 0.5V$ $R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -200\ \mu A, V_{DIFF} = 1V$		$V_{CC} - 1.2$	$V_{CC} - 0.75$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 1.6\ mA, V_{DIFF} = -1V$			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, $V_{DIFF} = -0.5V$ (Both Receivers)	$V_{CC} = 5.5V$		8	15	mA
			$V_{CC} = 15V$		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 15V, V_{DIFF} = 3V$			15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V, V_{DIFF} = -3V$			−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \leq 0.5V, I_{OUT} = 1.6\ mA$	$V_{CC} = 5V$	3.5	2.5		V
			$V_{CC} = 10V$	8.0	5.0		V
			$V_{CC} = 15V$	12.5	7.5		V

Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Logical "0" Strobe Input Voltage	V_{OH} V_{CC} − 1.2V, I_{OUT} = −200 μA	V_{CC} = 5V		2.5	1.5	V
			V_{CC} = 10V		5.0	2.0	V
			V_{CC} = 15V		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 15V, V_{STROBE} = 0V, (Note 4)		−5	−20	−40	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C120 and across the 0°C to +70°C range for the DS88C120. All typical values for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

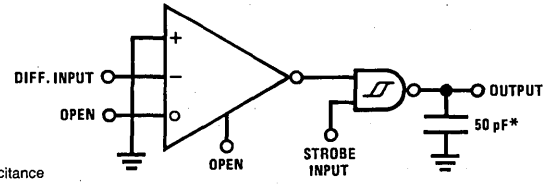
Note 5: Refer to EIA-RS422 for exact conditions.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	C_L = 50 pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	C_L = 50 pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	C_L = 50 pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	C_L = 50 pF		100	150	ns

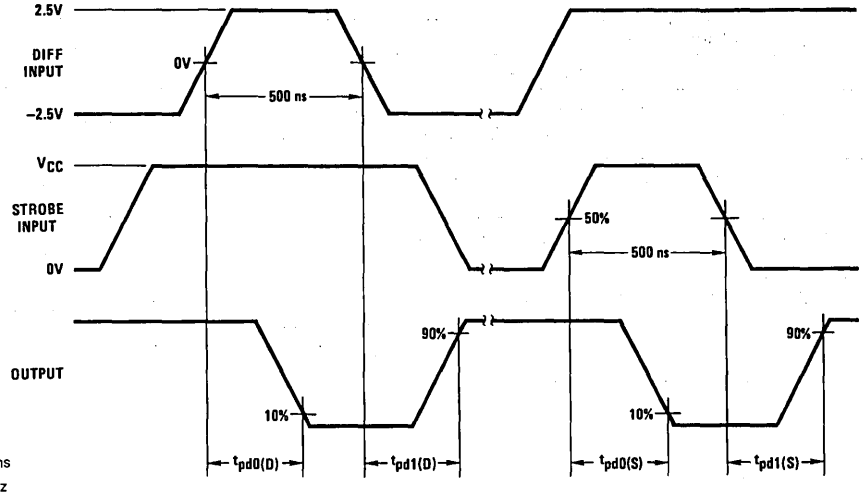
AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



*Includes probe and test fixture capacitance

TL/F/5801–3



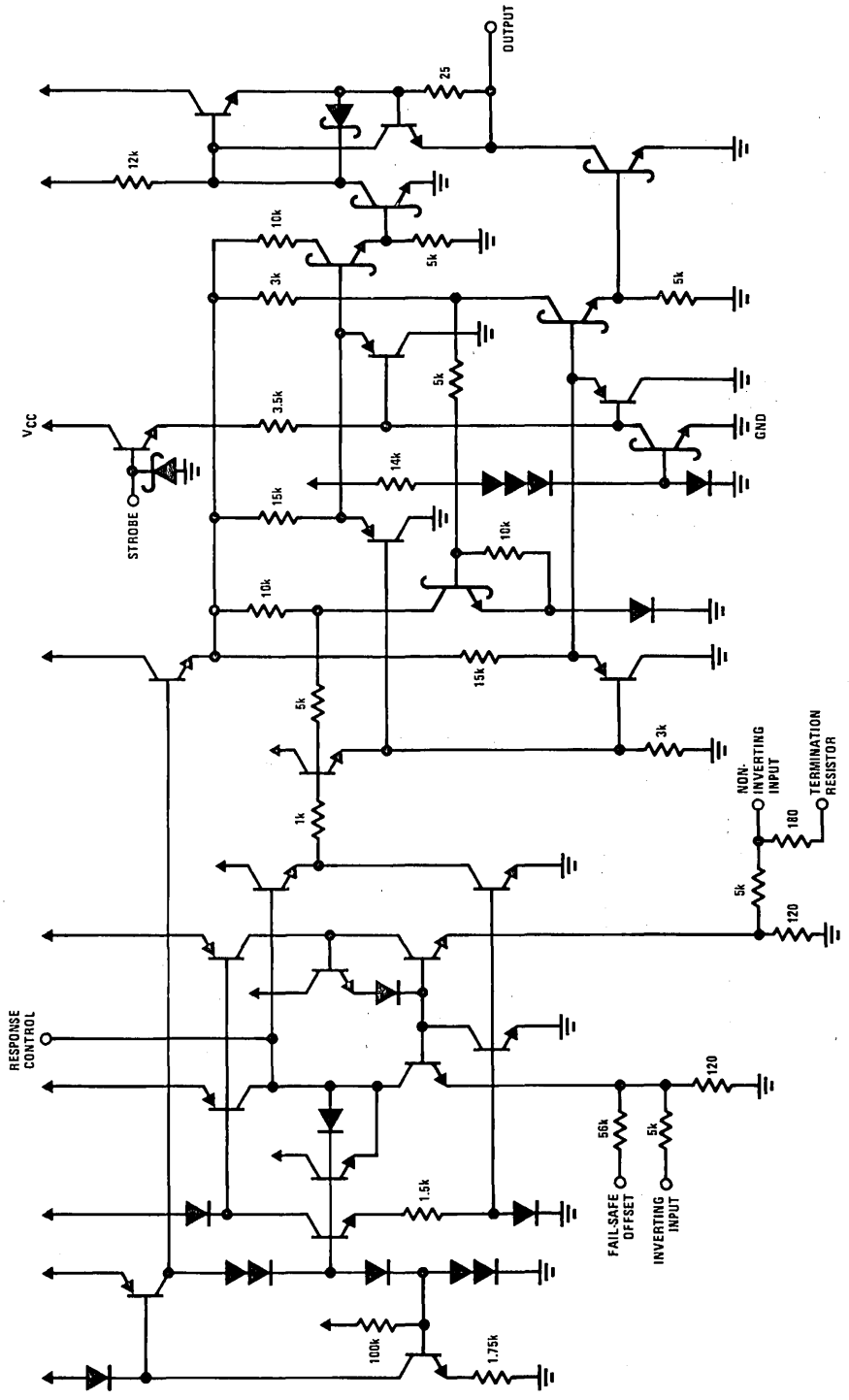
$t_r = t_f \leq 10$ ns

PRR = 1 MHz

TL/F/5801–4

Note: Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection).

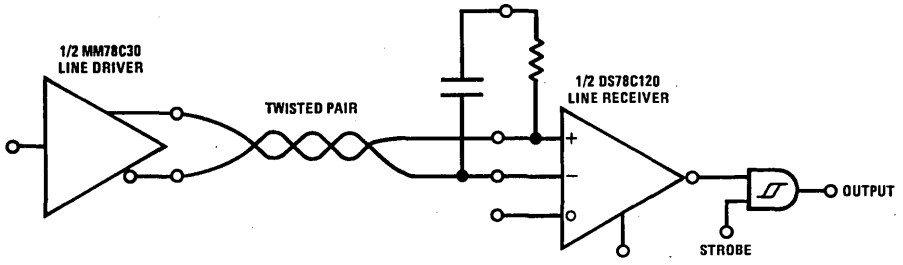
Schematic Diagram (½ Circuit Shown)



2

Application Hints

Balanced Data Transmission



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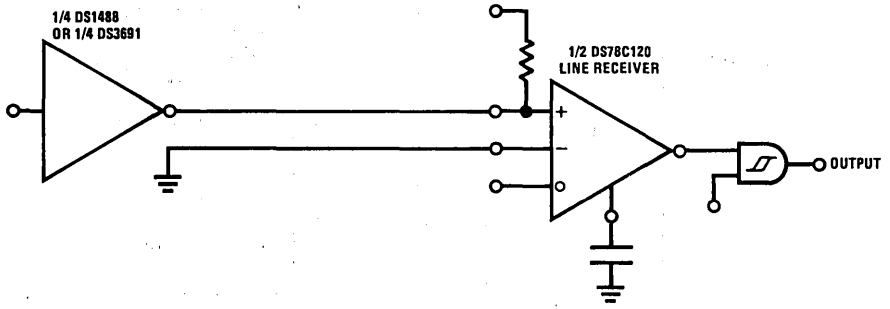
Unbalanced Data Transmission



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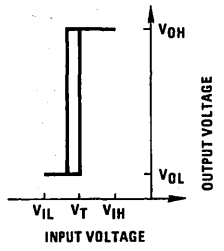
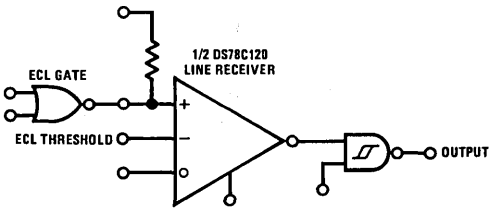
Logic Level Translator



TL/F/5801–7



TL/F/5801–8

The DS78C120/DS88C120 may be used as a level transistor to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

Application Hints (Continued)

LINE DRIVERS

Line drivers which will interface with the DS78C120/DS88C120 are listed below.

Balanced Drivers

DS26LS31	Quad RS-422 Line Driver
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE® TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691A, DS3691	Quad RS-423/Dual RS-422 TTL
DS1692, DS3692	Quad RS-423/Dual TRI-STATE RS-422 TTL
DS3587, DS3487	Quad TRI-STATE RS-422

Unbalanced Drivers

DS1488	Quad RS-232
DS14C88	Quad RS-232
DS75150	Dual RS-232

RESPONSE CONTROL AND HYSTERESIS

In unbalanced (RS-232/RS-423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78C120/DS88C120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78C120/DS88C120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1* and *2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/cross-talk. A 180Ω termination resistor is provided in the DS78C120/DS88C120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns) the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108.

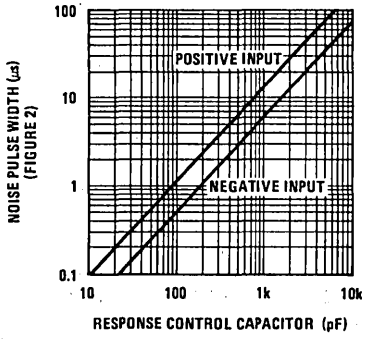


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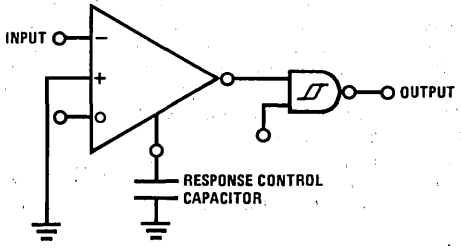
FIGURE 1. Noise Pulse Width vs Response Control Capacitor



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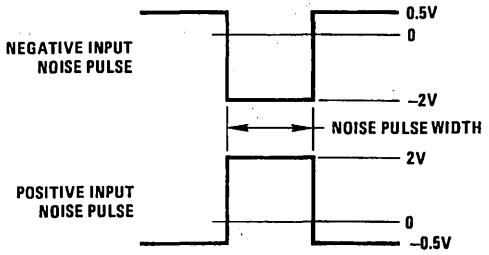


TL/F/5801–11

FIGURE 2

Application Hints (Continued)

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or shorted. To facilitate the detection of input opens or shorts, the DS78C120/DS88C120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or shorted, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ + 0.45V or $V_{IN(INVERTING)}$ + 0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS-423) or for balanced interface (RS-422) operation.

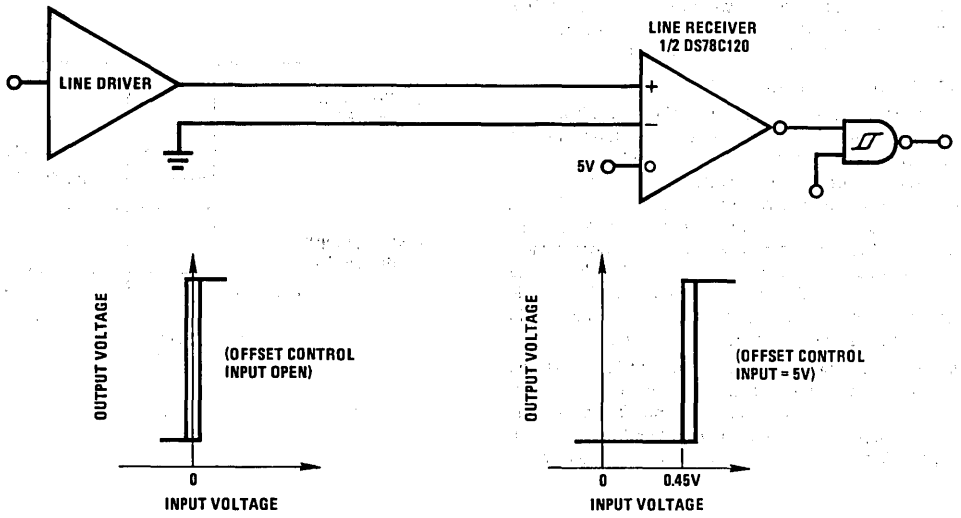
For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or shorted.

For balanced operation with inputs shorted or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of the NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

In a communications system, only the control signals are required to detect input fault condition. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths

Unbalanced RS-423 and RS-232 Fail-Safe



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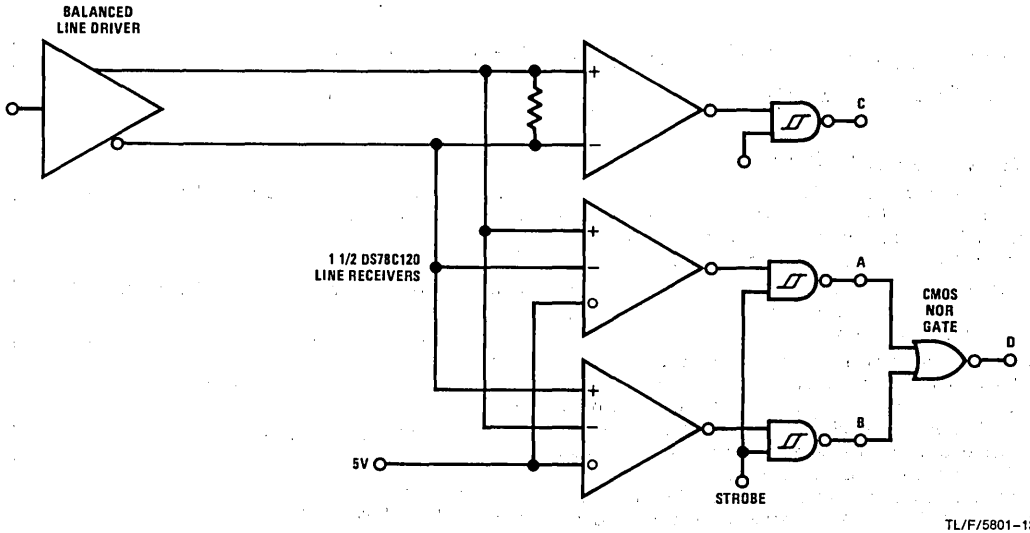
Application Hints (Continued)

Balanced RS-422 Fail-Safe



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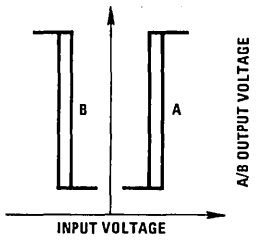

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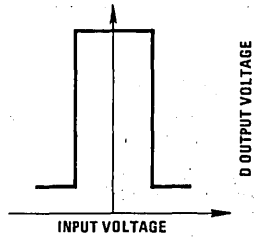

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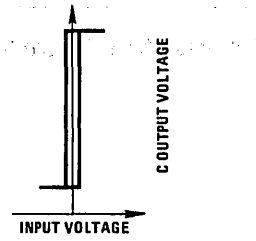

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Truth Table (For Balanced Fail-Safe)

Input	Strobe	A-OUT	B-OUT	C-OUT	D-OUT
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

National Semiconductor

DS78LS120/DS88LS120 Dual Differential Line Receiver (Noise Filtering and Fail-Safe)

General Description

The DS78LS120 and DS88LS120 are high performance, dual differential, TTL compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes an optional 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78LS120 is specified over a −55°C to +125°C temperature range and the DS88LS120 from 0°C to +70°C.

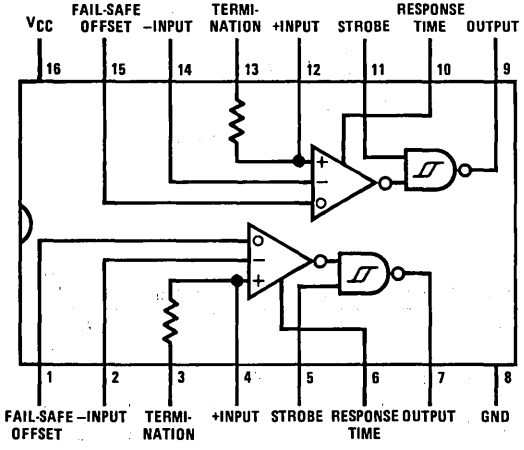
Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

Features

- Meets EIA standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 5k typical input impedance
- Optional 180Ω termination resistor
- 50 mV input hysteresis
- 200 mV input threshold
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS88LS120N or DS88LS120M
See NS Package Number M16A or N16A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS78LS120J/883 or DS78LS120W/883
See NS Package Number J16A or W16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	±25V
Strobe Voltage	7V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mV
Molded Package	1362 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS78LS120	−55	+125	°C
DS88LS120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	I_{OUT} = −400 μA, $V_{OUT} \geq$ 2.5V	−7V ≤ V_{CM} ≤ 7V		0.06	0.2	V
			−15 ≤ V_{CM} ≤15V		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	I_{OUT} = 4 mA, $V_{OUT} \leq$ 0.5V	−7V ≤ V_{CM} ≤7V		−0.08	−0.2	V
			−15V ≤ V_{CM} ≤ 15V		−0.08	−0.3	V
V_{TH} V_{TL}	Differential Threshold Voltage with Fail-Safe Offset = 5V	I_{OUT} = −400 μA, $V_{OUT} \geq$ 2.5V	−7V ≤ V_{CM} ≤ 7V		0.47	0.7	V
		I_{OUT} = 4 mA, $V_{OUT} \leq$ 0.5V	−7V ≤ V_{CM} ≤ 7V	−0.2	−0.42		V
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ 15V, 0V ≤ V_{CC} ≤ 7V		4	5		kΩ
R_T	Line Termination Resistance	T_A = 25°C		100	180	300	Ω
R_O	Offset Control Resistance	T_A = 25°C		42	56	70	kΩ
I_{IND}	Data Input Current (Unterminated)	V_{CM} = 10V	0V ≤ V_{CC} ≤ 7V		2	3.1	mA
		V_{CM} = 0V			0	−0.5	mA
		V_{CM} = −10V			−2	−3.1	mA
V_{THB}	Input Balance (Note 5)	I_{OUT} = −400 μA, $V_{OUT} \geq$ 2.5V, R_S = 500Ω	−7V ≤ V_{CM} 7V		0.1	0.4	V
		I_{OUT} = 4 mA, $V_{OUT} \leq$ 0.5V, R_S = 500Ω	−7V ≤ V_{CM} ≤ 7V		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −400 μA, V_{DIFF} = 1V, V_{CC} = 4.5V		2.5	3		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 4 mA, V_{DIFF} = −1V, V_{CC} = 4.5V			0.35	0.5	V
I_{CC}	Power Supply Current	V_{CC} = 5.5V, V_{DIFF} = −0.5V, (Both Receivers)	V_{CM} = 15V		10	16	mA
			V_{CM} = −15V		10	16	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	V_{STROBE} = 5.5V, V_{DIFF} = 3V			1	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	V_{STROBE} = 0V, V_{DIFF} = −3V			−290	−400	μA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \leq$ 0.5, I_{OUT} = 4mA		2.0	1.12		V
V_{IL}	Logical "0" Strobe Input Voltage	$V_{OH} \geq$ 2.5V, I_{OUT}, = −400 μA			1.12	0.8	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 5.5V, V_{STROBE} = 0V, (Note 4)		−30	−100	−170	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78LS120 and across the 0°C to +70°C for the DS88LS120. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

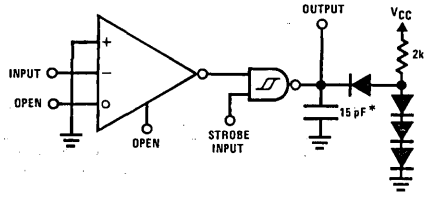
Note 5: Refer to EIA-RS422 for exact conditions.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	Response Pin Open, C_L = 15 pF, R_L = 2 kΩ		38	60	ns
$t_{pd1(D)}$	Differential Input to "1" Output			38	60	ns
$t_{pd0(S)}$	Strobe Input to "0" Output			16	25	ns
$t_{pd1(S)}$	Strobe Input to "1" Output			12	25	ns

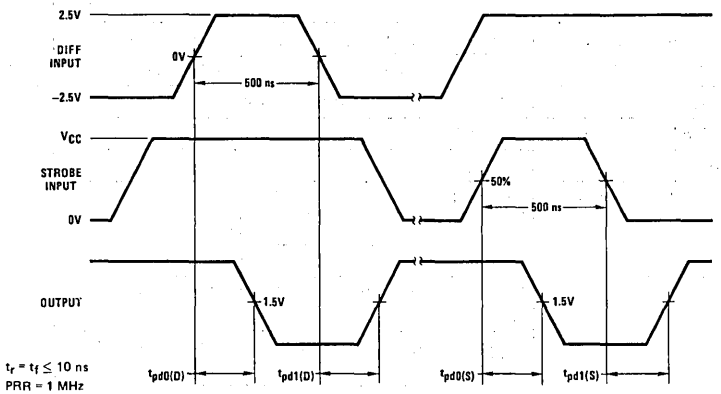
AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



TL/F/7499-3

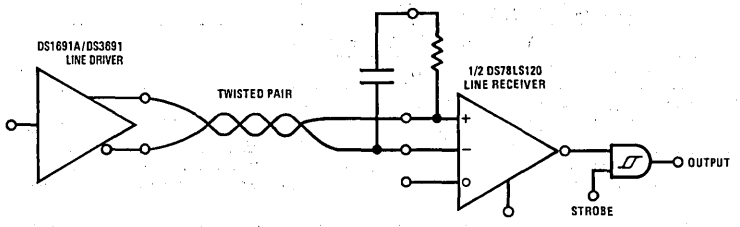
*Includes probe and test fixture capacitance



Note: Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection). TL/F/7499-4

Application Hints

Balanced Data Transmission



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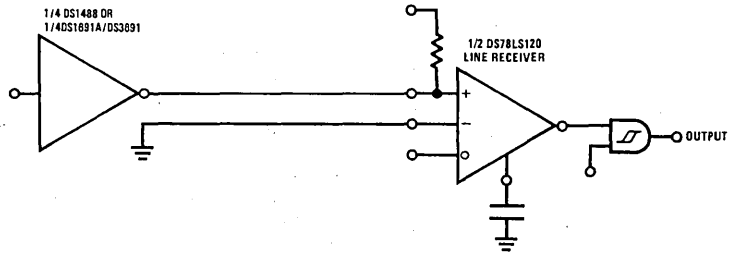
Application Hints (Continued)

Unbalanced Data Transmission



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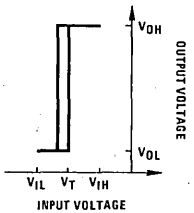
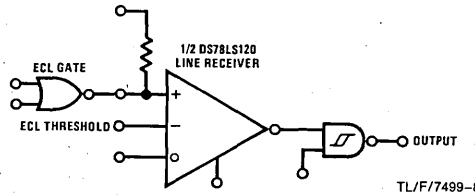


TL/F/7499-7

Logic Level Translator



TL/F/7499-8

The DS78LS120/DS88LS120 may be used as a level translator to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

LINE DRIVERS

Line drivers which will interface with the DS78LS120/DS88LS120 are listed below.

Balanced Drivers

DS26LS31	Quad RS-422 Line Driver Dual CMOS
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691A, DS3691	Quad RS-423/Dual RS-422 TTL
DS1692, DS3692	Quad RS-423/Dual TRI-STATE RS-422 TTL
DS3487	Quad TRI-STATE RS-422

Unbalanced Drivers

DS1488	Quad RS-232
DS75150	Dual RS-232

RESPONSE CONTROL AND HYSTERESIS

In unbalanced (RS-232/RS-423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78LS120/DS88LS120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78LS120/DS88LS120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1* and *2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

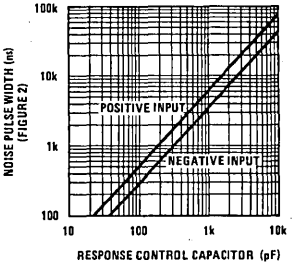


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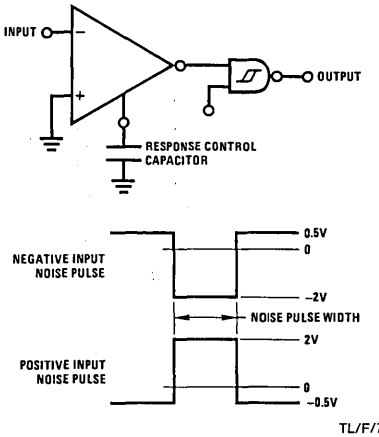
FIGURE 1. Noise Pulse Width vs Response Control Capacitor



TL/F/7499-10

FIGURE 2

Application Hints (Continued)

TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/crosstalk. A 180Ω termination resistor is provided in the DS78LS120/DS88LS120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns), and the termination resistor value is 180Ω, the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108.

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or shorted. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or shorted, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

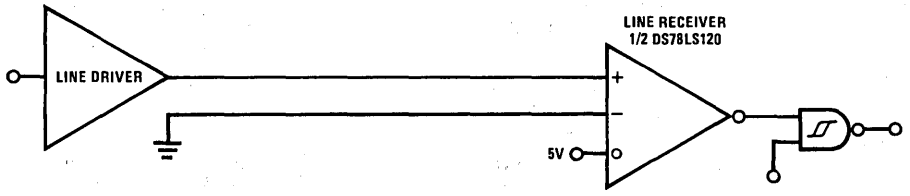
The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ +0.45V or $V_{IN(INVERTING)}$ +0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS-423) or for balanced interface (RS-422) operation.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the fail-safe offset pin to 5V, offsets the receiver threshold to 0.45V. The output is forced to a logic zero state if the input is open or shorted.

Unbalanced RS-423 and RS-232 Fail-Safe



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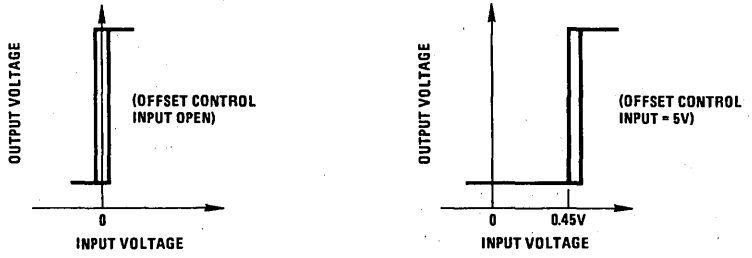

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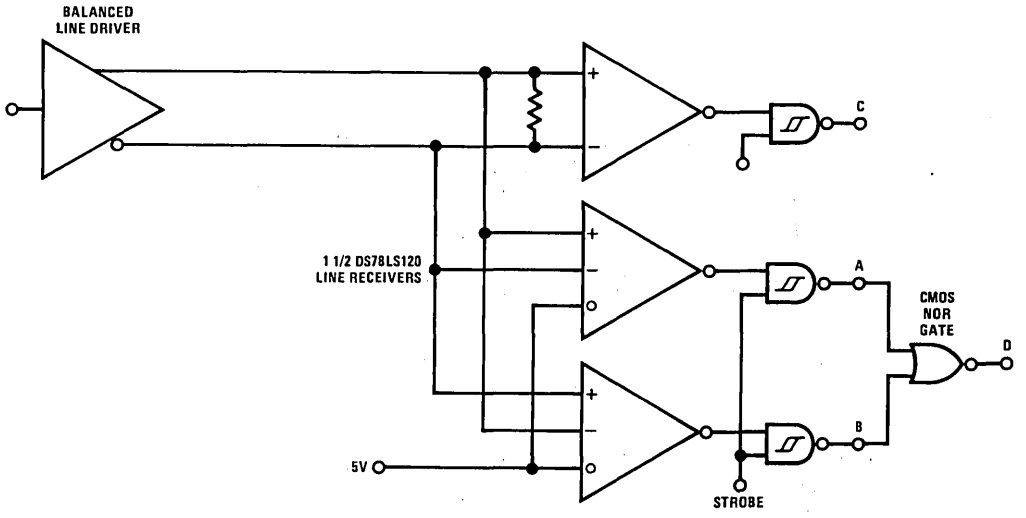
Application Hints (Continued)

Balanced RS-422 Fail-Safe



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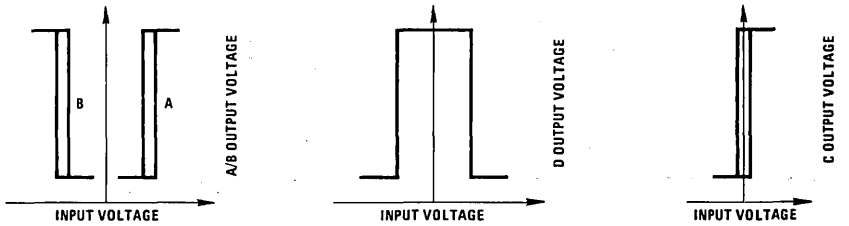


TL/F/7499–14

For balanced operation with inputs open or shorted, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the open or short condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

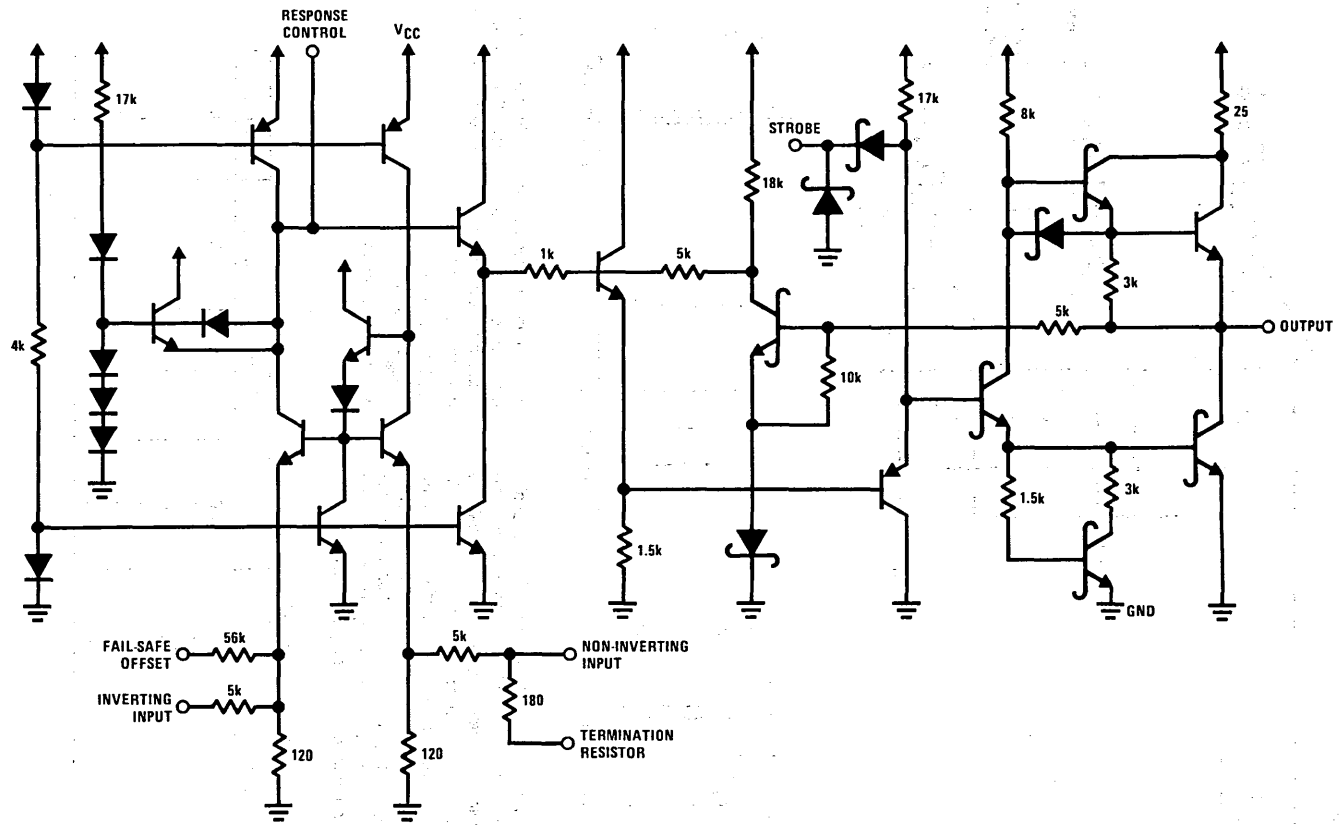
In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths

Truth Table (For Balanced Fail-Safe)

Input	Strobe	A-Out	B-Out	C-Out	D-Out
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

Schematic Diagram



TL/F/7499–2

National Semiconductor

DS8921/DS8921A/DS8921AT
Differential Line Driver and Receiver Pair

General Description

The DS8921, DS8921A are Differential Line Driver and Receiver pairs designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, these devices meet the requirements of the EIA Standard RS-422.

The DS8921, DS8921A receivers offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms.

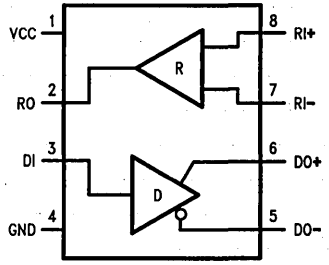
The DS8921, DS8921A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

The DS8921, DS8921A are designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew - 0.5 ns typical
- Meet the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input hysteresis-70 mV typical
- DS8921AT industrial temperature operation (−40°C to +85°C)

Connection Diagram



TL/F/8512–1

Order Number DS8921M, DS8921N, DS8921AM, DS8921AN, DS8921ATM, DS8921ATN or DS8921ATJ
See NS Package Number J08A, M08A or N08E

Truth Table

Receiver		Driver		
Input	V_{OUT}	Input	V_{OUT}	$\overline{V_{OUT}}$
$V_{ID} \geq V_{TH}$ (MAX)	1	1	1	0
$V_{ID} \leq V_{TH}$ (MIN)	0	0	0	1
Open	1			

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Driver Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V
Maximum Package Power Dissipation @ +25°C	
J Package	1220 mW
M Package	730 mW
N Package	1160 mW
Derate J Package	9.8 mW/°C above +25°C
Derate M Package	9.3 mW/°C above +25°C
Derate N Package	5.8 mW/°C above +25°C
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Maximum Junction Temperature	+150°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)			
DS8921/DS8921A	0	70	°C
DS8921AT	−40	+85	°C

DS8921/DS8921A Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Conditions	Min	Typ	Max	Units
RECEIVER					
V_{TH}	$-7V \le V_{CM} \le +7V$	−200	±35	+200	mV
V_{HYST}	$-7V \le V_{CM} \le +7V$	15	70		mV
R_{IN}	$V_{IN} = -7V, +7V$ (Other Input = GND)	4.0	6.0		kΩ
I_{IN}	$V_{IN} = 10V$			3.25	mA
	$V_{IN} = -10V$			−3.25	mA
V_{OH}	$I_{OH} = -400\ \mu A$	2.5			V
V_{OL}	$I_{OL} = 8$ mA			0.5	V
I_{SC}	V_{CC} = MAX, $V_{OUT} = 0V$	−15		−100	mA
DRIVER					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC} = MAX, $V_{IN} = 0.4V$		−40	−200	μA
I_{IH}	V_{CC} = MAX, $V_{IN} = 2.7V$			20	μA
I_I	V_{CC} = MAX, $V_{IN} = 7.0V$			100	μA
V_{CL}	V_{CC} = MIN, $I_{IN} = -18$ mA			−1.5	V
V_{OH}	V_{CC} = MIN, $I_{OH} = -20$ mA	2.5			V
V_{OL}	V_{CC} = MIN, $I_{OL} = +20$ mA			0.5	V
I_{OFF}	$V_{CC} = 0V$, $V_{OUT} = 5.5V$			100	μA
$\lvert V_T\rvert - \lvert\overline{VT}\rvert$				0.4	V
V_T		2.0			V
$\lvert V_{OS} - \overline{V_{OS}}\rvert$				0.4	V
I_{SC}	V_{CC} = MAX, $V_{OUT} = 0V$	−30		−150	mA
DRIVER and RECEIVER					
I_{CC}	V_{CC} = MAX, V_{OUT} = Logic 0			35	mA

Receiver Switching Characteristics (*Figures 1* and *2*)

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
T_{pLH}	C_L = 30 pF *(Figures 1, 2)*		14	22.5	20	20	ns
T_{pHL}	C_L = 30 pF *(Figures 1, 2)*		14	22.5	20	20	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	C_L = 30 pF *(Figures 1, 2)*		0.5	5	3.5	5	ns

Driver Switching Characteristics (*Figures 3* and *4*)

SINGLE ENDED CHARACTERISTICS

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
T_{pLH}	C_L = 30 pF *(Figures 3, 4)*		10	15	15	15	ns
T_{pHL}	C_L = 30 pF *(Figures 3, 4)*		10	15	15	15	ns
T_{TLH}	C_L = 30 pF *(Figures 7, 8)*		5	8	8	9.5	ns
T_{THL}	C_L = 30 pF *(Figures 7, 8)*		5	8	8	9.5	ns
Skew	CL = 30 pF *(Figures 3, 4)*		1	5	3.5	3.5	ns

Driver Switching Characteristics (*Figures 3* and *5*)

DIFFERENTIAL CHARACTERISTICS (Note 6)

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
T_{pLH}	C_L = 30 pF *(Figures 3, 5, 6)*		10	15	15	15	ns
T_{pHL}	C_L = 30 pF *(Figures 3, 5, 6)*		10	15	15	15	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	C_L = 30 pF *(Figures 3, 5, 6)*		0.5	6	2.75	2.75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.

Note 3: All typical values are V_{CC} = 5V, T_A = 25°C.

Note 4: Only one output at a time should be shorted.

Note 5: Difference between complementary outputs at the 50% point.

Note 6: Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE).

The calculated ATE results assume a linear transition between measurement points and are a result of the following equations:

$$T_{cr} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$$

Where: T_{cr} = Crossing Point

T_{ra}, T_{rb}, T_{fa} and T_{fb} are time measurements with respect to the input. See *Figure 6*.

AC Test Circuits and Switching Diagrams

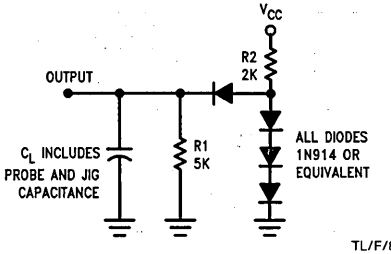


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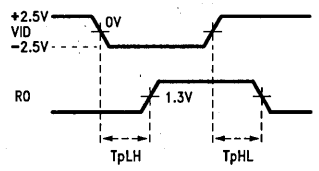
FIGURE 1



TL/F/8512-4

FIGURE 2

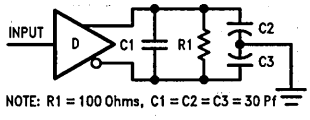


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FIGURE 3

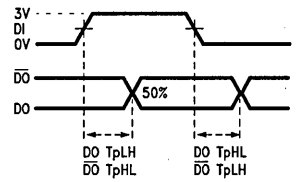

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FIGURE 4

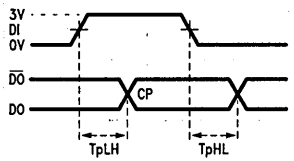

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FIGURE 5

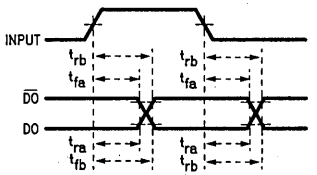

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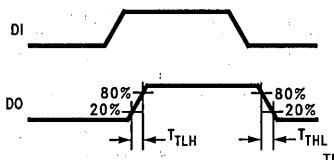
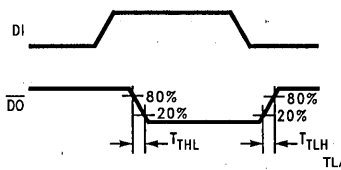
FIGURE 6



TL/F/8512-10

FIGURE 7

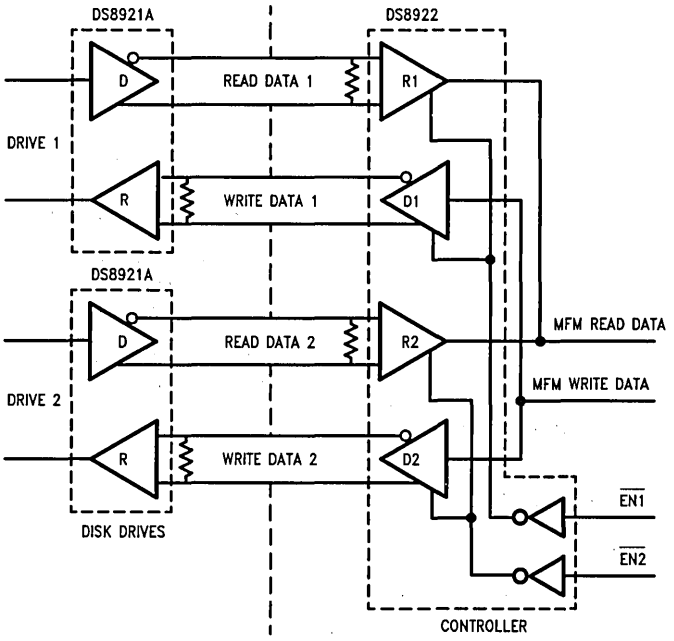


TL/F/8512-11

FIGURE 8

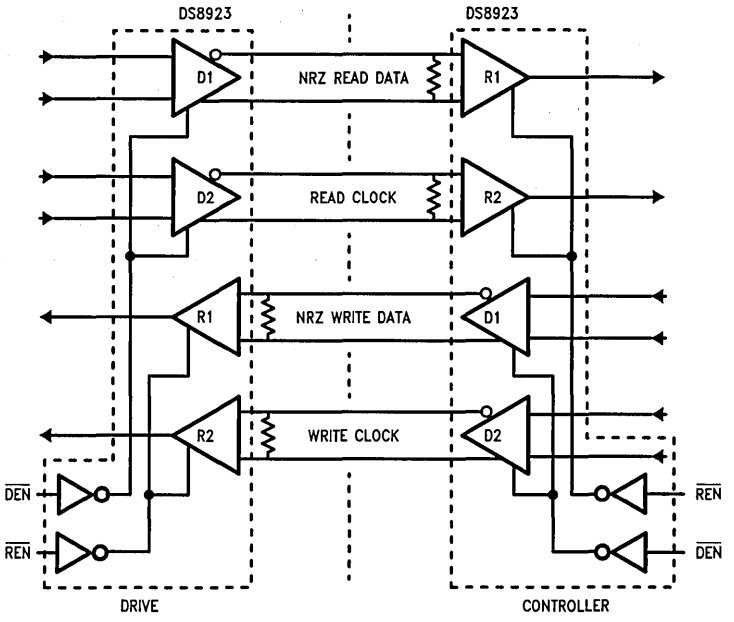
Typical Applications

ST506 and ST412 Application



TL/F/8512–8

ESDI Application



TL/F/8512–9

National Semiconductor

DS89C21
Differential CMOS Line Driver and Receiver Pair

General Description

The DS89C21 is a differential CMOS line driver and receiver pair, designed to meet the requirements of TIA/EIA-422-A (RS-422) electrical characteristics interface standard. The DS89C21 provides one driver and one receiver in a minimum footprint. The device is offered in an 8-pin SOIC package.

The CMOS design minimizes the supply current to 6 mA, making the device ideal for use in battery powered or power conscious applications.

The driver features a fast transition time specified at 2.2 ns, and a maximum differential skew of 2 ns making the driver ideal for use in high speed applications operating above 10 MHz.

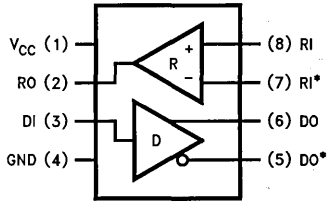
The receiver can detect signals as low as 200 mV, and also incorporates hysteresis for noise rejection. Skew is specified at 4 ns maximum.

The DS89C21 is compatible with TTL and CMOS levels (DI and RO).

Features

- Meets TIA/EIA-422-A (RS-422) and CCITT V.11 recommendation
- LOW POWER design—15 mW typical
- Guaranteed AC parameters:
  - — Maximum driver skew 2.0 ns
  - — Maximum receiver skew 4.0 ns
- Extended temperature range −40°C to +85°C
- Available in SOIC packaging
- Operates over 20 Mbps
- Receiver OPEN input failsafe feature

Connnection Diagram



TL/F/11753–1

Order Number DS89C21TM or DS89C21TN
See NS Package Number M08A or N08E

Truth Tables

Driver

Input	Outputs	
DI	**DO**	**DO***
H	H	L
L	L	H

Receiver

Inputs	Output
RI–RI*	**RO**
$V_{DIFF} \geq +200$ mV	H
$V_{DIFF} \leq -200$ mV	L
OPEN†	H

†Non-terminated

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Driver Input Voltage (DI)	−1.5V to V_{CC} + 1.5V
Driver Output Voltage (DO, DO*)	−0.5V to +7V
Receiver Input Voltage—V_{CM} (RI, RI*)	±14V
Differential Receiver Input Voltage—V_{DIFF} (RI, RI*)	±14V
Receiver Output Voltage (RO)	−0.5V to V_{CC} +0.5V
Receiver Output Current (RO)	±25 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering 4 sec.)	+260°C
Maximum Junction Temperature	150°C
Maximum Package Power Dissipation @ +25°C	
M Package	714 mW
N Package	1275 mW
Derate M Package	5.7 mW/°C above +25°C
Derate N Package	10.2 mW/°C above +25°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature (T_A)	−40	+85	°C
Input Rise or Fall Time (DI)		500	ns

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS								
V_{IH}	Input Voltage HIGH			DI	2.0		V_{CC}	V
V_{IL}	Input Voltage LOW				GND		0.8	V
I_{IH}, I_{IL}	Input Current	V_{IN} = V_{CC}, GND, 2.0V, 0.8V				0.05	±10	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA					−1.5	V
V_{OD1}	Unloaded Output Voltage	No Load		DO, DO*		4.2	6.0	V
V_{OD2}	Differential Output Voltage	R_L = 100Ω			2.0	3.0		V
ΔV_{OD2}	Change in Magnitude of V_{OD2} for Complementary Output States					5.0	400	mV
V_{OD3}	Differential Output Voltage	R_L = 150Ω			2.1	3.1		V
V_{OD4}	Differential Output Voltage	R_L = 3.9 kΩ				4.0	6.0	V
V_{OC}	Common Mode Voltage	R_L = 100Ω				2.0	3.0	V
ΔV_{OC}	Change in Magnitude of V_{OC} for Complementary Output States					2.0	400	mV
I_{OSD}	Output Short Circuit Current	V_{OUT} = 0V			−30	−115	−150	mA
I_{OFF}	Output Leakage Current	V_{CC} = 0V	V_{OUT} = +6V			0.03	+100	μA
			V_{OUT} = −0.25V			−0.08	−100	μA

2

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 3) (Continued)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TL}, V_{TH}	Differential Thresholds	V_{IN} = +7V, 0V, −7V		RI, RI*	−200	±25	+200	mV
V_{HYS}	Hysteresis	V_{CM} = 0V			20	50		mV
R_{IN}	Input Impedance	V_{IN} = −7V, +7V, Other = 0V			5.0	9.5		kΩ
I_{IN}	Input Current	Other Input = 0V, V_{CC} = 5.5V and V_{CC} = 0V	V_{IN} = +10V			+1.0	+1.5	mA
			V_{IN} = +3.0V		0	+0.22		mA
			V_{IN} = +0.5V			−0.04		mA
			V_{IN} = −3V		0	−0.41		mA
			V_{IN} = −10V			−1.25	−2.5	mA
V_{OH}	Output HIGH Voltage	I_{OH} = −6 mA	V_{DIFF} = +1V	RO	3.8	4.9		V
			V_{DIFF} = OPEN		3.8	4.9		V
V_{OL}	Output LOW Voltage	I_{OL} = +6 mA, V_{DIFF} = −1V				0.08	0.3	V
I_{OSR}	Output Short Circuit Current	V_{OUT} = 0V			−25	−85	−150	mA
DRIVER AND RECEIVER CHARACTERISTICS								
I_{CC}	Supply Current	No Load	DI = V_{CC} or GND	V_{CC}		3.0	6	mA
			DI = 2.4V or 0.5V			3.8	12	mA

Switching Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
t_{PLHD}	Propagation Delay LOW to HIGH	R_L = 100Ω, C_L = 50 pF	*(Figures 2, 3)*	2	4.9	10	ns
t_{PHLD}	Propagation Delay HIGH to LOW			2	4.5	10	ns
t_{SKD}	Skew, $\lvert t_{PLHD} - t_{PHLD} \rvert$				0.4	2.0	ns
t_{TLH}	Transition Time LOW to HIGH		*(Figures 2, 4)*		2.2	9	ns
t_{THL}	Transition Time HIGH to LOW				2.1	9	ns
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	C_L = 50 pF, V_{DIFF} = 2.5V, V_{CM} = 0V	*(Figures 5, 6)*	6	18	30	ns
t_{PHL}	Propagation Delay HIGH to LOW			6	17.5	30	ns
t_{SK}	Skew, $\lvert t_{PLH} - t_{PHL} \rvert$				0.5	4.0	ns
t_r	Rise Time		*(Figure 7)*		2.5	9	ns
t_f	Fall Time				2.1	9	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

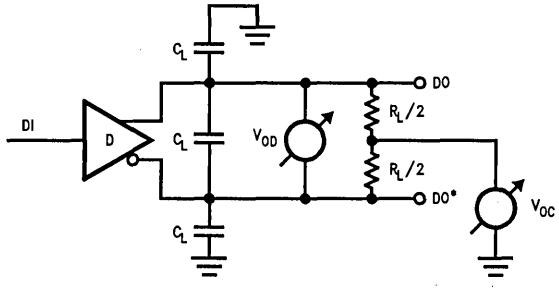
Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 4: f = 1 MHz, t_r and t_f ≤ 6 ns.

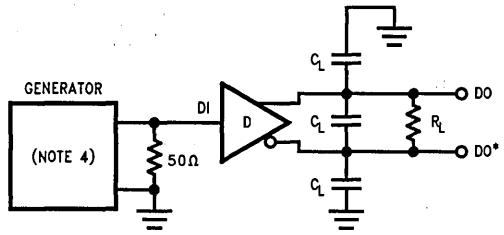
Note 5: ESD Rating: HBM (1.5 kΩ, 100 pF) all pins ≥ 2000V.
EIAJ (0Ω, 200 pF) ≥ 250V

Parameter Measurement Information



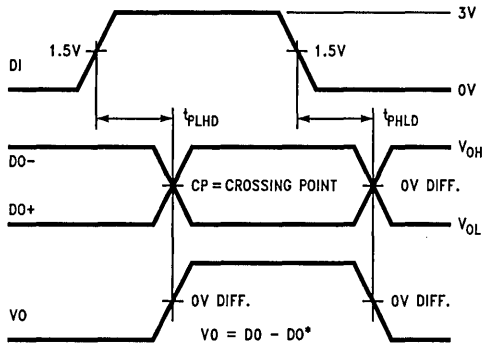
TL/F/11753-2

FIGURE 1. V_{OD} and V_{OC} Test Circuit



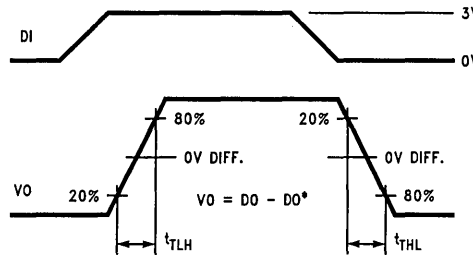
TL/F/11753-3

FIGURE 2. Driver Propagation Delay Test Circuit



TL/F/11753-4

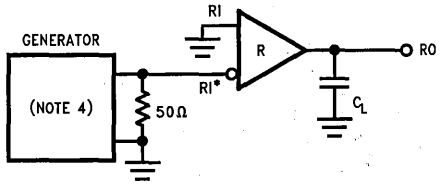
FIGURE 3. Driver Differential Propagation Delay Timing



TL/F/11753-5

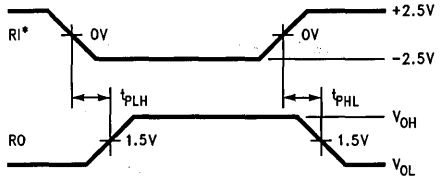
FIGURE 4. Driver Differential Transition Timing

Parameter Measurement Information (Continued)



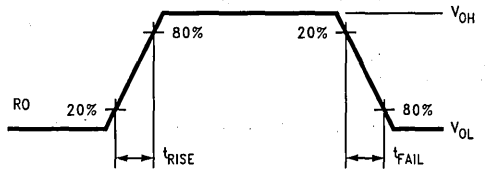
TL/F/11753–6

FIGURE 5. Receiver Propagation Delay Test Circuit



TL/F/11753–7

FIGURE 6. Receiver Propagation Delay Timing



TL/F/11753–8

FIGURE 7. Receiver Rise and Fall Times

National Semiconductor

DS8922/DS8922A/DS8923/DS8923A TRI-STATE® RS-422 Dual Differential Line Driver and Receiver Pairs

General Description

The DS8922/22A and DS8923/23A are Dual Differential Line Driver and Receiver pairs. These devices are designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, the devices meet the requirements of the EIA Standard RS-422.

These devices offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms. An input fail-safe circuit is provided such that if the receiver inputs are open the output assumes the logical one state.

The DS8922A and DS8923A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

Both devices feature TRI-STATE outputs. The DS8922/22A have independent control functions common to a driver and receiver pair. The DS8923/23A have separate driver and receiver control functions.

Power up/down circuitry is featured which will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or power down operation.

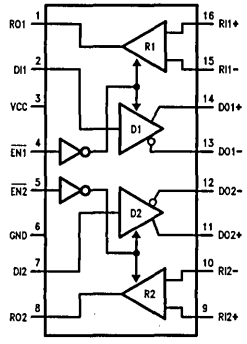
The DS8922/22A and DS8923/23A are designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew—±0.5 ns typical
- Meets the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input fail-safe circuitry
- Receiver input hysteresis—70 mV typical
- Glitch free power up/down
- TRI-STATE outputs

Connection Diagrams

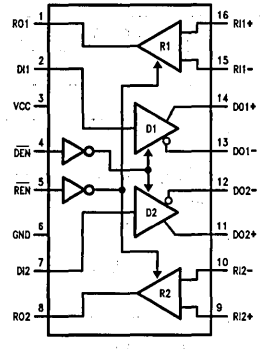
DS8922A Dual-In-Line



TL/F/8511–1

Order Number DS8922M, DS8922N, DS8922AM or DS8922AN
See NS Package Number M16A or N16A

DS8923A Dual-In-Line



TL/F/8511–2

Order Number DS8923M, DS8923N, DS8923AM or DS8923AN
See NS Package Number M16A or N16A

Truth Tables

DS8922/22A

$\overline{EN1}$	$\overline{EN2}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	HI-Z	ACTIVE	HI-Z	ACTIVE
0	1	ACTIVE	HI-Z	ACTIVE	HI-Z
1	1	HI-Z	HI-Z	HI-Z	HI-Z

DS8923/23A

$\overline{DEN}$	$\overline{REN}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	ACTIVE	ACTIVE	HI-Z	HI-Z
0	1	HI-Z	HI-Z	ACTIVE	ACTIVE
1	1	HI-Z	HI-Z	HI-Z	HI-Z

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Drive Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V

Maximum Package Power Dissapation @ +25°C	
M Package	1300 mW
N Package	1450 mW
Derate M Package 10.4 mW/°C above +25°C	
Derate N Package 11.6 mW/°C above +25°C	
Storage Temperature Range	−65°C to +165°C
Lead Temp. (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)	0	70	°C

DS8922/22A and DS8923/23A Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Conditions		Min	Typ	Max	Units
RECEIVER						
V_{TH}	$-7V \le V_{CM} \le +7V$		−200	±35	+200	mV
V_{HYST}	$-7V \le V_{CM} \le +7V$		15	70		mV
R_{IN}	V_{IN} = −7V, +7V (Other Input = GND)		4.0	6.0		kΩ
I_{IN}	V_{IN} = 10V				3.25	mA
	V_{IN} = −10V				−3.25	mA
V_{OH}	V_{CC} = MIN, I_{OH} = −400 μA		2.5			V
V_{OL}	V_{CC} = MAX, I_{OL} = 8 mA				0.5	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V		−15		−100	mA
DRIVER						
V_{OH}	V_{CC} = MIN, I_{OH} = −20 mA		2.5			V
V_{OL}	V_{CC} = MIN, I_{OL} = +20 mA				0.5	V
I_{OFF}	V_{CC} = 0V, V_{OUT} = 5.5V				100	μA
$\lvert VT\rvert - \lvert\overline{VT}\rvert$					0.4	V
VT			2.0			V
$\lvert V_{OS} - \overline{V_{OS}}\rvert$					0.4	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V		−30		−150	mA
DRIVER and RECEIVER						
I_{OZ} TRI-STATE Leakage	V_{CC} = MAX	V_{OUT} = 2.5V			50	μA
		V_{OUT} = 0.4V			−50	μA
I_{CC}	V_{CC} = MAX	ACTIVE			76	mA
		TRI-STATE			78	mA
DRIVER and ENABLE INPUTS						
V_{IH}			2.0			V
V_{IL}					0.8	V
I_{IL}	V_{CC} = MAX, V_{IN} = 0.4V			−40	−200	μA
I_{IH}	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	V_{CC} = MAX, V_{IN} = 7.0V				100	μA
V_{CL}	V_{CC} = MIN, I_{IN} = −18 mA				−1.5	V

Receiver Switching Characteristics (*Figures 1, 2* and *3*)

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
T_{pLH}	CL = 30 pF		12	22.5	20	ns
T_{pHL}	CL = 30 pF		12	22.5	20	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5	5	3.5	ns
Skew (Channel to Channel)	CL = 30 pF		0.5	3.0	2.0	ns
T_{pLZ}	CL = 15 pF S2 Open		15			ns
T_{pHZ}	CL = 15 pF S1 Open		15			ns
T_{pZL}	CL = 30 pF S2 Open		20			ns
T_{pZH}	CL = 30 pF S1 Open		20			ns

Driver Switching Characteristics

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
SINGLE ENDED CHARACTERISTICS (*Figures 4, 5, 6* and *8*)						
T_{pLH}	CL = 30 pF		12	15	15	ns
T_{pHL}	CL = 30 pF		12	15	15	ns
T_{TLH}	CL = 30 pF		5	10	10	ns
T_{THL}	CL = 30 pF		5	10	10	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5			ns
Skew	CL = 30 pF (Note 5)		0.5	5	3.5	ns
Skew (Channel to Channel)			0.5	3.0	2.0	ns
T_{pLZ}	CL = 30 pF		15			ns
T_{pHZ}	CL = 30 pF		15			ns
T_{pZL}	CL = 30 pF		20			ns
T_{pZH}	CL = 30 pF		20			ns
DIFFERENTIAL SWITCHING CHARACTERISTICS (Note 6, *Figures 4* and *7*)						
T_{pLH}	CL = 30 pF		12	15	15	ns
T_{pHL}	CL = 30 pF		12	15	15	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5	6.0	2.75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.

Note 3: All typical values are V_{CC} = 5V, T_A = 25°C.

Note 4: Only one output at a time should be shorted.

Note 5: Difference between complementary outputs at the 50% point.

Note 6: Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE).

The calculated ATE results assume a linear transition between measurement points and are a result of the following equations:

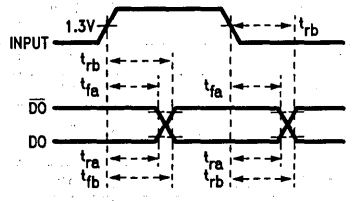
$$Tcp = \frac{(Tfb \times Trb) - (Tra \times Tfa)}{Trb - Tra - Tfa + Tfb}$$

Where: Tcp = Crossing Point

Tra, Trb, Tfa and Tfb are time measurements with respect to the input.

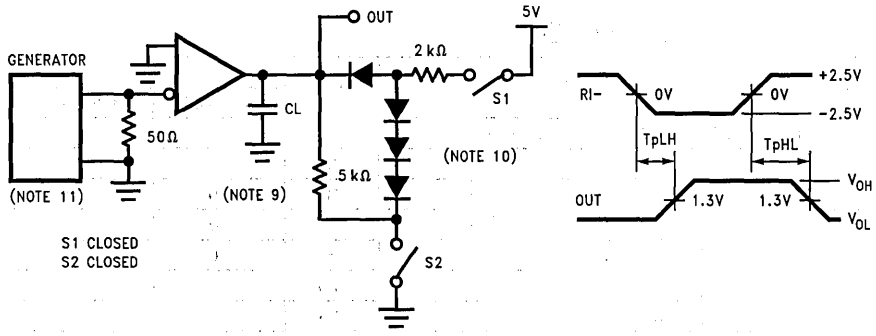
2

Switching Time Waveforms



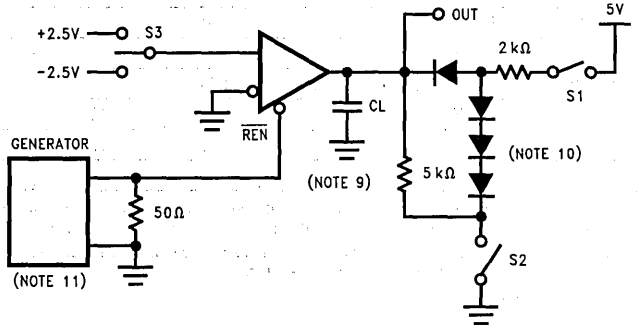
TL/F/8511–3

AC Test Circuits and Switching Waveforms



TL/F/8511–4

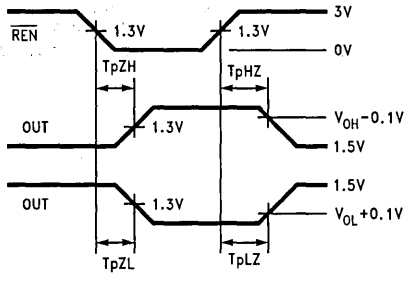
FIGURE 1



TL/F/8511–5

FIGURE 2

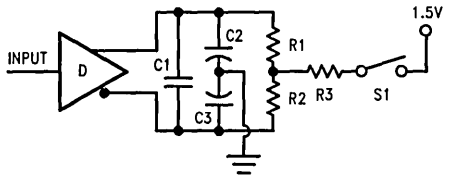
	S1	S2	S3
T_{PLZ}	Closed	Open	+2.5V
T_{PHZ}	Open	Closed	−2.5V
T_{PZL}	Closed	Open	+2.5V
T_{PZH}	Open	Closed	−2.5V



TL/F/8511–6

FIGURE 3

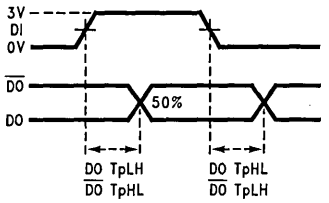
AC Test Circuit and Switching Waveforms (Continued)



NOTE: C1=C2=C3=30 pF, R1=R2=50 Ω, R3=500 Ω

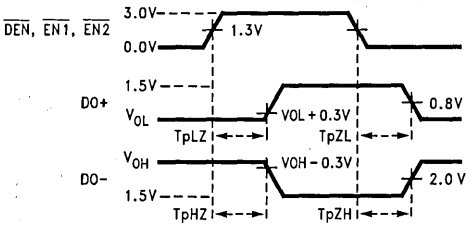
TL/F/8511-7

FIGURE 4



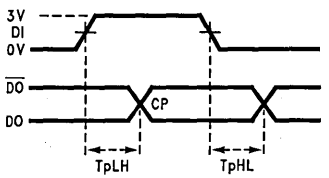
TL/F/8511-8

FIGURE 5



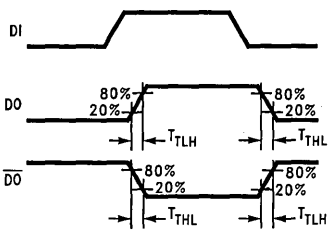
TL/F/8511-9

FIGURE 6



TL/F/8511-10

FIGURE 7

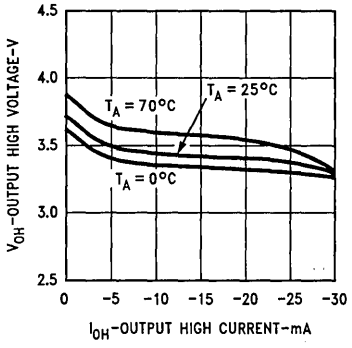


TL/F/8511-13

FIGURE 8

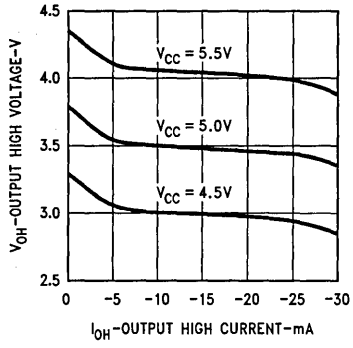
Typical Performance Characteristics (DS8923A)

Driver V_{OH} vs I_{OH} vs Temperature



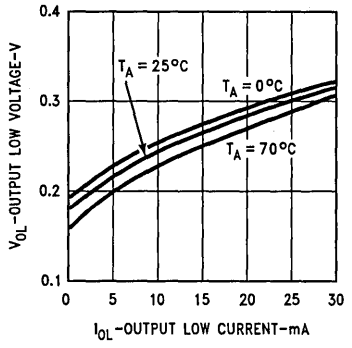
TL/F/8511–14

Driver V_{OH} vs I_{OH} vs V_{CC}



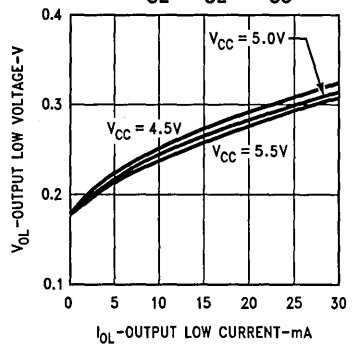
TL/F/8511–15

Driver V_{OL} vs I_{OL} vs Temperature



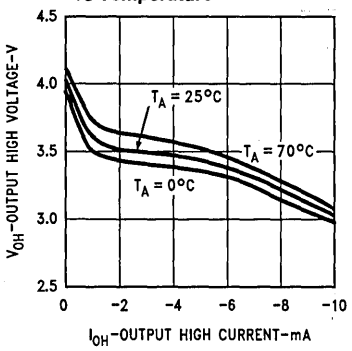
TL/F/8511–16

Driver V_{OL} vs I_{OL} vs V_{CC}



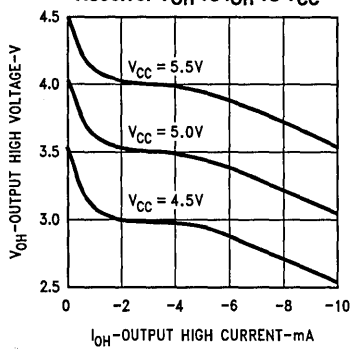
TL/F/8511–17

Receiver V_{OH} vs I_{OH} vs Temperature



TL/F/8511–18

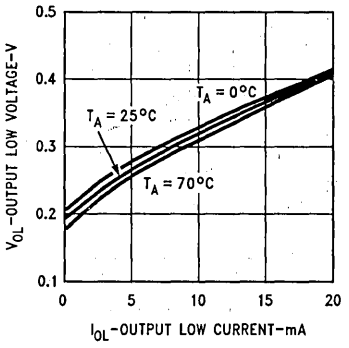
Receiver V_{OH} vs I_{OH} vs V_{CC}



TL/F/8511–19

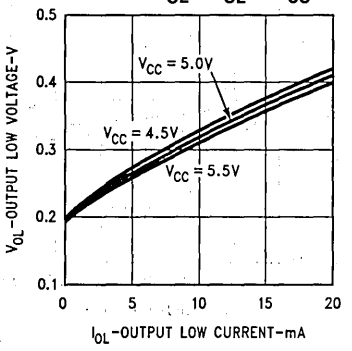
Typical Performance Characteristics (DS8923A) (Continued)

Receiver V_{OL} vs I_{OL} vs Temperature



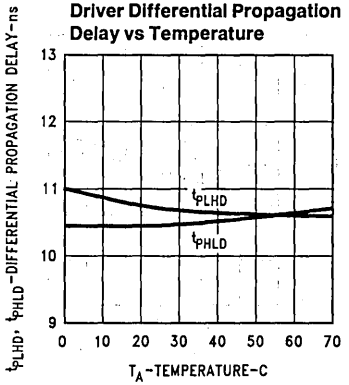
TL/F/8511–20

Receiver V_{OL} vs I_{OL} vs V_{CC}



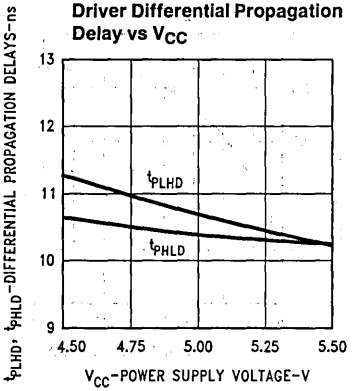
TL/F/8511–21

Driver Differential Propagation Delay vs Temperature



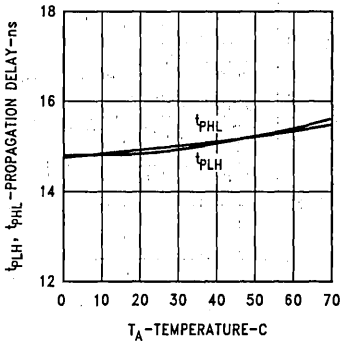
TL/F/8511–22

Driver Differential Propagation Delay vs V_{CC}



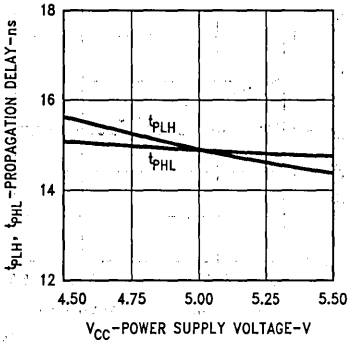
TL/F/8511–23

Receiver Propagation Delay vs Temperature



TL/F/8511–24

Receiver Propagation Delay vs V_{CC}

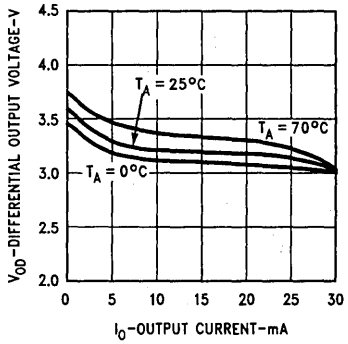


TL/F/8511–25

2

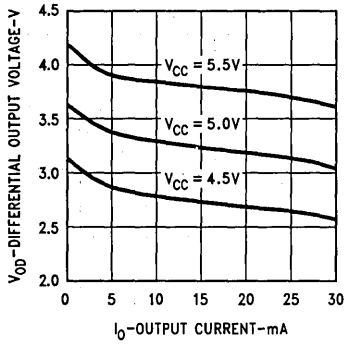
Typical Performance Characteristics (DS8923A) (Continued)

Driver V_{OD} vs Temperature



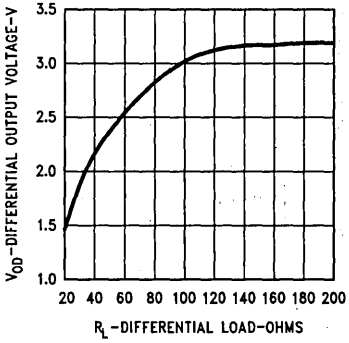
TL/F/8511–26

Driver V_{OD} vs V_{CC}



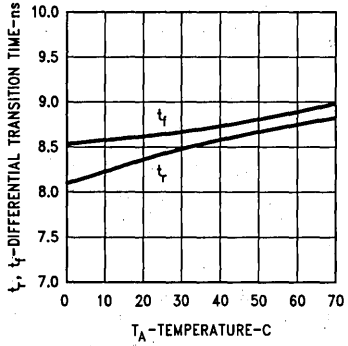
TL/F/8511–27

Driver V_{OD} vs R_L



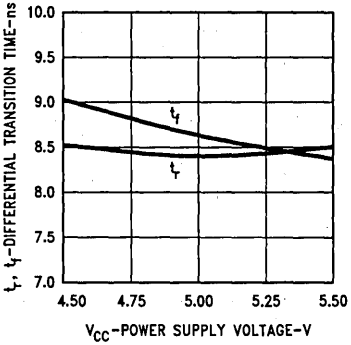
TL/F/8511–28

Driver Differential Transition Time vs Temperature



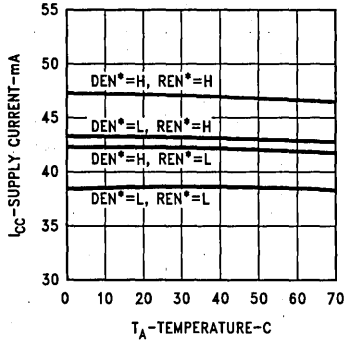
TL/F/8511–29

Driver Differential Transition Time vs V_{CC}



TL/F/8511–30

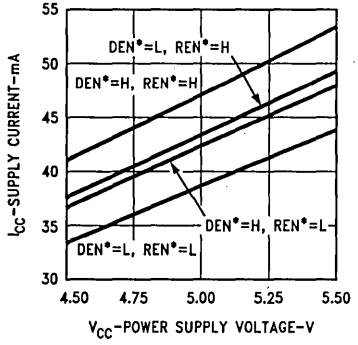
Supply Current vs Temperature



TL/F/8511–31

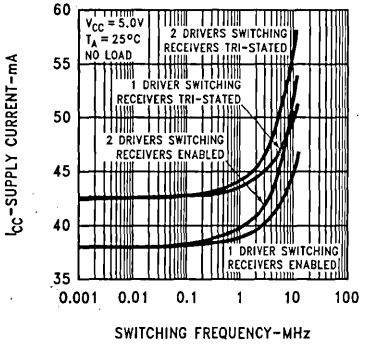
Typical Performance Characteristics (DS8923A) (Continued)

Supply Current vs V_{CC}



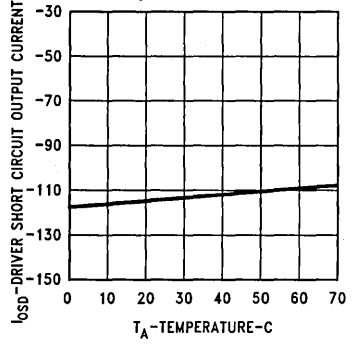
TL/F/8511–32

I_{CC} vs Driver Switching Frequency



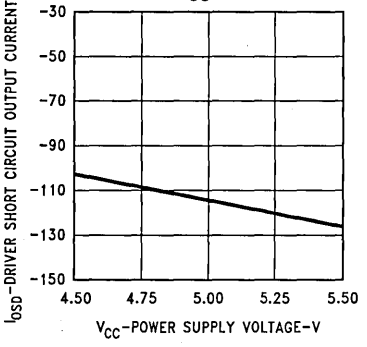
TL/F/8511–33

Driver Short Circuit Current vs Temperature



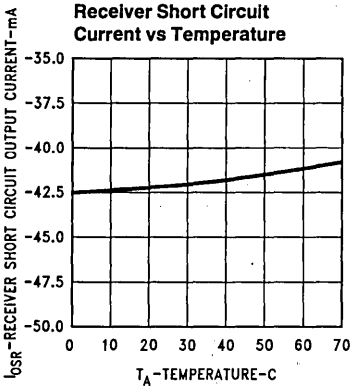
TL/F/8511–34

Driver Short Circuit Current vs V_{CC}



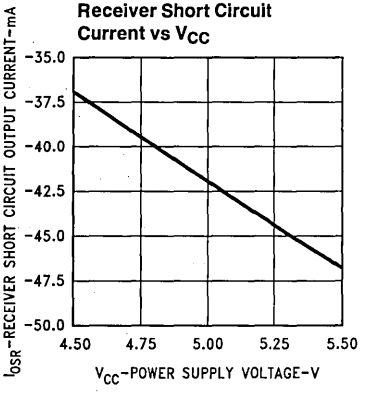
TL/F/8511–35

Receiver Short Circuit Current vs Temperature



TL/F/8511–36

Receiver Short Circuit Current vs V_{CC}

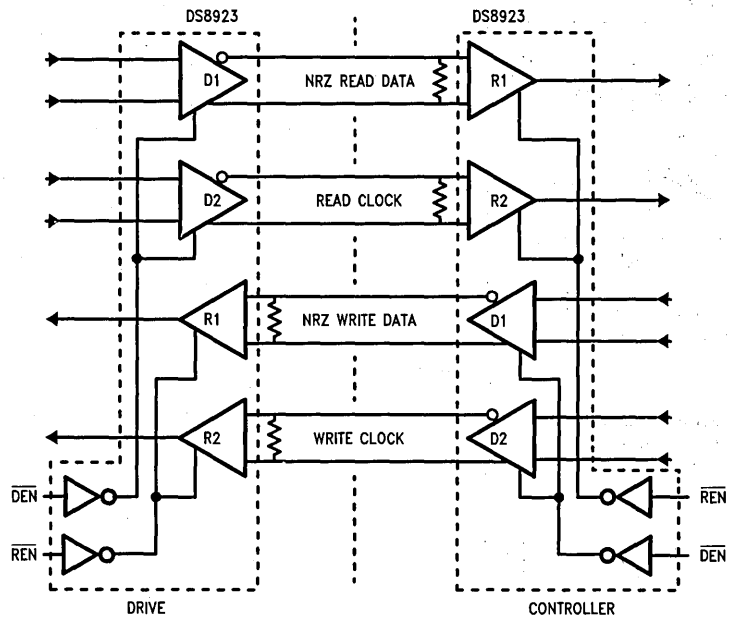


TL/F/8511–37

2

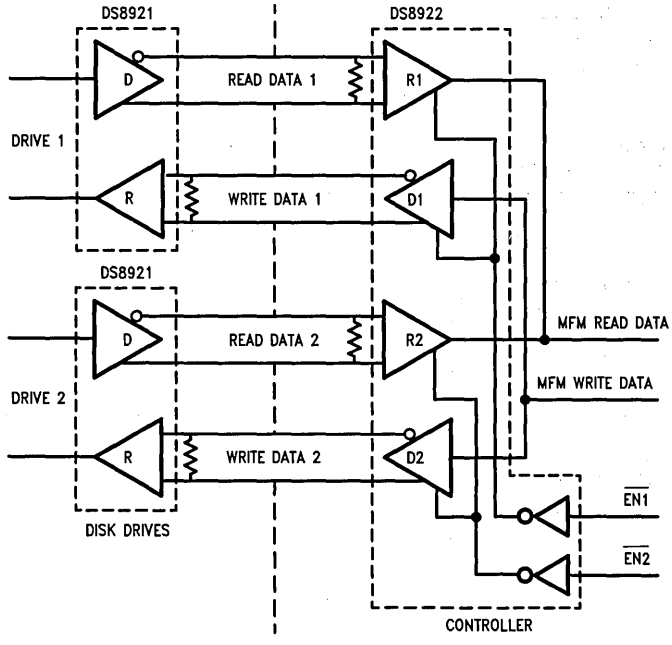
Typical Applications

ESDI Application



TL/F/8511–11

ST504 and ST412 Applications



TL/F/8511–12

National Semiconductor

PRELIMINARY

DS8925
LocalTalk™ Dual Driver/Triple Receiver

General Description

The DS8925 is a dual driver/triple receiver device optimized to provide a single chip solution for a LocalTalk Interface. The device provides one differential TIA/EIA-422 driver, one TIA/EIA-423 single ended driver, one TIA/EIA-422 receiver and two TIA/EIA-423 receivers, all in a surface mount 16 pin package. This device is electrically similar to the 26LS30 and 26LS32 devices.

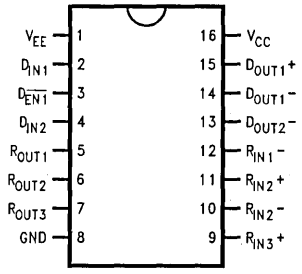
The drivers feature ±10V common mode range, and the differential driver provides TRI-STATEable outputs. The receivers offer ±200 mV thresholds over the ±10V common mode range.

Features

- Single chip solution for LocalTalk port
- Two driver/three receivers per package
- Wide common mode range: ±10V
- ±200 mV receiver sensitivity
- 70 mV typical receiver input hysteresis
- Available in SOIC packaging

Connection Diagram

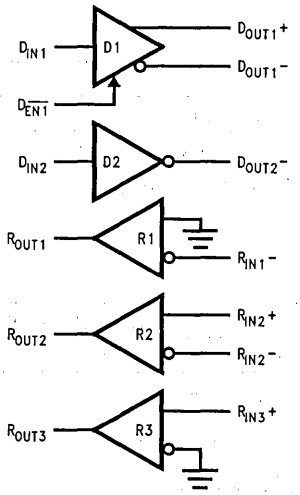
Dual-In-Line Package



TL/F/11895–1

Order Number DS8925M
See NS Package Number M16A

Functional Diagram



TL/F/11895–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+7V
Supply Voltage (V_{EE})	−7V
Enable Input Voltage ($D_{\overline{EN1}}$)	+7V
Driver Input Voltage (D_{IN})	+7V
Driver Output Voltage (Power Off: D_{OUT})	±15V
Receiver Input Voltage (V_{ID}: $R_{IN}+ - R_{IN}-$)	±25V
Receiver Input Voltage (V_{CM}: ($R_{IN}+ + R_{IN}-$)/2)	±25V
Receiver Input Voltage (Input to GND: R_{IN})	±25V
Receiver Output Voltage (R_{OUT})	+5.5V

Maximum Package Power Dissipation @ +25°C	
M Package	TBDW
Derate M Package TBD mW/°C above +25°C	
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 4 Sec.)	+260°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Supply Voltage (V_{EE})	−4.75	−5.0	−5.25	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS								
V_{OD}	Output Differential Voltage	$R_L = \infty$, R_L = 3.9 kΩ		$D_{OUT}+$, $D_{OUT}-$	±7	±8.5	±10	V
V_O	Output Voltage	$R_L = \infty$, R_L = 3.9 kΩ				±4.5	±5.25	V
V_{OD1}	Output Differential Voltage	R_L = 100Ω, *Figure 1*			4.0	TBD		|V|
V_{SS}	$\|V_{OD1} - V_{OD1}\bullet\|$				8.0	TBD		|V|
ΔV_{OD1}	Output Unbalance					0.02	0.4	V
V_{OS}	Offset Voltage					0	3	V
ΔV_{OS}	Offset Unbalance					0.05	0.4	V
V_{OD2}	Output Differential Voltage	RL = 140Ω, *Figure 1*			6.0	TBD		V
I_{OZD}	TRI-STATE® Leakage Current	V_{CC} = 5.25V, V_{EE} = −5.25V	V_O = +10V			2	150	μA
			V_O = +6V			1	100	μA
			V_O = −6V			−1	−100	μA
			V_O = −10V			−2	−150	μA
SINGLE ENDED DRIVER CHARACTERISTICS								
V_O	Output Voltage (No Load)	$R_L = \infty$, R_L = 3.9 kΩ, *Figure 2*		$D_{OUT}-$	4	4.4	6	|V|
V_T	Output Voltage	R_L = 450Ω, *Figure 2*			3.6	4.1		|V|
		R_L = 3 kΩ, *Figure 2*			TBD	TBD		|V|
ΔV_T	Output Unbalance					0.02	0.4	V
DRIVER CHARACTERISTICS								
V_{CM}	Common Mode Range	Power Off, or D1 Disabled		$D_{OUT}+$, $D_{OUT}-$	±10	±15		V
I_{OSD}	Short Circuit Current	V_O = 0V, Sourcing Current				−80	−150	mA
		V_O = 0V, Sinking Current				80	150	mA
I_{OXD}	Power-Off Leakage Current (V_{CC} = V_{EE} = 0V)	V_O = +10V				2	150	μA
		V_O = +6V				1	100	μA
		V_O = −6V				−1	−100	μA
		V_O = −10V				−2	−150	μA

Electrical Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS							
V_{TH}	Input Threshold	$-7V \le V_{CM} \le +7V$	$R_{IN}+$, $R_{IN}-$	−200	±35	+200	mV
V_{HY}	Hysteresis	$V_{CM} = 0V$			70		mV
R_{IN}	Input Resistance	$-10V \le V_{CM} \le +10V$		6.0	8.5		kΩ
I_{IN}	Input Current (Other Input = 0V, Power On, or $V_{CC} = V_{EE} = 0V$)	$V_{IN} = +10V$				3.25	mA
		$V_{IN} = +3V$		0		1.50	mA
		$V_{IN} = -3V$		0		−1.50	mA
		$V_{IN} = -10V$				−3.25	mA
I_B	Input Balance Test	$R_S = 500\Omega$				±400	mV
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$, $V_{ID} = +200$ mV	R_{OUT}	2.7	4.2		V
		$I_{OH} = -400\ \mu A$, V_{ID} = OPEN		2.7	4.2		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 8.0$ mA, $V_{ID} = -200$ mV			0.3	0.5	V
I_{OSR}	Short Circuit Current	$V_O = 0V$		−15		−100	mA
DEVICE CHARACTERISTICS							
V_{IH}	High Level Input Voltage		D_{IN}, $\overline{D_{EN}}$	2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_{CL}	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
I_{CC}	Power Supply Current	No Load, D1 Enabled or Disabled	V_{CC}		58	TBD	mA
I_{EE}			V_{EE}		−10	TBD	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (Notes 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$, $C_L = 500$ pF (*Figures 3* and *4*)	TBD	190	TBD	ns
t_{PLHD}	Differential Propagation Delay Low to High		TBD	190	TBD	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			TBD	TBD	ns
t_r	Rise Time			190	TBD	ns
t_f	Fall Time			190	TBD	ns
t_{PHZ}	Disable Time High to Z	$R_L = 200\Omega$, $C_L = 500$ pF (*Figures 7* and *8*)		80	TBD	ns
t_{PLZ}	Disable Time Low to Z			80	TBD	ns
t_{PZH}	Enable Time Z to High			180	TBD	ns
t_{PZL}	Enable Time Z to Low			180	TBD	ns
SINGLE ENDED DRIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 450\Omega$, $C_L = 500$ pF (*Figures 5* and *6*)	TBD	180	TBD	ns
t_{PLH}	Propagation Delay Low to High		TBD	180	TBD	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$			TBD	TBD	ns
t_r	Rise Time			120	TBD	ns
t_f	Fall Time			120	TBD	ns
RECEIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$C_L = 15$ pF (*Figures 9* and *10*)	10	22	35	ns
t_{PLH}	Propagation Delay Low to High		10	23	35	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$			1	TBD	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}, V_{OD1}, V_{SS}, and V_{ID}.

Note 3: All typicals are given for: $V_{CC} = +5.0V$, $V_{EE} = -5.0V$, $T_A = +25°C$.

Truth Tables

Driver (D1)

Inputs		Outputs	
$D_{\overline{EN1}}$	D_{IN1}	$D_{OUT1}+$	$D_{OUT1}-$
H	X	Z	Z
L	L	L	H
L	H	H	L

Driver (D2)

Input	Output
D_{IN2}	$D_{OUT2}-$
L	H
H	L

H = Logic High Level (Steady State)
L = Logic Low Level (Steady State)
X = Irrelevant (Any Input)
Z = Off State (TRI-STATE, High Impedance)
†OPEN = Non-Terminated

Receiver (1)

Input	Output
$R_{IN1}-$	R_{OUT1}
≤ −200 mV	H
≥ +200 mV	L
OPEN†	H

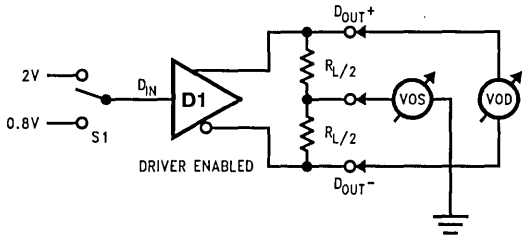
Receiver (2)

Inputs	Output
$R_{IN2}+ - R_{IN2}-$	R_{OUT2}
≤ −200 mV	L
≥ +200 mV	H
OPEN†	H

Receiver (3)

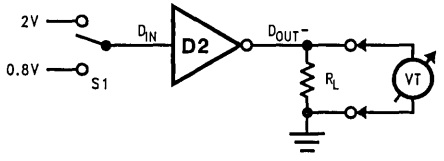
Input	Output
$R_{IN3}+$	R_{OUT3}
≤ −200 mV	L
≥ +200 mV	H
OPEN†	H

Parameter Measurement Information



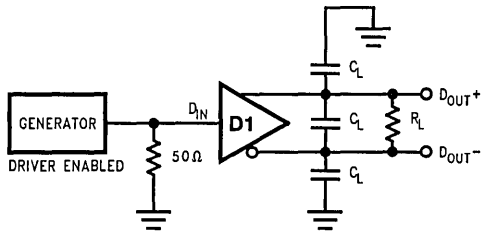
TL/F/11895–3

FIGURE 1. Differential Driver DC Test Circuit



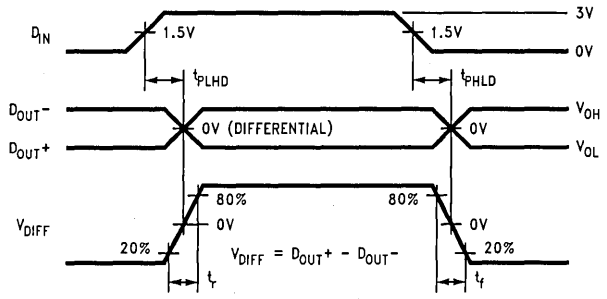
TL/F/11895–4

FIGURE 2. Single Ended Driver DC Test Circuit



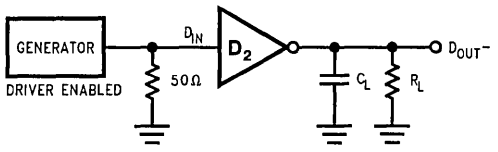
TL/F/11895–5

FIGURE 3. Differential Driver Propagation Delay and Transition Time Test Circuit



TL/F/11895–6

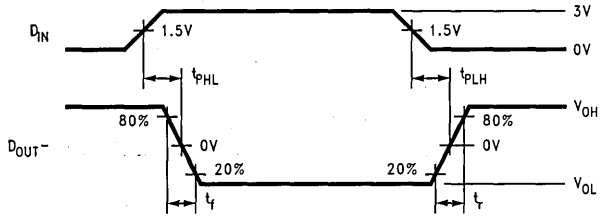
FIGURE 4. Differential Driver Propagation Delay and Transition Time Waveforms



TL/F/11895–7

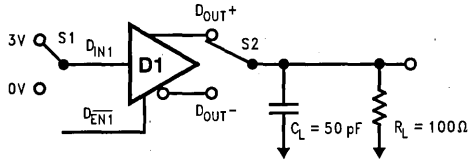
FIGURE 5. Single Ended Driver Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)



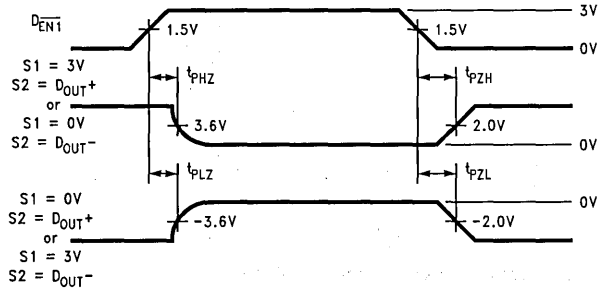
TL/F/11895–8

FIGURE 6. Single Ended Driver Propagation Delay and Transition Time Waveform



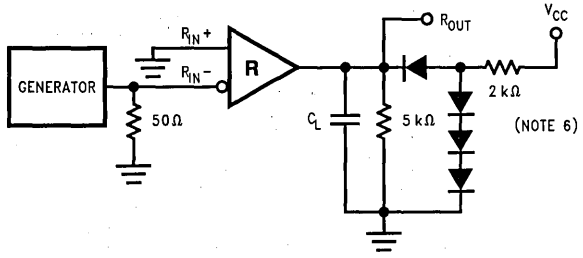
TL/F/11895–9

FIGURE 7. Differential Driver TRI-STATE Test Circuit



TL/F/11895–10

FIGURE 8. Differential Driver TRI-STATE Waveforms



TL/F/11895–11

FIGURE 9. Receiver Propagation Delay Test Circuit

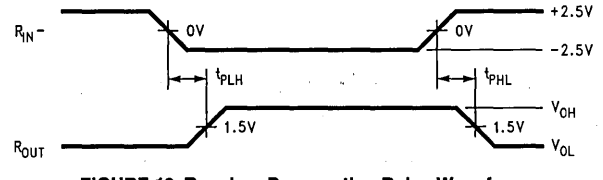


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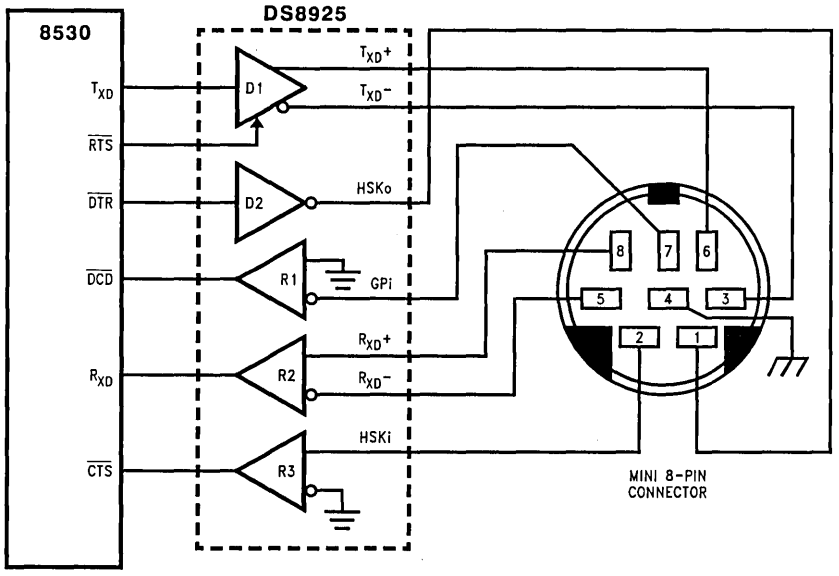
FIGURE 10. Receiver Propagation Delay Waveform

Note 4: Generator waveform for all tests unless otherwise specified: f = 500 kHz, Z_O = 50Ω, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note 5: C_L includes probe and jig capacitance.

Note 6: All diodes are 1N916 or equivalent.

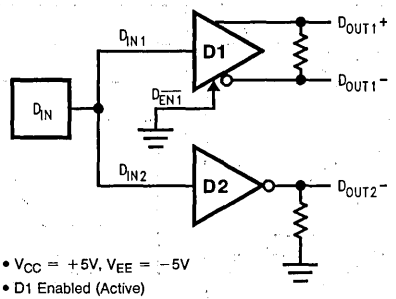
Typical Application Information



TL/F/11895–13

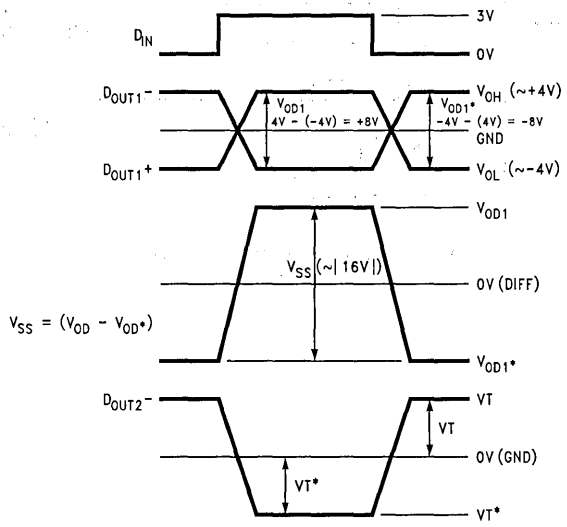
FIGURE 11. Typical LocalTalk Application

Typical Application Information (Continued)



NOTE: • V_{CC} = +5V, V_{EE} = −5V
• D1 Enabled (Active)

TL/F/11895–14



Note: Star (*) represents the opposite input condition for a parameter.

TL/F/11895–15

FIGURE 12. Typical Driver Output Waveforms

TABLE I. Device Pin Descriptions

Pin #	Name	Description
2, 4	D_{IN}	TTL Driver Input Pins
3	$D_{\overline{EN1}}$	Active Low Driver Enable Pin. A High on this Pin TRI-STATES the Driver Outputs (D1 Only)
15	$D_{OUT}+$	Non-Inverting Driver Output Pin
13, 14	$D_{OUT}-$	Inverting Driver Output Pin
9, 11	$R_{IN}+$	Non-Inverting Receiver Input Pin
10, 12	$R_{IN}-$	Inverting Receiver Input Pin
5, 6, 7	R_{OUT}	Receiver Output Pin
8	GND	Ground Pin
16	V_{EE}	Negative Power Supply Pin, −5V ±5%
1	V_{CC}	Positive Power Supply Pin, +5V ±5%

National Semiconductor

DS9636A
RS-423 Dual Programmable Slew Rate Line Driver

General Description

The DS9636A is a TTL/CMOS compatible, dual, single ended line driver which has been specifically designed to satisfy the requirements of EIA Standard RS-423.

The DS9636A is suitable for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between the wave shaping control lead (WS) and ground. This eliminates any need for external filtering of the output signals. Output voltage levels and slew rates are independent of power supply variations. Current-limiting is provided in both output states. The DS9636A is designed for nominal power supplies of ±12V.

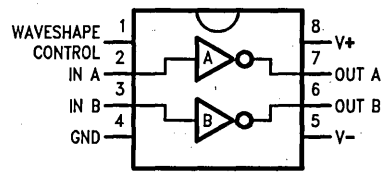
Inputs are TTL compatible with input current loading low enough (1/10 UL) to be also compatible with CMOS logic. Clamp diodes are provided on the inputs to limit transients below ground.

Features

- Programmable slew rate limiting
- Meets EIA Standard RS-423
- Commercial or extended temperature range
- Output short circuit protection
- TTL and CMOS compatible inputs

Connection Diagram

8-Lead DIP



TL/F/9620–1

Top View

Order Number DS9636ACJ, DS9636ACN or DS9636AMJ
See NS Package Number J08A or N08E

For Complete Military 883 Specifications, see RETS Data Sheet.

Order Number DS9636AJ/883
See NS Package Number J08A

2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP: −65°C to +150°C

Lead Temperature
- Ceramic DIP (Soldering, 60 seconds): 300°C
- Molded DIP (Soldering, 10 seconds): 265°C

Maximum Power Dissipation* at 25°C (Note 5)
- Cavity Package: 1560 mW
- Molded Package: 1300 mW

V+ Lead Potential to Ground Lead: V− to +15V

V− Lead Potential to Ground Lead: +0.5V to −15V

V+ Lead Potential to V− Lead: 0V to +30V

Output Potential to Ground Lead: ±15V

Output Source Current: −150 mA

Output Sink Current: 150 mA

Recommended Operating Conditions

Characteristics	DS9636AM			DS9636AC			Units
	Min	Typ	Max	Min	Typ	Max	
Positive Supply Voltage (V+)	10.8	12	13.2	10.8	12	13.2	V
Negative Supply Voltage (V−)	−13.2	−12	−10.8	−13.2	−12	−10.8	V
Operating Temperature (T_A)	−55	25	125	0	25	70	°C
Wave Shaping Resistance (R_{WS})	10		500	10		1000	kΩ

Electrical Characteristics Over recommended operating temperature, supply voltage and wave shaping resistance ranges unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH1}	Output Voltage HIGH	R_L to GND ($R_L = \infty$)	5.0	5.6	6.0	V
V_{OH2}		R_L to GND (R_L = 3.0 kΩ)	5.0	5.6	6.0	V
V_{OH3}		R_L to GND (R_L = 450Ω)	4.0	5.5	6.0	V
V_{OL1}	Output Voltage LOW	R_L to GND ($R_L = \infty$)	−6.0	−5.7	−5.0	V
V_{OL2}		R_L to GND (R_L = 3.0 kΩ)	−6.0	−5.6	−5.0	V
V_{OL3}		R_L to GND (R_L = 450Ω)	−6.0	−5.4	−4.0	V
R_O	Output Resistance	450Ω ≤ R_L		25	50	Ω
I_{OS+}	Output Short Circuit Current (Note 4)	V_O = 0V, V_I = 0V	−150	−60	−15	mA
I_{OS-}		V_O = 0V, V_I = 2.0V	15	60	150	mA
I_{CEX}	Output Leakage Current	V_O = ±6.0V, Power-Off	−100		+100	μA
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{IC}	Input Clamp Diode Voltage	I_I = 15 mA	−1.5	−1.1		V
I_{IL}	Input Current LOW	V_I = 0.4V	−80	−16		V
I_{IH}	Input Current HIGH	V_I = 2.4V		1.0	10	μA
		V_I = 5.5V		10	100	
I+	Positive Supply Current	V_{CC} = ±12V, $R_L = \infty$, R_{WS} = 100 kΩ, V_I = 0V		13	18	mA
I−	Negative Supply Current	V_{CC} = ±12V, $R_L = \infty$, R_{WS} = 100 kΩ, V_I = 0V	−18	−13		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range for the DS9636AM and across the 0°C to +70°C range for the DS9636AC. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

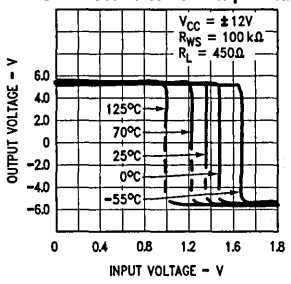
Note 5: Ratings apply to ambient temperature at 25°C. Above this temperature, derate J and N packages 10.4 mW/°C.

Switching Characteristics $V_{CC} = \pm 12V \pm 10\%$, $T_A = 25°C$, see AC Test Circuit

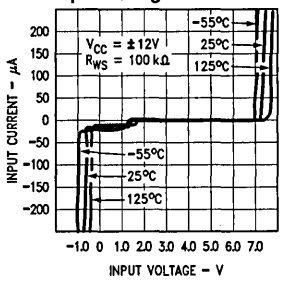
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r	Rise Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	μs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	
		$R_{WS} = 500\ k\Omega$	40	55	70	
		$R_{WS} = 1000\ k\Omega$	80	110	140	
t_f	Fall Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	μs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	
		$R_{WS} = 500\ k\Omega$	40	55	70	
		$R_{WS} = 1000\ k\Omega$	80	110	140	

Typical Performance Characteristics

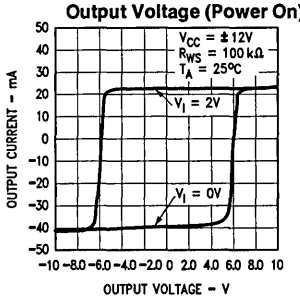
Input/Output Transfer Characteristic vs Temperature



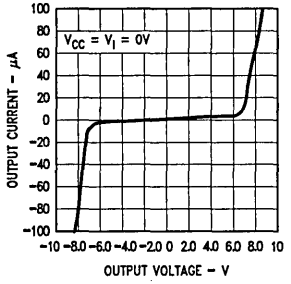
Input Current vs Input Voltage



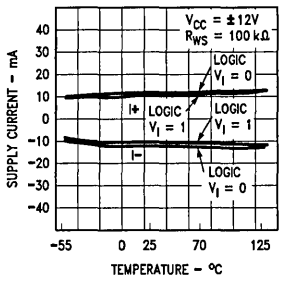
Output Current vs Output Voltage (Power On)



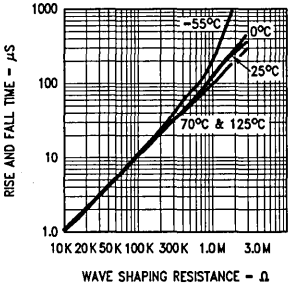
Output Current vs Output Voltage (Power Off)



Supply Current vs Temperature



Transition Time vs R_{WS}



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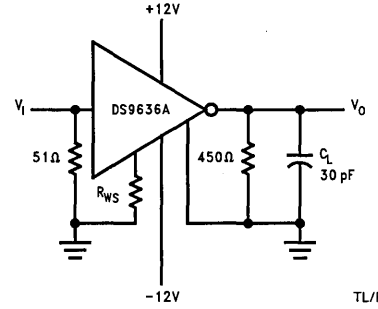
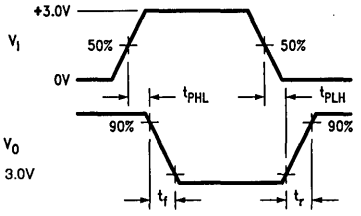


TL/F/9620–4



V_I V_O

Amplitude: 3.0V

Offset: 0V

Pulse Width: 500 µs

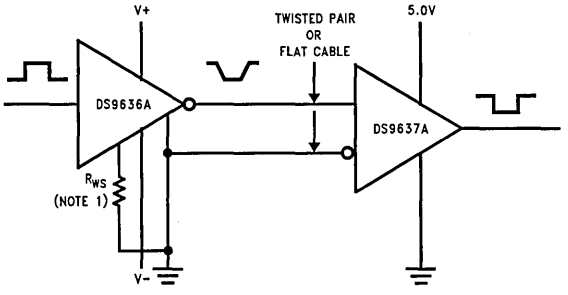
PRR: 1.0 kHz

$t_r = t_f \leq 10$ ns

TL/F/9620–5

Note: C_L includes jig and probe capacitance

FIGURE 1. AC Test Circuit and Waveforms



TL/F/9620–6

FIGURE 2. RS-423 System Application

National Semiconductor

DS9637A
Dual Differential Line Receiver

General Description

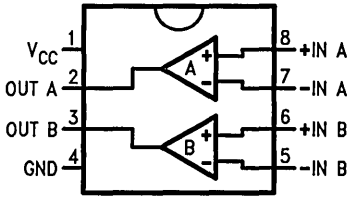
The DS9637A is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422 and RS-423. In addition, the DS9637A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The DS9637A is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5V power supply and has Schottky TTL compatible outputs. The DS9637A has an operational input common mode range of ±7V either differentially or to ground.

Features

- Dual channel
- Single 5V supply
- Satisfies EIA standards RS-422 and RS423
- Built-in ±35 mV hysteresis
- High input common mode voltage range
- High input impedance
- TTL compatible outputs
- Schottky technology
- Extended temperature range

Connection Diagram

8-Lead DIP and SO-8 Package



TL/F/9621–1

Top View

Order Number DS9637ACJ, DSA9637AMJ, DS9637ACM or DS9637ACN
See NS Package Number J08A, M08A or N08E

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS9637AMJ/883
See NS Package Number J08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to + 175°C
- Molded DIP: −65°C to + 150°C

Lead Temperature
- Ceramic DIP (Soldering, 30 seconds): 300°C
- Molded DIP and SO Package (Soldering, 10 seconds): 265°C

Maximum Power Dissipation* at 25°C
- Cavity Package: 1300 mW
- Molded Package: 930 mW
- SO Package: 810 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C; derate SO package 6.5 mW/°C above 25°C.

V_{CC} Lead Potential to Ground	−0.5V to 7.0V
Input Potential to Ground	±15V
Differential Input Voltage	±15V
Output Potential to Ground	−0.5V to +5.5V
Output Sink Current	50 mA

Recommended Operating Conditions

DS9637AM	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Temperature (T_A)	−55	+125	°C
DS9637AC			
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature (T_A)	0	+70	°C

Electrical Characteristics

Over recommended operating temperature and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold Voltage (Note 5)	$-7.0V \le V_{CM} \le +7.0V$	−0.2		+0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage (Note 6)	$-7.0V \le V_{CM} \le +7.0V$	−0.4		+0.4	V
I_I	Input Current (Note 7)	$V_I = 10V, 0V \le V_{CC} \le +5.5V$		1.1	3.25	mA
		$V_I = -10V, 0V \le V_{CC} \le +5.5V$		−1.6	−3.25	
V_{OL}	Output Voltage LOW	I_{OL} = 20 mA, V_{CC} = Min		0.35	0.5	V
V_{OH}	Output Voltage HIGH	I_{OH} = −1.0 mA, V_{CC} = Min	2.5	3.5		V
I_{OS}	Output Short Circuit Current (Note 4)	V_O = 0V, V_{CC} = Max	−40	−75	−100	mA
I_{CC}	Supply Current	V_{CC} = Max, V_I+ = 0.5V, V_I- = GND		35	50	mA
V_{HYST}	Input Hysteresis	V_{CM} = ±7.0V (See Curves)		70		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range for DS9637AM and across the 0°C to +70°C range for the DS9637ASC. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: V_{DIFF} (Differential Input Voltage) = $(V_I+) - (V_I-)$. V_{CM} (Common Mode Input Voltage) = V_I+ or V_I-.

Note 6: 500Ω ±1% in series with inputs.

Note 7: The input not under test is tied to ground.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High	See AC Test Circuit		15	25	ns
t_{PHL}	Propagation Delay Time High to Low	See AC Test Circuit		13	25	ns

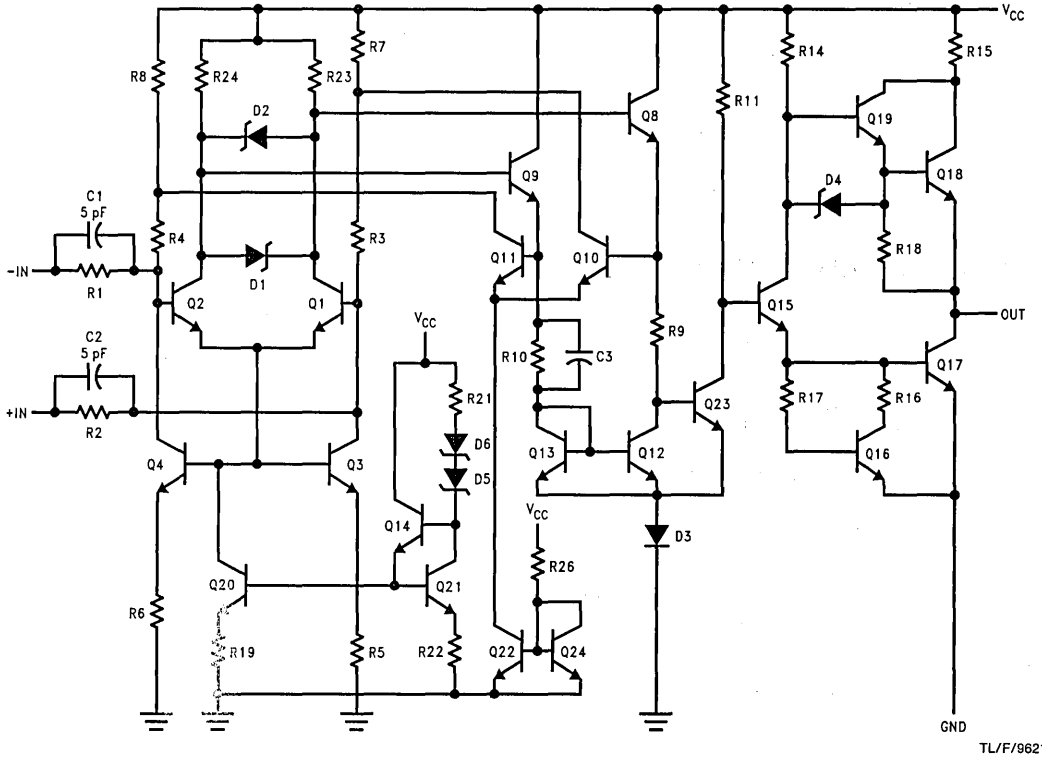
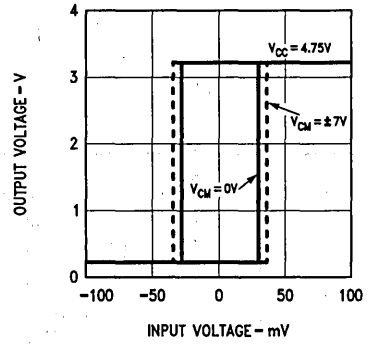
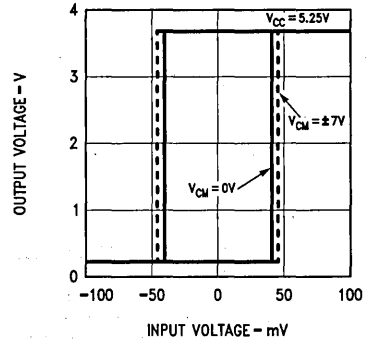


FIGURE 1. Equivalent Circuit

Typical Input/Output Transfer Characteristics

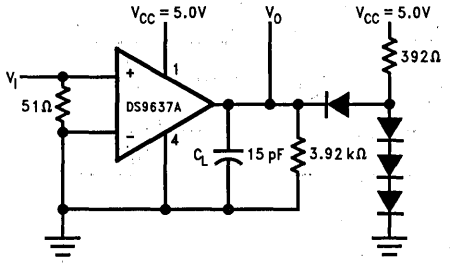


TL/F/9621–3



TL/F/9621–4

AC Test Circuit and Waveforms



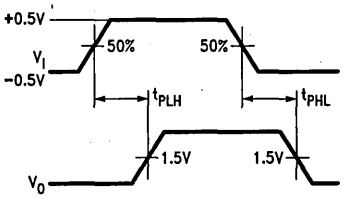
TL/F/9621–5

Notes:

C_L includes jig and probe capacitance.

All diodes are FD700 or equivalent.

FIGURE 2



TL/F/9621–6

V_I

Amplitude: 1.0V

Offset: 0.5V

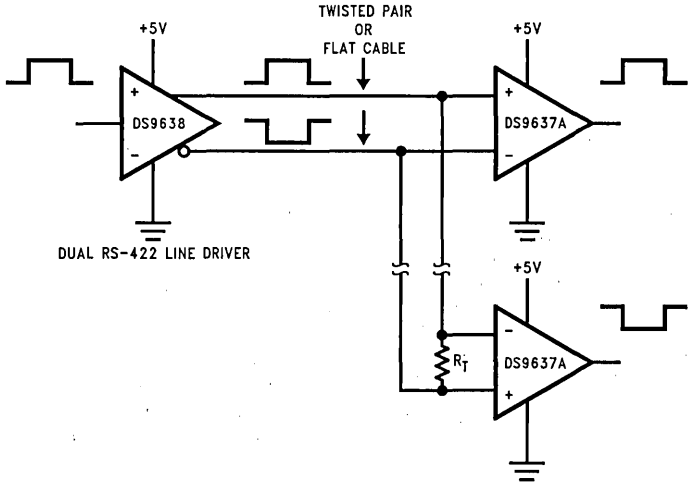
Pulse Width: 100 ns

PRR: 5.0 MHz

$t_r = t_f \leq 5.0$ ns

FIGURE 2a

Typical Applications



TL/F/9621–7

FIGURE 3. RS-422 System Application (FIPS 1020) Differential Simplex Bus Transmission

Notes:

$R_T \geq 50\Omega$ for RS-422 operation.

R_T combined with input impedance of receivers must be greater than 90Ω.

National Semiconductor

DS9638
RS-422 Dual High Speed Differential Line Driver

General Description

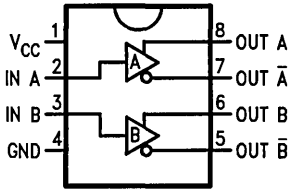
The DS9638 is a Schottky, TTL compatible, dual differential line driver designed specifically to meet the EIA Standard RS-422 specifications. It is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem pole TTL outputs, with active pull-up and pull-down. The device features a short circuit protected active pull-up with low output impedance and is specified to drive 50Ω transmission lines at high speed. The mini-DIP provides high package density.

Features

- Single 5V supply
- Schottky technology
- TTL and CMOS compatible inputs
- Output short circuit protection
- Input clamp diodes
- Complementary outputs
- Minimum output skew (<1.0 ns typical)
- 50 mA output drive capability for 50Ω transmission lines
- Meets EIA RS-422 specifications
- Propagation delay of less than 10 ns
- "Glitchless" differential output
- Delay time stable with V_{CC} and temperature variations (<2.0 ns typical) *(Figure 3)*
- Extended temperature range

Connection Diagram

8-Lead DIP



TL/F/9622–1

Top View

Order Number DS9638CJ, DS9638MJ, DS9638CM or DS9638CN
See NS Package Number J08A, M08A or N08E

For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS9638MJ/883
See NS Package Number J08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP and SO-8: −65°C to +150°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP (Soldering, 10 sec.): 265°C

Maximum Power Dissipation* at 25°C
- Cavity Package: 1300 mW
- Molded Package: 930 mW
- SO Package: 810 mW

V_{CC} Lead Potential to Ground: −5V to 7V

Input Voltage: −0.5V to +7V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C; derate SO package 6.5 mW°C above 25°C.

Recommended Operating Conditions

	DS9638M			DS9638C			
	Min	Typ	Max	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	4.75	5.0	5.25	V
Output Current HIGH (I_{OH})			−50			−50	mA
Output Current LOW (I_{OL})			50	40		50	mA
Operating Temperature (T_A)	−55	25	125	0	25	70	°C

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW	0°C to +70°C				0.8	V
		−55°C to +125°C				0.5	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.0	−1.2	V
V_{OH}	Output Voltage HIGH	V_{CC} = Min, V_{IH} = $V_{IH\ Min}$, V_{IL} = $V_{IL\ Max}$	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2.0			
V_{OL}	Output Voltage LOW	V_{CC} = Min, V_{IH} = $V_{IH\ Min}$, V_{IL} = $V_{IL\ Max}$, I_{OL} = 40 mA				0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, $V_{I\ Max}$ = 5.5V				50	μA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_{IH} = 2.7V				25	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_{IL} = 0.5V				−200	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V (Note 4)		−50		−150	mA
V_T, $\overline{V}_T$	Terminated Output Voltage	See *Figure 1*		2.0			V
V_T−$\overline{V}_T$	Output Balance					0.4	V
V_{OS}, $\overline{V}_{OS}$	Output Offset Voltage					3.0	V
V_{OS}−$\overline{V}_{OS}$	Output Offset Balance					0.4	V
I_X	Output Leakage Current	T_A = 25°C, −0.25V < V_X < 5.5V				100	μA
I_{CC}	Supply Current (Both Drivers)	V_{CC} = 5.5V, All input at 0V, No Load			45	65	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics provide conditions for actual device operation.

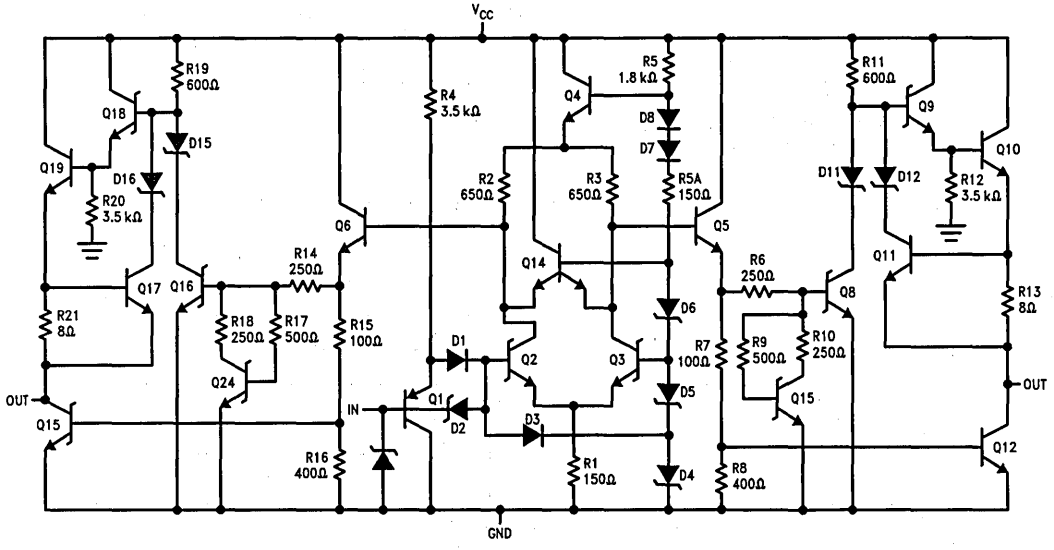
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS9638M and across the 0°C to +70°C range for the DS9638C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C.

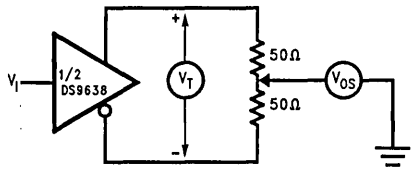
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay	C_L = 15 pF R_L = 100Ω, See *Figure 2*		10	20	ns
t_{PLH}				10	20	ns
t_f	Fall Time, 90%–10%			10	20	ns
t_r	Rise Time, 10%–90%			10	20	ns
$t_{PO}-t_{\overline{PO}}$	Skew Between Outputs A/$\overline{A}$ and B/$\overline{B}$			1.0		ns



TL/F/9622–2

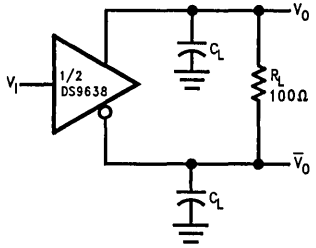
FIGURE 1. Equivalent Circuit

DC Test Circuit



TL/F/9622-3

FIGURE 2. Terminated Output Voltage and Output Balance



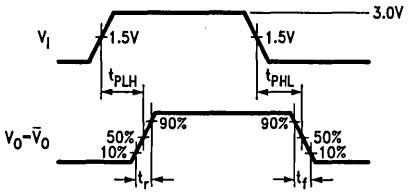
TL/F/9622-4

Note:

The pulse generator has the following characteristics:
PRR = 500 kHz, t_W = 100 ns,
$t_r \leq 5.0$ ns, $Z_O = 50\Omega$.

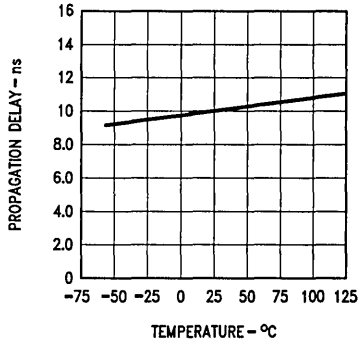
C_L includes probe and jig capacitance.

FIGURE 3. AC Test Circuit and Voltage Waveform



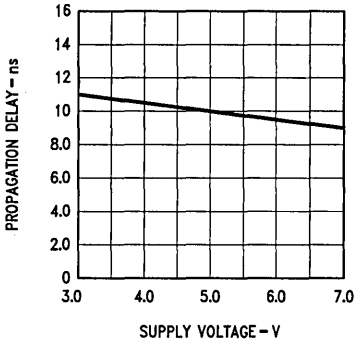
TL/F/9622-5

FIGURE 3a



TL/F/9622-6

FIGURE 4. Typical Delay Characteristics



TL/F/9622-7

FIGURE 4a

National Semiconductor

DS9639A
Dual Differential Line Receiver

General Description

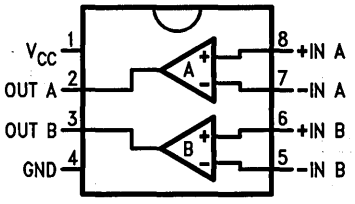
The DS9639A is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422, RS-423 and RS-232C. In addition, the DS9639A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The DS9639A is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5.0V power supply and has Schottky TTL compatible outputs. The DS9639A has an operational input common mode range of ±7.0V either differentially or to ground.

Features

- Dual channel
- Single 5.0V supply
- Satisfies EIA Standards RS-422, RS-423 and RS-232C
- Built-in ±35 mV hysteresis
- High input common mode voltage range
- High input impedance
- TTL compatible outputs
- Schottky technology

Connection Diagram

8-Lead DIP



TL/F/9623–1

Top View

Order Number DS9639ACN
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Molded DIP (soldering, 10 sec.)	265°C
V_{CC} Lead Potential to Ground	−0.5V to +7.0V
Input Potential to Ground Lead	±25V
Differential Input Voltage	±25V
Output Differential to Ground Lead	−0.5V to 5.5V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C Molded Package	930 mW

*Derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions (Note 1)	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold Voltage (Note 5)	$-7.0V \le V_{CM} \le +7.0V$	−0.2		+0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage (Note 6)	$-7.0V \le V_{CM} \le +7.0V$	−0.4		+0.4	V
I_I	Input Current (Note 7)	$V_I = 10V, 0V \le V_{CC} \le 5.5V$		1.1	3.25	mA
		$V_I = -10V, 0V \le V_{CC} \le 5.5V$		−1.6	−3.25	
V_{OL}	Output Voltage LOW	I_{OL} = 20 mA, V_{CC} = Min		0.35	0.5	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -1.0$ mA, V_{CC} = Min	2.5	3.5		V
I_{OS}	Output Short Circuit Current (Note 4)	V_O = 0V, V_{CC} = Max	−40	−75	−100	mA
I_{CC}	Supply Current	V_{CC} = Max, V_I+ = 0.5V, V_I- = GND		35	50	mA
V_{HYST}	Input Hysteresis	V_{CM} = ±7.0V (See Curves)		70		mV

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High	See AC Test Circuit		55	85	ns
t_{PHL}	Propagation Delay Time High to Low	See AC Test Circuit		50	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS9639A. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4. Only one output at a time should be shorted.

Note 5: V_{DIFF} (Differential Input Voltage) = $(V_I+) - (V_I-)$. V_{CM} (Common Mode Input Voltage) = V_I+ or V_I-.

Note 6: 500Ω ±1% in series with inputs.

Note 7: The input not under test is tied to ground.

Equivalent Circuit

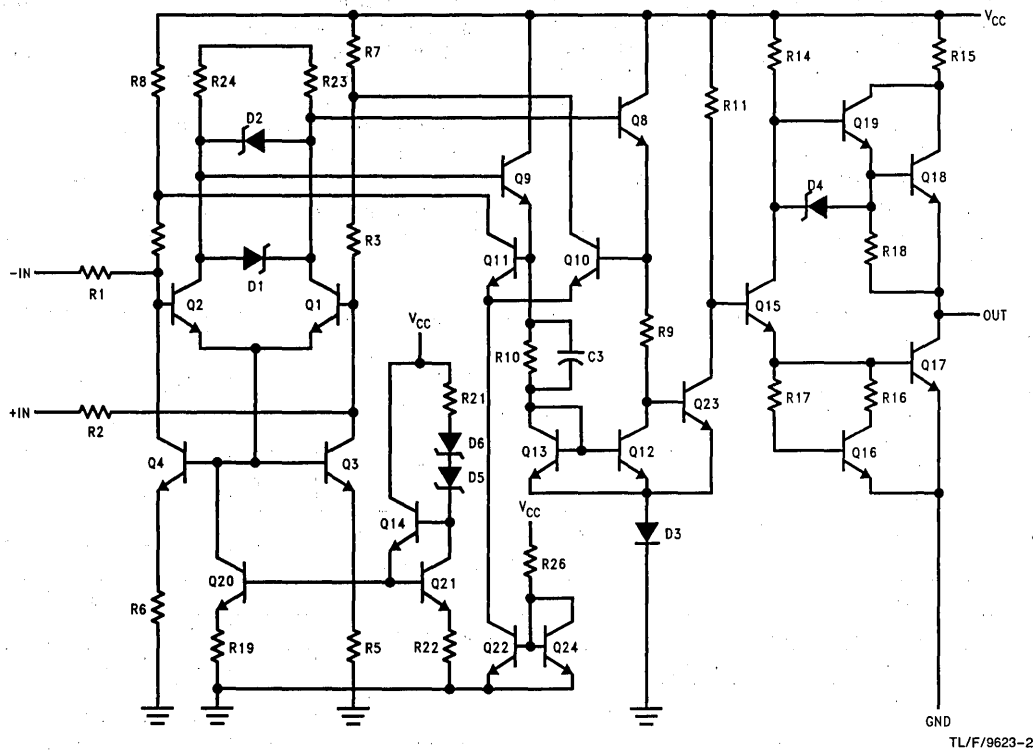


FIGURE 1. Equivalent Circuit

Typical Input/Output Transfer Characteristics

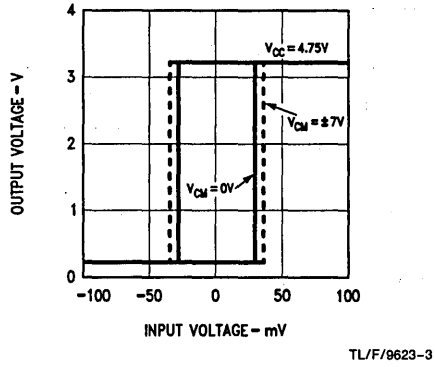


FIGURE 2

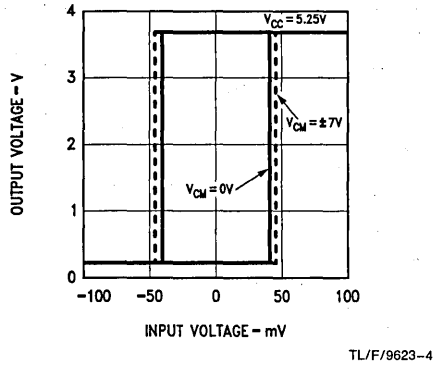
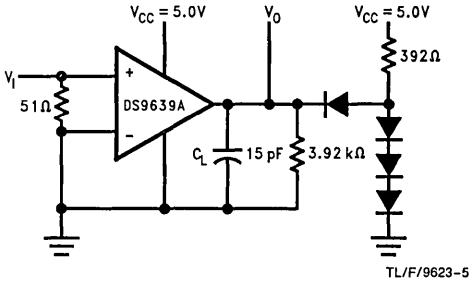


FIGURE 2a

AC Test Circuit and Switching Time Waveform

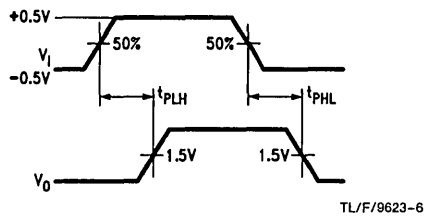


Notes:

C_L includes jig and probe capacitance.

All diodes are FD700 or equivalent.

FIGURE 3. AC Test Circuit and Waveforms



V_I

Amplitude: 1.0V

Offset: 0.5V

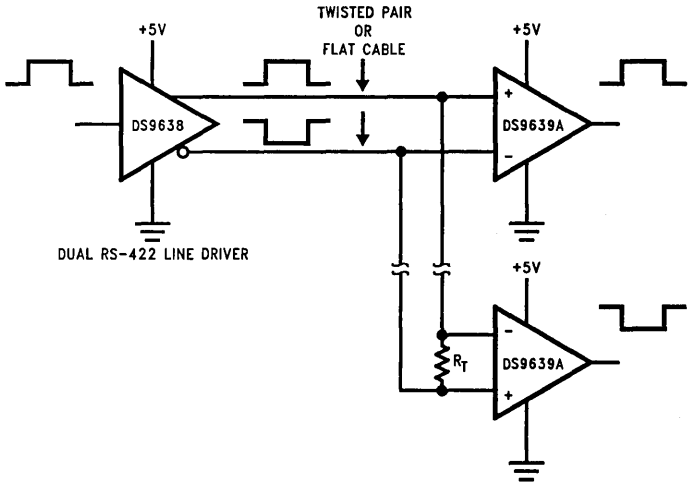
Pulse Width: 500 ns

PRR: 1 MHz

$t_r = t_f \leq 5.0$ ns

FIGURE 3a

Typical Applications



Notes:

$R_t \geq 50\Omega$ for RS-422 operation.

R_t combined with input impedance of receivers must be greater than 90Ω.

FIGURE 4. RS-422 System Application (FIPS 1020) Differential Simplex Bus Transmission

Section 3

TIA/EIA-485

Section 3 Contents

National Semiconductor

DS3695/DS3695T/DS3696/DS3696T/DS3697/DS3698 Multipoint RS485/RS422 Transceivers/Repeaters

General Description

The DS3695, DS3696, DS3697 and DS3698 are high speed differential TRI-STATE® bus/line transceivers/repeaters designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission.

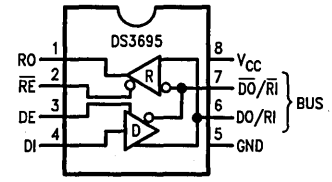
The driver and receiver outputs feature TRI-STATE capability. The driver outputs remain in TRI-STATE over the entire common mode range of +12V to −7V. Bus faults that cause excessive power dissipation within the device trigger a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696 and DS3698 provide an output pin TS (thermal shutdown) which reports the occurrence of the thermal shutdown of the device. This is an "open collector" pin with an internal 10 kΩ pull-up resistor. This allows the line fault outputs of several devices to be wire OR-ed.

Both AC and DC specifications are guaranteed over the 0°C to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422
- 15 ns driver propagation delays with 2 ns skew (typical)
- Single +5V supply
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus
- Thermal shutdown protection
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus
- 70 mV typical receiver hysteresis

Connection and Logic Diagrams



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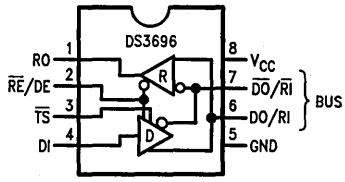
Top View



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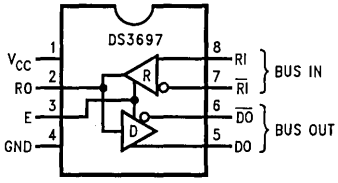
Top View



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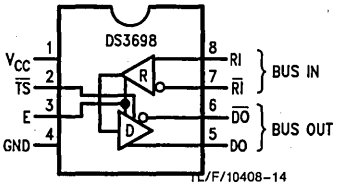
Top View



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Top View

Order Number DS3695N, DS3696N, DS3697N, DS3698N, DS3695TN, DS3696TN, DS3695TJ or DS3696TJ
See NS Package Number J08A or N08E

Note: $\overline{TS}$ pin was $\overline{LF}$ (Line Fault) in previous datasheets and reports the occurrence of a thermal shutdown of the device.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/−10V
Receiver Input Voltages (DS3695, DS3696)	+15V/−10V
Receiver Common Mode Voltage (DS3697, DS3698)	±25V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ 25°C N Package	1.07W (Note 4)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Free Air Temp. (T_A)			
Commercial	0	+70	°C
Industrial	−40	+85	°C

Electrical Characteristics $0°C \le T_A \le +70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		*(Figure 1)*	R = 50Ω; (RS-422) (Note 5)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States		*(Figure 1)*	R = 27Ω			0.2	V
V_{OC}	Driver Common Mode Output Voltage						3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, $\overline{DE}$, $\overline{RE}$, E, $\overline{RE}$/DE			2			V
V_{IL}	Input Low Voltage						0.8	V
V_{CL}	Input Clamp Voltage			$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current			$V_{IL} = 0.4V$			−200	μA
I_{IH}	Input High Current			$V_{IH} = 2.4V$			20	μA
I_{IN}	Input Current	DO/RI, $\overline{DO}$/$\overline{RI}$ RI, $\overline{RI}$	$V_{CC} = 0V$ or 5.25V $\overline{RE}$/DE or DE = 0V	$V_{IN} = 12V$			+1.0	mA
				$V_{IN} = -7V$			−0.8	mA
I_{OZD}	TRI-STATE Current DS3697 & DS3698	DO, $\overline{DO}$	$V_{CC} = 0V$ or 5.25V, E = 0V $-7V < V_O < +12V$				±100	μA
V_{TH}	Differential Input Threshold Voltage for Receiver		$-7V \le V_{CM} \le +12V$		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400$ μA		2.4			V
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16$ mA (Note 5)				0.5	V
		$\overline{TS}$	$I_{OL} = 8$ mA				0.45	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max $0.4V \le V_O \le 2.4V$				±20	μA
R_{IN}	Receiver Input Resistance		$-7V \le V_{CM} \le +12V$		12			kΩ
I_{CC}	Supply Current		No Load (Note 5)	Driver Outputs Enabled		42	60	mA
				Driver Outputs Disabled		27	40	mA

Electrical Characteristics (Continued)

$0°C \le T_A \le +70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 5)			−250	mA
		$V_O = +12V$ (Note 5)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$	−15		−85	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: Derate linearly at 11.1 mW/°C to 570 mW at 70°C.

Note 5: All limits for which Note 5 is applied must be derated by 10% for DS3695T and DS3696T. Other parameters remain the same for this extended temperature range device ($-40°C \le T_A \le +85°C$).

Switching Characteristics

$0°C \le T_A \le +70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 3, 6)

Receiver Switching Characteristics *(Figures 2, 3 and 4)*

Symbol	Conditions	Min	Typ	Max	Units
t_{PLH}	$C_L = 15$ pF S1 and S2 Closed	15	25	37	ns
t_{PHL}		15	25	37	ns
$\lvert t_{PLH} - t_{PHL} \rvert$		0			ns
t_{PLZ}	$C_L = 15$ pF, S2 Open	5	12	16	ns
t_{PHZ}	$C_L = 15$ pF, S1 Open	5	12	16	ns
t_{PZL}	$C_L = 15$ pF, S2 Open	7	15	20	ns
t_{PZH}	$C_L = 15$ pF, S1 Open	7	15	20	ns

Driver Switching Characteristics

Symbol	Conditions	Min	Typ	Max	Units
SINGLE ENDED CHARACTERISTICS *(Figures 5, 6 and 7)*					
t_{PLH}	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF	9	15	22	ns
t_{PHL}		9	15	22	ns
$t_{SKEW} \lvert t_{PLH} - t_{PHL} \rvert$			2	8	ns
t_{PLZ}	$C_L = 15$ pF, S2 Open	7	15	30	ns
t_{PHZ}	$C_L = 15$ pF, S1 Open	7	15	30	ns
t_{PZL}	$C_L = 100$ pF, S2 Open	30	35	50	ns
t_{PZH}	$C_L = 100$ pF, S1 Open	30	35	50	ns
DIFFERENTIAL CHARACTERISTICS (*Figures 5* and *8*)					
t_r, t_f	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF	6	10	18	ns

Note 6: Switching Characteristics apply for DS3695, DS3695T, DS3696, DS3696T, DS3697 only.

AC Test Circuits and Switching Waveforms

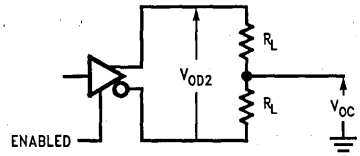

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FIGURE 1. Driver V_{OD} and V_{OC}

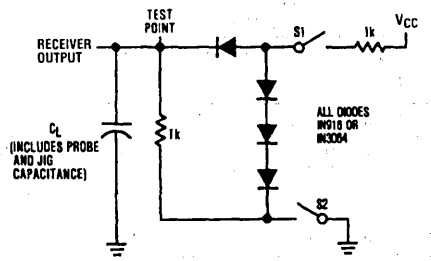

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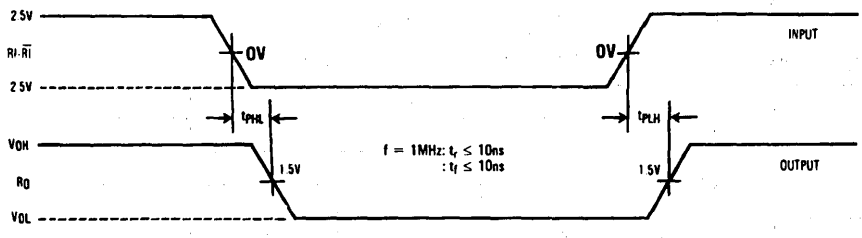
FIGURE 2. Receiver Propagation Delay Test Circuit



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Note: Differential input voltage may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V.

FIGURE 3. Receiver Input-to-Output Propagation Delay Timing

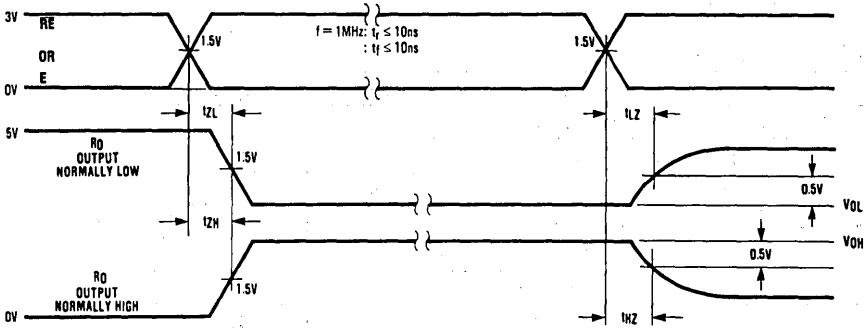

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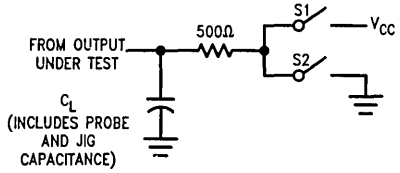
FIGURE 4. Receiver Enable/Disable Propagation Delay Timing

AC Test Circuits and Switching Waveforms (Continued)



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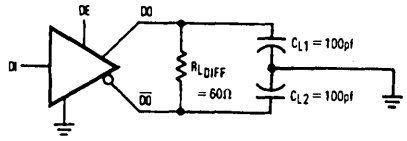

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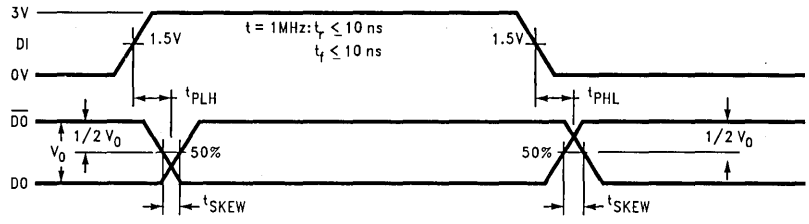
Note: Unless otherwise specified the switches are closed.

FIGURE 5. Driver Propagation Delay and Transition Time Test Circuits



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Note: t_{PLH} and t_{PHL} are measured to the respective 50% points. t_{SKEW} is the difference between propagation delays of the complementary outputs.

FIGURE 6. Driver Input-to-Output Propagation Delay Timing (Single-Ended)

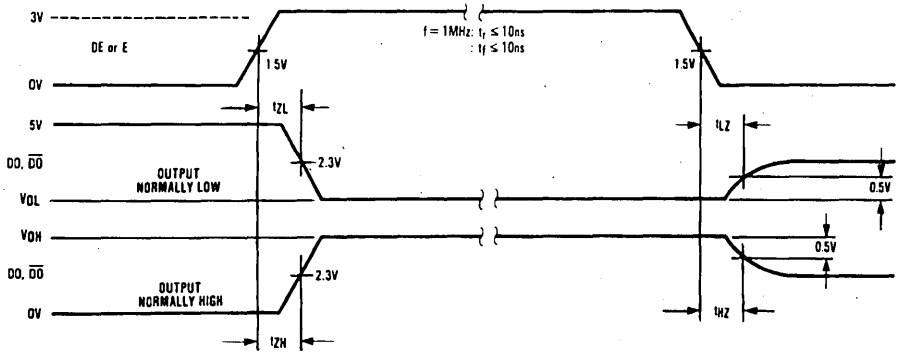

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FIGURE 7. Driver Enable/Disable Propagation Delay Timing

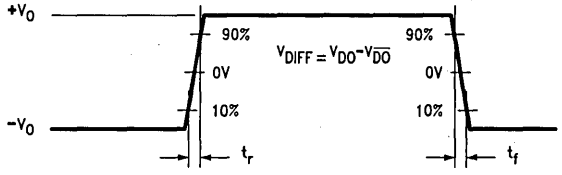

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FIGURE 8. Driver Differential Transition Timing

Function Tables

DS3695/DS3696 Transmitting

Inputs			Thermal Shutdown	Outputs		
$\overline{RE}$	DE	DI		$\overline{DO}$	DO	$\overline{TS}$* (DS3696 Only)
X	1	1	OFF	0	1	H
X	1	0	OFF	1	0	H
X	0	X	OFF	Z	Z	H
X	1	X	ON	Z	Z	L

DS3695/DS3696 Receiving

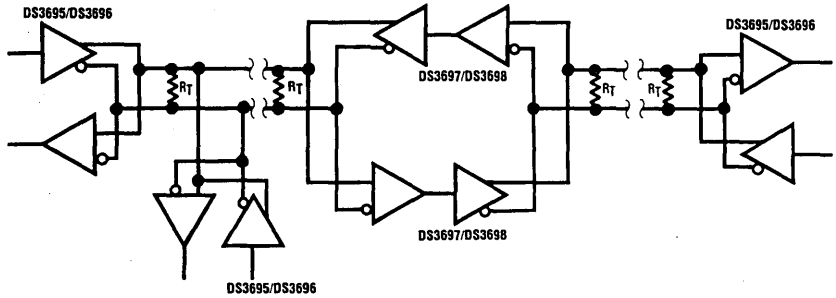
Inputs			Outputs	
$\overline{RE}$	DE	RI-$\overline{RI}$	RO	$\overline{TS}$* (DS3696 Only)
0	0	$\geq +0.2V$	1	H
0	0	$\leq -0.2V$	0	H
1	0	X	Z	H

DS3697/DS3698

Inputs		Thermal Shutdown	Outputs			
E	RI-$\overline{RI}$		$\overline{DO}$	DO	RO (DS3697 Only)	$\overline{TS}$* (DS3698 Only)
1	$\geq +0.2V$	OFF	0	1	1	H
1	$\leq -0.2V$	OFF	1	0	0	H
0	X	OFF	Z	Z	Z	H
1	$\geq +0.2V$	ON	Z	Z	1	L
1	$\leq -0.2V$	ON	Z	Z	0	L

X—Don't care condition
Z—High impedance state
*$\overline{TS}$ is an "open collector" output with an on-chip 10 kΩ pull-up resistor that reports the occurrence of a thermal shutdown of the device.

Typical Application



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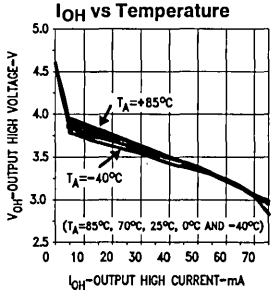
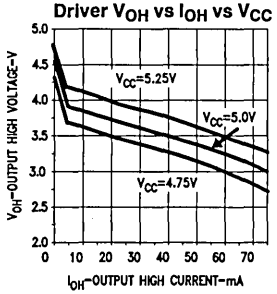
Note: Repeater control logic not shown, see AN-702.

Typical Performance Characteristics

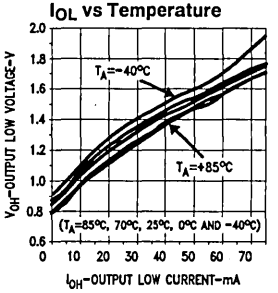
Driver V_{OH} vs I_{OH} vs Temperature



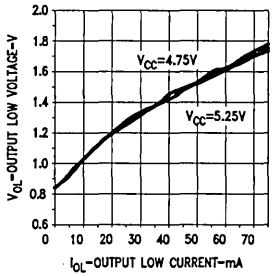
Driver V_{OH} vs I_{OH} vs V_{CC}



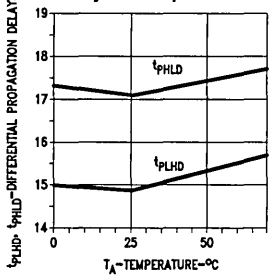
Driver V_{OL} vs I_{OL} vs Temperature



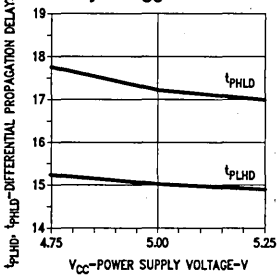
Driver V_{OL} vs I_{OL} vs V_{CC}



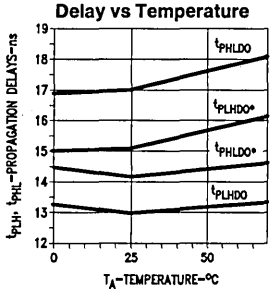
Driver Differential Propagation Delay vs Temperature



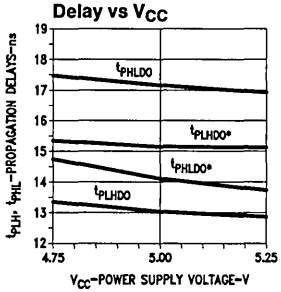
Driver Differential Propagation Delay vs V_{CC}



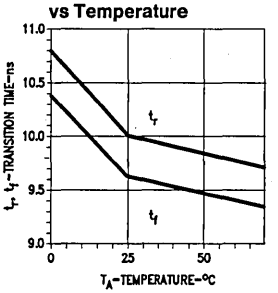
Driver Single-Ended Propagation Delay vs Temperature



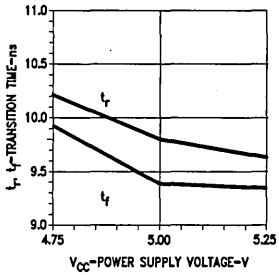
Driver Single-Ended Propagation Delay vs V_{CC}



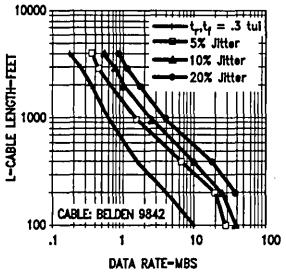
Driver Transition Time vs Temperature



Driver Transition Time vs V_{CC}



Cable Length vs Data Rate



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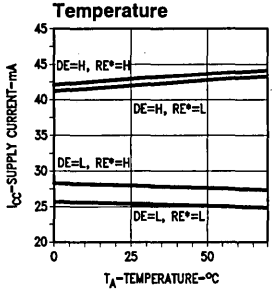
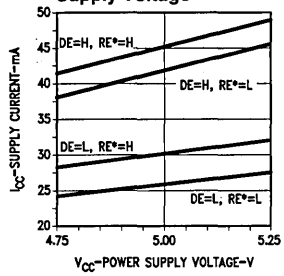
Typical Performance Characteristics (Continued)

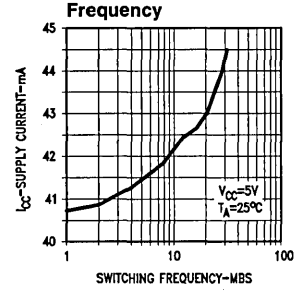
Supply Current vs Temperature



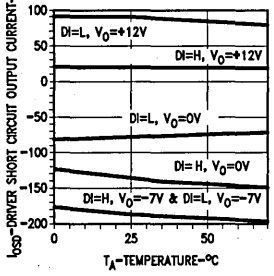
Supply Current vs Power Supply Voltage



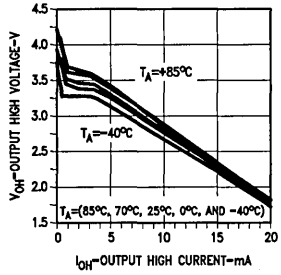
Driver I_{CC} vs Switching Frequency



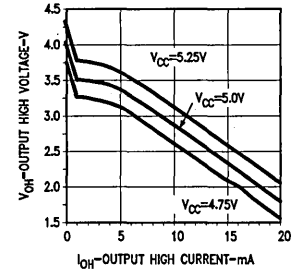
Driver Short Circuit Current vs Temperature



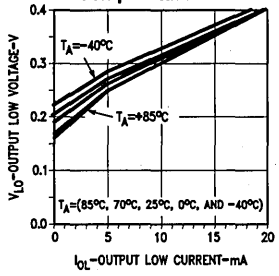
Receiver V_{OH} vs I_{OH} vs Temperature



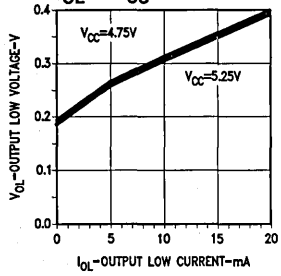
Receiver V_{OH} vs I_{OH} vs V_{CC}



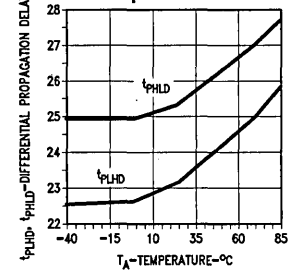
Receiver V_{OL} vs I_{OL} vs Temperature



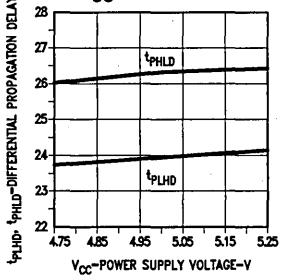
Receiver V_{OL} vs I_{OL} vs V_{CC}



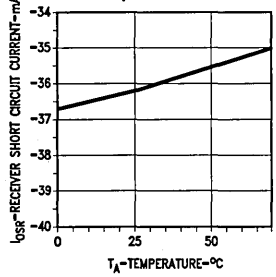
Receiver Differential Propagation Delay vs Temperature



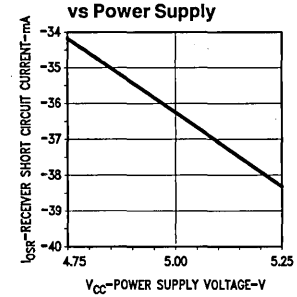
Receiver Differential Propagation Delay vs V_{CC}



Receiver Short Circuit Current vs Temperature



Receiver Short Circuit Current vs Power Supply



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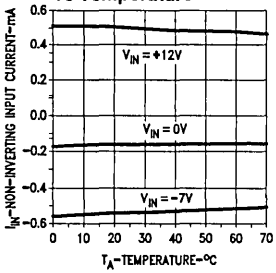
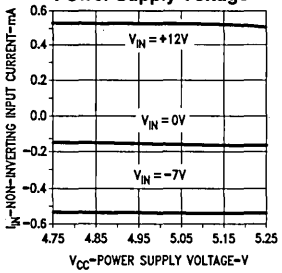
Typical Performance Characteristics (Continued)

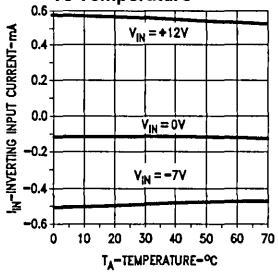
Receiver Non-Inverting Input Current vs Temperature



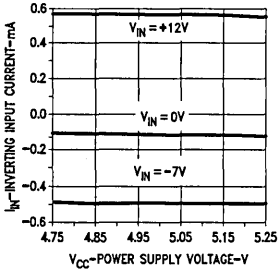
Receiver Non-Inverting Input Current vs Power Supply Voltage



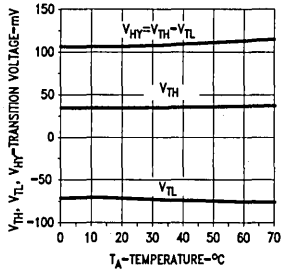
Receiver Inverting Input Current vs Temperature



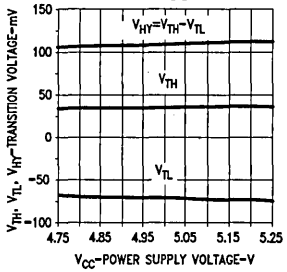
Receiver Inverting Input Current vs Power Supply Voltage



Hysteresis and Differential Transition Voltage vs Temperature



Hysteresis and Differential Transition Voltage vs V_{CC}



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3

National Semiconductor

DS3695A/DS3695AT/DS3696A Multipoint RS485/RS422 Transceivers

General Description

The DS3695A and DS3696A are high speed differential TRI-STATE® bus/line transceivers designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition they are compatible with requirements of RS-422.

The driver and receiver outputs feature TRI-STATE capability. The driver outputs remain in TRI-STATE over the entire common mode range of +12V to −7V. Bus faults that cause excessive power dissipation within the device trigger a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696A provides an output pin (TS) which reports the thermal shutdown of the device. TS is an "open collector" pin with an internal 10 kΩ pull-up resistor. This allows the TS outputs of several devices to be wire OR-ed.

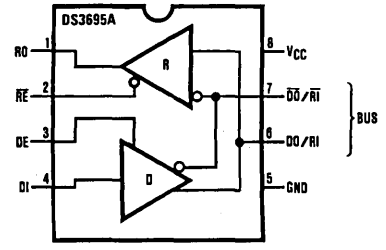
Both AC and DC specifications are guaranteed over the 0°C to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422
- 10 ns driver propagation delays (typical)
- Single +5V supply
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus
- Thermal shutdown protection
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus
- 70 mV typical receiver hysteresis
- Available in SOIC packaging

Connection and Logic Diagram

Molded Package, Small Outline (M)



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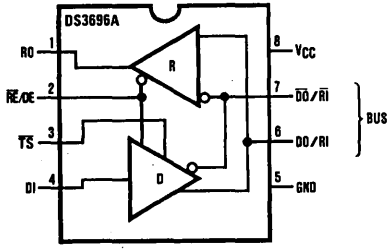
Top View



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Top View

Note: $\overline{TS}$ was $\overline{LF}$ (Line Fault) on previous datasheets, $\overline{TS}$ goes low upon thermal shutdown.

Order Number DS3695AM, DS3695ATM or DS3696AM
See NS Package Number M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/−10V
Receiver Input Voltages	+15V/−10V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ 25°C	
M Package	630 mW (Note 4)
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Free Air Temp. (T_A)			
Commercial (DS3695AM)	0	+70	°C
Industrial (DS3695ATM)	−40	+85	°C
Commercial (DS3696AM)	0	+70	°C

Electrical Characteristics $0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)			R = 50Ω; (RS-422) (Note 5)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States			R = 27Ω			0.2	V
V_{OC}	Driver Common Mode Output Voltage						3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, $R\overline{E}/DE$			2			V
V_{IL}	Input Low Voltage						0.8	V
V_{CL}	Input Clamp Voltage			$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current			$V_{IL} = 0.4V$			−200	μA
I_{IH}	Input High Current			$V_{IH} = 2.4V$			20	μA
I_{IN}	Input Current	DO/RI, $\overline{DO}/\overline{RI}$ RI, $\overline{RI}$	$V_{CC} = 0V$ or 5.25V DE or $R\overline{E}/DE = 0V$	$V_{IN} = 12V$			+1.0	mA
				$V_{IN} = -7V$			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver		$-7V \le V_{CM} \le +12V$		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400$ μA		2.4			V
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16$ mA (Note 5)				0.5	V
		$\overline{TS}$	$I_{OL} = 8$ mA				0.45	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max $0.4V \le V_O \le 2.4V$				±20	μA
R_{IN}	Receiver Input Resistance		$-7V \le V_{CM} \le +12V$		12			kΩ
I_{CC}	Supply Current		No Load (Note 5)	Driver Outputs Enabled		42	60	mA
				Driver Outputs Disabled		27	40	mA

3

Electrical Characteristics

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 5)			−250	mA
		$V_O = +12V$ (Note 5)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$	−15		−85	mA

Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: Derate linearly at 6.5 mW/°C to 337 mW at 70°C.

Note 5: All limits for which Note 5 is applied must be derated by 10% for DS3695AT. Other parameters remain the same for this extended temperature range device ($-40°C \le T_A \le +85°C$).

Switching Characteristics

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Note 3)

Receiver Switching Characteristics (*Figures 1, 2* and *3*)

Symbol	Conditions	Min	Typ	Max	Units
t_{PLH}	$C_L = 15$ pF S1 and S2 Closed	15	28	42	ns
t_{PHL}		15	28	42	ns
$\lvert t_{PLH} - t_{PHL} \rvert$		0	3		ns
t_{PLZ}	$C_L = 15$ pF, S2 Open	5	29	35	ns
t_{PHZ}	$C_L = 15$ pF, S1 Open	5	12	16	ns
t_{PZL}	$C_L = 15$ pF, S2 Open	7	15	28	ns
t_{PZH}	$C_L = 15$ pF, S1 Open	7	15	20	ns

Driver Switching Characteristics

Symbol	Conditions	Min	Typ	Max	Units
SINGLE ENDED CHARACTERISTICS (*Figures 4, 5* and *6*)					
t_{PLH}	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF	9	15	22	ns
t_{PHL}		9	15	22	ns
$t_{SKEW} \lvert t_{PLH} - t_{PHL} \rvert$		0	2	8	ns
t_{PLZ}	$C_L = 15$ pF, S2 Open	7	15	30	ns
t_{PHZ}	$C_L = 15$ pF, S1 Open	7	15	30	ns
t_{PZL}	$C_L = 100$ pF, S2 Open	30	35	50	ns
t_{PZH}	$C_L = 100$ pF, S1 Open	30	35	50	ns
DIFFERENTIAL SWITCHING CHARACTERISTICS (*Figure 7*)					
t_r, t_f	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF	6	10	18	ns

AC Test Circuits and Switching Waveforms

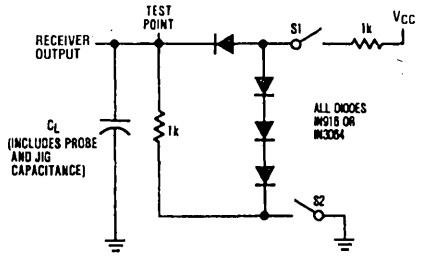

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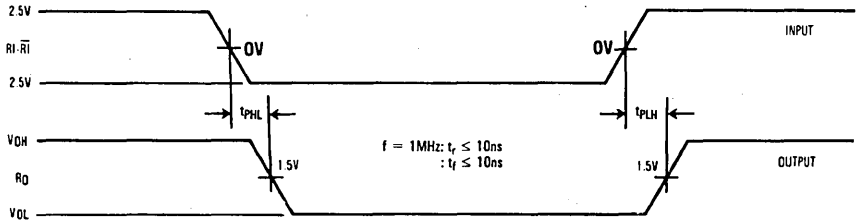
FIGURE 1. Receiver Propagation Delay Test Circuit



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Note: Differential input voltage may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 2. Receiver Input-to-Output Propagation Delay Timing

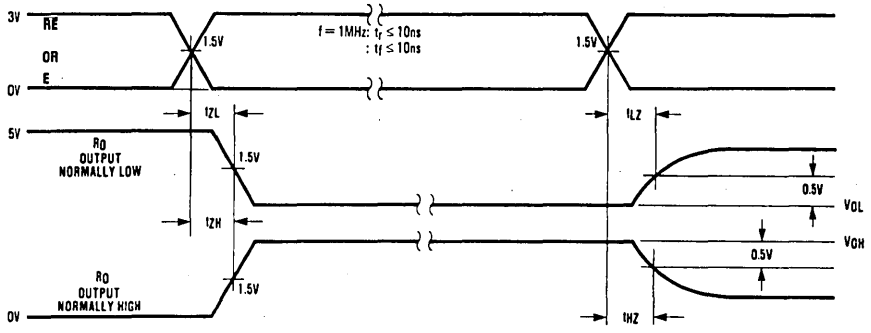

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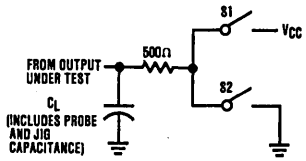
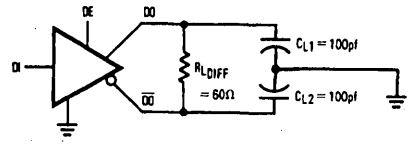
FIGURE 3. Receiver Enable/Disable Propagation Delay Timing

AC Test Circuits and Switching Waveforms (Continued)





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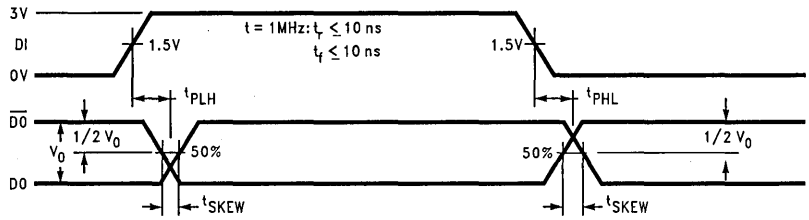
Note: Unless otherwise specified the switches are closed.

FIGURE 4. Driver Propagation Delay Test Circuits



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Note: t_{PLH} and t_{PHL} are measured to the respective 50% points. t_{SKEW} is the difference between propagation delays of the complementary outputs.

FIGURE 5. Driver Input-to-Output Propagation Delay Timing (Single-Ended)

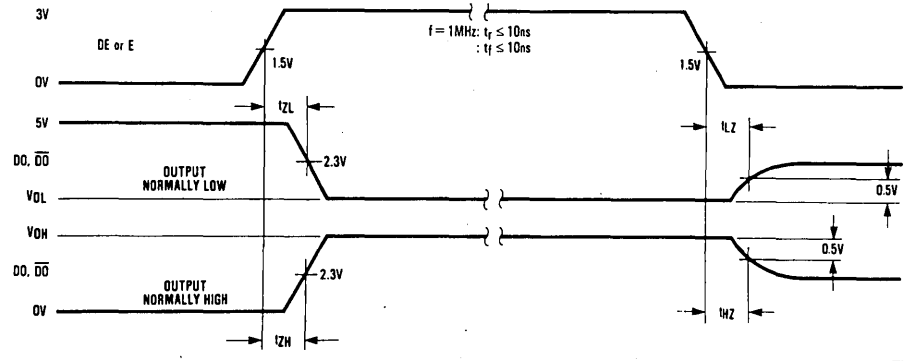

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FIGURE 6. Driver Enable/Disable Propagation Delay Timing

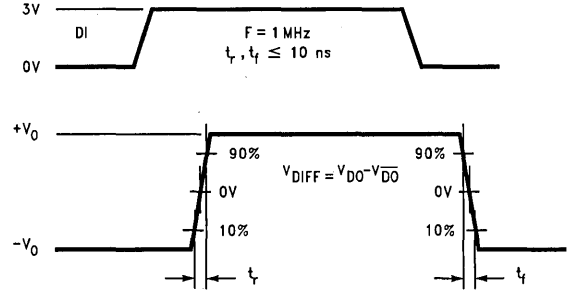

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FIGURE 7. Driver Differential Transition Timing

Function Tables

DS3695A/DS3696A Transmitting

Inputs			Line Condition	Outputs		
$\overline{RE}$	DE	DI		$\overline{DO}$	DO	$\overline{TS}$* (DS3696A Only)
X	1	1	No Fault	0	1	H
X	1	0	No Fault	1	0	H
X	0	X	X	Z	Z	H
X	1	X	Fault	Z	Z	L

DS3695A/DS3696A Receiving

Inputs			Output	
$\overline{RE}$	DE	RI–$\overline{RI}$	RO	$\overline{TS}$* (DS3696A Only)
0	0	≥ +0.2V	1	H
0	0	≤ −0.2V	0	H
0	0	Inputs Open**	1	H
1	0	X	Z	H

X — Don't care condition

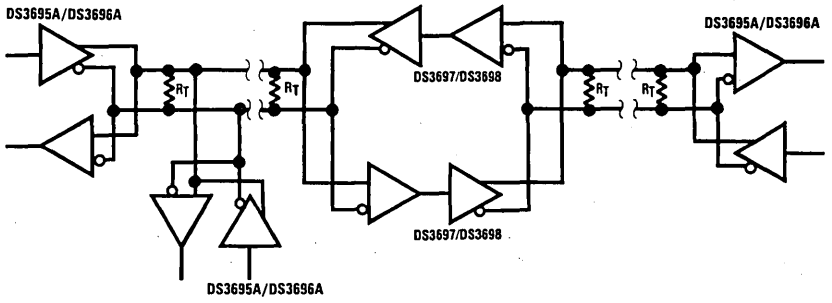
Z — High impedance state

Fault — Improper line conditions causing excessive power dissipation in the driver, such as shorts or bus contention situations

* $\overline{TS}$ is an "open collector" output with an on-chip 10 kΩ pull-up resistor.

** **This is a fail safe condition**

Typical Application



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Note: Repeater control logic not shown. See AN-702.

National Semiconductor

DS16F95, DS36F95
EIA-485/EIA-422A Differential Bus Transceiver

General Description

The DS16F95/DS36F95 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets both EIA-485 and EIA-422A standards.

The DS16F95/DS36F95 offers improved performance due to the use of L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by minimizing gate delay times. Thus, the DS16F95 and DS36F95 consume less power, and feature an extended temperature range as well as improved specifications.

The DS16F95/DS36F95 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

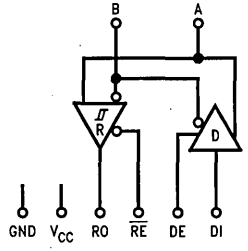
The driver is designed to accommodate loads of up to 60 mA of sink or source current and features positive and negative current limiting in addition to thermal shutdown for protection from line fault conditions.

The DS16F95/DS36F95 can be used in transmission line applications employing the DS96F172 and the DS96F174 quad differential line drivers and the DS96F173 and DS96F175 quad differential line receivers.

Features

- Meets EIA-485 and EIA-422A
- Meets SCSI-1 (5 MHZ) specifications
- Designed for multipoint transmission
- Wide positive and negative input/output bus voltage ranges
- Thermal shutdown protection
- Driver positive and negative current-limiting
- High impedance receiver input
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Reduced power consumption
- Pin compatible with DS3695 and SN75176A
- Military temperature range available
- Qualified for MIL-STD 883C
- Standard Military Drawings (SMD) available
- Available in DIP (J), LCC (E), and Flatpak (W) packages

Logic Diagram



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Function Tables

Driver

Driver Input	Enable	Outputs	
DI	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A–B	**$\overline{RE}$**	**RO**
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

COMMERCIAL

Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately on the following pages.

Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation* at 25°C 'J' Package	1300 mW
Supply Voltage	7.0V
Input Voltage (Bus Terminal)	+15V/−10V
Enable Input Voltage	5.5V

*Derate 'J' package 8.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS36F95	4.75	5.0	5.25	V
DS16F95	4.50	5.0	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0		+12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)				
DS36F95	0	+25	+70	°C
DS16F95	−55	+25	+125	°C

Driver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −55 mA	0°C to +70°C	3.0			V
V_{OL}	Output Voltage LOW	I_{OL} = 55 mA	0°C to +70°C			2.0	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.3	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, *Figure 1*		2.0	2.25		V
		R_L = 54Ω, *Figure 1*		1.5	2.0		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*	−40°C to +125°C			±0.2	V
			−55°C to +125°C			±0.4	
V_{OC}	Common Mode Output Voltage (Note 5)					3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current (Note 8) (Includes Receiver I_I)	Output Disabled	V_O = +12V			1.0	mA
			V_O = −7.0V			−0.8	
I_{IH}	Input Current HIGH	V_I = 2.4V				20	μA
I_{IL}	Input Current LOW	V_I = 0.4V				−50	μA
I_{OS}	Short Circuit Output Current (Note 9)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = +12V				250	
I_{CC}	Supply Current (Total Package)	No Load, All Inputs Open	DE = 2V, $\overline{RE}$ = 0.8V Outputs Enabled			28	mA
I_{CCX}			DE = 0.8V, $\overline{RE}$ = 2V Outputs Disabled			25	

COMMERCIAL

Driver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 3*	8.0	15	20	ns
t_{TD}	Differential Output Transition Time		8.0	15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 4*	6.0	12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		6.0	12	16	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 5*		25	32	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 6*		25	32	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 5*		20	25	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 6*		20	25	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND	Load per *Figure 5* Timing per *Figure 6*		300		ns
t_{SKEW}	Driver Output to Output	R_L = 60Ω		1.0	4.0	ns

Receiver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = 0.5V, I_O = 8.0 mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	V_{CM} = 0V		35	50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.3	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 2*	0°C to +70°C	2.8			V
			−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV, *Figure 2*	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High Impedance State Output	V_O = 0.4V to 2.4V				±20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V	V_I = +12V			1.0	mA
			V_I = −7.0V			0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−50	μA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load, All Inputs Open	DE = 2V, $\overline{RE}$ = 0.8V Outputs Enabled			28	mA
I_{CCX}			DE = 0.8V, $\overline{RE}$ = 2V Outputs Disabled			25	

COMMERCIAL

Receiver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to +3.0V, C_L = 15 pF, *Figure 7*	14	19	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		14	19	24	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 8*		10	16	ns
t_{ZL}	Output Enable Time to Low Level			12	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 8*		12	20	ns
t_{LZ}	Output Disable Time from Low Level			12	18	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 7*		1.0	4.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16F95 and across the 0°C to +70°C range for the DS36F95. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Note 5: In TIA/EIA-422A and TIA/EIA-485 Standards, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

Note 8: Refer to TIA/EIA-485 Standard for exact conditions.

Note 9: Only one output at a time should be shorted.

Order Number: DS16F95J, NS Package Number J08A
DS36F95J, NS Package Number J08A

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MIL-STD 883C

Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the RETS please contact your local National Semiconductor sales office or distributor.

Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Power Dissipation* at 25°C	
Ceramic 'E' Package	1800 mW
Ceramic 'J' Package	1300 mW
Ceramic 'W' Package	TBD
Supply Voltage	7.0V
Input Voltage (Bus Terminal)	+15V/−10V
Enable Input Voltage	5.5V

*Above T_A = 25°C, derate E package, J package 8.7 mW/°C, W package 12.5 mW/°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC}) DS16F95	4.50	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0	+12	V
Differential Input Voltage (V_{ID})		±12	V
Output Current HIGH (I_{OH})			
Driver		−60	mA
Receiver		−400	μA
Output Current LOW (I_{OL})			
Driver		60	mA
Receiver		16	mA
Operating Temperature (T_A) DS16F95	−55	+125	°C

Driver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	Input Voltage HIGH	V_{CC} = 5.5V		2.0		V
V_{IL}	Input Voltage LOW	V_{CC} = 5.5V			0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA, V_{CC} = 4.5V		3.0		V
V_{OL}	Output Voltage LOW	I_{OL} = +20 mA, V_{CC} = 4.5V			2.0	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA			−1.3	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA, V_{IN} = 0.8V or 2V, V_{CC} = 5.5V			6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, V_{CC} = 4.5V, *Figure 1*		2.0		V
		R_L = 54Ω, V_{CC} = 4.5V, *Figure 1*		1.5		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*, V_{CC} = 4.5V			±0.2	V
V_{OD3}	Differential Output Voltage	V_{CM} = −7V to +12V		1.0		V
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω			3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)	V_{CC} = 4.5V, R_L = 54Ω or 100Ω			±0.2	V
I_O	Output Current (Note 8) (Includes Receiver I_I)	Output Disabled V_{CC} = 0V or 5.5V	V_O = +12V		1.0	mA
			V_O = −7.0V		−0.8	
I_{IH}	Input Current HIGH	V_I = 2.4V			20	μA
I_{IL}	Input Current LOW	V_I = 0.4V			−50	μA
I_{OS}	Short Circuit Output Current (Note 9)	V_O = −7.0V, V_{IN} = 0V or 3V			−250	mA
		V_O = 0V, V_{IN} = 0V or 3V			−150	
		V_O = V_{CC}, V_{IN} = 0V or 3V			150	
		V_O = +12V, V_{IN} = 0V or 3V			250	
I_{CC}	Supply Current (Total Package)	No Load, DE = 2V, $\overline{RE}$ = 0.8V, Inputs Open			28	mA
I_{CCX}		No Load, DE = 0.8V, $\overline{RE}$ = 2V, Inputs Open			25	

MIL-STD 883C

Driver Switching Characteristics V_{CC} = 5.0V

Symbol	Parameter	Conditions	Min	Typ	T_A = 25°C Max	T_A = 125°C Max	T_A = −55°C Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 3*	8.0	15	25	30	30	ns
t_{TD}	Differential Output Transition Time		8.0	15	25	30	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 4*	6.0	12	18	25	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		6.0	12	18	25	25	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 5*		25	35	45	45	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 6*		25	40	50	50	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 5*		20	30	40	40	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 6*		20	30	40	40	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND	Load per *Figure 5* Timing per *Figure 6*		300				ns
t_{SKEW}	Driver Output to Output	R_L = 60Ω		1.0	6	12	12	ns

Receiver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.5V, I_O = −0.4 mA, V_{CM} = −7V, 0V, +12V V_{CC} = 4.5V, 5.5V			0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = 0.5V, I_O = 8.0 mA, V_{CM} = −7V, 0V, +12V, V_{CC} = 4.5V, 5.5V		−0.2		V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	V_{CM} = 0V, V_{CC} = 4.5V, 5.5V		35		mV
V_{IH}	Enable Input Voltage HIGH			2.0		V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA, V_{CC} = 5.5V			−1.3	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 2*, V_{CC} = 4.5V	−55°C to +125°C	2.5		V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV, *Figure 2*, V_{CC} = 4.5V	I_{OL} = 8.0 mA		0.45	V
			I_{OL} = 16 mA		0.50	
I_{OZ}	High Impedance State Output	V_O = 0.4V, 2.4V			±20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V V_{CC} = 5.5V or V_{CC} = 0V	V_I = +12V		1.0	mA
			V_I = −7.0V	−0.8		
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V			20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V			−50	μA
R_I	Input Resistance			10		kΩ
I_{OS}	Short Circuit Output Current	V_{IN} = 1V, V_{OUT} = 0.0V (Note 9)		−15	−85	mA
I_{CC}	Supply Current (Total Package)	No Load, DE = 2V, $\overline{RE}$ = 0.8V, Inputs Open			28	mA
I_{CCX}		No Load, DE = 0.8V, $\overline{RE}$ = 2.0V, Inputs Open			25	

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MIL-STD 883C

Receiver Switching Characteristics V_{CC} = 5.0V

Symbol	Parameter	Conditions	Min	Typ	T_A = 25°C Max	T_A = 125°C Max	T_A = −55°C Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to +3.0V C_L = 15 pF, *Figure 7*	10	19	27	38	38	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	19	27	38	38	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 8*		10	20	30	30	ns
t_{ZL}	Output Enable Time to Low Level			12	20	30	30	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 8*		12	20	30	30	ns
		C_L = 20.0 pF, *Figure 8* (Note 14)		12	30	40	40	ns
t_{LZ}	Output Disable Time from Low Level	C_{IL} = 50 pF, *Figure 8*		12	20	30	30	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 7*		1.0	8	16	16	ns

Ordering Number: **DS16F95J/883, NS Package Number J08A**
DS16F95E/883, NS Package Number E20A
DS16F95W/883, NS Package Number W10A

SMD Number: **DS16F95J/883 ⟷ 5962-896150PX**
DS16F95E/883 ⟷ 5962-8961502X
DS16F95W/883 ⟷ 5962-896150HX

Parameter Measurement Information

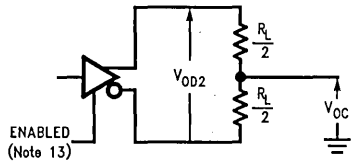

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FIGURE 1. Driver V_{OD} and V_{OC}

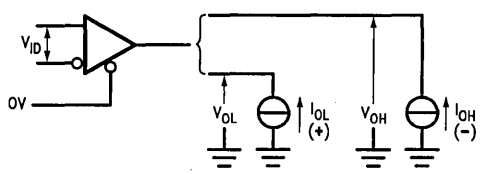

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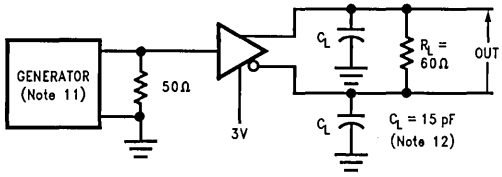
FIGURE 2. Receiver V_{OH} and V_{OL}



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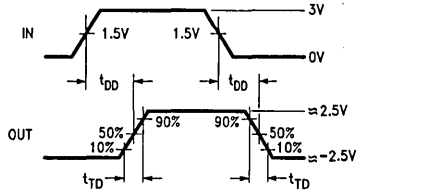

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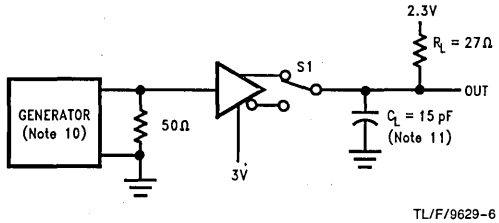
FIGURE 3. Driver Differential Output Delay and Transition Times



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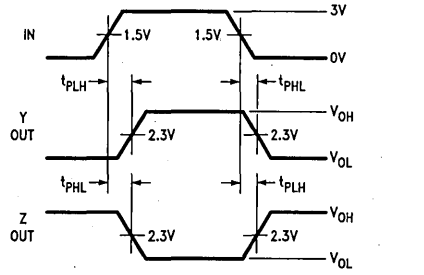

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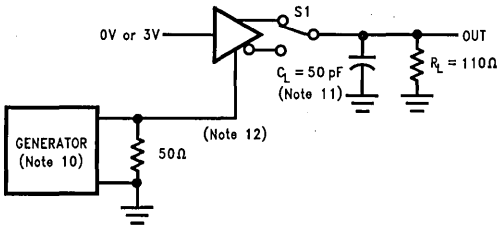
FIGURE 4. Driver Propagation Times



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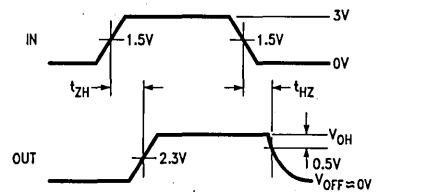

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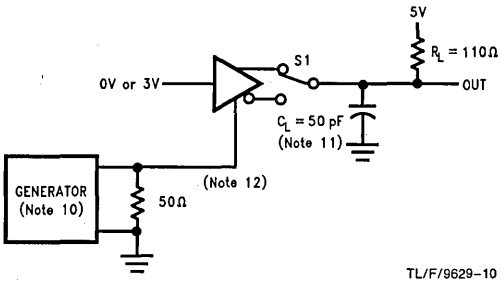
FIGURE 5. Driver Enable and Disable Times (t_{ZH}, t_{HZ})



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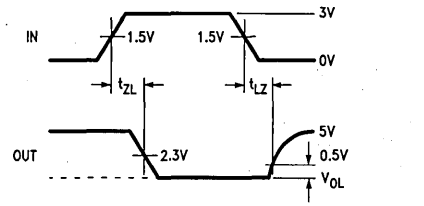

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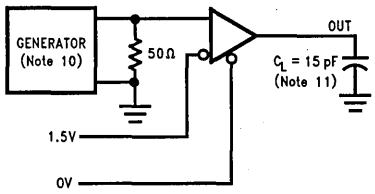
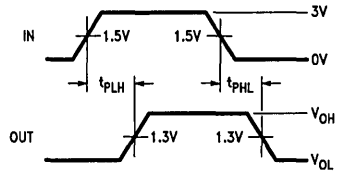
FIGURE 6. Driver Enable and Disable Times (t_{ZL}, t_{LZ}, t_{LZL})

Parameter Measurement Information (Continued)

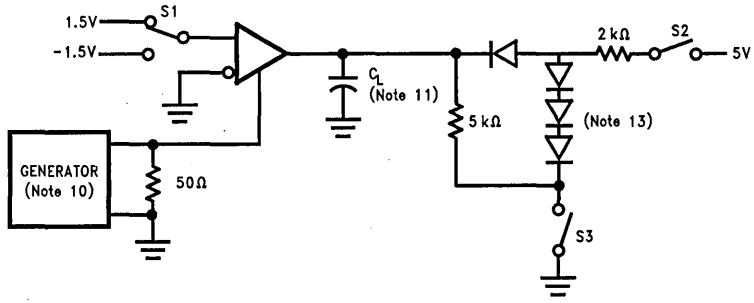


TL/F/9629-12

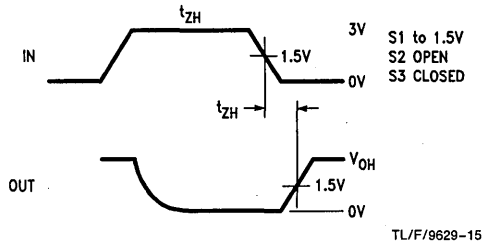


TL/F/9629-13

FIGURE 7. Receiver Propagation Delay Times



TL/F/9629-14



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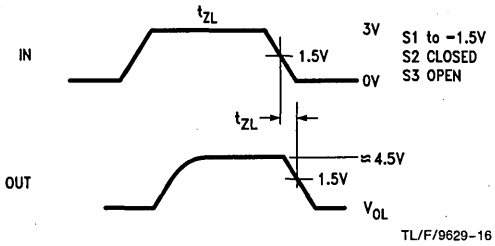
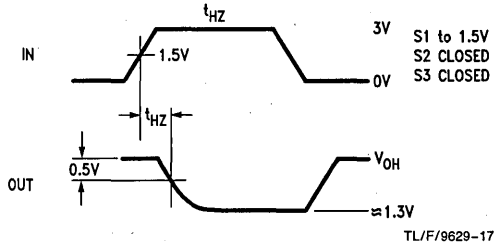


TL/F/9629-16



TL/F/9629-17

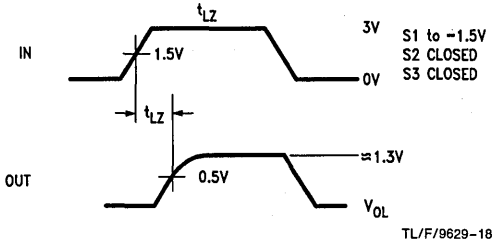


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FIGURE 8. Receiver Enable and Disable Times

Note 10: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

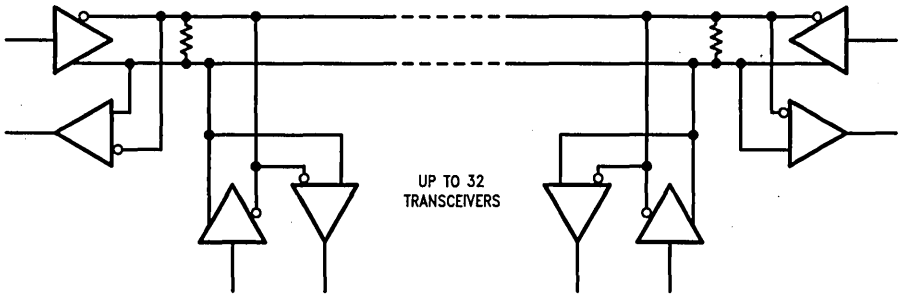
Note 11: C_L includes probe and stray capacitance.

Note 12: DS16F95/DS36F95 Driver enable is Active-High.

Note 13: All diodes are 1N916 or equivalent.

Note 14: Testing at 20 pF assures conformance to 5 pF specification.

Typical Application



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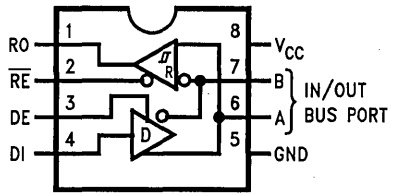
Note:

The line should be terminated at both ends in its characteristic impedance, typically 120Ω.
Stub lengths off the main line should be kept as short as possible.

Connection Diagrams

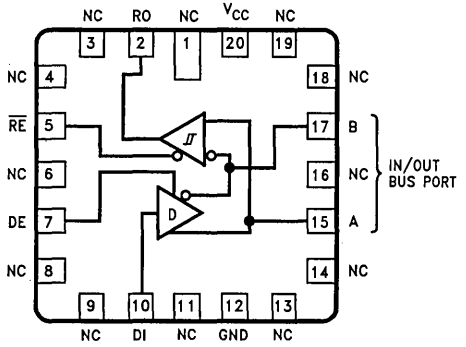
8-Lead Dual-In-Line Package



TL/F/9629–1

Order Number DS16F95, DS16F95J/883, DS36F95J
See NS Package Number J08A

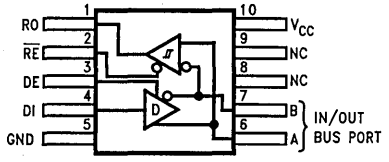
20-Lead Ceramic Leadless Chip Carrier



TL/F/9629–21

Order Number DS16F95E/883
See NS Package Number E20A

10-Lead Ceramic Flatpak



TL/F/9629–22

Order Number DS16F95W/883
See NS Package Number W10A

For Complete Military 883 Specifications, See RETS Data Sheet

3

National Semiconductor

DS36276
FAILSAFE Multipoint Transceiver

General Description

The DS36276 FAILSAFE Multipoint Transceiver is designed for use on bi-directional differential busses. It is compatible with existing TIA/EIA-485 transceivers, however, it offers an additional feature not supported by standard transceivers.

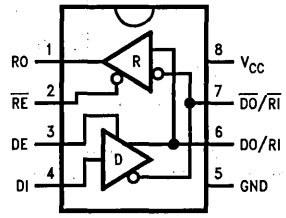
The FAILSAFE feature guarantees the receiver output to a known state when the Interface is in the following conditions: Floating Line, Idle Line (no active drivers), and Line Fault conditions (open or short). The receiver output is in a HIGH state for the following conditions: OPEN Inputs, Terminated Inputs (50Ω), and SHORTED Inputs.

FAILSAFE is a highly desirable feature when the transceivers are used with Asynchronous Controllers such as UARTs.

Features

- FAILSAFE receiver, RO = HIGH for:
  - — OPEN inputs
  - — Terminated inputs
  - — SHORTED inputs
- Compatible with popular interface standards:
  - — TIA/EIA-485 (RS-485)
  - — TIA/EIA-422-A (RS-422-A)
  - — CCITT Recommendation V.11
- Bi-Directional Transceiver
  - — Designed for multipoint transmission
- Separate driver input, driver enable, receiver enable, and receiver output for maximum flexibility
- Wide bus common mode range
  - — (−7V to +12V)
- Pin compatible with: DS75176B, DS96176, DS3695 and SN75176A and B
- Available in plastic DIP and SOIC packages

Connection and Logic Diagram



TL/F/11383–1

Order Number DS36276N or DS36276M
See NS Package Number N08E or M08A

Truth Tables

Driver

Inputs			Outputs	
$\overline{RE}$	DE	DI	DO/RI	$\overline{DO}/\overline{RI}$
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z

Receiver

Inputs			Output
$\overline{RE}$	DE	RI−$\overline{RI}$	RO
L	L	≥0V	H
L	L	≤−500 mV	L
H	X	X	Z

Receiver FAILSAFE

Inputs			Output
$\overline{RE}$	DE	RI−$\overline{RI}$	RO
L	L	SHORTED	H
L	L	OPEN	H
H	X	X	Z

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Voltage (DE, $\overline{RE}$, and DI)	5.5V
Driver Output Voltage/ Receiver Input Voltage	−10V to +15V
Receiver Output Voltage (RO)	5.5V
Maximum Package Power Dissipation @ +25°C	
N Package (derate 9.3 mW/°C above +25°C)	1168 mW
M Package (derate 5.8 mW/°C above +25°C)	726 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Max Junction Temperature	150°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Temperature (T_A) DS36276	0	+70	°C

Electrical Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_{OD}	Differential Output Voltage	I_O = 0 mA (No Load)		1.5	4.8	6.0	V
V_{oDO}	Output Voltage	I_O = 0 mA (Output to GND)		0		6.0	V
$V_{o\overline{DO}}$	Output Voltage			0		6.0	V
V_{T1}	Differential Output Voltage (Termination Load)	R_L = 54Ω (485)	*(Figure 1)*	1.5	2.0	5.0	V
		R_L = 100Ω (422)		2.0	2.3	5.0	V
ΔV_{T1}	Balance of V_{T1} $\lvert V_{T1}\rvert - \lvert\overline{V_{T1}}\rvert$	R_L = 54Ω	(Note 3)	−0.2	0.07	+0.2	V
		R_L = 100Ω		−0.2	0.07	+0.2	V
V_{OS}	Driver Common Mode Output Voltage	R_L = 54Ω	*(Figure 1)*	0	2.5	3.0	V
		R_L = 100Ω		0	2.3	3.0	V
ΔV_{OS}	Balance of V_{OS} $\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	R_L = 54Ω	(Note 3)	−0.2	0.08	+0.2	V
		R_L = 100Ω		−0.2	0.08	+0.2	V
I_{OSD}	Driver Short-Circuit Output Current	V_O = +12V	*(Figure 3)*		134	290	mA
		V_O = V_{CC}			140		mA
		V_O = 0V			−140		mA
		V_O = −7V			−180	−290	mA

Electrical Characteristics (Continued)

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TH}	Differential Input High Threshold Voltage (Note 5)	$V_O = V_{OH}$, $I_O = -0.4$ mA $-7V \le V_{CM} \le +12V$				−0.18	0	V
V_{TL}	Differential Input Low Threshold Voltage (Note 5)	$V_O = V_{OL}$, $I_O = 8.0$ mA $-7V \le V_{CM} \le +12V$			−0.5	−0.23		V
V_{HST}	Hysteresis (Note 6)	$V_{CM} = 0V$				50		mV
I_{IN}	Line Input Current (V_{CC} = 4.75V, 5.25V, 0V)	Other Input = 0V DE = V_{IH} (Note 7)	$V_I = +12V$			0.7	1.0	mA
			$V_I = -7V$			−0.5	−0.8	mA
I_{OSR}	Short Circuit Current	$V_O = 0V$		RO	−5.0	−30	−85	mA
I_{OZ}	TRI-STATE® Leakage Current	V_O = 0.4 to 2.4V			−20		+20	μA
V_{OH}	Output High Voltage *(Figure 12)*	$V_{ID} = 0V$, $I_{OH} = -0.4$ mA			2.5	3.5		V
		V_{ID} = OPEN, $I_{OH} = -0.4$ mA			2.5	3.5		V
V_{OL}	Output Low Voltage *(Figure 12)*	$V_{ID} = -0.5V$, $I_{OL} = +8$ mA				0.25	0.6	V
		$V_{ID} = -0.5V$, $I_{OL} = +16$ mA				0.35	0.7	V
R_{IN}	Input Resistance				12	19		kΩ
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			DE, $\overline{RE}$, or DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	V_{IH} = 2.4V					20	μA
I_{IL}	Low Level Input Current	V_{IL} = 0.4V					−100	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA				−0.75	−1.5	V
I_{CC}	Output Low Voltage Supply Current (No Load)	DE = 3V, $\overline{RE}$ = 0V, DI = 0V				42	60	mA
I_{CCR}		DE = 0V, $\overline{RE}$ = 0V, DI = 0V				28	45	mA
I_{CCD}		DE = 3V, $\overline{RE}$ = 3V, DI = 0V				43	60	mA
I_{CCX}		DE = 0V, $\overline{RE}$ = 3V, DI = 0V				31	50	mA

Switching Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLHD}	Diff. Prop. Delay Low to High	$R_L = 54\Omega$ $C_L = 50$ pF $C_D = 50$ pF *(Figures 4, 5)*	7	21	60	ns
t_{PHLD}	Diff. Prop. Delay High to Low		7	19	60	ns
t_{SKD}	Diff. Skew ($\lvert t_{PLHD} - t_{PHLD} \rvert$)			2	10	ns
t_r	Diff. Rise Time			12	50	ns
t_f	Diff. Fall Time			12	50	ns
t_{PLH}	Prop. Delay Low to High	$R_L = 27\Omega$, $C_L = 15$ pF *(Figures 6, 7)*		22	45	ns
t_{PHL}	Prop. Delay High to Low			22	45	ns
t_{PZH}	Enable Time Z to High	$R_L = 110\Omega$ $C_L = 50$ pF *(Figures 8–11)*		32	55	ns
t_{PZL}	Enable Time Z to Low			32	65	ns
t_{PHZ}	Disable Time High to Z			22	55	ns
t_{PLZ}	Disable Time Low to Z			16	55	ns
RECEIVER CHARACTERISTICS						
t_{PLH}	Prop. Delay Low to High	$V_{ID} = -1.5$V to $+1.5$V $C_L = 15$ pF *(Figures 13, 14)*	15	40	70	ns
t_{PHL}	Prop. Delay High to Low		15	42	70	ns
t_{SK}	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			2	15	ns
t_{PZH}	Enable Time Z to High	$C_L = 15$ pF *(Figures 15, 16)*		15	50	ns
t_{PZL}	Enable Time Z to Low			17	50	ns
t_{PHZ}	Disable Time High to Z			24	50	ns
t_{PLZ}	Disable Time Low to Z			19	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: $\Delta \lvert V_{T1} \rvert$ and $\Delta \lvert V_{OS} \rvert$ are changes in magnitude of V_{T1} and V_{OS}, respectively, that occur when the input changes state.

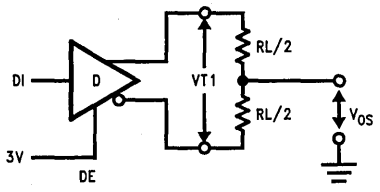
Note 4: All typicals are given for $V_{CC} = 5.0$V and $T_A = +25°C$.

Note 5: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 6: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

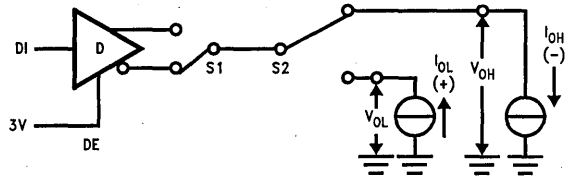
Note 7: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Parameter Measurement Information



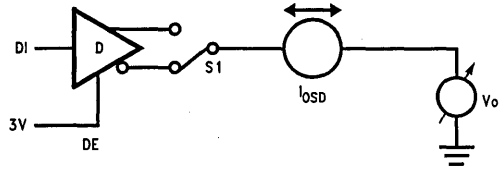
TL/F/11383–2

FIGURE 1. Driver V_{T1} and V_{OS} Test Circuit



TL/F/11383–3

FIGURE 2. Driver V_{OH} and V_{OL} Test Circuit



TL/F/11383–4

FIGURE 3. Driver Short Circuit Test Circuit

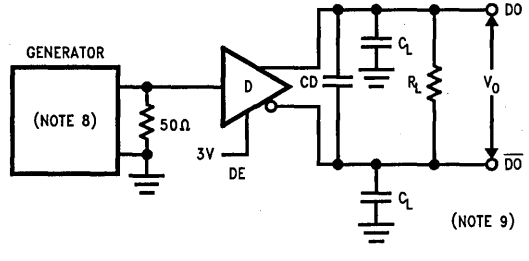


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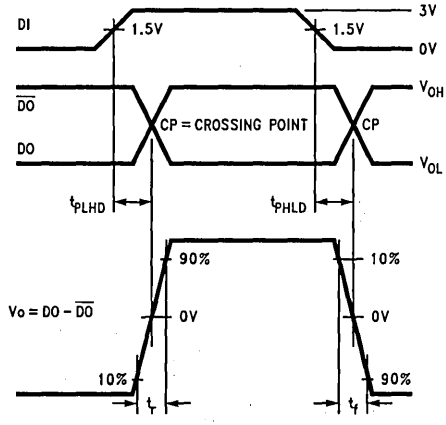
FIGURE 4. Driver Differential Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)



TL/F/11383–6

FIGURE 5. Driver Differential Propagation Delays and Transition Times

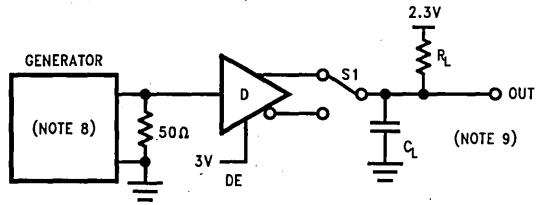


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FIGURE 6. Driver Propagation Delay Test Circuit

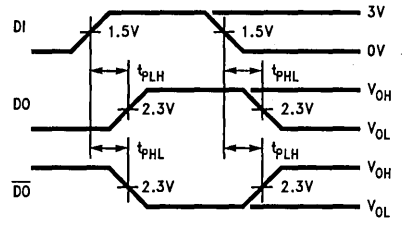

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FIGURE 7. Driver Propagation Delays

Parameter Measurement Information (Continued)

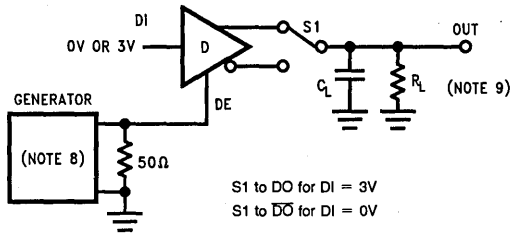

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FIGURE 8. Driver TRI-STATE Test Circuit (t_{PZH}, t_{PHZ})

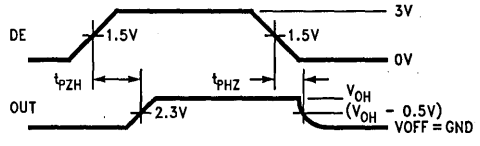

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FIGURE 9. Driver TRI-STATE Delays (t_{PZH}, t_{PHZ})

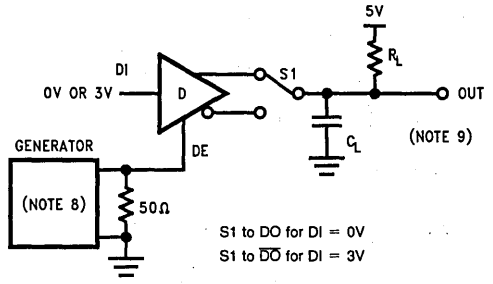

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FIGURE 10. Driver TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})

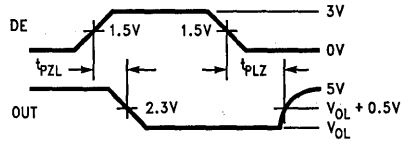

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FIGURE 11. Driver TRI-STATE Delays (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)

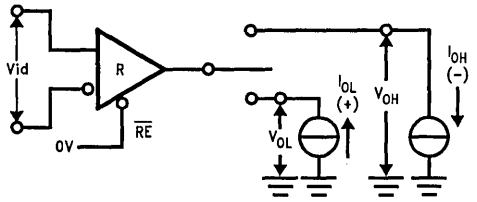

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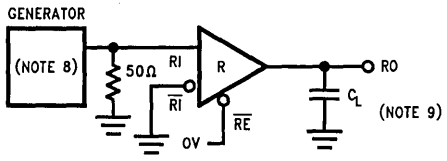
FIGURE 12. Receiver V_{OH} and V_{OL}



TL/F/11383–14

FIGURE 13. Receiver Propagation Delay Test Circuit

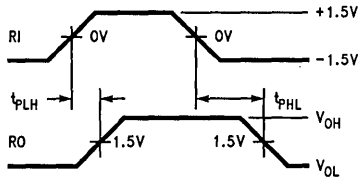


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FIGURE 14. Receiver Propagation Delays

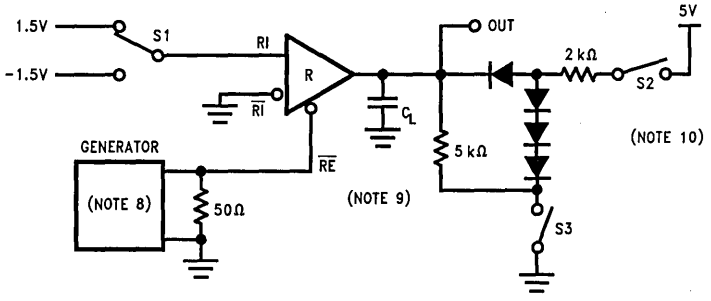

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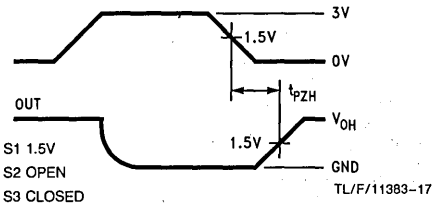
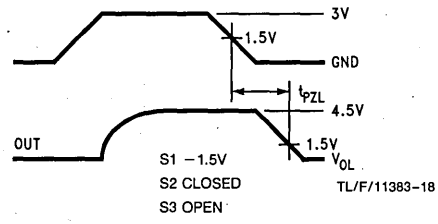
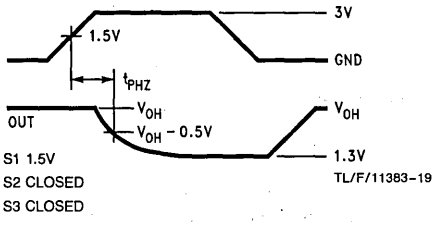
FIGURE 15. Receiver TRI-STATE Delay Test Circuit

Parameter Measurement Information (Continued)







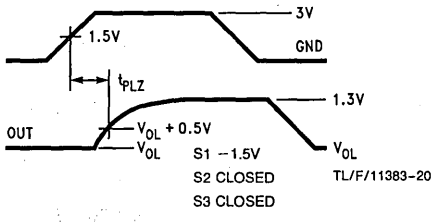


FIGURE 16. Receiver Enable and Disable Timing

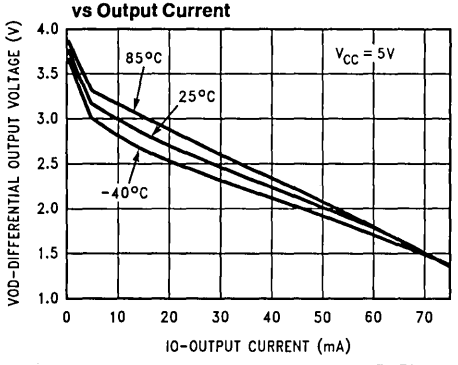
Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, t_r and t_f < 6.0 ns, Z_O = 50Ω.

Note 9: C_L includes probe and stray capacitance.

Note 10: Diodes are 1N916 or equivalent.

Typical Performance Characteristics

Differential Output Voltage vs Output Current



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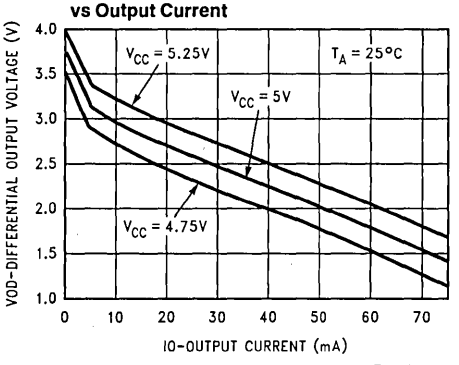
Differential Output Voltage vs Output Current



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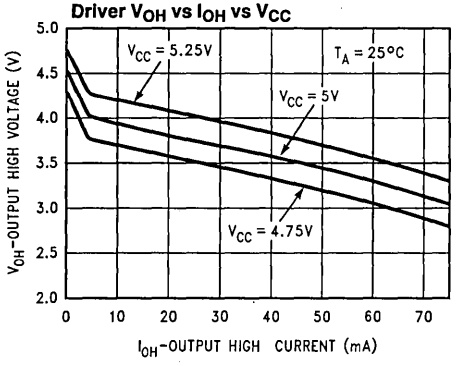
Driver V_{OH} vs I_{OH} vs V_{CC}



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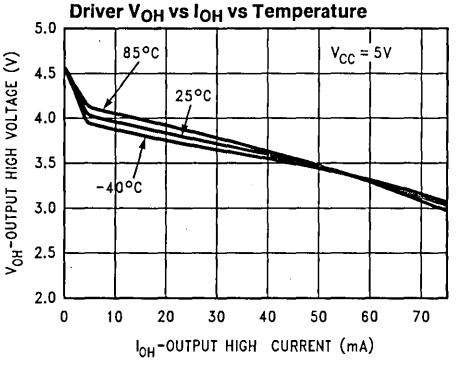
Driver V_{OH} vs I_{OH} vs Temperature



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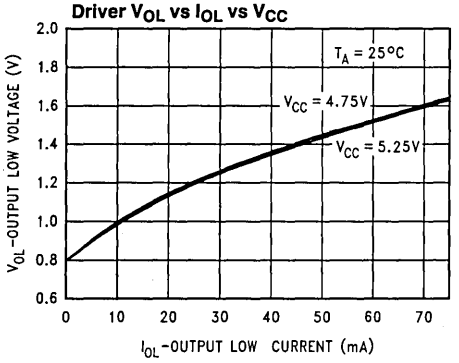
Driver V_{OL} vs I_{OL} vs V_{CC}



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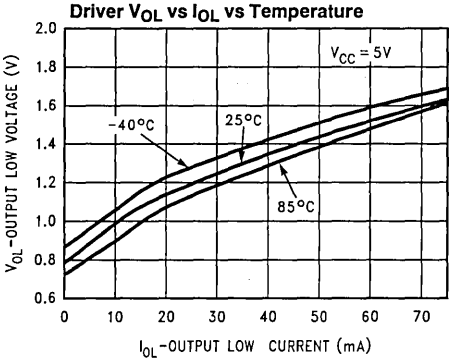
Driver V_{OL} vs I_{OL} vs Temperature



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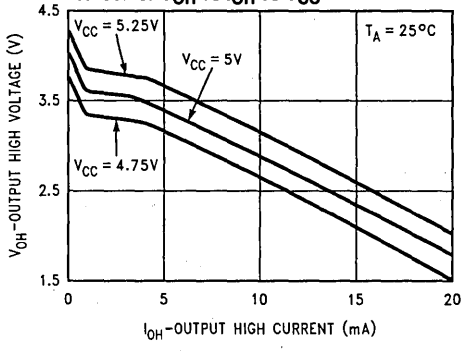
3

Typical Performance Characteristics (Continued)

Receiver V_{OH} vs I_{OH} vs V_{CC}



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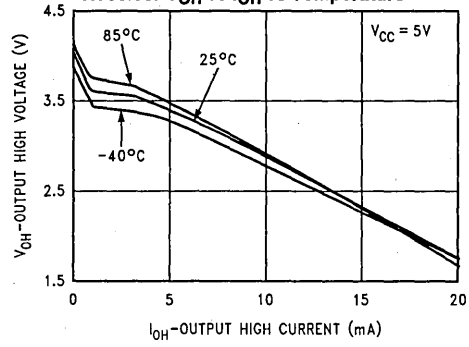
Receiver V_{OH} vs I_{OH} vs Temperature



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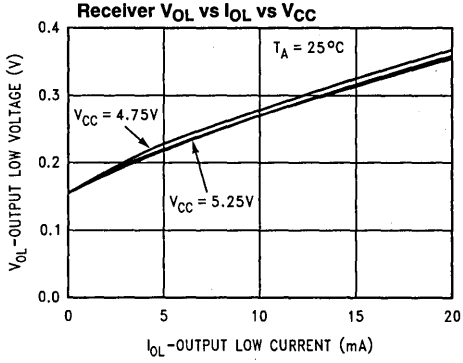
Receiver V_{OL} vs I_{OL} vs V_{CC}



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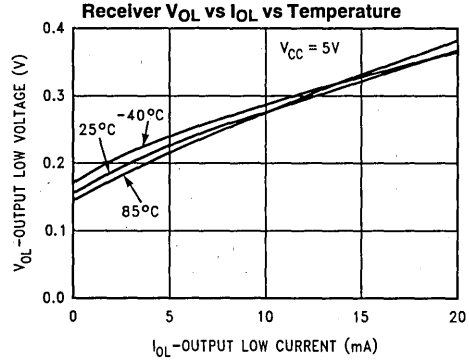
Receiver V_{OL} vs I_{OL} vs Temperature



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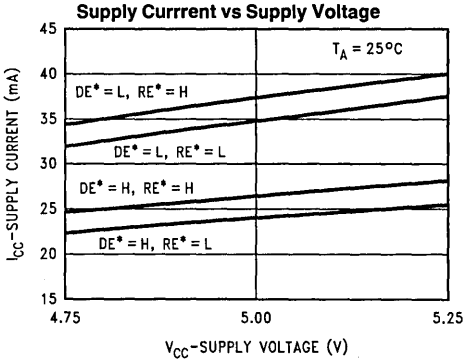
Supply Currrent vs Supply Voltage



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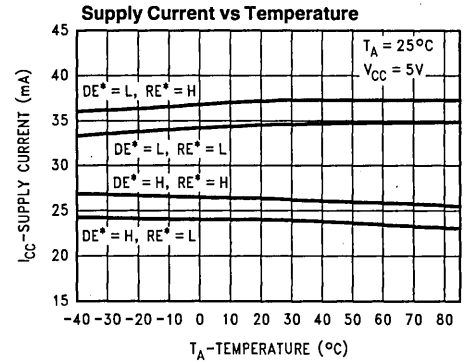
Supply Current vs Temperature



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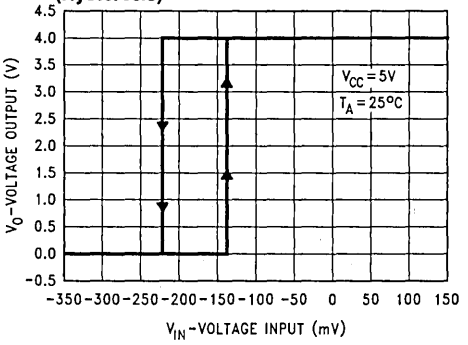
Typical Performance Characteristics (Continued)

Voltage Output vs Voltage Input (Hysteresis)



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National Semiconductor

DS36277
Dominant Mode Multipoint Transceiver

General Description

The DS36277 Dominant Mode Multipoint Transceiver is designed for use on bi-directional differential busses. It is optimal for use on Interfaces that utilize Society of Automotive Engineers (SAE) J1708 Electrical Standard.

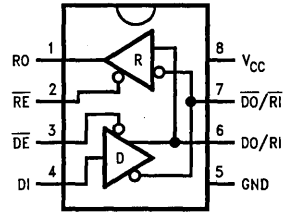
The device is similar to standard TIA/EIA-485 transceivers, but differs in enabling scheme. The Driver's Input is normally externally tied LOW, thus providing only two states: Active (LOW), or Disabled (OFF). When the driver is active, the dominant mode is LOW, conversely, when the driver is disabled, the bus is pulled HIGH by external bias resistors.

The receiver provides a FAILSAFE feature that guarantees a known output state when the Interface is in the following conditions: Floating Line, Idle Line (no active drivers), and Line Fault Conditions (open or short). The receiver output is HIGH for the following conditions: Open Inputs, Terminated Inputs (50Ω), or Shorted Inputs. FAILSAFE is a highly desirable feature when the transceivers are used with Asynchronous Controllers such as UARTs.

Features

- FAILSAFE receiver, RO = HIGH for:
  - — OPEN inputs
  - — Terminated inputs
  - — SHORTED inputs
- Optimal for use in SAE J1708 Interfaces
- Compatible with popular interface standards:
  - — TIA/EIA-485 and TIA/EIA-422-A
  - — CCITT recommendation V.11
- Bi-directional transceiver
  - — Designed for multipoint transmission
- Wide bus common mode range
  - — (−7V to +12V)
- Available in plastic DIP and SOIC packages

Connection and Logic Diagram



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Order Number DS36277TM or DS36277TN
See NS Package Number M08A or N08E

Truth Tables

Driver

Inputs		Outputs	
$\overline{DE}$	DI	DO/RI	$\overline{DO/RI}$
L	L	L	H
L	H	H	L
H	X	Z	Z

Receiver

Inputs		Output
$\overline{RE}$	DO/RI-$\overline{DO/RI}$	RO
L	≥ 0 mV	H
L	≤ −500 mV	L
L	SHORTED	H
L	OPEN	H
H	X	Z

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Voltage ($\overline{DE}$, $\overline{RE}$, and DI)	5.5V
Driver Output Voltage/ Receiver Input Voltage	−10V to +15V
Receiver Output Voltage (RO)	5.5V
Maximum Package Power Dissipation @ +25°C	
N Package (derate 9.3 mW/°C above +25°C)	1168 mW
M Package (derate 5.8 mW/°C above +25°C)	726 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Temperature (T_A) DS36277T	−40	+85	°C

Electrical Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_{OD}	Differential Output Voltage	I_O = 0 mA (No Load)		1.5	3.6	6	V
V_{oDO}	Output Voltage	I_O = 0 mA (Output to GND)		0		6	V
$V_{o\overline{DO}}$	Output Voltage			0		6	V
V_{T1}	Differential Output Voltage (Termination Load)	R_L = 54Ω (485)	*(Figure 1)*	1.3	2.2	5.0	V
		R_L = 100Ω (422)		1.7	2.6	5.0	V
ΔV_{T1}	Balance of V_{T1} $\lvert V_{T1} - \overline{V_{T1}} \rvert$	R_L = 54Ω	(Note 3)	−0.2		0.2	V
		R_L = 100Ω		−0.2		0.2	V
V_{OS}	Driver Common Mode Output Voltage	R_L = 54Ω	*(Figure 1)*	0	2.5	3.0	V
		R_L = 100Ω		0	2.5	3.0	V
ΔV_{OS}	Balance of V_{OS} $\lvert V_{OS} - \overline{V_{OS}} \rvert$	R_L = 54Ω	(Note 3)	−0.2		0.2	V
		R_L = 100Ω		−0.2		0.2	V
V_{OH}	Output Voltage High	I_{OH} = −22 mA	*(Figure 2)*	2.7	3.7		V
V_{OL}	Output Voltage Low	I_{OL} = +22 mA			1.3	2	V
I_{OSD}	Driver Short-Circuit Output Current	V_O = +12V	*(Figure 3)*		92	290	mA
		V_O = −7V			−187	−290	mA

Electrical Characteristics (Continued)

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TH}	Differential Input High Threshold Voltage (Note 5)	$V_O = V_{OH}$, $I_O = -0.4$ mA $-7V \le V_{CM} \le +12V$				−0.150	0	V
V_{TL}	Differential Input Low Threshold Voltage (Note 5)	$V_O = V_{OL}$, $I_O = 8.0$ mA $-7V \le V_{CM} \le +12V$			−0.5	−0.230		V
V_{HST}	Hysteresis (Note 6)	$V_{CM} = 0V$				80		mV
I_{IN}	Line Input Current (V_{CC} = 4.75V, 5.25V, 0V)	Other Input = 0V, $\overline{DE} = V_{IH}$ (Note 7)	$V_I = +12V$			0.5	1.5	mA
			$V_I = -7V$			−0.5	−1.5	mA
I_{OSR}	Short Circuit Current	$V_O = 0V$		RO	−15	−32	−85	mA
I_{OZ}	TRI-STATE® Leakage Current	V_O = 0.4 to 2.4V			−20	1.4	+20	μA
V_{OH}	Output High Voltage *(Figure 12)*	$V_{ID} = 0V$, $I_{OH} = -0.4$ mA			2.3	3.7		V
		V_{ID} = OPEN, $I_{OH} = -0.4$ mA			2.3	3.7		V
V_{OL}	Output Low Voltage *(Figure 12)*	$V_{ID} = -0.5V$, $I_{OL} = +8$ mA				0.3	0.7	V
		$V_{ID} = -0.5V$, $I_{OL} = +16$ mA				0.3	0.8	V
R_{IN}	Input Resistance				10	20		kΩ
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			$\overline{DE}$, $\overline{RE}$, or DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = 2.4V$					20	μA
I_{IL}	Low Level Input Current	$V_{IL} = 0.4V$					−100	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA				−0.7	−1.5	V
I_{CC}	Output Low Voltage Supply Current (No Load)	$\overline{DE} = 0V$, $\overline{RE} = 0V$, DI = 0V				39	60	mA
I_{CCR}		$\overline{DE} = 3V$, $\overline{RE} = 0V$, DI = 0V				24	50	mA
I_{CCD}		$\overline{DE} = 0V$, $\overline{RE} = 3V$, DI = 0V				40	75	mA
I_{CCX}		$\overline{DE} = 3V$, $\overline{RE} = 3V$, DI = 0V				27	45	mA

Switching Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLHD}	Diff. Prop. Delay Low to High	$R_L = 54\Omega$ $C_L = 50$ pF $C_D = 50$ pF *(Figures 4, 5)*	8	17	60	ns
t_{PHLD}	Diff. Prop. Delay High to Low		8	19	60	ns
t_{SKD}	Diff. Skew ($\lvert t_{PLHD} - t_{PHLD} \rvert$)			2	10	ns
t_r	Diff. Rise Time			11	60	ns
t_f	Diff. Fall Time			11	60	ns
t_{PLH}	Prop. Delay Low to High	$R_L = 27\Omega$, $C_L = 15$ pF *(Figures 6, 7)*		22	85	ns
t_{PHL}	Prop. Delay High to Low			25	85	ns
t_{PZH}	Enable Time Z to High	$R_L = 110\Omega$ $C_L = 50$ pF *(Figures 8–11)*		25	60	ns
t_{PZL}	Enable Time Z to Low			30	60	ns
t_{PHZ}	Disable Time High to Z			16	60	ns
t_{PLZ}	Disable Time Low to Z			11	60	ns
RECEIVER CHARACTERISTICS						
t_{PLH}	Prop. Delay Low to High	$V_{ID} = -1.5$V to $+1.5$V $C_L = 15$ pF *(Figures 13, 14)*	15	37	90	ns
t_{PHL}	Prop. Delay High to Low		15	43	90	ns
t_{SK}	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			6	15	ns
t_{PZH}	Enable Time Z to High	$C_L = 15$ pF *(Figures 15, 16)*		12	60	ns
t_{PZL}	Enable Time Z to Low			28	60	ns
t_{PHZ}	Disable Time High to Z			20	60	ns
t_{PLZ}	Disable Time Low to Z			10	60	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: $\Delta \lvert V_{T1} \rvert$ and $\Delta \lvert V_{OS} \rvert$ are changes in magnitude of V_{T1} and V_{OS}, respectively, that occur when the input changes state.

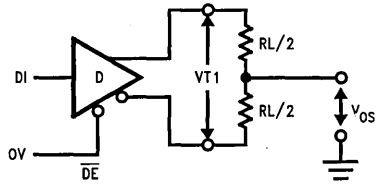
Note 4: All typicals are given for $V_{CC} = 5.0$V and $T_A = +25°C$.

Note 5: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 6: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

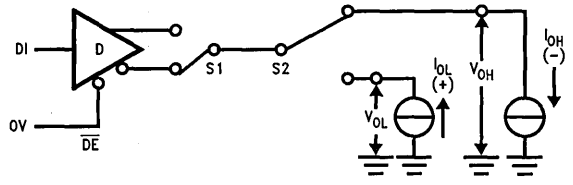
Note 7: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Parameter Measurement Information



TL/F/11384–2

FIGURE 1. Driver V_{T1} and V_{OS} Test Circuit



TL/F/11384–3

FIGURE 2. Driver V_{OH} and V_{OL} Test Circuit

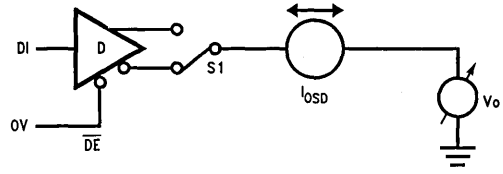


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FIGURE 3. Driver Short Circuit Test Circuit

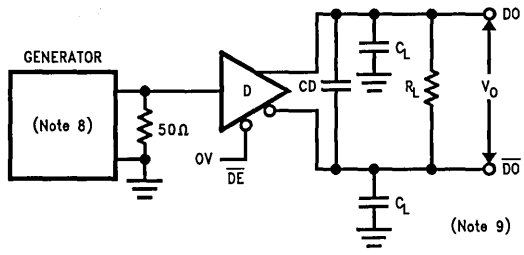

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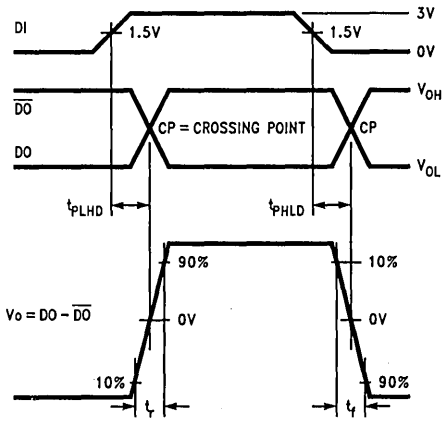
FIGURE 4. Driver Differential Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)



TL/F/11384–6

FIGURE 5. Driver Differential Propagation Delays and Transition Times

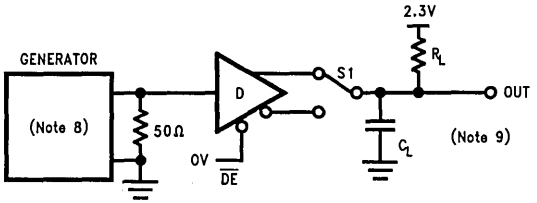


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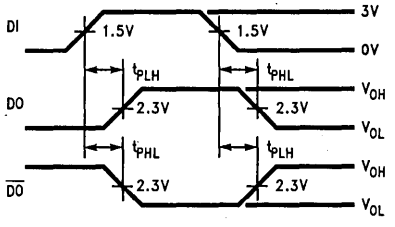
FIGURE 6. Driver Propagation Delay Test Circuit

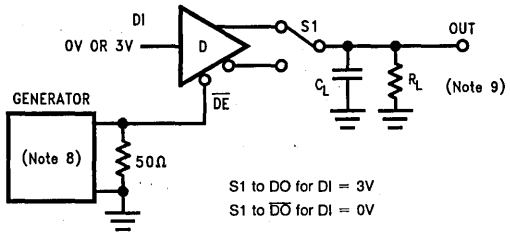


TL/F/11384–8

FIGURE 7. Driver Propagation Delays

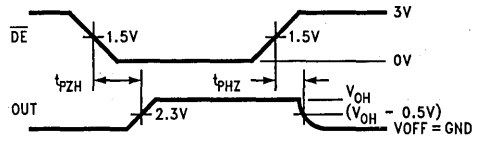
3

Parameter Measurement Information (Continued)



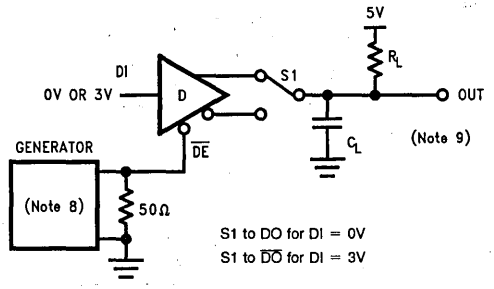
TL/F/11384–9

FIGURE 8. Driver TRI-STATE Test Circuit (t_{PZH}, t_{PHZ})



TL/F/11384–10

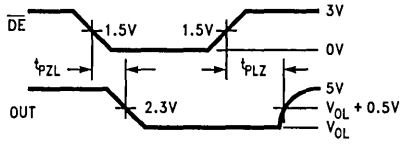
FIGURE 9. Driver TRI-STATE Delays (t_{PZH}, t_{PHZ})



TL/F/11384–11

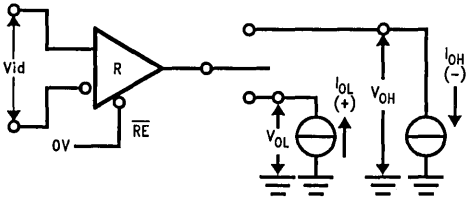
FIGURE 10. Driver TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)



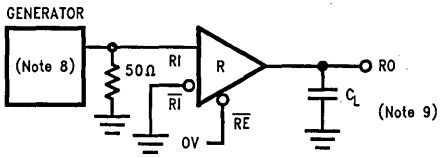
TL/F/11384–12

FIGURE 11. Driver TRI-STATE Delays (t_{PZL}, t_{PLZ})



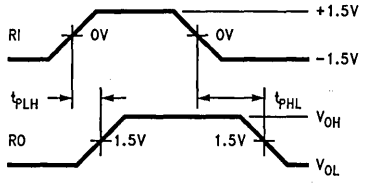
TL/F/11384–13

FIGURE 12. Receiver V_{OH} and V_{OL}



TL/F/11384–14

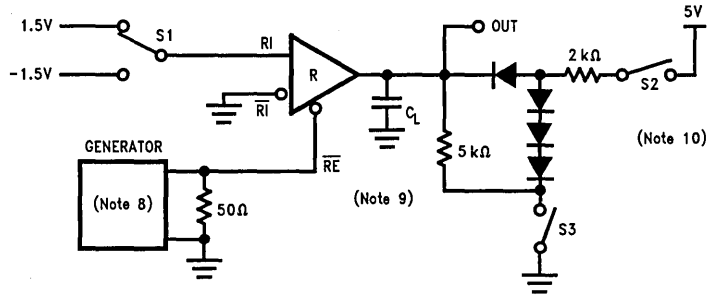
FIGURE 13. Receiver Propagation Delay Test Circuit



TL/F/11384–15

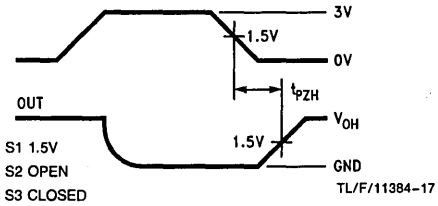
FIGURE 14. Receiver Propagation Delays

Parameter Measurement Information (Continued)

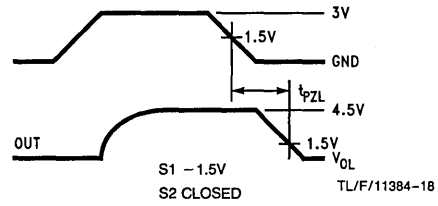


TL/F/11384–16

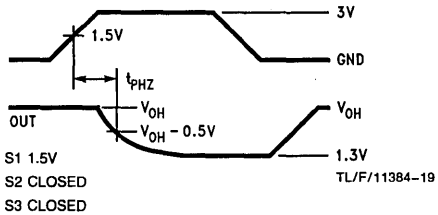
FIGURE 15. Receiver TRI-STATE Delay Test Circuit



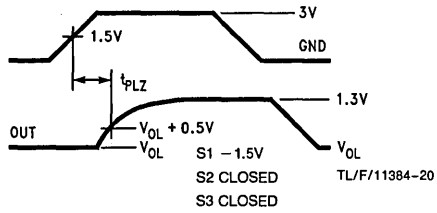
TL/F/11384–17



TL/F/11384–18



TL/F/11384–19



TL/F/11384–20

FIGURE 16. Receiver Enable and Disable Timing

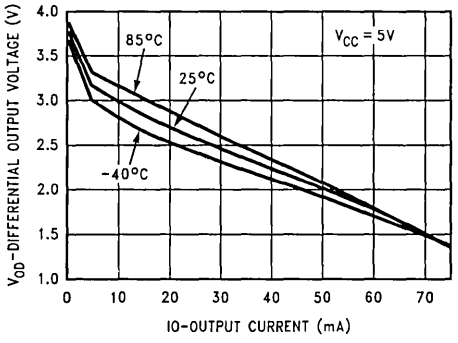
Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, t_r and t_f < 6.0 ns, Z_O = 50Ω.

Note 9: C_L includes probe and stray capacitance.

Note 10: Diodes are 1N916 or equivalent.

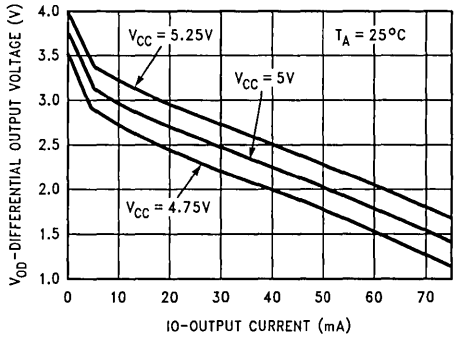
Typical Performance Characteristics

Differential Output Voltage vs Output Current



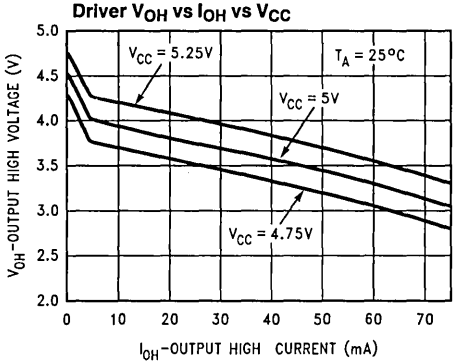
TL/F/11384-22

Differential Output Voltage vs Output Current



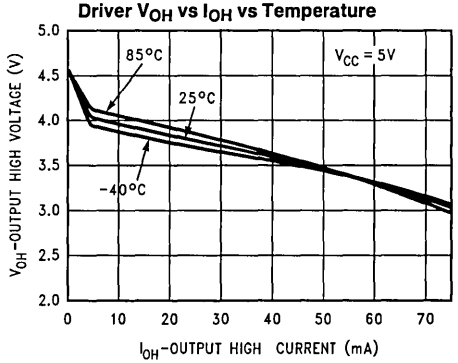
TL/F/11384-23

Driver V_{OH} vs I_{OH} vs V_{CC}



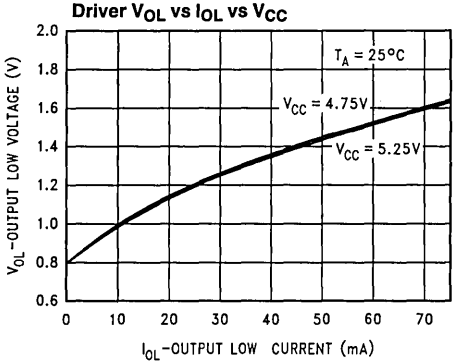
TL/F/11384-24

Driver V_{OH} vs I_{OH} vs Temperature



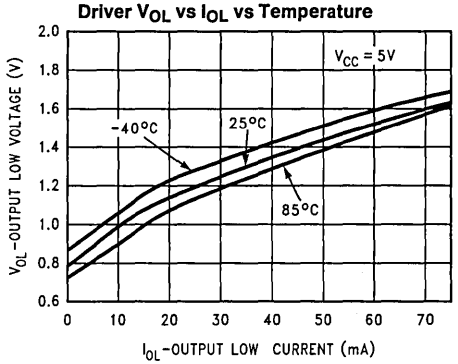
TL/F/11384-25

Driver V_{OL} vs I_{OL} vs V_{CC}



TL/F/11384-26

Driver V_{OL} vs I_{OL} vs Temperature

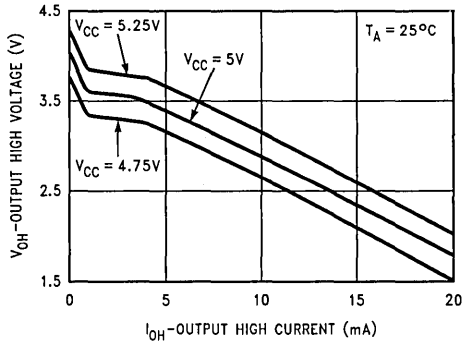


TL/F/11384-27

3

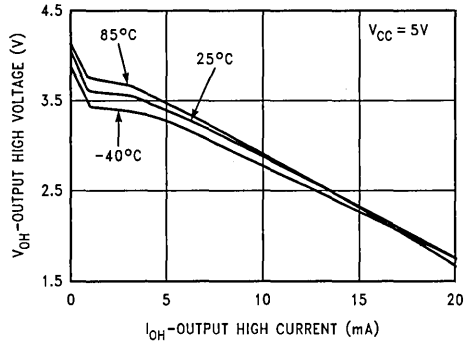
Typical Performance Characteristics (Continued)

Receiver V_{OH} vs I_{OH} vs V_{CC}



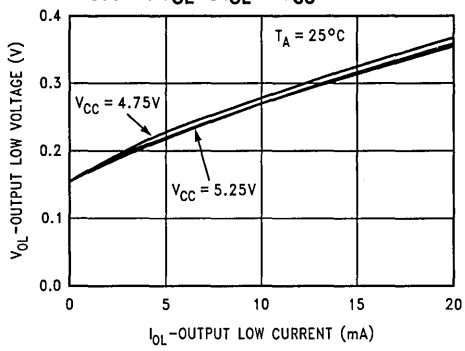
TL/F/11384–28

Receiver V_{OH} vs I_{OH} vs Temperature



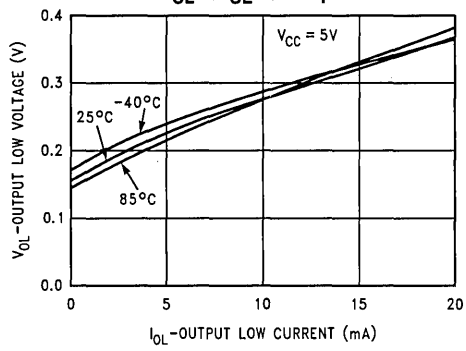
TL/F/11384–29

Receiver V_{OL} vs I_{OL} vs V_{CC}



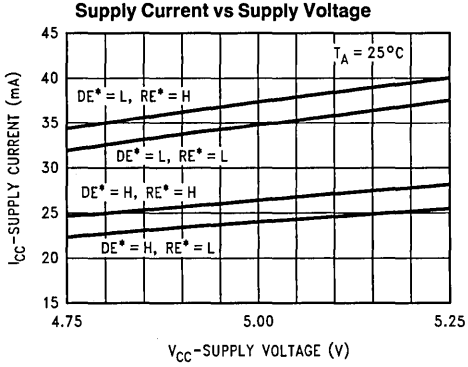
TL/F/11384–30

Receiver V_{OL} vs I_{OL} vs Temperature



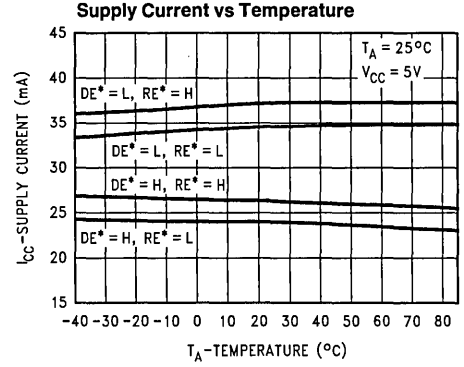
TL/F/11384–31

Supply Current vs Supply Voltage



TL/F/11384–32

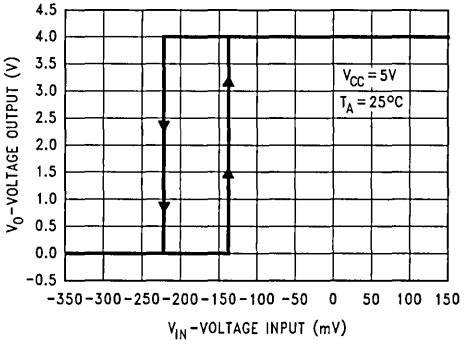
Supply Current vs Temperature



TL/F/11384–33

Typical Performance Characteristics (Continued)

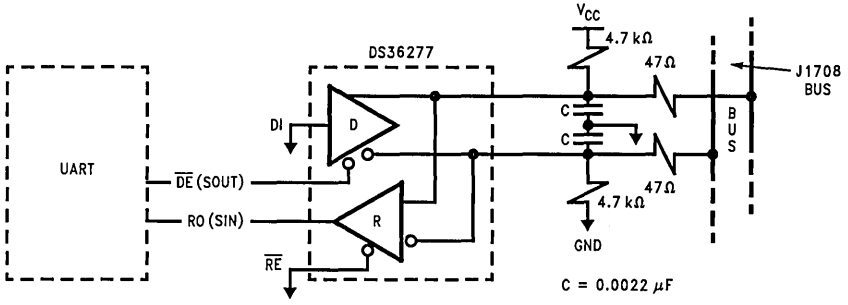
Voltage Output vs Voltage Input (Hysteresis)



TL/F/11384–34

Typical Applications Information

SAE J1708 Node with External Bias Resistors and Filters



TL/F/11384–21

National Semiconductor

DS36950
Quad Differential Bus Transceiver

General Description

The DS36950 is a low power, space-saving quad EIA-485 differential bus transceiver especially suited for high speed, parallel, multipoint, computer I/O bus applications. A compact 20-pin surface mount PLCC package provides high transceiver integration and a very small PC board footprint.

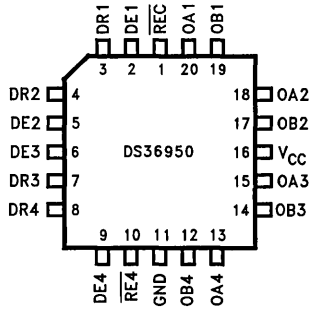
Timing uncertainty across an interface using multiple devices, a typical problem in a parallel interface, is specified—minimum and maximum propagation delay times are guaranteed.

Six devices can implement a complete IPI master or slave interface. Three transceivers in a package are pinned out for connection to a parallel databus. The fourth transceiver, with the flexibility provided by its individual enables, can serve as a control bus transceiver.

Features

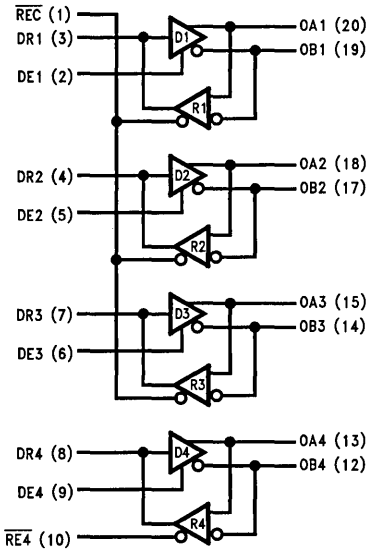
- Pinout for IPI interface
- Compact 20-pin PLCC package
- Meets EIA-485 standard for multipoint bus transmission
- Greater than 60 mA source/sink
- Thermal Shutdown Protection

Pinout and Logic Diagram



TL/F/10602-1

Order Number DS36950
See NS Package Number V20A



TL/F/10602-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Control Input Voltage	V_{CC} + 0.5V
Driver Input Voltage	V_{CC} + 0.5V
Driver Output Voltage/Receiver Input Voltage	−10V to +15V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ 25°C	
V Package	1.73W
Derate V Package 13.9 mW/°C above 25°C	
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering 4 Sec.)	260°C

Recommended Operating Conditions

Supply Voltage, V_{CC}	4.75V to 5.25V
Bus Voltage	−7V to +12V
Operating Free Air Temp. (T_A)	0°C to +70°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
V_{ODL}	Differential Driver Output Voltage (Full Load)	I_L = 60 mA, V_{CM} = 0V	1.5	1.9		V
V_{OD}	Differential Driver Output Voltage (Termination Load)	R_L = 100Ω (EIA-422)	2.0	3.5		V
		R_L = 54Ω (EIA-485)	1.5	3.2		V
$\Delta\|V_{OD}\|$	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R_L = 54Ω or 100Ω (Note 4) *(Figure 1)* (EIA-485)			0.2	V
V_{OC}	Driver Common Mode Output Voltage (Note 5)	R_L = 54Ω *(Figure 1)* (EIA-485)			3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage	(Note 4) *(Figure 1)* (EIA-485)			0.2	V
V_{OH}	Output Voltage HIGH	I_{OH} = −55 mA	2.7	3.2		V
V_{OL}	Output Voltage LOW	I_{OL} = 55 mA		1.4	1.7	V
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{CL}	Input Clamp Voltage	I = −18 mA			−1.5	V
I_{IH}	Input High Current	V_I = 2.4V (Note 3)			20	μA
I_{IL}	Input Low Current	V_I = 0.4V (Note 3)			−20	μA
I_{OSC}	Driver Short-Circuit Output Current (Note 9)	V_O = −7V (EIA-485)		−130	−250	mA
		V_O = 0V (EIA-422)		−90	−150	mA
		V_O = +12V (EIA-485)		130	250	mA
RECEIVER CHARACTERISTICS						
I_{OSR}	Short Circuit Output Current	V_O = 0V (Note 9)	−15	−28	−75	mA
I_{OZ}	TRI-STATE® Output Current	V_O = 0.4V to 2.4V			20	μA
V_{OH}	Output Voltage High	V_{ID} = 0.20V, I_{OH} = −0.4 mA	2.4	3.0		V
V_{OL}	Output Voltage Low	V_{ID} = −0.20V, I_{OL} = 4 mA		0.35	0.5	V
V_{TH}	Differential Input High Threshold Voltage	V_O = V_{OH}, I_O = −0.4 mA (EIA-422/485)		0.03	0.20	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = V_{OL}, I_O = 4.0 mA (EIA-422/485)	−0.20	−0.03		V
V_{HST}	Hysteresis (Note 7)	V_{CM} = 0V	35	60		mV

Electrical Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER AND RECEIVER CHARACTERISTICS							
V_{IH}	Enable Input Voltage High			2.0			V
V_{IL}	Enable Input Voltage Low					0.8	V
V_{CL}	Enable Input Clamp Voltage	$I = -18$ mA				−1.5	V
I_{IN}	Line Input Current (Note 8)	Other Input = 0V	$V_I = +12V$		0.5	1	mA
			$V_I = -7V$		−0.45	−0.8	mA
I_{IH}	Enable Input Current High	$V_{OH} = 2.4V$	$\overline{RE4}$ or DE			20	μA
			$\overline{REC}$			60	μA
I_{IL}	Enable Input Current Low	$V_{OL} = 0.4V$	$\overline{RE4}$ or DE			−20	μA
			$\overline{REC}$			−60	μA
I_{CC}	Supply Current (Note 10)	No Load, Outputs Enabled			75	90	mA
I_{CCZ}	Supply Current (Note 10)	No Load, Outputs Disabled			50	70	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Conditions		Min	Typ	Max	Units
DRIVER SINGLE-ENDED CHARACTERISTICS						
t_{PZH}	$R_L = 110\Omega$ *(Figure 4)*			35	40	ns
t_{PZL}	$R_L = 110\Omega$ *(Figure 5)*			25	40	ns
t_{PHZ}	$R_L = 110\Omega$ *(Figure 4)*			15	25	ns
t_{PLZ}	$R_L = 110\Omega$ *(Figure 5)*			35	40	ns
DRIVER DIFFERENTIAL CHARACTERISTICS						
t_R, t_F	Rise & Fall Time	$R_L = 54\Omega$, $C_L = 50$ pF, $C_D = 15$ pF *(Figures 3, 8)*		13	16	ns
t_{PLHD}	Differential Propagation Delays (Note 15)		9	15	19	ns
t_{PHLD}			9	15	19	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Differential Skew			3	6	ns

Switching Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS						
t_{PLHD}	Differential Propagation Delays		9	14	19	ns
t_{PHLD}	C_L = 15 pF, V_{CM} = 1.5V *(Figure 6)*		9	14	19	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Differential Receiver Skew			1	3	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF *(Figure 7)*		15	22	ns
t_{ZL}	Output Enable Time to Low Level			20	30	ns
t_{HZ}	Output Disable Time from High Level			10	17	ns
t_{LZ}	Output Disable Time from Low Level			17	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is define as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: I_{IH} and I_{IL} includes driver input current and receiver TRI-STATE leakage current.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes state.

Note 5: In EIA Standards EIA-422 and EIA-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 7: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

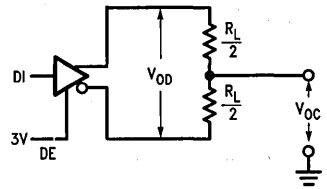
Note 8: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Note 9: Short one output at a time.

Note 10: Total package supply current.

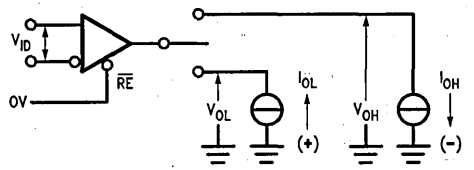
Note 11: All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Parameter Measurement Information



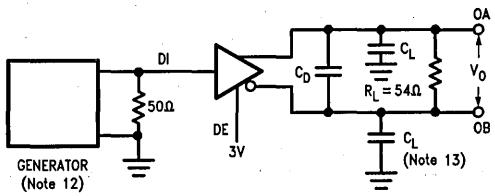
TL/F/10602–3

FIGURE 1. Driver V_{OD} and V_{OC}

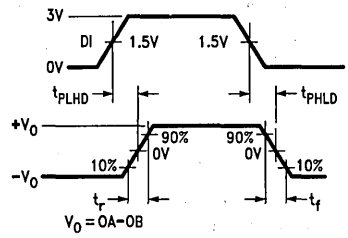


TL/F/10602–4

FIGURE 2. Receiver V_{OH} and V_{OL}

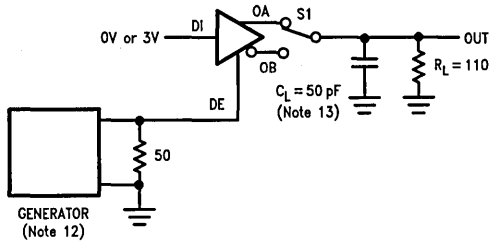


TL/F/10602–5



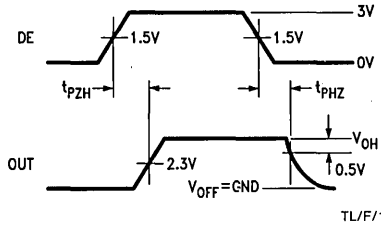
TL/F/10602–6

FIGURE 3. Driver Differential Propagation Delay and Transition Timing



TL/F/10602–9

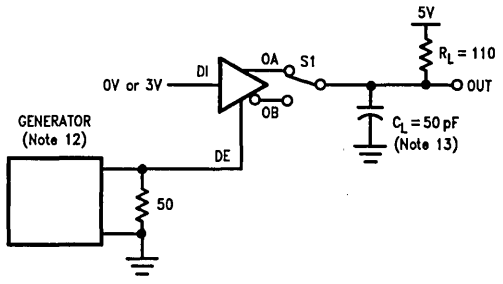
S1 to OA for DI = 3V
S1 to OB for DI = 0V



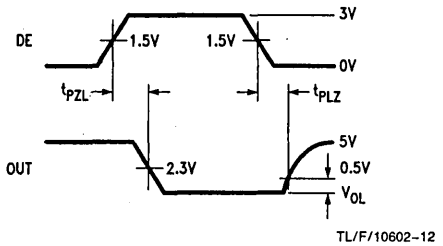
TL/F/10602–10

FIGURE 4. Driver Enable and Disable Timing (t_{PZH}, t_{PHZ})

Parameter Measurement Information (Continued)



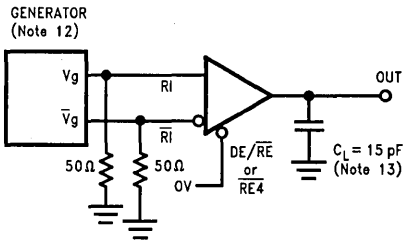
TL/F/10602–11

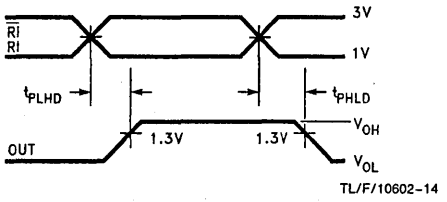


TL/F/10602–12

S1 to OA for DI = 0V
S1 to OB for DI = 3V

FIGURE 5. Driver Enable and Disable Timing (t_{PZL}, t_{PLZ})



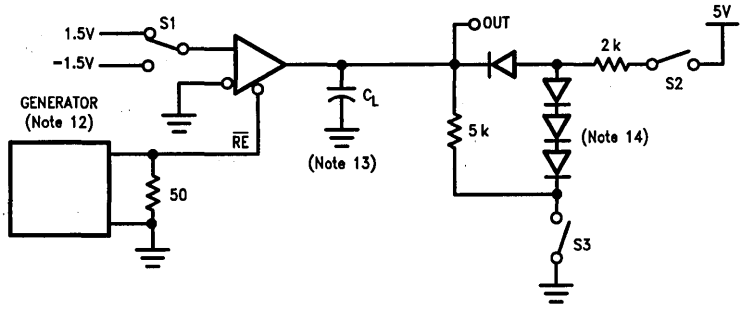


TL/F/10602–14

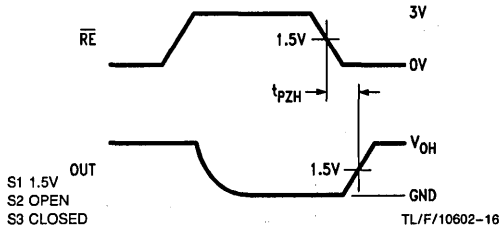
TL/F/10602–13

FIGURE 6. Receiver Differential Propagation Delay Timing

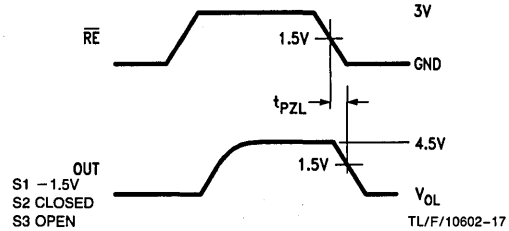
Parameter Measurement Information (Continued)



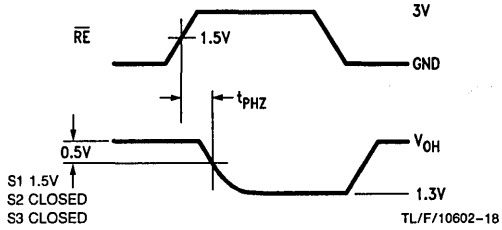
TL/F/10602-15



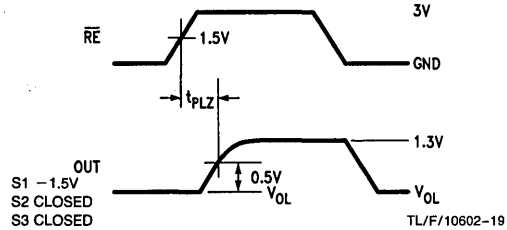
TL/F/10602-16



TL/F/10602-17

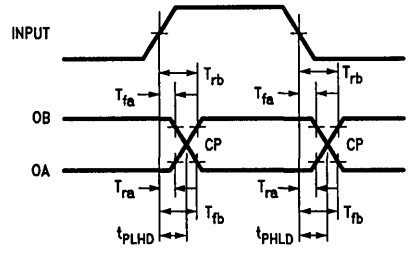


TL/F/10602-18



TL/F/10602-19

FIGURE 7. Receiver Enable and Disable Timing



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$$TCP = \frac{(Tfb \times Trb) - (Tra \times Tfa)}{Trb - Tra - Tfa + Tfb}$$

TCP = Crossing Point

Tra, Trb, Tfa, and Tfb are propagation delay measurements to the 20% and 80% levels.

FIGURE 8. Propagation Delay Timing for Calculation of Driver Differential Propagation Delays

Note 12: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% Duty Cycle, t_r and t_f < 6.0 ns, Z_O = 50Ω

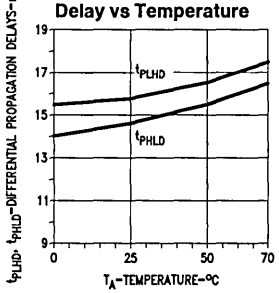
Note 13: C_L includes probe and stray capacitance.

Note 14: Diodes are 1N916 or equivalent.

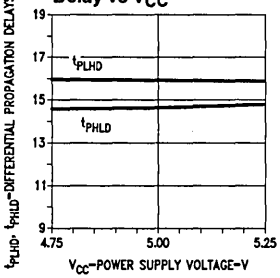
Note 15: Differential propagation delays are calculated from single-ended propagation delays measured from driver input to the 20% and 80% levels on the driver outputs (See *Figure 8*).

Typical Performance Characteristics

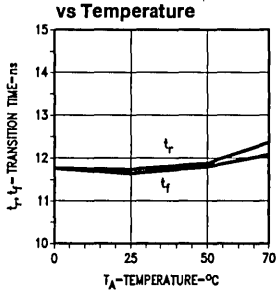
Driver Differential Propagation Delay vs Temperature



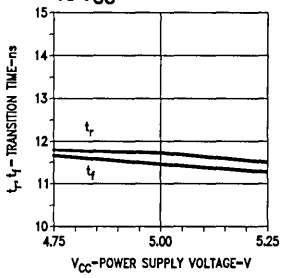
Driver Differential Propagation Delay vs V_{CC}



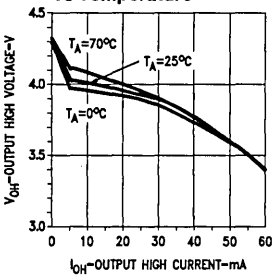
Driver Transition Time vs Temperature



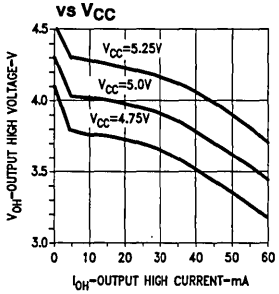
Driver Transition Time vs V_{CC}



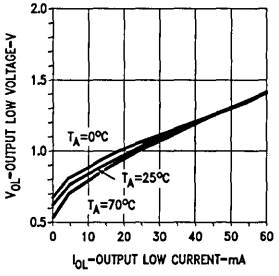
Driver V_{OH} vs I_{OH} vs Temperature



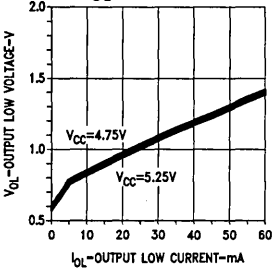
Driver V_{OH} vs I_{OH} vs V_{CC}



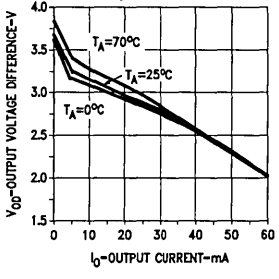
Driver V_{OL} vs I_{OL} vs Temperature



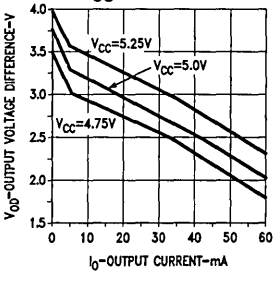
Driver V_{OL} vs I_{OL} vs V_{CC}



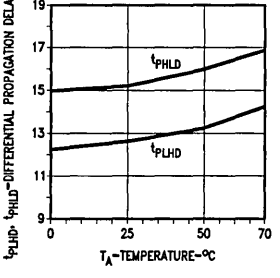
Driver V_{OD} vs I_O vs Temperature



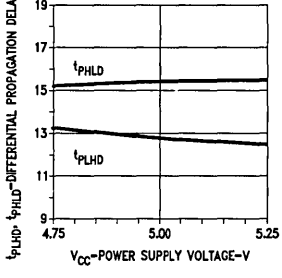
Driver V_{OD} vs I_O vs V_{CC}



Receiver Differential Propagation Delay vs Temperature



Receiver Differential Propagation Delay vs V_{CC}



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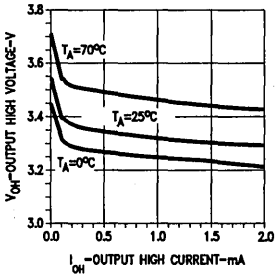
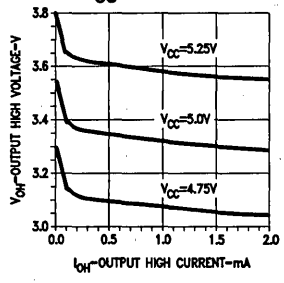
Typical Performance Characteristics (Continued)

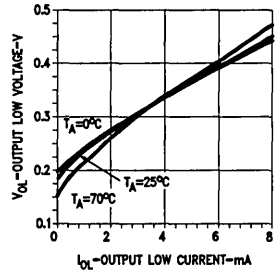
Receiver V_{OH} vs I_{OH} vs Temperature



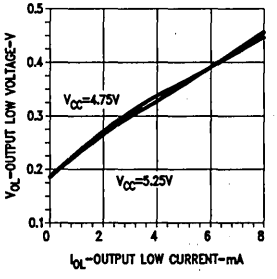
Receiver V_{OH} vs I_{OH} vs V_{CC}



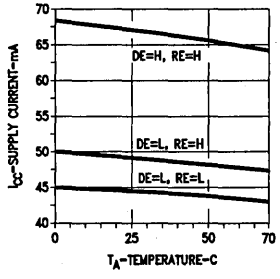
Receiver V_{OL} vs I_{OL} vs Temperature



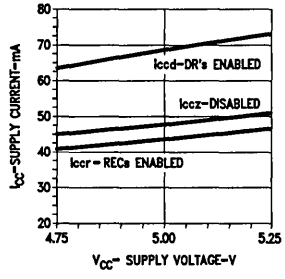
Receiver V_{OL} vs I_{OL} vs V_{CC}



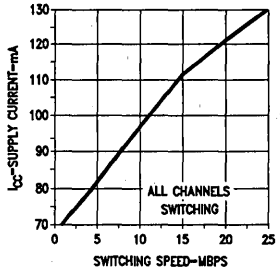
Supply Current vs Temperature



Power Supply Current vs Power Supply Voltage



Driver I_{CC} vs Switching Frequency



TL/F/10602-22

National Semiconductor

DS36954
Quad Differential Bus Transceiver

General Description

The DS36954 is a low power, quad EIA-485 differential bus transceiver especially suited for high speed, parallel, multipoint, I/O bus applications. A compact 20-pin surface mount PLCC or SOIC package provides high transceiver integration and a very small PC board footprint.

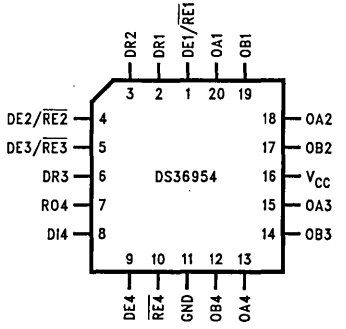
Propagation delay skew between devices is specified to aid in parallel interface designs—limits on maximum and minimum delay times are guaranteed.

Five devices can implement a complete SCSI initiator or target interface. Three transceivers in a package are pinned out for data bus connections. The fourth transceiver, with the flexibility provided by its individual enables, can serve as a control bus transceiver.

Features

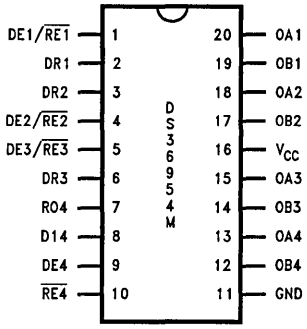
- Pinout for SCSI interface
- Compact 20-pin PLCC or SOIC package
- Meets EIA-485 standard for multipoint bus transmission
- Greater than 60 mA source/sink currents
- Thermal shutdown protection
- Glitch-free driver outputs on power up and down

Connection Diagrams



TL/F/11014–1

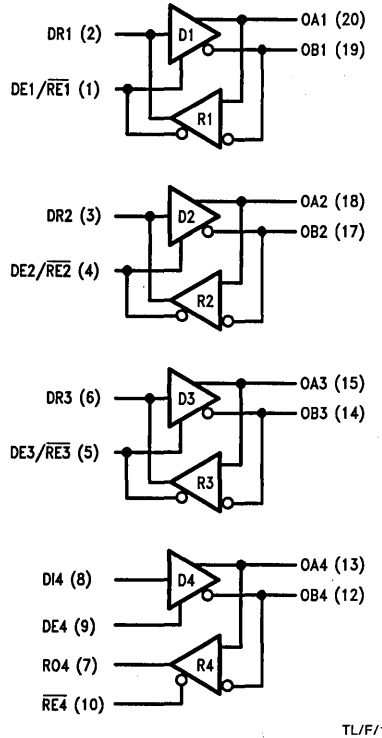
Order Number DS36954V
See NS Package Number V20A



TL/F/11014–19

Order Number DS36954M
See NS Package Number M20B

Logic Diagrams



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Control Input Voltage	V_{CC} + 0.5V
Driver Input Voltage	V_{CC} + 0.5V
Driver Output Voltage/ Receiver Input Voltage	−10V to +15V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ +25°C	
V Package	1.73W
M Package	1.73W
Derate V Package	13.9 mW/°C above +25°C
Derate M Package	13.7 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 Sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Free Air Temperature (T_A)	0	+70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
V_{ODL}	Differential Driver Output Voltage (Full Load)	I_L = 60 mA, V_{CM} = 0V	1.5	1.9		V
V_{OD}	Differential Driver Output Voltage (Termination Load)	R_L = 100Ω (EIA-422)	2.0	2.25		V
		R_L = 54Ω (EIA-485)	1.5	2.0		V
$\Delta\|V_{OD}\|$	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R_L = 54 or 100Ω (Note 4) *(Figure 1)* (EIA-422/485)			0.2	V
V_{OC}	Driver Common Mode Output Voltage (Note 5)	R_L = 54Ω *(Figure 1)* (EIA-485)			3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage	(Note 4) *(Figure 1)* (EIA-422/485)			0.2	V
V_{OH}	Output Voltage High	I_{OH} = −55 mA	2.7	3.2		V
V_{OL}	Output Voltage Low	I_{OL} = 55 mA		1.4	1.7	V
V_{IH}	Input Voltage High		2.0			V
V_{IL}	Input Voltage Low				0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	V
I_{IH}	Input High Current	V_{IN} = 2.4V (Note 3)			20	μA
I_{IL}	Input Low Current	V_{IN} = 0.4V (Note 3)			−20	μA
I_{OSC}	Driver Short-Circuit Output Current (Note 9)	V_O = −7V (EIA-485)		−130	−250	mA
		V_O = 0V (EIA-422)		−90	−150	mA
		V_O = +12V (EIA-485)		130	250	mA

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS							
I_{OSR}	Short Circuit Output Current	V_O = 0V (Note 9)		−15	−28	−75	mA
I_{OZ}	TRI-STATE® Output Current	V_O = 0.4V to 2.4V				20	μA
V_{OH}	Output Voltage High	V_{ID} = 0.2V, I_{OH} = 0.4 mA		2.4	3.0		V
V_{OL}	Output Voltage Low	V_{ID} = −0.2V, I_{OL} = 4 mA			0.35	0.5	V
V_{TH}	Differential Input High Threshold Voltage	V_O = V_{OH}, I_O = −0.4 mA (EIA-422/485)			0.03	0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = V_{OL}, I_O = 4.0 mA (EIA-422/485)		−0.20	−0.03		V
V_{HST}	Hysteresis (Note 7)	V_{CM} = 0V		35	60		mV
DRIVER AND RECEIVER CHARACTERISTICS							
V_{IH}	Enable Input Voltage High			2.0			V
V_{IL}	Enable Input Voltage Low					0.8	V
V_{CL}	Enable Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
I_{IN}	Line Input Current (Note 8)	Other Input = 0V, DE/$\overline{RE}$ = 0.8V, DE4 = 0.8V	V_I = +12V		0.5	1.0	mA
			V_I = −7V		−0.45	−0.8	mA
I_{ING}	Line Input Current (Note 8)	Other Input = 0V, DE/$\overline{RE}$ and DE4 = 2V, V_{CC} = 3.0V, T_A = +25°C	V_I = +12V			1.0	mA
			V_I = −7V			−0.8	mA
I_{IH}	Enable Input Current High	V_{IN} = 2.4V, DE/$\overline{RE}$	V_{CC} = 3.0V		1	40	μA
			V_{CC} = 4.75V		1		μA
			V_{CC} = 5.25V		1	40	μA
		V_{IN} = 2.4V, DE4 or $\overline{RE4}$	V_{CC} = 3.0V		1	20	μA
			V_{CC} = 5.25V		1	20	μA
I_{IL}	Enable Input Current Low	V_{IN} = 0.8V, DE/$\overline{RE}$	V_{CC} = 3.0V		−6	−40	μA
			V_{CC} = 4.75V		−12		μA
			V_{CC} = 5.25V		−14	−40	μA
		V_{IN} = 0.8V, DE4 or $\overline{RE4}$	V_{CC} = 3.0V		−3	−20	μA
			V_{CC} = 5.25V		−7	−20	μA
I_{CCD}	Supply Current (Note 10)	No Load, DE/$\overline{RE}$ and DE4 = 2.0V			75	90	mA
I_{CCR}	Supply Current (Note 10)	No Load, DE/$\overline{RE}$ and $\overline{RE4}$ = 0.8V			50	70	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER SINGLE-ENDED CHARACTERISTICS							
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω	*(Figure 5)*		35	40	ns
t_{PZL}	Output Enable Time to Low Level		*(Figure 6)*		25	40	ns
t_{PHZ}	Output Disable Time to High Level		*(Figure 5)*		15	25	ns
t_{PLZ}	Output Disable Time to Low Level		*(Figure 6)*		35	40	ns
DRIVER DIFFERENTIAL CHARACTERISTICS							
t_r, t_f	Rise and Fall Time	R_L = 54Ω C_L = 50 pF C_D = 15 pF *(Figures 3, 4,* and *9)*			13	16	ns
t_{PLHD}	Differential Propagation Delays (Note 15)			9	15	19	ns
t_{PHLD}				9	12	19	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Diff. Skew				3	6	ns
RECEIVER CHARACTERISTICS							
t_{PLHD}	Differential Propagation Delays	C_L = 15 pF V_{CM} = 2.0V *(Figure 7)*		9	14	19	ns
t_{PHLD}				9	13	19	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Diff. Receiver Skew				1	3	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF *(Figure 8)*			15	22	ns
t_{PZL}	Output Enable Time to Low Level				20	30	ns
t_{PHZ}	Output Disable Time from High Level				20	30	ns
t_{PLZ}	Output Disable Time from Low Level				17	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: I_{IH} and I_{IL} include driver input current and receiver TRI-STATE leakage current on DR(1–3).

Note 4: Δ IVODI and Δ IVOCI are changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes state.

Note 5: In EIA Standards EIA-422 and EIA-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 7: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

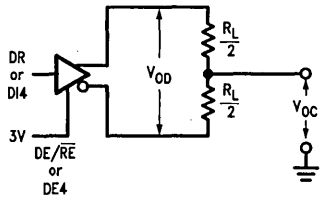
Note 8: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Note 9: Short one output at a time.

Note 10: Total package supply current.

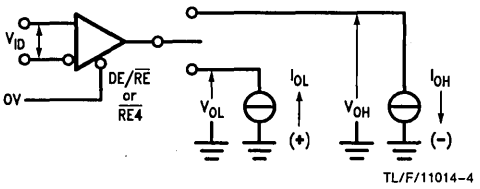
Note 11: All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Parameter Measurement Information



TL/F/11014-3

FIGURE 1. Driver V_{OD} and V_{OC} (Note 13)



TL/F/11014-4

FIGURE 2. Receiver V_{OH} and V_{OL}

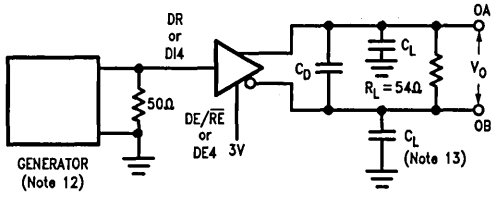


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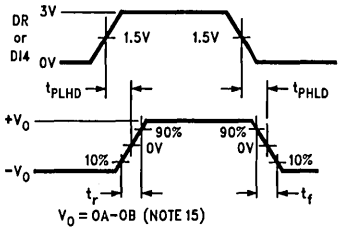
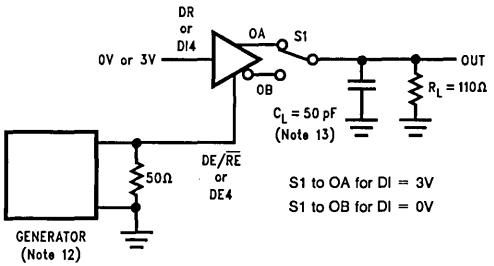
FIGURE 3. Driver Differential Propagation Delay Load Circuit



TL/F/11014-6

FIGURE 4. Driver Differential Propagation Delays and Transition Times



TL/F/11014-7

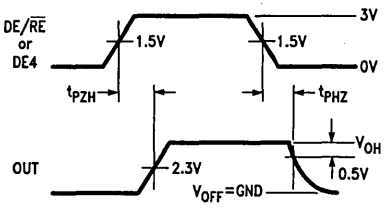


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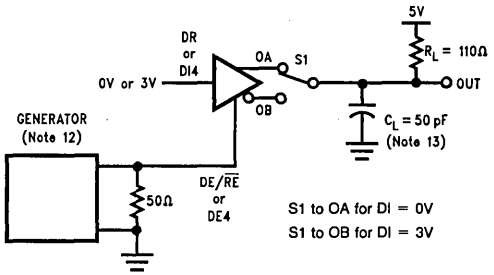
FIGURE 5. Driver Enable and Disable Timing (t_{PZH}, t_{PHZ})



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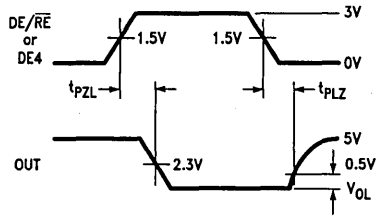
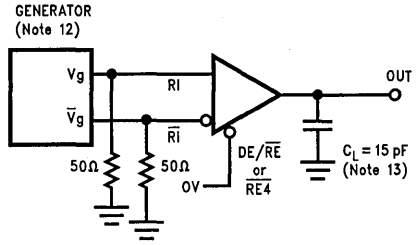


TL/F/11014-10

FIGURE 6. Driver Enable and Disable Timing (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)



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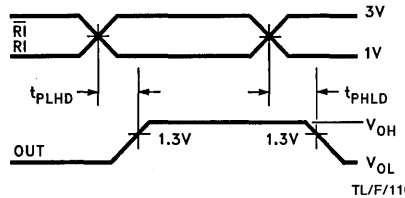

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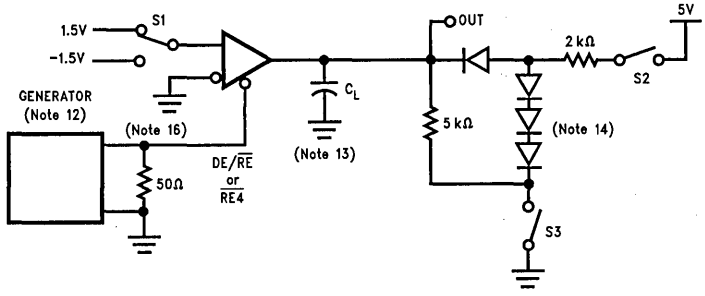
FIGURE 7. Receiver Differential Propagation Delay Timing



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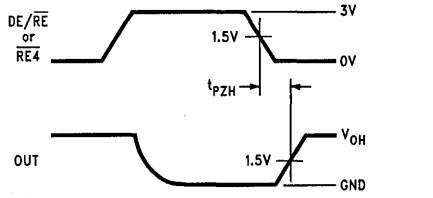
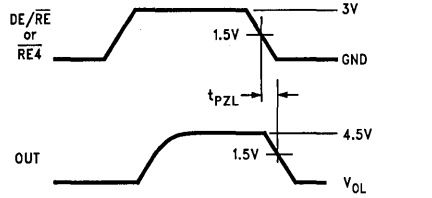


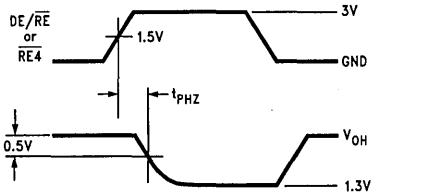
TL/F/11014–14

S1 1.5V
S2 Open
S3 Closed



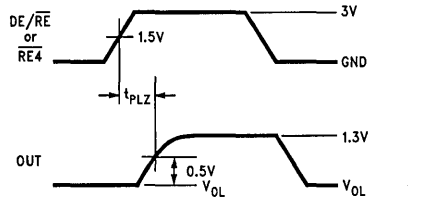
TL/F/11014–15

S1 −1.5V
S2 Closed
C3 Open



TL/F/11014–16

S1 1.5V
S2 Closed
C3 Closed

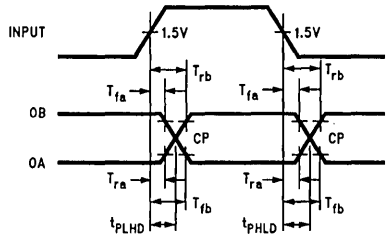


TL/F/11014–17

S1 −1.5V
S2 Closed
C3 Closed

FIGURE 8. Receiver Enable and Disable Timing

Parameter Measurement Information (Continued)



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$$T_{CP} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$$

T_{ra}, T_{rb}, T_{fa} and T_{fb} are propagation delay measurements to the 20% and 80% levels.

T_{CP} = Crossing Point

FIGURE 9. Propagation Delay Timing for Calculations of Driver Differential Propagation Delays

Note 12: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, t_r and t_f < 6.0 ns, Z_O = 50Ω.

Note 13: C_L includes probe and stray capacitance.

Note 14: Diodes are 1N916 or equivalent.

Note 15: Differential propagation delays are calculated from single-ended propagation delays measured from driver input to the 20% and 80% levels on the driver outputs *(Figure 9)*.

Note 16: On transceivers 1–3 the driver is loaded with receiver input conditions when DE/$\overline{RE}$ is high. Do not exceed the package power dissipation limit when testing.

National Semiconductor

PRELIMINARY

DS36BC956
Low Power BiCMOS HEX Differential Bus Transceiver

General Description

The DS36BC956 is a low power BiCMOS, six bit RS-485 Differential Bus Transceiver optimally designed for high speed parallel multipoint I/O buses including SCSI-1, -2, -3 and IPI interfaces. The device is offered in a thermally enhanced 48L SSOP package, offering a balance between integration and power dissipation (Junction Temperature) in an extremely small foot print. Three devices can implement a complete SCSI initiator or target interface.

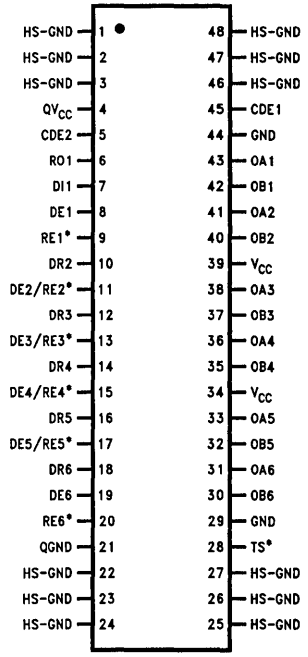
For maximum flexibility the device provides three different types of transceivers. Channel one is a type 1 configuration, with separate receiver output, driver input, and enable pins. Channels 2, 3, 4, 5 are type 2 transceivers, and provide a direction control pin and a bi-directional data pin. These channels are ideal for use on data lines and bi-directional control lines. Channel six is a type 3 transceiver, with a bi-directional data pin, and separate enable pins. This allows it to be configured as a driver, receiver, or transceiver and is ideal for use on single direction control lines.

Features

- Meets EIA RS-485 multipoint standard
- Meets SCSI-2 differential specifications
- Low power BiCMOS design
- High speed design/low skew specifications
- Available in thermally enhanced 48L SSOP package
- Glitch free driver outputs on power up and down
- Thermal shutdown protection and reporting pin (TS*)
- Wide common mode range: −7V to +12V
- 35 mV minimum hysteresis
- Flow-through pin-out

Connection Diagram

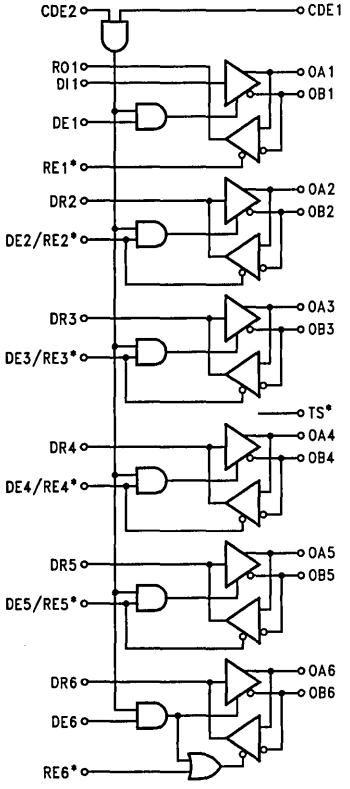
48L SSOP
DS36BC956



TL/F/11874–1

Order Number DS36BC956MEA
See NS Package Number MS48A

Logic Diagram



TL/F/11874–2

Note: * denotes active LOW pin

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}, QV_{CC})	7V
Input Voltage (DR, DI, CDE, DE/RE*, DE, RE*)	5.5V
Driver Output Voltage/Receiver Input Voltage (OA, OB)	−10V to +15V
Receiver Output Voltage (DR, RO)	5.5V
Thermal Shutdown Report Pin (TS*)	5.5V
Maximum Package Power Dissipation @ +25°C 48L SSOP Package (derate SSOP Package 16.2 mW/°C above +25°C)	2016 mW
Storage Temperatrure Range	−65°C to +150°C
Lead Temperature (Soldering 4 Sec)	+260°C
Maximum Junction Temperature (T_J)	+150°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7.0	+12	V
Operating Temperature (T_A) DS36BC956	0	70	°C

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 12)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_O	Output Voltage	I_O = 0 mA (V_{OA}, V_{OB})	OA, OB	0		V_{CC}	V
V_{OD0}	Differential Driver Output Voltage (No Load)	I_L = 0 mA, R_L = ∞ *(Figure 1)*		1.5		V_{CC}	V
V_{OD1}	Differential Driver Output Voltage (Full Load)	I_O = 60 mA, V_{CM} = 0V		1.5	1.7		V
V_{OD2}	Differential Driver Output Voltage (Termination Load)	R_L = 100Ω, (422) *(Figure 1,* Note 3)		0.5 V_{OD1} or 2.0	2.5		V
		R_L = 54Ω *(Figure 1)* (485)		1.5	2.2		V
V_{OD3}	Differential Driver Output Voltage	V_{TEST} = −7V to +12V *(Figure 2)* (485)		1.5		5.0	V
$\Delta\lvert V_{OD2}\rvert$, $\Delta\lvert V_{OD3}\rvert$	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	*(Figure 1,* Note 4) (422 and 485)				0.2	V
V_{OD4}	Differential Driver Output Voltage (SCSI-3)			1.0	2.2		V
V_{OC}	Driver Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω *(Figure 1)* (422 and 485)		−1.0	2.1	3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Common Mode Output Voltage	*(Figure 1,* Note 4) (422 and 485)				0.2	V
V_{OH}	Output Voltage HIGH	I_{OH} = −55 mA		2.7	3.0		V
V_{OL}	Output Voltage LOW	I_{OL} = 55 mA			1.5	1.7	V
V_{IH}	Input Voltage HIGH		DR, DI	2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4V (Note 6)				20	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4V (Note 6)				−100	µA

Electrical Characteristics (Continued)

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 12)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS (Continued)								
I_{OSD}	Driver Short-Circuit Output Current (Note 7)	$V_O = -7V$	(485)	OA, OB			−250	mA
		$V_O = 0V$	(422)				−150	mA
		$V_O = +12V$	(485)				250	mA
RECEIVER CHARACTERISTICS								
V_{OH}	Output Voltage HIGH *(Figure 3)*	$V_{ID} = 0.20V$	$I_{OH} = -0.4$ mA	DR, RO	2.4	3.3		V
			$I_{OH} = -0.1$ mA		3.0	3.5		V
		V_{ID} = Open	$I_{OH} = -0.4$ mA		2.4			V
V_{OL}	Output Voltage LOW	$V_{ID} = -0.20V$, $I_{OL} = 8$ mA *(Figure 3)*				0.3	0.5	V
V_{TH}	Differential Input HIGH Threshold Voltage (Note 8)	$V_O = V_{OH}$, $I_O = -0.4$ mA (422 and 485)		OA, OB			200	mV
V_{TL}	Differential Input LOW Threshold Voltage (Note 8)	$V_O = V_{OL}$, $I_O = 8.0$ mA (422 and 485)			−200			mV
V_{HST}	Hysteresis (Note 9)	$V_{CM} = 0V$			35			mV
I_{OSR}	Short Circuit Output Current	$V_O = 0V$ (Note 7)		DR, RO	−15	−30	−100	mA
I_{OZR}	TRI-STATE® Output Current	V_O = GND, 0.4V, 2.4V, V_{CC}		RO			20	μA
DEVICE CHARACTERISTICS								
V_{IH}	Enable Input Voltage HIGH			DE/RE*, CDE, DE, RE*	2.0			V
V_{IL}	Enable Input Voltage LOW						0.8	V
V_{CL}	Enable Input Clamp Voltage	$I_{CL} = -18$ mA					−1.5	V
I_{IH}	Enable Input Current HIGH	$V_{CC} = 5.25V$ and $V_{CC} = 3.0V$					20	μA
I_{IL}	Enable Input Current LOW						−20	μA
I_{IN}	Line Input Current (Note 10)	Other Input = 0V DE/RE*, CDE, and DE = 0.8V	$V_I = +12V$	OA, OB		0.5	1.0	mA
			$V_I = -7V$			−0.4	−0.8	mA
I_{ING}	Line Input Current (Power Up/Down)	Other Input = 0V DE/RE*, CDE, and DE = 2.0V $V_{CC} = 3.0V$	$V_I = +12V$			0.5	1.0	mA
			$V_I = -7V$			−0.4	−0.8	mA
V_{OL}	Output Voltage LOW	$I_{OL} = 8$ mA		TS*		0.3		V
I_{CCD}	No Load Supply Current (Note 11)	DR On, REC Off		V_{CC}		16	TBD	mA
I_{CCR}		DR Off, REC On				23	TBD	mA
I_{CCX}		DR Off, REC Off				8	TBD	mA

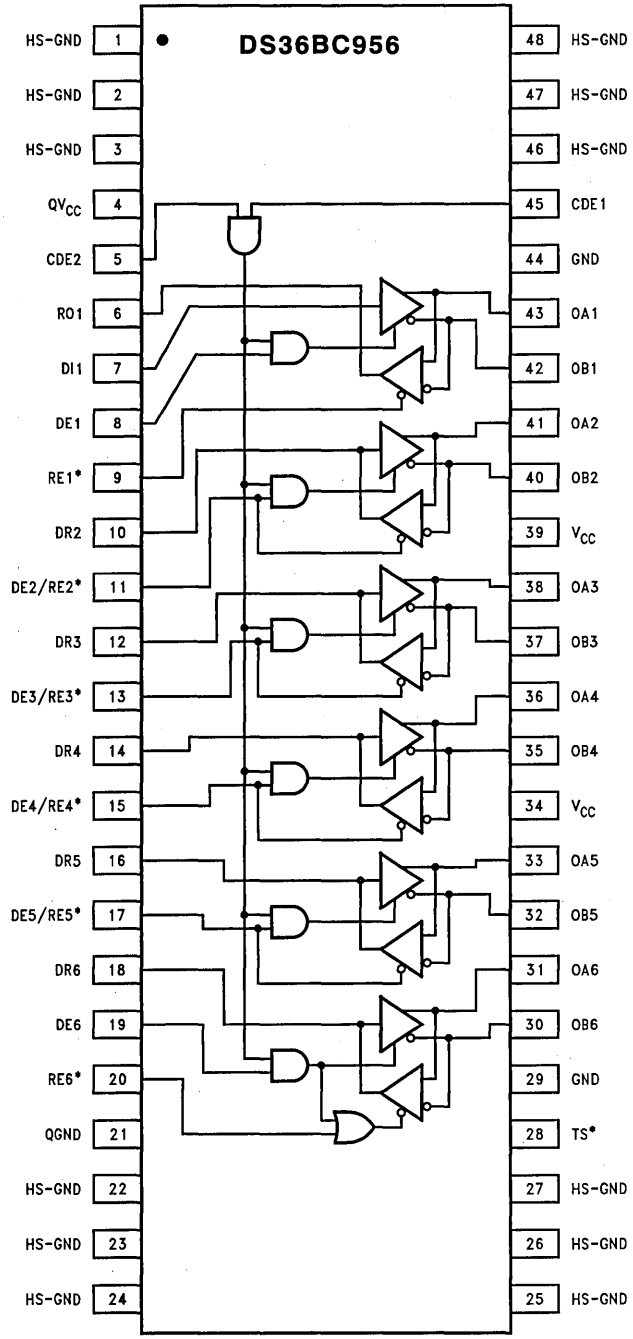
Switching Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Note 12)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DRIVER SINGLE-ENDED CHARACTERISTICS						
t_{PZH}	Output Enable Time To High Level	R_L = 110Ω *(Figure 8)*		30	60	ns
t_{PZL}	Output Enable Time To Low Level	R_L = 110Ω *(Figure 7)*		30	60	ns
t_{PHZ}	Output Disable Time From High Level	R_L = 110Ω *(Figure 8)*		30	60	ns
t_{PLZ}	Output Disable Time From Low Level	R_L = 110Ω *(Figure 7)*		30	60	ns
DRIVER DIFFERENTIAL CHARACTERISTICS (ΔV_{CC} = TBD mV, ΔT_A = TBD°C)						
t_{PLHD}	Differential Propagation Delay (Note 13)	R_L = 54Ω, C_L = 50 pF, CD = 50 pF *(Figure 4)*	tm1	9	tm1+4	ns
		R1 = R3 = 165Ω, R2 = 75Ω, CD = 60 pF *(Figure 5)*	tm2	9	tm2+4	ns
t_{PHLD}	Differential Propagation Delay (Note 13)	R_L = 54Ω, C_L = 50 pF, CD = 50 pF *(Figure 4)*	tm3	9	tm3+4	ns
		R1 = R3 = 165Ω, R2 = 75Ω, CD = 60 pF *(Figure 5)*	tm4	9	tm4+4	ns
t_r, t_f	Transition Times	R_L = 54Ω, C_L = 50 pF, CD = 50 pF *(Figure 4)*	2	4	16	ns
		R1 = R3 = 165Ω, R2 = 75Ω, CD = 60 pF *(Figure 5)*	2	4	16	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Differential Driver Skew	R_L = 54Ω, C_L = 50 pF, CD = 50 pF *(Figure 4)*		TBD	TBD	ns
		R1 = R3 = 165Ω, R2 = 75Ω, CD = 60 pF *(Figure 5)*		TBD	TBD	ns
t_{PZD}	Differential Output Enable Time	R1 = R3 = 165Ω, R2 = 75Ω CD = 60 pF *(Figure 6)*		30	60	ns
t_{PDZ}	Differential Output Disable Time			30	60	ns
RECEIVER CHARACTERISTICS (ΔV_{CC} = TBD mV, ΔT_A = TBD°C)						
t_{PLHD}	Differential Propagation Delay	C_L = 50 pF, *(Figure 9)*	tm5	TBD	tm5+5	ns
t_{PHLD}	Differential Propagation Delay		tm6	TBD	tm6+5	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Differential Receiver Skew			TBD	TBD	ns
t_{PZH}	Output Enable Time To High Level	C_L = 15 pF *(Figure 10)*		30	80	ns
t_{PZL}	Output Enable Time To Low Level			30	80	ns
t_{PHZ}	Output Disable Time From High Level			30	80	ns
t_{PLZ}	Output Disable Time From Low Level			30	80	ns

Note: TBD denotes "To Be Determined" and will be specified once characterization of the device is complete.

Logic Diagram (Continued)



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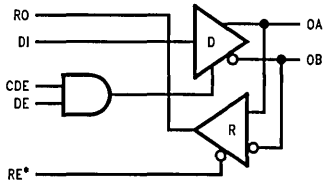
Note: * denotes active low pin.

Logic Diagram (Continued)

Transceiver 1



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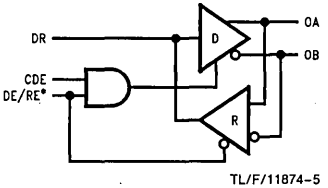
Type 1

Transceiver 2, 3, 4, and 5



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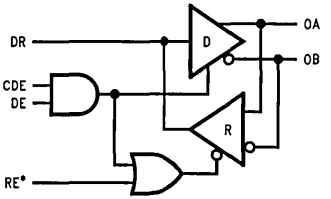
Type 2

Transceiver 6



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Type 3

Truth Tables

TRANSCEIVERS: 2, 3, 4, 5

Enables			Driver	Receiver
CDE1	CDE2	DE/RE*		
L	X	H	OFF	OFF
X	L	H	OFF	OFF
L	X	L	OFF	ON
X	L	L	OFF	ON
H	H	H	ON	OFF
H	H	L	OFF	ON

TRANSCEIVERS: 1, 6

DRIVER

Enables			Driver
CDE1	CDE2	DE	
L	X	H	OFF
X	L	H	OFF
L	X	L	OFF
X	L	L	OFF
H	H	H	ON
H	H	L	OFF

RECEIVER

Enable	Receiver
RE*	
H	OFF
L	ON

Note: For REC6 to be active (ON), DE6 must be L (LOW).

DRIVER

Driver	Input	Outputs	
	DR or DI	0A	OB
OFF	X	Z	Z
ON	L	L	H
ON	H	H	L

RECEIVER

Receiver	Inputs	Output
	OA–OB	DR or RO
OFF	X	Z
ON	OPEN	H
ON	≥ +200 mV	H
ON	≤ −200 mV	L

Parameter Measurement Information

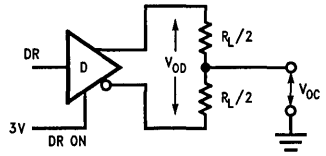


FIGURE 1. Driver Output (V_{OD},V_{OC})

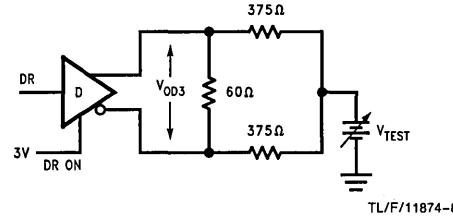


FIGURE 2. Driver Output (V_{OD3})

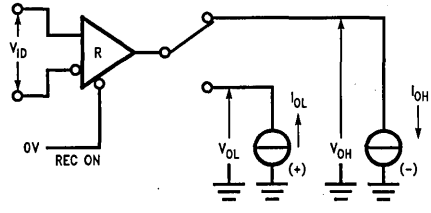
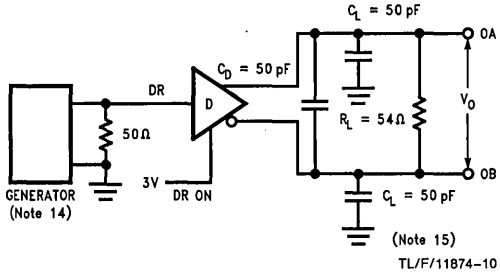


FIGURE 3. Receiver Output (V_{OH}, V_{OL})



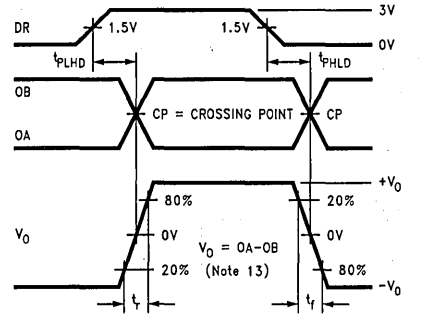
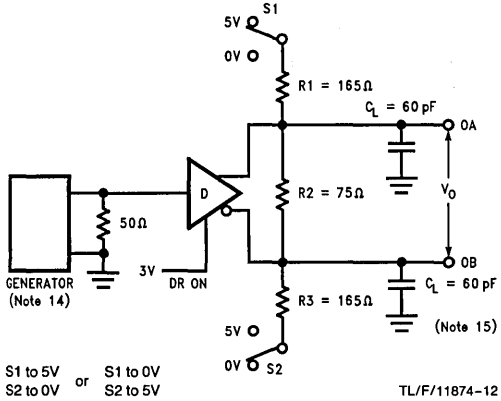


FIGURE 4. Driver Differential Propagation Delay and Transition Timing (t_{PLHD}, t_{PHLD}, t_r, t_f)



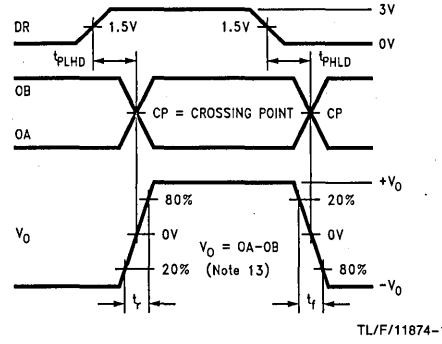
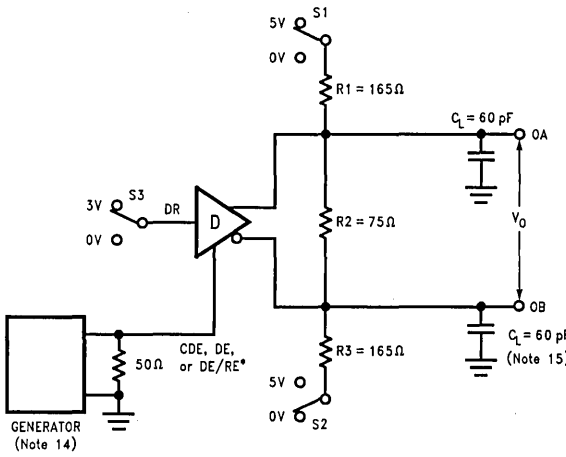


FIGURE 5. Driver Differential Propagation Delay and Transition Timing with SCSI Termination (t_{PLHD}, t_{PHLD}, t_r, t_f)

Parameter Measurement Information (Continued)



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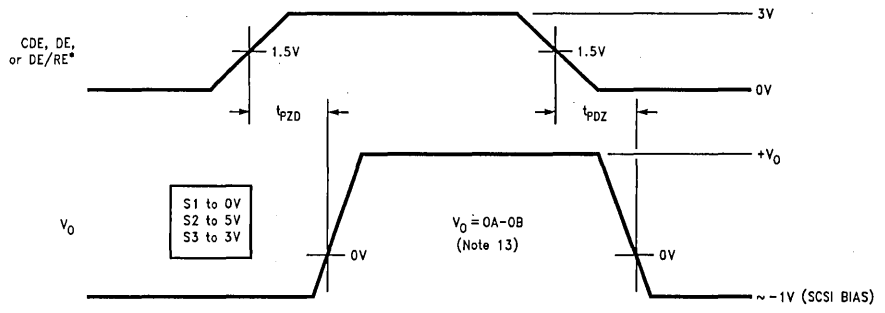

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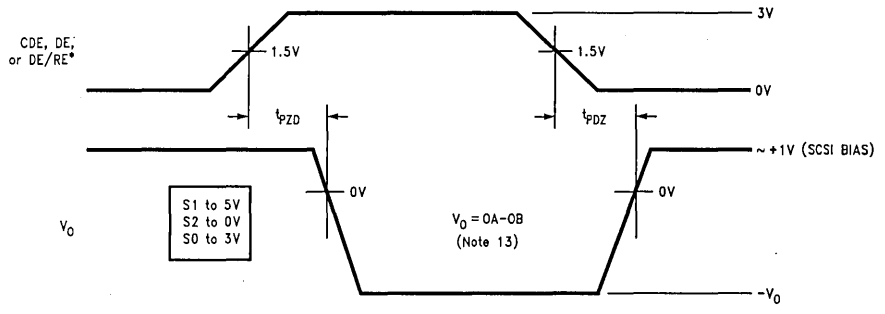

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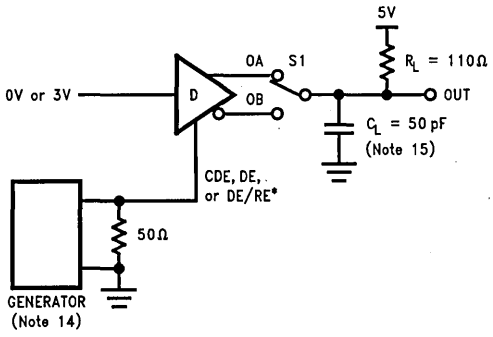
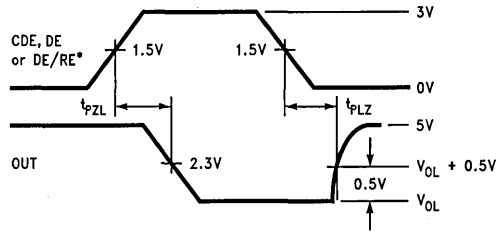
FIGURE 6. Driver Differential Enable and Disable Times with SCSI Termination (t_{PZD}, t_{PDZ})

Parameter Measurement Information (Continued)





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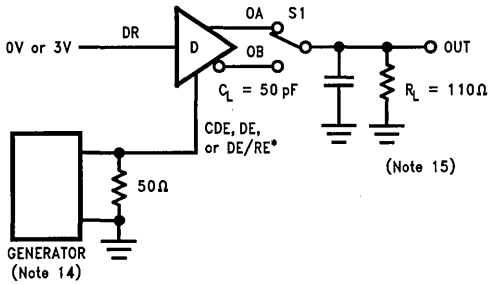
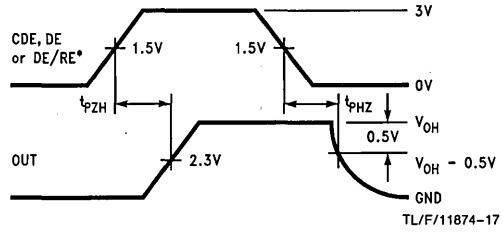
S1 to OA for DI = 0V
S1 to OB for DI = 3V

FIGURE 7. Driver Enable and Disable Timing (t_{PZL}, t_{PLZ})





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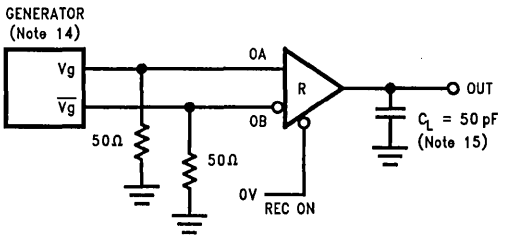
TL/F/11874–16

S1 to OA for DI = 3V
S1 to OB for DI = 0V

FIGURE 8. Driver Enable and Disable Timing (t_{PZH}, t_{PHZ})

Parameter Measurement Information (Continued)



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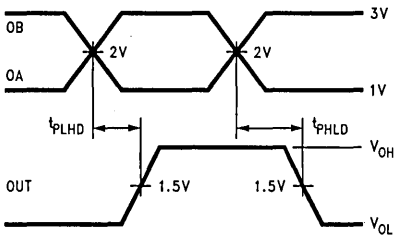

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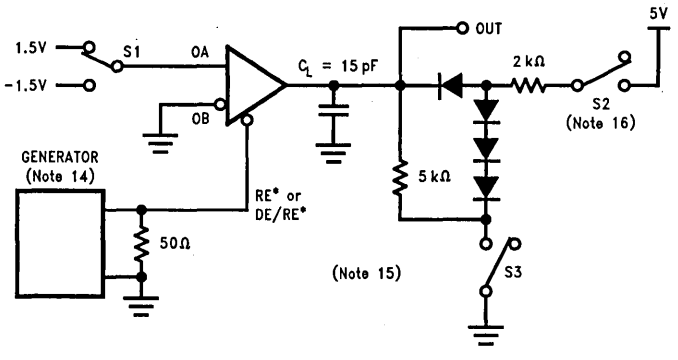
FIGURE 9. Receiver Differential Propagation Delay Timing (t_{PLHD}, t_{PHLD})



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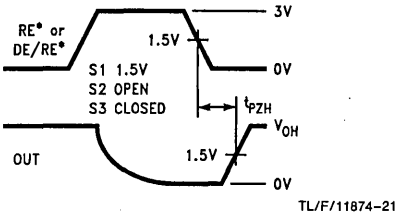

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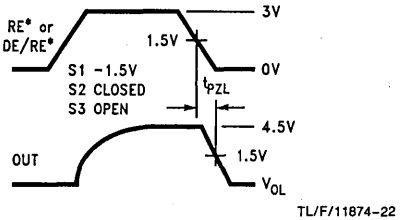

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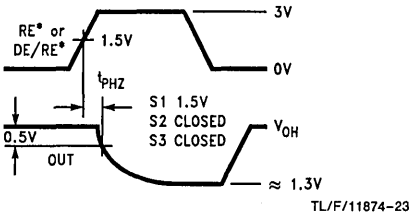

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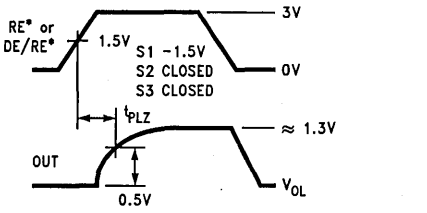

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FIGURE 10. Receiver Enable and Disable Timing (t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ})

3

Parameter Measurement Information (Continued)

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: The minimum limit is either 2.0V or 50% of the magnitude of V_{OD1}, whichever is greater.

Note 4: $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes state.

Note 5: In TIA/EIA-422-A and TIA/EIA-485 standards, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: I_{IH} and I_{IL} include driver input current and receiver TRI-STATE leakage current on DR(2-6).

Note 7: Short one output at a time to avoid causing a thermal shutdown of the device due to excessive power dissipation.

Note 8: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 9: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

Note 10: I_{IN} includes the receiver input current and TRI-STATE leakage current.

Note 11: Total package supply current.

Note 12: All typicals are given for $V_{CC} = 5.0V$ and $T_A = +25°C$.

Note 13: Differential propagation delays are calculated from single-ended propagation delays at the cross point.

Note 14: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, t_r and $t_f < 6.0$ ns, $Z_o = 50\Omega$.

Note 15: C_L includes probe and stray capacitance.

Note 16: Diodes are 1N916 or equivalent.

Pin Descriptions

V_{CC} (Pins 34, 39)—**Power Supply Pin:** Positive power supply pins for TIA/EIA-485 driver output structures. Both pins must be connected to power supply rail for proper operation of the drivers. V_{CC} range is specified from 4.75V to 5.25V, nominally 5.0V.

GND (Pins 29, 44)—**Ground Pin:** Ground pins for TIA/EIA-485 driver output structures. Both pins must be connected to ground plane for proper operation of the drivers.

QV_{CC} (Pin 4)—**Quiet Power Supply Pin:** Positive power supply pin for internal driver logic, thermal shutdown circuitry, and receivers. This pin must be connected to a power supply rail for the device to operate properly. QV_{CC} range is specified from 4.75V to 5.25V, nominally 5.0V.

QGND (Pin 21)—**Quiet Ground Pin:** Ground pin for internal driver logic, thermal shutdown circuitry, and receivers. This pin must be connected to a ground plane for the device to operate properly.

HS-GND (Pins 1, 2, 3, 22, 23, 24, 25, 26, 27, 46, 47, 48)—**Heat Sink Ground Pin:** Ground pins connected internally to an enhanced lead frame to improve the thermal performance of the package. These pins should be connected to the ground plane for maximum heat transfer. Additional PCB copper foil can be added to further enhance the thermal capabilities of the package.

CDE1,2 (Pins 45, 5)—**Common Driver Enable:** Common Driver Enable for TRI-STATE control of driver output stage. A HIGH on the driver enable pins enables the driver outputs. A LOW on a CDE pin will TRI-STATE all driver outputs.

DE1,6 (Pins 8, 19)—**Driver Enable:** Driver Enable for TRI-STATE control of driver output stage. A HIGH on the driver enable pins enables the driver output. A LOW on a DE pin will TRI-STATE the respective channels driver outputs.

DI1 (Pin 7)—**Driver Input Pin:** TTL/CMOS pin that is used as driver input.

RE*1,6 (Pins 9, 20)—**Receiver Enable Bar:** Receiver Enable for TRI-STATE control of receiver output stage. A LOW on this pin enables the receiver output. A HIGH on this pin will TRI-STATE the respective channel's receiver output.

DE/RE*2,3,4,5 (Pins 11 13, 15, 17)—**Driver Enable/Receiver Enable Bar:** Driver Enable/Receiver Enable pin provides direction control of the respective transceiver. A HIGH on this pin enables the driver output and will TRI-STATE the receiver output stage. A LOW on this pin will TRI-STATE the driver outputs and enable the receiver output stage.

DR2,3,4,5,6 (Pins 10, 12, 14, 16, 18)—**Driver Input/Receiver Output Pin:** Bi-directional TTL/CMOS pin that is used as driver input or receiver output depending upon the state of the enable pins. The driver input accepts TTL/CMOS levels. The receiver output stages are specified with TTL and CMOS loading conditions.

OA1,2,3,4,5,6 (Pins 43, 41, 38, 36, 33, 31)—**True Driver Output/Receiver Input Pin:** This pin is the true driver output (same state as input state) or the true receiver input pin depending upon enable state.

OB1,2,3,4,5,6 (Pins 42, 40, 37, 35, 32, 30)—**Inverted Driver Output/Receiver Input Pin:** This pin is the inverted driver output (opposite state of input) or the inverted receiver input pin depending upon enable state.

TS* (Pin 28)—**Thermal Shutdown:** This pin reports the occurrence of thermal shutdown which will TRI-STATE the driver outputs. Thermal shutdown typically results from severe bus faults which produce excessive on chip power dissipation. If this power dissipation elevates the function temperature above +150°C, the internal thermal shutdown circuitry is triggered and the TS* pin is asserted. The TS* pin is an open collector pin. This allows the TS* outputs of several devices to be wire ORed.

RO1 (Pin 6)—**Receiver Output Pin:** The receiver output pin is specified with TTL and CMOS loading conditions.

National Semiconductor

DS75176B/DS75176BT
Multipoint RS-485/RS-422 Transceivers

General Description

The DS75176B is a high speed differential TRI-STATE® bus/line transceiver designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition, it is compatible with RS-422.

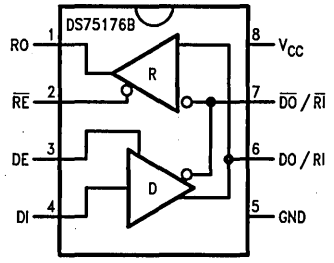
The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422.
- Small Outline (SO) Package option available for minimum board space.
- 22 ns driver propagation delays.
- Single +5V supply.
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Pin out compatible with DS3695/A and SN75176A/B.
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus.
- 70 mV typical receiver hysteresis.

Connection and Logic Diagram



TL/F/8759–1

Top View

Order Number DS75176BN, DS75176BTN, DS75176BM or DS75176BTM
See NS Package Number N08E or M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/ −10V
Receiver Input Voltages (DS75176B)	+15V/ −10V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @25°C	
for M Package	675 mW (Note 5)
for N Package	900 mW (Note 4)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Voltage at Any Bus Terminal (Separate or Common Mode)	−7	+12	V
Operating Free Air Temperature T_A			
DS75176B	0	+70	°C
DS75176BT	−40	+85	°C
Differential Input Voltage, VID (Note 6)	−12	+12	V

Electrical Characteristics (Notes 2 and 3)

0°C ≤ T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		I_O = 0				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		*(Figure 1)*	R = 50Ω; (RS-422) (Note 7)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States		*(Figure 1)*	R = 27Ω			0.2	V
V_{OC}	Driver Common Mode Output Voltage						3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E			2			V
V_{IL}	Input Low Voltage						0.8	
V_{CL}	Input Clamp Voltage			I_{IN} = −18 mA			−1.5	
I_{IL}	Input Low Current			V_{IL} = 0.4V			−200	μA
I_{IH}	Input High Current			V_{IH} = 2.4V			20	μA
I_{IN}	Input Current	DO/RI, $\overline{DO}$/$\overline{RI}$	V_{CC} = 0V or 5.25V, DE = 0V	V_{IN} = 12V			+1.0	mA
				V_{IN} = −7V			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver		−7V ≤ V_{CM} ≤ + 12V		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		V_{CM} = 0V			70		mV
V_{OH}	Receiver Output High Voltage		I_{OH} = −400 μA		2.7			V
V_{OL}	Output Low Voltage	RO	I_{OL} = 16 mA (Note 7)				0.5	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max, 0.4V ≤ V_O ≤ 2.4V				±20	μA
R_{IN}	Receiver Input Resistance		−7V ≤ V_{CM} ≤ +12V		12			kΩ
I_{CC}	Supply Current		No Load (Note 7)	Driver Outputs Enabled			55	mA
				Driver Outputs Disabled			35	mA

Electrical Characteristics (Notes 2 and 3)

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 7)			−250	mA
		$V_O = +12V$ (Note 7)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$	−15		−85	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: Derate linearly at 5.56 mW/°C to 650 mW at 70°C.

Note 5: Derate linearly @ 6.11 mW/°C to 400 mW at 70°C.

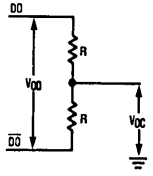
Note 6: Differential - Input/Output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

Note 7: All worst case parameters for which note 7 is applied, must be increased by 10% for DS75176BT. The other parameters remain valid for $-40°C < T_A < +85°C$.

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$

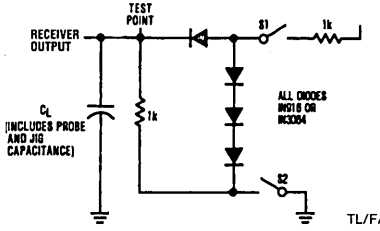
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Driver Input to Output	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF		12	22	ns
t_{PHL}	Driver Input to Output			17	22	ns
t_r	Driver Rise Time	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF (*Figures 3* and *5*)			18	ns
t_f	Driver Fall Time				18	ns
t_{ZH}	Driver Enable to Output High	$C_L = 100$ pF (*Figures 4* and *6*) S1 Open		29	100	ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100$ pF (*Figures 4* and *6*) S2 Open		31	60	ns
t_{LZ}	Driver Disable Time from Low	$C_L = 15$ pF (*Figures 4* and *6*) S2 Open		13	30	ns
t_{HZ}	Driver Disable Time from High	$C_L = 15$ pF (*Figures 4* and *6*) S1 Open		19	200	ns
t_{PLH}	Receiver Input to Output	$C_L = 15$ pF (*Figures 2* and *7*) S1 and S2 Closed		30	37	ns
t_{PHL}	Receiver Input to Output			32	37	ns
t_{ZL}	Receiver Enable to Output Low	$C_L = 15$ pF (*Figures 2* and *8*) S2 Open		15	20	ns
t_{ZH}	Receiver Enable to Output High	$C_L = 15$ pF (*Figures 2* and *8*) S1 Open		11	20	ns
t_{LZ}	Receiver Disable from Low	$C_L = 15$ pF (*Figures 2* and *8*) S2 Open		28	32	ns
t_{HZ}	Receiver Disable from High	$C_L = 15$ pF (*Figures 2* and *8*) S1 Open		13	35	ns

AC Test Circuits



TL/F/8759-2

FIGURE 1



TL/F/8759-3

Note: S1 and S2 of load circuit are closed except as otherwise mentioned.

FIGURE 2

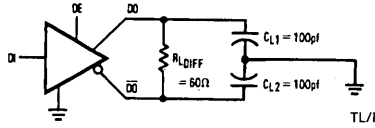


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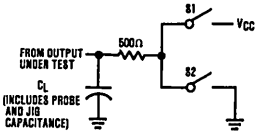
FIGURE 3



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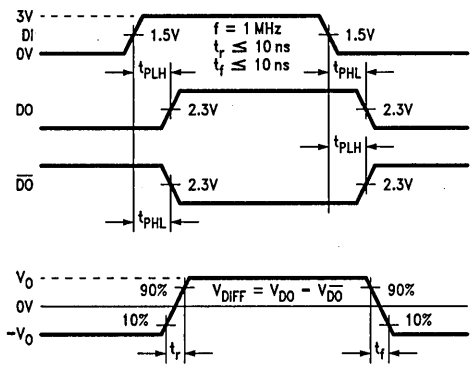
Note: Unless otherwise specified the switches are closed.

FIGURE 4

Switching Time Waveforms



TL/F/8759–6

FIGURE 5. Driver Propagation Delays and Transition Times

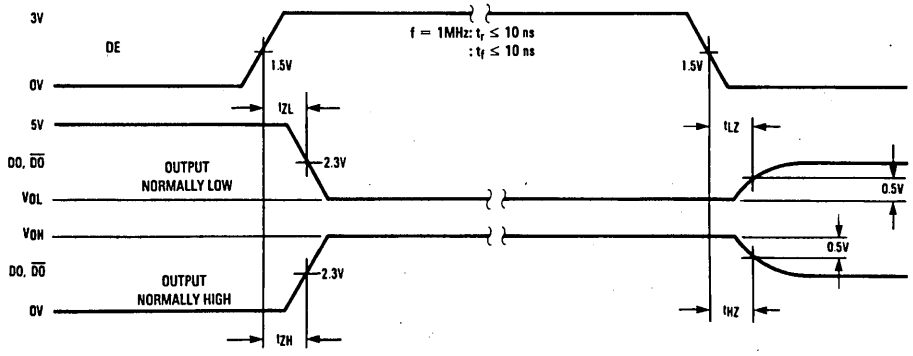


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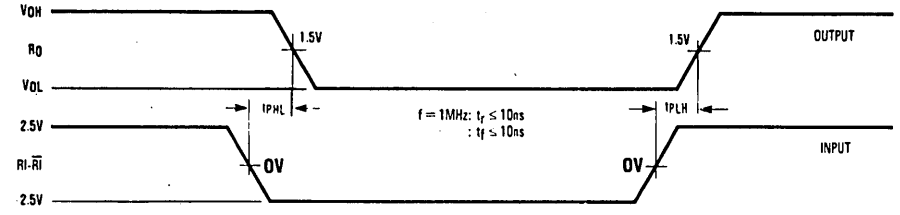
FIGURE 6. Driver Enable and Disable Times



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Note: Differential input voltage may may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 7. Receiver Propagation Delays

Switching Time Waveforms (Continued)

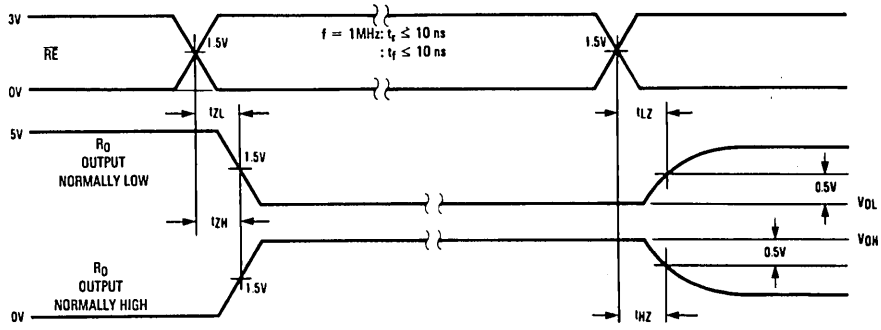

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FIGURE 8. Receiver Enable and Disable Times

Function Tables

DS75176B Transmitting

Inputs			Line Condition	Outputs	
$\overline{RE}$	DE	DI		$\overline{DO}$	DO
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

DS75176B Receiving

Inputs			Outputs
$\overline{RE}$	DE	RI-$\overline{RI}$	RO
0	0	$\geq +0.2V$	1
0	0	$\leq -0.2V$	0
0	0	Inputs Open**	1
1	0	X	Z

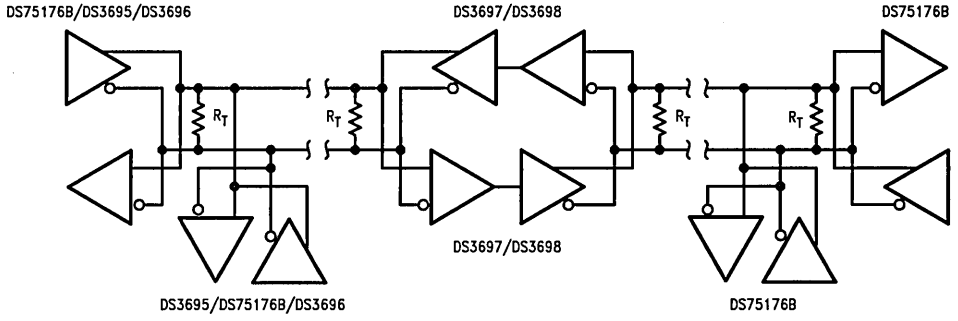
X — Don't care condition

Z — High impedance state

Fault — Improper line conditons causing excessive power dissipation in the driver, such as shorts or bus contention situations

**This is a fail safe condition

Typical Application



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National Semiconductor

DS96172/DS96174
RS-485/RS-422 Quad Differential Line Drivers

General Description

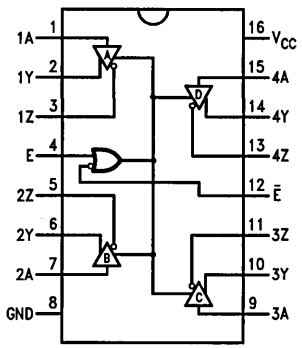
The DS96172 and DS96174 are high speed quad differential line drivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided and occurs at junction temperature of approximately 160°C. The DS96172 features an active high and active low Enable, common to all four drivers. The DS96174 features separate active high Enables for each driver pair. Compatible RS-485 receivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96173, DS96175, DS96176 AND DS96177.

Features

- Meets EIA Standard RS-485 and RS-422A
- Monotonic differential output switching
- Transmission rate to 10 Mbs
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: −7V to +12V
- Operates from single +5V supply
- Thermal shutdown protection
- DS96172/DS96174 are lead and function compatible with the SN75172/75174 or the AM26LS31/MC3487 respectively

Connection Diagrams

16-Lead DIP
DS96172



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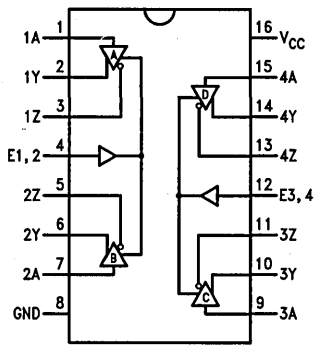
Top View

16-Lead DIP
DS96174



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Top View

Order Number DS96172CJ or DS96174CJ
See NS Package Number J16A
Order Number DS96172CN or DS96174CN
See NS Package Number N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Supply Voltage	7V
Enable Input Voltage	5.5V
Maximum Power Dissipation*	25°C
J-Cavity Package	1.74W
N-Molded Package	1.98W

*Derate cavity package 14 mW/°C above 25°C; derate molded DIP package 16 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5	5.25	V
Common Mode Output Voltage (V_{OC})	−7		+12	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

over recommended temperature and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA			3.1		V
V_{OL}	Output Voltage LOW	I_{OL} = 20 mA			0.8		V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 54Ω, *Figure 1*		1.5	2		V
		R_L = 100Ω, *Figure 1*		2	2.3		V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*				±0.2	V
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω, *Figure 1*				3	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to 12V				±100	μA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to 12V			±50	±200	μA
I_{IH}	Input Current HIGH	V_I = 2.7V				20	μA
I_{IL}	Input Current LOW	V_I = 0.5V				−100	μA
I_{OS}	Short Circuit Output Current (Note 6)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = 12V				250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled		50	70	mA
			Output Disabled		50	60	

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 2*		15	25	ns
t_{TD}	Differential Output Transition Time			15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 3*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 4*		30	45	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 5*		30	45	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 4*		25	35	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 5*		30	45	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96172/DS96174. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Δ $|V_{OD}|$ and Δ$|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: Only one output at a time should be shorted.

Parameter Measurement Information

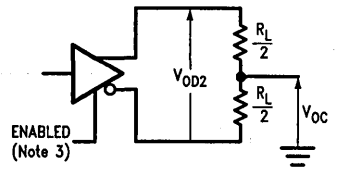

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FIGURE 1. Differential and Common Mode Output Voltage

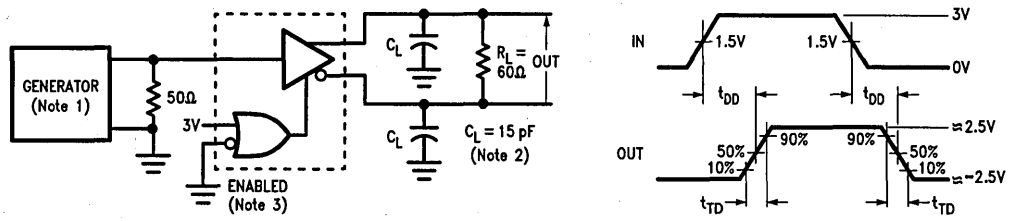

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FIGURE 2. Differential Output Delay and Transition Times

Parameter Measurement Information (Continued)

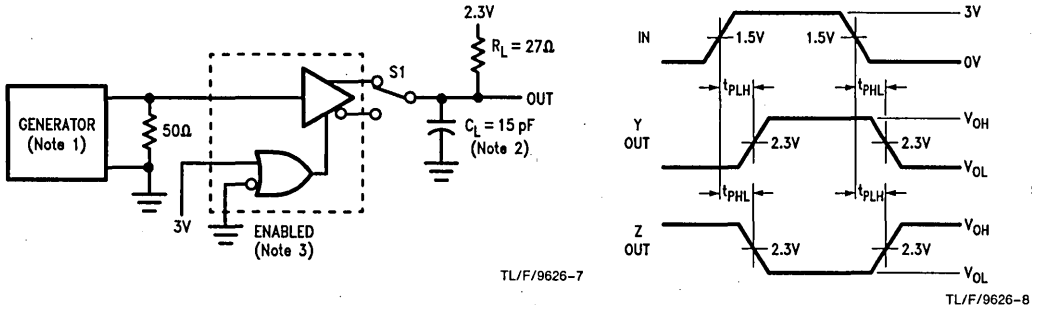

FIGURE 3. Propagation Delay Times

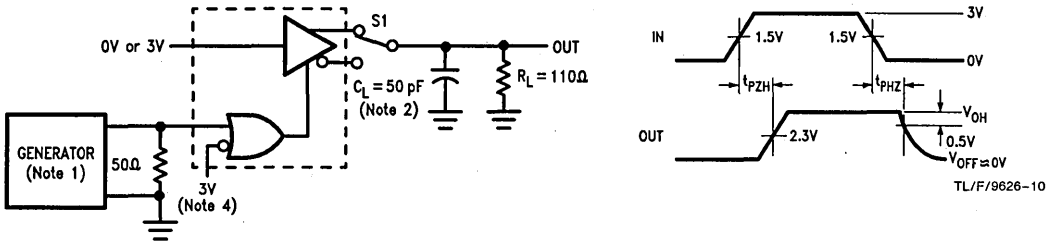

FIGURE 4. t_{PZH} and t_{PHZ}

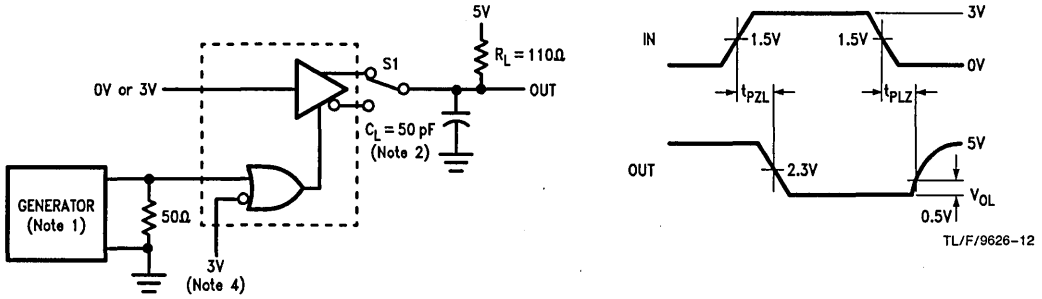

FIGURE 5. t_{PZL} and t_{PLZ}

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle = 50%, $t_r \leq 5.0$ ns, $t_f \leq 5.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Note 3: DS96172 with active high and active low Enables is shown here. DS96174 has active high Enable only.

Note 4: To test the active low Enable $\overline{E}$ of DS96172, ground E and apply an inverted waveform to $\overline{E}$. DS96174 has active high Enable only.

Function Tables

DS96172

Input A	Enables		Outputs	
	E	$\overline{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

DS96174

Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Typical Application

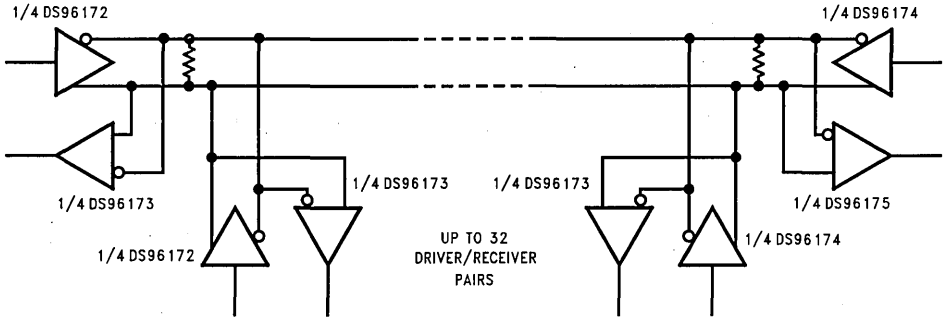

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FIGURE 6

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

National Semiconductor

DS96F172C/DS96F172M/DS96F174C/DS96F174M EIA-485/EIA-422 Quad Differential Drivers

General Description

The DS96F172 and the DS96F174 are high speed quad differential line drivers designed to meet EIA-485 Standards. The DS96F172 and the DS96F174 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F172 and DS96F174 to operate at higher speeds while minimizing power consumption.

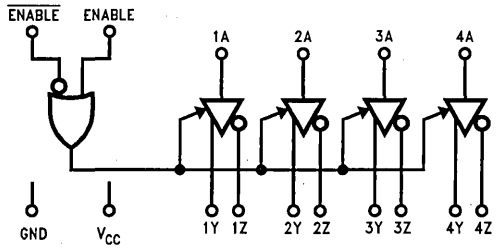
The DS96F172 and the DS96F174 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided. The DS96F172 features an active high and active low Enable, common to all four drivers. The DS96F174 features separate active high Enables for each driver pair.

Features

- Meets EIA-485 and EIA-422A standards
- Monotonic differential output switching
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: −7.0V to +12V
- Operates from single +5.0V supply
- Reduced power consumption
- Thermal shutdown protection
- DS96F172 and DS96F174 are lead and function compatible with the SN75172/174 or the AM26LS31/MC3487
- Military temperature range available
- Qualified for MIL-STD-883C
- Standard military drawings available (SMD)
- Available in DIP (J), LCC (E), and Flatpak (W) packages

Logic Diagrams

DS96F172



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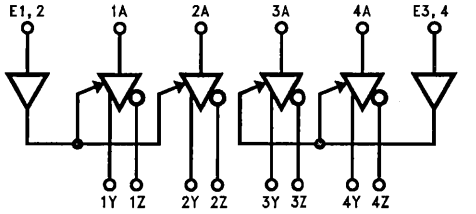
DS96F174



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Function Tables (Each Driver)

DS96F172

Input	Enable		Outputs	
A	E	$\overline{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

DS96F174

Input	Enable	Outputs	
A	E	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance (Off)

COMMERCIAL

Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately on the following pages.

Storage Temperature Range (T_{STG}) −65°C to +175°C

Lead Temperature (Soldering, 60 sec.) 300°C

Maximum Package Power Dissipation* at 25°C
Ceramic DIP (J) 1500 mW

Supply Voltage 7.0V

Enable Input Voltage 5.5V

*Derate "J" package 10 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F172C/DS96F174C	4.75	5.0	5.25	V
DS96F172M/DS96F174M	4.50	5.0	5.50	
Common Mode Output Voltage (V_{OC})	−7.0		+12.0	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A)				
DS96F172C/DS96F174C	0		+70	°C
DS96F172M/DS96F174M	−55		+125	

Electrical Characteristics

Over recommended supply voltage and operating temperature range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW		T_A = 0°C to +70°C			0.8	V
			T_A = −55°C to +125°C			0.7	
V_{OH}	Output Voltage HIGH	I_{OH} = −33 mA	T_A = 0°C to +70°C	3.0			V
V_{OL}	Output Voltage LOW	I_{OL} = 33 mA	T_A = 0°C to +70°C			2.0	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 54Ω, *Figure 1*	T_A = −55°C	1.2	2.0		V
				1.5			
		R_L = 100Ω, *Figure 1*		2.0	2.3		
V_{OD}	Differential Output Voltage	*Figure 1a*	T_A = 0°C to +70°C	1.0			V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*	−40°C to +125°C			±0.2	V
			−55°C to +125°C			±0.4	V
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω, *Figure 1*				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*				±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to +12V				±50	μA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to +12V			±20	±50	μA
I_{IH}	Input Current HIGH	V_I = 2.4V				20	μA
I_{IL}	Input Current LOW	V_I = 0.4V				−50	μA
I_{OS}	Short Circuit Output Current (Note 6)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = +12V				250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			30	

COMMERCIAL

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 2*		15	20	ns
t_{TD}	Differential Output Transition Time			15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 3*		12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	16	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 4*		25	32	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 5*		25	32	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 4*		25	30	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 5*		20	25	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND (Note 7)	*Figure 5*		300		ns
t_{SKEW}	Driver Output to Output	R_L = 60Ω		1.0	4.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS96F172M/DS96F174M and across the 0°C to +70°C range for the DS96F172C/DS96F174C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA-422A and EIA-485 standards, VOC, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: Only one output at a time should be shorted.

Note 7: For more information see Application Bulletin, contact Product Marketing.

Order Number:

DS96F172CJ
DS96F172CN
DS96F172MJ
DS96F174CJ
DS96F174MJ
NS Package Number J16A or N16A

MIL-STD-883C

Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest RETS please contact your local National Semiconductor sales office or distributor.

Storage Temperature Range (T_{STG})	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation* at 25°C	
Ceramic LCC (E)	2000 mW
Ceramic DIP (J)	1800 mW
Ceramic Flatpak (W)	1000 mW
Supply Voltage	7.0V
Enable Input Voltage	5.5V

*Above T_A = 25°C, derate "E" package 13.4, "J" package 12.5, "W" package 7.1 mW/°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC}) DS96F172M/DS96F174M	4.50	5.0	5.50	V
Common Mode Output Voltage (V_{OC})	−7.0		+12.0	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A) DS96F172M/DS96F174M	−55		+125	

Electrical Characteristics

Over recommended supply voltage and operating temperature range unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	Input Voltage HIGH			2.0		V
V_{IL}	Input Voltage LOW		T_A = 25°C		0.8	V
			T_A = −55°C, or +125°C		0.7	
V_{IC}	Input Clamp Voltage	I_I = −18 mA			−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA			6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 54Ω, V_{CC} = 4.5V *Figure 1*	T_A = −55°C	1.2		V
			T_A = 25°C, or +125°C	1.5		
		R_L = 100Ω, V_{CC} = 4.5V, *Figure 1*		2.0		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, V_{CC} = 4.5V, *Figure 1*	T_A = 25°C, or +125°C		±0.2	V
			−55°C		±0.4	V
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω, *Figure 1*			3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)	R_L = 54Ω or 100Ω, V_{CC} = 4.5V, *Figure 1*			±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to +12V			±50	μA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to +12V			±50	μA
I_{IH}	Input Current HIGH	V_I = 2.4V			20	μA
I_{IL}	Input Current LOW	V_I = 0.4V			−50	μA
I_{OS}	Short Circuit Output Current (Note 6)	V_O = −7.0V			−250	mA
		V_O = 0V			−150	
		V_O = V_{CC}			150	
		V_O = +12V			250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled		50	mA
I_{CCX}			Outputs Disabled		30	

MIL-STD-883C

Switching Characteristics V_{CC} = 5.0V

Symbol	Parameter	Conditions	T_A = 25°C		T_A = 55°C	T_A = 125°C	Units
			Typ	Max	Max	Max	
t_{DD}	Differential Output Delay Time	R_L = 60Ω, C_L = 15 pF, *Figure 2*	15	22	30	30	ns
t_{TD}	Differential Output Transition Time		15	22	40	40	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, C_L = 15 pF, *Figure 3*	12	16	25	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		12	16	25	25	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 4*	25	32	40	40	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 5*	25	35	100	100	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 4*, Note 13	25	30	80	80	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 5*	20	25	40	40	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND (Note 12)	*Figure 5*	300				ns
t_{SKEW}	Driver Output to Output	R_L = 60Ω	1.0	4.0	10	10	ns

SMD Numbers:

DS96F172MJ/883 5962-9076501MEA
DS96F172ME/883 5962-9076501M2A

DS96F174MJ/883 5962-9076502MEA
DS96F174MW/883 5962-9076502MFA
DS96F174ME/883 5962-9076502M2A

Order Number:

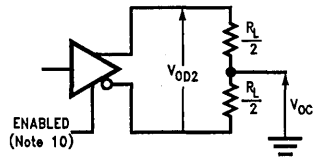
DS96F172MJ/883, DS96F174MJ/883
NS Package Number J16A

DS96F172ME/883, DS96F174ME/883
NS Package Number E20A

DS96F172MW-MIL, DS96F174MW/883
NS Package Number W16A

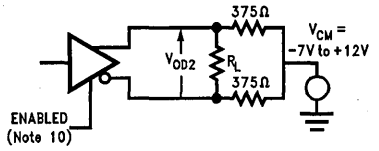
For Complete Military 883 Specifications, see RETS Data Sheet.

Parameter Measurement Information



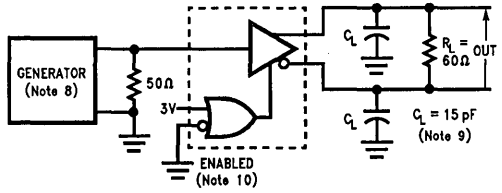
TL/F/9625-3

FIGURE 1. Differential and Common Mode Output Voltage

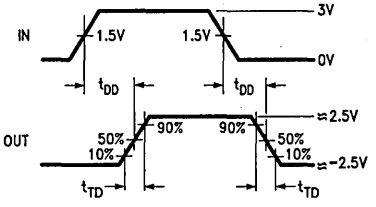


TL/F/9625-13

FIGURE 1a. Differential Output Voltage with Varying Common Mode Voltage

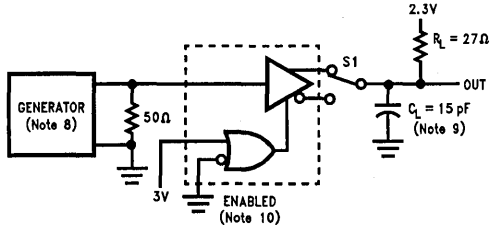


TL/F/9625-4

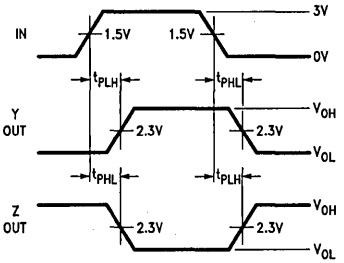


TL/F/9625-5

FIGURE 2. Differential Output Delay and Transition Times

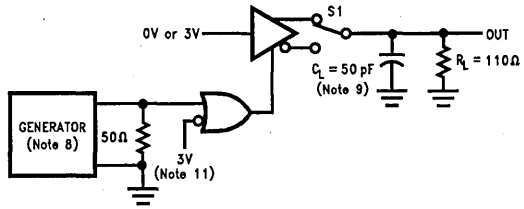


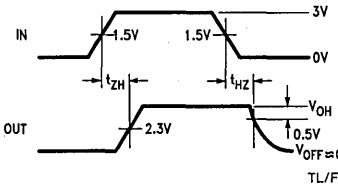
TL/F/9625-6



TL/F/9625-7

FIGURE 3. Propagation Delay Times



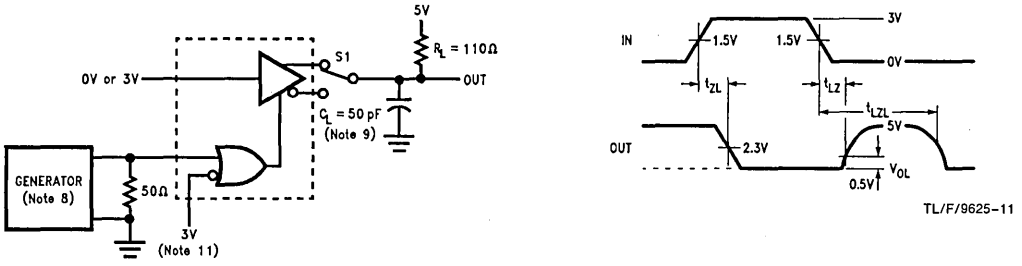


TL/F/9625-9

TL/F/9625-8

FIGURE 4. t_{ZH} and t_{HZ}

Parameter Measurement Information (Continued)



TL/F/9625-10

FIGURE 5. t_{ZL}, t_{LZ}, t_{LZL}

Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, duty cycle = 50%, $t_r \leq 5.0$ ns, $t_f \leq 5.0$ ns, $Z_O = 50\Omega$.

Note 9: C_L includes probe and jig capacitance.

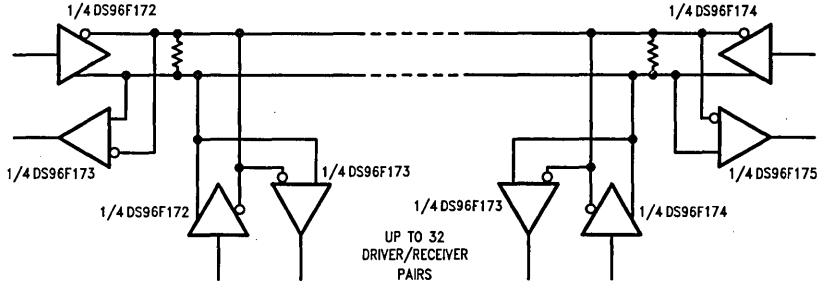
Note 10: DS96F172 with active high and active low Enables is shown. DS96F174 has active high Enable only.

Note 11: To test the active low Enable $\overline{E}$ of DS96F172 ground E and apply an inverted waveform to $\overline{E}$. DS96F174 has active high Enable only.

Note 12: For more information see Application Bulletin, Contact Product Marketing.

Note 13: Not tested for DS96F172MW-MIL device.

Typical Application



TL/F/9625-12

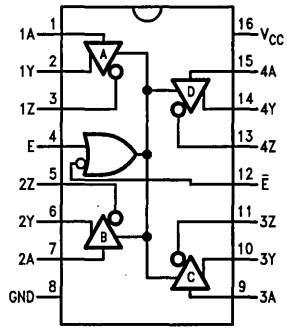
Note:

The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

Connection Diagrams

16-Lead Ceramic Dual-In-Line Package
NS Package Number J16A

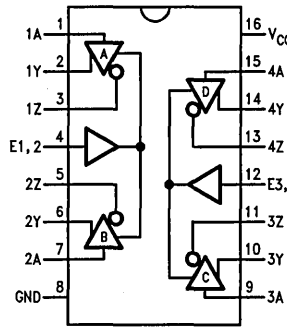
DS96F172



TL/F/9625–1

Top View

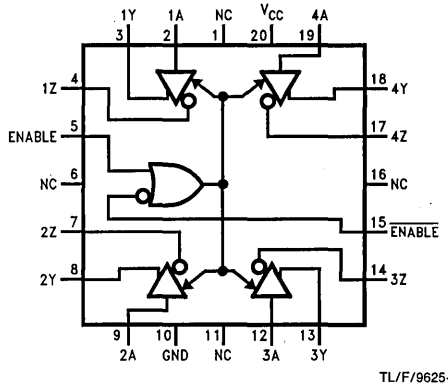
DS96F174



TL/F/9625–2

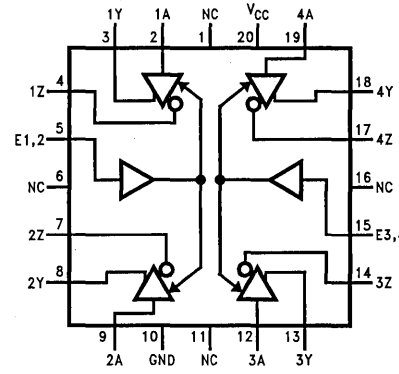
Top View

20-Lead Ceramic Leadless Chip Carrier
NS Package Number E20A



TL/F/9625–18

Top View

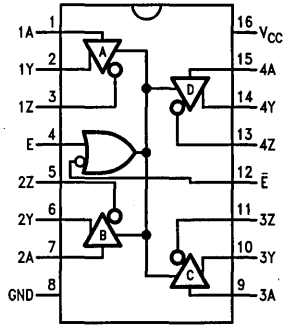


TL/F/9625–19

Top View

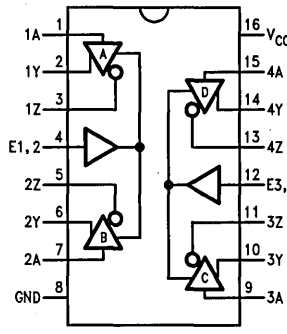
NC = No connection

16-Lead Ceramic Flatpak
NS Package Number W16A



TL/F/9625–1

Top View



TL/F/9625–2

Top View

Order Numbers are located at the end of the respective Electrical Tables.

National Semiconductor

DS96173/DS96175
RS-485/RS-422 Quad Differential Line Receivers

General Description

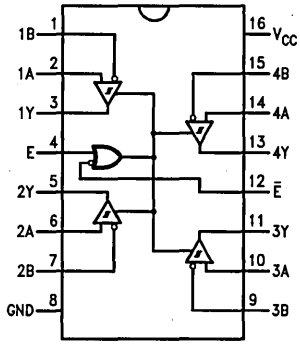
The DS96173 and DS96175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96173 features an active high and active low Enable, common to all four receivers. The DS96175 features separate active high Enables for each receiver pair. Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96172, DS96174, DS96176 and DS96177.

Features

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Designed for multipoint bus applications
- TRI-STATE Outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5V supply
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- DS96173/DS96175 are lead and function compatible with SN75173/75175 or the AM26LS32/MC3486 respectively

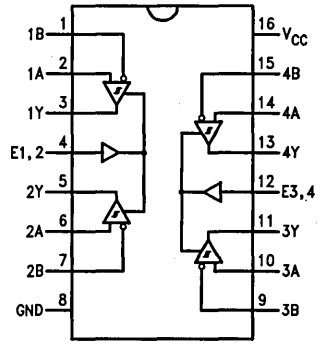
Connection Diagrams

16-Lead DIP
DS96173



TL/F/9628–1

16-Lead DIP
DS96175



TL/F/9628–2

Order Number DS96173CJ, DS96173CN, DS96175CJ or DS96175CN
See NS Package Number J16A or N16A

3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
J-Cavity Package	1.63W
N-Molded Package	1.84W
Supply Voltage	7V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7V
Low Level Output Current	50 mA

*Derate cavity package 13 mW/°C above 25°C; derate molded DIP package 15 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5	5.25	V
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})	−7		+12	V
Output Current High (I_{OH})			−400	μA
Output Current LOW (I_{OL})			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = − 0.4 mA				0.2	V
V_{TL}	Differential Input (Note 4) Low Threshold Voltage	V_O = 0.5V, I_O = 16 mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 5)	V_{CM} = 0V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA		2.7			V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High Impedance State Output	V_O = 0.4V to 2.4V				±20	μA
I_I	Line Input Current (Note 6)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15		−85	mA
I_{CC}	Supply Current	Outputs Disabled				75	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS96173/DS96175. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 5: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 6: Refer to EIA Standards RS-485 for exact conditions.

Note 7: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to 2.5V, C_L = 15 pF, *Figure 1*		15	25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			15	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 2*		15	22	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 15 pF, *Figure 3*		15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF, *Figure 2*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF, *Figure 3*		24	40	ns

Function Tables

(Each Receiver) DS96173

Differential Inputs	Enables		Outputs
A−B	E	$\overline{E}$	V
V_{ID} > 0.2V	H	X	H
	X	L	H
V_{ID} < −0.2V	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

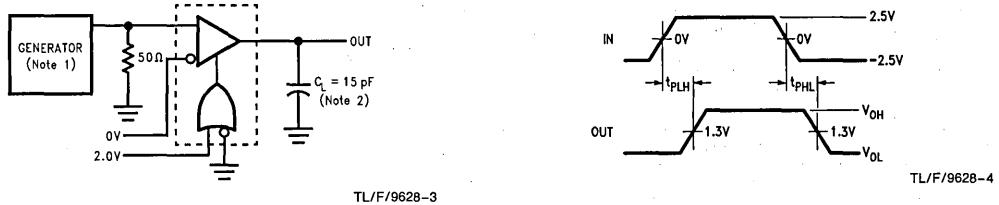
H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

(Each Receiver) DS96175

Differential Inputs A−B	Enable	Output Y
$V_{ID} \geq$ 0.2V	H	H
$V_{ID} \leq$ −0.2V	H	L
X	L	Z

3

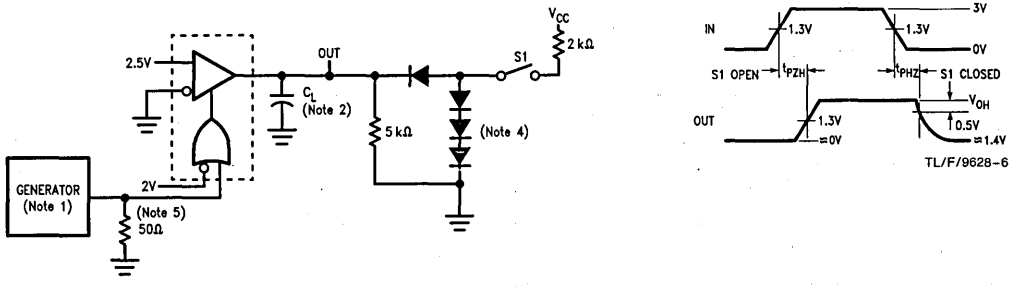
Parameter Measurement Information



TL/F/9628-3

TL/F/9628-4

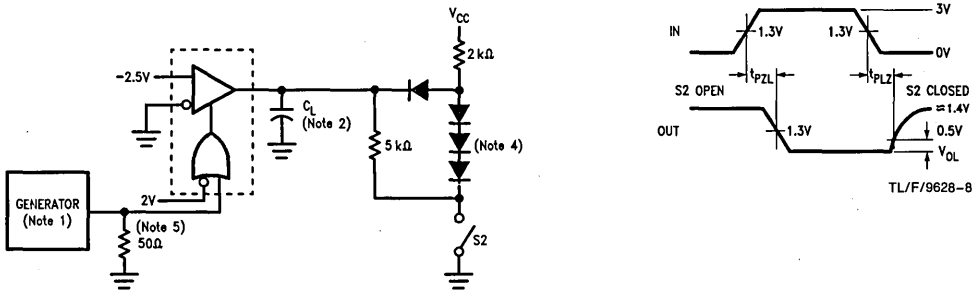
FIGURE 1. t_{PLH}, t_{PHL} (Note 3)



TL/F/9628-5

TL/F/9628-6

FIGURE 2. t_{PHZ}, t_{PZH} (Note 3)



TL/F/9628-7

TL/F/9628-8

FIGURE 3. t_{PZL}, t_{PLZ} (Note 3)

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

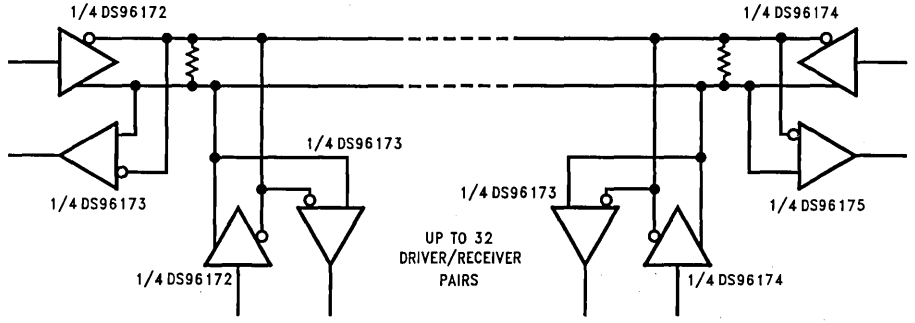
Note 2: C_L includes probe and stray capacitance.

Note 3: DS96173 with active high and active low Enables is shown here. DS96175 has active high Enable only.

Note 4: All diodes are 1N916 or equivalent.

Note 5: To test the active low Enable $\overline{E}$ of DS96173, ground E and apply an inverted input waveform to $\overline{E}$. DS96175 has active high Enable only.

Typical Application



TL/F/9628–9

FIGURE 4

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

National Semiconductor

DS96F173C/DS96F173M/DS96F175C/DS96F175M EIA-485/EIA-422 Quad Differential Receivers

General Description

The DS96F173 and the DS96F175 are high speed quad differential line receivers designed to meet the EIA-485 standard. The DS96F173 and the DS96F175 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F173 and DS96F175 to operate at higher speeds while minimizing power consumption.

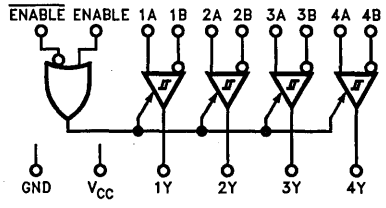
The DS96F173 and the DS96F175 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers. The DS96F175 features separate active high Enables for each receiver pair.

Features

- Meets EIA-485, EIA-422A, EIA-423A standards
- Designed for multipoint bus applications
- TRI-STATE outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5.0V supply
- Reduced power consumption (I_{CC} = 50 mA max)
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- Military temperature range available
- Qualified for MIL STD 883C
- Available to standard military drawings (SMD)
- Available in DIP(J), LCC(E), and FlatPak (W) packages
- DS96F173 and DS96F175 are lead and function compatible with SN75173/175 or the AM26LS32/MC3486

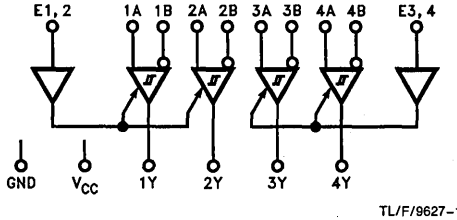
Logic Diagrams

DS96F173



TL/F/9627–10

DS96F175



TL/F/9627–11

Function Tables

(Each Receiver) DS96F173

Differential Inputs A–B	Enable E	Enable $\overline{E}$	Output Y
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

H = High Level
L = Low Level
Z = High Impedance (off)
X = Don't Care

(Each Receiver) DS96F175

Differential Inputs A–B	Enable E	Output Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

COMMERCIAL

Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately.

Storage Temperature Range (T_{STG})	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Max. Package Power Dissipation* at 25°C Ceramic DIP (J)	1500 mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50 mA

*Derate package 10 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F173C/DS96F175C	4.75	5.0	5.25	V
DS96F173M/DS96F175M	4.50	5.0	5.50	
Common Mode Input Voltage (V_{CM})	−12		+12	V
Differential Input Voltage (V_{ID})			|12|	V
Output Current HIGH (I_{OH})			−400	μA
Output Current LOW (I_{OL})			11	mA
Operating Temperature (T_A)				
DS96F173C/DS96F175C	0	25	70	°C
DS96F173M/DS96F175M	−55	25	125	

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	$V_O = V_{OH}$				0.2	V
V_{TL}	Differential-Input (Note 4) Low Threshold Voltage	$V_O = V_{OL}$		−0.2			V
$V_{TH} - V_{TL}$	Hysteresis (Note 5)	$V_{CM} = 0V$			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV	0°C to +70°C	2.8			V
		$I_{OH} = -400$ μA	−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV	$I_{OL} = 8.0$ mA			0.45	V
			$I_{OL} = 11$ mA			0.50	
I_{OZ}	High-Impedance State Output	$V_O = 0.4V$ to 2.4V				±20	μA
I_I	Line Input Current (Note 6)	Other Input = 0V	$V_I = 12V$			1.0	mA
			$V_I = -7.0V$			−0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$				−100	μA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15		−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			50	

3

COMMERCIAL

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to +2.5V, C_L = 15 pF, *Figure 1* V_{CM} = 0V	5.0	15	22	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		5.0	15	22	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 2*		12	16	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, *Figure 3*		13	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 2*		14	20	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0 pF, *Figure 3*		14	18	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 1*		1.0	3.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS96F173M/DS96F175M and across the 0°C to +70°C range for the DS96F173C/DS96F175C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 5: Hysteresis is the difference between the positive-going input threshold voltage. V_{TH}, and the negative going input threshold voltage, V_{TL}.

Note 6: Refer to EIA-485 Standard for exact conditions.

Note 7: Only one output at a time should be shorted.

Order Number:

DS96F173CJ
DS96F173MJ
DS96F175CJ
DS96F175MJ
See NS Package Number J16A

MIL-STD-883C

Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the current Reliability Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest version of the RETS please contact your local National Semiconductor sales office or distributor.

Storage Temperature Range (T_{STG})	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Max. Package Power Dissipation* at 25°C	
Ceramic DIP (J)	1500 mW
Ceramic Flatpak (W)	1034 mW
Ceramic LCC (E)	1500 mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50 mA

*Above T_A = 25°C derate J package 10 mW/°C, W package 6.90 mW/°C, E package 11.11 mW/°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC}) DS96F173M/DS96F175M	4.50	5.0	5.50	V
Common Mode Input Voltage (V_{CM})	−12		+12	V
Differential Input Voltage (V_{ID})			|12|	V
Output Current HIGH (I_{OH})			−400	μA
Output Current LOW (I_{OL})			11	mA
Operating Temperature (T_A) DS96F173M/DS96F175M	−55	25	125	°C

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	V_{CC} = 4.5V, 5.5V V_{CM} = 0V, 12V, −12V			0.2	V
V_{TL}	Differential-Input (Note 4) Low Threshold Voltage	V_{CC} = 4.5V, 5.5V V_{CM} = 0V, 12V, −12V		−0.2		V
V_{IH}	Enable Input Voltage HIGH			2.0		V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA, V_{CC} = 4.5V			−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV I_{OH} = −400 μA	−55°C to +125°C	2.5		V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV	I_{OL} = 8.0 mA		0.45	V
I_{OZ}	High-Impedance State Output	V_O = 0.4V, 2.4V, V_{CC} = 5.5V			±20	μA
I_I	Line Input Current (Note 6)	Other Input = 0V	V_I = 12V		1.0	mA
			V_I = −7.0V		−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V, V_{CC} = 5.5V			20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V, V_{CC} = 5.5V			−100	μA
R_I	Input Resistance			10		kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15	−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled or Disabled		50	mA
I_{CCX}						

MIL-STD-883C

Switching Characteristics V_{CC} = 5.0V

Symbol	Parameter	Conditions	T_A = 25°C		T_A = −55°C	T_A = 125°C	Units
			Typ	Max	Max	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to +2.5V, C_L = 15 pF, *Figure 1* V_{CM} = 0V	15	22	30	30	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		15	22	30	30	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 2*	12	16	27	27	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, *Figure 3*	13	18	27	27	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 2* (Note 13)	14	20	27	27	ns
		C_L = 20 pF, *Figure 2* (Note 13)	14	30	37	37	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0 pF, *Figure 3*	14	18	30	30	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 1*	1	3	5.0	5.0	ns

SMD Number:

DS96F173MJ	**5962-9076602 MEA**
DS96F173MW	**5962-9076602 MFA**
DS96F173ME	**5962-9076602 M2A**
DS96F175MJ	**5962-9076601 MEA**
DS96F175MW	**5962-9076601 MFA**
DS96F175ME	**5962-9076601 M2A**

Order Number:

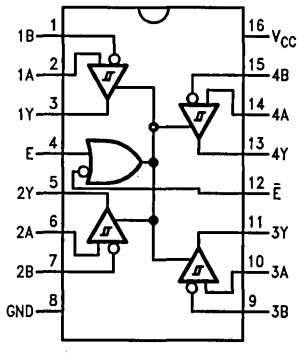
883 Marking	SMD Marking
DS96F173MJ/883	**DS96F173MJ-SMD**
DS96F175MJ/883	**DS96F175MJ-SMD**
See NS Package Number J16A	
DS96F173ME/883	**DS96F173ME-SMD**
DS96F175ME/883	**DS96F175ME-SMD**
See NS Package Number E20A	
DS96F173MW/883	**DS96F173MW-SMD**
DS96F175MW/883	**DS96F175MW-SMD**
See NS Package Number W16A	

For Complete Military 883 Specifications, see RETS Data Sheet.

Connection Diagrams

16-Lead Ceramic Dual-In-Line Package
NS Package Number J16A

DS96F173



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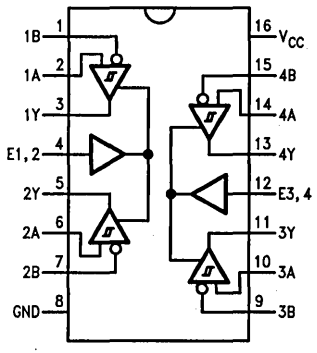
Top View

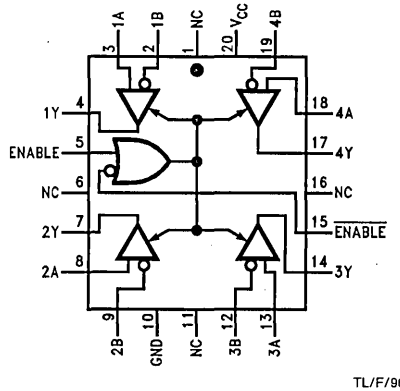
DS96F175



TL/F/9627–2

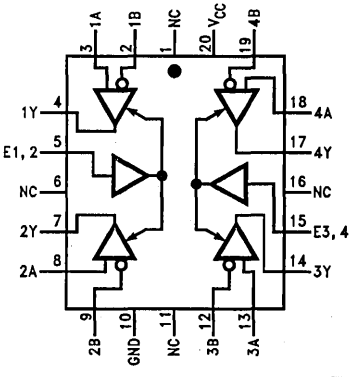
Top View

20-Lead Ceramic Leadless Chip Carrier
NS Package Number E20A



TL/F/9627–12

Top View

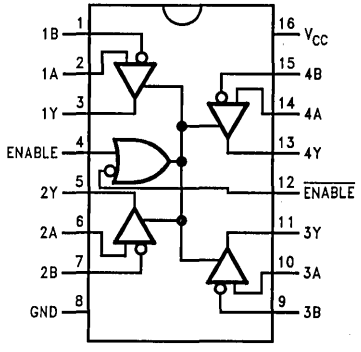


TL/F/9627–13

Top View

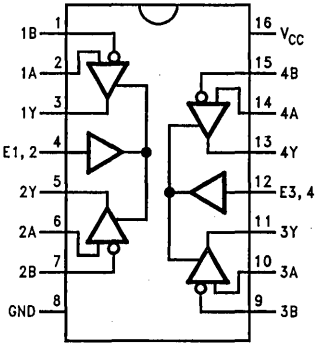
*NC—No Connection

16-Lead Ceramic FlatPak
NS Package Number W16A



TL/F/9627–14

Top View

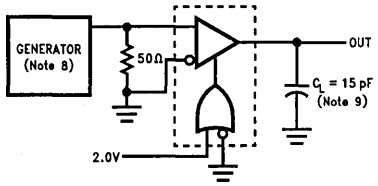


TL/F/9627–15

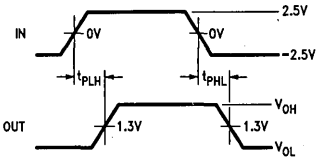
Top View

Order Numbers are located at the end of the respective Electrical Tables.

Parameter Measurement Information

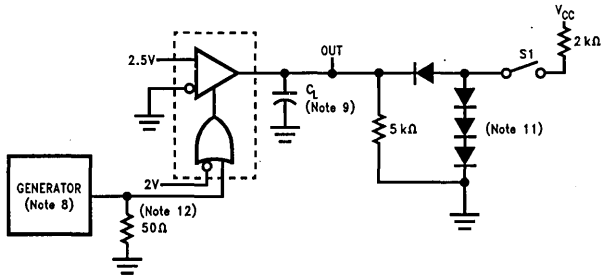


TL/F/9627–3



TL/F/9627–4

FIGURE 1. t_{PLH}, t_{PHL} (Note 10)



TL/F/9627–5

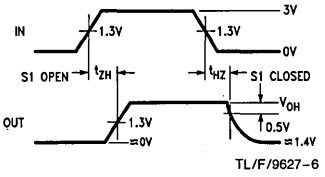


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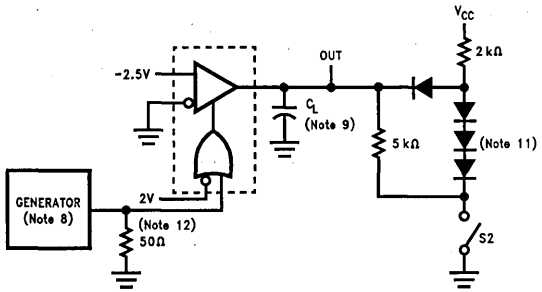
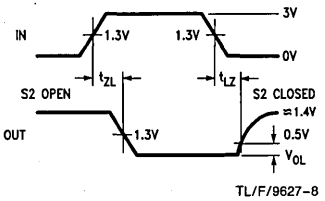
FIGURE 2. t_{HZ}, t_{ZH} (Note 10)



TL/F/9627–7



TL/F/9627–8

FIGURE 3. t_{ZL}, t_{LZ} (Note 10)

Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 9: C_L includes probe and stray capacitance.

Note 10: DS96F173 with active high and active low Enables are shown. DS96F175 has active high Enable only.

Note 11: All diodes are 1N916 or equivalent.

Note 12: To test the active low Enable $\overline{E}$ of DS96F173, ground E and apply an inverted input waveform to $\overline{E}$. DS96F175 has active high enable only.

Note 13: Testing at 20 pF assures conformance to 5 pF specification.

Typical Application

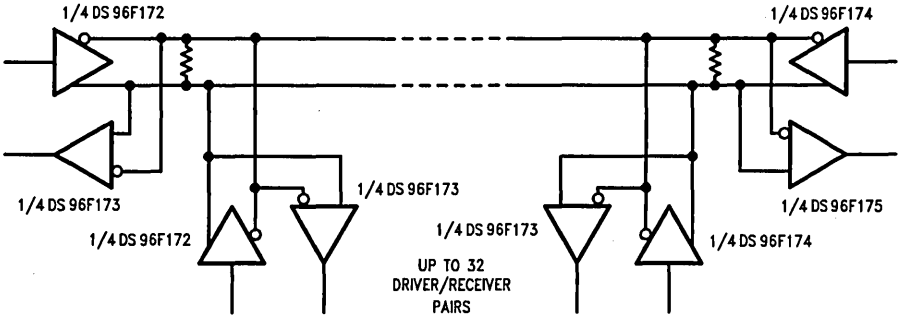


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FIGURE 4

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

National Semiconductor

DS96176
RS-485/RS-422 Differential Bus Transceiver

General Description

The DS96176 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets EIA Standard RS-485 as well as RS-422A.

The DS96176 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current-limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at junction temperature of approximately 160°C. The receiver features a typical input impedance of 15 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

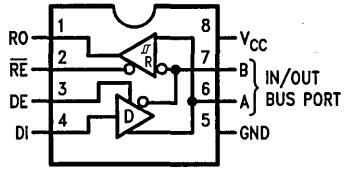
The DS96176 can be used in transmission line applications employing the DS96172 and the DS96174 quad differential line drivers and the DS96173 and DS96175 quad differential line receivers.

Features

- Bidirectional transceiver
- Meets EIA Standard RS-422A and RS-485
- Designed for multipoint transmission
- TRI-STATE driver and receiver enables
- Individual driver and receiver enables
- Wide positive and negative input/output bus voltage ranges
- Driver output capability ±60 mA Maximum
- Thermal shutdown protection
- Driver positive and Negative current-limiting
- High impedance receiver input
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power requirements

Connection Diagram

8-Lead DIP



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Top View

Order Number DS96176CJ or DS96176CN
See NS Package Number J08E or N08E

Function Table

Driver

Input	Enable	Outputs	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A-B	$\overline{RE}$	R
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP: −65°C to +150°C

Lead Temperature
- Ceramic DIP (soldering, 60 sec.): 300°C
- Molded DIP (soldering, 10 sec.): 265°C

Maximum Power Dissipation* at 25°C
- Cavity Package: 1300 mW
- Molded Package: 930 mW

Supply Voltage: 7.0V

Differential Input Voltage: +15V/−10V

Enable Input Voltage: 5.5V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Voltage at Any Bus Terminal (Separately or Common Mode)	−7.0		12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

DRIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA			3.1		V
V_{OL}	Output Voltage LOW	I_{OL} = 20 mA			0.85		V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, *Figure 1*		2.0	2.25		V
		R_L = 54Ω, *Figure 1* and *2*		1.5	2.0		
$\Delta\|V_{OD2}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω, V_{CM} = 0V *Figure 1* and *2*				±0.2	V
		R_L = 100Ω *Figure 1*					
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω, *Figure 1*				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current (Note 4) (Includes Receiver I_I)	Output Disabled	V_O = 12V			1.0	mA
			V_O = −7.0V			−0.8	
I_{IH}	Input Current HIGH	V_I = 2.4V				20	μA
I_{IL}	Input Current LOW	V_I = 0.4V				−100	μA
I_{OS}	Short Circuit Output Current (Note 9)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = 12V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

Electrical Characteristics (Continued)

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

RECEIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = 0.5V, I_O = 8.0 mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	V_{CM} = 0V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 3*		2.7			V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV, *Figure 3*	I_{OL} = 8,0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High Impedance State Output	V_O = 0.45V to 2.4V				±20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7.0V			0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			40	mA
			Outputs Disabled				

Driver Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{TD}	Differential Output Transition Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 6*		25	35	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 7*		25	35	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 6*		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 7*		29	35	ns

Receiver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to 3.0V, C_L = 15 pF, *Figure 8*		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 9*		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 9*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96176. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage V_{T+}, and the negative-going input threshold voltage, V_{T-}.

Note 8: Refer to EIA Standard RS-485 for exact conditions.

Note 9: Only one output at a time should be shorted.

Parameter Measurement Information

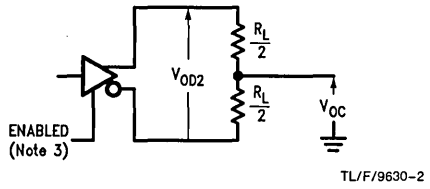


FIGURE 1. Driver V_{OD} and V_{OC}

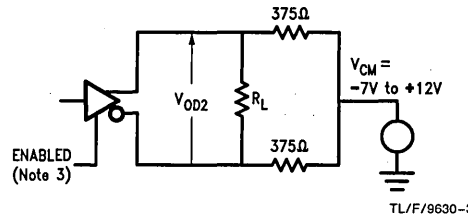


FIGURE 2. Driver V_{OD} with Varying Common Mode Voltage

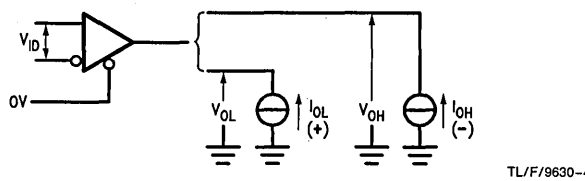
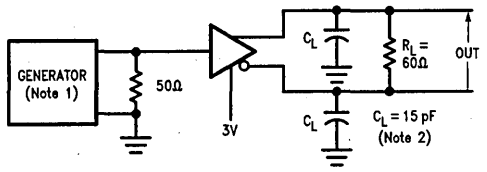


FIGURE 3. Receiver V_{OH} and V_{OL}

Parameter Measurement Information (Continued)



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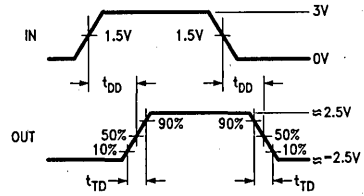

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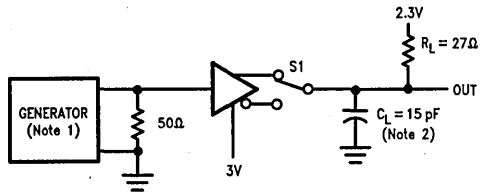
FIGURE 4. Driver Differential Output Delay and Transition Times



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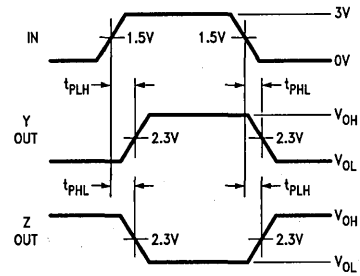

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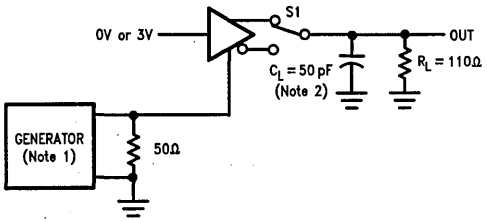
FIGURE 5. Driver Propagation Times



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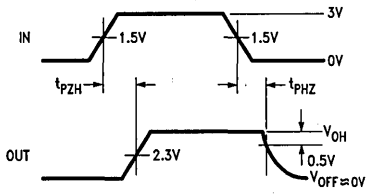

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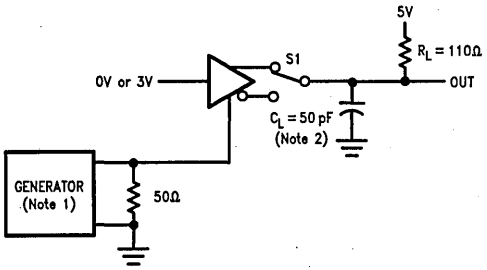
FIGURE 6. Driver Enable and Disable Times (t_{PZH}, t_{PHZ})



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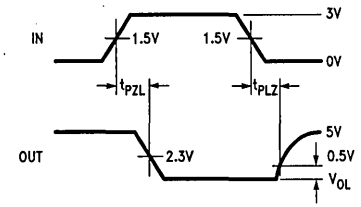

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FIGURE 7. Driver Enable and Disable Times (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)

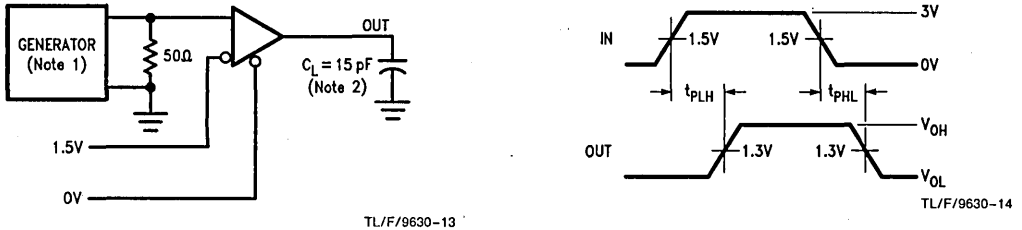
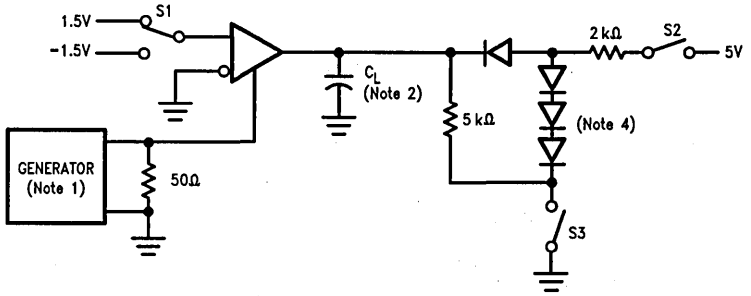


FIGURE 8. Receiver Propagation Delay Times



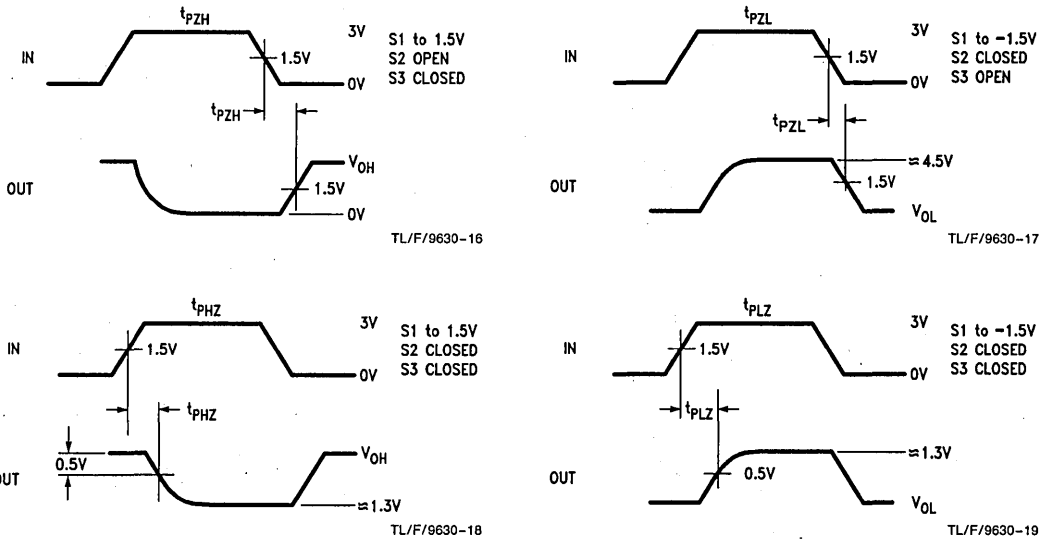


FIGURE 9. Receiver Enable and Disable Times

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96176 Driver enable is Active-High.

Note 4: All diodes are 1N916 or equivalent.

Typical Application

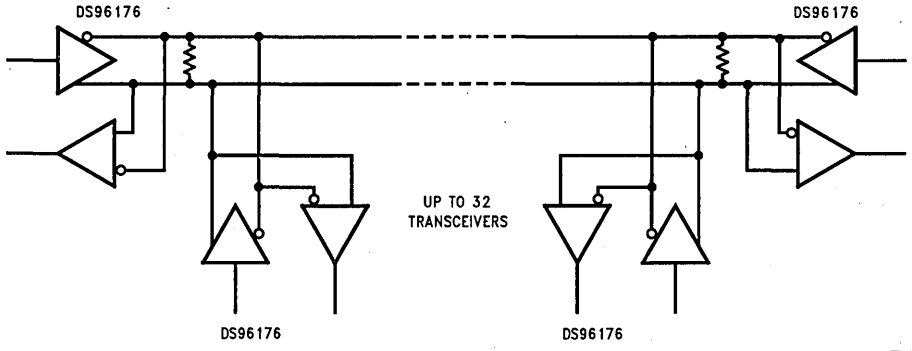


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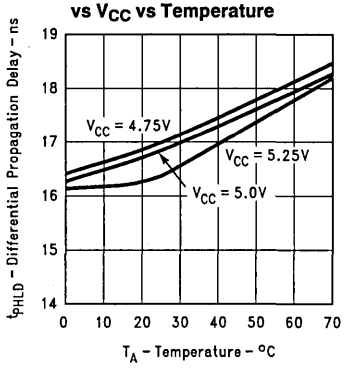
FIGURE 10

Note:

The line length should be terminated at both ends of its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

Typical Performance Characteristics

Driver Differential Propagation Delay vs V_{CC} vs Temperature



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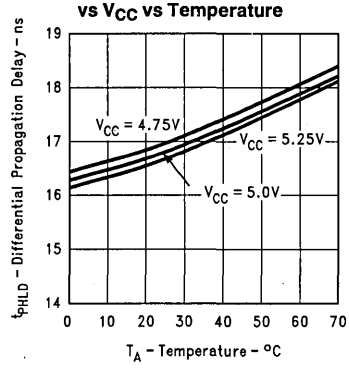
Driver Differential Propagation Delay vs V_{CC} vs Temperature



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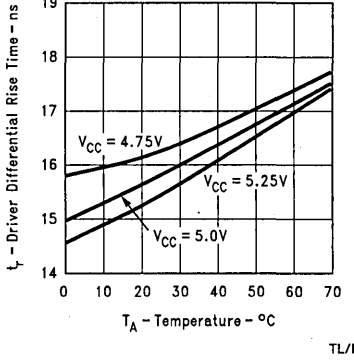
Driver Differential Rise Time vs V_{CC} vs Temperature



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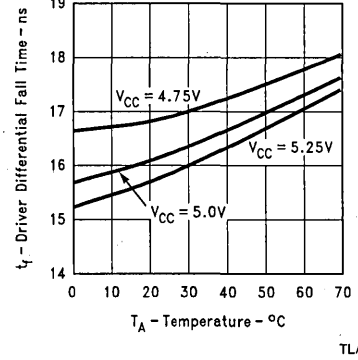
Driver Differential Fall Time vs V_{CC} vs Temperature



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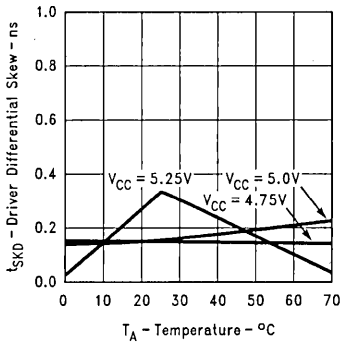
Typical Performance Characteristics (Continued)

Driver Skew vs V_{CC} vs Temperature
($|t_{PLDH}-t_{PHLD}|$)



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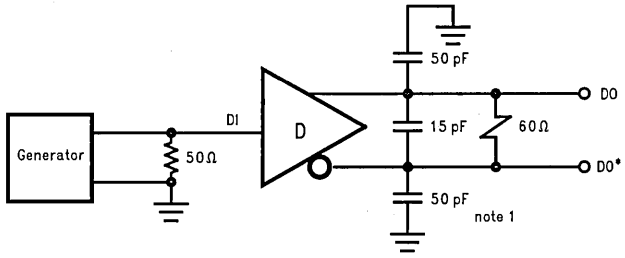

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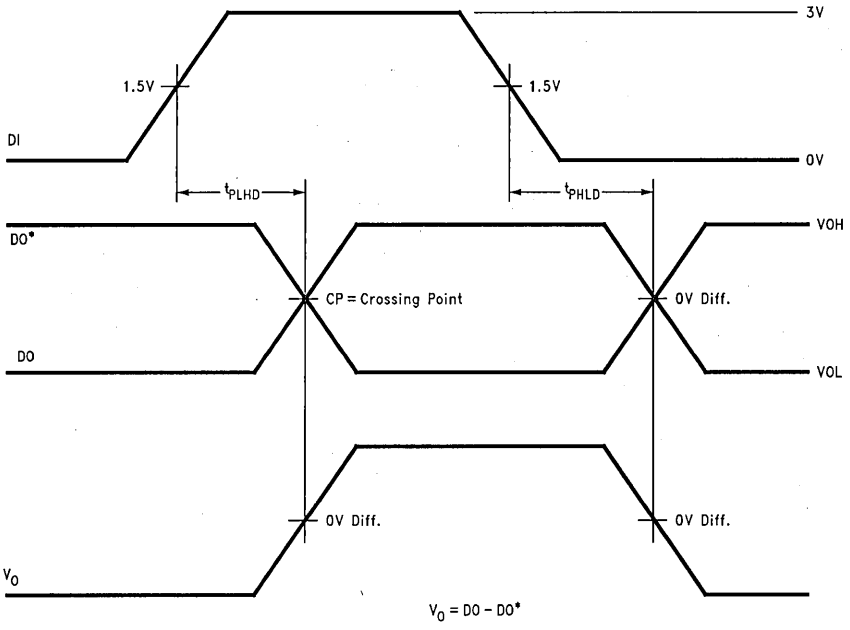
FIGURE 11. Typical Curve Driver Propagation Delay Test Circuit



TL/F/9630–28

FIGURE 12. Typical Curve Driver Differential Propagation Delay Timing

Typical Performance Curves

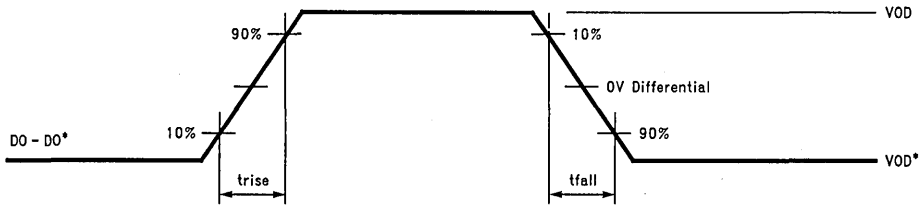


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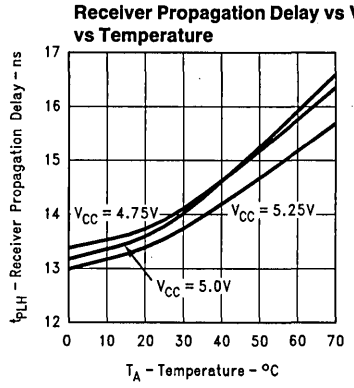
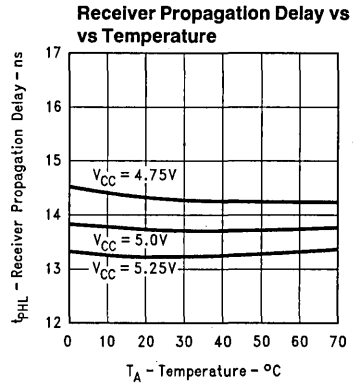
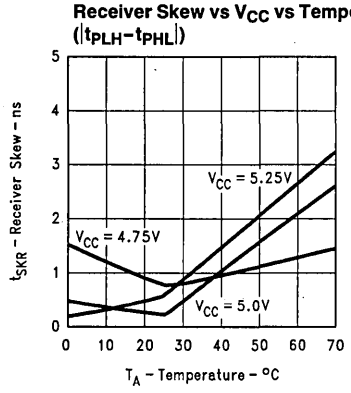
FIGURE 13. Typical Curve Driver Differential Rise and Fall Times



TL/F/9630-30



TL/F/9630-31



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Typical Performance Curves (Continued)

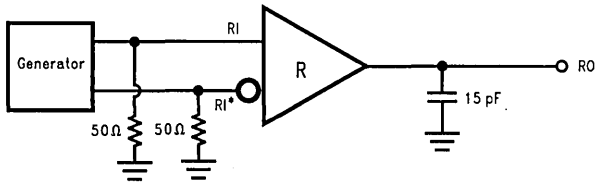

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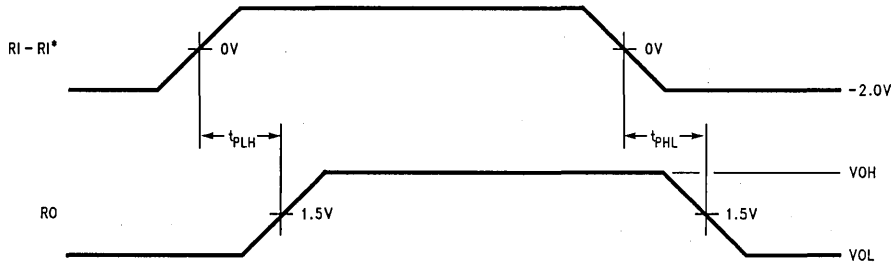
FIGURE 14. Typical Curve Receiver Differential Propagation Delay Test Circuit



TL/F/9630–34

FIGURE 15. Typical Curve Receiver Propagation Delay Timing

National Semiconductor

DS96177
RS-485/RS-422 Differential Bus Repeater

General Description

The DS96177 Differential Bus Repeater is a monolithic integrated device designed for one-way data communication on multipoint bus transmission lines. This device is designed for balanced transmission bus line applications and meets EIA Standard RS-485 and RS-422A. The device is designed to improve the performance of the data communication over long bus lines. The DS96177 has an active high Enable.

The DS96177 features positive and negative current limiting and TRI-STATE® outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12V to +12V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 160°C. The driver is designed to drive current loads up to 60 mA maximum.

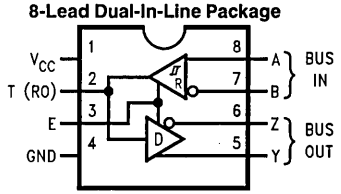
The DS96177 is designed for optimum performance when used on transmission buses employing the DS96172 and DS96174 differential line drivers, DS96173 and DS96175 differential line receivers, or DS96176 differential bus transceivers.

Features

- Meets EIA Standard RS-422A and RS-485
- Designed for multipoint transmission on long bus lines in noisy environments
- TRI-STATE outputs
- Bus voltage range −7.0V to +12V
- Positive and negative current limiting
- Driver output capability ±60 mA max
- Driver thermal shutdown protection
- Receiver input high impedance
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power requirements

Connection Diagram

8-Lead Dual-In-Line Package



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Top View

Order Number DS96177CN
See NS Package Number N08E

Function Table

Differential Inputs	Enable	Outputs		
A–B	E	T	Y	Z
$V_{ID} \geq 0.2V$	H	H	H	L
$V_{ID} \leq -0.2V$	H	L	L	H
X	L	Z	Z	Z

Note: T is an output pin only, monitoring the BUS (RO).

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP: −65°C to +150°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP (Soldering, 10 sec.): 265°C

Maximum Power Dissipation* at 25°C
- Molded Package: 930 mW

Supply Voltage: 7.0V

Input Voltage: 5.5V

*Derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Voltage at any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0		12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

DRIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, *Figure 1*		2.0	2.25		V
		R_L = 54Ω, *Figure 1* and *2*		1.5	2.0		
$\Delta\|V_{OD2}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 100Ω, *Figure 1*				±0.2	V
		R_L = 54Ω *Figure 1* and *2*	V_{CM} = 0V				
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω *Figure 1*				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to +12V				±100	μA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to +12V			±50	±200	μA
I_{IH}	Input Current HIGH	V_I = 2.7V				20	μA
I_{IL}	Input Current LOW	V_I = 0.5V				−100	μA
I_{OS}	Short Circuit Output Current (Note 9)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = 12V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

RECEIVER SECTION

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = −0.4 mA			0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = 0.5V, I_O = 8.0 mA	−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	V_{CM} = 0V		50		mV
V_{IH}	Enable Input Voltage HIGH		2.0			V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA			−1.5	V

Electrical Characteristics (Continued)

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

RECEIVER SECTION (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 3*		2.7			V
V_{OL}	Low Level Output Voltage	V_{ID} = −200 mV, *Figure 3*	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High-Impedance State Output	V_O = 0.4V				−360	μA
		V_O = 2.4V				20	
I_I	Line Input Current (Note 8)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7.0V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

Drive Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{TD}	Differential Output Transition Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 6*		25	45	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 7*		25	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 6*		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 7*		29	35	ns

Receiver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to 3.0V, C_L = 15 pF, *Figure 8*		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 9*		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 9*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS96177. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD}, V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

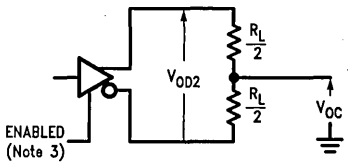
Note 6: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 8: Refer to EIA Standards RS-485 for exact conditions.

Note 9: Only one output at a time should be shorted.

Parameter Measurement Information



TL/F/9644-2

FIGURE 1. Driver V_{OD2} and V_{OC}

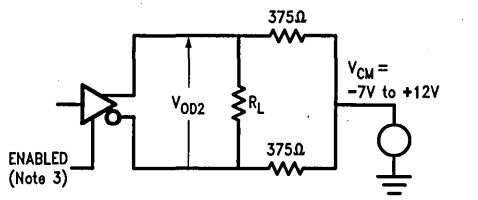


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FIGURE 2. Driver V_{OD2} with Varying Common Mode Voltage

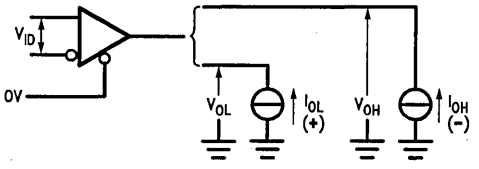

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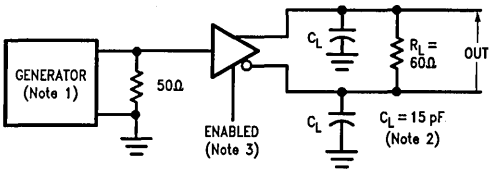
FIGURE 3. Receiver V_{OH} and V_{OL}



TL/F/9644-5

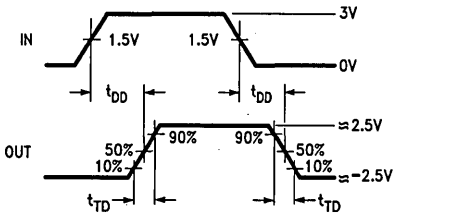


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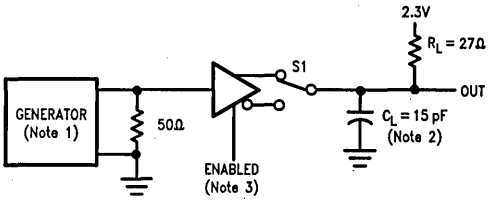
FIGURE 4. Driver Differential Output Delay and Transition Times



TL/F/9644-7

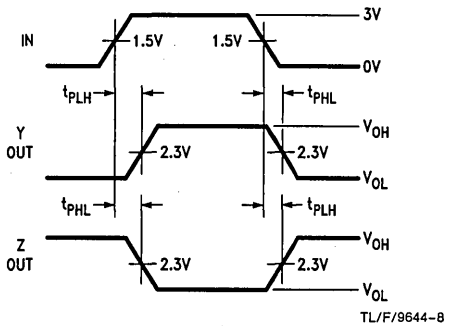


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FIGURE 5. Drive Propagation Times

Parameter Measurement Information (Continued)

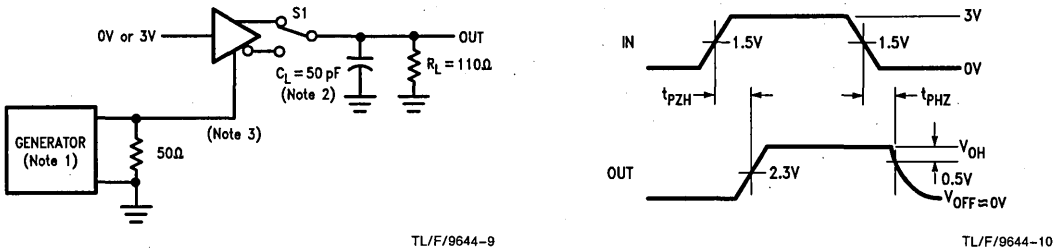

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FIGURE 6. Driver Enable and Disable Times (t_{PZH}, t_{PHZ})

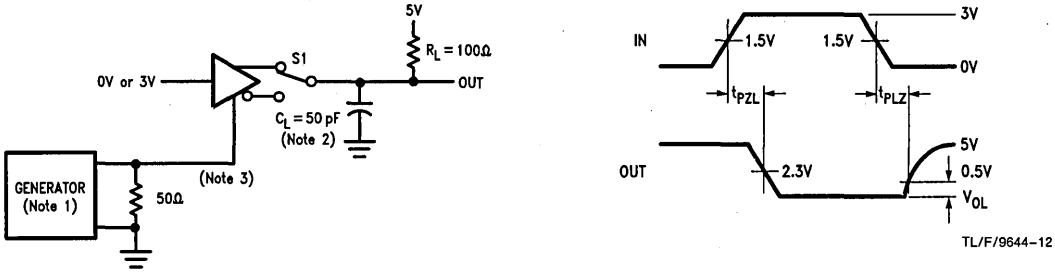

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FIGURE 7. Driver Enable and Disable Times (t_{PZL}, t_{PLZ})

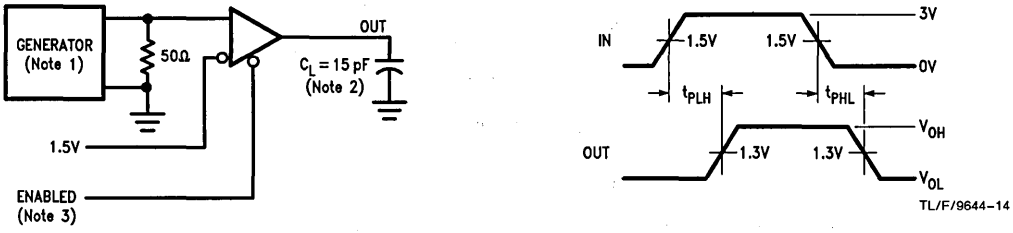

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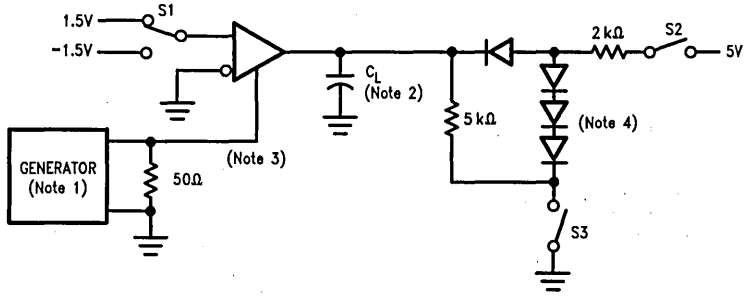
FIGURE 8. Receiver Propagation Delay Times

Parameter Measurement Information (Continued)



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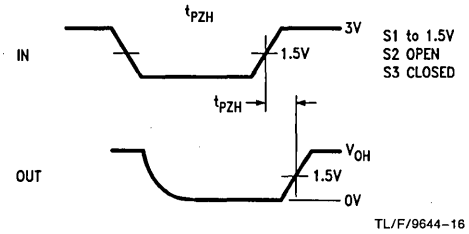

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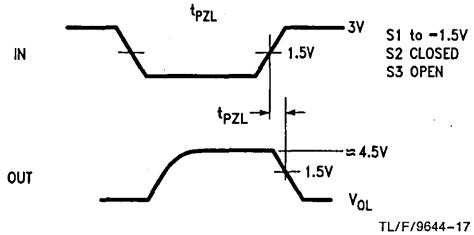

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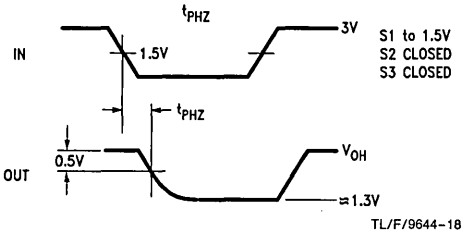

TL/F/9644–18

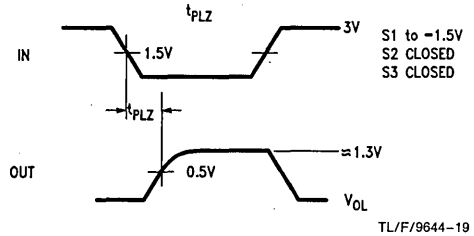

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FIGURE 9. Receiver Enable and Disable Times

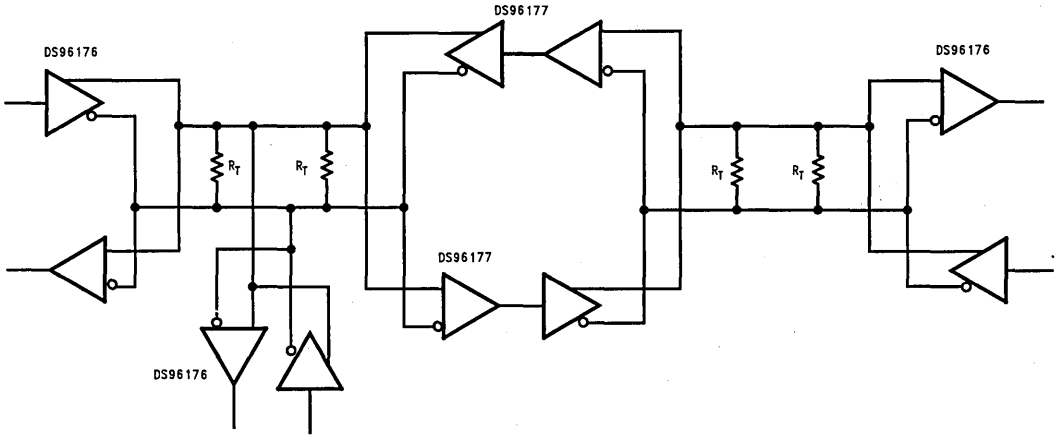
Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle ≈ 50%, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96177 Enable is active high.

Note 4: All diodes are 1N916 or equivalent.

Typical Application



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Notes:

The line length should be terminated at both ends in its characteristic impedance.

Stub lengths off the main line should be kept as short as possible.

Repeater control logic not shown

FIGURE 10

Section 4

LVDS—Low Voltage Differential Signaling

Section 4 Contents

LVDS Introduction

Low Voltage Differential Signaling (LVDS) is a new technology addressing the needs of today's high performance data transmission applications. It is designed to meet the needs of future applications since the power supply may be as low as 2V. This technology is based on the proposed IEEE 1596.3 LVDS draft standard as a basis of electrical parameters.

LVDS technology features a low voltage differential signal of 330 mV (250 mV MIN and 400 mV MAX) and fast transition times. This allows the products to address high data rates easily exceeding 300 Mbit/s for some devices such as the QR0001. Additionally, the low voltage swing minimizes power dissipation while providing all the benefits of differential transmission.

Included in this section are the following related products:

- DS90C031 LVDS Quad CMOS Differential Line Driver
- DS90C032 LVDS Quad CMOS Differential Line Receiver
- QR0001 QuickRing™ Data Stream Controller

These products, the first in a planned series, introduce LVDS technology and provide designers with new alternatives to solving high speed I/O interface problems.

National Semiconductor

ADVANCE INFORMATION

DS90C031
LVDS Quad CMOS Differential Line Driver

General Description

The DS90C031 is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 65 MHz utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C031 accepts TTL/CMOS input levels and translates them to low voltage (330 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 7.5 mW typical.

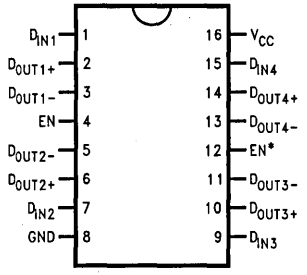
The DS90C031 and companion line receiver (DS90C032) provide a new alternative to high power psuedo-ECL devices for high speed point to point interfaces.

Features

- >65 MHz switching rates
- ±330 mV differential signaling
- Ultra low power dissipation
- 500 ps maximum differential skew
- 1.8 ns maximum chip to chip skew
- Industrial operating temperature range
- Available in surface mount packaging (SOIC)
- Pin compatible with DS26C31, MB571 and 41LG
- Compatible with IEEE P1596.3 SCI LVDS draft standard

Connection Diagram

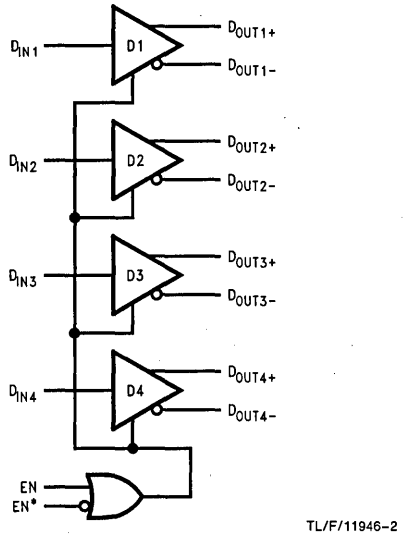
Dual-In-Line



TL/F/11946–1

Order Number
DS90C031M or DS90C031N
See NS Package Number
M16A or N16E

Functional Diagram and Truth Tables



TL/F/11946–2

DRIVER

Enables		Input	Outputs	
EN	**EN***	**D_{IN}**	**$D_{OUT}+$**	**$D_{OUT}-$**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage ($D_{OUT}+$, $D_{OUT}-$)	−0.3V to (V_{CC} + 0.3V)
Short Circuit Duration ($D_{OUT}+$, $D_{OUT}-$)	Continuous
Maximum Package Power Dissipation @ +25°C	
M Package	TBDW
N Package	TBDW
Derate M Package	TBD mW/°C above +25°C
Derate N Package	TBD mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+150°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	5.5	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (*Figure 1*)	$D_{OUT}-$, $D_{OUT}+$	250	330	400	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				TBD	25	|mV|
V_{OS}	Offset Voltage			1.125	1.2	1.275	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				TBD	25	|mV|
V_{OH}	Output Voltage High	R_L = 100Ω			1.365	1.4	V
V_{OL}	Output Voltage Low			1.0	1.035		V
V_{IH}	Input Voltage High		D_{IN}, EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_I	Input Current	V_{IN} = V_{CC}, GND, 2.5V, or 0.4V		−10		+10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5			V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V	$D_{OUT}-$, $D_{OUT}+$		TBD	6.0	mA
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V, V_{OUT} = 0V or V_{CC}		−10		+10	μA
I_{CC}	No Load Supply Current Drivers Enabled	D_{IN} = V_{CC} or GND	V_{CC}		1.5	2.5	mA
		D_{IN} = 2.5V or 0.4V			TBD	TBD	mA
I_{CCL}	Loaded Supply Current Drivers Enabled	R_L = 100Ω All Channels V_{IN} = V_{CC} or GND (all inputs)			1.47	TBD	mA
I_{CCZ}	No Load Supply Current Drivers Disabled	D_{IN} = V_{CC} or GND EN = GND, EN* = V_{CC}			TBD	TBD	mA

Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$, $C_L = 5$ pF (*Figures 2* and *3*)	0.6	1.3	2.4	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.6	1.3	2.4	ns
t_{SKD} $\lvert t_{PHLD} - t_{PLHD} \rvert$	Differential Skew		0	100	500	ps
t_{SK1}	Channel to Channel Skew			TBD	TBD	ns
t_{SK2}	Chip to Chip Skew	Note 4		TBD	1.8	ns
t_{TLH}	Rise Time	$R_L = 100\Omega$, $C_L = 5$ pF (*Figures 2* and *3*)	0.7	1.2	1.5	ns
t_{THL}	Fall Time		0.7	1.2	1.5	ns
t_{PHZ}	Disable Time High to Z			5	10	ns
t_{PLZ}	Disable Time Low to Z			5	10	ns
t_{PZH}	Enable Time Z to High			5	10	ns
t_{PZL}	Enable Time Z to Low			5	10	ns

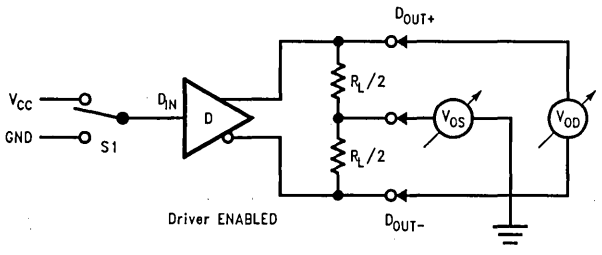
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.

Note 3: All typicals are given for: $V_{CC} = +5.0$V, $T_A = +25$°C.

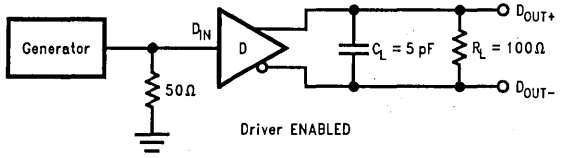
Note 4: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Parameter Measurement Information



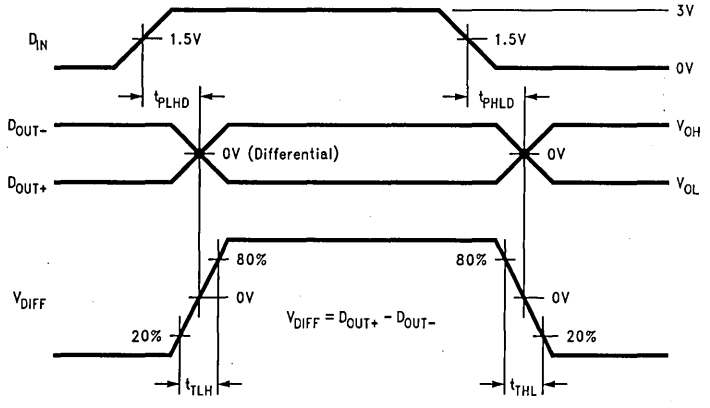
TL/F/11946-3

FIGURE 1. Driver V_{OD} and V_{OS} Test Circuit



TL/F/11946-4

FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit



TL/F/11946-5

FIGURE 3. Driver Propagation Delay and Transition Time Waveforms

National Semiconductor

ADVANCE INFORMATION

DS90C032
LVDS Quad CMOS Differential Line Receiver

General Description

The DS90C032 is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 65 MHz utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C032 accepts low voltage (330 mV) differential input signals and translates them to CMOS (TTL compatible) output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs.

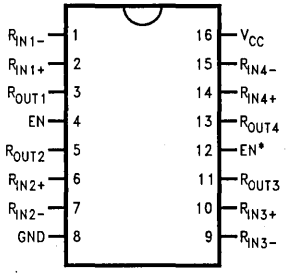
The DS90C032 and companion line driver (DS90C031) provide a new alternative to high power psuedo-ECL devices for high speed point to point interfaces.

Features

- >65 MHz Switching Rates
- Accepts small swing (330 mV) differential signal levels
- Ultra Low Power Dissipation
- 500 ps Maximum Differential Skew
- 3.5 ns Maximum Chip to Chip Skew
- Industrial Operating Temperature Range
- Available in Surface Mount Packaging (SOIC)
- Pin Compatible with DS26C32A, MB570 and 41LF
- Compatible with IEEE P1596.3 SCI LVDS draft standard

Connection Diagram

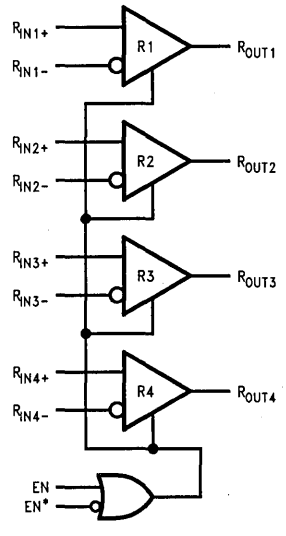
Dual-In-Line



TL/F/11945–1

Order Number
DS90C032M or DS90C032N
See NS Package Number
M16A or N16E

Functional Diagram and Truth Tables



TL/F/11945–2

RECEIVER

ENABLES		INPUTS	OUTPUT
EN	**EN***	**$R_{IN+} - R_{IN-}$**	**R_{OUT}**
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (RIN+, RIN−)	−0.3V to (V_{CC} +0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} +0.3V)
Output Voltage (ROUT)	−0.3V to (V_{CC} +0.3V)
Short Circuit Duration (ROUT)	continuous
Maximum Package Power Dissipation @ +25°C	
M Package	TBDW
N Package	TBDW
Derate M Package	TBD mW/°C above +25°C
Derate N Package	TBD mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+150°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	5.5	V
Receiver Input Voltage	GND		2.4	V
Operating Free Air Temperature (T_A)	−40	25	+85	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V		RIN+, RIN−		+TBD	+100	mV
V_{TL}	Differential Input Low Threshold				−100	−TBD		mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			TBD	±10	μA
		V_{IN} = 0V				TBD	±10	μA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		ROUT	3.8	TBD		V
		I_{OH} = −0.4 mA, Input terminated			3.8	TBD		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				TBD	0.3	V
I_{OS}	Output Short Circuit Current	Enabled, V_{OUT} = 0V			TBD	TBD	TBD	mA
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} = 0V or V_{CC}				TBD	±10	μA
V_{IH}	Input High Voltage			EN, EN*	2.0			V
V_{IL}	Input Low Voltage						0.8	V
I_I	Input Current						±10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA					−1.5	V
I_{CC}	No Load Supply Current	EN, EN* = V_{CC} or GND, Inputs Open		V_{CC}		10	15	mA
	Receivers Enabled	EN, EN* = 2.4 or 0.5, Inputs Open				12	17	mA
I_{CCZ}	No Load Supply Current Receivers Disabled	EN = GND, EN* = V_{CC} Inputs Open				TBD	TBD	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF, V_{ID} = 200 mV	1.5	3	5	ns
t_{PLHD}	Differential Propagation Delay Low to High	*Figures 1, 2* (Note 4)	1.5	3	5	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$		0	100	500	ps
t_{SK1}	Channel to Channel Skew			TBD	TBD	ns
t_{SK2}	Chip to Chip Skew	(Note 5)		TBD	3.5	ns
t_{TLH}	Rise Time	*Figures 1, 2*		1.6	2.5	ns
t_{THL}	Fall Time			1.6	2.5	ns
t_{PHZ}	Disable Time High to Z			TBD	TBD	ns
t_{PLZ}	Disable Time Low to Z			TBD	TBD	ns
t_{PZH}	Enable Time Z to High			TBD	TBD	ns
t_{PZL}	Enable Time Z to Low			TBD	TBD	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

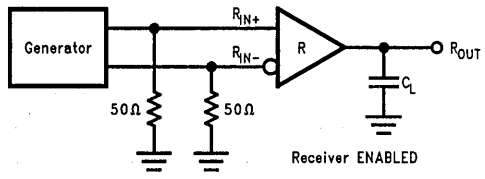
Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.

Note 4: AC input test waveforms for test purposes: $t_r = t_f$ = 1 ns (0-100%), V_{ID} = 200 mV.

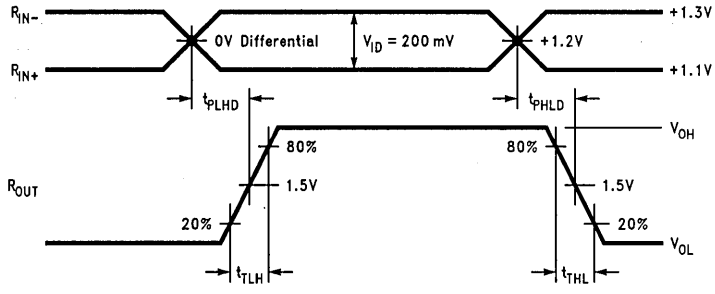
Note 5: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Parameter Measurement Information



TL/F/11945–3

FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit



TL/F/11945–4

FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms

National Semiconductor

ADVANCE INFORMATION

QR0001
QuickRing™ Data Stream Controller

General Description

QuickRing is a point-to-point data transfer architecture designed to facilitate high speed data streams. The QuickRing architecture can be applied both inside the chassis as well as outside the chassis environments to increase data throughput. Each QR0001 QuickRing Controller node in the ring is capable of streaming 350 MSamples/s per signal line simultaneously, including protocol overhead. This device is intended for use in applications that handle high-bandwidth data streams associated with graphics, uncompressed video, disk arrays, high-speed local area networks, multiprocessor systems, and to interconnect peripherals over a few meters of cable. The QR0001 QuickRing Controller can be used to augment the performance of traditional backplane buses in personal computers, workstations, and high-end systems. The QR0001 is useful for routing high-bandwidth streams in systems that are larger or topologically more complex than bus-based systems.

Features

- 160-pin PQFP package
- 16 node single ring capability
- Peak theoretical rate of 1.7 GBytes/sec for 16 node ring
- Support for Multi-Ring topologies
- Supports Separate Ring and Client Clock Rates
- Error detection detects 1- and 2-bit errors
- 2^{20} separate stream IDs possible

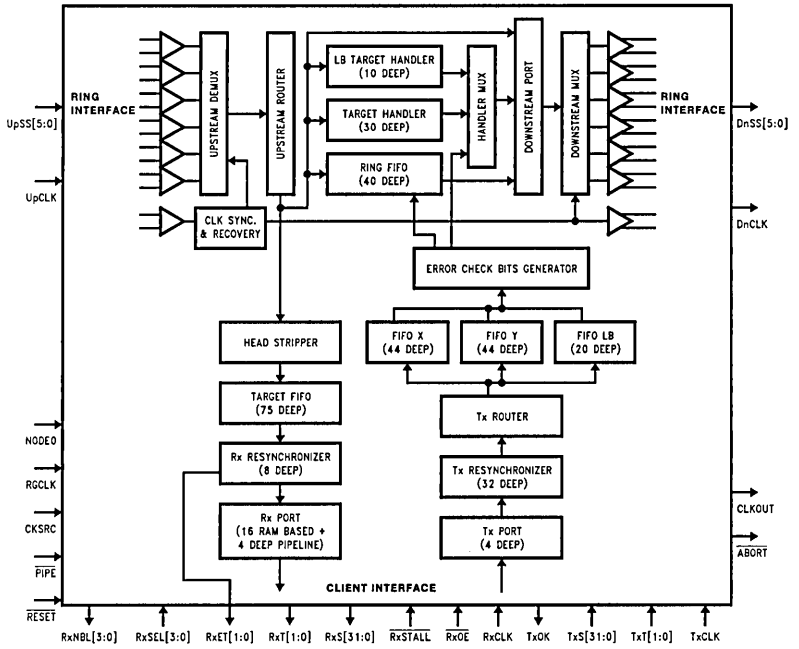
RING INTERFACE

- Precision PLL captures data at 350 MSamples/s
- 50 MHz maximum ring clock frequency
- Low Voltage Differential Signaling (LVDS) ring interface

CLIENT INTERFACE

- 200 MBytes/s data transfer rate at both Tx and Rx ports
- 32-bit transmit and receive data ports
- Readable internal diagnostic register
- TTL signal interface

Block Diagram



TL/F/11928–1

Section 5

Special Interface

Super I/O
PC I/O Communications

Section 5 Contents

NOTE: Super I/O and PC I/O Communications complete datasheets are available from the Customer Support Center at 1-800-272-9959 or your local National Sales Office or distributor.

National Semiconductor

PRELIMINARY

DS36001
SLIO1 Serial Link Input Output Device

General Description

The DS36001 SLIO1 is designed to conform to the ISO CAN protocol. The Controller Area Network (CAN) is a serial communication protocol that supports distributed real-time control and is specially designed to provide efficient data communication between automotive electronic subsystems.

The SLIO1 implements an 8-bit Serial Linked I/O port for a remote microcontroller with the link being provided by the CAN network. The device features capabilities of a microcontroller including, the ability to generate an interrupt for the master when one of it's I/O pins changes state.

The DS36001 is designed to allow the implementation of very low cost nodes. The port has been defined so as to cover the widest possible application range. To reduce the overall system cost, an on-board oscillator has been developed which requires no external components.

The use of the CAN bus and SLIO1 nodes represents a very cost effective way of increasing the I/O capability of a microcontroller and reducing the amount of wiring which is required to connect all peripherals to the microcontroller.

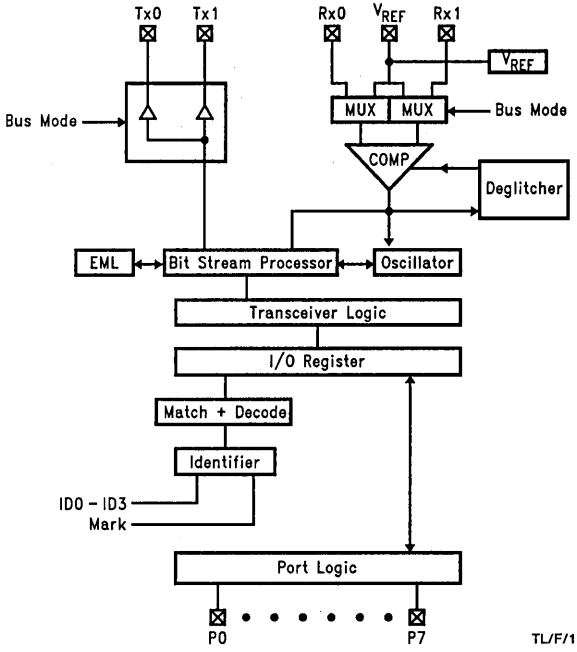
Features

- Supports CAN (Controller Area Network) specification 2.0 B.
- Provides variable port configuration
- Calibration of on-board oscillator is done internally (without external components)
- Operates from 20 Kbits/s to 125 Kbits/s
- On-chip error detection logic to provide automatic diagnostic
- Built-in reference voltage of 2.5V (one half of the power supply)
- Capable of operating in a single wire bus configuration. This feature guarantees safe operation even when one of the two wires is damaged
- Provides individual Enable/Disable for each port

Applications

- Automotive
  — Body electronics and instrumentation
- Industrial applications
  — Sensor/actuators interface
- Microprocessor-based System Designs
  — Extension of I/O capabilities of microprocessors

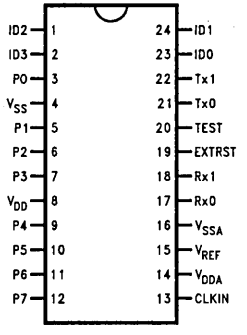
Logic Diagram



TL/F/11931–1

FIGURE 1

Connection Diagram



TL/F/11931–2

FIGURE 2. DS36001
Order Number DS36001TM
See NS Package Number M24B
Order Number DS36001TN
See NS Package Number N24D

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Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.5V
Input Voltage (Any Input)	V_{CC} + 0.5V to GND − 0.5V
D.C. Output Current for I/O Port Pins	±5 mA
D.C. Output Current for All Other Pins	±25 mA
Power Dissipation at 25°C	200 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage V_{CC}	4.8	5.2V	V
Input Voltage (Any pin)	−0.3	V_{CC} + 0.5	V
Operating Temperature (free air)	−40°	+125°	C

DC Electrical Characteristics T_A = −40°C to +125°C, V_{CC} = 5V ± 4% (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
INPUT COMPARATOR (Rx0 and Rx1)						
V_{IH}	Minimum Input High Voltage		V_{CC} − 1.5			V
V_{IL}	Maximum Input Low Voltage				1.5	V
V_{diff} (Dom)	Differential Voltage (Dominant)	(Note 4)			−25	mV
V_{diff} (Rec)	Differential Voltage (Recessive)	(Note 4)	+25			mV
OUTPUT DRIVERS (Tx0 and Tx1)						
V_{OL}	Output Voltage Low	I_{OL} = 1.5 mA @ Tx0			0.1	V
V_{OH}	Output Voltage High	I_{OH} = −1.5 mA @ Tx1	V_{CC} − 0.1			V
CONTROL SIGNALS (EXTRST, TEST, CLKIN)						
V_{IL}	Input Low Voltage				1.5	V
V_{IH}	Input High Voltage		3.5			V
DIGITAL PARALLEL PORT (P0–P7), Ext Clk						
V_{OL}	Output Low Voltage	Sink Current = 4.0 mA			1.0	V
V_{OH}	Output High Voltage	Source Current = −4.0 mA	V_{CC} − 0.1			V
V_{IL}	Input Low Voltage				1.5	V
V_{IH}	Input High Voltage		3.5			V
I_{IH}	Input High Current	V_{IN} = V_{CC} or GND	−10		+10	μA
I_{IL}	Input Low Current	V_{IN} = V_{CC} or GND	−10		+10	μA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −12 mA	−1.5			V
I_{CC}	Supply Current			26		mA
I_{SL}	Sleep Current				500	μA
V_{REF}	Reference Voltage	I_{OUT} ≥ −75 μA	(V_{CC}/2) − 0.12		(V_{CC}/2) + 0.12	V

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All input and/or output pins shall not exceed V_{CC} plus 0.5V and shall not exceed the absolute maximum rating at anytime, including power-up and power-down.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified. All typical values are specified under these conditions: V_{CC} = 5V and T_A = 25°C, unless otherwise stated.

Note 4: V_{diff} = Rx0–Rx1.

AC Electrical Characteristics $T_A = -40°C$ to $+125°C$, $V_{CC} = 5V \pm 4\%$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_d Total	Total Delay of the Input Comparator and Output Driver	$1.5V < (V_{Rx0} + V_{Rx1}) < V_{CC} - 1.5V$			200	ns
t_{CLK}	Clock Period	CLKIN = Ext Clock	100		250	ns
CAN Propagation Time						
t_{total}	$t_{setup} + t_{CLK}$ to Output Tx0	(See Waveform in *Figure 3*)			200	ns

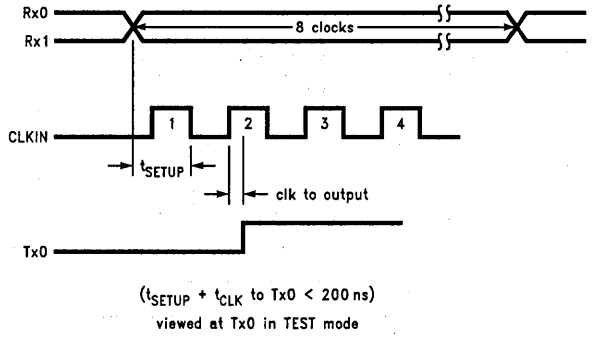

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FIGURE 3. Waveforms in TEST Mode

Pin Description (Note 5)

TABLE I. Pin Description

Pin Name	Number of Pins	Input/Output	Description
Clkin	1	I	External Clock
ExtRst	1	I	Reset and Decode Control
ID0–ID3	4	I	Identifiers
P0–P7	8	I/O	Port Receiver Input and Driver Output
Rx0–Rx1	2	I	Bus Driver Inputs
Tx0–Tx1	2	O	Bus Driver Outputs
TEST	1	I	Decode Control
V_{ref}	1	O	Reference Voltage
V_{DD}	1		Digital Power Supply
V_{DDA}	1		Analog Power Supply
V_{SS}	1		Digital Ground
V_{SSA}	1		Analog Ground

Note 5: The above listed functions of the pins are only valid for the normal mode of operation. The normal mode of operation is achieved by placing low on the TEST and ExtRst pins. (See information on the testing below.)

1.0 Introduction

The SLIO1 contains the following circuit blocks.

Bit Stream Processor (BSP)
Oscillator
Cyclic Redundancy Check Register (CRC Register)
Transmit/Receive Shift register (Tx/Rx Shift Register)
Match & Decode Logic
Identifier Logic
Port Logic
Error Management Logic (EML)

1.1 BIT STREAM PROCESSOR

The Bit Stream Processor (BSP) is a sequencer controlling the data stream between the Tx/Rx Shift Register, CRC Register, Identifier, Port Logic, and the bus line. The BSP also controls the Error Management Logic (EML) and the oscillator such that functions such as: reception, arbitration, transmission, and error signalling are performed according to the CAN protocol and the correct calibration of the oscillator's pre-scaler is maintained. Note that the automatic retransmission of messages which have been corrupted by noise or other external error conditions on the bus line is handled by the BSP.

1.2 OSCILLATOR

The clock is generated from the on-board oscillator which is calibrated using the calibration message received via CAN bus. These calibration messages are sent by those nodes which contain quartz controlled clocks. The circuit for calibrating the on-board oscillator is implemented in the DS36001; therefore, a frequency variation of 500% can be tolerated by the system. In order to maintain the clock synchronization by the SLIO1 nodes, a calibration message must be sent regularly. As a consequence of the internal clock generation, the bus speed range of such a SLIO1 node is limited between 20 kbits/s to 125 kbits/s.

1.3 REGISTERS AND COUNTERS

1.3.1 Cyclic Redundancy Check Register

This register generates the Cyclic Redundancy Check (CRC) code which is transmitted after the data bytes and checks the CRC code of incoming messages. This is done by dividing the data stream by the code generator polynomial.

1.3.2 Transmit/Receive Shift Register

This Tx/Rx Shift Register holds the destuffed bit stream from the bus line to allow the parallel access to the Identifier for the acceptance match test and, afterwards, the parallel transfer of the two data bytes to the port logic.

1.3.3 Identifier Register

During Reset, the programmabie four bits of the identifier are stored into this register as defined by the pull-up or pull-down resistors on the pins **ID0–ID3**. The other identifier bits are fixed and can oniy be changed by making a new rnask for the chip. The last bit of the identifier is generated by the BSP, depending on the direction of the message.

1.3.4 Error Counters

In each CAN module there are two error counters to perform a sophisticated error management. The Receive Error Count (REC) is 7-bits wide and switches the device to the error passive state if it overflows. The Transmit Error Count (TEC) is 8-bits wide. If it is greater then 127 the device is also switched to the error passive state. As soon as the TEC overflows the device is switched bus-off, i.e., it does not participate in any bus activity.

The following errors can be detected and lead to an increase by eight of either the Receive or Transmit Error Count in every module detecting.

- Bit Error — the transmitted bit is not the received one
- Stuff Rule — there is no stuff bit where it is supposed to be
- Frame check — a fixed frame bit does not have the specified value
- Bit CRC check — the calculated CRC does not match the received one
- ACK check — a transmitting node does not get any acknowledgment

1.4 PORT LOGIC

This block contains logic which enables the programming of the port functions. It interprets data received from the Tx/Rx Shift Register and loads data to be transmitted into this register.

1.5 ERROR MANAGEMENT LOGIC

The Error Management Logic (EML) is responsible for the fault confinement of the CAN device. All messages are received, checked and acknowledged by any node in the network. Even messages which are filtered by the acceptance filter are checked for errors. If any node detects an error it starts transmitting an error frame.

There are two error counters, one for the transmitted data and one for the received data, which are incremented as soon as an error occurs. If either counter goes beyond a specific value the node goes to an error state. A valid frame causes the error counters to decrease.

2.0 DS36001 Functional Description

2.1 BUS MODES

The comparator monitors levels of the Rx0 and Rx1 input pins. The output of the comparator is "1" if the voltage levels of the CAN bus lines are regarded as recessive and it is "0", if they are regarded as dominant.

There are three possibilities to generate the output signal of the comparator. In normal operation, the CAN bus is configured of two wires, and the Rx0 and Rx1 levels are compared against each other. If one of the two wires is damaged, the SLIO1 can still operate in a single wire CAN bus configuration. In this case, the level of one single wire is compared against the on-board generated reference voltage V_{REF}. Additionally, if only the Rx0 input is regarded the Tx1 output is turned off, to take into account the possibility of a short circuit between the two CAN bus lines. When enabled, the SLIO1 can exist in the following four bus configurations.

2.0 DS36001 Functional Description (Continued)

TABLE II. Comparator Input Configuration

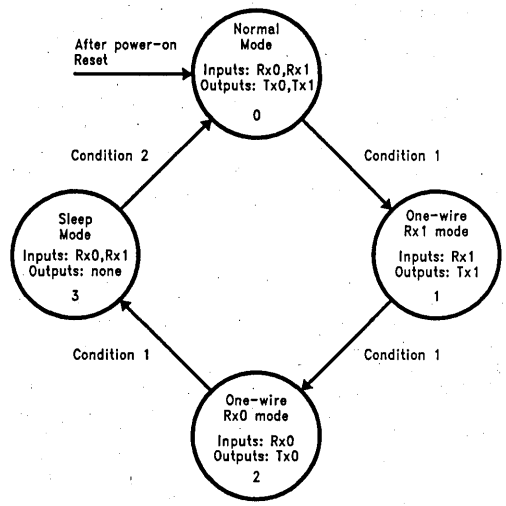
	Bus Mode	Mode Bits	Recessive	Dominant	Comment
0	Differential	00	Rx0 > Rx1	Rx0 < Rx1	Differential Communication
1	One-Wire Rx1	01	Rx1 < V_{REF}	Rx1 > V_{REF}	Communication on Tx1/Rx1
2	One-Wire Rx0	10	Rx0 > V_{REF}	Rx0 < V_{REF}	Communication on Tx0/Rx0
3	Sleep	11	Rx0 > V_{REF} and Rx1 < V_{REF}	*Rx0 < V_{REF} *Rx1 > V_{REF}	Low Current Mode

*Wake up condition.

When the external reset is performed, the normal mode is active and the SLIO1 waits for a suitable calibration message. If it does not receive such message within adequate time, it switches to the next mode in the numerical order. If it reaches sleep mode, all activities are stopped until the next dominant bit is monitored on the bus.

After the hardware reset, the SLIO1 will be always in the bus mode 0. There are three conditions to switch to the next bus mode, an overflow of the bit counter (8 Kbits since the last calibration message or since reset), or the Receive or Transmit Error Counters reach the error passive limit of 128. By switching to the next bus mode, the SLIO1 is internally reset and waits for the next calibration message before starting the CAN protocol bus off recovery sequence and going on bus again. The SLIO1 switches the bus modes from the bus mode 0 to mode 1 to mode 2. The SLIO1 can switch to the sleep mode only from the bus mode 2. The SLIO1 will leave this sleep mode upon detecting a dominant bit on either of the two bus lines.

The following state diagram shows the switch-over conditions for the possible four CAN-bus modes.



Condition 1: bit counter overflow (>8191) or error counter overflow (>255).
Condition 2: Dominant bit detected on Rx0 or Rx1

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FIGURE 4. CAN-bus Modes and Switch-Over Conditions

TABLE III. CAN Bus Modes

	Bus Mode	Mode Bits	Reception			Transmission	
			Diff	Rx1	Rx0	Tx1	Tx0
0	Differential	00	x			x	x
1	One-wire Rx1	01		x		x	
2	One-wire Rx0	10			x		x
3	Sleep	11		x	x		

Diff: differential input voltage on Rx0 and Rx1 (recessive Rx0 > Rx1)
Rx1: input voltage on Rx1 compared to V_{REF} (recessive Rx1 < V_{REF})
Rx0: input voltage on Rx0 compared to V_{REF} (recessive Rx0 < V_{REF})

2.0 DS36001 Functional Description (Continued)

The Tx1 output is disabled in bus mode 2 to tolerate the short-circuit between the CAN bus wires CAN_H and CAN_L.

The Deglitcher is an active filter which is realized by inhibiting the comparator output for 8 clock cycles after performing a signal change at the comparator output. A glitch at the comparator input will simply be ignored because, in order for a glitch to cause a change in the signal level at the comparator output, it should last for at least 8 clock cycles. The deglitcher will increase the system reliability.

2.2 OSCILLATOR AND CALIBRATOR

The on-board oscillator is an RC type oscillator. This oscillator is calibrated to the exact frequency required by examining messages coming over the CAN bus. On power-up, a calibration must be sent on the bus to calibrate the oscillator. Once the oscillator is well calibrated to correctly receive messages, the calibration logic will then only calibrate itself to nodes which send a particular calibration message, labeled by a special Identifier. The calibration message must be sent periodically (typically 20 ms) or the device will stop responding. This calibration message may be sent only by the quartz controlled nodes. Only when the SLIO1 is correctly synchronized to a quartz node, will it allow itself to write a dominant level onto the bus. The Identifier of this calibration message is defined by hardware and can only be changed by modifying one mask of the chip.

If the SLIO1 does not receive a suitable message for calibration of its oscillator within 8 Kbit times after the last suitable message or after waking up, it will switch to the next bus mode. After trying both one wire bus modes without success it will enter the sleep mode. During this mode, the total power consumption is reduced to less than 500 μA. Any extemal bus activity (either bus wire in the dominant state) will cause the device to wake up, whereupon it will reinitialize itself and calibrate its oscillator. On wakeup the bus mode is reset to normal two wire differential operation (bus mode 0). Note that on switching bus modes or entering sleep mode, the device is effectively reset to its power-up state, resetting also the port registers. The SLIO1 broadcasts this reset by sending a special message after the successful calibration.

As distinct from other CAN nodes, the SLIO1 CAN node is not able to wake up by local events or to wake up other nodes, because the SLIO1 CAN node cannot start transmission if its oscillator is not calibrated. Therefore, to keep the network alive, a quartz node should send the calibration message regularly with a repeating period less (to take into account the possibility of bus errors) than the maximum distance of 8 kbit/Baud-Rate.

Note: The calibration of the oscillator requires at least three consecutive messages, the second and third of them error free, if the node was in sleep mode. Therefore, it is possible for the quartz controlled node to go error-passive before it gets an acknowledge to its wake-up message.

Requirements for messages which are used for calibration are:

The message must come from a quartz controlled node and have the Identifier: 000 1010 1010.

In the message, the first recessive to dominant transition after the Control Field must be followed by another recessive to dominant transition in a distance of exactly 32 bit times, including stuff bits.

One suitable message is (there are many others, using different data bytes)

Identifier = 000 1010 1010

DLC = 0010

Data (2 bytes Data Field) = 10101010 00000100

Bus bit stream = 0 000 1010 1010 0 00 0|010 10101010 0000|0100

000|01011100000|0 ("|" signifies a recessive stuff bit)

In this example, the first recessive to dominant transition after the Arbitration Field is in the first data byte, from the first to the second bit. The bit number 32, after the first bit of the first data byte is (there are three stuff bits in the Data and CRC Fields) the last but one bit of the CRC Field. This last but one bit is recessive ("|") and is followed by a dominant ("0") bit. The total length of this message (from the Start of the Frame to the end of Intermission) is 67 bits.

2.3 ERROR MANAGEMENT LOGIC

2.3.1 Error States

With respect to fault confinement a unit may be in one of the following three states:

- error active
  A node is "error active" once it detects an error but has not yet become "error passive".
- error passive
  A node is "error passive" when the Transmit Error Count equals or exceeds 128, or when the "Receive Error Count" equals or exceeds 128. An error condition letting a node become "error passive" causes the node to send an Passive Error Flag.
- bus off
  A node is "bus off" when the Transmit Error Count is greater than or equal to 256.

An "error active" unit can normally take part in bus communication and send an Active Error Flag when an error has been detected.

An "error passive" unit must not send an Active Error Flag. It takes part in bus communication, but when an error is detected only Passive Error Flag is sent. Also, after the transmission, an "error passive" unit will wait before initiating a further transmission.

A "bus off" unit is not allowed to have any influence on the bus, (e.g., output drivers switched off.)

Special error handling is performed at following situations:

A stuff error occurs during arbitration when a transmitted recessive stuff bit is received as a dominant bit. This does not lead to an incrementation of the TEC.

An ACK error occurs in an error passive device and no dominant bits are detected in the passive error flag. This does not lead to an incrementation of the TEC.

A valid reception or transmission leads to a decrementation of the error counters by one. *Figure 5* shows the connection of different error states according to the error counters.

2.0 DS36001 Functional Description (Continued)

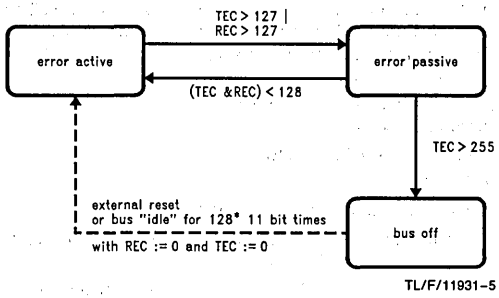

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FIGURE 5. CAN Bus States

2.3.2 Rules and Exceptions

There are two error counters implemented in this device for the error detection.

Transmit Error Count

Receive Error Count

These counters are modified according to the following rules:

1. When a receiver detects an error, the Receive Error Count will be increased by 1, except when the detected error was a Bit error during the sending of an Active Error Flag.
2. When a receiver detects a "dominant" bit as the first bit after sending an error flag the Receive Error Count will be increased by 8.
3. When a transmitter sends an Error Flag the Transmit Error Count is increased by 8.

Exception 1:

If the transmitter is "error passive", and it detects an Acknowledgment Error because of not detecting a "dominant" ACK and does not detect a "dominant" bit while sending its Passive Error Flag.

Exception 2:

If the transmitter sends an Error Flag because a stuff error occurred during arbitration whereby the stuff bit is located before the RTR bit, and should have been "recessive" and has been sent as "recessive" but monitored as "dominant".

In both exceptions, the Transmit Error Count is not changed.

If a transmitter detects a bit error while sending an Active Error Flag or an Overload Flag the Transmit Error Count is increased by 8.

If a receiver detects a bit error while sending an Active Error Flag or an Overload Flag the Receive Error Count is increased by 8.

Any node tolerates up to 7 consecutive "dominant" bits after sending an Active Error Flag, Passive Error Flag or Overload Flag. After detecting the 14th consecutive "dominant" bit (in case of an Active Error Flag or an Overload Flag) or after detecting the 8th consecutive "dominant" bit following a Passive Error Flag, and after each sequence of additional eight consecutive "dominant" bits every transmitter increases its Transmit Error Count by 8 and every receiver increases its Receive Error Count by 8.

After the successful transmission of a message (getting ACK and no error until the End of Frame is finished) the Transmit Error Count is decreased by 1 unless it was already 0.

After the successful reception of a message (reception without error up to the ACK SLOT and the successful sending of the ACK bit), the Receive Error Count is decreased by 1, if it was between 1 and 127, if the Receive Error Count was 0, it stays 0, and if it was greater than 127, then it will be set to a value between 119 and 127.

An "error passive" node becomes "error active" again when both the Transmit Error Count and the Receive Error Count are less than or equal to 127.

A node which is "bus off" is permitted to become "error active" (no longer "bus off") when both its error counters are set to 0 after 128 occurrences of 11 consecutive "recessive" bits have been monitored on the bus.

Note: If during system start-up only 1 node is on-line, and if this node transmits some message, it will get no acknowledgment, detect an error and repeat the message. It can become "error passive" but not "bus off" due to this condition.

2.4 PORT FUNCTIONS

The port functions are controlled by various registers. Each writeable register may be written by sending a Data Frame with a two byte long Data Field where the lower part of the first byte is the Register Marker for the addressed register and the remaining byte is the information which will be written to the register. The first part of the first byte is reserved.

2.4.1 SLIO1 Status Information and Register Marker

The first byte of each message transmitted by a SLIO1, contains status information and the Register Marker to describe the contents of the following byte.

7	6	5	4	3	2	1	0
Rstd	EW	Bus Mode		0	Register Marker		

Four parts of the status information are available:

Rstd (Bit 7) This bit is set in the first message after the SLIO1 has been reset.

Rstd = 1: SLIO1 has just entered the state where oscillator is calibrated.

Rstd = 0: Other data frame

EW (Bit 6) This bit is set if the Receive Error Count or the Transmit Error Count has exceeded, at least temporarily, the Error Warning limit (32) since the last successful transmission of a message.

EW = 1: error warning limit (32) reached.

EW = 0: error warning limit not reached.

Bus Mode (Bits 5,4) Valid values for the Bus Mode are [0, 1 and 2]

00: Mode 0 (two-wire mode)

01: Mode 1 (one-wire mode, Tx0 disconnected)

10: Mode 2 (one-wire mode, Tx1 disconnected)

Reserved (Bit 3) Reserved and transmitted as "0".

2.0 DS36001 Functional Description (Continued)

Register Marker (Bits 2,1,0) — Register marker bits are used to select the I/O register (Register Markers are shown below).

Marker	Abbr.	Function
0	P	Input Data (Port) Register (read only)
1	PE	Positive Edge Register (write only)
2	NE	Negative Edge Register (write only)
3	OD	Output Data Register (write only)
4	DD	Data Direction Register (write only)
5–7		reserved

These registers can be cleared by activating the ExtRst pin, or when entering the sleep mode. On wake up, or after reset, after the oscillator is calibrated, the SLIO1 will transmit the contents of the Input Data Register (all port pins input), with the Rstd bit in the status byte set to "1". In this way the CPU is made aware that a reset has been executed by the SLIO1 CAN node.

2.4.2 Input Data Register

Register Marker = 0

This register is loaded with the actual digital value of the port pins P0..P7 when it is transmitted by the SLIO1. The content of this register is sent in response to a Remote Frame, or by a SLIO1 initiated transmission when an edge has been detected on a pin and has been enabled in the appropriate Edge Register. A high/low level on the pin is transmitted as a 1/0 data bit respectively. Note that after detecting an edge, the register will not actually be loaded into the Tx/Rx shift register until the Control Field in the CAN message has been sent. This effectively provides an input settling delay. Additionally, this register will automatically be sent by the SLIO1 after the chip has been reset by the ExtRst signal, upon waking up after sleep mode or after changing its Bus Mode, once it has successfully calibrated its oscillator.

7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

2.4.3 Positive Edge Register

Register Marker = 1

This register is used to enable automatic transmission of the contents of the input data register in the event that the corresponding pin P0..P7 makes a positive transition. A logical one enables such a transmission on a rising edge of the corresponding pin; a logical zero disables it.

7	6	5	4	3	2	1	0
PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0

2.4.4 Negative Edge Register

Register Marker = 2

As for the positive edge register but for falling edges.

7	6	5	4	3	2	1	0
NE7	NE6	NE5	NE4	NE3	NE2	NE1	NE0

2.4.5 Output Data Register

Register Marker = 3

This register holds the logical value which is output to the port pins P0..P7 which are enabled as outputs by the corresponding bits in the Data Direction Register. A 1/0 bit in the Output Data Register corresponds to the high/low level respectively on the output pin. This register is written by sending a message with the Register Marker set to 3.

7	6	5	4	3	2	1	0
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

2.4.6 Data Direction Register

Register Marker = 4

This register controls which pins will be used for the output. A logical 1 means that the pin will be driven and used as an output. A logical 0 means that the pin will not be driven internally. This register is written by sending a message with the Register Marker set to 4.

7	6	5	4	3	2	1	0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

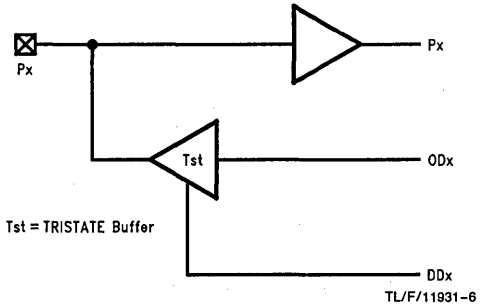

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FIGURE 6. Data Direction Control

2.5 IDENTIFIER PROGRAMMING

During Reset, the port pins will not be driven. At this time four bits for the Identifier for the messages for this chip will be read in from the pins ID0–ID3. The Identifier can therefore be set for each SLIO1 node by using resistors to V_{CC} and V_{SS} connected to these port pins. Port pins which are not otherwise used for input and output may be tied to V_{CC} or V_{SS}. The value of the resistors is determined solely by the fact that they must be able to ensure that the pin is at the required valid logic level before the reset signal is deactivated.

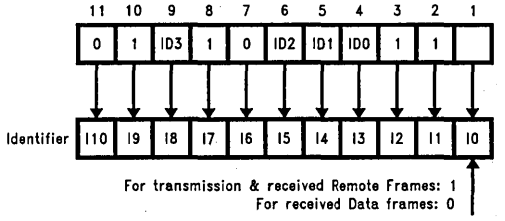

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FIGURE 7. Data and ID Formats

2.0 DS36001 Functional Description (Continued)

The SLIO1 uses the higher priority of the two adjacent 11 bit Identifiers for the Identifier of the messages to be received, and the lower priority Identifier for the transmission. (see Table IV).

Every device uses two adjacent addresses out of the 2032 possible in the standard CAN frame format. The higher prioritized ID (6 or E) is used to set up the device with a data frame. The lower prioritized ID (7 or F) is used for polling the SLIO1 via an RTR and is used from the SLIO1 to transmit its frame. This is required by the CAN protocol as only one transmitter for a specific data frame should exist.

The following table shows different address locations, which can be set up via the SLIO1 pins ID0 to ID3:

TABLE IV. Identifier Address Locations

ID3	ID2	ID1	ID0	Addresses (hex)
0	0	0	0	0x286 0x287
0	0	0	1	0x28E 0x28F
0	0	1	0	0x296 0x297
0	0	1	1	0x29E 0x29F
0	1	0	0	0x2A6 0x2A7
0	1	0	1	0x2AE 0x2AF
0	1	1	0	0x2B6 0x2B7
0	1	1	1	0x2BE 0x2BF
1	0	0	0	0x386 0x387
1	0	0	1	0x38E 0x38F
1	0	1	0	0x396 0x397
1	0	1	1	0x39E 0x39F
1	1	0	0	0x3A6 0x3A7
1	1	0	1	0x3AE 0x3AF
1	1	1	0	0x3B6 0x3B7
1	1	1	1	0x3BE 0x3BF

2.6 TRANSMISSION OF DATA FRAMES

A Data frame that is transmitted by the DS36001 device consists of two bytes. The first byte contains the SLIO1 status information and the register marker. The second byte contains the data from the I/O register. The Identifier will have a logical 1 for its least significant bit. This Identifier is also the Identifier which should be used by another node when sending a Remote Frame. Such a Remote Frame should always have its Data Length Code set to 2.

After successful transmission of a data frame, the SLIO1 delays the transmission of a possibly further pending message for a 3-bit time. This provides an opportunity for other CAN controllers having lower priority to transmit a message in case of a faulty contact at one of the edge-triggered port pins. In that case, the supererogatory bus load can be reduced by resetting the corresponding bit in the Positive or Negative Edge Register.

2.7 RECEPTION OF DATA FRAMES

Received data frames have the same format as the transmitted frames. Only the direction bit in the arbitration field is different. The status bits (Rstd, EW, Bus Mode, etc.) are ignored during reception. The Input Data Register will also be transmitted in response to the reception of a Remote Frame with the Transmit Identifier of the SLIO1. The device confirms each reception of a remote frame by transmitting a data frame containing the contents of the addressed I/O register.

2.8 ALTERNATE OPERATING MODES

2.8.1 External Clock

In addition to the normal operating mode, the DS36001 device can also operate with the external clock or in the TEST (SCAN) mode. These modes are controlled by the input pins TEST and ExtRst.

TEST	ExtRst	Mode
0	0	Normal mode using the integrated oscillator
0	1	Hardware reset
1	1	Normal mode using an external clock connected to ClkIn
1	0	Production test mode, port pins are redefined (SCAN mode)

How to Use an External Clock

In order to use an external clock, the external clock should be connected to the ClkIn input pin. The ExtRst pin should be connected to high, and the TEST pin can be used for the power-up reset function as shown in *Figure 8*. The frequency of the external clock can be selected between 4 MHz and 10 MHz.

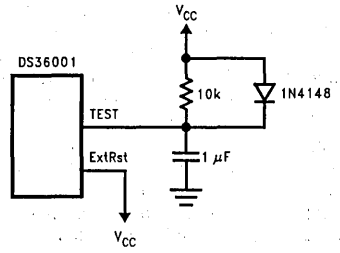

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FIGURE 8. Power-up Reset Circuit for External Clock Mode

The advantage of using an external Quartz-controlled clock is that it will allow the bus bandwidth (frequency limit) to be increased on both ends. For example, with an external clock of 5 MHz, the lower limit of the baud rate can be decreased from 20 kBaud to 10 kBaud. Likewise, with an external clock running at 10 MHz, the upper limit of the baud rate can be increased from 125 kBaud to 250 kBaud.

Note: The power-up reset circuit can also be used for the internal operating mode with internal oscillator. In this case, the TEST pin should be connected to "GND" and the ExtRst pin can be connected to the power-up reset circuit as shown below in *Figure 9*.

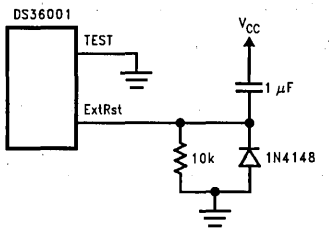

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FIGURE 9. Power-up Reset Circuit for Internal Clock Mode

2.0 DS36001 Functional Description

(Continued)

2.8.2 Production Test Mode

In this mode the function of the I/O port is redefined to allow a tester an access to the interior registers and signals; the clock of the integrated oscillator is replaced by an external clock which is connected to pin ClkIn. The information of the internal states, together with the signals at the Rx and Tx pins, provides sufficient data to ensure that the device behaves according to the CAN protocol and that the oscillator is calibrated to the bit stream.

The port pins are defined as shown below:

P0 Select second Function of P1, P3 and P4

P1 Scan-Path Output/Output of integrated Oscillator's Frequency

P2 Output of the calibrated Clock phl

P3 Scan-Path Input/Drive TxO Pin with the Signal of the Rx-Comparator

P4 Load PLA-Out in Scan Registers/Let Bit Counter run 10 Times Faster

P5 Scan-Path ck1

P6 Scan-Path ck2

P7 Error Warning

The Tx1 output pin is driven with the Tx Clock signal during this production test mode.

3.0 Protocol Overview

3.1 CAN DISCLAIMER

This overview describes some of the elements of the CAN protocol. For complete details, see the CAN Protocol Specification.

3.2 CAN FRAME FORMATS

There are two different types of frame used for data transmission and two types of frame used for control purposes in the CAN protocol.

3.2.1 Data Frame

Data frames consist of seven different bit fields:

Start of Frame (SOF)

Arbitration field

Control field (reserved bit, extended frame bit and DLC field)

Data field

CRC field

ACK field

End of Frame (EOF)

(DLC = Data Length Code, see explanation on "Control Field")

SOF	Arbitration Field Identifier + RTR	Control Field	Data Field	CRC Field	ACK Field	EOF
1 Bit	12 Bit	6 Bit	n*8 Bit	16 Bit	2 Bit	7 Bit

$n \in (0,8)$

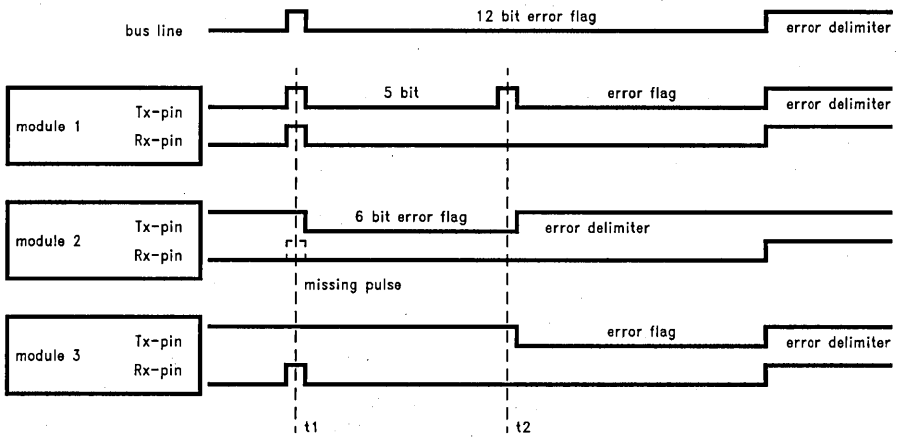
FIGURE 10. CAN Frame Format

3.2.2 Remote Frame

Remote frames are identical to Data frames except that they do not contain the data field. The DLC will contain the length code of the data requested.

3.2.3 Error Frame

The error Frame consists of two bit fields: the error flag and the error delimiter. The error flag field is built up from the various error flags of the different nodes. Therefore, its length may vary from a minimum of six bits up to a maximum of twelve bits depending on when a module is detecting the error. *Figure 11* shows how a local fault at one module (module 2) leads to a 12 bit error frame on the bus.

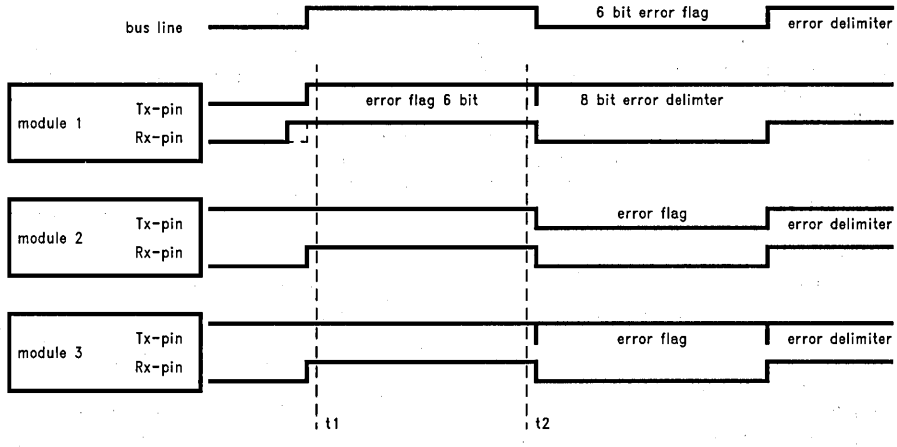


module 1 = error active transmitter detects bit error at t2
module 2 = error active receiver with a local fault at t1
module 3 = error active receiver detects stuff error at t2

TL/F/11931–10

FIGURE 11. Error Frame Length—Error Active Transmitter

3.0 Protocol Overview (Continued)



module 1 = error passive transmitter with local fault at t1
module 2 = error active receiver detects stuff error at t2
module 3 = error passive receiver detects stuff error at t2

TL/F/11931–11

FIGURE 12. Error Frame—Error Passive Transmitter

The bus level may either be dominant for an error-active node or recessive for an error-passive node. An error active node, detecting an error, starts transmitting an active error flag consisting of six dominant bits. This causes the destruction of the actual frame on the bus. The other nodes detect the error flag as either the rule of bit-stuffing or the value of a fixed bit field is destroyed. As a consequence all other nodes start transmission of their own error flag. This means, that the error sequence which can be monitored on the bus has a maximum length of twelve bits.

If an error passive node detects an error it transmits six recessive bits on the bus. This sequence does not destroy a message sent by another node and is not detected by other nodes. However if the node detecting an error was the transmitter of the frame the other modules will get an error condition by a violation of a fixed bit or the stuff rule. *Figure 12* shows how an error passive transmitter transmits a passive error frame and when the error is detected by the receivers.

After any module has transmitted its active or passive error flag it waits for the error delimiter which consists of eight recessive bits before continuing.

3.2.4 Overload Frame

Like an error frame, an overload frame consists of two bit fields: the overload flag and the overload delimiter. The bit fields have the same length as the error frame field: six bits for the overload flag and eight bits for the delimiter. The overload frame can only be sent after the end of frame (EOF) field and so destroys the fixed form of the intermission field. As a consequence all other nodes also detect an overload condition and start the transmission of an overload flag, too. After an overload flag has been transmitted the overload frame is closed by the overload delimiter.

3.3 DATA AND REMOTE FRAME FIELDS

3.3.1 Start of Frame (SOF)

The SOF indicates the beginning of data and remote frames. It consists of a single "dominant" bit. A node is only allowed to start transmission when the bus is idle. All nodes have to synchronize to the leading edge (first edge after the bus was idle) caused by the Start of Frame of the node which starts transmission first.

3.3.2 Arbitration Field

The arbitration field is composed of the identifier field and the RTR (Remote Transmission Request) bit. The value of the RTR bit is "dominant" in a data frame and "recessive" in remote frame.

3.3.3 Control Field

The control field consists of six bits. It starts with two bits reserved for future expansion followed by the four-bit Data Length Code. Receivers must accept all possible combinations of the two reserved bits. Until the function of these reserved bits is defined, the transmitter shall only send "0" bits. The first reserved bit is actually defined to indicate an extended frame with 29 Identifier bits if set to "1". The DS36001 will receive extended frames, and send ACK, however, no output will be changed.

The Data Length Code indicates the number of bytes in the data field. This Data Length Code consists of four bits. The data field can be of length zero. The admissible number of data bytes for a data frame ranges from 0 to 8. Other values than those specified in Table V may not be used.

3.0 Protocol Overview (Continued)

TABLE V. Coding of the Number of Data Bytes by the Data Length Code

Number of Data Bytes	Data Length Code			
	DLC3	DLC2	DLC1	DLC0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

3.3.4 Data Field

The Data field consists of the data to be transferred within a data frame. It can contain 0 to 8 bytes and each byte contains 8 bits. A remote frame has no data field. The SLIO1 can only have two bytes of data.

3.3.5 CRC Field

The CRC field consists of the CRC sequence followed by the CRC delimiter. The CRC sequence is derived by the transmitter from the modulo 2 division of the preceding bit fields, from the SOF to the end of the data field, excluding stuff-bits by the generator polynominal:

$$x^{15} + x^{14} + x^{10} + x^8 + x^7 + x^4 + x^3 + 1$$

The remainder of this division is the CRC sequence transmitted over the bus. On the receiver side the module divides all bit fields until the CRC delimiter, excluding stuff- bits, and checks if the result is zero. This will then be interpreted as a valid CRC. After the CRC sequence a single recessive bit is transmitted as the CRC delimiter.

3.3.6 ACK Field

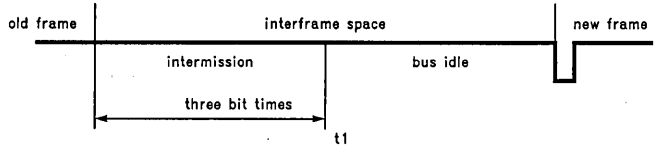
The ACK field is two bits long and contains the ACK slot and the ACK delimiter. The ACK slot is filled with a recessive bit by the transmitter. This bit is overwritten with a dominant bit by every receiver that has received a correct CRC sequence. The second bit of the ACK field is the acknowledge delimiter. It has a fixed form of recessive bits. As a consequence the acknowledge flag of a valid frame is surrounded by two recessive bits, the CRC delimiter and the ACK delimiter.

3.3.7 EOF Field

The End of Frame field closes a data and a remote frame. It consists of seven recessive bits.

3.3.8 Specification of the Inter Frame Space

Data and remote frames are separated from every preceding frame (data, remote, error and overload frames) by the inter frame space, see *Figure 13* and *Figure 14* for details. Error and Overload frames are not separated by an inter frame space in front of them. They can be transmitted as soon as the condition occurs. The inter frame space consists of a minimum of three bit fields relating to the error state of the node.



t1 is the first possible start bit of a new frame

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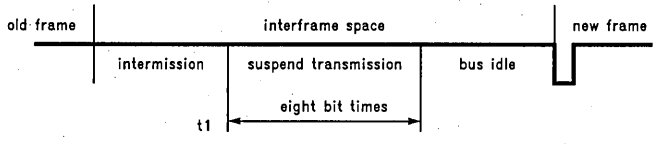
FIGURE 13. Inter Frame Space for Nodes Which are Not Error Passive or Have Been Receivers for the Last Frame



t1 except the error passive module which has transmitted the last frame any module can start transmission

TL/F/11931–13

FIGURE 14. Inter Frame Space for Nodes Which are Error Passive and Have Been Transmitters for the Last Frame

3.0 Protocol Overview (Continued)

These bit fields are coded as follows.

The intermission has the fixed form of three "recessive" bits. While this bit field is active no node is allowed to start a transmission of a data or a remote frame. The only action to be taken is signaling an overload condition. This means that also an error in this bit field would be interpreted as an overload condition. Suspend transmission has to be inserted by error-passive nodes that were transmitters for the last message. This bit field has the form of eight recessive bits. However, it may be overwritten by dominant start-bit from another non-error passive node which starts transmission. The bus idle field consists of recessive bits. Its length is not specified and depends on the bus load.

3.4 MULTI-MASTER PRIORITY BASED BUS ACCESS

The CAN protocol is a message based protocol that allows a total of 2032 different messages in the standard format and 512 million different messages in the extended frame format.

The CAN protocol allows several transmitting modules to start transmission at the same time as soon as they monitor the bus to be idle. During the start of transmission, every node monitors the bus line to determine if its message is overwritten by a message with a higher priority. As soon as a transmitting module detects another module with a higher priority accessing the bus, it stops transmitting its own frame and switches to receive mode. For illustration see *Figure 17*.

3.5 MULTICAST FRAME TRANSFER BY ACCEPTANCE FILTERING

Every CAN Frame is placed on the common bus. Each module receives every frame and filters out the frames which are not required for the module's task. For example if the dashboard sends a request to switch on the headlights, the CAN module responsible for the brake lights must not react to this message.

3.6 REMOTE DATA REQUEST

A CAN master module has the ability to set a specific bit called the Remote Transmission Request bit in a frame. This causes another module, either another master or a slave, to transmit a data frame.

3.7 SYSTEM FLEXIBILITY

Additional modules can be added to an existing network without a configuration change. These modules can either perform completely new functions requiring new data like an automatic window opener, or process existing data to perform a new function, such as oil-pressure measurement.

3.8 SYSTEM WIDE DATA CONSISTENCY

As the CAN network is message oriented, a message can be used like a variable which is automatically updated by the controlling processor. If any module cannot process information it can send an overload frame. However, the implementation of overload frame is optional.

If a data or remote frame was overwritten by either a higher-prioritized data frame or an error frame, the transmitting module will automatically retransmit it.

3.9 FRAME CODING

Remote and Data Frames are NRZ coded with bit-stuffing. In every bit field which holds computable information for the interface i.e., SOF, arbitration field, control field, data field (if present) and CRC field. Error and overload frames are NRZ coded without bit stuffing.

3.10 BIT STUFFING

After five consecutive bits of the same value, a stuff bit of the inverted value is inserted by the transmitter and deleted by the receiver (see *Figure 15*).

destuffed bit stream	100000x	011111x
stuffed bit stream	1000001x	0111110x
		$x \in \{0,1\}$

FIGURE 15. Bit-Stuffing

3.11 ORDER OF BIT TRANSMISSION

A frame is transmitted starting with the SOF, sequentially followed by the remaining bit fields. In every bit field the MSB is transmitted first. The transmission order from either data byte is not defined in the CAN specification. Here, it is assumed that the data bytes are transmitted in the same way as the bits are, i.e., most significant byte first.

SOF	Identifier	RTR	Control	Data	CRC
	ID10 ID0		MSB LSB	MSB LSB	MSB LSB

↑ first bit transmitted

FIGURE 16. Order of Bit Transmission

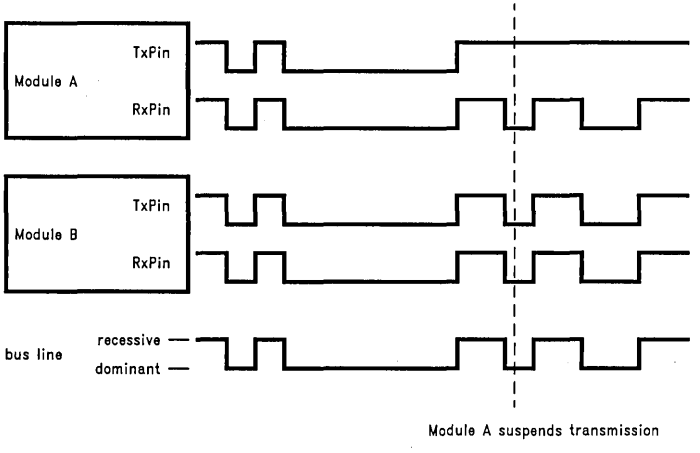
3.12 FRAME VALIDATION

According to the CAN 2.0 specification frames have a different validation point for the transmitter and receiver. A frame is valid for the transmitter of a message if there is no error until the first bit of End of Frame field. A frame is valid for a receiver, if there is no error until the last but one bit of the End of Frame.

3.13 FRAME ARBITRATION AND PRIORITY

Except for an error passive node which transmitted the last frame, all nodes are allowed to start transmission of a frame after the intermission, which can lead to two or more nodes starting transmission at the same time. To prevent a node from destroying another node's frame it monitors the bus during transmission of the identifier field and the RTR-bit. As soon as it detects a dominant bit while transmitting a recessive bit it releases the bus, immediately stops transmission and starts receiving the frame. This causes no data or remote frame to be destroyed by another. Therefore the highest priority message with the identifier 0x000 always gets the bus.

3.0 Protocol Overview (Continued)



TL/F/11931–14

FIGURE 17. Message Arbitration

There are three more items that should be taken into consideration to avoid unrecoverable collision on the bus:

- Within one system each message must be assigned to a unique identifier. Consider two messages, e.g. oil-pressure and rpm, having the same identifier but in most cases different data. So both modules may start transmission of a frame at the same time and both win arbitration. This will always result in bit errors in either or both of the modules as one is transmitting a dominant data bit while the other is transmitting a recessive data bit.
- Data frames with a given identifier and a non-zero DLC should only be initiated by one node. Otherwise in the worst cases, two nodes count up to the bus-off state, due to bit errors, if they always start transmitting the same ID with different data.
- Every remote frame should have a system-wide DLC which is the DLC of the corresponding data frame. Otherwise two modules starting transmission of a remote frame at the same time will overwrite each others DLC which results in bit errors as described above.

3.14 ACCEPTANCE FILTERING

Every node performs acceptance filtering on the identifier of a data or a remote frame to filter out the messages which are not required by the node. So only the data of frames which match the acceptance filter is stored in the corresponding data buffers.

However every node which is not in the bus-off state and has received a correct CRC-sequence acknowledges the frame.

3.15 BIT TIMING DEFINITION

3.15.2 Nominal Bit Rate

The nominal bit rate is the number of bits per second transmitted in the absence of resynchronization by an ideal transmitter.

The bit rate will adjust itself to that of the rest of the network system within the range of 20 Kbaud to 125 Kbaud.

3.15.2 Nominal Bit Time

Nominal Bit Time = 1/Nominal Bit Rate

3.15.3 Segments of Bit Time

The nominal bit time can be thought of as being divided into four non-overlapping time segments:

- Synchronization Segment
- Propagation Segment
- Phase Buffer Segment #1
- Phase Buffer Segment #2

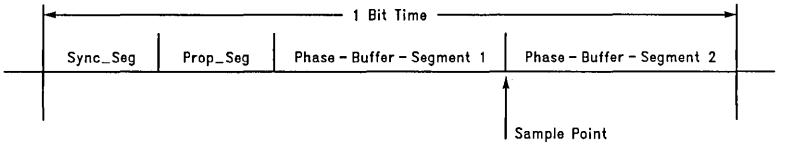


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FIGURE 18. Segments of 1 Bit Time

3.0 Protocol Overview (Continued)

Synch Segment:

This part of the bit time is used to synchronize various modes on the bus. An edge is expected to lie within this segment.

Propagation Segment:

This part is used to compensate for the physical delay times within the network. This segment is twice the sum of the signal's propagation time on the bus line, the input comparator delay, and the output driver delay.

Phase Segments 1 and 2:

The Phase Segment Buffers are used to compensate for edge phase errors. These segments can be lengthened or shortened by synchronization.

The nominal bit time is internally adjusted to the bit time of the calibration message, provided that its bit time is within the specified range.

Sample Point:

The sample point is the point of time at which the bus level is read and interpreted as the value of that respective bit. Its location is the end of Phase Segment.

Information Processing Time:

The information processing time is the time segment starting with the sample point reserved for the calculation of the subsequent bit level.

3.15.4 Time Quantum

The Time Quantum is a fixed unit of time derived from the oscillator period. There exists a programmable prescaler, with integral values, ranging at least from 1 to 32. Starting with the minimum Time Quantum, the Time Quantum can have a length of:

Time Quantum = m * minimum Time Quantum (m is the value of prescaler).

The length of each time segment is fixed for DS36001 and is given below.

Segment	Length in Time Quanta
Sync_Segment	1
Prop_Segment	1
Phase_Seg1	4
Phase_Seg2	4

3.15.5 Synchronization

Every receiver starts with a "hard synchronization" on the falling edge of the SOF bit. As stated before, one bit time consists of four time segments.

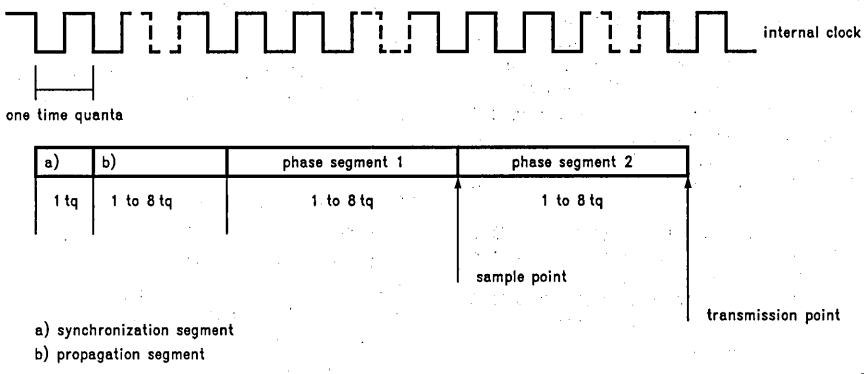

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FIGURE 19. Bit Timing

3.0 Protocol Overview (Continued)

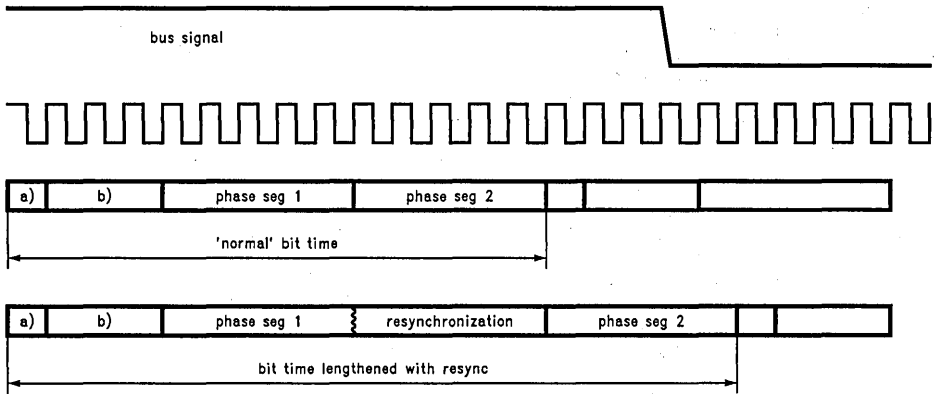
Either a rising or falling edge of the data signal should be in the synchronization segment. This segment has the fixed length of one time quanta. To compensate for the various delays within the network the propagation segment is used.

There are two types of synchronization supported:

"Hard synchronization" is done with the falling edge on the bus while the bus is idle, which is then interpreted as the SOF. It restarts the internal logic.

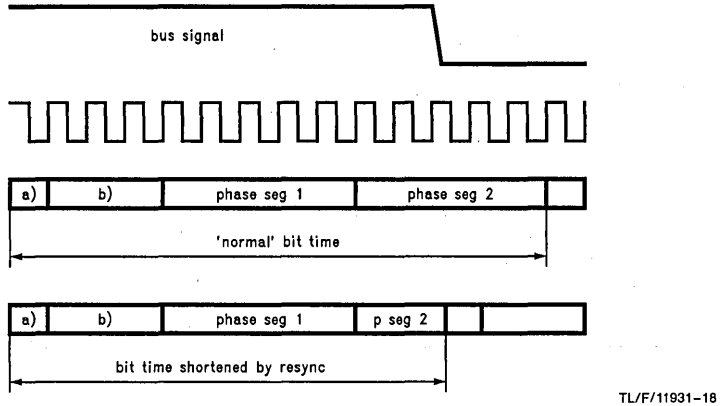
"Soft synchronization" is used to lengthen or shorten the bit time while a data or remote frame is received. Whenever a falling edge is detected in the propagation segment or in phase segment 1, the segment is lengthened by a specific value, the resynchronization jump width, see *Figure 20.*

If a falling edge lies in the phase segment 2 it is shortened by the resynchronization jump width. Only one resynchronization is allowed during one bit time. The sample point lies between the two phase segments and is the point where the received data is supposed to be valid. The transmission point lies at the end of phase segment 2 to start a new bit time with the synchronization segment.



TL/F/11931–17

FIGURE 20. Resynchronization 1



TL/F/11931–18

FIGURE 21. Resynchronization 2

National Semiconductor

PC87310 (SuperI/O™) Dual UART with Floppy Disk Controller and Parallel Port†

General Description

The PC87310 incorporates two full function UARTs, a floppy disk controller (FDC) with analog data separator, one parallel port, game port decode, hard disk controller decode, standard XT/AT address decoding for on-chip functions, and a Configuration Register in one chip. Thus it offers a single chip solution to the most commonly used IBM®PC, XT, and AT peripherals. The floppy disk controller is fully compatible with the industry standard 765 architecture, but it includes many more advanced options such as a high performance data separator, extended track range to 4096, implied seek command, scan command, and both standard IBM formats as well as ISO 3.5" formats. The UARTs are compatible with either the INS8250N-B or the NS16450. The parallel port, hard disk select, and game port select logic maintain complete compatibility with the IBM XT and AT. Hardware selects XT or AT compatibility.

The Configuration Register is one byte wide and can be programmed via hardware or software. Through its control, the user can assign standard AT addresses and disable any major on-chip function (e.g., the FDC, either UART, or the parallel port) independently of the others. This allows for flexibility in system configuration when adapter cards contain duplicate functions.

Features

- 100% compatible to the IBM PC, XT and AT architectures
- Software compatible to the INS8250N-B, INS8250A and NS16450 UARTs
- 100% compatible to the industry standard 765A architecture
- On-chip analog data separator operates up to 1 Mb/s
- Implements all DP8473 Floppy Disk Controller functions
- Bidirectional parallel port for printer or scanner operation. Provides all standard Centronics and IBM PC, XT, and AT interface signals.
- Decoding and chip selects for an IDE hard disk interface
- Address decoding and strobe generation for a game port
- Fabricated in NSC's 1.5 μ M2CMOS process
- Low power CMOS with a power down mode
- 100-pin EIAJ plastic flatpak package
- Integrates all PC-XT®, PC-AT® logic
  - On chip 24 MHz crystal oscillator
  - DMA enable logic
  - IBM compatible address decode of A0–A9
  - 24 mA μP bus interface buffers
  - 40 mA floppy drive interface buffers
  - Data rate and drive control registers
- Precision analog data separator
  - Self-calibrating PLL and delay line
  - Automatically chooses one of three filters
  - Intelligent read algorithm
- Two pin programmable precompensation modes
- Other enhancements
  - Implied seek up to 4000 tracks
  - IBM or ISO formatting
- Separate interrupt request lines for the parallel and serial ports
- Adds or deletes standard asynchronous communication bits (start, parity, and stop) to or from the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generators for each UART channel divide the input clock by 1 to ($2^{16} - 1$) and generate the internal 16 × sample clock
- MODEM control functions for each UART channel (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial-interface characteristics:
  - 5, 6, 7, or 8 bit characters
  - Even, odd, or no parity generation and detection
  - 1, 1½, or 2 stop bit generation
- High current drive capability for the parallel port

†**Note:** This part is patented.

National Semiconductor

PC87311A/PC87312 (SuperI/O™ II/III) Floppy Disk Controller with Dual UARTs, Parallel Port, and IDE Interface

General Description

The PC87311A/12 incorporates a floppy disk controller (FDC), two full function UARTs, a bidirectional parallel port, and IDE interface control logic in one chip. The PC87311A includes standard AT/XT address decoding for on-chip functions and a Configuration Register, offering a single chip solution to the most commonly used IBM® PC®, PC-XT®, and PC-AT® peripherals. The PC87312 includes standard AT address decoding for on-chip functions and a Configuration Register set, offering a single chip solution to the most commonly used ISA, EISA and Micro Channel peripherals.

The on-chip FDC is software compatible to the PC8477, which contains a superset of the DP8473 and NEC μPD765 and the N82077 floppy disk controller functions. The on-chip analog data separator requires no external components and supports the 4 Mb drive format as well as the other standard floppy drives used with 5.25″ and 3.5″ media.

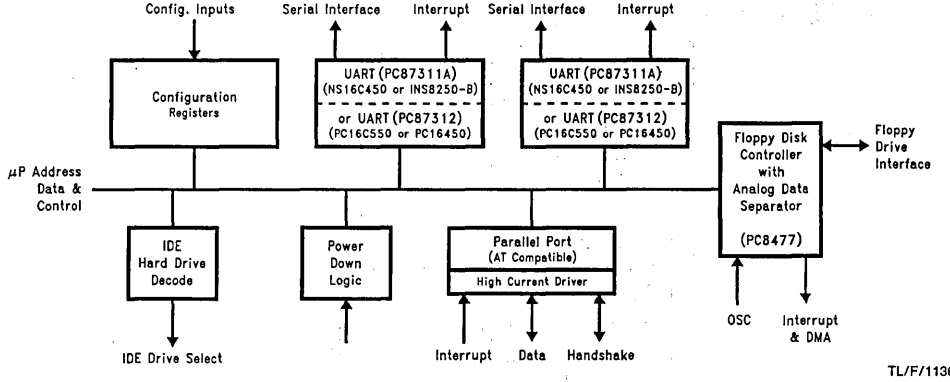
In the PC87311A, the UARTs are equivalent to two INS8250N-Bs or NS16450s. The bidirectional parallel port maintains complete compatibility with the IBM PC, XT and AT. In the PC87312 the UARTs are equivalent to two NS16450s or PC16550s. The bidirectional parallel port maintains complete compatibility with the ISA, EISA and Micro Channel parallel ports.

The IDE control logic provides a complete IDE interface except for the signal buffers. The Configuration Registers consist of three byte-wide registers. An Index and a Data Register which can be relocated within the ISA I/O address space access the Configuration Registers.

Features

- 100% compatible with IBM PC, XT, and AT architectures (PC87311A), or ISA, EISA, and Micro Channel architectures (PC87312)
- FDC:
  - Software compatible with the DP8473, the 765A and the N82077
  - 16-byte FIFO (default disabled)
  - Burst and Non-Burst modes
  - Perpendicular Recording drive support
  - High performance internal analog data separator (no external filter components required)
  - Low power CMOS with power down mode
- UARTs:
  - Software compatible with the INS8250N-B and the NS16450 (PC87311A), or PC16550A and PC16450 (PC87312)
- Parallel Port:
  - Bidirectional under either software or hardware control
  - Compatible with all IBM PC, XT and AT architectures (PC87311A), or all ISA, EISA, and Micro Channel architectures (PC87312)
  - Back Voltage protection circuit against damage caused when printer is powered up
- IDE Control Logic:
  - Provides a complete IDE interface except for optional buffers
- Address Decoder:
  - Provides selection of all primary and secondary ISA addresses including COM 1–4.
- 100-pin PQFP package
  - The PC87311A and PC87312 are pin compatible

Block Diagram



TL/F/11362–1

National Semiconductor

PC16550C/NS16550AF Universal Asynchronous Receiver/Transmitter with FIFOs†

General Description

The PC16550C/NS16550AF is an improved version of the original NS16450 Universal Asynchronous Receiver/Transmitter (UART). Functionally identical to the NS16450 on powerup (CHARACTER mode)* the PC16550C/NS16550AF can be put into an alternate mode (FIFO mode) to relieve the CPU of excessive software overhead.

In this mode internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. All the logic is on chip to minimize system overhead and maximize system efficiency. Two pin functions have been changed to allow signalling of DMA transfers.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to ($2^{16}-1$), and producing a 16 × clock for driving the internal transmitter logic. Provisions are also included to use this 16 × clock to drive the receiver logic. The UART has complete MODEM-control capability, and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

The UART is fabricated using National Semiconductor's advanced M²CMOS process.

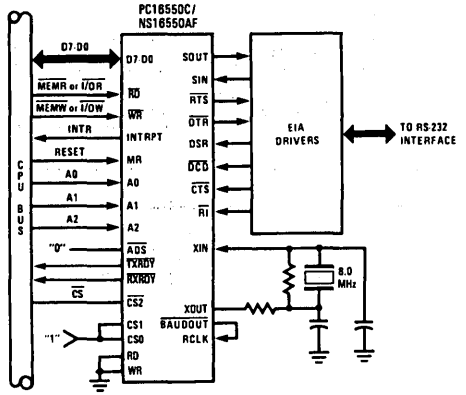
*Can also be reset to NS16450 Mode under software control.

†**Note: These parts are patented.**

Features

- Capable of running all existing 16450 software.
- Pin for pin compatible with the existing 16450 except for CSOUT (24) and NC (29). The former CSOUT and NC pins are $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$, respectively.
- After reset, all registers are identical to the 16450 register set.
- In the FIFO mode transmitter and receiver are each buffered with 16 byte FIFO's to reduce the number of interrrupts presented to the CPU.
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from the serial data.
- Holding and shift registers in the 16450 Mode eliminate the need for precise synchronization between the CPU and serial data.
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator divides any input clock by 1 to ($2^{16}-1$) and generates the 16 × clock.
- Independent receiver clock input.
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud generation (DC to 1.5M baud).
- False start bit detection.
- Complete status reporting capabilities.
- TRI-STATE® TTL drive for the data and control buses.
- Line break generation and detection.
- Internal diagnostic capabilities:
  - Loopback controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation.
- Full prioritized interrupt system controls.

Basic Configuration



TL/C/8652-1

Section 6

General Purpose Line Drivers

Section 6 Contents

National Semiconductor

DS1692/DS3692 TRI-STATE® Differential Line Drivers

General Description

The DS1692/DS3692 are low power Schottky TTL line drivers electrically similar to the DS1691A/DS3691 but tested to meet the requirements of MIL-STD-188-114A (see Application Note AN-216). MIL-STD-188-114A type 1 driver specifications can be met by adding an external three resistor voltage divider to the output of the DS3692/1692. The DS3692/1692 feature 4 buffered outputs with high source and sink current capability with internal short circuit protection.

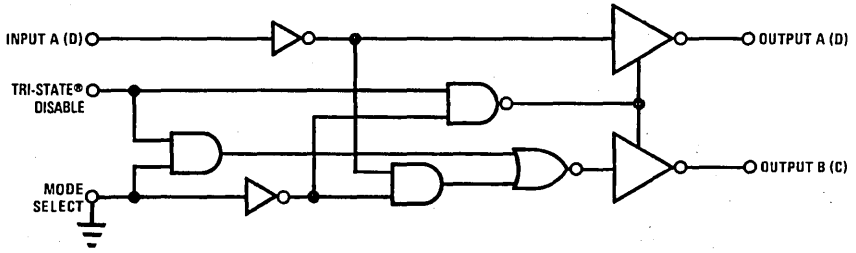
With the mode select pin low, the DS1692/DS3692 are dual differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE and 0V output unbalance when operated with ±5V supply.

Multipoint applications in differential mode with waveshaping capacitors is not allowed.

Features

- Short circuit protection for both source and sink outputs
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption
  - Differential mode I_{CC} = 9 mA/driver typ
  - I_{EE} = 5 mA/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Adaptable as MIL-STD-188-114A type 1 driver

Logic Diagram (½ Circuit Shown)



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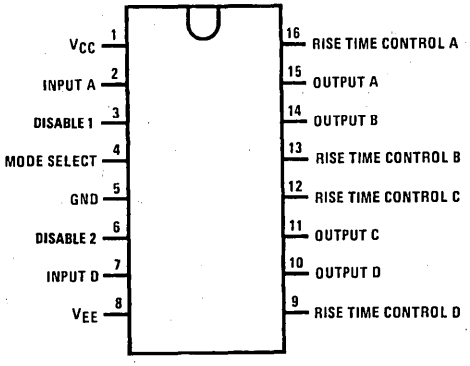
Connection Diagram



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Top View

Order Number DS1692J, DS3692J, DS3692M or DS3692N
See NS Package Number J16A, M16A* or N16A

*Contact Product Marketing for availability.

Truth Table

Inputs			Outputs	
Mode	A (D)	Disable1 (2)	A (D)	B (C)
0	0	0	0	1
0	0	1	TRI-STATE	TRI-STATE
0	1	0	1	0
0	1	1	TRI-STATE	TRI-STATE

6

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 10.1 mW/°C; derate molded package 11.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1692			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3692			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1692	−55	+125	°C
DS3692	0	+70	°C

Electrical Characteristics DS1692/DS3692 (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DS1692, V_{CC} = 5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_O $\overline{V_O}$	Differential Output Voltage $V_{A,B}$	R_L = ∞	V_{IN} = 2V	2.5	3.6		V
			V_{IN} = 0.8V	−2.5	−3.6		V
V_T $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	R_L = 100Ω V_{CC} ≥ 4.75V	V_{IN} = 2V	2	2.6		V
			V_{IN} = 0.8V	−2	−2.6		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	R_L = 100Ω, V_{CC} ≥ 4.75V		4.0	4.8		V
I_{OX}	TRI-STATE Output Current	V_O ≤ −10V			−0.002	−0.15	mA
		V_O ≥ 15V			0.002	0.15	mA
I_{SA}	Output Short Circuit Current	V_{IN} = 0.4V	V_{OA} = 6V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA
DS1692, V_{CC} = 5V ±10%, V_{EE} = −5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} = −5 ±5%, MODE SELECT ≤ 0.8V							
V_O $\overline{V_O}$	Differential Output Voltage $V_{A,B}$	R_L = ∞	V_{IN} = 2.4V	7	8.5		V
			V_{IN} = 0.4V	−7	−8.5		V
V_T $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	R_L = 200Ω	V_{IN} = 2.4V	6	7.3		V
			V_{IN} = 0.4V	−6	−7.3		V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Output Unbalance	$\lvert V_{CC} \rvert = \lvert V_{EE} \rvert$, R_L = 200Ω			0.02	0.4	V
I_{OX}	TRI-STATE Output Current		V_O = 10V		0.002	0.15	mA
			V_O = −10V		−0.002	−0.15	mA
I_S^+ I_S^-	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
			V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, R_L = ∞			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, R_L = ∞			−10	−22	mA

Electrical Characteristics (Notes 2 and 3) $V_{EE} \leq 0V$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
I_{XA} I_{XB}	Output Leakage Current Power OFF	$V_{CC} = V_{EE} = 0V$	$V_O = 15V$		0.01	0.15	mA
			$V_O = -15V$		−0.01	−0.15	mA

Switching Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{CC} = 5V$, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_f	Differential Output Fall Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
$V_{CC} = 5V$, $V_{EE} = -5V$, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_f	Differential Output Fall Time	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PDL}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PDH}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PZL}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns

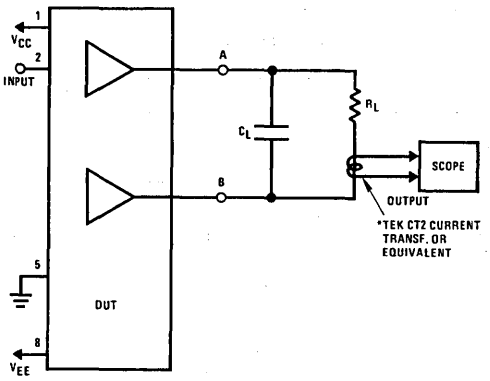
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1692 and across the 0°C to +70°C range for the DS3692. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

AC Test Circuits and Switching Time Waveforms



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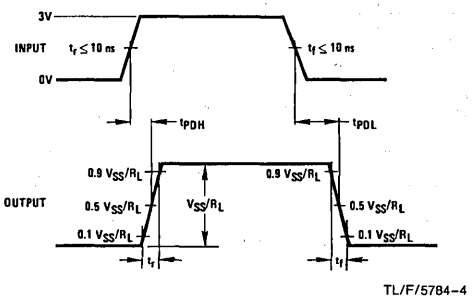

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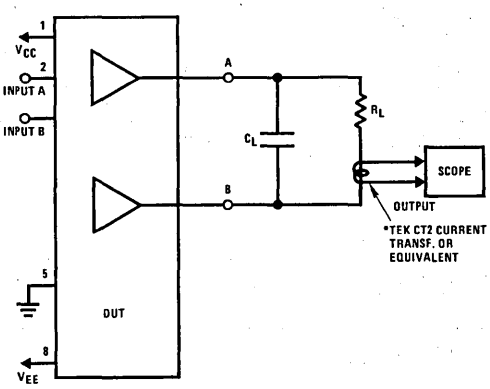
FIGURE 1. Differential Connection



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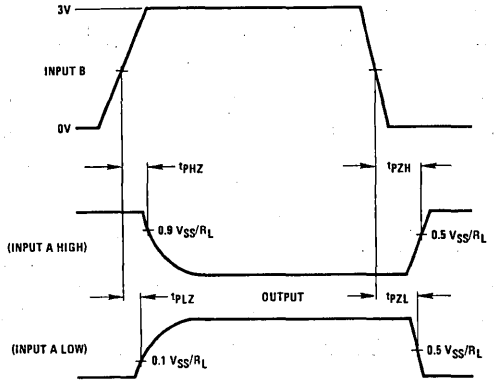

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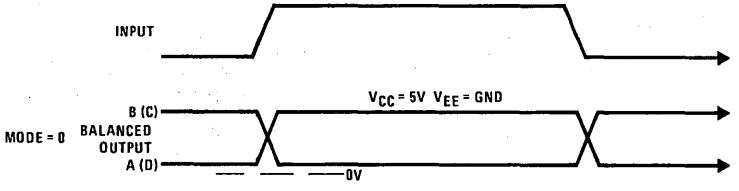
FIGURE 2. TRI-STATE Delays for DS1692/DS3692

Switching Waveforms



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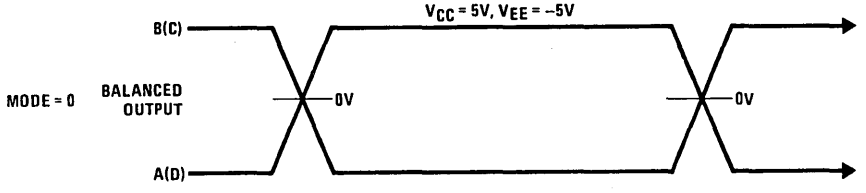


TL/F/5784–8

National Semiconductor

DS55110A/DS75110A Dual Line Drivers

General Description

The DS55110A, DS75110A are dual line drivers with independent channels, common supply and ground terminals featuring constant current outputs. These drivers are designed for optimum performance when used with the DS55107/DS75107, DS55108/DS75108 line receivers.

The output current of the DS55110A, DS75110A is nominally 12 mA and may be switched to either of two output terminals with the appropriate logic levels at the driver input.

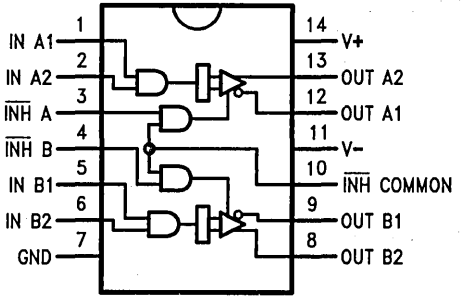
Separate or common control inputs are provided for increased logic versatility. These control or inhibit inputs allow the output current to be switched off (inhibited) by applying low logic levels to the control inputs. The output current in the inhibit mode, $I_{O(Off)}$, is specified so that minimum line loading is induced. This is highly desirable in system applications using party line data communications.

Features

- Improved stability over supply voltage and temperature ranges
- Constant current, high impedance outputs
- High speed: 15 ns max propagation delay
- Standard supply voltages
- Inhibitor available for driver selection
- High common mode output voltage range (−3.0V to 10V)
- TTL input compatibility
- Extended temperature range

Connection Diagram

14-Lead Dual-In-Line Package and SO-14 Package



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Top View

Order Number DS75110AM or DS75110AN
See NS Package Number M14A or N14A

For Complete Military 883 Specifications, see RETS Data Sheet.

Order Number DS55110AJ/883
See NS Package Number J14A

Function Table

Inputs				Outputs	
Logic		Inhibitor			
1	2	A/B	$\overline{INH}$	A1/B1	A2/B2
X	X	L	X	Off	Off
X	X	X	L	Off	Off
L	X	H	H	Off	On
X	L	H	H	Off	On
H	H	H	H	On	Off

H = High, L = Low, X = Don't Care

6

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP and SO-14: −65°C to +150°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP and SO-14 (Soldering, 10 sec.): 265°C

Maximum Power Dissipation* at 25°C
- Cavity Package: 1360 mW
- Molded Package: 1040 mW
- SO Package: 930 mW

*Derate cavity package 9.1 mW/°C above 25°C; derate molded DIP package 8.3 mW/°C above 25°C; derate SO package 7.5 mW/°C above 25°C.

Suppy Voltage: ±7.0V

Input Voltage (Any Input): 5.5V

Output Voltage (Any Output): −5.0V to +12V

Recommended Operating Conditions

	DS55110A			DS75110A			Units
	Min	Typ	Max	Min	Typ	Max	
Positive Supply Voltage (V^+)	4.5	5.0	5.5	4.75	5.0	5.25	V
Negative Supply Voltage (V^-)	−4.5	−5.0	−5.5	−4.75	−5.0	−5.25	V
Positive Common Mode Voltage (V_{CM}^+)	0		10	0		10	V
Negative Common Mode Voltage (V_{CM}^-)	0		−3.0	0		−3.0	V
Operating Temperature (T_A)	−55	25	125	0	25	70	°C

Electrical Characteristics

Over recommended operating temperature range, unless otherwise specified. (Notes 2 and 3)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA		−0.9	−1.5	V
$I_{O(On)}$	On-State Output Current		V_{CC} = Max, V_O = 10V		12	15	mA
			V_{CC} = Min, V_O = −3.0V	6.5	12		
$I_{O(Off)}$	Off-State Output Current (Inhibited Only)		V_{CC} = Min, V_O = 10V			100	μA
I_I	Input Current At Maximum Input Voltage	A, B or C Inputs	V_{CC} = Max, V_I = 5.5V			1.0	mA
		D Input				2.0	
I_{IH}	Input Current HIGH	A, B or C Input	V_{CC} = Max, V_I = 2.4V			40	μA
		D Input				80	
I_{IL}	Input Current LOW	A, B or C Input	V_{CC} = Max, V_I = 0.4V			−3.0	mA
		D Input				−6.0	
$I^+_{(On)}$	Positive Supply Current with Driver Enabled		V_{CC} = Max, A & B Inputs at 0.4V, C & D Inputs at 2.0V		23	35	mA
$I^-_{(On)}$	Negative Supply Current with Driver Enabled				−34	−50	mA
$I^+_{(Off)}$	Positive Supply Current with Driver Inhibited		V_{CC} = Max, A, B, C & D Inputs at 0.4V		21		mA
$I^-_{(Off)}$	Negative Supply Current with Driver Inhibited				−17		mA

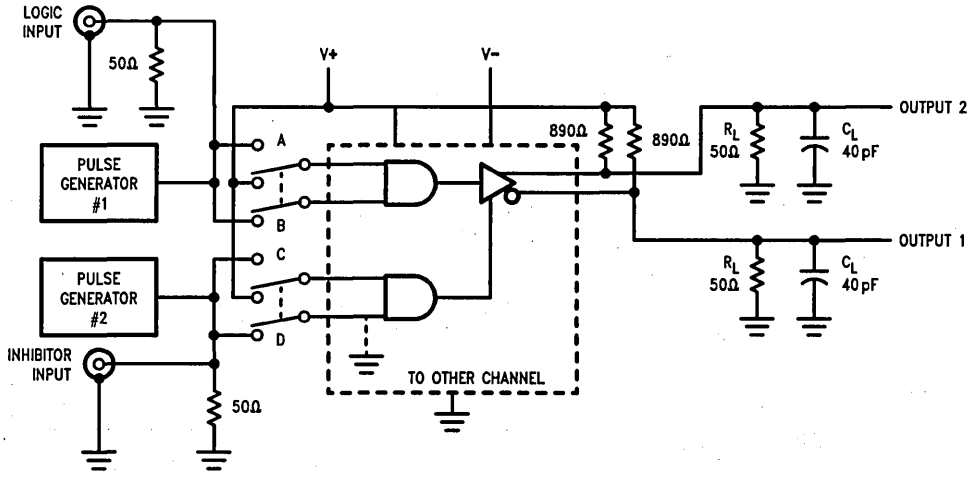
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55110 and across the 0°C to +70°C range for the DS75110. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

Switching Characteristics $V_{CC} = \pm 5V, T_A = 25°C$

Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, LOW to HIGH	C_L = 40 pF, R_L = 50Ω See Test Circuit	A or B	1 or 2		9.0	15	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					9.0	15	ns
t_{PLH}	Propagation Delay Time, LOW to HIGH		C or D	1 or 2		16	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					13	25	ns



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Note 1: The pulse generators have the following characteristics:
$t_r = t_f$ = 10 ns ±5.0 ns, t_{w1} = 500 ns, PRR = 1.0 MHz, t_{w2} = 1.0 μs, PRR = 500 kHz, Z_O = 50Ω.

Note 2: C_L includes probe and jib capacitance.

Note 3: For simplicity, only one channel and the inhibitor connections are shown.

FIGURE 2. AC Test Circuit

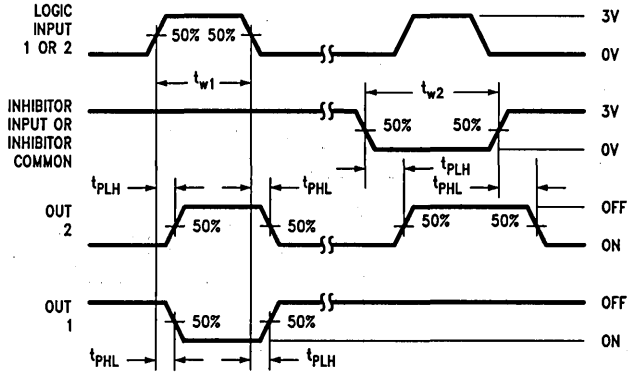

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FIGURE 3. AC Waveforms

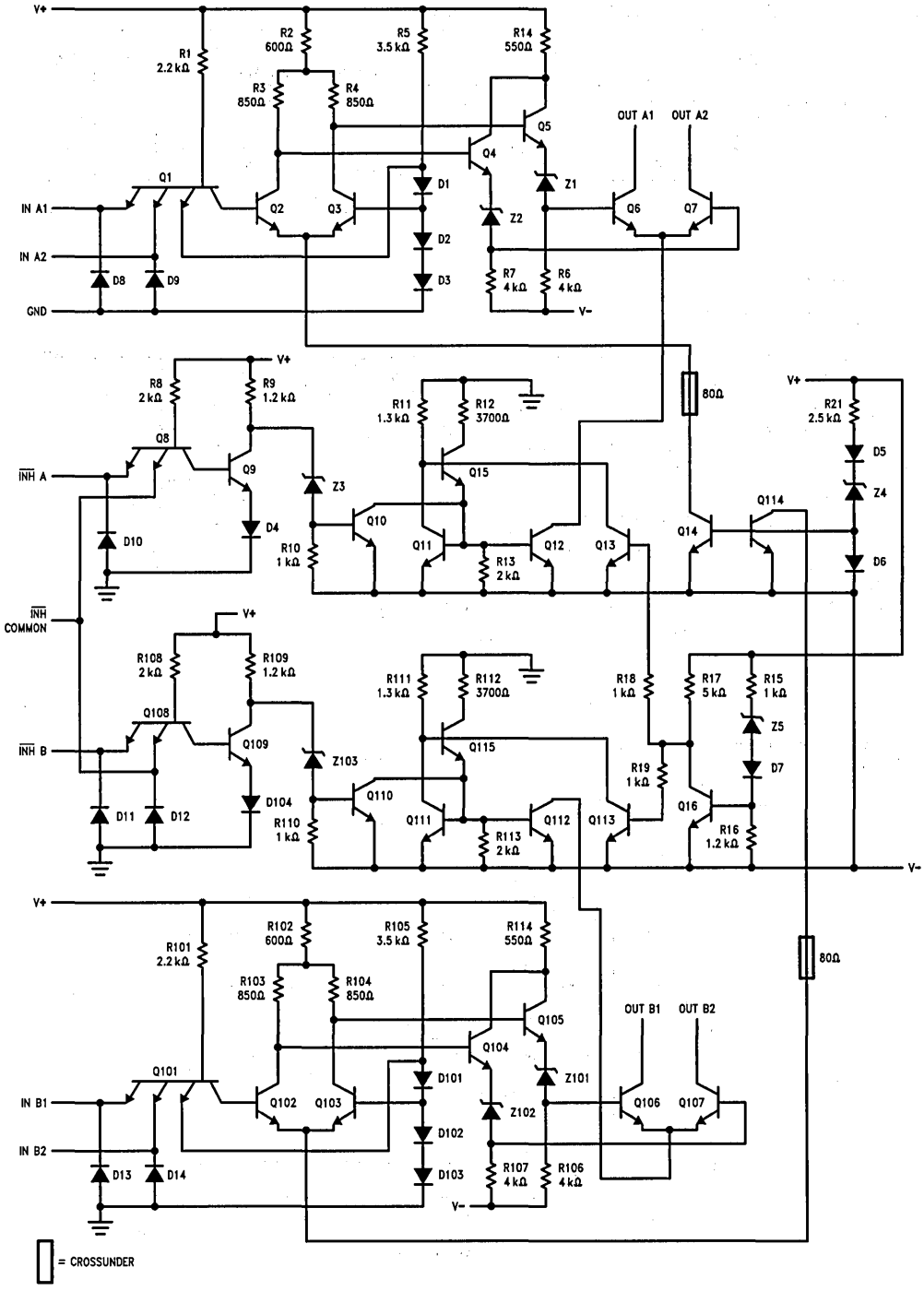

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FIGURE 1. Equivalent Circuit

Typical Applications

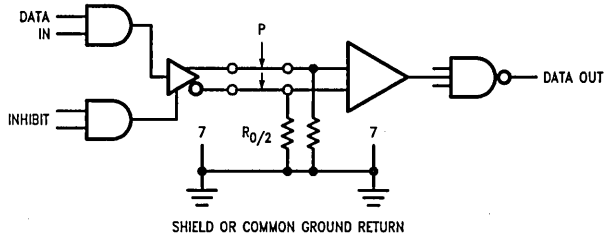

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FIGURE 4. Simplex Operation

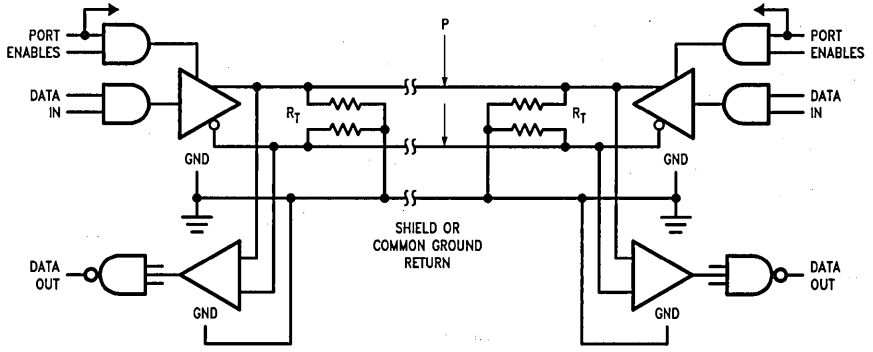

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FIGURE 5. Half-Duplex Operation

Note 1: All drivers are DS75110A or DS55110A. Receivers are DS75107 or DS75108. Twisted-pair or coaxial transmission line should be used for minimum noise and cross talk.

Note 2: When only one driver in a package is being used, the outputs of the other driver should either be grounded or inhibited to reduce power dissipation.

National Semiconductor

DS55113/DS75113 Dual TRI-STATE® Differential Line Driver

General Description

The DS55113/DS75113 dual differential line drivers with TRI-STATE outputs are designed to provide all the features of the DS55114/DS75114 line drivers with the added feature of driver output controls. There are individual controls for each output pair, as well as a common control for both output pairs. When an output control is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

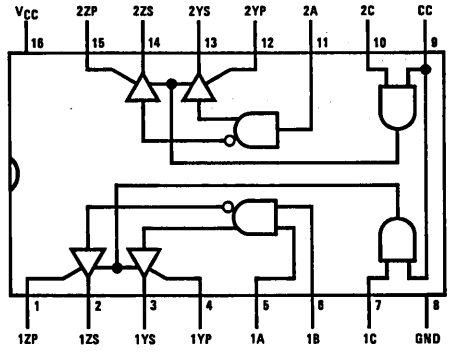
The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

Features

- Each circuit offers a choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- High-impedance output state for party-line applications
- Short-circuit protection
- High current outputs
- Single-ended or differential AND/NAND outputs
- Common and individual output controls
- Clamp diodes at inputs
- Easily adaptable to DS55114/DS75114 applications

Connection Diagram

Dual-In-Line Package



Positive logic: $Y = AB$
$Z = \overline{AB}$

Output is OFF when C or CC is low

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Top View
Order Number DS55113J, DS75113M or DS75113N
See NS Package Number J16A, M16A or N16A

For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS55113J/883
See NS Package Number J16A

Truth Table

Inputs				Outputs	
Output Control		Data		AND	NAND
C	CC	A	B*	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H*
H	H	X	L	L	H
H	H	H	H	H	L

H = high level
L = low level
X = irrelevant
Z = high impedance (OFF)
*B input and 4th line of truth table applicable only to driver number 1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 1) 7V

Input Voltage 5.5V

OFF-State Voltage Applied to Open-Collector Outputs 12V

Maximum Power Dissipation* at 25°C
- Cavity Package 1433 mW
- Molded DIP Package 1362 mW
- SO Package 1002 mW

Operating Free-Air Temperature Range
- DS55113 −55°C to +125°C
- DS75113 0°C to +70°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C (Note 2).

Storage Temperature Range −65°C to +150°C

Lead Temperature (1/16" from case for 60 seconds): J Package 300°C

Lead Temperature (1/16" from case for 4 seconds): N Package 260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS55113	4.5	5.5	V
DS75113	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55113	−55	125	°C
DS75113	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Conditions (Note 3)			DS55113 Min	DS55113 Typ (Note 4)	DS55113 Max	DS75113 Min	DS75113 Typ (Note 4)	DS75113 Max	Units
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage							0.8			0.8	V
V_{IK}	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.23	0.4		0.23	0.4	V
V_{OK}	Output Clamp Voltage		V_{CC} = Max, I_O = −40 mA				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	Off-State Open-Collector Output Current		V_{CC} = Max	V_{OH} = 12V	T_A = 25°C		1	10				μA
					T_A = 125°C			200				
				V_{OH} = 5.25V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	Off-State (High-Impedance-State) Output Current		V_{CC} = Max, Output Controls at 0.8V	T_A = 25°C, V_O = 0 to V_{CC}				±10			±10	μA
				T_A = Max	V_O = 0V			−150			−20	
					V_O = 0.4V			±80			±20	
					V_O = 2.4V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input Current at Maximum Input Voltage	A, B, C	V_{CC} = Max, V_I = 5.5V					1			1	mA
		CC						2			2	
I_{IH}	High Level Input Current	A, B, C	V_{CC} = Max, V_I = 2.4V					40			40	μA
		CC						80			80	
I_{IL}	Low Level Input Current	A, B, C	V_{CC} = Max, V_I = 0.4V					−1.6			−1.6	mA
		CC						−3.2			−3.2	

6

Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions (Note 3)		DS55113			DS75113			Units
				Min	Typ (Note 4)	Max	Min	Typ (Note 4)	Max	
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0V		−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	All Inputs at 0V, No Load T_A = 25°C	V_{CC} = Max		47	65		47	65	mA
			V_{CC} = 7V		65	85		65	85	

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section.

Note 3: All parameters with the exception of OFF-state open-collector output current are measured with the active pull-up connected to the sink output.

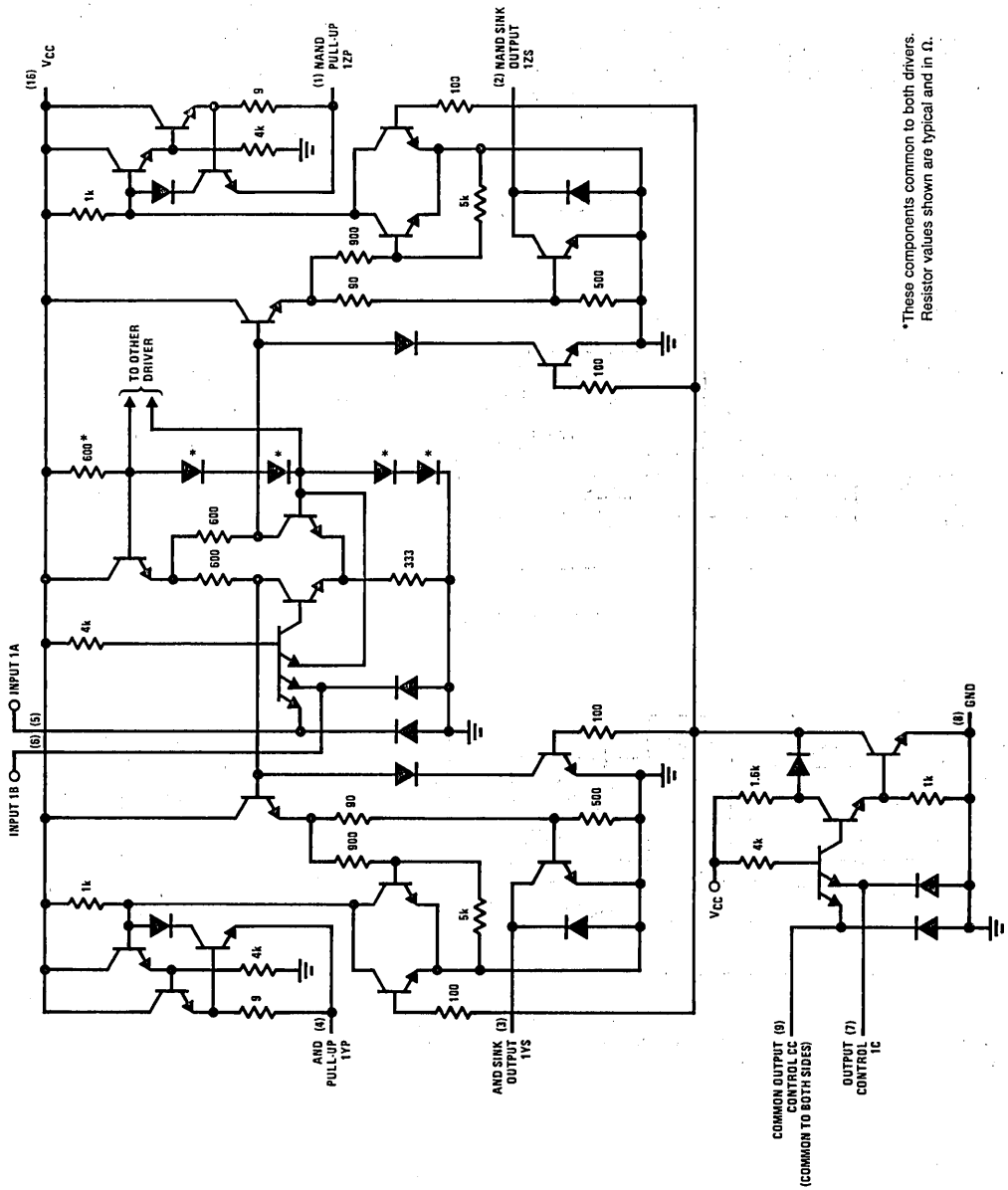
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

Symbol	Parameter	Conditions	DS55113			DS75113			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to High-Level Output	*(Figure 1)*		13	20		13	30	ns
t_{PHL}	Propagation Delay Time, High-to Low-Level Output			12	20		12	30	ns
t_{PZH}	Output Enable Time to High Level	R_L = 180Ω, *(Figure 2)*		7	15		7	20	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 250Ω, *(Figure 3)*		14	30		14	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 180Ω, *(Figure 2)*		10	20		10	30	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 250Ω, *(Figure 3)*		17	35		17	35	ns

Schematic Diagram (One side shown only)



AC Test Circuits and Switching Time Waveforms

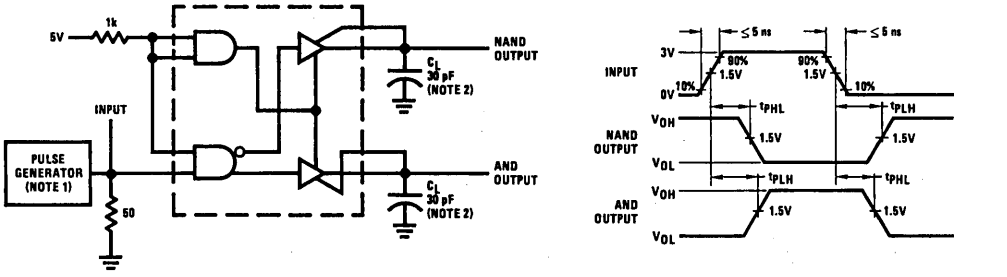


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FIGURE 1. t_{PLH} and t_{PHL}

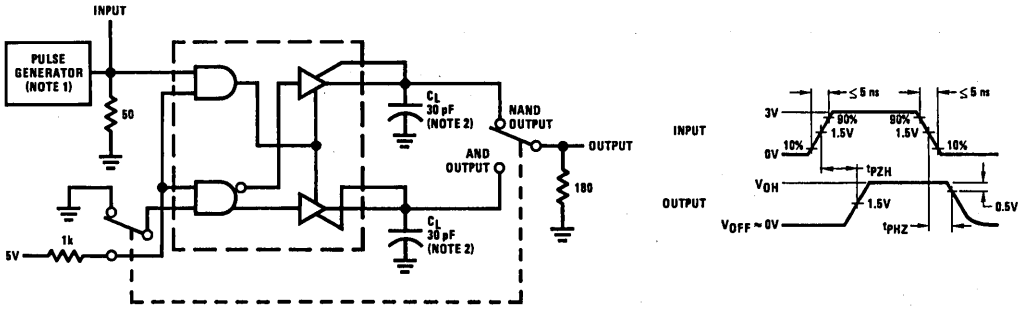

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FIGURE 2. t_{PZH} and t_{PHZ}

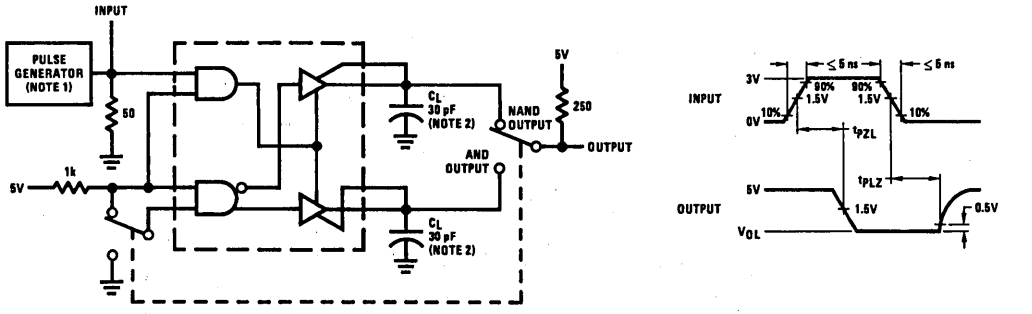

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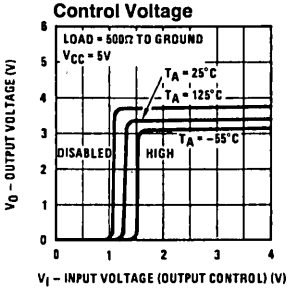
FIGURE 3. t_{PZL} and t_{PLZ}

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 500 kHz, t_W = 100 ns.

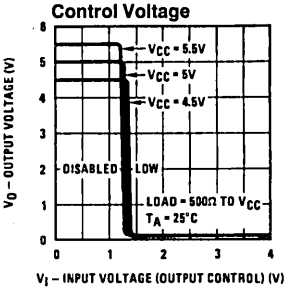
Note 2: C_L includes probe and jig capacitance.

Typical Performance Characteristics*

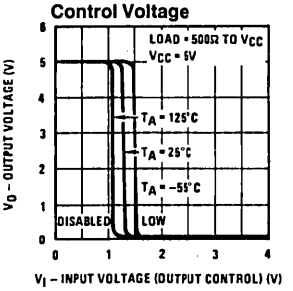
Output Voltage vs Output Control Voltage



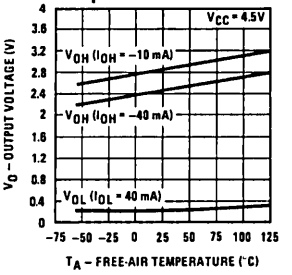
Output Voltage vs Output Control Voltage



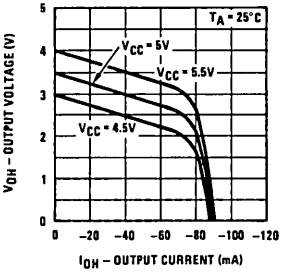
Output Voltage vs Output Control Voltage



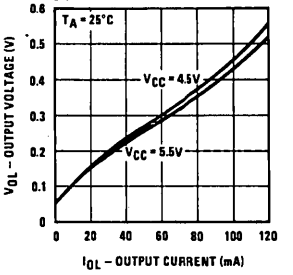
Output Voltage vs Free-Air Temperature



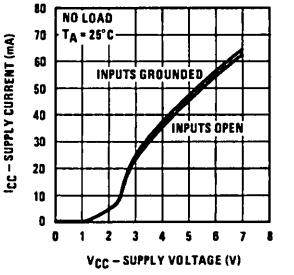
High Level Output Voltage vs Output Current



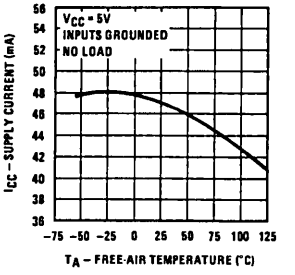
Low Level Output Voltage vs Output Current



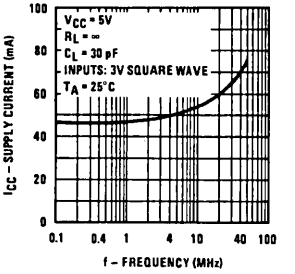
Supply Current (Both Drivers) vs Supply Voltage



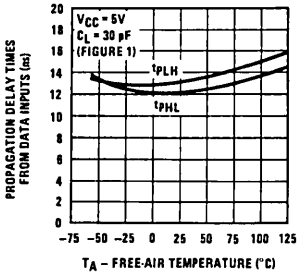
Supply Current (Both Drivers) vs Free-Air Temperature



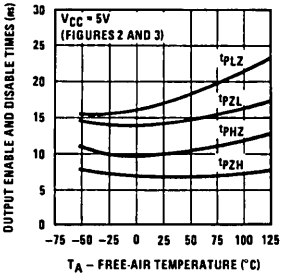
Supply Current (Both Drivers) vs Frequency



Propagation Delay Times from Data Inputs vs Free-Air Temperature



Output Enable and Disable Times vs Free-Air Temperature



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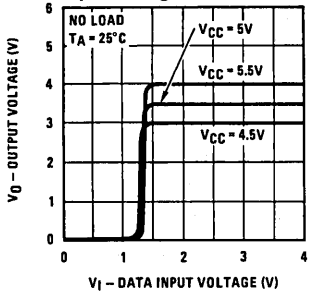
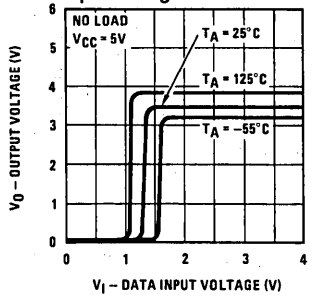
*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Typical Performance Characteristics* (Continued)

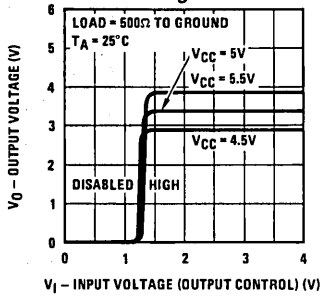
Output Voltage vs Data Input Voltage



Output Voltage vs Data Input Voltage



Output Voltage vs Output Control Voltage



TL/F/5785–6

*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

National Semiconductor

DS55114/DS75114 Dual Differential Line Drivers

General Description

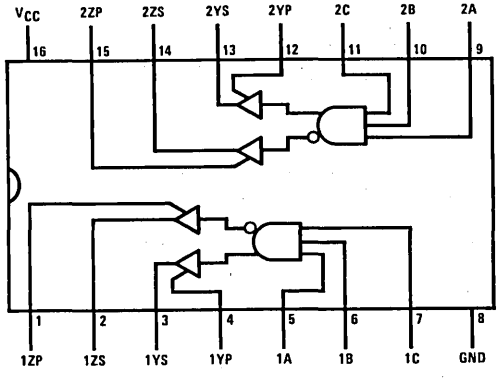
The DS55114/DS75114 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair at normal line impedances, without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL compatible output levels, these devices may also be used as TTL expanders or phase splitters.

Features

- Each circuit offers a choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- Designed to be interchangeable with Fairchild 9614 line drivers
- Short-circuit protection of outputs
- High current outputs
- Clamp diodes at inputs and outputs to terminate line transients
- Single-ended or differential AND/NAND outputs
- Triple inputs

Connection Diagram

Dual-In-Line Package



TL/F/5786–1

Top View

Positive logic: $Y = ABC$

$Z = \overline{ABC}$

Order Number DS75114N
See NS Package Number N16A

*Contact Product Marketing

Truth Table

Inputs			Outputs	
A	B	C	Y	Z
H	H	H	H	L
All Other Input Combinations			L	H

H = high level

L = low level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Free-Air Temperature Range	
DS55114	−55°C to +125°C
DS75114	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature ($1/16$" from case for 60 seconds): J Package	300°C
Lead Temperature ($1/16$" from case for 4 seconds): N Package	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C (Note 2).

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS55114	4.5	5.5	V
DS75114	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55114	−55	125	°C
DS75114	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)			DS55114 Min	DS55114 Typ (Note 4)	DS55114 Max	DS75114 Min	DS75114 Typ (Note 4)	DS75114 Max	Units
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	V
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
		V_{IL} = 0.8V		I_{OH} = −40 mA	2	3.0		2	3.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.2	0.4		0.2	0.45	V
V_{OK}	Output Clamp Voltage	V_{CC} = 5V, I_O = 40 mA, T_A = 25°C				6.1	6.5		6.1	6.5	V
		V_{CC} = Max, I_O = −40 mA, T_A = 25°C				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	OFF-State Open-Collector Output Current	V_{CC} = Max	V_{OH} = 12V	T_A = 25°		1	100				μA
				T_A = 125°C			200				μA
			V_{OH} = 5.25V	T_A = 25°C					1	100	μA
				T_A = 70°C						200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V					1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0V			−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	Inputs Grounded, No Load, T_A = 25°C		V_{CC} = Max		37	50		37	50	mA
				V_{CC} = 7V		47	65		47	70	mA

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section.

Note 3: All parameters, with the exception of OFF-state open-collector output current, are measured with the active pull-up connected to the sink output.

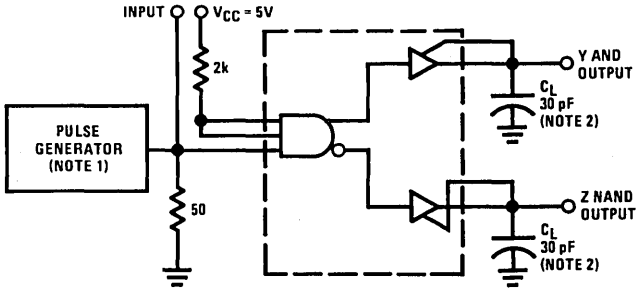
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	DS55114			DS75114			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 30 pF, *(Figure 1)*		15	20		15	30	ns
t_{PHL}	Propagation Delay Time High-to-Low-Level Output			11	20		11	30	ns

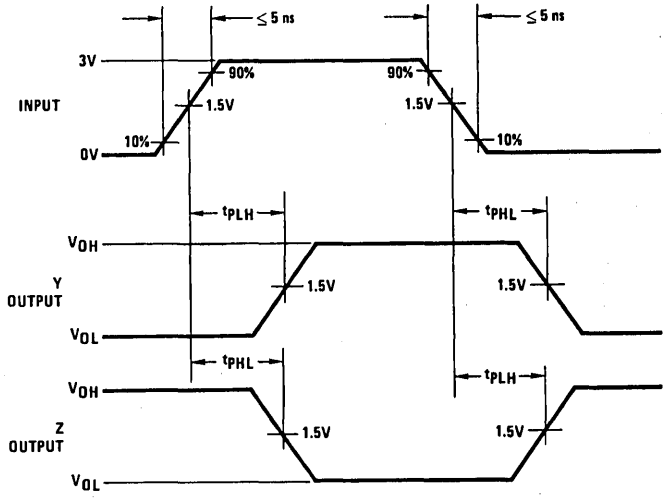
AC Test Circuit and Switching Time Waveforms



TL/F/5786–3

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, t_w = 100 ns, PRR = 500 kHz.

Note 2: C_L includes probe and jig-capacitance.

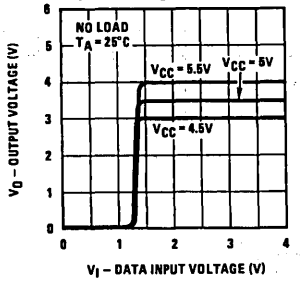


TL/F/5786–4

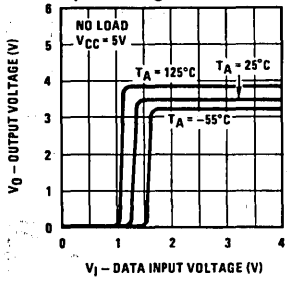
FIGURE 1

Typical Performance Characteristics*

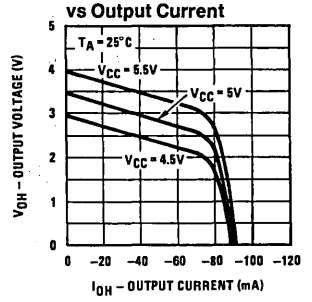
Output Voltage vs Data Input Voltage



Output Voltage vs Data Input Voltage



High Level Output Voltage vs Output Current



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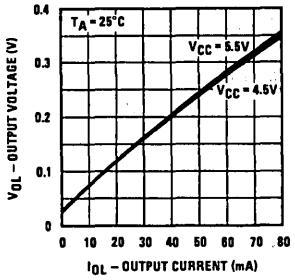
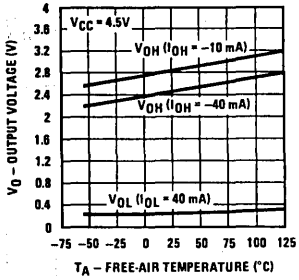
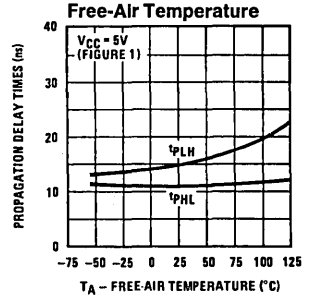
Low Level Output Voltage vs Output Current



Output Voltage vs Free-Air Temperature

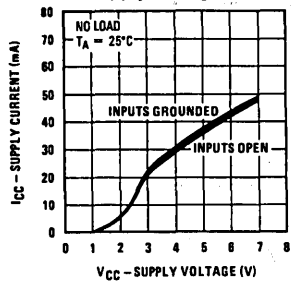


Propagation Delay Times vs Free-Air Temperature

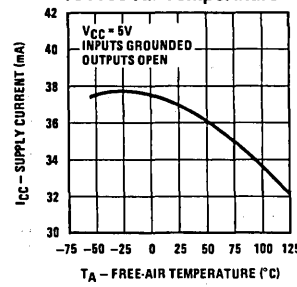


TL/F/5786–6

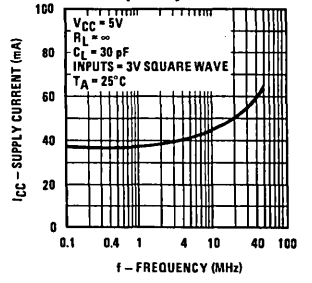
Supply Current (Both Drivers) vs Supply Voltage



Supply Current (Both Drivers) vs Free-Air Temperature



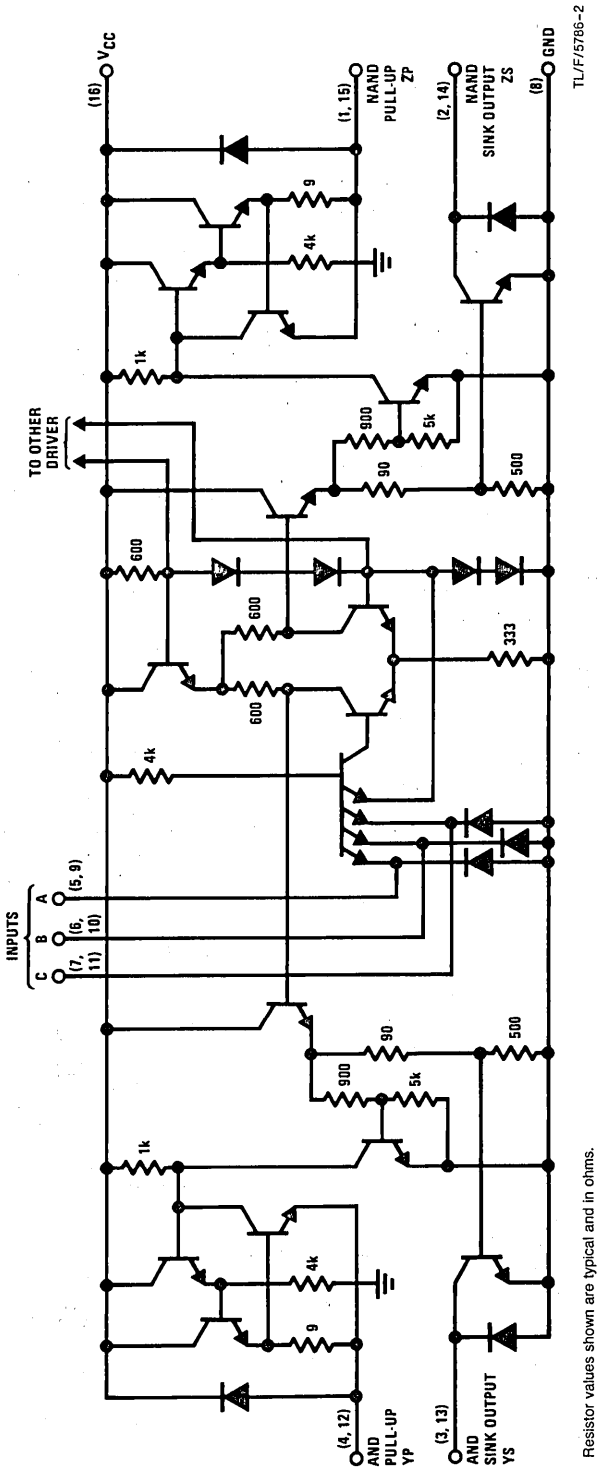
Supply Current (Both Drivers) vs Frequency



TL/F/5786–7

*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Schematic Diagram (Each Driver)



TL/F/5786–2

Resistor values shown are typical and in ohms.

National Semiconductor

DS75121 Dual Line Drivers

General Description

The DS75121 is a monolithic dual line driver designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines having impedances from 50Ω to 500Ω. It is compatible with standard TTL logic and supply voltage levels.

The DS75121 will drive terminated low impedance lines due to the low-impedance emitter-follower outputs. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

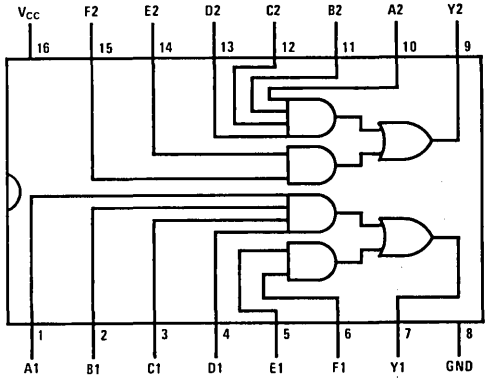
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Designed for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or twisted pair transmission lines
- TTL compatible
- Open emitter-follower output structure for party-line operation
- Short-circuit protection
- AND-OR logic configuration
- High speed (max propagation delay time 20 ns)
- Plug-in replacement for the SN75121 and the 8T13

Connection Diagram

Dual-In-Line Package

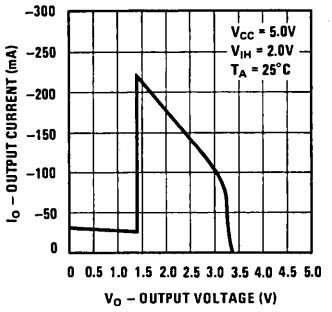


TL/F/5788–1

Top View
Order Number DS75121N
See NS Package Number N16A

Typical Performance Characteristics

Output Current vs Output Voltage



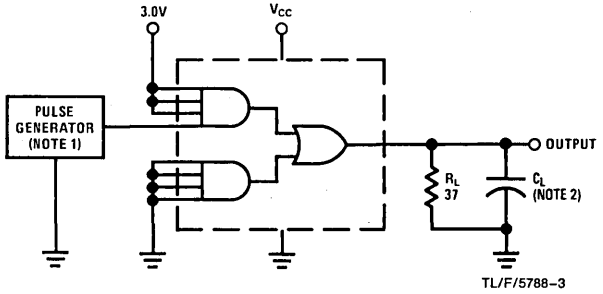
TL/F/5788–2

Truth Table

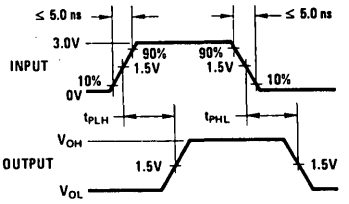
Inputs						Output
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = High Level, L = Low Level, X = Irrelevant

AC Test Circuit and Switching Time Waveforms



TL/F/5788–3



TL/F/5788–4

Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%, $t_r = t_f = 5.0$ ns.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	6.0V
Input Voltage	6.0V
Output Voltage	6.0V
Output Current	−75 mA
Maximum Power Dissipation* at 25°C Molded Package	1280 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A			
DS75121	0	+75	°C

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
V_{OH}	High Level Output Voltage	V_{IH} = 2.0V, I_{OH} = −75 mA (Note 4)	2.4			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.75V, V_{OH} = 2.0V, T_A = 25°C (Note 4)	−100		−250	mA
I_{OL}	Low Level Output Current	V_{IL} = 0.8V, V_{OL} = 0.4V (Note 4)			−800	μA
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0V, V_O = 3.0V			500	μA
I_{IH}	High Level Input Current	V_I = 4.5V			40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C			−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open			28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open			60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 37Ω, (See AC Test Circuit and Switching Time Waveforms)	C_L = 15 pF		11	20	ns
			C_L = 1000 pF		22	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 37Ω, (See AC Test Circuit and Switching Time Waveforms)	C_L = 15 pF		8.0	20	ns
			C_L = 1000 pF		20	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75121. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

DS75123 Dual Line Driver

General Description

The DS75123 is a monolithic dual line driver designed specifically to meet the I/O interface specifications for IBM System 360. It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the DS75123 enable driving terminated low impedance lines. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

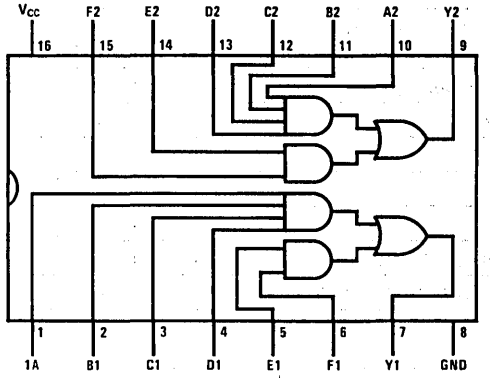
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Meet IBM System 360 I/O interface specifications for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or terminated pair transmission lines
- TTL compatible with single 5.0V supply
- 3.11V output at I_{OH} = −59.3 mA
- Open emitter-follower output structure for party-line operation
- Short circuit protection
- AND-OR logic configuration
- Plug-in replacement for the SN75123 and the 8T23

Connection Diagram

Dual-In-Line Package



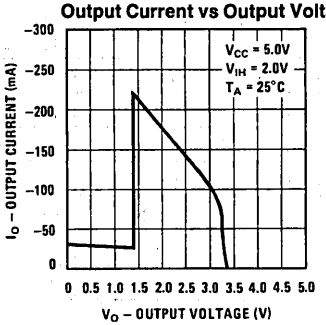
TL/F/5790-1

Top View

Order Number DS75123N
See NS Package Number N16A

Typical Performance Characteristics

Output Current vs Output Voltage



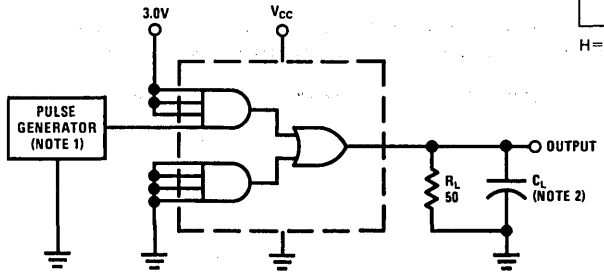
TL/F/5790-3

Truth Table

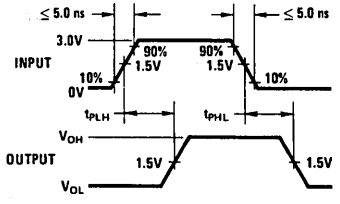
INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = High level, L = Low level, X = Irrelevant

AC Test Circuit and Switching Time Waveforms



TL/F/5790-2



TL/F/5790-4

Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	7.0V
Maximum Power Dissipation* at 25°C	
Molded Package	1280 mW
Operating Free-Air Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−100	mA
Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA				−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V				1	mA
V_{OH}	High Level Output Voltage	V_{CC} = 5.0V, V_{IH} = 2.0V, I_{OH} = −59.3 mA, (Note 4)	T_A = 25°C	3.11			V
			T_A = 0°C to +75°C	2.9			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.5V, T_A = 25°C, V_{OH} = 2.0V, (Note 4)		−100		−250	mA
V_{OL}	Low Level Output Voltage	V_{IL} = 0.8V, I_{OL} = −240 μA, (Note 4)				0.15	V
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0, V_O = 3.0V				40	μA
I_{IH}	High Level Input Current	V_I = 4.5V				40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C				−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open				28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open				60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 50Ω, (See AC Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 50Ω, (See AC Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75123, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

DS7830/DS8830 Dual Differential Line Driver

General Description

The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

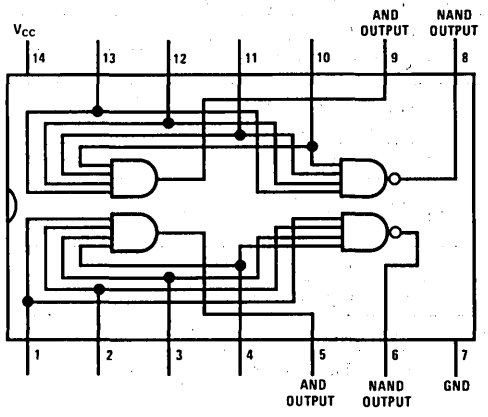
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Features

- Single 5V power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High speed
- Short circuit protection

Connection Diagram

Dual-In-Line and Flat Package



TL/F/5799-2

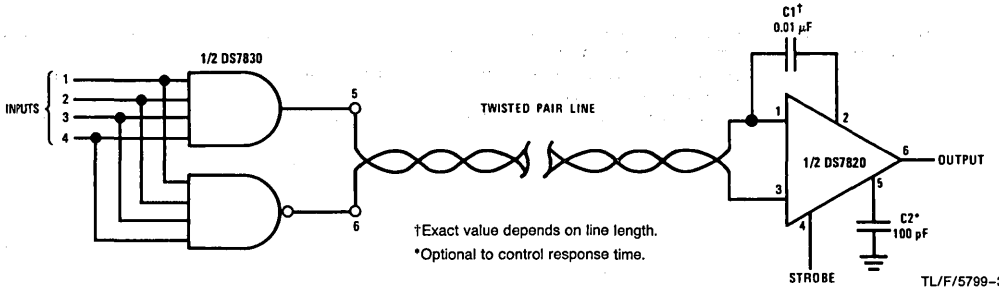
Top View

Order Number DS8830N
See NS Package Number N14A

For Complete Military 883 Specificatons, See RETS Data Sheet.
Order Number DS7830J/883 or DS7830W/883
See NS Package Number J14A

Typical Application

Digital Data Transmission



†Exact value depends on line length.
*Optional to control response time.

TL/F/5799-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Output Short Circuit Duration (125°C)	1 second
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS8730	4.5	5.5	V
DS8830	4.75	5.25	V
Temperature (T_A)			
DS7830	−55	+125	°C
DS8830	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V	I_{OUT} = −0.8 mA	2.4			V
			I_{OUT} = 40 mA	1.8	3.3		V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	I_{OUT} = 32 mA		0.2	0.4	V
			I_{OUT} = 40 mA		0.22	0.5	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				120	μA
		V_{IN} = 5.5V				2	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−4.8	mA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0V, T_A = 125°C, (Note 4)		−40	−100	−120	mA
I_{CC}	Supply Current	V_{IN} = 5.0V, (Each Driver)			11	18	mA
V_I	Input Clamp	V_{CC} = Min, I_{IN} = −12 mA			−1.0	−1.5	V

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay AND Gate	R_L = 400Ω, C_L = 15 pF *(Figure 1)*		8	12	ns
t_{pd0}				11	18	ns
t_{pd1}	Propagation Delay NAND Gate	R_L = 400Ω, C_L = 15 pF *(Figure 1)*		8	12	ns
t_{pd0}				5	8	ns
t_1	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns
t_2	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns

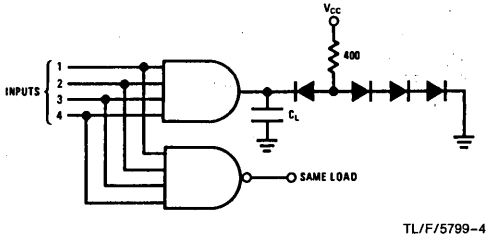
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7830 and across the 0°C to +70°C range for the DS8830. Typical values for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms



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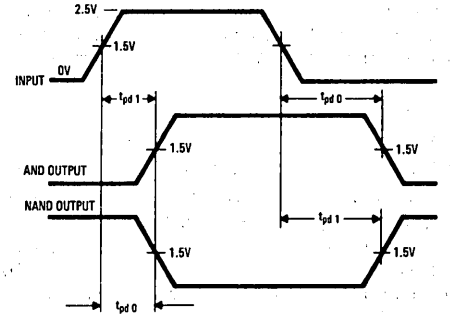
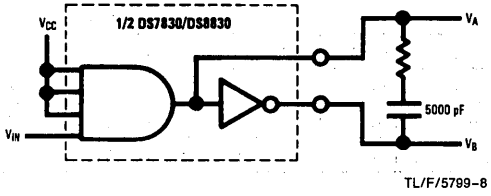


$f = 1$ MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
Duty cycle = 50%

TL/F/5799-9

FIGURE 1



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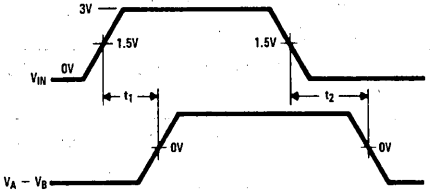

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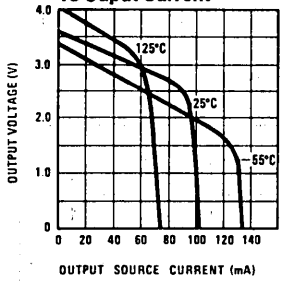
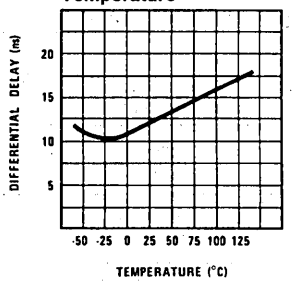
FIGURE 2

Typical Performance Characteristics

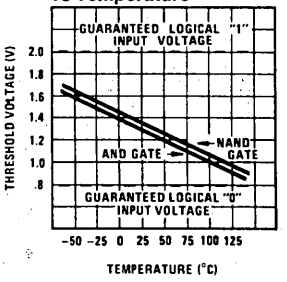
Output High Voltage (Logical "1") vs Ouput Current



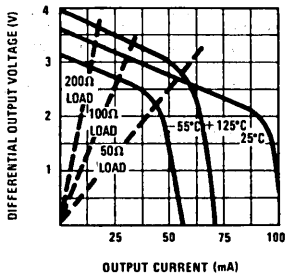
Differential Delay vs Temperature



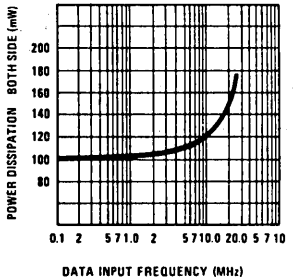
Threshold Voltage vs Temperature



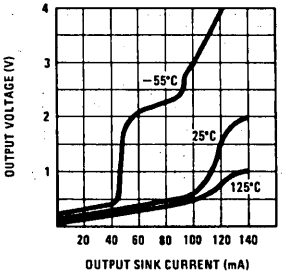
Differential Output Voltage ($|V_{AND} - V_{NAND}|$) vs Differential Output Current



Power Dissipation (No Load) vs Data Input Frequency



Output Low Voltage (Logical "0") vs Output Current



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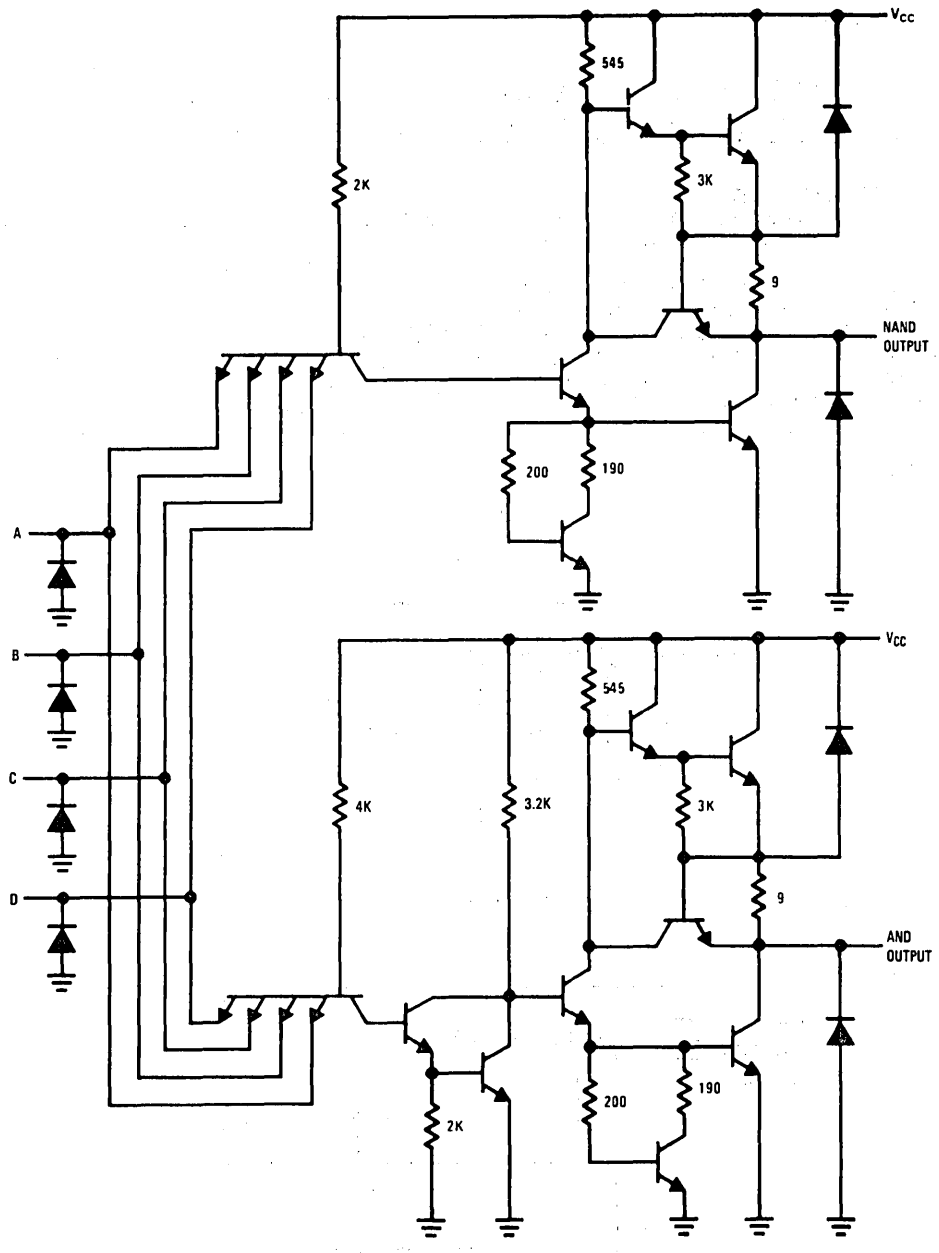
Schematic Diagram



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*2 Per Package

National Semiconductor

MM78C29/MM88C29 Quad Single-Ended Line Driver
MM78C30/MM88C30 Dual Differential Line Driver

General Description

The MM78C30/MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry of the MM78C30/MM88C30 allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM78C30 line driver. The differential output of the MM78C30/MM88C30 eliminates ground-loop errors.

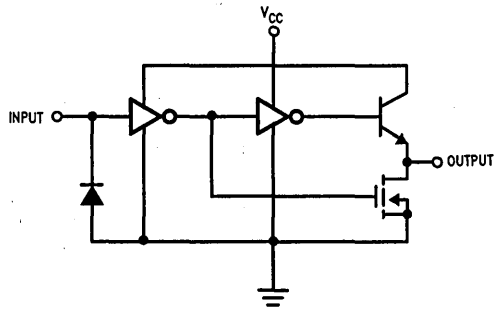
The MM78C29/MM88C29 is a non-inverting single-wire transmission line driver. Since the output ON resistance is a low 20Ω typ., the device can be used to drive lamps, relays, solenoids, and clock lines, besides driving data lines.

Features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low output ON resistance	20Ω (typ.)

Logic Diagrams

1/4 MM78C29/MM88C29



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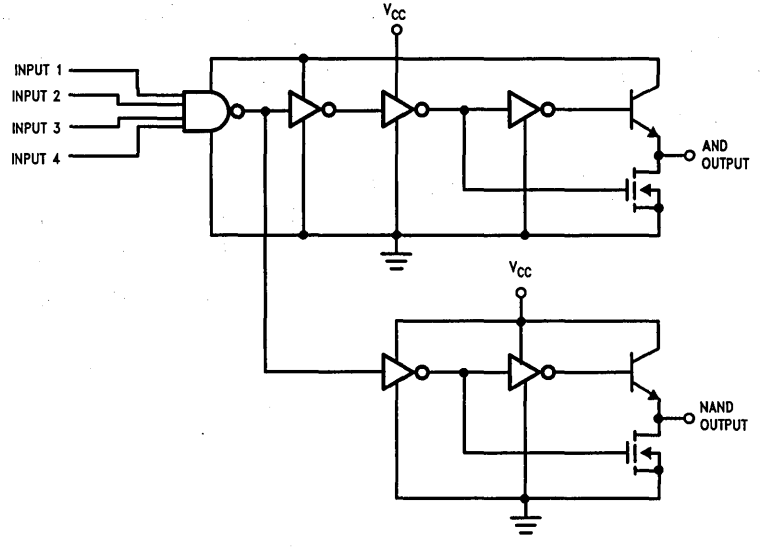
1/2 MM78C30/MM88C30



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC} + 16V$
Operating Temperature Range	
MM78C29/MM78C30	$-55°C$ to $+125°C$
MM88C29/MM88C30	$-40°C$ to $+85°C$
Storage Temperature	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Average Current at Output	
MM78C30/MM88C30	50 mA
MM78C29/MM88C29	25 mA
Maximum Junction Temperature, T_j	150°C
Lead Temperature	
(Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	−1	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 5V$		0.05	100	mA
OUTPUT DRIVE						
I_{SOURCE}	Output Source Current MM78C29/MM78C30	$V_{OUT} = V_{CC} - 1.6V$, $V_{CC} \geq 4.5V$, $T_j = 25°C$ $T_j = 125°C$	 −57 −32	 −80 −50		 mA mA
	MM88C29/MM88C30	$V_{OUT} = V_{CC} - 1.6V$, $V_{CC} \geq 4.75V$, $T_j = 25°C$ $T_j = 85°C$	 −47 −32	 −80 −60		 mA mA
	MM78C29/MM88C29 MM78C30/MM88C30	$V_{OUT} = V_{CC} - 0.8V$ $V_{CC} \geq 4.5V$	−2	−20		mA
I_{SINK}	Output Sink Current MM78C29/MM78C30	$V_{OUT} = 0.4V$, $V_{CC} = 4.5V$, $T_j = 25°C$ $T_j = 125°C$	 11 8	 20 14		 mA mA
		$V_{OUT} = 0.4V$, $V_{CC} = 10V$, $T_j = 25°C$ $T_j = 125°C$	 22 16	 40 28		 mA mA
	MM88C29/MM88C30	$V_{OUT} = 0.4V$, $V_{CC} = 4.75V$, $T_j = 25°C$ $T_j = 85°C$	 9.5 8	 22 18		 mA mA
		$V_{OUT} = 0.4V$, $V_{CC} = 10V$, $T_j = 25°C$ $T_j = 125°C$	 19 15.5	 40 33		 mA mA
I_{SOURCE}	Output Source Resistance MM78C29/MM78C30	$V_{OUT} = V_{CC} - 1.6V$, $V_{CC} \geq 4.5V$, $T_j = 25°C$ $T_j = 125°C$		 20 32	 28 50	 Ω Ω
	MM88C29/MM88C30	$V_{OUT} = V_{CC} - 1.6V$, $V_{CC} \geq 4.75V$, $T_j = 25°C$ $T_j = 85°C$		 20 27	 34 50	 Ω Ω

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DC Electrical Characteristics

Min/Max limits apply across temperature range, unless otherwise noted (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (Continued)						
I_{SINK}	Output Sink Resistance					
	MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.50V,				
		T_j = 25°C		20	36	Ω
		T_j = 125°C		28	50	Ω
		V_{OUT} = 0.4V, V_{CC} = 10V,				
		T_j = 25°C		10	18	Ω
		T_j = 125°C		14	25	Ω
	MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V,				
		T_j = 25°C		18	41	Ω
		T_j = 85°C		22	50	Ω
		V_{OUT} = 0.4V, V_{CC} = 10V,				
		T_j = 25°C		10	21	Ω
		T_j = 85°C		12	26	Ω
	Output Resistance Temperature Coefficient					
	Source			0.55		%/°C
	Sink			0.40		%/°C
θ_{JA}	Thermal Resistance					
	MM78C29/MM78C30 (D-Package)			100		°C/W
	MM88C29/MM88C30 (N-Package)			150		°C/W

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	(See *Figure 2*)				
	MM78C29/MM88C29	V_{CC} = 5V		80	200	ns
		V_{CC} = 10V		35	100	ns
	MM78C30/MM88C30	V_{CC} = 5V		110	350	ns
		V_{CC} = 10V		50	150	ns
t_{pd}	Differential Propagation Delay Time to Logical "1" or "0"	R_L = 100Ω, C_L = 5000 pF (See *Figure 1*)				
	MM78C30/MM88C30	V_{CC} = 5V			400	ns
		V_{CC} = 10V			150	ns
C_{IN}	Input Capacitance					
	MM78C29/MM88C29	(Note 3)		5.0		pF
	MM78C30/MM88C30	(Note 3)		5.0		pF
C_{PD}	Power Dissipation Capacitance					
	MM78C29/MM88C29	(Note 3)		150		pF
	MM78C30/MM88C30	(Note 3)		200		pF

*AC Parameters are guaranteed by DC correlated testing.

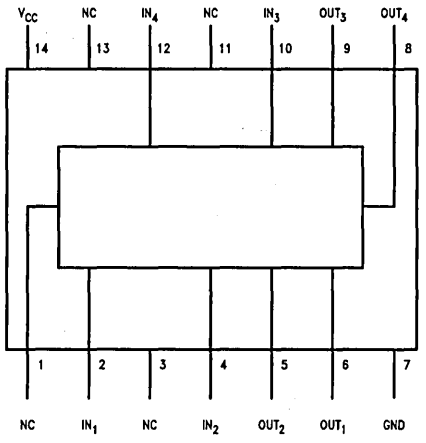
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90 (CMOS Logic Databook).

Connection Diagrams

Dual-In-Line Package
MM78C29/MM88C29



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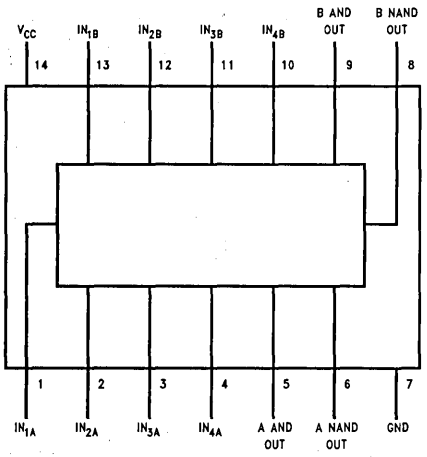
Top View

Order Number MM88C29M or MM88C29N

Dual-In-Line Package
MM78C30/MM88C30



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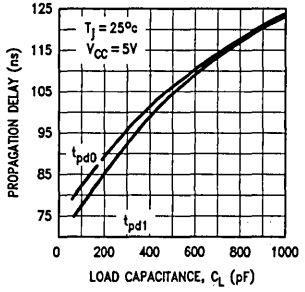
Top View

Order Number MM88C30M or MM88C30N

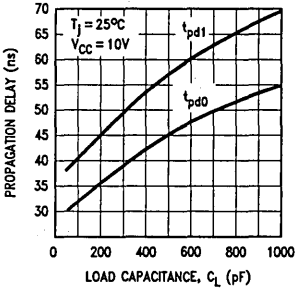
For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number MM78C29J/883, MM78C29W/883, MM78C30J/883 or MM78C30W/883

Typical Performance Characteristics

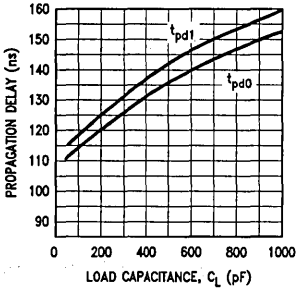
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



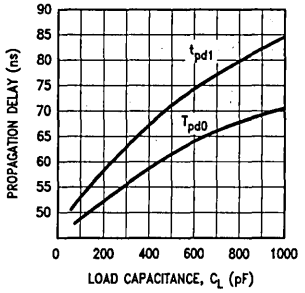
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



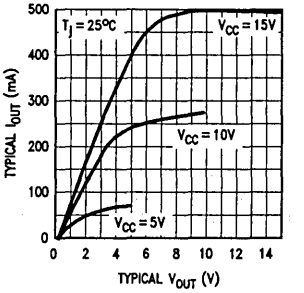
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



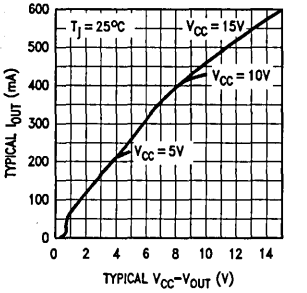
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



Typical Sink Current vs Output Voltage



Typical Source Current vs Output Voltage



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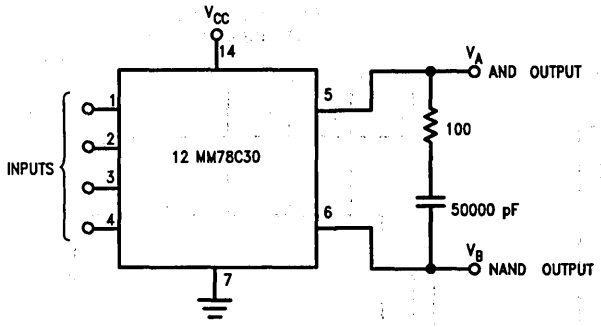
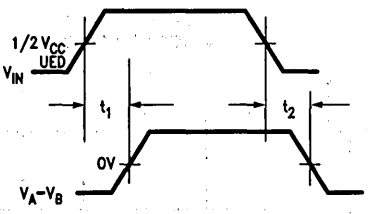
6

AC Test Circuits

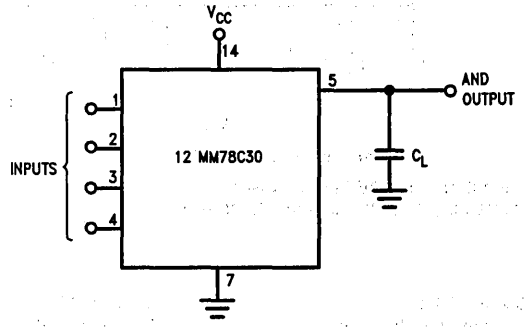




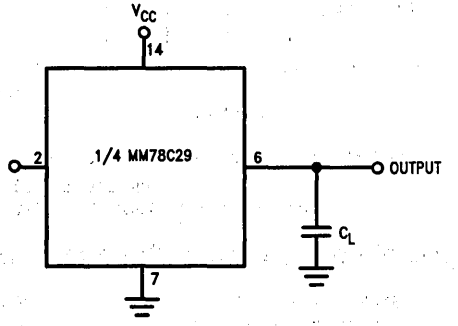
TL/F/5908-7

TL/F/5908-6

FIGURE 1



TL/F/5908-8

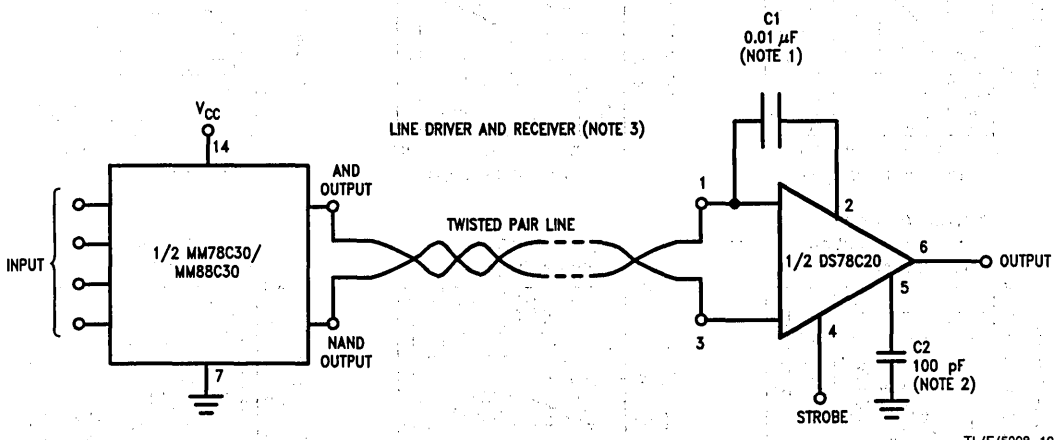


TL/F/5908-9

FIGURE 2

Typical Applications

Digital Data Transmission



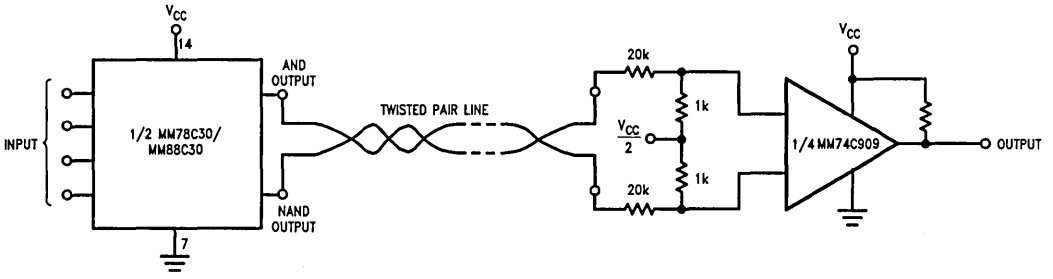
TL/F/5908-10

Note 1: Exact value depends on line length.

Note 2: Optional to control response time.

Note 3: V_{CC} = 4.5V to 5.5V for the DS7820, V_{CC} = 4.5V to 15V for the DS78C20.

Typical Applications (Continued)



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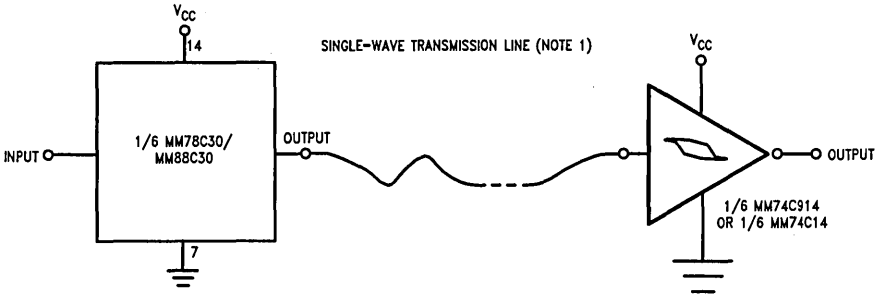

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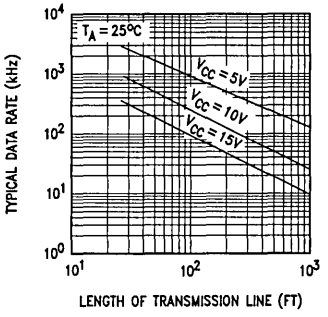
Note 1: V_{CC} is 3V to 15V

Typical Data Rate vs Transmission Line Length



TL/F/5908–13

Note 1: The transmission line used was #22 gauge unshielded twisted pair (40k termination).

Note 2: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.

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National Semiconductor

DS7831/DS8831/DS7832/DS8832
Dual TRI-STATE® Line Driver

General Description

Through simple logic control, the DS7831/DS8831, DS7832/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS7832/DS8832 does not have the V_{CC} clamp diodes found on the DS7831/DS8831.

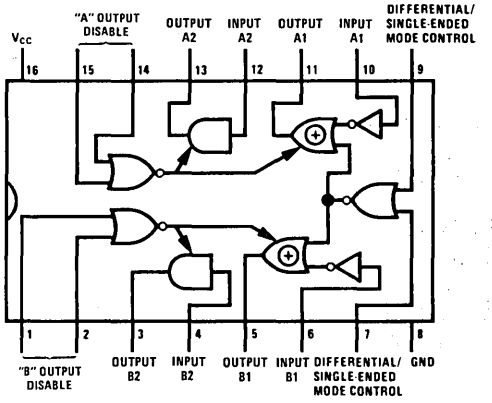
The DS7831 and DS7832 are specified for operation over the −55°C to +125°C military temperature range. The DS8831 and DS8832 are specified for operation over the 0°C to +70°C temperature range.

Features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line

Connection and Logic Diagram

Dual-In-Line Package



TL/F/5800–1

Top View

Order Number DS8831N, DS8832J or DS8832N
See NS Package Number J16A or N16A

For Complete Military 883 Specificatons,
See RETS Data Sheet.
Order Number DS7831J/883, DS7831W/883,
DS7832J/883 or DS7832W/883
See NS Package Number J16A or W16A

Truth Table (Shown for A Channels Only)

"A" Output Disable		Differential/ Single-Ended Mode Control		Input A1	Output A1	Input A2	Output A2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A1	Logical "1" or Logical "0"	Same as Input A2
0	0	X 1	1 X	Logical "1" or Logical "0"	Opposite of Input A1	Logical "1" or Logical "0"	Same as Input A2
1 X	X 1	X	X	X	High Impedance State	X	High Impedance State

X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7831/DS7832	4.5	5.5	V
DS8831/DS8832	4.75	5.25	V
Temperature (T_A)			
DS7831/DS7832	−55	+125	°C
DS8831/DS8832	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min					0.8	V
V_{OH}	Logical "1" Output Voltage	DS7831/DS7832	V_{CC} = Min	I_O = −40 mA	1.8	2.3		V
				I_O = −2 mA	2.4	2.7		V
		DS8831/DS8832		I_O = −40 mA	1.8	2.5		V
				I_O = −5.2 mA	2.4	2.9		V
V_{OL}	Logical "0" Output Voltage	DS7831/DS7832	V_{CC} = Min	I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
		DS8831/DS8832		I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	DS7831/DS7832, V_{IN} = 5.5V				1	mA
			DS8831/DS8832, V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{OD}	Output Disable Current	V_{CC} = Max, V_O = 2.4V or 0.4V			−40		40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−100	−120	mA
I_{CC}	Supply Current	V_{CC} = Max in TRI-STATE				65	90	mA
V_{CLI}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA					−1.5	V
V_{CLO}	Output Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA	DS7831/DS8831 DS7832/DS8832			−1.5	V
			I_{OUT} = 12 mA	DS7831/DS8831			V_{CC} + 1.5	V

Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs	(See *Figures 4* and *5*)		13	25	ns
t_{pd1}	Propagation Delay to a Logical "1" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs			13	25	ns
t_{1H}	Delay from Disable Inputs to High Impedance State (from Logical "1" Level)			6	12	ns
t_{0H}	Delay from Disable Inputs to High Impedance State (from Logical "0" Level)			14	22	ns
t_{H1}	Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State)			14	22	ns
t_{H0}	Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State)			18	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7831 and DS7832 and across the 0°C to +70°C range for the DS8831 and DS8832. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies for $T_A = 125°C$ only. Only one output should be shorted at a time.

Mode of Operation

To operate as a quad single-ended line driver apply logical "0"s to the output disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

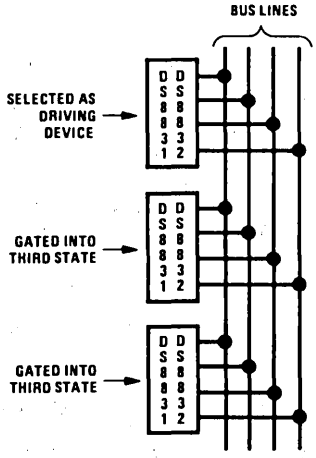
To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs.

The inputs to the A channels should be connected together and the inputs to the B channels should be connected together.

In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

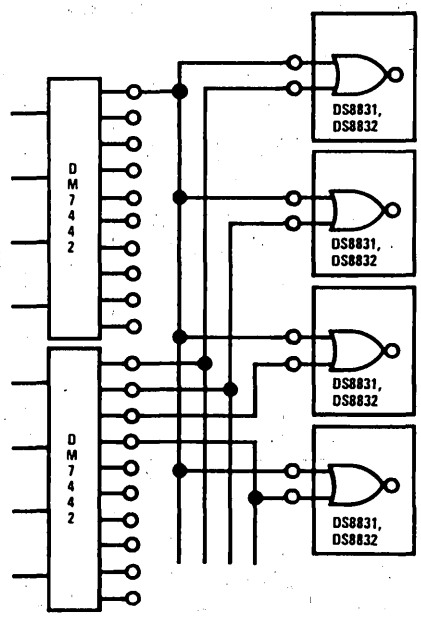
When operating in a bus-organized system with outputs tied directly to outputs of other DS7831/DS8831's, DS7832/DS8832's *(Figure 1)*, all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DS7831/DS8831's, DS7832/DS8832's *(Figure 2)*.

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DS7831/DS8831's, DS7832/DS8832's and still have available drive for the bus line *(Figure 3)*.



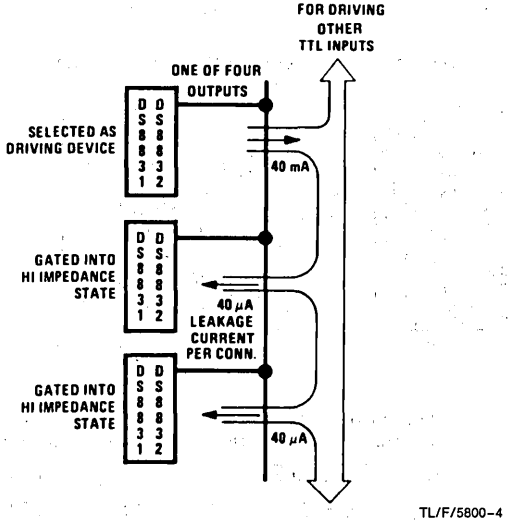
TL/F/5800–2

FIGURE 1



TL/F/5800–3

FIGURE 2

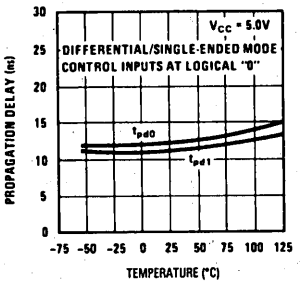


TL/F/5800–4

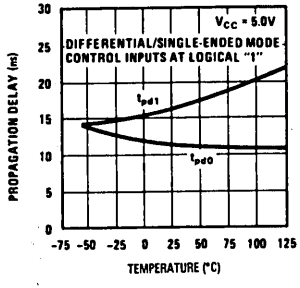
FIGURE 3

Typical Performance Characteristics

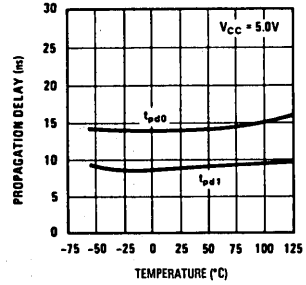
Propagation Delay from Input to Output (Channel 1)



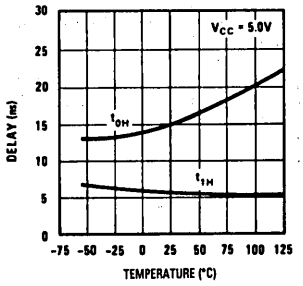
Propagation Delay from Input to Output (Channel 1)



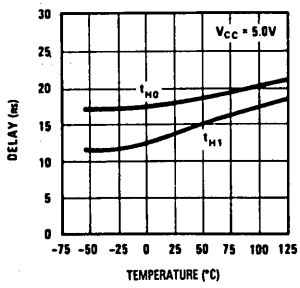
Propagation Delay from Input to Output (Channel 2)



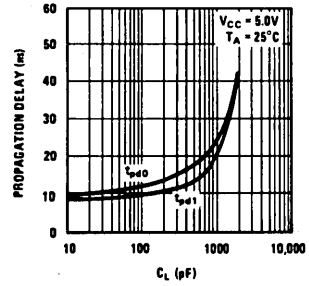
Delay from Disable to High Impedance State



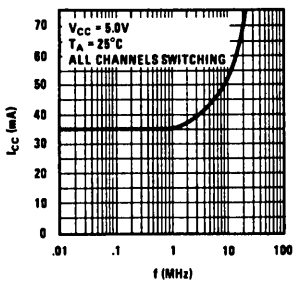
Delay from Disable to Low Impedance State



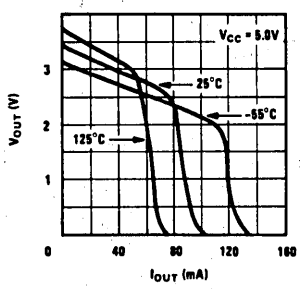
Propagation Delay vs Load Capacitance



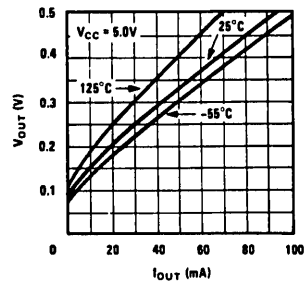
Total Supply Current vs Frequency



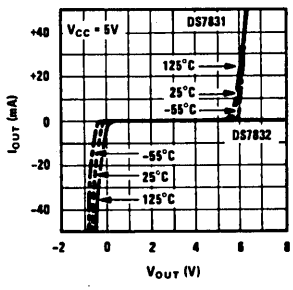
Logical "1" Output Voltage vs Source Current



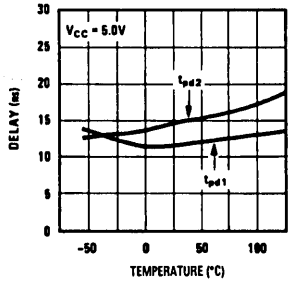
Logical "0" Output Voltage vs Sink Current



I_{OUT} vs V_{OUT} High Impedance Output State



Propagation Delay In Differential Mode



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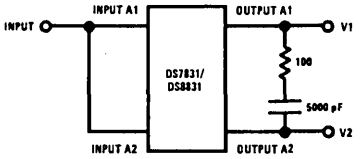
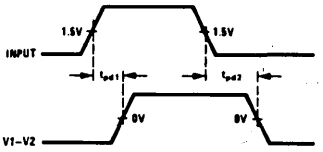
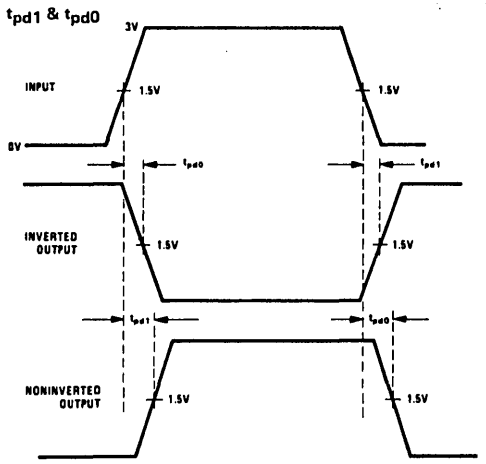
Typical Performance Characteristics (Continued)

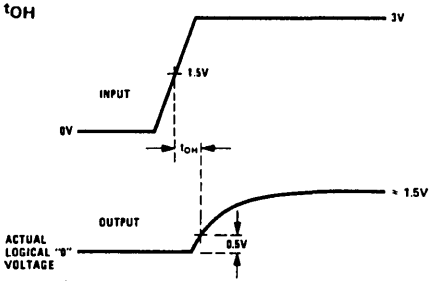


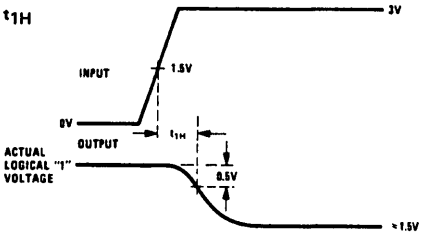


TL/F/5800–6

Switching Time Waveforms

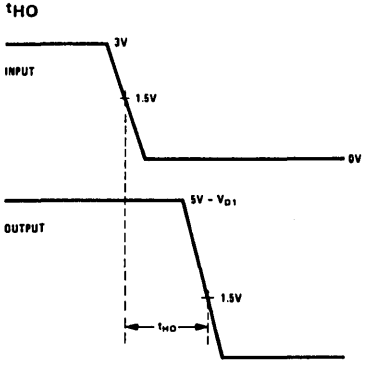


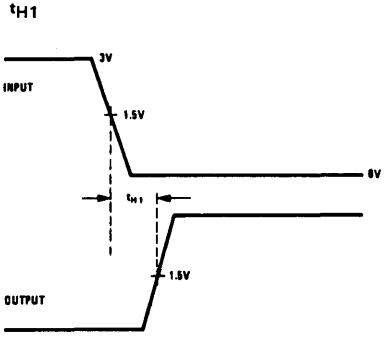




Input characteristic:
Amplitude = 3.0V
Frequency = 1.0 MHz, 50% duty cycle
$t_r = t_f \leq$ ns (10% to 90%)

TL/F/5800–7

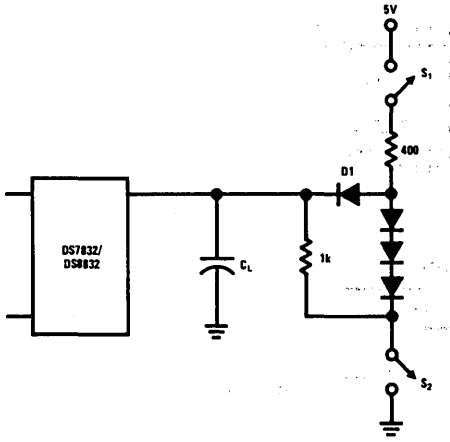




TL/F/5800–8

FIGURE 4

AC Load Circuit



Symbol	Switch S1	Switch S2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{0H}	closed	closed	*5 pF
t_{1H}	closed	closed	*5 pF
t_{H0}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*Jig capacitance

TL/F/5800–9

FIGURE 5

Section 7

General Purpose Receivers

Section 7 Contents

National Semiconductor

DS1603/DS3603 TRI-STATE® Dual Receivers

General Description

The DS1603/DS3603 are dual differential TRI-STATE line receivers designed for a broad range of system applications. They feature a high input impedance and low input current which reduces the loading effects on a digital transmission line, making them ideal for use in party line systems and general purpose applications like transducer preamplifiers, level translators and comparators.

The receivers feature a ±25 mV input sensitivity specified over a ±3V common mode range. Input protection diodes are incorporated in series with the collectors of the differential stage. These diodes are useful in applications that have multiple $V_{CC}+$ supplies or $V_{CC}+$ supplies that are turned off thus avoiding signal clamping. In addition, TTL compatible strobe and control lines are provide for flexibility in the application.

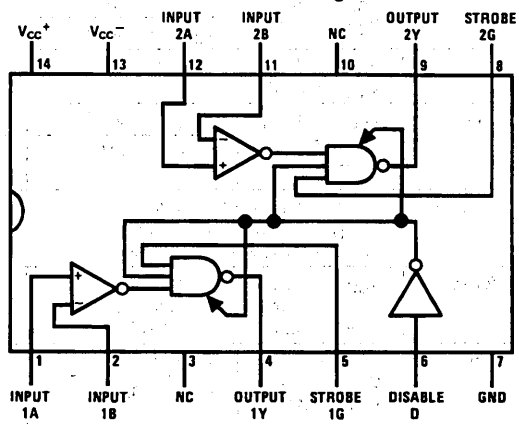
The DS1603/DS3603 are pin compatible with the DS75107, DS75108 and DS75208 series of dual line receivers.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±25 mV input sensitivity
- ±3V input common-mode range
- High-input inpedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- TRI-STATE outputs for high speed buses

Connection Diagram

Dual-In-Line Package



TL/F/5781–2

Top View

Order Number DS3603N
See NS Package Number N14A

For Complete Military 883 Specifications, See RETS Data Sheet.
Order Number: DS1603J/883 or DS1603W/883
See NS Package Number J14A

7

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}^+)	7V
Supply Voltage (V_{CC}^-)	−7V
Differential Input Voltage	±6V
Common Mode Input Voltage	±5V
Strobe Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	DS1603			DS3603		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
Supply Voltage V_{CC}^+	4.5V	5V	5.5V	4.75	5V	5.25V
Supply Voltage V_{CC}^-	−4.5V	−5V	−5.5V	−4.75	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

Electrical Characteristics $T_{MIN} \le T_A \le T_{MAX}$ (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current into 1A, 1B, 2A or 2B	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current into 1A, 1B, 2A or 2B	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current into 1G, 2G or D	V_{CC}^+ = Max, V_{CC}^- = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC}^+			1	mA
I_{IL}	Low Level Input Current into D	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0.4V				−1.6	mA
I_{IL}	Low Level Input Current into 1G or 2G	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(G)}$ = 0.4V	$V_{IH(D)}$ = 2V			−40	μA
			$V_{IL(D)}$ = 0.8V			−1.6	mA
V_{OH}	High Level Output Voltage	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −2 mA, V_{ID} = 25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V				0.4	V
I_{OD}	Output Disable Current	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V	V_{OUT} = 2.4V			40	μA
			V_{OUT} = 0.4V			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0.8V (Note 4)		−18		−70	mA
I_{CCH}^+	High Logic Level Supply Current from V_{CC}^+	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C			28	40	mA
I_{CCH}^-	High Logic Level Supply Current from V_{CC}^-	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or D	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1603 and across the 0°C to +70°C range for the DS3603. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

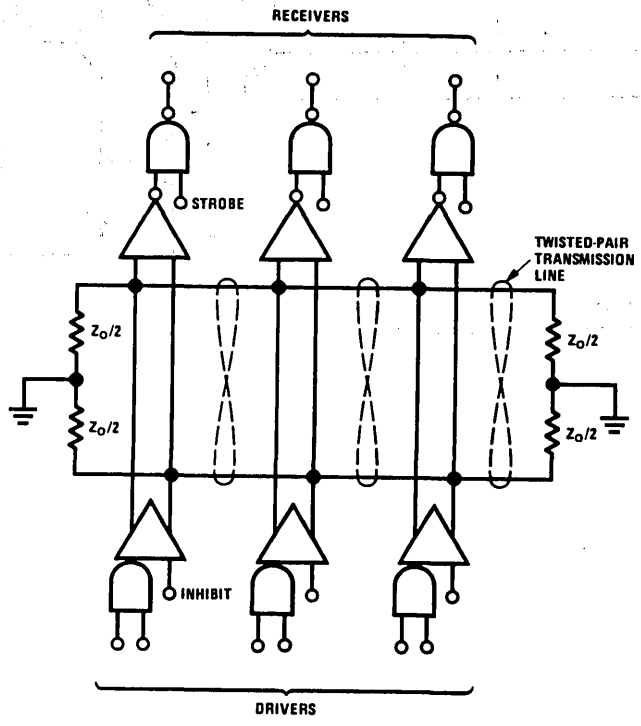
Switching Characteristics $V_{CC}^+ = 5V, V_{CC}^- = -5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, from Differential Inputs A and B to Output	$R_L = 390\Omega, C_L = 50$ pF, (Note 1)		17	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, from Differential Inputs A and B to Output	$R_L = 390\Omega, C_L = 50$ pF, (Note 1)		17	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, from Strobe Input G to Output	$R_L = 390\Omega, C_L = 50$ pF		10	15	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, from Strobe Input G to Output	$R_L = 390\Omega, C_L = 50$ pF		8	15	ns
t_{1H}	Disable Low-to-High to Output High to Off	$R_L = 390\Omega, C_L = 5$ pF			20	ns
t_{0H}	Disable Low-to-High to Output Low to Off	$R_L = 390\Omega, C_L = 5$ pF			30	ns
t_{H1}	Disable High-to-Low to Output Off to High	$R_L = 1k$ to 0V, $C_L = 50$ pF			25	ns
t_{H0}	Disable High-to-Low to Output Off to Low	$R_L = 390\Omega, C_L = 50$ pF			25	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Typical Application

Line Receiver Used in a Party-Line or Data-Bus System



Line receivers are DS75107/DS75108 or DS3603

Line drivers are SN75109/μA75110/DS75110 or DS8831

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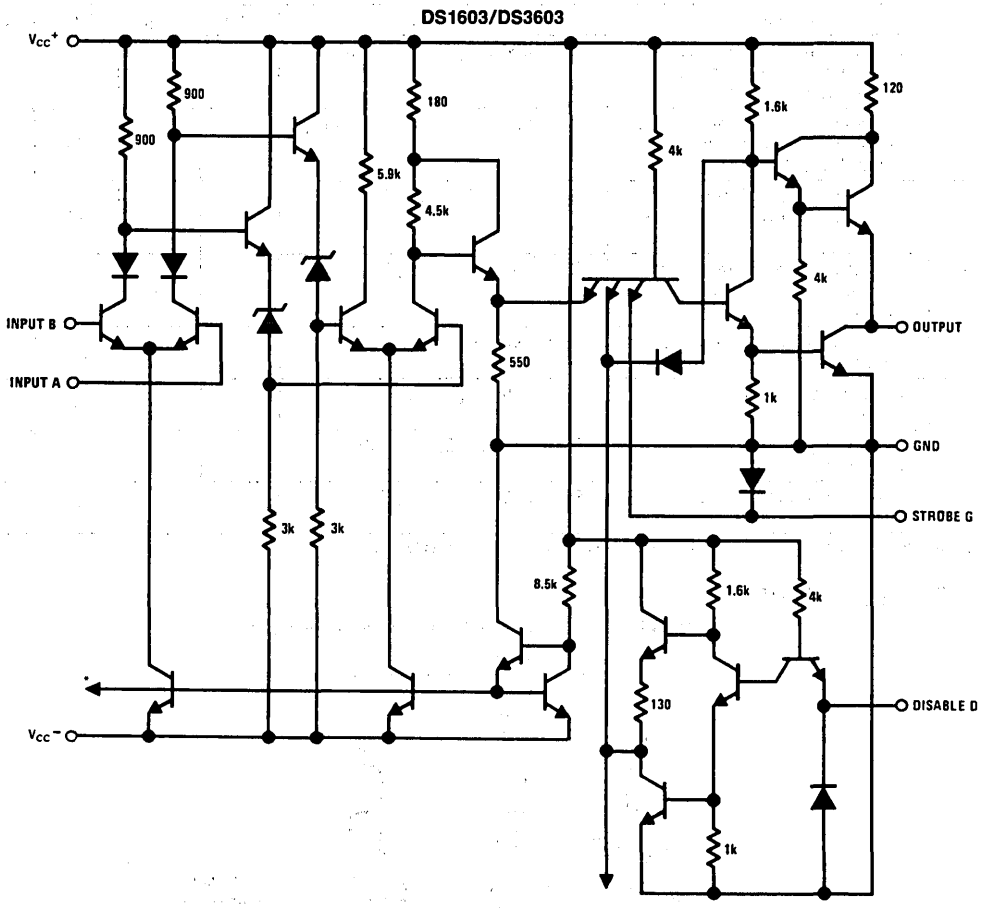
Schematic Diagram (Note 1)



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Note 1: ½ of the dual circuit is shown.

Note 2: *Indicates connections common to second half of dual circuit.

National Semiconductor

DS1652/DS3650/DS3652
Quad Differential Line Receivers

General Description

The DS3650 and DS1652/DS3652 are TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bussed organizations.

The DS3650 has active pull-up outputs and offers a TRI-STATE strobe, while the DS1652/DS3652 offers open collector outputs providing implied "AND" operation.

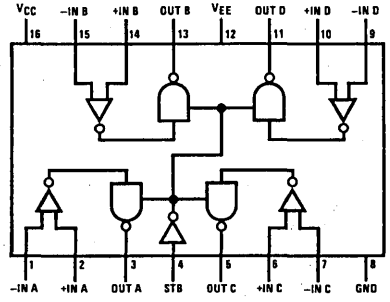
The DS1652/DS3652 can be used for address decoding as illustrated below. All outputs of the DS1652/DS3652 are tied together through a common resistor to 5V. In this configuration, the DS1652/DS3652 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

Features

- High speed
- TTL compatible
- Input sensitivity ±25 mV
- TRI-STATE outputs for high speed busses
- Standard supply voltages ±5V
- Pin and function compatible with MC3450 and MC3452

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS3650M, DS3652M or DS3650N
See NS Package Number M16A or N16A

For Complete Military 883 Specifications, see RETS Data Sheet.

Order Number DS1652J
See NS Package Number J16A

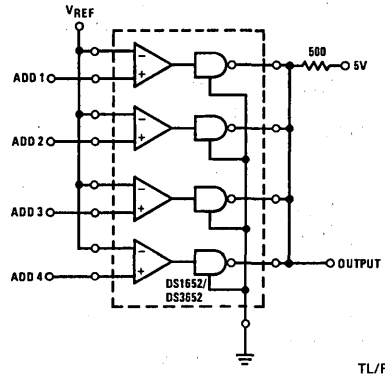
Truth Table

Input	Strobe	Output	
		DS3650	DS1652/ DS3652
$V_D \geq 25$ mV	L	H	Open
	H	Open	Open
-25 mV $\leq V_{ID} \leq 25$ mV	L	X	X
	H	Open	Open
$V_{ID} \leq -25$ mV	L	L	L
	H	Open	Open

L = Low Logic State Open = TRI-STATE
H = High Logic State X = Indeterminate State

Typical Applications

Implied "AND" Gating



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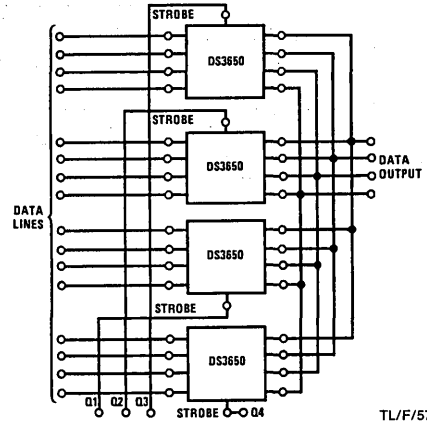
Wired "OR" Data Selecting Using TRI-STATE Logic



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltages	
V_{CC}	+7.0 V_{DC}
V_{EE}	−7.0 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6.0 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5.0 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.8 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1652	4.5	5.5	V_{DC}
DS3650, DS3652	4.75	5.25	V_{DC}
Supply Voltage, V_{EE}			
DS1652	−4.5	−5.5	V_{DC}
DS3650, DS3652	−4.75	−5.25	V_{DC}
Operating Temperature, T_A			
DS1652	−55	+125	°C
DS3650, DS3652	0	+70	°C
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	−3.0	+3.0	V_{DC}
Input Voltage Range Input to GND, V_{IR}	−5.0	+3.0	V_{DC}

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range = −3V ≤ V_{IN} ≤ 3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max				±25.0	mV
$I_{IH(I)}$	High Level Input Current to Receiver Input	*(Figure 5)*				75	µA
$I_{IL(I)}$	Low Level Input Current to Receiver Input	*(Figure 6)*				−10	µA
$I_{IH(S)}$	High Level Input Current to Strobe Input	*(Figure 3)*	$V_{IH(S)}$ = 2.4V, DS1652			100	µA
			$V_{IH(S)}$ = 2.4V, DS3650, DS3652			40	µA
			$V_{IH(S)}$ = V_{CC}			1	mA
$I_{IL(S)}$	Low Level Input Current to Strobe Input		$V_{IH(S)}$ = 0.4V			−1.6	mA
V_{OH}	High Level Output Voltage	*(Figure 1)*	DS3650	2.4			V
I_{CEX}	High Level Output Leakage Current	*(Figure 1)*	DS1652, DS3652			250	µA
V_{OL}	Low Level Output Voltage	*(Figure 1)*	DS3650, DS3652			0.45	V
			DS1652			0.50	
I_{OS}	Short-Circuit Output Current (Note 4)	*(Figure 4)*	DS3650	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	*(Figure 7)*	DS3650			40	µA

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CCH}	High Logic Level Supply Current from V_{CC}	*(Figure 2)*			45	60	mA
I_{EEH}	High Logic Level Supply Current from V_{EE}	*(Figure 2)*			−17	−30	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3650, DS3652 and the −55°C to +125°C range for the DS1652. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

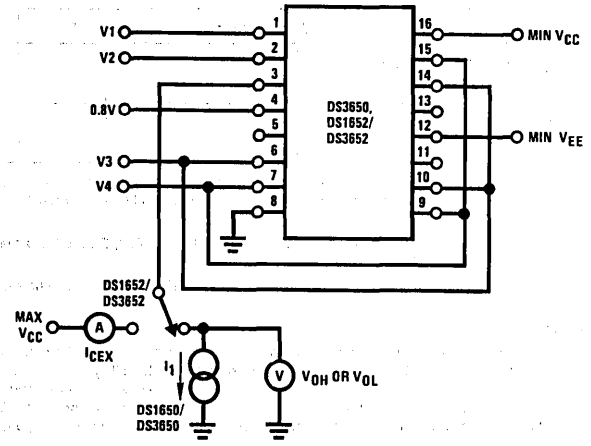
Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with line receivers is, what is the minimum differential input voltage required as the receiver input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1652 and the DS3650, DS3652 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Characteristics (V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	*(Figure 8)*	DS3650		21	25	ns
			DS1652/DS3652		20	25	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)		DS3650		20	25	ns
			DS1652/DS3652		22	25	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 9)*	DS3650		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS3650		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)		DS3650		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS3650		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 10)*	DS1652/DS3652		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)		DS1652/DS3652		13	25	ns

Electrical Characteristic Test Circuits



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	V1		V2		V3		V4		I_1
	DS3650	DS1652/ DS3652	DS3650	DS1652/ DS3652	DS3650	DS1652/ DS3652	DS3650	DS1652/ DS3652	
V_{OH}	+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V		−0.4 mA −0.4 mA
I_{CEX}		+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V	
V_{OL}	+3.0V −2.975V	+3.0V −2.975V	+2.975V −3.0V	+2.975V −3.0V	GND −3.0V	GND −3.0V	+3.0V GND	+3.0V GND	+16 mA +16 mA

Channel A shown under test. Other channels are tested similarly.

FIGURE 1. I_{CEX}, V_{OH} and V_{OL}

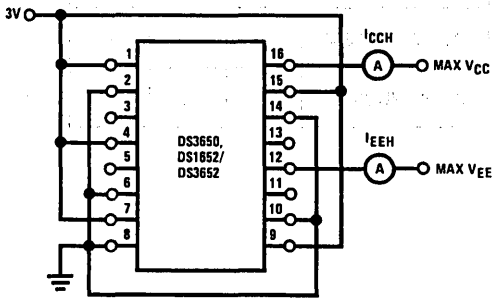

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FIGURE 2. I_{CCH} and I_{EEH}

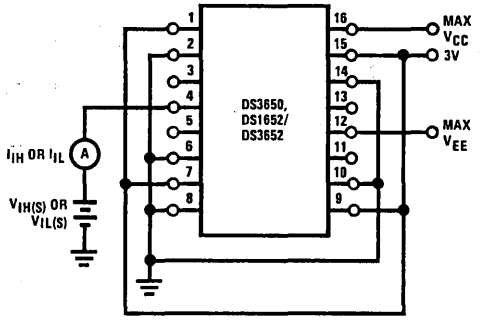

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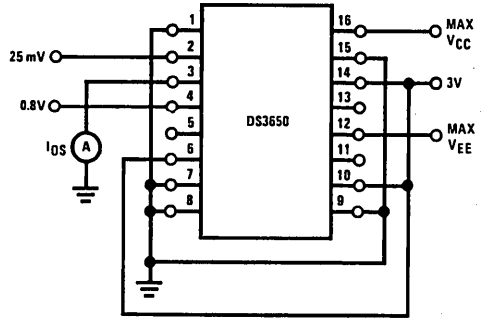
FIGURE 3. $I_{IH(S)}$ and $I_{IL(S)}$

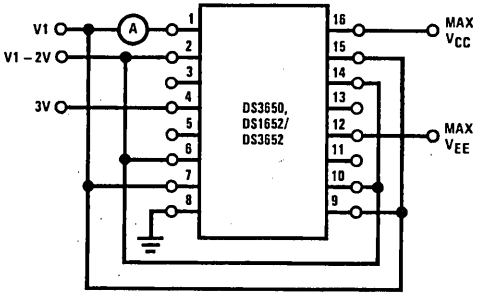
Electrical Characteristic Test Circuits (Continued)



TL/F/5782–7

Note: Channel A shown under test, other channels are tested similiarly. Only one output shorted at a time.

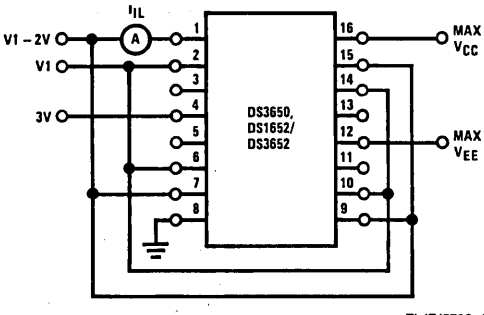
FIGURE 4. I_{OS}



TL/F/5782–8

Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to −3V.

FIGURE 5. I_{IH}



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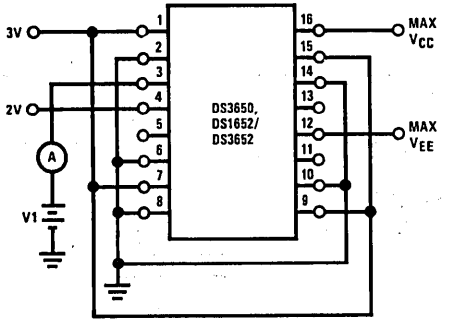
Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to −3V.

FIGURE 6. I_{IL}



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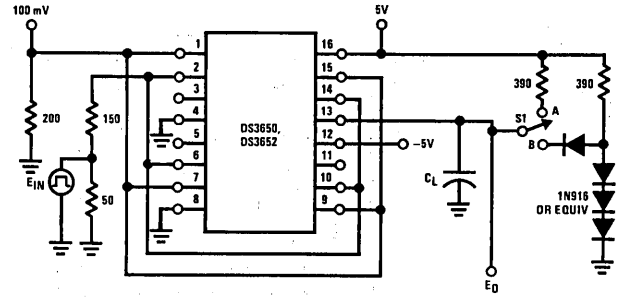
Note: Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4V and 2.4V.

FIGURE 7. I_{OFF}

7

AC Test Circuits and Switching Time Waveforms



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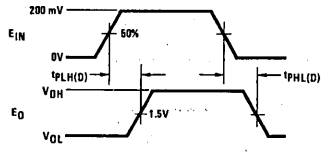

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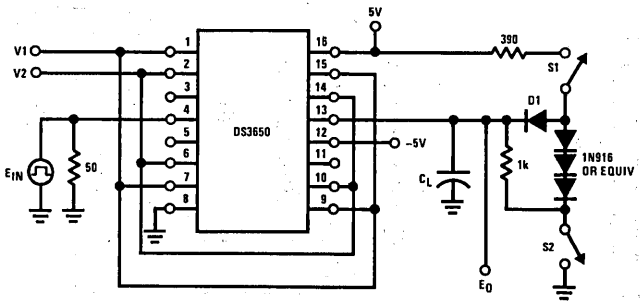
Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 50%

Note: Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for DS1652/DS3652
S1 at "B" for DS1650/DS3650
C_L = 15 pF total for DS1652/DS3652
C_L = 50 pF total for DS1650/DS3650

FIGURE 8. Receiver Propagation Dealy $t_{PLH(D)}$ and $t_{PHL(D)}$



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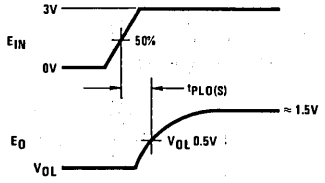
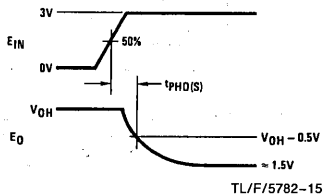


TL/F/5782–14

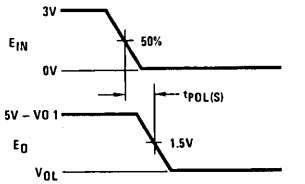


TL/F/5782–15

Note: Output of Channel B shown under test, other channels are tested similiarly.

	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 50%



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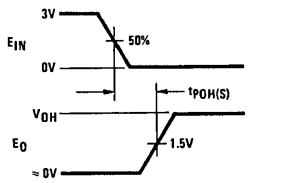

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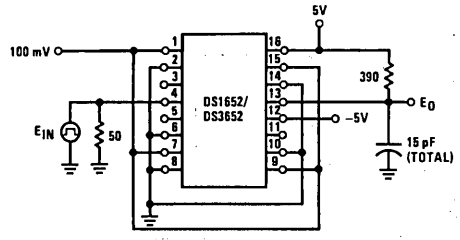
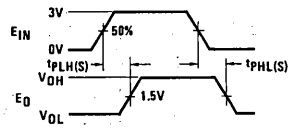
FIGURE 9. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHO(S)}$ and $t_{POH(S)}$

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5782–18



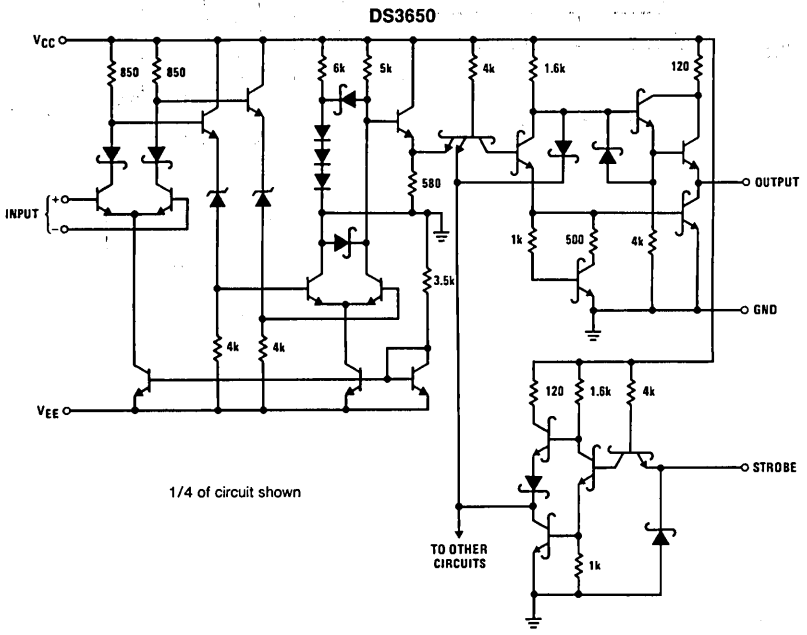
TL/F/5782–19

Note: Output of Channel B shown under test, other channels are tested similarly.

Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% and 90%
PRR = 1 MHz
Duty Cycle = 500 ns

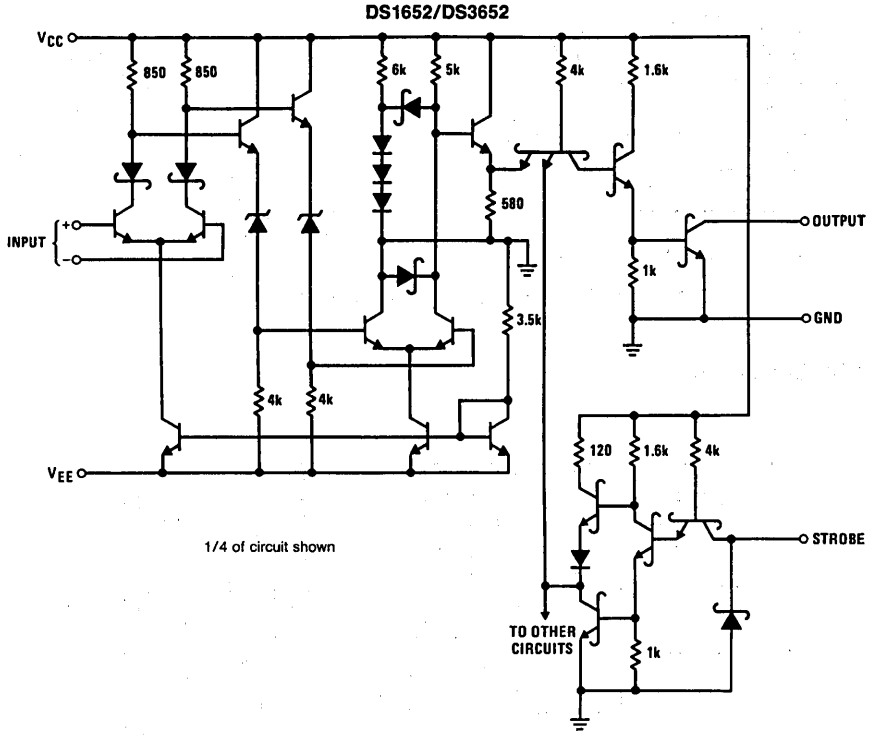
FIGURE 10. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

Schematic Diagrams



TL/F/5782–20

Schematic Diagrams (Continued)



1/4 of circuit shown

TL/F/5782–21

National Semiconductor

DS55107/DS75107/DS75108/DS75208 Dual Line Receivers

General Description

The products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers of MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the SN55109/SN75109 and μA75110/DS75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the DS75208 make it ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators.

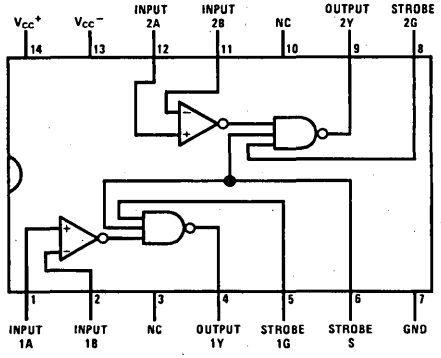
Input protection diodes are incorporated in series with the collectors of the differential input stage. These diodes are useful in certain applications that have multiple $V_{CC}+$ supplies or $V_{CC}+$ supplies that are turned off.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

Connection Diagram

Dual-In-Line Package



TL/F/9446–1

Top View

Order Number DS55107J, DS75107J, DS75107M, DS75107N, DS75107AM, DS75107AN, DS75108M, DS75108N, DS75208J or DS75208N
See NS Package Number J14A, M14A or N14A

For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS55107AJ/883
See NS Package Number J14A

Selection Guide

Temperature → / Package →	$-55°C \le T_A \le +125°C$ Cavity Dip	$0°C \le T_A \le +70°C$ Cavity or Molded Dip	
Input Sensitivity → / Output Logic ↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-Up	DS55107	DS75107	
TTL Open Collector		DS75108	DS75208

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, $V_{CC}+$	7V
Supply Voltage, $V_{CC}-$	−7V
Differential Input Voltage	±6V
Common Mode Input Voltage	±5V
Strobe Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	DS55107			DS75107, DS75108, DS75208		
	Min	Nom	Max	Min	Nom	Max
Supply Voltage $V_{CC}+$	4.5V	5V	5.5V	4.75V	5V	5.25V
Supply Voltage $V_{CC}-$	−4.5V	−5V	−5.5V	−4.75V	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55107 and across the 0°C to +70°C range for the DS75107, DS75108 and DS75208. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

DS55107/DS75107, DS75108 Electrical Characteristics $T_{MIN} \le T_A \le T_{MAX}$ (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current into A1, B1, A2 or B2	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current into A1, B1, A2 or B2	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current into G1 or G2	$V_{CC}+$ = Max, $V_{CC}-$ = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ Max $V_{CC}+$			1	mA
I_{IL}	Low Level Input Current into G1 or G2	$V_{CC}+$ = Max, $V_{CC}-$ = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current into S	$V_{CC}+$ = Max, $V_{CC}-$ = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max $V_{CC}+$			2	mA
I_{IL}	Low Level Input Current into S	$V_{CC}+$ = Max, $V_{CC}-$ = Max, $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OH}	High Level Output Voltage	$V_{CC}+$ = Min, $V_{CC}-$ = Min, I_{LOAD} = −400 μA, V_{ID} = 25 mV, V_{IC} = −3V to 3V, (Note 3)		2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC}+$ = Min, $V_{CC}-$ = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	$V_{CC}+$ = Min, $V_{CC}-$ = Min V_{OH} = Max $V_{CC}+$, (Note 4)				250	μA
I_{OS}	Short Circuit Output Current	$V_{CC}+$ = Max, $V_{CC}-$ = Max, (Notes 2 and 3)		−18		−70	mA
$I_{CCH}+$	High Logic Level Supply Current from V_{CC}	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = 25 mV, T_A = 25°C			18	30	mA
$I_{CCH}-$	High Logic Level Supply Current from V_{CC}	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	$V_{CC}+$ = Min, $V_{CC}-$ = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics $V_{CC+} = 5V, V_{CC-} = -5V, T_A = 25°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low to High Level, from Differential Inputs A and B to Output	$R_L = 390\Omega, C_L = 50$ pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High to Low Level, from Differential Inputs A and B to Output	$R_L = 390\Omega, C_L = 50$ pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low to High Level, from Strobe Input G or S to Output	$R_L = 390\Omega, C_L = 50$ pF	(Note 3)		10	15	ns
			(Note 4)		13	20	ns
$t_{PHL(S)}$	Propagation Delay Time, High to Low Level, from Strobe Input G or S to Output	$R_L = 390\Omega, C_L = 50$ pF	(Note 3)		8	15	ns
			(Note 4)		13	20	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Note 2: Only one output at a time should be shorted.

Note 3: DS55107/DS75107 only.

Note 4: DS75108 only.

DS75208

Electrical Characteristics $0°C \le T_A \le +70°C$

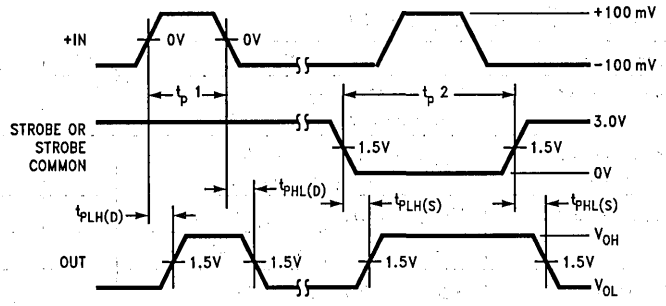
Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current into G1 or G2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current into S	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current into S	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min, V_{OH} = Max V_{CC+}				250	μA
I_{CCH+}	High Logic Level Supply Current from V_{CC+}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current from V_{CC-}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics $V_{CC+} = 5V, V_{CC-} = -5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, from Differential Inputs A and B to Output	$R_L = 470\Omega, C_L = 15$ pF, (Note 1)			35	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, from Differential Inputs A and B to Output	$R_L = 470\Omega, C_L = 15$ pF, (Note 1)			20	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, from Strobe Input G or S to Output	$R_L = 470\Omega, C_L = 15$ pF			17	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, from Strobe Input G or S to Output	$R_L = 470\Omega, C_L = 15$ pF			17	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.

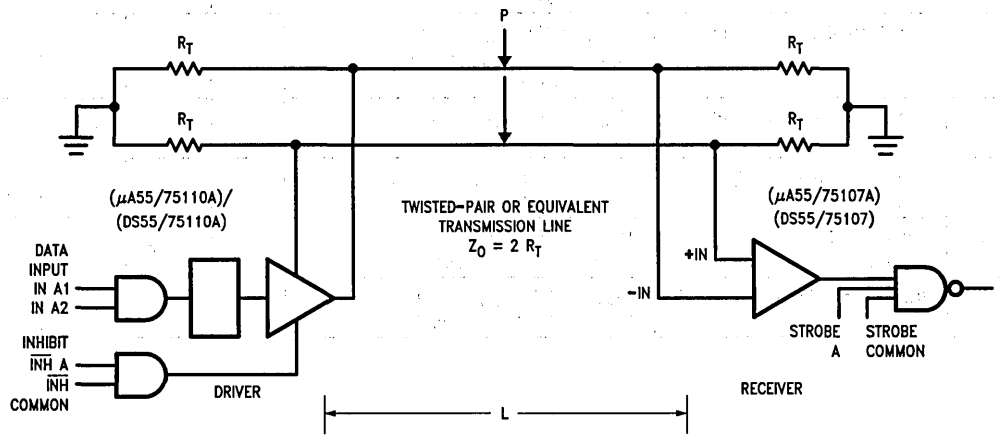
Voltage Waveforms



TL/F/9446–12

Typical Applications

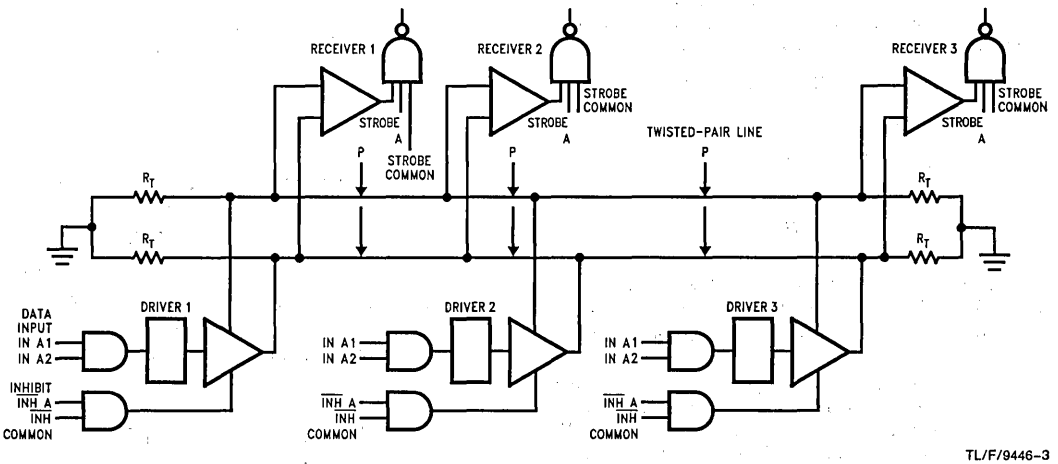
Basic Balanced-Line Transmission System



TL/F/9446–2

Typical Applications (Continued)

Data-Bus or Party-Line System



TL/F/9446–3

APPLICATION

The DS55107, DS75107 dual line circuits are designed specifically for use in high speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver input logic levels. The voltage difference is approximately:

$$V_{DIFF} \cong \tfrac{1}{2} I_{O(on)} \times R_T \qquad (1)$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \cong I_{O(on)} \times R_T \qquad (2)$$

The strobe feature of the receivers and the inhibit feature of the drivers allow the DS55107, DS75107 dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time multiplexed on the transmission line. The DS55107, DS75107 device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

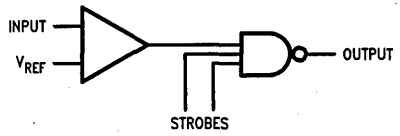
The DS55107, DS75107 dual line circuits may also be used in unbalanced or single line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.

The receiver threshold level is established by applying a DC reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal

Typical Applications (Continued)

swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3.0V to +3.0V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

Unbalanced or Single-Line Systems



TL/F/9446–4

Precautions in the Use of DS1603, DS3603, DS55107, DS75107, DS75108 and DS75208 Dual Line Receivers

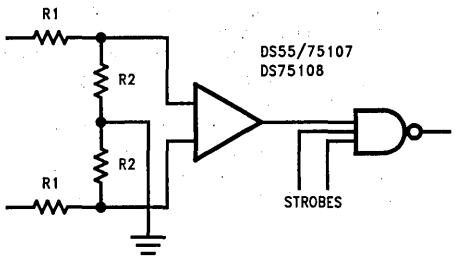
The following precaution should be observed when using or testing DS55107, DS75107 line circuits.

When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0V and +3.0V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

The DS55107, DS75107 and DS75108 line receivers feature a common mode input voltage range of ±3.0V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common mode range can be extended by the use of external input attenuators. Common mode input voltages can in this way be reduced to ±3.0V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

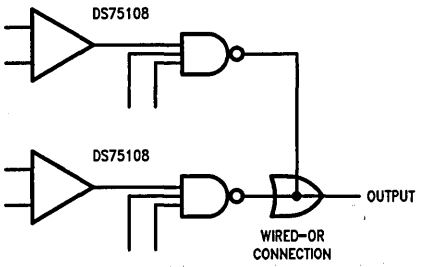
The DS75108 line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other DS75108 outputs. This allows a level of logic to be implemented without addtional logic delay.

Increasing Common Mode Input Voltage Range of Receiver



TL/F/9446–5

DS75108 Wired-OR Output Connections

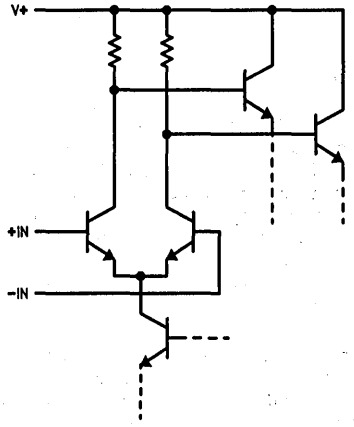


TL/F/9446–6

Circuit Differences Between "A" and Standard Devices

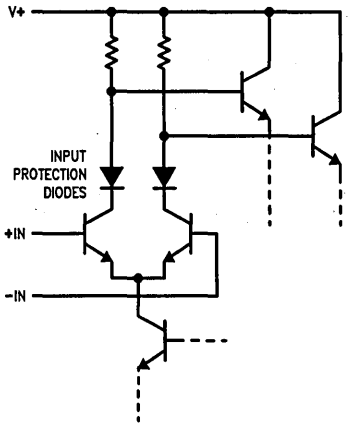
The difference between the "A" and standard devices is shown in the following schematics of the input stage.

"A" Devices



TL/F/9446–7

Standard Devices

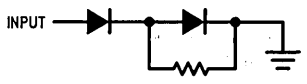


TL/F/9446–8

Typical Applications (Continued)

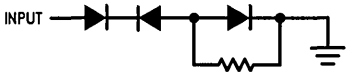
The input protection diodes are useful in certain party-line systems which may have multiple V+ power supplies and, in which case, may be operated with some of the V+ supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

"A" Devices



TL/F/9446–9

Standard Devices



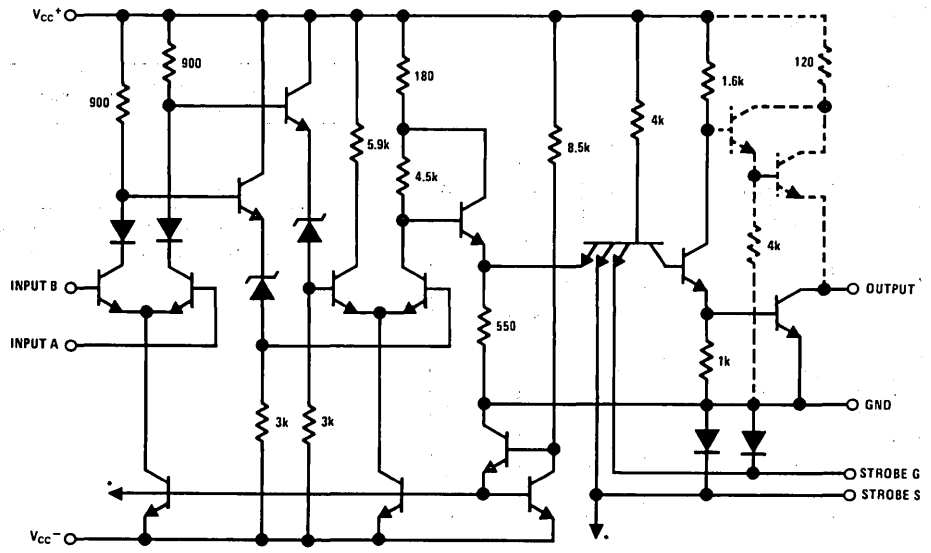
TL/F/9446–10

This would be a problem in specific systems which might possibly have the transmission lines biased to some potential greater than 1.4V. Since this is not a widespread application problem, both the "A" and standard devices will be available. The ratings and characteristic specifications of the "A" devices are the same as those of the standard devices.

The DS55107A feature the "A" device input stage.

Schematic Diagrams

DS55107/DS75107, DS75108, DS75208



TL/F/9446–11

Note 1: ½ of the dual circuit is shown.

Note 2: *Indicates connections common to second half of dual circuit.

Note 3: Components shown with dash lines are applicable to the DS55107, DS75207 and DS75107 only.

7

National Semiconductor

DS55115/DS75115 Dual Differential Line Receiver

General Description

The DS55115/DS75115 is a dual differential line receiver designed to sense differential signals from data transmission lines. Designed for operation over military and commercial temperature ranges, the DS55115/DS75115 can typically receive ±500 mV differential data with ±15V common-mode noise. Outputs are open-collector and give TTL compatible signals which are a function of the polarity of the differential input signal. Active output pull-ups are also available, offering the option of an active TTL pull-up through an external connection.

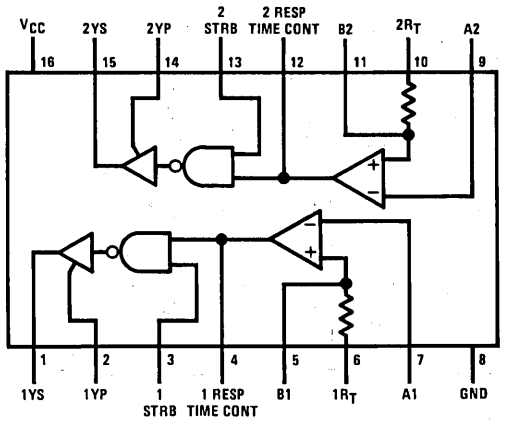
Response time may be controlled with the use of an external capacitor. Each channel may be independently controlled and optional input termination resistors are also available.

Features

- Single 5V supply
- High common-mode voltage range
- Each channel individually strobed
- Independent response time control
- Uncommitted collector or active pull-up option
- TTL compatible output
- Optional 130Ω termination resistors
- Direct replacement for 9615

Connection Diagram

Dual-In-Line Package



TL/F/5787–1

Top View

Order Number DS75115N
See NS Package Number N16A

For Complete Military 883 Specifications, See RETS Datasheet.
Order Number DS9615M*

*Contact Product Marketing

Function Table

Strobe	Diff. Input	Output
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 1) 7V

Input Voltage at A, B and R_T Inputs ±25V

Input Voltage at Strobe Input 5.5V

Off-State Voltage Applied to Open-Collector Outputs 14V

Maximum Power Dissipation* at 25°C

Cavity Package 1433 mW

Molded Package 1362 mW

Operating Free-Air Temperature Range

DS55115 −55°C to +125°C

DS57115 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature

($\frac{1}{16}$ inch from case for 4 seconds) 260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS55115	4.5	5.5	V
DS75115	4.75	5.25	V
High Level Output Current (I_{OH})		−5	mA
Low Level Output Current (I_{OL})		15	mA
Operating Temperature (T_A)			
DS55115	−55	125	°C
DS75115	0	70	°C

Electrical Characteristics (Notes 2, 3 and 5)

Symbol	Parameter	Conditions		DS55115			DS75115			Units
				Min	Typ	Max	Min	Typ	Max	
V_{TH}	Differential Input High-Threshold Voltage	V_O = 0.4V, I_{OL} = 15 mA, V_{IC} = 0V			200	500		200	500	mV
V_{TL}	Differential Input Low-Threshold Voltage	V_O = 2.4V, I_{OH} = −5 mA, V_{IC} = 0V			−200	−500		−200	−500	mV
V_{ICR}	Common-Mode Input Voltage Range	V_{ID} = ±1V		15 to −15	24 to −19		15 to −15	24 to −19		V
$V_{IH(STROBE)}$	High-Level Strobe Input Voltage			2.4			2.4			V
$V_{IL(STROBE)}$	Low-Level Strobe Input Voltage					0.4			0.4	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{ID} = −0.5V, I_{OH} = −5 mA	T_A = Min	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = Max	2.4			2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{ID} = 0.5V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, Other Input at 5.5V	T_A = Min			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = Max			−0.7			−0.7	
I_{SH}	High Level Strobe Current	V_{CC} = Min, V_{ID} = −0.5V, V_{STROBE} = 4.5V	T_A = 25°C		0.5	2		0.5	5	µA
			T_A = Max			5			10	
I_{SL}	Low Level Strobe Current	V_{CC} = Max, V_{ID} = 0.5V, V_{STROBE} = 0.4V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
I_4, I_{12}	Response Time Control Current (Pin 4 or Pin 12)	V_{CC} = Max. V_{ID} = 0.5V, V_{RC} = 0V	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(OFF)}$	Off-State Open-Collector Output Current	V_{CC} = Min, V_{OH} = 12V, V_{ID} = −4.5V	T_A = 25°C			100				µA
			T_A = Max			200				
		V_{CC} = Min, V_{OH} = 5.25V, V_{ID} = −4.75V	T_A = 25°C						100	
			T_A = Max						200	

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Electrical Characteristics (Notes 2, 3 and 5) (Continued)

Symbol	Parameter	Conditions		DS55115			DS75115			Units
				Min	Typ	Max	Min	Typ	Max	
R_T	Line Terminating Resistance	V_{CC} = 5V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, V_O = 0V, V_{ID} = −0.5V, (Note 4)	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply Current (Both Receivers)	V_{CC} = Max, V_{ID} = 0.5V, V_{IC} = 0V	T_A = 25°C		32	50		32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for the actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55115 and across the 0°C to +70°C range for the DS75115. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

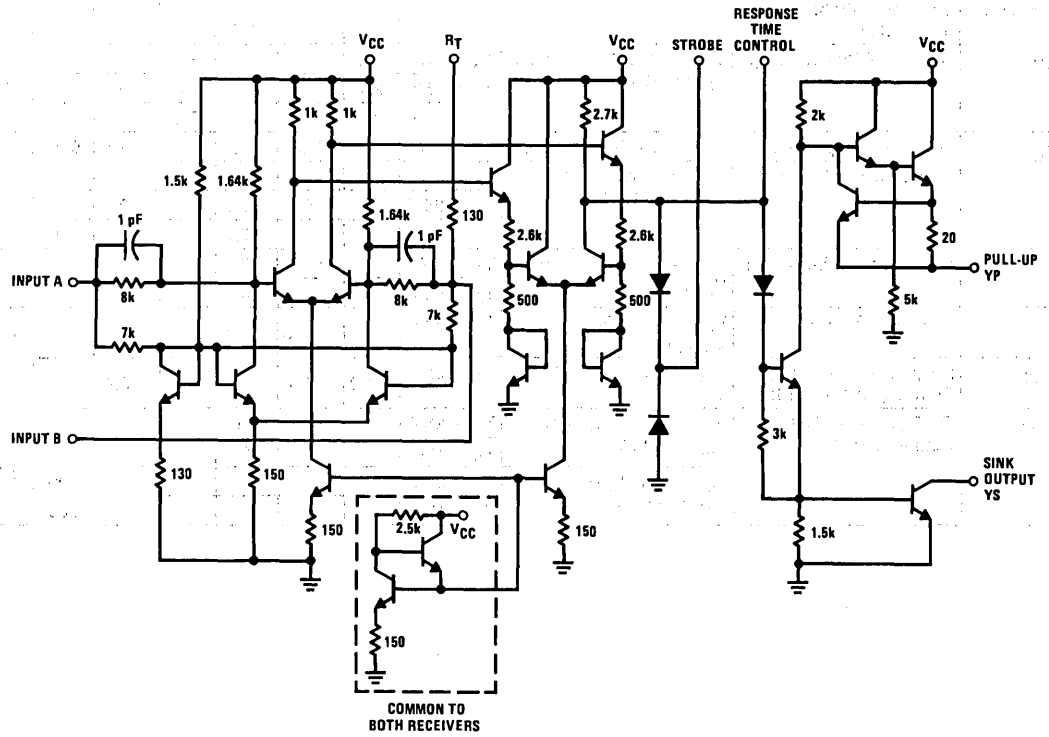
Note 4: Only one output at a time should be shorted.

Note 5: Unless otherwise noted, V_{STROBE} = 2.4V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

Symbol	Parameter	Conditions	DS55115			DS75115			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 3.9 kΩ, *(Figure 1)*		18	50		18	75	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 390Ω, *(Figure 1)*		20	50		20	75	ns

Schematic Diagram



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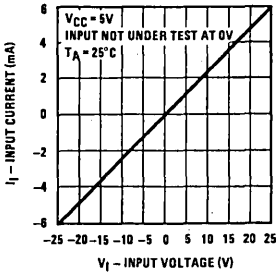
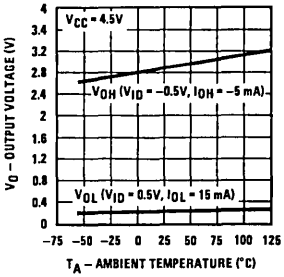
Typical Performance Characteristics (Note 3)

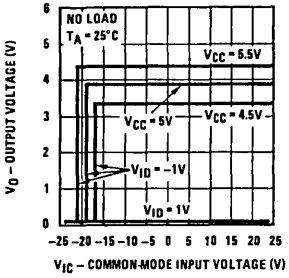
Input Current vs Input Voltage



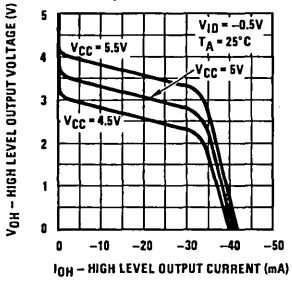
Output Voltage vs Temperature



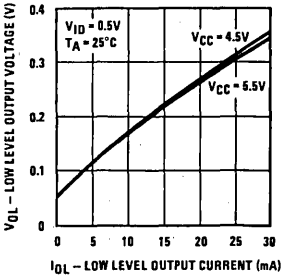
Output Voltage vs Common-Mode Input Voltage



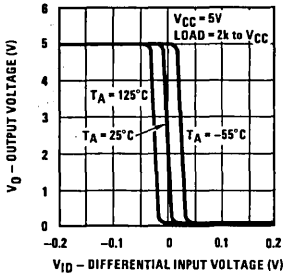
High Level Output Voltage vs Output Current



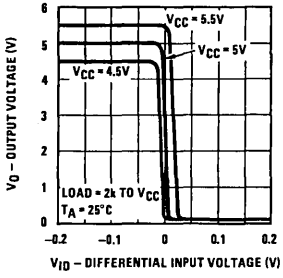
Low Level Output Voltage vs Output Current



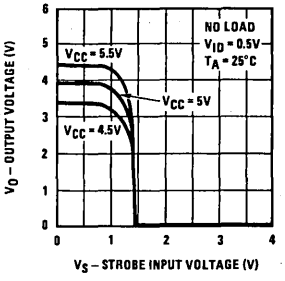
Output Voltage vs Differential Input Voltage



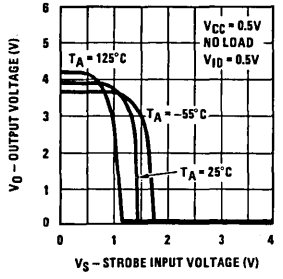
Output Voltage vs Differential Input Voltage



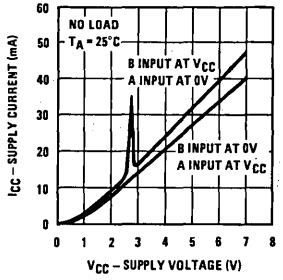
Output Voltage vs Strobe Input Voltage



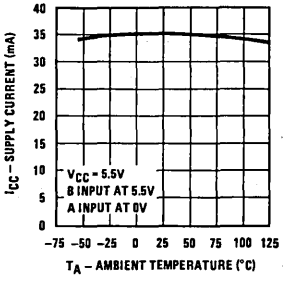
Output Voltage vs Strobe Input Voltage



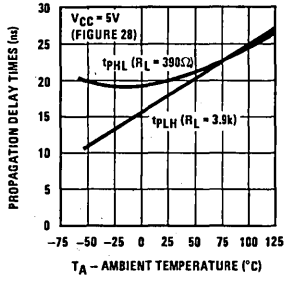
Supply Current (Both Receivers) vs Supply Voltage



Supply Current (Both Receivers) vs Temperature



Propagation Delay Times vs Temperature



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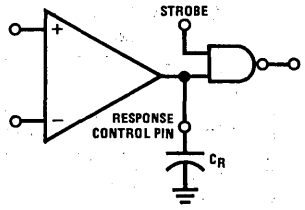
Frequency Response Control



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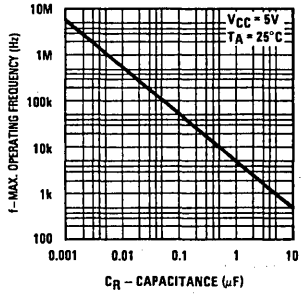
Note: C_R (response control) > 0.01 μF may cause slowing of rise and fall times of the output.

Frequency Response as a Function of Capacitance



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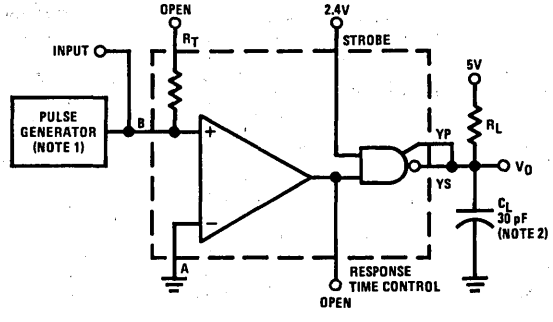
AC Test Circuit and Switching Time Waveforms



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Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 500 kHz/t_W = 100 ns

Note 2: C_L includes probe and test fixture capacitance

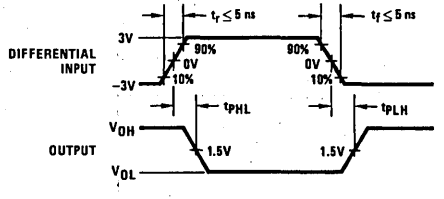

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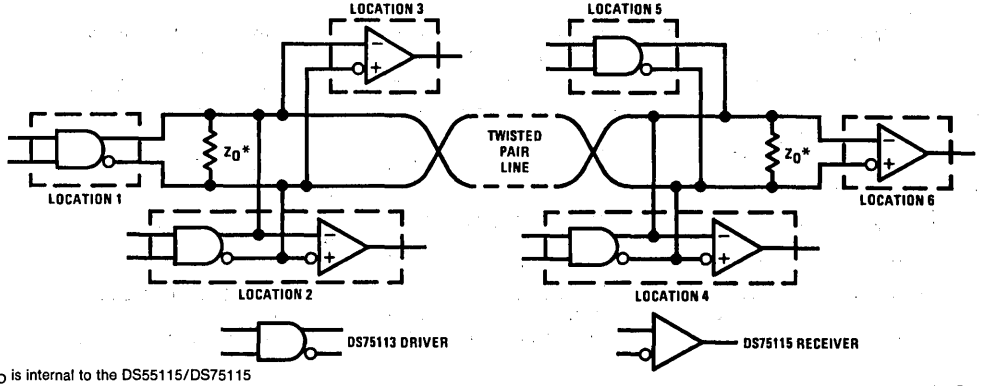
FIGURE 1. Propagation Delay Time

Typical Application

Basic Party-Line or Data-Bus Differential Data Transmission



*Z_O is internal to the DS55115/DS75115

A capacitor may be connected in series with Z_O to reduce power dissipation.

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National Semiconductor

DS55122
Triple Line Receiver

General Description

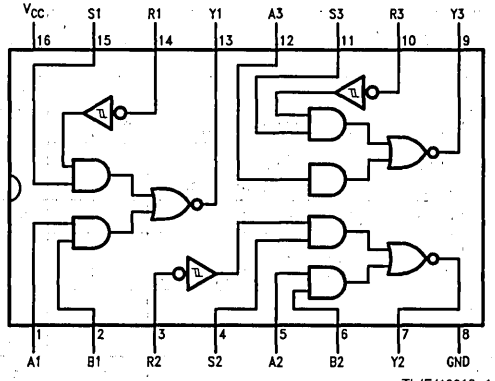
The DS55122 is a triple line receiver designed for digital data transmission with line impedances from 50Ω to 500Ω. Each receiver has one input with built-in hysteresis which provides a large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS55122 is compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed—typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Fanout to 10 series standard loads
- Plug-in replacement for the SN55122

Connection Diagram

Dual-In-Line Package



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Top View

For Complete Military 883 Specifications, see RETS Data Sheet.

Order Number DS55122J/883 or DS55122W/883
See NS Package Number J16A or W16A

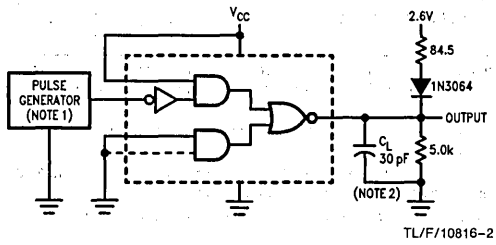
Truth Table

Inputs				Output
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant

† B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

AC Test Circuit and Switching Time Waveforms



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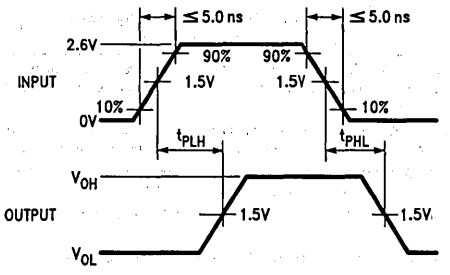

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Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%, $t_r = t_f$ = 5.0 ns.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.0V
Input Voltage	
R Input	6.0V
A, B, or S Input	5.5V
Output Voltage	6.0V
Output Current	±100 mA
Maximum Power Dissipation* at 25°C (J)	1433 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature (T_A)			
DS55122	−55	+125	°C
High Level Output Current (I_{OH})		−500	μA
Low Level Output Current (I_{OL})		16	mA

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	A, B, R, or S		2.0			V
V_{IL}	Low Level Input Voltage	A, B, R, or S				0.8	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)		0.3	0.6		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S				−1.5	V
I_I	Input Clamp at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S				1.0	mA
V_{OH}	High Level Output Voltage	I_{OH} = −500 μA	V_{IH} = 2V, V_{IL} = 0.8V, (Note 4)	2.6			V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 7)	2.6			V
V_{OL}	Low Level Output Voltage	I_{OL} = 16 mA	V_{IH} = 2.0V, V_{IL} = 0.8V, (Note 4)			0.4	V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 8)			0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S				40	μA
		V_I = 3.8V, R				170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)		−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V				72	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for DS55122 and 0°C to +75°C for DS75122, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

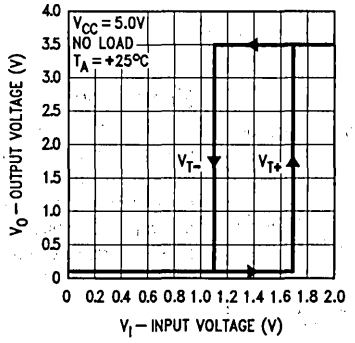
Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 7: Receiver input was at a high level immediately before being reduced to 1.45V.

Note 8: Receiver input was at a low level immediately before being raised to 1.45V.

Typical Performance Characteristics

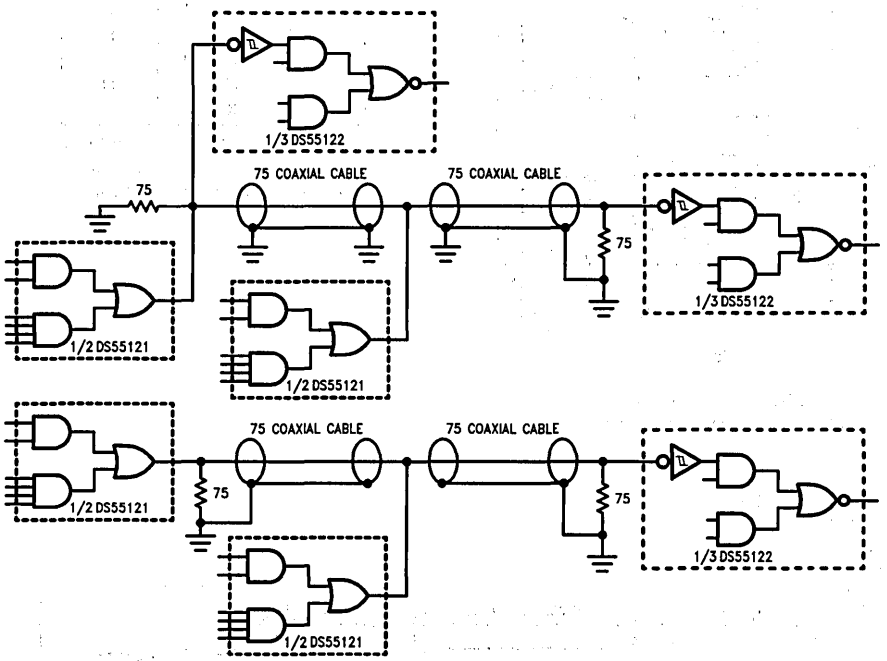
Output Voltage vs Receiver Input Voltage



TL/F/10816–4

Typical Applications

Single-Ended Party Line Circuits



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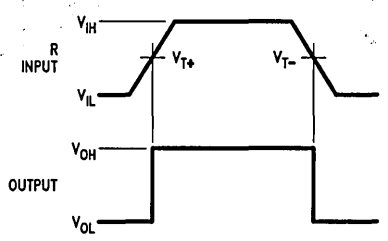
Pulse Squaring



TL/F/10816–6

The high gain and built-in hystersis of the DS55122 line receiver enables it to be used as a Schmitt trigger in squaring up pulses.

National Semiconductor

DS75124 Triple Line Receiver

General Description

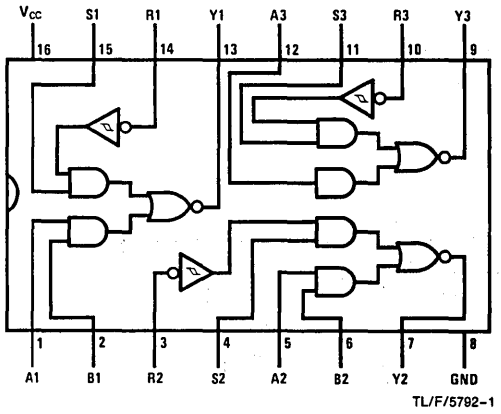
The DS75124 is designed to meet the input/output interface specifications for IBM System 360. It has built-in hysteresis on one input on each of the three receivers to provide large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS75124 is compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed . . . typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Plug-in replacement for the SN75124 and the 8T24

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5792-1

Top View

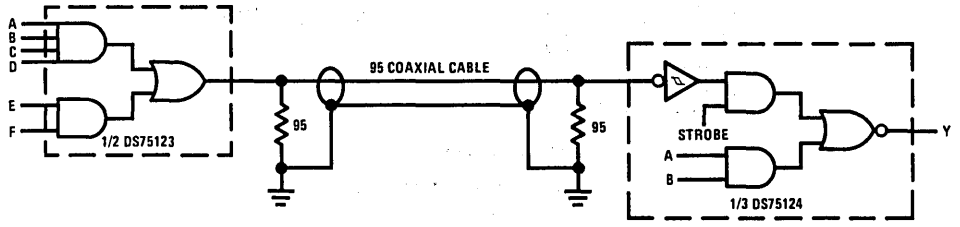
Order Number DS75124N
See NS Package Number N16A

Inputs				Output
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant

†B input and last two lines of the truth table are applicable to receivers 1 and 2 only

Typical Application



TL/F/5792-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	
R Input with V_{CC} Applied	7.0V
R Input with V_{CC} not Applied	6.0V
A, B, or S Input	5.5V
Output Voltage	7.0V
Output Current	±100 mA
Maximum Power Dissipation* at 25°C	
Molded Package	1362 mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−800	μA
Low Level Output Current, I_{OL}		16	mA
Operating Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	A, B, or S	2.0			V
		R	1.7			V
V_{IL}	Low Level Input Voltage	A, B, or S			0.8	V
		R			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)	0.2	0.4		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S			−1.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S			1	mA
		R, V_I = 7.0V			5.0	mA
		R, V_I = 6.0V, V_{CC} = 0V			5.0	mA
V_{OH}	High Level Output Voltage	$V_{IH} = V_{IHMIN}$, $V_{IL} = V_{ILMAX}$, I_{OH} = −800 μA, (Note 4)	2.6			V
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{IHMIN}$, $V_{IL} = V_{ILMAX}$, I_{OL} = 16 mA, (Note 4)			0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S			40	μA
		V_I = 3.11V, R			170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)	−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V			72	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

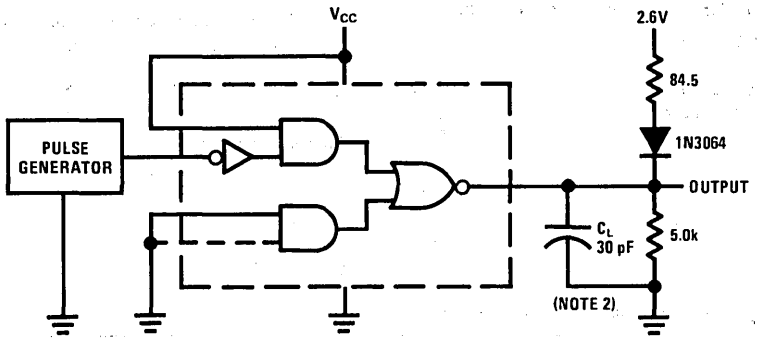
Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75124, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

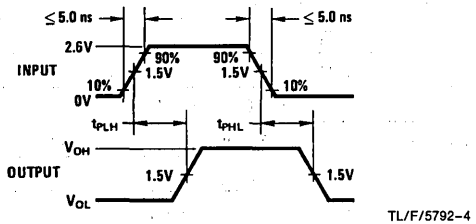
AC Test Circuit and Switching Time Waveforms



TL/F/5792-3

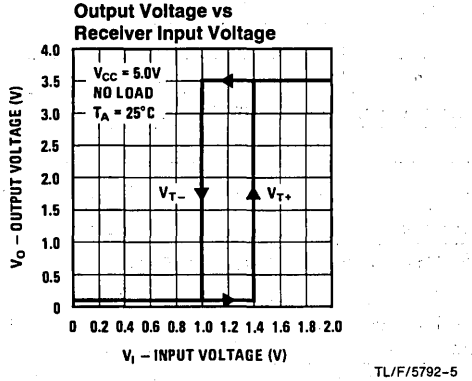
Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%

Note 2: C_L includes probe and jig capacitance.



TL/F/5792-4

Typical Performance Characteristics



TL/F/5792-5

National Semiconductor

DS75129 Eight-Channel Line Receivers

General Description

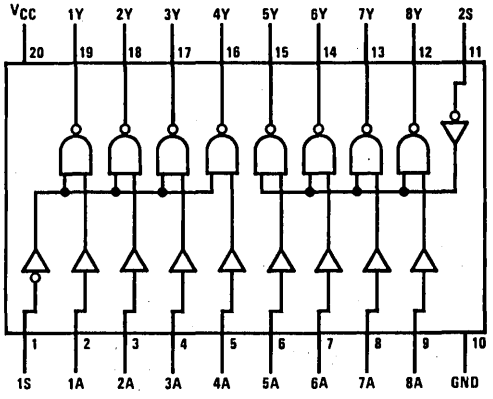
The DS75129 is an eight-channel line receiver designed to satisfy the requirements of the input-output interface specification for IBM 360/370. The device features common strobes for each group of four receivers. The DS75129 has an active-low strobe. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The DS75129 is characterized for operation from 0°C to 70°C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance—7 kΩ to 20 kΩ
- Output compatible with TTL
- Schottky-clamped transistors
- Operates from a single 5V supply
- High speed—low propagation delay
- Ratio specification—t_{PLH}/t_{PLH}
- Common strobe for each group of four receivers
- DS75129 strobe—active-low

Connection Diagram

DS75129
Dual-In-Line Package



positive logic: $Y = \overline{AS}$

TL/F/5793–2

Top View

Order Number DS75129N
See NS Package Number N20A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage Range	−0.15V to 7V
Strobe Input Voltage	7V
Maximum Power Dissipation* at 25°C (Note 2)	
Molded Package	1687 mW
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

*Derate molded package 13.5 mW/°C above 25°C.

Lead Temperature	260°C
1/16 Inch from Case for 4 Seconds: N Package	

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Symbol	Parameter		Conditions	Min	Typ (Note 5)	Max	Units
V_{IH}	High-Level Input Voltage	A		1.7			V
		S		2			
V_{IL}	Low-Level Input Voltage	A				0.7	V
		S				0.7	
V_{OH}	High-Level Output Voltage		V_{CC} = 4.5V, V_{IL} = 0.7V, I_{OH} = 0.4 mA	2.4	3.1		V
V_{OL}	Low-Level Output Voltage		V_{CC} = 4.5V, V_{IH} = 1.7V, I_{OL} = 16 mA		0.4	0.5	V
V_I	Input Clamp Voltage	S	V_{CC} = 4.5V, I_I = −18 mA			−1.5	V
I_{IH}	High-Level Input Current	A	V_{CC} = 5.5V, V_I = 3.11V		0.3	0.42	mA
		S	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low-Level Input Current	A	V_{CC} = 5.5V, V_I = 0.15V			−0.24	mA
		S	V_{CC} = 5.5V, V_I = 0.4V			−0.4	
I_{OS}	Short-Circuit Output Current (Note 4)		V_{CC} = 5.5V, V_O = 0V	−18		−60	mA
r_I	Input Resistance		V_{CC} = 4.5V, 0V, or Open, ΔV, = 0.15V to 4.15V	7		20	kΩ
I_{CC}	Supply Current		V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 0.7V		19	31	mA
			V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 4V		32	53	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: For operation above 25°C free-air temperature, refer to Thermal Ratings for ICs, in App Note AN-336.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

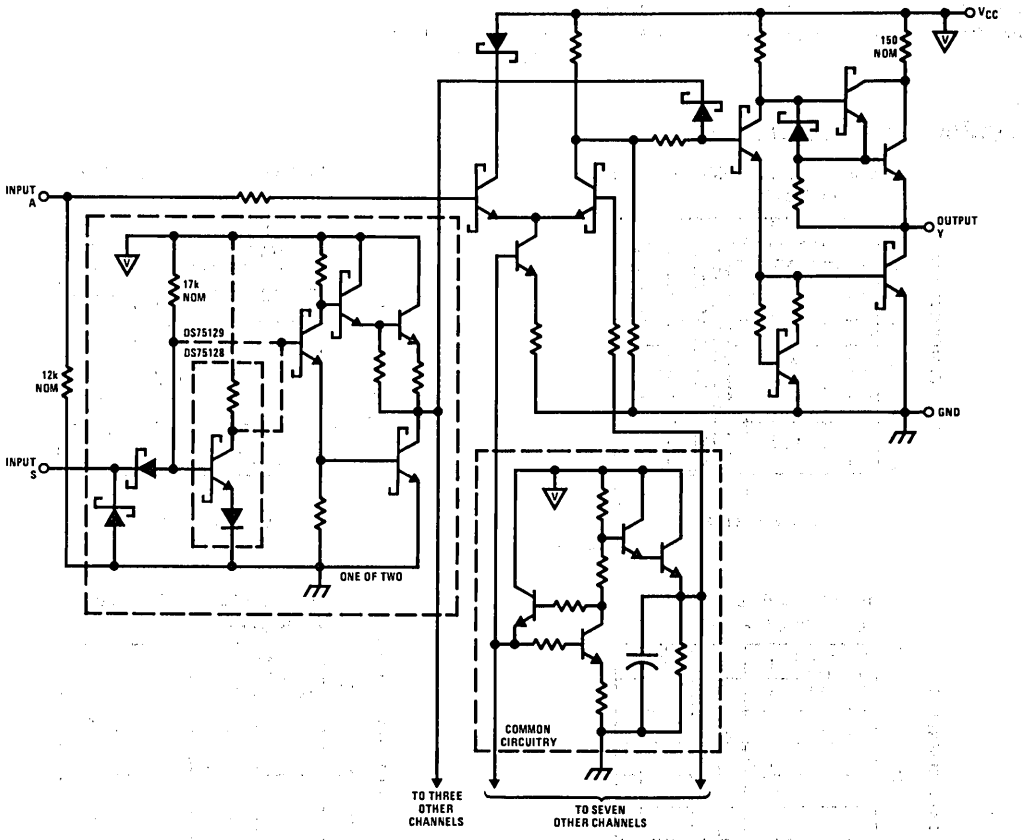
Note 4: Only one output should be shorted at a time.

Note 5: All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter		Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	A	R_L = 400Ω, C_L = 50 pF, See *Figure 1*	7	14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	A		10	18	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	S			20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	S			16	30	ns
t_{PLH} / t_{PHL}	Ratio of Propagation Delay Times	A		0.5	0.8	1.3	
t_{TLH}	Transition Time, Low-to-High-Level Output			1	7	12	ns
t_{THL}	Transition Time, High-to-Low-Level Output			1	3	12	ns

Schematic Diagram (each receiver)



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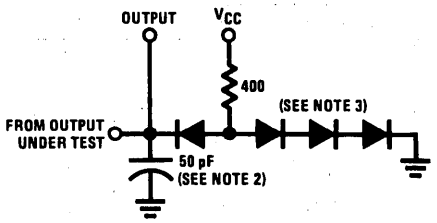
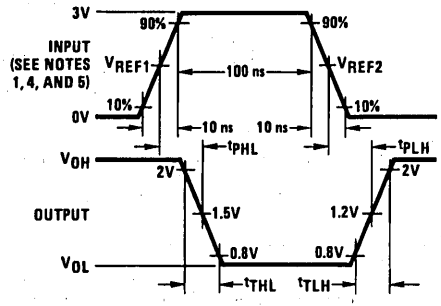
AC Test Circuit and Switching Time Waveforms



TL/F/5793–4



TL/F/5793–5

Note 1: Input pulses are supplied by a generator having the following characteristics: Z_O = 50Ω, PRR = 5 MHz.

Note 2: Includes probe and jig capacitance.

Note 3: All diodes are 1N3064 or equivalent.

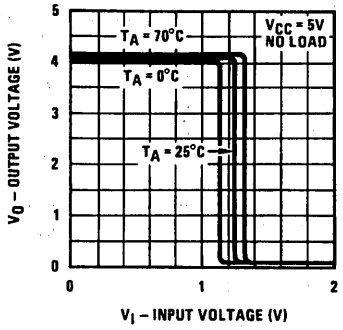
Note 4: The strobe inputs of DS75129 are in-phase with the output.

Note 5: V_{REF1} = 0.7V and V_{REF2} = 1.7V for testing data (A) inputs, V_{REF1} = V_{REF2} = 1.3V for strobe inputs.

FIGURE 1

Typical Characteristics

Voltage Transfer Characteristics From A Inputs



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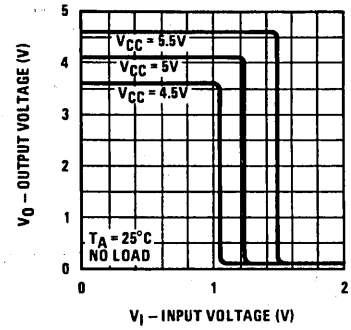
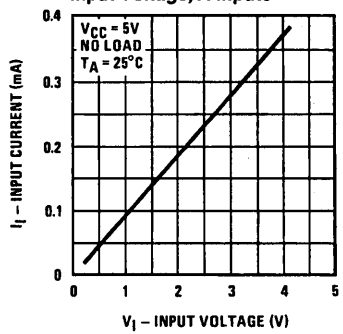
Voltage Transfer Characteristics From A Inputs



TL/F/5793–7

Input Current vs Input Voltage, A Inputs



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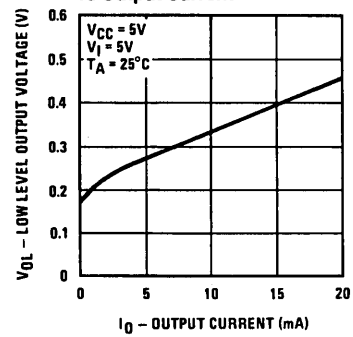
Low-Level Output Voltage vs Output Current



TL/F/5793–9

National Semiconductor

DS7820/DS8820 Dual Line Receiver

General Description

The DS7820, specified from −55°C to +125°C, and the DS8820, specified from 0°C to +70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

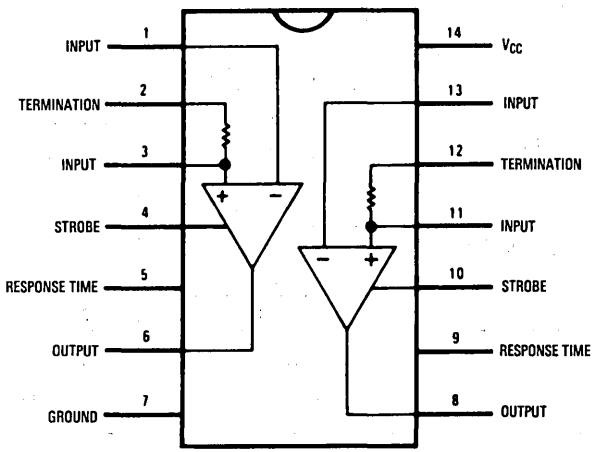
The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Each channel can be strobed independently
- High input resistance
- Fan out of two with TTL integrated circuits
- Strobe low forces output to "1" state

Connection Diagram

Dual-In-Line Package



TL/F/5796–2

Top View

Order Number DS7820J or DS8820N
See NS Package Number J14A or N14A

For Complete Military 883 Specifications, See RETS Data Sheet.
Order Number: DS7820J/883 or DS7820W/883
See NS Package Number J14A or W14B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Maximum Power Dissipation* at 25°C

Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7820	4.5	5.5	V
DS8820	4.75	5.25	V
Temperature (T_A)			
DS7820	−55	+125	°C
DS8820	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Input Threshold Voltage	V_{CM} = 0V	−0.5	0	0.5	V
		−15V ≤ V_{CM} ≤ 15V	−1.0	0	1.0	V
V_{OH}	High Output Level	I_{OUT} ≤ 0.2 mA	2.5		5.5	V
V_{OL}	Low Output Level	I_{SINK} ≤ 3.5 mA	0		0.4	V
R_I^-	Inverting Input Resistance		3.6	5.0		kΩ
R_I^+	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_T	Line Termination Resistance	T_A = 25°C	120	170	250	Ω
t_r	Response Time	C_{DELAY} = 0 pF		40		ns
		C_{DELAY} = 100 pF		150		ns
I_{ST}	Strobe Current	V_{STROBE} = 0.4V		−1.0	−1.4	mA
		V_{STROBE} = 5.5V			5.0	μA
I_{CC}	Power Supply Current	V_{IN} = 15V		3.2	6.0	mA
		V_{IN} = 0V		5.8	10.2	mA
		V_{IN} = −15V		8.3	15.0	mA
I_{IN}^+	Non-Inverting Input Current	V_{IN} = 15V		5.0	7.0	mA
		V_{IN} = 0V	−1.6	−1.0		mA
		V_{IN} = −15V	−9.8	−7.0		mA
I_{IN}^-	Inverting Input Current	V_{IN} = 15V		3.0	4.2	mA
		V_{IN} = 0V		0	−0.5	mA
		V_{IN} = −15V	−4.2	−3.0		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

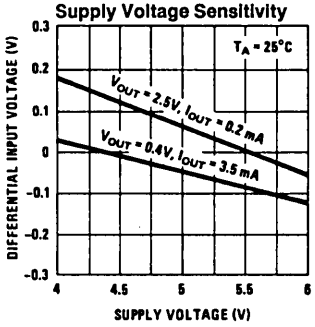
Note 2: These specifications apply for 4.5V ≤ V_{CC} ≤ 5.5V, −15V ≤ V_{CM} ≤ 15V and −55°C ≤ T_A ≤ +125°C for the DS7820 or 0°C ≤ T_A ≤ +70°C for the DS8820 unless otherwise specified; typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0 unless stated differently.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

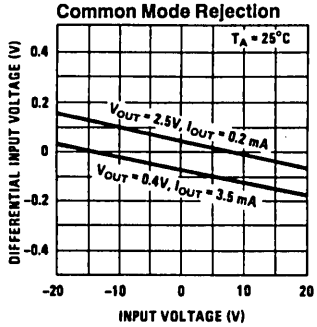
Note 4: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

Typical Performance Characteristics (Note 3)

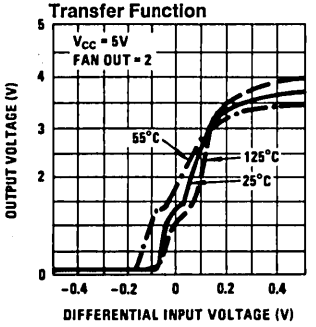
Supply Voltage Sensitivity



Common Mode Rejection



Transfer Function



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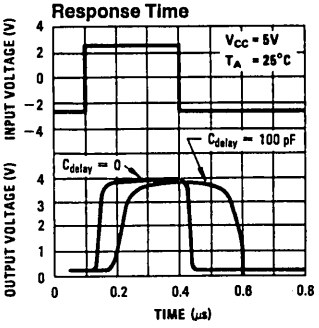
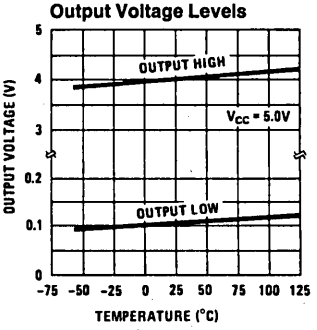
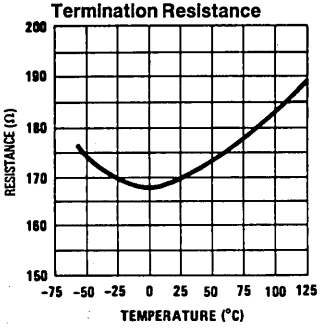
Response Time



Output Voltage Levels

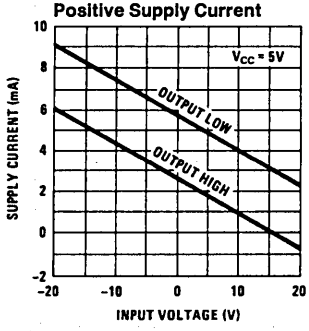


Termination Resistance

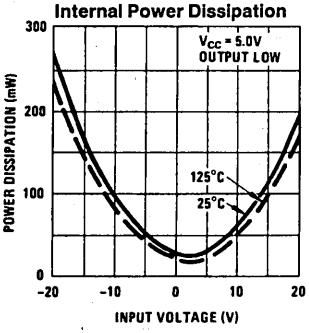


TL/F/5796–5

Positive Supply Current



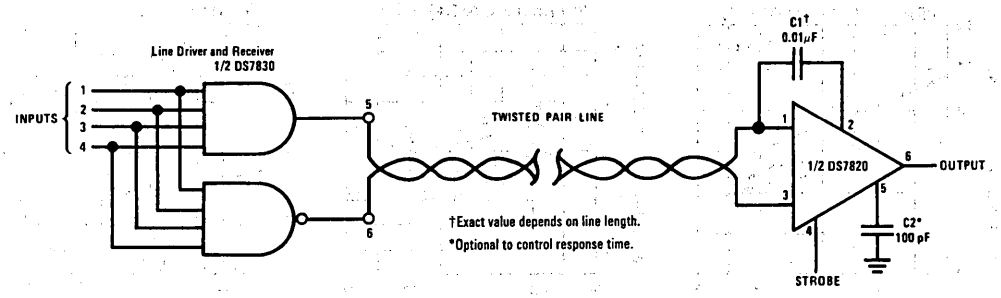
Internal Power Dissipation



TL/F/5796–6

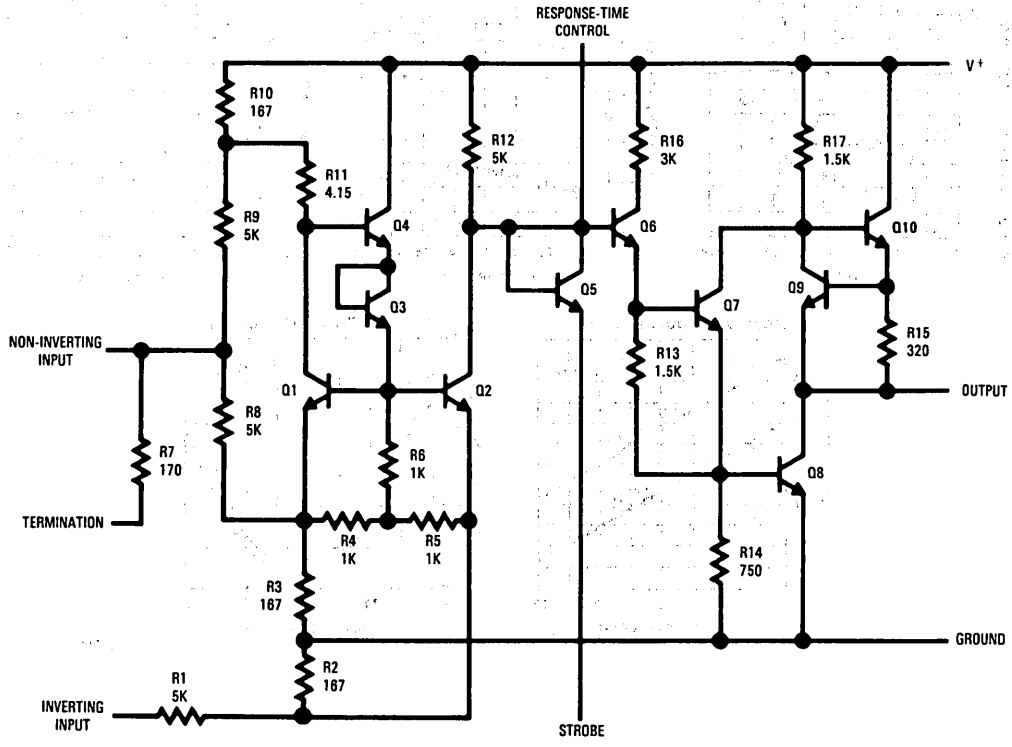
7

Typical Application



TL/F/5796–3

Schematic Diagram



TL/F/5796–1

National Semiconductor

DS7820A/DS8820A Dual Line Receiver

General Description

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

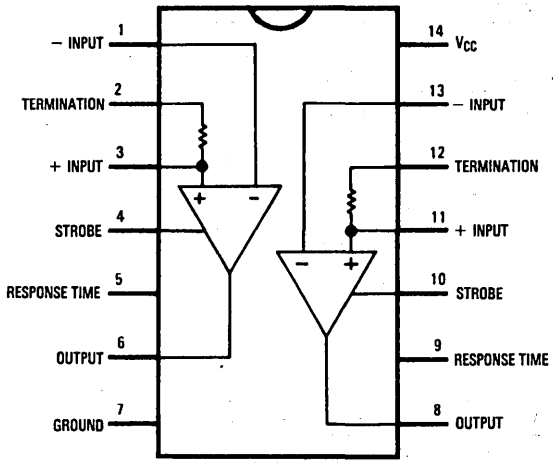
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (−55°C to +125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

Connection Diagram

Dual-In-Line Package



Note: Pin 7 connected to bottom of cavity package. TL/F/5797–2

Top View

Order Number DS7820AJ or DS8820AN
See NS Package Number J14A or N14A

For Complete Military 883 Specificatons, See RETS Data Sheet.
Order Number DS7820AJ/883 or DS7820AW/883
See NS Package Number J14A or W14B

7

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to 150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7820A	4.5	5.5	V
DS8820A	4.75	5.25	V
Temperature (T_A)			
DS7820A	−55	+125	°C
DS8820A	0	+70	°C

Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	I_{OUT} = −400 μA, V_{OUT} ≥ 2.5V	−3V ≤ V_{CM} ≤ +3V			0.06	0.5	V
			−15V ≤ V_{CM} ≤ +15V			0.06	1.0	V
		I_{OUT} = +16 mA, V_{OUT} ≤ 0.4V	−3V ≤ V_{CM} ≤ +3V			−0.08	−0.5	V
			−15V ≤ V_{CM} ≤ +15V			−0.08	−1.0	V
R_I^-	Inverting Input Resistance	−15V ≤ V_{CM} ≤ +15V			3.6	5		kΩ
R_I^+	Non-Inverting Input Resistance	−15V ≤ V_{CM} ≤ +15V			1.8	2.5		kΩ
R_T	Line Termination Resistance	T_A = 25°C			120	170	250	Ω
I_I^-	Inverting Input Current	V_{CM} = 15V				3.0	4.2	mA
		V_{CM} = 0V				0	−0.5	mA
		V_{CM} = −15V				−3.0	−4.2	mA
I_I^+	Non-Inverting Input Current	V_{CM} = 15V				5.0	7.0	mA
		V_{CM} = 0V				−1.0	−1.6	mA
		V_{CM} = −15V				−7.0	−9.8	mA
I_{CC}	Power Supply Current One Side Only	I_{OUT} = Logical "0"	V_{DIFF} = −1V	V_{CM} = 15V		3.9	6.0	mA
				V_{CM} = −15V		9.2	14.0	mA
			V_{DIFF} = −0.5V, V_{CM} = 0V			6.5	10.2	mA
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −400 μA, V_{DIFF} = 1V			2.5	4.0	5.5	V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = +16 mA, V_{DIFF} = −1V			0	0.22	0.4	V
V_{SH}	Logical "1" Strobe Input Voltage	I_{OUT} = +16 mA, V_{OUT} ≤ 0.4V, V_{DIFF} = −3V			2.1			V
V_{SL}	Logical "0" Strobe Input Voltage	I_{OUT} = −400 μA, V_{OUT} ≥ 2.5V, V_{DIFF} = −3V					0.9	V
I_{SH}	Logical "1" Strobe Input Current	V_{STROBE} = 5.5V, V_{DIFF} = 3V				0.01	5.0	μA
I_{SL}	Logical "0" Strobe Input Current	V_{STROBE} = 0.4V, V_{DIFF} = −3V				−1.0	−1.4	mA
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = 5.5V, V_{STROBE} = 0V			−2.8	−4.5	−6.7	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for 4.5V ≤ V_{CC} ≤ 5.5V, −15V ≤ V_{CM} ≤ 15V and −55°C ≤ T_A ≤ +125°C for the DS7820A or 4.75V ≤ V_{CC} ≤ 5.25V, 0°C ≤ T_A ≤ +70°C for the DS8820A unless otherwise specified. Typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0V unless stated differently.

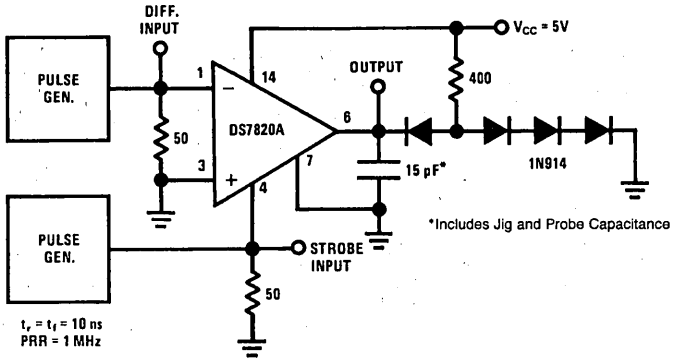
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

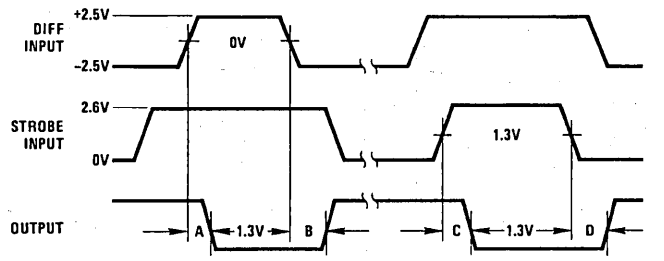
Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay, Differential Input to "0" Output	$R_L = 400\ \Omega$, $C_L = 15$ pF, see *Figure 1*		30	45	ns
t_{pd1}	Propagation Delay, Differential Input to "1" Output			27	40	ns
t_{pd0}	Propagation Delay, Strobe Input to "0" Output			16	25	ns
t_{pd1}	Propagation Delay, Strobe Input to "1" Output			18	30	ns

AC Test Circuit and Waveforms



TL/F/5797–7



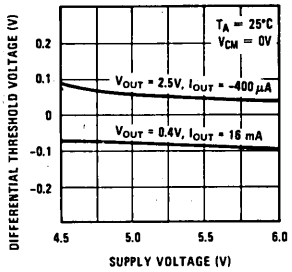
TL/F/5797–8

A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

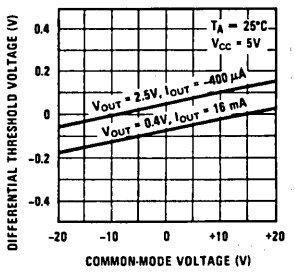
FIGURE 1

Typical Performance Characteristics (Note 3)

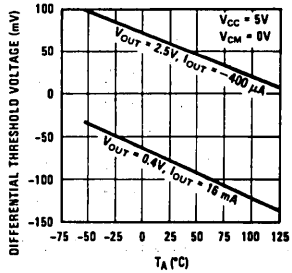
Supply Voltage Sensitivity



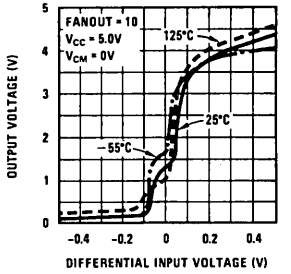
Common-Mode Voltage Sensitivity



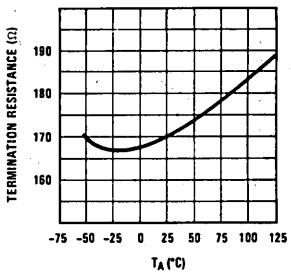
Temperature Sensitivity



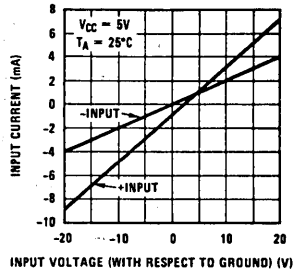
Transfer Function



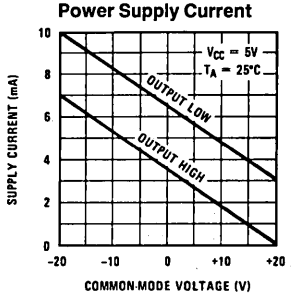
Termination Resistance



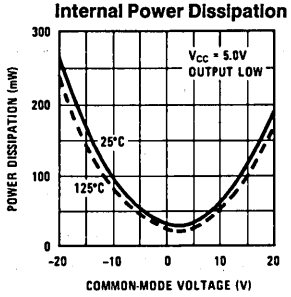
Input Characteristics



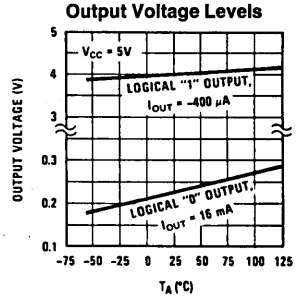
Power Supply Current



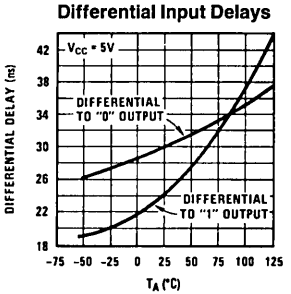
Internal Power Dissipation



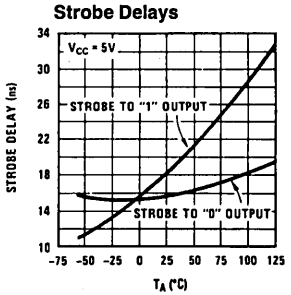
Output Voltage Levels



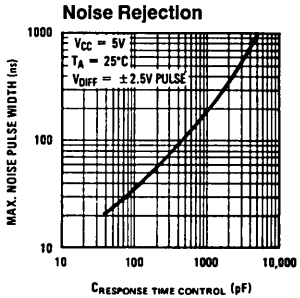
Differential Input Delays



Strobe Delays

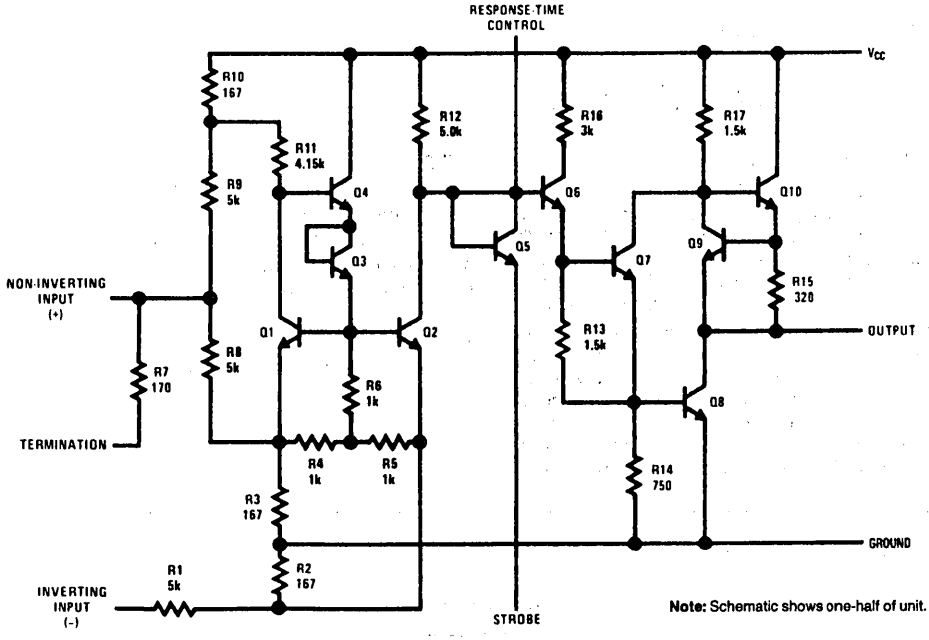


Noise Rejection



TL/F/5797–6

Schematic Diagram

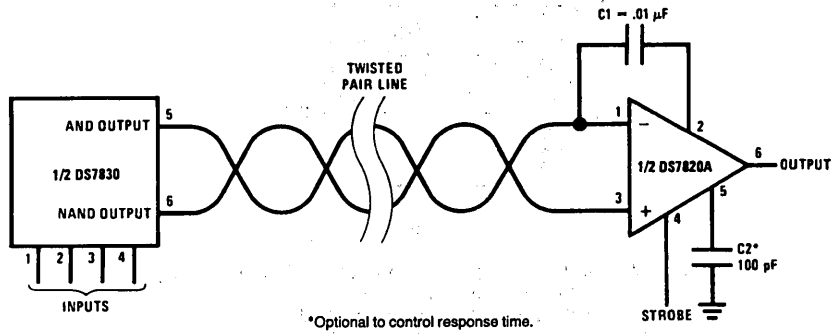


Note: Schematic shows one-half of unit.

TL/F/5797–1

Typical Applications

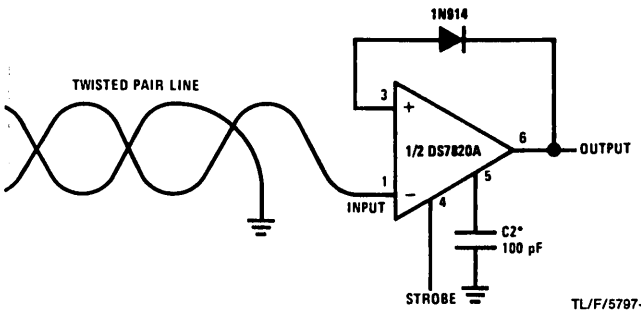
Differential Line Driver and Receiver



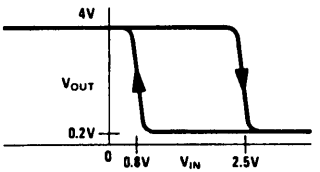
*Optional to control response time.

TL/F/5797–3

Single Ended (EIA-RS232C) Receiver with Hysteresis



TL/F/5797–4



TL/F/5797–5

(Output = "1" for Open Input)

7

National Semiconductor

DS9622 Dual Line Receiver

General Description

The DS9622 is a dual line receiver designed to discriminate a worst case logic swing of 2V from a ±10V common mode noise signal or ground shift. A 1.5V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors.

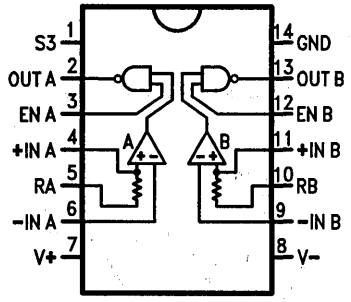
The DS9622 allows the choice of output states with the input open, without affecting circuit performance by use of S3. A 130Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output high level can be increased to 12V by tying it to a positive supply through a resistor. The output circuits allow wired-OR operation.

Features

- TTL compatible threshold voltage
- Input terminating resistors
- Choice of output state with inputs open
- TTL compatible output
- High common mode
- Wired-OR capability
- Enable inputs
- Logic compatible supply voltages

Connection Diagram

14-Lead DIP



TL/F/9760–2

Top View

For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS9622ME/883,
DS9622MJ/883 or DS9622MW/883
See NS Package Number E20A, J14A or W14B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Internal Power Dissipation (Note 5)	400 mW
V^+ to GND	−0.5V to +7.0V
Input Voltage	±15V
Voltage Applied to Outputs for Output High State	−0.5V to +13.2V
V^- to GND	−0.5V to −12V
Enable to GND	−0.5V to +15V

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Temperature, T_A	−55	+125	°C

Electrical Characteristics (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{OL}	Output Voltage LOW	$V^+ = S3 = 4.5V, V^- = -11V,$ $V_{DIFF} = 2.0V, I_{OL} = 12.4$ mA, EN = Open			0.4	V
V_{OH}	Output Voltage HIGH	$V^+ = 4.5V, V^- = -9.0V,$ $S3 = 0V, V_{DIFF} = 1.0V,$ $I_{OH} = -0.2$ mA, EN = Open		2.8		V
I_{CEX}	Output Leakage Current	$V^+ = 4.5V, V^- = -11V,$ $S3 = 0V, V_{DIFF} = 1.0V,$ $V_O = 12V$, EN = Open			200	μA
I_{OS}	Output Short Circuit Current (Note 4)	$V^+ = 5.0V, V^- = -10V,$ $V_{DIFF} = 1.0V, V_O = S3 = 0V,$ EN = Open		−3.1	−1.4	mA
I_R(EN)	Enable Input Leakage Curent	$V^+ = S3 = 4.5V, V^- = -11V,$ I_N = Open, EN = 4.0V			5.0	μA
I_F(EN	Enable Input Forward Current	$V^+ = 5.5V, V^- = -9.0V$ V_I = Open, EN = S3 = 0V		−1.5		mA
I_F(+IN)	+Input Forward Current	$V^+ = 5.0V, V^- = -10V,$ $V_I{}^+ = 0V, V_I{}^- = GND,$ EN = S3 = Open		−2.3		mA
I_F(−IN)	−Input Forward Curent	$V^+ = S3 = 5.0V, V^- = -10V,$ $V_I{}^+ = GND, V_I{}^- = 0V,$ EN = Open		−2.6		mA
V_{IL}(EN)	Input Voltage LOW	$4.5V \le V^+ \le 5.5V,$ $-11V \le V^- \le -9.0V,$ EN = Open	+25°C		1.0	V
			+125°C		0.7	V
			−55°C		1.3	V
V_{TH}	Differential Input Threshold Voltage	$4.5V, \le V^+ \le 5.5V,$ $-11V \le V^- \le -9.0V,$ EN = Open		1.0	2.0	V
V_{CM}	Common Mode Voltage	$V^+ = 5.0V, V^- = -10V,$ $1.0V \le V_{DIFF} \le 2.0V$	25°C	−10	+10	V
R_T	Terminating Resistance		25°C	91	215	Ω
I^+	Positive Supply Current	$V^+ = S3 = V_I{}^+ = 5.5V,$ $V^- = 11V, V_I{}^- = 0V$	25°C		22.9	mA
I^-	Negative Supply Current			−11.1		mA
SWITCHING CHARACTERISTICS $T_A = 25°C$						
t_{PLH}	Propagation Delay to High Level	$V^+ = 5.0V,$ $V^- = -10V,$ $0V \le V_I \le 3.0V,$ $C_L = 30$ pF (See *Figure 1*)	$R_L = 3.9$ kΩ		50	ns
t_{PHL}	Propagation Delay to Low Level		$R_L = 390Ω$		50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Rating applies to ambient temperatures up to +125°C. Above 125°C ambient, derate linearity at 120°C/W.

Switching Time Test Circuit and Waveforms

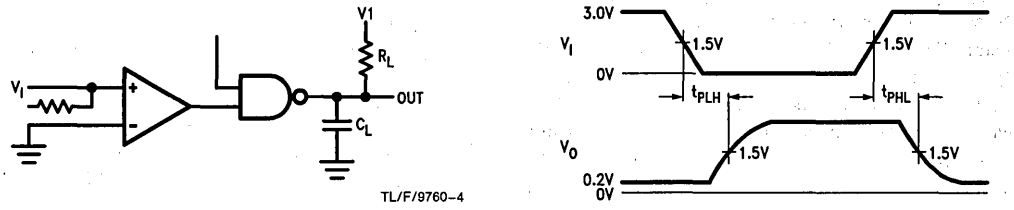
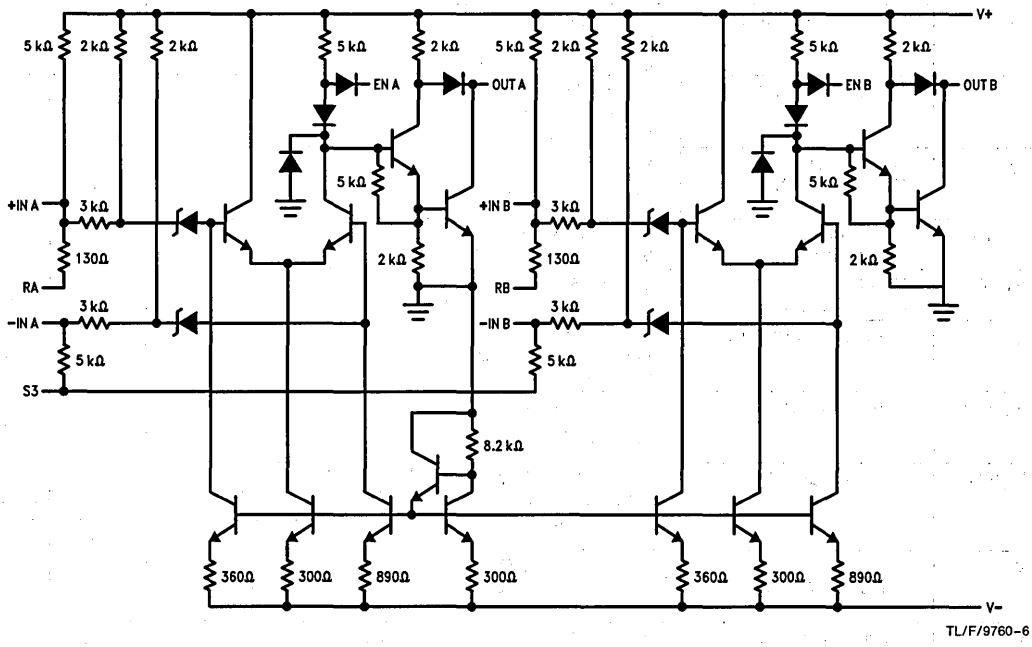


FIGURE 1

Equivalent Circuit



Typical Applications

When S3 is connected to V−, open inputs cause output to be high. When V+ = 5V, V− = −10V and S3 is connected to ground, open inputs cause output to be low.

Section 8

Application Notes

Section 8 Contents

National Semiconductor

Application Note—Selection Guide

Application Note Number AN-XXX	Title	DTP Devices Referenced	TIA/EIA Standards Referenced
AN-22	Integrated Circuits for Digital Data Transmission	DS7830/DS8830, DS7820/DS8820	
AN-108	Transmission Line Characteristics	DS7820/DS8820	
AN-214	Transmission Line Drivers and Receivers for EIA Standards, RS-422 and RS-423	DS3691, DS88LS120	422 423
AN-216	Summary of Well Known Interface Standards		ALL
AN-336	Understanding Integrated Circuit Package Power Capabilities		
AN-409	Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard	DS3695/DS3696, DS3697/DS3698	485
AN-438	Low Power RS-232C Driver and Receiver in CMOS	DS14C88, DS14C89A	232
AN-450	Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability		
AN-454	Automotive Multiplex Wiring	DS75176B DS3695	485
AN-457	High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Programs	DS8921/A, DS8922/A, DS8923/A	422
AN-643	EMI/RFI Board Design		
AN-702	Build a Directional-Sensing Bidirectional Repeater	DS75176B, DS96175C	485
AN-759	Comparing EIA-485 and EIA-422-A Line Drivers and Receivers in Multipoint Applications		422 485
AN-805	Calculating Power Dissipation for Differential Line Drivers	DS26LS31, DS96F172	422 485
AN-806	Data Transmission Lines and Their Characteristics		
AN-807	Reflections: Computations and Waveforms		
AN-808	Long Transmission Lines and Data Signal Quality		
AN-847	FAILSAFE Biasing of Differential Buses	DS3695, DS96172, DS96F172	422 485
AN-876	Inter-Operation of the DS14C335 with +5V UARTs	DS14C335	232
AN-878	Increasing System ESD Tolerance for Line Drivers and Receivers used in RS-232 Interfaces	DS1488, DS1489A	232

Application Note—Selection Guide (Continued)

Application Note Number AN-XXX	Title	DTP Devices Referenced	TIA/EIA Standards Referenced
AN-903	A Comparison of Differential Termination Techniques		422 485
AN-904	An Introduction to the Differential SCSI Interface	DS36954 DS36BC956	485
AN-912	Common Data Transmission Parameters and their Definitions		All
AN-914	Understanding Power Requirements in RS-232 Applications	DS14C335	232 562
AN-915	Automotive Physical Layer SAE J1708 and the DS36277	DS36277 DS75176B	485
AN-916	A Practical Guide to Cable Selection		All
AN-917	Popular Connector Pin Assignments for Data Communication		All

Integrated Circuits for Digital Data Transmission

National Semiconductor
Application Note 22

INTRODUCTION

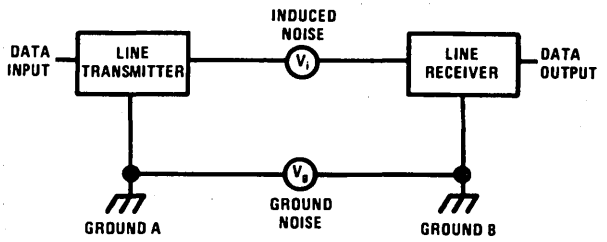
It is frequently necessary to transmit digital data in a high-noise environment where ordinary integrated logic circuits cannot be used because they do not have sufficient noise immunity. One solution to this problem, of course, is to use high-noise-immunity logic. In many cases, this approach would require worst case logic swings of 30V, requiring high power-supply voltages. Further, considerable power would be needed to transmit these voltage levels at high speed. This is especially true if the lines must be terminated to eliminate reflections, since practical transmission lines have a low characteristic impedance.

A much better solution is to convert the ground referred digital data at the transmission end into a differential signal and transmit this down a balanced, twisted-pair line. At the receiving end, any induced noise, or voltage due to ground-loop currents, appears equally on both ends of the twisted-pair line. Hence, a receiver which responds only to the differential signal from the line will reject the undesired signals even with moderate voltage swings from the transmitter.

Figure 1 illustrates this situation more clearly. When ground is used as a signal return as in *Figure 1a*, the voltage seen at the receiving end will be the output voltage of the transmitter plus any noise voltage induced in the signal line. Hence, the noise immunity of the transmitter-receiver combination must be equal to the maximum expected noise from both sources.

The differential transmission scheme diagrammed in *Figure 1b* solves this problem. Any ground noise or voltage induced on the transmission lines will appear equally on both inputs of the receiver. The receiver responds only to the differential signal coming out of the twisted-pair line and delivers a single-ended output signal referred to the ground at the receiving end. Therefore, extremely high noise immunities are not needed; and the transmitter and receiver can be operated from the same supplies as standard integrated logic circuits.

This article describes the operation and use of a line driver and line receiver for transmission systems using twisted-pair lines. The transmitter provides a buffered differential output from a DTL or TTL input signal. A four-input gate is included on the input so that the circuit can also perform logic. The receiver detects a zero crossing in the differential input voltage and can directly drive DTL or TTL integrated circuits at the receiving end. It also has strobe capability to blank out unwanted input signals. Both the transmitter and the receiver incorporate two independent units on a single silicon chip.



a. Single-Ended System

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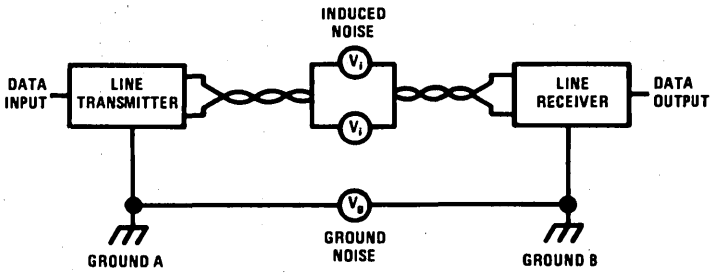

b. Difference System

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FIGURE 1. Comparing Differential and Single-Ended Data Transmission

LINE DRIVER

Figure 2 shows a schematic diagram of the line transmitter. The circuit has a marked resemblance to a standard TTL buffer. In fact, it is possible to use a standard dual buffer as a transmitter. However, the DS7830 incorporates additional features. For one, the output is current limited to protect the driver from accidental shorts in the transmission lines. Secondly, diodes on the output clamp sever voltage transients that may be induced into the transmission lines. Finally, the circuit has internal inversion to produce a differential output signal, reducing the skew between the outputs and making the output state independent of loading.

As can be seen from the upper half of *Figure 2*, a quadruple-emitter input transistor, Q9, provides four logic inputs to the transmitter. This transistor drives the inverter stage formed by Q10 and Q11 to give a NAND output. A low state logic input on any of the emitters of Q9 will cause the base drive to be removed from Q10, since Q9 will be saturated by current from R8, holding the base of Q10 near ground. Hence, Q10 and Q11 will be turned off; and the output will be in a high state. When all the emitters of Q9 are at a one logic level, Q10 receives base drive from R8 through the forward biased collector-base junction of Q9. This saturates Q10 and also Q11, giving a low output state. The input voltage at which the transition occurs is equal to the sum of the emitter-base turn on voltages of Q10 and Q11 minus the saturation voltage of Q9. This is about 1.4V at 25°C.

A standard "totem-pole" arrangement is used on the output stage. When the output is switched to the high state, with Q10 and Q11 cut off, current is supplied to the load by Q13 and Q14 which are connected in a modified Darlington configuration. Because of the high compound current gain of these transistors, the output resistance is quite low and a large load current can be supplied. R10 is included across the emitter-base junction of Q13 both to drain off any collector-base leakage current in Q13 and to discharge the collector-base capacitance of Q13 when the output is switched to

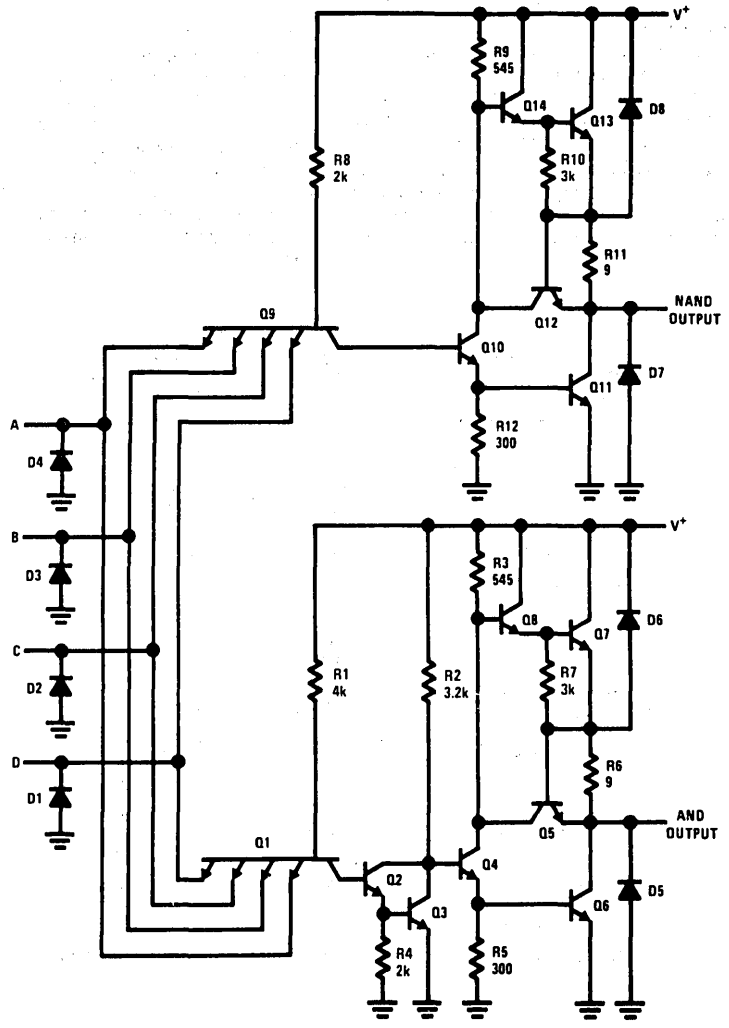

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FIGURE 2. Schematic Diagram of the DS7830 Line Driver

the low state. In the high state, the output level is approximately two diode drops below the positive supply, or roughly 3.6V at 25°C with a 5.0V supply.

With the output switched into the low state, Q10 saturates, holding the base of Q14 about one diode drop above ground. This cuts off Q13. Further, both the base current and the collector current of Q10 are driven into the base of Q11 saturating it and giving a low-state output of about 0.1V. The circuit is designed so that the base of Q11 is supplied 6 mA, so the collector can drive considerable load current before it is pulled out of saturation.

The primary purpose of R12 is to provide current to remove the stored charge in Q11 and charge its collector-base capacitance when the circuit is switched to the high state. Its value is also made less than R9 to prevent supply current transients which might otherwise occur* when the power supply is coming up to voltage.

The lower half of the transmitter in *Figure 2* is identical to the upper, except that an inverter stage has been added. This is needed so that an input signal which drives the output of the upper half positive will drive the lower half negative, and vice versa, producing a differential output signal. Transistors Q2 and Q3 produce the inversion. Even though the current gain is not necessarily needed, the modified Darlington connection is used to produce the proper logic transition voltage on the input of the transmitter. Because of the low load capacitance that the inverter sees when it is completely within the integrated circuit, it is extremely fast, with a typical delay of 3 ns. This minimizes the skew between the outputs.

One of the schemes used when dual buffers are employed as a differential line driver is to obtain the NAND output in the normal fashion and provide the AND output by connecting the input of the second buffer to the NAND output. Using an internal inverter has some distinct advantages over this: for one, capacitive loads which slow down the response of the NAND output will not introduce a time skew between the two outputs; secondly, line transients on the NAND output will not cause an unwanted change of state on the AND output.

Clamp diodes, D1 through D4, are added on all inputs to clamp undershoot. This undershoot and ringing can occur in TTL systems because the rise and fall times are extremely short.

Output-current limiting is provided by adding a resistor and transistor to each of the complementary outputs. Referring again to *Figure 2*, when the current on the NAND output increases to a value where the voltage drop across R11 is sufficient to turn on Q12, the short circuit protection comes into effect. This happens because further increases in output current flow into the base of Q12 causing it to remove base drive from Q14 and, therefore, Q13. Any substantial increase in output current will then cause the output voltage to collapse to zero. Since the magnitude of the short circuit depends on the emitter base turn-on voltage of Q12, this current has a negative temperature coefficient. As the chip temperature increases from power dissipation, the available short circuit current is reduced. The current limiting also serves to control the current transient that occurs when the output is going through a transition with both Q11 and Q13 turned on.

*J. Kalb, "Design Considerations for a TTL Gate", *National Semiconductor* TP-6, May, 1968.

The AND output is similarly protected by R6 and Q5, which limits the maximum output current to about 100 mA, preventing damage to the circuit from shorts between the outputs and ground.

The current limiting transistors also serve to increase the low state output current capability under severe transient conditions. For example, when the current into the NAND output becomes so high as to pull Q11 out of saturation, the output voltage will rise to two diode drops above ground. At this voltage, the collector-base junction of Q12 becomes forward biased and supplies additional base drive to Q11 through Q10 which is saturated. This minimizes any further increase in output voltage.

When either of the outputs are in the high state, they can drive a large current towards ground without a significant change in output voltage. However, noise induced on the transmission line which tries to drive the output positive will cut it off since it cannot sink current in this state. For this reason, D6 and D8 are included to clamp the output and keep it from being driven much above the supply voltage, as this could damage the circuit.

When the output is in a low state, it can sink a lot of current to clamp positive-going induced voltages on the transmission line. However, it cannot source enough current to eliminate negative-going transients so D5 and D7 are included to clamp those voltages to ground.

It is interesting to note that the voltage swing produced on one of the outputs when the clamp diodes go into conduction actually increases the differential noise immunity. For example with no induced common mode current, the low-state output will be a saturation voltage above ground while the high output will be two diode drops below the positive supply voltage. With positive-going common mode noise on the line, the low output remains in saturation; and the high output is clamped at a diode drop above the positive supply. Hence, in this case, the common mode noise increases the differential swing by three diode drops.

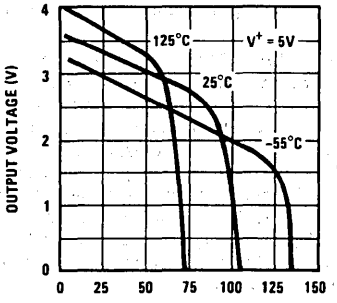

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FIGURE 3. High State Output Voltage as a Function of Output Current

Having explained the operation of the line driver, it is appropriate to look at the performance in more detail. *Figure 3* shows the high-state output characteristics under load. Over the normal range of output currents, the output resistance is about 10Ω. With higher output currents, the short circuit protection is activated, causing the output voltage to drop to zero. As can be seen from the figure, the short-circuit current decreases at higher temperatures to minimize the possibility of over-heating the integrated circuit.

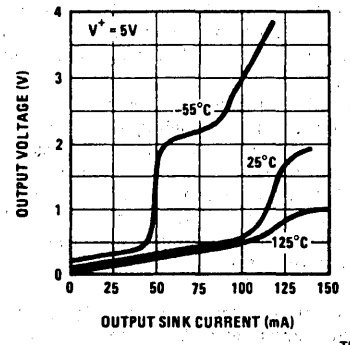

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FIGURE 4. Low-State Output Current as a Function of Output Current

Figure 4 is a similar graph of the low-state output characteristics. Here, the output resistance is about 5Ω with normal values of output current. With larger currents, the output transistor is pulled out of saturation; and the output voltage increases. This is more pronounced at −55°C where the transistor current gain is the lowest. However, when the output voltage rises about two diode drops above ground, the collector-base junction of the current-limit transistor becomes forward biased, providing additional base drive for the output transistor. This roughly doubles the current available for clamping positive common-mode transients on the twisted-pair line. It is interesting to note that even though the output level increases to about 2V under this condition, the differential noise immunity does not suffer because the high-state output also increases by about 3V with positive going common-mode transients.

It is clear from the figure that the low state output current is not effectively limited. Therefore, the device can be damaged by shorts between the output and the 5V supply. However, protection against shorts between outputs or from the outputs to ground is provided by limiting the high-state current.

The curves in *Figures 3* and *4* demonstrate the performance of the line driver with large, capacitively-coupled common-mode transients, or under gross overload conditions. *Figure 5* shows the ability of the circuit to drive a differential load: that is, the transmission line. It can be seen that for output currents less than 35 mA, the output resistance is approximately 15Ω. At both temperature extremes, the output falls off at high currents. At high temperatures, this is caused by current limiting of the high output state. At low temperatures, the fall off of current gain in the low-state output transistor produces this result.

Load lines have been included on the figure to show the differential output with various load resistances. The output swing can be read off from the intersection of the output characteristic with the load line. The figure shows that the driver can easily handle load resistances greater than 100Ω.

This is more than adequate for practical, twisted-pair lines.

Figure 6 shows the no load power dissipation, for one-half of the dual line driver, as a function of frequency. This information is important for two reasons. First, the increase in

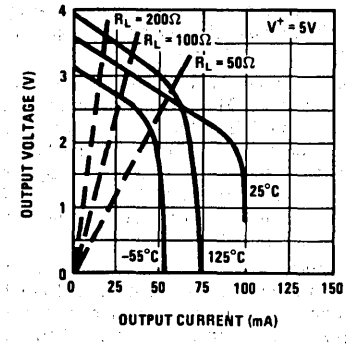

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FIGURE 5. Differential Output Voltage as a Function of Differential Output Current

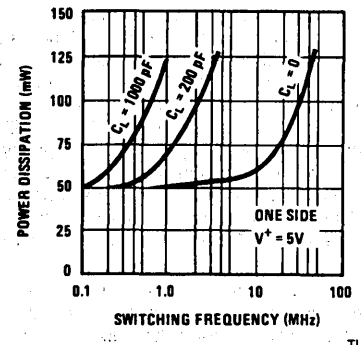

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FIGURE 6. Power Dissipation as a Function of Switching Frequency

power dissipation at high frequencies must be added to the excess power dissipation caused by the load to determine the total package dissipation. Second, and more important, it is a measure of the "glitch" current which flows from the positive supply to ground through the output transistors when the circuit is going through a transition. If the output stage is not properly designed, the current spikes in the power supplies can become quite large; and the power dissipation can increase by as much as a factor of five between 100 kHz and 10 MHz. The figure shows that, with no capacitive loading, the power increases with frequencies as high as 10 MHz is almost negligible. However, with large capacitive loads, more power is required.

The line receiver is designed to detect a zero crossing in the differential output of the line driver. Therefore, the propagation time of the driver is measured as the time difference between the application of a step input and the point where the differential output voltage crosses zero. A plot of the propagation time over temperature is shown in *Figure 7*. This delay is added directly to the propagation time of the transmission line and the delay of the line receiver to determine the total data-propagation time. However, in most cases, the delay of the driver is small, even by comparison to the uncertainties in the other delays.

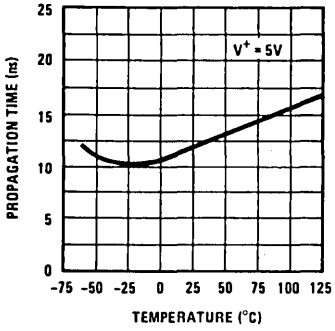

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FIGURE 7. Propagation Time as a Function of Temperature

To summarize the characteristics of the DS7830 line driver, the input interfaces directly with standard TTL circuits. It presents a load which is equivalent to a fan out of 3 to the circuit driving it, and it operates from the 5.0V, ±10% logic supplies. The output can drive low impedance lines down to 50Ω and capacitive loads up to 5000 pF. The time skew between the outputs is minimized to reduce radiation from the twisted-pair lines, and the circuit is designed to clamp common mode transients coupled into the line. Short circuit protection is also provided. The integrated circuit consists of two independent drivers fabricated on a 41 x 53 mil-square die using the standard TTL process. A photomicrograph of the chip is shown in *Figure 8*.

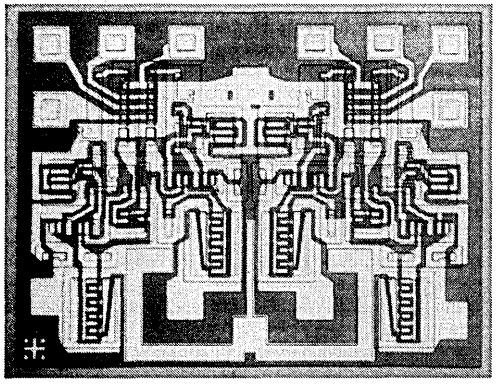

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FIGURE 8. Photomicrograph of the DS7830 Dual Line Driver

LINE RECEIVER

As mentioned previously, the function of the line receiver is to convert the differential output signal of the line driver into a single ended, ground-referred signal to drive standard digital circuits on the receiving end. At the same time it must reject the common mode and induced noise on the transmission line.

Normally this would not be too difficult a task because of the large signal swings involved. However, it was considered important that the receiver operate from the +5V logic supply without requiring additional supply voltages, as do most other line receiver designs. This complicates the situation because the receiver must operate with ±15V input signals which are considerably greater than the operating supply voltage.

The large common mode range over which the circuit must work can be reduced with an attenuator on the input of the receiver. In this design, the input signal is attenuated by a factor of 30. Hence, the ±15V common mode voltage is reduced to ±0.5V, which can be handed easily by circuitry operating from a 5V supply. However, the differential input signal, which can go down as low as ±2.4V in the worst case, is also reduced to ±80 mV. Hence, it is necessary to employ a fairly accurate zero crossing detector in the receiver.

System requirements dictated that the threshold inaccuracy introduced by the zero crossing detector be less than 17 mV. In principle, this accuracy requirement should not pose insurmountable problems because it is a simple matter to make well matched parts in an integrated circuit.

Figure 9 shows a simplified schematic diagram of the circuit configuration used for the line receiver. The input signal is attenuated by the resistive dividers R1-R2 and R8-R3. This attenuated signal is fed into a balanced DC amplifier, operating in the common base configuration. This input amplifier, consisting of Q1 and Q2, removes the common mode component of the input signal. Further, it delivers an output signal at the collector of Q2, which is nearly equal in amplitude to the original differential input signal. this output signal is buffered by Q6 and drives an output amplifier, Q8. The output stage drives the logic load directly.

An understanding of the circuit can be obtained by first considering the input stage. Assuming high current gains and neglecting the voltage drop across R3, the collector current of Q1 will be:

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R11} \quad (1)$$

With equal emitter-base voltages for all transistors, this becomes:

$$I_{C1} = \frac{V^+ - 3V_{BE}}{R11} \quad (2)$$

The output voltage at the collector of Q2 will be:

$$V_{C2} = V^+ - I_{C2}R12 \quad (3)$$

When the differential input voltage to the receiver is zero, the voltages presented to the emitters of Q1 and Q2 will be equal. If Q1 and Q2 are matched devices, which is easy to arrange when they are fabricated close together on a single silicon chip, their collector currents will be equal with zero input voltage. Hence, the output voltage from Q2 can be determined by substituting (2) into (3):

$$V_{C2} = V^+ - \frac{R12}{R11}(V^+ - 3V_{BE}) \quad (4)$$

For R11 = R12, this becomes:

$$V_{C2} = 3V_{BE}$$

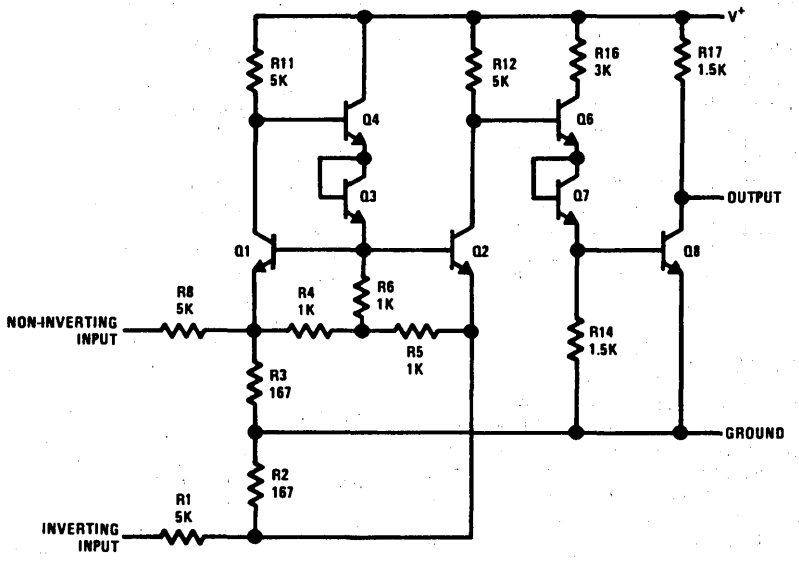

FIGURE 9. Simplified Schematic of the Line Receiver

The voltage on the base of Q6 will likewise be $3V_{BE}$ when the output is on the verge of switching from a zero to a one state. A differential input signal which causes Q2 to conduct more heavily will then make the output go high, while an input signal in the opposite direction will cause the output to saturate.

It should be noted that the balance of this circuit is not affected by absolute values of components—only by how well they match. Nor is it affected by variations in the positive supply voltage, so it will perform well with standard logic supply voltages between 4.5V and 5.5V. In addition, component values are chosen so that the collector currents of Q4 and Q6 are equal. As a result, the base currents of Q4 and Q6 do not upset the balance of the input stage. This means that circuit performance is not greatly affected by production or temperature variations in transistor current gain.

A complete schematic of the line receiver, shown in *Figure 10*, shows several refinements of the basic circuit which are needed to secure proper operation under all conditions. For one, the explanation of the simplified circuit ignores the fact that the collector current of Q1 will be affected by common mode voltage developed across R3. This can give a 0.5V threshold error at the extremes of the ±15V common mode range. To compensate for this, a separate divider, R9 and R10, is used to maintain a constant collector current in Q1 with varying common mode signals. With an increasing common mode voltage on the non-inverting input, the voltage on the emitter of Q1 will increase. Normally, this would cause the voltage across R11 to decrease, reducing the collector current of Q1. However, the increasing common mode signal also drives the top end of R11 through R9 and R10 so as to hold the voltage drop across R11 constant.

In addition to improving the common mode rejection, R9 also forces the output of the receiver into the high state when nothing is connected to the input lines. This means that the output will be in a pre-determined state when the transmission cables are disconnected.

A diode connected transistor, Q5, is also added in the complete circuit to provide strobe capability. With a logic zero on the strobe terminal, the output will be high no matter what the input signal is. With the strobe, the receiver can be made immune to any noise signals during intervals where no digital information is expected. The output state with the strobe on is also the same as the output state with the input terminals open.

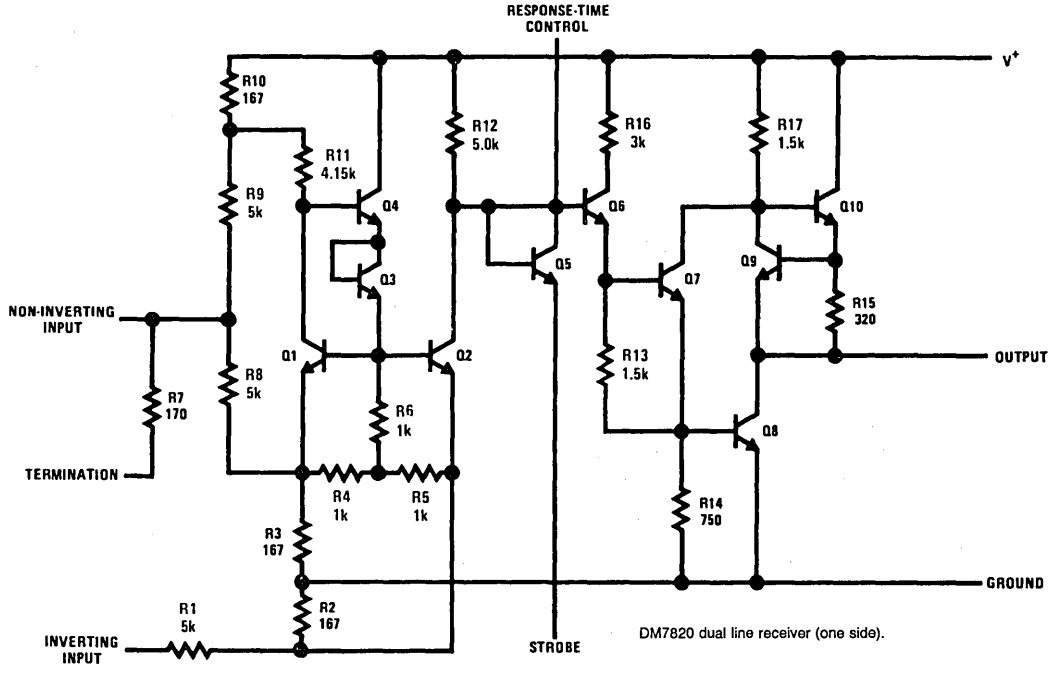

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FIGURE 10. Complete Schematic of One Half of the DS7820 Line Receiver

The collector of Q2 is brought out so that an external capacitor can be used to slow down the receiver to where it will not respond to fast noise spikes. This capacitor, which is connected between the response-time-control terminal and ground, does not give exactly-symmetrical delays. The delay for input signals which produce a positive-going output will be less than for input signals of opposite polarity. This happens because the impedance on the collector of Q2 drops as Q6 goes into saturation, reducing the effectiveness of the capacitor.

Another difference in the complete circuit is that the output stage is improved both to provide more gain and to reduce the output resistance in the high output state. This was accomplished by adding Q9 and Q10. When the output stage is operating in the linear region, that is, on the verge of switching to either the high or the low state, Q9 and Q10 form sort of an active collector load for Q8. The current through R15 is constant at approximately 2 mA as the output voltage changes through the active region. Hence, the percentage change in the collector current of Q8 due to the voltage change across R17 is made smaller by this pre-bias current; and the effective stage gain is increased.

With the output in the high state (Q8 cut off), the output resistance is equal to R15, as long as the load current is less than 2 mA. When the load current goes above this value, Q9 turns on; and the output resistance increases to 1.5k, the value of R17.

This particular output configuration gives a higher gain than either a standard DTL or TTL output stage. It can also drive enough current in the high state to make it compatible with TTL, yet outputs can be wire OR'ed as with DTL.

Remaining details of the circuit are that Q7 is connected as an emitter follower to make the circuit even less sensitive to transistor current gains. R16 limits the base drive to Q7 with the output saturated, while R17 limits the base drive to the output transistor, Q8. A resistor, R7, which can be used to terminate the twisted-pair line is also included on the chip. It is not connected directly across the inputs. Instead, one end is left open so that a capacitor can be inserted in series with the resistor. The capacitor significantly reduces the power dissipation in both the line transmitter and receiver, especially in low-duty-cycle applications, by terminating the line at high frequencies but blocking steady-state current flow in the terminating resistor.

Since line receivers are generally used repetitively in a system, the DS7820 has been designed with two independent receivers on a single silicon chip. The device is fabricated on a 41 x 49 mil-square die using the standard six mask planar-epitaxial process. The processing employed is identical to that used on TTL circuits, and the design does not impose any unusual demands on the processing. It is only required that various parts within the circuit match well, but this is easily accomplished in a monolithic integrated circuit without any special effort in manufacturing. A photomicrograph of the integrated circuit chip is shown in *Figure 11*.

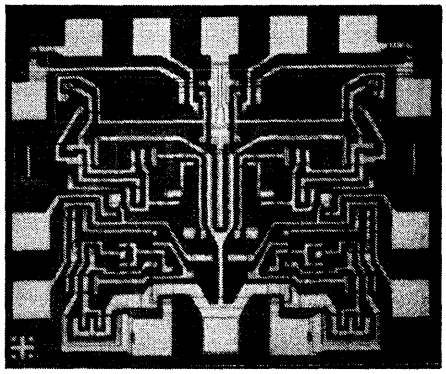

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FIGURE 11. Photomicrograph of the DS7820 Dual Line Receiver

The only components in the circuit which see voltages higher than standard logic circuits are the resistors used to attenuate the input signal. These resistors, R1, R7, R8 and R9, are diffused into a separate, floating, N-type isolation tub, so that the higher voltage is not seen by any of the transistors. For a ±15V input voltage range, the breakdown voltages required for the collector-isolation and collector-base diodes are only 15V and 19V, respectively. These breakdown voltages can be achieved readily with standard digital processing.

The purpose of the foregoing was to provide some insight into circuit operation. A more exact mathematical analysis of the device is developed in Appendix A.

RECEIVER PERFORMANCE

The characteristics of the line receiver are described graphically in *Figures 12* through *18*. *Figure 12* illustrates the effect of supply voltage variations on the threshold accuracy. The upper curve gives the differential input voltage required to hold the output at 2.5V while it is supplying 200 μA to the digital load. The lower curve shows the differential input needed to hold the output at 0.4V while it sinks 3.5 mA from the digital load. This load corresponds to a worst case fanout of 2 with either DTL or TTL integrated circuits. The data shows that the threshold accuracy is only affected by ±60 mV for a ±10% change in supply voltage. Proper operation can be secured over a wider range of supply voltages, although the error becomes excessive at voltages below 4V.

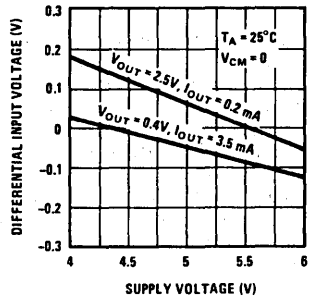

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FIGURE 12. Differential Input Voltage Required for High or Low Output as a Function of Supply Voltage

Figure 13 is a similar plot for varying common mode input voltage. Again the differential input voltages are given for high and low states on the output with a worst case fanout of 2. With precisely matched components within the integrated circuit, the threshold voltage will not change with common mode voltage. The mismatches typically encountered give a threshold voltage change of ±100 mV over a ±20V common mode range. This change can have either a positive slope or a negative slope.

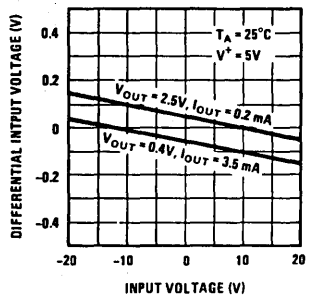

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FIGURE 13. Differential Input Voltage Required for High or Low Output as a Function of Common Mode Voltage

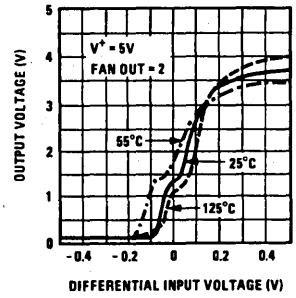

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FIGURE 14. Voltage Transfer Function

The transfer function of the circuit is given in *Figure 14*. The loading is for a worst case fanout of 2. The digital load is not linear, and this is reflected as a non-linearity in the transfer function which occurs with the output around 1.5V. These transfer characteristics show that the only significant effect of temperature is a reduction in the positive swing at −55°C. However, the voltage available remains well above the 2.5V required by digital logic.

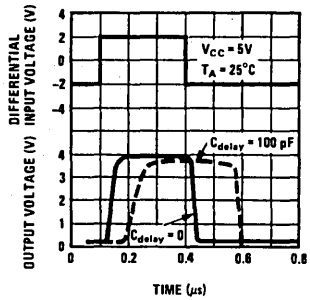

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FIGURE 15. Response Time with and without an External Delay Capacitor

Figure 15 gives the response time, or propagation delay, of the receiver. Normally, the delay through the circuit is about 40 ns. As shown, the delay can be increased, by the addition of a capacitor between the response-time terminal and ground, to make the device immune to fast noise spikes on the input. The delay will generally be longer for negative going outputs than for positive going outputs.

Under normal conditions, the power dissipated in the receiver is relatively low. However, with large common mode input voltages, dissipation increases markedly, as shown in *Figure 16*. This is of little consequence with common mode transients, but the increased dissipation must be taken into account when there is a DC difference between the grounds of the transmitter and the receiver. It is important to note that *Figure 16* gives the dissipation for one half the dual receiver. The total package dissipation will be twice the values given when both sides are operated under identical conditions.

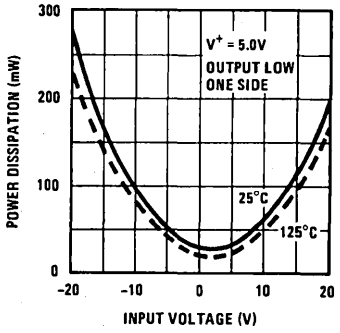

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FIGURE 16. Internal Power Dissipation as a Function of Common Mode Input Voltage

Figure 17 shows that the power supply current also changes with common mode input voltage due to the current drawn out of or fed into the supply through R9. The supply current reaches a maximum with negative input voltages and can actually reverse with large positive input voltages. The figure also shows that the supply current with the output switched into the low state is about 3 mA higher than with a high output.

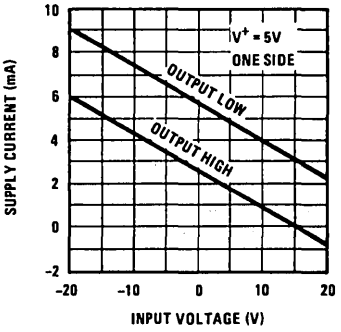

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FIGURE 17. Power Supply Current as a Function of Common Mode Input Voltage

The variation of the internal termination resistance with temperature is illustrated in *Figure 18*. Taking into account the initial tolerance as well as the change with temperature, the termination resistance is by no means precise. Fortunately, in most cases, the termination resistance can vary appreciably without greatly affecting the characteristics of the transmission line. If the resistor tolerance is a problem, however, an external resistor can be used in place of the one provided within the integrated circuit.

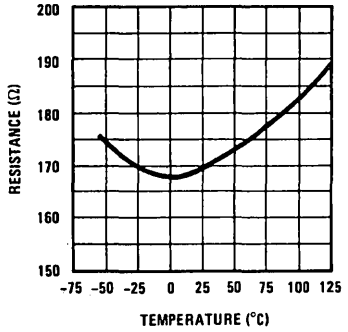

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FIGURE 18. Variation of Termination Resistance with Temperature

DATA TRANSMISSION

The interconnection of the DS7830 line driver with the DS7820 line receiver is shown in *Figure 19*. With the exception of the transmission line, the design is rather straightforward. Connections on the input of the driver and the output or strobe of the receiver follow standard design rules for DTL or TTL integrated logic circuits. The load presented by the driver inputs is equal to 3 standard digital loads, while the receiver can drive a worst-case fanout of 2. The load presented by the receiver strobe is equal to one standard load.

The purpose of C1 on the receiver is to provide DC isolation of the termination resistor for the transmission line. This capacitor can both increase the differential noise immunity, by reducing attenuation on the line, and reduce power dissipation in both the transmitter and receiver. In some applications, C1 can be replaced with a short between Pins 1 and 2, which connects the internal termination resistor of the DS7820 directly across the line. C2 may be included, if necessary, to control the response time of the receiver, making it immune to noise spikes that may be coupled differentially into the transmission lines.

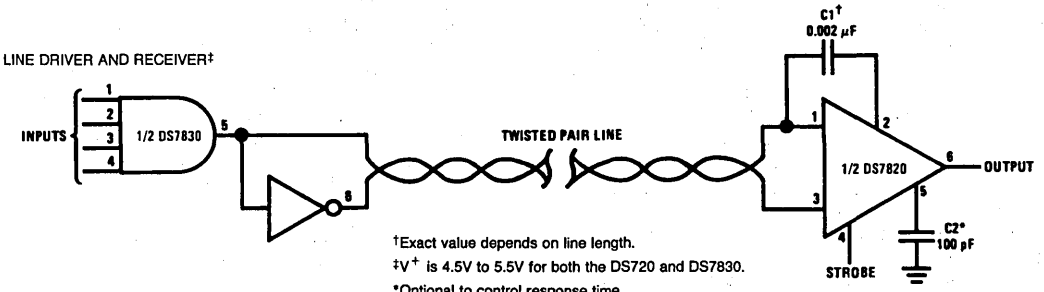

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FIGURE 19. Interconnection of the Line Driver and Line Receiver

The effect of termination mismatches on the transmission line is shown in *Figure 20*. The line was constructed of a twisted pair of No. 22 copper conductors with a characteristic impedance of approximately 170Ω. The line length was about 150 ns and it was driven directly from a DS7830 line driver. The data shows that termination resistances which are a factor of two off the nominal value do not cause significant reflections on the line. The lower termination resistors do, however, increase the attenuation.

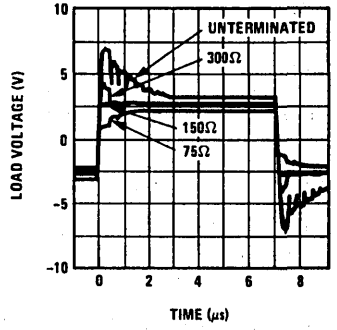

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FIGURE 20. Transmission Line Response with Various Termination Resistances

Figure 21 gives the line-transmission characteristics with various termination resistances when a DC isolation capacitor is used. The line is identical to that used in the previous example. It can be seen that the transient reponse is nearly the same as a DC terminated line. The attenuation, on the other hand, is considerably lower, being the same as an unterminated line. An added advantage of using the isolation capacitor is that the DC signal current is blocked from the termination resistor which reduces the average power drain of the driver and the power dissipation in both the driver and receiver.

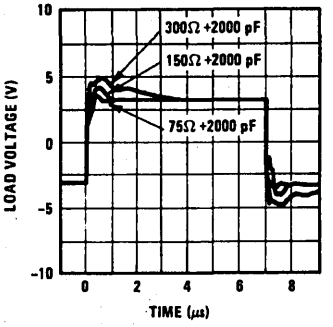

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FIGURE 21. Line Response for Various Termination Resistances with a DC Isolation Capacitor

The effect of different values of DC isolation capacitors is illustrated in *Figure 22*. This shows that the RC time constant of the termination resistor/isolation capacitor combination should be 2 to 3 times the line delay. As before, this data was taken for a 150 ns long line.

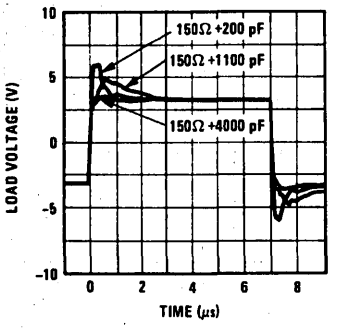

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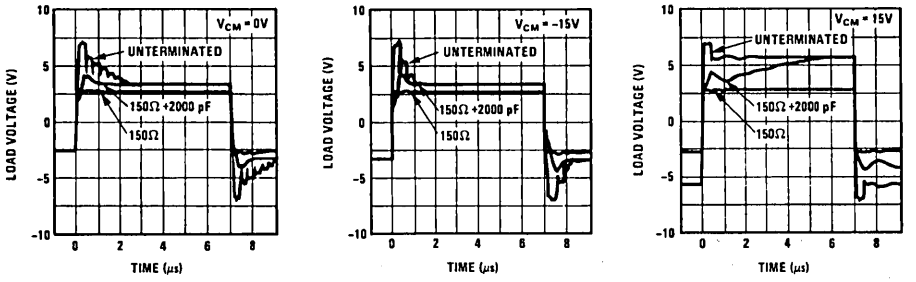
FIGURE 22. Response of Terminated Line with Different DC Isolation Capacitors



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a. V_{CM} = 0V b. V_{CM} = −15V c. V_{CM} = 15V

FIGURE 23. Line Response With Different Terminations and Common Mode Input Voltages

In *Figure 23*, the influence of a varying ground voltage between the transmitter and the receiver is shown. The difference in the characteristics arises because the source resistance of the driver is not constant under all conditions. The high output of the transmitter looks like an open circuit to voltages reflected from the receiving end of the transmission line which try to drive it higher than its normal DC state. This condition exists until the voltage at the transmitting end becomes high enough to forward bias the clamp diode on the 5V supply. Much of the phenomena which does not follow simple transmission-line theory is caused by this. For example, with an unterminated line, the overshoot comes from the reflected signal charging the line capacitance to where the clamp diodes are forward biased. The overshoot then decays at a rate determined by the total line capacitance and the input resistance of the receiver.

When the ground on the receiver is 15V more negative than the ground at the transmitting end, the decay with an unterminated line is faster, as shown in *Figure 23b*. This occurs because there is more current from the input resistor of the receiver to discharge the line capacitance. With a terminated line, however, the transmission characteristics are the same as for equal ground voltages because the terminating resistor keeps the line from getting charged.

Figure 23c gives the transmission characteristics when the receiver ground is 15V more positive than the transmitter ground. When the line is not terminated, the differential voltage swing is increased because the high output of the driver will be pulled against the clamp diodes by the common mode input current of the receiver. With a DC isolation capacitor, the differential swing will reach this same value with a time constant determined by the isolation capacitor and the input resistance of the receiver. With a DC coupled termination, the characteristics are unchanged because the differential load current is large by comparison to the common mode current so that the output transistors of the driver are always conducting.

The low output of the driver can also be pulled below ground to where the lower clamp diode conducts, giving effects which are similar to those described for the high output. However, a current of about 9 mA is required to do this, so it does not happen under normal operating conditions.

To summarize, the best termination is an RC combination with a time constant approximately equal to 3 times the transmission-line delay. Even though its value is not precisely determined, the internal termination resistor of the integrated circuit can be used because the line characteristics are not greatly affected by the termination resistor.

The only place that an RC termination can cause problems is when the data transmission rate approaches the line delay and the attenuation down the line (terminated) is greater than 3 dB. This would correspond to more than 1000 ft. of twisted-pair cable with No. 22 copper conductors. Under these conditions, the noise margin can disappear with low-duty-cycle signals. If this is the case, it is best to operate the twisted-pair line without a termination to minimize transmission losses. Reflections should not be a problem as they will be absorbed by the line losses.

CONCLUSION

A method of transmitting digital information in high-noise environments has been described. The technique is a much more attractive solution than high-noise-immunity logic as it has lower power consumption, provides more noise rejection, operates from standard 5V supplies, and is fully compatible with almost all integrated logic circuits. An additional advantage is that the circuits can be fabricated with integrated circuit processes used for standard logic circuits.

APPENDIX A

LINE RECEIVER

Design Analysis

The purpose of this appendix is to derive mathematical expressions describing the operation of the line receiver. It will be shown that the performance of the circuit is not greatly affected by the absolute value of the components within the integrated circuit or by the supply voltage. Instead, it depends mostly on how well the various parts match.

The analysis will assume that all the resistors are well matched in ratio and that the transistors are likewise matched, since this is easily accomplished over a broad temperature range with monolithic construction. However, the effects of component mismatching will be discussed where important. Further, large transistor current gains will be assumed, but it will be pointed out later that this is valid for current gains greater than about 10.

A schematic diagram of the DS7820 line receiver is shown in *Figure A-1*. Referring to this circuit, the collector current of the input transistor is given by

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R9//R10 + R11 + R3//R8} - \frac{\frac{R3}{R4 + 2R6 + R3} V_{BE1} - \frac{R3//R11}{R8 + R3//R1} V_{IN}}{R9//R10 + R11 + R3//R8} + \frac{(V_{IN} - V^+)\frac{R10//R11}{R9 + R10//R11}}{R9//R10 + R11 + R3//R8} \quad (A.1)$$

where V_{IN} is the common mode input voltage and $R_a//R_b$ denotes the parallel connection of the two resistors. In Equation (A.1), R8 = R9, R3 = R10, R10 ≪ R11, R9 ≫ R10, R3 ≪ R11, R8 ≫ R3 and

$$\frac{R3}{R4 + 2R6 + R3} \ll 3$$

so it can be reduced to

$$I_{C1} = \frac{V^+ - 3V_{BE} - \frac{R10}{R9} V^+}{R10 + R11 + R3} \quad (A.2)$$

which shows that the collector current of Q1 is not affected by the common mode voltage.

The output voltage on the collector of Q2 is

$$V_{C2} = V^+ - I_{C2}R12 \quad (A.3)$$

For zero differential input voltage, the collector currents of Q1 and Q2 will be equal so Equation (A.3) becomes

$$V_{C2} = V^+ - \frac{R12\left(V^+ - 3V_{BE} - \frac{R10}{R9} V^+\right)}{R10 + R11 + R3} \quad (A.4)$$

It is desired that this voltage be $3V_{BE}$ so that the output stage is just on the verge of switching with zero input. Forcing this condition and solving for R12 yields

$$R12 = (R10 + R11 + R3)\frac{V^+ - 3V_{BE}}{V^+ - 3V_{BE} - \frac{R10}{R9} V^+} \quad (A.5)$$

This shows that the optimum value of R12 is dependent on supply voltage. For a 5V supply it has a value of 4.7 kΩ. Substituting this and the other component values into (A.4),

$$V_{C2} = 2.83V_{BE} + 0.081V^+, \quad (A.6)$$

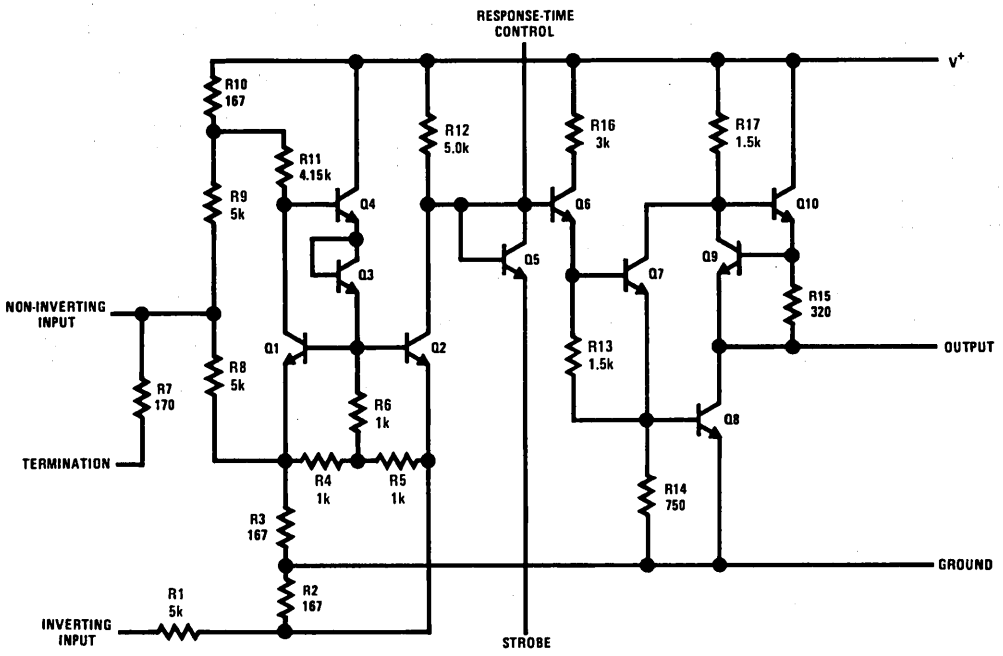

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FIGURE A-1. Schematic Diagram of One Half of the DS7820 Line Receiver

which shows that the voltage on the collector of Q2 will vary by about 80 mV for a 1V change in supply voltage.

The next step in the analysis is to obtain an expression for the voltage gain of the input stage.

An equivalent circuit of the input stage is given in *Figure A-2.* Noting that R6 = R7 = R8 and R2 ≅ 0.1 (R6 + R7//R8), the change in the emitter current of Q1 for a change in input voltage is

$$\Delta I_{E2} = \frac{0.9\,R2}{R1\,(0.9\,R2 + R_{E2})}\,\Delta V_{IN} \qquad (A.7)$$

Hence, the change in output voltage will be

$$\Delta V_{OUT} = \alpha I_{E2} R12$$

$$= \frac{0.9\,\alpha\,R2\,R12}{R1\,(0.9\,R2 + R_{E2}}\,\Delta V_{IN} \qquad (A.8)$$

Since $\alpha \cong 1$, the voltage gain is

$$A_{V1} = \frac{0.9\,R2\,R12}{R1\,(0.9\,R2 + R_{E2})} \qquad (A.9)$$

The emitter resistance of Q2 is given by

$$R_{E2} = \frac{kT}{qI_{C2}} \qquad (A.10)$$

where

$$I_{C2} = \frac{V^+ - 3V_{BE}}{R12} \qquad (A.11)$$

so

$$R_{E2} = \frac{kT\,R12}{q\,(V^+ - 3V_{BE})} \qquad (A.12)$$

Therefore, at 25°C where V_{VE} = 670 mV and kT/q = 26 mV, the computed value for gain is 0.745. The gain is not greatly affected by temperature as the gain at −55°C where V_{BE} = 810 mV and kT/q = 18 mV is 0.774, and the gain at 125°C where V_{BE} = 480 mV and kT/q = 34 mV is 0.730.

With a voltage gain of 0.75, the results of Equation (A.6) show that the input referred threshold voltage will change by 0.11V for a 1V change in supply voltage. With the standard ±10-percent supplies used for logic circuits, this means that the threshold voltage will change by less than ±60 mV.

Finally, the threshold error due to finite gain in the output stage can be considered. The collector current of Q7 from the bleeder resistor R14, is large by comparison to the base current of Q8, if Q8 has a reasonable current gain. Hence, the collector current of Q7 does not change appreciably when the output switches from a logic one to a logic zero. This is even more true for Q6, an emitter follower which drives Q7. Therefore, it is safe to presume that Q6 does not load the output of the first-stage amplifier, because of the compounded current gain of the three transistors, and that Q8 is driven from a low resistance source.

It follows that the gain of the output stage can be determined from the change in the emitter-base voltage of Q8 required to swing the output from a logic one state to a logic zero state. The expression

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \qquad (A.13)$$

describes the change in emitter-base voltage required to vary the collector current from one value, I_{C1}, to a second, I_{C2}. With the output of the receiver in the low state, the collector current of Q8 is

$$I_{OL} = \frac{V^+ - V_{OL} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} + I_{SINK}, \qquad (A.14)$$

where V_{OL} is the low state output voltage and I_{SINK} is the current load from the logic that the receiver is driving. Noting that R13 = 2R14 and figuring that all the emitter-base voltages are the same, this becomes

$$I_{OL} = \frac{V^+ - V_{OL} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} + I_{SINK} \qquad (A.15)$$

Similarly, with the output in the high state, the collector current of Q8 is

$$I_{OH} = \frac{V^+ - V_{OH} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} - I_{SOURCE}, \qquad (A.16)$$

where V_{OH} is the high-level output voltage and I_{SOURCE} is the current needed to supply the input leakage of the digital circuits loading the comparator.

With the same conditions used in arriving at (A.15), this becomes

$$I_{OH} = \frac{V^+ - V_{OH} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} - I_{SOURCE} \qquad (A.17)$$

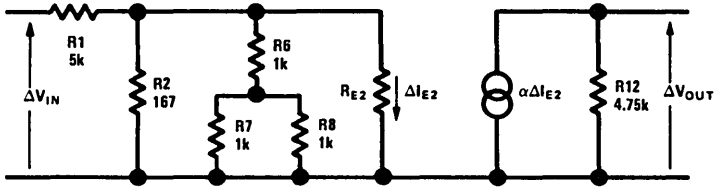

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FIGURE A-2. Equivalent Circuit Used to Calculate Input Stage Gain

From (A.13) the change in the emitter-base voltage of Q8 in going from the high output level to the low output level is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{OL}}{I_{OH}} \qquad (A.18)$$

providing that Q8 is not quite in saturation, although it may be on the verge of saturation.

The change of input threshold voltage is then

$$\Delta V_{TH} = \frac{kT}{qA_{v1}} \log_e \frac{I_{OL}}{I_{OH}} \qquad (A.19)$$

where A_{v1} is the input stage gain. With a worst case fanout of 2, where V_{OH} = 2.5V, V_{OL} = 0.4V, I_{SOURCE} = 40 μA and I_{SINK} = 3.2 mA, the calculated change in threshold is 37 mV at 25°C, 24 mV at −55°C and 52 mV at 125°C.

The measured values of overall gain differ by about a factor of two from the calculated gain. This is not too surprising because a number of assumptions were made which introduce small errors, and all these errors lower the gain. It is also not too important because the gain is high enough where another factor of two reduction would not cause the circuit to stop working.

The main contributors to this discrepancy are the non-ideal behavior of the emitter-base voltage of Q8 due to current crowding under the emitter and the variation in the emitter base voltage of Q7 and Q8 with changes in collector-emitter voltage (h_{RE}).

Although these parameters can vary considerably with different manufacturing methods, they are relatively fixed for a given process. The ΔV_{BE} errors introduced by these quantities, if known, can be added directly into Equation (A.18) to give a more accurate gain expression.

The most stringent matching requirement in the receiver is the matching of the input stage divider resistors: R1 with R8 and R2 with R3. As little as 1% mismatch in one of these pairs can cause a threshold shift of 150 mV at the extremes of the ±15V common mode range. Because of this, it is necessary to make the resistors absolutely identical and locate them close together. In addition, since R1 and R8 do dissipate a reasonable amount of power, they have to be located to minimize the thermal gradient between them. To do this, R9 was located between R1 and R8 so that it would heat both of these resistors equally. There are not serious heating problems with R2 and R3; however, because of their low resistance value, it was necessary even to match the lengths of the aluminum interconnects, as the resistance of the aluminum is high enough to cause intolerable mismatches. Of secondary importance is the matching of Q1 and Q2 and the matching of ratios between R11 and R12. A 1 mV difference in the emitter-base voltages of Q1 and Q2 causes a 30 mV input offset voltage as does a 1% mismatch in the ratio of R11 to R12.

The circuit is indeed insensitive to transistor current gains as long as they are above 10. The collector currents of Q4 and Q6 are made equal so that their base currents load the collectors of Q1 and Q2 equally. Hence, the input threshold voltage is affected only by how well the current gains match. Low current gain in the output transistor, Q8, can cause a reduction in gain. But even with a current gain of 10, the error produced in the input threshold voltage is less than 50 mV.

Transmission Line Characteristics

National Semiconductor
Application Note 108
Bill Fowler

INTRODUCTION

Digital systems generally require the transmission of digital signals to and from other elements of the system. The component wavelengths of the digital signals will usually be shorter than the electrical length of the cable used to connect the subsystems together and, therefore, the cables should be treated as a transmissions line. In addition, the digital signal is usually exposed to hostile electrical noise sources which will require more noise immunity than required in the individual subsystems environment.

The requirements for transmission line techniques and noise immunity are recognized by the designers of subsystems and systems, but the solutions used vary considerably. Two widely used example methods of the solution are shown in *Figure 1.* The two methods illustrated use unbalanced and balanced circuit techniques. This application note will delineate the characteristics of digital signals in transmission lines and characteristics of the line that effect the quality, and will compare the unbalanced and balanced circuits performance in digital systems.

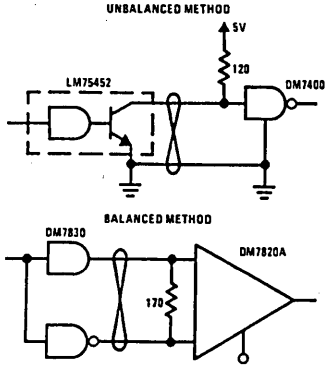

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FIGURE 1

NOISE

The cables used to transmit digital signals external to a subsystem and in route between the subsystem, are exposed to external electromagnetic noise caused by switching transients from actuating devices of neighboring control systems. Also external to a specific subsystem, another subsystem may have a ground problem which will induce noise on the system, as indicated in *Figure 2.*

The signals in adjacent wires inside a cable may induce electromagnetic noise on other wires in the cable. The induced electromagnetic noise is worse when a line terminated at one end of the cable is near to a driver at the same end, as shown in *Figure 3.* Some noise may be induced from relay circuits which have very large transient voltage swings compared to the digital signals in the same cable. Another source of induced noise is current in the common ground wire or wires in the cable.

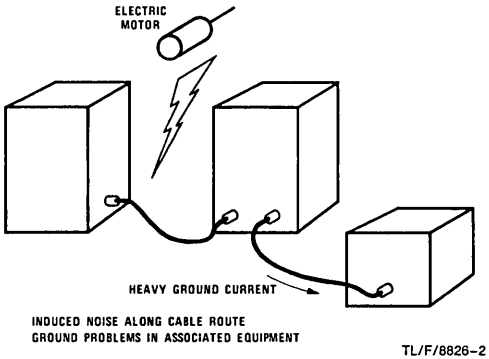

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FIGURE 2. External Noise Sources

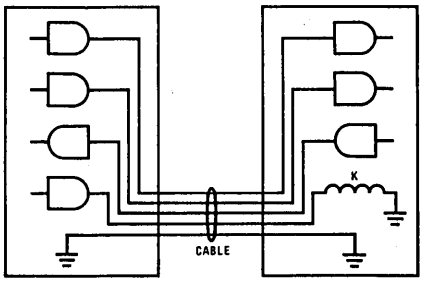

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FIGURE 3. Internal Noise Sources

DISTORTION

The objective is the transmission and recovery of digital intelligence between subsystems, and to this end, the characteristics of the data recovered must resemble the data transmitted. In *Figure 4* there is a difference in the pulse width of the data and the timing signal transmitted, and the corresponding signal received. In addition there is a further difference in the signal when the data is "AND"ed with the timing signal. The distortion of the signal occurred in the transmission line and in the line driver and receiver.

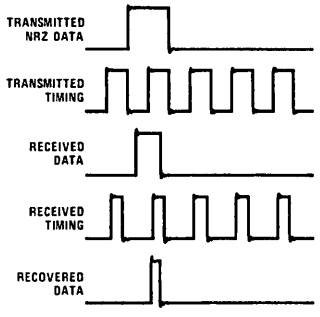

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FIGURE 4. Effect of Distortion

A primary cause of distortion is the effect the transmission line has on the rise time of the transmitted data. *Figure 5* shows what happens to a voltage step from the driver as it travels down the line. The rise time of the signal increases as the signal travels down the line. This effect will tend to affect the timing of the recovered signal.

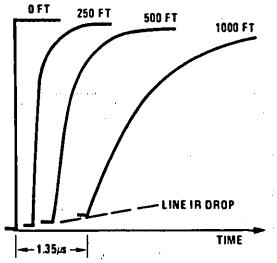

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FIGURE 5. Signal Response at Receiver

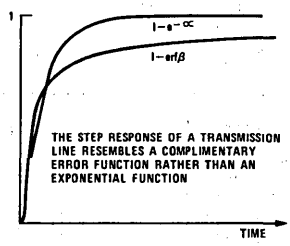

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FIGURE 6. Signal Rise Time

The rise time in a transmission line is not an exponential function but a complementary error function. The high frequency components of the step input are attenuated and delayed more than the low frequency components. This attenuation is inversely proportional to the frequency. Notice in *Figure 6* particularly that the signal takes much longer to reach its final DC value. This effect is more significant for fast risetimes.

The Duty Cycle of the transmitted signal also causes distortion. The effect is related to the signal rise time as shown in *Figure 7.* The signal doesn't reach one logic level before the signal changes to another level. If the signal has a ½ (50%) Duty Cycle and the threshold of the receiver is halfway between the logic levels, the distortion is small. But if the Duty Cycle is ⅛ as shown in the second case the signal is considerably distorted. In some cases, the signal may not reach the receiver threshold at all.

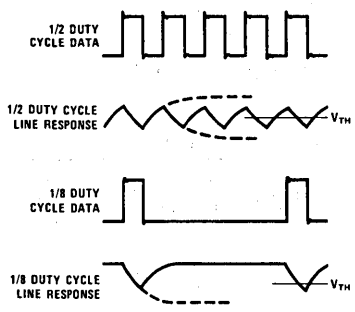

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FIGURE 7. Signal Distortion Due to Duty Cycle

In the previous example, it was assumed that the threshold of the receiver was halfway between the ONE and ZERO logic levels. If the receiver threshold isn't halfway the receiver will contribute to the distortion of the recovered signal. As shown in *Figure 8,* the pulse time is lengthened or shortened, depending on the polarity of the signal at the receiver. This is due to the offset of the receiver threshold.

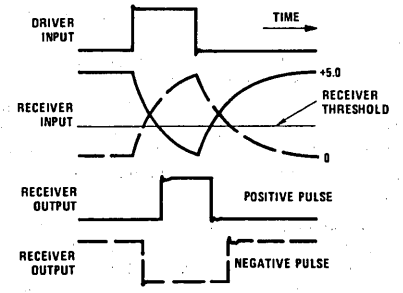

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FIGURE 8. Slicing Level Distortion

UNBALANCED METHOD

Another source of distortion is caused by the IR losses in the wire. *Figure 9* shows the IR losses that occur in a thousand feet of no. 22 AWG wire. Notice in this example that the losses reduce the signal below the threshold of the receiver in the unbalanced method. Also that part of the IR drop in the ground wire is common to other circuits—this ground signal will appear as a source of noise to the other unbalanced line receivers in the system.

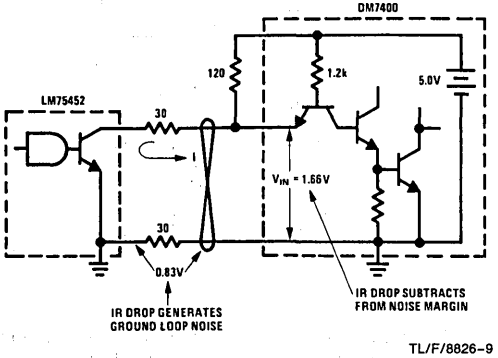

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FIGURE 9. Unbalanced Method

Transmission lines don't necessarily have to be perfectly terminated at both ends, (as will be shown later) but the termination used in the unbalanced method will cause additional distortion. *Figure 10* shows the signal on the transmission line at the driver and at the receiver. In this case the receiver was terminated in 120Ω, but the characteristic impedance of the line is much less. Notice that the wave forms have significant steps due to the incorrect termination of the line. The signal is subject to misinterpretation by the line receiver during the period of this signal transient because of the distortion caused by Duty Cycle and attenuation. In addition, the noise margin of the signal is reduced.

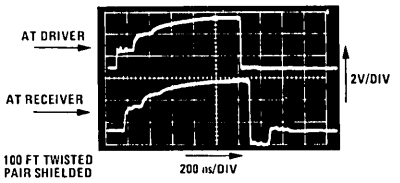

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FIGURE 10. LM75451, DM7400 Line Voltage Waveforms

The signal waveforms on the transmission line can be estimated before hand by a reflection diagram. *Figure 11* shows the reflection diagram of the rise time wave forms. The voltage versus current plot on left then is used to predict the transient rise time of the signal shown on the right. The initial condition on the transmission line is an IR drop across the line termination. The first transient on the line traverses from this initial point to zero current. The path it follows corresponds to the characteristic impedance of the line. The second transient on the diagram is at the line termination. As shown, the signal reflects back and forth until it reaches its final DC value.

Figure 12 shows the reflection diagram of the fall time. Again the signal reflects back and forth between the line termination until it reaches its final DC value. In both the rise and fall time diagrams, there are transient voltage and current signals that subtract from the particular signal and add to the system noise.

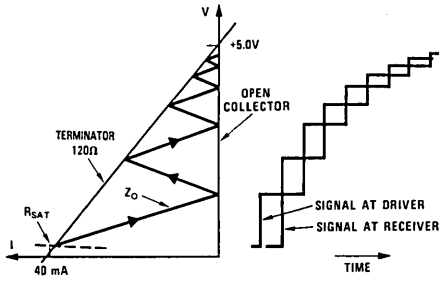

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FIGURE 11. Line Reflection Diagram of Rise Time

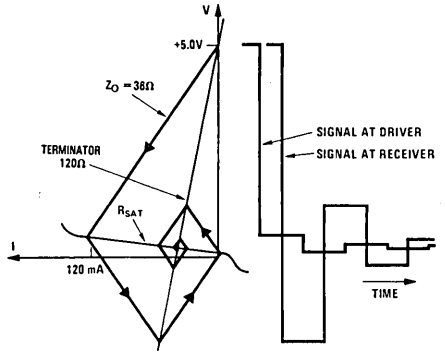

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FIGURE 12. Line Reflection Diagram of Fall Time

BALANCED METHOD

In the balanced method shown in *Figure 13*, the transient voltages and currents on the line are equal and opposite and cancel each others noise. Also unlike the unbalanced method, they generate very little ground noise. As a result, the balanced circuit doesn't contribute to the noise pollution of its environment.

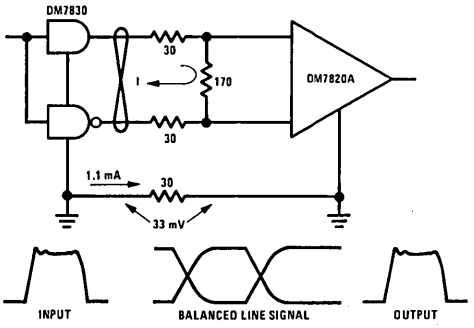

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FIGURE 13. Cross Talk of Signals

The circuit used for a line receiver in the balanced method is a differential amplifier. *Figure 14* shows a noise transient induced equally on lines A and line B from line C. Because the signals on line A and B are equal, the signals are ignored by the differential line receiver.

Likewise for the same reason, the differential signals on lines A and B from the driver will not induce transients on line C. Thus, the balanced method doesn't generate noise and also isn't susceptible to noise. On the other hand the unbalanced method is more sensitive to noise and also generates more noise.

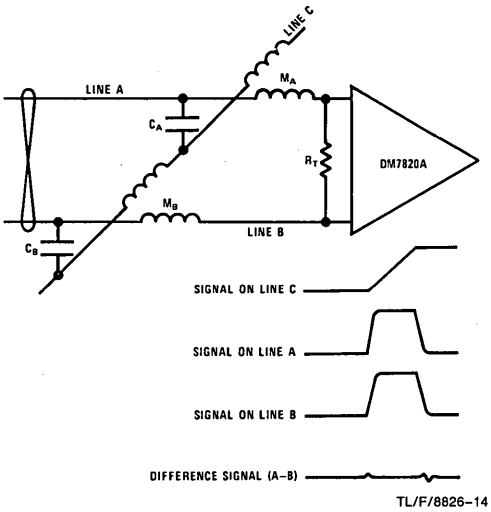

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FIGURE 14. Cross Talk of Signals

The characteristic impedance of the unbalanced transmission line is less than the impedance of the balanced transmission line. In the unbalanced method there is more capacitance and less inductance than in the balanced method. In the balanced method the Reactance to adjacent wires is almost cancelled (see *Figure 15*). As a result a transmission line may have a 60Ω unbalanced impedance and a 90Ω balanced impedance. This means that the unbalanced

method, which is more susceptible to IR drop, must use a smaller value termination, which will further increase the IR drop in the line.

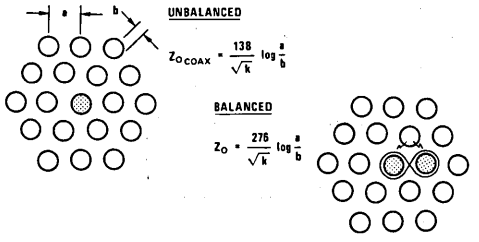

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FIGURE 15. Z_O Unbalanced < Z_O Balanced

The impedance measurement of an unbalanced and balanced line must be made differently. The balanced impedance must be measured with a balanced signal. If there is any unbalance in the signal on the balanced line, there will be an unbalance reflection at the terminator. Therefore, the lines should also be terminated for unbalanced signals. *Figure 16* shows the perfect termination configuration of a balanced transmission line. This termination method is primarily required for accurate impedance measurements.

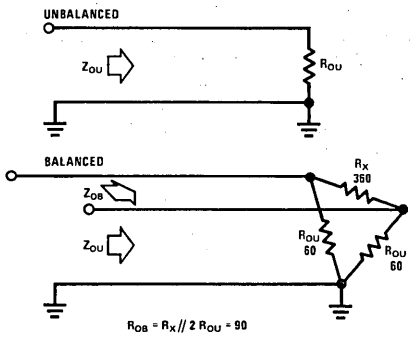

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FIGURE 16. Impedance Measurement

MEASURED PERFORMANCE

The unbalanced method circuit used in this application note up to this point is the unbalanced circuit shown in *Figure 1.* The termination of its transmission line was greater than the characteristic impedance of the unbalanced line and the circuit had considerable threshold offset. The measured performance of the unbalanced circuit wasn't comparable to the balanced method. Therefore, for the following comparison of unbalanced and balanced circuits, an improved termination shown in *Figure 17* will be used. This circuit terminates the line in 60Ω and minimized the receiver threshold offset.

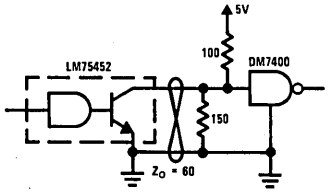

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FIGURE 17. Improved Unbalanced Method

A plot of the Absolute Maximum Data Rate versus cable type is shown in *Figure 18.* The graph shows the different performances of the DM7820A line receiver and the DM7830 line driver circuits with a worse case 1/8 Duty Cycle in no. 22 AWG stranded wire cables. In a single twisted pair cable there is less reactance than in a cable having nine twisted pairs and in turn this cable has less reactance than shielded pairs. The line length is reduced in proportion to the increased line attenuation which is proportional to the line reactance. The plot shows that the reactance and attenuation has a significant effect on the cable length. Absolute Maximum Data Rate is defined as the Data Rate at which the output of the line receiver is starting to be degraded. The roll off of the performance above 20 mega baud is due to the circuit switching response limitation.

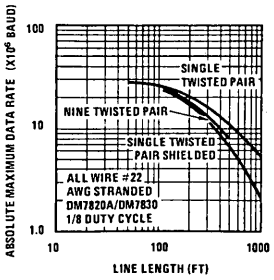

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FIGURE 18. Data Rate vs Cable Type

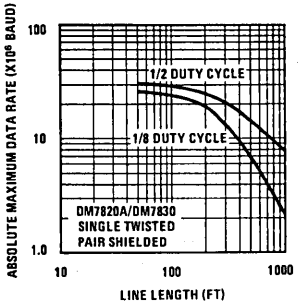

FIGURE 19. Data Rate vs Duty Cycle

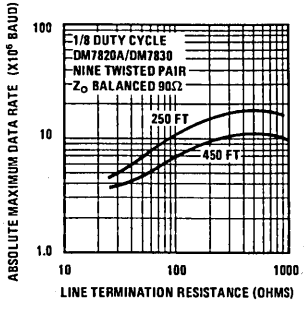

FIGURE 20. Data Rate vs Line Termination

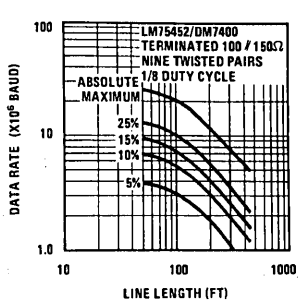

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FIGURE 21. Data Rate vs Distortion of LM75452, DM7400

Figure 19 shows the reduction in Data Rate caused by Duty Cycle. It can be observed that the Absolute Maximum Duty Rate of 1/8 Duty Cycle is less than 1/2 Duty Cycle. The following performance curves will use 1/8 Duty Cycle since it is the worst case.

Absolute Maximum Duty Rate versus the Line Termination Resistance for two different lengths of cable is shown in *Figure 20*. It can be seen from the figure that the termination doesn't have to be perfect in the case of balanced circuits. It is better to have a termination resistor to minimize the extra transient signal reflecting between the ends of the line. The reason the Data Rate increases with increased Termination Resistance is that there is less IR drop in the cable.

The graphs in *Figure 21* show the Data Rate versus the Line Length for various percentages of timing distortion using the unbalanced LM75452 and DM7400 circuits shown in *Figure 17*. The definition of Timing Distortion is the percentage difference in the pulse width of the data sent versus the data received.

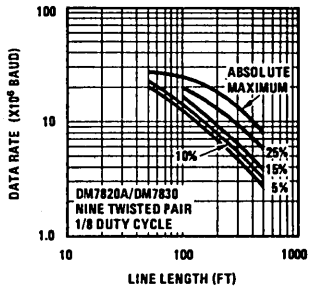

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FIGURE 22. Data Rate vs Distortion of DM7820A, DM7830

Data Rate versus the Line Length for various percentage of timing distortion using the balanced DM7820A and DM7830 circuit is shown in *Figure 22*. The distortion of this method is improved over the unbalanced method, as was previously theorized.

The Absolute Maximum Data Rate versus Line Lengths shown in the previous two figures didn't include any induced signal noise. *Figure 23* shows the test configuration of the unbalanced circuits which was used to measure near end cross talk noise. In this configuration there are eight line drivers and one receiver at one end of the cable. The performance of the receiver measured in the presence of the driver noise is shown in *Figure 24*.

Figure 24 shows the Absolute Maximum Duty Rate of the unbalanced method versus line length and versus the number of line drivers corresponding to the test configuration delineated in *Figure 23*. In the noise measurement set-up there was a ground return for each signal wire. If there is only one ground return in the cable the performance is worse. The graph shows that the effective line length is drastically reduced as additional Near End Drivers are added. When this performance is compounded by timing distortion the performance is further reduced.

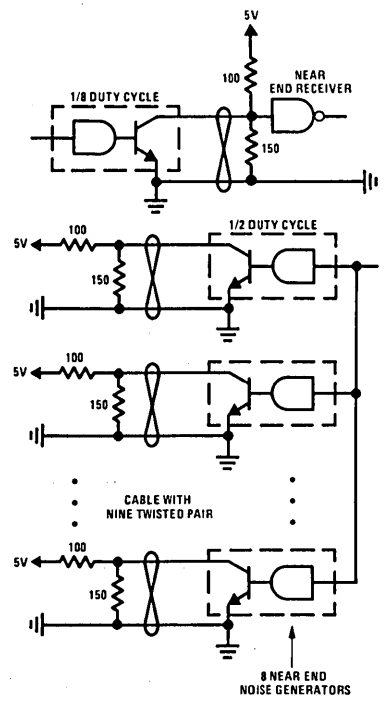

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FIGURE 23. Signal Cross Talk Experiment Using DM75452, DM7400

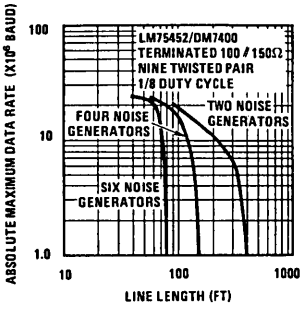

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FIGURE 24. Data Rate vs Signal Cross Talk of LM75452, DM7400

Figure 25 shows the test configuration of the balanced circuit used to generate worst case Near End cross talk noise similar to the unbalance performance shown in the previous figure. Unlike the unbalanced case, there was no measurable degradation of the circuits Data Rate or distortion.

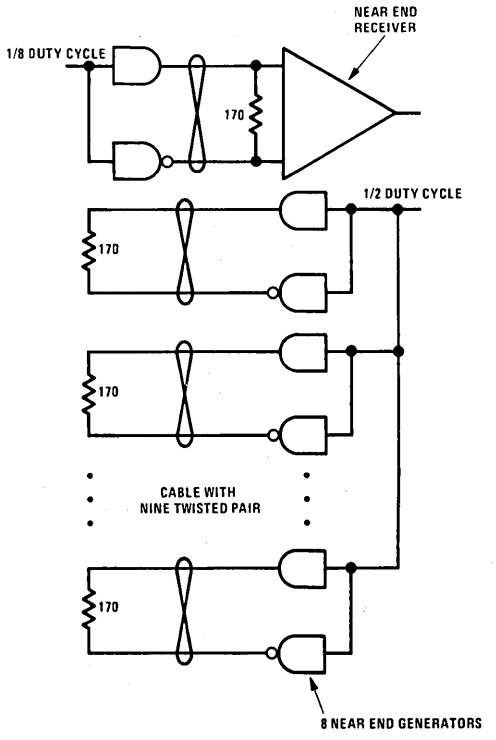

FIGURE 25. Signal Cross Talk Experiment Using DS7830, DS7820A

CONCLUSION

National has a full line of both Balanced and Unbalanced Line Drivers and Receivers. Both circuit types work well when used within their limitation. This application note shows that the balanced method is preferable for long lines in noisy electrical environments. On the other hand the unbalanced circuit works perfectly well with shorter lines and reduced data rates.

DEFINITION OF BAUD RATE

Baud Rate ≡ modulation rate of the channel and is defined as the reciprocal of the minimum pulse width.

Bits/sec (bps) ≡ information rate of the channel and is defined as the number of bits transmitted in one second.

Note: For Non-Return to Zero (NRZ) coding, the baud rate is equal to the bit rate. For Manchester coding, the baud rate is equal to twice the bit rate.

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Transmission Line Drivers and Receivers for TIA/EIA Standards RS-422 and RS-423

National Semiconductor
Application Note 214
John Abbott
John Goldie

INTRODUCTION

With the advent of the microprocessor, logic designs have become both sophisticated and modular in concept. Frequently the modules making up the system are very closely coupled on a single printed circuit board or cardfile. In a majority of these cases a standard bus transceiver will be adequate. However because of the distributed intelligence ability of the microprocessor, it is becoming common practice for the peripheral circuits to be physically separated from the host processor with data communications being handled over cables (e.g. plant environmental control or security system). And often these cables are measured in hundreds or thousands of feet as opposed to inches on a backplane. At this point the component wavelengths of the digital signals may become shorter than the electrical length of the cable and consequently must be treated as transmission lines. Further, these signals are exposed to electrical noise sources which may require greater noise immunity than the single chassis system.

It is the object of this application note to underscore the more important design requirements for balanced and unbalanced transmission lines, and to show that National's DS1691 driver and DS78LS120 receiver meet or exceed all of those requirements.

THE REQUIREMENTS

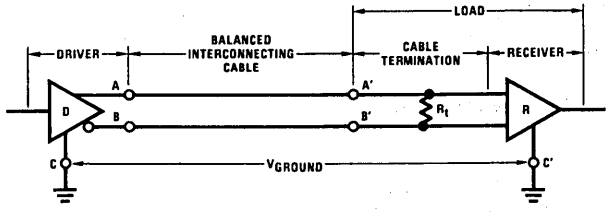
The requirements for transmission lines and noise immunity have been adequately recognized by National Semiconductor's application note AN-108 and TIA/EIA standards TIA/EIA-422-B (balanced) and TIA/EIA-423-B (unbalanced). In this application note the generic terms of RS-422 and RS-423 will be used to represent the respective TIA/EIA standards. A summary review of these notes will show that the controlling factors in a voltage digital interface are:

1) The cable length
2) The data signaling rate
3) The characteristic of the interconnection cable
4) The rise time of the signal

RS-422 and RS-423 contain several useful guidelines relative to the choice of balanced circuits versus unbalanced circuits. *Figures 1a* and *1b* are the digital interface for balanced *(1a)* and unbalanced *(1b)* circuits.

Even though the unbalanced interface circuit is intended for use at lower modulation rates than the balanced circuit, its use is not recommended where the following conditions exist:

1) The interconnecting cable is exposed to noise sources which may cause a voltage sufficient to indicate a change of binary state at the load.
2) It is necessary to minimize interference with other signals, such as data versus clock.
3) The interconnecting cable is too long electrically for unbalanced operation *(Figure 2)*.



Legend:
R_t = Optional cable termination resistance/receiver input impedance.
V_{GROUND} = Ground potential difference
A, B = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

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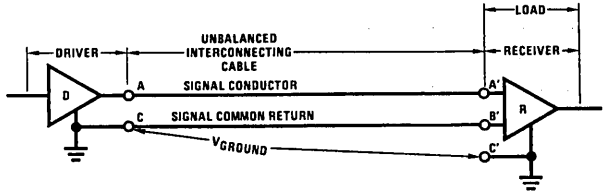
FIGURE 1a. Balanced Digital Interface Circuit



Legend:
R_t = Transmission line termination and/or receiver input impedance
V_{GROUND} = Ground potential difference
A, C = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

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FIGURE 1b. Unbalanced Digital Interface Circuit

CABLE LENGTH

While there is no maximum cable length specified, guidelines are given with respect to conservative operating distances as a function of data signaling rate. *Figure 2* is a composite of the guidelines provided by RS-422 and RS-423 for data signaling rate versus cable length. The data is for 24 AWG twisted pair cable terminated for worst case (due to IR drop) in a 100Ω load, with rise and fall times equal to or less than one half unit interval at the applied data rate.

The maximum cable length between driver and load is a function of the data signaling rate. But it is influenced by:

1) A maximum common noise range of ±7 volts
   A) The amount of common-mode noise
      Difference of driver and receiver ground potential plus driver offset voltage and coupled peak random noise.
   B) Ground potential differences between driver and load.
   C) Cable balance
      Differential noise caused by imbalance between the signal conductor and the common return (ground)
2) Cable termination
   At rates above 200 kbps or where the rise time is 4 times the one way propagation delay time of the cable
3) Tolerable signal distortion

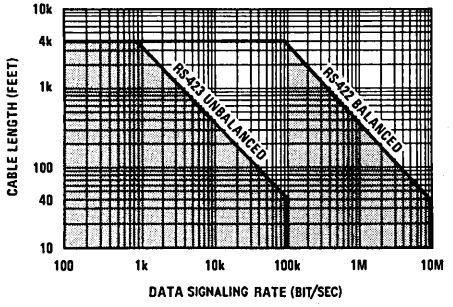

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FIGURE 2. Data Signaling Rate vs Cable Length

DATA SIGNALING RATE

The TIA/EIA Standards recommend that the unbalanced voltage interface will normally be utilized on data, timing or control circuits where the data signaling rate on these circuits is below 100 kbps, and balanced voltage digital interface on circuits up to 10 Mbps. The voltage digital interface drivers and receivers meeting the electrical characteristics of this standard need not meet the entire data signaling range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower data signaling rates.

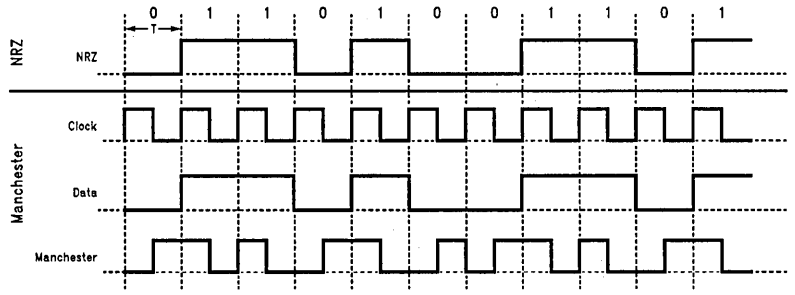
As pointed out in AN-108, the duty cycle of the transmitted signal contributes to the distortion. The effect is the result of rise time. Due to delay and attenuation caused by the cable, it is possible due to AC averaging of the signal, to be unable to reach one binary level before it is changed to another. If the duty cycle is ½ (50%) and the receiver threshold is midway between logic levels, the distortion is small. However if the duty cycle were ⅛ (12.5%) the signal would be considerably distorted.

CHARACTERISTICS

Driver Unbalanced (RS-423)

The unbalanced driver characteristics as specified by RS-423 are as follows:

1) A driver circuit should be a low impedance (50Ω or less) unbalanced voltage source that will produce a voltage applied to the interconnecting cable in the range of 4V to 6V.
2) With a test load of 450Ω connected between the driver output terminal and the driver circuit ground, the magnitude of the voltage (VT) measured between the driver output and the driver circuit ground shall not be less than 90% of the open circuit voltage magnitude (≥ 3.6V) for either binary state.
3) During transitions of the driver output between alternating binary states, the signal measured across a 450Ω test load connected between the driver output and circuit ground should be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS}. Thereafter, the sig-



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	Baud	Bits per Second	Hertz
CLOCK	—	—	1/T
NRZ	1/T	1/T	—
Manchester	2/T	1/T	—

Note: bps (bits per second) - Data Information Rate "the number of bits passed along in one second."
baud-Modulation Rate "the reciprocal of the minimum pulse width."
For NRZ bps = bauds

FIGURE 3a. Definition of Baud, Bits per Second (bps), Hertz (Hz) for NRZ and Manchester Coding

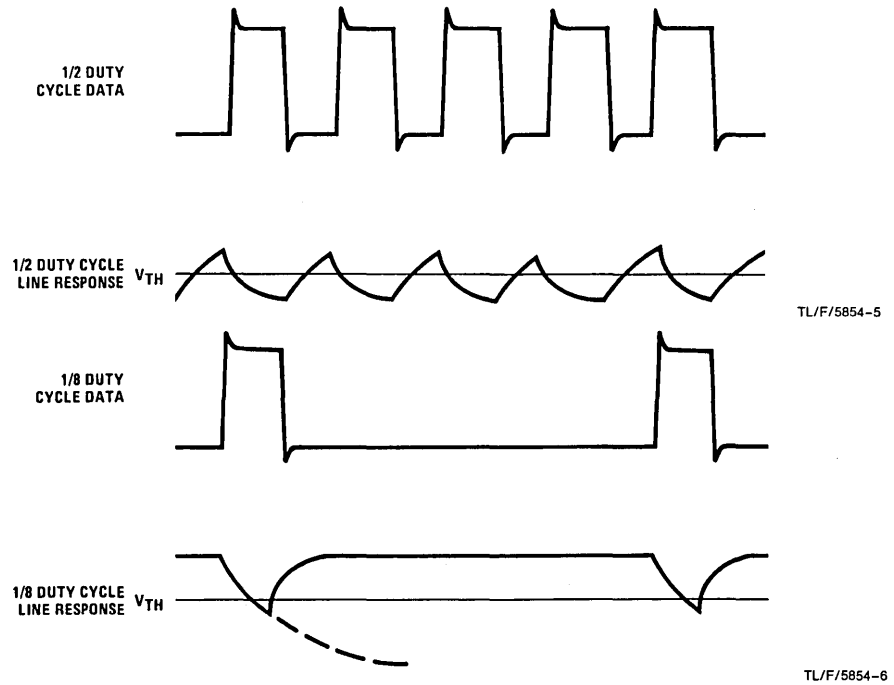
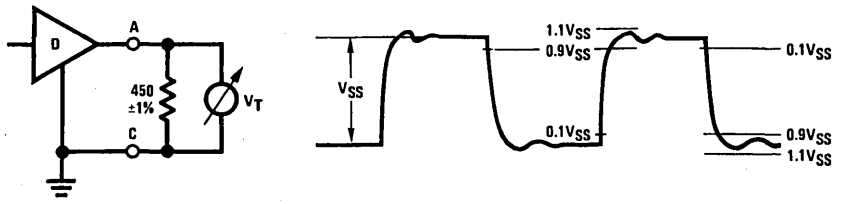


FIGURE 3b. Signal Distortion Due to Duty Cycle



$V_{SS} = |V_t - V_t|$

V_{SS} = Difference in steady state voltages

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FIGURE 4. Unbalanced Driver Output Signal Waveform

nal shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT and $\overline{VT}$ exceed |6V|, nor be less than |3.6V|. V_{SS} is defined as the voltage difference between the two steady state values of the driver output.

Driver Balanced (RS-422)

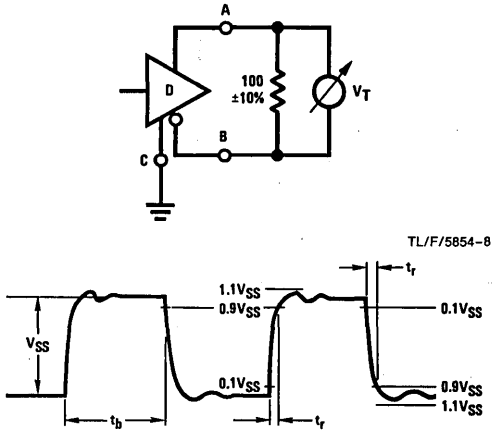
The balanced driver characteristics as specified by RS-422 are as follows:

1) A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage applied to the interconnecting cable in the range of 2V to 10V.
2) With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the 2 output terminals shall not be less than either 2.0V or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT shall be reversed ($\overline{VT}$). The magnitude of the difference in the magnitude of VT and $\overline{VT}$ shall be less than 0.4V. The magnitude of the driver offset voltage (V_{OS}) measured between the center point of the test load and driver circuit ground shall not be greater than 3.0V. The magnitude of the difference in the magnitude of V_{OS} for one binary state and $\overline{V_{OS}}$ for the opposing binary state shall be less than 0.4V.
3) During transitions of the driver output between alternating binary states, the differential signal measured across a 100Ω test load connected between the driver output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS} within 10% of the unit interval or 20 ns, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT or $\overline{VT}$ exceed 6V, nor less than 2V.

Interconnecting Cable

The characteristics of the interconnecting cable should result in a transmission line with a characteristic impedance in the general range of 100Ω to frequencies greater than 100 kHz, and a DC series loop resistance not exceeding 240Ω. The cable may be composed of twisted or untwisted pair (flat cable) and is not further specified within the standards.

1) Conductor size of the 2 wires 24 AWG or larger, and wire resistance not to exceed 30Ω per 1000 feet per conductor.
2) Mutual pair capacitance between 1 wire in the pair to the other should be less than 20 pF/ft.



t_b = Time duration of the unit interval at the applicable modulation rate.

$t_r \leq 0.1\ t_b$ when $t_b \geq 200$ ns

$t_r \leq 20$ ns when $t_b < 200$ ns

V_{SS} = Difference in steady state voltages

$V_{SS} = |V_t - V_t|$

FIGURE 5. Balanced Driver Output Signal Waveform

Receiver

The receiver characteristics are identical for both balanced (RS-422) and unbalanced (RS-423) circuits. The electrical characteristics of a single receiver without termination or optional fail-safe provisions are specified as follows:

1) Over an entire common-mode voltage range of −7V to +7V, the receiver shall not require a differential input voltage of more than 200 mV to correctly assume the intended binary state. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. Reversing the polarity of VT shall cause the receiver to assume the opposite binary state. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2) To maintain correct operation for differential input signal voltages ranging between 200 mV and 6V in magnitude.
3) The maximum voltage present between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal plus 7V common-mode) in magnitude nor cause the receiver to operationally fail. Additionally, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4) The total load including up to 10 receivers shall not have a resistance less than 90Ω for balanced, and 450Ω for unbalanced at its input points and shall not require a differential input voltage of greater than 200 mV for all receivers to assume the correct binary state.

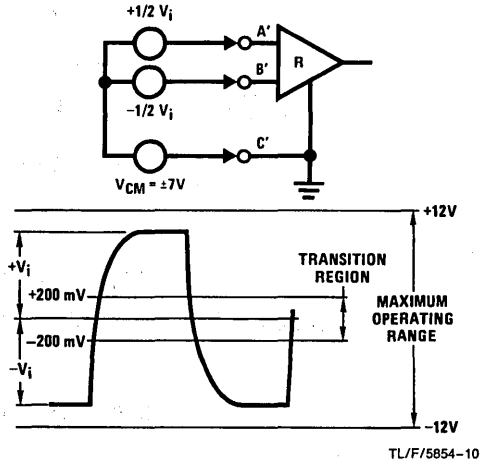


FIGURE 6. Receiver Input Sensitivity Measurement

SIGNAL RISE TIME

The signal rise time is a high frequency component which causes interference (near end cross-talk) to be coupled to adjacent channels in the interconnecting cable. The near-end crosstalk is a function of both rise time and cable length, and in considering wave shaping, both should be considered. Since in the balanced voltage digital interface the output is complementary, there is practically no cross-talk coupled and therefore wave shaping is limited to unbalanced circuits.

Per RS-423 the rise time of the signal should be controlled so that the signal has reached 90% of V_{SS} between 10% and 30% of the unit interval at the maximum data signaling rate. Below 1 kbps the time to reach 90% V_{SS} shall be between 100 μs and 300 μs. If a driver is to operate over a range of data signaling rates and employ a fixed amount of wave shaping which meets the specification for the maximum data signaling rate of the operating range, the wave shaping is considered adequate for all lesser modulation rates.

However a major cause of distortion is the effect the transmission line has on the rise time of the transmitted signal. *Figure 7* shows the effect of line attenuation and delay to a voltage step as it progresses down the cable. The increase of the rise time with distance will have a considerable effect on the distortion at the receiver. Therefore in fixing the amount of wave shaping employed, caution should be taken not to use more than the minimum required.

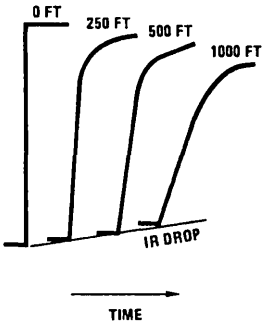


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FIGURE 7. Signal Rise Time on Transmission Line vs Line Length

DS1691A, DS78LS120

The Driver

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the above listed requirements of both standards. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. The DS1691/DS3691 employ a mode selection pin which allows the circuit to become either a pair of balanced drivers *(Figure 8)* or 4 independent unbalanced drivers *(Figure 9)*. When configured for unbalanced operation *(Figure 10)* a rise time control pin allows the use of an external capacitor to control rise time for suppression of near end cross-talk to adjacent channels in the interconnect cable. *Figure 11* is the typical rise time vs external capacitor used for wave shaping. Note that the rise time control capacitors are connected betwen the control pins and the respective outputs.

The DS3691 configured for RS-422 is connected V_{CC} = 5V V_{EE} = 0V, and configured for RS-423 is connected V_{CC} = 5V V_{EE} = −5V. For applications with greater cable lengths the DS1691/DS3691 may be connected with a V_{CC} of 5 volts and V_{EE} of −5 volts. This will create an output which is symmetrical about ground, similar to Mil Standard 188-114. This mode is also allowed by the "B" revision of RS-422 (TIA/EIA-422-B) which relaxed to open circuit voltage from 6V to 10V in magnitude.

When configured as balanced drivers *(Figure 8)*, each of the drivers is equipped with an independent TRI-STATE® control pin. By use of this pin it is possible to force the driver into its high impedance mode for applications using party line techniques. If the driver is used in multi-point applications (multiple drivers) the use of the response control capacitors is not allowed.

If the common-mode voltage, between driver 1 and all other drivers in the circuit, is small then several line drivers (and receivers) may be incorporated into the system. However, if the common-mode voltage exceeds the TRI-STATE common-mode range of any driver, then the signal will become attenuated by that driver to the extent the common-mode voltage exceeds its common-mode range (see *Figure 12*, top waveform).

It is important then to select a driver with a common-mode range equal to or larger than the common-mode voltage requirement of the system. In the case of RS-422 and RS-423 the minimum common-mode range would be ±7V. The DS1691/DS3691 driver is tested to a common-mode range of ±10V and will operate within the requirements of such a system (see *Figure 12*, bottom waveform).

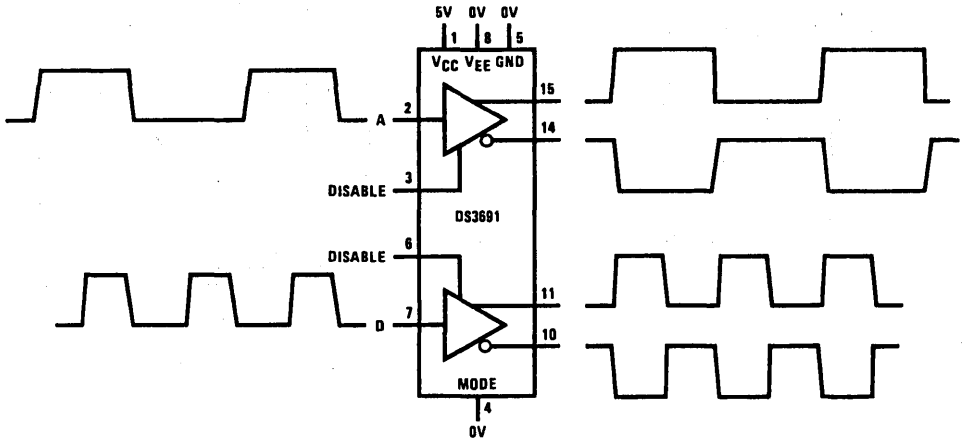

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FIGURE 8. DS3691 Connected for Balanced Mode Operation

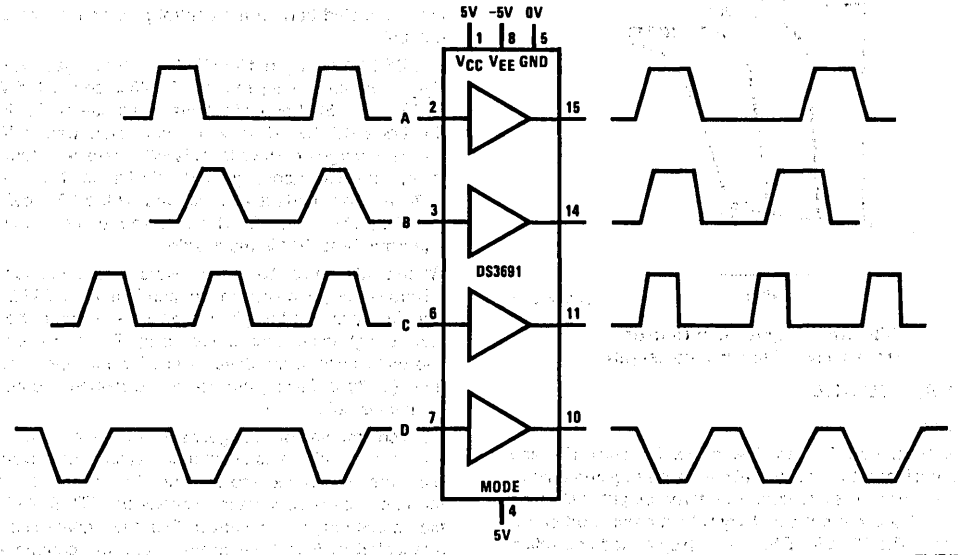

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FIGURE 9. DS3691 Connected for Unbalanced Mode Operation (Non-Inverting)

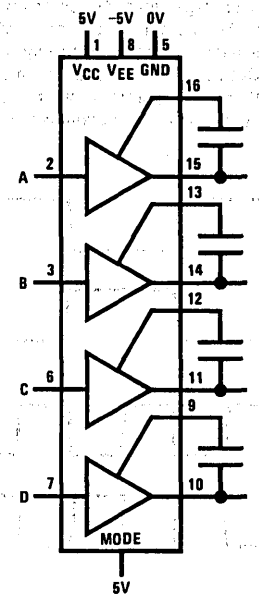

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FIGURE 10. Using an External Capacitor to Control Rise Time of DS3691

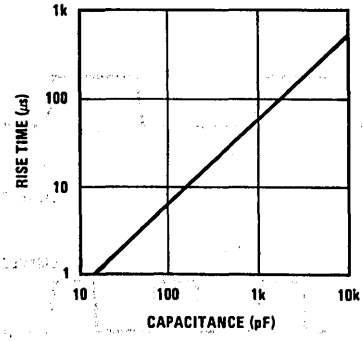

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FIGURE 11. DS3691 Rise Time vs External Capacitor

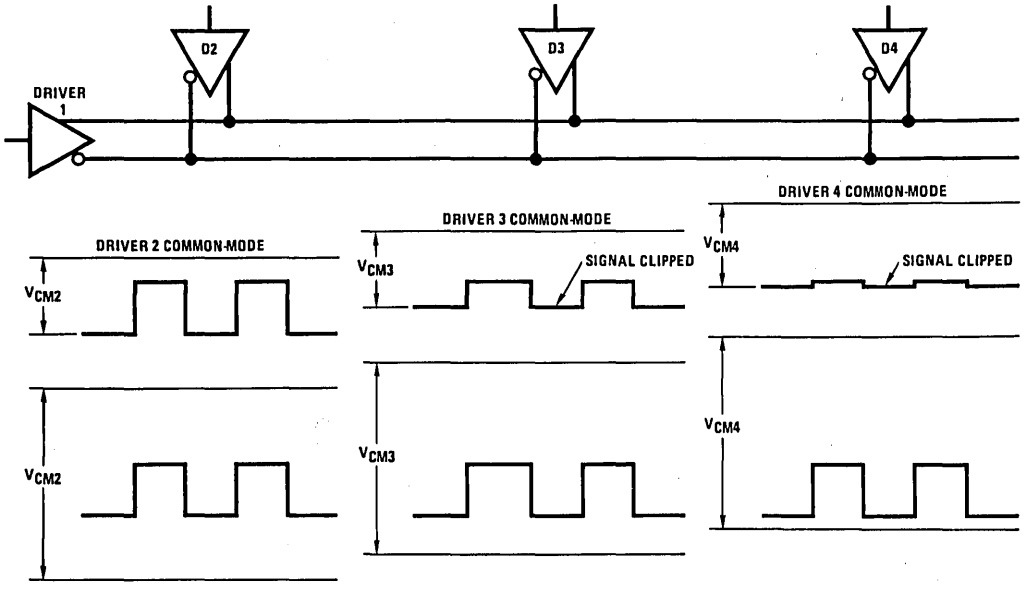

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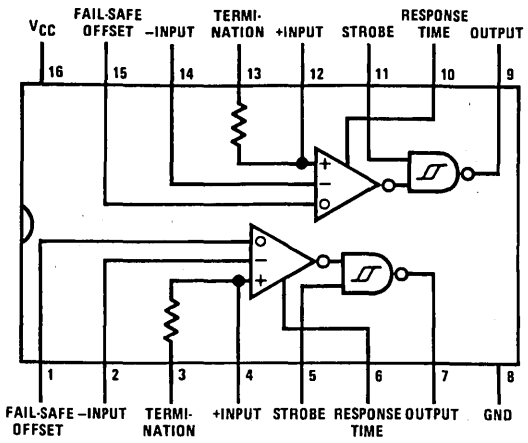
FIGURE 12. Comparison of Drivers without TRI-STATE Common-Mode Output Range (top waveforms) to DS3691 (bottom waveforms)



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Top View

FIGURE 13. DS78LS120/DS88LS120 Dual Differential Line Receiver

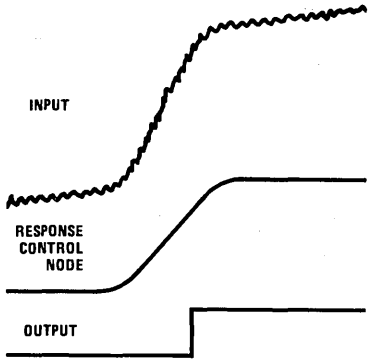
DS78LS120/DS88LS120

The Receiver

The DS78LS120/DS88LS120 are high peformance, dual differential TTL compatible line receivers which meet or exceed the above listed requirements for both balanced and unbalanced voltage digital interface.

The line receiver will discriminate a ±200 millivolt input signal over a full common-mode range of ±10 volts and a ±300 millivolt signal over a full common-mode range of ±15 volts.

The DS78LS120/DS88LS120 include response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Switching noise which may occur on the input signal can be eliminated by the 50 mV (referred to input) of hysteresis built into the output gate *(Figure 14)*. The DS78LS120/DS88LS120 makes use of a response control pin for the addition of an external capacitor, which will not affect the line termination impedance of the interconnect cable. Noise pulse width rejection versus the value of the response control capacitor is shown in *Figure 15*. The combination of the filter followed by hysteresis will optimize performance in a worst case noise environment. The DS78C120/DS88C120 is identical in performance to the DS78LS120/DS88LS120, except it's compatible with CMOS logic gates.



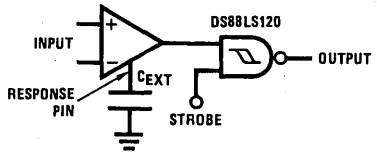


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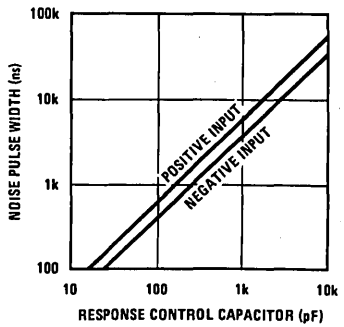
FIGURE 14. Application of DS88LS120 Receiver Response Control and Hysteresis



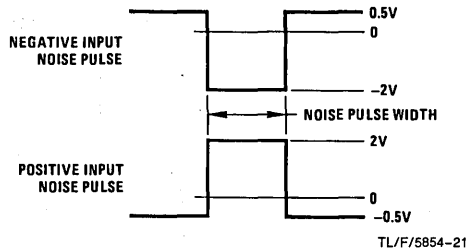


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FIGURE 15. Noise Pulse Width vs Response Control Capacitor

FAIL-SAFE OPERATION

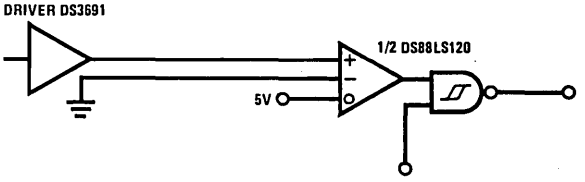
Some communication systems require elements of a system to detect the loss of signals in the transmission lines. And it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault condition exists.

The receiver input threshold is ±200 mV and an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input is connected to a V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will remain in a specific state (see *Figure 16*).

It is recommended that the receiver be terminated in 500Ω or less to insure it will detect an open circuit in the presence of noise.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to +5V, offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open fault condition. The "strobe" input will disable the A and B receivers and therefore may be used to "sample" the fail-safe detector (see *Figure 17*).



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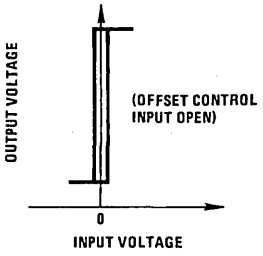

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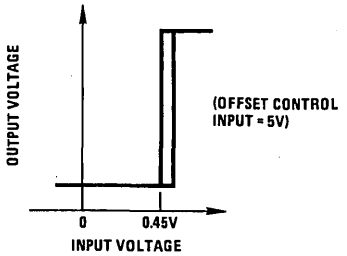

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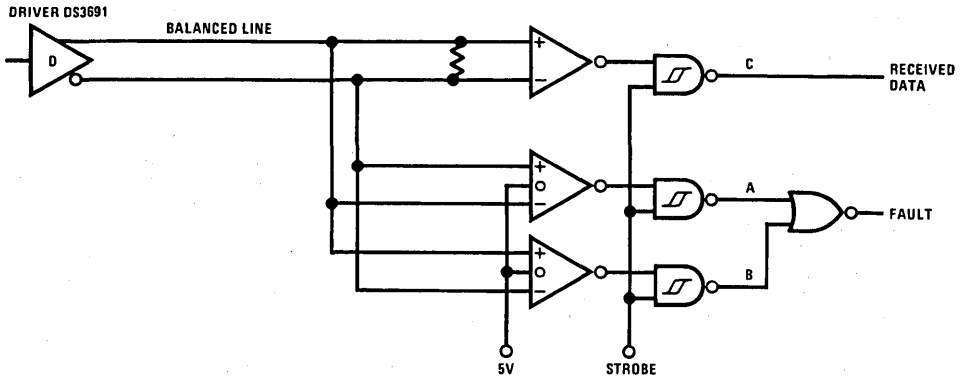
FIGURE 16. Fail-Safe Using the DS88LS120 Threshold Offset for Unbalanced Lines



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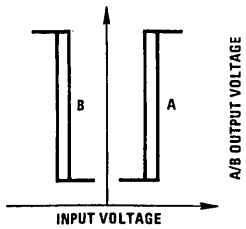

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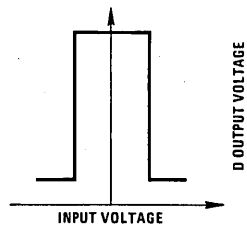

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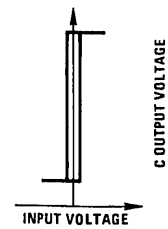

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FIGURE 17. Fail-Safe Using the DS88LS120 Threshold Offset for Balanced Lines

CONCLUSION

This application note provides a brief overview of TIA/EIA-422-B and TIA/EIA-423-B. At the time of publication of this application note the Rev. B standards were draft standard proposals only. For complete/current information on the respective standards the reader is referenced to the respective standards, as minor differences may exist between this document and the final versions.

Summary of Well Known Interface Standards

National Semiconductor
Application Note 216
John Goldie

FORWARD

Designing an interface between systems is not a simple or straight-forward task. Parameters that must be taken into account include: data rate, data format, cable length, mode of transmission, termination, bus common mode range, connector type, and system configuration. Noting the number of parameters illustrates how complex this task actually is. Additionally, the interface's compatibility with systems from other manufacturers is also critically important. Thus, the need for standardized interfaces becomes evident. Interface Standards resolve both the compatibility issue, and ease the design through the use of non-custom standardized Drivers and Receivers.

INTRODUCTION

This application note provides a short summary of popular Interface Standards. In most cases, a table of the major electrical requirements and a typical application is illustrated. Interface Standards from the following standardization organizations are covered in this application note:

- TIA/EIA Telecommunications Industry Association/Electronics Industry Association
- CCITT International Telegraph and Telephone Consultative Committee—now replaced by the ITU International Telecommunications Union
- MIL-STD United States Military Standards
- FED-STD Federal Telecommunications Standard Committee now known as ITU
- Other selected interface standards

There are two basic modes of operation for line drivers (generators) and receivers. The two modes are Unbalanced (Single-ended) and Balanced (Differential).

UNBALANCED (SINGLE-ENDED) DATA TRANSMISSION

Unbalanced data transmission uses a single conductor, with a voltage referenced to signal ground (common) to denote logical states. In unbalanced communication only one line is switched. The advantage of unbalanced data transmission is when mulitple channels are required, a common ground can be used (see *Figure 1*). This minimizes cable and connector size, which helps to minimize system cost. The disadvantage of unbalanced data transmission is in its inability to reliably send data in noisy environments. This is due to very limited noise margins. The sources of system noise can include externally induced noise, cross talk, and ground potential differences.

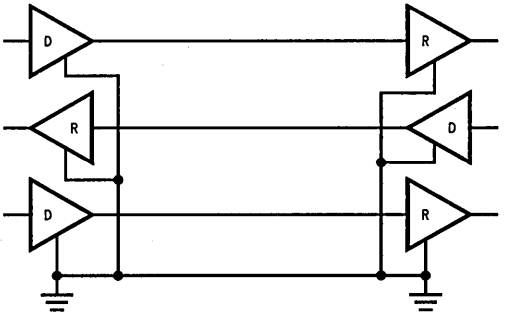

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FIGURE 1. Unbalanced Data Transmission-3 Channel, 4 Line

BALANCED (DIFFERENTIAL) DATA TRANSMISSION

Balanced data transmission requires two conductors per signal. In balanced communication two lines are switched. The logical states are referenced by the difference of potential between the lines, not with respect to ground. This fact makes differential drivers and receivers ideal for use in noisy environments (See *Figure 2*). Differential data transmission nullifies the effects of coupled noise and ground potential differences. Both of these are seen as common mode voltages (seen on both lines), not differential, and are rejected by the receivers. In contrast to unbalanced drivers, most balanced drivers feature fast transition times allowing for operation at higher data rates.

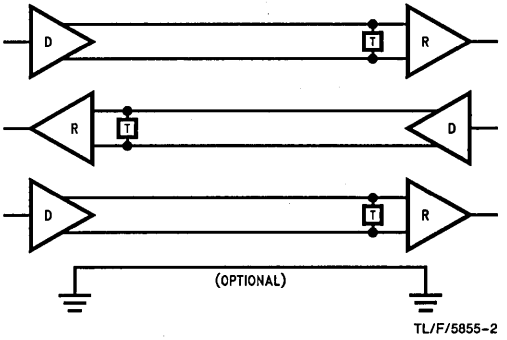

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FIGURE 2. Balanced Data Transmission-3 Channel, 7 Line, Ground Optional

8

TIA/EIA DATA TRANSMISSION STANDARDS

The Electronic Industry Association (EIA) and the Telecommunications Industry Association (TIA) are industry trade associations that have developed standards to simplify interfaces in data communication systems. The standards are intended for use in Data Terminal Equipment/Data Circuit-terminating Equipment (DTE/DCE) Interfaces. The classic example of the DTE/DCE interface is the "terminal to modem serial interface". However, the standards are not limited to use in DTE/DCE interfaces alone. In fact, many of the standards are commonly used in a wide variety of applications. Examples include Hard Disk Drive Interfaces, Factory Control Busses, and generic I/O Busses. Previously, EIA labeled the standards with the prefix "RS", which stood for recommended standard. This has been replaced with "TIA/EIA", to help in identifying the source of the standard. The letter suffix represents the revision level of the standard. For example, TIA/EIA-232-E represents the fifth revision of RS-232.

TIA/EIA Data Transmission Standards cover the following areas: Complete Interface Standards, Electrical Only Standards, and Signal Quality Standards. Complete standards define functional, mechanical, and electrical specifications. Electrical only standards, as their name implies only defines electrical specifications. They are intended to be referenced by complete standards. Signal Quality Standards define terms and methods for measuring signal quality. Examples of each type are listed below.

- Complete DTE/DCE Interface Standards
  - EIA/TIA-232-E
  - EIA/TIA-530-A
  - EIA/TIA-561
  - EIA/TIA-574
  - TIA/EIA-613
- Electrical Only Standards
  - Unbalanced Standards
    - EIA/TIA-232-E (Section 2)
    - TIA/EIA-423-B (draft)
    - EIA/TIA-562
  - Balanced Standards
    - TIA/EIA-422-B (draft)
    - EIA-485
    - TIA/EIA-612
- Signal Quality Standards
  - EIA-334-A
  - EIA-363
  - EIA-404-A

TIA/EIA—UNBALANCED (SINGLE-ENDED) STANDARDS

EIA/TIA-232-E (RS-232)

EIA/TIA-232-E is the oldest and most widely known DTE/DCE Interface Standard. It is a complete standard specifying the mechanical (connector(s)), electrical (driver/receiver characteristics), and functional (definition of circuits) requirements for a serial binary DTE/DCE Interface. Under the electrical section, the standard specifies an unbalanced, unidirectional, point-to-point interface. The drivers feature a controlled slew rate, this allows the cable to be seen as a lumped load, rather than a transmission line. This is due to the fact that the driver's transition time is substantially greater than the cable delay (velocity $\times$ length). The maximum capacitive load seen by the driver is specified at 2,500 pF. The standard allows for operation up to 20 kbps (19.2 kbps). For higher data rates EIA/TIA-562 or TIA/EIA-423-B are recommended. *Figure 3* illustrates a typical application, and Table I lists the major electrical requirements.

Key Features of the standard are:

- Single-Ended
- Point-to-Point Interface
- Large Polar Driver Output Swing
- Controlled Driver Slew Rate
- Fully Defined Interface
- 20 kbps Maximum Data Rate

TABLE I. EIA/TIA-232-E Major Electrical Specifications

Parameter	Limit & Units
Driver Loaded Output Voltages (3 kΩ)	$\geq \lvert 5.0V \rvert$
Driver Open Circuit Voltage	$\leq \lvert 25V \rvert$
Driver Short Circuit Current	$\leq \lvert 100\ mA \rvert$
Maximum Driver Slew Rate	$\leq 30\ V/\mu s$
Driver Output Resistance (Power Off)	$\geq 300\Omega$
Receiver Input Resistance	3 kΩ to 7 kΩ
Maximum Receiver Input Voltage	±25V
Receiver Thresholds	±3V

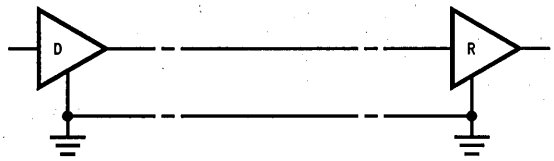

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FIGURE 3. Typical EIA/TIA-232-E Application

TIA/EIA-423-B

TIA/EIA-423-B while similar to EIA/TIA-232-E features a reduced driver output swing, and supports higher data rates. This standard specifies an unbalanced driver and a balanced receiver. It is an electrical standard, specifying driver and receiver requirements only. The receivers' requirements are identical to the receivers' requirements specified in TIA/EIA-422-B standard. TIA/EIA-423-B is intended to be referenced by complete standards, such as EIA/TIA-530-A. TIA/EIA-423-B specifies a unidirectional, multidrop (up to ten receivers) interface. Advantages over EIA/TIA-232-E include: multiple receiver operation, faster data rates, and common power supplies (typically ±5V). *Figure 4* illustrates a typical application, and Table II lists the major electrical requirements.

Note: RS-423-A is currently being revised; once approved it will become TIA/EIA-423-B. This is expected by the end of 1993. This section is based on the proposed draft standard.

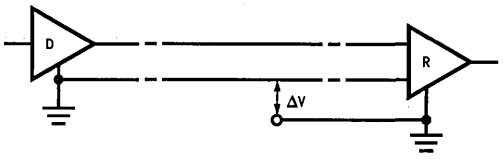

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FIGURE 4. Typical TIA/EIA-423-B Application

Key Features of the standard are:

- Unbalanced Driver and Balanced Receivers
- Multi-Drop (multiple receivers)
- Wave Shape Control (Driver Output)
- ±7V Receiver Common Mode Range
- ±200 mV Receiver Sensitivity
- 100 kbps Maximum Data Rate (@40 feet)
- 4000 Foot Maximum Cable Length (@ 1 kbps)

TABLE II. TIA/EIA-423-B Major Electrical Specifications

Parameter	Limit & Units
Driver Output Voltage (450Ω Load)	≥ |3.6V|
Driver Open Circuit Voltage	≥ |4.0V| & ≤ |6.0V|
Driver Short Circuit Current	≤ |150 mA|
Transition Time	Controlled
Driver Output Leakage Current	≤ |100 μA|
Receiver Specifications	See TIA/EIA-422-B

EIA/TIA-562

EIA/TIA-562 is a new electrical standard which is very similar to EIA/TIA-232-E, but supports higher data rates (64 kbps). It is an electrical only standard, which is intended to be referenced by complete standards, such as EIA/TAI-561. EIA/TIA-562 specifies an unbalanced, unidirectional, point-to-point interface. This standard supports interoperability with EIA/TIA-232-E devices. *Figure 5* illustrates a typical application, and Table III lists the major electrical requirements.

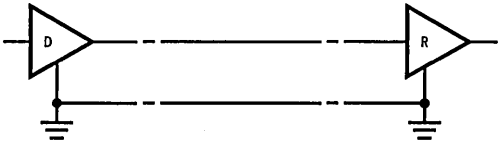

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FIGURE 5. Typical EIA/TIA-562 Application

Key Features of the standard are:

- Unbalanced Driver and Receiver
- Point-to-Point
- Inter-Operability with EIA/TIA-232-E Devices
- 64 kbps Maximum Data Rate

TABLE III. EIA/TIA-562 Major Electrical Specifications

Parameter	Limit & Units
Driver Loaded Output Voltage (Min. Level)	≥ | 3.3V |
Driver Open Circuit Output Voltage	≤ | 13.2V |
Driver Loaded Output Voltage (3 kΩ)	≥ | 3.7V |
Driver Short Circuit Current	≤ | 60 mA |
Driver Transition Time	Controlled
Maximum Driver Slew Rate	≤ 30 V/μs
Driver Output Resistance (Power Off)	≥ 300Ω
Receiver Input Resistance	3 kΩ to 7 kΩ
Maximum Receiver Input Voltage	±25V
Receiver Thresholds	±3V

TIA/EIA BALANCED (DIFFERENTIAL) STANDARDS

TIA/EIA-422-B

TIA/EIA-422-B is an electrical standard, specifying a balanced driver and balanced receivers. The receivers' requirements are identical to the receivers' requirements specified in TIA/EIA-423-B. This standard specifies a unidirectional, single driver, multiple receivers, terminated, balanced interface. *Figure 6* illustrates a point-to-point typical application with termination located at the receiver input (end of cable). *Figure 7* illustrates a fully loaded TIA/EIA-422-B interface. Again termination is located at the end of the cable, also stub length should be minimized to limit reflections. Table IV lists the major electrical requirements of the TIA/EIA-422-B Standard.

NOTE: RS-422-A is currently being revised; once approved it will become TIA/EIA-422-B. This is expected by the end of 1993. This section is based on the proposed draft standard.

Key Features of the standard are:

- Balanced Interface
- Multi-Drop (Multiple Receiver Operation)
- 10 Mbps Maximum Data Rate (@ 40 feet)
- 4000 Foot Maximum Cable Length (@ 100 kbps)

TABLE IV. TIA/EIA-422-B Major Electrical Specifications

Parameter	Limit & Units
Driver Open Circuit Voltage	≤ | 10V |
Driver Loaded Output Voltage	≥ | 2.0V |
Balance of Loaded Output Voltage	≤ 400 mV
Driver Output Offset Voltage	≤ 3.0V
Balance of Offset Voltage	≤ 400 mV
Driver Short Circuit Current	≤ |150 mA |
Driver Leakage Current	≤ | 100 μA |
Driver Output Impedance	≤ 100Ω
Receiver Input Resistance	≥ 4 kΩ
Receiver Thresholds	±200 mV
Receiver Internal Bias	≤ 3.0V
Maximum Receiver Input Current	3.25 mA
Receiver Common Mode Range	±7V (±10V)
Receiver Operating Differential Range	±200 mV to ±6V
Maximum Differential Input Voltage	±12V

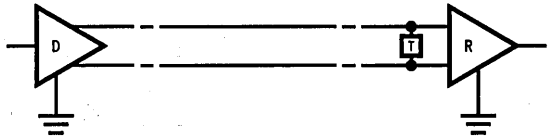

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FIGURE 6. Typical TIA/EIA-422-B Point-to-Point Application

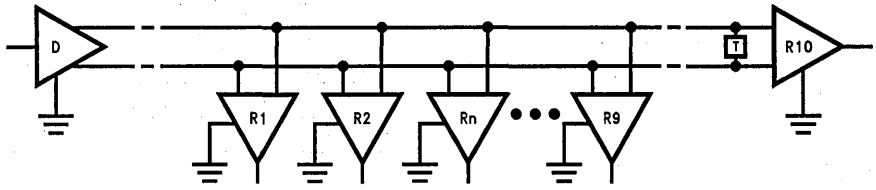

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FIGURE 7. Typical TIA/EIA-422-B Multidrop Application

EIA-485

EIA-485 is an electrical standard, specifying balanced drivers and receivers. It provides all the advantages of TIA/EIA-422-B along with supporting multiple driver operation. EIA-485 is the only TIA/EIA standard that allows for multiple driver operation. This fact allows for multipoint (party line) configurations. The standard specifies a bi-directional (half duplex), multipoint interface. *Figure 8* illustrates a typical multipoint application, and Table V lists the major electrical requirements.

Key Features are:

- Balanced Interface
- Multipoint Operation
- Operation From a Single +5V Supply
- −7V to +12V Bus Common Mode Range
- Up to 32 Transceiver Loads (Unit Loads)
- 10 Mbps Maximum Data Rate (@ 40 feet)
- 4000 Foot Maximum Cable Length (@ 100 kbps)

TABLE V. EIA-485 Major Electrical Specifications

Parameter	Limit & Units
Driver Open Circuit Voltage	≤ | 6.0V |
Driver Loaded Output Voltage	≥ | 1.5V |
Balance of Driver Loaded Output Voltage	≤ | 200 mV |
Maximum Driver Offset Voltage	3.0V
Balance of Driver Offset Voltage	≤ | 200 mV |
Driver Transition Time	≤ 30% Tui
Driver Short Circuit Current (−7V to +12V)	≤ | 250 mA |
Receiver Thresholds	±200 mV
Maximum Bus Input Current +12V/−7V	≤1.0 mA/≤ 0.8 mA

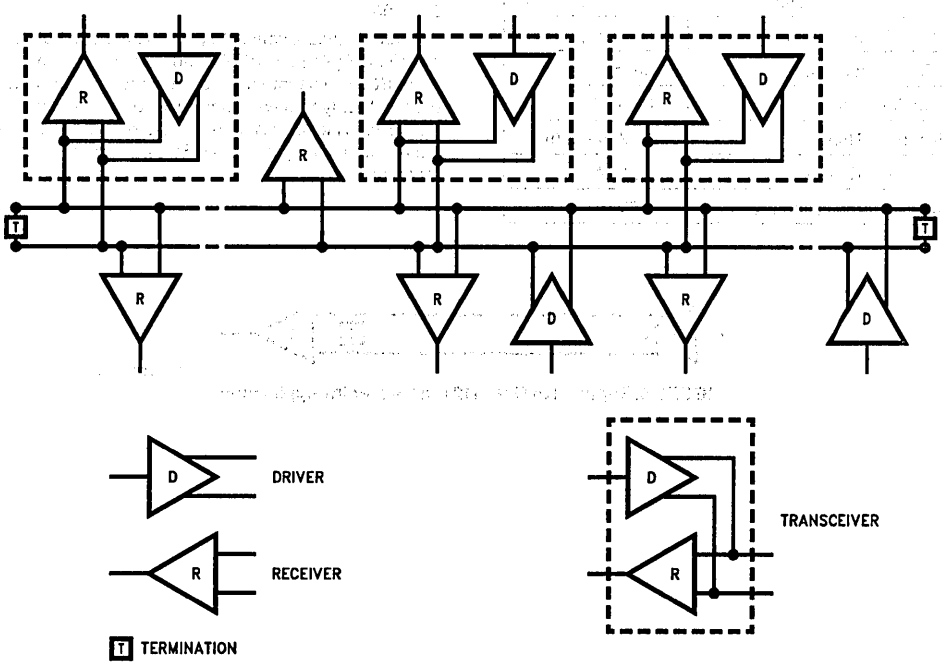

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FIGURE 8. Typical EIA-485 Application

TIA/EIA BALANCED (DIFFERENTIAL) STANDARDS

TIA/EIA-612

TIA/EIA-612 is an electrical standard, specifying a balanced driver and balanced receiver. This standard specifies data rates up to 52 Mbps using ECL technology. This standard specifies a unidirectional, point-to-point interface. *Figure 9* illustrates a typical application with termination located at the receiver input (end of cable). Table VI lists the major electrical requirements of the TIA/EIA-612 Standard. This Standard is referenced by TIA/EIA-613, and together implement a HSSI (High Speed Serial Interface).

TABLE VI. TIA/EIA-612 Major Electrical Specifications

Parameter	Limit and Units
Driver Open Circuit Voltage	≤ |1.5V|
Driver Loaded Output Voltage	≥ |590 mV|
Balance of Loaded Output Voltage	≤ |100 mV|
Driver Output Offset Voltage	≤ 0V and ≥ −1.6V
Balance of Offset Voltage	≤ |100 mV|
Driver Short Circuit Current	≤ 50 mA
Receiver Thresholds	±150 mV
Receiver Input Range	−0.5V to −2.0V
Receiver Input Current	≤ 350 μA
Maximum Differential Input Voltage	≤ 1.5V

OTHER EIA/TIA STANDARDS

EIA-334-A

EIA-334-A defines signal quality terms for synchronous serial DTE/DCE interfaces. This standard is referenced by the complete synchronous standards.

EIA-363

EIA-363 defines signal quality terms for non-synchronous serial DTE/DCE interfaces. This standard is referenced by the complete non-synchronous standards.

EIA-366-A

EIA-366-A defines a complete interface between Data Terminal Equipment (DTE) and Automatic Calling Equipment (ACE). The electrical requirements for the drivers and receivers are identical to those in EIA/TIA-232-E.

EIA-404-A

EIA-404-A defines signal quality for start-stop non-synchronous DTE/DCE interfaces.

EIA-408

EIA-408 defines a complete parallel interface between Data Terminal Equipment (DTE) and Numerical Control Equipment (NCE). The interface is limited to short distances and utilizes TTL type drivers and receivers. The drivers are required to sink 48 mA with a VOL of ≤0.4V, and source 1.2 mA with a V_{OH} of ≥ 2.4V. Short circuit protection is also recommended.

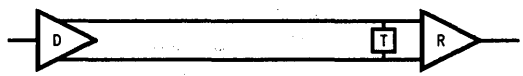

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FIGURE 9. Typical TIA/EIA-612 Point-to-Point Application

EIA-449

EIA-449 is a complete standard specifying a general purpose DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 37 position connector. This standard references TIA/EIA-422-B and TIA/EIA-423-B standards for line driver and receiver requirements and characteristics. The standard supports data rates up to 2 Mbps. The size of the specified connector has prevented wide spread acceptance of this standard. New designs are utilizing EIA/TIA-530-A instead of EIA-449.

EIA/TIA-530-A

EIA/TIA-530-A is a complete standard specifying a high speed DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 25 position connector. This standard references TIA/EIA-422-B and TIA/EIA-423-B standards for line driver and receiver requirements and characteristics. The standard supports data rates up to 2.1 Mbps. Two connector options are provided; a common 25 position D connector, and a smaller 26 position connector.

Note: Connector pinout differences exists between EIA-530 and EIA/TIA-530-A.

EIA/TIA-561

EIA/TIA-561 is a complete standard specifying a non-synchronous DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing & Control) and a small 8 position connector (MJ8). This standard references EIA/TIA-562 standard for line driver and receiver requirements and characteristics. The standard supports data rates up to 38.4 kbps.

EIA/TIA-574

EIA/TIA-574 is a complete standard specifying a non-synchronous DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 9 position connector. This standard references EIA/TIA-562 standard for line driver and receiver requirements and characteristics. The standard supports data rates up to 38.4 kbps.

TIA/EIA-613

TIA/EIA-613 is a complete standard specifying a general purpose DTE/DCE interface for data rates up to 52 Mbps. This standard specifies functional and connector specifications and references TIA/EIA-612 for electrical characteristics. Together TIA/EIA-612 and TIA/EIA-613 implement a HSSI interface.

CCITT STANDARDS (ITU)

CCITT (International Telegraph and Telephone Consultative Committee) creates and maintains standards which are intended to help standardize international telecommunication services. These standards are recommended technical practices and approaches, however, in some countries they can be considered mandatory. CCITT reviews its standards on a 4 year cycle. Many of the Interface standards are located in volume eight of the CCITT "V" series. This volume is titled "Data Communication over the Telephone Network". Some of the Interface standards are also covered in the "X" series. The CCITT prefix has been replaced by ITU for International Telecommunications Union and the term CCITT will eventually be phased out. A cross reference is provided in Table VII.

TABLE VII. V and X Series Cross Reference

V Series	X Series
V.10	X.26
V.11	X.27

Recommendation V.10

Recommendation V.10 defines the electrical characteristics for an unbalanced interface. This recommendation specifies an unbalanced driver and a balanced receiver. With the exception of generator (driver) open circuit output voltage specification, V.10 generator (driver) requirements are very similar to the TIA/EIA-423-B standard. In V.10 the driver is loaded with a 3.9 kΩ resistor to ground, while in the TIA/EIA-423-B standard the driver is unloaded. The V.10 receiver is specified with ±300 mV thresholds, while the TIA/EIA-423-B receiver supports a tighter specification of ±200 mV. Other smaller differences also exist. Therefore, for exact conditions and requirements consult the respective standards.

Recommendation V.11

Recommendation V.11 defines the electrical characteristics for a balanced Interface. V.11 specifies a balanced driver and balanced receivers. With the exception of generator (driver) open circuit output voltage specification, V.11 generator (driver) requirements very similar to the TIA/EIA-422-B

standard. V.11 requires a 3.9 kΩ differential load for the driver's open circuit output, while TIA/EIA-422-B test conditions require no load (open circuit). The Receiver specifications are also very similar, with the exception of the input threshold specification. Recommendation V.11 requires thresholds of ±300 mV while TIA/EIA-422-B requires a tighter specification of ±200 mV. Other smaller differences also exist. Therefore, for exact conditions and requirements consult the respective standards.

Recommendation V.24

Recommendation V.24 defines the function of interchange circuits for DTE/DCE interfaces. Circuit class (Data, Timing, or Control), direction, and definition are all defined in this recommendation. V.24 is intended to be referenced by other recommendations.

Recommendation V.28

Recommendation V.28 defines the electrical characteristics for an unbalanced Interface. This standard specifies driver output and receiver input characteristics. The standard is very similar to the Electrical section (2) of the EIA/TIA-232-E standard. The one notable exception in the generator (driver) requirements is the slew rate specification. The EIA/TIA-232-E lower limit for slew rate is 3 V/μs (@20 kbps), (measured between the +3V and −3V level), while in V.28 the lower limit is 4 V/μs (@20 kbps). Both standards specify the same upper limit of 30 V/μs under light loading conditions. EIA/TIA-232-E defines the complete interface, while V.28 only defines the electrical section of EIA/TIA-232-E. The complete interface standard is covered by CCITT Recommendations V.28 (electrical), V.24 (functional), and ISO 2110 & 4902 (mechanical). For complete specifications refer to CCITT Recommendation V.28.

Recommendation V.35

Recommendation V.35 is actually a modem standard that also defines a balanced interface. While many applications operate at data rates substantially higher than 48 kbps (typically > 1 Mbps), the interface is only defined to operate up to 48 kbps. For low speed control lines the standard recommends the use of V.28 generators (drivers) and receivers. For use on high speed data and timing lines the standard recommends the use of unique V.35 balanced generators (drivers). The drivers feature a small swing of ±0.55V across a termination load of 100Ω. The generator is also specified to have polar swings around ground, yielding a 0V offset voltage. Most implementations use differential current mode drivers with external resistors to implement V.35 balanced generators. V.35 has been rescinded, and V.10 and V.11 generators are recommended as replacements.

US MILITARY STANDARDS

MIL STD 188C (Low Level)

Military Standard 188C (MIL-STD-188C) is similar to EIA/TIA-232-E in the fact that it specifies an unbalanced point-to-point interface. However, the driver's requirements are slightly different. The driver is still required to develop a | 5V | level. The maximum driver output level is specified at | 7V |, and the match between V_{OL} and V_{OH} levels must be within 10% of each other. The driver's slew rate is specified to be between 5% and 15% of the applicable modulation rate. Most drivers require an external capacitor to control the slew rate. *Figure 10* illustrates a typical application, and Table VIII lists the major electrical specification of MIL-STD-188C.

TABLE VIII. MIL-STD-188C Major Electrical Specifications

Parameter	Limit & Units
Unloaded Driver Output Level	±5V Min., ±7V Max.
Driver Output Resistance (Power ON) ($I_O \leq 10$ mA)	100Ω Max.
Driver Output Short Circuit Current	±100 mA
Driver Output Slew Rate	5% to 15% of Modulation Rate
Receiver Input Resistance	≥6 kΩ
Receiver Input Thresholds	±100 μA

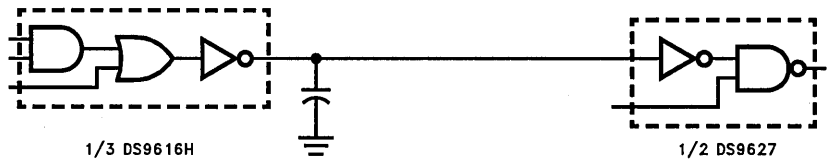

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FIGURE 10. Typical MIL-STD-188C Application

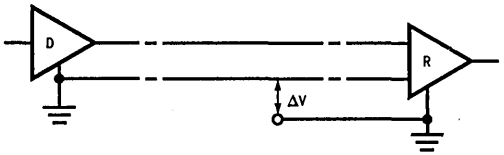

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FIGURE 11. MIL STD 188-114A Unbalanced Typical Application

MIL STD 188-114A

Military Standard 188-114 specifies four different interfaces; three balanced and one unbalanced. The balanced interfaces are divided into three types, two of which are voltage mode, and one of which is current mode. See *Figures 11, 12* and *13*. Voltage mode, type 1, defines an interface for data rates up to 100 kbps. An additional requirement of type 1 is a polar (around ground) output swing. This provides a zero offset output voltage. Voltage mode, type 2, drivers operate up to 10 Mbps and require the same parameters as EIA/TIA-422-A drivers. Additionally, type 2, drivers can have an output offset up to 3V. Current mode, type 3, drivers operate beyond 10 Mbps. The receiver specified for type 1 & 2 balanced, and unbalanced drivers are identical to the receivers specified in TIA/EIA-422-B and TIA/EIA-423-B standards.

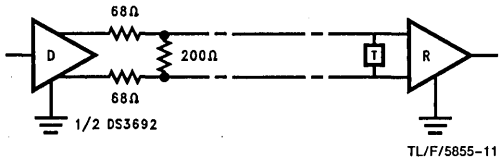

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FIGURE 12. MIL STD 188-114A Balanced, Type 1 Typical Application

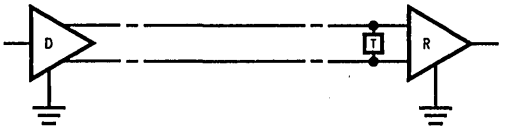

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FIGURE 13. MIL STD 188-114A Balanced, Type 2 Typical Application

MIL STD 1397

Military Standard 1397 specifies two interfaces. These are termed "slow" and "fast". The slow interface operates up to 42 kbps, while the fast interface is defined to operate up to 250 kbps. Comparators and/or discretes components are used to implement drivers and receivers.

FEDERAL TELECOMMUNICATIONS STANDARDS

Federal Standards are from the Federal Telecommunications Standards Committee, which is an advisory committee that adopts TIA/EIA interface standards.

FED STD 1020A

The FEDSTD 1020A is identical to TIA/EIA-423-B. It is intended for United States, non-military government use.

FED STD 1030A

The FEDSTD 1030A is identical to TIA/EIA-422-B. It is intended for United States, non-military government use.

OTHER STANDARDS

IEEE488

The IEEE (Institute of Electrical and Electronics Engineers) also has a standard developing arm. Generally the IEEE standards deal with complete Bus specifications. IEEE488 is a complete Bus standard covering the electrical, mechanical, and functional specification of a parallel instrumentation bus. The bus is commonly used for communication of lab test equipment and machinery control. The standard allows for 15 devices to be connected together, over cable lengths up to 60 feet. The standard defines 16 lines composed of 3 control, 5 management, and 8 data lines. The major electrical specifications are summarized in Table IX.

TABLE IX. Major IEEE488 Electrical Requirements

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Driver Output Voltage	$I_{OH} = -5.2$ mA	2.4		V
V_{OL}	Driver Output Voltage	$I_{OL} = 48$ mA		0.4	V
I_{OZ}	Driver Output Leakage Current	$V_O = 2.4V$		±40	μA
I_{OH}	Driver Output Current Open Collector	$V_O = 5.25V$		250	μA
V_{IH}	Receiver Input Voltage		2.0		V
V_{IL}	Receiver Input Voltage			0.8	V
I_{IH}	Receiver Input Current	$V_{IN} = 2.4V$		40	μA
I_{IL}	Receiver Input Current	$V_{IN} = 0.4V$		−1.6	mA
I_{CL}	Receiver Clamp Current	$V_{IN} = -1.5V$		12	mA
RL_1	Termination Resistor	$V_{CC} = 5V \pm 5\%$	2850	3150	Ω
RL_2	Termination Resistor	V = GND	5890	6510	Ω

GA-22-6974-0

IBM specification GA-22-6974-0 specifies the electrical characteristics, format of information, and the control scheme of an unbalanced interface. This interface is mainly used on 360/370 equipment and allows up to 10 I/O ports. This unbalanced interface employs 95Ω terminated coax cable. Drivers normally feature open-emitter designs, and short-circuit limiting. Receivers normally feature hysteresis to prevent output oscillations for slow rising inputs in noisy environments. Care should be taken to limit cable lengths such that noise is limited to less than 400 mV. *Figure 14* illustrates a typical application, and Table X lists the major electrical requirements.

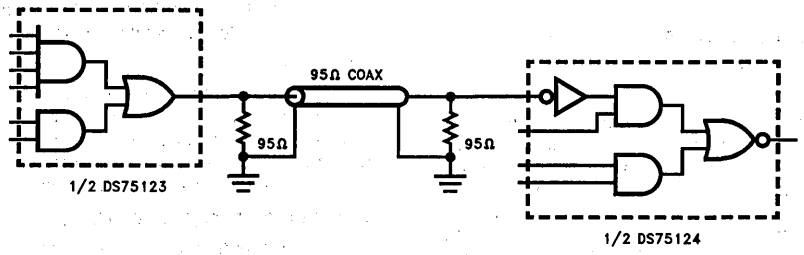

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FIGURE 14. GA-22-6974-0 Typical Application

TABLE X. Major Electrical Requirements of GA-22-6974-0

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Driver Output Voltage	I_{OH} = 123 mA		7	V
V_{OH}		I_{OH} = 30 μA		5.85	V
V_{OH}		I_{OH} = 59.3 mA	3.11		V
V_{OL}		I_{OL} = −240 μA		0.15	V
V_{IH}	Receiver Input Threshold			1.7	V
V_{IL}			0.7		V
I_{IH}	Receiver Input Current	V_{IN} = 3.11V		−0.42	mA
I_{IL}		V_{IN} = 0.15V	0.24		mA
	Receiver Input Voltage Range				
V_{IN}	Power ON		−0.15	7	V
V_{IN}	Power OFF		−0.15	6	V
R_{IN}	Receiver Input Impedance	0.15V ≤ V_{IN} ≤ 3.9V	7.4		kΩ
I_{IN}	Receiver Input Current	V_{IN} = 0.15V		240	μA
Z_O	Cable Impedance		83	101	Ω
R_O	Cable Termination	PD ≤ 390 mW	90	100	Ω
	Noise (Signal and Ground)			400	mV

CONCLUSION

This application note provides a brief overview of various interface standards from several standardization organizations. It is only intended to point out the major requirements of each standard and to illustrate a typical application. When selecting or designing a standardized interface it is highly recommended to carefully review the complete standard.

Standards can be ordered from the respective organizations or from:

Global Engineering Documents
2805 McGraw Avenue
P.O. Box 19539
Irvine, CA 92714
USA
(800) 854-7179

Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard

National Semiconductor
Application Note 409
Sivakumar Sivasothy

INTRODUCTION

The Electronics Industries Association (EIA), in 1983, approved a new balanced transmission standard called RS-485. The EIA RS-485 standard addresses the problem of data transmission, where a balanced transmission line is used in a party-line configuration. It is similar in many respects to the popular EIA RS-422 standard; in fact RS-485 may be considered the outcome of expanding the scope of RS-422 to allow multipoint—multiple drivers and receivers sharing the same line—data transmission. The RS-485 standard, like the RS-422 standard, specifies only the electrical characteristics of the driver and the receiver to be used at the line interface; it does not specify or recommend any protocol. The protocol is left to the user.

The EIA RS-485 standard has found widespread acceptance and usage since its ratification. Users are now able to configure inexpensive local area networks and multi-drop communication links using twisted pair wire and the protocol of their choice. They also have the flexibility to match cable quality, signalling rate and distance to the specific application and thus obtain the best tradeoff between cost and performance. The acceptance of the RS-485 standard is also reflected by the fact that other standards refer to it when specifying multipoint data links. The ANSI (American National Standards Institute) standards IPI (Intelligent Peripheral Interface) and SCSI (Small Computer Systems Interface) have used the RS-485 standard as the basis for their voltage mode differential interface class. The IPI standard specifies the interface between disc drive controllers and host adapters and requires a data rate of 2.5 megabaud over a 50 meters NRZ data link. The SCSI standard specifies the interface between personal computers, disc drives and printers at data rates up to a maximum of 4 megabaud over 25 meters.

It is not possible to use standard gate structures and meet the requirements of RS-485. The modifications necessary to comply with the DC requirements of the standard, tend to exact a heavy toll on speed and other AC characteristics like skew. However, it is possible to vastly improve the ac performance by employing special design techniques. The DS3695 family of chips made by National Semiconductor meets all the requirements of EIA RS-485, and still provides ac performance comparable with most existing RS-422 devices. The chip set consists of four devices; they are the DS3695/DS3696 transceivers and the DS3697/DS3698 repeaters. National's RS-485 devices incorporate several features in addition to those specified by the RS-485 standard. These features provide greater versatility, easier use and much superior performance. This article discusses the requirements of a multi-point system, and the way in which RS-485 addresses these requirements. It also explains the characteristics necessary and desirable in the multi-point drivers and receivers, so that these may provide high performance and comply with generally accepted precepts of data transmission practice.

WHY RS-485?

Until the introduction of the RS-485 standard, the RS-422 standard was the most widely accepted interface standard for balanced data transmission. The RS-422 drivers and re-

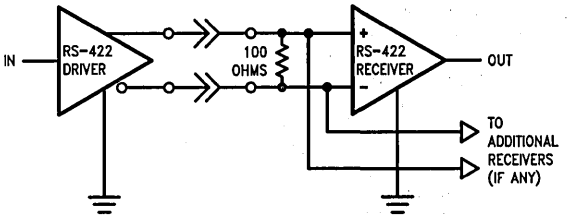

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FIGURE 1a. An RS-422 Configuration

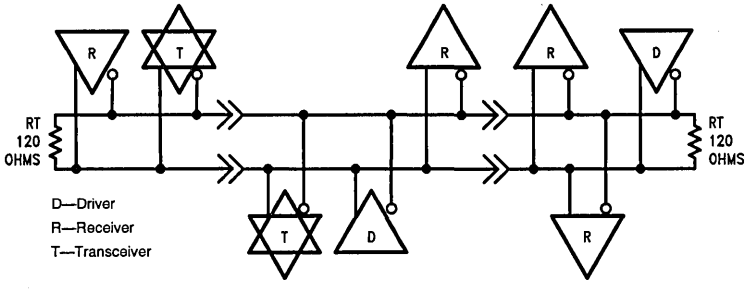

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FIGURE 1b. A Typical RS-485 Party-Line Configuration

ceivers were intended for use in the configuration shown in *Figure 1a*. The driver is at one end of the line; the termination resistor (equal to 100Ω) and up to 10 receivers reside at the other end of the line. This approach works well in simplex (unidirectional) data transmission applications, but creates problems when data has to be transmitted back and forth between several pieces of equipment. If several Data Terminal Equipments (DTEs) have to communicate with one another over long distances using RS-422 links, two such balanced lines have to be established between each pair of DTEs. The hardware cost associated with such a solution would normally be unacceptable.

A party line is the most economical solution to the above problem. RS-422 hardware could conceivably be used to implement a party line if the driver is provided with TRI-STATE® capability, but such an implementation would be subjected to severe restrictions because of inadequacies in the electrical characteristics of the driver. The biggest problem is caused by ground voltage differences. The common mode voltage on a balanced line is established by the enabled driver. The common mode voltage at the receiver is the sum of the driver offset voltage and the ground voltage difference between the driver and the receiver. In simplex systems only the receiver need have a wide common mode range. Receiver designs that provide a wide common mode range are fairly straightforward. In a party-line network several hundred feet long, in which each piece of equipment is earthed at a local ac outlet, the ground voltage difference between two DTEs could be as much as a few volts. In such a case both the receiver and the driver must have a wide common mode range. Most RS-422 drivers are not designed to remain in the high impedance state over a wide enough common mode range, to make them immune to even small ground drops.

Classical line drivers are vulnerable to ground drops because of their output stage designs. A typical output stage is shown in *Figure 2a*. Two such stages driven by complementary input signals, may be used to provide the complementary outputs of a differential line driver. Transistors Q1 and Q4 form a Darlington pull up for the totem pole output stage; Q2 is the pull down transistor. The phase splitter Q3 switches current between the upper and lower transistors to obtain the desired output state. DSUB is the diode formed by the collector of Q2 and the grounded substrate of the integrated circuit. The output in *Figure 2a* can be put into the high impedance state by pulling down the bases of transistors Q3 and Q4. Unfortunately, the high impedance state cannot be maintained if the output is pulled above the power supply voltage or below ground voltage. In party-line applications, where ground voltage differences of a few volts will be common, it is essential that the drivers be able to hold the high impedance state while their outputs are taken above V_{CC} and below ground.

The output in *Figure 2a* can be taken high until the emitter-base junction of Q1 breaks down. Thereafter, the output will be clamped to a zener voltage plus a base-collector diode voltage above V_{CC}; V_{CC} could be zero if the device is powered off. If the output is taken below ground, it will cause the substrate diode, DSUB, associated with Q2 to turn on and clamp the output voltage at a diode drop below ground. If a disabled driver turns on and clamps the line, the signal put out by the active driver will get clipped and distorted. It is also possible for ground drops to cause dangerously large substrate currents to flow and damage the devices as illustrated in *Figure 2b*. *Figure 2b* depicts two drivers A and B; it shows the pull down transistors (Q2A and Q2B) and their associated substrate diodes (DSUB-A and DSUB-B) for the two drivers A and B. Here driver A is ON in the low output state; driver B is disabled, and therefore, should neither source nor sink current. The ground of driver A is 3 volts lower than that of driver B. Consequently, the substrate diode DSUB-B sees a forward bias voltage of about 2.7V (the collector-emitter voltage of Q2A will be about 0.3V), which causes hundreds of milliamperes of current to flow out of it.

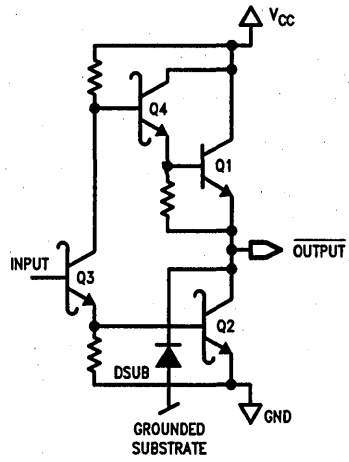

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FIGURE 2a. Driver Output Stage (not RS-485)

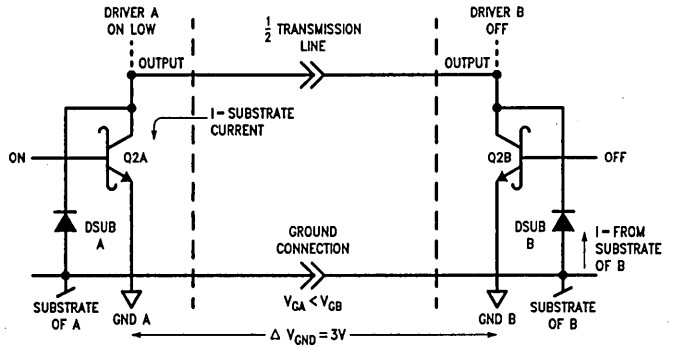

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FIGURE 2b. Two DCEs Separated by a Ground Drop

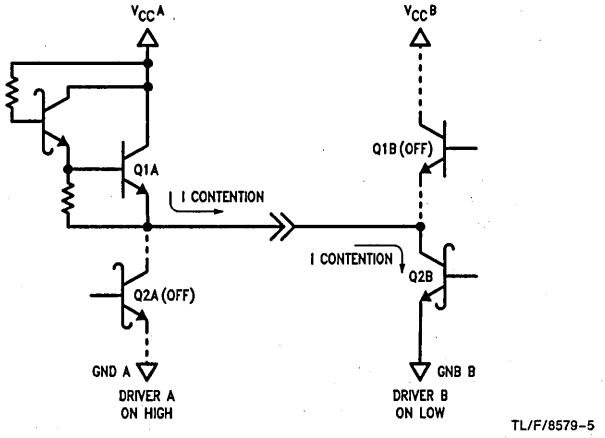

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FIGURE 2c. Bus Contention

Another problem is line contention, i.e. two drivers being 'ON' simultaneously. Even if the protocol does not allow two drivers to be on at the same time, such a contingency could arise as a result of a fault condition. A line contention situation, where two drivers are on at the same time, is illustrated in *Figure 2c*. Here, drivers A and B are 'ON' simultaneously; driver A is trying to force a high level on the line whereas driver B is trying to force a low level. Transistors Q1A and Q2B are 'ON' while transistors Q2A and Q1B are 'OFF'. As a result, a large current is sourced by Q1A and sunk by Q2B; the magnitude of this current is limited only by the parasitic resistances of the two devices and the line. The problem is compounded by any ground drop that may exist between the two contending drivers. This large contention current can cause damage to one or both of the contending drivers. Most RS-422 drivers are not designed to handle line contention.

A multi-point driver should also be capable of providing more drive than a RS-422 driver. The RS-422 driver is only required to drive one 100Ω termination resistor, and ten receivers each with an input impedance no smaller than 4 kΩ. A party-line, however, would have to be terminated at both ends; it should also be able to drive more devices to be useful and economical.

Because of the above limitations, it is quite impractical to use RS-422 hardware to interconnect systems on a party-line. Clearly, a new standard had to be generated to meet the more stringent hardware requirements of muti-point data links.

THE RS-485 STANDARD

The RS-485 standard specifies the electrical characteristics of drivers and receivers that could be used to implement a balanced milti-point transmission line (party-line). A data exchange network using these devices will operate properly in the presence of reasonable ground drops, withstand line contention situations and carry 32 or more drivers and receivers on the line. The intended transmission medium is a 120Ω twisted pair line terminated at both ends in its characteristic impedance. The drivers and receivers can be distributed between the termination resistors as shown in *Figure 1b*.

The effects of ground voltage differences are mitigated by expanding the common mode voltage (V_{CM}) range of the driver and the receiver to $-7V < V_{CM} < +12V$. A driver forced into the high impedance state, should be able to have its output taken to any voltage in the common mode range and still remain in the high impedance state, whether powered on or powered off. The receiver should respond properly to a 200 mV differential signal super-imposed on any common mode voltage in this range. With a 5V power supply, the common mode voltage range specified by RS-485 has a 7V spread from either supply terminal. The system will therefore perform properly in the presence of ground drops and longitudinally coupled extraneous noise, provided that the sum of these is less than 7 volts.

The output drive capability of the driver and the input impedance of the receiver are increased to accommodate two termination resistors and several devices (drivers, receivers and transceivers) on the line. The RS-485 standard defines a 'unit load' so that the load presented to the line by each device can be expressed in terms of unit loads (a 12 kΩ resistor, with one end tied to any voltage between ground and $V_{CC}/2$, will satisfy the requirements of a unit load). It was anticipated that most manufacturers would design their drivers and receivers such that the combined load of one receiver and one disabled driver would be less than one unit load. This would require the RS-485 receiver to have three times the input resistance of a RS-422 receiver. The required receiver sensitivity is ±200 mV—the same as for RS-422. The driver is required to provide at least 1.5V across its outputs when tied to a terminated line populated with 32 transceivers. Although this output voltage is smaller than the 2.0V specified for RS-422, a careful design of the driver, with special regard to ac performance, can allow the user to operate a multi-point network at data rates and distances comparable to RS-422.

RS-485 has additional specifications to guarantee device safety in the event of line contention or short circuits. An enabled driver whose output is directly shorted to any voltage in the common mode range, is required to limit its current output to ±250 mA. Even with such a current limit, it is possible for a device to dissipate as much as 3 Watts (if the device draws 250 mA while shorted to 12 volts). Power dissipation of such a magnitude will damage most ICs; therefore, the standard requires that manufacturers include some additional safeguard(s) to protect the devices in such situations.

The ±250 mA current limit also serves another purpose. If a contending driver is abruptly turned off, a voltage transient, of magnitude $I_C Z/2$, is reflected along the line as the line discharges its stored energy (I_C is the contention current and Z is the characteristic impedance of the line). This voltage transient must be small enough to avoid breaking down the output transistors of the drivers on the line. If the contention current is limited to 250 mA, the magnitude of this voltage transient, on a 120Ω line, is limited to 15V, a value that is a good compromise between transistor breakdown voltage and speed.

AC PERFORMANCE

To achieve reliable transmission at high data rates over long distances, the driver should have optimum ac characteristics. The response should be fast and the output transients sharp and symmetrical.

(1) **Propagation Delay:** The propagation delay through the driver should be small compared to the bit interval so that the data stream does not encounter a bottle-neck at the driver. If the propagation delay is comparable to the bit interval, the driver will not have time to reach the full voltage swing it is capable of. In lines a few hundred feet long, the line delay would impose greater limits on data throughput than the driver propagation delay. However, a fast driver would be desirable for short haul networks such as those in automobile vehicles or disc drives; in the latter case high data throughput would be essential. Driver propagation delays less than 20 ns would be very good for a wide range of applications.

(2) **Transition Time:** For distortion free data transmission, the signal at the farthest receiver must have rise and fall times much smaller than the bit interval. Signal distortion results from driver imbalance, receiver threshold offset and skew. RS-485 limits the DC imbalance in the driver output to ±0.2V i.e., 13% of worst-case signal amplitude. Usually, the greatest distortion is caused by offset in the receiver threshold. In a long line in which a 1.5V driver output signal amplitude is attenuated by the loop resistance to about 0.4V, a 200 mV offset in the receiver threshold can cause severe pulse width distortion if the rise time is comparable to the bit interval. For lines longer than about five hundred feet, the rise time would be dominated by the line and not the driver. In short-haul networks, the transient response of the driver can significantly affect signal distortion; a faster transient creates less distortion and hence permits a smaller bit interval and a higher baud rate. A rise time less than 20 ns will be a good target spec., for it will permit a baud rate of 10 Meg over 50′ of standard twisted pair wire with less than 5% distortion.

The driver should provide the above risetime and propagation delay numbers while driving a reasonable capacitance, say 100 pF from each output, in addition to the maximum resistive load of 54Ω. A properly terminated transmission line appears purely resistive to the driver. Most manufacturers take this into account and specify their driver delays with 15 pF loads. However, if any disabled transceivers are situated close to the driver (such that the round trip delay is less than the rise time), the input capacitances of these transceivers will appear as lumped circuit loads to the driver. The driver output rise time will then be affected by all other devices in such close proximity. In the case of high speed short-haul networks, where rise time and propagation delay are critical, several devices could be clustered in a short span. In such an instance, specifying propagation delays with 15 pF loads is quite meaningless. A 100 pF capacitive load is more reasonable; even if we allocate a generous 20 pF per transceiver, it allows up to six transceivers to be clustered together in an eight foot span (the eight foot span is the approximate round trip distance travelled by the wavefront in one rise time of 20 ns).

(3) **Skew:** The ideal differential driver will have the following waveform characteristics: the propagation delay times from the input to the high and low output states will be equal; the rise and fall times of the complementary outputs will be equal and the output waveforms will be perfectly symmetrical.

If the propagation delay to the low output state is different from the propagation delay to the high output state, there is said to be 'propagation skew' between output states. If a square wave input is fed into a driver with such skew, the output will be distorted in that it will no longer have a 50% duty cycle.

If the mid-points of the waveforms from the two complementary driver outputs are not identical, there is said to be SKEW between the complementary outputs. This type of skew is undesirable because it impairs the noise immunity of the system and increases the amount of electromagnetic emission.

Figure 3a shows the differential signal from a driver that has no skew. *Figure 3b* shows the case when there is 80 ns of skew. The first signal makes its transition uniformly and passes rapidly through 0V. The second waveform flattens out for tens of nanoseconds near 0V. Unfortunately, this flat region occurs near the receiver threshold. A common mode noise spike hitting the inputs of a slightly unbalanced receiver would create a small differential noise pulse at the receiver inputs. If this noise

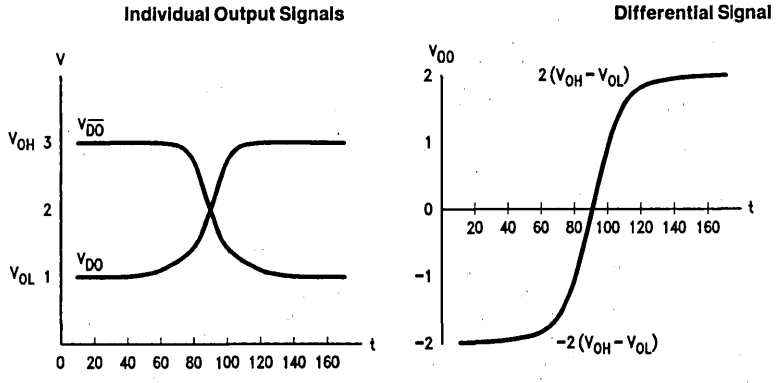

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FIGURE 3a. Transients with no Skew

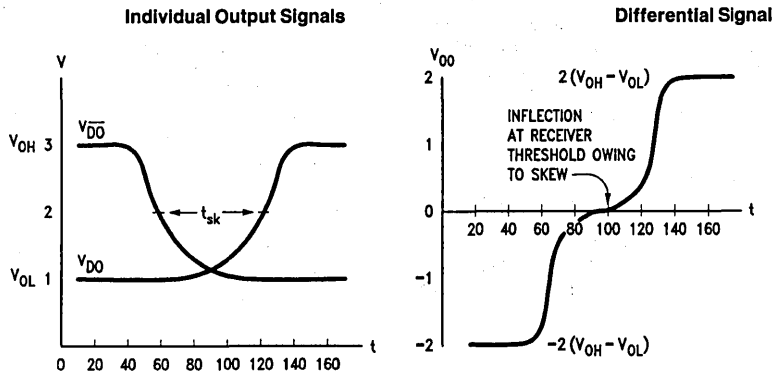

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FIGURE 3b. Skewed Transients

pulse occurs when the driver transition is flat near 0V, there will be a glitch at the receiver output. A glitch could also occur if a line reflection reaches the receiver input when the driver transition is temporarily flat. Skew is insidious in that it can cause erroneous outputs to occur at random. It can also increase the amount of electromagnetic interference (EMI) generated by the transmission system. If the complementary outputs are perfectly symmetrical, and the twisted pair medium is perfectly balanced, the radiation from one wire is cancelled exactly by the radiation from the other wire. If there is skew between the outputs, there will be net radiation proportional to the skew.

(4) **Balance:** The impedance seen looking into each of the complementary inputs of the transceiver should be identical. If there is any imbalance at these nodes, the common mode rejection will be degraded. Any DC imbalance, due to a mismatch in the receiver input resistances, will manifest itself as an offset in the receiver threshold, and can be easily detected during testing. AC imbalance is more difficult to detect, but it can hurt noise immunity at high frequencies. A sharp common mode noise spike striking an unbalanced receiver will cause a spurious differential signal. If the receiver is fast enough (as it is bound to be in most cases), it will respond to this noise signal. It is best to keep the imbalance below 4 pF. This number is reasonable to achieve; in addition, the combined imbalance of 32 transceivers will still provide sufficient immunity from h.f. interference.

DESIGN CONSIDERATIONS

The driver poses the greatest design challenge. Its speed, drive and common mode voltage requirements are best met using a bipolar process. National Semiconductor uses an established Schottky process with a 5μ deep epitaxial layer. NPN transistors are fabricated with LVCEO values greater than 15V to satisfy the breakdown requirements. It will be seen that lateral PNP transistors are crucial to the driver. The 5μ EPI process provides adequate lateral PNP transistors, and NPN transistors of sufficient speed.

Figure 4 shows the driver output circuit used by National. It is a standard totem pole output circuit modified to provide a common mode range that exceeds the supply limits. If the driver output is to be taken to −7V while the driver is in TRI-STATE, precautions must be taken to prevent the substrate diodes from turning on. This is achieved in the lower output transistor Q1 by including Schottky diode S1 in series. The only way to isolate the upper half of the totem pole from the substrate is by using a lateral PNP transistor. In *Figure 4,* a lateral PNP transistor is used to realize current source IG. Lateral PNP transistors are, however, notoriously slow; the trick therefore is not to use the PNP transistor in the switching path. In the circuit shown, the PNP transistor is a current source which feeds NPN transistor Q2 and therefore, does not participate in the switching function. This allows National's driver to have 15 ns propagation delays and 10 ns rise times. A Darlington stage cannot be used instead of Q2 because it would reduce the voltage swing below the 1.5V specification. Consequently, the rise time is bound to be significantly larger than the fall time, resulting in a large skew. National's driver uses a patented circuit with a plurality of discharge paths, to slow down the fall time so that it matches the rise time, and to keep the two transition times on track over temperature. This keeps the skew small (2 ns typical at 25°C) over the entire operating temperature range. The symmetry of the complementary outputs of National's DS3695 driver can be seen from the photographs in *Figure 5.* The lateral PNP transistor which has been kept out of the switching path has nevertheless got to be turned on or off when the driver is respectively enabled or disabled. Another patented circuit is used to hasten turn-on and turn-off of the lateral PNP transistors so that these switch in 25 ns instead of in 100 ns. Consequently, the driver can be enabled or disabled in 35 ns.

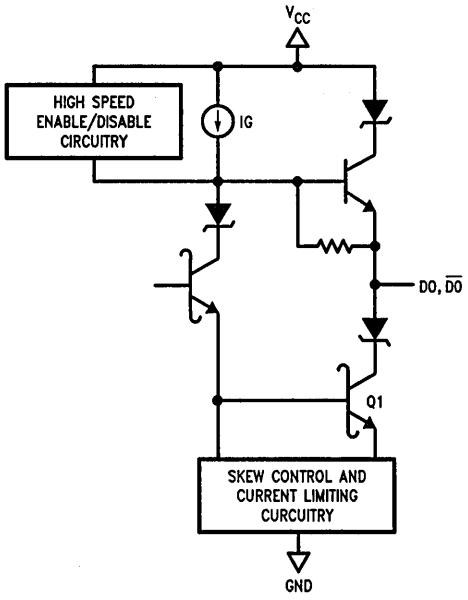

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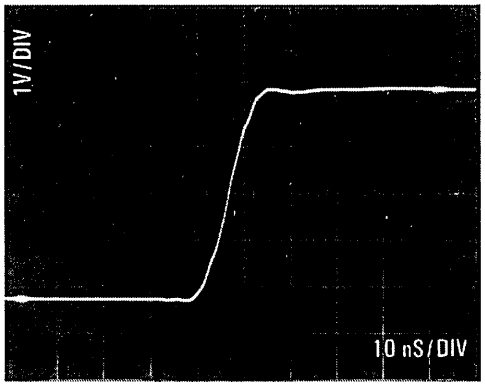
FIGURE 4

Differential Output of National's RS-485 Driver



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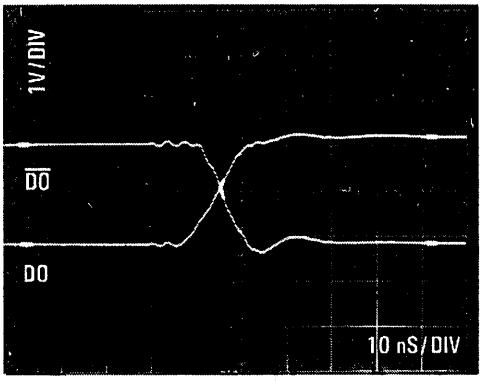
Complementary Outputs of National's RS-485 Driver



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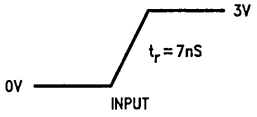

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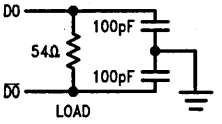

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FIGURE 5

The devices must be protected in fault conditions and contention situations. One way of doing this is by sensing current and voltage to determine power, and then if necessary, turning the device off or limiting its output current to prevent damage. This method has the advantage of fast detection of a fault and rapid recovery from one. However, too many contingencies have to be accounted for; the corresponding circuitry will increase the die size and the cost beyond what would be acceptable in many low cost applications. National preferred the simpler and inherently more reliable thermal shutdown protection scheme. Here, the device is disabled when the die temperature exceeds a certain value. This method is somewhat slower (order of milliseconds), but fast enough to protect the part. A fault would usually result from a breakdown in network protocol or from a hardware failure. In either case it is immaterial how long the device takes to shut down or recover as long as it stays undamaged. It would be useful to be notified of the occurrence of a fault in any particular channel, so that remedial action may be taken. Two of National's devices, the DS3696 receiver and the DS3698 repeater, provide a fault reporting pin which can flag the processor or drive an alarm LED in the event of a fault. National also decided to make its devices as single transceivers housed in 8 pin mini DIP packages. If thermal shutdown protection is employed, it is pointless to have dual or quad versions because a faulty channel will shut down a good one. Since most RS-485 applications will employ single channel serial data, the 8 pin package will give optimum flexibility, size and economy.

The receiver has 70 mV (typical) hysteresis for improved noise immunity. Hysteresis can contribute some distortion, especially in short lines, if the rise and fall times are different. However, this is more than adequately compensated for by the noise immunity it provides with long lines where rise times are slow. The matched rise and fall times with National's drivers assure low pulse width distortion even at short distances and high data rates.

Low Power RS-232C Driver and Receiver in CMOS

National Semiconductor
Application Note 438
Gordon W. Campbell

This article sets out to describe the new innovative low power CMOS RS-232C driver and receiver IC's introduced by National Semiconductor with particular reference to the EIA RS-232C standard. Comparison will also be made with existing bipolar driver and receiver circuits.

The DS14C88 and DS14C89A are monolithic MOS circuits utilizing a standard CMOS process. Important features are a wide operating voltage range (4.5V–12.6V), together with ESD and latch up protection and proven reliability.

The Electronics Industries Association released Data Terminal Equipment (DTE) to Data Communications Equipment (DCE) interface standards to cover the electrical, mechanical and functional interface between/among terminals (i.e. teletypewriters, CRT's etc.) and communications equipment (i.e. modems, cryptographic sets etc.).

The EIA RS-232C is the oldest and most widely known DTE/DCE standard. Its European version is CCITT V.24 specification. It provides for one-way/non-reversible, single ended (unbalanced) non-terminated line, serial digital data transmission.

The DS14C88 quad CMOS driver and its companion circuit, the DS14C89A quad CMOS receiver, combine to provide an efficient low power system for RS-232C or CCITT V.24 applications.

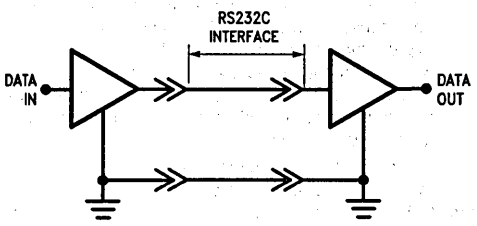

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FIGURE 1. EIA RS-232C Application

THE DRIVER

The DS14C88 quad CMOS line driver is a pin replacement of the existing bipolar circuit DS1488/MC1488.

The DS14C88 is fabricated in CMOS technology and therefore has an inherent advantage over the bipolar DS1488/MC1488 line driver in terms of current consumption. Under worst case static conditions, the DS14C88 is a miser when it comes to current consumption. In comparison with the DS1488/MC1488 line driver, a current consumption reduction to 500 μA max versus 25 mA can be achieved.

The RS-232C specification states that the required driver output voltage is defined as being between +5V and +15V and is positive for a logic "0" (+5V to +15V) and negative for a logic "1" (−5V to −15V). These voltage levels are defined when driver is loaded ($3000\Omega < R_L < 7000\Omega$). The DS14C88 meets this voltage requirement by converting HC or TTL/LSTTL levels into RS-232C levels through one stage of inversion.

In applications where strict compliance to RS-232C voltage levels is not essential, a ±5V power supply to the driver may be used. The output voltage of the DS14C88 will be high enough to be recognized by either the 1489 or 14C89A receiver as valid data.

The RS-232C specification further states that, during transitions, the driver output slew rate must not exceed 30V/μs. The inherent slew rate of the equivalent bipolar circuit DS1488/MC1488 is much too fast and requires the connection of one external capacitor (330–400 pF) to each driver output in order to limit the slew rate to the specified value. However, the DS14C88 does not require any external components. The DS14C88 has a novel feature in that unique internal slew rate control circuitry has been incorporated which eliminates the need for external capacitors; to be precise, a saving of four capacitors per package. The 14C88 minimizes RFI and transition noise spikes by typically setting the slew rate at 5V–6V/μs. This will enable optimum noise performance, but will restrict data rates to below 40k baud.

The DS14C88 can also withstand an accidental short circuit from a conductor in the interconnecting cable to any one of four outputs in a package without sustaining damage to itself or its associated equipment.

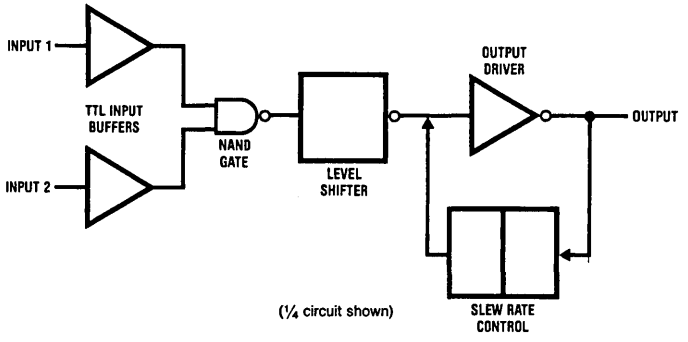

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FIGURE 2. DS14C88 Line Driver Block Diagram

THE RECEIVER

The DS14C89A quad CMOS line receiver is a pin replacement of the existing bipolar circuit DS1489/MC1489/DS1489A/MC1489A.

The DS14C89A is fabricated in CMOS technology giving it an inherent advantage over the bipolar DS1489/MC1489/DS1489A/MC1489A circuits in terms of power consumption. Under worst case static conditions a power consumption reduction of 97% (900 μA against 26 mA) is achieved.

The RS-232C specification states that the required receiver input impedance as being between 3000Ω and 7000Ω for input signals between 3.0V and 25.0V. Furthermore, the receiver open circuit bias voltage must not be greater than +2V.

The DS14C89A meets these requirements and is able to level shift voltages in the range of −30V to +30V to HC or TTL/LSTTL logic levels through one stage of inversion. A voltage of between −3.0V and −25.0V is detected as a logic "1" and a voltage of between +3.0V and +25.0V is detected as logic "0".

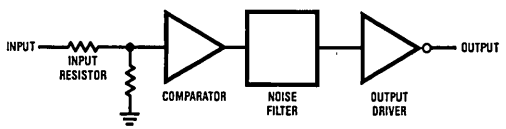
The RS-232C specification states that the receiver should interpret an open circuit or power off condition (source impedance of driver must be 300Ω or more to ground) as an OFF condition. In order to meet this requirement the input threshold of the DS14C89A is positive with respect to ground resulting in an open circuit or "power off" condition being interpreted as a logic "0" at the input.

Although the DS14C89A is pin replacement for the bipolar circuits DS1489/MC1489/DS1489A/MC1489A, its performance characteristics are modeled on the DS1489A/MC1489A.

The response control input on each of the bipolar circuits facilitates the rejection of noise signals by means of an external capacitor between each response control pin and ground.

When communicating between components of a data processing system in a hostile environment, spurious data such as ground shifts and noise signals may be introduced and it can become difficult to distinguish between a valid data signal and those signals introduced by the environment.

The DS14C89A eliminates the need for external response control capacitors and overcomes the effects of spurious data by means of unique internal noise filtering circuitry. *Figure 4* shows typical turn on threshold versus response control capacitance for existing bipolar devices. Note the curve for the DS14C89A CMOS device. The DS14C89A will not recognize any input signal whose pulse width is less than 1 μs, regardless of the voltage level of that input signal. Noise rejection in the bipolar parts depends on the voltage level of the noise transients. Therefore, in hostile environments the CMOS parts offer improved noise rejection properties. The DS14C89A has an internal comparator which provides input hysteresis for noise rejection. The DS14C89A has a typical turn-on voltage of 2.0V and a typical turn-off voltage of 1.0V resulting in 1.0V of hysteresis.



(¼ circuit shown) TL/F/8681–3

FIGURE 3. DS14C89A Line Receiver Block Diagram

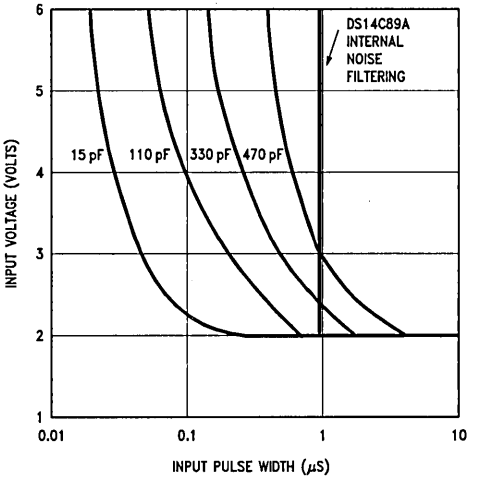


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FIGURE 4

TYPICAL APPLICATIONS

Obviously the major advantage of these CMOS devices is that with the large reduction of operating current, it is now possible to implement the "FULL" RS-232 interface in remote or portable equipment. Imagine that previously a designer, using a CMOS μP, RAM, ROM, and peripherals, could implement a complete system that consumes between 200 and 300 mW, but just adding the RS-232 interface (one driver, and one receiver) would add another 450 to 700 mW to the total system power consumption. This would severely shorten the battery life. The CMOS driver and receiver would only add about 40–50 mW.

In addition, the CMOS devices provide better noise rejection in harsh EMI environments, thus better data integrity. At the same time the internal slew rate limiting of the driver reduces the output transition time along the cable interface, hence reducing RFI emission, and easing the ability for portable (or non-portable) systems to meet FCC noise emission regulations. Also, since space is a premium in remote and portable systems, by integrating the function of the external capacitors on-chip (eliminating 8 capacitors), and designing these into S.O. packages, significant reduction in board space can be achieved.

For example, *Figure 5* shows a small CMOS system utilizing a CMOS NSC800 microprocessor, NSC858 CMOS UART, CMOS RAM/ROM, and a clock timer. This system runs off a 9V battery so a DC–DC converter is used to generate −9V for the RS-232 interface. In this design a standard DC–DC convert IC is used to generate a −9V supply from the single +9V battery.

As a second example, a "cheater" RS-232 interface is sometimes implemented. This interface is compatible with the current RS-232 driver/receiver products, but rather than using a ±(9–15)V supply, a ±5V supply is used. The drivers will not meet the RS-232 output voltage level specifications, but will correctly drive either the CMOS or bipolar receivers. The DC–DC converter circuit in *Figure 5* may be used to implement this. While for non-portable applications this can be done with the old bipolar 1488/89s, the DC–DC

converter is somewhat simpler with the CMOS parts due to the much reduced current consumption.

The RS-232 driver/receivers are also useful in non-power sensitive multi-user computers. Imagine a 16 terminal cluster controller for a multi-user computer system, *Figure 6*. This controller would require 16 drivers and 16 receivers with a total power of 8 watts when using the bipolar devices. The CMOS devices need only 400 mW.

Also proper noise rejection for receivers and slew rate limiting for the driver would require 128 capacitors for the bipolar parts, but they are unnecessary in the CMOS implementation.

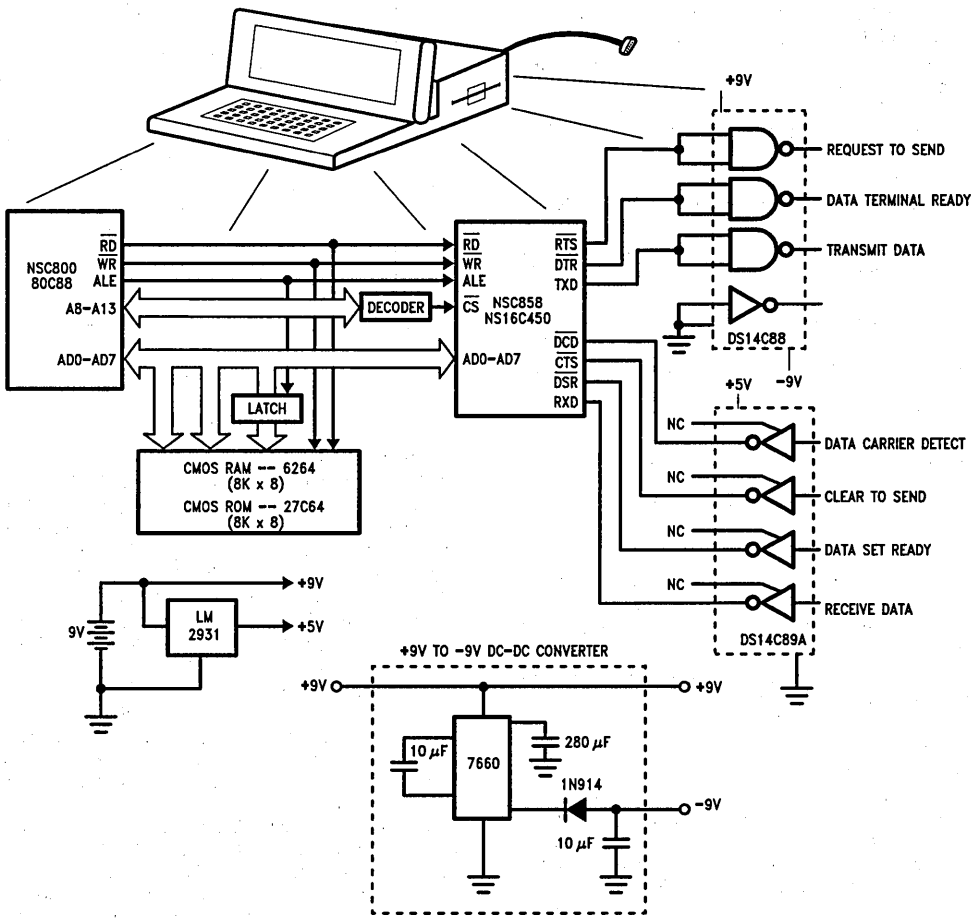

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FIGURE 5. Typical portable system application using CMOS μP, ROM, RAM, and UART. RS-232 interface is shown using 7660 supply inverter and CMOS Receiver/Driver.

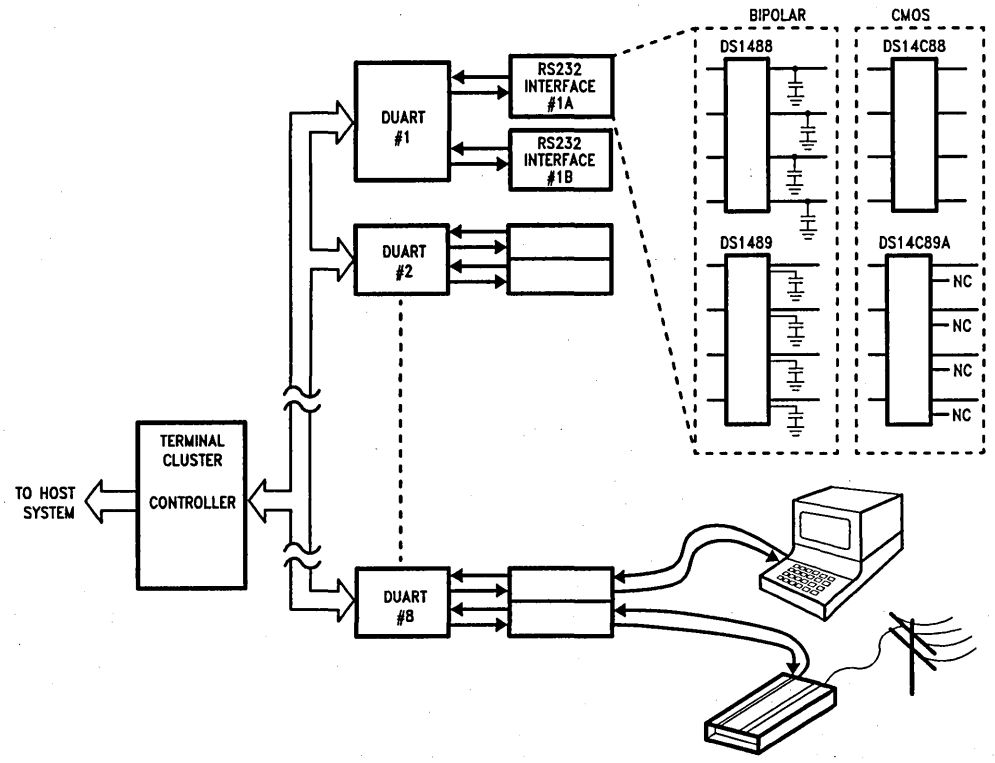

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FIGURE 6. A multi-terminal application showing a comparison of Bipolar vs CMOS solutions.

Automotive Multiplex Wiring

National Semiconductor
Application Note 454
Abdul H. Aleaf

INTRODUCTION

The evolutionary development of vehicle electronic systems has rapidly increased the number of individual wires in the vehicle. The conventional wiring harness will not provide solutions to the problems such as reducing size and weight in addition to meeting cost and reliability objectives. Several approaches have been taken to provide long term solutions. None has succeeded. Miniaturization of cables and wires is one example of a temporary solution.

Multiplexing on the other hand has been regarded as a technique which allows considerable savings to be made in the size and cost of the harness. It can also enhance reliability by reducing the number of electrical connections.

In a multiplex system the control functions will be distributed around the vehicle and complex interconnections between diagnostic terminals, sensors, instruments and switches will not add to the harness complexity. With all its advantages it has not been implemented on a production car yet. The reason has been economical feasibility and lack of suitable semiconductor components for power switching. But, with the rapid technology advances in power FETs and introduction of low cost microcomputers, multiplex wiring can be regarded as a logical successor to conventional wiring systems. Extended development efforts are necessary to introduce a reliable system at reasonable cost.

The Microcontroller Applications Group at National Semiconductor has taken a step towards this goal. A low end multiplex wiring system focusing on asynchronous serial communication in a multi node network has been developed. This paper describes the development of this system on an abstract model which forms the basis for analysis of communication protocol and various node functions.

SYSTEM CONFIGURATION

Figure 1 presents a general view of the system. The system is a centralized single master multiple slave-node scheme. All units are connected together by a balanced twisted pair. The expandable interconnection of different subsystems is achieved with 9600 Baud communication over a standard UART bus. The bus handles the interface between a master controller and the intelligent nodes.

The approach to have a centralized control system offers several advantages as compared against a non-centralized system. It prevents the problem of bus monopolization by a faulty node and is potentially cheaper due to the need for only one complex node (master). The master-slave architecture also prevents bus contention problems.

The master is a COP420L. The COP420L is a 4-bit microcontroller with a software UART that handles asynchronous communication with other processors at speeds up to 9600 Baud.

The use of 4-bit 49¢ microcontrollers (COP413L) at the nodes not only provides intelligence which reduces the required bus bandwidth, it also reduces the incremental cost associated with automotive multiplexing. All standard nodes are identical. One standard program is used. This uniformity contributes to the system flexibility and expandability. External standard nodes may be added to the system to control additional functions. Node types and addresses are selected via external wire jumpers or switches. The slave nodes consist of four remote units to handle functions such as headlamps, tail lamps, etc. These nodes are the front right, front left, rear right and rear left nodes. Incorporated into the system are also a keyboard node, a EIC node and a display node.

The keyboard node may call for a control action at any time. This node is being continuously monitored by the master controller which receives status and processes the command or information.

Overall system intelligence and flexibility is increased by dedicating a node to NS455 the Terminal Management Processor. This node takes the responsibility to display information on a 4" flat CRT display.

An Electronic Instrument Cluster (EIC) system is a completely independent system. It typically performs all functions associated with the automobile dashboard such as vehicle speed, odometers to accumulate mileage, gauges to display engine temperature, fuel level and so on. It also indicates error conditions such as high engine temperatures, low fuel level etc. The multiplex wiring system uses a standard slave node as a bridge between the two independent systems. The slave node monitors error conditions from the EIC system and passes them to the master node upon request. It becomes relatively simple to allow the master to access all activity in the EIC system via additional commands to the slave node serving the EIC system:

THE COMMUNICATION PROTOCOL

The master unit addresses the remote units sequentially and receives a status reply from each individual node. Data communication is via the standard UART format. It has a start bit, eight data bits, an even parity bit and one stop bit.

Information to be transmitted from the master to a slave node is organized as a frame. Each frame contains the address of destination and command or data. The information in a frame is transmitted as byte format. Address/data differentiation is done by means of a flag. The byte is an address byte if the MSB is set ("1"), otherwise it is a data byte.

Two different types of addressing schemes have been incorporated into the communication protocol; node addressing and class addressing. A class of nodes is formed by grouping together slave nodes with common functions. Commands may be executed either by specific individual nodes or by slave classes. All nodes of the same class execute the command simultaneously. The system implementation at National involved four classes with seven slave nodes per class. So, the total number of nodes possible in this system is 28.

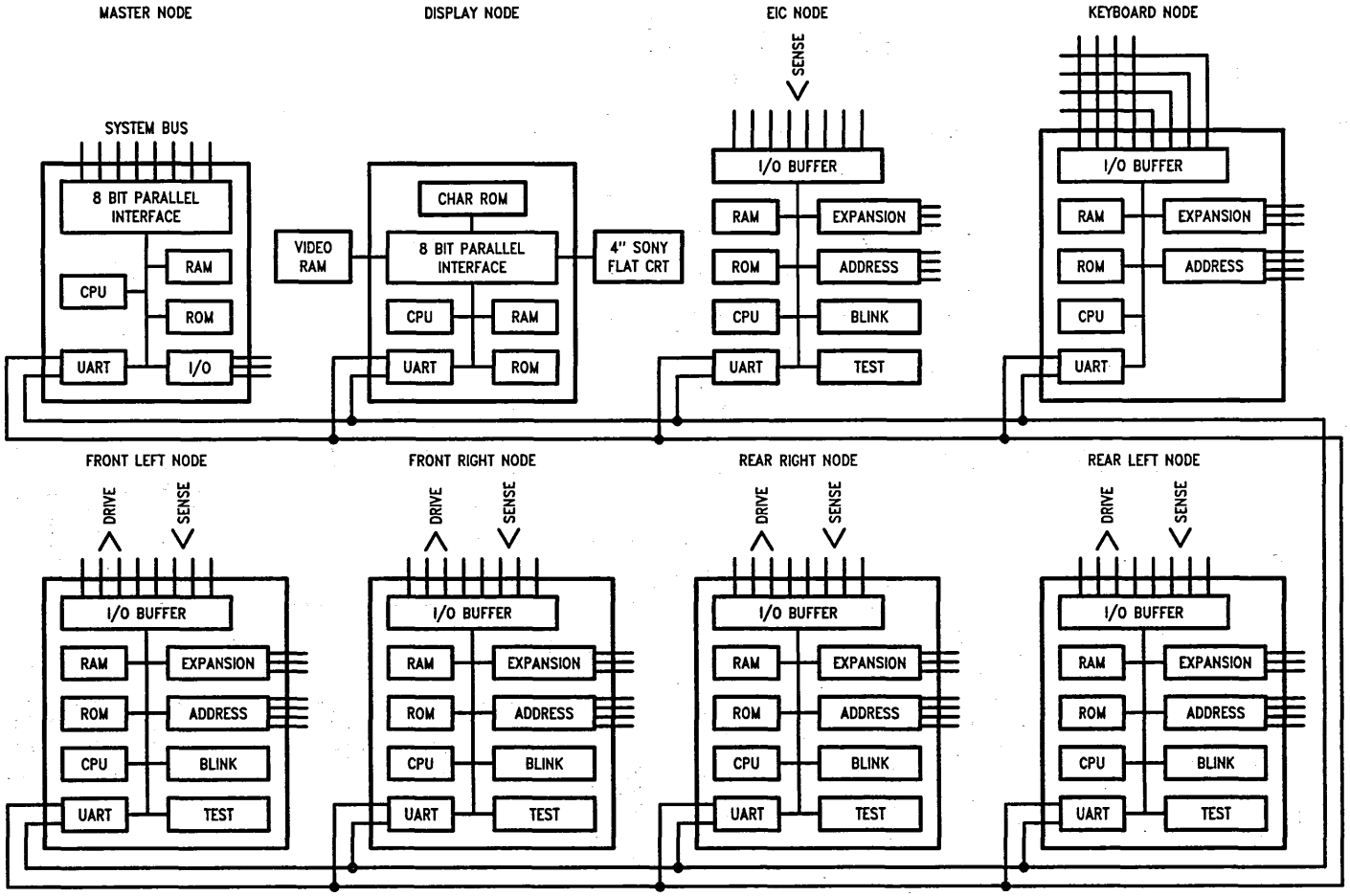

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FIGURE 1. Block Diagram

The partitioning between the class address and node address reduces the density of bus traffic significantly by eliminating repetative command transmission to individual node class. Lower bus traffic implies that lower transmission bit rate can be used, allowing additional noise immunity. Another advantage of the class addressing is the provision of synchronization for control signals such as HAZARD, LEFT/RIGHT turns.

Error correction is incorporated into the communication protocol. The UART error flags such as PARITY and FRAMING ERRORS protect the system at the physical layer. At the system level, the nodes simply avoid sending an acknowledgement to the master when an error is detected. The master times out and sends the command again.

THE MASTER NODE

The master controller is the heart of the system. Its responsibility is to generate the controlling commands and synchronize the system. It transmits to the remote units and listens to them to get the vehicle status and acts accordingly. Circuit complexity is reduced by implementing extensive software programming in the master controller. This means that the burden is essentially on the master and must be engineered to very high standards of reliability. The device used in the implementation as the master is the COP1430. It is a cost effective 4-bit single chip microcontroller. It features on chip UART which handles asynchronous communications at speeds up to 9600 Baud.

THE SLAVE NODES

The standard slave nodes are based upon the COP413L. The COP413L is a low cost 4-bit microcontroller which may be customized in production. A system such as multiplex wiring requires power consumption to be absolutely minimal. Another basic requirement is that the system should be cost effective. These two facts directed us to use the COP413L at the standard slave node. The COP413L is a low cost (49¢!) low power microcontroller from NSC drawing less than 7 mA at 4.5V to 5.5V. The device contains an 8-bit bidirectional I/O port and a serial expansion port. The CMOS version of COP413L will also be available.

THE DISPLAY NODE

This node can serve as a condition monitoring unit for the vehicle. A considerable quantity of diagnostic information collected from transducers, switches, sensors and various loads are fed to this unit to be displayed on a CRT display. The node is based on a Terminal Management Processor the NS455. The NS455 is a CRT controller on chip. The messages are updated over the serial I/O line by the master controller. The communication format is:

a) The node receives the address.

b) If address matches the local node address, send the copy command

c) Receive new address and execute.

OUTPUT STAGES

The power FETs used for local switching throughout the system are IRF541[4]. These N-channel FETs provide much better drive circuit specification as compared to bipolar output stages. They also feature all of the well established advantages of MOSFET such as voltage control, very fast switching, and very low on state resistance. Another advantage is the lower cost as compared to comparibly rated p-channel devices.

TRANSMISSION MEDIUM

A balanced twisted pair is used for bus medium which provides high noise immunity. The transceiver selected for the bus is DS3695 *(Figure 2)*. This device is a high speed differential TRI-STATE® Bus/line transceiver designed to meet EIA standard for multipoint bus transmission. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a standard thermal shutdown circuit, which forces the driver outputs into the high impedance state.

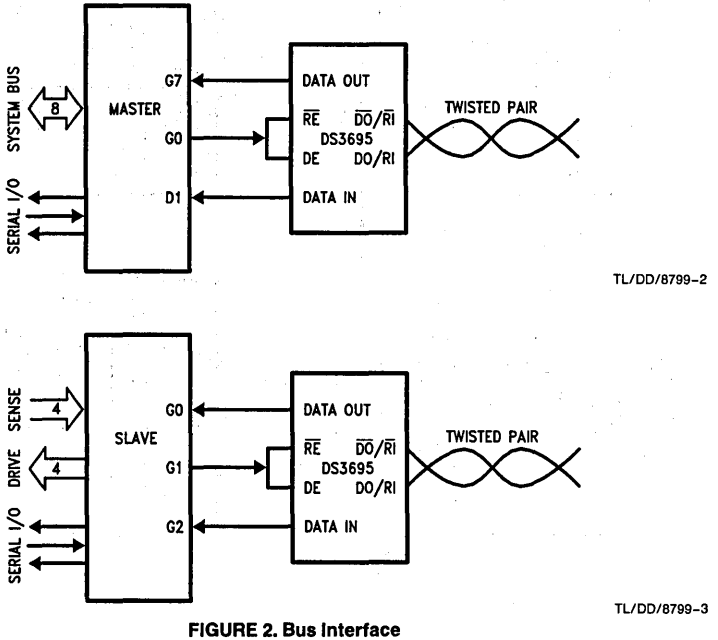

FIGURE 2. Bus Interface

CONCLUSIONS

Multiplex wiring system potentially seems to be a good replacement for conventional wiring system. Reduced complexity, increased flexibility and diagnostic capability could be achieved by incorporating microcontroller devices at nodes within the wiring system. The 4-bit microcontrollers selected are available in a price range, as low as 49¢, that will allow multiplex wiring to compare favorably on a cost-performance basis with the conventional harness.

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High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Problems

National Semiconductor
Application Note 457
Toan Tran
Larry Kendall

In system design, due to the distributed intelligence ability of the microprocessor, it is a common practice to have the peripheral circuits physically separated from the host processor with data communications being handled over cables. Usually, these cables are measured in hundreds or thousands of feet. Signals transmitted on these lines (or cables) are exposed to electrical noise sources which may require large noise immunity. The requirements for transmission lines and noise immunity are covered in E.I.A. standard RS-422.

The object of this application note is to describe the design requirement of RS-422 standard and to show that National's DS8921, DS8922 and DS8923 Differential Driver and Receiver pair meet all of those requirements. Special circuit design techniques are used to achieve small skew on complementary signals of the driver outputs. In fact, these devices are designed specifically for applications which must meet stringent timing constraints including the ESDI Disk Drive standard. Additionally, the DS8921 series meet the requirement of ST506 and ST412HP standards.

BALANCED VOLTAGE DIGITAL INTERFACE CIRCUITS (RS-422) REQUIREMENT

Balanced circuits are normally used in data, timing, or control applications where the data signaling rate approaches speeds of 10 Mbit/s. In addition, balanced data transmission techniques should be used whenever the following conditions exist:

1. The interconnecting cable is too long for effective unbalanced operation.
2. The interconnecting cable is exposed to a noise source which may cause a voltage sufficient to indicate a change of binary state at the load.
3. It is necessary to minimize interference with other signals.

Figure 1 below is a balanced circuit connection.

There are three major controlling factors in balanced voltage digital interface:

1. The cable length
2. The modulation rate
3. The characteristics of the Driver and Receiver

CABLE LENGTH

There is no maximum cable length specified in the RS-422 standard. Guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 2* below is the guideline provided by RS-422 for data modulation rate versus cable length.

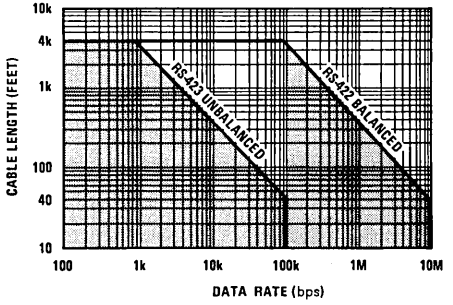

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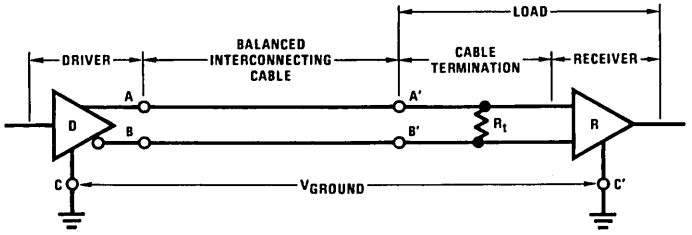
FIGURE 2. Data Modulation Rate vs Cable Length

The curve is based on empirical data using a 24 AWG, copper conductor, twisted pair cable terminated for worst case in a 100Ω load, with rise and fall time equal or less than one half unit interval at the applied modulation rate.

Even though the maximum cable length between driver and load is a function of data signaling rate, it is also influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and ground potential difference introduced between the generator and load circuit grounds.



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Legend:

R_t = Optional cable transmission resistance/receiver input impedance.

V_{GROUND} = Ground potential difference

A, B = Driver interface

A', B' = Load Interface

C = Driver circuit ground

C' = Load circuit ground

FIGURE 1. RS-422 Balanced Digital Interface Circuit

MODULATION RATE

The balanced (or differential) voltage mode interface will normally be utilized on data, timing or control circuits operating at up to 10 Mbps. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates. The DS8921 family of devices meets or exceeds all of the recommended RS-422 performance specifications.

RS-422 CHARACTERISTICS

A. The Driver

The balanced driver characteristics are specified in RS-422 as follows:

1. A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage to the interconnecting cable in the range of 2V to 6V.
2. With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the two output terminals shall be equal to or greater than 2V, or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT is reversed ($\overline{VT}$).
3. During transitions of the driver output between alternating binary states, the differential voltage measured across 100Ω load shall monotonically change between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter, the signal voltage shall not change more than 10% of V_{SS} from the steady state value until the binary state occurs.

B. The Receiver

The electrical characteristics of the receiver are specified in RS-422 as follows:

1. The receiver shall not require a differential input voltage more than 200 mV to correctly assume the intended binary state, over an entire common-mode voltage range of −7 to +7V. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2. The receiver shall maintain correct operation for a differential input signal ranging between 200 mV and 6V in magnitude.
3. The maximum voltage between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal +7V common-mode) in magnitude. Also, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4. The total load (up to 10 receivers) shall not have a resistance more than 90Ω at its input points.

DS8921, DS8922 AND DS8923

The DS8921 is a single differential line driver and receiver pair. Whereas, the DS8922 and DS8923 are dual differential line driver and receiver pairs. The difference between the DS8922 and DS8923 is in the TRI-STATE® control *(Figure 3)*.

These devices are designed to meet the full specifications of RS-422. The driver features high source and sink current capability.

The receiver will discriminate a ±200 mV input signal over a full common-mode range of ±7V. Switching noise which may occur on input signal can be eliminated by the built-in hysteresis (50 mV typical, and 15 mV min.). An input fail-safe circuit is provided so that if the receiver inputs are open, the output will assume the logical one state.

These devices have power up/down circuitry that will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or down operation.

The most attractive feature of these devices is the small skew beween the complementary outputs of the driver, typically about 0.5 ns. This small skew specification is often necessary to meet tight system timing requirements.

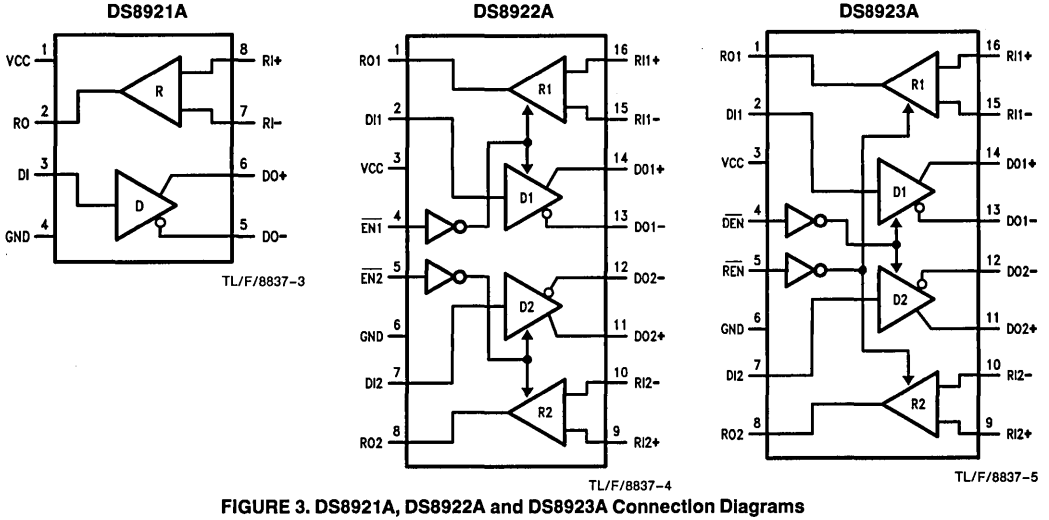
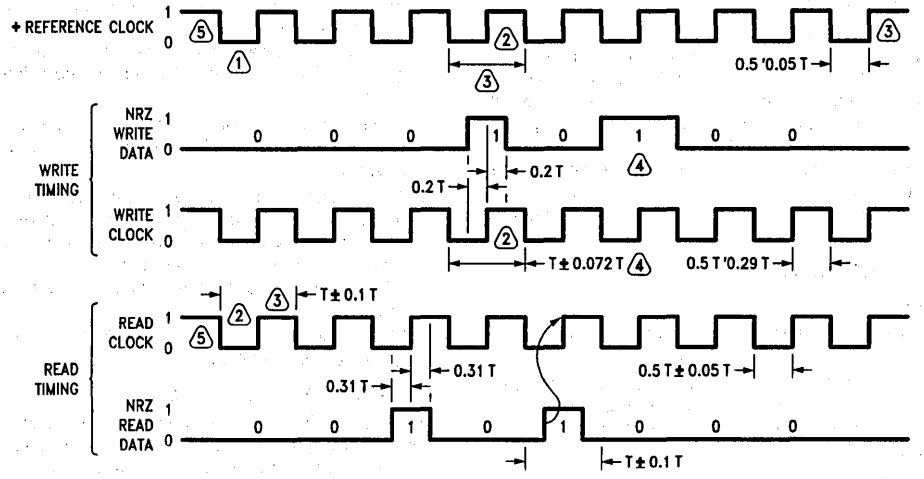


FIGURE 3. DS8921A, DS8922A and DS8923A Connection Diagrams



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Note 1. All times in ns measured at I/O connector of the drive. T is the period of the clock signals and is the inverse of the reference or read clock frequency.

Note 2. Similar period symmetry shall be in ±4 ns between any two adjacent cycles during reading and writing.

Note 3. Except during a head change or PLO synchronization the clock variances for spindle speed and circuit tolerances shall not vary more than −5.5% to +5.0%. Phase relationship between reference clock and NRZ write data or write clock is not defined.

Note 4. The write clock must be the same frequency as the drive supplied reference clock (i.e., the write clock is the controller received and retransmitted drive reference clock).

Note 5. Reference clock is valid when read gate is inactive. Read clock is valid when read gate is active and PLO synchronization has been established.

FIGURE 4. ESDI Timing Diagrams

DM74AS74 Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Parameter	From	To	Conditions	DM74AS74			Units
				Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	105			MHz
T_{PLH}	Preset or clear	Q or Q		3.3		7.5	ns
T_{PHL}				3.5		10.5	ns
T_{PLH}	Clock	Q or Q		3.5		8	ns
T_{PHL}				4.5		9	ns

Note 1: See Section 1 for test waveforms and output load.

FIGURE 5. 1 ns Clock Skew

ESDI ENHANCED SMALL DEVICE INTERFACE

The ESDI specification requires that the read and Reference Clock must meet the symmetry shown in *Figure 4*. This necessitates the use of National's DS8921A/22A/23A series of transceivers.

All specifications are in % T, where $T = \frac{1}{F}$, the ESDI specification is assumed to be a 10 Mbits/second standard, T = 100 ns.

Given this, the negative pulse width measured at the drive connector must equal 0.5T ±0.05T (50 ns ±5 ns). The best available RS-422 driver, other than the DS8921A Family, is specified at ±4 ns differential skew. If the clock is from a high speed 74AS74 device, shown in *Figure 5*, it will have a typical skew of 1 ns.

This combination of 4 ns +1 ns uses all of the ESDI specified 5 ns and leaves no margin for noise. Use of the DS8921A, 22A, or 23A, specified at ±2.75 ns max. differential skew would allow up to ±2.25 ns for clock skew and noise. This is as close a guarantee to meeting the ±5 ns spec. of ESDI, as is possible with todays advanced testing systems.

One other consideration is the relationship between Read Clock and Read Data. *Figure 4* shows that the positive edge of Read Clock must be 0.31T (31 ns) after the leading edge of Read Data, and 0.31T (31 ns) before the trailing edge of Read Data.

The Read Clock positive edges will be used to strobe Read Data into the controller after both signals go through their respective cable lines and receivers. Use of the DS8922A/23A assures minimum skew between these two signals. Because both drivers, or both receivers, are on the same piece of silicon an optimum match is achieved.

The above is applicable to an ESDI controller as well as the Drive itself. The controller receives the Reference Clock and uses both positive and negative edges to generate WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe out WRITE DATA and the positive edge will strobe WRITE DATA into the Drive.

The WRITE CLOCK positive edge has to be centered within WRITE DATA after it is received by the Drive. The transmitted WRITE CLOCK and WRITE DATA must be as closely matched as possible.

National's DS8921A, 22A, and DS8923A devices offer the combination of tightly spec'd parameters and drivers and receivers on one chip to meet various system timing constraints.

EMI/RFI Board Design

National Semiconductor
Application Note 643
Joe Cocovich

INTRODUCTION

The control and minimization of Electro-Magnetic Interference (EMI) is a technology that is, out of necessity, growing rapidly. EMI will be defined shortly but, for now, you might be more familiar with the terms Radio Noise, Electrical Noise, or Radio Frequency Interference (RFI). The technology's explorations include a wide frequency spectrum, from dc to 40 GHz. It also deals with susceptibility to EMI as well as the emissions of EMI by equipment or components. Emission corresponds to that potential EMI which comes out of a piece of equipment or component. Susceptibility, on the other hand, is that which couples from the outside to the inside.

In HPC designs to date, we have looked at noise situations ranging from 2 MHz to 102 MHz. EMI, in some cases, can affect radio reception, TV reception, accuracy of navigation equipment, etc. In severe cases, EMI might even affect medical equipment, radar equipment, and automotive systems.

This Application Note will define ElectroMagnetic Interference and describe how it relates to the performance of a system. We will look at examples of Inter-system noise and Intra-system noise and present techniques that can be used to ensure ElectroMagnetic Compatibility throughout a system and between systems.

We will investigate and study the sources of noise between systems through wire-harness and backplane cables and connectors. Active circuit components can be contributors of noise and be susceptible to it. The fast switching times of CMOS devices fabricated in today's technology can cause incredible noise in a system. This noise typically is made up of crosstalk, power supply spiking, transient noise, and ground bounce.

The minimization and suppression of EMI can be obtained by utilizing proper control techniques. Intra-system noise, noise within a single module, sometimes can be controlled with methods such as filtering, shielding, careful selection of components, and following good wiring and grounding procedures. Controlling noise between systems, Inter-system noise, uses subtler techniques such as frequency management and time management, etc.

Appropriate time and resources should be spent during the design of a system or systems to insure that no problems will be encountered due to effects of EMI. Design guidelines will be presented that can be used to increase ElectroMagnetic Compatibility between systems by reducing the effects of noise between them. Above all, don't forget that the development tools used are also systems and are important to consider in your planning.

A brief look will be taken at the environment and tools required for different levels of noise testing. Relative risk-costs between preparing for EMC or excluding EMI concerns from the project will be listed.

DESCRIPTION OF NOISE

ElectroMagnetic Interference

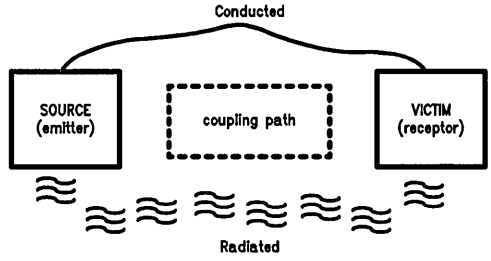
EMI is a form of electrical-noise pollution. Think of the time when an electric drill or some other power tool jammed a nearby radio with buzzing or crackling noises. Sometimes it got so bad that it prevented you from listening to the radio while the tool was in use. Or the ignition of an automobile idling outside your house caused interference to your TV picture making lines across the screen or even losing sync altogether making the picture flip. These examples are quite annoying but not catastrophic.

More serious, how about a sudden loss in telephone communication caused by electrical interference or noise while you are negotiating an important business deal? Now EMI can be economically damaging.

The results of EMI incidences can be even farther reaching than these examples. Aircraft navigation errors resulting from EMI or interruption of air traffic controller service and maybe even computer memory loss due to noise could cause two aircraft to collide resulting in the loss of lives and property.

These were just a few examples to help you identify the results of EMI in a familiar context. To help understand an ElectroMagnetic Interference situation, the problem can be divided into three categories. They are the source, the victim, and the coupling path. Secondary categories involve the coupling path itself. It the source and victim are separated by space with no hard wire connection, then the coupling path is a radiated path and we are dealing with radiated noise. If the source and victim are connected together through wires, cables, or connectors, then the coupling path is a conducted path and we are dealing with conducted noise. Incidentally, both types of noise can exist at the same time.

ElectroMagnetic Interference Situation



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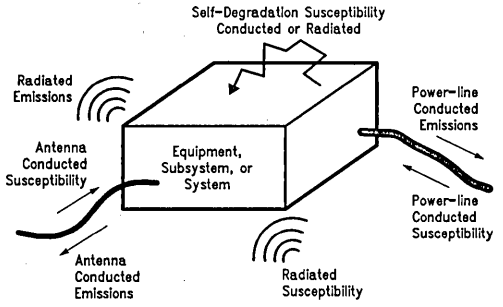
ElectroMagnetic Compatibility

If you think about the examples given, one can understand that EMI or electrical noise is of national concern. The Government and certain industry bodies have issued specifications with which all electrical, electromechanical, and electronic equipment must comply. These specifications and limitations are an attempt to ensure that proper EMC techniques are followed by manufactures during the design and fabrication of their products. When these techniques are properly applied, the product can then operate and perform with other equipment in a common environment such that no degradation of performance exists due to internally or externally conducted or radiated electromagnetic emissions. This is defined as ElectroMagnetic Compatibility or EMC.

Inter-System EMI

For the purpose of this Application Note, when the source of noise is a module, board, or system and the victim is a different and separate module, board, or system under the control of a different user, that is considered to be an inter-system interference situation. Examples of inter-system interference situations could be a Personal Computer interfereing with the operation of a TV or an anti-lock brake module in a car causing interference in the radio. This type of interference is more difficult to contain because, as mentioned earlier, the systems are generally not under the control of a single user. However, design methods and control techniques used to contain the intra-system form of EMI, which are almost always under the control of a single user, will inherently help reduce the inter-system noise.

Intra-System EMI Manifestations



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This Application Note will address problems and solutions in the area of intra-system noise. Intra-system interference situations are when the sources, victims, and coupling paths are entirely within one system or module or PC board. Systems may provide emissions that are conducted out power lines or be susceptible to emissions conducted in through them. Systems may radiate emissions through space as well as be susceptible to radiated noise. Noise conducted out antenna leads turns into radiated noise. By the same token, radiated noise picked up by the antenna is turned into conducted noise within the system. A perfect example is ground loops on a printed circuit board. These loops make excellent antennas. The system itself is capable of degrading performance due to its own internal generation of conducted and radiated noise and its susceptibility to it.

Some results of EMI within a system: Noise on power line causing false triggering of logic circuits, rapidly changing signals causing "glitches" on adjacent steady state signal lines (crosstalk) causing erratic operation, mutiple simultaneously switching logic outputs propagating ground bounce noise throughout system, etc.

Coupling Paths

The modes of coupling an emitter source to a receptor victim can become very complicated. Remember, each EMI situation can be classified into two categories of coupling, conducted and radiated. Coupling can also result from a combination of paths. Noise can be conducted from an emitter to a point of radiation at the source antenna, then picked up at the receptor antenna by induction, and re-conducted to the victim. A further complication that multiple coupling paths presents is that it makes it difficult to determine if eliminating a suspected path has actually done any good. If two or more paths contribute equally to the problem, eliminating only one path may provide little apparent improvement.

Conducted Interference

In order to discuss the various ways in which EMI can couple from one system to another, it is necessary to define a few terms. When dealing with conducted interference, there are two varieties that we are concerned with. The first variety is differential-mode interference. That is an interference signal that appears between the input terminals of a circuit. The other variety of conducted interference is called common-mode interference. A common-mode interference signal appears between each input terminal and a third point; that third point is called the common-mode reference. That reference may be the equipment chassis, an earth ground, or some other point.

Let's look at each type of interference individually. In *Figure 1* we show a simple circuit consisting of a signal source, V_S, and a load, R_L. In *Figure 2* we show what happens when differential-mode interference is introduced into the circuit by an outside source. As is shown, an interference voltage, V_D, appears between the two input terminals, and an interference current, I_D, flows in the circuit. The result is noise at the load. If, for instance, the load is a logic gate in a computer, and the amplitude of V_D is sufficiently high, it is possible for the gate to incorrectly change states.

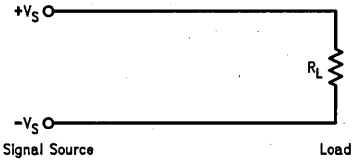

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FIGURE 1

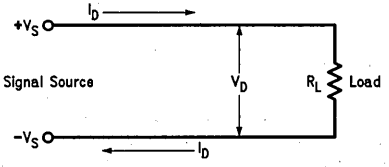

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FIGURE 2. Differential-Mode Interference

Figure 3 shows what happens when a ground loop is added to our circuit. Ground loops, which are undesirable current paths through a grounded body (such as a chassis), are usually caused by poor design or by the failure of some component. In the presence of an interference source, common-mode currents, I_C, and a common-mode voltage, V_C, can develop, with the ground loop acting as the common-mode reference. The common-mode current flows on both input lines, and has the same instantaneous polarity and direction (the current and voltage are in phase), and returns through the common-mode reference. The common-mode voltage between each input and the common-mode reference is identical.

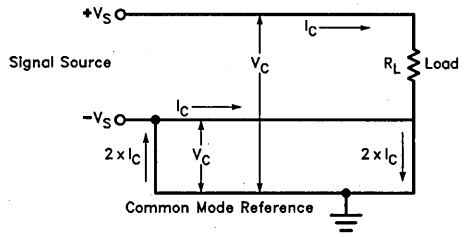

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FIGURE 3. Common-Mode Interference

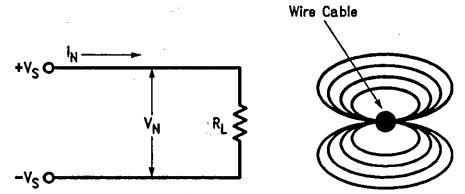

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FIGURE 4. Field-to-Cable Coupling

Radiated Interference

Radiated coupling itself can take place in one of several ways. Some of those include field-to-cable coupling, cable-to-cable coupling, and common-mode impedance coupling. Let's look at those types of coupling one at a time.

The principle behind field-to-cable coupling is the same as that behind the receiving antenna. That is, when a conductor is placed in a time-varying electromagnetic field, a current is induced in that conductor. That is shown in *Figure 4*. In this figure, we see a signal source, V_S, driving a load, R_L. Nearby there is a current carrying wire (or other conductor). Surrounding the wire is an electromagnetic field induced by the current flowing in the wire. The circuit acts like a loop antenna in the presence of this field. As such, an interference current, I_N, and an interference voltage, V_N, are induced in the circuit. The magnitude of the induced interference signal is roughly proportional to the frequency of the incoming field, the size of the loop, and the total impedance of the loop.

Cable-to-cable coupling occurs when two wires or cables are run close to one another. *Figure 5* shows how cable-to-cable coupling works. *Figure 5a* shows two lengths of cable (or other conductors) that are running side-by-side. Because any two conducting bodies have capacitance between them, called stray capacitance, a time-varying signal in one wire can couple via that capacitance into the other wire. That is referred to as capacitive coupling. This stray capacitance, as shown in *Figure 5c* makes the two cables behave as if there were a coupling capacitor between them. Another mechanism of cable-to-cable coupling is mutual inductance. Any wire carrying a time-varying current will develop a magnetic field around it. If a second conductor is placed near enough to that wire, that magnetic field will induce a similar current in the second conductor. That type of coupling is called inductive coupling. Mutual inductance, as shown in *Figure 5b*, makes the cables behave as if a poorly wound transformer were connected between them. In cable-to-cable coupling, either or both of those mechanisms may be responsible for the existance of an interference condition. Though there is no physical connection between the two cables, the properties we have just described make it possible for the signal on one cable to be coupled to the other.

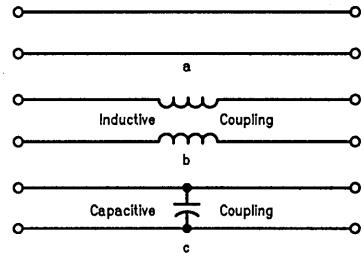

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FIGURE 5. Cable-to-Cable Coupling

Either or both of the above-mentioned properties cause the cables to be electromagnetically coupled such that a time-varying signal present on one will cause a portion of that signal to appear on the other. The "efficiency" of the coupling increases with frequency and inversely with the distance between the two cables. One example of cable-to-cable coupling is telephone "crosstalk", in which several phone conversations can be overheard at once. The term crosstalk is now commonly used to describe all types of cable-to-cable coupling.

Common-mode impedance coupling occurs when two circuits share a common bus or wire. In *Figure 6* we show a circuit that is susceptible to that type of coupling. In that figure a TL092 op-amp and a 555 timer share a common return or ground. Since any conductor (including a printed circuit board trace) is not ideal, that ground will have a non-zero impedance, Z. Because of that, the current, I, from pin 1 of the 555 will cause a noise voltage, V_N, to develop; that voltage is equal to $I \times Z$. That noise voltage will appear in series with the input to the op-amp. If that voltage is of sufficient amplitude, a noise condition will result.

While not all inclusive, these coupling paths account for, perhaps, 98% of all intra-system EMI situations.

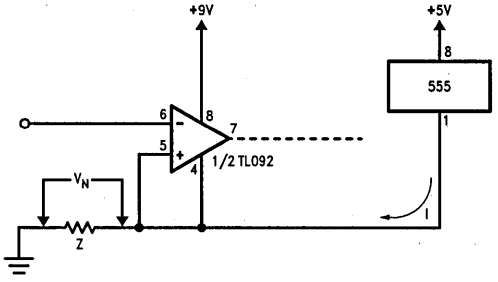

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FIGURE 6. Common-Mode Impedance Coupling

NOISE SOURCES

In this Application Note, we will look at sources of EMI which involve components that may conduct or radiate electromagnetic energy. These sources, component emitters, are different from the equipment and subsystems we have

been talking about. Component emitters are sources of EMI which emanate from a single element rather than a combination of components such as was previously described. Actually, these component emitters require energy and connecting wires from other sources to function. Therefore, they are not true sources of EMI, but are EMI Transducers. They convert electrical energy to electrical noise.

Cables and Connectors

The three main concerns regarding the EMI role of cables are conceptualized in *Figure 7.* They act as (1) radiated emission antennas, (2) radiated susceptibility antennas, and (3) cable-to-cable or crosstalk couplers. Usually, whatever is done to harden a cable against radiated emission will also work in reverse for controlling EMI radiated susceptibility. The reason for the word usually, is that when differential-mode radiated emission or susceptibility is the failure mode, twisting leads and shielding cables reduces EMI. If the failure mechanism is due to common-mode currents circulating in the cable, twisting leads has essentially no effect on the relationship between each conductor and the common-mode reference. Also cable shields may help or aggravate EMI depending upon the value of the transfer impedance of the cable shield. Transfer impedance is a figure of merit of the quality of cable shield performance defined as the ratio of coupled voltage to surface current in ohms/meter. A good cable shield will have a low transfer impedance. The effectiveness of the shield also depends on whether or not the shield is terminated and, if so, how it is terminated.

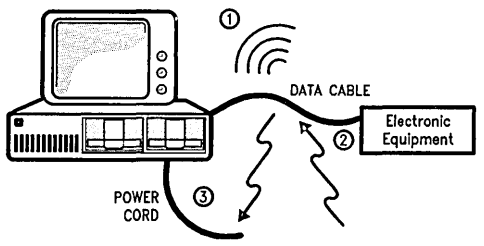

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FIGURE 7. Cables and Connectors

Connectors usually are needed to terminate cables. When no cable shields or connector filters or absorbers are used, connectors play essentially no role in controlling EMI. The influence of connector types, however, can play a major role in the control of EMI above a few MHz. This applies especially when connectors must terminate a cable shield and/or contain lossy ferrites or filter-pins.

Connectors and cables should be viewed as a system to cost-effectively control EMI rather than to consider the role of each separately, even though each offers specific interference control opportunities.

Components

Under conditions of forward bias, a semiconductor stores a certain amount of charge in the depletion region. If the diode is then reverse-biased, it conducts heavily in the reverse direction until all of the stored charge has been removed as shown in *Figure 8.* The duration, amplitude, and configuration of the recovery-time pulse (also called switching time or period) is a function of the diode characteristics and circuit parameters. These current spikes generate a broad spectrum of conducted transient emissions. Diodes with mechanical imperfections may generate noise when physically agitated. Such diodes may not cause trouble if used in a vibration-free environment.

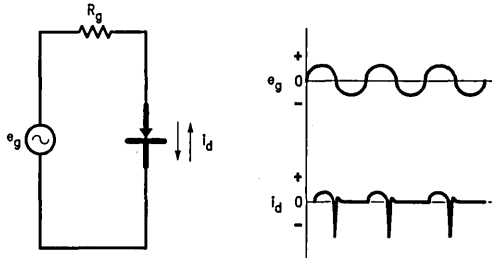

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FIGURE 8. Diode Recovery Periods and Spikes

Power Supply Noise

Power-supply spiking is perhaps the most important contributor to system noise. When any element switches logic states, it generates a current spike that produces a voltage transient. It these transients become too large, they can cause logic errors because the supply voltage drop upsets internal logic, or because a supply spike on one circuit's output feeds an extraneous noise voltage into the next device's input.

With CMOS logic in its quiescent state, essentially no current flows between V_{CC} and ground. But when an internal gate or an output buffer switches state, a momentary current flows from V_{CC} to ground. The switching transient caused by an unloaded output changing state typically equals 20 mA peak. Using the circuit shown in *Figure 9,* you can measure and display these switching transients under different load conditions.

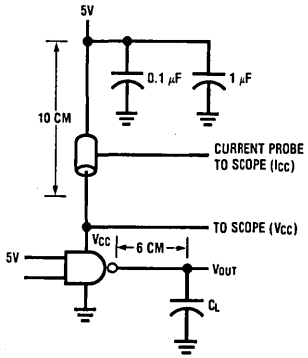

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FIGURE 9

Figure 10a shows the current and voltage spikes resulting from switching a single unloaded (C_L = 0 in *Figure 9*) NAND gate. These current spikes, seen at the switching edges of the signal on V_{IN}, increase when the output is loaded. *Figures 10b, 10c,* and *10d* show the switching transients when the load capacitance, C_L, is 15 pF, 50 pF, and 100 pF, respectively. The large amount of ringing results from the test circuit's transmission line effects. This ringing occurs partly because the CMOS gate switches from a very high impedance to a very low one and back again. Even for medium-size loads, load capacitance current becomes a major current contributor.

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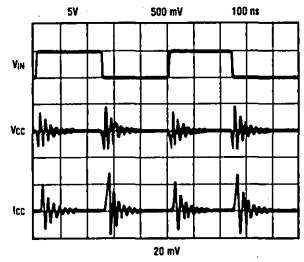

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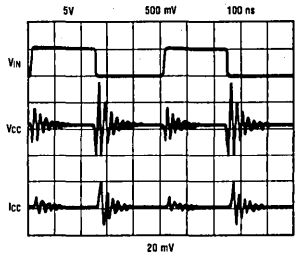

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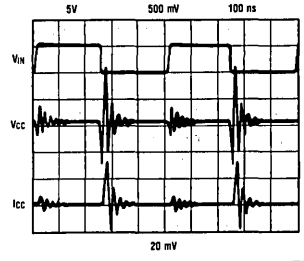
b



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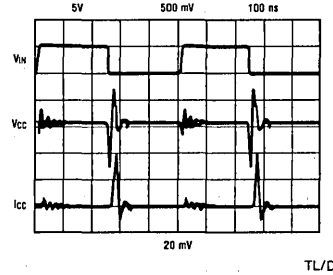

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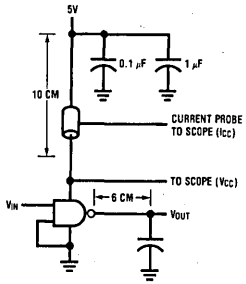
d

FIGURE 10

Although internal logic generates current spikes when switching, the bulk of a spike's current comes from output circuit transitions. *Figure 11* shows the I_{CC} current for a NAND gate, as shown in the test circuit, with one input switching and the other at ground resulting in no output transitions. Note the very small power-supply glitches provoked by the input-circuit transitions.



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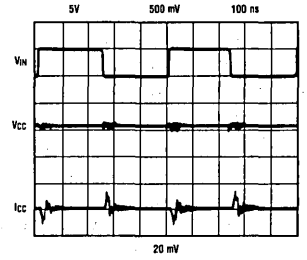

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FIGURE 11

High-Speed CMOS Logic Switching

The magnitude of noise which can be tolerated in a system relates directly to the worst case noise immunity specified for the logic family. Noise immunity can be described as a device's ability to prevent noise on its input from being transferred to its output. It is the difference between the worst case output levels (V_{OH} and V_{OL}) of the driving circuit and the worst case input voltage requirements (V_{IH} and V_{IL}, respectively) of the receiving circuit.

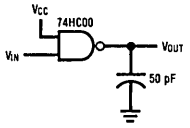
Using *Figure 12* as a guide, it can be seen that for TTL (LS or ALS) devices the worst case noise immunity is typically 700 mV for the high logic level and 300 mV for the low logic level. For HCMOS devices the worst case noise immunity is typically 1.75V for high logic levels and 800 mV for low logic levels. AC high speed CMOS logic families have noise immunity of 1.75V for high logic levels and 1.25V for low logic levels. ACT CMOS logic families have noise immunity of 2.9V for high logic levels and 700 mV for low logic levels.

Logic Family Comparisons

Characteristic	Symbol	LS/ALS TTL	HCMOS	AC	ACT
Input Voltage (Limits)	V_{IH} (Min)	2.0V	3.15V	3.15V	2.0V
	V_{IL} (Max)	0.8V	0.9V	1.35V	0.8V
Output Voltage (Limits)	V_{OH} (Min)	2.7V	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$
	V_{OL} (Max)	0.5V	0.1V	0.1V	0.1V

FIGURE 12

To illustrate noise margin and immunity, *Figure 13* shows the output that results when you apply several types of simulated noise to a 74HC00's input. Typically, even 2V or more input noise produces little change in the output. The top trace shows noise induced on the high logic level signal and the bottom trace shows noise induced on the low logic level signal.



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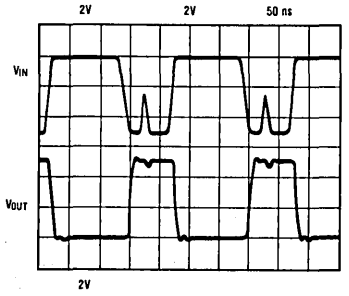

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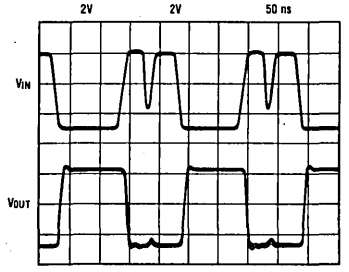

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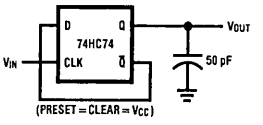
FIGURE 13

Figure 14 shows how noise affects a 74HC74's clock input. Again, no logic errors occur with 2V or more of noise on the clock input.

When using high speed CMOS, even with its greater noise immunity, crosstalk, induced supply noise and noise transients become factors. Higher speeds allow the device to respond more quickly to externally induced noise transients and accentuate the parasitic interconnection inductances and capacitances that increase self-induced noise and crosstalk.



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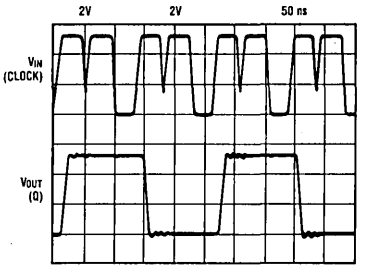

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FIGURE 14

Signal Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Our discussion on cable-to-cable coupling described crosstalk as appearing due to the distributed capacitive coupling and the distributed inductive coupling between two signal lines. When crosstalk is measured on an undriven sense line next to a driven line (both terminated at their characteristic impedances), the near end crosstalk and the far end crosstalk have quite distinct features, as shown in *Figure 15*. It should be noted that the near end component reduces to zero at the far end and vice versa. At any point in between, the crosstalk is a fractional sum of the near and far end crosstalk waveforms as shown in the figure. It also can be noted that the far end crosstalk can have either polarity whereas the near end crosstalk always has the same polarity as the signal causing it.

The amplitude of the noise generated on the undriven sense line is directly related to the edge rates of the signal on the driven line. The amplitude is also directly related to

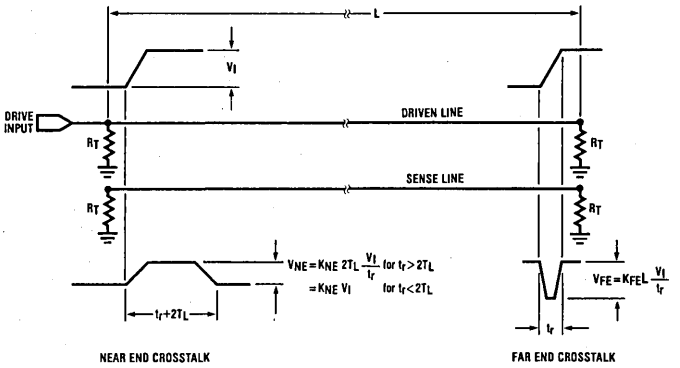

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FIGURE 15. Crosstalk

the proximity of the two lines. This is factored into the coupling constants K_{NE} and K_{FE} by terms that include the distributed capacitance per unit length, the distributed inductance per unit length, and the length of the line. The lead-to-lead capacitance and mutual inductance thus created causes "noise" voltages to appear when adjacent signal paths switch.

Several useful observations that apply to a general case can then be made:

- The crosstalk always scales with the signal amplitude V_I.
- Absolute crosstalk amplitude is proportional to slew rate V_I/t_r, not just $1/t_r$.
- Far end crosstalk width is always t_r.
- For $t_r < 2\ T_L$, where t_r is the transition time of the signal on the driven line and T_L is the propagation or bus delay down the line, the near end crosstalk amplitude V_{NE} expressed as a fraction of signal amplitude V_I is K_{NE} which is a function of physical layout only.
- The higher the value of 't_r' (slower transition times) the lower the percentage of crosstalk (relative to signal amplitude).

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than about three times the propagation delay of the line. Significant transmission line properties may be exhibited, for example, where devices having edge rates of 3 ns are used to drive traces of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Signal Interconnects

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{oe}, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{oe} and t_{pde} can be calculated with:

$$Z_{oe} = Z_o/(1 + C_t/C_i)^{**}0.5$$

$$t_{pde} = t_{pd} * (1 + C_t/C_i)^{**}0.5$$

where C_i = intrinsic line capacitance

C_t = additional capacitance due to gate loading.

These formulas indicate that the loading of lines *decreases* the effective impedance of the line and *increases* the propagation delay. As was mentioned earlier, lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced. One of these parasitic electrical characteristics is the inductance found in all leadframe materials.

Figure 16 shows a simple circuit model for a CMOS device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

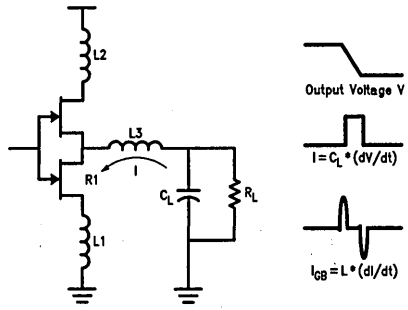

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FIGURE 16. Ground Bounce

The three waveforms shown represent how ground bounce is generated. The top waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, and the inductors L1 and L3, and C_L, the load capacitance. In order to change the output from a HIGH to a LOW, current must flow to discharge the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = -C_L * (dV/dt)$]. This current, as it changes, causes a voltage to be generated across the inductances in the circuit. The formula for the voltage across an inductor is $V = L(dI/dt)$. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{GB} = L1 * (dI/dt)$]. This induced voltage creates what is known as ground bounce.

Because the inductor is between the external system ground and the internal device ground, the induced voltage causes the internal ground to be at a different potential than the external ground. This shift in potential causes the device inputs and outputs to behave differently than expected because they are referenced to the internal device ground, while the devices which are either driving into the inputs or being driven by the outputs are referenced to the external system ground. External to the device, ground bounce causes input thresholds to shift and output levels to change.

Although this discussion is limited to ground bounce generated during HIGH-to-LOW transitions, it should be noted that the ground bounce is also generated during LOW-to-HIGH transitions. This ground bounce though, has a much smaller amplitude and therefore does not present the same concern.

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60–70 pF, increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load itself. Moving the load away from the output also reduces the ground bounce.

- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away due to effectively lower L1 and L3.
- Voltage: lowering V_{CC} reduces ground bounce.

Ground bounce produces several symptoms:

- Altered device states.
- Propagation delay degradation.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.

NOISE SUPPRESSION TECHNIQUES

EMI control techniques involve both hardware implementations and methods and procedures. They may also be divided into intra-system and inter-system EMI control. Our major concern in this Application Note is intra-system EMI control, however, an overview of each may be appropriate at this time.

Figure 17 illustrates the basic elements of concern in an intra-system EMI problem. The test specimen may be a single box, an equipment, subsystem, or system (an ensemble of boxes with interconnecting cables). From a strictly nearsighted or selfish point-of-view, the only EMI concern would appear to be degradation of performance due to self jamming such as suggested at the top of the figure. While this might be the primary emphasis, the potential problems associated with either (1) susceptibility to outside conducted and/or radiated emissions or (2) tendency to pollute the outside world from its own undesired emissions, come under the primary classification of intra-system EMI. Corresponding EMI-control techniques, however, address themselves to both self-jamming and emission/susceptibility in accordance with applicable EMI specifications. The techniques that will be discussed include filtering, shielding, wiring, and grounding.

Inter-system EMI distinguishes itself by interference between two or more discrete and separate systems or platforms which are frequently under independent user control. Culprit emissions and/or susceptibility situations are divided into two classes: (1) antenna entry/exit and (2) back-door entry/exit. More than 95% of inter-system EMI problems involve the antenna entry/exit route of EMI. We can group inter-system EMI-control techniques by four fundamental categories: frequency management, time management, location management, and direction management.

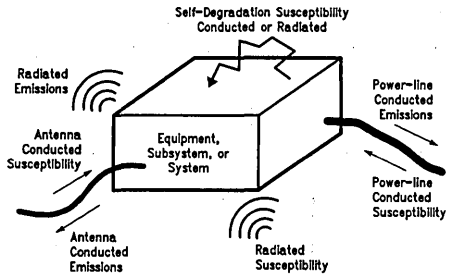

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FIGURE 17. Intra-System EMI Manifestations

The first step in locating a solution is to identify the problem as either an inter-system or intra-system EMI situation. Generally, if the specimen has an antenna and the problem develops from what exits or enters the antenna from another specimen or ambient, then the problem is identified as an inter-system EMI one. Otherwise, it is an intra-system EMI situation which we will discuss now.

Intra-System EMI-Control Techniques

Shielding

Shielding is used to reduce the amount of electromagnetic radiation reaching a sensitive victim circuit. Shields are made of metal and work on the principle that electromagnetic fields are reflected and/or attenuated by a metal surface. Different types of shielding are needed for different types of fields. Thus, the type of metal used in the shield and the shield's construction must be considered carefully if the shield is to function properly. The ideal shield has no holes or voids, and, in order to accommodate cooling vents, buttons, lamps, and access panels, special meshes and "EMI-hardened" components are needed.

Once a printed-circuit board design has been optimized for minimal EMI, residual interference can be further reduced if the board is placed in a shielded enclosure. A box's shielding effectiveness in decibels depends on three main factors: its skin, the control of radiation leakage through the box's apertures or open areas (like cooling holes), and the use of filters or shields at entry or exit spots of cables.

A box skin is typically fabricated from sheet metal or metallized plastic. Normally sheet metal skin that is 1 mm thick is more than adequate; it has a shielding effectiveness of more than 100 dB throughout the high-frequency spectrum from 1 MHz to 20 GHz. Conductive coatings on plastic boxes are another matter. Table I shows that at 10 MHz the shielding effectiveness can be as low as 27 dB if a carbon composite is used, or it can run as high as 106 dB for zinc sprayed on plastic by an electric arc process. Plastic filled materials or composites having either conductive powder, flakes, or filament are also used in box shielding; they have an effectiveness similar to that of metallized plastics.

TABLE I

Shielding Material	Surface Resistance,* Ohms/ Square	Shielding Effectiveness, dB		
		At 10 MHz	At 100 MHz	At 1 GHz
Silver Acrylic Paint	0.004	67	93	97
Silver Epoxy Paint	0.1	59	81	87
Silver Deposition	0.05	57	82	89
Nickel Composite	3.0	35	47	57
Carbon Composite	10.0	27	35	41
Arc-Sprayed Zinc	0.002	106	92	98
Wire Screen (0.64 mm Grid)	N.A.	86	66	48

*Effectiveness of shielding materials with 25-μm thickness and for frequencies for which the largest dimension of the shielding plate is less than a quarter of a wavelength.

In many cases shielding effectiveness of at least 40 dB is required of plastic housings for microcontroller-based equipment to reduce printed-circuit board radiation to a level that meets FCC regulations in the United States or those of the VDE in Europe. Such skin shielding is easy to achieve. The problem is aperture leakage. The larger the aperture, the greater its radiation leakage because the shield's natural attenuation has been reduced. On the other hand, multiple small holes matching the same area as the single large aperture can attain the same amount of cooling with little or no loss of attenuation properties.

Filtering

Filters are used to eliminate conducted interference on cables and wires, and can be installed at either the source or the victim. *Figure 18* shows an AC power-line filter. The values of the components are not critical; as a guide, the capacitors can be between 0.01 and 0.001 μF, and the inductors are nominally 6.3 μH. Capacitor C1 is designed to shunt any high-frequency differential-mode currents before they can enter the equipment to be protected. Capacitors C2 and C3 are included to shunt any common-mode currents to ground. The inductors, L1 and L2, are called common-mode chokes, and are placed in the circuit to impede any common-mode currents.

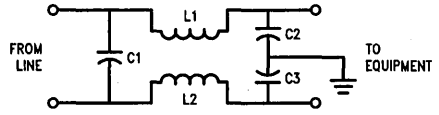

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FIGURE 18. Filtering

Wiring

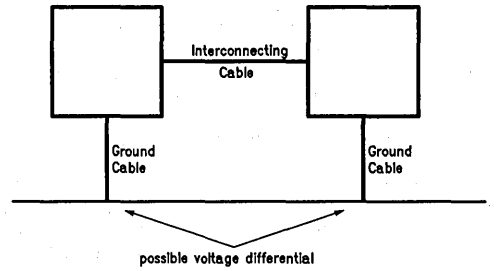
Now that the equipment in each box can be successfully designed to combat EMI emission and susceptibility separately, the boxes may be connected together to form a system. Here the input and output cables and, to a lesser extent, the power cable form an "antenna farm" that greatly threatens the overall electromagnetic compatibility of the system. Most field remedies for EMI problems focus on the coupling paths created by the wiring that interconnects systems. By this time most changes to the individual equipment circuits are out of the question.

Let us address five coupling paths that are encountered in typical systems comprised of two or more pieces of equipment connected by cables. These should adequately cover most EMI susceptibility problems. They are:

- *A common ground impedance coupling*—a conducting path in which a common impedance is shared between an undesired emission source and the receptor.
- *A common-mode, radiated field-to-cable coupling,* in which electromagnetic fields penetrate a loop formed by two pieces of equipment, a cable connecting them, and a ground plane.
- *A differential-mode, radiated field-to-cable coupling,* in which the electromagnetic fields penetrate a loop formed by two pieces of equipment and an interconnecting transmission line or cable.
- *A crosstalk coupling*, in which signals in one transmission line or cable are capacitively or inductively coupled into another transmission line.
- *A conductive path* through power lines feeding the equipment.

The first coupling path is formed when two pieces of equipment are connected to the same ground conductor at different points, an arrangement that normally produces a voltage difference between the two points. If possible, connecting both pieces of equipment to a single-point ground eliminates this voltage. Another remedy is to increase the impedance along a loop that includes the path between the ground connections of the two boxes. Examples include the isolation of printed-circuit boards from their cabinet or case, the use of a shielded isolation transformer in the signal path, or the insertion of an inductor between one or both boxes and the ground conductor. The use of balanced circuits, differential line drivers and receivers, and absorbing ferrite beads and rods on the interconnecting cable can further reduce currents produced by this undesirable coupling path.

Common Ground Impedance Coupling



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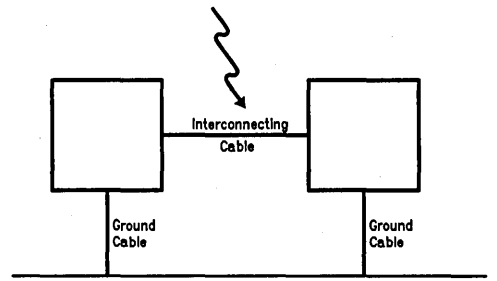
A balanced circuit is configured so its two output signal leads are electrically symmetrical with respect to ground, as the signal increases on one output the signal on the other decreases. Differential line drivers produce a signal that is electrically symmetrical with respect to ground from a single-ended circuit in which only one lead is changing with respect to ground. Ferrite beads, threaded over electrical conductors, substantially attentuate electromagnetic interference by turning radio-frequency energy into heat, which is dissipated in them.

In the second coupling path, a radiated electromagnetic field is converted into a common-mode voltage in the ground plane loop containing the interconnect cable and both boxes. This voltage may be reduced if the loop area is trimmed.

Common-Mode, Radiated Field-to-Cable Coupling



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The third coupling path produces a differential-mode voltage that appears across the input terminals of the EMI receptor. One way of controlling this is to cancel or block the pickup of differential-mode radiation. In a balanced transmission line, this is done by use of twisted-wire pairs and a shielded cable.

As for crosstalk, the fourth coupling path—the reduction of capacitive coupling can be achieved by the implementation of at least one of these steps:

- Reducing the spacing between wire pairs in either or both of the transmission lines.
- Increasing the separation between the two transmission lines.
- Reducing the frequency of operation of the source, if possible.
- Adding a cable shield over either or both transmission lines.
- Twisting the source's or receptor's wire pairs.
- Twisting both wire pairs in opposite directions.

The fifth coupling path conductively produces both common-mode and differential-mode noise pollution on the power mains. Among several remedies that can suppress the EMI here are the filters and isolation transformers.

There are only about 50 common practical remedies that can be used in most EMI situations. Of these, about 10 suffice in 80 percent of the situations. Most engineers are aware of at least some of these remedies—for example, twisting wires to reduce radiation pickup.

In order to attack the EMI problem, one can make use of the information contained in Table II. First, decide what coupling path has the worst EMI interference problem. From the 11 most common coupling paths listed at the top of the table, find the problem coupling path. Using the numbers found in that table entry, locate the recommended remedy or remedies from the 12 common EMI fixes identified at the bottom of the table. This procedure should be repeated until all significant coupling paths have been properly controlled and the design goal has been met.

Inter-System EMI Control Techniques

There are many EMI controls that may be carried out to enhance the chances of inter-system EMC. They can be grouped into four categories which we will discuss briefly. The following discussion is not intended to be complete but merely provide an overview of some EMI control techniques available to the intersystem designer and user.

Frequency management suggests both transmitter emission control and improvement of receptors against spurious responses. The object is to design and operationally maintain transmitters so that they occupy the least frequency spectrum possible in order to help control electromagnetic pollution. For example, this implies that long pulse rise and fall times should be used. Quite often one of the most convenient, economic and rapid solutions to an EMI problem in the field, is to change frequency of either the victim receiver or the culprit source.

In those applications where information is passed between systems, a possible time management technique could be utilized where the amount of information transferred is kept to a minimum. This should reduce the amount of time that the receptor is susceptible to any EMI. In communication protocols, for example, essential data could be transmitted in short bursts or control information could be encoded into fewer bits.

Location management refers to EMI control by the selection of location of the potential victim receptor with respect to all other emitters in the environment. In this regard, separation distance between transmitters and receivers is one of the most significant forms of control since interfering source emissions are reduced greatly with the distance between them. The relative position of potentially interfering transmitters to the victim receiver are also significant. If the emitting source and victim receiver are shielded by obstacles, the degree of interference would be substantially reduced.

Direction management refers to the technique of EMI control by gainfully using the direction and attitude of arrival of electromagnetic signals with respect to the potential victim's receiving antenna.

TABLE II. Electromagnetic Interference Coupling Paths

Radiated Field to Interconnecting Cable (Common-Mode)	**2, 7, 8, 9, 11**	**Radiated Field to Box**	**12, 13**
Radiated Field to Interconnecting Cable (Differential-Mode)	**2, 5, 6**	**Box to Radiated Field**	**12, 13**
Interconnecting Cable to Radiated Field (Common-Mode)	**1, 3, 9, 11**	**Box-to-Box Radiation**	**12, 13**
Interconnecting Cable to Radiated Field (Differential-Mode)	**1, 3, 5, 6, 7**	**Box-to-Box Conduction**	**1, 2, 7, 8, 9**
Cable-to-Cable Crosstalk	**1, 2, 3, 4, 5, 6, 10, 11**	**Power Mains to Box Conduction**	**4, 11**
		Box to Power Mains Conduction	**4**

Electromagnetic Interference Fixes

1. **Insert Filter In Signal Source**
2. **Insert Filter in Signal Receptor**
3. **Insert Filter in Power Source**
4. **Insert Filter in Power Receptor**
5. **Twist Wire Pair**
6. **Shield Cable**
7. **Use Balanced Circuits**
8. **Install Differential Line Drivers and Receivers**
9. **Float Printed Circuit Board(s)**
10. **Separate Wire Pair**
11. **Use Ferrite Beads**
12. **Use a Multilayer Instead of a Single-Layer Printed Circuit Boards**

DESIGN GUIDELINES

The growth of concern over electromagnetic compatibility (EMC) in electronic systems continues to rise in the years since the FCC proclaimed that there shall be no more pollution of the electromagnetic spectrum. Still, designers have not yet fully come to grips with a major source and victim of electromagnetic interference—the printed circuit board. The most critical stage for addressing EMI is during the circuit board design. Numerous tales of woe can be recounted about the eleventh hour attempt at solving an EMI problem by retrofit because EMC was given no attention during design. This retrofit ultimately costs much more than design stage EMC, holds up production, and generally makes managers unhappy. With these facts in mind, let's address electromagnetic compatibility considerations in printed circuit board design.

Logic Selection

Logic selection can ultimately dictate how much attention must be given to EMC in the total circuit design. The first guideline should be: use the slowest speed logic that will do the job. Logic speed refers to transition times of output signals and gate responses to input signals. Many emissions and susceptibility problems can be minimized if a slow speed logic is used. For example, a square wave clock or signal pulse with a 3 ns rise time generates radio frequency (100 MHz and higher) energy that is gated about on the PC board. It also means that the logic can respond to comparable radio frequency energy if it gets onto the boards.

The type of logic to be used is normally an early design decision, so that control of edge speeds and, hence, emissions and susceptibility is practical early. Of course, other factors such as required system performance, speed, and timing considerations must enter into this decision. If possible, design the circuit with a slow speed logic. The use of slow speed logic, however, does not guarantee that EMC will exist when the circuit is built; so proper EMC techniques should still be implemented consistently during the remainder of the circuit design.

Component Layout

Component layout is the second stage in PC board design. Schematics tell little or nothing about how systems will perform once the board is etched, stuffed, and powered. A circuit schematic is useful to the design engineer, but an experienced EMC engineer refers to the PC board when troubleshooting. By controlling the board layout in the design stage, the designer realizes two benefits: (1) a decrease in EMI problems when the circuit or system is sent for EMI or quality assurance testing; and (2) the number of EMI coupling paths is reduced, saving troubleshooting time and effort later on.

Some layout guidelines for arranging components according to logic speed, frequency, and function are shown in *Figure 19*. These guidelines are very general. A particular circuit is likely to require a combination and/or tradeoffs of the above arrangements. Isolation of the I/O from digital circuitry is important where emissions or susceptibility may be a problem. For the case of emissions, a frequently encountered coupling path involves a digital energy coupling through I/O circuitry and signal traces onto I/O cables and wires, where the latter subsequently radiate. When susceptibility is a problem, it is common for the EMI energy to couple from I/O circuits onto sensitive digital lines, even though the I/O lines may be "opto-coupled" or otherwise supposedly isolated. In both situations, the solution often lies in the proper electrical and physical isolation of analog and low speed digital lines from high speed circuits. When high speed signals are designed to leave the board, the reduction of EMI is usually performed via shielding of I/O cables and is not considered here.

Therefore, a major guideline in laying out boards is to isolate the I/O circuitry from the high speed logic. This method applied even if the logic is being clocked at "only" a few MHz. Often, the fundamental frequency is of marginal interest, with the harmonics generated from switching edges of the clock being the biggest emission culprits. Internal system input/output PCB circuity should be mounted as close to the edge connector as possible and capacitive filtering of these lines may be necessary to reduce EMI on the lines.

High speed logic components should be grouped together. Digital interface circuitry and I/O circuitry should be physically isolated from each other and routed on separate connectors, if possible as shown in *Figure 19d*.

- No High Frequency Signals to the Backplane

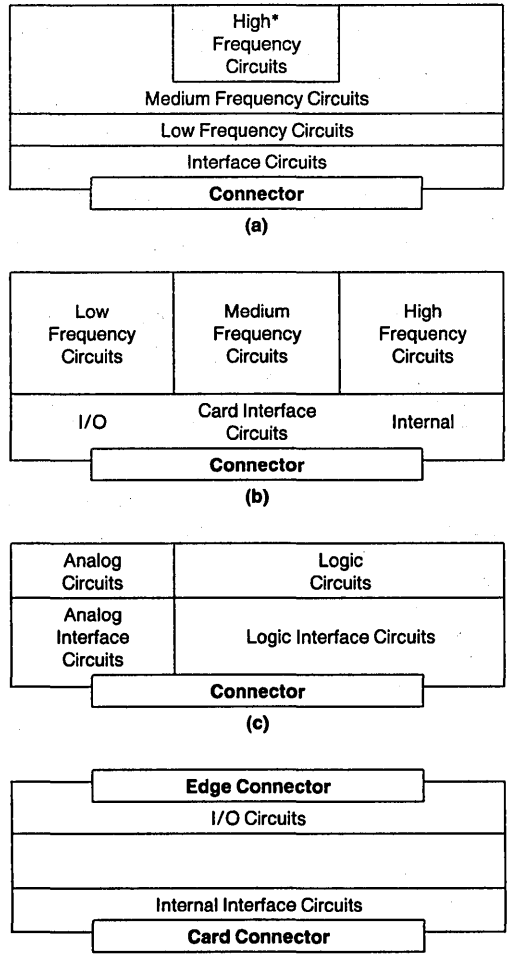

FIGURE 19. Board Layout

Power Supply Bussing

Power supply bussing is the next major concern in the design phase. Isolated digital and analog power supplies must be used when mixing analog and digital circuitry on a board. The design preferably should provide for separate power supply distribution for both the analog and digital circuitry. Single point common grounding of analog and digital power supplies should be performed at one point and one point only—usually at the motherboard power supply input for multi-card designs, or at the power supply input edge connector on a single card system. The fundamental feature of good power supply bussing, however, is low impedance and good decoupling over a large range of frequencies. A low impedance distribution system requires two design features: (1) proper power supply and return trace layout and (2) proper use of decoupling capacitors.

At high frequencies, PCB traces and the power supply busses ($+V_{CC}$ and 0V) are viewed as transmission lines with associated characteristic impedance, Z_O, as modeled in *Figure 20*. The goal of the designer is to maximize the capacitance between the lines and minimize the self-inductance, thus creating a low Z_O. Table III shows the characteristic impedance of various two-trace configurations as a function of trace width, W, and trace separation, h.

TABLE III

W/h or D/W	#1 Parallel Strips*	#2 Strip Over Ground Plane*	#3 Strips Side by Side**
0.5	377	377	NA
0.6	281	281	NA
0.7	241	241	NA
0.8	211	211	NA
0.9	187	187	NA
1.0	169	169	0
1.1	153	153	25
1.2	140	140	34
1.5	112	112	53
1.7	99	99	62
2.0	84	84	73
2.5	67	67	87
3.0	56	56	98
3.5	48	48	107
4.0	42	42	114
5.0	34	34	127
6.0	28	28	137
7.0	24	24	146
8.0	21	21	153
9.0	19	19	160
10.0	17	17	166
12.0	14	14	176
15.0	11.2	11.2	188
20.0	8.4	8.4	204
25.0	6.7	6.7	217
30.0	5.6	5.6	227
40.0	4.2	4.2	243
50.0	3.4	3.4	255

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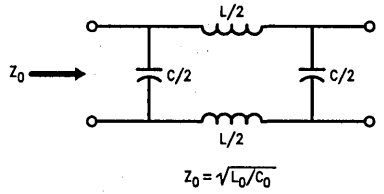
*Mylar dielectric assumed: DC = 5.0 D ≫ nearby ground plane

**Paper base phenolic or glass epoxy assumed: DC = 4.7

$Z01 = (377/\sqrt{DC}) \times (h/W)$, for $W > 3h$ and $h > 3t$

$Z02 = (377/\sqrt{DC}) \times (h/W)$, for $W > 3h$

$Z03 = (120/\sqrt{DC}) \ln (D/W + \sqrt{D/W^2 - 1})$ for $W \gg t$



TL/DD/10562-29

where L_O and C_O are, respectively, the distributed inductance and capacitance per unit length of the line

FIGURE 20

Any one of the three configurations may be viewed as a possible method of routing power supply (or signal) traces. The most important feature of Table III is the noticeable difference in impedance between the parallel strips and strip over ground plane compared with the side-by-side configurations.

As an example of the amount of voltage that can be generated across the impedance of a power bus, consider TTL logic which pulls a current of approximately 16 mA from a supply that has a 25Ω bus impedance (this assumes no decoupling present). The transient voltage is approximately $dV = 0.016 \times 25\Omega = 400$ mV, which is equal to the noise immunity level of the TTL logic. A 25Ω (or higher) impedance is not uncommon in many designs where the supply and return traces are routed on the same side of the board in a side-by-side fashion. In fact, it is not uncommon to find situations where the power supply and return traces are routed quite a distance from each other, thereby increasing the overall impedance of the distribution system. This is obviously a poor layout.

Power and ground planes offer the least overall impedance. The use of these planes leads the designer closer to a multi-layer board. At the very least, it is recommended that all open areas on the PC board be "landfilled" with a 0V reference plane so that ground impedance is minimized.

Multi-layer boards offer a considerable reduction in power supply impedance, as well as other benefits. As shown in Table III, the impedance of a multi-layer power/ground plane bus grows very small (on the order of an ohm or less), assuming a W/h ratio greater than 100. Multi-layer board designs also pay dividends in terms of greatly reduced EMI, and they provide close control of line impedances where impedance matching is important. In addition, shielding benefits can be realized. For high-density, high-speed logic applications, the use of a multi-layer board is almost mandatory. The problem with multi-layer boards is the increased cost of design and fabrication and increased difficulty in board repair.

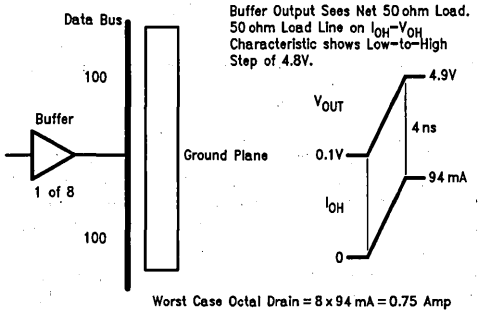
Decoupling

High-speed CMOS has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with CMOS devices in system performance and EMC performance.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to a HIGH value. This power is necessary to charge the load capacitance or drive a line impedance.

For most power distribution networks, the typical impedance can be between 50 and 100Ω. This impedance appears in series with the load impedance and will cause a droop in the

V_{CC} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example presented in *Figure 21* used to help calculate the amount of decoupling necessary. This circuit utilizes an octal buffer driving a 100Ω bus from a point somewhere in the middle.

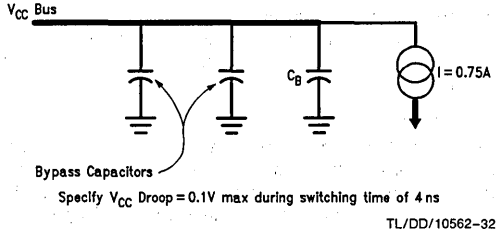


TL/DD/10562–31

FIGURE 21

Being in the middle of the bus, the driver will see two 100Ω loads in parallel, or an effective impedance of 50Ω. To switch the line from rail to rail, a drive of 94 mA is needed (4.8V/50Ω) and more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will be to lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current demands. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in *Figure 22*.

In this example, if the V_{CC} droop is to be kept below 0.1V and the edge rate equals 4 ns, we can calculate the value of the decoupling capacitor by use of the charge on a capacitor equation: Q = CV. The capacitor must supply the high demand current during the transition period and is represented by I = C (dV/dt). Rearranging this somewhat yields C = I (dt/dV).



TL/DD/10562–32

Q = CV charge on capacitor
I = C dV/dt
C = I dt/dV = 750 mA × 4 ns / 0.1V = 0.030 μF
Select C_B = 0.047 μF or greater

FIGURE 22

Now, I = 750 mA assuming all 8 outputs switch simultaneously for worst case conditions, dt = switching period or 4 ns, and dV is the specified V_{CC} droop of 0.1V. This yields a calculated value of 0.030 μF for the decoupling capacitor. So, a selection of 0.047 μF or greater should be sufficient.

It is good practice to distribute decoupling capacitors evenly throughout the logic on the board, placing one capacitor for every package as close to the power and ground pins as possible. The parasitic induction in the capacitor leads can be greatly reduced or eliminated by the use of surface mount chip capacitors soldered directly onto the board at the appropriate locations. Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

Proper Signal Trace Layout

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

For those situations where lines must run parallel as in address and data buses, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing.

There are several termination schemes which may be used. They are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula:

$$V_W = V_{CC} * Z_{oe} / (Z_{oe} + R_S + Z_S)$$

Series Termination

TL/DD/10562–33

$$V_w = V_{CC} \times Z_{oe}/(Z_{oe} + R_S + Z_S)$$

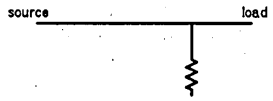
where R_S is the series resistor
Z_S is the output impedance of the driver
Z_{oe} is the equivalent line impedance

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance (Z_{oe}). The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has

propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground depending on which bus the resistor is connected to. While this feature is not desirable for driving CMOS inputs because the trip levels are typically $V_{CC}/2$, it can be useful for driving TTL inputs where level shifting is desirable in order to interface with CMOS devices.

Parallel Termination



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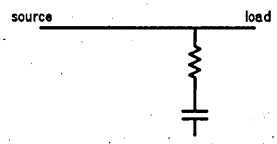
AC parallel terminations work well for applications where the increase in bus delays caused by series terminations are undesirable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

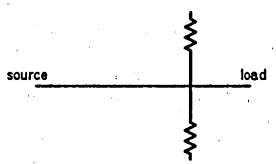
Thevenin terminations are not generally recommended due to their power consumption.

AC Parallel Termination



TL/DD/10562-35

Thevenin Termination



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Like parallel terminations, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally be independent of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that output lines with Thevenin terminations should not be left floating since this will cause the undriven input levels to float between V_{CC} and ground, increasing power consumption.

Ground Bounce

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

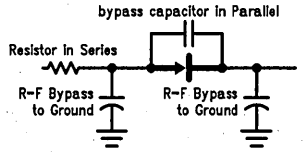
- First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs. Ground bounce glitches may cause spurious inputs that will alter the state of non-clocked logic.
- Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

  When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:
- Choose package outputs that are as close to the ground pin as possible to drive asynchronous TTL-level inputs.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Components

The interference effect by rectifier diodes, typically found in power supply sections of PC boards, can be minmized by one or more of the following measures:

- Placing a bypass capacitor in parallel with each rectifier diode.
- Placing a resistor in series with each rectifier diode.
- Placing an R-F bypass capacitor to ground from one or both sides of each rectifier diode.
- Operating the rectifier diodes well below their rated current capability.



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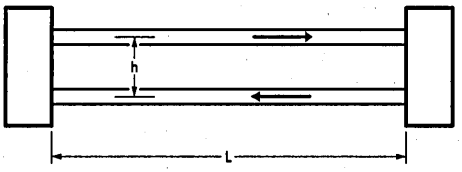
Connectors



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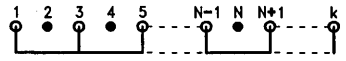
Cables and Connectors

Several options are available to reduce EMI from a typical ribbon cable used to interconnect pieces of equipment. These include:

- Reduce spacing between conductors (h in the figure) by reducing the size of wires used and reducing the insulation thickness.
- Join alternate signal returns together at the connectors at each end of the cable.
- Twist parallel wire pairs in ribbon cables.
- Shield ribbon cable with metal foil cover (superior to braid).
- Replace discrete ribbon cable with stripline flexprint cable.

In the case of joining alternate signal returns, wire N is carryig the signal current, i_n, whereas its mates, N−1 and N+1 wires are each carrying one half of the return currents, i_{n-1} and i_{n+1}, respectively. Thus, radiation from pair N and N−1 is out of phase with radiation from pair N and N+1 and will tend to cancel. In practice, however, the net radiation is reduced by 20–30 dB with 30 dB being a good default value.

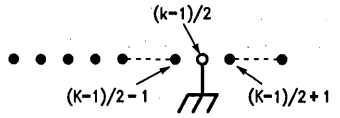
Alternating Signal Returns Minimizes Radiation



TL/DD/10562–39

The opposite of this is to conserve signal returns by only using one, or two, wires to service N data lines in a ribbon cable. For data lines farther from the return line, the differential mode radiation becomes so great that this cable tends to maximize EMI radiation. Another disadvantage of this approach is poor impedance control in the resulting transmission line. This could result in distortion of pulses and cause reflections, especially for high-speed logic, and common return impedance noise in this single ground wire.

Single Signal Return Maximizes Radiation



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Ideally, connectors should have negligible resistance for obvious reasons other than EMI control. They should provide foolproof alignment to minimize the possibility of contact damage over time and use which would increase the resistance and be prone to vibration and shock. Adequate force to provide good mating between contacts which will insure low resistance and limit likelihood of damage. Connectors should mate with little friction to minimize the effects of continual disconnections and connections increasing the contact resistance with use as the contacts wear out. A contamination free design should be used to avoid corrosion and oxidation increasing resistance and susceptibility to shock and vibration causing intermittent contact.

Special Considerations with Development Tools

The following set of guidelines have been compiled from the experiences of the Development Systems Group and the Microcontroller Applications Group in Santa Clara. They should be considered *additional* techniques and guidelines to be followed concurrently with the standard ones already presented. Some are general and some may be specific to development systems use.

Ground bounce prevention and minimization techniques presented in this Application Note should be strictly adhered to when using '373 type transparent latches on the HPC's external address/data bus. Multiple simultaneously switching outputs could produce ground bounce significant enough to cause false latching. Observe good EMI planning by locating the latches as close to the HPC as possible. The use of multi-layer printed circuit boards with good ground planes and following appropriate layout techniques is also essential, especially if emulation will be done at frequencies above 10 MHz. With the foregoing discussions about "antenna farms", radiated noise, and ideal connector characteristics, it becomes obvious that wire-wrap boards and the use of IC sockets is absolutely out of the question. The concern here is not so much EMI affecting the outside world but EMI strangling the operation of the module itself.

The inputs to the buffers in a '244 type octal buffer package are placed adjacent or side-by-side outputs of other buffers in the package. This configuration would tend to maximize the crosstalk or noise coupling from the inputs to the outputs. On the other hand, the buffer inputs in a '544 type package are on one side of the package and the outputs are on the other. The use of these package types in high speed designs can facilitate board layout to help reduce the effects of crosstalk.

Use extra heavy ground wires between emulator and target board. Rely on the ground returns in the emulator cable for reduction of differential-mode noise radiated from the cable but heavy-duty help is required for reducing power line impedance in the integrated development system.

Unused HPC inputs, most importantly NMI and RDY/$\overline{\text{HLD}}$, must be tied to V_{CC} directly or through a pull-up resistor. This not only tends to reduce power consumption, but will avoid noise problems triggering an unwanted action.

In order to reduce the effects of noise generated by high speed signal changes, a sort of Frequency Management technique might be applied. If possible, develop application hardware and software at a slower crystal operating frequency. If ringing, crosstalk, or other combinations of radiated and conducted noise problems exist, the result may be to move the problem from one point in the affected signal waveform to a different point. Thus, apparent "noise glitches" that caused a latch to erroneously trigger when the input data was still changing, may now come at a time when they are non-destructive such as at a point when the input data is now stable.

Some applications require driving the HPC clock input, CKI, with an external signal. The emulator tools are all clocked using a crystal network with the HPC so that the generation of the system timing is contained on the tool itself. Consequently, there is no connection between the emulator cable connector on the tool and the CKI pin at the HPC. However, when the emulator cable is now inserted into the target board, the target board's clock signal travelling along the cable couples noise onto adjacent signal lines causing symptoms pointing to an apparent failure of the emulator tool. The recommendation is to disable the clock drive to the CKI pin at the HPC pad on the target board whenever the emulator tool is connected. The emulator tools supply the system clock so there is no need for the clock on the target and signal crosstalk on the emulator cable can be greatly reduced with minimal implementation. If one insists that the emulator tool and the target be synchronous, then bring the clock signal from the target to the emulator tool external to the emulator cable via twisted wire pair or coax cable. Remove the clock drive connection to CKI at the target to prevent the signal from entering the cable. Finally, remove crystal components on emulator tool to prevent problems with the signal.

Connecting boards and modules together to make a totally unique system in which EMC was practiced is necessary to ensure little problem with the environment. But, connecting

an emulator tool makes it an entirely new and unique system, both in physical and electrical properties. Treat the emulator tool as part of the system during the design phase and development phase.

NOISE MEASUREMENT

The basic purpose of FCC Part 15J is to minimize the jamming of commercial broadcasting systems by computer devices. Toward this end, the FCC has established test limits, for both conducted and radiated emissions, which must be met. These two tests together span the frequency range from 450 kHz to 1000 MHz. To accomplish FCC Part 15J testing requires the following equipment and associated support items:

- EMC Receivers or Spectrum Analyzers to cover the frequency range from 450 kHz to 1000 MHz.
- Dipole antennas (2) to cover the frequency range from 30 MHz to 1000 MHz.
- Masts or supports which will allow antenna elevation to be increased to at least 4 meters and also allow the polarization to be changed.
- Line impedance stabilization networks (LISN) built in accordance with CISPR requirements. These are 50Ω, 50 μH devices and are inserted between power mains and test item to permit making repeatable conducted EMI measurements.
- Power line filters.
- An appropriate test site.

Environment

The most controversial item on the test requirement list is the appropriate test site. The FCC required emission limits are comparable with the ambient RF level. These low limits and the noisy ambient would indicate that the tests should be made in a shielded enclosure. Unfortunately, all shielded enclosures introduce significant errors into the radiated measurements because of room reflections, room resonances, and antenna loading. To reduce the magnitude of these problems, the FCC has specified that measurements should be made at an open-field test site. Open-field test sites frequently have high ambient levels especially in the FM broadcast band. They may also have ground reflection variations as a function of soil moisture.

The FCC will permit the use of anechoic shielded enclosures which have reduced reflections, provided an error analysis is made to show correlation of interior RF levels with those of an open-field test site. The cost of an anechoic enclosure is its major drawback. For measurements other than for certification, the test site does not have to be in accordance with government regulations. There are also alternatives where an agency or private company will perform the tests for you at their facility for a nominal fee.

Many manufacturers are using shielded enclosures that they have constructed on site or purchased from one of the shielded enclosures manufacturers. The measurement requirement is that the RF ambient levels should be 6 dB or more below the specifications limits. This may require 20 dB worth of aluminum foil or 160 dB worth of electrical seals. Only a site survey can provide that answer. In any case, some margin of safety should be made, 6–10 dB, plus periodic check for reflection problems.

Instrumentation

After the appropriate test site has been obtained, whether a room or a quiet open field, then the testing can begin. If the equipment to be tested is not floor standing, the test sample is placed on a non-conducting stand 80 cm high and at least 40 cm from the wall of the enclosure. Antennas are then set up so that radiated emission levels can be measured. The test sample should be loaded with full electrical and mechanical loads and operated in a manner that closely approximates normal operation. During operation of the equipment under test, the EMI measuring equipment is used to determine the amplitude of the radiated emission.

At NSC, we have a spectrum analyzer than can be attached to a Personal Computer that runs software to control experiments and report results. It automatically marks the computer display with FCC limits for quick comparison with the amplitude of the emissions signal. This setup is outside the shielded enclosure and can be used to determine if the equipment under test is failing any FCC requirements.

If the test sample fails, we can move inside the room and use near-field probes to help pinpoint the source of emissions. The spectrum analyzer samples the signal generated by the source at many different frequencies. The scale across the bottom of the screen is frequency and the scale along the side is signal amplitude in dBuV/m. Thus, we can quickly determine where the peak amplitude of the generated noise is located, read what level that is, and at what frequency it is being generated.

A little analysis and thought should then allow you to determine what signal could be the culprit. For example, if the noise problem is at 16 MHz and the system clock is 16 MHz, then the basic clock signal is causing the problem. If the noise problem is at even multiples of 16 MHz it could be caused by rise and fall times on the 16 MHz clock or overshoot and undershoot on that clock. In the case of the HPC, since it generates a clock output that is the system clock divided by 2 (CK2 = CKI/2), the noise frequency generated at the multiple of the 16 MHz signal could also be due to CK2 or any device that is clocked by that signal. Unfortunately for the investigator, everything else inside the part is clocked by CK2, which includes bus transitions and input sampling.

Cost

Basically, the risks of no EMI control will include the following:

- Vehicle/System Performance Degradation
- Degradation to outside world equipment
- Personal Hazards
- Ordinance Hazards
- Acceptance Delays

The sum which can mean anything from a minor system or equipment performance compromise to the total cancellation of a project.

The cost of EMI control will vary and include the following:

- Government procurement requirements
- Company proposal preparation
- EMI Control Plan
- Test Plan
- EMI Tests and Reports

A rough guideline that can be used might be:

1%–3%% of $100 Million projects
3%–7% of $1 Million to $10 Million projects
7%–12% of small items

SUMMARY

The design and construction of an electromagnetically compatible printed circuit board does not necessarily require a big change in current practices. On the contrary, the implementation of EMC principles during the design process can fit in with the ongoing design. When EMC is designed into the board, the requirements to shield circuitry, cables, and enclosures, as well as other costly eleventh hour surprises, will be drastically reduced or even eliminated. Without EMC in the design stage, production can be held up and the cost of the project increases.

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Build a Direction-Sensing Bidirectional Repeater

National Semiconductor
Application Note 702
Gary Murdock
John Goldie

When designing an EIA-485 control bus to link widely separated machinery and process controllers, devising a scheme to control the repeaters can be one of the more awkward tasks. In long buses, bus segments are joined with repeaters if the distance exceeds the maximum allowed by one cable segment.

Usually the buses are of a master-slave configuration—a bus network can consist of a master, two slaves, and two repeaters, for instance *(Figure 1)*. Amplifying control signals and making sure that they're clearly received by the slaves is one task performed by the repeaters. Repeaters can also increase the number of slaves per cable segment, extending the control bus's reach. To ensure that signals travel through repeaters correctly in both master-to-slave and slave-to-master directions, though, the repeaters must be switched.

Controlling the switching can be a cumbersome task. One way to handle it is to generate a repeater-reversing signal at the slave location and carry it over a dedicated control line to the repeaters. The catch is that the repeater control line needs to be very long—the length of the cable segment, in fact. Handling direction control remotely introduces delays and increases the possibility of errors. Ideally, control of the repeater switching would occur locally, at the repeaters themselves. Designers can achieve this local control and get rid of repeater lines by building a smart, direction-sensing repeater.

CONTROLLING REPEATERS

To see the advantages of direction-sensing repeaters, look at a design that uses repeater control lines *(Figure 2)*. Based on the repeater control circuit used by the Intel Bitbus, this design is for twisted-pair cable. (Sometimes ribbon cable can be used instead). The differential line drivers and receivers are designed for multipoint applications and meet the EIA-485 standard.

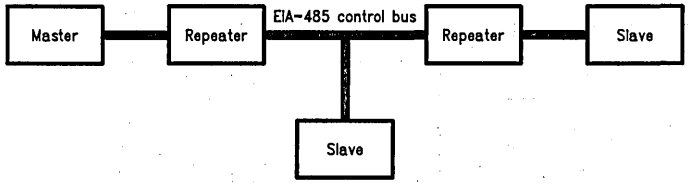

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FIGURE 1. Repeaters Extend the Length of the Twisted-Pair Bus by Transmitting the Signal on to the Next Cable Segment

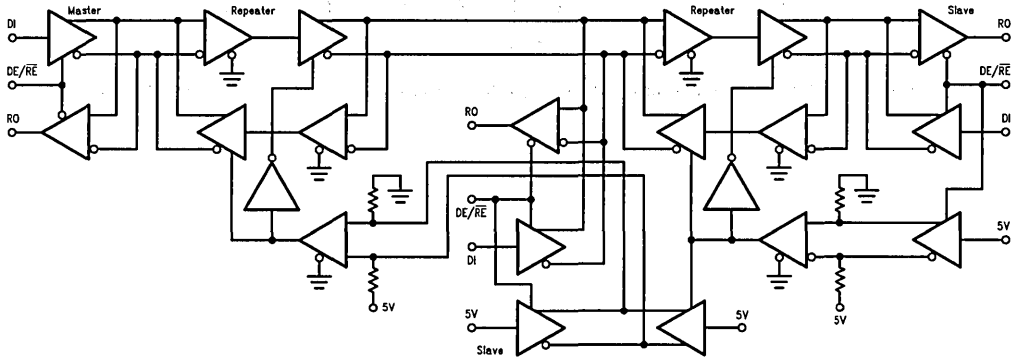

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FIGURE 2. Repeater Direction Can Be Switched from the Slave's End with a Biased Repeater-Control Line

Bias resistors on the control line typically enable the repeater in the direction away from the master. In this case, the master is the talker and the data flows in the master-to-slave direction. When a slave responds to a poll from the master, it drives its direction control line—DE/$\overline{RE}$—high. This drives the slave's repeater control line high, overriding the low state normally imposed by the bias resistors. The orientation of each repeater between the slave and the master is switched to the slave-to-master direction. All other repeaters stay enabled in the direction away from the master—letting slaves talk to any other slave, if the protocol allows it. The repeater control line is actively driven to only one state (high), so that if more than one slave tries to drive the control line at the same time, contention current is minimized.

Eliminating the repeater control line in the network greatly simplifies the circuit *(Figure 3)*. Here, a local data direction-sensing control circuit switches repeater direction. The circuit switches the repeater in the right direction by sensing which side of the data line is active first. If the master side is active first, the repeater is enabled in the master-to-slave direction, and vice versa. If the master and slave are active simultaneously, neither direction is enabled.

Two line-sense circuits work in the local control circuit. One monitors the master side of the data line, the other the slave side. The data line is active when driven to a differential high or low. The data line is inactive when all drivers connected to it are in TRI-STATE®. Resistors bias the sense circuit receiver inputs to produce high receiver outputs when the data line is inactive. When the data line is driven, the bias is overridden and the receivers respond to the signals on the data line. One output switches to the same state as the data line, and the other output switches to the complementary state. An active line sends complementary inputs to the AND gate and switches the sense circuit output low. An inactive data line produces high inputs to the AND gate (because of the resistor bias) and switches the output high. Data direction is determined by detecting which sense-circuit output (master or slave) goes low first.

The direction-sensing repeater design divides into six functional blocks *(Figure 4)*. The first block—block a—is a bidirectional repeater. Block b senses the state of the data line on each side of the repeater. It checks for either a driven state (active) or a high impedance state (inactive). Block c determines the enable signals according to the line states. Block d generates pulses used for masking, clocking, and error signals. Block e filters, generates a pulse, and detects a valid line state change. Block f latches in the most current line state information and generates the enable signals to the repeaters.

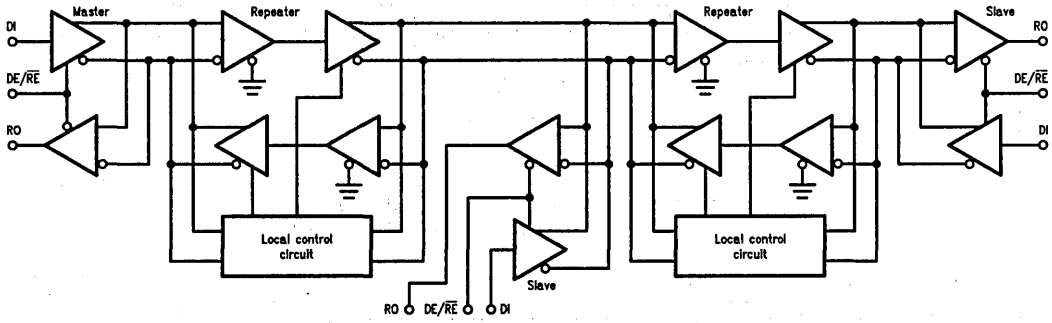

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FIGURE 3. Switching Repeater Direction Locally Avoids a Cumbersome and Costly Repeater Control Line

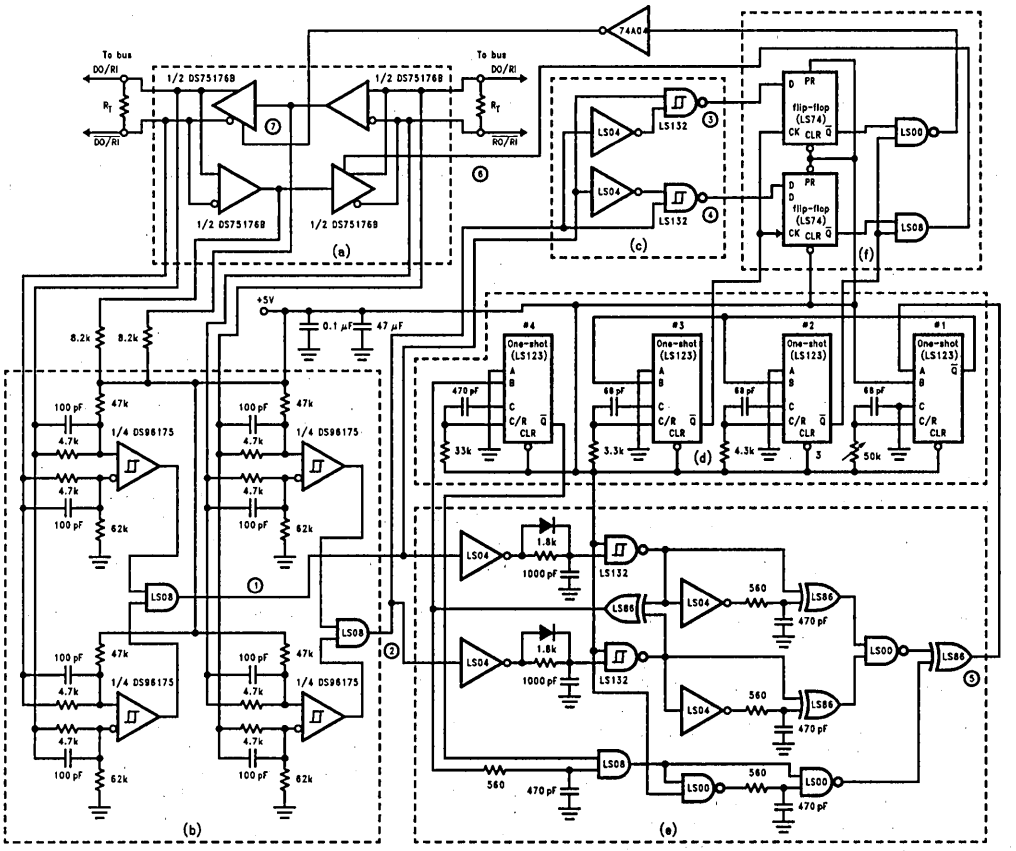

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FIGURE 4. Direction-Sensing Circuitry Switches the Repeater in the Direction that Data Is Being Transmitted

The bidirectional repeater consists of two standard-pinout EIA-485 transceivers. The inverter inverts the enable line on one of the transceivers, so that two standard transceivers can be used. The "active-low" receiver enables are permanently enabled by hard-wiring them to ground. The driver enables are set by the output of the LS00 and LS08 gates. Data lines must be terminated on each side of the repeater to bias the line for the line-sense circuits. The termination resistor should be selected to match the transmission line's characteristic impedance—100Ω to 120Ω is typical for twisted pair.

In block b, an EIA-485 quad receiver senses the line to determine whether it's active or inactive. Each receiver pair monitors one side of the transmission line. The quad receiver's enable should be hard-wired ON. Resistors bias the receiver input to a positive differential voltage that produces a high ouptut when all drivers are in TRI-STATE mode. The receiver outputs are combined with an AND gate. A falling edge at the AND gate output indicates an active line, and a rising edge indicates a return to the Z line state.

The logic in block c—standard gates and the LS132 NAND gate—prevents the repeater from being enabled in case of collision. If both data lines become active at the same time, logic will disable transmission in both directions. In addition to the NAND function, the LS132 gate's inputs have hysteresis to increase noise immunity. This yields a jitter-free output from a slow input signal.

When drivers on each side of the repeater drive the line simultaneously, a collision occurs. To prevent this, the logic in block c keeps both repeater drivers off until the lines on both sides have returned to the inactive state. When a collision occurs, a low appears at signal locations 1 and 2. The logic sets the D flip-flop inputs high, however, so repeater disables—instead of enables—are generated.

When signals 1 and 2 are high, the D flip-flop inputs are high, and both repeater drivers are disabled. If either 1 or 2 is low while the other is high, an enable signal travels to one of the repeater drivers, depending upon which line is low. A valid line state change causes block d to generate a clock pulse that will latch the D flip-flops. After the repeater has turned on, signals 1 and 2 go low, since data is passing through the repeater. Because data transitions don't change the line state—it stays active—no new clock pulse is generated and the enables aren't updated.

TRIGGERING ONE-SHOTS

Block d includes four retriggerable LS123 one-shots for timing functions. The first one-shot is triggered when a valid line state change is detected. Its output trips the second and third one-shots on the same edge. The second one-shot's output is used as an enable mask, while the output of the third generates the clock pulse that latches in the latest enable bits. The fourth one-shot senses errors. It is activated when a collision occurs.

The one-shot's output pulse widths are set by external capacitors and resistors. Standard 74123 one-shots shouldn't be substituted for the LS123 devices, because the LS123 IC's clear pin is also a trigger. Also, the resistor and capacitor should be as close to the device pins as possible, to minimize stray capacitance and noise pickup. In this application, these can affect the one-shots' time constants.

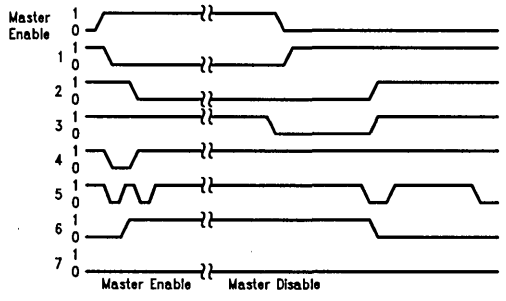
The first one-shot's resistor value is adjustable with a 50K trim pot to adjust the output pulse width. This one-shot is triggered on power-up, or by a valid line state change. Its output triggers the next two one-shots. The one-shot's output pulse is set wide enough to mask out the second pulse, caused when the data line on the other side of the repeater becomes active. When one side becomes active, a pulse is genered at point 5, triggering the first one-shot. When the repeater is enabled, the repeater drives the other side of the line. The newly active side of the line generates a second pulse, as it has changed from inactive to active. The second pulse at point 5 retriggers the first one-shot, preventing a new clock pulse. Consequently, the second and third one-shots aren't triggered.

The output of the second one-shot disables both repeater enable lines for about 200 ns. This disable inserts a minimum inactive state between every repeater direction switch, preventing it from toggling. After the minimum interval, however, the repeater can change direction. The third one-shot generates the D flip-flop clock pulse upon a valid line state change. The fourth one-shot sends an error signal to disable the repeater. The error occurs when the repeater isn't enabled between the time that one side of the transmission line becomes active and the time the other side becomes active. This scenario is also a collision, and is related to the propagation delay of the local control circuit. In this case, the enables to the repeater are kept off.

Block e filters and converts a valid line state change into a pulse, which triggers the first one-shot. The first low-pass filter cleans up spikes from the output of the line-sense circuits. Spikes appear from the difference in switching thresholds between receivers in the sense circuit. For a short time, receiver outputs are in the same state, causing a glitch at points 1 and 2 on every other signal transition. The width of the spikes depends on the data line signal transition time. For a short line, the data line capacitance is small, the signal transitions are fast, and the pulses out of the LS08 are very narrow. In most applications, though, the data line between repeaters is long, so transition time is much slower. In this case, the pulses at the LS08 output are wider. These pulses must be filtered out before they mislead the repeater into switching direction.

The first low-pass filter performs this function, with component values for a repeater linking two 1000-meter cable segments and a data rate of 200 kbaud. This filter also controls the length of time required to enable and disable the repeater. The difference between these two times is the delay of the low-pass filter. The enable time—375 ns from LS04 output to LS132 output—is shorter than the disable time—about 3.5 μs—because during enable, the capacitor charges through the diode *(Figure 5)*.

The final block masks the enable bits to the repeater when the second one-shot is triggered by the first. A latch holds the repeater direction enable bits when a valid line change has occurred. The enable lines are automatically masked for 200 ns, guaranteeing return to the inactive state and disabling the repeater when the D flip-flops are changing states.



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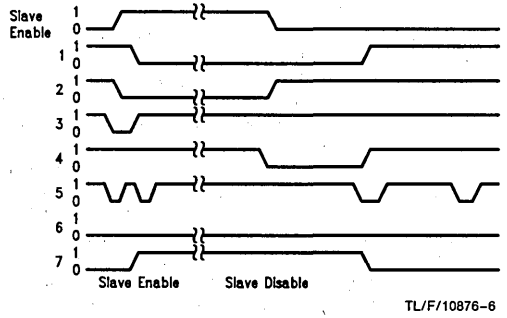

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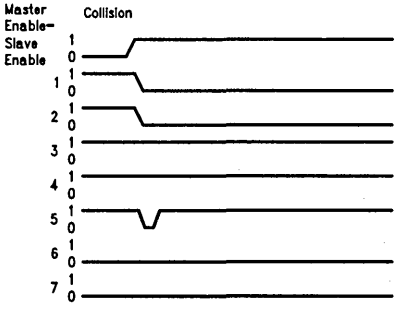

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FIGURE 5. Signals at different points in the circuit vary according to the data line conditions. There are five possible cases: Master Enable, Master Disable, Slave Enable, Slave Disable, and Collision (master and slave attempting to enable simultaneously).

To understand the timing in the master enable case, assume the master is located on the left side of the repeater and the slave on the right (*Figure 4,* again). First, both lines on either side of the repeater are inactive. The line-sense circuit outputs are high and Enables 6 and 7 are low. Next, the master drives the line high. The rising-edge line ME is the driving master's enable line. As soon as the master drives the line high, the sense circuit on the master side detects an active line state. The output of the LS08 gate pulls low, indicating the inactive-to-active state change. Lines 3 and 4 show the D flip-flop input signals. When 4 is low, the repeater is enabled in the master-to-slave direction.

On line 5, two pulses appear. The first occurs when the master side of the line changes from inactive to active. The first one-shot is triggered, generating a clock pulse. The D flip-flop latches its inputs and one repeater driver is enabled. Line 7 stays low, disabling the repeater in the direction towards the master. Line 6 becomes enabled, as a result of the master side becoming active first. The pulse created when the slave side becomes active is the second pulse on line 5. The second pulse doesn't generate a clock pulse; it retriggers the first one-shot. This one-shot can be adjusted so that the second pulse occurs within the output pulse of the first trigger. This guarantees that a new clock pulse won't be generated and keeps the repeater enabled in the same direction.

When the master has completed transmission, it is disabled and lets go of the line. The line-sense circuit detects the state change, data is latched into the D flip-flops, and enable lines 6 and 7 are pulled low.

In the slave enable case the same timing cycle takes place, with the roles of sense lines 1 and 2 and enable lines 6 and 7 reversed. When collision occurs, lines 3 and 4 stay high and neither direction is enabled. The line-sense circuits on both sides of the repeater detect a state change—from inactive to active—upon collision. The logic in block c, however, keeps the repeater disabled. The second pulse usually seen on line 5 doesn't occur, because the repeater is disabled in both directions. Both sides must return to the inactive state before the repeater can be enabled again in either direction.

Comparing EIA-485 and EIA-422-A Line Drivers and Receivers in Multipoint Applications

National Semiconductor
Application Note 759
John Goldie

INTRODUCTION

EIA-485 is a unique interface standard because, of all the EIA Standards, only EIA-485 allows for multiple driver operation. At first glance EIA-485 and EIA-422-A appear to be very similar. Thus, EIA-485 is commonly confused with EIA-422-A. EIA-485 components (drivers and receivers) are backward compatible with EIA-422-A devices and may be interchanged. However, EIA-422-A drivers should not be used in EIA-485 applications. This application note describes the differences between EIA-422-A and EIA-485 devices.

EIA-422-A drivers face three major problems if they are used in multipoint (multiple driver) applications. The first deals with the common mode range of the drivers. The TRI-STATE® common mode range for a EIA-422-A driver is −250 mV to +6V. If a ground potential difference exists between drivers as shown in *Figure 1,* the disabled driver can come out of its high impedance state and clamp the line to one diode drop below ground. The second problem deals with contention between active drivers. Faults may occur that cause two drivers to be enabled at the same time. If this happens and the drivers are in opposite states, high currents will flow between devices. The maximum package power dissipation ratings for the devices can be easily exceeded, thermally damaging the devices. The third problem deals with drive current. For bi-directional data flow, the line should be terminated with a resistor at both ends of the cable. Therefore drivers are required to source/sink twice the current required by an EIA-422-A termination (single resistor).

PROBLEM #1—COMMON MODE RANGE

A typical bipolar EIA-422-A output structure is shown in *Figure 2.* Associated with the classical totem pole output structure is the parasitic substrate diode formed between the EPI layer and the substrate. This parasitic diode limits the negative common mode range of the driver's output. Given the case when the driver on the left is disabled (high impedance state), the driver on the right is active, and the two drivers are referenced to local grounds a fault can occur. If a ground potential difference exists between the two grounds (V_{CM}), the disabled driver can clamp the line. An example of this occurs when the disabled driver's ground is two volts higher in potential than the active driver's ground. If the output voltage goes below its ground by one diode drop, the parasitic diode becomes forward biased. For this example, assume a V_{OL} of 0.5V, and a V_{CM} of +2V. The active driver's V_{OL} is 0.5V, but with respect to the disabled driver's ground it becomes −1.5V. Clearly the EPI/SUB diode is forward biased and the line is clamped to −0.7V instead of the driven level. Data flow is not guaranteed, if the line is clamped. EIA-485 driver output structures, shown in *Figure 3,* include a Schottky diode in both the source and sink side of the output structure. This diode isolates the EPI/SUB diode from the output pin, and eliminates the possibility of the parasitic diode from turning on and clamping the data line. The common mode range is now −7V to +12V (7V from either rail). The adverse affects of this diode are minimal. The driver's V_{OL} is a Schottky diode drop higher, and V_{OH} is one diode drop lower. However, the driver's output will remain in a high impedance state for applied voltages between −7V and +12V.

PROBLEM #2—CONTENTION BETWEEN DRIVERS

If by hardware or software error two drivers are enabled at the same time, a fault occurs. In applications that use multiple drivers, protection from this fault should be considered. This fault can be more damaging to the drivers if the two active drivers are separated by a large ground potential difference. For example, transceiver one (T1) shown in *Figure 1* is referenced to earth ground GND1 (0V). While T2's ground potential (GND2) is 7V higher in magnitude with respect to GND1. If the two drivers are in opposite states, then a 12V difference exists between the drivers (12V = V_{CM} + V_{CC}). A large current will flow, and the maximum package power dissipation rating would be exceeded. EIA-422-A drivers do not have contention protection built in, since they are intended for use in single driver/multiple receiver applications. Power dissipation increases if multiple drivers are involved. EIA-485 line drivers are protected from this contention problem through the use of short circuit cur-

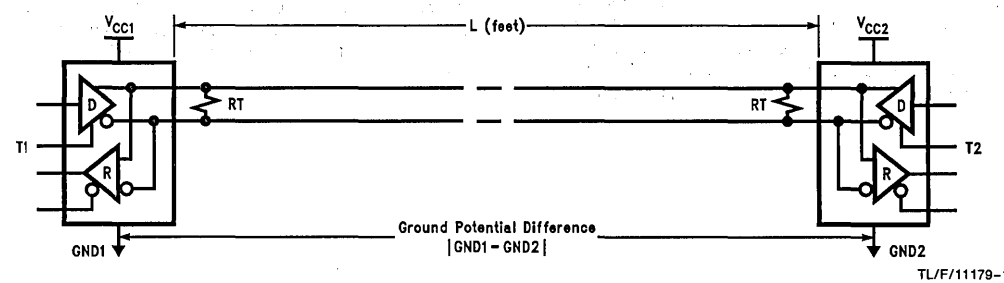

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FIGURE 1. Typical Multiple Driver Application

rent limiting over a wide common mode range. Most EIA-485 drivers have a thermal shutdown feature (although not required by EIA-485). If an active EIA-485 driver output is shorted to any voltage between −7V and +12V, the resulting current will be less than 250 mA. Realizing that drivers can be thermally damaged, ALL National Semiconductor's EIA-485 drivers feature thermal shutdown protection (TS). For example, a worse case fault occurs if the driver is shorted to +12V, and the resulting current is 250 mA. The power dissipated on the device is simply current multiplied by voltage (P=IV): 12V (250 mA) = 3W. Three watts clearly exceeds the rated maximum package power dissipation specification for all common packages. However, the thermal shutdown feature senses this fault and disables the drivers output. Hence, the 250 mA current drops to 0 mA; the device cools down and is automatically reset. If the fault is still present, the device will cycle into and out of thermal shutdown until the fault is removed. Some of National's devices feature an open collector pin that reports the occurrence of a thermal shutdown (DS3696 for example). EIA-422-A drivers would commonly incur damage when this fault occurs.

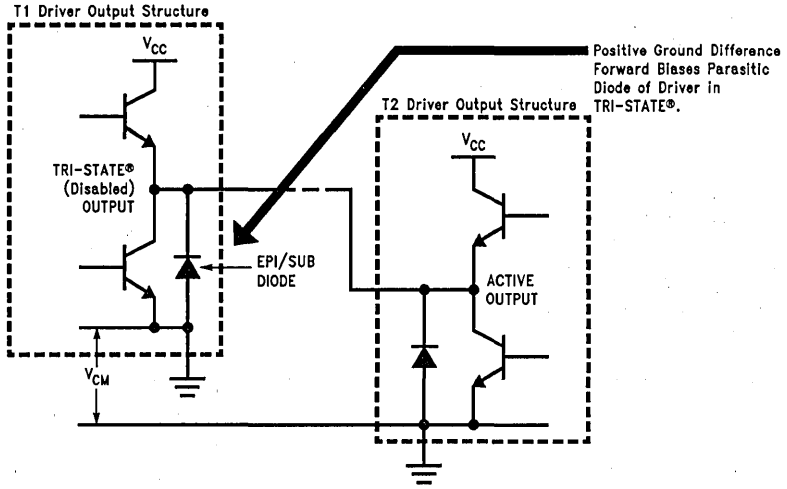

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FIGURE 2. EIA-422-A Driver Output Structures Have A Limited Common Mode Range

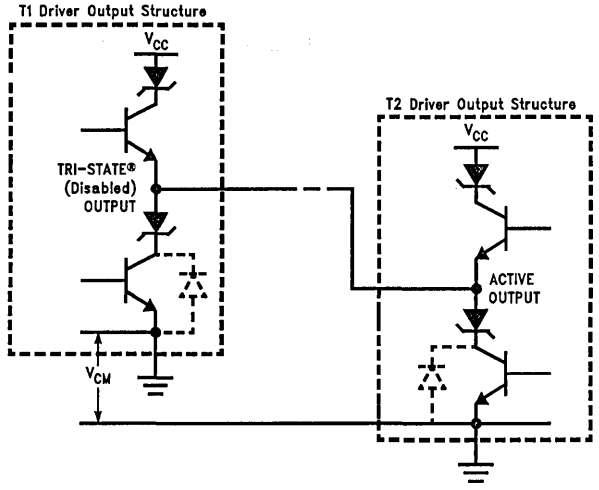

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FIGURE 3. EIA-485 Driver Output Supports −7V to +12V Common Mode Range

PROBLEM #3—DRIVE CURRENT

The third problem deals with the drivers load current capability. EIA-422-A drivers are rated at ±20 mA minimum, while EIA-485 devices have ±55 mA minimum drive capability. Current sourced by the driver either flows through the termination resistor(s), or into receiver input structures. In multiple driver applications, two termination resistors (RT) are required (one at each end of the cable), a driver would see these two resistors in parallel, resulting in a 60Ω load (assuming the termination resistors are 120Ω each). Receiver input structures are also seen in parallel by the driver, and the EIA-422-A receiver input impedance is also too low to be used in applications requiring a high number of receivers. To overcome these problems EIA-485 drivers have roughly three times the drive capability of EIA-422-A drivers. In addition EIA-485 receivers feature a higher input impedance, which is typically three times the EIA-422-A limit of 4 kΩ.

CONCLUSIONS

EIA-485 drivers are the best choice for multipoint (multiple driver) applications as shown in *Figure 4.* They can tolerate ground potential differences of up to 7V from either rail. They are contention safe and thermally protected. Finally, the drivers can handle up to 32 transceiver loads compared to EIA-422-A's limit of ten receivers. National offers a wide range of EIA-485 devices: Transceivers, Repeaters, Quad Drivers, Quad Receivers and Quad Transceivers are all offered. Select devices are available in the Industrial and Military temperature ranges. National also offers MIL-883C qualified Quad Drivers, Quad Receivers and Transceiver (see the selection guide located in the front of chapter one of the Interface Databook for a complete listing of all EIA-485 Devices).

REFERENCES

1. EIA Standard EIA-485 (RS-485), Standard for Electrical Characteristics of Generators and Receivers for use in a Balanced Digital Multipoint Systems, EIA, Washington, D.C.
2. EIA Standard EIA-422-A (EIA RS-422-A), Electrical Characteristics of Balanced Voltage Digital Interface Circuits, EIA, Washington, D.C.
3. Application Note 409, Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard, Interface Databook, National Semiconductor, Santa Clara, CA.

EIA Standards can be obtained for a fee from:

Electronic Industries Association
EIA Engineering Department/Standard Sales Office
2001 Pennsylvania Avenue, N.W.
Washington, D.C. 20006
Tel: (202) 457-4988

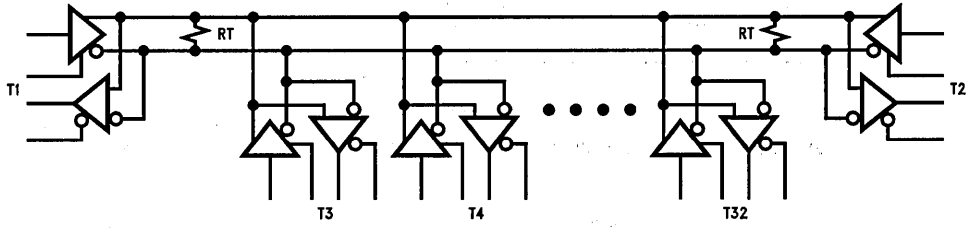

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FIGURE 4. Typical EIA-485 Multipoint Application

Calculating Power Dissipation for Differential Line Drivers

National Semiconductor
Application Note 805
Joe Vo

INTRODUCTION

In many board and system level designs, it is often necessary to determine the total power dissipated by the individual components of that application. This determination of total device power dissipation is important for two reasons. First, it can be used to select the power supply best suited to satisfy the needs of the application. And second, a power dissipation calculation facilitates the analysis of how the board or system's operating conditions might adversely affect the reliability of, or otherwise damage, the on board components.

The purpose of this application note is to provide end users with a sample power dissipation calculation for typical TIA/EIA-422 and TIA/EIA-485 differential line drivers. Other topics which will be addressed by this application note include worst case power dissipation, and packaging/thermal considerations.

CONTRIBUTIONS TO TOTAL DEVICE POWER DISSIPATION

Under normal operating conditions, the total device power dissipation is determined primarily by output load current and quiescent current. These current terms are modified by external loading conditions, device switching frequency, power supply voltage and ambient operating temperature. The following discussion of device power dissipation will take all these factors into consideration.

The power dissipated by a device in its quiescent state and that dissipated by the outputs when the device is switching constitute the primary contributions to total device power dissipation. Quiescent power dissipation is defined as the product of power supply voltage (V_{CC}) and power supply current (I_{CC}).

(1) $$PD_{QUIESCENT} = (V_{CC})(I_{CC})$$

The power dissipation by the outputs, takes into account the power dissipated by the output structures of the device when the outputs are driving a load. When the device output is in the LOW state, the output sinks a sufficient amount of load current to develop a V_{OL} with respect to ground. Conversely, when the device output is in the HIGH state, the output sources a load current sufficient to develop a V_{OH} with a respect to ground. The power dissipated, then, by a single channel is:

(2) $$PD_{OUTPUT} = I_{OH}(V_{CC} - V_{OH}) + I_{OL}(V_{OL})$$

where, I_{OH} = HIGH level output current
I_{OL} = LOW level output current

The general expression to describe the dissipated power for all outputs is:

(3) $$PD_{OUTPUTS} = (\#\text{ of channels})\,[I_{OH}(V_{CC} - V_{OH} + I_{OL}(V_{OL}))]$$

Together, the sum of quiescent power dissipation and power dissipation at the device outputs approximates the total power dissipated by the device.

(4) $$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$

A more comprehensive total device power dissipation calculation, however, might also incorporate the contribution to device power dissipation from the device's switching frequency. Therefore, Equation (4) could be changed to look like the following.

(5) $$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS} + C_{OUT}(V_{CC})^2(f)$$

where, C_{OUT} = device output capacitive load
f = device switching frequency

For this application note, the last term of Equation (5) was intentionally omitted. These are several reasons for this omission. First, switching frequency does not lend itself well to this general discussion of power dissipation since it varies from application to application. Second, in terms of the quiescent and output power dissipation components, the magnitude of the CV^2f term on total device power dissipation is negligibly small for most line drivers. And third, *Figure 1* demonstrates that switching frequency will not heavily impact quiescent device power dissipation (see Equation 1) since the magnitude of the change in I_{CC} due to switching frequency is small.

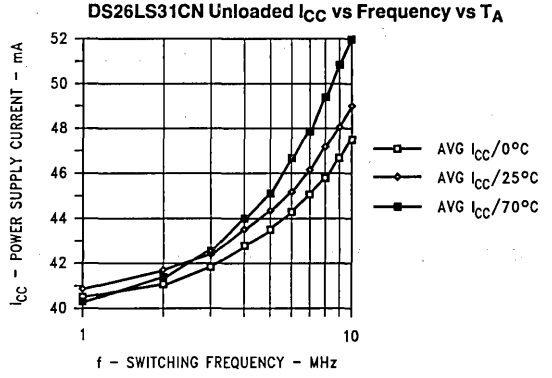

FIGURE 1. Supply Current vs Switching Frequency vs Temperature

TYPICAL POWER DISSIPATION CALCULATIONS USING THE DS26LS31CN

To better illustrate a total power dissipation calculation in a typical TIA/EIA-422 application, consider the DS26LS31CN (molded DIP package) Quad Differential Line Driver operating under following conditions:

V_{CC} = 5.0V
Ambient Operating Temperature = 25°C
Switching Frequency = 1 MHz
Duty Cycle = 50%
Measured V_{OH} = 3.2V
Measured V_{OL} = 0.3V
Termination Resistor = 100Ω

Figure 2 indicates that the I_{CC} typically associated with a V_{CC} of 5.0V, at room temperature, is approximately 39 mA. *Figure 1* indicated that a device, operating at room temperature, switching at 1 MHz will generate an I_{CC} of approximately 41 mA. Note in both *Figures 1* and *2* that the change in I_{CC} with respect to switching frequency and the change in I_{CC} with respect to V_{CC}, respectively, is rather small. Also note that in both figures there is little I_{CC} dependence on temperature.

For this typical calculation, 41 mA will be used for $I_{CCtypical}$ since it is a better representation of actual device operating conditions.

From (1), the static power dissipation is:

$$PD_{QUIESCENT} = (V_{CCtypical}\ (I_{CCtypical}) = (5.0V)\ (41.0\ mA) \doteq 205.0\ mW$$

Given that the measured V_{OH} is 3.2V, one can extract the corresponding I_{OH} from *Figure 3*. The I_{OH} required to develop a V_{OH} of 3.2V is approximately 30 mA.

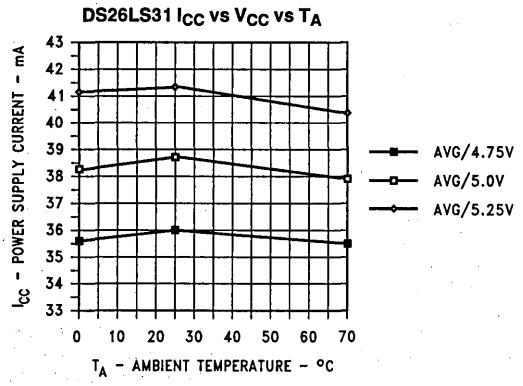

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FIGURE 2. Supply Current vs Supply Voltage vs Temperature

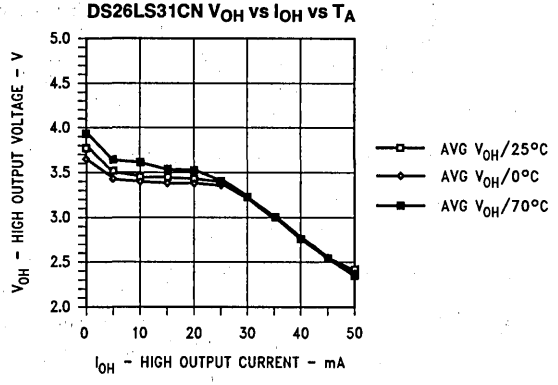

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FIGURE 3. High Output Voltage vs High Output Current vs Temperature

From *Figure 4*, one can likewise obtain an I_{OL} of approximately 30 mA given a measured V_{OL} of 0.3V.

The outputs, then, of the DS26LS31CN dissipate power according to the following relationship:

$$PD_{OUTPUTS} = (\#\text{ of Channels})\,[I_{OH}(V_{CC} - V_{OH}) + I_{OL}(V_{OL})]$$
$$= (4)\,[30\text{ mA}(5.0V - 3.2V) + 30\text{ mA}(0.3V)]$$
$$= (4)\,[54.0\text{ mW} + 0.9\text{ mW}]$$
$$= 252.0\text{ mW}$$

From the given typical operating conditions, the total power dissipated by the DS26LS31CN is:

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$
$$= 205.0\text{ mW} + 252.0\text{ mW}$$
$$= 457.0\text{ mW}$$

WORST CASE POWER DISSIPATION CALCULATIONS

While a typical power dissipation calculation is informative, a board or system level designer will invariably be forced to also perform a worst case calculation. With the exception of several minor changes, the same procedure is followed for both typical and worst case power dissipation calculations.

Starting with static power dissipation, this calculation must now use the maximum values for both power supply voltage (V_{CCmax}) and power supply current (I_{CCmax}). The I_{CCmax} used is normally that specified by the data sheet. However, if the application were to force the device beyond its 10 MHZ operating window, the I_{CCmax} could exceed the data sheet specifications of 60 mA (see *Figure 1*). In either case, the larger current value must be used for I_{CCmax} in the worst case quiescent power calculation.

The next step is to calculate the power dissipation from the device outputs. To do so, place the device under the worst case board or system conditions, and measure the resulting V_{OH} and V_{OL} levels. Given these worst case V_{OH} and V_{OL} values, one can extract the corresponding worst case I_{OH} and I_{OL} values with the help of *Figures 3* and *4*, respectively. A substitution of these values into Equation (3) will then yield the worst case power dissipation due to the device outputs.

An alternative method to calculate the power dissipated by the device outputs requires that a differential output voltage versus output current (V_{OD} vs I_O) curve be generated. Keeping in mind that $V_{OD} \equiv V_{OH} - V_{OL}$, a V_{OD} vs I_O curve can be developed by "subtracting" the V_{OL} vs I_{OL} curve from the V_{OH} vs I_{OH} curve. On the resulting V_{OD} vs I_O curve, draw a load line corresponding to the worst case loading conditions. This will then yield the output differential voltage and output currents being sourced and sunk by the device under a worst case loading condition. A substitution of these quantities into Equation (6) will yield the power being dissipated by the device outputs.

(6) $$PD_{DIFFERENTIAL\,OUTPUTS} = (\#\text{ of channels})\,[I_O(V_{CC} - V_{OD})]$$

As an example, consider the output voltage versus output current curves previously given for the DS26LS31CN (*Figures 3* and *4*). The V_{OD} vs I_O curve for the DS26LS31CN, as illustrated in *Figure 5*, can be drawn by "subtracting" *Figure 4* from *Figure 3*.

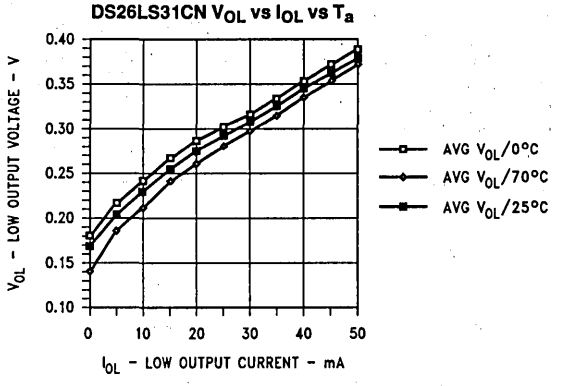

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FIGURE 4. Low Output Voltage vs Low Output Current vs Temperature

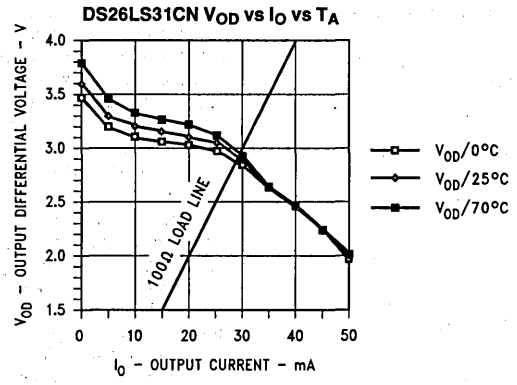

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FIGURE 5. Output Differential Voltage vs Output Current vs Temperature

A sample worst case load line of 100Ω superimposed upon *Figure 5* reveals the corresponding worst case operating point for the DS26LS31CN; that is, it reveals the device's output differential voltage and output current given a sample worst case output load. When substituted into Equation (6), these voltage and current quantities will yield the worst case power dissipation at the device outputs.

The sum of the worst case quiescent and output power dissipation components will approximate the total worst case device power dissipation.

POWER CALCULATION FOR TIA/EIA-485 DIFFERENTIAL LINE DRIVERS

Let's first compare a typical TIA/EIA-422 output structure to a typical TIA/EIA-485 output structure. As shown in *Figure 6*, the presence of Schottky diodes in the output stage of an TIA/EIA-485 device clearly differentiates it from a similar TIA/EIA-422 device. The addition of the Schottky diodes to the TIA/EIA-485 output stage enable it to safely operate in multipoint (multiple driver) applications over a −7V to +12V common mode range versus the −250 mV to +6V common mode range of TIA/EIA-422. However, the Schottky diodes in the TIA/EIA-485 outputs have the net effect of raising the value of V_{OL} by one diode drop and decreasing the value of V_{OH} by the same amount. This change in output voltage levels will, in turn, affect the amount of power being dissipated in the output stage.

Despite the fact that the output structure of an TIA/EIA-422 line driver differs from that of the TIA/EIA-485 line driver, the procedure outlined earlier to calculate power dissipation is applicable for both TIA/EIA-422 devices and TIA/EIA-485 devices. Quiescent and output power dissipation calculations for an TIA/EIA-485 line driver will again employ Equations (1) and (3) respectively.

As with the sample power calculation for the TIA/EIA-422 device, the sum of the quiescent and output power components will yield the total approximated power dissipated by the TIA/EIA-485 device.

As an example, consider the worst case power dissipation of the DS96F172CJ (ceramic DIP package). Other than the fact that the DS96F172CJ is an TIA/EIA-485 device, it is pin for pin compatible with the DS26LS31CN. As outlined earlier, the first step is to calculate the quiescent power dissipa-

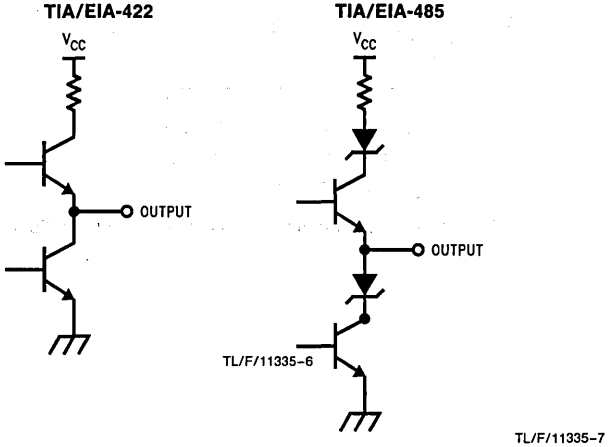

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FIGURE 6. TIA/EIA-422 and TIA/EIA-485 Output Structures

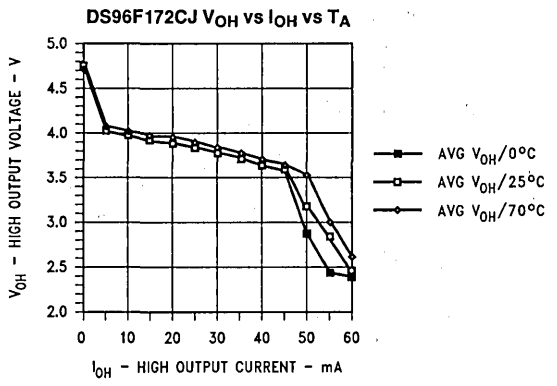

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FIGURE 7. High Output Voltage vs High Output Current vs Temperature

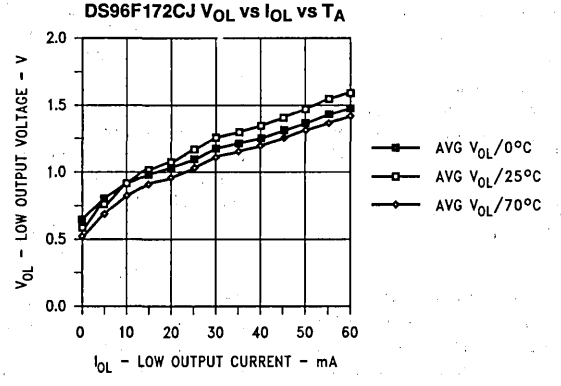

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FIGURE 8. Low Output Voltage vs Low Output Current vs Temperature

tion. From Equation (1), the worst case quiescent power dissipation is:

$$PD_{QUIESCENTmax} = (V_{CCmax})\,(I_{CCmax})$$
$$= (5.25V)\,(50\ mA)$$
$$= 262.5\ mW$$

The next step is to calculate the power dissipated at the device outputs under a worst case load condition. Again, there are two ways to do this. First, one can measure the worst case output voltage levels and reference them with *Figures 7* and *8* to extract the corresponding worst case output currents.

A substitution of these resulting quantities into Equation (3) will yield the power dissipated at the device outputs given a worst case load. The second method to calculate output power dissipation involves drawing a worst case load line on the differential output voltage versus output current curve. In the case of the DS96F172CJ, the worst case load line is assumed to be 60Ω. This assumption was made because in a typical TIA/EIA-485 application, both ends of the transmission line are terminated with 120Ω and so the TIA/EIA-485 driver is effectively loaded with 60Ω. In *Figure 9* a 60Ω load line has been superimposed upon the differential output versus output current curve and consequently, worst case values of output current and differential output voltage (under the given load) have been obtained.

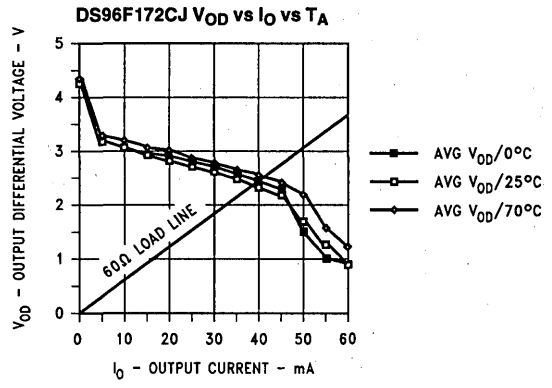

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FIGURE 9. Output Differential Voltage vs Output Current vs Temperature

At room temperature, the worst case power dissipation at the device outputs is (from Equation (6)):

$$PD_{DIFFERENTIAL\ OUTPUTS} = (\#\ \text{of channels})\ [I_O\ (V_{CC} - V_{OD})]$$
$$= (4)\ [39\ mA\ (5.25V - 2.4V)]$$
$$= 444.6\ mW$$

The only remaining task is to sum together the quiescent and output power dissipation terms to obtain a total worst case power dissipation. From (4), the DS96F172CJ operating at room temperature, under a worst case load of 60Ω, will dissipate:

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$
$$= 262.5\ mW + 444.6\ mW$$
$$= 707.1\ mW$$

PACKAGING AND THERMAL CONSIDERATIONS

Having calculated the total power dissipated by the device, the next logical step is to ascertain that the power dissipated does not thermally damage the device. To do so, the following equation is used:

(7) $T_J = [PD_{TOTAL}(\theta_{JA})] + T_A$

where, θ_{JA} = Thermal Resistance from Junction to Ambient (°C/W)

PD_{TOTAL} = Total Power Dissipated by Device (W)

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The only variable which remains unknown is θ_{JA}. θ_{JA} information for the available package types of most devices can be found in the respective device's data sheet. Keep in mind that the data sheet often refers to θ_{JA} in terms of derate factors. Determining θ_{JA} involves taking the inverse of the derate factor.

(8) θ_{JA} = 1/Derate Factor

For example, all the information is now available for a sample calculation of the DS26LS31CN's junction temperature using the operating conditions specified earlier. The data sheet of the DS26LS31CN specifies a derate factor, for the plastic DIP package, of 11.9 mW/°C. From (8), the θ_{JA} is:

$$\theta_{JA} = 1/\text{Derate Factor}$$
$$= 1/(0.0119\ W/°C)$$
$$= 84.0\ °C/W$$

The thermal resistance from junction to ambient for the DS26LS31CN is now known. Also known are the ambient operating temperature and the total power dissipated (obtained earlier). From (7), the junction temperature is:

$$T_J = [(PD_{TOTAL})\ (\theta_{JA})] + T_A$$
$$= [(0.457W)\ (84.0°C/W)] + 25°C$$
$$= 63.4°C$$

The maximum allowable junction temperature for plastic DIP packages is 150°C. The junction temperature of the DS26LS31CN operating under the conditions specified earlier, by the typical power dissipation calculation, is well within the allowed maximum. Applications where the maximum

allowable junction temperature is exceeded should be avoided since this condition may thermally damage the device and package.

Looking at this thermal analysis from a slightly different perspective, Equation (7) can be rewritten as:

(9) $PD_{PACKAGEmax} = (T_{Jmax} - T_A)/\theta_{JA}$

By substituting 150°C for the maximum allowable junction temperature, the maximum allowable package power dissipation at 25°C can be calculated using the θ_{JA} for the DS26LS31CN plastic DIP (N) package.

$$PD_{PACKAGE_{max\ @\ 25°C}} = (T_{Jmax} - T_A)/\theta_{JA}$$
$$= (150°C - 25°C)/84.0°C/W$$
$$= 1.48W$$

To calculate the maximum allowable package power dissipation at 70°C, the 1.48W maximum at 25°C must be derated using the following procedure:

(10) $PD_{PACKAGE_{max\ @\ 70°C}} =$
$PD_{PACKAGEmax\ @\ 25°C} - (\text{Derate})\ (\Delta T_A)$
$= 1.48W - (0.0119W/°C)$
$(45°C)$
$= 0.94W$

This sample calculation illustrates that as ambient temperature increases, the DS26LS31CN is able to dissipate less power before the maximum allowable junction temperature specification is violated. Keep in mind that this thermal analysis also applies to TIA/EIA-485 devices such as the DS96F172CJ.

It should be noted that this general thermal analysis is applicable to all other packages and device types assuming that the maximum power dissipation and θ_{JA} are known.

SUMMARY

A method for calculating the total power dissipated by an TIA/EIA-422 driver was presented. This method is also applicable to similar devices conforming to the TIA/EIA-485 standard. Samples calculations for the DS26LS31CN and the DS96F172CJ were presented. Worst case considerations were also discussed. And finally, the relationship between power dissipation and thermal/packaging limitations was introduced.

SPECIAL NOTES

Figure 1: Ten samples from three data codes.

Figure 2: Ten samples from three data codes. Outputs unloaded and V_{CC} = 5.0V.

Figures 3, 4, 5: Ten samples from three date codes.
V_{CC} = 5.0V

Figures 7, 8, 9: Ten samples from two date codes.
V_{CC} = 5.0V

The graphical data referenced in this application note are not intended to guarantee performance as they only represent typical values.

REFERENCES

HC-CMOS Power Dissipation, K. Karakotsios, National Semiconductor, 1988 CMOS Logic Data Book, Application Note AN-303.

Understanding Integrated Circuit Package Power Capabilities, C. Carinalli and J. Huljev, National Semiconductor, 1990 Interface Data Book, Application Note AN-336.

Data Transmission Lines and Their Characteristics

National Semiconductor
Application Note 806
Kenneth M. True

OVERVIEW

This application note discusses the general characteristics of transmission lines and their derivations. Here, using a transmission line model, the important parameters of characteristics impedance and propagation delay are developed in terms of their physical and electrical parameters. This application note is a revised reprint of section two of the Fairchild Line Driver and Receiver Handbook. This application note, the first of a three part series (see AN-807 and AN-808), covers the following topics:

- Transmission Line Model
- Input Impedance of a Transmission Line
- Phase Shift and Propagation Velocity for the Transmission Line
- Summary—Characteristics Impedance and Propagation Delay

INTRODUCTION

A data transmission line is composed of two or more conductors transmitting electrical signals from one location to another. A parallel transmission line is shown in *Figure 1*. To show how the signals (voltages and currents) on the line relate to as yet undefined parameters, a transmission line model is needed.

TRANSMISSION LINE MODEL

Because the wires A and B could not be ideal conductors, they therefore must have some finite resistance. This resistance/conductivity is determined by length and cross-sectional area. Any line model, then, should possess some series resistance representing the finite conductivity of the wires. It is convenient to establish this resistance as a per-unit-length parameter.

Similarly, the insulating medium separating the two conductors could not be a perfect insulator because some small leakage current is always present. These currents and dielectric losses can be represented as a shunt conductance per unit length of line. To facilitate development of later equations, conductance is the chosen term instead of resistance.

If the voltage between conductors A and B *is not variable* with time, any voltage present indicates a static electric field between the conductors. From electrostatic theory it is known that the voltage V produced by a static electric field E is given by

$$V = \int E \bullet dl \qquad (1)$$

This static electric field between the wires can only exist if there are free charges of equal and opposite polarity on both wires as described by Coulomb's law.

$$E = \frac{q}{4\pi\epsilon r^2} \qquad (2)$$

where E is the electric field in volts per meter, q is the charge in Coulombs, ϵ is the dielectric constant, and r is the distance in meters. These free charges, accompanied by a voltage, represent a capacitance (C = q/V); so the line model must include a shunt capacitive component. Since total capacitance is dependent upon line length, it should be expressed in a capacitance per-unit-length value.

It is known that a current flow in the conductors induces a magnetic field or flux. This is determined by either Ampere's law

$$\int H \bullet dl = I \qquad (3)$$

or the Biot-Savart law

$$dB = \frac{\mu I dl \times r}{4\pi r^3} \qquad (4)$$

where r = radius vector (meters)
l = length vector (meters)
I = current (amps)
B = magnetic flux density (Webers per meter)
H = magnetic field (amps per meter)
μ = permeability

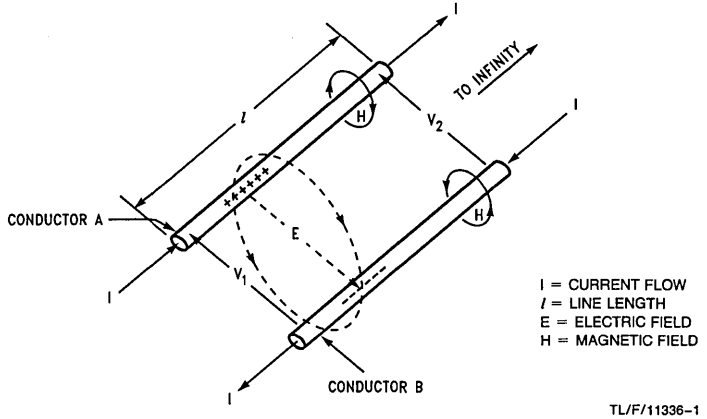


FIGURE 1. Infinite Length Parallel Wire Transmission Line

If the magnetic flux (ϕ) linking the two wires *is variable* with time, then according to Faraday's law

$$V = \frac{d\phi}{dt} \quad (5)$$

A small line section can exhibit a voltage drop—in addition to a resistive drop—due to the changing magnetic flux (ϕ) within the section loop. This voltage drop is the result of an inductance given as

$$V = L\frac{di}{dt} \quad (6)$$

Therefore, the line model should include a series inductance per-unit-length term. In summary, it is determined that the model of a transmission line section can be represented by two series terms of resistance and inductance and two shunt terms of capacitance and conductance.

From a circuit analysis point of view, the terms can be considered in any order, since an *equivalent* circuit is being generated. *Figure 2* shows three possible arrangements of circuit elements.

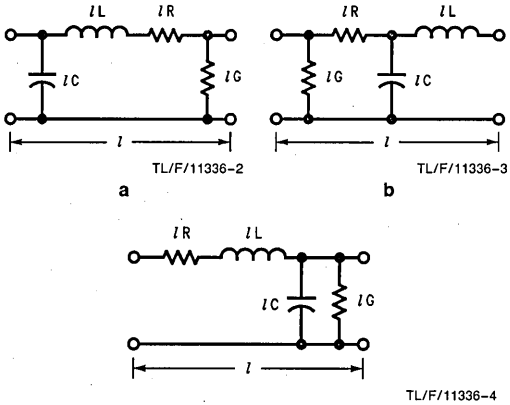


FIGURE 2. Circuit Elements

For consistency, the circuit shown in *Figure 2c* will be used throughout the remainder of this application note. *Figure 3* shows how a transmission line model is constructed by series connecting the short sections into a ladder network.

Before examining the pertinent properties of the model, some comments are necessary on applicability and limitations. A *real* transmission line does not consist of an infinite number of small lumped sections—rather, it is a distributed network. For the lumped model to accurately represent the transmission line (see *Figure 3*), the section length must be quite small in comparison with the shortest wavelengths (highest frequencies) to be used in analysis of the model. Within these limits, as differentials are taken, the section length will approach zero and the model should exhibit the same (or at least very similar) characteristics as the actual distributed parameter transmission line. The model in *Figure 3* does not include second order terms such as the increase in resistance due to skin effect or loss terms resulting from non-linear dielectrics. These terms and effects are discussed in the references rather than in this application note, since they tend to obscure the basic principles under consideration. For the present, assume that the signals applied to the line have their minimum wavelengths a great deal longer than the section length of the model and ignore the second order terms.

INPUT IMPEDANCE OF A TRANSMISSION LINE

The purpose of this section is to determine the input impedance of a transmission line; i.e., what amount of input current I_{IN} is needed to produce a given voltage V_{IN} across the line as a function of the LRCG parameters in the transmission line, (see *Figure 4*).

Combining the series terms *l*R and *l*L together simplifies calculation of the series impedance (Z_s) as follows

$$Z_s = l(R + j\omega L) \quad (7)$$

Likewise, combining *l*C and *l*G produces a parallel impedance Z_p represented by

$$Z_p = \frac{1}{Y_p} = \frac{1}{l(G + j\omega C)} \quad (8)$$

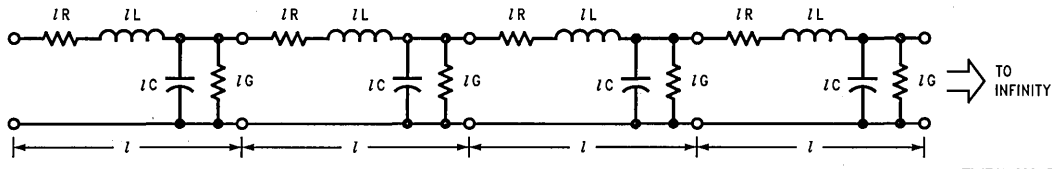


FIGURE 3. A Transmission Line Model Composed of Short, Series Connected Sections

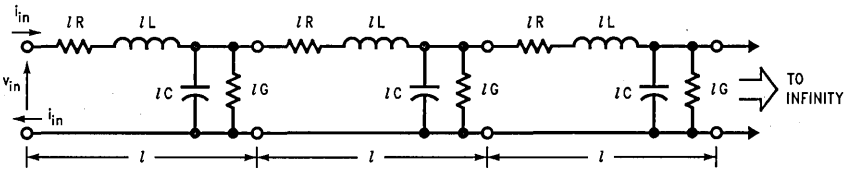
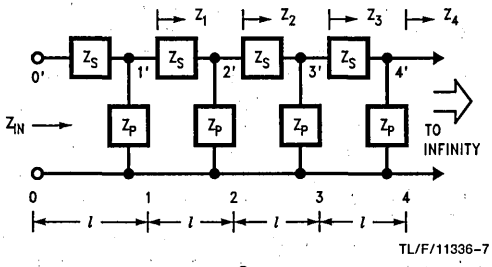


FIGURE 4. Series Connected Sections to Approximate a Distributed Transmission Line



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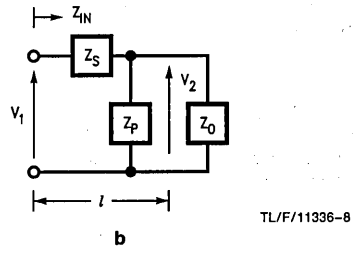


b

FIGURE 5. Cascaded Network to Model Transmission Line

Since it is assumed that the line model in *Figure 5a* is infinite in length, the impedance looking into any cross section should be equal, that is $Z_1 = Z_2 = Z_3$, etc. So *Figure 5a* can be simplified to the network in *Figure 5b* where Z_0 is the characteristic impedance of the line and Z_{in} must equal this impedance ($Z_{in} = Z_0$). From *Figure 5b*,

$$Z_{in} = Z_s + \frac{Z_0 Z_p}{Z_0 + Z_p} = Z_0 \qquad (9)$$

Multiplying through both sides by $(Z_0 + Z_p)$ and collecting terms yields

$$Z_0^2 - Z_s Z_0 - Z_s Z_p = 0 \qquad (10)$$

which may be solved by using the quadratic formula to give

$$Z_0 = \frac{Z_s \pm \sqrt{Z_s^2 + 4Z_s Z_p}}{2} \qquad (11)$$

Substituting in the definition of Z_s and Z_p from Equations 7 and 8, Equation 11 now appears as

$$Z_0 = \frac{l(R + j\omega L)}{2} \pm \frac{1}{2}\sqrt{l^2 (R + j\omega L)^2 + 4\frac{R + j\omega L}{G + j\omega C}} \qquad (12)$$

Now, as the section length is reduced, all the parameters (lR, lL, lG, and lC) decrease in the same proportion. This is because the per-unit-length line parameters R, L, G, and C are constants for a given line. By sufficiently reducing l, the terms in Equation 12 which contain l as multipliers will become negligible when compared to the last term

$$\frac{R + j\omega L}{G + j\omega C}$$

which remains constant during the reduction process. Thus Equation 12 can be rewritten as

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{Z_s Z_p} \qquad (13)$$

particularly when the section length l is taken to be very small. Similarly, if a high enough frequency is assumed,

$$\frac{\omega}{2\pi} > 100\ \text{kHz}$$

such that the ωL and ωC terms are much larger respectively than the R and G terms, $Z_s = j\omega lL$ and $Z_p = 1/j\omega l C$ can be used to arrive at a lossless line value of

$$Z_0 = \sqrt{\frac{L}{C}} \qquad (14)$$

In the lower frequency range,

$$\frac{\omega}{2\pi} \cong 1\ \text{kHz}$$

the R and G terms dominate the impedance giving

$$Z_0 = \sqrt{\frac{R}{G}} \qquad (15)$$

A typical twisted pair would show an impedance versus applied frequency curve similar to that shown in *Figure 6*. The Z_0 becomes constant above 100 kHz, since this is the region where the ωL and ωC terms dominate and Equation 13 reduces to Equation 14. This region above 100 kHz is of primary interest, since the frequency spectrum of the fast rise/fall time pulses sent over the transmission line have a fundamental frequency in the 1-to-50 MHz area with harmonics extending upward in frequency. The expressions for Z_0 in Equations 13, 14 and 15 do not contain any reference to line length, so using Equation 14 as the normal characteristic impedance expression, allows the line to be replaced with a resistor of $R_0 = Z_0\ \Omega$ neglecting any small reactance. This is true when calculating the initial voltage step produced on the line in response to an input current step, or an initial current step in response to an input voltage step.

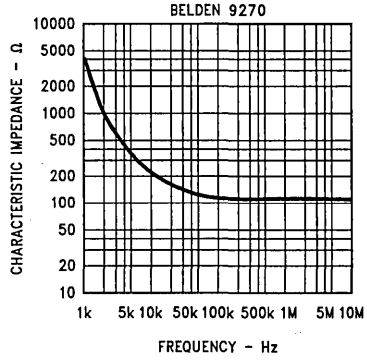


FIGURE 6. Characteristics Impedance versus Frequency

Figure 7 shows a 2V input step into a 96Ω transmission line (top trace) and the input current required for line lengths of 150, 300, 450, 1050, 2100, and 3750 feet, respectively (second set of traces). The lower traces show the output voltage waveform for the various line lengths. As can be seen, maximum input current is the same for all the different line lengths, and depends only upon the input voltage and the characteristic resistance of the line. Since $R_0 = 96\Omega$ and $V_{IN} = 2V$, then $I_{IN} = V_{IN}/R_0 \cong 20$ mA as shown by *Figure 7*.

A popular method for estimating the input current into a line in response to an input voltage is the formula

$$C(dv/dt) = i$$

where C is the total capacitance of the line (C = C per foot × length of line) and dv/dt is the slew rate of the input signal. If the 3750-foot line, with a characteristic capacitance per unit length of 16 pF/ft is used, the formula C_{total} = (C × *l*) would yield a total lumped capacitance of 0.06 μF. Using this C(dv/dt) = *i* formula with (dv/dt = 2V/10 ns) as in the scope photo would yield

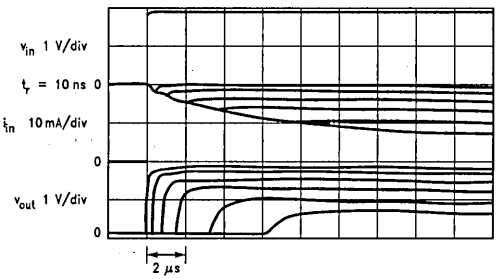
$$I = \frac{2V}{10\ ns} \times 0.06\ \mu F = 12A$$

This is clearly not the case! Actually, since the line impedance is approximately 100Ω, 20 mA are required to produce 2V across the line. If a signal with a rise time long enough to encompass the time delay of the line is used ($t_r \gg \tau$), then the C(dv/dt) = *i* formula will yield a resonable estimate of the peak input current required. In the example, if the dv/dt is 2V/20 μs ($t_r = 20\ \mu s > \tau = 6\ \mu s$), then $i = 2V/20\ \mu s \times 0.06\ \mu F = 6$ mA, which is verified by *Figure 8*.

Figure 8 shows that C(dv/dt) = *i* only when the rise time is greater than the time delay of the line ($t_r \gg \tau$). The maximum input current requirement will be with a fast rise time step, but the line is essentially resistive, so $V_{IN}/I_{IN} = R_0 = Z_0$ will give the actual drive current needed. These effects will be discussed later in Application Note 807.

PHASE SHIFT AND PROPAGATION VELOCITY FOR THE TRANSMISSION LINE

There will probably be some phase shift and loss of signal v_2 with respect to v_1 because of the reactive and resistive parts of Z_s and Z_p in the model (*Figure 5b*). Each small section of the line (*l*) will contribute to the total phase shift and amplitude reduction if a number of sections are cascaded as in *Figure 5a*. So, it is important to determine the phase shift and signal amplitude loss contributed by each section.



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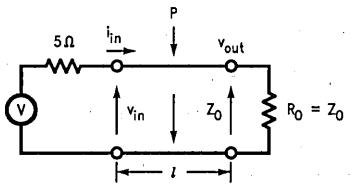

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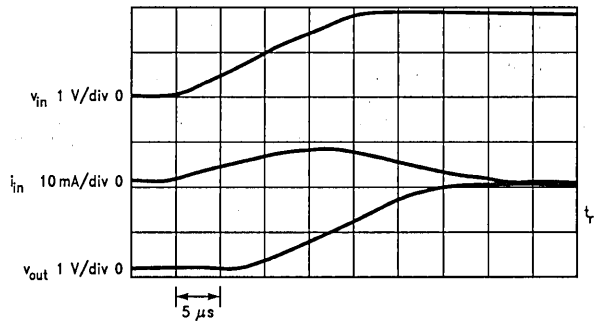
l = 150, 300, 450, 1050, 2100, 3750 ft.
24 AWG TWISTED PAIR $R_0 \cong 96\Omega$

FIGURE 7. Input Current Into a 96Ω Transmission Line for a 2V Input Step for Various Line Lengths



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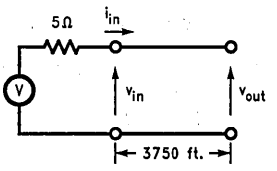

t_r = 20 μs
$R_0 = 96\Omega$, δ = 1.6 ns/ft.

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FIGURE 8. Input Current Into Line with Controlled Rise Time $t_r > 2\tau$

Using *Figure 5b*, v_2 can be expressed as

$$v_2 = v_1 \frac{Z_p Z_0}{Z_p + Z_0} \quad \frac{1}{Z_s + Z_p Z_0/(Z_p + Z_0)} \tag{16}$$

or

$$\frac{v_1}{v_2} = \frac{Z_s(Z_p + Z_0) + Z_p Z_0}{Z_p Z_0} \tag{17}$$

and further simplification yields

$$\frac{v_1}{v_2} = 1 + Z_s \left[\frac{1}{Z_0} + \frac{1}{Z_p} \right] \tag{18}$$

Remember that a per-unit-length constant, normally called γ is needed. This shows the reduction in amplitude and the change in the phase per unit length of the sections.

$$\gamma_l = \alpha_l = j\beta_l \tag{19}$$

Since

$$v_2 = v_1 \, ^{-\gamma_l} = v_1 \, ^{-\alpha_l + \nu_1 \, ^{-j\beta_l}} \tag{20}$$

where $v_1 \, ^{\alpha_l}$ is a signal attenuation and $v_1 \, ^{-j\beta_l}$ is the change in phase from v_1 to v_2,

$$ln \left[\frac{v_1}{v_2} \right] = ln \, (\alpha_l + j\beta_l) = \alpha_l + j\beta_l = \gamma_l \tag{21}$$

Thus, taking the natural log of both sides of Equation 18

$$ln \left[\frac{v_1}{v_2} \right] = ln \left[1 + Z_s \left(\frac{1}{Z_0} + \frac{1}{Z_p} \right) \right] \tag{22}$$

Substituting Equation 13 for Z_0 and Y_p for $1/Z_p$

$$\gamma_l = ln \left[1 + Z_s \left(\sqrt{\frac{Y_p}{Z_s}} + Y_p \right) \right] \tag{23}$$

Now when allowing the section length l to become small,

$$Y_p = l(G + j\omega C)$$

will be very small compared to the constant $\sqrt{Y_p/Z_s} = 1/Z_0$, since the expression for Z_0 does not contain a reference to the section length l. So Equation 23 can be rewritten as

$$\gamma_l = ln \left(1 + Z_s \sqrt{\frac{Y_p}{Z_s}} \right) = ln \, (1 + \sqrt{Y_p Z_s}) \tag{24}$$

By using the series expansion for the natural log:

$$ln \, (1 + \zeta) = \zeta - \frac{\zeta^2}{2} + \frac{\zeta^3}{3} \ldots \text{ etc.} \tag{25}$$

$$\cong \zeta \text{ for small } \zeta$$

and keeping in mind the $\sqrt{Z_s Y_p}$ value will be much less than one because the section length is allowed to become very small, the higher order expansion terms can be neglected, thereby reducing Equation 24 to

$$\gamma_l = \sqrt{Z_s Y_p} = l\sqrt{(R + j\omega L)\,(G + j\omega C)} \tag{26}$$

If Equation 26 is divided by the section length,

$$\gamma = \frac{\gamma_l}{l} = \sqrt{(R + j\omega L)\,(G + j\omega C)} \tag{27}$$

the propagation constant per unit length is obtained. If the resistive components R and G are further neglected by assuming the line is reasonably short, Equation 26 can be reduced to read

$$\gamma_l = j\beta_l = j\omega l\sqrt{LC} \tag{28}$$

Equation 28 shows that the lossless transmission line has one very important property: signals introduced on the line have a constant phase shift per unit length with no change in amplitude. This progressive phase shift along the line actually represents a wave traveling down the line with a velocity equal to the inverse of the phase shift per section. This velocity is

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} \tag{29}$$

for lossless lines. Because the LRCG parameters of the line are independent of frequency except for those upper frequency constraints previously discussed, the signal velocity given by Equation 29 is also independent of signal frequency. In the practical world with long lines, there is in fact a frequency dependence of the signal velocity. This causes sharp edged pulses to become rounded and distorted. More on these long line effects will be discussed in Application Note 807.

SUMMARY—Characteristic Impedance and Propagation Delay

Every transmission line has a characteristic impedance Z_0, and both voltage and current at any point on the line are related by the formula

$$Z_0 = \frac{v}{i}$$

In terms of the per-unit-length parameters LRCG,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Since $R \ll j\omega L$ and $G \ll j\omega C$ for most lines at frequencies above 100 kHz, the characteristic impedance is best approximated by the lossless line expression

$$Z_0 \cong \sqrt{\frac{L}{C}}$$

The propagation constant, γ, shows that signals exhibit an amplitude loss and phase shift with the latter actually a velocity of propagation of the signal down the line. For lossless lines, where the attenuation is zero, the phase shift per unit length is

$$\beta = \frac{\beta_l}{l} = \omega\sqrt{LC}$$

This really represents a signal traveling down the line with a velocity

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}}$$

This velocity is independent of the applied frequency.

The larger the LC product of the line, the slower the signal will propagate down the line. A time delay per unit length can also be defined as the inverse of v

$$\delta = \frac{1}{v} = \sqrt{LC} \tag{30}$$

and a total propagation delay for a line of length l as

$$\tau = l\delta = l\sqrt{LC} \tag{31}$$

For a more detailed discussion of characteristic impedances and propagation constants, the reader is referred to the references below.

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Matrick, R.F.; *Transmission Lines for Digital and Communications Networks;* McGraw-Hill, New York, 1969.

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Reflections: Computations and Waveforms

National Semiconductor
Application Note 807
Kenneth M. True

OVERVIEW

In this application note, the logical progression from the ideal transmission line to the real world of the long transmission line with its attendant losses and problems is made; specifically, the methods to determine the practicality of a certain length of line at a given data rate is discussed. Transmission line effects on various data formats are examined as well as the effects of several types of sources (drivers) on signal quality. A practical means is given to measure signal quality for a given transmission line using readily available test equipment. This, in turn, leads to a chart that provides the designer a way to predict the feasibility of a proposed data-transmission circuit when twisted-pair cable is used. This application note is a revised reprint of section three of the Fairchild Line Driver and Receiver Handbook. This application note, the second of a three-part series (see AN-806 and AN-808), covers the following topics:

- The Initial Wave
- Cut Lines and a Matched Load
- Kirchoff's Laws and Line-Load Boundary Conditions
- Fundamental Principles
- Tabular Method for Reflections—The Lattice Diagram
- Limitations of the Lattice Diagram Method
- Reflection Effects for Voltage-Source Drivers
- Reflection Effects for Matched-Source Drivers
- Reflection Effects for Current-Source Drivers
- Summary—Which are the Advantageous Combinations?
- Effect of Source Rise Time on Waveforms

INTRODUCTION

In AN-806 it was determined that transmission lines have two important properties: one, a characteristic impedance relating instantaneous voltages and currents of waves traveling along the line and, two, a wave propagation velocity or time delay per unit length. In this chapter, both Z_0 and δ are used to compute the line voltages and currents at any point along the line and at any time after the line signal is applied. Also, concepts of reflections and reflection coefficients are explored along with calculating methods for voltages and currents.

THE INITIAL WAVE

Application Note AN-806 also showed that for most practical purposes, where fast rise and fall time signals are concerned, the characteristic impedance of the line actually behaves as a pure resistance ($R_0 = \sqrt{L/C}$).

Figure 1a shows a generator comprised of a voltage source (magnitude V), a source resistance of R_S ohms, and a switch closing at time t = 0 connected to a lossless, infinite length transmission line having a characteristic resistance, R_0. Because the relationship of V_{IN} to I_{IN} is known as $V_{IN} = R_0 I_{IN}$, the lossless transmission line can be replaced with a resistor as shown in *Figure 1b*. The loop equation is

$$I_{IN}(R_S + R_0) = V \quad (1)$$

Substituting V_{IN}/R_0 for I_{IN} and collecting terms shows

$$V_{IN} = V\left(\frac{R_0}{R_0 + R_S}\right) \quad (2)$$

This shows that both source and characteristic resistances act as voltage dividers for the source voltage V. *Figure 2* shows voltage and current steps for the various source resistances. Source resistances of less than R_0 produce initial voltage steps on the line which are greater than half the compliance of the source voltage, V. A matched source ($R_S = R_0$) produces voltage steps exactly half of V and source resistances greater than R_0 produce an initial voltage step less than one half V in magnitude. Generators can be classified into three categories:

- Voltage source types where $R_S < R_0$
- Matched source types where $R_S = R_0$
- Current source types where $R_S > R_0$

Waveforms of these types will be discussed more fully in AN-808 on long line effects. Suffice to say that initial voltage wave amplitude depends greatly on source resistance. Voltage source type drivers produce higher amplitude initial voltage waves in the line than either matched source or current source type drivers.

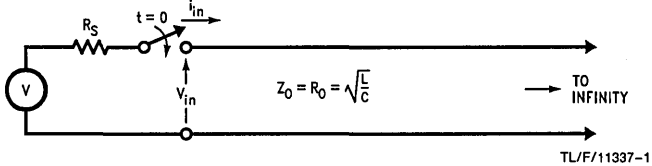

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FIGURE 1a. Generator Driving an Infinite Transmission Line

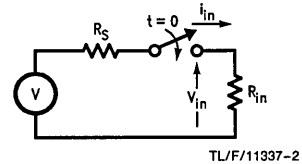

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FIGURE 1b. Thevenin Equivalent for Initial Wave

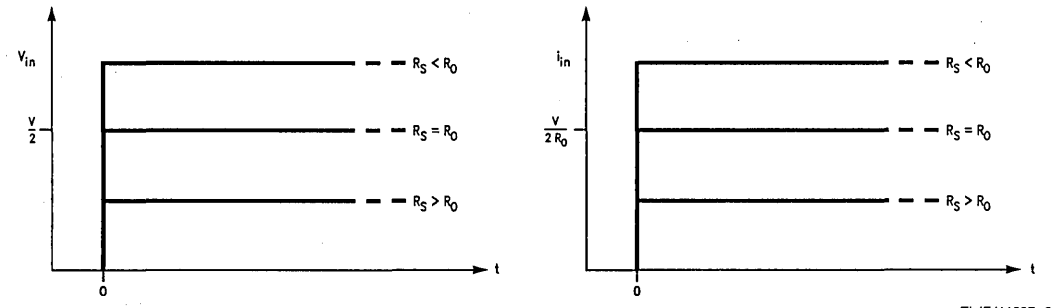

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FIGURE 2. Voltage/Current Steps for Three Source Resistances

CUT LINES AND A MATCHED LOAD

In examining an infinite, lossless line *(Figure 3)*, it is already known that the ratio of line voltage to current is equal to the characteristic resistance of that line. The line is lossless, and the same voltages and currents should appear at point x down the line after a time delay of $x\delta$. If the line at point x is cut, and a resistor of value R_0 is inserted, there would not be a difference between the cut, terminated finite line and the infinite line. The v_x and i_x waves see the same impedance (R_0) they were launched into at time $t = 0$, and indeed, the waves are absorbed into R_L ($= R_0$) after experiencing a time delay of $\tau = x\delta$. So, from an external viewpoint, an infinite-length lossless line behaves as a finite-length lossless line terminated in its characteristic resistance.

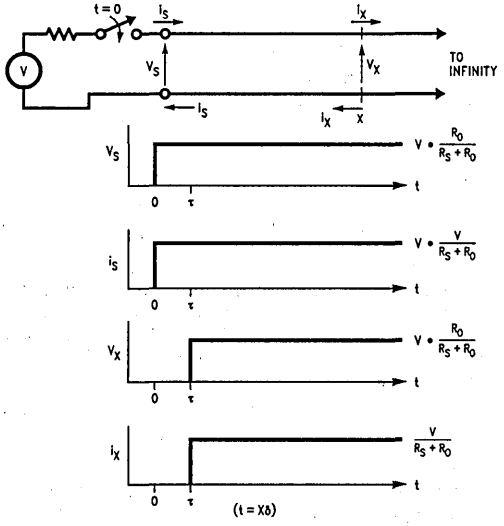

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FIGURE 3. Voltages and Current on an Infinite Length Line

KIRCHOFF's LAWS AND LINE-LOAD BOUNDARY CONDITIONS

The principle of energy conservation, widely known and accepted in the sciences, applies as well to transmission line theory; therefore, energy (as power) must be conserved at boundaries between line and load. This is expressed in an English language equation as follows.

$$\left[\begin{array}{c}\text{Power available at}\\ \text{the line end}\end{array}\right] = \left[\begin{array}{c}\text{Power absorbed}\\ \text{by the load}\end{array}\right] + \left[\begin{array}{c}\text{Power not absorbed}\\ \text{by the load}\end{array}\right]$$

Figure 4 shows power available at the line end is derived by the following formula. (This is assuming in-phase current and voltage.)

$$P_x = i_x \bullet v_x = \frac{v_x^2}{R_0} \tag{3}$$

The power *absorbed* by the load will be

$$P_L = v_L \bullet i_L = \frac{v_L^2}{R_L} \tag{4}$$

while power *not absorbed* by the load is represented by

$$P_r = v_r \bullet i_r = \frac{v_r^2}{R_0} \tag{5}$$

Here, the r subscript stands for reflected (not absorbed) power, voltage or current, respectively.

Applying Kirchoff's laws to point x in *Figure 4*, the current to the load is

$$i_L = i_x - i_r \tag{6}$$

and voltage across the load is

$$v_L = i_L R_L = v_x + v_r \tag{7}$$

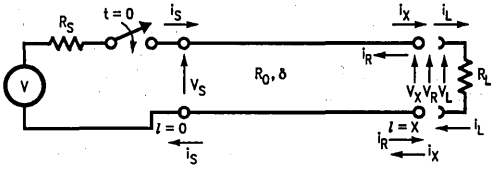

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FIGURE 4. Boundary Conditions at the Line/Load Interface

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To find the ratio of v_r to v_x so that it can be ascertained how much power is absorbed by the load, and how much is not absorbed (therefore, reflected), substitute v_x/R_0 for i_x and v_r/R_0 for i_r into Equation 6.

$$i_L = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{8}$$

Rearranging Equation 7 and substituting for i_L in Equation 8 yields

$$\frac{v_x + v_r}{R_L} = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{9}$$

The minus sign associated with v_r/R_0 means, in this case, that the reflected voltage wave v_r travels in the $-x$ direction toward the generator.

Collecting like terms of Equation 9 yields

$$v_x\left(\frac{1}{R_0} - \frac{1}{R_L}\right) = v_r\left(\frac{1}{R_0} - \frac{1}{R_L}\right) \tag{10}$$

So,

$$v_r = v_x \frac{\left(\frac{R_L - R_0}{R_0 R_L}\right)}{\left(\frac{R_L + R_0}{R_0 R_L}\right)} = v_x\left(\frac{R_L - R_0}{R_0 + R_L}\right) \tag{11}$$

and the desired relation for v_r/v_x is

$$\frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{12}$$

This ratio is defined as the voltage reflection coefficient of the load ρ_{VL}

$$\rho_{VL} \equiv \frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{13}$$

A similar derivation for currents shows

$$\rho_{IL} = -\frac{R_L - R_0}{R_L + R_0} = -\rho_{VL} \tag{14}$$

For the remainder of this application note and AN-808, the v or i subscript on the reflection coefficient is dropped, and ρ_L is assumed to be the *voltage* reflection coefficient of the load. Similarly, applying Kirchoff's laws to the source-line interface, the voltage reflection coefficient of the source is

$$\rho_S = \frac{R_S - R_0}{R_S + R_0} \tag{15}$$

The current reflection coefficient of the source has the same magnitude as ρ_S, but is opposite in algebraic sign.

When a traveling wave v_x, i_x meets a boundary such as the line load interface, a reflected wave is instantaneously generated so that Kirchoff's laws are satisfied at the boundary conditions. This is the direct result of the conservation of energy principle. Referring again to *Figure 4*, the effects of three different termination resistance R_L values are shown.

Case 1, $R_L = R_0$

In this case, R_L is equal to the characteristic resistance of the line. Using Equation 13, the voltage reflection coefficient of the load ρ_L is

$$\rho_L = \frac{R_0 - R_0}{R_0 + R_0} = \frac{0}{2R_0} = 0 \tag{16}$$

Since $v_r/v_x = \rho_L$, then $v_r = \rho_L v_x = 0$ and no reflection is generated. This agrees with the discussion of cut lines and matched load where a line terminated in its characteristic impedance behaves the same as an infinite line. All power delivered by the line is absorbed into the load. The waveforms appear as shown in *Figure 5*. The wave starting at the source at time $t = 0$ is reproduced at point x down the line after a time delay of $t = x\delta = \tau$.

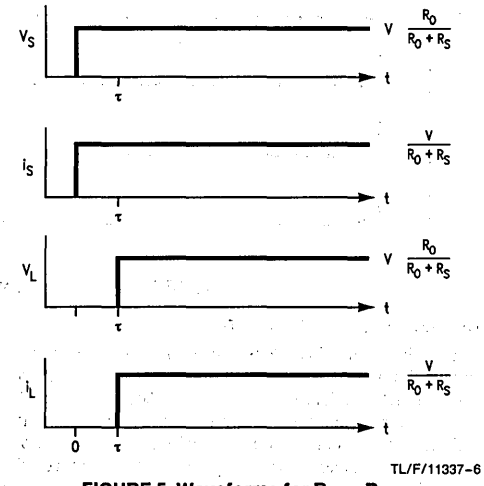

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FIGURE 5. Waveforms for $R_L = R_0$

Case 2, $R_L > R_0$

To simplify this case, assume that $R_S = R_0$. This means that the initial voltage is

$$V\frac{R_0}{R_0 + R_0} = \frac{V}{2} \tag{17}$$

Also assume $R_L = 3\ R_0$, then the load voltage reflection coefficient is

$$\rho_L = \frac{3R_0 - R_0}{3R_0 + R_0} = +\frac{1}{2} \tag{18}$$

The voltage wave arriving at point x at time $t = x\delta$ generates a reflected voltage wave of magnitude

$$v_r = \rho_L v_x = \left(+\frac{1}{2}\right)\left(\frac{V}{2}\right) = \frac{V}{4} \tag{19}$$

and the load voltage is

$$v_L = v_x + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{20}$$

The reflected voltage wave v_r generated at $t = x\delta = \tau$ travels back down the line toward the source arriving at the source at time $t = 2x\delta = 2\tau$. This wave will be absorbed without generating another reflection because R_S was picked to equal R_0, making ρ_S equal to zero. The source voltage is now

$$v_s + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{21}$$

and equilibrium is achieved.

If the circuit in *Figure 4* is analyzed using simple circuit theory and neglecting the transmission line effects, it is easily seen that

$$v_S = v_L = V\frac{R_L}{R_0 + R_L} = \frac{3V}{4} \tag{22}$$

This agrees exactly with Equation 21 and will always be the case. After all reflections cease and the circuit reaches equilibrium, the steady state voltages and currents on the line are the same as those produced using simple dc circuit analysis. Waveforms for $R_L > R_0$ (specifically $R_L = 3\ R_0$) appear in *Figure 6*.

In general, the case where $R_L > R_0$ is viewed in the following manner. Because the line is capable of delivering more power than can be instantaneously absorbed by the load, the excess power is returned to the source and absorbed in the source resistor (assuming $R_S = R_0$).

An upper limit on the voltage reflection coefficient is found by allowing R_L to go to infinity. In this case, Equation 13 goes to $+1$.

Case 3, $R_L < R_0$

In this case, again set $R_S = R_0$ and allow R_L to equal $R_0/3$. The initial wave, as before, is

$$v_S = V\frac{R_0}{R_0 + R_S} = \frac{V}{2} \tag{23}$$

and the load voltage reflection coefficient is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{\frac{R_0}{3} - R_0}{\frac{R_0}{3} + R_0} = -\frac{1}{2} \tag{24}$$

Therefore, the reflected voltage wave v_r is

$$v_r = \rho_L\frac{V}{2} = -\frac{V}{4} \tag{25}$$

which starts propagating back toward the source at time $t = \tau$. The load voltage at time $t = \tau$ is

$$v_x + v_r = \frac{V}{2} + -\frac{V}{4} = +\frac{V}{4} \tag{26}$$

The $(-V/4)$ reflected wave arrives back at the source at time $t = 2\tau$. Because R_S is set equal to R_0, ρ_S is, then, equal to zero and no reflected wave will be generated. The voltage at the source is now

$$v_S + v_r + \rho_S v_r = \frac{V}{2} + -\frac{V}{4} + 0 = \frac{V}{4} \tag{27}$$

From a dc circuit analysis, the steady state voltage is

$$V_{SS} = V\frac{R_L}{R_L + R_0} = \frac{V}{4} \tag{28}$$

This agrees with the result of Equation 27. The waveforms for Case 3 ($R_L < R_0$) appear in *Figure 7*.

An interpretation of the actions occurring when load resistance is less than the characteristic line resistance is as follows: when power available at the line end is less than the power the load can absorb, a signal is sent back to the source saying, in essence, "send more power".

It has been shown that a ratio of line and load resistance (ρ) can be used to calculate the voltages and currents in terms of a wave arriving at the boundary, possibly generating a reflected, reverse-traveling wave to satisfy the conservation of energy principle at the line-to-load boundary. This ratio is

$$\rho_B = \frac{R_B - R_0}{R_B + R_0} \tag{29}$$

where R_B represents the resistance into the boundary, R_B is R_S when considering the source-to-line interface and R_B would be R_L when considering the line-to-load interface. It is obvious that if discussing impedances, then Z_S would be substituted for R_S in Equation 29, and there may be some phase angle between the voltage and current waves.

The forward traveling wave, v_x, plus the reflected wave, v_r, is equal to the load voltage (V_L). Since v_r is $\rho_L v_x$, this can be expressed as

$$v_x(1 + \rho_L) = v_L \tag{30}$$

This quantity $(1 + \rho)$ can be defined as the voltage *transmission* coefficient of the load and it is known that

$$\frac{v_L}{v_x} = (1 + \rho_L) \tag{31}$$

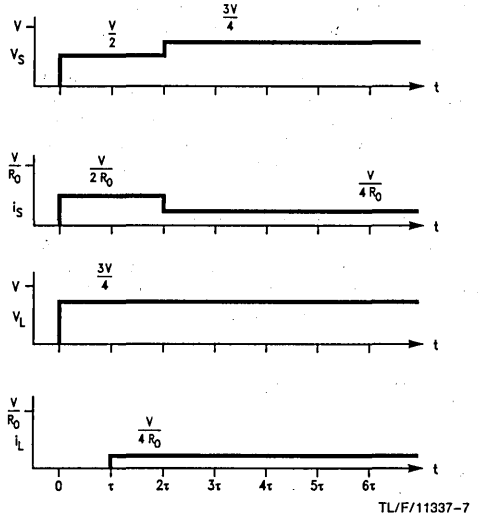

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FIGURE 6. $R_S = R_0$, $R_L = 3R_0$

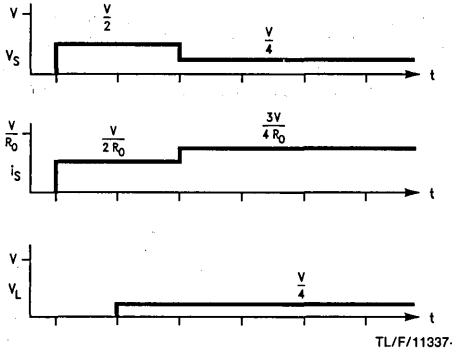

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FIGURE 7. $R_L = \frac{R_0}{3}$

The cases with various load resistances can be summarized.

	Condition		Circuit at time t = τ (one line delay time)
1.	$R_L = R_0$	$\rho_L = 0$	No reflection is produced—circuit reaches steady state immediately.
2.	$R_L > R_0$	$\rho_L > 0$	Positive voltage reflection—wave is sent back toward source. Voltage at load is higher than steady stage voltage (overshoot).
3.	$R_L < R_0$	$\rho_L < 0$	Negative voltage reflection—wave is sent back toward source. Voltage at load is lower than steady state voltage (undershoot).

FUNDAMENTAL PRINCIPLES

Before examining the algorithm for keeping track of reflections, there are two principles to keep in mind.

- Energy (as power) is conserved at boundary conditions (as explored previously)
- The principle of linear superposition applies. This means any arbitrary excitation function can be broken down into step functions, or ramps. The reaction of the circuit to each part can be analyzed, and the results can be added together when finished. This means that a positive pulse of duration t is examined by superimposing two step functions, one positive and one negative, starting after a delay of t *(Figure 8)*. It also means the voltage at any point on the line is the sum of initial voltage plus the sum of all voltage waves that have arrived at or passed through the point up to and including the time of examination. Also, the current on the line is, at any point, the sum of initial current plus any forward or reverse traveling currents passing the point up to and including the time the current is examined.

It has also been established that the steady state solution for voltages and currents on the line can be found by simple dc circuit analysis.

In examining reflection effects for the remainder of this application note, the following conventions are used.

A voltage or current wave traveling *toward* the point of interest will have the subscript "i" for *incident* wave,

A voltage or current wave traveling *away* from the point of interest will have the subscript "r" for *reflected* wave,

The subscript "S" means the parameter applied to the *source* (v_S for the voltage at the source, etc.), and

The subscript "L" means the parameter applied to the *load* (v_L for the voltage at the load, etc.)

Sign conventions for voltage waves and their associated currents are shown in *Figure 9*.

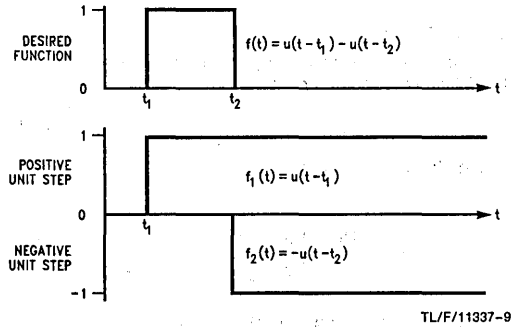

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FIGURE 8. Superposition of Simple Waveforms to Form More Complex Excitations

TABULAR METHOD FOR REFLECTIONS—THE LATTICE DIAGRAM

The waves going up and down the line can be monitored by drawing a time scale, as a vertical line with time increasing in the down direction, to represent the location on the line under examination. Because voltages at the source and load ends of the transmission line are normally of primary interest, two time scales are necessary. Drawing arrows from one time scale to the other as in *Figure 10* shows the direction of travel of the waves during a specific time interval. Since the main concern is only with the waveforms at the line ends, time scales are ruled off in multiples of the time delay of the line τ. If a unit-step type wave is launched from the source at time t = 0+, it is known that the magnitude of the wave will persist unchanged until a wave arrives back from the load after a round trip delay time of two line delays. The source time scale then is incremented in multiples of 2 mτ where m = 0, 1, 2, 3, ... Likewise, the first wave arrives at the load after a single time delay, so the first increment ruling on the load time scale is τ, or one time delay of the line. Because the subsequent waves arrive back at the load in increments of 2τ, the load time scale is ruled off in multiples of (2m + 1)τ where m = 0, 1, 2, 3, ... The operation of the lattice diagram is discussed using the example in *Figure 10b* which is the lattice diagram for the associated circuit.

time t = 0− (just before the switch closes)

The voltages at the source and load are equal with a magnitude of $v_{initial}$. Assume that no initial voltage is present. So, in this case, the voltage at the source and load equals zero.

$$V_{initial} = v_S(0-) = V_L(0-) = 0$$

time t = 0+ (just after the switch has closed)

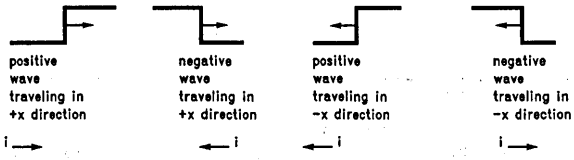

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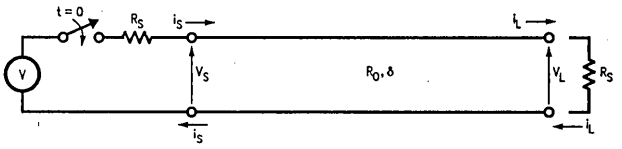
FIGURE 9. Sign Conventions for Waves



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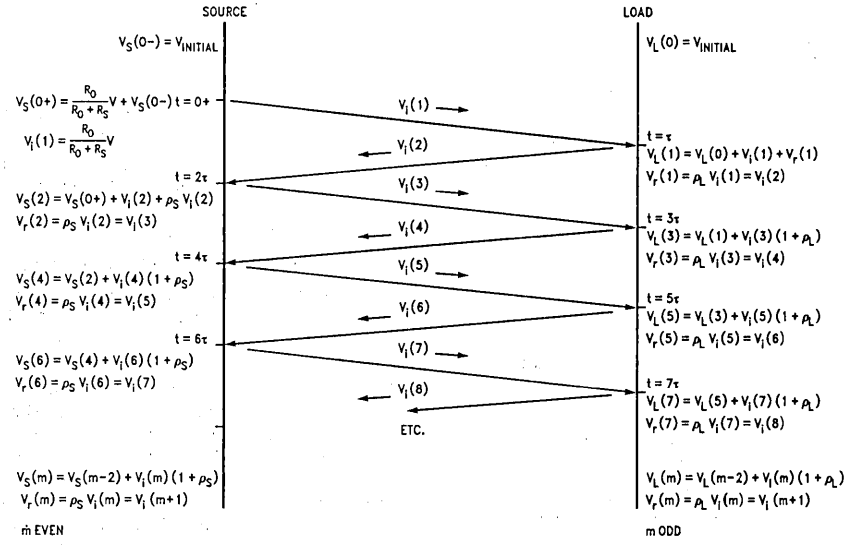
(a) Line Circuit to be Analyzed



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(b) Lattice Diagram

FIGURE 10. Reflection Bookkeeping with the Lattice Diagram

The first wave $v_i(1)$ is launched at the source and begins to travel toward the load end of the line. As previously mentioned, a voltage divider action between R_S and R_0 is used to derive the magnitude of the initial voltage wave.

$$v_i(1) = V\frac{R_0}{R_0 + R_S}$$

At this time, the voltage at the source is the sum of the initial voltage plus the voltage wave $v_i(1)$ just generated.

$$v_S(0+) = v_S(0-) + v_i(1) = 0 + V\frac{R_0}{R_0 + R_S}$$

Because the switch closure represents a step function, the source voltage remains at this level until a wave returns after reflecting from the load at time $t = 2\tau$.

time $t = \tau$

The incident voltage wave $v_i(1)$ now arrives at the load and generates a reflected voltage wave

$$v_r(1) = \rho_L v_i(i);\ \rho_L = \frac{R_L - R_0}{R_L + R_0}$$

where ρ_L is the voltage reflection coefficient of the load. The reflected voltage wave $v_r(1)$ immediately starts traveling back toward the source becoming the incident voltage wave $v_i(2)$ which arrives back at the source at $t = 2\tau$. The voltage at the load is now the sum of the initial voltage plus the incident voltage wave $v_i(1)$ that just arrived plus the reflected voltage wave that is just departing.

$$\begin{aligned} v_L(1) &= v_L(0-) + v_i(1) + v_r(1) \\ &= 0 + v_i(1) + \rho_L v_i(1) \\ &= v_i(1)(1 + \rho_L) \end{aligned}$$

Again, because of the step function excitation, the load voltage remains unchanged until the new wave arrives at time $t = 3\tau$.

time $t = 2\tau$

$v_i(2)$ now arrives at the source and generates a reflected voltage wave $v_r(2)$ of magnitude

$$v_r(2) = \rho_S v_i(2);\ \rho_S = \frac{R_S - R_0}{R_S + R_0}$$

where ρ_S is the source voltage reflection coefficient.

The reflected voltage wave $v_r(2)$ starts back toward the load end of the line and becomes the incident voltage wave $v_i(3)$ arriving at the load at time $t = 3\tau$. The voltage at the source is now the sum of the voltage that was there plus the incident voltage wave just arrived plus the reflected voltage wave just departed for the load.

$$\begin{aligned} v_S(2) &= v_S(0+) + v_i(2) + v_r(2) \\ &= v\frac{R_0}{R_0 + R_S} + v_i(2) + \rho_S v_i(2) \\ &= v\frac{R_0}{R_0 + R_S} + v_i(2)(1 + \rho_S) \end{aligned}$$

time $t = 3\tau$

$v_i(3)$ arrives at the load generating $v_r(3)$

$$v_r(3) = \rho_L v_i(3)$$

$v_r(3)$ departs back toward the source becoming $v_i(4)$ to the source. The load voltage is now

$$v_L(3) = v_L(1) + v_i(3)\,(1 + \rho_L)$$

time $t = 4\tau$

When $v_i(4)$ arrives at the source and generates $v_r(4)$, then

$$v_r(4) = \rho_S v_i(4)$$

starts back toward the load to become $v_i(5)$ to the load. The load voltage is now

$$v_L(4) = v_L(2) + v_i(4)\,(1 + \rho_L)$$

This process can continue ad infinitum or until no measurable changes are detected. The reflection process at that time is considered complete and the line assumes a steady state condition. Steady state conditions can be found by applying simple dc circuit theory to source load circuits.

Summarizing this lattice diagram method, any time $t = m\tau$ and $m > 1$, the following relationships exist:

If m is odd, the $v_i(m)$ wave is arriving at the load and generates a reflected wave

$$v_r(m) = \rho_L v_i(m)$$

This becomes $v_i(m + 1)$ as it starts toward the source. The voltage at the load at time $t = m\tau$ will be

$$v_L(m) = v_L(m - 2) + v_i(m)\,(1 + \rho_L)$$

This is the sum of the voltage that was there before the wave arrived, i.e., $v_L(m - 2)$, plus the wave arriving $v_i(m)$ and the reflected wave $v_r(m)$ departing.

If m is even, the $v_i(m)$ wave is arriving at the source and generates a reflected wave

$$v_r(m) = \rho_S v_i(m)$$

This becomes $v_i(m + 1)$ as it starts toward the load. The voltage at the source is now

$$v_S(m) = v_S(m - 2) + v_i(m)\,(1 + \rho_S)$$

This is the sum of the voltage that was present $v_S(m - 2)$ plus the incident wave arriving $v_i(m)$ plus the reflected wave departing $v_r(m)$.

The voltage and current at the source end of the line for a lossless line can be expressed as a summation.

$$v_S(t) = \frac{R_0}{R_S + R_0} \bullet \tag{32}$$

$$\left[e(t)u(t) + (1 + \frac{1}{\rho_S}) \sum_{n=1}^{\infty} \rho_S{}^n \rho_L{}^n e(t - 2n\tau)u(t - 2n\tau)\right]$$

$$i_S(t) = \frac{1}{R_S + R_0} \bullet \tag{33}$$

$$\left[e(t)u(t) + (1 - \frac{1}{\rho_S}) \sum_{n=1}^{\infty} \rho_S{}^n \rho_L{}^n e(t - 2n\tau)u(t - 2n\tau)\right]$$

where e(t) is the generator voltage as a function of time, and u(t) is the unit step function.

Likewise, the load voltage and load current for the lossless line can be expressed as a summation.

$$v_L(t) = \frac{R_0}{R_S + R_0} \bullet \tag{34}$$

$$(1 + \rho_L)\left[\sum_{n=0}^{\infty} \rho_S{}^n \rho_L{}^n e(t-(2n + 1)\tau)u(t-(2n + 1)\tau)\right]$$

$$i_L(t) = \frac{1}{R_S + R_0} \bullet \tag{35}$$

$$(1 - \rho_L)\left[\sum_{n=0}^{\infty} \rho_S{}^n \rho_L{}^n e(t-(2n + 1)\tau)u(t-(2n + 1)\tau)\right]$$

A similar expression of summation can be developed for the voltage (or current) at any point along the line at any time.

Because the lattice diagram is tabular in method, a computer program can be written releving the designer of bookkeping and repetitive calculations. A BASIC computer program for lattice diagrams appears in *Figure 13*.

LIMITATIONS OF THE LATTICE DIAGRAM METHOD

Before using the lattice diagram to explore reflection effects with various source and load characteristics, it is necessary to pause at this point and examine the models used by the lattice diagram.

First, both the line driver and receiver are simulated either by a constant input or output resistance. The source has two voltage sources and a switch representing the internal source voltage at a time less than zero and equal to (or greater than) zero. The receiver is represented by a single resistor shunting the line end opposite the driver site. The line itself is represented by its characteristic resistance R_0 and its total one-way time delay (τ). This is equal to length times propagation delay per unit length. This model is shown in *Figure 11*.

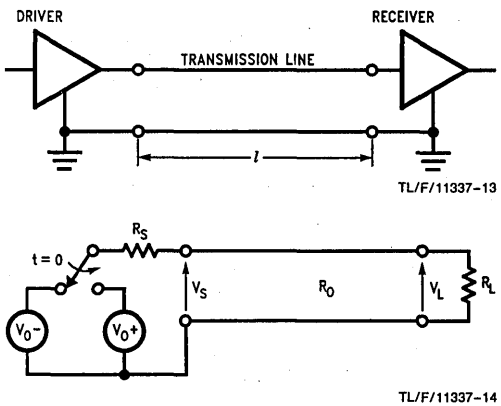


FIGURE 11. Model Used for Lattice Diagram Method

Because most data communication circuits are voltage types, that is, the receiver senses the line voltage to decide if a logic One or logic Zero is present, the primary interest is in voltages at the source and load as a function of time. Major exceptions include the current loops used in teletypewriters, telegraphs, and burglar alarm systems. The majority of data communications circuits used in computers, peripherals, and general controllers are voltage types.

The lattice diagram method cannot easily use source or receiver current/voltage relationships that are non-linear; i.e., not purely resistive. For non-linear current/voltage characteristics such as found in diodes, a graphic method can be used called the reflection diagram or the Bergeron method.

Note: A French hydraulic engineer, L.J.B. Bergeron developed the method to study the propagation of water hammer effects in hydraulics. See references, AN-806.

Signals exchanged using lattice diagrams are of the unit step variety. When ramps or more complex waves are exchanged, the complexity of the bookkeeping increases dramatically. Additionally, the lines are presumed to be lossless, although a constant line attenuation factor could be accommodated without excessive bookkeeping. These limitations should be kept in mind when examining various source and load resistance combinations and their reflection characteristics.

There are three classes of source resistance, $R_S < R_0$, $R_S = R_0$ and $R_S > R_0$. There are also three classes of load resistance, $R_L < R_0$, $R_L = R_0$ and $R_L > R_0$. This gives nine types of single driver, single receiver line circuits. Each circuit will be examined in turn to determine reflection effects for these combinations with evaluations of each combination for voltage type communications.

REFLECTION EFFECTS FOR VOLTAGE SOURCE DRIVERS

Initial waves launched by a voltage source type driver ($R_S < R_0$) are greater than one-half the magnitude of the internal voltage source. Referring to *Figure 11*, the initial voltage wave is derived as follows.

$$v_i(1) = (V_{0+} - V_{0-}) \bullet \frac{R_0}{R_0 + R_S} \qquad (36)$$

while the voltage at the source at $t = 0+$ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \bullet \frac{R_L}{R_L + R_S} + v_i(1) \qquad (37)$$

If the receiver switching point is at the mean of the driver voltage swing, the initial wave always has sufficient magnitude to indicate the correct logic state as it passes the receiver site. This maximizes the noise margins of the receiver.

Since $R_S < R_0$, the source voltage reflection coefficient ρ_S is less than zero. Any voltage waves, then, arriving back at the source are changed in sign, reduced in amplitude (assuming $R_S > 0\Omega$), and sent back toward the load. If the load resistance equals the characteristic line resistance ($R_L = R_0$), the voltage reflection coefficient of the load is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{0}{2R_0} = 0$$

No reflections, therefore, are generated at the load. The voltage wave produced at the source is reproduced at the load after a time delay of $\tau = \ell\,\delta$, and the line assumes a steady state condition. *Figure 12b* illustrates the source and load voltage waveforms for this case.

If R_L is greater than R_0, ρ_L is positive. Waves arriving at the load generate the same polarity reflections as the arriving waves. ρ_S and ρ_L are of opposite signs, so a dampened oscillatory behavior of the load voltage is expected. The oscillation period or *ringing* is 4τ. The overshoot of v_L from $t = \tau$ to 3τ may cause breakdown of the input circuitry of a receiver, depending on the receiver voltage rating. The undershoot at $t = 3\tau$ or 5τ can reduce the noise immunity of a receiver or even cause a logic level misinterpretation—an error in the data. These waveforms are shown in *Figure 12a*.

If R_L is less than R_0, then ρ_L is negative and a wave arriving at the load generates a reflection opposite in polarity to the incident wave. This causes the voltage at the source to overshoot steady state voltage at $t = 0$. Each reflection returning from the load causes the source voltage to continually step down toward the steady state voltage V_{SS}. These steps last for 2τ, or one round trip delay. Load voltage starts an increasing step-up waveform towards V_{SS} at time $t = \tau$, with steps again taking one round trip delay, 2τ. A line receiver placed in the middle of the line sees an entirely different waveform—dampened oscillations much like the load voltage in *Figure 12a*. This is caused by the negative signs of both source and load voltage reflection coefficients. Each time an incident wave arrives at either source or load, the reflected wave generated at that time has a sign opposite to the sign of the incident voltage wave. The voltage at a distance half way down the line is composed of these forward and reverse traveling waves arriving at that point commencing at time $t = 0.5\tau$, and with each new wave passing that point after one line delay (τ). These waveforms are shown in *Figure 12c*.

The optimum load resistance for voltage signal communications on transmission lines driven by a low impedance source ($R_S < R_0$) is equal to the characteristic line resistance. Large signal line voltages are produced and there are no reflection effects complicating the waveforms *(Figure 12b)*.

However, a matched load ($R_L = R_0$) is a dc load on the driver, thus it increases system power dissipation. But, it does preserve signal fidelity and amplitude allowing use of multiple bridging receivers ($R_{in} \gg R_0$) along the line.

The unterminated case ($R_L > R_0$) reduces dc driver loading and also reduces system power dissipation over the matched load case. The unterminated case does, however, allow the load signal to exhibit pronounced overshoot and undershoot around the steady state voltage. If the load signal undershoot places the receiver in its threshold uncertainty region, data errors result. There is a way to "civilize" the voltage waveform of the unterminated line load by trading off signal rise time versus line time delay. This is discussed later.

The final case of $R_S < R_0$ and $R_L < R_0$ is not generally useful in terms of voltage signals produced *(Figure 12c)*. Systems using this case consume more power than the previous two cases and have no particular advantage for voltage mode communications.

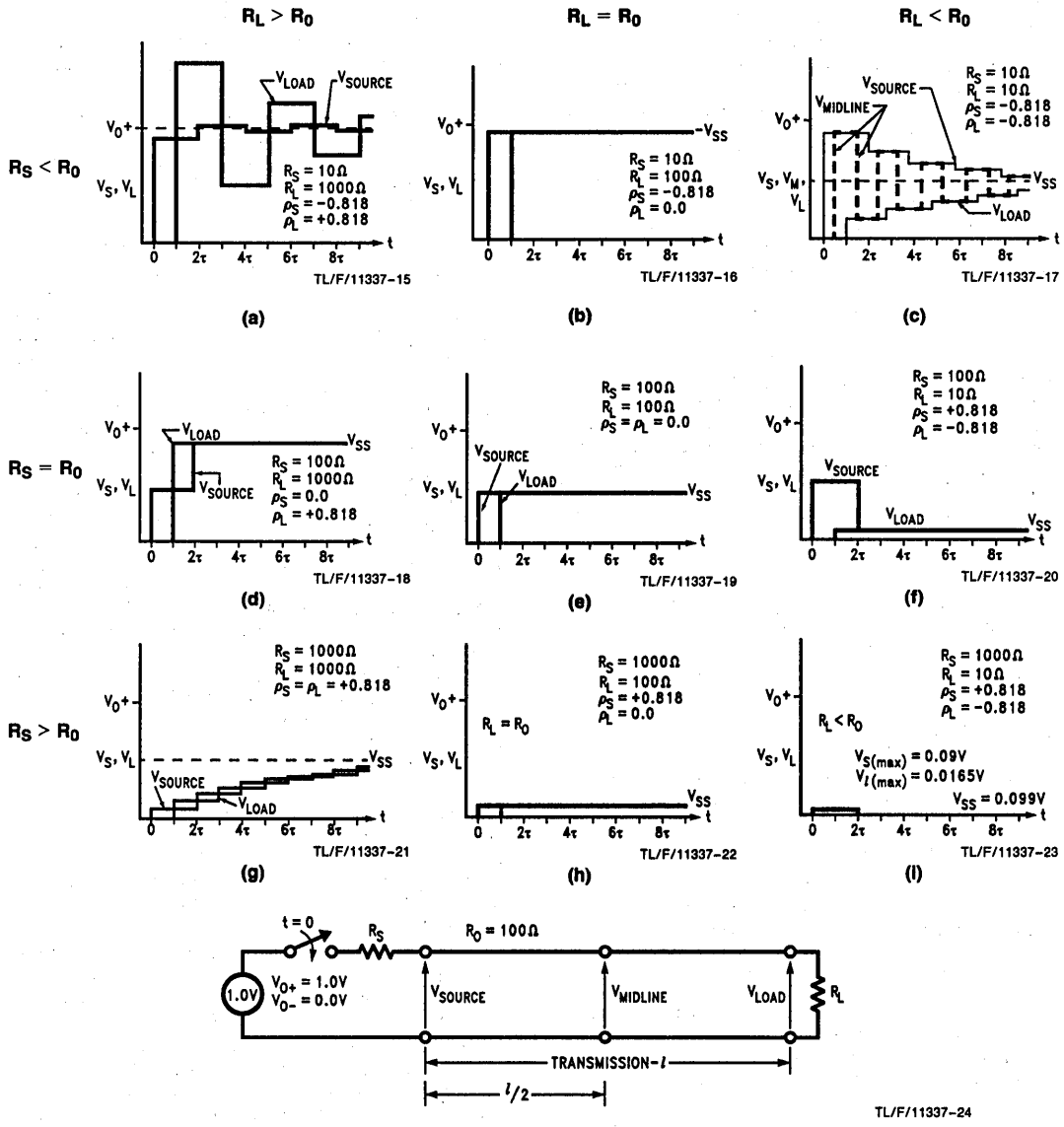


FIGURE 12. Source and Load Voltage Waveforms for Various R_S and R_L

REFLECTION EFFECTS FOR MATCHED-SOURCE DRIVERS

In all three cases under discussion here, the initial voltage produced by the driver onto the line is

$$v_i(1) = (V_{0+} - V_{0-})\frac{R_0}{R_0 + R_S} = \frac{1}{2}(V_{0+} + V_{0-}) \quad (38)$$

since $R_S = R_0$. The voltage at the source at time $t = 0+$ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \bullet \frac{R_L}{R_L + R_S} + v_i(1) \quad (39)$$

Assume, for clarity, that initial voltage (V_{0-}) is zero, thus Equation 39 simplifies to

$$v_S(0+) = \frac{V_{0+}}{2} \quad (40)$$

Since $R_S = R_0$, ρ_S is equal to zero. This means that load-generated reflections due to load mismatch are absorbed at the source when, at time $t = 2\tau$, the reflected wave arrives back at the source. The line then assumes a steady state throughout. This back match or series termination effect of a matched source allows a wide latitude in choice of load resistance without sacrificing the signal fidelity of the load voltage waveform.

If the load resistance equals the characteristic line resistance $R_L = R_0$, then ρ_L equals zero and no load site reflections are generated. The initial voltage wave arrives at the load at time $t = \tau$ (one line delay) and voltages (and currents) on the line immediately assume steady state conditions (see *Figure 12e*). The optimum receiver threshold here is one-half the steady state voltage or $V_{0+}/4$. The main advantage over the voltage source type driver with matched load case ($R_S < R_0$, $R_L = R_0$) is that R_S and R_L resistance tolerances may be relaxed without incurring much signal *ringing*. This effect is due primarily to the termination provided by both line ends, rather than just one line end. Any reflected voltage wave on either system is attenuated by the product of ρ_S and ρ_L for each round trip line delay time. Since the $\rho_S\rho_L$ product for the fully matched case is smaller than the $\rho_S\rho_L$ product for the single matched case, the reflections are attenuated and die out in fewer round trips. For example, if 20% tolerance resistors are used in both cases, ρ_S and ρ_L values for the fully matched case become 0.0 ± 0.0909, which is a $\rho_S\rho_L$ product of ± 0.0033. This means that after one round trip (2τ), the reflection amplitude starting back toward the load would be less than 0.33% of the initial wave.

Using $R_S = 10\Omega$, $R_L = 100\Omega$, and $R_0 = 100\Omega$ as for *Figure 12a*, shows the same 20% tolerances applied to the single matched case

$$-0.8519 \leq \rho_S \leq -0.7857$$
$$-0.0909 \leq \rho_L \leq +0.0909$$

and

$$|\rho_S\rho_L| \leq 0.0774$$

The voltage reflection amplitude after one round trip is a maximum of 7.7% of the initial wave.

The choice between using the single and fully matched system should be carefully considered because the fully matched system does sacrifice signal voltage magnitude to get a decreased dependence on absolute resistor values.

If the load resistance for a matched driver circuit is made much greater than the line resistance, the initial wave arriving at the load at time $t = \tau$ will be almost double since ρ_L will be close to $+1.0$. Because source resistance is set equal to line resistance, ρ_S becomes zero, the reflected voltage wave from the load is absorbed by the source at time $t = 2\tau$, and steady state conditions prevail. Waveforms for this case are shown in *Figure 12d*. This is called *back matching* or *series termination*.

The main advantage of series termination is a great reduction in steady state power consumption when compared with the parallel terminated case ($R_S \ll R_0$, $R_L = R_0$). At the same time, series termination provides the same signal fidelity to a receiver placed at the line end. Compare the load voltage waveforms for the two cases in *Figure 12b* and *12d*. The main disadvantage to series termination is that receivers placed along the line see a waveform similar to that shown for the source in *Figure 12d*. That is, receivers along the line see the $V_{0+}/2$ initial wave as it passes that point on the line, and do not see a full signal swing until the load end reflection passes that point. Consequently, receivers along the line do not see a signal sufficient to produce the valid logic state output until the load reflection returns. Depending on actual line length and receiver characteristics, the receiver may even oscillate, having been placed in its linear operation region. With the benefit, then, of reducing system power, the series termination method has a constraint of allowing only one line receiver located at the line load end. The parallel termination method should be used if other receivers along the line are required.

The final case of matched source drivers is with the use of a load resistance less than the characteristic line resistance. The waveforms for this case are shown in *Figure 12f*. A line receiver with a threshold of $V_0/4$ placed at the source responds like a positive, edge triggered one-shot and produces a pulse in response to a $+V/2$ initial wave of 2τ duration. Aside from its use as a one-shot, this circuit doesn't seem to offer any advantages for voltage mode communications.

REFLECTION EFFECTS FOR CURRENT-SOURCE DRIVERS

The name *current source drivers* is somewhat of a misnomer, and might be more properly called *current-limited voltage source drivers*. True *current source* drivers such as the DS75110A are normally used in conjunction with parallel termination resistors to create a matched source.

The *current source* drivers ($R_S > R_0$) discussed resemble true current sources in the respect that their output resistance is usually much greater than the characteristic line resistance. The initial voltage step produced on the line is thus usually small $v_i(1) = (i_S(1)R_0)$. This is due to the voltage divider action of the driver source resistance and the characteristic line resistance.

Voltage waveforms for a current source type driver either step up to V_{SS}, reach steady state after 2τ, or execute a dampened oscillation around V_{SS}, depending on whether the load resistance R_L is greater, equal, or less than R_0, respectively. The second case $R_L = R_0$ provides signals much the same as the other two cases where $R_L = R_0$, that is, the source voltage steps immediately to V_{SS}, with the load voltage following after one line time delay. Here the amplitude of the signal is much smaller than previous matched load cases. Since the current source type drivers (DS75110A) have high off-state impedances, they allow multiple drivers on the line to produce data bus or party line. Waveforms for the matched load case are shown in *Figure 12h*.

The case $R_L < R_0$ really provides no useful advantage for voltage mode communications. The negative sign for ρ_L and the positive sign for ρ_S lead to dampened oscillatory behavior, or ringing. The maximum perturbation takes place at the source end of the line. Waveforms for this case are similar to those shown in *Figure 12a*, and are shown to scale in *Figure 12i*. With the given values used to produce the figure, the maximum amplitude ringing appears at the source line end.

The $R_L > R_0$ case is of interest because it is representative of DTL driving a transmission line with the output going from LOW to HIGH. DTL has a high value R_S, (2 kΩ or 6 kΩ) in the HIGH logic state. Since both R_S and R_L are greater than R_0, both ρ_S and ρ_L are positive. A small voltage step starts from the source at $t = 0+$; its magnitude is

$$v_i(1) = V\frac{R_0}{R_0 + R_S}$$

Note: Since the input diode is not represented, the representation of DTL input as a single resistor to ground is not strictly correct. For purposes of approximation, this simple representation is used. Treatment of non-linear current/voltage sources and loads is covered by Metzger & Vabre. (op. cit.)

Upon arrival at the load at time $t = \tau$, this initial wave generates a positive voltage reflection since $\rho_L > 0$. The voltage reflection arrives back at the source site at time $t = 2\tau$. Since ρ_S is also positive, another positive voltage reflection is launched back toward the load. The process repeats, and the source and load voltages both execute a step-up approach toward steady state voltage V_{SS}. These waveforms are shown in *Figure 12g*.

In examining voltage at the line midpoint ($x = \ell/2$), a step-up type waveform is seen which is the sum of all the incident voltage waves passing the line midpoint up to the time of examination. The midpoint voltage is expressed as follows.

$$v_m(t) = V_{SS}\,(1 - \exp[-(t + 0.5\tau)/T]) \qquad (41)$$

Note: This equation is presented without derivation, but a procedure similar to that used by Matick (Ref. 2, AN-806) can be used.

for $t = n + 0.5\tau$ with $n = 0, 1, 2, 3$, etc. V_{SS} in Equation 41 is the steady state line voltage

$$V_{SS} = V_{0+} \bullet \frac{R_L}{R_S + R_L}$$

and T is a time constant given by

$$T = -\frac{2\tau}{\ell\, n(\rho_S \rho_L)} \qquad (42)$$

with τ being one line delay ($\tau = \ell\,\delta$).

Note: This equation is presented without derivation, but a procedure similar to that used by Matick (Ref. 2, AN-806) can be used.

Equation 41 provides an exact solution for odd multiples of n ($n = 1, 3, 5 \ldots$, so $t = 1.5\tau, 3.5\tau, 5.5\tau \ldots$), while it approximates $v_m(t)$ for even multiples of n ($n = 0, 2, 4 \ldots$, so $t = 0.5\tau, 2.5\tau, 4.5\tau \ldots$). The closer the $\rho_S\rho_L$ product is to 1, the better Equation 41 predicts $v_m(t)$, particularly for even multiples of n. To illustrate the fitting, the two tables in *Figure 13* are generated by the BASIC language computer program (Table C) and their data is plotted in *Figure 14*.

Designers familiar with DTL circuits should quickly recognize that the waveforms shown in *Figure 14* are very similar to the rising edge waveforms found when a DTL gate output goes from the LOW to HIGH state. This characteristic waveform has usually been attributed to the series RC circuit (a gate output resistance driving a lumped transmission line capacitance). The time constant for this approach, based on the C(dv/dt) = i rule from simple circuit theory, provides only an approximation. The actual cause of the waveform shape, however, is due to reflection effects. Unfortunately, the only way to speed up the rising edge is to reduce source resistance, (providing an initial step greater than the receiving threshold) and terminate the line to eliminate the load reflections.

DTL inability to drive transmission lines at high repetition rates is the direct result of the signal rise time limitation caused by positive reflection coefficients for both the source and load. A transmitted positive pulse may be missed if its duration is less than the time required for the load signal to reach the receiver threshold.

The $R_S > R_0$ and $R_L > R_0$ case provides no definite advantages as voltage mode communication is concerned. This case, in fact, poses a definite hazard to high speed data communications because the reflections cause, in effect, a slow, exponential signal transition. Because line delay is a factor, longer lines will only increase the effect.

TABLE A. (R_S = 2000Ω, R_0 = 100Ω, R_L = 4000Ω)

RHOS = 0.904762 RHOL = 0.951220
TAU = −13.3250 V1(1) = 4.76190H-C2
V_{SS} = 0.666667

TIME	VM(T)	VAPPX	%DIFF
0.5	0.04762	0.04820	+1.220%
1.5	0.09292	0.09292	+0.000%
2.5	0.13390	0.13440	+0.373%
3.5	0.17288	0.17288	+0.000%
4.5	0.20815	0.20858	+0.207%
5.5	0.24170	0.24170	+0.000%
6.5	0.27206	0.27243	+0.136%
7.5	0.30093	0.30093	+0.000%
8.5	0.32705	0.32737	+0.097%
9.5	0.35190	0.35190	+0.000%
10.5	0.37439	0.37466	+0.073%
11.5	0.39577	0.39577	+0.000%
12.5	0.41512	0.41536	+0.057%
13.5	0.43353	0.43353	+0.000%
14.5	0.45018	0.45038	+0.045%
15.5	0.46602	0.46602	+0.000%
16.5	0.48035	0.48053	+0.036%
17.5	0.49399	0.49399	+0.000%
18.5	0.50632	0.50647	+0.030%
19.5	0.51805	0.51805	+0.000%
20.5	0.52867	0.52880	+0.024%
21.5	0.53877	0.53877	+0.000%

TABLE B. (R_S = 500Ω, R_0 = 75Ω, R_L = 10 kΩ)

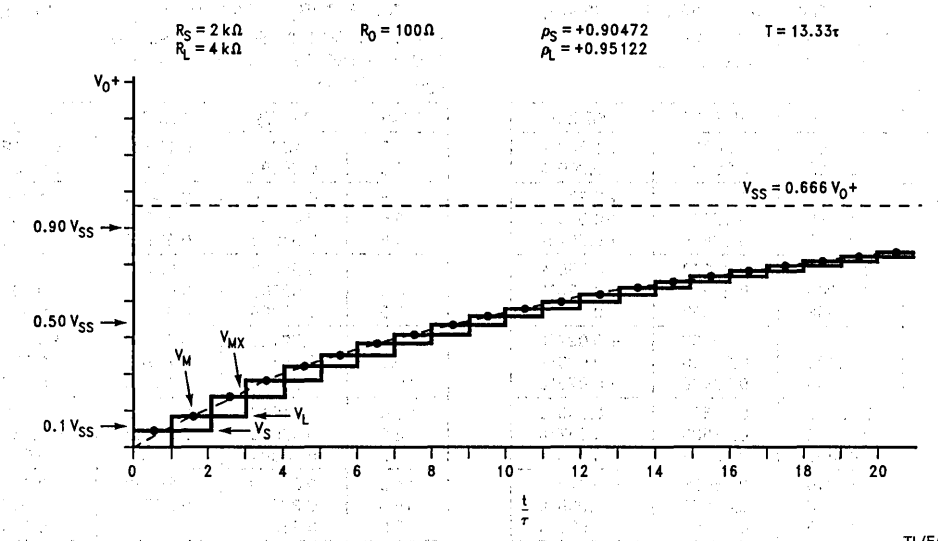
RHOS = 0.739130 RHOL = 0.985112
TAU = −6.30356 V1(1) = 1.30435
V_{SS} = 0.952381

TIME	VM(T)	VAPPX	%DIFF
0.5	0.13043	0.13971	+7.112%
1.5	0.25893	0.25893	+0.000%
2.5	0.35390	0.36066	+1.909%
3.5	0.44746	0.44746	+0.000%
4.5	0.51661	0.52153	+0.952%
5.5	0.58473	0.58473	+0.000%
6.5	0.63509	0.63867	+0.564%
7.5	0.68469	0.68469	+0.000%
8.5	0.72135	0.72396	+0.361%
9.5	0.75747	0.75747	+0.000%
10.5	0.78416	0.78606	+0.242%
11.5	0.81046	0.81046	+0.000%
12.5	0.82990	0.83128	+0.167%
13.5	0.84904	0.84904	+0.000%
14.5	0.86320	0.86420	+0.117%
15.5	0.87714	0.87714	+0.000%
16.5	0.88744	0.88818	+0.083%
17.5	0.89759	0.89759	+0.000%
18.5	0.90510	0.90563	+0.059%
19.5	0.91249	0.91249	+0.000%
20.5	0.91795	0.91834	+0.042%
21.5	0.92334	0.92334	+0.000%

TABLE C. BASIC Program Listing

```
100 PRINT'ENTER RS, RO, RL'1
110 INPUT R1, RO, R2
120 P1=(R1-RO)/(R1+RO)
130 P2=(R2-RO)/(R2+RO)
140 V1=RO/(R1+RO)
150 K1=2./LOG(P1*P2)
160 V9=R2/(R1+R2)
170 PRINT'RHOS='; P1;'RHOL=';P2;'TAU=';K1
180 PRINT 'V1(1)=';V1;'VSS=';V9
190 V=V1
200 PRINT'TIME   VM(T)   VAPPX   %DIFF'
210 FOR T=0.5 TO 20.5 STEP 2.
220 V2=V9*(1.-EXP((T+.5)/K1))
230 P=100.*(V2-V)/V
240 PRINT USING 250,T,V,V2,P
250 :##.# -#.##### -#.##### +###.###%
260 V1=V1*P2
270 V=V+V1
280 REM  SOURCE END
290 V2=V9*(1.-EXP( (T+1.5)/K1 ) )
300 P=100.*(V2-V)/V
310 PRINT USING 250,T+1.,V,V2,P
320 V1=P1*V1
330 V=V+V1
340 NEXT T
350 PRINT
360 PRINT
370 PRINT
380 GOTO 100
390 END
```

FIGURE 13. Comparison of v_m Formula to Computed Midline Voltage



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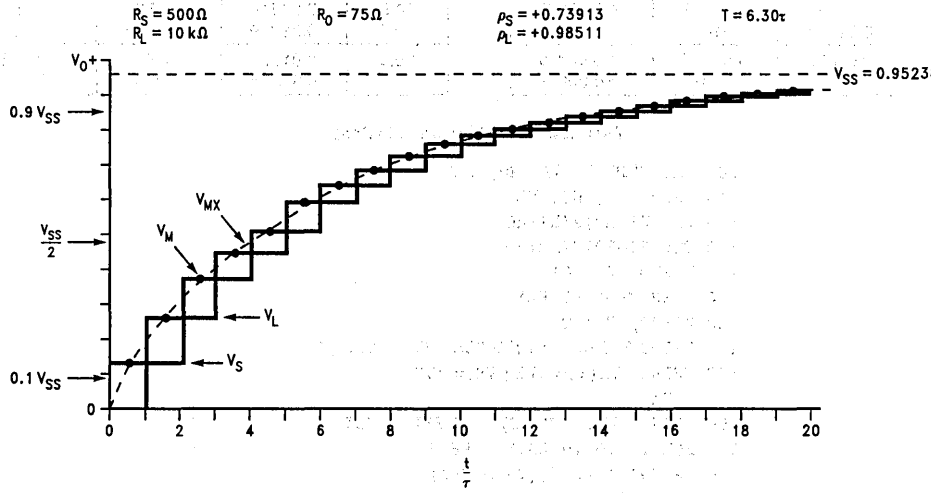

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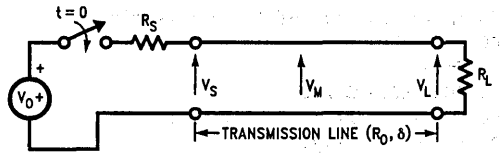

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$$v_{MX}(t) = V_{SS}\left(1 - \exp[-(t + 0.5\tau)/T]\right)$$

$$t = \frac{-2\tau}{\ell n\,(\rho_S\,\rho_L)}$$

FIGURE 14. Approximation of Midline Voltage with $R_S > R_0$ and $R_L > R_0$

SUMMARY—Which are the Advantageous Combinations?

In examining the basic combinations of source, line and load resistances, and typical waveforms characteristic of each case, advantageous combinations can be determined. The primary results are tabulated in *Figure 15*. those combinations generally used in voltage mode communications circuits are as follows.

1. Unterminated case ($R_S \ll R_0$, $R_L \gg R_0$). This situation provides low steady state power dissipation and large signal levels, but also shows pronounced "ringing" effects. The "ringing" can be reduced by controlling signal rise/fall time versus τ, or by clamping diodes to limit load signal excursions. This case is representative of TTL circuits and is thus widely employed.
2. The parallel terminated case ($R_S \ll R_0$, $R_L = R_0$) provides large signal levels, and excellent signal fidelity. However, it is power consuming with most of that power dissipated in the load resistor. This case is useful for cleaning up the reflection effects of Case 1 but, at the same time, does require a driver circuit to have its internal current limits set at greater values than those required to produce the desired signal level into the minimum line resistance used. Thus, this case requires specific line driver devices such as the DS75114/DS9614. Ordinary TTL, except for the above mentioned circuits, has too low a current limit point to adequately drive 50Ω lines.
3. The series terminated or backmatched driver case $R_S = R_0$, $R_L \gg R_0$ provides a low steady state power dissipation system for use with one receiver located at the load end of the line. The positive reflection coefficient of the load is used to approximately double the initial wave arriving at the load. Setting $R_S = R_0$ terminates the reflected wave when it arrives back at the source site after two line delays, and the line then assumes steady state conditions. The use of other receivers located along the line is not recommended, because they will not see the full driver signal swing until the reflection from the load passes their particular bridging points Such receivers could malfunction, as they would see a voltage very close to their threshold, and perhaps even place the line receiver in its linear operating region. This could make the line receiver sensitive to oscillatory, parasitic feedback. If these constraints are acceptable, the series termination method can be used to good advantage in providing the same signal fidelity and signal amplitude as with the parallel termination method, while at the same time, contributing a significant savings in steady state power consumption.
4. The fully matched case $R_S = R_0$, $R_L = R_0$ not only provides excellent signal fidelity all along the line, but also has reduced signal amplitude over that of the parallel terminated case. Additionally, the power consumption is somewhat less than the parallel termination case and the power is divided equally by the source and load. The primary advantage of the fully matched system is that termination resistor tolerances can be relaxed somewhat without incurring large amounts of ringing. This is because both the source and load act as line terminations.

Configuration Name (if any)	(Driver) Source Resistance	(Receiver) Load Resistance	Signal Characteristics	Optimum Receiver Threshold	Line Receivers Allowed at Other Than Load End of Line?	Comments
Unterminated	$\ll R_0$	$\gg R_0$	Ringing Pronounced	0.5 V_{SS}	Yes	Undershoot May Cause Data Errors
Parallel Terminated	$\ll R_0$	$= R_0$	Excellent Fidelity	0.5 V_{SS}	Yes	Load Resistor Consumes Power $P_L = \frac{(V_{SS})^2}{R_L}$
	$\ll R_0$	$\ll R_0$	Awful—Different Signals at Each Point on the Line	NA	No	Not Generally Useful
Series Terminated or Backmatched Driver	$= R_0$	$\gg R_0$	Load Signal Excellent	0.5 V_{SS}	No	Reduced Power Consumption Over Parallel Termination
Fully Matched	$= R_0$	$= R_0$	Excellent Fidelity	0.25 V_{SS}	Yes	Greater Tolerances on Resistors Allowed for Same Fidelity as Parallel Termination
	$= R_0$	$< R_0$	Load Signal Like a One-Shot	NA	NA	Not Generally Useful for Data, is Useful as Pulse Generator
	$\gg R_0$	$\gg R_0$	Exponential Like Signal Waveforms	0.5 V_{SS}	Yes	Low Power Consumption. Increased Delay due to Signal "Rise" Times.
	$\gg R_0$	$= R_0$	Small Signal Amplitude and Excellent Fidelity	0.5 V_{SS}	Yes	Produces Only Small Signal Voltages Compared with Other Methods. Uses Current Sinking Drivers such as the 75110A.
	$\gg R_0$	$< R_0$	Very Small Signal Amplitudes, also Ringing	NA	NA	Not Generally Useful

FIGURE 15. Summary of Effects

EFFECT OF SOURCE RISE TIME ON WAVEFORMS

Previously, it was assumed that the source-produced signal rise time was always much less than the line time delay (τ). Because the waveforms for the source and load voltage were the superposition of incident and reflected waves occurring at their proper times, and because the shape of each wave was a square edged step function, the resultant source and load waveforms were thus also square edged, or *ideal* in nature. In many practical cases, particularly when line length is short, the source excitation possesses a finite, and non-negligible, rise time. Therefore, depending on the ratio of rise time to line delay, it is possible to have a new wave start arriving at the point of interest *before* the previous wave can reach its final value. The net waveform for voltage or current at that point, then, would consist of the superposition of two or more waves during their time of overlap. To study the superposition effect on signal waveforms, the source excitation is represented as a simple linear ramp rise to its final value of V_{0+}, so

$$e(t) = 0 \text{ for } t < 0$$

$$e(t) = V_{0+} \bullet t/t_r \text{ for } 0 \le t \le t_r$$

$$e(t) = V_{0+} \text{ for } t > t_r$$

and where t_r represents the 0-to-100% source rise time. The circuit model and its lattice diagram are shown in *Figure 16*. The values of R_S, R_0 and R_L were chosen to equal those of an actual circuit on hand, allowing the theoretical waveforms, obtained by graphical superposition, to be compared with the measured response of an actual circuit.

Figure 17 shows the load voltage v_L, source voltage v_S and source current i_S waveforms versus time for a circuit with a source rise time very much less than τ. The actual waveforms for v_L, v_S and i_S are composed of the superposition of both incident and reflected waves in their proper time sequence. In the figures, these waves are shown as dotted lines. Each wave represents the sum of the incident wave plus its reflection. The resultant v_L, v_S and i_S waveforms (shown as solid lines) are the superposition of the waves represented by the dotted lines. With the exception of a slight rounding of the edges, the actual waveforms for the circuit, shown in the oscilloscope photograph in *Figure 17*, closely approximate the waveforms predicted by theory.

Source					Load				
t in (τ)	$v_I + v_r$ (V)	$I_I + I_r$ (mA)	v_S (V)	I_S (mA)	t in (τ)	$v_I + v_r$ (V)	$I_I + I_r$ (mA)	v_L (V)	I_L (mA)
0	0.9400	12.53	0.9400	12.53	1	1.8500	0.40	1.8500	0.40
2	0.1224	−22.64	1.0624	−10.10	3	−1.5500	−0.34	0.3000	0.06
4	−0.1026	18.97	0.9599	8.87	5	1.2986	0.28	1.5986	0.35
6	0.0859	−15.90	1.0458	−7.03	7	−1.0881	−0.24	0.5106	0.11
8	−0.0720	13.32	0.9738	6.29	9	0.9116	0.20	1.4222	0.31
10	0.0603	−11.17	1.0341	−4.87	11	−0.7638	−0.17	0.6584	0.14
12	−0.0505	9.36	0.9836	4.48	13	0.6399	0.14	1.2983	0.28
14	0.0424	−7.84	1.0259	−3.36	15	−0.5362	−0.12	0.7622	0.16
16	0.0355	6.57	0.9904	3.21	17	0.4492	0.10	1.2114	0.26

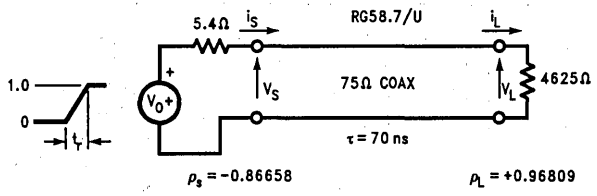

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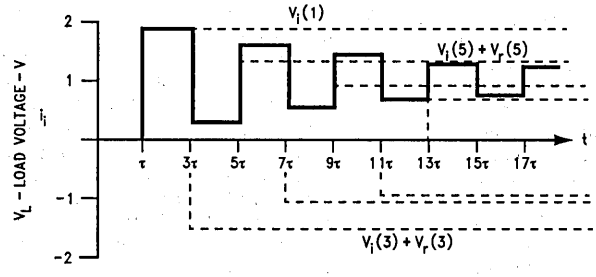
FIGURE 16. Transmission Line Model and Its Lattice Diagram



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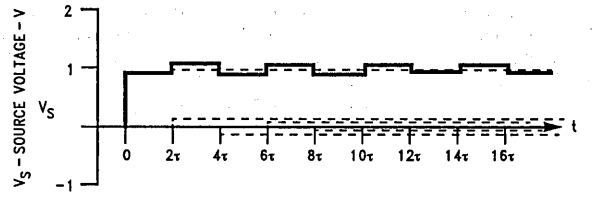

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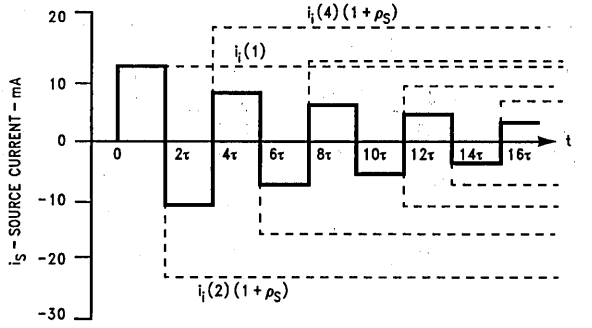

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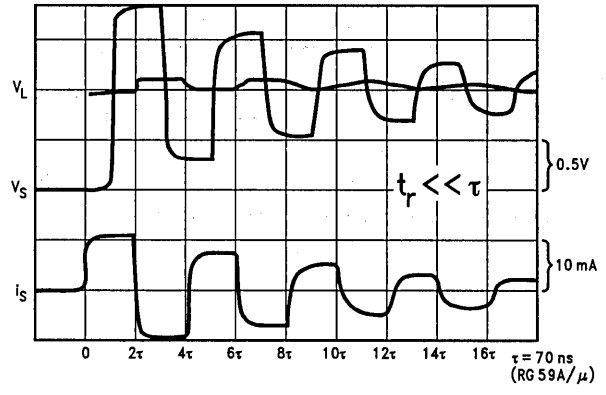

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FIGURE 17. Waveforms for $t_r = 2 \ll \tau$

If the source excitation is adjusted so that its 0-to-100% rise time t_r is equal to 2τ, each of the $v_i + v_r$ and $i_i + i_r$ waveforms must be modified to include this rise time. The waves will have the same final value as predicted by the lattice diagram, but they now require two line time delays to reach this final value. The v_L, v_S and i_S waveforms consist of the superposition of these linear ramps. Because each wave reaches its final value just as a new wave arrives, their superposition converts the square edged v_L, v_S and i_S waveforms into triangular waveforms. This is shown in *Figure 18*. The accompanying oscilloscope plot shows the close correspondence between the actual and theoretical waveforms whereas an additional oscilloscope photograph in *Figure 18* shows the actual waveforms for the case where $t_r = \tau$. Not surprisingly, the $t_r = \tau$ case changes the v_L, v_S and i_S waveforms of the $t_r \ll \tau$ case into trapeziodal forms because each arriving wave reaches its final value well before a new wave arrives.

If the source excitation is adjusted such that its rise time equals three line delays $t_r = 3\tau$, the $v_i + v_r$ and $I_i + i_r$ waves overlap for a period of time equal to τ. That is, each wave reaches only ⅔ of its final value when a new wave starts arriving. Considering the waveform, the load voltage from time τ to 3τ is

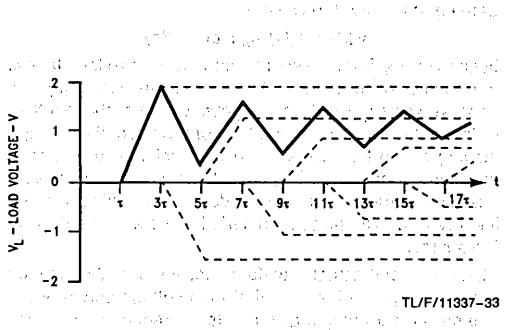
$$v_i(1)\,(1 + \rho_L)\,e\,(t - \tau)$$

Starting at $t = 3\tau$, the wave

$$v_i(3) = v_i(1)\rho_S\rho_L\,e(t - 3\tau).$$

begins arriving from the source, and the load voltage then is the superposition of these two waves. Because $v_i(3)$ is a negative wave ($\rho_S < 0$), the algebraic sum of the last third of the first wave and the first third of the second wave $v_i(3)$ arriving at the load causes the load voltage to reduce in amplitude from the ($t_r \ll \tau$) case. Likewise, the source voltage and source current show reduced amplitudes over the ideal case, due to the overlap period of the waves arriving at the source.

Theoretical and actual waveforms for the $t_r = 3\tau$ case are shown in *Figure 19*. Notice that load voltage perturbations and source current i_S requirements are reduced from those of the $t_r \ll \tau$ case. Similarly, the ratio of t_r to τ can be successively increased. This results in reduced ringing on the load voltage and reduced source current due to the overlapping of more and more $v_i + v_r$ (or $i_i + i_r$) waves. Actual and theoretical waveforms for t_r equal to 4τ, 6τ, and 8τ are shown in *Figures 20, 21* and *22*, respectively. In each case, as the t_r to τ ratio is increased, the instantaneous source and load voltages become more equal. The source current is also reduced so that the circuit exhibits fewer reflection effects and the transmission line itself can be considered as a simple interconnection from dc circuit theory.



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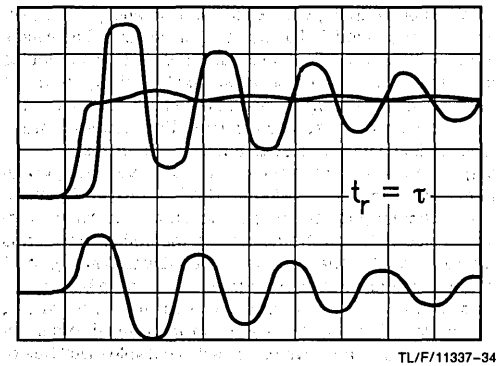
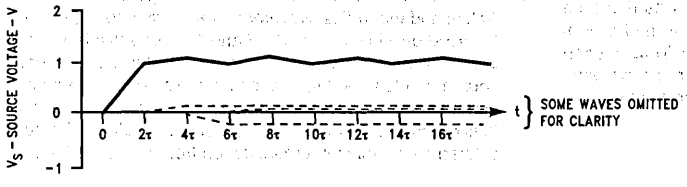
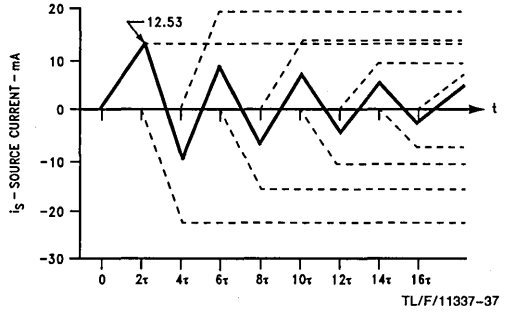


TL/F/11337–34



TL/F/11337–35



TL/F/11337–37

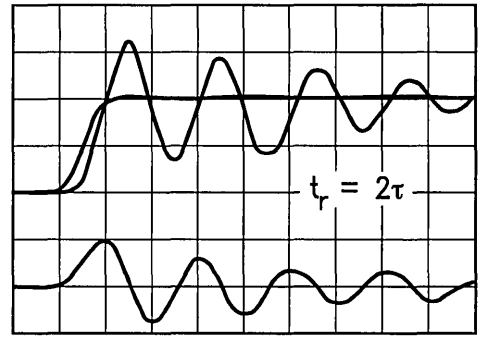


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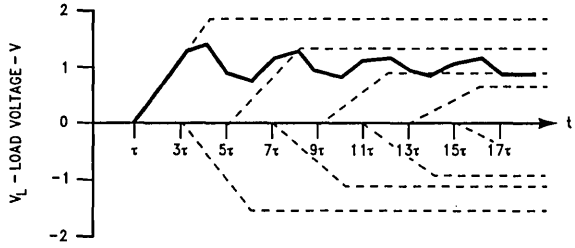
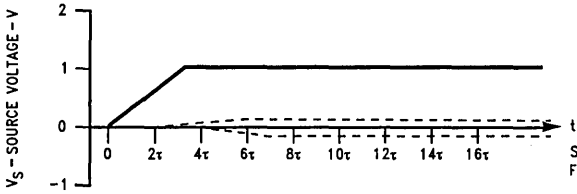
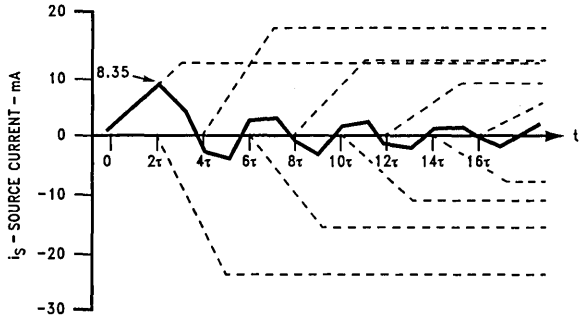
FIGURE 18. Waveforms for $t_r = 2\tau$



TL/F/11337–38



TL/F/11337–39



TL/F/11337–41

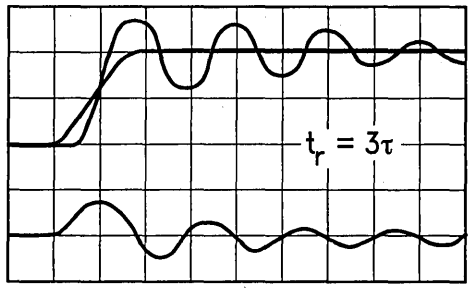


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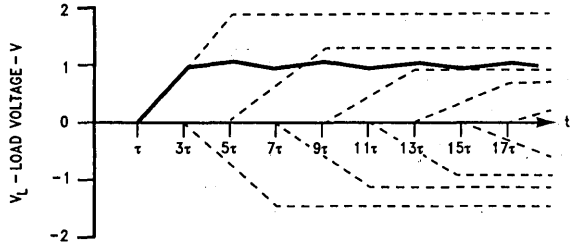
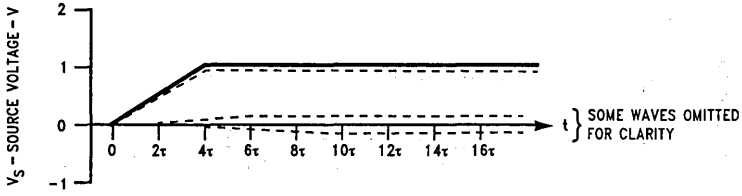
FIGURE 19. Waveforms for $t_r = 3\tau$



TL/F/11337–42



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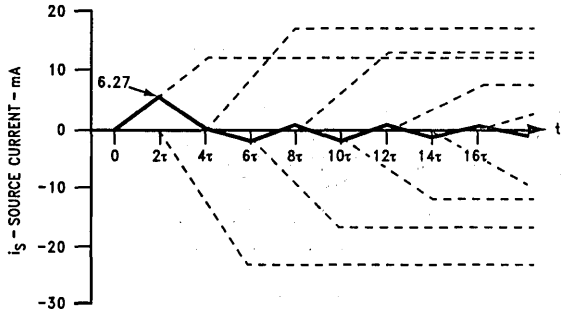

TL/F/11337–45

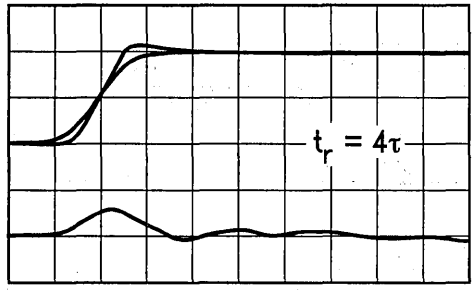

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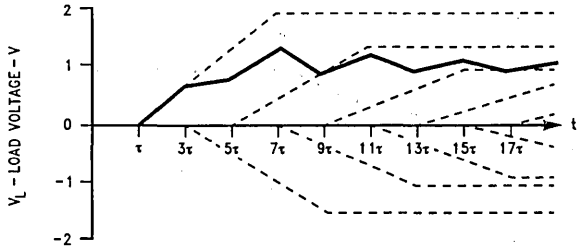
FIGURE 20. Waveforms for $t_r = 4\tau$



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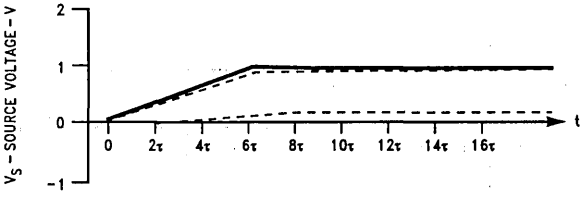
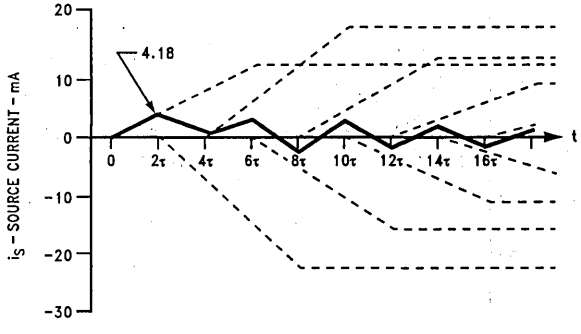


TL/F/11337–47



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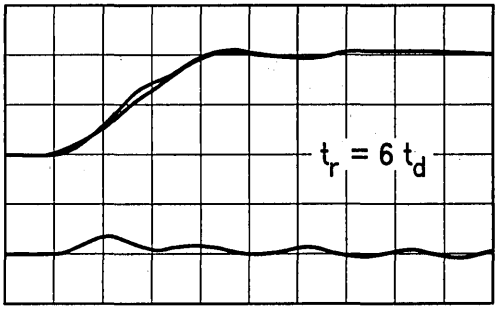

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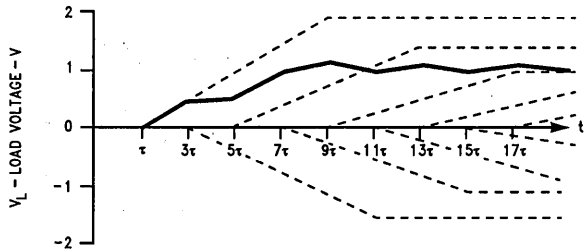
FIGURE 21. Waveforms for $t_r = 6\tau$



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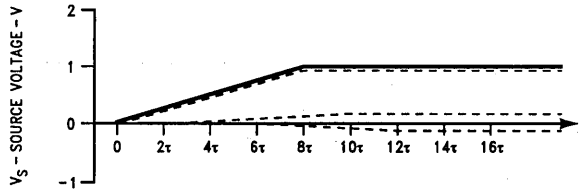

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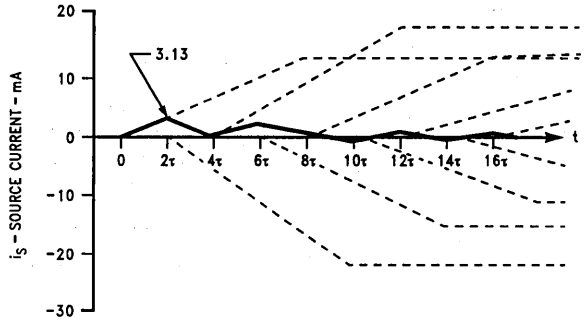

TL/F/11337–53

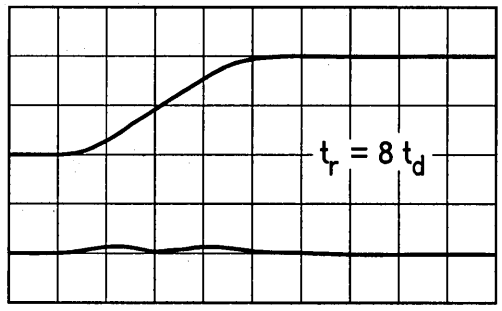

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FIGURE 22. Waveforms for $t_r = 8\tau$

Using the t_r to τ ratio to reduce reflection effects has many practical advantages in digital design. The low source and high input resistance of TTL or ECL circuits allows one gate to drive many receiving gates. The reflection effects of this unterminated combination, however, can cause data errors or at least lead to reduced noise immunity due to the pronounced load voltage undershoot. Since the rise and fall times of these devices are easily measured, a maximum line length can be set such that the resulting t_r to τ ratio provides the desired reduction in ringing. This is the primary basis for the wiring rules of each logic family and, usually, the t_r to τ ratio is chosen somewhere between 3:1 and 4:1. As an example, the rise and fall time for normal TTL is $t_{10\%-90\%} = 6$ ns. When this is converted to an equivalent linear 0% to 100% time, $t_r = 8$ ns. A common propagation delay of 1.7 ns/ft, in combination with the requirement that $t_r = 3\tau$, gives the maximum line length of approximately 18 inches. This corresponds with the published recommendation of the various manufacturers for the 74 series TTL circuits. A similar computation of the rise and fall times for other logic families yields their respective line length recommendations. The faster families require shorter line lengths for the same t_r to τ ratio, and slower logic families allow relatively longer line length. This ratio can also be used to make stubs or taps on lines "disappear". In other words, if the stub's time delay is made very short when compared to the t_r of the signal at the stub line location, the stub reflections will have a minimal effect on the line signals. A stub length to generate a t_r to τ ratio of greater than 8:1 is usually considered adequate to negate the stub reflections.

The third primary application of the t_r to τ ratio for controlling reflection effects is that used in some standard data communications interfaces such as EIA/TIA-232-E (RS-232). Here, driver slew rate is explicitly controlled. This, along with the implied maximum interconnect cable length serves to produce a t_r to τ ratio of 3:1 or greater. This, in turn, reduces the reflection effects inherent in a voltage source driver, unterminated line system. The main disadvantage of using the t_r to τ ratio to control reflection effects is in the overall time for the signal representing the data to rise above the receiver threshold level. With the parallel terminated method, the minimum time delay was τ or one line delay. When the t_r to τ ratio is used, an additional delay time of approximately 0.5 t_r is added to the line delay yielding, therefore, a greater effective signal propagation delay. This increased delay may or may not be acceptable in the desired system so the trade-off between ease of usage of the unterminated case must be weighed against the increased effective signal delay over that delay obtainable with the terminated case.

REFERENCES

See AN-806 and AN-808

8

Long Transmission Lines and Data Signal Quality

National Semiconductor
Application Note 808
Kenneth M. True

OVERVIEW

This application note explores another important transmission line characteristic, the reflection coefficient. This concept is combined with the material in AN-806 to present graphical and analytical methods for determining the voltages and currents at any point on a line with respect to distance and time. The effects of various source resistances and line termination methods on the transmitted signal are also discussed. This application note is a revised reprint of section four of the Fairchild Line Driver and Receiver Handbook. This application note, the third of a three part series (See AN-806 and AN-807), covers the following topics:

- Factors Causing Signal Wave-Shape Changes
- Influence of Loss Effects on Primary Line Parameters
- Variations in Z_0, $\alpha(\omega)$ and Propagation Velocity
- Signal Quality—Terms
- Signal Quality Measurement—The Eye Pattern
- Other Pulse Codes and Signal Quality

INTRODUCTION

Transmission lines as discussed in AN-806 and AN-807 have always been treated as ideal lossless lines. As a consequence of this simplified model, the signals passing along the lines did not change in shape, but were only delayed in time. This time delay is given as the product of per-unit-length delay and line length ($\tau = \ell\,\delta$). Unfortunately, real transmission lines always possess some finite resistance per unit length due to the resistance of the conductors composing the line. So, the lossless model only represents *short* lines where this resistance term can be neglected. In AN-806 the per-unit-length line parameters, L, R, C, G, were assumed to be both constant and independent of frequency (up to the limits mentioned, of course). But with real lines, this is not strictly correct as four effects alter the per-unit-length parameters, making some of them frequency dependent. These four effects are skin effect, proximity effect, radiation loss effect, and dielectric loss effect. These effects and how they influence the intrinsic line parameters are discussed later in this application note. Since these effects make simple ac analysis virtually impossible, operational (Laplace) calculus is usually applied to various simplified line models to provide somewhat constrained analytical solutions to line voltages and currents. These analytical solutions are difficult to derive, perhaps even more difficult ot evaluate, and their accuracy of prediction depends greatly on line model accuracy. Analytical solutions for various lines (primarily coaxial cables) appear in the references, so only the salient results are examined here.

Engineers designing data transmission circuits are not usually interested in the esoterica of lossy transmission line theory. Instead, they are concerned with the following question: given a line length of x feet and a data rate of n bps, does the system work—and if so—what amount of transition jitter is expected? To answer this question using analytical methods is quite difficult because evaluation of the expressions representing the line voltage or current as a function of position and time is an involved process. The references at the end of this application note provide a starting point to generate and evalute analytical expressions for a given cable.

The effects on the LRCG line parameters, the variations in Z_0, $\alpha(\omega)$, and propagation velocity as a function of applied frequency are discussed later in this application note. Using an empirical approach to answer the "how far—how fast" question involves only easily made laboratory measurements on that selected cable. This empirical approach, using the binary eye pattern as the primary measurement tool, enables the construction of a graph showing the line length/data rate/signal quality trade-offs for a particular cable. The terms describing *signal quality* are discussed later in this application note. The technique of using actual measurements from cables rather than theoretical predictions is not as subject to error as the analytical approach. The only difficulties in the empirical method are the requirements for a high quality, real time (or random sampling) oscilloscope and, of course, the requisite amount of transmission line to be tested.

Also discussed in this application note are commonly used pulse codes.

FACTORS CAUSING SIGNAL WAVE SHAPE CHANGES

In AN-806 and AN-807, it was assumed that the transmission lines were ideal so the step functions propagated along the lines without any change in wave shape. Because a single pulse is actually composed of a continuous (Fourier) spectrum, the phase velocity independence on an applied frequency, and the absence of attenuation (R = 0, G = 0) of the ideal line always allows the linear addition of these frequency components to reconstruct the original signal without alteration. For real lines, unfortunately, the series resistance is not quite zero, and the phase velocity is slightly dependent on the applied frequency. The latter results in *dispersion; i.e.*, the propagation velocity will differ for the various frequencies, while the former results in signal *attenuation* (reduction in amplitude). This attenuation may also be a function of frequency. Attenuation and dispersion cause the frequency components of a signal, at some point down the line, to be quite different from the frequency components of the signal applied to the input of the line. Thus, at some point down the line, the frequency components add together to produce a wave shape that may differ significantly from the input signal wave shape. In many ways, then, a real transmission line may be thought of as a distributed lowpass filter with loss. The fast rise and fall times of the signals become progressively "rounded" due to attenuation and dispersion of the high frequency signal components.

It should be noted that there is a theoretical condition where attenuation is independent of frequency and dispersion is zero. This results in a line causing signal amplitude reduction, but no change in signal wave shape. This condition was first discussed by Heavyside and is called the *distortionless* line. To make a line distortionless, the primary line parameters must satisfy the relation (R/L) = (G/C). Because for real lines (R/L) > (G/C), the distortionless line is only of historical interest, and it is not possible to satisfy the (R/L) = (G/C) condition over a sufficiently wide bandwidth to allow a proper transmission of short duration pulses. Over a limited frequency range such as that encountered in telephony (0 kHz–4 kHz), the L term can be increased by either adding lumped inductances at fixed intervals along the line or by winding a magnetic material (as a thin tape) around the conductors of the line throughout its length. Lumped loading is commonly applied to long telephone circuits to reduce the signal attenuation over a narrow frequency range; however this linearity is at the expense of in-band attenuation and non-linear delay distortion. The distributed loading method has been tried, but the mechanical characteristics of the magnetic materials have made the winding process very difficult. In any event, neither method allows short pulses to retain their wave shapes. The interest in line loading to produce the Heavyside condition for pulse transmission is therefore largely academic.

The following sections discuss the origins of the second-order effects—skin effect, proximity effect, radiation loss effect, and dielectric loss effect—and their influence on the LRCG transmission line parameters.

- Skin Effect: The phenomenon is based on two facts: a current flow in any real conductor produces an electric field given by Ohm's Law; the current distribution and/or magnetic field distribution in a conductor is frequency dependent. For dc current in a single isolated conductor, the current density is uniform across the conductor. When alternating current is used, the current density is not uniform across the conductor. Instead, the current tends to concentrate on the conductor surface. Current density continuously increases from the conductor center to its surface, but for practical purposes, the current *penetration depth*, d, is assumed as a dividing line for current density. The current is assumed to flow in a imaginary cylinder of thickness d with a constant current density throughout the cylinder thickness. Distribution of current densities for both actual and assumed models is shown in *Figure 1*.

  It can be seen that for *classical* skin effects, the penetration depth is given by

$$d = K\frac{1}{\sqrt{f}} \qquad (1)$$

  where $K = 1/\sqrt{\pi\mu\sigma}$, μ = magnetic permeability of the conducting material expressed in henries per unit length, and σ = conductivity of the conducting material. For MKS (SI) units and for a copper conductor

$$\sigma = 5.85 \times 10^7\ (\Omega\ \text{meter})^{-1}$$

$$\mu = 4\pi \times 10^{-7}\ (\text{H/meter})$$

  in which case, d would be the penetration depth expressed in meters.

  Because the skin effect reduces the equivalent conductor cross-sectional area, increasing frequencies cause an increase in the effective resistance per unit length of the line. This in turn leads to signal attenuation increasing with frequency. If the frequency response of a cable is plotted on log-log graph paper, log dB, or Nepers vs log frequency, the curve slope will be 0.5 if the cable losses are primarily governed by *classical* skin effects. The slope of the attenuation curve, along with the attenuation at a particular frequency, can be used to estimate coaxial cable transient response as a function of length.[2, 4]

*See Reference 2 and 4.

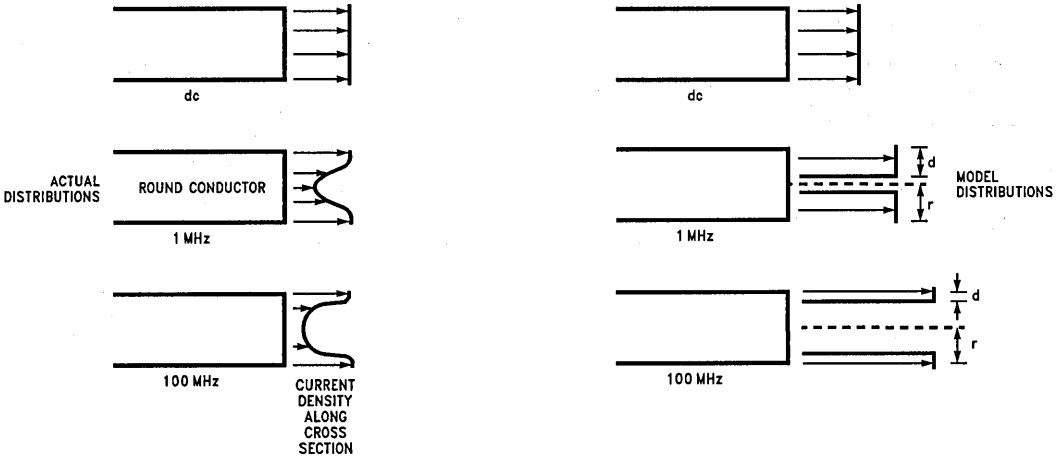

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FIGURE 1. Current Distributions Across and Conductor for Several Frequencies

- Proximity Effect: This is a current density redistribution in a conductor due to the mutual repulsion (or attraction) generated by currents flowing in nearby conductors. The current density at those points on the conductor close to neighboring conductors varies from the current density when the conductor is isolated from other conductors. This current density redistribution reduces the effective cross-sectional area of the conductor, thereby increasing the per-unit-length line resistance. This effect is a function of the conductor diameters, the separation of the conductors from each other, and frequency. The analytical evaluation of the proximity effect is quite complicated and except for certain limited cases*, no general rule of thumb expressions have been proposed. The proximity effect is not present in coaxial cables because of their circular symmetry. The proximity effect is a significant contributor to signal losses particularly in cases of a twisted pair or parallel wire lines.
- Radiation Loss: Radiation losses cause an apparent rise in resistance per unit length increasing with frequency. The mechanism of radiation loss is energy dissipation either as heat or magnetization via eddy currents in nearby metallic or magnetic masses, with the eddy currents induced by line currents. Coaxial cables do not exhibit this effect because the signal magnetic field is confined between the shield and the outside of the center conductor. Ideally, the magnetic field produced by shield current cancels the field produced by current in the center conductor (for points outside the shield).

  Both twisted pair and parallel wire lines exhibit radiation losses and these losses contribute to the effective per-unit-length line resistance. Radiation loss is dependent to a large extent on the characteristics of the materials close to the line; so radiation loss is quite difficult to calculate, but can be measured if necessary.
- Dielectric Loss Effect: Dielectric losses result from leakage currents through the dielectric material. This causes an increase in the shunt conductance per unit length and produces signal attenuation. Fortunately, for most dielectric materials in common use, this loss is very small particularly for frequencies below 250 MHz. For most practical purposes, then, dielectric losses may be neglected as they are usually overshadowed by skin effect losses.

INFLUENCE OF LOSS EFFECTS ON PRIMARY LINE PARAMETERS

Resistance Per Unit Length, R. It is composed of a basic dc resistance term R_{dc} plus the contributions of skin effect, proximity effect and radiation loss effect. For coaxial lines, the proximity and radiation loss effects are negligible in most cases, so the primary contribution is made by the skin effect. Thus the resistance per unit length becomes

$$R \doteq R_{dc} + Ks^m \qquad (2)$$

where $0 < m < 1$.

For 2-wire lines (twisted pair, parallel wire), the resistance per unit length is increased by the skin effect. For closely spaced wires, however, the proximity effect also contributes significantly to a resistance increase. Radiation loss should also be included, but is very difficult to calculate because it depends on the surroundings of the line.

Inductance Per Unit Length, L. It can be shown** that, as the frequency is increased, the skin effect, proximity effect, and radiation loss effect cause a reduction in the effective per-unit-length self-inductance of the line.

Capacitance Per Unit Length, C. This depends primarily on the dielectric constant of the insulating medium and conductor geometry. This term is constant over a wide range of frequencies for most dielectrics (Teflon®, Polyethylene). For Polyvinylchloride (PVC) insulation, the relative dielectric constant shows a decrease as frequency increases ($\epsilon_r \approx 4.7$ @ 1 kHz, $\epsilon_r \approx 2.9$ @ 100 MHz). The capacitance per unit length, therefore, will show a decrease corresponding with increasing frequency for PVC insulation and little change for most other dielectrics.

Conductance Per Unit Length, G. Because resistance per unit length usually has a much greater magnitude, this value is negligible. When this term cannot be neglected, it is represented as

$$G = \omega C \tan\phi \qquad (3)$$

where C is capacitance per unit length, ω is the angular frequency ($= 2\pi f$) and $\tan\phi$ is a dielectric material coefficient. The angle ϕ is called the dielectric loss angle. This angle is usually quite small (< 0.005 radians) for the majority of dielectrics up to several hundred megahertz.

VARIATIONS IN Z_0, $\alpha(\omega)$, AND PROPAGATION VELOCITY

The variations in the primary line parameters as a function of frequency shown by *Figure 2* have a profound influence on the three secondary line parameters of characteristic impedance, attenuation, and velocity of propagation.

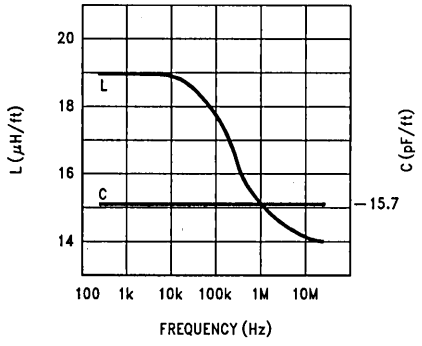
In the expression for the characteristic impedance of a line,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

at low frequencies, $j\omega L$ is small compared to R, and G is small compared to $j\omega C$. So the characteristic impedance is $\sqrt{R/j\omega C}$. At high frequencies, the increase in R is overshadowed by $j\omega L$ even though L is being reduced. With G still much smaller than $j\omega C$, the characteristic impedance is almost a pure resistance $R_0 = \sqrt{L/C}$. The behavior of the characteristic impedance as a function of frequency ($Z_0 = R_0 - jX_0$) is shown in *Figure 3*.

*See References Arnold[11] and Dwight[12].

**See References 5 and 6



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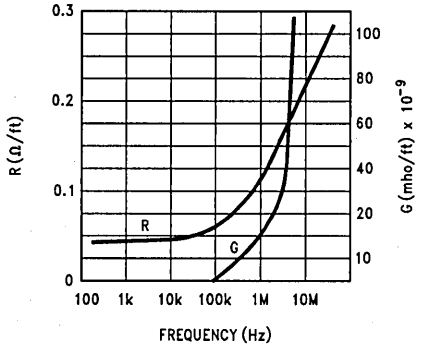

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FIGURE 2. Variations in Primary Parameters as a Function of Frequency (22 AWG Polyethylene Insulated Twisted Pair)

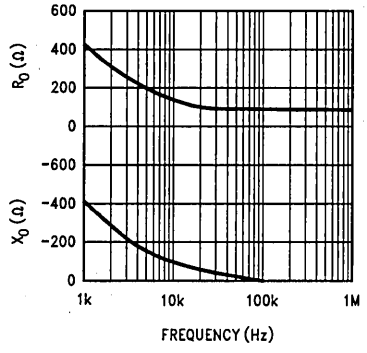

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FIGURE 3. Typical Variation in Z_0 as a Function of Frequencies

Typical behavior of the line attenuation as a function of frequency is shown in *Figure 4*. This line attenuation is the real part of the equation

$$\gamma(\omega) = \sqrt{(R + j\omega L)(G + j\omega C)}.$$

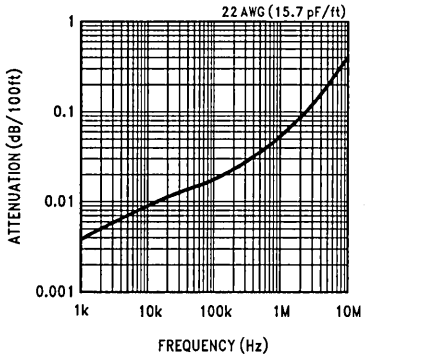

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FIGURE 4. Attenuation vs Frequency

The change in resistance is the primary contributor to the attenuation increase as a function of frequency. For coaxial cables, this resistance increase is due primarily to the skin effect ($R_{SK} = Kf^m$). The slope of the attenuation curve on a log-log graph (log dB vs log frequency), therefore, is essentially linear and, at the same time, equal to m. For twisted pair and parallel wire lines, proximity effects and radiation losses make the curves less linear, but for high frequencies (over 100 kHz), the attenuation expressed in nepers per unit length is approximated by

$$\alpha \cong \frac{R}{2}\sqrt{\frac{C}{L}} \qquad (4)$$

The R term is, of course, the sum of the dc resistance, plus the incremental resistance due to skin, proximity and radiation loss effects. This R term usually varies as follows.

$$R_{SK} = Kf^m$$

where $0.6 \leq m < 1.0$

The signal velocity propagation ($v = \omega/\beta$) is given by the imaginary part of the propagation constant γ. As shown in AN-807, v is a constant given by $v = \sqrt{LC}$ for lossless lines. For real lines, this value is approached at high frequencies. At low frequencies, however, (when ω is small compared to R/L or G/C), then $v_{LF} \cong (C/2)\sqrt{R/G}$ and the velocity is reduced. The propagation velocity as a function of frequency is shown in *Figure 5*. This variation in signal velocity as a function of signal frequency is *dispersion* which was previously discussed.

The signal at a point down the line represents the sum of that original signal's Fourier spectrum. Because both the attenuation and propagation velocity of these Fourier components increase with frequency, the resultant signal shape at that point down the line depends greatly on the winners of the race to get to that point. The high frequency components, with their faster propagation velocities, arrive first, but the increased attenuation minimizes their effect. The low frequency signals arrive later, but the reduced attenuation allows them a greater influence on the resultant signal. In general, the output signal from the line should show a relatively fast rise up to some signal value (20% to 50% of the final value). This is due to arrival of the high frequency components, followed by a more leisurely rise to the final value as the slower, low frequency components arrive.

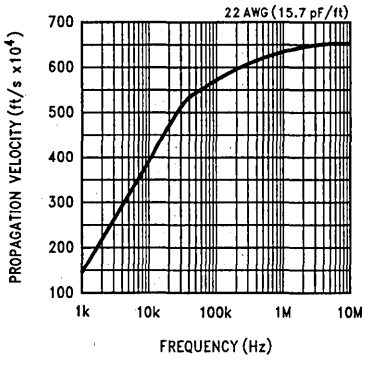

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FIGURE 5. Propagation Velocity vs Frequency

SIGNAL QUALITY—TERMS

Before the concepts presented in the previous sections can be used to answer the "how far—how fast" question, some familiarity with the terms describing data and signal quality is necessary.

The primary objective of data transmission is the transfer of *information* from one location to another. The information here is *digital* in nature; i.e., a finite number of separate states or choices. This is in contrast to *analog* which has an infinite number of separate states or a continuous range of choices. The digital information is *binary* or two-valued; thus two different, recognizable electrical states/levels are used to symbolize the digital information. A binary symbol is commonly called a binary-digit or *bit*. A single binary symbol or bit, by itself, can represent only one of two possible things. To represent alphabetic or numeric characters, a group of bits is arranged to provide the necessary number of unique combinations. This arrangement of bits which is then considered an information unit is called a *byte*. In the same manner that a group of bits can be called a byte, a collection of bytes, considered as a unit, is called a *word*. Selective arrangement of seven bits will provide 2^7 (or 128) distinct character combinations (unique bytes). The American Standard Code for Information Interchange (ASCII) is an excellent example of just such an arrangement—upper and lower case alphabetic, zero to nine numeric, punctuation marks, and miscellaneous information-code control functions.

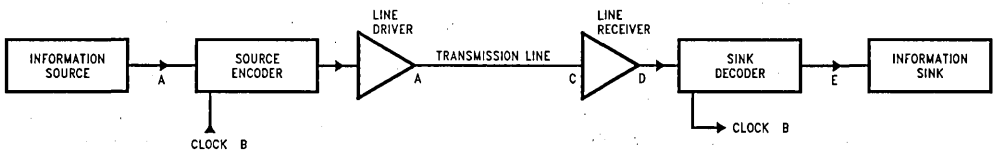
Now with the means for representing information as bits or bytes, and the means for transmission of the bits (symbols) from one location to another (transmission line), the remaining task is to ensure that a particular bit arriving at its destination is interpreted in the proper context. To achieve this, both the sender and receiver of the data must accomplish the five following requirements.

1. Agree upon the nominal rate of transmission; or how many bits are to be emitted per second by the sender.
2. Agree upon a specified information code providing a one-to-one mapping ratio of information-to-bit pattern and vice versa.
3. Establish a particular scheme whereby each bit can be properly positioned within a byte by the receiver of the data (assuming that bit-serial transmission is used).
4. Define the protocol (handshaking) sequences necessary to ensure an orderly flow of information.
5. Agree to the electrical states representing the logic values of each bit and the particular pulse code to be used.

These are by no means all of the points that must be agreed upon by sender and receiver—but these are probably the most important. Items 2, 3 and 4 are more or less "software" type decisions, because the actual signal flow along the transmission line is usually independent of these decisions. Because items 1 and 5 are much more dependent on the characteristics of line drivers, line receivers, and transmission lines, they are the primary concern here.

Figure 6 represents the components of a typical data transmission system. The *information source* can be a computer terminal or a digitized transducer output, or any device emitting a stream of bits at the rate of one bit every t_B seconds. This establishes the *information rate* of the system at $1/t_B$ bits per second. The information source in the figure feeds a *source encoder* which performs logic operations not only on the data, but also on the associated clock and, perhaps, the past data bits. Thus, the source encoder produces a binary data stream controlling the *line driver*. The line driver interfaces the source internal logic levels (TTL, CMOS, etc.) with transmission line current/voltage requirements. The transmission line conveys signals produced by the line driver to the line receiver. The line receiver makes a decision on the signal logic state by comparing the received signal to a decision threshold level, and the *sink decoder* performs logic operations on the binary bit stream recovered by the line receiver. For example, the sink decoder may extract the clock rate from the data or perhaps detect and correct errors in the data. From the optional sink decoder, the recovered binary data passes to the *information sink*—the destination for the information source data.

Assume for the moment that the source encoder and sink decoder are "transparent"; that is, they will not modify the binary data presented to them in any way. Line driver signals, then, have the same timing as the original bit stream. The data source emits a new bit every t_B seconds. The *pulse code* produced by the source encoder and line driver is called Non-Return to Zero (NRZ), a very common signal in TTL logic systems. A sample bit pattern with its NRZ representation is shown in *Figure 7a*. The arrows at the top represent the *ideal instants*, or the times the signal can change state. The term *unit interval* is used to express the time duration of the shortest signaling element. The shortest signaling element for NRZ data is one bit time t_B, so the unit interval for NRZ data is also t_B. The rate at which the signal changes is the *modulation rate* (or signaling speed), and *baud* is the unit of modulation rate. A modulation rate of one baud corresponds to the transmission of one unit interval per second. Thus the modulation rate, in baud, is just the reciprocal of the time for one unit interval. A unit interval of 20 ms, therefore, means the signaling speed is 50 baud. The reason for differentiating between the *information rate* in bits per second (bps) and the *modulation rate* in baud will be clarified after examining some of the other pulse codes later in this application note.



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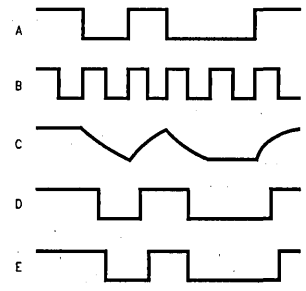

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FIGURE 6. Data Transmission System

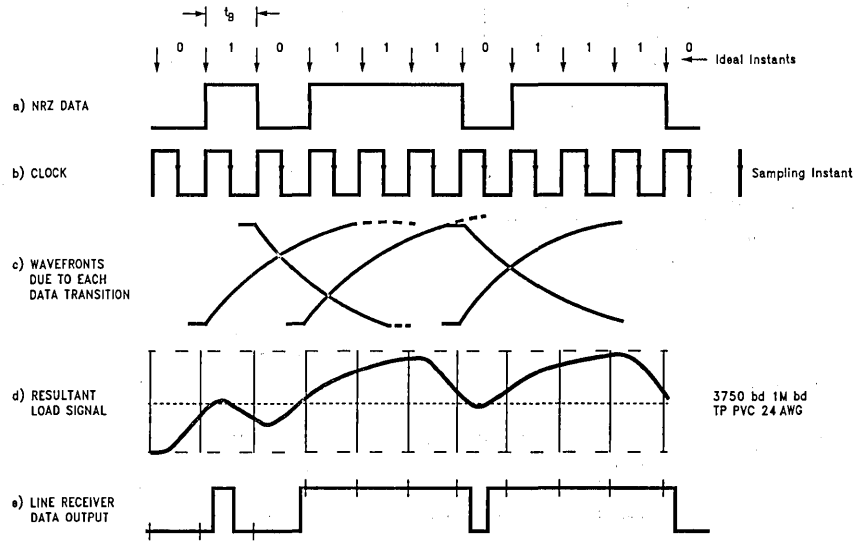

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FIGURE 7. NRZ Signaling

NRZ data should always be accompanied by a clock signal, *Figure 7b*, which tells the receiver when to sample the data signal and thus determine the current logic state. For the example in *Figure 7b*, the falling edge of the clock corresponds to the middle of the data bits, so it could be used to transfer the line receiver data output into a binary latch. The falling edge of the clock is thus the *sampling instant* for the data. The line receiver does have a *decision threshold* or slicing point so that voltages above that threshold level produce one logic state output, while voltages below the threshold produce the other logic state at the receiver output. The receiver may incorporate positive feedback to produce *hysteresis* in its transfer function. This reduces the possibility of oscillation in response to slow rise or fall time signals applied to the receiver inputs.

Previously in this application note, it was stated that the fast rise and fall times of signals, corresponding to the transisions between data bits, are rounded out and slowed down by a real transmission line. Each transition of the signal applied to the line by the line driver is transformed to a rounded out transition by the dispersion and attenuation of the transmission line. The resultant signal at the load end of the line consists of the superposition of these transformed transitions. The waves arriving at the load end of the line are shown in *Figure 7c* and their superposition is shown in *Figure 7d*. It is assumed that the line is terminated in its characteristic resistance so that reflections are not present. The receiver threshold level is shown here, superimposed on the resultant load signal, and the re-converted data output of the line receiver is shown in *Figure 7e* along with the ideal instants for the data transitions (tick marks).

Comparing the original data *(Figure 7a)* to the recovered data *(Figure 7e)* shows that the actual recovered data transitions may be displaced from their ideal instants (tic marks on *Figure 7e*). This time displacement of the transitions is due to a new wave arriving at the receiver site before the previous wave has reached its final value. Since the wave representing a previous data bit is *interfering* with the wave representing the present data bit, this phenomenon is called *intersymbol interference* (in telegraphy it is called *characteristic distortion*). The intersymbol interference can be reduced to zero by making the unit interval of the data signal quite long in comparison to the rise/fall time of the signal at the receiver site. This can be accomplished by either reducing the modulation rate for a given line length, or by reducing the line length for a given modulation rate.

Signal quality is concerned with the variance between the ideal instants of the original data signal and the actual transition times for the recovered data signal.

For synchronous signaling, such as NRZ data, the *isochronous distortion* of the recovered data is the ratio of the unit interval to the maximum measured difference irrespective of sign between the actual and theoretical significant instants.

The isochronous distortion is, then, the peak-to-peak time jitter of the data signal expressed as a percentage of the unit interval. A 25% isochronous distortion means that the peak-to-peak time jitter of the transition is 0.25 unit interval (max).

Another type of received-signal time distortion can occur if the decision threshold point is misplaced from its optimum value. If the receiver threshold is shifted up toward the *One signal level*, then the time duration of the One bits shortens with respect to the duration of the *Zero bits*, and vice versa. This is called *bias distortion* in telegraphy and can be due to receiver threshold offset (bias) and/or asymmetrical output levels of the driver. These effects are shown in *Figure 8*.

Bias distortion and characteristic distortion (intersymbol interference) together are called systemic distortion, because their magnitudes are determined by characteristics within the data transmission system. Another variety of time distortion is called *fortuitous distortion* and is due to factors outside the data transmission system such as noise and crosstalk, which may occur randomly with respect to the signal timing.

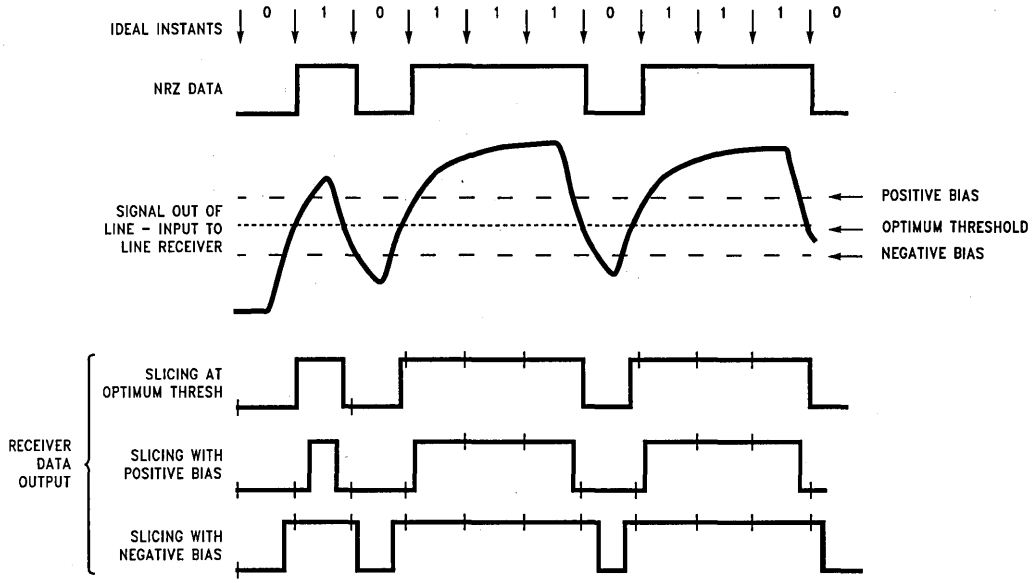

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FIGURE 8. Bias Distortion

SIGNAL QUALITY MEASUREMENT—THE EYE PATTERN

To examine the relative effects of intersymbol interference on random NRZ data and a "dotting"* pattern, see *Figure 9.* The top two waveforms represent the NRZ data and dotting pattern as outputs into two identical long transmission lines. The middle two traces illustrate the resultant signals at the line outputs and the bottom two traces show the data output of the line receivers. The respective thresholds are shown as dotted lines on the middle two traces. The arrows indicate the ideal instants for both data and dotting signals.

Notice that the dotting signal (D) is symmetrical, i.e., every One is preceded by a Zero and vice versa, while the NRZ data is random. The resultant dotting signal out of the line is also symmetrical. Because, in this case, the dotting half-cycle time is less than the rise/fall time of the line, the resultant signal out of the line (E) is a *partial response*—it never reaches its final level before changing. The dotting signal, due to its symmetry, does not show intersymbol interference in the same way that a random NRZ signal does. The intersymbol interference in the dotting signal shows up as a uniform displacement of the transitions as shown in *Figure 9f.* The NRZ data shows intersymbol interference, in its worst light, due to its unpredictable bit sequence. Thus, whenever feasibility of a data transmission system is to be tested, a random data sequence should be used. This is because a symmetrical dotting pattern or clock signal cannot always show the effects of possible intersymbol interference.

*The term dotting pattern is from telegraphy and means an alternating sequence of 1 bits and 0 bits (the "dot dot dot" etc). Note that an NRZ dotting pattern generates a signal which has a 50% duty cycle and a frequency of $\frac{1}{2}\ t_B$ (Hz).

A very effective method of measuring time distortion through a data transmission system is based on the eye pattern. The eye pattern, displayed on an oscilloscope, is simply the superposition—over one unit interval—of all the Zero-to-One and One-to-Zero transitions, each preceded and followed by various combinations of One and Zero, and also constant One and Zero levels. The name *eye pattern* comes from the resemblance of the open pattern center to an eye. The diagramatic construction of an eye pattern is shown in *Figure 10.* The data sequence can be generated by a pseudo-random sequence generator (PRSG), which is a digital shift register with feedback connected to produce a maximum length sequence.

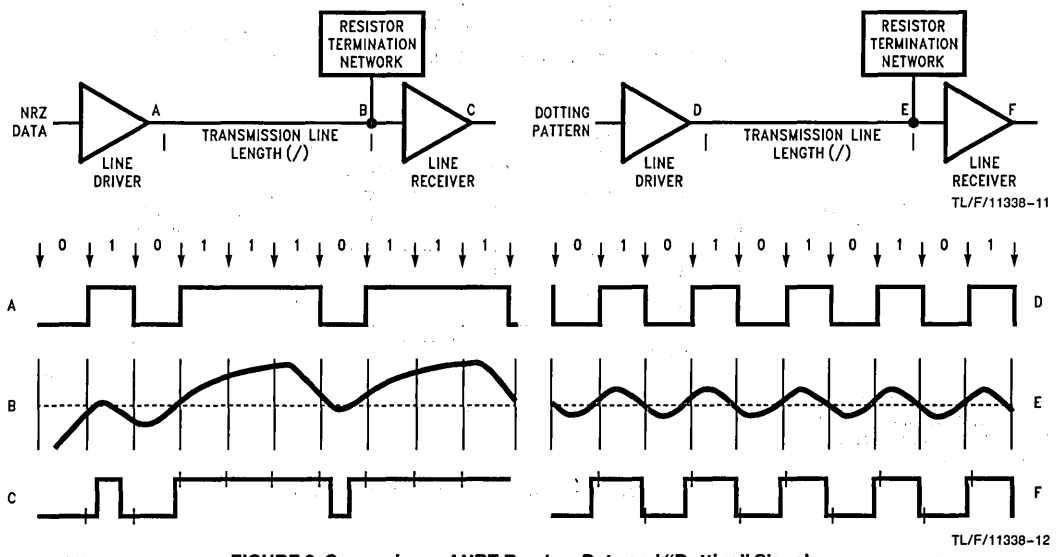


FIGURE 9. Comparison of NRZ Random Data and "Dotting" Signals

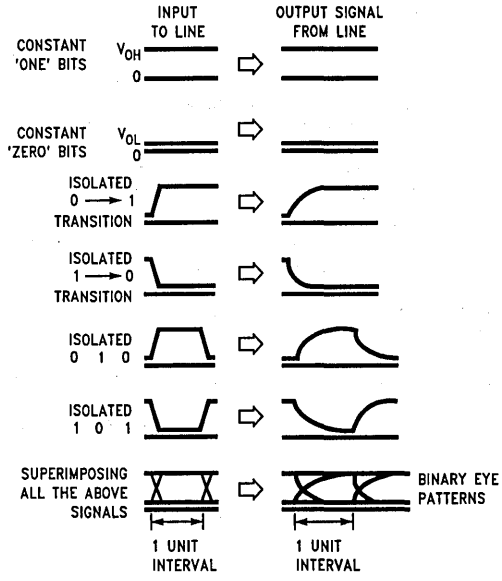
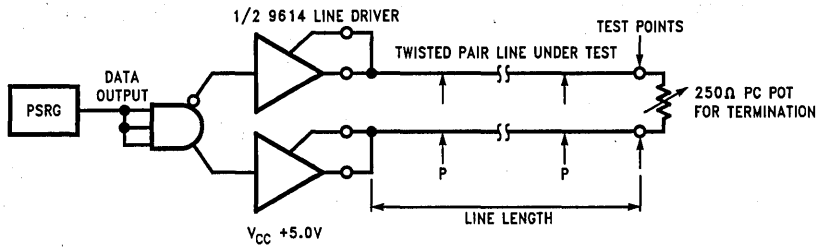


FIGURE 10. Formation of an Eye Pattern by Superposition

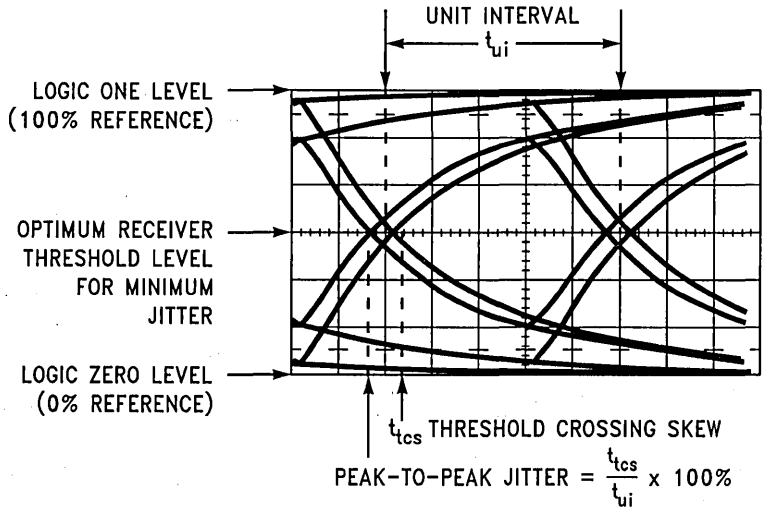


USE DIFFERENTIAL PROBE ACROSS TEST POINTS AND WIDE BANDWIDTH DIFFERENTIAL INPUT OSCILLOSCOPE TO DISPLAY EYE PATTERN.

FIGURE 11. Bench Set-Up to Measure Data Signal Quality

Several features of the eye pattern make it a useful tool for measuring data signal quality. *Figure 13* shows a typical binary eye pattern for NRZ data. The spread of traces crossing the receiver threshold level (dotted line) is a direct measure of the peak-to-peak transition jitter—isochronous distortion in a synchronous system—of the data signal. The rise and fall time of the signal can be conveniently measured by using the built-in 0% and 100% references produced by long strings of Zeros and Ones. The height of the trace above or below the receiver threshold level at the sampling instant is the noise margin of the system. If no clear transition-free space in the eye pattern exists, the eye is closed. This indicates that error-free data transmission is not possible at the data rate and line length with that particular transmission line without resorting to equalizing techniques. In some extreme cases, error-free data recovery may not be possible even when using equalizing techniques.

The eye pattern can also be used to find the characteristic resistance of a transmission line. The 250Ω printed circuit-type potentiometer termination resistor *(Figure 11)* can be adjusted to yield the minimum overshoot and undershoot of the data signal. *Figure 14* shows the NRZ data eye patterns for $R_T > R_O$, $R_T = R_O$ and $R_T < R_O$. The 100% and 0% reference levels are again provided by long strings of Ones and Zeros, and any overshoot or undershoot is easily discernible. The termination resistor is adjusted so that the eye pattern transitions exhibit the minimum perturbations *(Figure 13b)*. The resistor is then removed from the transmission line, and its measured value is the characteristic resistance of the line.



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2100 ft—Terminated
24 AWG Twisted Pair
Cable—PVC Insulation

FIGURE 12. NRZ Data Eye Pattern

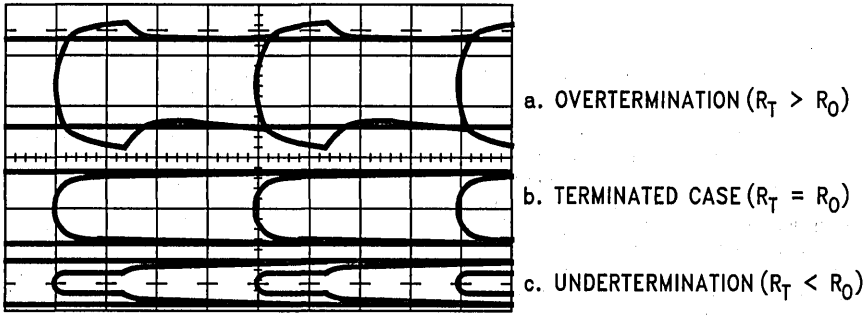

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FIGURE 13. Using Eye Pattern to Determine Characteristic Resistance of Line

By using the eye pattern to measure signal quality at the load end of a given line, a graph can be constructed showing the tradeoffs in signal quality—peak-to-peak jitter—as a function of line length and modulation rate for a specific pulse code. An example graph for NRZ data is shown in *Figure 14*. The graph was constructed using eye pattern measurements on a 24 AWG twisted pair line (PVC insulation) driven by a differential voltage source driver (75114/9614) with the line parallel-terminated in its characteristic resistance (96Ω). The oscilloscope plots in *Figure 15* show the typical eye patterns for NRZ data with various amounts of isochronous distortion. The straight lines represent a "best fit" to the actual measurement points. Since the twisted pair line used was not specifically constructed for pulse service, the graph probably represents a reasonably good worst-case condition insofar as signal quality vs line length is concerned. Twisted pair lines with polyethylene or Teflon® insulation have shown better performance at a given length than the polyvinyl chloride insulation. Likewise, larger conductors (20 AWG, 22 AWG) also

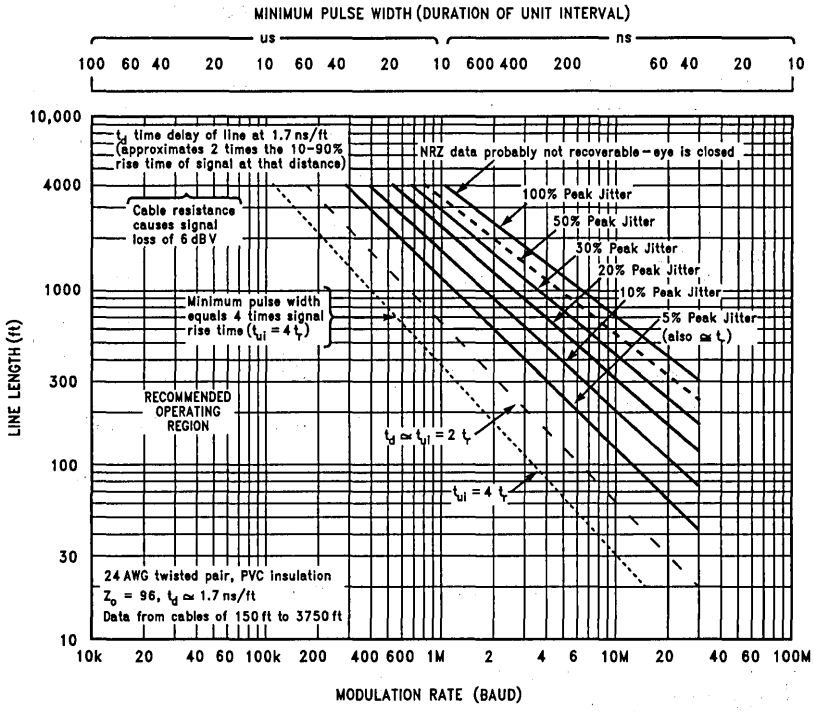

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FIGURE 14. Signal Quality as a Function of Line Length and Modulation Rate for Terminated 24 AWG Twisted Pair (PVC Insulation)

provide better performance at a given length. Thus, the graph in *Figure 14* can be used to estimate feasibility of a data transmission system when the actual cable to be used is unavailable for measurement purposes. The arbitrary cutoff of 4000 feet on the graph was due to the observed signal amplitude loss of 6 dBV (½ voltage) of the 24 AWG line at that distance. The cutoff of 10 Mbaud is based on the propagation delays of the typical TTL line drivers and receivers. Field experience has shown that twisted pair transmission systems using TTL drivers and receivers have operated essentially error-free when the line length and modulation rate are kept to within the recommended operating region shown in *Figure 14*. This has not precluded operation outside this region for some systems, but these systems must be carefully designed with particular attention paid to defining the required characteristics of the line, the driver, and the receiver devices. The use of coaxial cable instead of twisted pair lines almost always yields better performance, i.e., greater modulation rate at a given line length and signal quality. This is because most coaxial cable has a wider bandwidth and reduced attenuation at a given length than twisted pair line (one notable exception is RG 174/U cable).

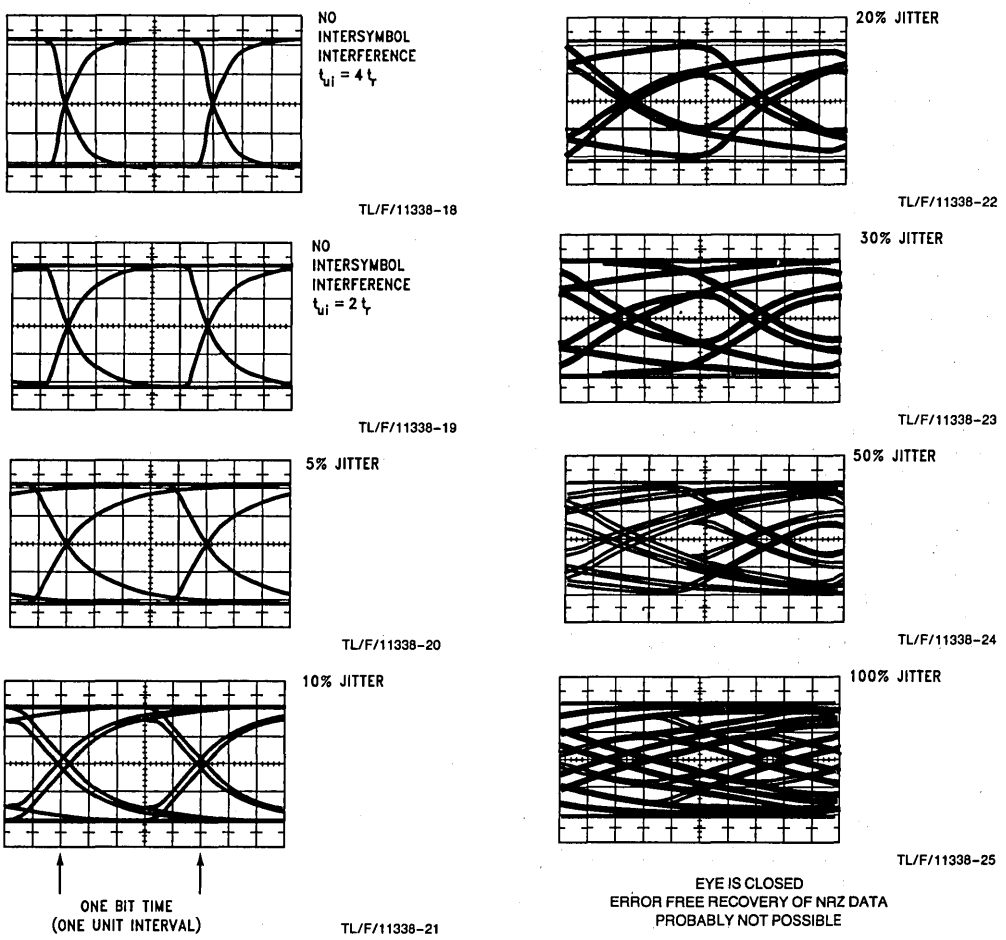


FIGURE 15. Eye Patterns for NRZ Data Corresponding to Various Peak-to-Peak Transition Jitter

It should be remembered that, in some ways, the eye pattern gives the *minimum* peak-to-peak transition jitter for a given line length, type, pulse code, and modulation rate. This is because the eye pattern transition spread is the result of intersymbol interference and reflection effects (if present) and this minimum jitter is only obtainable if the following conditions are met.

- The One and Zero signal levels produced by the line driver are symmetrical, and the line receiver's decision threshold (for NRZ signaling) is set to coincide with the mean of those two levels.
- The line is perfectly terminated in its characteristic resistance to prevent reflections from altering the signal threshold crossings.
- The time delays through driver and receiver devices for both logic states is symmetrical and there is no relative skew in the delays (difference between t_{plh} and t_{phl} propagation delays = 0). This is especially important when the device propagation delays become significant fractions of the unit interval for the applicable modulation rate.

If any one of these conditions is not satisfied, the signal quality is reduced (more distortion). The effects of receiver bias or threshold ambiguity and driver offset can be determined by location of the decision threshold(s) on the oscillograph of the eye pattern for that driver/cable modulation rate combination. For eye patterns displaying more than 20% isochronous distortion, the slope of the signal in the transition region is relatively small. Therefore, a small amount of bias results in a large increase in net isochronous distortion. See *Figure 16* for a graphic illustration of this effect. In the interest of conservative design practices, systems should always be designed with less than 5% transition spread in the eye pattern. This allows the detrimental effects due to bias to be minimized, thus simplifying construction of line drivers and receivers.

OTHER PULSE CODES AND SIGNAL QUALITY

In the preceding sections, the discussion of signal quality has been centered around the use of NRZ signaling, because it represents the simplest and most commonly used pulse code. Other pulse codes have been developed which provide one or more of the following desirable features:

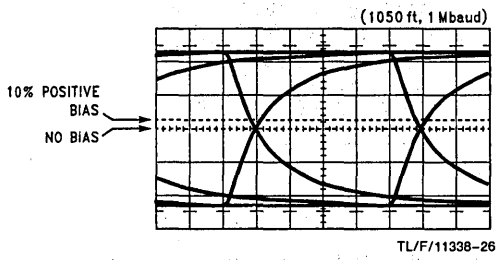
- Compress the overall bandwidth normally required to adequately transmit the signal yet still ensure recovery of the binary data.
- Eliminate the need for a dc response in the transmission medium so that transformer coupling can be used for phantom power distribution on repeated lines. (The elimination of a dc characteristic of the pulse code also allows ac coupling of amplifier circuits).
- Provide a clocking scheme within the signal so that no separate clock channel is required for synchronization.
- Provide built-in error detection.

The following discussion is restricted to the binary class of baseband signals. This simply means that each decision by the line receiver yields one bit of information. The *M*-ary schemes ($M \geq 3$) can encode more than one bit of information per receiver decision*, but these schemes are seldom applied to baseband signaling due to the complexities of the driver and receiver circuits (especially for $M > 3$). *M*-ary schemes, however, are applied to high speed non-baseband data transmission systems using modems. The price to be paid for the increased bit-packing with multi-level signaling is decreased immunity to noise relative to a binary system. This is because a smaller relative threshold displacement (or amount of noise) is required to produce a signal representing another logic state in the *M*-ary schemes.

* It can be shown that, for *M* levels, the information per receiver decision will be $S = \log_2 M$ bits/decision. Thus, three levels theoretically yield 1.58 bits; four levels yield 2 bits of information, eight levels yield 3 bits, etc.

In general, the binary class of pulse codes can be grouped into four categories:

- Non-Return to Zero (NRZ)
- Return to Zero (RZ)
- Phase Encoded (PE) (sometimes called Split Phase)
- Multi-Level Binary (MLB). (The MLB scheme uses three levels to convey the binary data, but each decision by the line receiver yields only one bit of information.)



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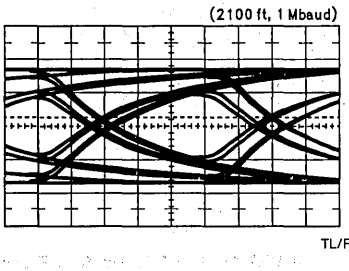

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$$\text{ISOCHRONOUS DISTORTION (ID)} = \frac{t_{ics}}{t_{ui}} \times 100\%$$

BIAS	1050 ft	2100 ft
0%	5% ID	20% ID
10%	12% ID	36% ID

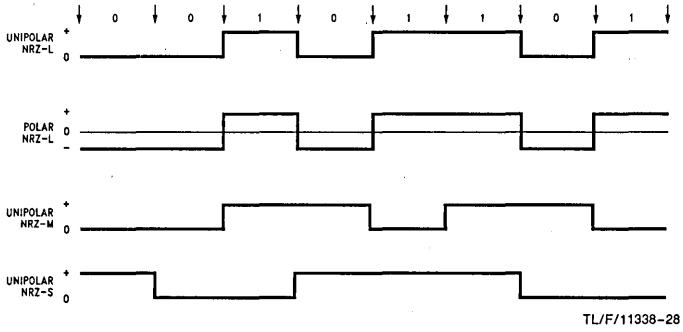
FIGURE 16. Receiver Bias Effect on Total Isochronous Distortion

A secondary differentiation among the pulse codes in concerned with the algebraic signs of the signal levels. If the signal levels have the same algebraic sign for their voltages (or currents) and differ only in their magnitudes, the signaling is called *unipolar*. A very common example of unipolar signaling is TTL or ECL logic. TTL uses two positive voltages to represent its logic states, while ECL uses two negative voltages for its logic states. The complement of unipolar signaling is *polar* signaling. Here, one logic state is represented by a signal voltage or current having a positive sign and the other logic state is represented by a signal with a negative sign. For binary signals, the magnitude of both signals should be equal, ideally. Their only difference should be in the algebraic signs. This allows the receiver to use ground as its decision thershold reference.

Non-Return to Zero (NRZ) Pulse Codes

There are three NRZ pulse codes: NRZ-Level (NRZ-L), NRZ-Mark (NRZ-M), and NRZ-Space (NRZ-S). NRZ-L is the same pulse code as previously discussed. In NRZ-L signaling, data is represented by a constant signal level during the bit time interval, with one signal level corresponding to one logic state, and the other signal level corresponding to the opposite logic state. In NRZ-M or NRZ-S signaling, however, a change in signal level at the start of a bit interval corresponds to one logic state and no change in signal level at the start of a bit interval corresponds to the opposite logic state. For NRZ-M pulse codes, a change in signal level at the start of the bit interval indicates a logic One (Mark), while no change in signal level indicates a logic Zero (Space). NRZ-S is a logical complement to NRZ-M. A change in signal level means a logic Zero and no change means logic One. With NRZ-M and NRZ-S pulse codes, therefore, there is no direct correspondence between signal levels and logic states as there is with NRZ-L signaling. Any of the NRZ pulse codes may, of course, be used in unipolar or polar form. The NRZ codes are shown in *Figure 17*, along with their generation algorithm*, signal levels vs time, and their general power density spectrum.

* The generation algorithm showing the sequence of signal levels on the line, represented by the set $\{b_n\}$, is determined by the sequence of input logic states, represented by the set $\{a_n\}$. See Bennet[14] for detailed usage of this notation.



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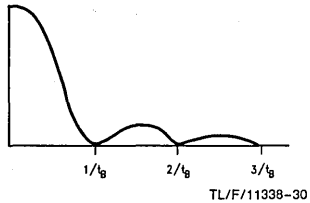

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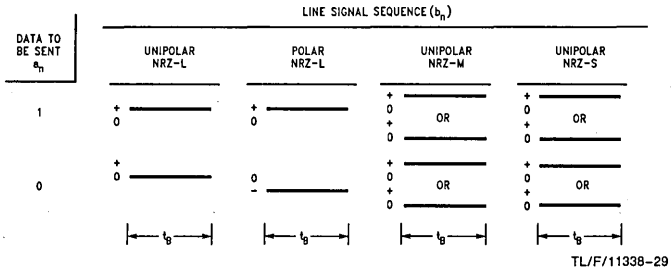
GENERAL POWER SPECTRUM FOR NRZ CODES



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t_{ui}	t_B	t_B	t_B	t_B
$a_n = 1$	$b_n = +$	$b_n = +$	$b_n = (-)\, b_n - 1$	$b_n = b_n - 1$
$a_n = 0$	$b_n = 0$	$b_n = -$	$b_n = b_n - 1$	$b_n = (-)b_n - 1$

FIGURE 17. Non-Return to Zero (NRZ) Pulse Codes

The degradation in signal quality caused by intersymbol interference for NRZ-L signaling was discussed earlier. Since the minimum signaling element (unit interval) for all three NRZ pulse codes is equal to t_B, the previous signal quality discussion for NRZ-L also applies equally to NRZ-M and NRZ-S pulse codes. The following is a capsule summary of the previous discussion on NRZ signal quality.

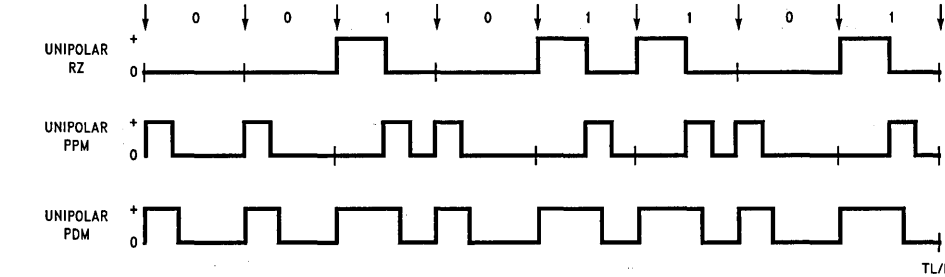
- When t_B is less than the 0%–50% rise or fall time of the signal at the line end, the open space in the eye pattern closes, thereby indicating error-free data transmission is unlikely.
- When t_B is less than the 10%–90% rise or fall time of the line end signal, some intersymbol interference is present and thus, some time jitter in the transitions of the recovered data will be present.

NRZ codes are simple to generate and decode because no precoding or special treatment is required. This simplicity makes them probably the most widely used pulse codes, with NRZ-L the leader by far. NRZ-M has been widely used in digital magnetic recording where it is usually called NRZI for Non-Return to Zero, Invert-on-Ones. In terms of the four desirable features for a pulse code listed at the start of this section, however, non of the NRZ codes are all that great—NRZ codes do possess a strong dc component, and have neither intrinsic clocking, nor error detection features. Even so, their power frequency spectra are used as references for comparison with other pulse codes.

Return to Zero (RZ) Pulse Codes

The RZ group of pulse codes are usually simple combinations of NRZL data and its associated single or double frequency clock. By combining the clock with data, all RZ codes possess some intrinsic synchronization feature. Three representative RZ pulse codes are shown in *Figure 18*. Unipolar RZ is formed by performing a logic AND between the NRZ-L data and its clock. Thus a logic Zero is represented by the absence of a pulse during the bit time interval, and a logic One is represented by a pulse as shown. Pulse Position Modulation (PPM) uses a pulse of $t_B/4$ duration beginning at the start of the bit interval to indicate a logic Zero, and a $t_B/4$ pulse beginning at the middle of the bit interval to indicate a logic One. Pulse Duration Modulation (PDM) uses a $t_B/3$ duration pulse for a logic Zero and a $(2/3)$ t_B pulse for a logic One, with the rising edge of both pulses coinciding with the start of the bit interval. PDM with $t_B/4$ pulse widths is also used but better results are usually obtained with the $t_B/3$, 2 $t_B/3$ scheme.

The reason for differentiating between information rate and modulation rate can now be further clarified. Each of the RZ pulse codes in *Figure 18* has the same information rate; i.e., $1/t_B$ bits per second. Their respective minimum signaling elements (unit intervals) however, are all less than t_B so the *modulation rate* for the RZ pulse code is greater than the *information rate*. Remember that with NRZ signaling, the



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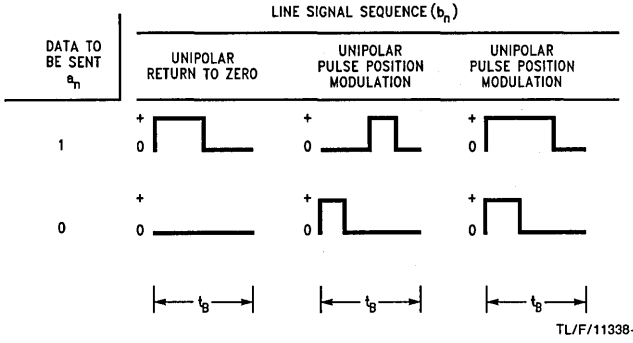

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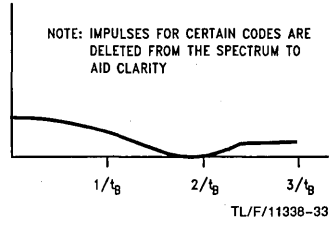

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GENERAL POWER SPECTRUM FOR RZ CODES

t_{ui}	$t_B/2$	$t_B/4$	$t_B/3$
$a_n = 1$	$b_n = (+)\ \{0 \le t < t_B/2$ $b_n = (0)\ \{t_B/2 \le t < t_B$	$b_n = (+)\ \{t_B/2 \le t \le 3t_B/4$ $b_n = (0)\ \begin{cases} 0 \le t < t_B/2 \\ 3t_B/4 < t < t_B \end{cases}$	$b_n = (+)\ \{0 \le t \le 2t_B/3$ $b_n = (0)\ \{2t_B/3 \le t < t_B$
$a_n = 0$	$b_n = (0)$	$b_n = (+)\ \{0 \le t \le t_B/4$ $b_n = (0)\ \{t_B/4 < t < t_B$	$b_n = (+)\{0 \le t \le t_B/3$ $b_n = (0)\{t_B/3 \le t_B$

FIGURE 18. Return to Zero (RZ) Pulse Codes

unit interval and the bit time interval are equal in duration, so the information rate in bps is equal to the modulation rate in bauds. For isochronous NRZ signaling, the measures bps and baud are both synonymous and interchangeable.

Inspection of unipolar RZ signaling reveals that the unit interval is ½ bit interval ($t_{ui} = t_B/2$). When this unit interval is less than the 0%–50% rise or fall time of the line, the data is likely to be unrecoverable. With a fixed modulation rate, the price paid to include clocking information into unipolar RZ is reduced information rate over that for NRZ signaling. Likewise, for PPM with its unit interval of $t_B/4$, the information rate reduces to ¼ that of NRZ data under the same conditions. This is because the maximum modulation rate is determined by the 50% rise time of the line which is constant for a given length and type of line. PDM has a unit interval of $t_B/3$ so, for a given maximum modulation rate, the resulting information rate is ⅓ that of NRZ data.

The preceding argument should not be taken as strictly correct—since the actual intersymbol interference patterns for the three RZ codes discussed differ somewhat from the pattern with NRZ codes. A random sequence of NRZ data can easily consist of a long sequence of Zeros followed by a single One and then a long sequence of Zeros, so the $t_{50\%}$ limit can be accurately applied. Unipolar RZ, in response to the same long data sequence, produces a $t_B/2$ pulse, so the $t_{50\%}$ argument can be applied here too. With PPM and PDM, the maximum time that the line signal can be in one state is quite reduced from the NRZ case. For PPM, this time is 1.25 t_B (010 data sequence) while for PDM, it is 0.67 t_B (see *Figure 18*). With PPM and PDM, then, the line signal may never reach the final signal levels that it does with NRZ data. So, the PPM and PDM signals have a head start, so to speak, in reaching the threshold crossing of the receiver. Because of the reduced time that PDM and PPM signal levels are allowed to remain at one signal level, their signaling may still operate at a modulation rate slightly above that where the NRZ data shows 100% transition jitter. Even with this slight correction to the previous discussion, the RZ group of pulse codes still sacrifice information rate in return for synchronization. The PPM scheme appears to be a poor trade in this respect, since PDM allows a greater information rate while retaining the self-clocking feature. Unipolar RZ, because it provides no clocking for a logic Zero signal, is not generally as useful as PDM for baseband data transmission. However, unipolar RZ is used in older digital magnetic tape recorders.

Examination of RZ codes shows only one more desirable feature than NRZ codes: clocking. RZ codes still have a dc component in their power density spectrum *(Figure 18)* and their bandwidth is extended (first null at $2/t_B$) over that of NRZ (first null $1/t_B$). RZ codes do not have any intrinsic error detection features.

Phase Encoded (PE) Pulse Codes

The PE group of pulse codes uses signal level transitions to carry both binary data and synchronization information. Each of the codes provides at least one signal level transition per bit interval aiding synchronous recovery of the binary data. Simply stated, Biphase-Level (Biϕ-L) code is binary phase shift keying (PSK) and is the result of an Exclusive-OR logic function performed on the NRZ-L data and its clock; it is further required that the resultant signal be phase coherent (i.e., no glitches). Biphase—Mark (Biϕ-M) and Biphase-Space (Biϕ-S) codes are essentially phase coherent, binary frequency shift keying (FSK). In Biϕ-M, a logic One is represented by a constant level during the bit interval (one-half cycle of the lower frequency $1/(2\ t_B)$, while a logic Zero is represented by one-half cycle of the higher frequency $1/t_B$. In Biϕ-S, the logic states are reversed from those in Biϕ-M. Another way of thinking of Biϕ-M or Biϕ-S is as follows.

- Change signal level at the end of each bit interval regardless of the logic state of the data.
- Change signal level at the middle of each bit interval to mean a particular logic state.

In Biϕ-M (sometimes call diphase), a mid-bit interval change in signal level indicates a logic One (Mark), while no change indicates a logic Zero. For Biϕ-S, no signal level change in the middle of the bit interval means a logic One, while a change means a logic Zero.

In Biϕ-L (also called Manchester Code), a positive-going transition at the middle of the bit interval means a logic Zero, while a negative-going transition there indicates a logic One.

The fourth member of the PE family is Delay Modulation (DM)[15, 16] sometimes referred to as Miller code. Here logic One is represented by a mid-bit interval signal level change, and a logic Zero is represented by a signal level change at the end of the bit interval if the logic Zero is followed by another logic Zero. If the logic Zero is immediately followed by a logic One, no signal level transition at the end of the first bit interval is used. The waveforms encoding algorithms, and general power density spectra for the PE pulse code family are shown in *Figure 19*.

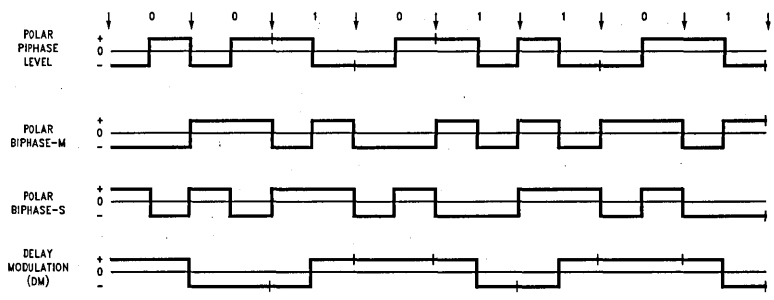
* Delay Modulation[15, 16] has a maximmum of 2 t_B without a signal level transition.

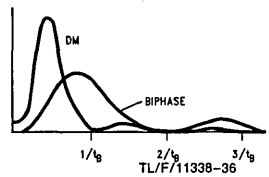
A brief inspection of the signal waveforms for the three Biphase pulse codes reveals that their minimum signaling element has a duration of one-half bit interval ($t_{ui} = t_B/2$); the longest duration of either signal level is one bit interval. Similarly, DM is seen to have a minimum signaling element of one bit interval ($t_{ui} = t_B$) and the maximum duration of either signal level is two bit intervals (produced by a 101 pattern). Biphase codes should exhibit eye closure (they would not be recoverable without equalization) when $t_{ui} \leq t_{0\%-50\%}$. So, a 50% jitter on NRZ signaling approximately corresponds to the Biphase codes non-operation point. Biphase codes, therefore, provide one-half the information rate of NRZ signals at a given maximum modulation rate. This is in exchange for synchronization information and a dc-free spectrum when used in polar form.

DM should have essentially the same intersymbol interference characteristics as NRZ, since the unit interval is the same for both codes. DM may perform slightly better than NRZ, because the maximum duration of either signal level is two bit intervals. Overall, DM is better coding scheme than the Biϕ. It does not require as much bandwidth as Biϕ and still possesses the desirable dc response and synchronization qualities.

Both Biϕ and DM are good choices for digital magnetic recording[16]; Biϕ is widely used in disc memory equipment, and DM is rapidly gaining acceptance where high bit packing densities are desired. Overall scoring, in terms of the four desirable characteristics, shows the PE pulse codes with three primary features; bandwidth compression, no dc, and intrinsic synchronization.

Th Biϕ family does not possess any intrinsic error detection scheme. DM does possess the capability of detecting some—but not all—single bit errors. This detection process is accomplished by checking to see if a single level persists longer than two bit intervals, in which case, an error is indicated. DM detection requires two samples per bit interval.





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GENERAL POWER SPECTRUM FOR SPLIT PHASE CODES

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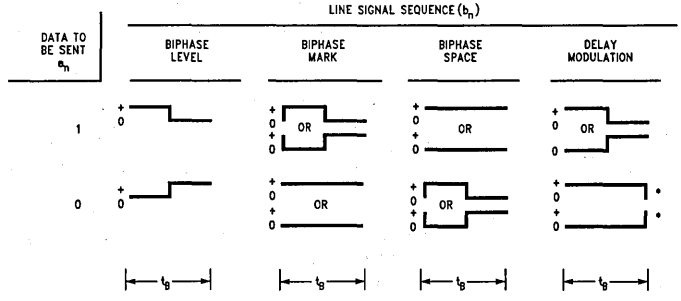

*Transition only if followed by another "0" ($a_{k+1} = 0$)

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t_{ui}	$t_B/2$	t_B2	$t_B/2$	t_B
$a_n = 1$	$b_n = (+)\{0 < t < t_B/2$ $b_n = (-)\{t_B/2 \le t \le t_B$	‡	$b_n = (-)\, b_{n-1}$* *complement of final level of last b_n	if final value of $b_{n-1} = (+)$ then $b_n = (+)\{0 < t < t_B/2$ and $b_n = (-)\{t_B/2 \le t \le t_B$ else, compliment above b_n values for times shown
$a_n = 0$	$b_n = (-)\{0 < t < t_B/2$ $b_n = (+)\{t_B/2 \le t \le t_B$	$b_n = (-)\, b_{n-1}$* *complement of final level of last b_n	‡	if final value of $b_{n-1} = (+)$ then $b_n = (+)\{0 \le t < t_B$ if $a_{n+1} = (0)$ then $b_n = (-)\{t = t_B$ else $b_n = (+)\{t = t_B$ if final value of $b_{n-1} = (-)$ then complement b_n values above

‡ If b_{n-1} final level = (+), then $\begin{cases} b_n = (-)\{0 \le t < t_B/2 \\ b_n = (+)\{t_B/2 \le t < t_B \end{cases}$

If b_{n-1} final level = (−), then $\begin{cases} b_n = (+)\{0 \le t < t_B/2 \\ b_n = (-)\{t_B/2 \le t < t_B \end{cases}$

FIGURE 19. Phase Encoded (PE) Pulse Codes

Multi-Level Binary (PLB) Pulse Codes

The pulse codes in the MLB groupd discussed have a common characteristic of using three signal levels (expressed in shofthand notation as +, 0, −) to represent the binary information, but each receiver decision yields only one bit of information. These are sometimes called *pseudoternary* codes to distinguish them from true ternary codes wherein each receiver decision can yield 1.58 information bits.

The most straightforward pulse code in the MLB group is polar RZ *(Figure 20)*. Some authors place PRZ in the RZ group, but since PRZ uses three signal levels, it is placed in the MLB group here. A logic One is represented by a positive polarity pulse, and a logic Zero is represented by a negative polarity pulse. Each pulse lasts for one-half bit interval. PRZ has excellent synchronization properties since there is a pulse present during every bit interval.

Bipolar (BP)[17, 18] uses a $t_B/2$ duration pulse to signify a logic One, and no pulse during the bit interval to signify a logic Zero. The polarity of the pulses for a logic One is alternated as shown in *Figure 20*. Bipolar coding is also known as Alternate Mark Inversion. BP is widely used in Bell Systems T1–PCM carrier systems as a pulse code transmitted along a regenerative repeated transmission line. Since BP has no dc component, the regenerative repeaters along the span line may be transformer coupled and powered by a phantom constant current power loop from the central office. The synchronization properties of BP are excellent if the number of Zero bits transmitted in series is constrained. This constraint on the number of sequential Zeros allows clock circuits in each repeater to remain in synchronization. A scheme called Binary with 6 Zeros Substitution (B6ZS) was developed to replace 6 Zeros with a given signal sequence to offset this loss of synchronization[18]. Bipolar coding has a limited capability to detect single errors, all odd errors, and certain even error combinations which violate the mark alternation rule. Another scheme called High Density Bipolar with 3 Zeros substitution (HDB-3) replaces four successive Zeros (no pulses) with three Zeros followed by a pulse whose polarity violates the Mark alternation rule[19]. Subsequent detection of this pattern (three Zeros and pulse violating the polarity coding rule) causes the receiver to substitute four Zeros for the received 0001 pattern.

In Dicode (DI)[20, 21], a polar pulse (either t_B for DI-NRZ or $t_B/2$ for DI-RZ) is sent for every input data transition. The limiting constraint is that the successive pulses must alternate in sign *(Figure 19)*. As in NRZ-M and NRZ-S, the actual polarity of the pulses does not necessarily correspond to

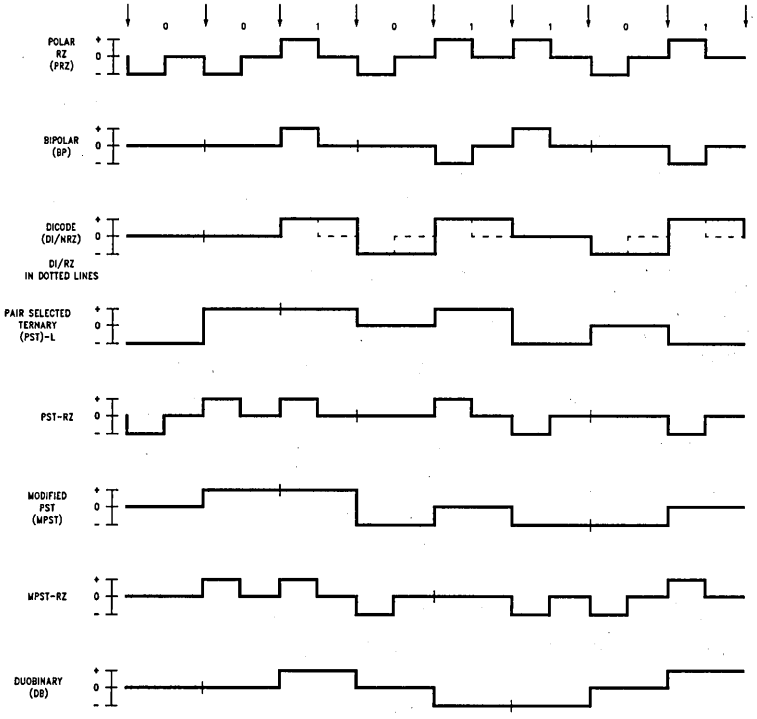

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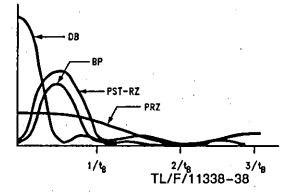
FIGURE 20. Multilevel Binary (MLB) or Pseudoternary Pulse Codes



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GENERAL POWER DENSITY SPECTRUM
RANDOM SEQUENCE P(0) = P(1) = 0.5

8

the logic state of the data (a positive pulse may represent either a Zero-to-One or a One-to-Zero transition of the input data). The power spectrum for DI is the same as for BP (no dc component). Bit synchronization for DI can be obtained in the same manner as for BP, but with DI, the number of bits of the same logic state must be controlled in order for the receiver to maintain bit synchronization. DI also has the intrinsic capability of detecting single bit errors (via two successive positive or negative signal levels), all odd, and some even numbers of errors.

Pair Selected Ternary (PST)[18, 22] and Modified PST (MPST)[22] were proposed to minimize the disadvantages of BP coding: loss of synchronization with long strings of Zeros and timing jitter. PST/MPST maintains the strong features of BP: dc free spectrum, single error detection. To produce PST or MPST, the incoming bits are grouped into pairs, and the signal produced on the line is governed by a coding table. Two modes are also used in the coding table with a change in mode occurring after a certain bit pair is transmitted. The features of PST/MPST thus include:

- No dc spectral component,
- No loss of synchronization with long strings of Zeros,
- Intrinsic error detection,
- Simplification of requirements for timing extraction circuits with respect to BP.

MPST coding was developed primarily to speed up the framing process, i.e., selecting which two successive pulses constitute a valid pair, when the probability for a Zero and a One are not equal.

Duobinary[23, 24] is an example of a correlative level coding technique, wherein a correlation exists between successive signal levels. Duobinary uses three signal levels with the middle level corresponding to a logic Zero, and the other two levels corresponding to a logic One. The pseudoternary signal is generated by precoding the input data, which results in constraining the line signal to change only to the neighboring level, i.e., the (+) to (−) and (−) to (+) level changes are not allowed. This precoding process uses controlled intersymbol interference as part of the coding scheme. The benefit is an effective doubling of the bit rate for a given bandwidth and concentration of the power spectrum toward dc *(Figure 20)*. Duobinary has the capability to detect single errors which violate the encoding rules. In terms of bandwidth utilization, Duobinary ranks first among all the binary and MLB codes[20], but its strong dc component prohibits the use of ac-coupled transmission media. Synchronization properties are similar to NRZ, thus external clocking must be used to recover the data.

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FAILSAFE Biasing of Differential Buses

National Semiconductor
Application Note 847
John Goldie

OVERVIEW

Multi-Point bus configurations present two potential problems to the system I/O designer that do not commonly occur in Point-to-Point configurations. The two problems that the I/O system designer should take into account are bus contentions and the idle bus state. Bus contention occurs when more than one driver is active at a time during which the state of the bus is undetermined. Contentions may occur either by software or hardware errors. The second problem is an unknown bus state when all drivers are OFF. FAILSAFE biasing solves this problem by biasing the bus to a known state when ALL drivers are in TRI-STATE® (OFF). This application note is devoted to the topic of FAILSAFE biasing of differential buses.

INTRODUCTION

FAILSAFE biasing provides a known state when all drivers are in TRI-STATE (Hi-Z, OFF). This is especially important in bus configurations that employ more than one driver (transceiver), and is commonly known as a Multi-Point application (see *Figure 1*).

Electrical Characteristics Standard TIA/EIA-485 specifies that a maximum of 32 unit loads can be connected to a bus. A transceiver (driver/receiver pair) normally represents one unit load (see *Figure 1*). The bus is a half duplex bi-directional bus, (as data can flow in both directions), but only one driver should be active at a time. Termination is required (in most cases), and is only located at the two extreme ends of the bus. Note, that the termination shown on the left of *Figure 1* also provides a FAILSAFE bias.

BUS STATES

A FAILSAFE biased bus has only two states, HIGH (driven HIGH and FAILSAFE HIGH) and LOW (neglecting the transition region, and bus contentions). The bus can be driven HIGH or LOW by an active driver, or biased to a known state by external pull up and pull down resistors. These resistors provide the FAILSAFE bias, and the termination configuration is also known as a "power termination". The two bus states are shown in *Figure 2*.

In some applications these two states are defined as MARK/SPACE, OFF/ON, or 1/0. The definition of the two states is application dependent. When the signal transitions through the threshold region (±200 mV) the output state of the receiver is undefined. In *Figure 2*, the line is driven LOW, transitions HIGH, then the driver is disabled. The bus however, remains HIGH due to external FAILSAFE biasing.

Without FAILSAFE biasing, the receiver output would be undetermined when all drivers are OFF. The line would settle to only 1 mV–5 mV of each other ($|V_{OA}-V_{OB}|$, due to the internal input impedance network of the receiver), which is within the receiver's threshold limits (≤200 mV). If external noise is coupled onto the line, a false transition could occur, causing an error. In an asynchronous application, this false transition could be interpreted as a framing error, false start bit, or cause a false interrupt.

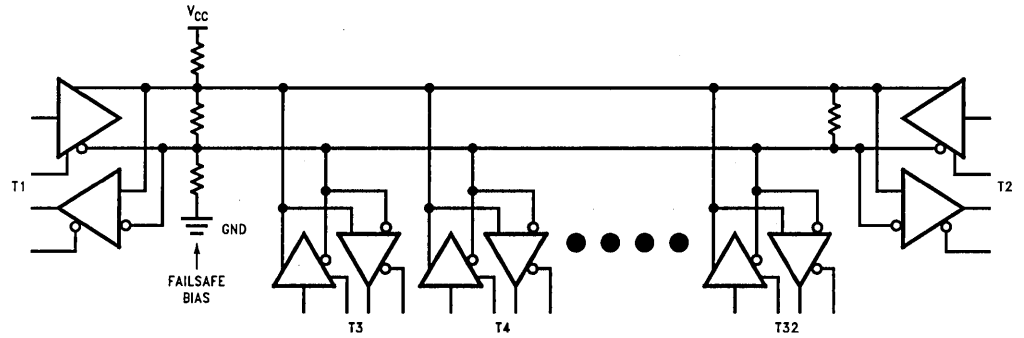

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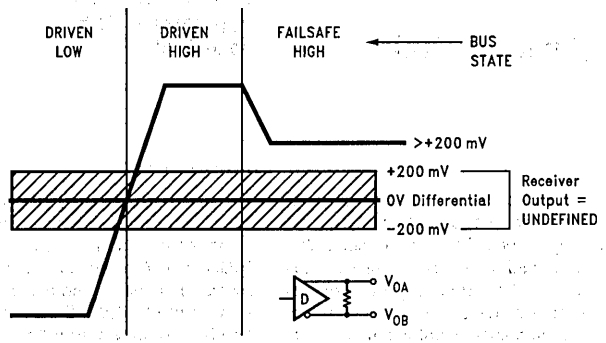
FIGURE 1. Typical Multi-Point Application



Note: Differential Plot $V_{OA} - V_{OB}$, not with respect to GND.

FIGURE 2. Bus States

SERIAL PROTOCOL

A popular format for low speed data transmission is an asynchronous protocol. A typical format is composed of 12 bits. The start bit initiates the timing sequence. This is detected by a transition from HIGH to LOW. Next are eight data bits, followed by an optional parity bit. Lastly, the line is driven HIGH for one or two bits (stop bits), signifying the end of the character. This format is illustrated in *Figure 3*. If another character is to be sent, the next start bit initiates the whole process all over again. However, if this was the last character, the line should remain HIGH until the next start bit, but the active driver is disabled. This presents a problem in multi-point applications, because between data transmissions all drivers are OFF. With no active drivers, the line is floating, and receiver outputs are undetermined. There are several solutions to this problem. One is through the use of alternate protocols (software), while the other is a hardware fix. The hardware fix uses external resistors to bias the line HIGH, when all drivers are off. The remainder of the application note describes the hardware method and the selection of component values.

In a Point-to-Point application (see *Figure 4*), the driver is normally always enabled. In this case the bus has only two states, driven HIGH, and driven LOW. FAILSAFE biasing is not needed, unless the drivers's enabling pin is also switched.

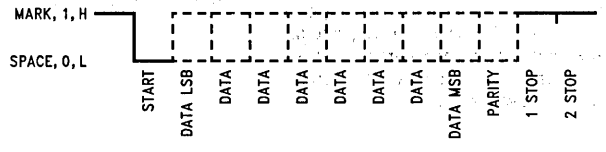


FIGURE 3. Asynchronous-UART Timing Format

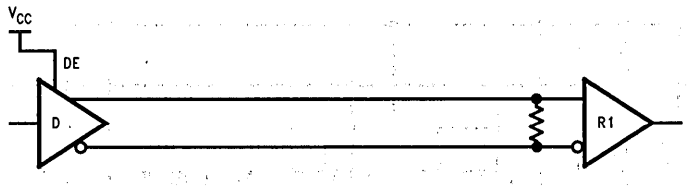


FIGURE 4. Typical Point-to-Point Application

CALCULATING RESISTOR VALUES FOR FAILSAFE BIASING

The external resistors are selected such that they provide at least a 200 mV (maximum receiver threshold) bias across the line, and not substantially load down the active driver.

In addition, the following guidelines should be met. The pull up resistor (Ra) and the pull down resistor (Rd) should be of equal value. This provides symmetrical loading for the driver. Termination resistor Rb should be selected such that it matches the characteristic impedance (Z_O) of the twisted pair cable. If the termination resistor matches the line, Rb = Z_O, there will be no reflections. At the other end of the cable, the equivalent resistance of Rc, Ra and Rd should also match the characteristic impedance of the line. In this case Rc is in parallel with Ra plus Rd (Rc//(Ra + Rd)). For this equivalent resistance to be matched to the line Rc must be greater than Z_O. Rc is typically 10Ω–20Ω greater than Z_O, but the actual value depends upon the values Ra and Rd. The FAILSAFE bias (Vfsb) is the potential dropped across the line. Note that this equation neglects cable resistance (see appendix), and that Rb is in parallel with Rc (Req = Rb // Rc). Therefore, the FAILSAFE bias is simply a voltage divider between Req, Ra, and Rd. The worst case occurs at V_{CC} − 5%, Ra and Rd + % tolerance, and Rc and Rb − % tolerance. Under the worst case conditions the FAILSAFE bias must be greater than 200 mV for the receiver output to be in a guaranteed state.

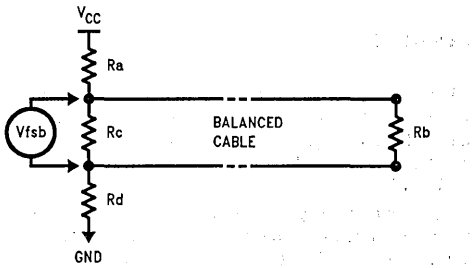


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FIGURE 5. External FAILSAFE Bias Resistors

Example calculations for selecting FAILSAFE bias resistors:

Note: For this example assume the cable has a characteristic impedance (Z_O) of 120Ω.

Step 1 Assume that Rc and Rb are equal and are selected to match Z_O.

$$Rc = Rb = Z_O = 120\Omega$$

Step 2 Calculate the equivalent resistance of Rc//Rb.

$$Rc\ //\ Rb = 120\Omega\ //\ 120\Omega = 60\Omega$$

Step 3 Calculate the Pull up and Pull down resistor values knowing that the FAILSAFE bias is 200 mV, and V_{CC} = 5V.

$$Vfsb = V_{CC}\,(Req/(Ra + Req + Rd))$$

solving for R′ (defined as Ra + Rd)

$$R' = ((Req)V_{CC} / Vfsb) - Req$$

$$R' = ((60\Omega)5V/0.2V) - 60\Omega = 1440\Omega$$

Since Ra and Rd are equal, Ra = Rd = 1440Ω/2 = 720Ω

Step 4 Recalculate the equivalent resistance of Rc//(Ra + Rd).

$$Rc//(Ra + Rd) = 120\Omega//(720\Omega + 720\Omega) = 110\Omega$$

Since the equivalent resistance is close (within 10%) to the characteristic impedance of the cable (Z_O), no further adjustment of resistor values is required.

However, for the perfectionist, the matched value of Rc can be calculated by setting the following equation to Z_O and solving for Rc.

$$Z_O = Rc\ //\ (Ra + Rd)$$

$$\therefore Rc = 131\Omega$$

Now the equivalent resistance (Req = Rc // Rb) becomes 131Ω // 120Ω = 62Ω, which is very close to the original 60Ω. Standard value resistors values can be substituted to ease resistor selection, availability, and cost, before recalculating the FAILSAFE bias potential. Using a 5% tolerance table we find the following standard resistor values:

$$Ra = 750\Omega,\ Rb = 120\Omega,\ Rc = 130\Omega,\ Rd = 750\Omega$$

In order to verify that the selected values meet the criteria the following calculations should be completed:

1. $Rc//(Ra + Rd) = Z_O$

   $130\Omega//(750\Omega + 750\Omega) = 120\Omega$

2. $Req = Rb//Rc$

   $120\Omega//130\Omega = 62\Omega$

3. $Vfsb = V_{CC}\,(Req/(Ra + Req + Rd))$

   $5V(62\Omega/(750\Omega + 62\Omega + 750\Omega)) = 200\ mV$

Based on the example shown above, and a twisted pair cable with characteristic impedance of 120Ω, it has been determined that a 750Ω pull up and pull down resistor will provide a FAILSAFE bias of 200 mV. This value could be decreased slightly to provide a greater bias (>200 mV), and to meet the worst case power supply and resistor tolerance conditions. However, the value of Ra and Rd should not be reduced too low in order to minimize loading seen by the driver. This example illustrated that the largest values used for the pull up (Ra) and pull down (Rd) resistors should be 750Ω. The pull resistors should not be decreased substantially. Because when the driver is active (ON), it is required to develop a minimum of 1.5V across the cable termination. Using low impedance pull resistors further loads down the driver, making the 1.5V differential voltage even more difficult to meet.

Figure 6 illustrates the fully loaded (32 unit loads) TIA/EIA-485 bus with an external FAILSAFE bias network. Note that the FAILSAFE bias (Power Termination) is only located at one end of the bus. The other end employs a single resistor termination. The power termination is commonly located on the Master node of a Master/Slave bus configuration. This assures that the power to the pull up resistor is always on.

Before looking at the driver's load, the receiver's input impedance needs to be modeled to understand its effect upon the driver. The TIA/EIA-485 standard specifies a high receiver input impedance and an Input Voltage vs Input Current curve. An input impedance of 12 kΩ or greater is typically required to meet the V_{IN}/I_{IN} curve. A common mistake is to model the receiver's input impedance as a differential resistance, which is seen between the input pins. The input resistance is correctly modeled as a series resistor to a voltage reference node (AC ground point). The TIA/EIA-485 standard also allows for 32 unit loads to be connected in parallel. Therefore, the driver could see 32 12 kΩ resistors in parallel on each line. This is equivalent to a 375Ω resistor to an internal voltage reference point.

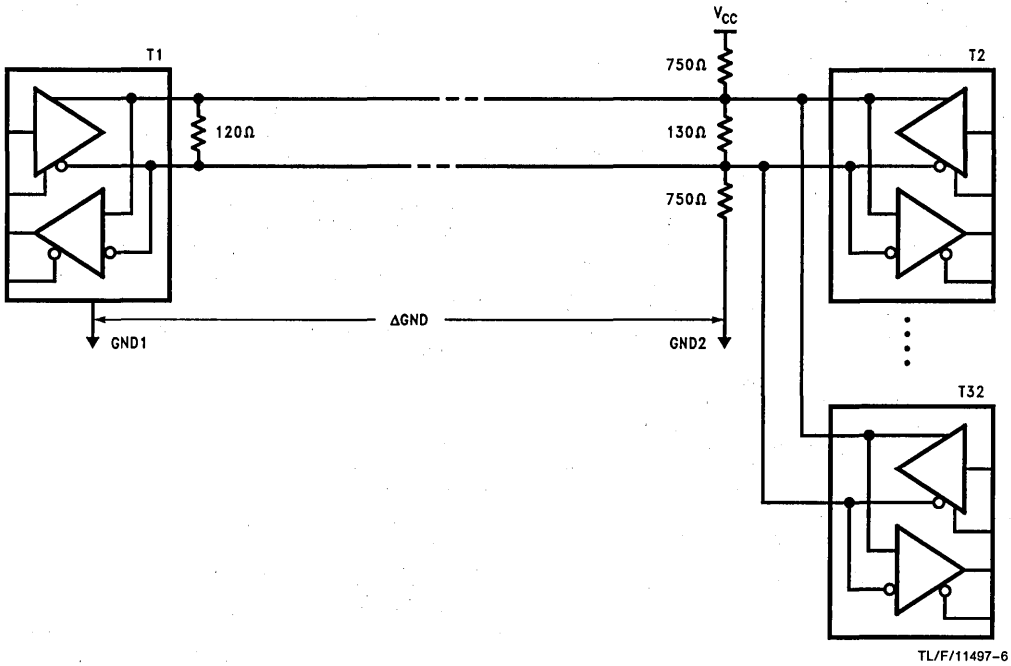

FIGURE 6. Fully Loaded TIA/EIA-485 Bus

The test circuit shown in *Figure 7* models the fully loaded TIA/EIA-485 bus. The 375Ω resistors that model the 32 parallel receiver input impedances, have been changed to 330Ω for two reasons. First, an active driver would also see 31 Tri-stated driver leakage currents (I_{OZ}), which is equivalent to 31 times 100 μA or 3.1 mA. This is equivalent to roughly 3 more unit loads. Therefore, 12 kΩ divided by 35(32 + 3) equals 342Ω. This value is further reduced to 330Ω to select standard value resistors. The dashed box represents 32 receiver loads and 31 passive driver leakage loads. The V_{CM} power supply models the maximum ground shifting specified (allowed) by TIA/EIA-485 (±7V). The differential voltage (VOD), measured across the 62Ω load (120Ω//130Ω), is required to be greater than 1.5V in magnitude by TIA/EIA-485.

Test data taken on three popular National TIA/EIA-485 drivers are shown in Table I. With the common mode voltage varied from −7V to +7V, all of the devices meet the 1.5V minimum differential voltage (VOD column).

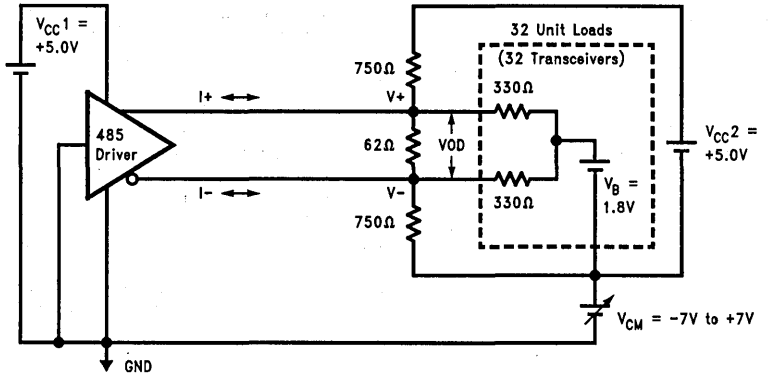

FIGURE 7. Full Load Equivalent Test Circuit

TABLE I. Test Data for TIA/EIA-485 Drivers

Device	V_{CM} (V)	I− (mA)	I+ (mA)	V− (V)	V+ (V)	VOD (V)
DS3695	0	−41.7	+38.4	3.39	1.44	1.95
	−7	−56.1	+23.5	3.18	1.24	1.94
	+7	−13.4	+69.1	3.78	1.77	2.01
DS96172/4	0	−43.4	+42.4	3.25	1.14	2.11
	−7	−59.6	+28.0	3.08	0.94	2.14
	+7	−12.0	+70.4	3.47	1.46	2.01
DS96F172/4	0	−49.5	+45.3	3.67	1.33	2.34
	−7	−63.5	+30.6	3.47	1.14	2.33
	+7	−19.2	+74.2	4.00	1.71	2.29

Note: Current into device pin is defined as positive, current out of device pin is defined as negative, VOD ≥ 1.5V (TIA/EIA-485).

OPEN INPUT FAILSAFE FEATURE

All of National's TIA/EIA-485 receivers support the *OPEN INPUT FAILSAFE* feature. This feature provides a known state (HIGH) on the receiver output for the following cases, which are illustrated in *Figure 8*. The OPEN INPUT FAILSAFE feature is integrated into the input stage of the device. Normally high value (typically 120 kΩ) bias resistors pull the plus input high, and the minus input low. The value is large enough to properly bias the receiver when the inputs are open (non-terminated).

VALID OPEN INPUT CASES:

A. Unterminated Cables—With restrictions on data rate, stub length, and cable length, it is possible to construct an interface without termination resistors. Normally the cable length is very short with respect to the driver's rise time and the reflections that occur die out long before the next transition. For the idle line, the impedance seen acros the receiver input pins is very large (open) and thus the receiver output will be a HIGH state.

B. Unconnected Nodes—In a Multi-Point configuration, up to 32 nodes can be connected to the twisted pair. Termination should only be located at the two extreme ends of the cable. Therefore, if a middle node is disconnected from the cable, the OPEN INPUT FAILSAFE feature will put the receiver output into a stable HIGH state.

C. Unused Channels—If a high integration receiver IC (multichannel) is being used, and all channels are not required, the unused channel(s) inputs can be left as no-connects. The OPEN INPUT FAILSAFE feature will force the unused channel into a stable HIGH state. This prevents the unused channel picking up external noise and oscillating, thereby increasing the power supply current (I_{CC}).

In all three cases, the impedance seen across the receiver input pins is very large or open, (∞) in contrast to a low impedance termination resistor of 150Ω or less. For these cases the receiver output will be HIGH. If the termination resistors were connected across the receiver input pins, then the receiver output is undetermined, unless the bus employs FAILSAFE biasing resistors.

SUMMARY

External FAILSAFE bias resistors can be used to solve the idle line state problem that commonly occurs in Multi-Point applications using asynchronous protocols. This is a well accepted hardware approach to solving the idle line state problem. In fact many complete INTERFACE standards have accepted this method. Examples include the Differential SCSI-1 and 2 (Small Computer System Interface) specifications, as well as the IPI (Intelligent Peripheral Interface) standard. This application note provides guidance to selecting proper resistor values that will provide an adequate FAILSAFE bias (Vfsb) while minimizing the loading effect on the driver.

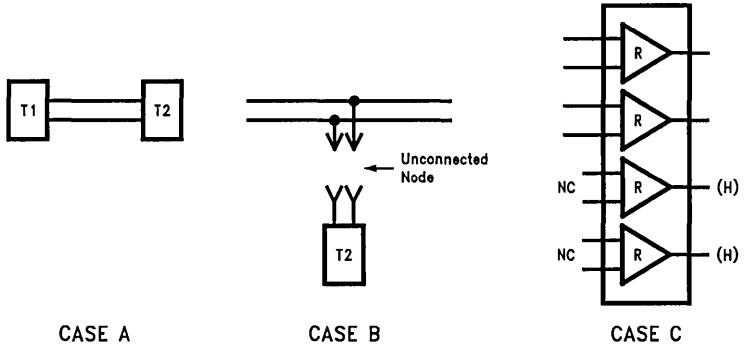

FIGURE 8. Applications of OPEN INPUT FAILSAFE Feature

APPENDIX

A more elaborate calculation that takes into account the DC resistance of the twisted pair cable is provided in this appendix. (See *Figure A-1*). For this example assume the following:

Ra = Pull Up Resistor
Rb = Slave End Cable Termination Resistor
Rc = Master End Cable Termination Resistor
Rd = Pull Down Resistor
Re = Cable DC Resistance
Rf = Cable DC Resistance
Rdcr = Re + Rf
Vfsbm = FAILSAFE Bias Potential @ Master end of cable
Vfsbs = FAILSAFE Bias Potential @ Slave end of cable

and

1. Ra = Rd for symmetrical loading
2. REQ = Rc//(Ra + Rd)
   REQ = (Rc(Ra + Rd))/(Ra + Rc + Rd).

Note A: Assume V_{CC} = 5V ± 5%.

Note B: Resistor Tolerance = ±2%.

Note C: Worst Case occurs at V_{CC} − 5%, Ra and Rd + 2%, Rb and Rc − 2%.

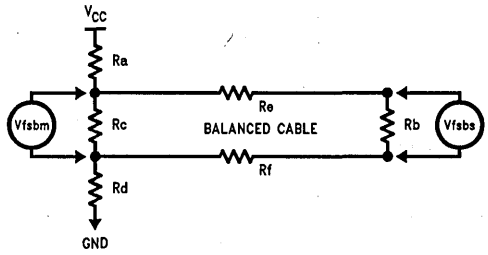

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FIGURE A-1. Cable Model

Equations:

FAILSAFE Bias at the Master end of the cable is:

$$Vfsbm = \frac{Rc//(Rb + Rdcr)}{Ra + Rd + (Rc//(Rb + Rdcr))}V_{CC}$$

$$Vfsbm = \frac{Rc(Rb + Rdcr)}{(Ra + Rd)(Rc + Rb + Rdcr) + Rc(Rb + Rdcr)}V_{CC}$$

The FAILSAFE Bias at the Slave end is simply a voltage divider between the cable DC resistance and the Slave end termination resistor.

$$Vfsbs = \frac{Rb}{Rb + Rdcr}Vfsbm$$

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3. FAILSAFE Lab Notes, Gary Murdock, National Semiconductor, 1987.

Inter-Operation of the DS14C335 with +5V UARTs

National Semiconductor
Application Note 876
John Goldie
Joe Vo

This application brief describes the inter-operation between the DS14C335 (+3.3V supply TIA/EIA-232 3 x 5 Driver/Receiver) and a +5V UART. The DS14C335, illustrated in *Figure 1,* is ideally suited for notebook and laptop computer applications which either employ one uniform +3.3V supply for all internal components or mixed +3.3V and +5V power supplies. In mixed supply applications, the DS14C335 does NOT require a +5V to +3.3V translator device between it and the UART. This application brief describes how this is accomplished.

Figure 2 illustrates a typical application where the DS14C335 provides the interface between the +5V UART and the RS-232 port. The drivers provide translation from TTL/CMOS voltage levels on the driver input pins to RS-232 compliant driver output voltage levels (> |5V|), while the receivers accept standard RS-232 input levels and translate them back to TTL/CMOS compatible output voltage levels.

Because this application specifies a +5V UART, care must be taken to consider the characteristics of three pins on the DS14C335. They are the:

D_{IN} Driver Input,
SD Shutdown,
R_{OUT} Receiver Output

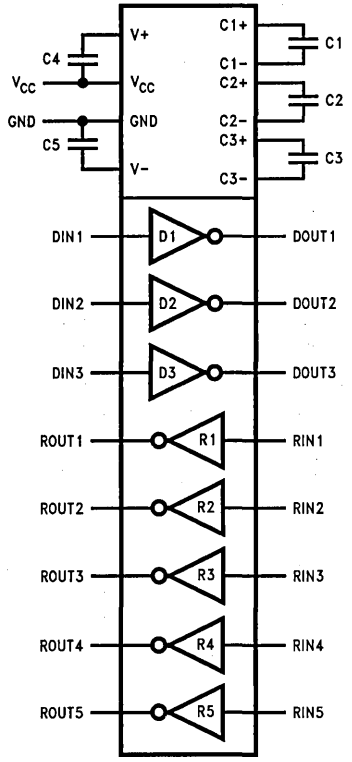

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FIGURE 1. DS14C335 Functional Diagram

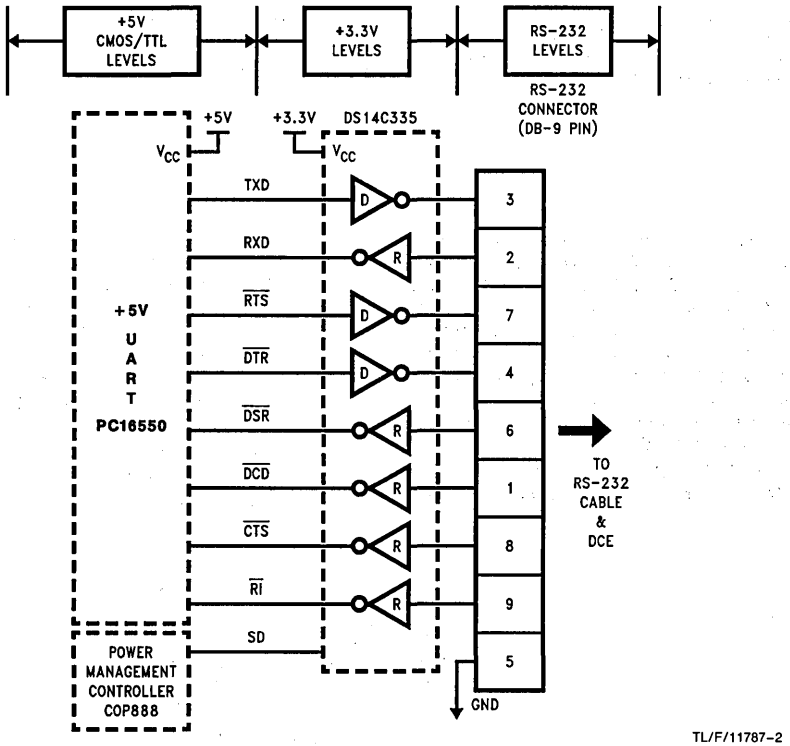
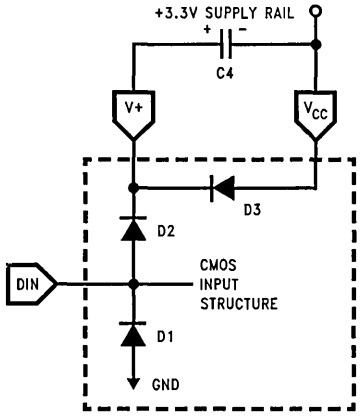


FIGURE 2. Typical Mixed Supply (3V/5V) DTE Application

Let us first examine the input structures of the D_{IN} and SD input pins, as these structures are very similar. The common circuitry is illustrated in *Figure 3* and is composed of two input protection diodes (D1 and D2). In addition, a third diode (D3) exists between the V_{CC} and V+ pins and is normally reversed biased. Diode D1 is situated between the input (D_{IN} or SD) pin and GND to clamp negative input voltages. Diode D2 is situated between the input pin and the V+ pin. When the DS14C335 is active (ON), the V+ pin is typically greater than +9V. External charge pump capacitor C4, holds 6V of charge, and is referenced to the V_{CC} (+3.3V) pin. This creates a potential of greater than +9V on the V+ pin, and is used to power the driver outputs. The input pins (D_{IN} and SD) present standard input current loading to the driving device (UART) since D1 and D2 remain reversed biased between −0.3V and one diode above the V+ pin potential (typically greater than +9V).

The DS14C335 supports another unique feature that allows the CPU to disable the device to save power when RS-232 communication is not required. The DS14C335 is put into shutdown mode, by asserting the SD pin high. This disables the internal charge pump circuit, the drivers, and also 4 of the 5 receivers, droping I_{CC} to typically 1.0 μA (10 μA maximum). One receiver remains active to monitor the Ring Indicator (RI) modem control line, to inform the CPU that a call is coming in from a remote site. In the shutdown mode, the charge pump is disabled, and the charge on C4 eventually drops to one diode below V_{CC}, or the input voltage, whichever is greater. If C4 has discharged to one diode below V_{CC}, and an input voltage is applied that is greater than V_{CC}, C4 will charge up to one diode below that level. However, no DC current flows between the input pin and the +3.3V power supply. The D_{IN} and SD pins still present standard DC loading to the driving logic. Blocking diode D3 prevents a large DC current from flowing between the input pins and the +3.3V supply when the input pin is taken above the device's +3.3V (V_{CC}) power supply pin. This is the classical problem that can occur when directly interfacing a +5V device to some +3.3V devices. A minimal amount of noise is coupled onto the V_{CC} (+3.3V) supply rail if the driver input pin is switched (0V to 5V) while the DS14C335 is in the shutdown mode. However, the magnitude is small, and power supply bypassing capacitors effectively filter out the noise. To prevent noise from coupling onto the V_{CC} rail to begin with, simply hold the driver inputs at a V_{IL} (voltage input low), since with a V_{IL} applied both diodes (D1 and D2) will remain off.



TL/F/11787–3

FIGURE 3. Input Protection Circuitry

This unique input structure allows the driver input pins and shutdown pin to accept any standard TTL/CMOS levels regardless of the DS14C335 mode (active or shutdown) or the fact that the DS14C335 is powered from a +3.3V power supply. The input pins (D_{IN} and SD) present standard loading to the driving logic with input voltages ranging from 0V to +5.5V, in magnitude.

The last pin of concern is the receiver output (R_{OUT}) pin. The R_{OUT} pin must have the drive capability to meet standard TTL/CMOS requirements. The R_{OUT} V_{OH} is specified to be greater than 2.4V at 1 mA. This drive capability should meet all standard TTL/CMOS requirements.

SUMMARY

The DS14C335's unique input structure allows the driver input (D_{IN}) and shutdown (SD) pins to present standard steady state input loading to the driving logic. Valid input voltages can range from −0.3V to greater than +5.5V, thereby enabling the device to be driven by a +5V UART in applications that employ mixed power supplies. The high drive capability of the receiver output meets the requirements of +5V logic levels, or CMOS compliant JEDEC +3.3V levels. These features make the DS14C335 the optimal single chip solution for RS-232 serial ports in +3.3V/+5V or pure +3.3V power supply laptop and notebook computer applications.

Increasing System ESD Tolerance for Line Drivers and Receivers Used in RS-232 Interfaces

National Semiconductor
Application Note 878
John Goldie
Greg Krikorian, Electromer

OVERVIEW

The Data Transmission Applications Group at National Semiconductor investigated field failures of TIA/EIA-232-E (RS-232) DS14C88 Line Drivers and DS14C89A Receivers. The devices are commonly used in computer Input/Output Interfaces, such as a terminal-DTE (Data Terminal Equipment) to modem-DCE (Data Circuit-terminating Equipment) interface. Upon completion of detailed failure analysis on the devices, it was determined that they failed due to electrical over-stress, more commonly known as EOS.

In order to identify the source and type of EOS, a number of DS14C88 and DS14C89A devices were subjected to controlled Electrostatic Discharge—ESD (Electrostatic Discharge) events in the lab using a KeyTek Human Body ESD Simulator, (per IEC801-2 requirements). Additional units were tested with PolyClamp® ESD protection devices to determine their effectiveness and to demonstrate a possible solution for providing greater system ESD tolerance.

The following conclusions have been made as a result of the investigation and bench testing:

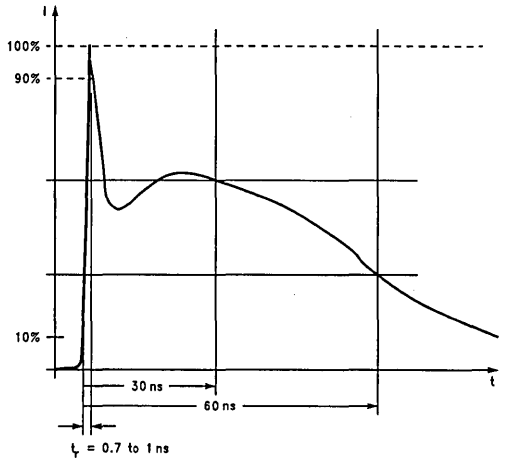
- The pins most commonly damaged are Driver Output and Receiver Input. This implies that the EOS is reaching the IC from the "outside world" via the interface cable and connector. Damage was not seen on driver input or receiver output pins.
- The external source was determined to be an ESD event by matching the failure modes and comparing die photographs of the lab induced failures with the field failures.
- The DS14C88 Line Driver and the DS14C89A Receiver would incur functional failures when subjected to an ESD event below 5,000V without the use of any external ESD protection devices.
- With PolyClamp ESD protection devices installed in the test fixture, all the IC's passed parametric and functional tests at the maximum tested ESD level of 15,000V per IEC 801-2 Specification.

INTRODUCTION

The DS14C88 Quad Line Drivers and the DS14C89A Quad Receivers are predominantly used on TIA/EIA-232-E (RS-232) serial interfaces that connect DTE's to DCE's or other DTE's. The driver outputs and receiver inputs are connected to the outside world through: a printed circuit board (PCB) trace, a connector, and a cable. The driver outputs and receiver inputs are exposed to the outside world (i.e., off the PCB). These devices can be damaged by ESD events that can be directly discharged to the connector pin. To prevent damage to the parts external transient voltage suppression (TVS) diodes have been used in the past to clamp transients to levels that the driver outputs and receiver inputs can withstand. This approach requires a board modification, and a substantial amount of PCB real estate, not to mention cost. This application brief describes a new technology that is available to provide greater ESD system protection without requiring a board modification or any extra PCB real estate. The protection device tested is known as a PolyClamp and is offered by Electromer Corporation. Testing has been conducted on a sample of driver and receiver devices and the remainder of this brief will describe the testing and the results.

TEST FIXTURES AND ESD

Special test fixtures were constructed to replicate a PCB environment. The DS14C88's and DS14C89A's were mounted in standard DIP sockets. Driver output and receiver input pins were connected to a protected 9-pin D Shell connector with the PolyClamp product integrated into the connector shell. For testing, the power supply pins V+ and V− of the DS14C88 device and the V_{CC} pin for the DS14C89A device were grounded. A single positive and a single negative ESD pulse was air discharged to the connector pin which was connected to a driver output or receiver input depending upon the IC under test. The tests were repeated with the supply pins left open. The ESD pulse applied to the connector pins conforms to the IEC801.2 Standard. The energy storage capacitance is 150 pF, while the discharge resistor is 330Ω. The ESD waveform is shown in *Figure 1*.



(Source: Electromer Corporation) TL/F/11789–1

FIGURE 1. Typical Waveform of the Output Current of the ESD Generator

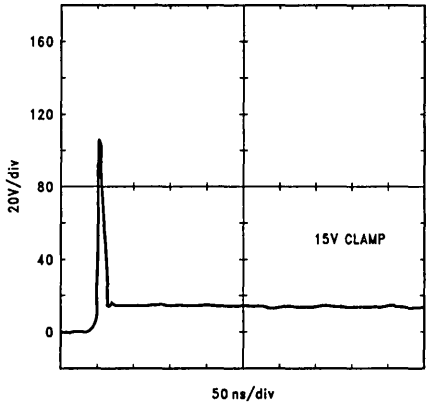
TEST RESULTS

Ten DS14C88 Quad Line Drivers were tested with the PolyClamp product. After the ESD testing, the parts were retested on the ATE (Automatic Test Equipment) final test program to determine if the device incurred any permanent damage or any degraded parameters. The results determined that the PolyClamp protected devices could withstand ESD pulses up to 15,000V, which was the upper limit of the KeyTek ESD simulator. Without the PolyClamp protected connector the DS14C88's failed functional tests after a 2,000V discharge.

Ten DS14C89A Quad Receivers were tested with the PolyClamp product. After the ESD testing, the parts were retested on the ATE final test program to determine if the device incurred any permanent damage or degraded parameters. Again the results determined that the PolyClamp protected devices could withstand ESD pulses up to 15,000V. Without the PolyClamp protected connector the DS14C89A's failed at 1,000V.

The PolyClamp product provides a high level of ESD protection to line driver and receiver integrated circuits.

Characterization testing of the PolyClamp device shows that it provides a 15V DC clamp for a 15,000V IEC801.2 ESD event (see *Figure 2*). In addition, *Figure 2* shows a typical front edge inductive spike of 100V due to test fixtures and inherent lead inductance which is similar to the performance of TVS diodes. Also, after 860 consecutive ESD pulses the PolyClamp protected connector provides the same level of ESD clamping response (see *Figure 3*). Note that the current limiting resistor (330Ω) specified in the IEC test differs from the industry standard Human Body Model (MIL-STD 883C Method 3015), which employs a 1.5 kΩ resistor. The 1.5 kΩ resistor proves a greater current limit, thus the IEC model is a more stringent test.



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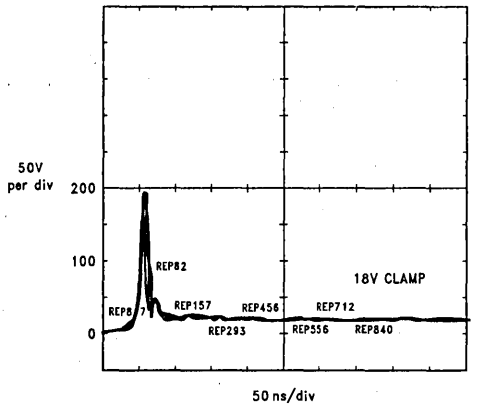
(Source: Electromer Corporation)

FIGURE 2. PolyClamp TVS Device Response to 15 kV ESD Pulse



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(Source: Electromer Corporation)

FIGURE 3. PolyClamp TVS Device Response to 860 Consecutive 15 kV ESD Pulses

CONCLUSIONS

With the use of the PolyClamp protected connectors, protection from ESD events can easily be raised to greater than 15,000V. Additional features of the PolyClamp besides its ESD clamping capability include the following:

- Requires no PCB space—by switching the connector to a protected connector, existing PCBs can be upgraded without a PCB redesign. Many different protected connectors are offered including D-Shells and modular jacks.
- No increase in part count—the protected connector provides ESD clamping for all lines in one piece (the connector), compared to TVS diodes that typically uses 1–2 devices per signal line.
- Economical—in both cost and PCB space compared to other solutions.
- Low capacitance—the protected connector presents a 5 pF typical load to the signal line, minimizing signal distortion.

There are many different ways to protect printed circuit boards and their integrated circuits from ESD and EOS events. These include on-chip enhanced ESD protection of the integrated circuits, TVS diodes, and protected connectors, to name a few. Each of these examples has its own merits and limitations. Enhancements to processes and the development of internal ESD protection circuits has raised integrated circuit tolerance from the several hundreds of volts in some cases to the thousands of volts, but at the expense of die size and cost. TVS diodes require additional PCB space compared to the protected connectors. These two points further illustrate the merits that the protected connectors offer. The PolyClamp protected connectors offer an extremely high level of protection, without additional

PCB space, minimizes part count, and provides a *new* economical solution to increased system level ESD protection.

It should also be noted that protection capability is also offered integrated into common I/O connectors such a D-Sub, MJ, DIN, from AMP Corporation and a similar technology is available from other vendors.

RECOMMENDATIONS

The following guidelines are recommended to reduce the chance of ESD events damaging the line drivers and receivers:

a) When installing or removing the cable, power should be turned off at both ends of the system if possible.

b) Avoid physically touching the connector pins when handling the cable, and wear a ground strap when possible.

c) The use of built-in system level ESD protection devices can extend the level of ESD tolerance.

REFERENCE

For additional information on ESD see also:

Reliability and Electrostatic Discharge, Chapter 10, *Reliability Handbook*, National Semiconductor, 1987

AN-248, Electrostatic Discharge Prevention, *CMOS Logic Databook*, National Semiconductor, 1988

For additional information on PolyClamp Products contact:

Electromer Corporation
1047 Elwell Court
Palo Alto, CA 94303
415-903-7050
415-903-9011 (FAX)

A Comparison of Differential Termination Techniques

National Semiconductor
Application Note 903
Joe Vo

INTRODUCTION

Transmission line termination should be an important consideration to the designer who must transmit electrical signals from any point A to any point B. Proper line termination becomes increasingly important as designs migrate towards higher data transfer rates over longer lengths of transmission media. However, the subject of transmission line termination can be somewhat confusing since there are so many ways in which a signal can be terminated. Therefore, the advantages and disadvantages of each termination option are not always obvious.

The purpose of this application note is to remove some of the confusion which may surround signal termination. This discussion, however, will focus attention upon signal termination only as it applies to differential data transmission over twisted pair cable. Common differential signal termination techniques will be presented and the advantages and disadvantages of each will be discussed.

Each discussion will also include a sample waveform generated by a setup consisting of a function generator whose signals are transmitted across a twisted pair cable by a differential line driver and sensed at the far end by a differential line receiver. This application note will specifically address the following differential termination options:

- Unterminated
- Series/Backmatch
- Parallel
- AC
- Power (Failsafe)
- Alternate Failsafe
- Bi-Directional

For the purposes of discussion, popular TIA/EIA-422 drivers and receivers, such as the DS26LS31 and DS26LS32A, will be used to further clarify differential termination.

UNTERMINATED

The selection of one termination option over another is oftentimes dictated by the performance requirements of the application. The selection criteria may also hinge upon other factors such as cost. From this cost perspective the option of not terminating the signal is clearly the most cost effective solution. Consider *Figure 1,* where a DS26LS31 differential driver and a DS26LS32A differential receiver have been connected (using a twisted pair cable) together without a termination element. Because there is no signal termination element, the DS26LS31 driver's worst case load is the DS26LS32A receiver's minimum input resistance.

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FIGURE 1. Unterminated Configuration

Since, TIA/EIA-422-A (RS-422) standard defines the DS26LS32A's minimum input resistance to be 4 kΩ, the driver's worst case load, as seen in *Figure 1,* is then 4 kΩ.

In the unterminated configuration, the DS26LS31 driver is only required to source a minimal amount of current in order to drive a signal to the receiver. This minimal DC current sourcing requirement in turn minimizes the driver's on chip power dissipation. In addition, the 4 kΩ driver output load results in a higher driver output swing (than if the driver was loaded with 100Ω) which in turn increases DC noise margin. This increase in noise margin further diminishes the possibility that system noise will improperly switch the receiver. To be sure that there is no confusion, noise margin is defined as the difference between the minimum driver output swing and the maximum receiver sensitivity. On the other hand, if a receiver was used which complies to TIA/EIA-485 (RS-485), the resulting noise margin would be even greater. This is because the minimum input resistance of an RS-485 receiver must be greater than 12 kΩ as compared to 4 kΩ for an RS-422 receiver.

The absence of a termination element at the DS26LS32A's inputs also guarantees that the receiver output is in a known logic state when the transmission line is in the idle or open line state (receiver dependent). This condition is commonly referred to as open input receiver failsafe. This receiver failsafe (Note 1) bias is guaranteed by internal pull up and pull down resistors on the positive and negative receiver inputs, respectively. These pull up and pull down resistors bias the input differential voltage (V_{ID}) to a value greater than 200 mV when the line is, for example, idle (un-driven). This bias is significant in that it represents the minimum guaranteed V_{ID} required to switch the receiver output into a logic high state.

Note 1: A complete discussion of receiver failsafe can be found in Application Note 847 (AN-847).

There are, however, some disadvantages with an unterminated cable. The most significant effect of unterminated data transmission is the introduction of signal reflections onto the transmission line. Basic transmission line theory states that a signal propagating down a transmission line will be reflected back towards the source if the outbound signal encounters a mismatch in line impedance at the far end. In the case of *Figure 1,* the mismatch occurs between the characteristic impedance of the twisted pair (typically 100Ω) and the 4 kΩ input resistance of the DS26LS32A. The result is a signal reflection back towards the driver. This reflection then encounters another impedance mismatch at the driver outputs which in turn generates additional reflections back toward the receiver, and so on. The net result is a number of reflections propagating back and forth between the driver and receiver. These reflections can be observed in *Figure 2.*

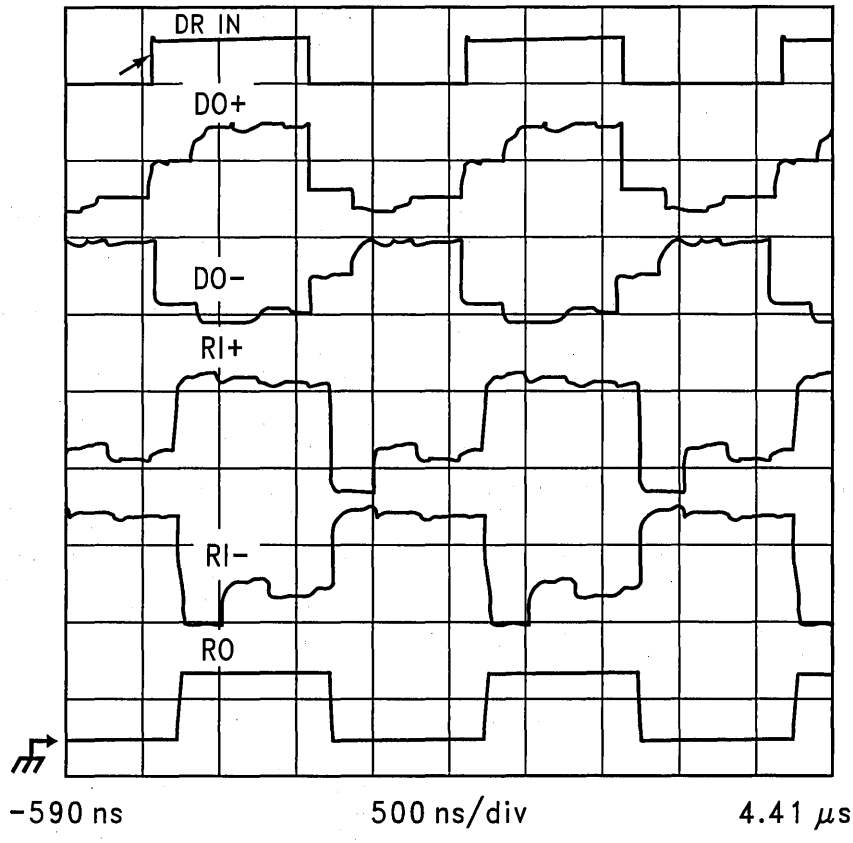

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FIGURE 2. Unterminated Waveforms

The main limitation of unterminated signals can be clearly seen in *Figure 2.* A positive reflection is generated when the signal encounters the large input resistance of the receiver. These reflections propagate back and forth until a steady state condition is reached after several round trip cable delays. The delay is a function of the cable length and the cable velocity. *Figure 2* shows that the reflections settle after three round trips. To limit the effect of these reflections, unterminated signals should only be used in applications with low data rates and short driving distances.

The data being transmitted should, therefore, not make any transitions until after this steady state condition has been reached. A low data rate ensures that reflections have sufficient time to settle before the next signal transition. At the same time, a short cable length ensures that the time required for the reflections to settle is kept to a minimum. The low data rate and short cable length dictated by the lack of termination is probably the most significant shortcoming of the unterminated option.

Low speed is generally characterized to be either signalling rates below 200 kbits/sec or when the cable delay (the time required for an electrical signal to transverse the cable) is substantially shorter than the bit width (unit interval) or when the signal rise time is more than four times the one way propagation delay of the cable (i.e., not a transmission line). As a general rule, if the signal rise time is greater than four times the propagation delay of the cable, the cable is no longer considered a transmission line.

It should be mentioned that most differential data transmission applications provide for some kind of signal termination. This is because most differential applications transmit data at relatively high transfer rates over relatively long distances. In these type of applications, signal termination is critically important. If the application only requires low speed operation over short distances, an unterminated transmission line may be the simplest solution.

SERIES TERMINATION

Another termination option is popularly known as either series or backmatch termination. *Figure 3* illustrates this type of termination. The termination resistors, R_S, are chosen such that their value plus the impedance of the driver's output equal the characteristic impedance of the cable. Now as the driven signal propagates down the transmission line an impedance mismatch is still encountered at the far end of the cable (receiver inputs).

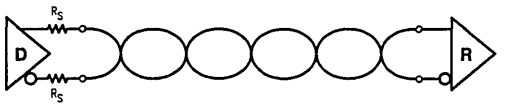

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FIGURE 3. Series Termination Configuration

However, when that signal propagates back to the driver the reflection is terminated at the driver output. There is only one reflection before the driven signal reaches a steady state condition. How long it takes for the driven signal to reach steady state is still dependent upon the length of cable the signal must traverse. As with the unterminated option the driver power dissipation is still minimized due to the light loading presented by the 4 kΩ receiver input resistance. The driver loading remains unchanged from the unterminated option. In both cases the driver is effectively loaded with the receiver's input impedance. DC noise margin has again increased and the open input receiver failsafe feature is still supported for idle and open line conditions.

There are three major disadvantages in using series termination. First, the driver output impedances can vary, due to normal process variations, from one manufacturer to another and from one driver load to another. Should there be a problem which involves replacing line drivers, there is a chance that the designer might have to rework the board in order to ensure that the R_S matches the new driver's output impedance.

Second, series termination is commonly limited to only point to point applications. Consider the following example. If a second receiver (multidrop application) was located halfway between the driver and receiver at the far end of the cable, the noise margin seen by the middle receiver would change between the incident signal and the reflected signal. Such a problem would not exist in a point to point application where only one receiver is used with one driver.

Third, there is still an impedance mismatch at the receiver inputs. Again, this mismatch is caused by a signal propagating down a 100Ω cable suddenly encountering a 4 kΩ receiver input resistance. This impedance mismatch will continue to cause reflections on the transmission line as illustrated in *Figure 4*.

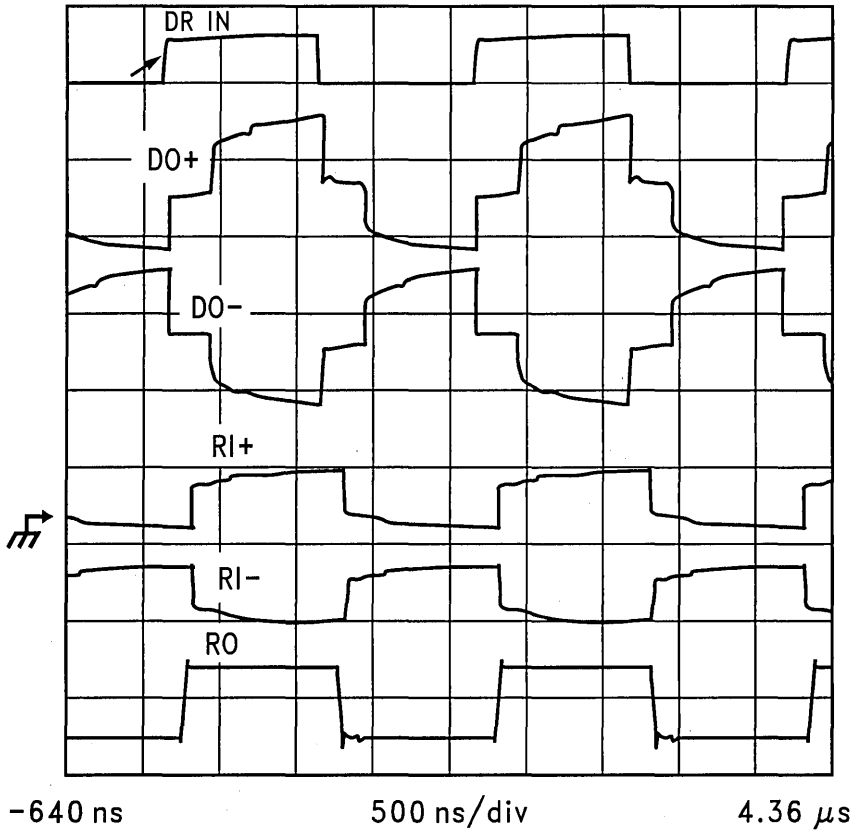

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FIGURE 4. Series Termination Waveforms

Notice the reflections which result when the driven signal encounters an impedance mismatch at the receiver input. The reflection propagates back to the driver and is somewhat terminated by the driver's output impedance. The reflected signal is terminated because the combined impedance of the series resistor (R_S) and the driver's output impedance comes close to matching the characteristic impedance of the cable. In contrast with *Figure 2's* unterminated signal waveform, the waveform seen in *Figure 4* is characterized by only one reflection.

In all it will take the signal one round trip cable delay to be reflected back towards the signal source. Since all reflections should be allowed to settle before the next data transition (to maintain data integrity), it is imperative that the round trip cable delay be kept much less than the time unit interval (TUI—defined to be the minimum bit width or the "distance" between signal transitions). In other words, series termination should be limited to applications where the cable lengths are short (to minimize round trip cable delays) and the data rate is low (to maximize the TUI). And to a lesser degree, the series termination option may not be the ideal choice from a cost perspective in that it requires two additional external components.

PARALLEL TERMINATION

Parallel termination is arguably one of the most prevalent termination schemes today. In contrast to the series termination option, parallel termination employs a resistor across the differential lines at the far (receiver) end of the transmission line to eliminate all reflections. See *Figure 5.*

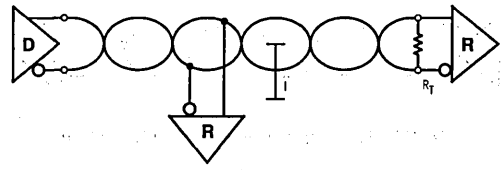

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FIGURE 5. Parallel Termination Configuration

Eliminating all reflections requires that R_T be selected to match the characteristic impedance (Z_O) of the transmission line. As a general rule, however, it is usually better to select R_T such that it is slightly greater than Z_O. Over-termination tends to be more desirable than under-termination since over-termination has been observed to improve signal quality. R_T is typically chosen to be equal to Z_O. When over-termination is used R_T is typically chosen to be up to 10% larger than Z_O. The elimination of reflections permits higher data rates over longer cable lengths. Keep in mind, however, that there is an inverse relationship between data rate and cable length. That is, the higher the data rate the shorter the cable and conversely the lower the data rate the longer the cable. Higher data rates and longer cable lengths translate simply into smaller TUI's and longer cable delays. Unlike series termination where high data rates and long cable lengths can negatively impact data integrity, parallel termination can effectively remove all reflections; thereby removing all concerns about reflections interfering with data transitions. See *Figure 6.*

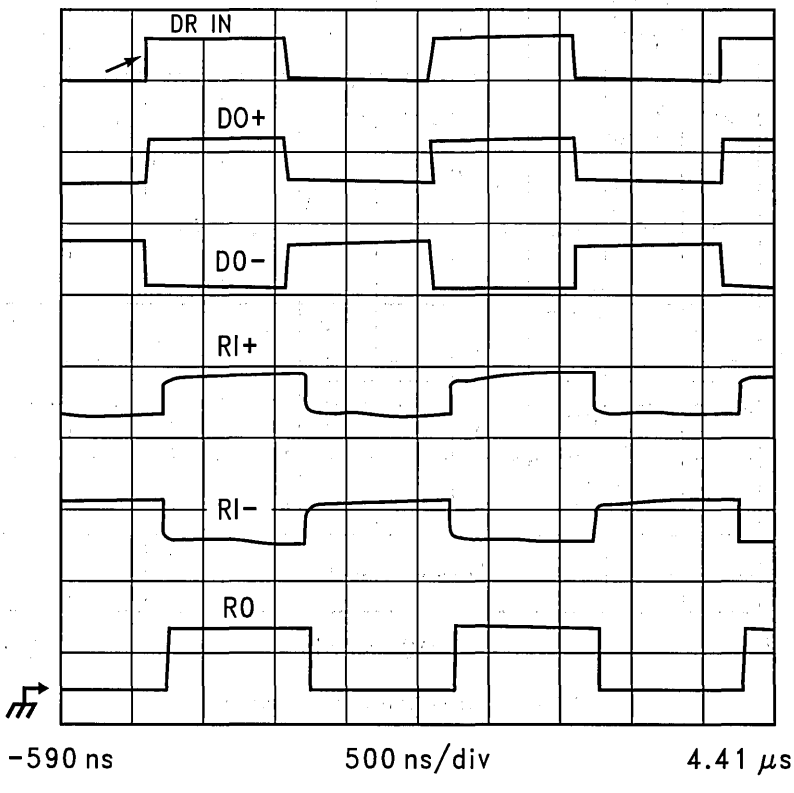

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FIGURE 6. Parallel Termination Waveforms

As seen in *Figure 6* both driver output and receiver input signals are free of reflections. Such results make parallel termination optimal for use in either high speed (10 Mb/s), or long cable length (up to 4000 feet), applications.

Another benefit the parallel termination provides is that both point to point and multidrop applications are supported. Recall that multidrop is defined as a distribution system composed of one driver and up to ten receivers spread out along the cable as defined in the TIA/EIA-422 standard. The parallel termination is located at the far end (opposite the driver) of the cable and effectively terminates the signal at that location, preventing reflections.

There are also disadvantages to parallel termination. Let's examine these disadvantages as they pertain to multidrop configurations. An intrinsic assumption to multidrop operation is that stub lengths, as measured by "l" in *Figure 5*, are minimized. Despite the fact that all receivers are effectively terminated with R_T, long stub lengths will once again reintroduce impedance mis-matches and reflections. So while parallel termination may remove reflections and permit multidrop configurations, it does place a restriction upon the stub lengths associated with these other receivers. Typically stubs should be kept to less that ¼ of the drivers rise time in length to minimize transmission line effects, and reflections.

TIA/EIA-422-A standard does recommend a 100Ω resistor to be used when the differential line is parallel terminated. Therefore, applications which use a TIA/EIA-422-A driver such as the DS26LS31 or DS26C31 are commonly terminated with 100Ω at the far end of the twisted pair cable. While the 100Ω parallel termination eliminates all reflections, the power dissipated by the driver will increase substantially with the addition of this resistor. This increased driver power dissipation is a major disadvantage of parallel termination. The absence of this termination resistor keeps driver power dissipation low for unterminated and series terminated drivers and is a major advantage of these two termination options.

Noise margin will also decrease with parallel termination. The relatively light loading (4 kΩ) of unterminated and series terminated drivers led to larger driver output swings. The heavier driver load (typically 100Ω) brought on by parallel termination reduces the driver's output signal swing. However, even with this reduction, there is ample noise margin left to ensure that the receiver does not improperly switch.

Recall the discussion earlier about receiver failsafe with the unterminated and series options. In both cases, open input receiver failsafe operation was guaranteed because of internal circuitry (receiver dependent) which biases the differential input voltage (V_{ID}) to a value greater than its differential threshold. Since the resulting bias voltage at the receivers inputs (V_{ID}), is greater than +200 mV, the output of the DS26LS32A receiver remains in a stable HIGH state. Unlike unterminated and series options, parallel termination cannot support open input receiver failsafe when the transmission line is in the idle state. This shortcoming of parallel termination is discussed in much greater detail later in the section which describes power and alternate failsafe termination (see AN-847 for more of information on failsafe biasing differential buses).

AC TERMINATION

The effectiveness of parallel termination is oftentimes countered by increased driver power dissipation and receiver failsafe concerns. The DC loop current required by the termination resistor, R_T (see *Figure 5*), is often too large in order to be useful for power conscious applications or for seldomly switched control lines. In asynchronous applications, parallel termination's is not able to guarantee receiver failsafe during idle bus states which in turn makes the system susceptible to errors such as false start bits and framing errors. The primary reason for the AC termination, however, grew out of the need for effective transmission line termination with minimal DC loop current.

A representation of an AC terminated differential line is shown in *Figure 7*.

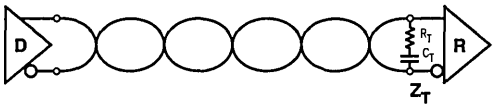

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FIGURE 7. AC Termination Configuration

The value of R_T generally ranges from 100Ω–150Ω (cable Z_O dependent) and is selected to match the characteristic impedance (Z_O) of the cable. C_T, on the other hand, is selected to be equal to the round trip delay of the cable divided by the cable's Z_O.

EQ1: $C_T \leq$ (Cable round trip delay) / Z_O

For this example:

Cable Length = 100 feet
Velocity = 1.7 ns/foot
Char. Impedance = 100Ω

Therefore,

$C_T \leq (100\text{ ft} \times 2 \times 1.7\text{ ns/ft})/100\Omega$ or $\leq$ 3,400 pF.

Further, the resulting R_C time constant should be less than or equal to 10% of the unit interval (TUI). In the example provided the maximum switching rate therefore should be less than 300 kHz. This termination should now behave like a parallel termination during transitions, but yield the expanded noise margins during steady state conditions. See *Figure 8*.

Figure 8 illustrates the tradeoff between parallel terminated and unterminated signals. There are no major reflections and driver power dissipation is reduced at the expense of a low pass filtering effect which essentially limits the application of AC termination to low speed control lines. Note that the frequency of the driven signal in *Figure 8* is 300 kHz whereas it was 500 kHz for the other plots. This was done to maintain the ratio between bit time and the R_C time constant. The draft revision of RS-422-A will include AC termination as an alternative to parallel termination.

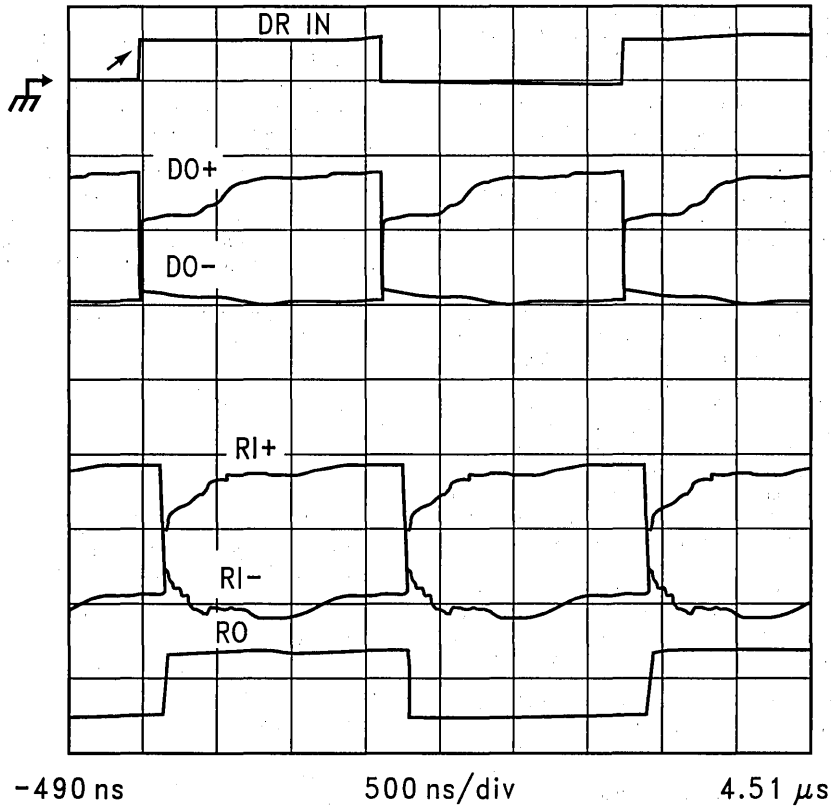

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FIGURE 8. AC Termination Waveforms

The waveforms in *Figure 8* should be viewed together with the following brief explanation of how AC termination works. When the driven signal transitions from one logic state to another, the capacitor C_T behaves as a short circuit and consequently, the load presented to the driver is essentially R_T. However, once the driven signal reaches its intended levels, either a logic HIGH or logic LOW, C_T will behave as an open circuit. DC loop current is now blocked. The driver power dissipation will then decrease. The load presented to the driver also decreases. This is due to the fact that the driver is now loaded with a large receiver input resistance typically greater than 4 kΩ; versus the typical R_T of 100Ω–120Ω. This reduced loading condition increases the signal swing of the driver and results in increased noise margin. The idle bus state also forces C_T into the open circuit mode. Once this takes place, the receiver's internal pull up and pull down resistors will bias the output into a known state. Therefore, besides minimizing DC loop current, preventing line reflections, and increasing noise margin, AC termination also supports open input receiver failsafe.

As with all the previously discussed termination options, there are disadvantages in using AC termination. AC termination introduces a low pass filtering effect on the driven signal which tends to limit the maximum data rate of the application. This data rate limitation is the result of the impact that R_T and C_T, together, have upon the driven signal's rise time. How much the data rate is limited is dependent upon the selection of R_T and C_T. Long R_C time constants will have a greater impact upon the driven signal's maximum data rate, and vice versa. Because of of these data rate limitations, the transmission lines best suited for AC termination are typically low speed control lines where level sensitivity is desired over edge sensitivity. Finally, the part count required by AC termination can put it at a disadvantage in cost conscious applications.

POWER TERMINATION

Recall that AC termination is intended primarily to eliminate the large DC loop current inherent in parallel termination. The power termination, on the other hand, addresses parallel termination's inability to support receiver failsafe during the idle bus state. See *Figure 9* for an illustration of a transmission line terminated using the power option.

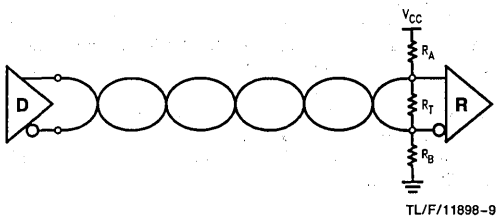

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FIGURE 9. Power Termination Configuration

The lack of R_A and R_B, when the bus is idle, almost assures that the receiver output will not be in a known state. This is due to the insufficient voltage across R_T (on the order of 1 mV–5 mV) as caused by the receiver's internal high value pull up and pull down resistors. The presence of these internal pull up and pull down resistors will guarantee receiver failsafe only for the open input condition. In order to switch the receiver into the logic high state, regardless of whether the bus is open or idle, a minimum of +200 mV (with respect to the inverted receiver input) must be developed across R_T. The sole purpose, then, of R_A and R_B is to establish a voltage divider whereby at least +200 mV will be dropped across R_T. A complete explanation of selection criteria for resistor values (R_A and R_B) can be found in AN-847.

The addition of external receiver failsafe biasing resistors, however, does pose some concerns. The primary drawback relates to the increased driver loading with the addition of R_A and R_B. The increased driver loading decreases the driver's output swing and, in turn, reduces the noise margin. Higher driver power dissipation is also symptomatic of the increased driver loading since the driver must source the additional current required by the external failsafe network. One last concern is that the extra cost and subsequent handling of two additional resistors (excluding R_T) might outweigh power termination's advantages in some applications.

ALTERNATE-FAILSAFE TERMINATION

This version of failsafe termination is essentially an extension of power termination. The addition of R_C and R_D greatly enhances the receiver's ability to operate in harsher environments. See *Figure 10*.

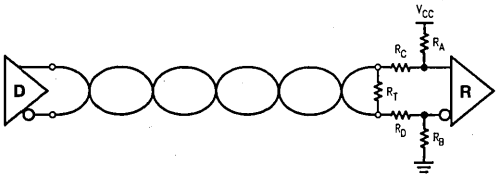

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FIGURE 10. Alternate Failsafe Termination Configuration

The advantages of this failsafe termination point directly to this increased ruggedness. A transmission line terminated using the failsafe option will be able to withstand larger common mode voltages. A careful selection of R_C and R_D will determine how much more common mode voltage a line can endure. This is because R_C and R_D act as a voltage dividers between the receivers input resistance. The TIA/EIA-422-A standard allows for common mode shifting up to 7V in magnitude, however most integrated circuits support absolute maximum rating that exceed the ±7V limit. The DS26LS32A supports a ±25V ABS MAX input rating. Careful selection of resistors can allow common mode voltages in the 35V–45V range on the cable, while still honoring the 25V limit in the receiver input pins. R_C and R_D are typically 4.7 kΩ, while R_A and R_B are 47 kΩ. This provides 9.5 kΩ between the receiver input pins, and also allows the pull up and pull down resistors to be increased in value to 47 kΩ. This capability lends itself well to applications, such as factory control and building to building data transmission, where the common mode range can occasionally exceed ±7V.

Failsafe termination also guarantees receiver failsafe for open, idle, as well as shorted line conditions. Of all the terminations options discussed, the failsafe option is the only one for which receiver failsafe can be guaranteed for shorted differential lines. Shorting the differential lines together merely shorts out R_T. In this short condition, the receiver will still see the series combination of R_C and R_D across its inputs. Receiver failsafe can, therefore, still be supported. The short condition just described yields another benefit of failsafe termination. The increased impedance between V_{CC} and ground, with the addition of R_C and R_D, also results in increased fault or short circuit current limiting.

While the addition of R_C and R_D improves the transmission line's ability to withstand larger common mode voltages, it might also negatively impact the receiver's sensitivity. Consider, for example, a TIA/EIA-422 receiver. The minimum differential input signal (V_{ID}) required to switch the receiver is normally |200 mV|. Depending on the values of R_C and R_D, it may be necessary to develop a minimum of +400 mV across R_T in order to ensure that there is at least 200 mV across the receiver input terminals. The other significant disadvantage with failsafe termination may be the number of resistors required to implement it. Five resistors per line may prove too costly.

BI-DIRECTIONAL TERMINATION

The last type of termination which will be discussed is known as bi-directional termination. *Figure 11* illustrates a typically multipoint application composed of drivers, receivers, and transceivers. Bi-directional termination is parallel termination carried one step further. Bi-directional termination now permits multiple drivers (multipoint configuration) to be connected to the same twisted pair. With multiple drivers connected to the same twisted pair, data can now be transmitted in two directions. Keep in mind, however, that while data transmission can now take place in two directions, only half duplex transmission is allowed (as defined by TIA/EIA-485 standard). Multiple TIA/EIA-485 drivers cannot simultaneously drive the line since this would result in line contention. It should be mentioned that system timing should be carefully inspected to ensure that line contention does not occur. The advantages in using bi-directional termination are almost identical to those with parallel termination.

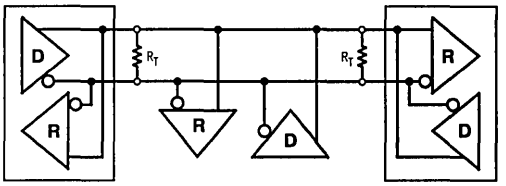

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FIGURE 11. Bi-Directional Termination Configuration

These advantages include the prevention of signal reflections, and the ability to drive long transmission lines at high data rates. As with parallel termination, R_T should be selected so that it matches the characteristic impedance (Z_O) of the twisted pair cable.

The disadvantages in using parallel termination also extend to bi-directional termination. Receiver failsafe cannot be guaranteed due to the interaction between R_T and the receiver's open circuit failsafe network. Stub lengths must be minimized and an R_T must each be placed at both extreme ends of the line in order to minimize transmission line effects. However, when two termination resistors are placed at the far ends of the cable, the effective load of the driver is

now 60Ω (since R_T is typically 120Ω). This "doubling" of the driver load, using bidirectional termination, has two effects. First, it places a greater demand upon the driver's ability to source current. As described above, a multipoint driver must be able to source approximately twice the amount of current that is required from a multidrop driver. A driver expected to meet this increased current demand naturally experiences greater power dissipation. And second, noise margin tends to be reduced since the driver's output levels tend to decrease with increased loading.

CONCLUSION

The advantages and disadvantages of unterminated lines and those with series, parallel, AC, power, failsafe, and bidirectional terminations were contrasted. It should now be clear that there is no one termination scheme which is suited for all applications. Table I provides a summary of the differential termination options discussed in this application note.

TABLE I. Termination Summary

Termination	Signal Quality	Data Rate	Comments
Unterminated	Poor	Low	Low Power
Series	Good	Low	Low Power
Parallel	Excellent	High	Single Resistor
AC	Good	Med.	Ideal for use on control lines
Power	Excellent	High	Failsafe bias for idle line
Alt. Failsafe	Excellent	High	Failsafe for open, shorted, and idle lines
Bi-Directional	Excellent	High	Ideal for bidirectional half duplex operation

The termination scheme used will essentially be dictated by the needs of the system. Specifically, the choice of termination will depend upon the system's data transmission requirements.

SPECIAL NOTES

The waveforms illustrated in this application note were acquired from laboratory testing of TIA/EIA-422 (RS-422) Drivers, and Receivers under the following conditions:

- DS26LS31 Quad Differential Driver
- DS26LS32A Quad Differential Receiver
- Cable = 100', 24AWG, 100Ω, twp cable (Berk-Tek #520382)
- Driver input signal with f = 500 kHz, V_{IH} = 3.0V, V_{IL} = 0V, Duty cycle = 50%
- V_{CC} = 5.0V
- T_A = 25°C

The cable selected for this testing was supplied by Berk-Tek Inc. and represents a typical twisted pair cable commonly used in TIA/EIA-422 applications. Additional information on cables can be obtained from:

Berk-Tek Inc.
132 White Oak Road
New Holland, PA 17557
(717) 354-6200

The RS-422-A standard was developed by the Technical Recommendation (TR30.2) TIA/EIA committee on DTE-DCE Interfaces. Since publication of the revision A, the EIA (Electronic Industries Association) has aligned with the TIA (Telecommunications Industry Association), and future revisions and new standards carry the TIA/EIA prefix, replacing the familiar "RS" (for Recommended Standard) prefix. Revision "B" of RS-422-A is expected in late 1993, and will become TIA/EIA-422-B.

REFERENCES

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Data Transmission Lines and Their Characteristics,
K. True, National Semiconductor, Application Note AN-806.

Reflections: Computations and Waveforms, K. True, National Semiconductor, Application Note AN-807.

FAILSAFE Biasing of Differential Buses,
J. Goldie, National Semiconductor, Application Note AN-847.

An Introduction to the Differential SCSI Interface

National Semiconductor
Application Note 904
John Goldie

OVERVIEW

This application note is the first in a two part series on the SCSI interface and National's new RS-485 (TIA/EIA-485) hex transceiver. The scope of this application note is to provide an introduction to the SCSI Parallel Interface and insight into the differential option specified by the SCSI standards. This application covers the following topics:

- The SCSI Interface
- Why Differential SCSI?
- The SCSI Bus
- SCSI Bus States
- SCSI Options: Fast and Wide
- The SCSI Termination
- The DS36BC956 Hex Transceiver
- SCSI Controller Requirements and the National DP8497 SDDC
- Other SCSI Controller Connections
- Summary of SCSI Standards
- References/Standards

The companion Application Note (AN-905) focuses on the features of National's new RS-485 hex transceiver. The DS36BC956 specifically designed for use in differential SCSI applications is also optimal for use in other high speed, parallel, multipoint applications.

THE SCSI INTERFACE

The Small Computer System Interface is an ANSI (American National Standards Institute) interface standard defining a peer to peer generic input/output bus (I/O bus). The intention of the SCSI standard is to provide a fast, multipoint parallel bus that is easily upgradeable and keeps pace with advancing technologies.

The SCSI interface is commonly the interconnect of choice for high performance hard disk drives. Being a generic interface, the SCSI bus is not limited to only one type of peripheral. It is also commonly used to interconnect optical drives, tape drives, disk arrays, scanners, printers, and other targets to a wide range of terminals, computers, and other hosts. It is important to also remember that a SCSI bus is not a point to point bus, but rather a multipoint bus, allowing up to eight different devices to be connected to the same daisy chained cable (SCSI-1 and 2 allows up to eight devices while the proposed SCSI-3 standard will allow up to 32 devices). A typical SCSI bus configuration is shown in *Figure 1*.

WHY DIFFERENTIAL SCSI?

In comparison to single-ended SCSI, differential SCSI costs more and has additional power and PC board space requirements. However, the gained benefits are well worth the additional IC cost, PCB space, and required power in many applications. Differential SCSI provides the following benefits over single-ended SCSI:

- **Reliable High Transfer Rates**—easily capable of operating at 10MT/s without special attention to terminations.
- **High Noise Rejection**—the differential transmission scheme provides excellent common mode rejection over a wide bus voltage range.
- **Long Cable Lengths**—cables can be as long as 25 meters in length compared to 3 meters or less for single-ended interfaces.
- **Superior AC Performance**—high performance transceivers with tightly specified and guaranteed AC performance.
- **Fault Tolerance**—current limiting and thermal shutdown protection integrated into the differential driver design.

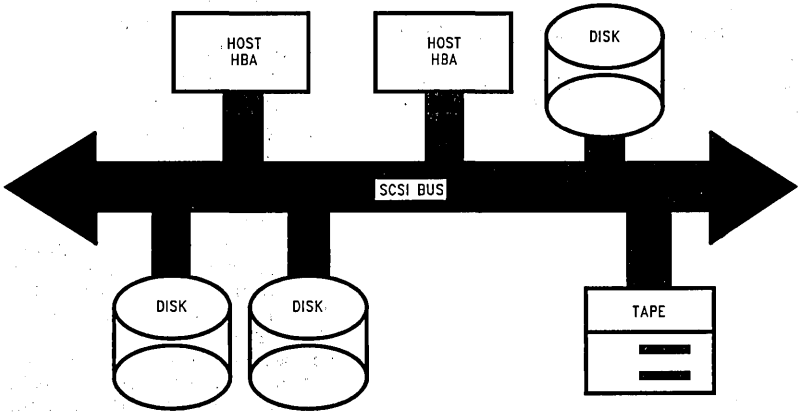

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FIGURE 1. Typical SCSI Bus Configuration-Multiple Hosts/Multiple Targets

Signal quality and long cable runs are the two major enhancements differential SCSI offers over single-ended SCSI. As stated above, differential SCSI allows for cable runs up to 25 meters in length compared to only 3 meters of single-ended SCSI. Differential SCSI is optimal for connecting together terminals with storage arrays located in a separate cooled computer room. The differential transmission scheme offers superior noise rejection and signal quality compared to a TTL single-ended bus.

Differential buses are also immune to minor termination problems that commonly plague the single-ended SCSI bus. These problems can, and commonly do have major impact on single-ended system performance. By expanding the cable length beyond 3 meters, by mixing different cable types (impedance), by using different types of termination, or by using the standard passive termination, system throughput may be reduced as great as 50%. Since it has been determined that the original single-ended termination recommended in the SCSI-1 standard does not provide adequate signal termination performance for Fast SCSI, the SCSI-2 and proposed SCSI-3 standards recommend the use of alternate terminations. There are three popular alternatives to the passive resistive terminators. These are the Boulay termination (voltage regulated), Current Regulated Terminations, and the FPT (forced perfect termination). Each has its own merits and limitations, and in fact the FPT offers good performance but is not sanctioned by the standard. Trouble can arise in single-ended SCSI applications when different types of termination are used on the bus. In addition, some SCSI controllers now provide totem pole outputs on the high speed lines (REQ and ACK) to improve the signal quality on those lines on the de-assert edge (active negation in industry jargon). These active negation drivers can become in contention with the alternative termination techniques and cause thermal problems and data corruption. Single-ended SCSI termination have caused much grief, and discussion in the SCSI standard committee.

In contrast Differential SCSI has not encountered the problems that drove the single-ended interface to develop so many alternative terminations. Differential SCSI uses a standard passive resistor termination (described in detail later in this application note). This terminator remains unchanged from the original SCSI-1 standard to the proposed SCSI-3 physical layer.

National's DS36BC956 Low Power BiCMOS HEX Differential Bus Transceiver supports these benefits and features listed above and also provides the designer with the following features over other single-ended drivers and other lower performance RS-485 transceivers:

- Ultra Low Power BiCMOS Transceiver
- Lower Maximum Junction Temperature
- Tighter Skew Specifications
- Full Compliance to the RS-485 Standard
- Full Compliance to the SCSI Standard
- Reduction in Package Height
- Smaller PCB Footprint

These features make the DS36BC956 the ideal choice for leading edge differential SCSI applications, as it offers a true balance between AC performance, integration and PCB footprint.

THE SCSI BUS

The SCSI bus is composed of a minimum of 18 signal lines. An option is provided to add extra bytes to boost system throughput (Mega Bytes per second (MB/s)) if required by the application. The SCSI 1 and 2 standards define two types of electrical characteristics; single-ended and differential.

Single-ended drivers (typically 48 mA open drain drivers) and receivers are commonly integrated onto the SCSI controller chips. For the differential option, external RS-485 transceivers are required. Integrating the differential transceivers onto the SCSI controller is not feasible due to the additional pins required for differential operation, and the additional power dissipation. Additionally the semiconductor processes commonly used for the controllers are not compatible with the special high speed/high voltage breakdown processes used for RS-485 transceivers.

The single-ended and differential modes are exclusive, and can not inter-operate. Of the 18 lines, 9 are data path (data plus parity) and the others are control. The lines are:

- Data Path
  - DB(7–0,P)—Data Bus
- Control
  - REQ—Request
  - ACK—Acknowledge
  - BSY—Busy
  - SEL—Select
  - C/D—Control/Data
  - I/O—Input/Output
  - MSG—Message
  - ATN—Attention
  - RST—Reset

The SCSI Standard has two types of devices, which are "Initiators" (typically a host computer); and "Targets" (typically drives). Of the 18 lines, 9 are bi-directional, 7 are unidirectional direction, and 2 are wire-ORed. The data bus (DB0–DB7 and DBP) are the bi-directional lines. Three control lines are Initiator to Target only lines; these are the ACK, ATN, and SEL* lines. Four lines are Target to Initiator only lines; these are the C/D, I/O, REQ, and MSG lines. A pictorial representation of the signal lines is shown in *Figure 2.*

(* SEL can also be a wire-ORed line, but is more commonly implemented as a initiator to target line).

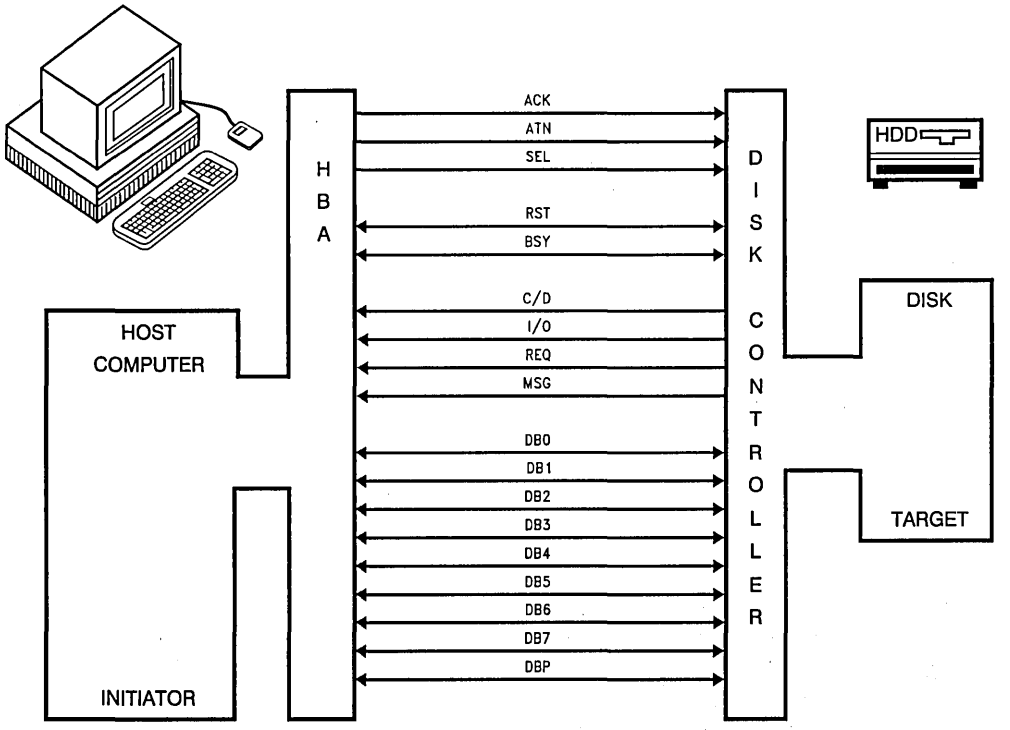

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FIGURE 2. The SCSI Signal Lines

Of the 18 lines, two, REQ and ACK, can operate at switching rates up to 10 MHz. They are defined as handshake lines, that in the asynchronous mode, strobe every byte of data. The maximum defined data transfer rate is 10MT/s. This corresponds to a bit width of 100 ns. The data path bits are the second fastest lines on the SCSI bus operating at 10MT/s maximum (5 MHz maximum for a 1-0-1-0 pattern). The other control lines are low speed lines and are level sensitive not edge sensitive. These lines typically only switch between bus states, and a substantial amount of time is provided for settling.

SCSI BUS STATES

The SCSI bus has eight different states which are:

- BUS FREE
- ARBITRATION
- SELECTION
- RESELECTION
- COMMAND
- DATA
- STATUS
- MESSAGE

The SCSI bus state is determined by the state of the SEL, BSY, I/O, MSG, and C/D control lines. Initiators are in control of the bus up to the command phase, and targets control the last three information transfer phases. For example when SEL and BSY are both false, the SCSI bus is in a bus free state.

SCSI OPTIONS: FAST AND WIDE

The FAST option allows for operation at 10MT/s (Mega Transfers per second) compared to the original 5MT/s specified in the original SCSI standard (now commonly referred to as SCSI-1). Single-ended drivers and receivers should be limited to cables less than 3 meters in length and be properly terminated. In contrast, the differential RS-485 transceivers can operate at 10MT/s over 25 meters of cable and due to the differential scheme, offer high noise rejection. The SCSI-2 (draft, 1993) introduced this option to SCSI and has gained wide acceptance.

The WIDE option (also introduced in the SCSI-2 specification) defines extra lines that double or quadruple the system throughput (MB/s). Adding a second byte of data can be accomplished in two different ways. First, one could select the P cable which, with 68 conductors can house both bytes of data and the nine control lines (for a total of 27 lines). The other option specifies two cables (A and B); the A for the first byte and the nine control lines, while the B cable carries the second byte plus an additional REQB and ACKB line (for a total of 29 lines). Since the second option requires two sets of connectors and cables, the P cable has become the more popular of the two, as it saves money and back panel space. The P cable (and Q for Byte 3 and 4) is included in the SCSI-3 Parallel Interface (known as SPI) draft standard, however A and B 50-pin cables are also still allowed. With two bytes of data being transferred, 20MB/s is obtainable. Four bytes achieves a 40MB/s maximum transfer rate. However, the four byte option is not very popular since it again requires two cables (P and Q).

THE SCSI TERMINATION

The differential SCSI bus requires line termination at both ends of the cable. Unlike the single-ended SCSI option, only one type of termination is defined. The line is terminated with a 3 resistor network commonly called a power termination. The three resistors are: 330Ω between the -Signal and the termination voltage (+5V), 150Ω between the signal pair (−Signal and +Signal), and 330Ω from +Signal to ground. The equivalent resistance of this network is 122Ω (150Ω // (330Ω + 330Ω)), and closely approximates the characteristic impedance (Z_O) of the defined cable. The termination network is shown in *Figure 3*.

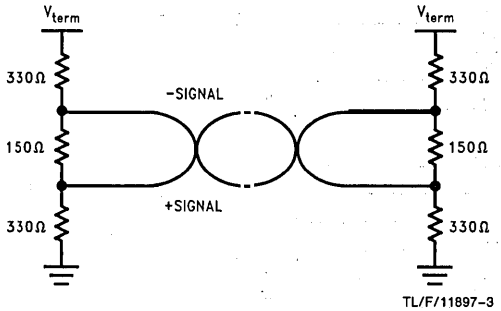


FIGURE 3. The SCSI Differential Termination

By using this termination reflections are minimized and a failsafe bias is provided. When all drivers are in TRI-STATE® (OFF), the resistors bias the line to approximately −1V differential. The SCSI standard defines this as a FALSE state or not-asserted. The minus sign comes from the fact that the +Signal is less in potential than the −Signal by one volt. It does not imply that the voltage is one volt below ground. A common problem that occurs when installing SCSI networks is employing greater than two termination networks. Devices connected in the middle of the bus should not include (enabled) termination networks. The termination networks should only be located at the extreme ends of the cable. Installing three or more terminations loads down the driver's output signal and reduces or eliminates the noise margin.

THE DS36BC956 HEX TRANSCEIVER

National's new hex transceiver was designed with SCSI in mind. However, the device is also ideal for IPI (Intelligent Peripheral Interface) and other high speed proprietary parallel buses. The choice of six transceivers was selected to offer a balance between integration, PCB footprint and power dissipation (junction temperature). Since the majority of on-chip power dissipation is a result of the external SCSI defined termination load, six transceivers were selected as the optimal configuration to limit the power dissipation per package. Three devices provide the 18 transceivers required for the standard 1 byte interface. Five devices implement a wide SCSI (2 Byte) interface. The device meets both RS-485 and SCSI standard specifications. The AC parameters on the device are fully characterized under both RS-485 standard loads and SCSI loads. This includes differential propagation delays, skew, TRI-STATE delays, and transition times. The functional diagram of the DS36BC956 is shown in *Figure 4*.

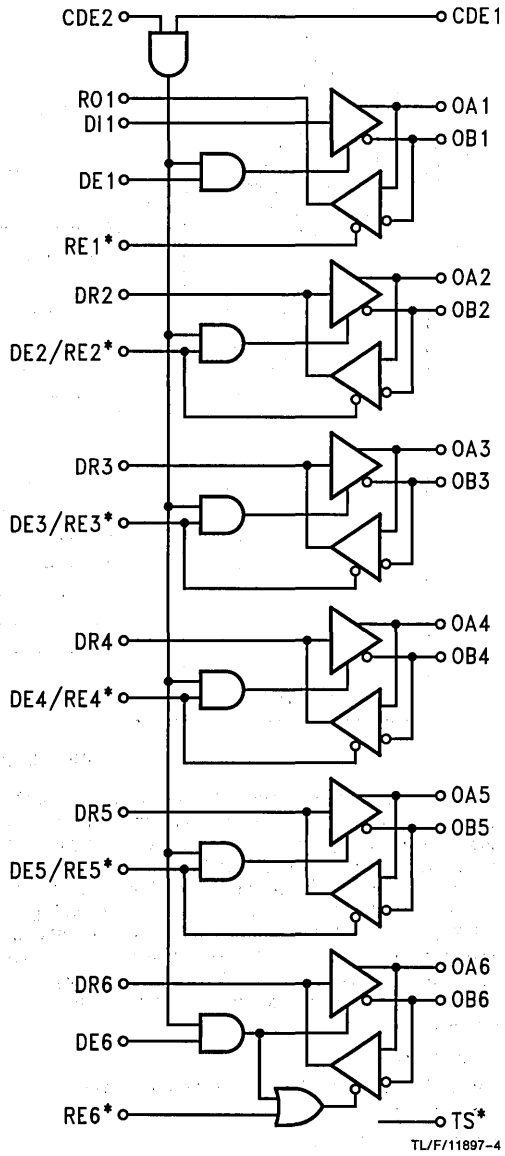


FIGURE 4. DS36BC956 Functional Diagram

SCSI CONTROLLER REQUIREMENTS AND THE DP8497 SDDC

Not all SCSI controllers support the differential mode. This is due to the fact that the external transceivers require direction control signals. For example the National DP8496 is a SCSI-2 Disk Data Controller (SDDC) which provides on-chip single-ended transceivers that are directly connected to the SCSI bus in single-ended applications. A related device, the DP8497 supports the differential SCSI option. This device provides the necessary output signals to control data flow direction through the external RS-485 transceivers. A unique feature of the DP8496/DP8497 SDDCs are that they are offered in the same footprint and package. The DP8497 direction control pins replace NC (no connect) pins on the

DP8496. This enables a user to upgrade an existing single-ended design to differential SCSI by simply swapping the controller and adding three DS36BC956s to the PCB. This provides an excellent upgrade option.

Figure 5 illustrates the interconnection between the DP8497 SCSI-2 Disk Data Controller (SDDC) and three DS36BC956 Hex Differential Bus Transceivers. As discussed in the companion Application Note (AN-905), the low speed SCSI control lines are spread out into each package to reduce and to balance on-chip power dissipation. Note, that in the connection diagram there are three (two minimum) control lines per DS36BC956. And a maximum of four high speed lines. Also, note that REQ and ACK are located in the same package. This is acceptable because REQ and ACK are not driven simultaneously by a SCSI device. REQ is driven by a Target, while ACK is driven by an Initiator. In a Target application (typically a Hard Disk Drive—HDD) the ATN and ACK lines are not driven, they are input signals only (received). These two lines should be located in separate packages for power balancing. RST is another line that is seldom switched. Locating each of these lines in separate packages helps lower the total device power dissipation (since these lines are rarely driven by a Target). Power balancing provides the designer a methodology to gain lower and equalized junction temperature for the transceivers, but at the expense of complexing the PCB layout.

Trade offs of power balancing include stub lengths, trace impedance, and any additional capacitive loading due to via structures. It is also possible to route the SCSI signals through the three DS36BC956s in the same order as the SCSI connector for the easiest PCB layout at the expense of power balancing. In either case the maximum junction temperature of the DS36BC956s will be less than +150°C.

The DP8497 does not require separate driver input (DI) and receiver output (RO) pins for the wire-or SCSI lines (BSY and RST). The DI and RO pins were tied together to form a bidirectional data line (DR), and the separate driver enable (DE) and receiver enable (RE*) pins were also tied together to implement a direction control line. Other SCSI controllers commonly require access to these lines independently, therefore the signals were pinned out separately. This provides the maximum amount of flexibility for the transceivers to interface to the widest number of SCSI controllers from a wide range of manufacturers.

Depending upon the SCSI controller used, an extra inversion might be required. This is the case of the DP8497 which supports active high outputs. By reversing the roles of the OA and OB bus pins on the DS36BC956, a logical inversion is achieved (Note, compare the termination connections illustrated in *Figures 5* and *6*).

The common driver enable (CDE1) on the DS36BC956s are ganged together and employ a pull up resistor to +5V. If a single-ended device is connected to the SCSI bus, the differential drivers will be disabled automatically. This occurs since the single-ended bus assigns a GND to the pin assigned to DIFF SENSE (Differential Sense) on the differential bus connector pinout. This assures that a differential device can not be enabled and damage a single-ended device that was inadvertently connected to the bus. The second common driver enable (CDE2) can be used by a local power up reset circuit if desired, otherwise, it should be tied high.

OTHER SCSI CONTROLLER CONNECTIONS

Figure 6 illustrates the interconnection between the NCR53C700 SCSI Controller and the three DS36BC956 Hex Differential Bus Transceivers as a second connection example.

Connecting the DS36BC956s to other controllers that support differential SCSI from other vendors is similar to the connection diagrams shown in *Figures 5* and *6*. However, due to the lack of a standard SCSI controller pinout, minor differences may exist between the control (direction) and data pins on the SCSI controller and the TTL/CMOS pins (DR, DI, RO, and enable) on the DS36BC956. But, since the pinout of the DS36BC956 was set with flexibility in mind, a wide variety of different vendor's SCSI controllers are supported. (For more information on the DS36BC956 pinout and enable pins see AN-905).

SUMMARY OF SCSI STANDARDS

This application note provides an introduction and brief overview of the differential option for the SCSI parallel interface. The reader is referenced to the standards listed below for complete, current SCSI specifications. Also, a number of SCSI handbooks are available that cover SCSI basics and protocol details written in plain English compared to the more encrypted standards.

Various manufactures reference different version of the SCSI standard. This creates some confusion to new users. The original version of SCSI released in 1986 is commonly referred to as SCSI or SCSI-1. The ANSI committee has created the second edition of SCSI known as SCSI-2, which is currently in industry ballot (1993). This is still a draft standard until balloting is complete. Approval should occur some time in 1993. Work has started on SCSI-3 also. This proposed standard was broken down into many smaller standards to speed up the ballot/approval process. The parallel interface standard is specified in the SPI document (SCSI Parallel Interface). SCSI-3 differs from SCSI-1 and -2 in the fact that it also specifies alternate physical layers. Currently a serial bus based on a proposed IEEE standard (P1394) is being standardized for small form factor drives and also a fiber physical layer. Table I describes some of the major differences in the physical layers in SCSI-1, 2, and 3 standard and draft standards.

TABLE I. SCSI Standard Comparison

Parameter	SCSI-1	SCSI-2	SCSI-3
Maximum Nodes	8	8	8, 16, and 32
Fast SCSI	NO	YES	YES
Wide SCSI	NO	YES	YES
Maximum Transfer Rate	5MT/s	10MT/s	10MT/s
MB/s-1 Byte	5	10	10
MB/s-2 Byte	X	20	20
MB/s-4 Byte	X	40	40
Document	X3.131 -1986	X3.131 -199x	SPI draft

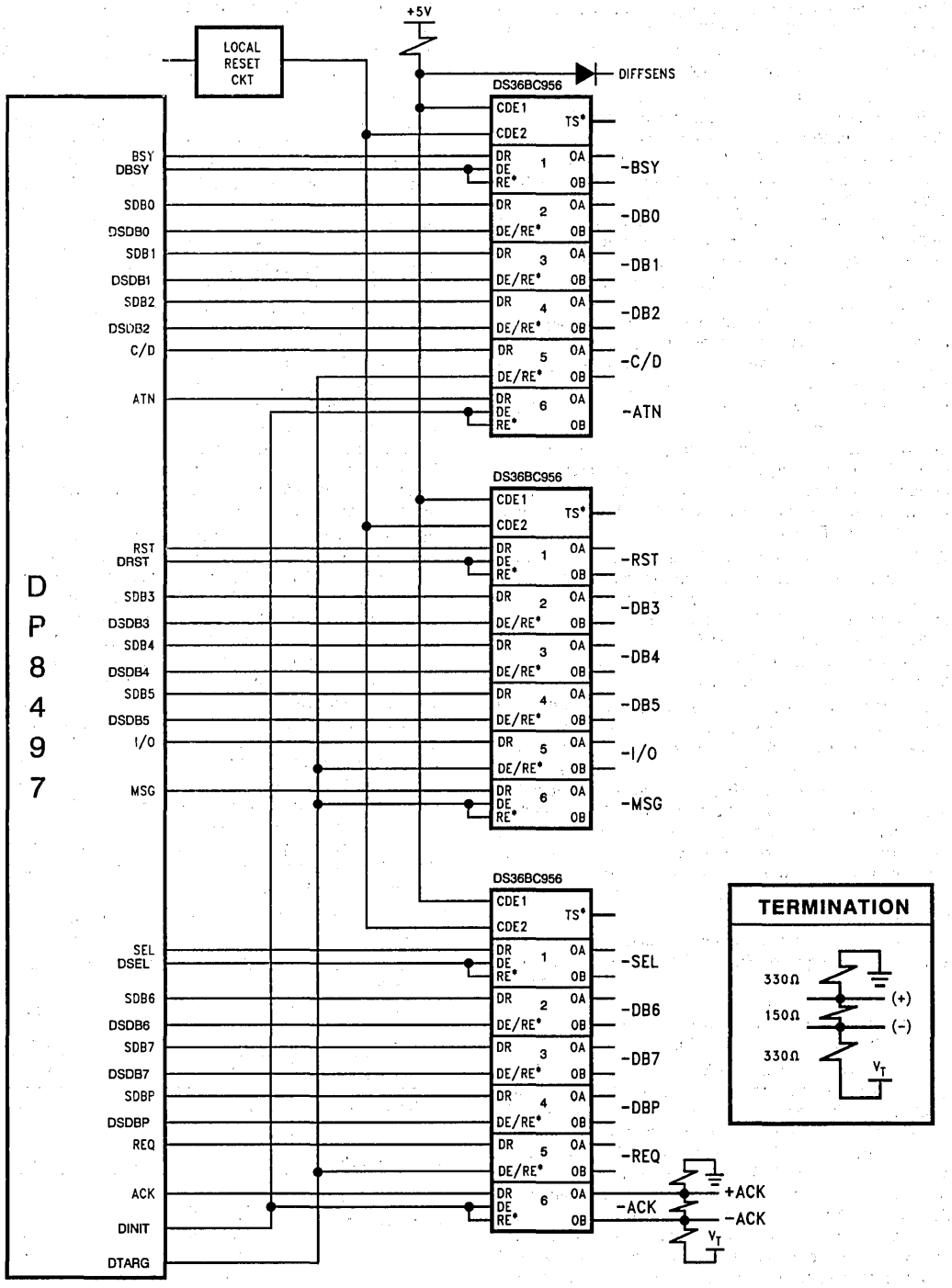
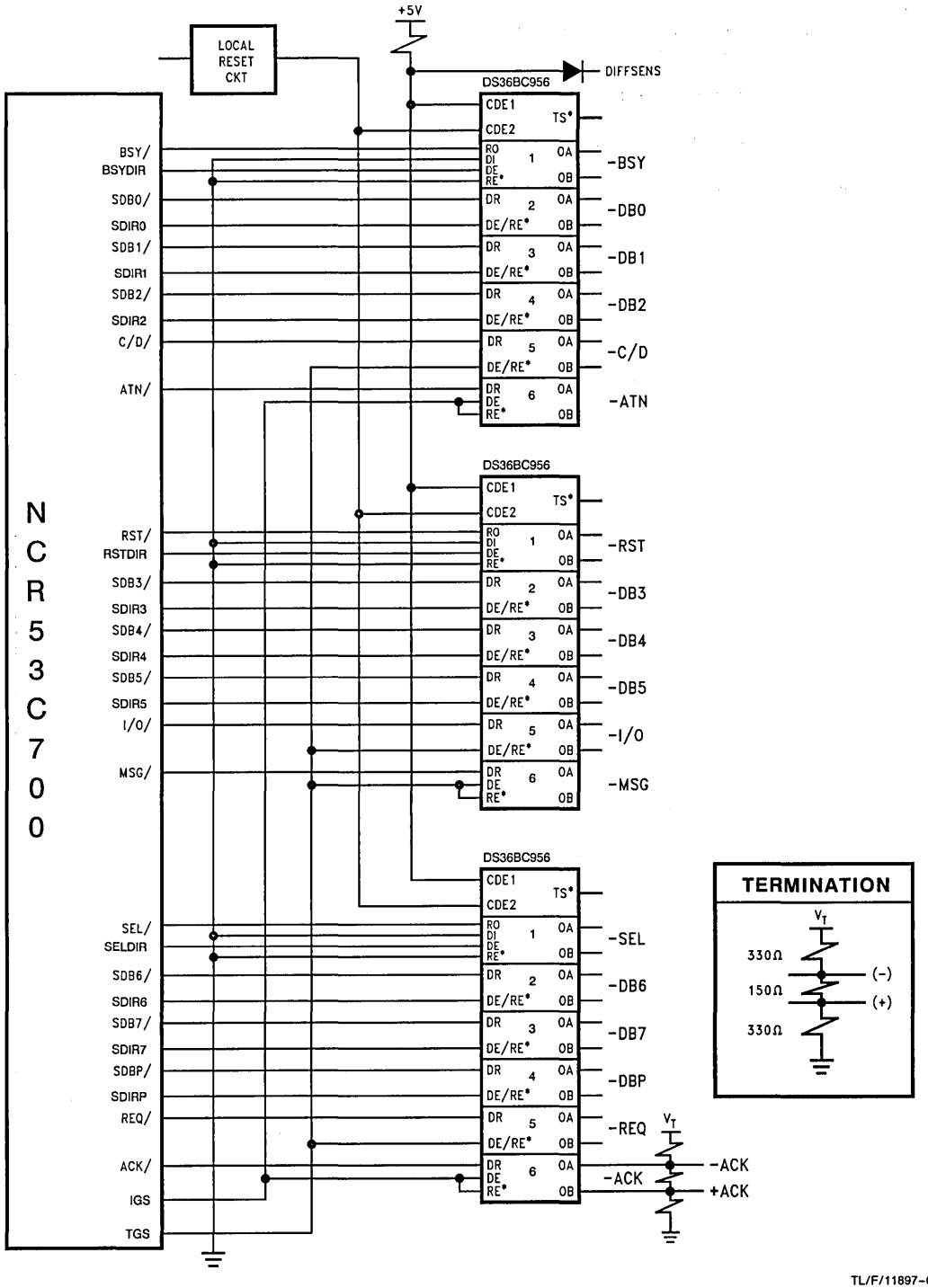


FIGURE 5. DP8497 Connection Diagram



TL/F/11897–6

FIGURE 6. NCR53C700 Connection Diagram

Note: *NCR53C700 open collector outputs require 680Ω pull up resistors (not shown)

REFERENCES/STANDARDS

Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems, EIA RS-485-1983, TIA/EIA

Small Computer System Interface (SCSI-1), X3.131-1986, ANSI

Small Computer System Interface (SCSI-2), X3.131-199x, ANSI

SCSI-3 Parallel Interface (SPI), X3T9.2/91-010, Draft Standard, ANSI

Understanding Power Requirements in RS-232 Applications

National Semiconductor
Application Note 914
Syed Huq

INTRODUCTION

As the popularity of asynchronous serial communication became widely accepted by the industry, the RS-232 standard gained very wide acceptance. The use of this standard is visible in almost all Industrial, Portable, Desktop, Data Acquistion and Test Measurement applications using a serial port for communication. Even though the standard specifies a maximum data rate for RS-232 of 20 kbps, some applications need for higher speed is overwhelming. More and more applications today require at least 120 kbps to support Laplink®, a popular communication software used by Laptop/Desktop computers for fast file transfer between two computers. RS-232 type Drivers and Receivers must also support this higher data rate to be Laplink compatible.

This application note covers the RS-232 circuit functions, an explanation of hardware handshaking, a step by step analysis of the hardware handshaking between a local and remote terminal, and power requirements/dissipation of the DS14C335.

RS-232 HANDSHAKING CIRCUITS

In a Terminal (DTE-Data Terminal Equipment) to Modem (DCE-Data Circuit Terminating Equipment) application, as shown in *Figure 1*, commonly only eight dedicated lines are required. Even though the standard defines a 25 pin connection, the de-facto 9 pin connector is very popular. These lines are DCD, RXD, TXD, DTR, DSR, RTS, CTS, RI and GND and are shown in *Figure 2*. Lets take a quick look at these dedicated lines along with their respective functions. Note that ON is defined as a positive voltage and OFF is a negative voltages on the cable.

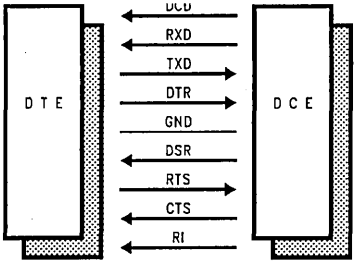


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FIGURE 2. Direction of Flow from DTE/DCE

DCD: DATA CARRIER DETECT (DCE TO DTE)

When this circuit is OFF locally, it indicates to the local terminal that the remote DTE has not switched its RTS circuit ON yet and the local terminal can gain control over the carrier line if needed. When this circuit is ON locally, it indicates to the local terminal that the remote modem has received a RTS ON condition from its terminal and the remote DTE is in control over the carrier line.

RXD: RECEIVE DATA (DCE TO DTE)

Receive data circuit from modem to DTE.

TXD: TRANSMIT DATA (DTE TO DCE)

Transmit data circuit from DTE to modem.

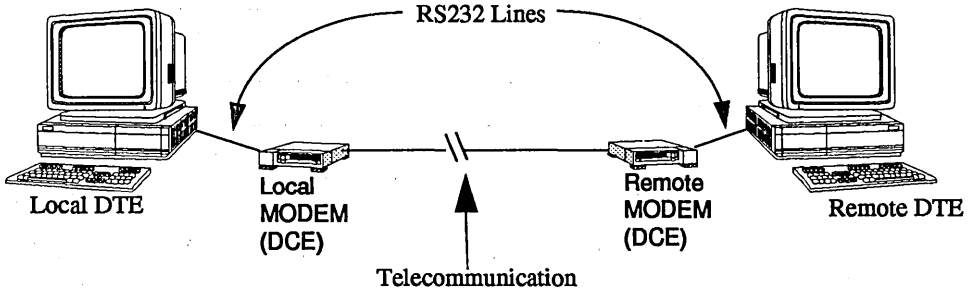

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FIGURE 1. DTE to DCE Interface

DTR: DATA TERMINAL READY (DTE TO DCE)

The DTR pin is generally ON when the terminal is ready to establish communication channel through its modem. By keeping the DTR circuit ON the DTE lets an *"auto answer"* modem accept the call unattended. The DTR circuit is OFF, only when the DTE does not want its modem to accept calls from remote locations. This is known as *local mode*.

DSR: DATA SET READY (DCE TO DTE)

Both modems switch their DSR circuit ON when a communication path has been established between the two sites (local and remote modem).

RTS: REQUEST TO SEND (DTE TO DCE)

When a terminal is ready to transmit data, it switches the RTS circuit ON, indicating to the local modem that it is ready to transmit data. This information also gets passed to the remote modem. The RTS line controls the direction of data transmission. During transmit mode, the line is ON and during receive mode it's OFF.

CTS: CLEAR TO SEND (DCE TO DTE)

When CTS swicthes ON, the local modem is ready to receive data from its DTE and the local modem has control over the telephone lines for data transmission.

RI: RING INDICATOR (DCE TO DTE)

When the modem receives a call, the RI circuit switches ON/OFF in sequence with the phone ringing informing the DTE that a call is coming in. This indicates that a remote modem is requesting a dial-up connection.

GND

Ground, signal common.

HARDWARE HANDSHAKE FLOW

A step by step analysis of handshaking illustrates how each circuit is used to establish communication between a local and a remote site. To keep the subject simple, assumption has been made that transmission is from Local to Remote only.

1. Local DTE switches DTR ON and local modem dials the phone number of the remote modem.
2. If DTR at remote location is ON, the remote modem's RI turns ON/OFF in sequence with the phone ringing, indicating a call coming in.
3. The remote modem returns an answer-back tone to the local modem. Upon detection of this tone, the local modem and the remote modem establishes the on-line connection. At this point both modems switch their DSR pins ON indicating that a connection has been established.
4. The local DTE switches RTS ON indicating that it is ready to send data. This signal gets passed on to the remote modems DCD circuit.
5. The local modem checks to make sure that local DCD is OFF, which indicates that the remote modem is not in control of the carrier line.
6. The local modem then switches CTS ON to the local DTE to inform that it can start sending data. Locally the DCD circuit stays OFF. On the remote modem DCD stays ON. RTS is held ON by the local DTE throughout the duration of the connection.
7. The local DTE sends data through TXD to modem for transmittal.
8. The remote modem receives the data and sends the data to its terminal via the RXD circuit.
9. When data transmittal is finished, local DTE drops RTS, which drops the DCD at remote modem and CTS at local modem. Transmission of data can be discontinued by hanging up the phone line, by the DTE dropping its DTR circuit, by disconnecting the modem cable from the DTE.
10. Now, either DTE is ready to start all over again and gain control of the telecommunication line.

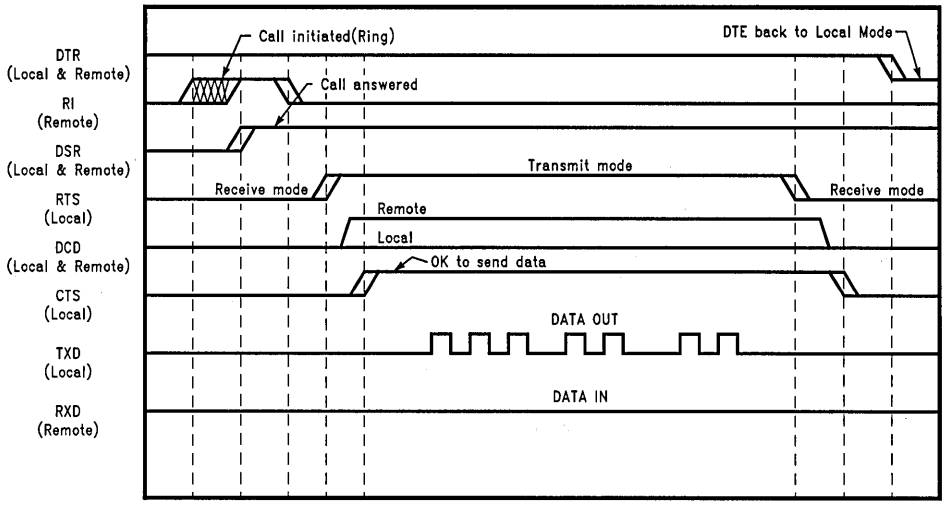

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FIGURE 3. Graphical Illustration of Hardware Handshaking

From the above explanations, in half-duplex communication, we can derive that in transmit mode, only one driver (TXD) is switching (up to 120 kbps) while the other drivers/receivers are at some known steady state (not switching). Similarly, on a receive mode, only one receiver (RXD) is switching while other lines maintain known steady state levels.

POWER CONSUMPTION

Based on the above observations, lets determine how I_{CC}, frequency, internal/external capacitance and load resistance play a role in power consumption for the DS14C335. Total power consumption is the static and the dynamic power combined. CMOS devices typically consume minimal power in a static condition. This can be calculated simply by multiplying I_{CC} with V_{CC}.

Under a loaded condition, the external loading of the driver directly effects the power dissipation of the device and application. The RS-232 driver is normally connected to a cable and a receiver at the far end. Since the transition time of the driver is set to be substantially longer than the cable delay, the cable load represents a lumped capacitive load and a series resistance. The series resistance on short cables (< 200 feet) can be neglected since it is very small compared to the receiver input resistance. This means the cable may be modeled as a lumped capacitive load equal to the capacitance per unit length multiplied by the length of the cable. 1000 pF is commonly used to represent a 20 foot cable, and 2500 pF is used as the maximum specified cable load. The receiver input resistance is specified to be between 3 kΩ and 7 kΩ, 5 kΩ is used as a typical, and 3 kΩ is the worst case from a power point of view. This equivalent load is illustrated in *Figure 4*.

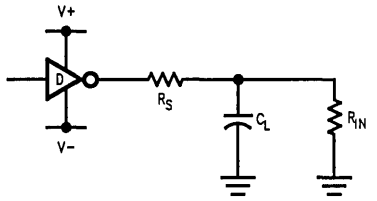

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FIGURE 4. Load Seen by the Driver

Where: R_S = Cable series resistance.

C_L = Cable load capacitance.

R_{IN} = Input resistance of the Receiver.

A channel that is in a steady state is loaded by the receivers input impedance since the cable capacitance has charged up. The output current of the driver is determined by the output voltage of the driver (V_{OH} or V_{OL}) divided by the input resistance of the receiver. For example, a 7V level, across the 3 kΩ load, requires 2.3 mA.

Dynamic power consumption has three major components. The switching current (spike current, also commonly called Conduction Overlap Current) during transitions, external load resistance and external load capacitance transient dissipation.

When the voltages to an NMOS/PMOS pair are in transition, both transistors turn on partially, creating a relatively low impedance path between the supply rails (V+ and V−). This is known as simultaneous conduction and is illustrated in *Figure 5*. As input frequency increases, the period decreases. At some point the output transistors fail to charge and discharge fully causing both upper and lower output transistor to stay on momentarily. This simultaneous conduction increases I_{CC} as the input signal's frequency is increased.

The charging and discharging of the large load capacitance C_L contributes to power consumption as well. The external load capacitance increases power in the same manner as the internal capacitance. A channel that is switching at speed is affected by all the components described previously. These new components contribute to the increased output current sourced or sunk by the driver to charge or discharge the capacitive load. This component of the load current will increase if the external capacitance is increased and also if the switching rate of the device is increased.

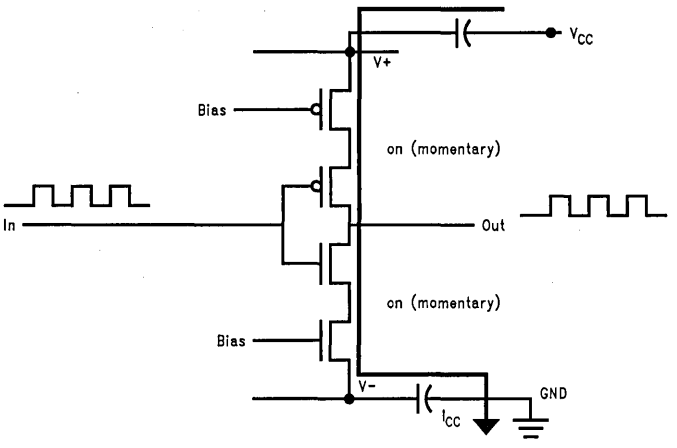

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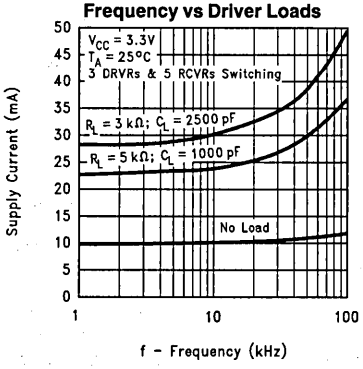
FIGURE 5. Simultaneous Conduction and I_{CC}

DS14C335 AND POWER CONSUMPTION

National's DS14C335 is a 3 X 5 Driver/Receiver combination providing a one-chip solution for a 9 pin RS-232 DTE application. *Graph 1* shows a worst case situation where all 3 drivers and 5 receivers are switching under different loading conditions. Under this worst case condition, at 10 kHz (20 kbps), supply current is 30 mA (2500 pF). Under a no load condition, supply current stays relatively flat. *Graph 2* shows a true RS-232 application where one driver (TXD) is switching while the other two are driver (DTR and RTS) remain High (loaded) as shown in *Figure 3*. At 10 kHz, supply current reads 26 mA (2500 pF), under this real world RS-232 application. Decreasing the capacitive load also decreases the supply current as shown in *Graph 2*. *Graph 3* illustrates one receiver (RXD) switching. Supply current is almost constant under this operating condition.

DS14C335 Supply Current vs Frequency vs Driver Loads



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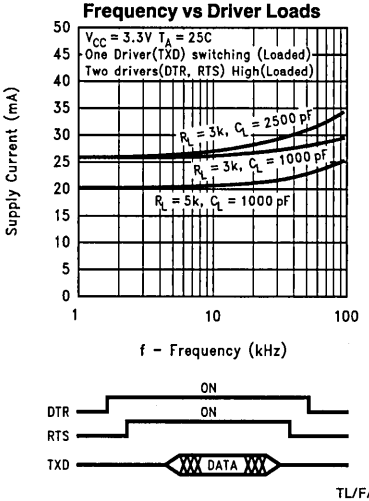
GRAPH 1. All Driver and Receiver Switching

DS14C335 Supply Current vs Frequency vs Driver Loads



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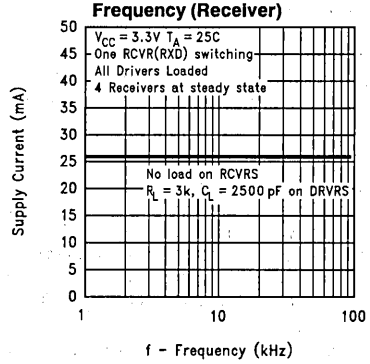
GRAPH 2. One Driver (TXD) Switching

DS14C335 Supply Current vs Frequency (Receiver)



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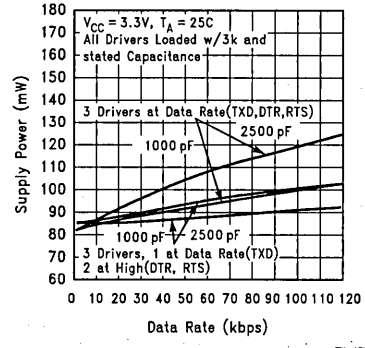
GRAPH 3. One Receiver (RXD) Switching

Looking at the Supply Power vs Data Rate (*Graph 4*) we can see that under multiple driver switching and at a maximum data rate of 120 kbps, the supply power is 120 mW (2500 pF load). With one driver switching and the other two driver output at High (RS-232 Application), the supply power at maximum data rate of 120 kbps drops to 103 mW (2500 pF load).

DS14C335 Supply Power vs Data Rate



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GRAPH 4. Supply Power vs Data Rate

The DS14C335 also offers a SHUTDOWN (SD) feature where the device can be de-activated by applying a logic High on the SD pin. This will lower the supply current to less than 1 μA (typical). In addition, in this mode one receiver (R5) remains active to monitor RI (Ring Indicator). This active receiver can sense incoming calls and inform the power management circuit to activate the device. SHUTDOWN mode saves battery life when the serial port is not used. In this mode, power dissipation is only 3.3 μW allowing battery charge to be used by other active circuitry.

OTHER INDUSTRY STANDARDS (RS-232)

RS-562 is another standard that is gaining popularity in the Industry. RS-562 is compatible to RS-232, however, there are some trade-offs. Table I illustrates a comparison and the major differences between the two standards.

TABLE I. Comparison and Major Differences between RS-232 and RS-562

Specifications	RS-232	RS-562
Mode of Operation	Single-ended	Single-ended
Receiver Input Resistance (Ω)	3 kΩ to 7 kΩ	3 kΩ to 7 kΩ
Receiver Sensitivity	±3V	±3V
Driver Output Current (Powered Off, ±2V)	±6.67 mA (300Ω)	±6.67 mA (300Ω)
Driver Output Short Circuit Current Limit	**≤100 mA**	**≤60 mA**
Number of Drivers and Receivers Allowed	1 Driver 1 Receiver	1 Driver 1 Receiver
Max Cable Length	~50' (2500 pF)	2500 pF (20 kbps) 1000 pF (64 kbps)
Max Data Rate	**20 kbps**	**64 kbps**
Driver Output	**±5V Min** **±15V Max**	**±3.7V Min** **±13.2V Max**
Driver Load	3 kΩ to 7 kΩ	3 kΩ to 7 kΩ
Driver Slew Rate	≤30 V/μs	≤30 V/μs

Even though RS-562 standard specifies data rates greater than RS-232, the DS14C335 (RS-232) far exceeds the 64 kbps of RS-562. The most significant difference between the two standards is the noise margin. As shown in *Figure 6*, RS-232 devices have a noise margin of 2V or greater. Typically for DS14C335, the noise margin is 4.5V (7.5V − 3V) whereas RS-562 has a noise margin as low as 700 mV (3.7V − 3V). A lower noise margin (RS-562) means limited rejection of external noise, crosstalk and ground potential differences which can all commonly occur in RS-232 typo communication.

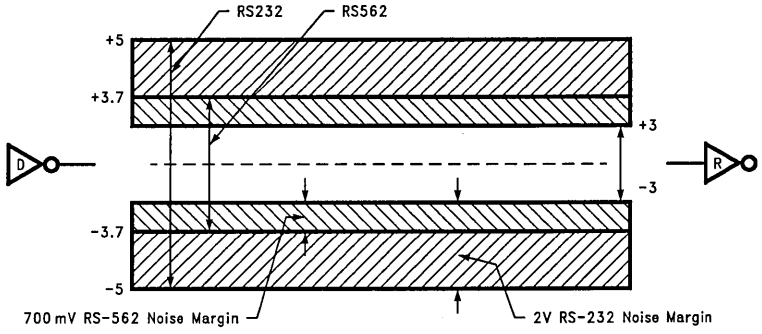

FIGURE 6. Noise Margin Comparison

CONCLUSION

Design Engineers are plagued with ground shift, noise problems and a noise margin of only 700 mV is not acceptable in many applications. RS-232 guarantees a 2V noise margin and Nationals DS14C335 is the preferred choice for applications requiring data rates pushing 120 kbps. Also, we have observed that in a half-duplex RS-232 DTE to DCE application, the supply current of the device is lower than simultaneous switching of all drivers and receivers as the application only requires one driver (TXD) or one receiver (RXD) switching at a time while the rest of the drivers/receivers maintain known steady state levels. Along with the power dissipation calculations, a discussion of the SHUTDOWN feature was also presented. This SHUTDOWN mode is highly desirable for any application that is battery powered, as it saves battery charge when the serial port is inactive.

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54C/74C Family Characteristics, Thomas P. Redfern, National Semiconductor Corp., *Application Note AN-90.*

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RS-232 Made Easy: Connecting Computers, Printers, Terminals and Modems, Martin D. Seyer.

Automotive Physical Layer SAE J1708 and the DS36277

National Semiconductor
Application Note 915
Michael Wilson
Todd Nelson

INTRODUCTION

Multiplex (MUX) wiring, or networking, has been introduced in automotive applications to address the increase in complexity and the number of onboard electronic devices in automobiles. Both standardized and proprietary solutions exist to address these issues. A standardized approach may be more desirable as cost and interoperability become important factors to consider for all original equipment manufacturers including automobile manufacturers.

The purpose of this application note is to give a general understanding of the J1708 recommended practice (SAE J1708) and the DS36277 transceiver which is optimized for use with SAE J1708. Additionally, this application note explains the significant differences between the DS36277 and a standard RS-485 transceiver, the DS75176B.

EXPLANATION OF TERMS

Dominant Mode—This is a mode of operation in which one logic state is dominant over any other state on the bus.

Listen Mode—This is a mode of operation in which a receiver is always active (assuming the device is powered) and its output is always in a known state.

DEFINITION OF TIA/EIA-485 AND SAE J1708

This section explains the definition of TIA/EIA-485 (RS-485) and SAE J1708. However, this section does not explain the electrical characteristic specifications of RS-485 or SAE J1708. The provisions for SAE J1708 will be discussed in the next section and for a brief definition of the RS-485 electrical specifications, refer to National application note AN-216.

First, RS-485 is an interface standard that specifies only electrical characteristics for balanced multipoint interface circuits. A complete interface standard will specify electrical, mechanical, and functional characteristics as does the popular interface standard TIA/EIA-232-E (see Table I). Second, SAE J1708 specifies only the functional characteristics for balanced interface circuits. RS-485 is referenced by SAE J1708 for its electrical specifications but with a few modifications. Thus, the end designer of a SAE J1708 application must specify their own mechanical connections.

TABLE I. Definition of RS-485 and SAE J1708

	Mechanical	Functional	Electrical
TIA/EIA-485			✓
SAE J1708		✓	REF. RS-485
TIA/EIA-232-E	✓	✓	✓

THE SAE RECOMMENDED PRACTICE J1708

The Society of Automotive Engineers (SAE) has defined this recommended practice for serial data communications between microcomputer systems in heavy duty vehicle applications. It is also well suited to passenger car applications (as shown in *Figure 1*) and many non-automotive uses. The bus is expected to be used for sharing data. An applications document, like SAE J1587 or SAE J1922, defines the actual data and/or functions to be transmitted. SAE J1708 only defines the hardware and basic software.

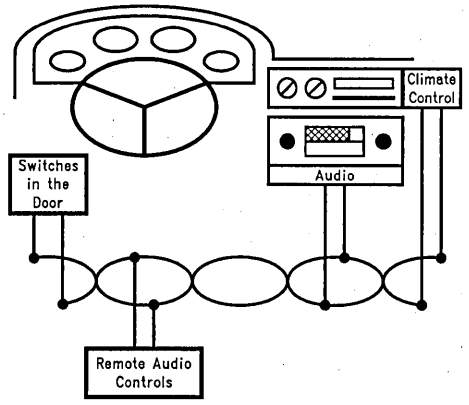

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FIGURE 1. Automobile Controls on a SAE J1708 Bus

The physical media is a two-wire bus using 18-gauge twisted pair with a minimum of 1 twist per inch. The maximum length is intended to be 40m. A maximum of 20 nodes is specified. Deviations from this must be carefully analyzed to determine impact on bus performance over the entire operating range.

Each node may access the bus randomly once the bus is idle for a predetermined access time. If two or more nodes attempt to access the bus at the same time, the contending nodes must arbitrate for the bus. Arbitration is determined by priority, which is set between 1 (top priority) and 8. An applications document shall reference SAE J1708 and define the priority associated with each message. Since there can be up to 20 nodes, it is possible for two contending nodes to have the same priority. When contention exists between two or more nodes, arbitration is determined by the bus access time. This is the time a node is required to wait before it can attempt to access the bus.

The protocol is consistent with standard UART operation. A message consists of a Message Identification character (MID), a data character(s) and a checksum character. The total message length should not exceed 21 characters. A character is defined as 10 bits: the first bit is always the start bit (logic level LOW), followed by eight bits of data and, the tenth bit is the stop bit (logic level HIGH) (see *Figure 2*).

The bit timing equates to a baud rate of 9600. The logic LOW and HIGH levels are encoded as "dominant" and "recessive" which will be described later. The hardware is defined by the RS-485 standard for its electrical characteristics, with some exceptions and modifications.

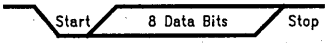

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FIGURE 2. Character Format

J1708 BUS LOADING

The recommended implementation for a SAE J1708 load is shown in *Figure 3*. The recommended implementation for a SAE J1708 system using a standard RS-485 transceiver, such as the DS75176B (see *Figure 4*), is shown in *Figure 7*. The circuitry between the bus and the transceiver differs from RS-485 and is intended to provide several features:

- R1 and R2 provide the bias for the "recessive" state.
- C1 and C2 combine to form a 6 MHz low pass filter, effective for reducing FM interference.
- R2, C1, R4 and C2 combine to form a 1.6 MHz low pass filter, effective for reducing AM interference.
- Since the bus is unterminated, at high frequencies R3 and R4 perform a pseudo-termination. This makes the implementation more flexible as no specific "termination nodes" are required at the ends of the bus.

The resistor and capacitor values are as follows and are shown in *Figure 3:*

Resistor 1 and 2 (R1 and R2)— 4.7 kΩ

Resistor 3 and 4 (R3 and R4)— 47Ω

Capacitor 1 and 2 (C1 and C2)— 2.2 nF

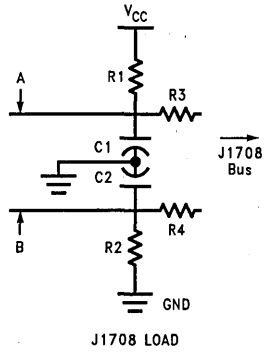

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FIGURE 3. Node Load Circuit

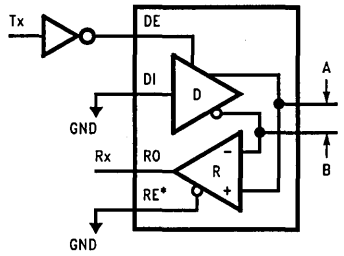

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FIGURE 4. The DS75176B in a SAE J1708 Application

DOMINANT MODE

The drivers used by SAE J1708 are used in a dominant mode application. The driver's input (DI) is tied LOW and the signal (Tx) to be transmitted is tied to the driver's enable. The enable (DE) is active HIGH for the DS75176B while the enable (DE*) for the DS36277 is active LOW. First, this information is very important because this tells us that the driver is only capable of driving LOW. Therefore, a logic level LOW is encoded as "dominant". When the driver is disabled, the bus is pulled high by external bias resistors R1 and R2 (as shown in *Figure 3*). Thus, a logic level HIGH is encoded as "recessive". Second, if the driver's enable is active LOW, then you will transmit positive logic. But, if the driver's enable is active HIGH you will transmit negative logic. SAE J1708 is only defined for positive logic. Therefore, to implement a SAE J1708 application using DS75176B, which has an active HIGH driver enable, an inverter is needed for the driver enable (see *Figures 4* and *6*). However, the active LOW driver enable pin on the DS36277 saves the user an externally needed inverter (see *Figure 5*).

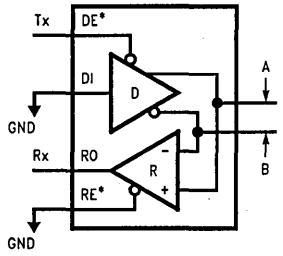

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FIGURE 5. The DS36277 in a SAE J1708 Application

In the case of a SAE J1708 application, a logic LOW can overwrite a logic HIGH. Thus, if contention exists between two drivers with transmitting signals (Tx) in opposite states, the driver driving the "dominant" state wins.

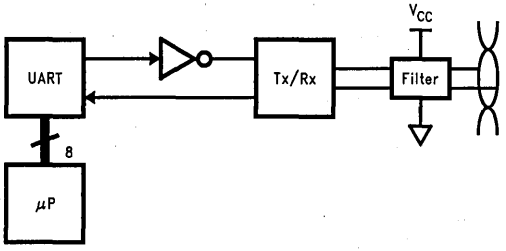

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FIGURE 6. Typical SAE J1708 System Block Diagram

SAE J1708 requires all receivers to listen to every message identification character transmitted to determine if contention exists. Unlike the driver, the receiver's enable (RE*) is always tied LOW (see *Figures 4* and *5*). This means the receiver is always in listen mode (see Explanation of Terms).

The external components shown in *Figure 3* provide the necessary bias for a logic High "recessive" state. SAE J1708 requires no additional external components other than the J1708 load. This means that no parallel termination can be used at the ends of the SAE J1708 bus. The required loading also provides failsafe protection.

FEATURES OF THE DS75176B

The DS75176B offers full compliance with the RS-485 standard and it is compatible with RS-422 and V.11. The device is available with industrial temperature range. Additionally, a thermal shutdown circuit protects the device against thermal overstress due to excessive power dissipation. Furthermore, the receiver has failsafe protection. However, the receiver's output is only guaranteed to be in a logic HIGH state for an open input line condition. The receiver also has ±200 mV threshold levels. The driver has an active HIGH enable while the receiver has an active LOW enable.

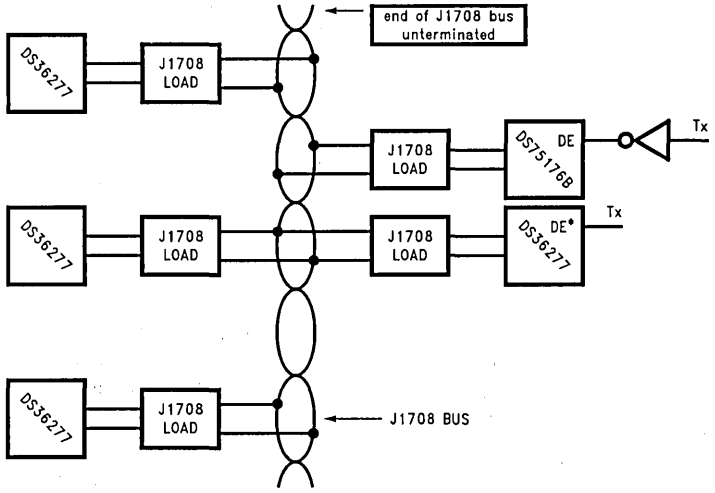

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FIGURE 7. SAE J1708 Typical Bus Configuration and Loading

FEATURES OF THE DS36277

The DS36277 is optimized for use with SAE J1708 electrical applications and the device is still compatible with RS-485, RS-422, and V.11 standards. Like the DS75176B, the device is available with industrial temperature range. Also the device includes thermal shutdown protection; plus the receiver has failsafe protection. Additionally, the receiver has full failsafe defenses that includes shorted and terminated line fault/conditions as well as open line conditions. The receiver's output is guaranteed to be in a logic HIGH state for all three line faults/conditions. The receiver's 0V to −500 mV threshold provides the protection from shorted line faults. Unlike the DS75176B, both the driver and the receiver have an active LOW enable.

The DS36277 also has a very rugged ESD structure that allows it to withstand electrostatic discharges (ESD) up to 7 kV (HBM). The device is also available in SOIC as well as DIP packages.

CONCLUSIONS

Selecting an established physical layer such as J1708 can eliminate many of the challenges of designing a serial communications system. The dominant mode operation allows for a non-destructive arbitration scheme.

J1708 is based on RS-485 electrical specifications and therefore benefits from the ruggedness, low cost and availability of compliant ICs already on the market.

The DS36277 transceiver has been optimized for J1708. It provides failsafe protection against bus faults and eliminates the need for an external inverter.

This application note provides a brief overview of the recommended practice and the interface standard. It is highly recommended to carefully review the complete documents. The documents can be obtained from:

SAE, 400 Commonwealth Dr.
Warrendale, PA 15096-0001

Global Engineering Documents
2805 McGraw Avenue
P.O. Box 19539
Irvine, CA 92174

REFERENCES

1. EIA RS-485, Standard for *Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems,* Electronic Industries Association Engineering Department. Washington D.C. 1983.

2. SAE J1708, *Serial Data Communications Between Microcomputer Systems In Heavy Duty Vehicle Applications.* Society of Automotive Engineers. 1990.

A Practical Guide To Cable Selection

National Semiconductor
Application Note 916
David Hess, Berk-Tek
John Goldie

Berk-Tek

1.0 INTRODUCTION

This application note provides an overview of the various considerations necessary for selecting suitable copper multiconductor or twisted pair cables for use with standard interface devices. It is important that a cable is well matched to the application; as well as, that the various cable selection trade-offs are considered for a cost effective system design. Cable types, constructions, and characteristics are covered and then related to the various device requirements.

2.0 TYPES OF CABLES

The two most basic cable categories are flat and round (see *Figures 1* and *2*). Both flat and round cables are available in multiconductor or twisted pair configurations and each with or without shielding. Shielding of various types is also available in both cases. Flat cables have carefully controlled conductor spacing making them suitable for mass termination. Round cables are suited for long cable runs or where flexibility and compactness are required.

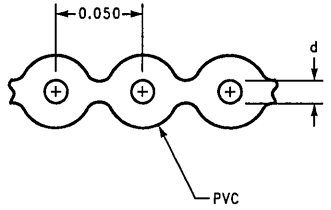

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FIGURE 1. Drawing of Flat Cable, Cross-Section

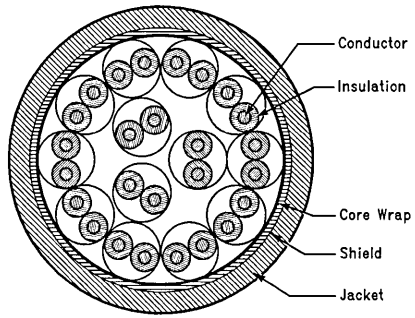

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FIGURE 2. Drawing of Round Cable, Cross-Section

Multiconductor cables are available for basic single-ended, i.e., unbalanced applications. Twisted pair cables are available for differential, i.e., balanced applications *(Figure 3)*. Note that a coaxial cable, a single insulated conductor with an overall shield; is, in this context, a "multiconductor" cable with only one conductor (the shield serving the dual purpose of signal return path and signal containment). In a similar sense, a two conductor multiconductor cable, since it is twisted, is equivalent to a single twisted pair cable.

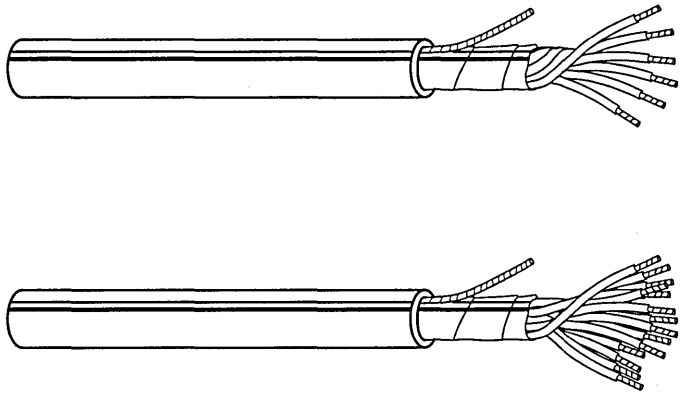

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FIGURE 3. Drawing Comparison of Multiconductor Cable and Twisted Pair Cable

It is common and preferable to use a twisted pair cable for single-ended applications. Some higher speed or longer distance single-ended applications provide a separate return conductor for each data and timing circuit, helping to reduce crosstalk. Note that single-ended applications cannot fully utilize the special capability of a twisted pair. Multiconductor cable should not be used for differential applications where twisted pairs are essential.

It is important to recognize that a twisted pair serves a fundamental electrical purpose. A twisted pair maintains, along its length, the balance necessary for and thus the common mode rejection sought in differential applications. The degree of physical symmetry achieved in constructing a twisted pair of insulated conductors determines how well it is balanced electrically. The double helix configuration of the pair produces symmetrical parasitics for each conductor. Symmetrical parasitics assure that induced noise signals are equal, or "common", to both conductors. This is the primary means of reducing crosstalk between various circuits within a cable. Flat cables constructed with twisted pairs are also available to achieve improved crosstalk characteristics.

Advantages of Flat Cables

By providing a means for mass termination, flat cables are relatively inexpensive to terminate. Connectors are available in configurations with insulation displacement contacts aligned for flat cable termination. The contacts are simultaneously pressed through the insulation onto all of the conductors of a flat cable. The cable conductor to connector contact alignment is critical. The two industry standard conductor centerline spacings are 0.050 and 0.025 inches. Controlling this parameter is a primary concern in producing flat cable and somewhat limits the range of cables' electrical characteristics available.

Advantages of Round Cables

Round cable flexibility is not limited to a single plane, as in the case of flat cable. For long cable runs, especially installed in conduit or raceway, flat cable is impractical. The flexibility of round cables is the result of having the individual elements, single conductors or twisted pairs, "cabled"; that is, they are "laid" at a pitch angle relative to the axis of the cable, forming a helix. The greater the pitch angle the greater the degree of flexibility. Color coding is usually provided as the means of identifying the individual conductors aiding the process of individually terminating each conductor. A round cable is simpler to manufacture with a shield. Capacitance can be reduced with thicker insulation walls, since there are no inherent conductor spacing requirements. Other than the case of simple, flat, strait, unshielded multiconductor cables; round cables have less cross-sectional area for a given number of conductors. More cross-sectional area is required for a shield or jacket on a flat cable.

3.0 CABLE CONSTRUCTION

Overall Construction

Conductors

Standard subminiature D-style connectors are designed to accept conductor sizes ranging typically from 22 AWG down to 26 AWG. Stranded tinned copper is normally used. Stranding provides a considerable improvement in flexibility and protection from conductor breaks due to repeated flexing, i.e., improved flex life. Tin coating on the strands improves environmental resistance by preventing corrosion of the conductor. The tin coating also makes the conductor more suitable for soldering. Standard connector pins are sized to accept the stranded conductor's increased diameter compared to solid conductor diameters.

Solid or non-tinned conductors are not recommended for use with some connectors. Some connector pins are crimped onto the end of the conductor where a small section of the insulation has been removed. This leaves a short section of exposed conductor susceptible to corrosion. Given the minimal space provided within the connector backshell, the added flexibility of stranded conductor makes the job of cramming the terminated conductors into the backshell a lot easier and more reliable. Conductor stranding also increases the overall cable flexibility, easing installa-

tion, and making the cable more likely to withstand the related abuses. If there will be even occasional flexing required in the cable application, stranded conductors are strongly recommended.

Nominal cost savings are gained by eliminating stranding or tin coating, but consideration should be given to the reduction in reliability. Stranding and tin coating have an effect on the signal loss of a transmission line, but these effects are insignificant below frequencies of about 10 MHz. These effects are essentially immeasurable at the frequencies associated with current TIA data communication standards; furthermore, other far more predominant limiting factors arise at data rates greater than 1 Mbps.

For typical serial data links, the de-facto standard gauge size is 24 AWG. TIA/EIA interface standards' recommendations are based on 24 AWG. This is the appropriate size to use with common subminiature D-style connectors. For smaller conductors to be properly captured in crimped contacts, special sized contacts may be required. Overall cable size and weight reduction can be achieved using 26 AWG or smaller conductors at the expense of increased fragility. Note, there are National Electrical Code restrictions that prevent conductors smaller than 24 AWG from being used in premises communication applications. Smaller conductors are recommended for restricted applications, such as equipment cables or where overall cable size must be limited; say for wide parallel data links used in short distances, up to 10 or 20 meters.

Larger conductors cannot provide very much improvement in performance. The overwhelming performance limiting factor in serial data communication systems is noise. An attempt to increase data rate and/or distance by increasing conductor size and thus reducing attenuation, is likely to be offset by crosstalk and other noise limitations. Consider, for instance, that EIA-422-A gives recommendations for transmission up to 1,200 meters (4000 feet) at data rates up to 90 kbps on 24 AWG cable. Typical data communication applications fall within the restrictions imposed by the voltage drop limitations of 24 AWG conductor. Special sized connector contacts may be required for larger conductors.

Copper conductors come in standard sizes according to the American Wire Gauge (AWG) system. A conductor gauge size is based on its cross-sectional area, and thus DC resistance. The overall diameter of the conductor depends on whether it is solid or stranded. Stranding is provided as a means of improving flexibility and flex-life, and the strand bundle is twisted similarly and for the same reasons mentioned above for the overall cable. The basic stranding configuration is 7 strands; 6 around 1. For a given gauge size; the more strands, the more flexible. Stranded conductors are considerably more expensive than solid conductors and the cost increases with greater numbers of finer strands. Stranded conductors utilize standard AWG size strands and numbers of strands. Their size is designated by the largest AWG size less than or equal to the sum cross-sectional area of the individual strands. Note, insulation displacement connector contacts are specifically designed for either solid or stranded conductors.

TABLE I. Conductors Solid Stranded Tinned and Bare from 30 AWG to 20 AWG vs Diameter DCR Weight, etc.

AWG	Stranding	Diameter		Weight		D. C. Resistance @20°C			
						Tin Coated		Bare or Silver Plated	
		inches	mm	lbs./kft.	kg/km	ohms/kft.	ohms/km	ohms/kft.	ohms/km
40	solid	0.0031	0.079	0.0291	0.0433	1158	3799	1080	3540
38	solid	0.0040	0.102	0.0484	0.0720	696	2283	648	2130
36	solid	0.0050	0.127	0.0757	0.113	445	1461	415	1360
34	solid	0.0063	0.160	0.120	0.179	281	920	261	857
32	solid	0.0080	0.203	0.194	0.289	174	571	162	532
32	7/40	0.010	0.254	0.21	0.31	176	577	164	539
30	solid	0.0100	0.254	0.30	0.45	113	371	104	340
30	7/38	0.012	0.305	0.35	0.52	106	348	92.6	303
28	solid	0.0126	0.320	0.48	0.72	70.8	232	65.3	214
28	7/36	0.015	0.381	0.55	0.82	67.5	221	59.3	194
26	solid	0.0159	0.404	0.77	1.14	44.5	146	41.0	135
26	7/34	0.019	0.483	0.87	1.29	42.5	139	37.3	122
24	solid	0.0201	0.511	1.22	1.82	27.2	89.2	25.7	84.2
24	7/32	0.024	0.610	1.38	2.05	25.7	84.2	23.1	75.9
22	solid	0.0253	0.643	1.94	2.89	16.7	54.8	16.2	53.2
22	7/30	0.031	0.787	2.19	3.26	16.6	54.4	14.8	48.6
20	solid	0.0320	0.813	3.10	4.61	10.5	34.4	10.1	33.2
20	7/28	0.038	0.965	3.49	5.19	10.3	33.8	9.33	30.6

The conductor, or individual strands in the case of stranded conductors, can be coated or "bare". Tin is the most common coating. Diffusion of the tin coating into the surface of the copper causes the DC resistance to be somewhat higher than bare conductors, but this is a concern mainly at frequencies above 10 MHz. Tinning, although providing for superior soldering, mainly provides substantial corrosion resistance over bare copper. The very short section of exposed conductor, even inside a connector body, between the end of insulation and, say a crimped on contact pin, can be a point of failure in a cable assembly. Other coatings, silver used to achieve improved soldering and corrosion resistance without the higher resistance penalty, and nickel used for high heat resistance with the higher resistance penalty; are used only in special applications.

INSULATIONS

In addition to providing basic insulating properties, the plastics used to coat the conductors have various signal altering characteristics. The two properties of insulating plastics that affect transmission are the dielectric constant and the dissipation factor. The dielectric constant is a function of the velocity at which energy travels through the dielectric (another name for insulation). The dissipation factor is a function of the rate at which energy is absorbed by the dielectric. Reducing either of these factors results in better signal transmission performance.

The plastic most commonly used for conductor insulation is polyvinylchloride (PVC). Its dielectric properties are good but, generally not good enough for any data communication application more demanding than basic low speed (<100 kbps), short distance (<50 m) links. PVC is normally used for power, control, instrumentation, and audio cables; applications that operate at relatively low frequencies. High performance serial data cables normally use a polyolefin insulation; either polyethylene or polypropylene, because their dielectric properties are far superior to PVC. Even though a data signal may be operating at a fairly low data rate the signal may be made up of pulses with fast rise times. The rise time of the pulse determines the frequency range covered by the signal. Typical data signals have power spectrums well into the 1 MHz to 10 MHz range. The polyolefins' dielectric constants and dissipation factors are low compared to PVC's and, unlike PVC, remain low well into the microwave region of the spectrum.

There is no great disadvantage to using polyolefins compared to PVC. The cost, at most, is only marginally higher. Some cable design precautions must be taken to meet flammability regulations. Polyolefins are far more flammable than PVC, but this can be overcome with a flame retardant outer cable jacket. As will be seen later, polyolefin insulation is essential for good performance with shielded cables.

The only exception to the choice of polyolefin insulation is the case of plenum cables used in premises wiring applications. Fluorinated ethylene/propylene copolymer (FEP), available in Teflon®, is substituted to achieve low smoke and flame producing characteristics to meet special National Electrical Code (NFPA) requirements. The dielectric properties of FEP are slightly superior to polyolefins.

SHIELDS

One problem that arises with long distances is a transmission line's susceptibility to interfering signals. Electro-magnetic interference (EMI) is basically unavoidable and a long transmission line is very susceptible. Long wires make good antennas.

Most of the serial interface standards do not require shielding, although provisions are made for shields within the standard connectors and recommendations for grounding. The standards basically avoid the subject of shielding as one which is outside of their scopes. On the other hand, the primary caution given in the distance and data rate guidelines is that outside interference is not taken into consideration. Shielding can greatly reduce or eliminate the possibility that the system will fail after you have followed all the other guidelines. Regardless of the effects interference may have directly on the serial interface, shielded cable may be required due to the overall system's susceptibility or emissions passed through the enclosure via an interface port. Shielding should be considered for all but very short low speed data circuits; above 10 meters or 100 kbps.

Shields are additional conductors added to cables and are designed to isolate electro-magnetic fields surrounding conductors or pairs within the shield from those outside of the shield. Shields may be placed over individual conductors, twisted pairs, or may be placed over the entire bundle of

TABLE II. Insulation Types vs Qualitative Performance Characteristics Electricals, etc.

Insulation Type	Specific Gravity	Dielectric Constant	Dissipation Factor	Volume Resistivity ohm-cm	Dielectric Strength Volts/Mil	Flammability	Temperature Range °C
PVC (Standard)	1.25–1.38	4–6	0.06–0.10	10^{11}	800–900	Good	−20 to 80
PVC (Premium)	1.38	3–5	0.080–0.085	10^{12}	800–900	Good	−55 to 105
Polyethylene	0.92	2.27	0.0002	$>10^{16}$	1200	Poor	−60 to 80
Polypropylene	0.90	2.24	0.0003	$>10^{16}$	850	Poor	−60 to 80
Cellular Polyethylene	0.50	1.5	0.0002	—	500	Poor	−60 to 80
Flame Retardant Polyethylene	1.30	2.5	0.0015	$>10^{16}$	1000	Fair	−60 to 80
FEP (or TFE)	2.15	2.1	0.0007	$>10^{18}$	1200	Excellent	−70 to 200 (or 260)
Cellular FEP	1.2	1.4	0.0007	—	500	Good	−70 to 200

cable elements or in both locations. Multiple shields within a cable may be electrically isolated from each other with additional insulating layers.

Typical cables use three basic kinds of shields; a tape shield, a braided or served wire shield, or a double shield consisting of a tape plus braided or served wires (see *Figures 4* and *5*). The tape shield always includes an uninsulated "drain" wire in contact with the aluminum, used to terminate the shield. The double shield includes a braided or served layer of wires in contact with the conductive side of a tape shield. Special shields are used for special applications such as corrugated rigid metal tapes used in telecommunications cables, solid tubes used on CATV cables, or woven or expanded metal screens used for flat cables.

The ideal shield is a seamless metallic tube as with the aluminum tubing utilized by the CATV industry on semi-rigid coaxial cable trunk lines; the emphasis is on "semi-rigid". To achieve flexibility a shield is made up of braided or served layers of fine wires or helical wrapped tapes.

Braided shields are made up of groups of fine; 34, 36, or 38 AWG, depending on the overall cable size; usually tinned,

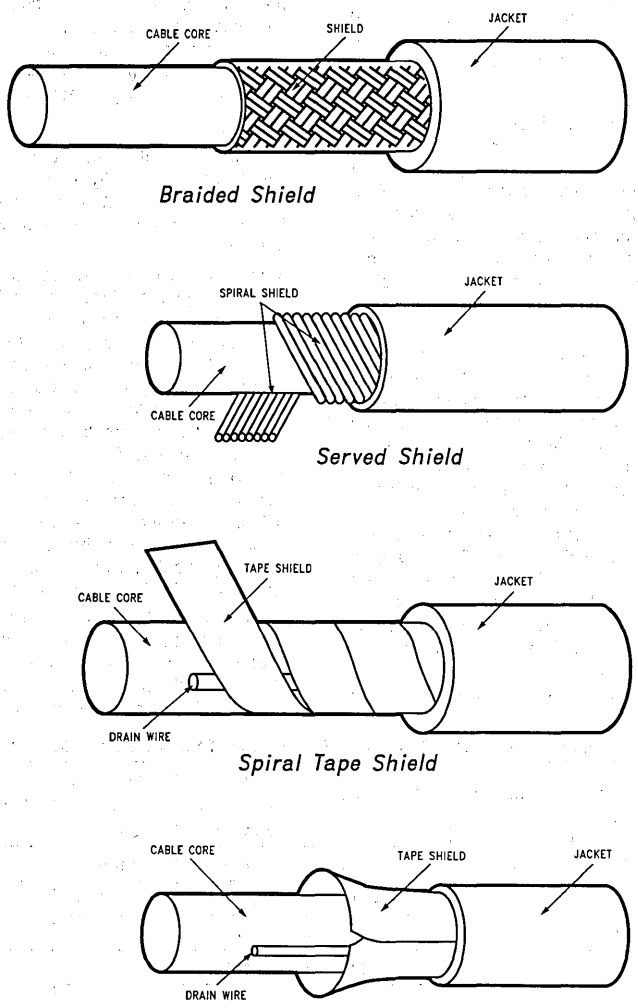

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FIGURE 4. Braid, Serve, Tape Shielding

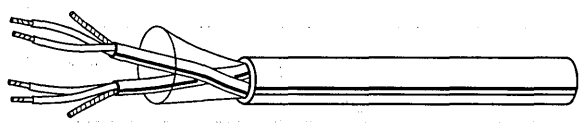

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FIGURE 5. Individual Pair Shields

copper strands; groups of these strands are woven Maypole fashion, in opposite directions, around the cable. Served shields consist of a single layer of strands laid in a single direction around the cable. Served shields are very flexible and are used in applications such as microphone or mouse cables. The small gaps in single layer served shields make them unsuitable for high frequencies (>10 MHz).

Tapes are a thin foil, usually aluminum, laminated to one or both sides of a plastic film, usually polyester or polypropylene. Tapes come in various thicknesses. The aluminum can be 1/3 to 2 mils thick. The plastic film, typically polyester or polypropylene, can be 1/5 to 2 mils thick. Thicknesses are selected by trading off flexibility with shielding effectiveness and signal attenuation in cases where the shield provides signal return path. Effective overlap of the tape is important for reliable performance. Uninsulated drain wires are normally of the same construction as the cable's conductors, but must be tinned to permit direct contact with the aluminum.

A simple model for shielding effectiveness is the shield's DC resistance. A shield is equally effective in both directions, in and out, and its effectiveness is proportional to its surface transfer impedance (which equals shield DCR at 0 Hz). Surface transfer impedance is the frequency dependent voltage/current ratio derived from a current driven on one side of the shield resulting in an induced voltage on the other side of the shield (see *Figure 6*). A detailed explanation of the surface transfer impedance model is outside of the scope of this application note.

Braids and serves have much lower resistances than tape shields. A typical double shield has about 1/5 the resistance of a tape shield, so it will be about 5 times more effective than a tape shield over the same distance. Another way of looking at it; a double shield extends the effectiveness of the tape shield to about 5 times the distance. A tape shield is effective for short cables. A double shield should be used on short distances in very noisy environments. A double shield should be used in any extended distance application, over 100 meters.

Braids are a trade-off between flexibility and ideal tubular conductors. The lower resistance of the braid results in good shielding effectiveness, but only up to a point. The small holes between the crossovers of the braid strands, become large at some frequency. Braids are specified by percent coverage as a means of determining the size of the holes. Closing up the holes, say by specifying 95% coverage, will be effective; two layers of braid can be specified for still greater effectiveness, but all at the expense of flexibility.

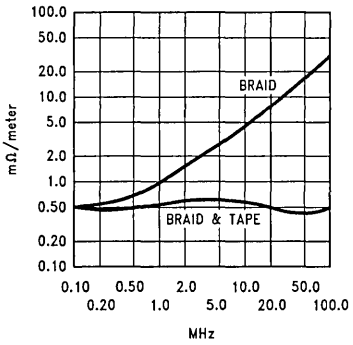

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FIGURE 6. Comparison Graph of Transfer Impedances, Tape Shield vs Braid Shield

A very effective means of closing the holes and lowering the resistance is to use the combination of tape and braid. The double shield achieves low resistance through the additional cross-sectional area of the braid. The tape is overlapped to provide as near to a true tubular performance as possible.

Jackets

The most common cable jacket material is PVC, which has good environmental resistance and can be compounded to have good cold temperature flexibility and meet a range of flammability requirements.

Flammability Requirements

Equipment cables are generally required to meet some level of vertical flames test. The National Electrical Code (NEC) sets standards for the flammability ratings of cables to be installed in buildings. Cables must pass the vertical cable tray flame test to be suitable for general purpose locations. This is the same test generally required for industrial environments. Two special locations are identified by the NEC; riser and plenum, each having respectively greater degrees of flammability requirements. Plenum cable can be used in plenums, risers or general purpose locations, riser cable can only be used in risers and general purpose locations, and general purpose cables are restricted from risers and plenums. In the case of plenum cables, Polyvinylidene Fluoride (PVDF) copolymer, available as Kynar®, jackets may be used for their low smoke and flame producing characteristics.

4.0 CABLE CHARACTERISTICS

Resistance

A DC resistance requirement is the best way to assure that the wire is indeed the size it should be. It also has a specific relationship to the TIA standards. Some requirements include maximum voltage drop for the signals. The cable termination load resistance and the total cable loop resistance determine the maximum permissible cable length for given length for a given voltage drop limitation.

Capacitance

A stated cable capacitance can be one of a number of possible capacitance values that can be measured on any given cable. Depending on how the cable is actually terminated to the generator, these various capacitance values may need to be considered. The different termination possibilities derive from, for instance, unbalanced vs balanced operation. Normally the mutual capacitance of a pair is provided in cable specifications. Mutual capacitance provides a measure of the capacitance that the generators will "see" when terminated to the cable. Another specification, sometimes given, is the capacitance of one wire to all the other wires and shield connected together.

Shielded cables must use insulation with good dielectric properties (i.e., low dielectric constant) to assure that cable capacitances are kept low when a shield is added to the cable. The proximity of two conductors in a cable and the dielectric constant of the insulation between the conductors determine the capacitance measured between the conductors. The addition of a shield around the two conductors introduces two very significant "parasitic" capacitances; those between each conductor and the shield. The conductor to shield capacitances combine with the conductor to conductor capacitance to significantly increase the overall capacitance of the pair.

Impedance, Velocity of Propagation, Attenuation, Rise Time Degradation

These four parameters have a less direct bearing on data communications applications. Sometimes they are specified, but after the basic cable dimensions are given, these parameters essentially depend on the Capacitance and DC Resistance.

The various lumped circuit element parameters; capacitance, inductance, resistance, and conductance of a transmission line, are all interrelated in a single parameter known as the characteristic impedance of a transmission line. This is the impedance that if used to terminate a transmission line, no signal will be reflected back to the source. If there is a mismatch, the bigger it is, the bigger the reflections will be. Impedance matched conditions are sought for all system designs, particularly at high data rates, because the reflections affect the performance of the generators and prevent some of the signal from ever reaching the receiver. The generator and cable termination load of EIA-422-A and EIA-485 are specified in such a way as to closely match the impedance of typical "low capacitance" cables having about 12 to 16 pF/ft mutual capacitance.

Velocity of propagation, the speed at which a signal (an electromagnetic wave) will travel along a cable (a transmission line) is dependent on the properties of the insulation. The dielectric constant of a plastic is actually the inverse of the square root of the velocity of propagation; the speed that electromagnetic radiation will travel through a dielectric compared to the speed of light in a vacuum. The velocity of propagation is normally expressed as a fraction of the speed of light. The actual velocity of propagation is complicated somewhat by the fact that the signal normally travels through a combination of air and plastic, but the result is to make it a little faster than the theoretic speed derived from the insulation dielectric constant alone. The velocity of propagation determines the impedance relative to the capacitance.

The impedance and resistance determine the attenuation vs frequency. This parameter is normally expressed in dB/1000 ft at a given frequency. This is a measure of the amount of signal loss that occurs from the cable. More signal is lost at higher frequencies than at low frequencies. Remember that the rise time of the pulse, not the data rate, determines the frequency range covered by the signal.

Since there is more attenuation at higher frequencies than at lower frequencies, signal pulses are dispersed as they travel down the cable. This property is measured as rise time degradation. Rise time degradation is roughly proportional to cable length. System designers are constantly balancing rise time effects. On one hand, fast rise times produce more crosstalk, that will, if great enough, result in errors. On the other hand, slow rise times that get further degraded will cause receiver errors.

5.0 CABLE APPLICATIONS

Lowering capacitance improves the performance of cables used for both unbalanced and balanced transmission.

Unbalanced transmission is limited by near-end-crosstalk. The unbalanced lines interfere with each other primarily through capacitive coupling between the lines. Lowering any capacitance parameter of a multi-conductor or twisted pair cable will result in proportionally lowering all of the various capacitances within the cable. In the case of unbalanced lines, coupling capacitance, and therefore crosstalk, is lowered proportionally. The mutual capacitance of a paired cable used for unbalanced transmission does not directly indicate the coupling capacitance between lines, but comparing the mutual capacitance of two cables is generally a good indication of their relative crosstalk performance.

Balanced transmission is primarily limited by rise time degradation. The primary cable capacitance of concern, in this case, is the shunt capacitance across the signal generator's two output terminals. Keeping everything else equal, lowering capacitance results in a decrease in attenuation vs frequency proportional to the square root of the capacitance reduction. In the general domain of data rate and distance for current applications, the resulting change in rise time degradation is nearly proportional to the square of the change in attenuation vs frequency. This gives a relation, similar to the unbalanced case, where a comparison of the mutual capacitance of two cables is generally a good indication of their respective proportional rise time performances.

TABLE III. Applications

Application	Multiconductor or Twisted Pair	Number of Conductors or Pairs	AWG Specified	Shielding Requirements	Transmission Characteristics Specified
EIA/TIA-232-E Section 2	Multiconductor	3 to 25	none specified	none required provisions included	2500 pF max total shunt capacitance
TIA/EIA-422-B	Twisted Pair	not specified	none specified guidelines use 24	none specified	none specified, 90–150Ω impedance recommended, guidelines use 100Ω impedance, 66% max. voltage drop
TIA/EIA-423-B	Multiconductor (Twisted Pair Better)	not specified	none specified guidelines use 24	none specified	none specified, guidelines use 100Ω impedance, 66% max. voltage drop
EIA-485	Twisted Pair	not specified	none specified	none specified	none specified, similar to TIA/EIA-422-B, guidelines use 120Ω impedance
EIA/TIA-562	Multiconductor	not specified	none specified	none specified	none specified
TIA/EIA-612 HSSI	Twisted Pair	not specified (companion spec TIA/EIA-613 requires 25)	none specified 28 recommended	shield required	110Ω impedance 4.5 dB max. total attenuation @50 MHz 79 ns max. total delay 2.0 ns/m max. total skew
X3T9.2 SCSI I	Multiconductor or Twisted Pair	50 conductor (flat) 25 pair (round)	28 AWG	required for external	100Ω impedance
X3T9.2 SCSI II	Twisted Pair	"A" Cable: 25 "B, P, Q" Cables: 34 "L" Cable: 55	28 or 30 AWG	required for external	90–132Ω nominal impedance (122Ω typical), 0.095 dB/m max. attenuation @5 MHz 0.20 ns/m max. skew
X3T9.2 SCSI III	Twisted Pair	"P or Q" Cables: 34	30 minimum	required for external	122 (84)Ω nom. impedance differential (single-ended) 0.095 dB/m max. attenuation @5 MHz 5.4 ns/m max. delay 0.15 ns/m max. skew

TABLE III. Applications (Continued)

Application	Multiconductor or Twisted Pair	Number of Conductors of Pairs	AWG Specified	Shielding Requirements	Transmission Characteristics Specified
X3T9.3 IPI (ISO 9318)	Multiconductor flat or Twisted Pair round	50 conductor (flat) 25 pair (round)	26 or 28 AWG	required for round	120Ω impedance 0.095 dB/m max. attenuation @5 MHz 5.4 ns/m max. delay 0.49 ns/m max. skew
X3T9.3 HIPPI	Twisted Pair	25	28 AWG	two shields required	108Ω impedance 0.28 dB/m max. attenuation @50 MHz 0.13 ns/m max. skew

6.0 SUMMARY

The range of cable types and basic options available for data communications applications is limited, making the basic cable design selection reasonably easy. The scope of the basic selection criteria is covered by the choices, flat or round, multiconductor or twisted pairs, and shielded or non-shielded. Basic attributes of the application; distance, environment, and flexibility requirements determine the basic cable type selected. Cable construction details, conductor size, stranding and coating, insulation type, shield options, and jacket types are determined by more specific application considerations; connector type, signal speeds, emissions and susceptibility, work and abuse, flammability, life expectancy and cost. Every cable has inherent electrical characteristics, which can be expressed in several ways, but are interrelated and dependent upon a few simple parameters. A cable's electrical characteristics determine its suitability for use with particular interface components.

Author Biography:

David Hess, V.P. Technology, Berk-Tek, Inc., 132 White Oak Road, New Holland, Pennsylvania 17757, has worked for 17 years in product engineering and product development in the fields of copper and optical fiber data communication cables, participates in various data communications standards committees in TIA/EIA and ANSI X3T9, holds a B.S. degree in Mathematics from Pennsylvania State University and is a member of IEEE.

Popular Connector Pin Assignments for Data Communication

National Semiconductor
Application Note 917
John Goldie
Syed Huq

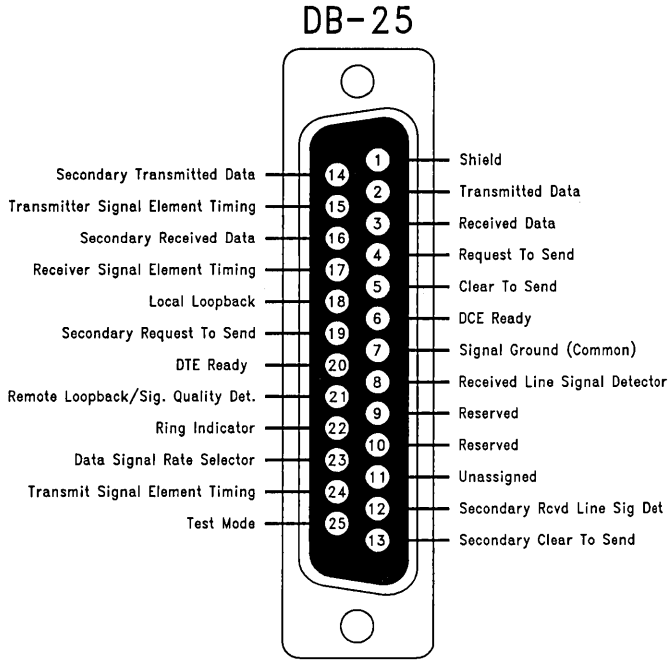
INTRODUCTION

This application note provides a graphical reference to popular connector pin assignments (pin outs) that are commonly used in telecom and computing applications.

In the field of data communication, the cable and connector play a critical part in the system's performance along with the line driver and receiver integrated circuits. Together the components (PCBs, ICs, cables, and connectors) form a channel, which all information must pass through. This channel forms a true chain, and a fault in any link may break the chain.

As stated in the introduction, this application note focuses on the connectors, and more specifically the pin assignments of the connectors. When equipment is built by a manufacturer and is intended to interwork with equipment from different manufacturers the use of an industry standard is critical. To properly inter-operate, the two pieces of equipment must support the same protocol (functional specifications), electrical levels, mechanical dimensions of the connector, and most importantly the connector's pin assignment. Since industry standards, TIA/EIA (Telecommunications Industry Association/Electronic Industries Association) for example, commonly specify or reference all three areas: Functional, Electrical, and Mechanical specifications, the chance of success is greatly increased when hooking up the two pieces of equipment.

A substantial amount of standardization work has been done in the telecommunications and computing area for interface standards. In addition to the connector pin outs, this application note also provides a short description of the standard or historical perspective. The reader is referenced to the actual standards from complete information on the standard.



TL/F/11940–1

FIGURE 1. RS-232 DB-25

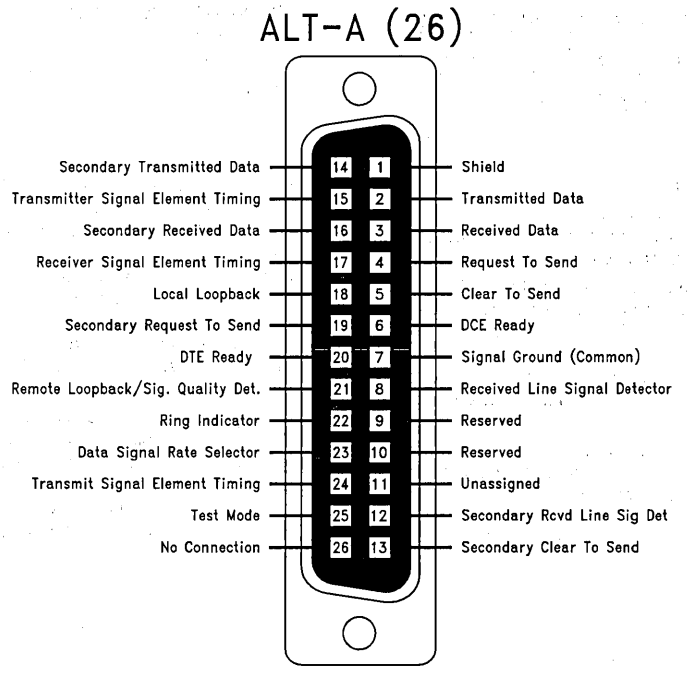


FIGURE 2. RS-232 ALT-A

RS-232

RS-232 is one of the most popular interface standards in the world. Originally intended for DTE/DCE interfacing, this standard has been used in a wide range of applications including telecom, computing, test and measurement, and industrial control applications. Now in its fifth revision (E), RS-232 is still very popular, and new devices (line drivers and receivers) are being developed to support the standard. The correct name of the standard is EIA/TIA-232-E which has replaced the more common RS-232 nomenclature. This standard specifies two connectors, the standard DB-25, also a new smaller alternate connector with 26 pins. The original version of RS-232 dates back to the early 1960s and is known as a complete standard as it specifies all functional, electrical, and mechanical specifications. There is also a very popular 9 pin defacto version of this standard commonly employed on personal computers that was developed by IBM®. The two full (25 line) connector pin outs are shown on *Figures 1* and *2*. See *Figure 7* for an illustration of the defacto 9 pin implementation, now standardized as EIA/TAI-574.

RS-449

RS-449 was intended to replace RS-232 at one time. It also specifies a DTE/DCE interface, but references the RS-422-A and RS-423-A standards for electrical specifications. This standard specified a DB-37 pin connector along with an additional DB-9 pin connector when additional lines were required. The 37 pin connector proved too large for many applications and limited the acceptance of this interface. RS-449 is mainly found in high-end telecom applications but rarely elsewhere. It has been replaced with a new standard that specifies the common DB-25 connector (EIA/TIA-530-A). The pin out of the DB-37 pin connector is shown in *Figure 3.*

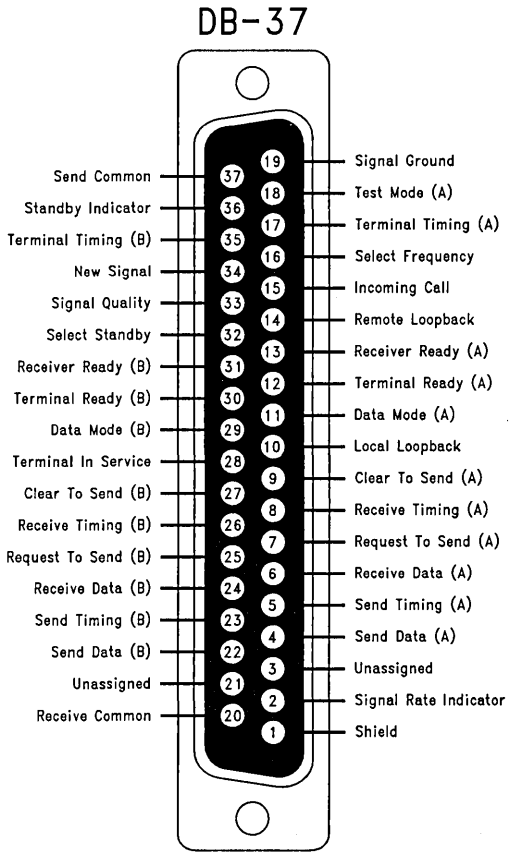


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FIGURE 3. RS-449 DB-37

EIA-530 AND EIA/TIA-530-A

EIA-530 is an extension of RS-449 but is based on the DB-25 connector. This standard specifies both functional and mechanical specifications, and references RS-422-A and RS-423-A standards for electrical specifications. This connector is the same one commonly used in EIA/TIA-232-E (RS-232) applications. This standard has been revised (denoted by the letter suffix — "A"), which altered the pin assignments slightly from EIA-530. Both pin assignments are shown in *Figures 4* and *5*.

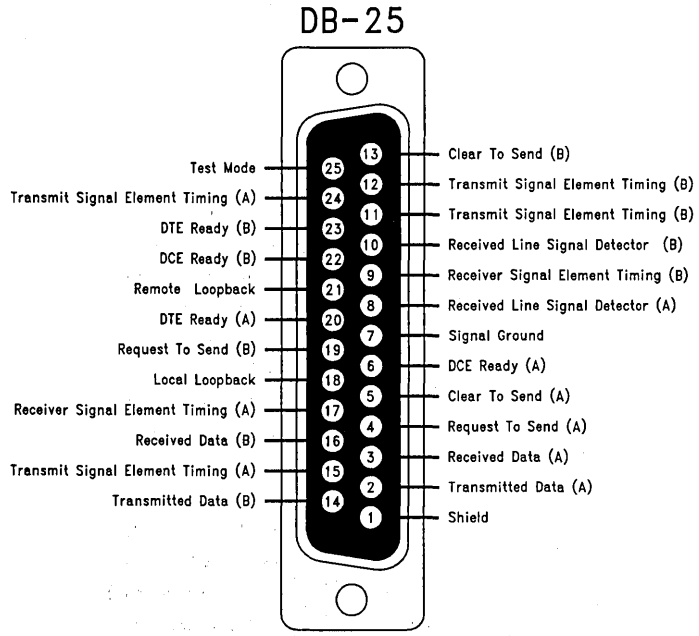

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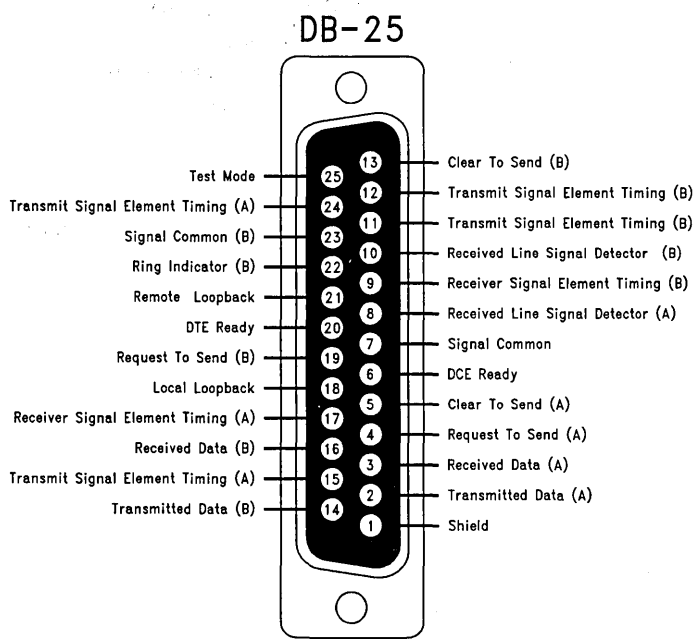
FIGURE 4. EIA-530 DB-25

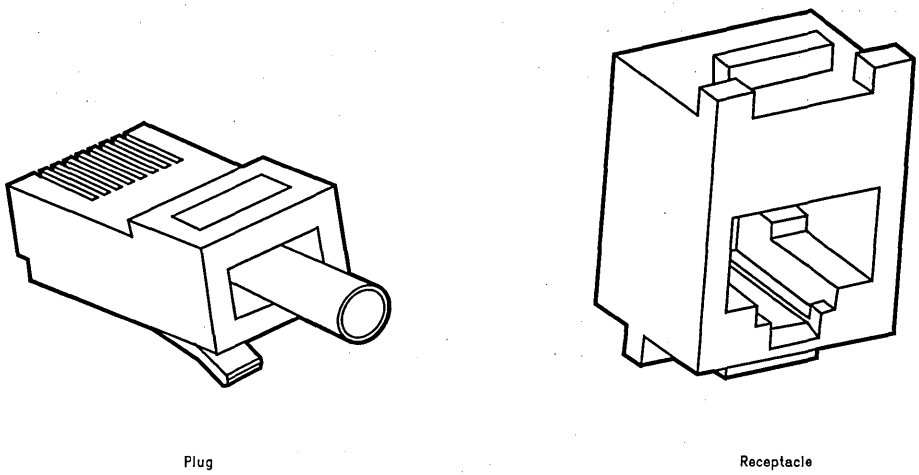


TL/F/11940–5

FIGURE 5. EIA/TIA-530-A DB-25

EIA/TIA-561

EIA/TIA-561 is a new standard released in 1990 and specifies a small 8 position interface for non-synchronous interface between DTEs and DCEs. The uniqueness of this standard is the fact that it does not specify a DB style connector, but rather a modular receptacle and plug type connector. This standard references the companion standard EIA/TIA-562 for electrical levels (similar to RS-232 but lower power and faster). The plug and jack are shown in *Figure 6.*



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1. Ring Indicator
2. Received Line Signal Detector
3. DTE Ready
4. Signal Common
5. Received Data
6. Transmitted Data
7. Clear to Send
8. Request to Send/Ready for Receiving

FIGURE 6. EIA/TIA-561 MJ-8

EIA/TIA-574

EIA/TIA-574 was developed due to confusion arising between the official RS-232 interface and the exceedingly popular defacto 9-pin version developed by IBM. This standard specifies the DB-9 interface, however, it recommends the use of the RS-562 standard instead of RS-232 electrical levels. It is noted that EIA/TIA-562 can inter-operate with RS-232 drivers and receivers in many applications. This standard supplies the minimum number of lines for non-synchronous serial data interchange between DTEs and DCEs. The connector pin out is shown in *Figure 7.*

V.35

Recommendations V.35 was developed by the CCITT (International Telegraph and Telephone Consultative Committee) as a high speed modem standard that also specified the DTE/DCE interface. This standard used RS-232 type line drivers and receivers for control circuits, and its own unique differential drivers and receivers for high speed data and timing lines. This recommendation specifies a unique connector and is shown in *Figure 8.* It should also be noted that the CCITT has been replaced with the ITU (International Telecommunications Union) and new standards will adopt the ITU prefix instead of CCITT.

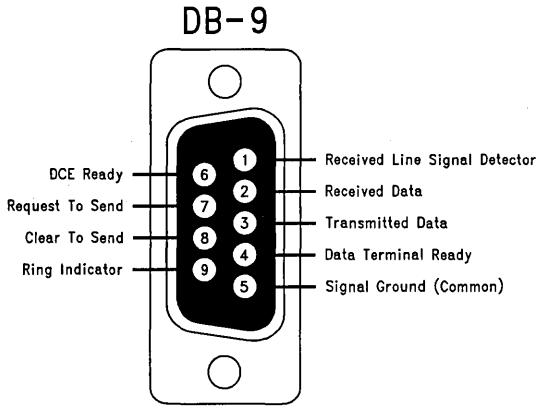

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FIGURE 7. EIA/TIA-574 DB-9

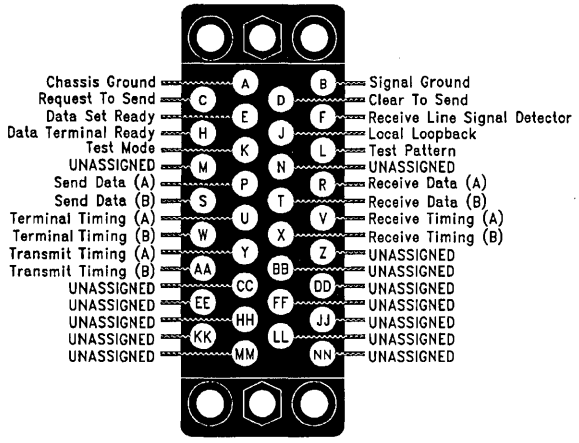

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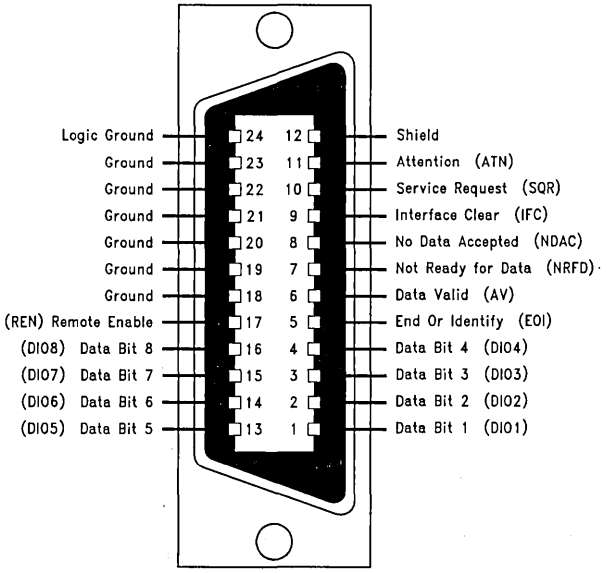
FIGURE 8. CCITT V.35

IEEE-488

The IEEE (Institute of Electrical and Electronic Engineers) also standardizes many interfaces in the area of computing and instrumentation. IEEE-488 is a complete standard specifying all functional, electrical, and mechanical specifications for a 16 line parallel bus for instrumentation. This interface is commonly found on test, and measurement equipment that feature computerized programming and control. This standard is also known under the acronym as GPIB (General Purpose Interface Bus). The pin out of the standardized connector is shown in *Figure 9*.

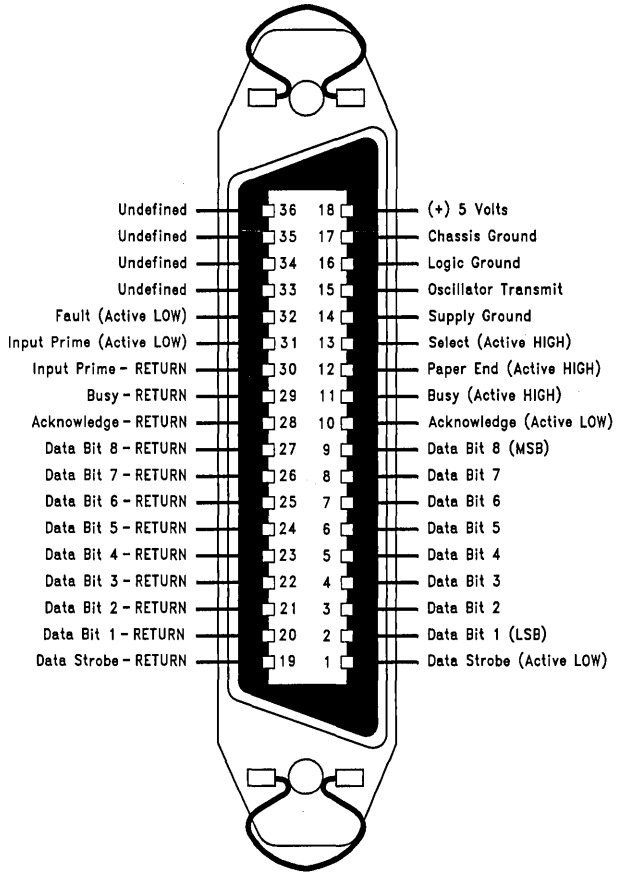


TL/F/11940–9

FIGURE 9. IEEE-488

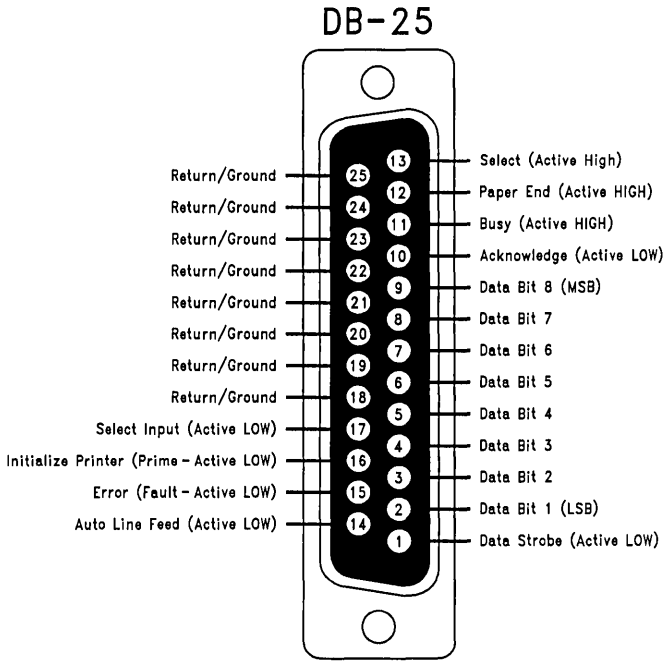
CENTRONICS PORT AND IBM PC PARALLEL PORT

These two defacto standards both specify parallel interface that are commonly used in computing applications (computer to peripheral-printer). Both are defacto standards, and support similar functions but different pin outs and mechanical specifications. There is active work by the IEEE to standardize this interface (Computer to peripheral-parallel port). The two connectors are shown in *Figures 10* and *11.*



TL/F/11940–10

FIGURE 10. Centronics Port



TL/F/11940–11

FIGURE 11. IBM PC Parallel Port

SUMMARY

By selecting an industry standard, the problem of getting signals from one board or box to another is greatly reduced. This is especially true when inter-operation between systems built by different manufacturers is required (open system).

Interface standards from the TIA/EIA and other standards groups greatly resolve this interfacing problem. This application note provides insight into those standards by providing a graphical representation of the connectors referenced in the standards. As always, whenever designing a system to an industry standard, a thorough review of the most recent revision of the standard is highly recommended.

REFERENCE

Most standards are available from:

Global Engineering Documents
Irvine, CA, USA
714-261-1455 or 800-854-7179

Various connector, cable and data communication products are available from:

South Hills Datacom
Pittsburgh, PA, USA
Toll-Free: 800-245-6215
Local: 412-921-9000
FAX: 412-921-2254

Section 9

Military Interface

Section 9 Contents

National Semiconductor

Line Drivers and Receivers
Military Products—Selection Guide

Device No.	Pin Count	Description	Process Flows	Desc SMD/ Slash Sheet*	Package Types
TIA/EIA-232					
DS14C232	16	Dual Line Driver and Receiver	883		CDIP, LCC
DS9616HM	14	Triple Line Driver	883		CDIP, LCC
DS9627M	16	Dual Line Driver	883	5692-8978701MxA	CDIP,LCC
TIA/EIA-422/423					
DS1691A		Single Line Driver	883		CDIP
DS26C31M	16	Quad Line Driver	883, MLS	5962-9163901MxA	CDIP, LCC, FP
DS26C32AM	16	Quad Line Receiver	883, MLS	5962-9164001MxA	CDIP, LCC, FP
DS26F31M	16	Quad Line Driver	883, MLS	5962-7802302MxA	CDIP, LCC, FP
DS26F32M	16	Quad Line Receiver	883, MLS	5962-7802005MxA	CDIP, LCC, FP
DS26LS31M	16	Quad Line Driver	883, MLS	5962-7802301MxA	CDIP, LCC, FP
DS26LS32M	16	Quad Line Receiver	883, MLS		CDIP, LCC, FP
DS26LS33M	16	Quad Line Receiver	883, MLS		CDIP, LCC, FP
DS78C20	14	Dual Line Receiver	883		CDIP
DS78C120	16	Dual Line Receiver	883, MLS		CDIP, FP
DS78LS120	16	Dual Line Receiver	883, MLS		CDIP, FP
DS9636AM	8	Dual Line Driver	883	5962-8752301xA	CDIP
DS9637AM	8	Dual Line Receiver	883	5962-8752401xA	CDIP
DS9638M	8	Dual Line Driver	883, MLS	5962-8754601xA	CDIP
TIA/EIA-485					
DS16F95	8	Single Transceiver	883, MLS	5962-8961501xA	CDIP, LCC, FP
DS96F172M	16	Quad Line Driver	MIL	5962-9076501MxA	CDIP, LCC, FP
DS96F173M	16	Quad Line Receiver	883	5962-9076602MxA	CDIP, LCC, FP
DS96F174M	16	Quad Line Driver	883, MLS	5962-907502MxA	CDIP, LCC, FP
DS96F175M	16	Quad Line Receiver	883, MLS	5962-9076601MxA	CDIP, LCC, FP
GENERAL PURPOSE					
DS1603	14	Dual TRI-STATE Line Receiver	883		CDIP
DS7820	14	Dual Line Receiver	883, MLS		CDIP, FP
DS7820A	14	Dual Line Receiver	883, MLS		CDIP, FP
DS7830	16	Dual Differential Line Driver	883, MLS		CDIP, FP
DS7831	16	Dual Differential TRI-STATE Line Driver	883	8004101xX	CDIP, FP
DS7832	16	Dual Differential TRI-STATE Line Driver	883	8004102xA	CDIP, FP
DS9615M	16	Dual Differential Line Receiver	883, MLS	10404*	CDIP, FP
DS9622M	16	Triple Line Receiver	883	5962-8752201xA	CDIP, LCC, FP
DS55107A	14	Dual Line Receiver	883	10401*	CDIP
DS55110A	14	Dual Line Driver	883		CDIP
DS55113	16	Dual Differential TRI-STATE Line Driver	883		CDIP
DS55115	16	Dual Differential Line Receiver	883, MLS	10404*	CDIP, FP
DS55122	16	Triple Line Receiver	883		CDIP
MM78C29	14	Quad Single-Ended Line Driver	883		CDIP, FP
MM78C30	14	Dual Differential Line Driver	883		CDIP

PACKAGING KEY:

Code	Suffix	Description
CDIP	J, D	Ceramic Dual-in-Line
LCC	E	Leadless Chip Carrier (Ceramic)
FP	W	Flatpak (Dual-in-Line, Ceramic)

National Semiconductor

Military/Aerospace Programs from National Semiconductor

The following is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our *Reliability Handbook.*

MIL-I-38535

National Semiconductor's Mil/Aero Division has received QML approval for the FAB and Assembly sites manufacturing Military Aerospace devices. The following section regarding MIL-M-38510 is undergoing revision and is expected to eventually merge into the MIL-I-38535 QML program. Please contact your local sales office for further details regarding this qualification timeline and status.

TABLE A. QML Marking Code

NS JM38510/33001
BCA 27014QS
Δ ZSSXXYYA

		Legend
NS	=	Corporate Logo
27014	=	Cage Code
Δ	=	ESD Indicator (as applicable)*
Z	=	Assembly Code Location
SS	=	Wafer Fab/Sort Data Code**
XXYY	=	Calendar Year/Seal Week***
Q	=	QML Processing
S	=	Test Location

***ESD Indicator Codes**

Mark	Class	Voltage
Δ	1	0-1999V
ΔΔ	2	2000–3999V
——	3	≥ 4000V

****Assembly Code Locations**

Country	Code
Bangkok	B
Combined Country of Origin	C
Cebu Philippines	D
Hong Kong	K
Indy Electronics	W
Japan	J
Korea	E
Malacca	M
Mountain View	V
Pantronix	A
Penang	P
Philippines	H
Puyallup	G
Salt Lake	L
Santa Clara	F
Singapore	S
South Portland	Z
Taiwan	T
Tucson	Y
United Kingdom	U
Outside Vendor	N

*****Calendar/Seal Week Codes**

2nd digit: Last digit of the year wafer sort was performed

3rd digit: Alpha character indicating the calendar quarter in which wafer sort was performed.

Character	Months	Weeks
A	Jan–Mar	13
B	April–June	14–26
C	July–Sept	27–39
D	Oct–Dec	40–53
GF	Prior to 1988	

4th & 5th digits: Calendar Year

6th & 7th digits: Sealweek

8th digit: Alphacharacter indicating the lot is a sublot (when applicable).

MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

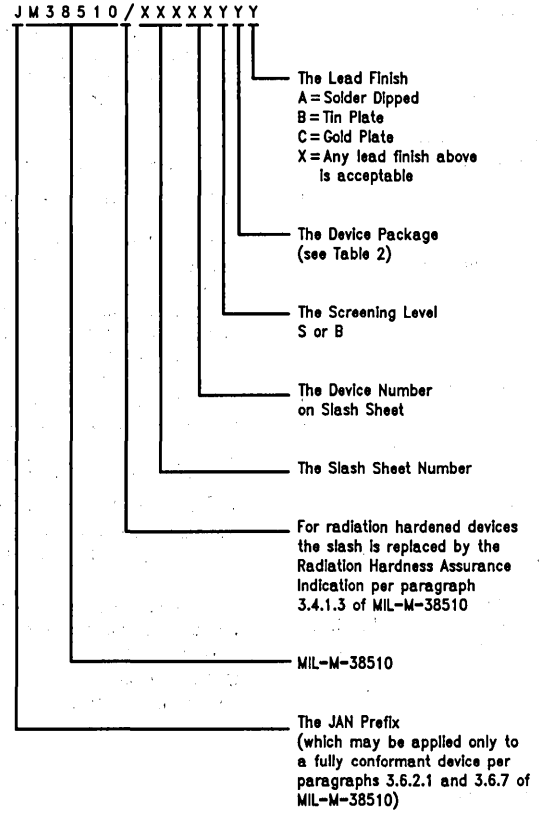
There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table 3.

Tables 1 and 2 explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

TABLE I. The MIL-M-38510 Part Marking



TL/XX/0113-1

MIL-M-38510 (Continued)

TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-Pin 1/4" x 1/4" (Metal) Flatpack
B	14-Pin 3/16" x 1/4" (Metal) Flatpack
C	14-Pin 1/4" x 3/4" Dual-In-Line
D	14-Pin 1/4" x 3/8" (Ceramic) Flatpack
E	16-Pin 1/4" x 7/8" Dual-In-Line
F	16-Pin 1/4" x 3/8" (Metal or Ceramic) Flatpack
G	8-Pin TO-99 Can or Header
H	10-Pin 1/4" x 1/4" (Metal) Flatpack
I	10-Pin TO-100 Can or Header
J	24-Pin 1/2" x 1 1/4" Dual-In-Line
K	24-Pin 3/8" x 5/8" Flatpack
L	24-Pin 1/4" x 1 1/4" Dual-In-Line
M	12-Pin TO-101 Can or Header
N	(Note 1)
P	8-Pin 1/4" x 3/8" Dual-In-Line
Q	40-Pin 3/16" x 2 1/16" Dual-In-Line
R	20-Pin 1/4" x 1 1/16" Dual-In-Line
S	20-Pin 1/4" x 1/2" Flatpack
T	(Note 1)
U	(Note 1)
V	18-Pin 3/8" x 15/16" Dual-In-Line
W	22-Pin 3/8" x 1 1/8" Dual-In-Line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-Terminal 0.350" x 0.350" Chip Carrier
3	28-Terminal 0.450" x 0.450" Chip Carrier

Note 1: These letters are assigned to packages by individuals MIL-M-38510 detail specifications and may be assigned to different packages in different specifications.

DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales representatives, of DESC. DESC is located in Dayton, Ohio.

MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision D of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification Program). The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883, but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product, but are marked "-MIL".

Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

Reliability Electrical Test Specifications (RETS)

National has implemented the first realtime, electronic catalog of military test specifications called RETS.

Included in this computerized directory is a detailed listing of the electrical tests performed on all military devices qualified by National, including forcing functions, test limits and temperature ranges.

Call your local National sales office for essential up-to-the-minute information on device testing.

TABLE III. Classes S and B Screening*

Screen	Class S		Class B	
	Method	Reqt	Method	Reqt
3.1.1 Wafer Lot Acceptance (Note 1)	5007	All Lots		
3.1.2 Nondestructive Bond Pull	2023	100%		
3.1.3 Internal Visual (Note 2)	2010, Test Condition A	100%	2010, Test Condition B	100%
3.1.4 Temperature Cycling (Note 3)	1010, Test Condition C	100%	1010, Test Condition C	100%
3.1.5 Constant Acceleration	2001, Test Condition E (Min) Y_1 Orientation Only	100%	2001, Test Condition E (Min) Y_1 Orientation Only	100%
3.1.6 Visual Inspection (Note 4)		100%		100%
3.1.7 Particle Impact Noise Detection (PIND)	2020, Test Condition A	100% (Note 5)		
3.1.8 Serialization		100% (Note 6)		
3.1.9 Pre Burn-In Electrical Parameters	In accordance with Applicable Device Specification	100% (Note 7)	In accordance with Applicable Device Specification	100% (Note 8)
3.1.10 Burn-In Test	1015 (Note 9) 240 Hours at 125°C Minimum	100%	1015 160 Hours at 125°C Minimum	100%
3.1.11 Interim (Post-Burn-In) Electrical Parameters	In accordance with Applicable Device Specification	100% (Note 7)		
3.1.12 Reverse Bias Burn-In (Note 10)	1015; Test Condition A or C, 72 Hours at 150°C Minimum	100%		
3.1.13 Interim (Post Burn-In) Electrical Parameters	In accordance with Applicable Device Specification	100% (Note 7)	In accordance with Applicable Device Specification	100% (Note 8)
3.1.14 Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters at 25°C	All Lots	5%	All Lots
3.1.15 Final Electrical Test	In accordance with Applicable Device Specification		In accordance with Applicable Device Specification	
a. Static Tests		100%		100%
1. 25°C (Subgroup 1, Table I, 5005)		100%		100%
2. Maximum and Minimum Rated Operating Temperature (Subgroups 2, 3, Table I, 5005)				
b. Dynamic or Functional Tests (Note 11)				
1. 25°C (Subgroup 4 or 7, Table I Method 5005)		100%		100%
2. Minimum and Maximum Rated Operating Temperature (Subgroups 5 and 6, or 8, Table I Method 5005)		100%		100%
c. Switching Tests 25°C (Subgroup 9, Table I, Method 5005)		100%		100%

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

TABLE III. Classes S and B Screening* (Continued)

Screen	Class S		Class B	
	Method	Reqt	Method	Reqt
3.1.16 Seal a. Fine b. Gross	1014	100% (Note 12)	1014	100% (Note 12)
3.1.17 Radiographic (Note 13)	2012 Two Views (Note 14)	100%		
3.1.18 Qualification or Quality Conformance Inspection Test Sample Selection		(Note 15)		(Note 15)
3.1.19 External Visual (Note 16)	2009	100%	2009	100%
3.1.20 Radiation Latch-Up (Note 17)	1020	100%	1020	100%

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: All lots shall be selected for testing in accordance with the requirements of Method 5007 herein.

Note 2: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam).

Note 3: For Class B devices, this test may be replaced with thermal shock Method 1011, test condition A, minimum.

Note 4: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 5: See MIL-I-38535, 40.6.3. The PIND test may be performed in any sequence after 3.1.4 and prior to 3.1.13.

Note 6: Class S devices shall be serialized prior to initial electrical parameter measurements.

Note 7: Post burn-in electrical parameters shall be read and recorded (see 3.1.13, subgroup 1). Pre burn-in or interim electrical parameters (see 3.1.9 and 3.1.11) shall be read and recorded only when delta measurements have been specified as part of post burn-in electrical measurements.

Note 8: When specified in the applicable device specification, 100 percent of the devices shall be tested for those parameters requiring delta calculations.

Note 9: Dynamic burn-in only. Test condition F of Method 1015 shall not apply.

Note 10: Reverse bias burn-in (see 3.1.12) is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be of concern. When reverse bias burn-in is not required, interim electrical parameter measurements 3.1.11 are omitted. The order of performing the burn-in (see 3.1.10) and the reverse bias burn-in may be inverted.

Note 11: Functional tests shall be conducted at input test conditions as follows:
$V_{IH} = V_{IH}(\min) + 20\%, -0\%$; $V_{IL} = V_{IL}(\max) + 0\%, -50\%$; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH}(\min)$ and $V_{IL}(\max)$.
CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH}(\min)$ and $V_{IL}(\max)$ requirements are not violated at the device terminals.

Note 12: For Class B devices, the fine and gross seal tests (3.1.16) shall be performed separately or together, between constant acceleration (3.1.5) and external visual (3.1.19). For class S devices, the fine and gross seal tests (3.1.16) shall be performed separately or together, between final electrical testing (3.1.15) and external visual (3.1.19). In addition, for classes S and B devices, all device lots (sublots) having any physical processing steps (e.g., lead shearing, lead forming, solder dipping to the glass seal, change of, or rework to, the lead finish, etc.) performed following seal (3.1.16) or external visual (3.1.19) shall be retested for hermeticity and visual defects. This shall be accomplished by performing, and passing, as a minimum, a sample seal test (Method 1014) using an acceptance criteria of a quantity (accept number) of 116(0), and an external visual inspection (Method 2009) on the entire inspection lot (sublot). For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance. For class S devices, with the approval of the qualifying activity, an additional room temperature electrical test may be performed subsequent to seal (3.1.16), but before external visual (3.1.19) if the devices are installed in individual carriers during electrical test.

Note 13: The radiographic (see 3.1.17) screen may be performed in any sequence after 3.1.8.

Note 14: Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides.

Note 15: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005. See 3.5 of Method 5005.

Note 16: External visual shall be performed on the lot any time after 3.1.17 and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing. Exposed underplate or base metal on leads of hard glass seals, bead seals, or individual feedthrough seals due to acceptable glass meniscus chipouts shall not be considered rejectable provided salt atmosphere test requirements (Method 1009) are met in accordance with applicable group D requirements. Acceptable glass meniscus chipouts are defined as chipouts in the glass meniscus that are located within the region one-half the distance from the lead to the case.

Note 17: Radiation latch-up screen shall be conducted when specified in purchase order or contract. Latch-up screen is note required for SOS, SIO, and DI technology when latch-up is physically not possible. At the manufacturer's option, latch-up screen may be conducted at any screening operation step after seal.

TABLE IV. Group A Electrical Tests for Classes S and B Devices* (Note 1)

Subgroups (Note 2) Quality/Accept No. = 116/0 (Notes 3 to 5)
Subgroup 1 Static Tests at 25°C
Subgroup 2 Static Tests at Maximum Rated Operating Temperature
Subgroup 3 Static Tests at Minimum Rated Operating Temperature
Subgroup 4 Dynamic Tests at 25°C
Subgroup 5 Dynamic Tests at Maximum Rated Operating Temperature
Subgroup 6 Dynamic Tests at Minimum Rated Operating Temperature
Subgroup 7 Functional Tests at 25°C
Subgroup 8A Functional Tests at Maximum Rated Operating Temperatures
Subgroup 8B Functional Tests at Minimum Rated Operating Temperatures
Subgroup 9 Switching Tests at 25°C
Subgroup 10 Switching Tests at Maximum Rated Operating Temperature
Subgroup 11 Switching Tests at Minimum Rated Operating Temperature

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

Note 2: At the manufacturer's option, the applicable tests required for Group A testing (see Note 1) may be conducted individually or combined into sets of tests, subgroups (as defined in Table I), or sets of subgroups. However, the munufacturer shall predesignate these groupings prior to Group A testing. Unless otherwise specified, the individual tets, subgroups, or sets of tests/subgroups may be performed in any sequence.

Note 3: The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in Note 2, shall be 116/0.

Note 4: A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

Note 5: If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For class S only, if this testing results in a percent defective greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/ subgroups, as applicable, using a 116/0 sample.

TABLE V. Group B Tests for Class S Devices* (Note 1)

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 1			
a. Physical Dimensions (Note 2)	2016		2(0)
b. Internal Water-Vapor Content (Notes 2 and 3)	1018	5,000 ppm Maximum Water Content at 100°C	3(0) or 5(1) (Note 4)
Subgroup 2 (Note 5)			
a. Resistance to Solvents	2015		3(0)
b. Internal Visual and Mechanical	2013, 2014	Failure Criteria from Design and Construction Requirements of Applicable Acquisition Document	2(0)
c. Bond Strength	2011		LTPD = 10 (Note 6)
1. Thermocompression		1. Test Condition C or D	
2. Ultrasonic		2. Test Condition C or D	
3. Flip-Chip		3. Test Condition F	
4. Beam Lead		4. Test Condition H	
d. Die Shear Test or Substrate Attach Strength Test		In accordance with Method 2019 or 2027 for the Applicable Die Size	3(0)
Subgroup 3			
Solderability (Note 7)	2003 or 2022	Soldering Temperature of 245°C ±5°C	LTPD = 10
Subgroup 4 (Note 2)			LTPD = 5
a. Lead Integrity (Note 8)	2004	Test Condition B_2, Lead Fatigue	
b. Seal	1014	As applicable	
1. Fine			
2. Gross			
c. Lid Torque (Note 9)	2024	As applicable	
Subgroup 5 (Note 10)			LTPD = 5
a. End-Point Electrical Parameters (Note 11)		As Specified in the Applicable Device Specification	
b. Steady State Life (Note 12)	1005	Test Condition C, D, or E	
c. End-Point Electrical Parameter (Note 11)		As specified in the applicable device specification	
Subgroup 6			LTPD = 15
a. End-Point Electrical Parameters		As specified in the Applicable Device Specification	
b. Temperature Cycling	1010	Condition C, 100 Cycles Minimum	
c. Constant Acceleration	2001	Test Condition E: Y1 Orientation Only	
d. Seal	1014		
1. Fine			
2. Gross			
e. End-Point Electrical Parameters		As Specified in the Applicable Device Specification	
Subgroup 7 (Note 13)			

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Electrical reject devices from that same inspection lot may be used for all subgroups when end-point measurements are not required, provided that the rejects are processed identically to the inspection lot through pre burn-in electricals and provided the rejects are exposed to the full temperature/time exposure of burn-in.

Note 2: Not required for qualification or quality conformance inspections where Group D inspection is being performed on samples from the same inspection lot.

Note 3: This test is required only if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed Method 1018, procedure 3 shall be used. See Note 6 of Table IV.

Note 4: Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., three or five devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot.

Note 5: Resistance to solvents testing required only on devices using inks or paints as a marking medium.

Note 6: Unless otherwise specified, the LTPD sample size for conditions C and D is the number of bond pulls selected from a minimum number of four devices, and for condition F or H is the number of dice (not bonds).

Note 7: All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.

TABLE V. Group B Tests for Class S Devices* (Note 1) (Continued)

Note 8: The LTPD of 5 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of three devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable (see Note 9), in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use Method 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a LTPD of 15 based on the number of pads tested taken from three devices minimum. Seal test (subgroup 46) need be performed only on packages having leads exiting through a glass seal.

Note 9: Lid torque test shall apply only to glass-frit-sealed packages.

Note 10: The alternate removal-of-bias provisions of 3.3.1 of Method 1005 shall not apply for test temperature above +125°C.

Note 11: Read and record group A subgroups 1, 2, and 3.

Note 12: The same test temperature that was used for burn-in shall be used for the steady-state life test.

Note 13: Subgroup 7 has been deleted from Table V. The requirements for ESD testing are specified in MIL-M-38510.

TABLE VI. Group B Tests for Class B* (Notes 1 and 2)

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 2 (Note 3) a. Resistance to Solvents	2015		3 (0)
Subgroup 3 a. Solderability (Note 4)	2003 or 2022	Soldering Temperature of 245°C ±5°C	10
Subgroup 5 a. Bond Strength (Note 5) 1. Thermocompression 2. Ultrasonic or Wedge 3. Flip-Chip 4. Beam Lead	2011	 1. Test Condition C or D 2. Test Condition C or D 3. Test Condition F 4. Test Condition H	15

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electricals and provided the rejects are exposed to the full temperature/time exposure of burn-in.

Note 2: Subgroups 1, 4, 6, 7, and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.

Note 3: Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium.

Note 4: All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.

Note 5: Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in Method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of four devices, and for condition F or H is the number of dice (not bonds) (see Method 2011).

TABLE VII. Group C (Die-Related Tests) (For Class B Only)*

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 1			
a. Steady-State Life Test	1005	Test Condition to be Specified (1,000 Hours at 125°C or Equivalent in Accordance with Table I)	5
b. End-Point Electrical Parameters		As specified in the Applicable Device Specification	

TABLE VIII. Group D (Package-Related Tests for All Classes)*

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 1 (Note 2)			
a. Physical Dimensions	2016		15
Subgroup 2 (Note 2)			
a. Lead Integrity (Note 3)	2004	Test Condition B_2 (Lead Fatigue)	5
b. Seal (Note 4)			
1. Fine	1014	As Applicable	
2. Gross			
Subgroup 3 (Note 5)			
a. Thermal Shock	1011	Test Condition B as a Minimum, 15 Cycles Minimum	15
b. Temperature Cycling	1010	Test Condition C, 100 Cycles Minimum	
c. Moisture Resistance (Note 6)	1004		
d. Visual Examination		In accordance with visual criteria of Method 1004 and 1010	
e. Seal	1014	As Applicable	
1. Fine			
2. Gross (Note 7)			
f. End-point Electrical Parameters (Note 8)		As specified in the Applicable Device Specification	
Subgroup 4 (Note 5)			
a. Mechanical Shock	2002	Test Condition B Minimum	15
b. Vibration, Variable Frequency	2007	Test Condition A Minimum	
c. Constant Acceleration	2001	Test Condition E Minimum (See Note 3), Y_1 Orientation Only	
d. Seal	1014	As Applicable	
1. Fine			
2. Gross			
e. Visual Examination	(Note 9)		
f. End-Point Electrical Parameters		As Specified in the Applicable Device Specification	
Subgroup 5 (Note 2)			
a. Salt Atmosphere (Note 6)	1009	Test Condition A Minimum	15
b. Visual Examination		In accordance with visual criteria of Method 1009	
c. Seal	1014	As Applicable	
1. Fine			
2. Gross (Note 7)			
Subgroup 6 (Note 2)			
a. Internal Water-Vapor Content	1018	5,000 ppm Maximum Water Content at 100°C	3(0) or 5(1) (Note 10)
Subgroup 7 (Note 2)			
a. Adhesion of Lead Finish (Notes 11 and 12)	2025		15
Subgroup 8			
a. Lid Torque (Notes 2 and 13)	2024		5 (0)

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: In-line monitor data may be substituted for subgroups D1, D2, D6, D7 and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. This in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.

Note 2: Electrical reject devices from that same inspection lot may be used for samples.

TABLE VIII. Group D (Package-Related Tests for All Classes) (Continued)

Note 3: The LTPD of 5 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of three devices. All devices required for the lead integrity test shall pass the seal test if applicable (see Note 4) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use Method 2028. For leadless chip carrier packages only, use test condition D and an LTPD of 15 based on the number of pads tested taken from three devices minimum.

Note 4: Seal test (Subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

Note 5: Devices used in Subgroup 3, "Thermal and Moisture Resistance" may be used in Subgroup 4, "Mechanical".

Note 6: Lead bend stress initial conditioning is not required for leadless chip carrier packages.

Note 7: After completion of the required visual examinations and prior to submittal to Method 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.

Note 8: At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

Note 9: Visual examination shall be in accordance with Method 1010 or 1011.

Note 10: Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., three or five devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot.

Note 11: The adhesion of lead finish test shall not apply for leadless chip carrier packages.

Note 12: LTPD based on number of leads.

Note 13: Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermeticity or package integrity).

TABLE IX. Group E (Radiation Hardness Assurance Tests)* (Note 1)

Test	MIL-STD-883		Class S		Class B	
	Method	Condition	Quantity/Accept Number	Notes	Quantity/Accept Number	Notes
Subgroup 1 (Note 2)						
Neutron Irradiation	1017	25°C				
a. Qualification			a. 11(0)	(Note 3)	a. 11(0)	(Note 4)
b. QCI			b. 11(0)	(Note 3)	b. 11(0)	(Note 4)
Endpoint Electrical Parameters		As specified in accordance with detail specification				
Subgroup 2 (Note 5)						
Steady-State Total Dose Irradiation	1019	25°C, Maximum Supply Voltage				
a. Qualification			a. 4(0) 2(0)	a. (Note 6) (Note 8)	a. 22(0)	(Note 7)
b. QCI			b. 4(0) 2(0)	b. (Note 6) (Note 8)	b. 22(0)	(Note 7)
Endpoint Electrical Parameters		As specified in accordance with detail specification				
Subgroup 3 (Note 9)						
Transient						
Ionizing	1021	25°C	11(0)	(Note 3)	11(0)	(Note 4)
Irradiation	1023	25°C				
Endpoint Electrical Parameters		As specified in accordance with detail specification				

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. Group E tests may be performed prior to device screening.

Note 2: Waive neutron tests for MOS devices where neutron susceptability is less than 10^{13} neutrons/cm^2 (e.g. charge coupled devices, BICMOS, etc.). When testing is required, the limit for neutron fluence shall be 2×10^{12} neutrons/cm^2.

Note 3: In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

Note 4: In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

Note 5: Class B devices shall be inspected using either the class B quantity/accept number criteria as specified, or by using the class S criteria on each wafer.

Note 6: In accordance with wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.

Note 7: In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

Note 8: In accordance with wafer for device types with greater than 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.

Note 9: Upset testing during qualification on first QCI shall be conducted when specified in purchase order or contract. When specified, the same microcircuits may be tested in more than one subgroup.

TABLE X. Wafer Lot Acceptance Tests*

Test	Conditions (Note 1)	Limits (Note 3)	Sampling Plan
1. Wafer Thickness	MIL-STD-977 Method 1580. Measurement shall be performed after final lap or polish. All readings shall be recorded. (Note 2)	Maximum deviation of ±2 mil from approved design nominal 6 mil minimum.	Two wafers per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.
2. Metallization Thickness	MIL-STD-977 Method 5500. All readings shall be recorded.	a. Conductor: 8 kÅ minimum for single level metal and for the top level of multi-level metal; 5 kÅ minimum for lower levels, with a maximum deviation of ±20% from the approved design nominal. b. Barrier: Maximum deviation of ±30% from the approved design nominal.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.
3. Thermal stability (applicable to: All linear; all MOS; all bipolar digital operating at 10V or more)	MIL-STD-977, Method 2500. Record V_{FB} or V_T.	a. ΔV_{FB} or $\Delta V_T \leq 0.75$, normalized to an oxide thickness of 1000Å for bipolar digital devices operating at 10V or greater and all bipolar linear devices not containing MOS transistor(s). The monitor shall have an oxide and shall be metallized with the lot. b. ΔV_{FB} or $\Delta V_T \leq 1.0V$, normalized to an oxide thickness of 1,000Å for bipolar linear devices that operate above 5V and containing MOS transistor(s), and digital devices that operate above 10V and containing MOS structures. The V_{FB} limit shall not be exceeded by the sum of the absolute values of the MOS oxide transistors and the metallization Δ. The monitor(s) shall be oxidized and metallized with the lot. Separate monitors may be used for this test. c. ΔV_{FB} or $V_T \leq 0.4V$, normalized to an oxide thickness of 1,000Å for MOS devices. A monitor consisting of a gate oxide metallized with the lot shall be used.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Approved equivalent test methods may be used in lieu of the MIL-STD-977 reference method.

Note 2: This test is not required when the finished wafer design thickness is greater than 10 mil.

Note 3: Approved design nominal values or tolerances shall be submitted for line certification in accordance with DESC-EQM-42.

TABLE X. Wafer Lot Acceptance Tests* (Continued)

Test	Conditions (Note 1)	Limits (Note 3)	Sampling Plan
4. SEM	MIL-STD-883, Method 2018.	MIL-STD-883, Method 2018.	MIL-STD-883, Method 2018. Lot acceptance basis.
5. Glassivation thickness	MIL-STD-977, Method 5500. All readings shall be recorded.	6 kÅ minimum for SiO_2 and 2 kÅ for Si_3N_4 with maximum deviation of ±20% from approved design nominal.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.
6. Gold backing thickness (When applicable)	MIL-STD-977, Method 5500. All readings shall be recorded.	In accordance with approved design nominal thickness and tolerance.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Approved equivalent test methods may be used in lieu of the MIL-STD-977 reference method.

Note 2: This test is not required when the finished wafer design thickness is greater than 10 mil.

Note 3: Approved design nominal values or tolerances shall be submitted for line certification in accordance with DESC-EQM-42.

Section 10

Appendices and Physical Dimensions

Section 10 Contents

Common Data Transmission Parameters and their Definitions

National Semiconductor
Application Note 912
John Goldie

OVERVIEW

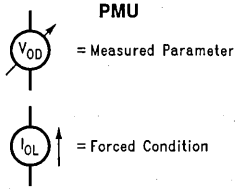
The scope of this application note is to introduce common data transmission parameters and to provide their definitions. This application note is subdivided into five sections, which are:

- Voltage Parameters
- Current Parameters
- Timing Parameters
- Miscellaneous Parameters
- Truth Table Explanations

Each parameter definition typically includes the following information: symbol, full name, description of measurement, measurement diagram, and a list of alternate names where applicable. Due to historical reasons (Fairchild origin, National origin, second sourcing, etc.) some devices use alternate symbols for the same parameters. Whenever possible, a list of common alternate symbols is provided for cross reference. New and future devices from National's Data Transmission Products Group will use the parameters as described in this application note for consistency and clarity reasons and to limit confusion.

This application note will be revised to add new parameters as required by new product definition.

In this application note the following symbols are used in test circuit diagrams. The measured parameter symbol represents a PMU—Precision Measurement Unit located at the test points illustrated in the test circuit. The PMU symbol also includes the parameter's name that is under test. The forced condition represents a forced voltage or current which is required to make the parameter measurement. Once again, it includes the parameter symbol that is being forced.



TL/F/11932–1

VOLTAGE PARAMETERS

Input Voltage Parameters

V_{CL}—Input Clamp Voltage. An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{CM}—Common Mode Voltage. The algebraic mean of the two voltages applied to the referenced terminals, for example the receiver's input terminals. This voltage is referenced to circuit common (ground). This parameter is illustrated in *Figure 1* along with its mathematical equation.

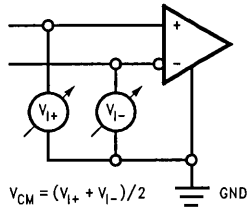


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FIGURE 1. Common Mode Voltage

V_{DIFF}—Differential Input Voltage. The potential difference between the input terminals of the device (receiver) with respect to one of the inputs (typically the inverting input terminal). This parameter may be a positive or negative voltage, and commonly specifies the minimum operating voltage and the absolute maximum differential input voltage. See *Figure 2*. V_{DIFF} is also known as V_{ID} for input differential voltage.

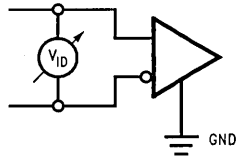

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FIGURE 2. Differential Input Voltage

V_{IH}—High-Level Input Voltage. An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. For example an input voltage between 2.0V and 5.0V in the case of standard TTL logic.

Note: A minimum is specified that is the least positive value of the high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL}—Low-Level Input Voltage. An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables. For example an input voltage between 0.0V and 0.8V in the case of standard TTL logic.

Note: A maximum is specified that is the most positive value of the low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{TH}—Positive-Going Threshold Voltage. The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage rises from a level below the negative-going threshold voltage, V_{TL}. See *Figure 3*. Note that V_{TH} has also been used in the past to specifiy both thresholds in one parameter. In this case, V_{TH} represents the Threshold Voltages and supports a minimum and maximum limit, for example, ±200 mV.

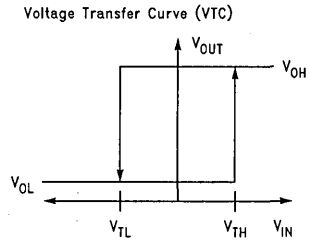

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FIGURE 3. Threshold Voltages

V_{TL}—Negative-Going Threshold Voltage. The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage falls from a level above the positive-going threshold voltage, V_{TH}. See *Figure 3* above.

V_{HYS}—Hysteresis. The absolute difference in voltage value between the positive going threshold and the negative going threshold. See *Figure 4*. Hysteresis is the most widely symbolized parameter. Alternate symbols include: V_{HY}, $V_{T+}-V_{T-}$, V_{HYST}, ΔV_{TH}, $V_{TH}-V_{TL}$, and V_{HST}.

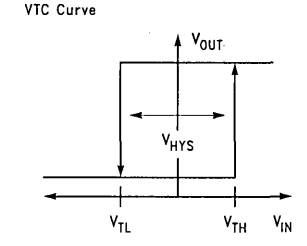

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FIGURE 4. Hysteresis Voltage

OUTPUT VOLTAGE PARAMETERS

V_{OD}—Output Differential Voltage. The output voltage between the output terminals of a differential driver with input conditions applied that, according to the product specification, will establish a voltage level at the output. This voltage is measured with respect to the inverting output of the differential driver. V_{OD} is defined as the voltage at true output (A, $D_{OUT}+$, or DO) minus the voltage at the inverting output (B, $D_{OUT}-$, or DO*). Commonly an alpha-numeric suffix is added to designate specific test conditions. For example the case of different resistive loads. Also a star "*" or over-score bar is used with the parameter to designate the parameters' value with the opposite input state applied. This parameter has also been designated Terminated Output Voltage (V_T) in some datasheets.

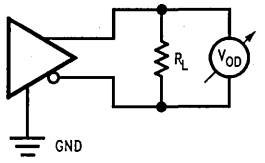

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FIGURE 5. V_{OD} Test Circuit

ΔV_{OD}—Output Voltage Unbalance. The change in magnitude of the differential output voltage between the output terminals of a differential driver with opposite input conditions applied. ΔV_{OD} is defined as: $\Delta V_{OD}=|V_{OD}|-|V_{OD}*|$.

V_{OH}—High Level Output Voltage. The output voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the output. This voltage is measured with respect to circuit common (ground). See *Figure 6*.

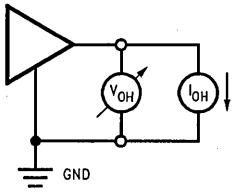

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FIGURE 6. V_{OH} Test Circuit

V_{OL}—Low Level Output Voltage. The output voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic low level at the output. This voltage is measured with respect to circuit common (ground). See *Figure 7*.

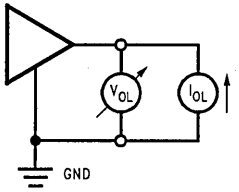

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FIGURE 7. V_{OL} Test Circuit

V_{OS}—Offset Voltage. The center point output voltage between the output terminals of a differential driver with input conditions applied that, according to the product specification, will establish a voltage level at the output. This voltage is measured with respect to the driver's circuit common (ground). Commonly a star "*" or over-score bar is used with the parameter to designate the parameter's value with the opposite input state applied (see *Figure 8*). This parameter is also referred to as V_{OC}—Common Mode Voltage.

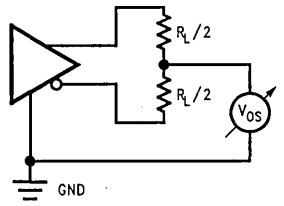

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FIGURE 8. V_{OS} Test Circuit

ΔV_{OS}—Offset Voltage Unbalance. The change in magnitude of the offset voltage at the output terminals of a differential driver with opposite input conditions applied. ΔV_{OS} is defined as:

$$\Delta V_{OS} = |V_{OS}| - |V_{OS}^*|.$$

V_{SS}—Steady State Output Voltage. The steady state differential output voltage is defined as $|V_{OD}| + |V_{OD}^*|$. This is typically a calculated parameter only, based on the formula shown above. The V_{OD} parameter is defined above and illustrated in *Figure 5*. V_{SS} is equal to twice the magnitude of V_{OD} and is shown in *Figure 9*.

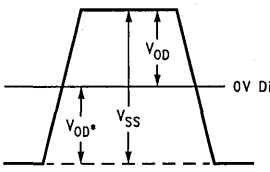

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FIGURE 9. Differential Output Steady State Voltage

V_T—Terminated Output Voltage. The output voltage at an output terminal with input conditions applied that, according to the product specification, will establish a known logic level at the output. This voltage is measured with respect to circuit common (ground) with a stated resistance, and may be a positive or negative voltage. This parameter is typically used in conjunction with single-ended (unbalanced) line drivers. See *Figure 10*.

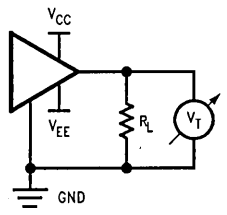

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FIGURE 10. V_T Test Circuit

ΔV_T—Terminated Output Voltage Unbalance. The change in magnitude of the terminated output voltage at the output terminal of a single-ended line driver with opposite input conditions applied. ΔV_T is defined as:

$$\Delta V_T = |V_T| - |V_T^*|.$$

CURRENT PARAMETERS

Note: Current is specified as magnitude value only, with the sign denoting the current direction only. A negative sign defines current flowing out of a device pin, while a positive sign defines current flowing into a device pin. The largest current limit is specified as a maximum, and zero (0) by default is the smallest minimum. All future DTP datasheets will follow this convention, and only some existing datasheets follow this convention.

I_{IH}—High-Level Input Current. The current into (out of) an input when a high-level voltage is applied to that input. Note that current out of a device pin is given as a negative value. Typically this parameter specifies a positive maximum value for bipolar devices.

I_{IL}—Low-Level Input Current. The current into (out of) an input when a low-level voltage is applied to that input. Note that current out of a device pin is given as a negative value.

I_I—Maximum Input Current. The current into (out of) an input when the maximum specified input voltage is applied to that input. Note that current out of a device pin is given as a negative value.

I_{IN}—Input Current. The current into (out of) a receiver input when a specified input voltage, or voltage range is applied to that input. Note that current out of a device pin is given as a negative value. This parameter is typically tested at the maximum voltage specified for the input. For differential receivers the other input (not under test) is held at 0V (in the case of RS-422/3 and 485 receivers).

I_{ING}—Input Current, Power Up Glitch. The current into (out of) an input when a specified input voltage, or voltage range is applied to that input. Note that current out of a device pin is given as a negative value. This parameter applies to transceivers (RS-485) only, and is actually specifying the driver's performance at a specific power supply level. Additionally the driver is biased such that it is enabled, with the specified power supply voltage applied. This parameter assures that the driver is disabled by an internal circuit at the specified power supply level, even though the enable pin is active. If the driver was enabled, I_{OS} current would be observed, instead of the combined measured current of driver TRI-STATE® leakage (I_{OZ}) plus receiver input current (I_{IN}). For example $V_{CC} = 3.0V$ is commonly referenced to represent a single point in a power up/down cycle. (See AN-905 for more information on this parameter).

I_{OS}—Output Short Circuit Current. The current into (out of) an output when that output is short-circuited to circuit common (ground) or any other specified potential, with input conditions as noted, typically such that the output logic level is the furthest potential from the applied voltage. This parameter commonly includes an identifying suffix. For example I_{OSD} represents the output short circuit current of a driver, while I_{OSR} represents the receiver's output short circuit current. Output short circuit current is also designated by the following symbols: I_{O+}, I_{SC}, and I_S. See *Figure 11*.

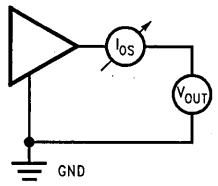

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FIGURE 11. I_{OS} Test Circuit

I_{OZ}—TRI-STATE Output Current. The current into (out of) a TRI-STATE output having input (control) conditions applied that, according to the product specification, will establish a high impedance state at the output. This parameter commonly includes an identifying suffix. For example, I_{OZD} represents the TRI-STATE output current of a driver, while I_{OZR} represents the receiver's TRI-STATE output current. In addition I_{OZH} and I_{OZL} are also commonly used and denote the forced voltage (logic) level. See *Figure 12.*

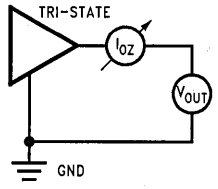

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FIGURE 12. I_{OZ} Test Circuit

I_{OX}—Power Off Leakage Current. The current flowing into (out of) an output with input conditions applied that, according to the product specification, will establish a high impedance state at the output. Commonly a known state is required on the power supply pin as an input condition. For example, power supply terminal (V_{CC}) equal to zero volts may be a required condition of an I_{OX} parameter. See *Figure 13.*

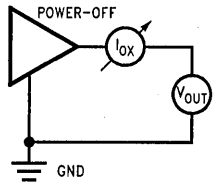

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FIGURE 13. I_{OX} Test Circuit

I_{OD}—Differential Output Current. The current flowing between the output terminals of a differential line driver with an external differential load applied that, according to the product specification, will establish a known state at the output. See *Figure 14.*

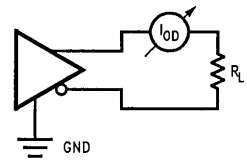

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FIGURE 14. Differential Output Current

I_{OH}—High-Level Output Current. The current into (out of) an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the corresponding output. Note that current out of a terminal is given as a negative value.

I_{OL}—Low-Level Output Current. The current into (out of) an output terminal with input conditions applied that, according to the product specification, will establish a logic low level at the corresponding output. Note that current out of a terminal is given as a negative value.

I_{CC}—Supply Current. The current into the V_{CC} supply terminal of the integrated circuit. Normally the parameter is measured with all loads removed. It may also include a suffix that denotes that state of the device. For example:

I_{CCD} = Power Supply Current
(drivers enabled, receivers disabled)

I_{CCR} = Power Supply Current
(receivers enabled, drivers disabled)

I_{CCZ} = Power Supply Current
(drivers and receivers disabled)

I_{CCX} = Power Supply Current
(sleep or shutdown mode)

I_{EE}—Supply Current. The current into the V_{EE} supply terminal of the integrated circuit. Normally the parameter is measured with all loads removed. It may also include a suffix that denotes that state of the device. Note that current out of a terminal is given as a negative value. For example:

I_{EED} = Power Supply Current
(drivers enabled, receivers disabled)

I_{EER} = Power Supply Current
(receivers enabled, drivers disabled)

I_{EEZ} = Power Supply Current
(drivers and receivers disabled)

I_{EEX} = Power Supply Current
(sleep or shutdown mode)

TIMING PARAMETERS

t_{PLH}—Propagation Delay Time, Low-to-High-Level Output. The time between specified reference points on the input and output voltage waveforms with the output changing from a logic low level to a logic high level.

t_{PHL}—Propagation Delay Time, High-to-Low-Level Output. The time between specified reference points on the input and output voltage waveforms with the output changing from a logic high level to a logic low level.

t_{SK}—Propagation Delay Skew. The magnitude difference between complementary propagation delays. Skew is defined as $|t_{PLH} - t_{PHL}|$. This specification is a per channel parameter unless specified otherwise.

t_{PLHD}—Differential Propagation Delay Time, Low-to-High-Level Output. The time between specified reference points on the input and output differential voltage waveforms with the output changing from a logic low level to a logic high level.

t_{PHLD}—Differential Propagation Delay Time, High-to-Low-Level Output. The time between specified reference points on the input and output differential voltage waveforms with the output changing from a logic high level to a logic low level.

t_{SKD}—Differential Propagation Delay Skew. The magnitude difference between complementary differential propagation delays. Skew is defined as $|t_{PLHD} - t_{PHLD}|$. This specification is a per channel parameter unless specified otherwise.

t_{PZH}—Output Enable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from a high impedance (off) state to a logic high level.

t_{PZL}—Output Enable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from a high impedance (off) state to a logic low level.

t_{PHZ}—Output Disable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from logic high level to a high impedance (off) state.

t_{PLZ}—Output Disable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from logic low level to a high impedance (off) state.

t_{PSH}—Propagation Delay Time, Sleep-to-High-Level Output. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from an off state to a logic high level.

t_{PSL}—Propagation Delay Time, Sleep-to-Low-Level Output. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from an off state to a logic low level.

t_{PHS}—Propagation Delay Time, High-Level Output to Sleep. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from logic high level to an off state.

t_{PLS}—Propagation Delay Time, Low-Level Output to Sleep. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from logic low level to an off state.

t_r—Rise Time. The time between two specified reference points on an input waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from low to high. Note, also commonly specified as transition time (t_{TLH}).

t_f—Fall Time. The time between two specified reference points on an input waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from high to low. Note, also commonly specified as transition time (t_{THL}).

t_{TLH}—Transition Time Low to High. The time between two specified reference points on an input waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from low to high. Note, also commonly specified as rise time (t_r).

t_{THL}—Transition Time High to Low. The time between two specified reference points on an output waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from high to low. Note, also commonly specified as fall time (t_f).

t_{NW}—Noise Pulse Width. The width in time of a pulse applied to a device. The parameter is commonly specified with receivers that feature low pass noise filters. t_{NW} is the pulse width assumed to be noise and guaranteed to be rejected.

MISCELLANEOUS PARAMETERS

SR—Slew Rate. The time between two specified reference points on an output waveform, normally between the ±3V level for TIA/EIA-232 (RS-232) drivers, divided by the voltage difference. Note, this parameter is normally specified in Volts per microsecond (V/μs). A suffix may be added to denote different loading conditions.

R_{IN}—Input Resistance. The slope of the input voltage vs. input current curve of an input when a specified voltage range is applied to that input and the current is measured. Note, that two points must be measured for the parameter to be calculated correctly as R_{IN} is defined as $\Delta V/\Delta I$ not V/I.

R_{OUT}—Output Impedance. The resulting output impedance calculated from measured currents at applied voltages.

TRUTH TABLE EXPLANANTIONS

Symbols generally associated with functional truth tables are listed below:

H or 1 = Logic High Level (steady state)

L or 0 = Logic Low Level (steady state)

Z = TRI-STATE® (high impedance off state)

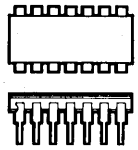
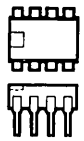
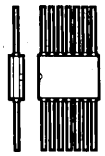
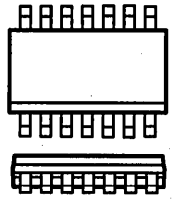
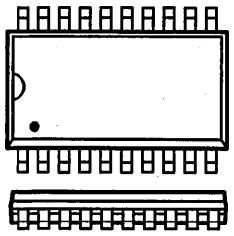
X = irrelevant (input, including transitions)

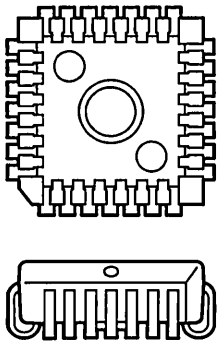
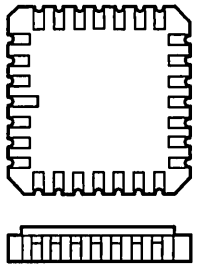
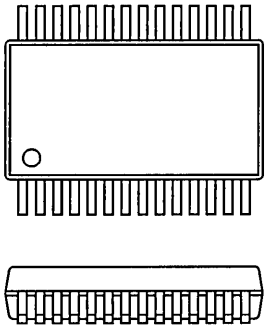
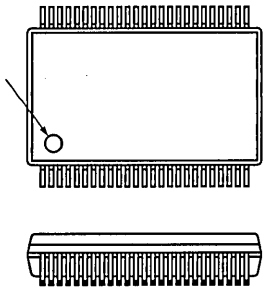
REFERENCES

ALS/AS IC Device Testing, ALS/AS Logic Databook. National Semiconductor Corp., 1990

Glossary of Terms, ALS/AS Logic Databook. National Semiconductor Corp., 1990

DTP Package Cross-Reference Guide

	NSC	Motorola	TI	AMD
 8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	U	J	D
 8-, 14- and 16-Lead Plastic DIP	N	P	P, N	P
 Low Temperature Glass Hermetic Flat Pack	W	F	W	F
 SO (Narrow Body)	M	D	D	
 SO (Wide Body)	WM		DW	

	NSC	Motorola	TI	AMD
 PCC	V	FN	FN	L
 LCC Leadless Ceramic Chip Carrier	E	U	FK/ FD	
 SSOP Shrink Small Outline Package (EIAJ, Type II)	MSA		DB	
 SSOP Shrink Small Outline Package (JEDEC)	MEA		DL	

Understanding Integrated Circuit Package Power Capabilities

National Semiconductor
Application Note 336
Charles Carinalli
Josip Huljev

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

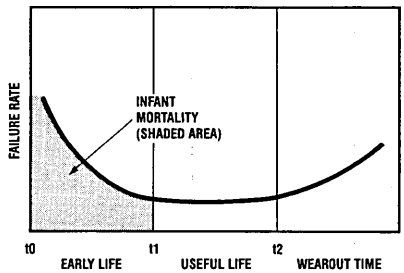


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

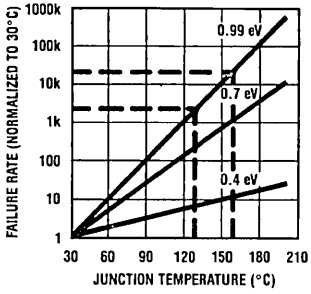

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All interface circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using interface components.

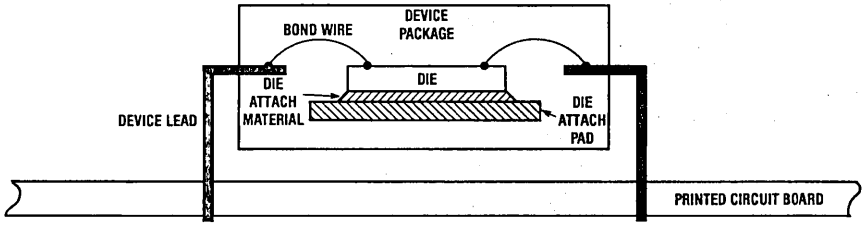

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

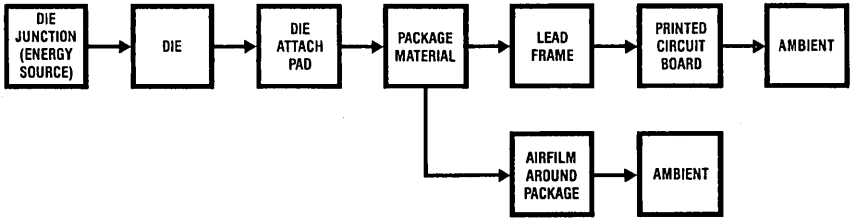

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, $T_A(max)$, the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

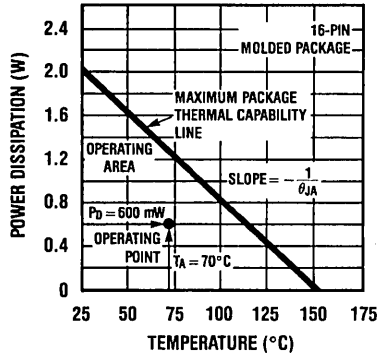

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all interface circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

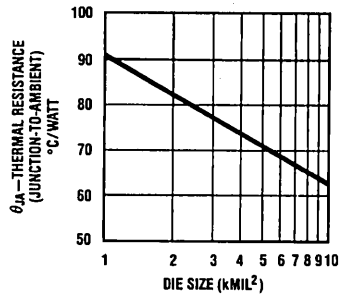

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 43 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

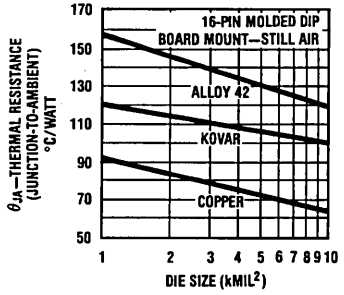

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

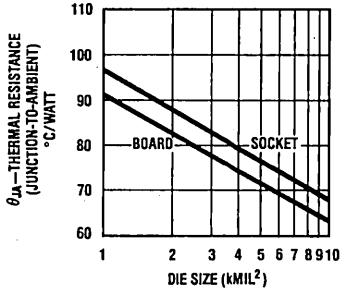

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

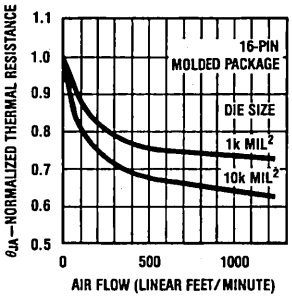

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Interface Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Interface Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the interface data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

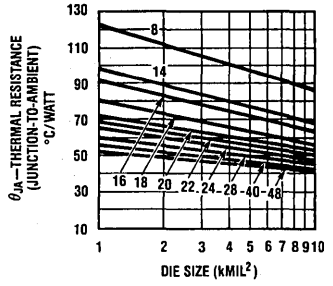
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D @ 70°C = 1476\ mW - (11.8\ mW/°C) \times (70°C - 25°C)$$
$$= 945\ mW$$

Molded (N Package) DIP* Copper Leadframe—HTP Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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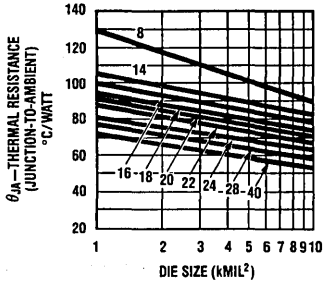
FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Cavity (J Package) DIP* Poly Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

TL/F/5280–11

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

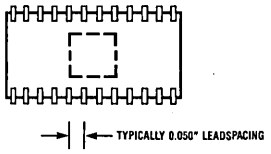
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliability

National Semiconductor
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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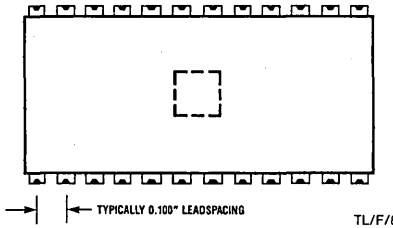
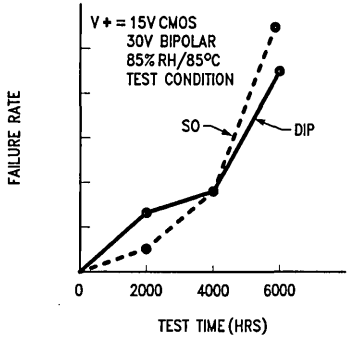
Standard DIP Package



TL/F/8766–2

Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.



TL/F/8766–3

FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

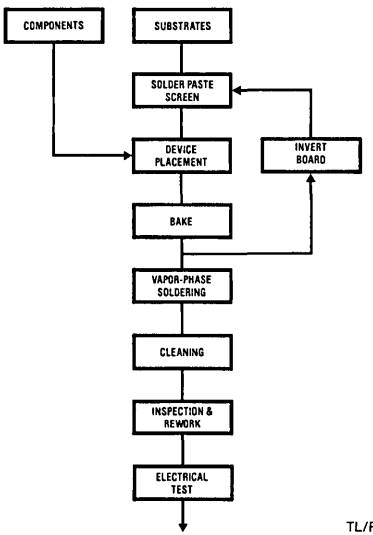
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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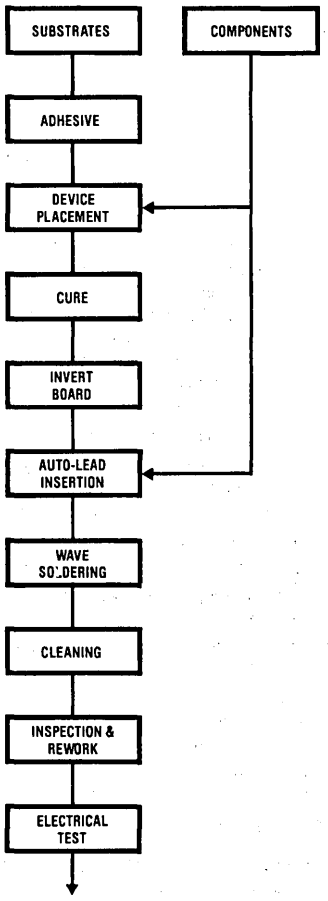
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

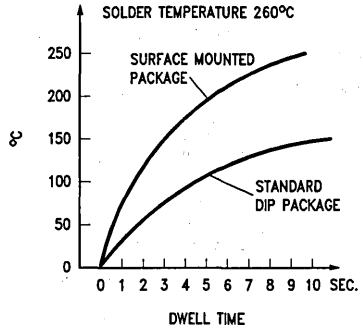

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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

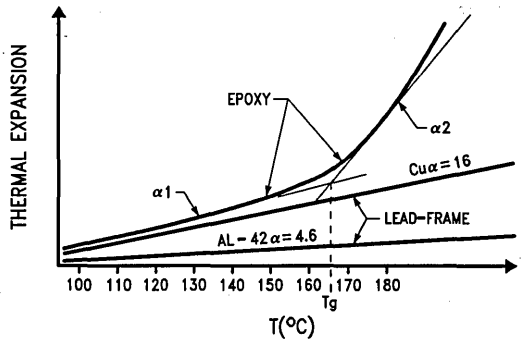

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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

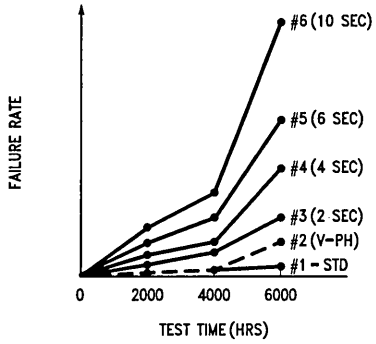

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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

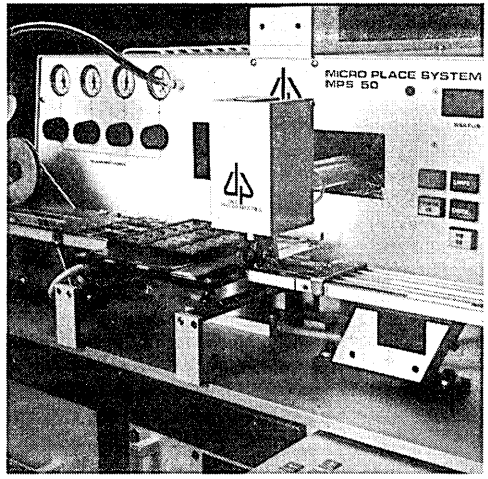
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

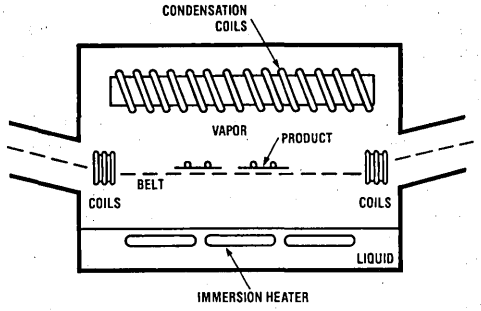
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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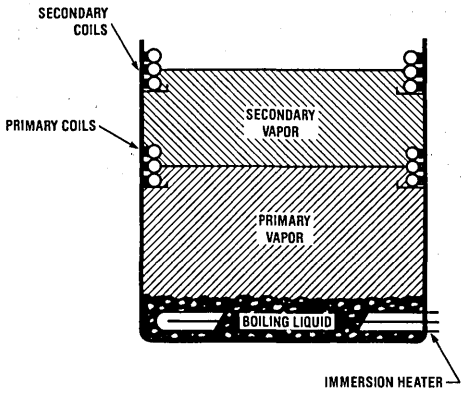
The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

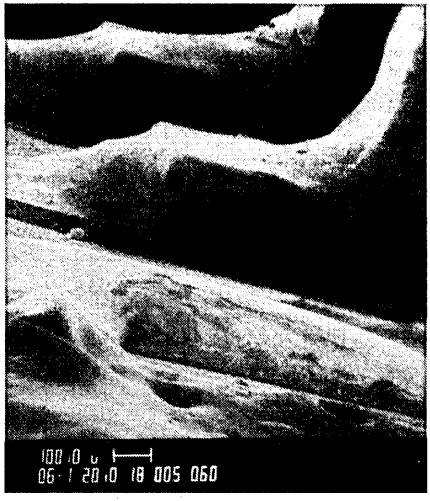
TL/F/8766–10

Batch-Fed Production Vapor-Phase Soldering Unit



TL/F/8766–11

Solder Joints on a SO-14 Package on PCB



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Solder Joints on a SO-14 Package on PCB

TL/F/8766–13

PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed $\frac{1}{8}$″, to avoid damage to screens and minimize distortion.

SOLDER PASTE

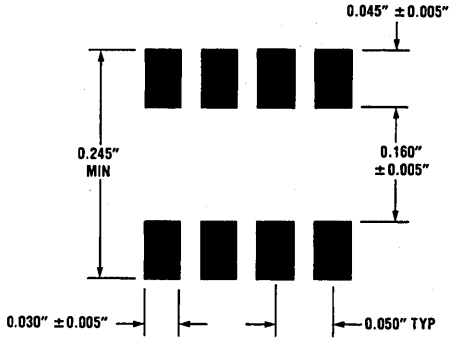
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



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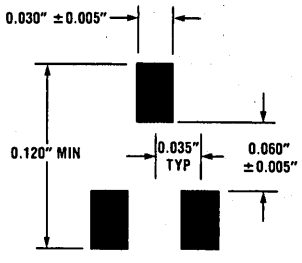
SOT-23



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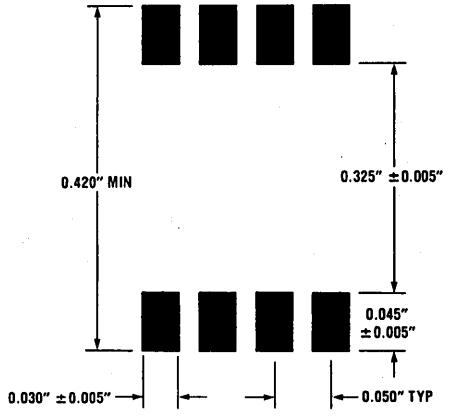
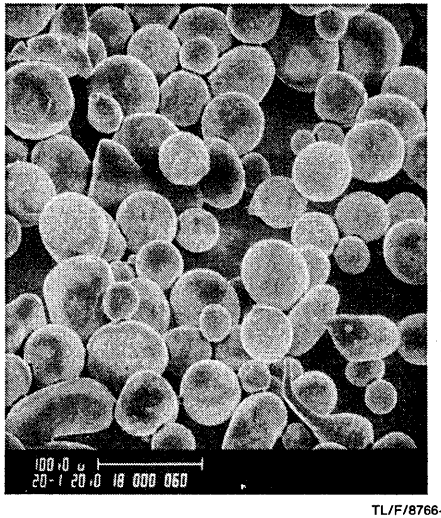
SO-16L, SO-20



TL/F/8766–15

Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



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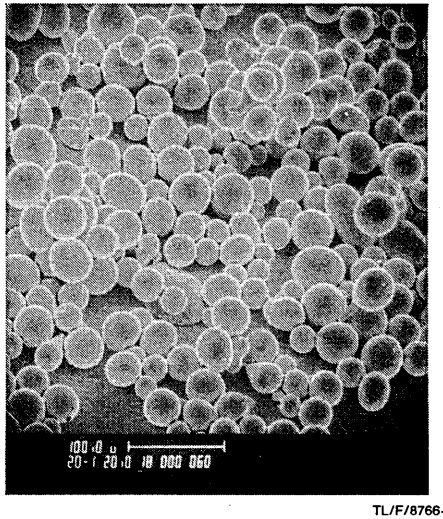
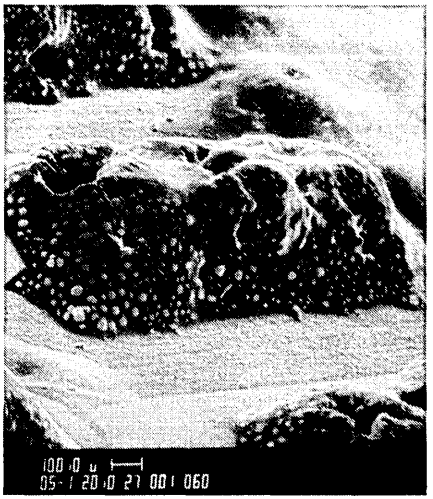
200 × Kester (63/37)



TL/F/8766–18

Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



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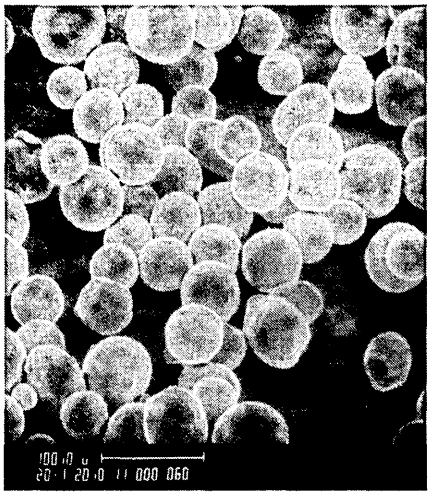
200 × Fry Metal (63/37)



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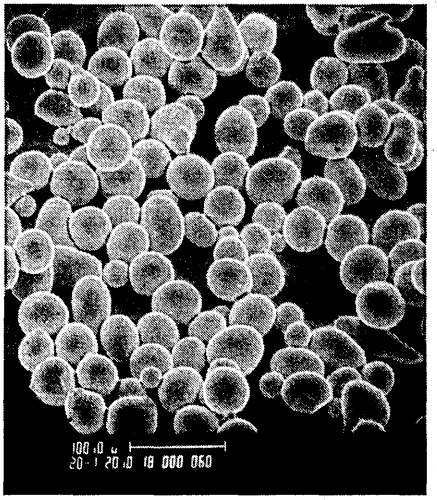
200 ESL (63/37)



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CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

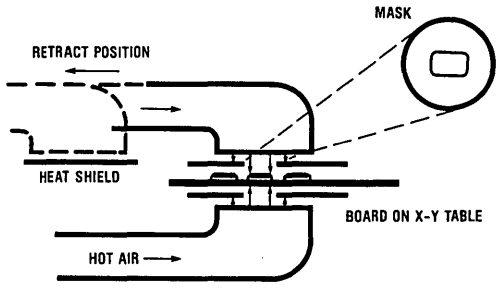
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



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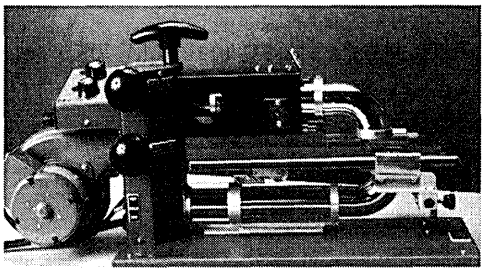
Hot-Air Rework Machine



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WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

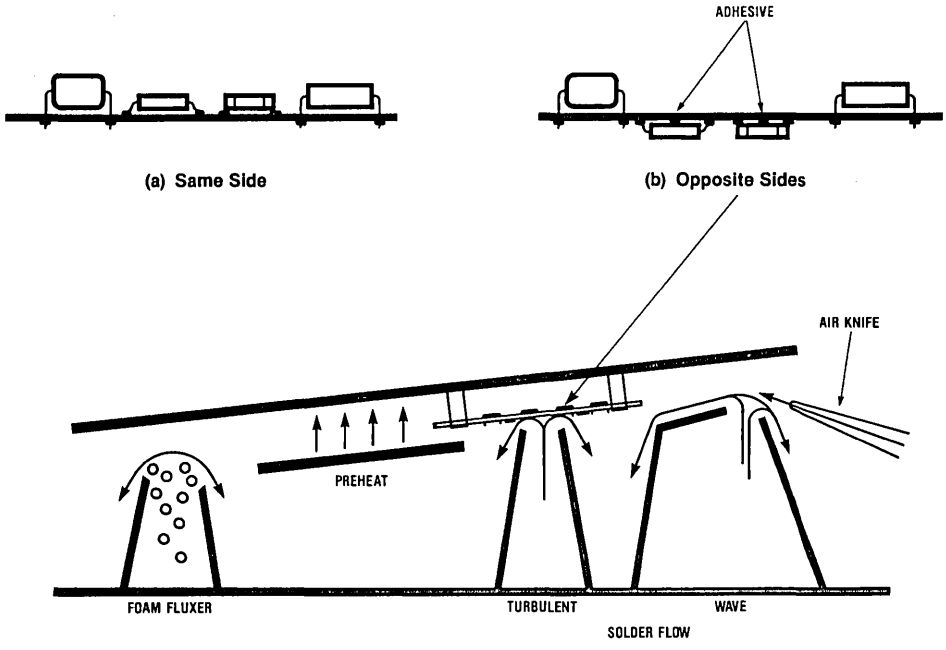
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050" vs 0.100" for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



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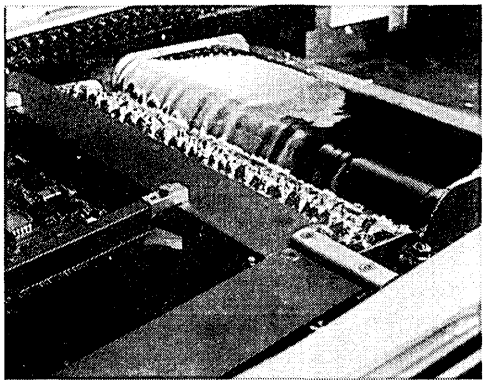
A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/F/8766–25

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

National Semiconductor

Data Transmission Products Nomenclature Revisions and Obsolescence Cross Reference Guide

The Data Transmission Products Nomenclature Revision and Obsolescence Cross Reference Guide is provided as an aid in identifying part numbers of products that have been revised or obsoleted.

The Nomenclature Table provides a list of old device designations vs new device designations for devices that have been revised or encountered name changes along with a respective comment.

The Obsolescence Cross Reference Guide provides a list of parts that have been discontinued recently. This includes device types, temperature grades, and or package options. Whenever possible a cross reference to a similar part is provided.

Before replacing a specific part, it is recommended to compare electrical, functional, and mechanical specifications as interchangeability for all applications is not guaranteed.

Nomenclature Revisions

Old Device Designation	New Device Designation	Comments
DS26C31C	DS26C31T	ESD Enhancement
DS26C32C	DS26C32AT	Name Change
DS26C32AC	DS26C32AT	ESD Enhancement
DS34C86	DS34C86T	ESD Enhancement
DS34C87	DS34C87T	ESD Enhancement
DS75176A	DS75176B	Name Change
DS75176AT	DS75176BT	Name Change
DS96F172	DS96F172C/M	Temp. Range Suffix Added
DS96F173	DS96F173C/M	Temp. Range Suffix Added
DS96F174	DS96F174C/M	Temp. Range Suffix Added
DS96F175	DS96F175C/M	Temp. Range Suffix Added

Obsolescence Cross Reference Guide

Obsolete NSID	Similar Device	Comments
DS1650		
DS3587	DS35F87	Different Process
DS3696AT	DS3696A	Com. Temp. Range Only
DS3696AT	DS3696T	DIP Package Only
DS55108	DS75108	Com. Temp. Range Only
DS55121	DS75121	Com. Temp. Range Only
DS75125		
DS75127		
DS75128		
DS8924		
DS8921T	DS8921AT	Enhanced AC Specs.
DS96F177	DS96177	
DS96F178		

National Semiconductor

National's A+ Program

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who need better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the repair and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connote identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population of faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction; the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

National's A+ Program (Continued)

Five Temperature Cycles (0°C to 100°C)

Exercising each device over a 100°C temperature range provides an additional die and package stress.

High Temperature (100°C)

Functional Electrical Test

A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C—15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing

Every device is tested at 25°C for functional and DC parameters.

Burn-In Test

Each device is burned-in for 160 hours at a minimum junction temperature of +125°C or under equivalent conditions of time and temperature, as established by a time-temperature regression curve based on 0.96 eV activation energy (i.e., 23 hours at +155°C). All burn-in done under steady-state conditions unless otherwise specified.

DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-Than-Normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

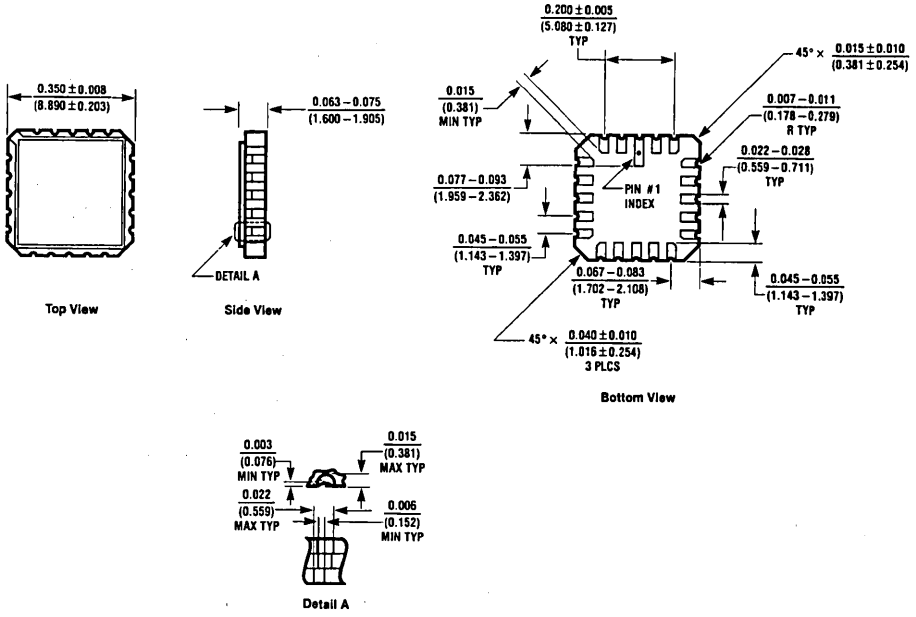
Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

National Semiconductor

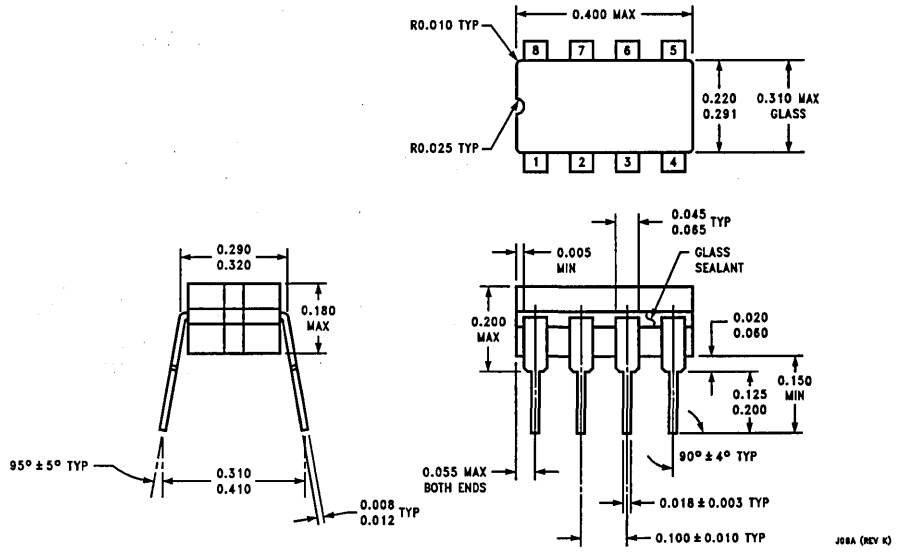
All dimensions are in inches (millimeters)

20 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E20A



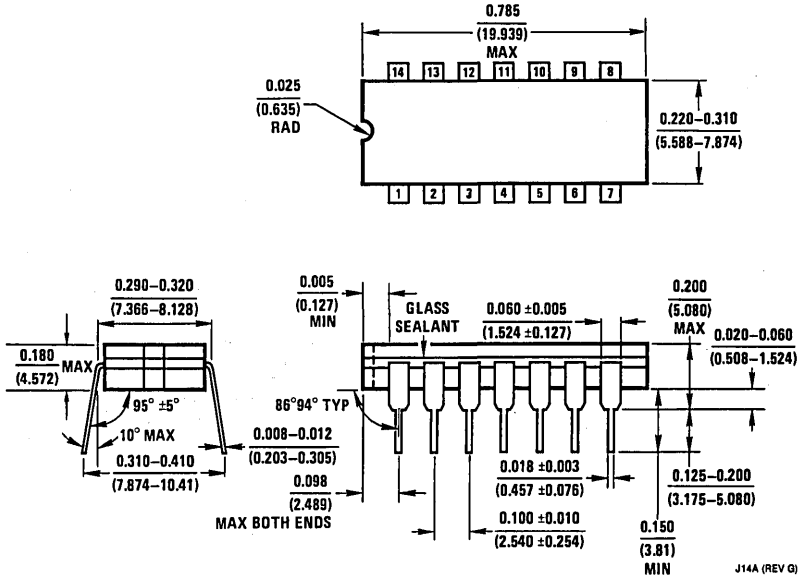
E20A (REV D)

8 Lead Ceramic Dual-in-Line Package
NS Package Number J08A

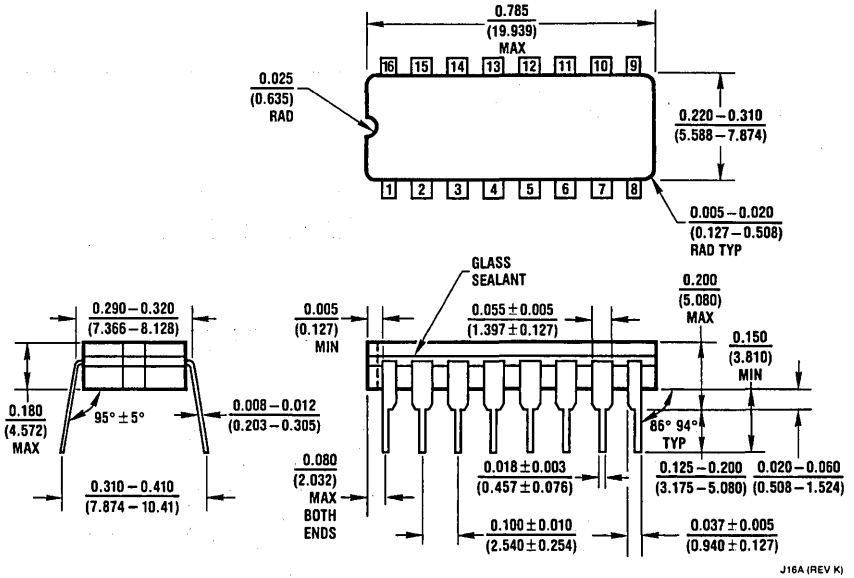


J08A (REV K)

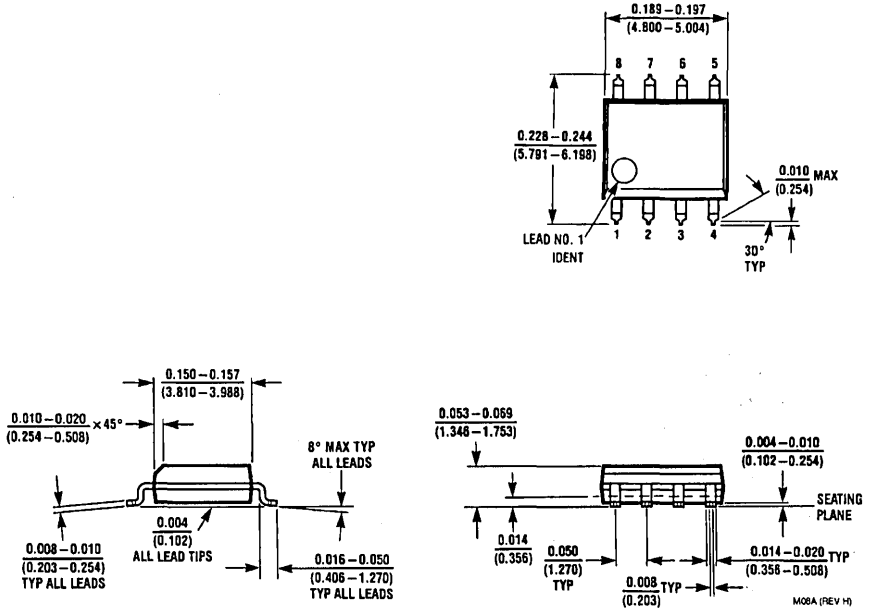
14 Lead Ceramic Dual-in-Line Package
NS Package Number J14A



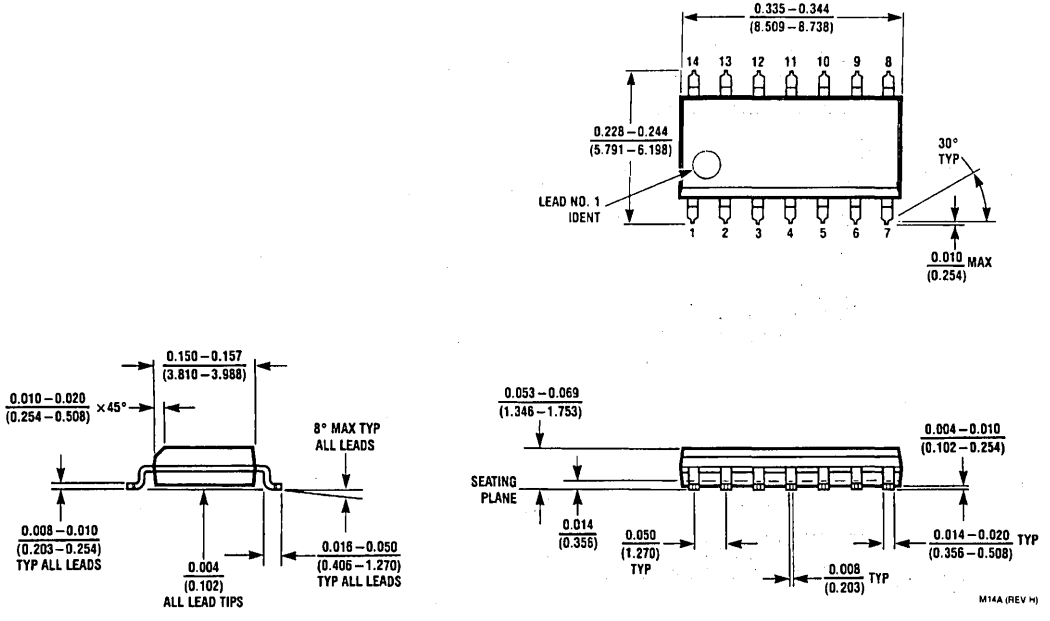
16 Lead Ceramic Dual-in-Line Package
NS Package Number J16A



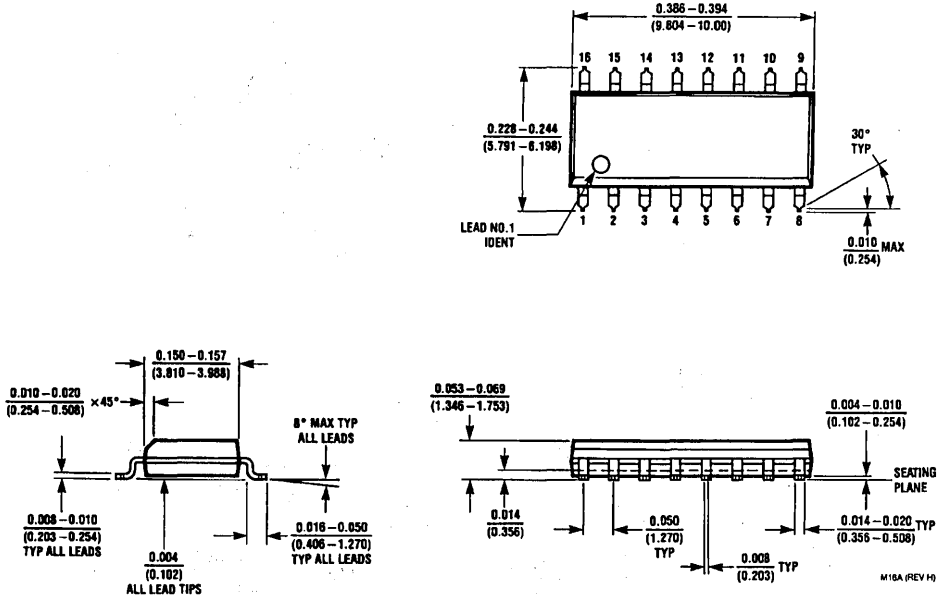
8 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M08A



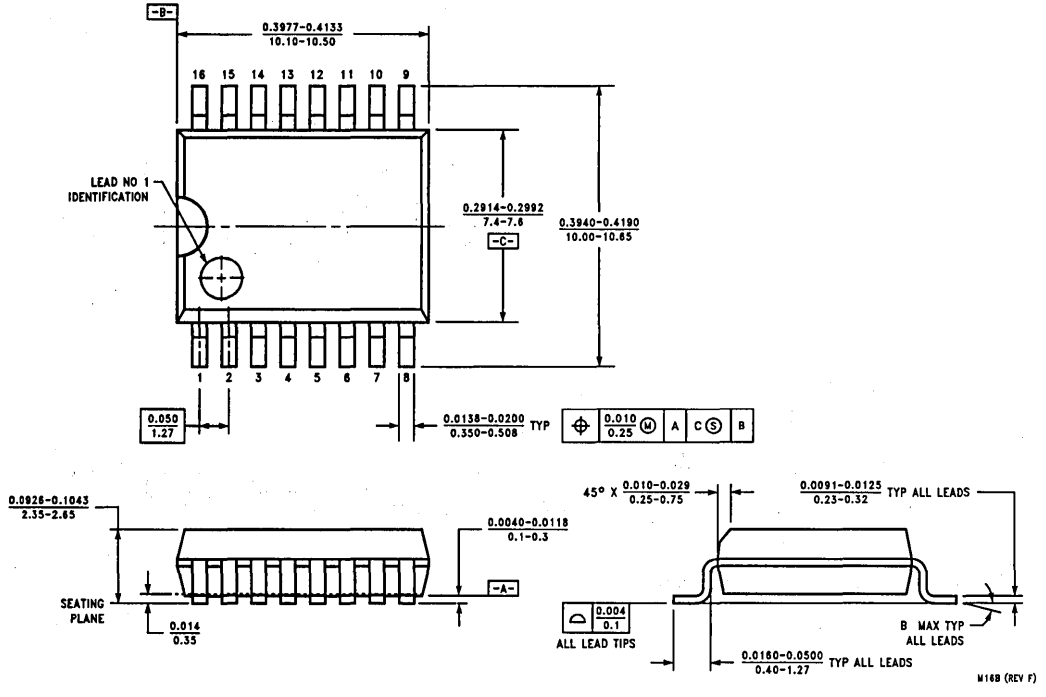
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14A



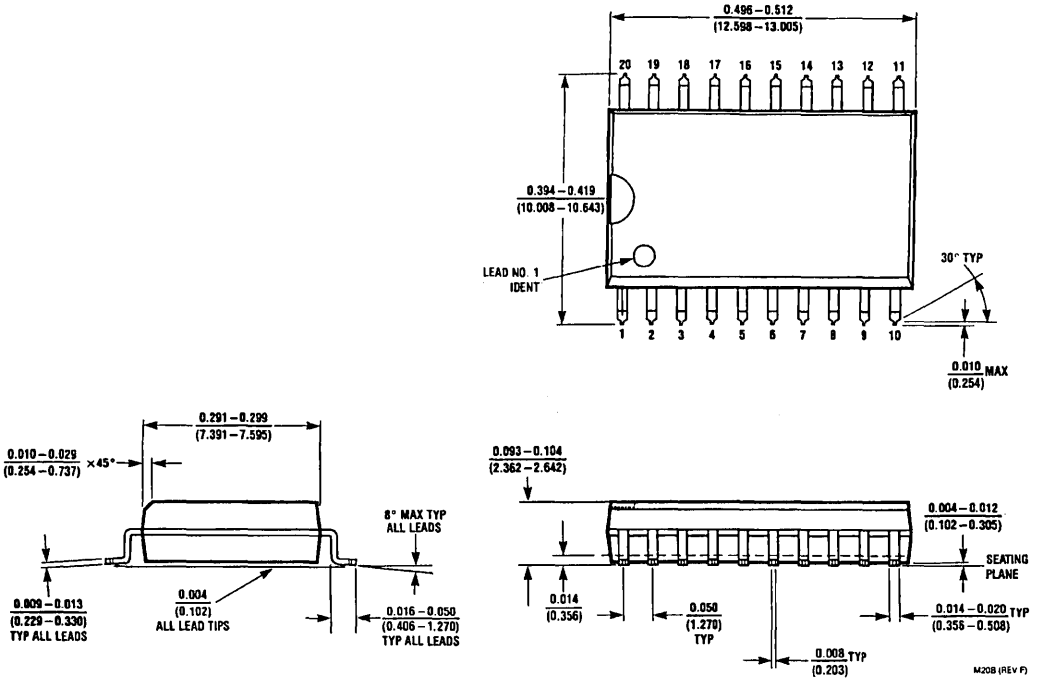
16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A



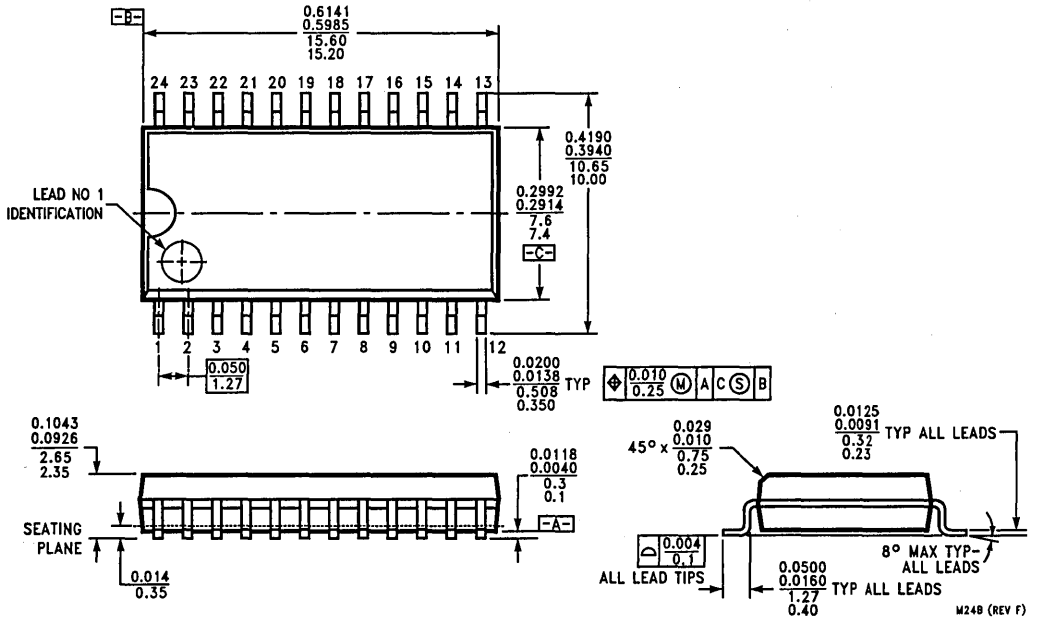
16 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16B



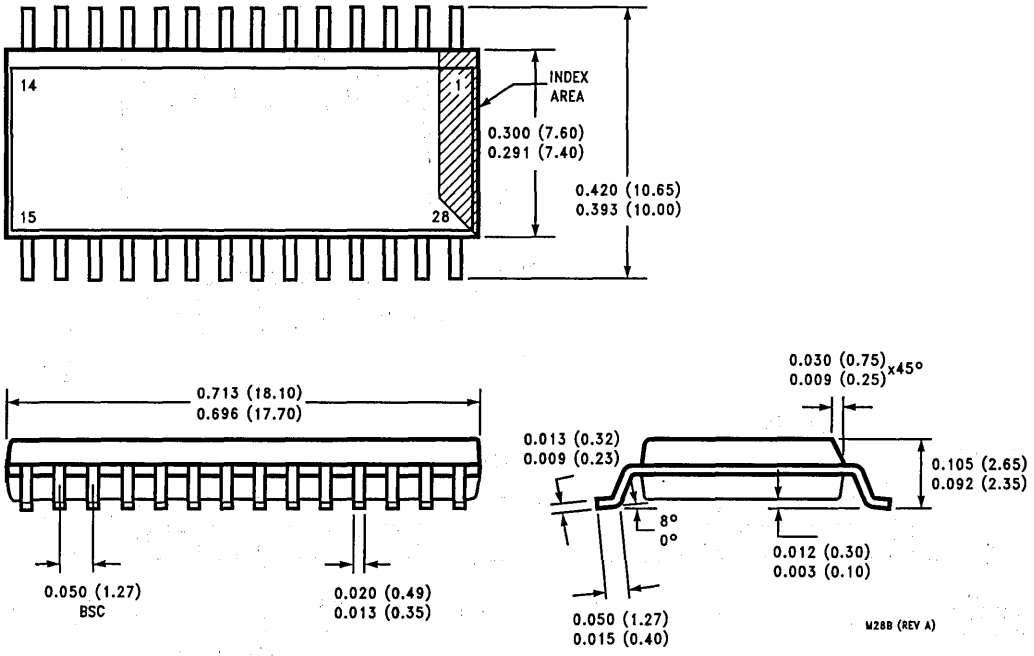
20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B



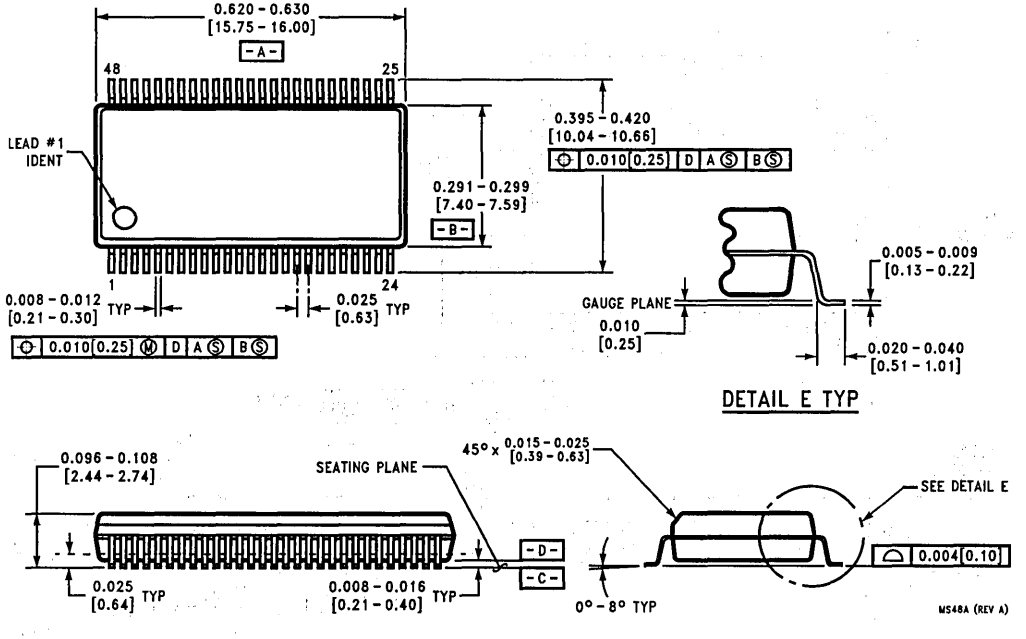
24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M24B



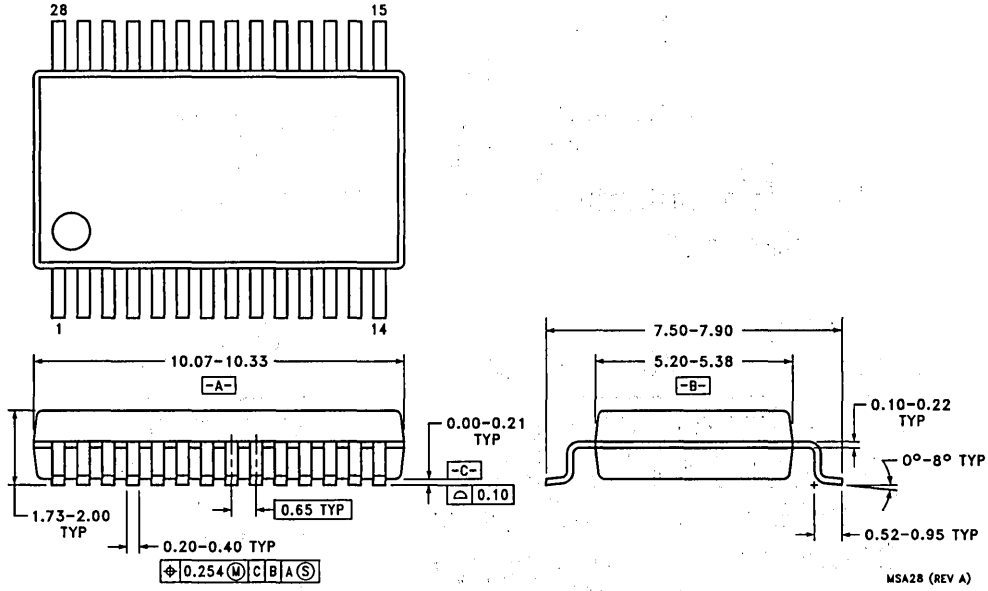
28 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M28B



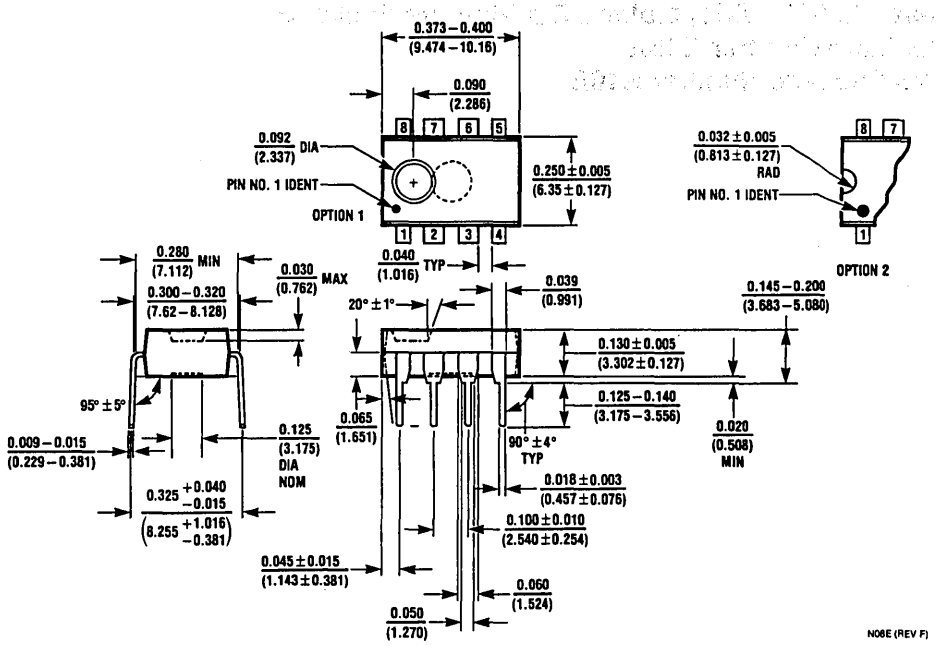
48 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS48A



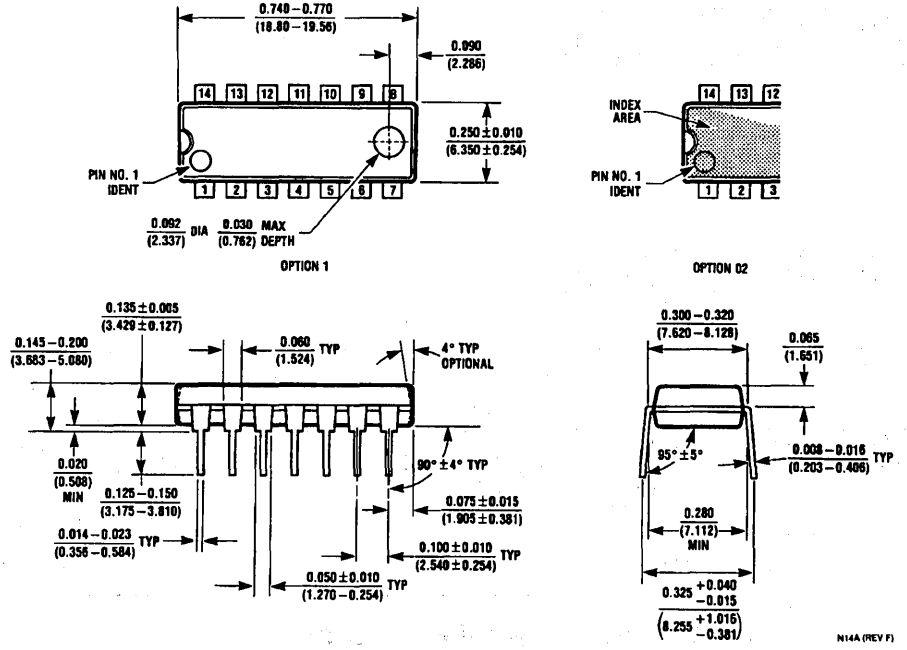
28 Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA28



8 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N08E

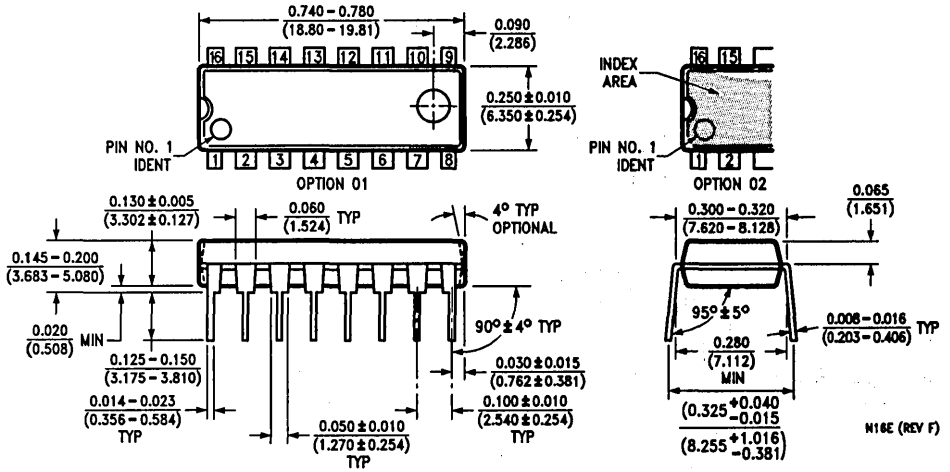


14 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N14A

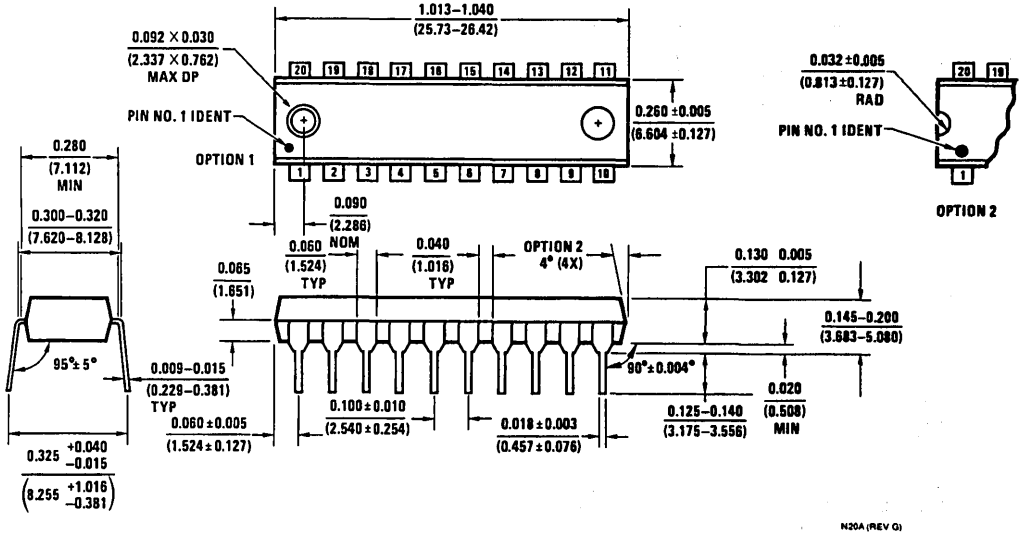


16 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N16A
See NS Package Number N16E

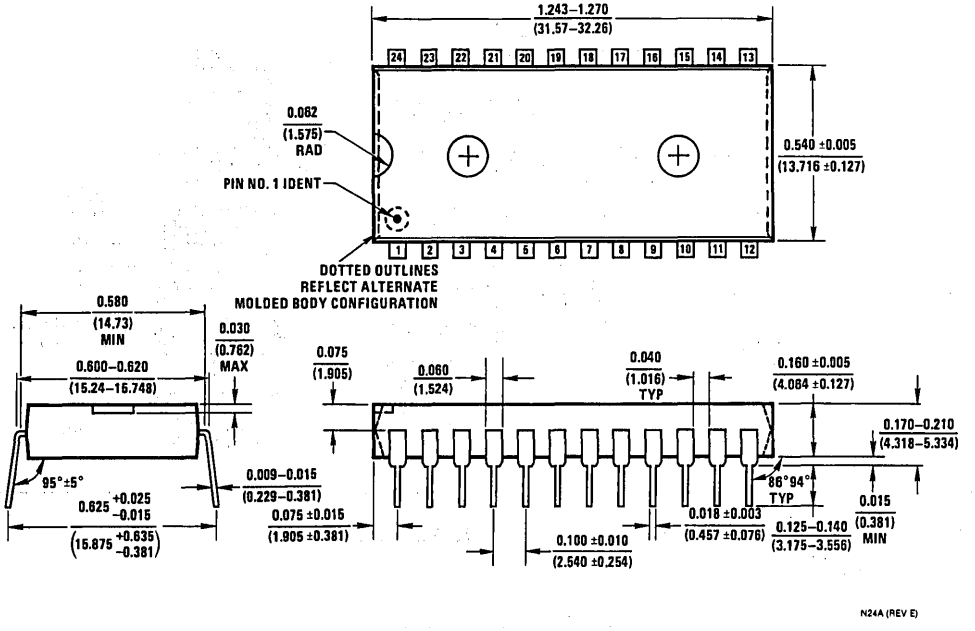
16 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N16E



20 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N20A

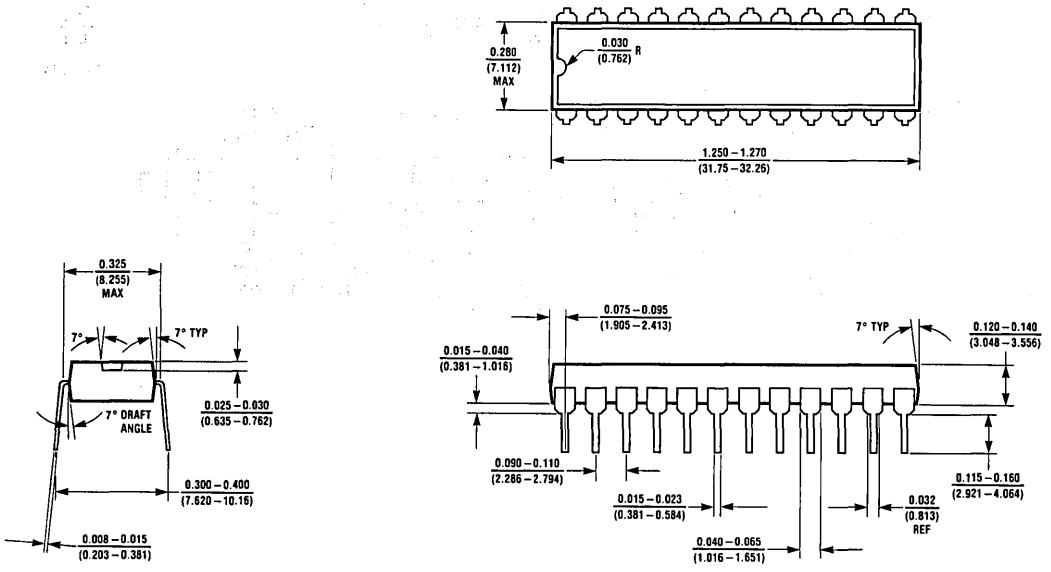


24 Lead (0.600″ Wide) Molded Dual-in-Line Package
NS Package Number N24A



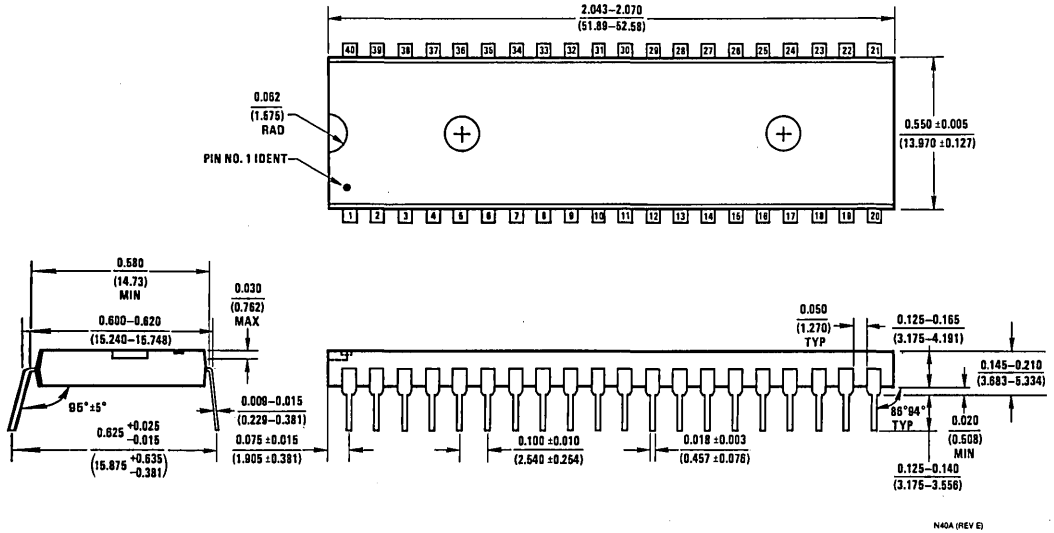
N24A (REV E)

24 Lead (0.300″ Wide) Molded Dual-in-Line Package
NS Package Number N24D

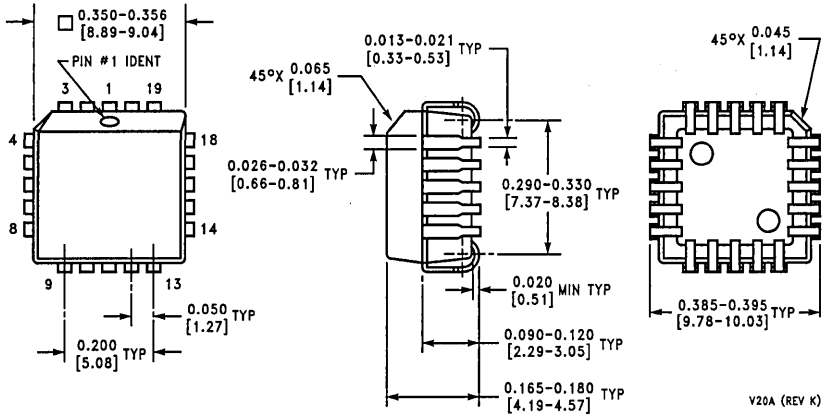


N24D (REV D)

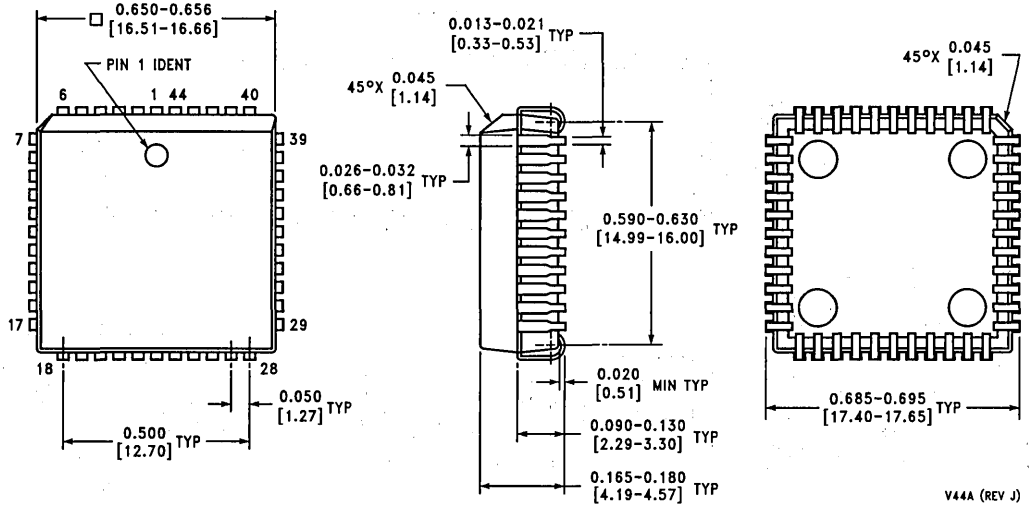
40 Lead (0.600" Wide) Molded Dual-in-Line Package
NS Package Number N40A



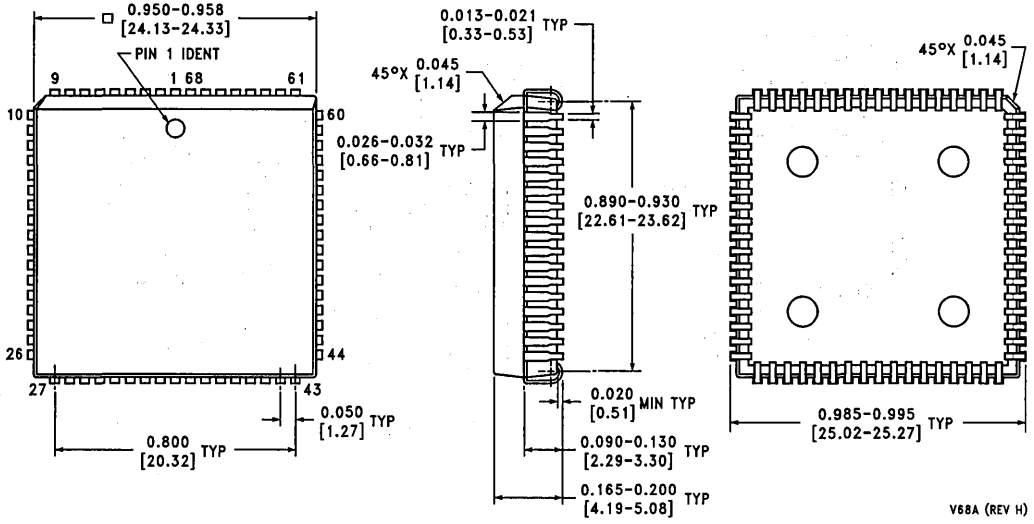
20 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V20A



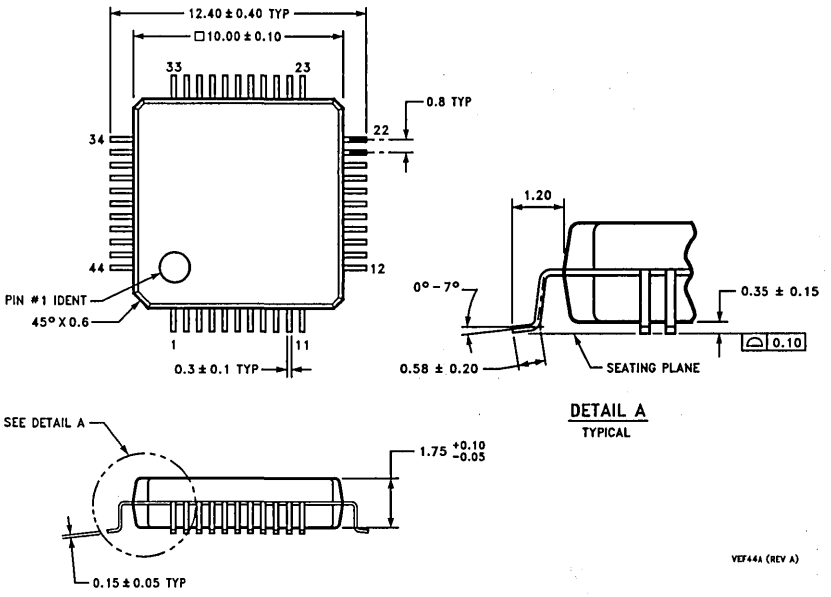
44 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V44A



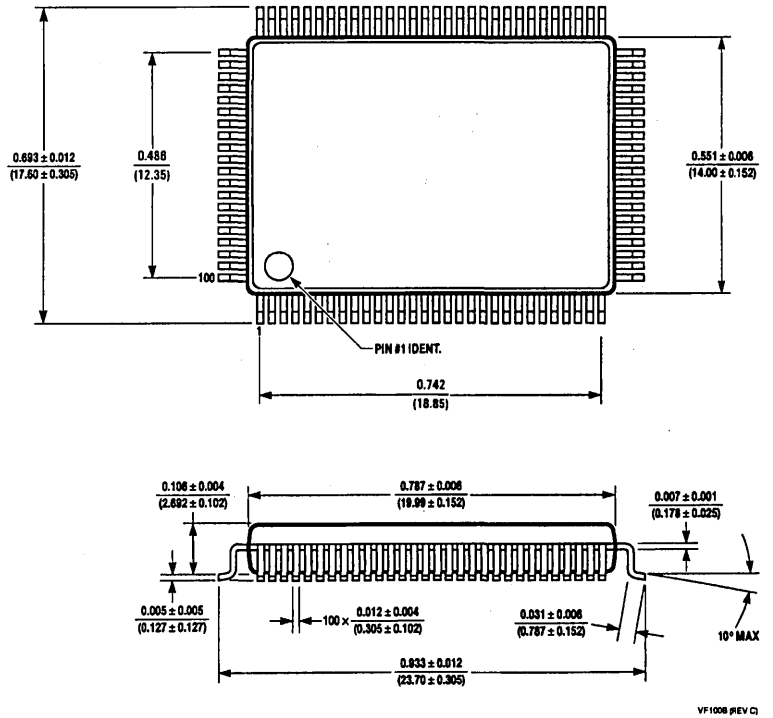
68 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V68A



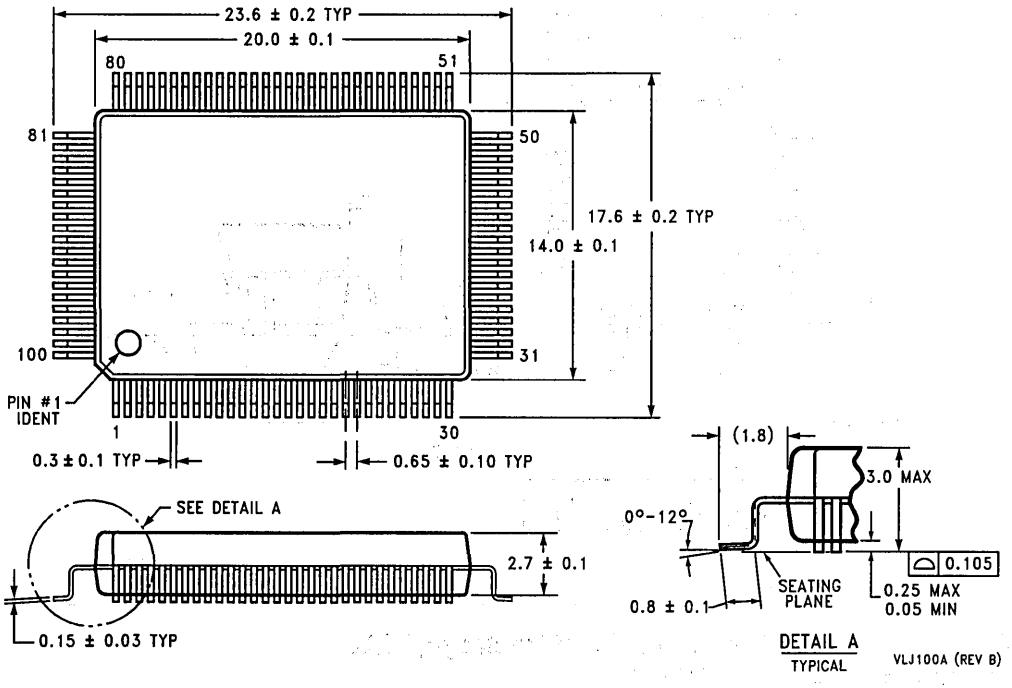
44 Lead (10mm x 10mm) Molded Plastic Quad Flat Package, EIAJ
NS Package Number VEF44A



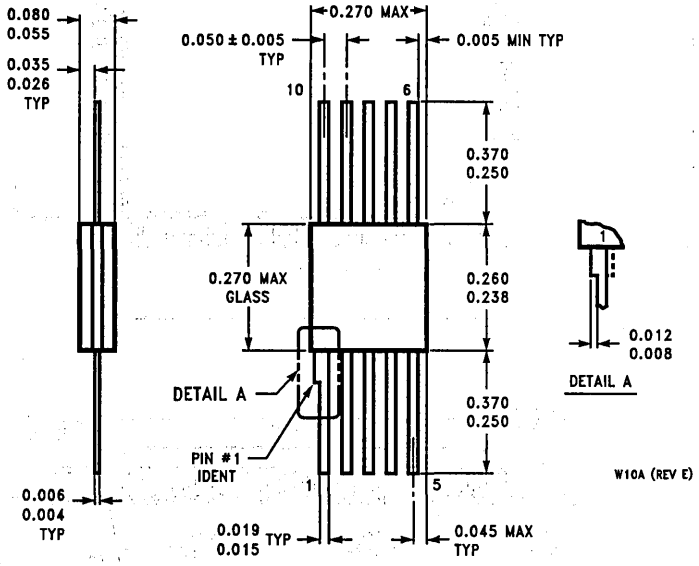
100 Lead Molded Plastic Quad Flat Package, EIAJ
NS Package Number VF100B



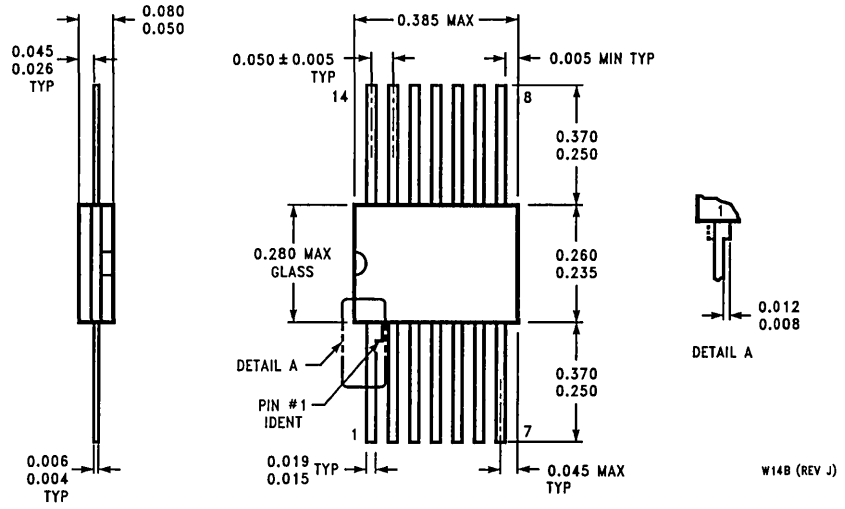
100 Lead (14mm x 20mm) Molded Plastic Quad Flat Package, EIAJ
NS Package Number VLJ100A



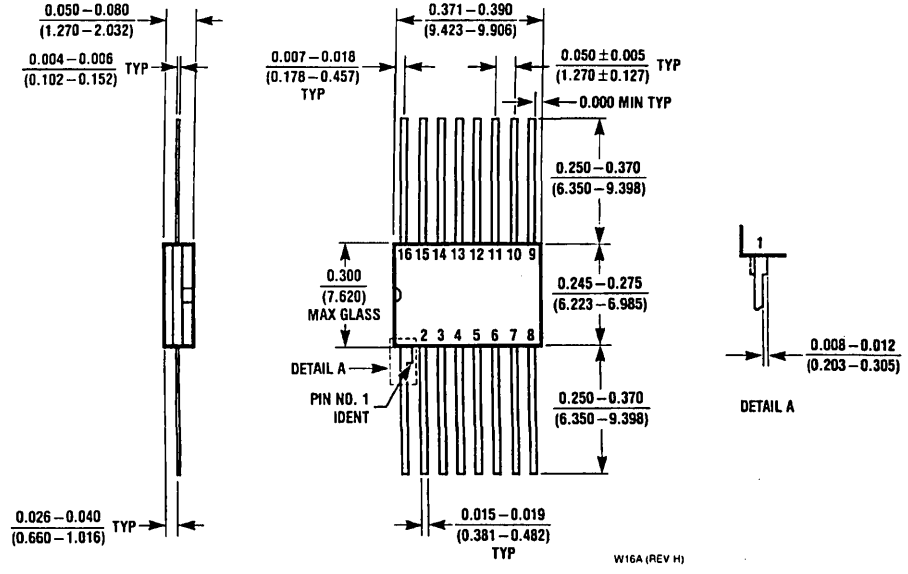
10 Lead Cerpack
NS Package Number W10A



14 Lead Cerpack
NS Package Number W14B



16 Lead Cerpack
NS Package Number W16A



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Bookshelf of Technical Support Information

National Semiconductor Corporation recognizes the need to keep you informed about the availability of current technical literature.

This bookshelf is a compilation of books that are currently available. The listing that follows shows the publication year and section contents for each book.

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ADVANCED BiCMOS LOGIC (ABTC, IBF, BCT) DATABOOK—1993

ABTC/BCT Description and Family Characteristics • ABTC/BCT Ratings, Specifications and Waveforms
ABTC Applications and Design Considerations • Quality and Reliability • Integrated Bus Function (IBF) Introduction
54/74ABT3283 Synchronous Datapath Multiplexer • 74FR900/25900 9-Bit 3-Port Latchable Datapath Multiplexer
54/74ACTQ3283 32-Bit Latchable Transceiver with Parity Generator/Checker and Byte Multiplexing
54/74ABTCXXX • 74BCTXXX

ALS/AS LOGIC DATABOOK—1990

Introduction to Advanced Bipolar Logic • Advanced Low Power Schottky • Advanced Schottky

ASIC DESIGN MANUAL/GATE ARRAYS & STANDARD CELLS—1987

SSI/MSI Functions • Peripheral Functions • LSI/VLSI Functions • Design Guidelines • Packaging

CMOS LOGIC DATABOOK—1988

CMOS AC Switching Test Circuits and Timing Waveforms • CMOS Application Notes • MM54HC/MM74HC
MM54HCT/MM74HCT • CD4XXX • MM54CXXX/MM74CXXX • Surface Mount

CLOCK GENERATION AND SUPPORT (CGS) DESIGN DATABOOK—1994

Low Skew Clock Buffers/Drivers • Video Clock Generators • Low Skew PLL Clock Generators
Crystal Clock Generators

DATA ACQUISITION DATABOOK—1993

Data Acquisition Systems • Analog-to-Digital Converters • Digital-to-Analog Converters • Voltage References
Temperature Sensors • Active Filters • Analog Switches/Multiplexers • Surface Mount

DATA ACQUISITION DATABOOK SUPPLEMENT—1992

New devices released since the printing of the 1989 Data Acquisition Linear Devices Databook.

DISCRETE SEMICONDUCTOR PRODUCTS DATABOOK—1989

Selection Guide and Cross Reference Guides • Diodes • Bipolar NPN Transistors
Bipolar PNP Transistors • JFET Transistors • Surface Mount Products • Pro-Electron Series
Consumer Series • Power Components • Transistor Datasheets • Process Characteristics

DRAM MANAGEMENT HANDBOOK—1993

Dynamic Memory Control • CPU Specific System Solutions • Error Detection and Correction
Microprocessor Applications

EMBEDDED CONTROLLERS DATABOOK—1992

COP400 Family • COP800 Family • COPS Applications • HPC Family • HPC Applications
MICROWIRE and MICROWIRE/PLUS Peripherals • Microcontroller Development Tools

FDDI DATABOOK—1991

FDDI Overview • DP83200 FDDI Chip Set • Development Support • Application Notes and System Briefs

F100K ECL LOGIC DATABOOK & DESIGN GUIDE—1992

Family Overview • 300 Series (Low-Power) Datasheets • 100 Series Datasheets • 11C Datasheets
Design Guide • Circuit Basics • Logic Design • Transmission Line Concepts • System Considerations
Power Distribution and Thermal Considerations • Testing Techniques • 300 Series Package Qualification
Quality Assurance and Reliability • Application Notes

FACT™ ADVANCED CMOS LOGIC DATABOOK—1993

Description and Family Characteristics • Ratings, Specifications and Waveforms
Design Considerations • 54AC/74ACXXX • 54ACT/74ACTXXX • Quiet Series: 54ACQ/74ACQXXX
Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA/B

FAST® ADVANCED SCHOTTKY TTL LOGIC DATABOOK—1990

Circuit Characteristics • Ratings, Specifications and Waveforms • Design Considerations • 54F/74FXXX

FAST® APPLICATIONS HANDBOOK—1990

Reprint of 1987 Fairchild FAST Applications Handbook
Contains application information on the FAST family: Introduction • Multiplexers • Decoders • Encoders
Operators • FIFOs • Counters • TTL Small Scale Integration • Line Driving and System Design
FAST Characteristics and Testing • Packaging Characteristics

HIGH-PERFORMANCE BUS INTERFACE DESIGNER'S GUIDE—1992

Futurebus+ /BTL Devices • BTL Transceiver Application Notes • Futurebus+ Application Notes
High Performance TTL Bus Drivers • PI-Bus • Futurebus+ /BTL Reference

IBM DATA COMMUNICATIONS HANDBOOK—1992

IBM Data Communications • Application Notes

INTERFACE: DATA TRANSMISSION DATABOOK—1994

TIA/EIA-232 (RS-232) • TIA/EIA-422/423 • TIA/EIA-485 • Line Drivers • Receivers • Repeaters
Transceivers • Low Voltage Differential Signaling • Special Interface • Application Notes

LINEAR APPLICATIONS HANDBOOK—1994

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

LINEAR APPLICATION SPECIFIC IC's DATABOOK—1993

Audio Circuits • Radio Circuits • Video Circuits • Display Drivers • Clock Drivers • Frequency Synthesis
Special Automotive • Special Functions • Surface Mount

LOCAL AREA NETWORKS DATABOOK—1993 SECOND EDITION

Integrated Ethernet Network Interface Controller Products • Ethernet Physical Layer Transceivers
Ethernet Repeater Interface Controller Products • Token-Ring Interface Controller (TROPIC)
Hardware and Software Support Products • FDDI Products • Glossary and Acronyms

LOW VOLTAGE DATABOOK—1992

This databook contains information on National's expanding portfolio of low and extended voltage products. Product datasheets included for: Low Voltage Logic (LVQ), Linear, EPROM, EEPROM, SRAM, Interface, ASIC, Embedded Controllers, Real Time Clocks, and Clock Generation and Support (CGS).

MASS STORAGE HANDBOOK—1989

Rigid Disk Pulse Detectors • Rigid Disk Data Separators/Synchronizers and ENDECs
Rigid Disk Data Controller • SCSI Bus Interface Circuits • Floppy Disk Controllers • Disk Drive Interface Circuits
Rigid Disk Preamplifiers and Servo Control Circuits • Rigid Disk Microcontroller Circuits • Disk Interface Design Guide

MEMORY DATABOOK—1992

CMOS EPROMs • CMOS EEPROMs • PROMs • Application Notes

MEMORY APPLICATION HANDBOOK—1993

OPERATIONAL AMPLIFIERS DATABOOK—1993

Operational Amplifiers • Buffers • Voltage Comparators • Instrumentation Amplifiers • Surface Mount

PACKAGING DATABOOK—1993

Introduction to Packaging • Hermetic Packages • Plastic Packages • Advanced Packaging Technology
Package Reliability Considerations • Packing Considerations • Surface Mount Considerations

POWER IC's DATABOOK—1993

Linear Voltage Regulators • Low Dropout Voltage Regulators • Switching Voltage Regulators • Motion Control
Peripheral Drivers • High Current Switches • Surface Mount

PROGRAMMABLE LOGIC DEVICE DATABOOK AND DESIGN GUIDE—1993

Product Line Overview • Datasheets • Design Guide: Designing with PLDs • PLD Design Methodology
PLD Design Development Tools • Fabrication of Programmable Logic • Application Examples

REAL TIME CLOCK HANDBOOK—1993

3-Volt Low Voltage Real Time Clocks • Real Time Clocks and Timer Clock Peripherals • Application Notes

RELIABILITY HANDBOOK—1987

Reliability and the Die • Internal Construction • Finished Package • MIL-STD-883 • MIL-M-38510
The Specification Development Process • Reliability and the Hybrid Device • VLSI/VHSIC Devices
Radiation Environment • Electrostatic Discharge • Discrete Device • Standardization
Quality Assurance and Reliability Engineering • Reliability and Documentation • Commercial Grade Device
European Reliability Programs • Reliability and the Cost of Semiconductor Ownership
Reliability Testing at National Semiconductor • The Total Military/Aerospace Standardization Program
883B/RETS™ Products • MILS/RETS™ Products • 883/RETS™ Hybrids • MIL-M-38510 Class B Products
Radiation Hardened Technology • Wafer Fabrication • Semiconductor Assembly and Packaging
Semiconductor Packages • Glossary of Terms • Key Government Agencies • AN/ Numbers and Acronyms
Bibliography • MIL-M-38510 and DESC Drawing Cross Listing

SCAN™ DATABOOK—1993

Evolution of IEEE 1149.1 Standard • SCAN Buffers • System Test Products • Other IEEE 1149.1 Devices

TELECOMMUNICATIONS—1992

COMBO and SLIC Devices • ISDN • Digital Loop Devices • Analog Telephone Components • Software
Application Notes

VHC/VHCT ADVANCED CMOS LOGIC DATABOOK—1993

This databook introduces National's Very High Speed CMOS (VHC) and Very High Speed TTL Compatible CMOS (VHCT) designs. The databook includes Description and Family Characteristics • Ratings, Specifications and Waveforms Design Considerations and Product Datasheets. The topics discussed are the advantages of VHC/VHCT AC Performance, Low Noise Characteristics and Improved Interface Capabilities.

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