400019

National Semiconductor

FACT™ Advanced CMOS Logic Databook

Includes New Quiet Series™ and FCT/FCTA Product Information

FACT™ Advanced CMOS Logic Databook

1990

National Semiconductor

FACT
DATABOOK

1990 Edition

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Introduction

FACT™ (Fairchild Advanced CMOS Technology) is a very high-speed, low power CMOS Logic family utilizing a 1.3 μM Isoplanar silicon gate CMOS process. FACT logic functions can attain speeds similar to that of Advanced Low Power Schottky while retaining the advantages of CMOS logic: Ultra low static power and high noise immunity. FACT offers the system designer the added benefit of superior line driving characteristics and excellent ESD and Latch-up immunity.

FACT Quiet Series, an extension of the FACT family, is a high speed, low power CMOS family IDEAL for ACMOS applications requiring increased noise margins. Utilizing NSC Quiet Series Technology, FACT QS features GTO™ outputs control, undershoot corrector and a split ground bus for superior ACMOS performance. In addition, FACT QS features improved AC specifications, specifies maximum pin-to-pin output skew and provides enhanced ESD immunity and latch-up protection.

FACT FCT, an extension of the FACT family, features 7 ns propagation delays and 64/48 mA output drive. The series incorporates National's Quiet Series Technology to provide the lowest noise performance of any FCT logic family. FACT FCTA is the high speed, high drive extension of the FACT family featuring 5 ns maximum propagation delays and 64/48 mA output drive. In addition, FACT FCTA features quiet circuitry to provide increased noise margins.

The FACT/FACT QS families consist of devices in two categories:

1. AC/ACQ—standard logic functions with CMOS compatible inputs and TTL and MOS compatible outputs;
2. ACT/ACTQ—standard logic functions with TTL compatible inputs and TTL and MOS compatible outputs.

Product Index and Selection Guide

Lists FACT, FACT QS, FACT FCT, and FACT FCTA circuits currently available, in design or planned. The selection guide groups the circuits by function.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

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FACT™ Selection Guide

Gates

Function	Device
NAND	
Quad 2-Input	54AC/74AC00
Quad 2-Input	54ACT/74ACT00
Triple 3-Input	54AC/74AC10
Triple 3-Input	54ACT/74ACT10
Dual 4-Input	54AC/74AC20
AND	
Quad 2-Input	54AC/74AC08
Quad 2-Input	54ACT/74ACT08
Triple 3-Input	54AC/74AC11
OR/NOR/Exclusive-OR	
Quad 2-Input OR	54AC/74AC32
Quad 2-Input OR	54ACT/74ACT32
Quad 2-Input NOR	54AC/74AC02
Quad 2-Input NOR	54ACT/74ACT02
Quad 2-Input Exclusive-OR	54AC/74AC86
Inverter	
Hex Inverter	54AC/74AC04
Hex Inverter	54ACT/74ACT04
Hex Schmitt Trigger Inverter	54AC/74AC14

Registers

Function	Device	Clock Inputs
Parallel D Register w/Enable	54AC/74AC378	No
Quad 2-Port Register	54ACT/74ACT399	1(⌐)
Diagnostic and Pipeline Register	54ACT/74ACT818	2

Parity Generator/Checkers

Function	Device
Parity Generator/Checker	54AC/74AC280
Octal Bidirectional Bus Transceiver w/Parity Generator/Checker	54ACTQ/74ACTQ657
Octal Bidirectional Bus Transceiver w/Parity Generator/Checker	54FCT/74FCT657
9-Bit Registered Transceiver w/Parity Generator/Checker	54AC/74AC899
9-Bit Registered Transceiver w/Parity Generator/Checker	54ACT/74ACT899
9-Bit Registered Transceiver w/Parity Generator/Checker	54FCT/74FCT899

Flip-Flops

Function	Device	TRI-STATE® Outputs	Master Reset
Dual D	54AC/74AC74	No	Yes
Dual D	54ACT/74ACT74	No	Yes
Dual J$\overline{K}$	54AC/74AC109	No	Yes
Dual J$\overline{K}$	54ACT/74ACT109	No	Yes
Hex D	54AC/74AC174	No	Yes
Hex D	54ACT/74ACT174	No	Yes
Quad D	54AC/74AC175	No	Yes
Quad D	54ACT/74ACT175	No	Yes
Octal D	54AC/74AC273	No	Yes
Octal D	54ACT/74ACTQ273	No	Yes
Octal D	54FCT/74FCT273	No	Yes
Octal D	54FCT/74FCT273A	No	Yes
Octal D	54AC/74AC374	Yes	No
Octal D	54ACT/74ACT374	Yes	No
Octal D	54ACQ/74ACQ374	Yes	No
Octal D	54ACTQ/74ACTQ374	Yes	No
Octal D	54FCT/74FCT374	Yes	No
Octal D	54FCT/74FCT374A	Yes	No
Octal D	54AC/74AC377	No	No
Octal D	54ACT/74ACT377	No	No
Octal D	54ACQ/74ACQ377	No	No
Octal D	54ACTQ/74ACTQ377	No	No
Octal D	54FCT/74FCT377	No	No
Octal D	54FCT/74FCT377A	No	No
Octal D	54ACT/74ACT534	Yes	No
Octal D	54ACQ/74ACQ534	Yes	No
Octal D	54ACTQ/74ACTQ534	Yes	No
Octal D	54FCT/74FCT534	Yes	No
Octal D	54FCT/74FCT534A	Yes	No
Octal D	54ACT/74ACT564	Yes	No
Octal D	54ACQ/74ACQ564	Yes	No
Octal D	54ACTQ/74ACTQ564	Yes	No
Octal D	54FCT/74FCT564	Yes	No
Octal D	54FCT/74FCT564A	Yes	No
Octal D	54AC/74AC574	Yes	No
Octal D	54ACT/74ACT574	Yes	No
Octal D	54ACQ/74ACQ574	Yes	No
Octal D	54ACTQ/74ACTQ574	Yes	No
Octal D	54FCT/74FCT574	Yes	No
Octal D	54FCT/74FCT574A	Yes	No
Octal D	54ACT/74ACT825	Yes	Yes
8-Bit D	54FCT/74FCT825A/B	Yes	Yes
9-Bit D	54ACT/74ACT823	Yes	Yes
9-Bit D	54FCT/74FCT823A/B	Yes	Yes
10-Bit D	54ACT/74ACT821	Yes	Yes
10-Bit D	54ACQ/74ACQ821	Yes	Yes
10-Bit D	54FCT/74FCT821A/B	Yes	Yes

Latches

Function	Device	TRI-STATE Outputs	Broadside Pinout
Octal	54AC/74AC373	Yes	No
Octal	54ACT/74ACT373	Yes	No
Octal Transparent	54ACQ/74ACQ373	Yes	No
Octal Transparent	54ACTQ/74ACTQ373	Yes	No
Octal Transparent	54FCT/74FCT373	Yes	No
Octal Transparent	54FCT/74FCT373A	Yes	No
Octal D	54ACQ/74ACQ533	Yes	No
Octal D	54ACTQ/74ACTQ533	Yes	No
Octal D	54FCT/74FCT533	Yes	No
Octal D	54FCT/74FCT533A	Yes	No
Octal D	54ACT/74ACT563	Yes	Yes
Octal D	54ACQ/74ACQ563	Yes	Yes
Octal D	54ACTQ/74ACTQ563	Yes	Yes
Octal D	54FCT/74FCT563	Yes	Yes
Octal D	54FCT/74FCT563A	Yes	Yes
Octal D	54AC/74AC573	Yes	Yes
Octal D	54ACT/74ACT573	Yes	Yes
Octal D	54ACQ/74ACQ573	Yes	Yes
Octal D	54ACTQ/74ACTQ573	Yes	Yes
Octal D	54FCT/74FCT573	Yes	Yes
Octal D	54FCT/74FCT573A	Yes	Yes
Octal Transparent	54ACT/74ACT845	Yes	Yes
8-Bit Transparent	54FCT/74FCT845A/B	Yes	Yes
9-Bit Transparent	54AC/74AC843	Yes	Yes
9-Bit Transparent	54ACT/74ACT843	Yes	Yes
9-Bit Transparent	54ACTQ/74ACTQ843	Yes	Yes
9-Bit Transparent	54FCT/74FCTQ843A/B	Yes	Yes
10-Bit Transparent	54ACT/74ACT841	Yes	Yes
10-Bit Transparent	54FCT/74FCT841A/B	Yes	Yes
10-Bit Transparent	54ACTQ/74ACTQ841	Yes	Yes

Counters

Function	Device	Parallel Entry	Reset	U/D	TRI-STATE Outputs
4-Bit Binary	54AC/74AC161	S	A	No	No
4-Bit Binary	54ACT/74ACT161	S	A	No	No
4-Bit Binary	54AC/74AC163	S	S	No	No
4-Bit Binary	54ACT/74ACT163	S	S	No	No
4-Bit Binary	54AC/74AC169	S	—	Yes	No
4-Bit Binary	54ACT/74ACT169	S	—	Yes	No
4-Bit Binary	54AC/74AC191	A	—	Yes	No

S = Synchronous
A = Asynchronous

Buffers/Line Drivers

Function	Device	Enable Inputs (Level)	Inverting/ Non-Inverting	Broadside Pinout
Quad	54AC/74AC125	1(L)	N	No
Quad	54ACT/74ACT125	1(L)	N	No
Octal	54AC/74AC240	2(L)	I	No
Octal	54ACT/74ACT240	2(L)	I	No
Octal	54ACQ/74ACQ240	2(L)	I	No
Octal	54ACTQ/74ACTQ240	2(L)	I	No
Octal	54FCT/74FCT240	2(L)	I	No
Octal	54FCT/74FCT240A	2(L)	I	No
Octal	54AC/74AC241	1(H) & 1(L)	N	No
Octal	54ACT/74ACT241	1(H) & 1(L)	N	No
Octal	54ACQ/74ACQ241	1(H) & 1(L)	N	No
Octal	54ACTQ/74ACTQ241	1(H) & 1(L)	N	No
Octal	54FCT/74FCT241	1(H) & 1(L)	N	No
Octal	54FCT/74FCT241A	1(H) & 1(L)	N	No
Octal	54AC/74AC244	2(L)	N	No
Octal	54ACT/74ACT244	2(L)	N	No
Octal	54ACQ/74ACQ244	2(L)	N	No
Octal	54ACTQ/74ACTQ244	2(L)	N	No
Octal	54FCT/74FCT244	2(L)	N	No
Octal	54FCT/74FCT244A	2(L)	N	No
Hex	54ACT/74ACT367	1(L)	N	No
Hex	54ACT/74ACT368	1(L)	I	No
Octal	54AC/74AC540	2(L)	I	Yes
Octal	54FCT540	2(L)	I	Yes
Octal	54AC/74AC541	1(H) & 1(L)	N	Yes
Octal	54FCT541	1(H) & 1(L)	N	Yes
10-Bit	54ACTQ/74ACTQ827	2(L)	N	Yes
10-Bit	54FCT/74FCT827A/B	2(L)	N	Yes

L = LOW
H = HIGH

FIFOs

Function	Device	Input	Output	TRI-STATE Outputs
64 x 9 FIFO Memory	54AC/74AC2708	Parallel	Parallel	Yes
64 x 9 FIFO Memory	54ACT/74ACT2708	Parallel	Parallel	Yes
512 x 9 FIFO Memory	54ACT/74ACT2725	Parallel	Parallel	Yes
512 x 9 Bidirectional FIFO Memory	54ACT/74ACT2726	Parallel	Parallel	Yes

Decoders/Demultiplexers

Function	Device	LOW Enable	Active-HIGH Enable	Active-LOW Outputs	Active-Address Inputs
1-of-8	54AC/74AC138	2	1	8	3
1-of-8	54ACT/74ACT138	2	1	8	3
1-of-8	54FCT/74FCT138	2	1	8	3
1-of-8	54FCT/74FCT138A	2	1	8	3
Dual 1-of-4	54AC/74AC139	1 & 1	No	4 & 4	2 & 2
Dual 1-of-4	54ACT/74ACT139	1 & 1	No	4 & 4	2 & 2

Arithmetic Functions

Function	Device	Features
16 x 16 Multiplier	54ACT/74ACT1016	2s Complement & Unsigned Arithmetic
Arithmetic Logic Unit for DSP	54ACT/74ACT705	16-Bit ALU and 8 x 8 Parallel Multiplier/Accumulator

Video Support

Function	Device	Features
Video Sync Generator	54ACT/74ACT715	High Speed, Programmable Video Signal Generation

Shift Registers

Function	Device	No. of Bits	Reset	Serial Inputs	TRI-STATE Outputs
Octal Shift/Storage	54AC/74AC299	8	A	2	Yes
Octal Shift/Storage	54ACT/74ACT299	8	A	2	Yes
Octal Shift/Storage	54AC/74AC323	8	S	2	Yes
Octal Shift/Storage	54ACT/74ACT323	8	S	2	Yes

A = Asynchronous
S = Synchronous

Multiplexers

Function	Device	Enable Inputs (Level)	True Output	Complement Output
8-Input	54AC/74AC151	1(L)	Yes	Yes
8-Input	54ACT/74ACT151	1(L)	Yes	Yes
8-Input	54AC/74AC251	1(L)	Yes	Yes
8-Input	54ACT/74ACT251	1(L)	Yes	Yes
Dual 4-Input	54AC/74AC153	2(L)	Yes	No
Dual 4-Input	54ACT/74ACT153	2(L)	Yes	No
Dual 4-Input	54ACTQ/74ACTQ153	2(L)	Yes	No
Dual 4-Input	54AC/74AC253	2(L)	Yes	No
Dual 4-Input	54ACT/74ACT253	2(L)	Yes	No
Quad 2-Input	54AC/74AC157	1(L)	Yes	No
Quad 2-Input	54ACT/74ACT157	1(L)	Yes	No
Quad 2-Input	54AC/74AC158	1(L)	No	Yes
Quad 2-Input	54ACT/74ACT158	1(L)	No	Yes
Quad 2-Input	54AC/74AC257	1(L)	Yes	No
Quad 2-Input	54ACT/74ACT257	1(L)	Yes	No
Quad 2-Input	54AC/74AC258	1(L)	No	Yes
Quad 2-Input	54ACT/74ACT258	1(L)	No	Yes

Comparators

Function	Device	Features
Octal Identity Comparator	54AC/74AC520	Expandable
Octal Identity Comparator	54ACT/74ACT520	Expandable
Octal Identity Comparator	54AC/74AC521	Expandable
Octal Identity Comparator	54ACT/74ACT521	Expandable
Octal Identity Comparator	54FCT/74FCT521	Expandable
Octal Identity Comparator	54FCT/74FCT521A	Expandable

Transceivers/Registered Transceivers

Function	Device	Registered	Enable Inputs (Level)	TRI-STATE Output
Octal Bidirectional Transceiver	54AC/74AC245	No	1(L)	Yes
Octal Bidirectional Transceiver	54ACT/74ACT245	No	1(L)	Yes
Octal Bidirectional Transceiver	54ACQ/74ACQ245	No	1(L)	Yes
Octal Bidirectional Transceiver	54ACTQ/74ACTQ245	No	1(L)	Yes
Octal Bidirectional Transceiver	54FCT/74FCT245	No	1(L)	Yes
Octal Bidirectional Transceiver	54FCT/74FCT245A	No	1(L)	Yes
Octal Bus Transceiver and Register	54AC/74AC646	Yes	1(L) & 1(H)	Yes
Octal Bus Transceiver and Register	54ACT/74ACT646	Yes	1(L) & 1(H)	Yes
Octal Bus Transceiver and Register	54ACQ/74ACQ646	Yes	1(L) & 1(H)	Yes
Octal Bus Transceiver and Register	54ACTQ/74ACTQ646	Yes	1(L) & 1(H)	Yes
Octal Bus Transceiver and Register	54FCT/74FCT646	Yes	1(L) & 1(H)	Yes
Octal Bus Transceiver and Register	54FCT/74FCT646A	Yes	1(L) & 1(H)	Yes
Octal Bus Transceiver and Register	54AC/74AC648	Yes	1(L) & 1(H)	Yes
Octal Registered Transceiver	54ACQ/74ACQ543	Yes	2(L)	Yes
Octal Registered Transceiver	54ACT/74ACTQ543	Yes	2(L)	Yes
Octal Registered Transceiver	54FCT/74FCT543	Yes	2(L)	Yes
Octal Registered Transceiver	54FCT/74FCT543A	Yes	2(L)	Yes
Octal Registered Transceiver	54ACQ/74ACQ544	Yes	2(L)	Yes
Octal Registered Transceiver	54ACT/74ACTQ544	Yes	2(L)	Yes
Octal Registered Transceiver	54FCT/74FCT544	Yes	2(L)	Yes
Octal Registered Transceiver	54FCT/74FCT544A	Yes	2(L)	Yes
Octal Bus Transceiver	54ACTQ/74ACTQ657		1(L) & 1(H)	
Octal Bus Bidirectional Transceiver w/Parity	54FCT/74FCT657	No	1(L) & 1(H)	Yes
9-Bit Registered w/Parity	54ACQ/74AC899	Yes	1 (L) & 1 (H)	Yes
9-Bit Registered w/Parity	54ACTQ/74ACT899	Yes	1 (L) & 1 (H)	Yes
9-Bit Registered w/Parity	54FCT/74FCT899	Yes	1 (L) & 1 (H)	Yes

Clock Drivers

Function	Device	Multiplexed Clock
1 to 8 Minimum Skew Clock Driver	54AC/74AC2525	No
1 to 8 Minimum Skew Clock Driver	54AC/74AC2526	Yes

Section 1

Descriptions and Family Characteristics

Section 1 Contents

National Semiconductor

FACT™ Descriptions and Family Characteristics

National Semiconductor Advanced CMOS Technology—FACT—Logic

Fairchild Semiconductor introduced FACT (Fairchild Advanced CMOS Technology) logic, a family of high speed advanced CMOS circuits, in 1985.

FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

The 1.3-micron silicon gate CMOS process utilized in this family has been proven in the field of high performance gate arrays, CMOS ASIC, and FACT. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

In 1989, National Semiconductor introduced the FACT Quiet Series™ product line. This line of mostly octal bus-oriented logic functions is an enhancement of the original FACT line. Manufactured on a sub-micron silicon gate CMOS process, the FACT QS devices offer the lowest noise characteristics of any Advanced CMOS process with AC performance that is faster than FACT.

Also in 1989, National Semiconductor introduced its offering of fast CMOS technology or FACT FCT/FCTA. These product lines offer the fastest speeds of any TTL or CMOS logic, high DC output current drive, as well as the low noise design innovations of FACT QS.

For direct replacement of LS, ALS and other TTL devices, the 'ACT, 'ACTQ, 'FCT and 'FCTA circuits with TTL-type input thresholds are included in the FACT family.

Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
  - — Common Output Structure for Standard Gates and Buffer/Drivers
  - — Output Sink/Source Current of 24 mA on AC/ACT and ACQ/ACTQ
  - — Output Sink/Source Current of 48/64 mA on FCT/FCTA
  - — Transmission Line Driving 50Ω (Commercial)/75Ω (Military) Guaranteed
- Operation from 2V–6V V_{DD} Guaranteed ('AC/'ACQ)
- Temperature Range
  - — Commercial −40°C to +85°C
  - — Military −55°C to +125°C
- Improved ESD Protection Network
- High Current Latch-Up Immunity
- Patented Noise Suppression Circuitry on ACQ/ACTQ and FCT/FCTA

Interfacing

FACT devices have a wide operating voltage range (V_{DD} = 2 V_{DC} to 6 V_{DC}, 'AC/'ACQ) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

'AC/'ACQ — These are high speed CMOS devices with CMOS input switching levels and buffered CMOS outputs that can drive ±24 mA of I_{OH} and I_{OL} current. Industry standard 'AC/'ACQ nomenclature and pinouts are used.

'ACT/'ACTQ — These are high speed CMOS devices with a 'FCT/'FCTA TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a V_{DD} = 5V ±0.5V with V_{OH} = 2.4V and V_{OL} = 0.4V, but are functional over the entire FACT operating voltage range of 2.0 V_{DC} to 5.5 V_{DC}. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. 'ACT/'ACTQ devices have the same output structures as 'AC/'ACQ devices. 'FCT/'FCTA can drive +64 mA of I_{OL} and −15 mA of I_{OH} current.

Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws 1000 times less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

FACT	= 0.1 mW/Gate
ALS	= 1.2 mW/Gate
LS	= 2.0 mW/Gate
HC	= 0.1 mW/Gate

FACT Product Comparision

Feature	FACT AC/ACT	FACT ACQ/ACTQ	FACT FCT/FCTA
Dynamic line driving guaranteed to switch on incident wave into transmission line impedance as low as 50Ω at +85°C; 75Ω at +125°C	Yes I_{OLD}/I_{OHD}: ±75 mA	Yes I_{OLD}/I_{OHD}: ±75 mA	
Guaranteed High Output Drive	I_{OL}/I_{OH}: ±24 mA	I_{OL}/I_{OH}: ±24 mA	I_{OL}: +64 mA Commercial (Buffers/Drivers) +48 mA Military I_{OH}: −15 mA
Very High Speed Frequency	1 ns Internal Gate Delay; up to 100 MHz Toggle Frequency	≤1 ns Internal Gate Delay; up to 100 MHz Toggle Frequency	≤1 ns Internal Gate Delay; up to 200 MHz Toggle Frequency
CMOS Power	5 μW/Gate	5 μW/Gate	5 μW Gate
CMOS Input Loading	±1 μA	±1 μA	±1 μA
Extended Operating Voltage Range	2.0V to 6.0V	2.0V to 6.0V	2.0V to 6.0V
DC/AC Characteristics Guaranteed	3V and 5V ±10%	3V and 5V ±10%	5V ±5% Commercial 5V ±10% Military
Excellent Symmetrical Noise Margin (CMOS Inputs)	1.55V High; 1.55V Low	1.55V High; 1.55V Low	
Dynamic Thresholds (TTL-Compatible Inputs)		Maximum 2.2V High (V_{IHD}); Minimum 0.8V Low (V_{ILD})	Maximum 2.2V High (V_{IHD}); Minimum 0.8V Low (V_{ILD})
Guaranteed Latchup Immunity	±100 mA at +125°C	±300 mA at +125°C	
ESD Immunity	MIL Class 2 (2,000V − 3,999V); Typical 6,000V	MIL Class 2 (2,000V − 3,999V); Typical 6,000V	MIL Class 3 (4,000V or Greater); Typical 6,000V
Pin-to-Pin Output Propagation Delay Skew (Maximum)		1.0 ns (t_{OS}); Typical 0.5 ns	
Wafer Fabrication	JAN Class S DESC Certified		
Guaranteed Output Noise Levels (Maximum)		1.5V V_{OLP} (ground Bounce); −1.2V V_{OLV} (Undershoot)	FCTA: −1.2V V_{OLV} (Undershoot) FCT: 2.0V V_{OLP} (Ground Bounce) −1.2V V_{OLV} (Undershoot)
Driving Force for JEDEC Standard for Advanced CMOS	Yes		
Inherently Radiation Tolerant	Yes	Yes	Yes
Inputs Compatible with: CMOS TTL	AC ACT	ACQ ACTQ	 FCT, FCTA
Ful Compatibility (Function, Part Number, Pinout) with Standard 54/74 Functions	Yes	Yes (≥8 Bits)	Yes (≥8 Bits)

Low Power CMOS Operation (Continued)

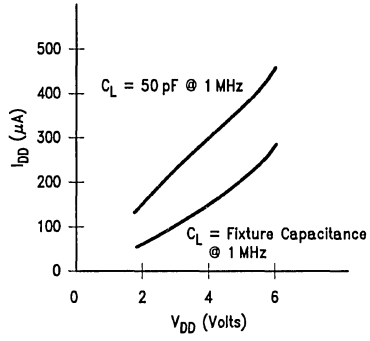

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FIGURE 1-1. I_{DD} vs V_{DD}

Figure 1-1 illustrates the effects of I_{DD} versus power supply voltage (V_{DD}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays as well as the basic gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The examples below describe typical values for a 74XX138, 3-to-8 line decoder and a 74xx244 line driver.

'138	
FACT AC	= 6.0 ns @ C_L = 50 pF
ALS	= 12.0 ns @ C_L = 50 pF
LS	= 22.0 ns @ C_L = 15 pF
HC	= 17.5 ns @ C_L = 50 pF

'244	
FACT FCTA	= 3.0 ns @ C_L = 50 pF
FACT ACQ	= 4.0 ns @ C_L = 50 pF
FACT AC	= 5.0 ns @ C_L = 50 pF
ALS	= 7.0 ns @ C_L = 50 pF
LS	= 12.0 ns @ C_L = 45 pF
HC	= 14.0 ns @ C_L = 50 pF

AC performance specifications are guaranteed at 5.0V ±0.5V and 3.3V ±0.3V. For worst case design at 2.0V V_{DD} on all device types, the formula below can be used to determine AC performance.

AC performance at 2.0V V_{DD} = 1.9 × AC specification at 3.3V.

Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 5.0V ±10% V_{DD}.

Noise Immunity

The DC noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL} - V_{OL}|/|V_{IH} - V_{OH}|$ at 4.5V V_{DD}.

FACT	= 1.25V/1.25V
ALS	= 0.4V/0.7V
LS	= 0.3V/0.7V @ 4.75V V_{DD}
HC	= 0.8V/1.25V

Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both 'AC/'ACQ and 'ACT/'ACTQ device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All SSI and MSI devices ('AC, 'ACT, 'ACQ or 'ACTQ) are guaranteed to source and sink 24 mA. FACT FCT and FACT FCTA are guaranteed to sink 64 mA (comm)/48 mA (mil) and source 15 mA (comm)/12 mA (mil). Commercial devices, 74AC/ACTXXX, are capable of driving 50Ω transmission lines, while military grade devices, 54AC/ACTXXX, can drive 75Ω transmission lines.

I_{OL}/I_{OH} Characteristics

FACT AC/ACT	= 24 mA/−24 mA
FACT ACQ/ACTQ	= 24 mA/−24 mA
FACT FCT/FCTA	= 64 mA/−15 mA
ALS	= 24 mA/−15 mA
LS	= 8 mA/−0.4 mA @ 4.75V V_{DD}
HC	= 4 mA/−4 mA

Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied "typical" output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these "typical" performance values across the operating voltage and temperature limits. Fortunately for the system designers, FACT has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50Ω for the commercial temperature range and 75Ω for the military temperature range.

Figure 1-2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ($I_{OUT} > 0$), are the V_{OH} and I_{IH} curves for FACT logic while on the left side ($I_{OUT} < 0$), are the curves for V_{OL} and I_{IL}. Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.

Dynamic Output Drive (Continued)

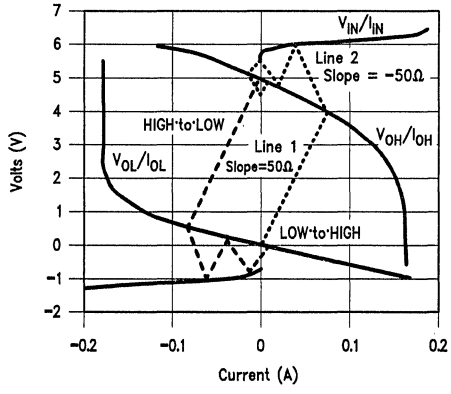

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FIGURE 1-2. Gate Driving 50Ω Line Reflection Diagram

Begin analysis at the V_{OL} (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the V_{IN}/I_{IN} curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a 50Ω load line from this intersection to the V_{OH}/I_{OH} curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95V. Then draw a line with a slope of −50Ω from this first intersection point to the V_{IN}/I_{IN} curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the V_{IN}/I_{IN} curve will be waves travelling from the receiver to the driver.

Figures 1-3a thru *1-3d* show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.

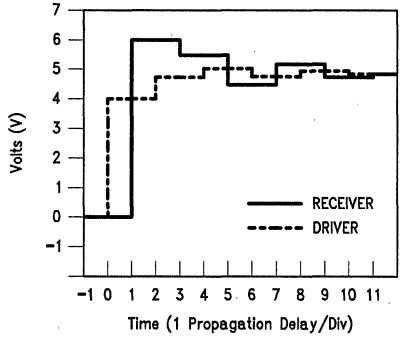

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FIGURE 1-3a. Resultant Waveforms Driving 50Ω Line—Theoretical

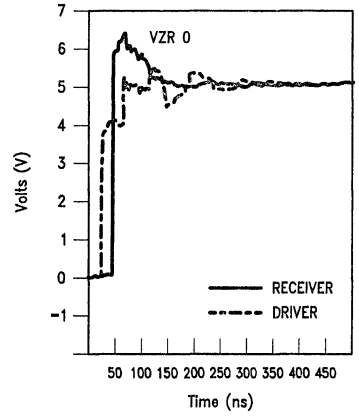

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FIGURE 1-3b. Resultant Waveforms Driving 50Ω Line—Actual

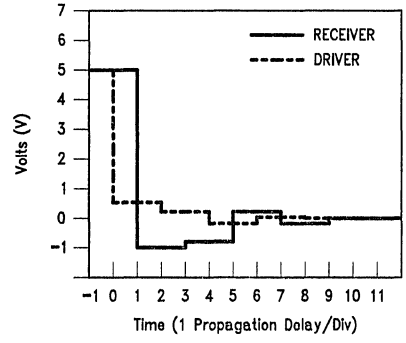

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FIGURE 1-3c. Resultant Waveforms Driving 50Ω Line—Theoretical

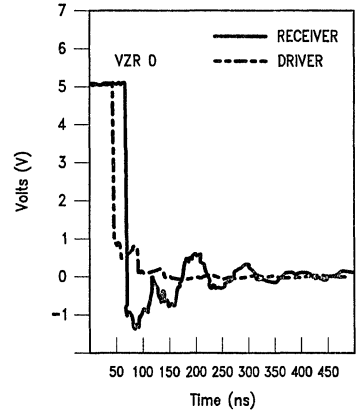

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FIGURE 1-3d. Resultant Waveforms Driving 50Ω Line—Actual

Dynamic Output Drive (Continued)

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V_{DD}. The formula for calculating the current and voltage required is $|(V_{OQ} - V_I)/Z_O|$ at V_I. For V_{OQ} = 100 mV, V_{IH} = 3.85V, V_{DD} = 5.5V and Z_O = 50Ω, the required I_{OH} at 3.85V is 75 mA. For the HIGH-to-LOW transition, V_{OQ} = 5.4V, V_{IL} = 1.65V and Z_O = 50Ω, I_{OL} is 75 mA at 1.65V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50Ω, the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA DC drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IN} level.

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

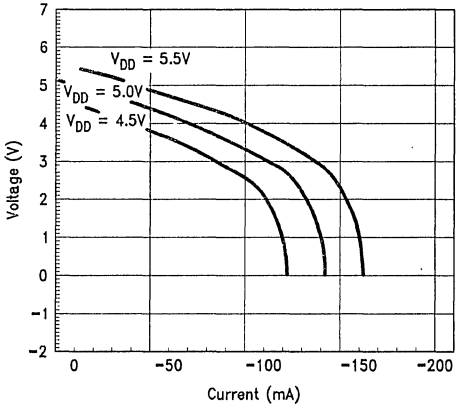

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FIGURE 1-4a. Output Characteristics V_{OH}/I_{OH}, 'AC00

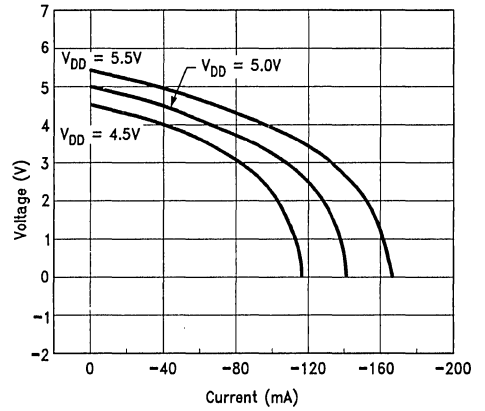

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FIGURE 1-4b. Output Characteristics V_{OH}/I_{OH}, 'ACTQ244

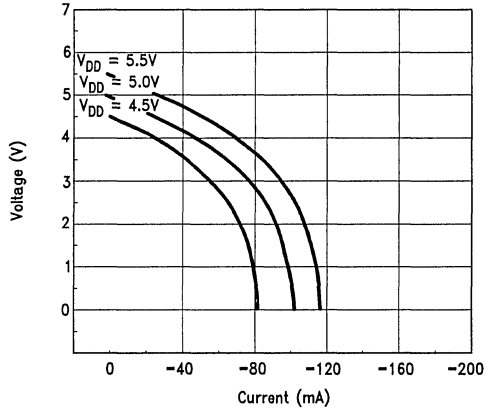

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FIGURE 1-4c. Output Characteristics V_{OH}/I_{OH}, 'FCT244A

Dynamic Output Drive (Continued)

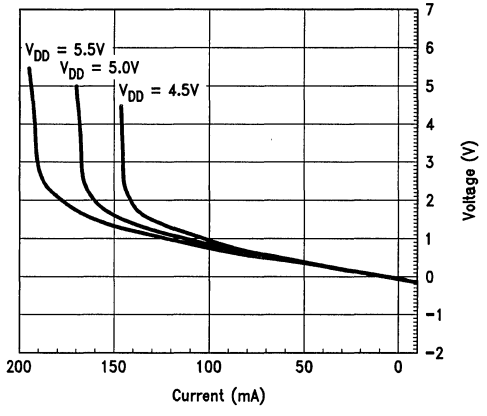

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FIGURE 1-5a. Output Characteristics V_{OL}/I_{OL}, 'AC00

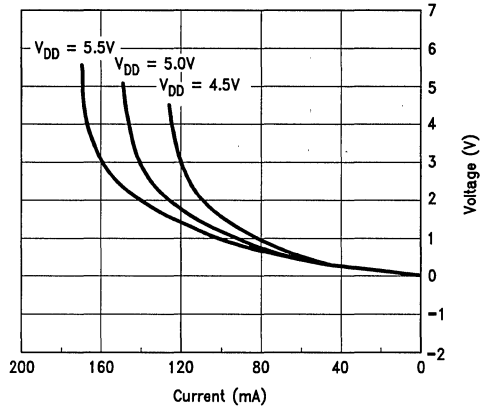

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FIGURE 1-5b. Output Characteristics V_{OL}/I_{OL}, 'ACTQ244

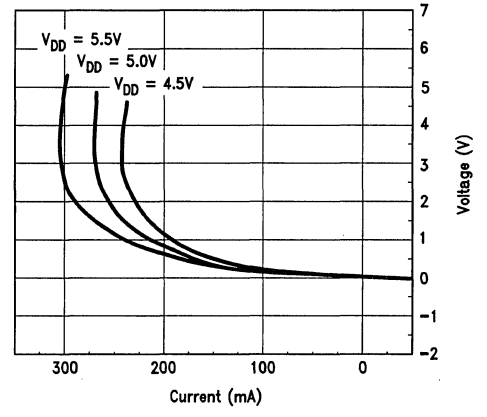

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FIGURE 1-5c. Output Characteristics V_{OL}/I_{OL}, 'FCT244A

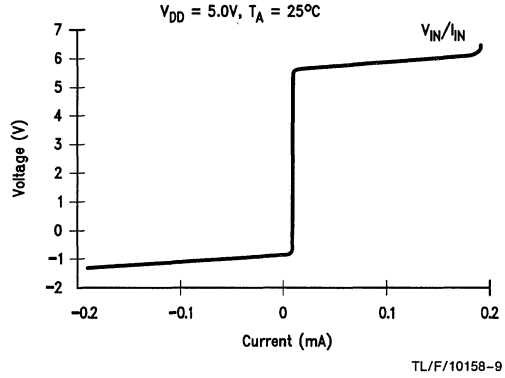

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FIGURE 1-6. Input Characteristics V_{IN}/I_{IN}

Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at 3.3V ±0.3V. To this end, National Semiconductor guarantees all of its devices operational at 3.3V ±0.3V. Note also that AC and DC specifications are guaranteed between 3.0V and 5.5V. Operation of FACT logic is also guaranteed from 2.0V to 6.0V 'AC/'ACQ on V_{DD}.

Operating Voltage Ranges

FACT = 2.0V to 6.0V ('AC/'ACQ)
FACT = 5.0V ±10% ('ACT/'ACTQ)
FACT = 5.0V ±5% ('FCT/'FCTA)
ALS = 5.0V ±10%
LS = 5.0V ±5%
HC = 2.0V to 6.0V

FACT Replaces Existing Logic

National Semiconductor's Advanced CMOS family is specifically designed to outperform existing CMOS and Bipolar logic families. *Figure 1-7* shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation delays while consuming 1 μW of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

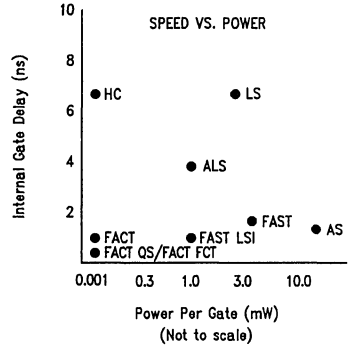

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FIGURE 1-7. Internal Gate Delays

General Characteristics (All Max Ratings)

Symbol	Characteristics	ALS	HCMOS	FACT			Units
				'AC/'ACQ	'ACT/'ACTQ	'FCT/'FCTA	
$V_{CC/EE/DD}$	Operating Voltage Range	5 ±10%	5 ±10%	5 ±5%	5 ±10%	5 ±5%	V
T_A 74 Series T_A 54 Series	Operating Temperature Range	0 to +70 −55 to +125	−40 to +85 −55 to +125	−40 to +85 −55 to +125	−40 to +85 −55 to +125	0 to +70 −55 to +125	°C
V_{IH} (Min)	Input Voltage (Limits)	2.0	3.15	3.85	2.0	2.0	V
V_{IL} (Max)		0.8	0.9	1.65	0.8	0.8	V
V_{OH} (Min)	Output Voltage (Limits)	2.7	V_{DD} − 0.1	V_{DD} − 0.1	V_{DD} − 0.1	V_{DD} − 0.2	V
V_{OL} (Max)		0.5	0.1	0.1	0.1	0.2	V
I_{IH}	Input Current	20	+1.0	+1.0	+1.0	+5.0	μA
I_{IL}		−200	−1.0	−1.0	−1.0	−5.0	μA
I_{OH}	Output Current at V_O (Limit)	−0.4	−4.0 @ V_{DD} − 0.8	−24 @ V_{DD} − 0.8	−24 @ V_{DD} − 0.8	−15 mA @ 2.4V	mA
I_{OL}		8.0	4.0 @ 0.4V	24 @ 0.44V	24 @ 0.44V	64 mA @ 0.5V	mA
DCM	DC Noise Margin LOW/HIGH (V_{DD} = 4.5V)	0.4/0.7	0.8/1.25	1.25/1.25	0.7/2.4	0.6/2.3	V

Note: All DC parameters are specified over the commercial temperature range.

Speed/Power Characteristics (All Typical Ratings)

Symbol	Characteristics	ALS	HCMOS	FACT AC	FACT FCTA	Units
I_G	Quiescent Supply Current/Gate	0.2	0.0005	0.0005	0.0005	mA
P_G	Power/Gate (Quiescent)	1.2	0.0025	0.0025	0.0025	mW
t_{Pd}	Propagation Delay ('244 Typ.)	7.0	14.0	5.0	3.0	ns
	Speed Power Product	8.4	0.04	0.01	0.008	pJ
f_{max}	Clock Frequency D/FF	50	50	160	225	MHz

FIGURE 1-8. Logic Family Comparisons

Propagation Delay (Commercial Temperature Range)

Symbol	Product		LS	ALS	HCMOS	FACT	Units
t_{PLH}/t_{PHL}	74XX00	Typ	10.0	5.0	8.0	5.0	ns
		Max	—	11.0	23.0	8.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX74	Typ	30.0	12.0	12.0	8.0	ns
		Max	—	18.0	44.0	10.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX163	Typ	27.0	10.0	20.0	5.0	ns
		Max	—	20.0	52.0	10.0	ns

Conditions: (LS) V_{DD} = 5.0V, C_L = 15 pF, 25°C;
(ALS/HC/FACT) V_{DD} = 5.0V ±10%, C_L = 50 pF, Over Temp, Max values at 0°C to +70°C for ALS, −40°C to +85°C for HC/FACT.

FIGURE 1-8. Logic Family Comparisons (Continued)

Circuit Characteristics

POWER DISSIPATION

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Total power dissipation of FACT device under AC conditions is a function of three basic sources, quiescent power, internal dynamic power, and output dynamic power dissipation. Firstly, a FACT device will dissipate power in the quiescent or static condition. This can be calculated by using the formula: (Note: In many datasheets I_{DD}, ΔI_{DD}, I_{DDT}, and V_{DD} are referred to as I_{CC}, ΔI_{CC}, I_{CCT}, and V_{CC}, respectively. There are no differences.)

Eq. 1 $PD_Q = I_{DD} \bullet V_{DD}$

PD_Q = Quiescent Power Dissipation
I_{DD} = Quiescent Power Supply Current Drain
V_{DD} = Power Supply Voltage

Secondly, a FACT device will dissipate power dynamically by charging and discharging internal capacitance. This can be calculated by using one of the following two formulas:

Eq. 2A (AC/ACQ)

$$PD_{INT} = (C_{PD} \bullet V_S \bullet f) \bullet V_{DD}$$

PD_{INT} = Internal Dynamic Power Dissipation
C_{PD} = Device Power Dissipation Capacitance
V_S = Output Voltage Swing
f = Internal Frequency of Operation
V_{DD} = Power Supply Voltage

C_{PD} values are specified for each FACT device and are measured per JEDEC standards as described later on in Section 2. On FACT device data sheets, C_{PD} is a typical value and is given either for the package or for the individual stages with the device. (See Section 2). For FACT devices, V_S and V_{DD} are the same value and can be replaced by V_{DD}^2 in the above formula.

Eq. 2B (ACT/ACTQ)

$$PD_{INT} = [(I_{DDT} \bullet D_H \bullet N_T) \bullet V_{DD}] + [(C_{PD} \bullet V_S \bullet f) \bullet V_{DD}]$$

PD_{INT} = Internal Dynamic Power Dissipation
I_{DDT} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs HIGH
N_T = Number of TTL Inputs at D_H
V_{DD} = Power Supply Voltage
C_{PD} = Device Power Dissipation Capacitance
V_S = Output Voltage Swing
f = Internal Frequency of Operation

Eq. 2C (FCT/FCTA)

$$PD_{INT} = [(\Delta I_{DD} \bullet D_H \bullet N_T) \bullet V_{DD}] + [(I_{DD} \bullet \{f_{CP}/2 + f_{IN} \bullet N_{IN}\}) \bullet V_{DD}]$$

PD_{INT} = Internal Dynamic Power Dissipation
V_{DD} = Power Supply Voltage
ΔI_{DD} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs HIGH
N_T = Number of TTL Inputs at D_H
I_{DDD} = Dynamic Current Caused by an Input Transition Pair (HLM or LHL)
f_{CP} = Clock Frequency for Registered Devices (Zero for Non-Registered Devices)
f_{IN} = Input Frequency
N_{IN} = Number of Inputs at f_{IN}

See Section 3 for more information on I_{DDT} or ΔI_{DD}.

Thirdly, a FACT device will dissipate power dynamically by charging and discharging any load capacitance. This can be calculated by using the following formula:

Eq. 3 $PD_{OUT} = (C_L \bullet V_S \bullet f) \bullet V_{DD}$

PD_{OUT} = Output Power Dissipation
C_L = Load Capacitance
V_S = Output Voltage Swing
f = Output Operating Frequency
V_{DD} = Power Supply Voltage

In many cases the output frequency is the same as the internal operation frequency. Also V_S is similar to V_{DD} and can be replaced by V_{DD}^2. In the case of internal and output frequencies being identical Eq. 2A and Eq. 3 may be combined as follows:

Eq. 4 $PD = (C_L + C_{PD}) \bullet V_{DD}^2 \bullet f$

The total FACT device power dissipation is the sum of the quiescent power and all of the dynamic power dissipation. This is best described as:

Eq. 5 $PD_{TOTAL} = PD_Q + PD_{DYNAMIC}$ or
$PD_{TOTAL} = PD_Q + PD_{INT} + PD_{OUT}$

The following is an exercise in calculating total dynamic I_{DD} for the FACT Advanced CMOS family. The device used as an example is the ACTQ374. Static I_{DD}, I_{DDT} and C_{PD} numbers can be found in the ACTQ374 data sheet. I_{DD} numbers used will be worst-case commercial guarantees. Room temperature power will be less. These are approximate worst-case calculations.

The following assumptions have been made:

1. I_{DD} will be calculated per input/output (as per JEDEC C_{PD} calculations). The total for the ACTQ374 will be the calculated $I_{DD} \times 8$.
2. Worst case conditions and JEDEC would require that the data is being toggled at the clock frequency in order to change the outputs at the maximum rate (½ CP).
3. The data and clock input signals are derived from TTL level drivers (0V to 3.0V swing) at 50% duty cycle.
4. The clock frequency is 16 MHz.
5. I_{DD} will be calculated for C_L = 50 pF, 100 pF and 150 pF.
6. V_{DD} = 5V.
7. Total POWER dissipation can be obtained by multiplying total I_{DD} by V_{DD} (5.0V).
8. Quiescent I_{DD} will be neglected in the total I_{DD} calculation because it is 1000 times less than dynamic I_{DD}.
9. There is no DC load on the outputs, i.e. outputs are either unterminated or terminated with series or AC shunt termination.

The I_{DD} calculations are as follows:

I_{DD} Total = Input I_{DD} + Internal Switching I_{DD} + Output Switching (AC load) I_{DD}

Input I_{DD} = $(I_{DDT}) \times$ (number of TTL inputs) $\times$ (Duty Cycle)
= $(1.5 \times 10^{-3}) \times (1) \times (0.50)$
= 0.75 mA per input being toggled at TTL levels

Internal I_{DD} = $(V_{SWING}) \times (C_{PD}) \times$ (CP freq)
= $(5.0) \times (42 \times 10^{-12}) \times (16 \times 10^{+6})$
= 3.36 per mA per input being toggled by CP

Output I_{DD} = $(V_{SWING} \times (C_L) \times$ (Q freq)

a) C_L = 50 pF
= $(5.0) \times (50 \times 10^{-12}) \times (8 \times 10^{+6})$
= 2 mA per output toggled at ½ CP

b) C_L = 100 pF
= $(5.0) \times (100 \times 10^{-12}) \times (8 \times 10^{+6})$
= 4 mA per output toggled at ½ CP

c) C_L = 150 pF
= $(5.0) \times (150 \times 10^{-12}) \times (8 \times 10^{+6})$
= 8 mA per output toggled at ½ CP

Adding Input, Internal and Output I_{DD} together and multiplying by 8 I/O per ACTQ374, the approximate worst-case I_{DD} calculations are as follows:

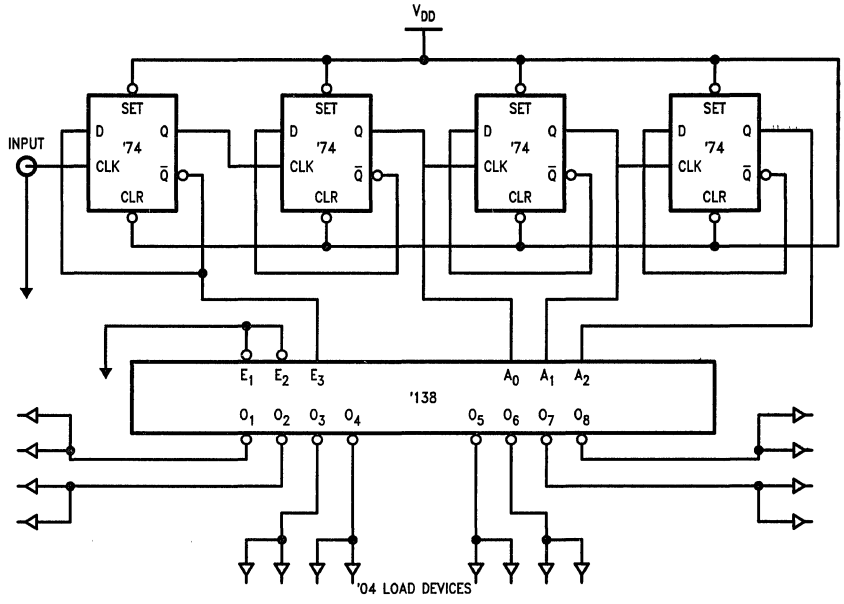
C_L = 50 pF I_{DD} total = 48.9 mA or 244.5 mW* at CP
= 16 MHz

C_L = 100 pF I_{DD} total = 64.9 mA or 324.5 mW* at CP
= 16 MHz

C_L = 150 pF I_{DD} total = 96.9 mA or 484.5 mW* at CP
= 16 MHz

(*Power is obtained by multiplying I_{DD} by V_{DD})

Circuit Characteristics (Continued)

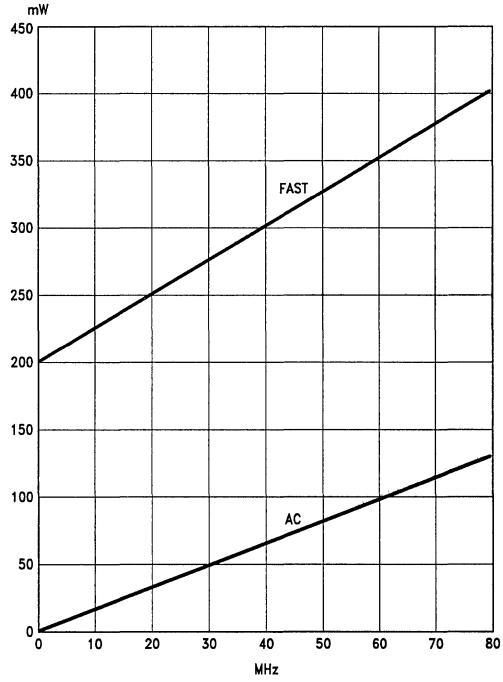


TL/F/10158–11

FIGURE 1-9. Power Demonstration Circuit Schematic

The circuit shown in *Figure 1-9* was used to compare the power consumption of FACT versus FAST devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were connected to the inputs of a '138 decoder. This generated eight non-overlapping clock pulses on the outputs of the '138, which were then connected to an '04 inverter. The input frequency was then varied and the power consumption was measured. *Figure 1-10* illustrates the results of these measurements.



TL/F/10158–12

FIGURE 1-10. FACT vs FAST Circuit Power

Circuit Characteristics (Continued)

The FACT circuit dissipates much less power than the FAST version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to zero; the FAST circuit continued to dissipate 200 mW.

SPECIFICATION DERIVATION

At first glance, the specifications for FACT logic might appear to be widely spread, possibly indicating wide design margins are required. However, several effects are reflected in each specification.

Figures 1-11a through *1-11i* illustrate how the data from the characterization of actual devices is transformed into the specifications that appear on the data sheet. This data is taken from the 'XX244.

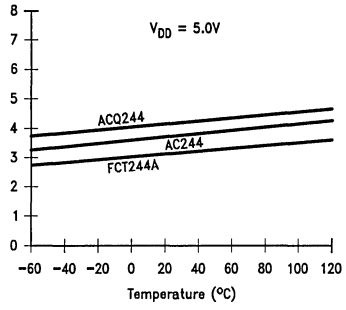
Figure 1-11a shows the data taken (from one part) on a typical, single path, t_{PHL}, over temperature at 5.0V; there is negligible variation in the value of t_{PHL}. The next set of graphs, *Figure 1-11b* through *1-11d*, depict data taken on the same device; these sets of curves represents the data on all paths. The data on this plot indicates only a small variation for t_{PHL}.

The graphs in *Figures 1-11a–d* include data at 5.0V; *Figure 1-11e* shows the variation of delay times over the standard 5.0V ±0.5V voltage range. Note there is only a ±6% variation in delay time due to voltage effects.

Now refer to *Figure 1-11f* which illustrates the process effects on delay time. This graph indicates that the process effects contribute to the spread in specifications more than any other factor in that the effects of the theoretical process spread can increase or decrease specification times by 30%. Because this 30% spread represents considerably more than ±3 standard deviations, this guarantees an increase in the manufacturability and the quality level of FACT product. To further ensure parts within specification will pass on testers at the limits of calibration, tester guardbands are incorporated.

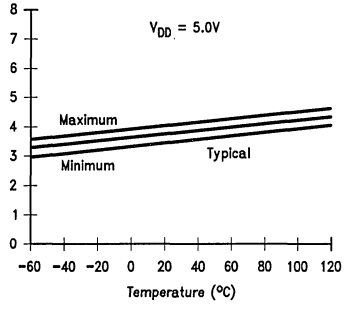
With voltage and process effects added *(Figures 1-11g, 1-11h,* and *1-11i)*, the full range of the specification can be seen. For reference, the data sheet values are shown on the graph.

This linear behavior with temperature and voltage is typical of CMOS. Although the graphs are drawn for a specific device, other part types have very similar graphical representations. Therefore, for performance-critical applications, where not all variables need to be taken into account at once, the user can narrow the specifications. For example, all parts in a critically timed subcircuit are together on a board, so it may be assumed the devices are at the same supply and temperature.



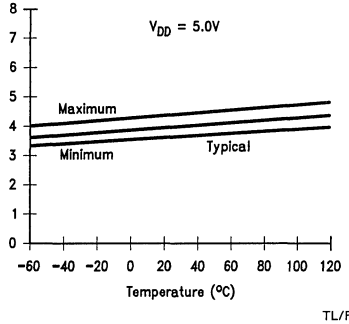
TL/F/10158–14

FIGURE 1-11a. t_{PHL} Single Path



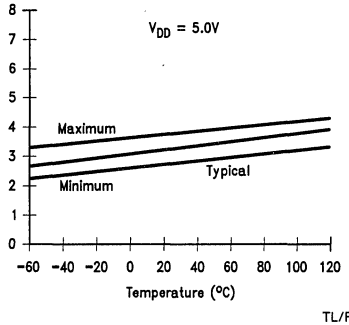
TL/F/10158–15

FIGURE 1-11b. t_{PHL}, 'AC244, All Paths



TL/F/10158–31

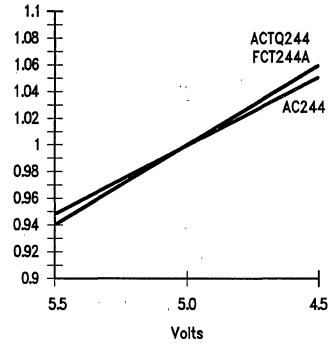
FIGURE 1-11c. t_{PHL}, 'ACQ244, All Paths



TL/F/10158–32

FIGURE 1-11d. t_{PHL}, 'FCT244A, All Paths

Circuit Characteristics (Continued)



TL/F/10158–16

FIGURE 1-11e. Voltage Effects on Delay Times

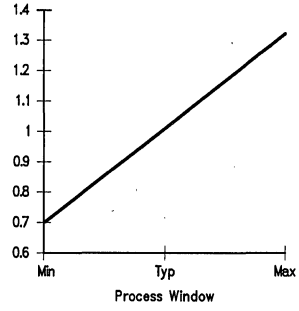


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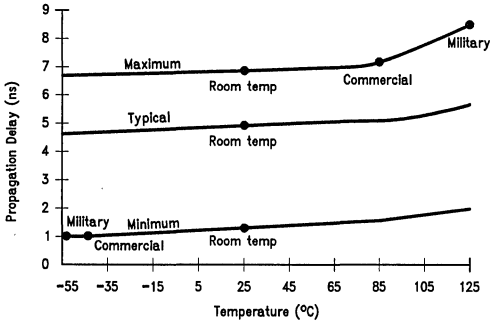
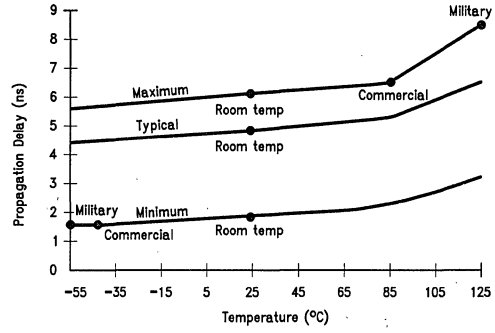
FIGURE 1-11f. FACT Process Effects on Delay Times



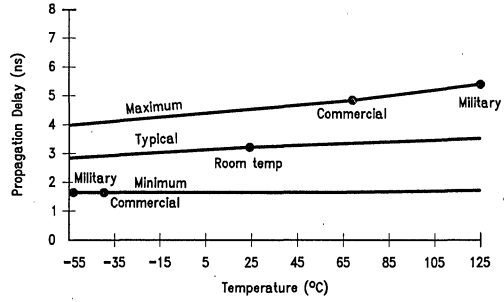
TL/F/10158–18

FIGURE 1-11g. t_{PHL}, 'AC244, with Voltage and Process Variation



TL/F/10158–33

FIGURE 1-11h. t_{PHL}, 'ACQ244, with Voltage and Process Variation



TL/F/10158–34

FIGURE 1-11i. t_{PHL}, 'FCT244A, with Voltage and Process Variation

Circuit Characteristics (Continued)

The same reasoning can be applied to setup and hold times. Consider the 'AC74. The setup time is 3.0 ns while the hold time is 0.5 ns. Theoretically, if these numbers were violated, the device would malfunction; however, in actuality, the device probably will not malfunction. Looking at the typical setup and hold times gives a better understanding of the device operation.

At 25°C and 5.0V, the setup time is 1.0 ns while the hold time is −1.5 ns. They are virtually the same; a positive setup time means the control signal to be valid before the clock edge, a positive hold time indicates the control signal will be held valid after the clock edge for the specified time, and a negative hold time means the control signal can transition before the clock edge. FACT devices were designed to be as immune to metastability as possible. This is reflected in the typical specifications. The true "critical" time where the input is actually sampled is extremely short: less than 50 ps.

By applying the same reasoning as we did to the propagation delays to the setup and hold times, it becomes obvious that the spread from setup to hold time (2.5 ns worst-case) really covers devices across the entire process/temperature/voltage spread. The real difference between the setup and hold times for any single device, at a specified temperature and voltage, is negligible.

CAPACITIVE LOADING EFFECTS

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from the table below. Propagation delay are measured to the 50% point of the output waveform.

Parameter		Voltage (V)			Units
		3.0	4.5	5.5	
t_{PLH}	FACT AC	31	22	19	ps/pF
	FACT QS	34	19	19	
	FACT FCTA	45	29	27	
t_{PHL}	FACT AC	18	13	13	ps/pF
	FACT QS	32	22	20	
	FACT FCTA	17	13	12	

T_A = 25°C

Figures 1-12 and *1-13*, describe propagation delays on FACT devices as affected by variations in power supply voltage (V_{DD}) and lumped load capacitance (C_L). *Figures 1-14* and *1-15* show the effects of lumped load capacitance on rise and fall times for FACT devices.

Circuit Characteristics (Continued)

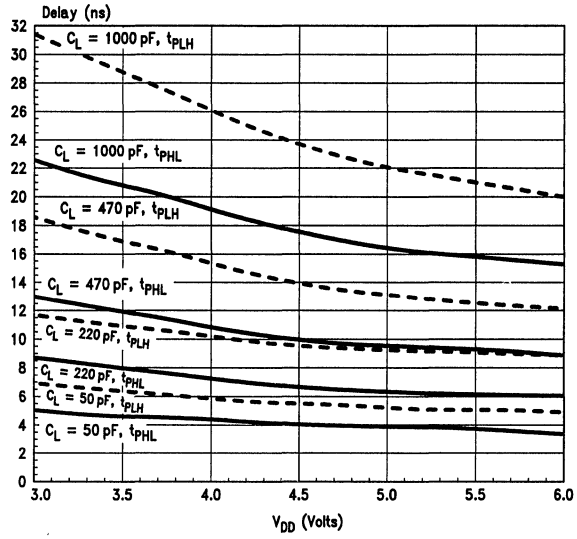


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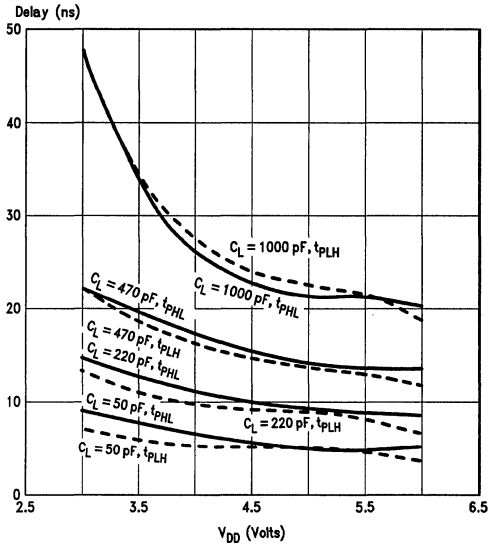
FIGURE 1-12a. Propagation Delay vs V_{DD} ('AC00)



TL/F/10158–35

FIGURE 1-12b. Propagation Delay vs V_{DD} ('ACTQ244)

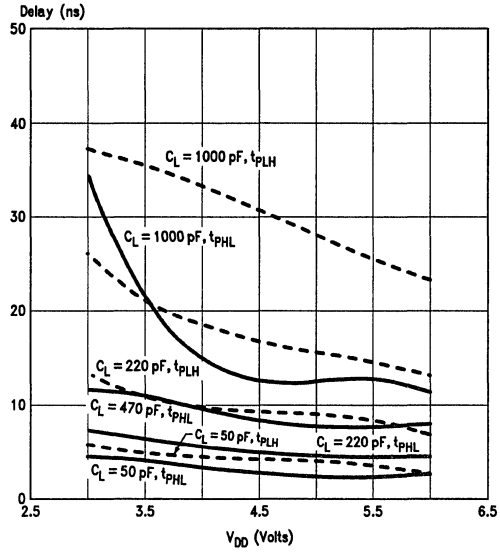


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FIGURE 1-12c. Propagation Delay vs V_{DD} ('FCT244A)

Circuit Characteristics (Continued)

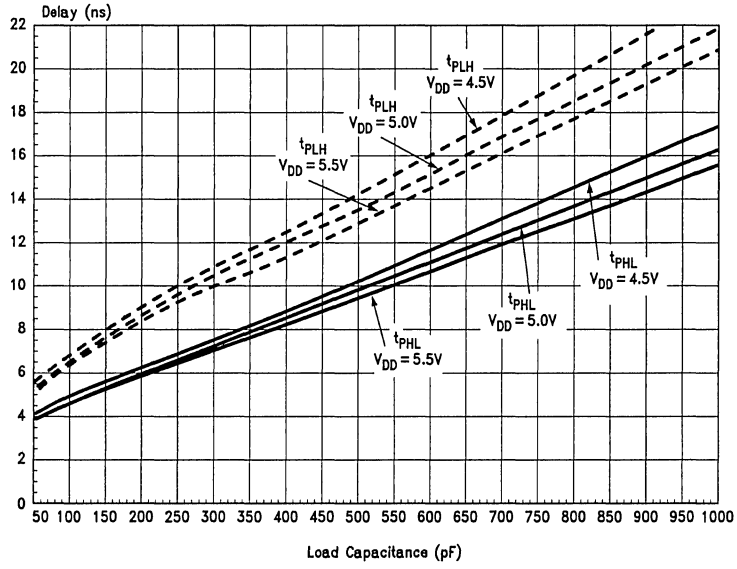

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FIGURE 1-13a. Propagation Delay vs C_L ('AC00)

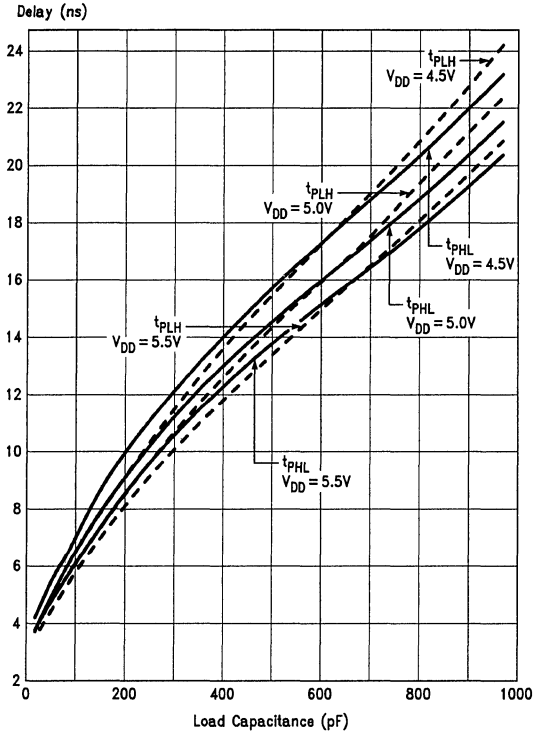

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FIGURE 1-13b. Propagation Delay vs C_L ('ACTQ244)

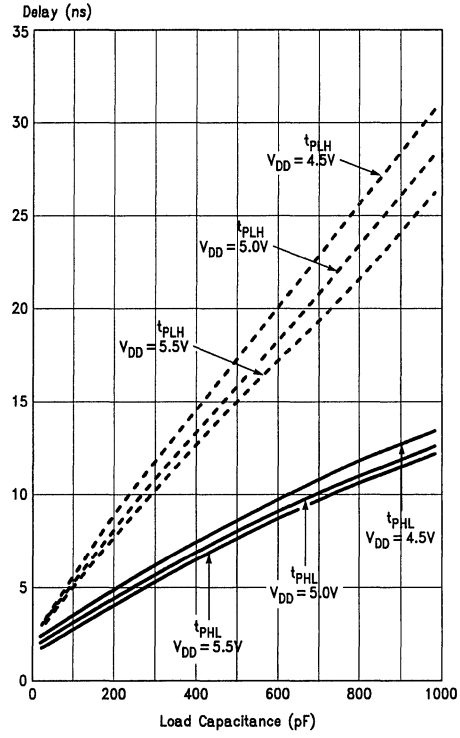

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FIGURE 1-13c. Propagation Delay vs C_L ('FCT244A)

Circuit Characteristics (Continued)

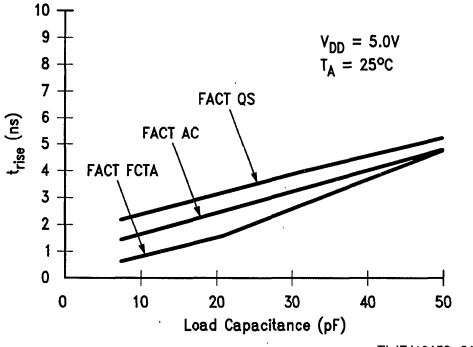

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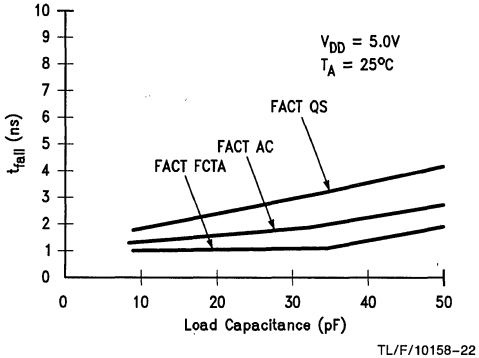
FIGURE 1-14. t_{rise} vs Capacitance



TL/F/10158–22

FIGURE 1-15. t_{fall} vs Capacitance

LATCH-UP

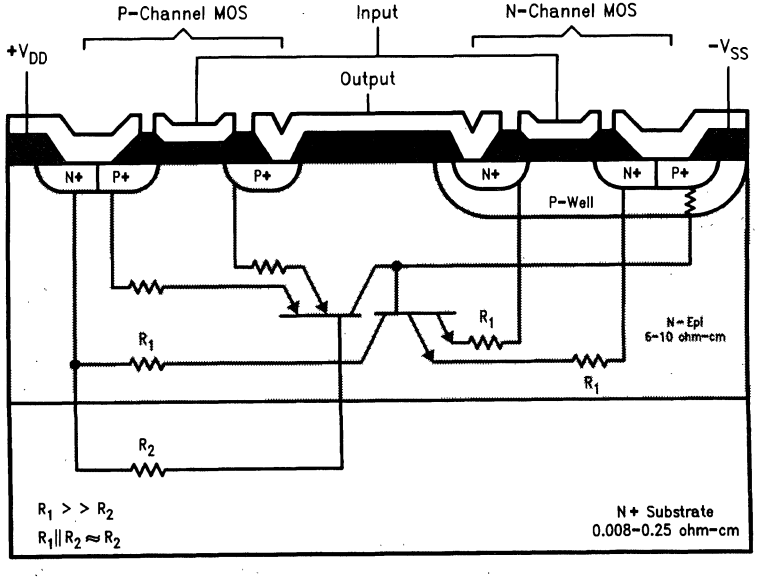
A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA (300 mA for FACT QS) forced into or out of the inputs or the outputs under worst case conditions (T_A = 125°C and V_{DD} = 5.5 V_{DC}). At room temperature the parts can typically withstand dynamic currents of close to 1A. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

FACT devices have been specifically designed to reduce the possibility of latch-up occurring; National Semiconductor accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY

FACT circuits show excellent resistance to ESD-type damage. These logic devices are classified as category "B" of MIL-STD-883C, test method 3015, and withstand in excess of 4000V typically. FACT logic is guaranteed to have 2000V ESD immunity on all inputs and outputs. Some FACT QS and FACT FCT/FCTA are guaranteed to have 4000V ESD immunity. FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 1-17 shows the ESD test circuit used in the sensitivity analysis for this specification. *Figure 1-18* is the pulse waveform required to perform the sensitivity test.



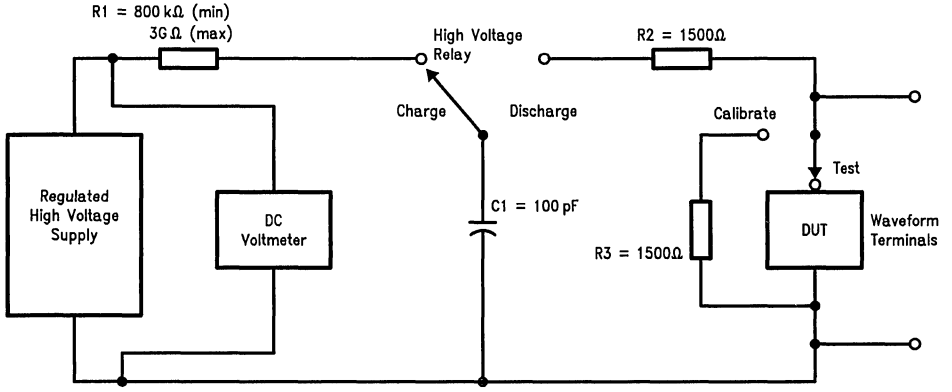
TL/F/10158–23

FIGURE 1-16. FACT EPI Process Cross Section with Latch-up Circuit Model

Circuit Characteristics (Continued)

The test procedure is as follows; five pulses, each of at least 2000V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883C, TM-3015. Devices that result in ESD immunity in the 2000V–3999V range are listed as ESD Class 2. Devices that result in ESD immunity in the 4000+V range are listed as ESD Class 3. Several devices on the FACT QS and FACT FCT/FCTA lines are guaranteed as Class 3 (see individual data sheets).

For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.



TL/F/10158–24

FIGURE 1-17. ESD Test Circuit

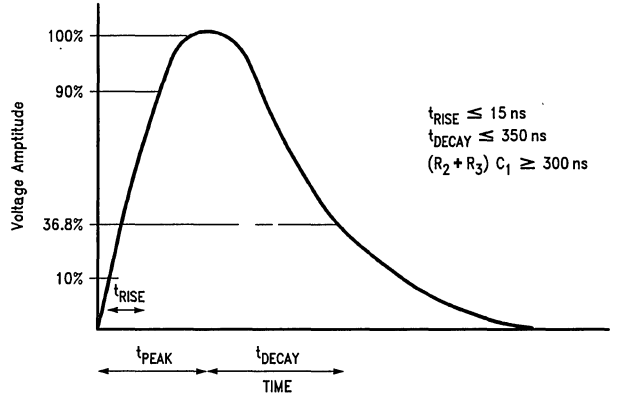


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FIGURE 1-18. ESD Pulse Waveform

Circuit Characteristics (Continued)

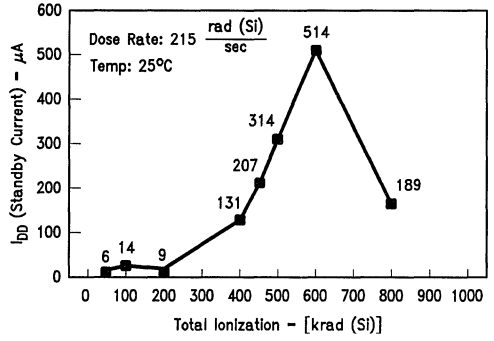
RADIATION TOLERANCE

Semiconductors subjected to radiation environments undergo degradation in operating life as their exposure to radiation increases. As technology advances, so does the demand for radiation-tolerant devices. National is meeting this challenge by developing the FACT family into a comprehensive radiation tolerant product for present and future rad-hard needs. Such applications include:

- Space (Commercial and Military)
  - — Satellites
  - — Space Stations
- Airborne and Military (Tactical Arena)
  - — Fighters/Bombers
  - — Missile Systems
  - — Ground Based Systems
  - — Navigation & Communications
- Commercial
  - — Power Stations
  - — Medical
  - — Food and Bacterial Control

Radiation tolerant semiconductors increase the useful life of the product in which they are incorporated. Additionally, radiation tolerant devices reduce shielding requirements and improve stabilization of parametric performance, resulting in cost reductions for shielding and weight, reduce power consumption and size.

SUMMARY OF TESTING



TL/F/10158–26

FIGURE 1-19. Total Dose Response (54AC245)

Total dose irradiation is presently performed "in-house" using a AECL Gamma Cell 220, Cobalt-60, source (National Bureau of Standards certified). Step-stress radiation testing is performed on each part-type per MIL STD 883 Method 1019.3. After each total dose level, a complete parametric test (DC and AC) is done and the parametric values evaluated.

FACT IS RADIATION TOLERANT

FACT logic employs the use of thin gate oxides, oxidation cycles, and annealing steps that enhance the tolerance of the standard FACT product line.

FACT's epitaxial layer and low-resistivity substrate provide inherent latch-up immunity under dose rate and single event phenomenon (SEP) conditions.

Figure 19 shows a FACT 'AC245 I_{DD} supply current versus total dose radiation. With the exception of I_{DD} and I_{OZ}, all FACT devices tested to date suffer no parametric degradation or functional failures up to several hundred krads. Due to circuit and layout differences, each function has a unique response to radiation. Relaxed limits for I_{DD} and I_{OZ} are per the applicable /750XX slash sheet, standard military drawing (SMD), or datasheet.

DOSE RATE TEST RESULTS

Analysis of the FACT 54AC299 8-Bit Universal Shift Register upset test data indicates that minimum upset threshold levels occurred under the worst-case conditions of a wide pulse (1 μs), lowest V_{DD} voltage (4.0V DC), and the DUT in the dynamic operating mode.

Measured minimum upset levels were 1.90 to 2.22 $\times$ 10^9 rad(Si)/sec. Narrow pulse (50 ns) data demonstrated radiation upset levels from 4.40 to 5.66 $\times$ 10^9 rad(Si)/sec under dynamic operation.

Upon completion of radiation upset testing, latchup and survivability tests were performed at +25°C, +80°C, +100°C, and +116°C for V_{DD} = 4.5V DC, 5.0V DC, and 5.5V DC. Test results indicated no latchup occurred for either narrow pulse (50 ns) or wide pulse (1 ms) radiation. The radiation test level for narrow pulse was 10^{10} rad(Si)/sec at +25°C. Due to the heating of the circuit, the highest radiation level was limited at +116°C to 7.5 $\times$ 10^9 rad(Si)/sec.

After completion of latchup and survivability tests, verification of latchup windows was performed. Test results indicate no existence of latchup windows under worst case conditions for narrow and wide pulse radiation.

Section 2

Ratings, Specifications, and Waveforms

Section 2 Contents

National Semiconductor

Ratings, Specifications, and Waveforms

Specifying FACT™ Devices

Traditionally, when a semiconductor manufacturer completed a new device for introduction, specifications were based on the characterization of just a few parts. While these specifications were appealing to the designer, they were often too tight and, over time, the IC manufacturers had difficulty producing devices to the original specs. This forced the manufacturer to relax circuit specifications to reflect the actual performance of the device.

As a result, designers were required to review system designs to ensure the system would remain reliable with the new specifications. National Semiconductor realized and understood the problems associated with characterizing devices too aggressively.

To provide more realistic and manufacturable specs, National Semiconductor devised a systematic and thorough process to generate specifications. Devices are selected from multiple wafer lots to ensure process variations are taken into account. In addition, the process parameters are measured and compared to the known process limits. With more than five years of experience manufacturing FACT logic, National Semiconductor can accurately predict how these wafer lots compare with the best and worse case lots that can possibly be expected.

This method of characterizing parts more accurately represents the product across time, voltage, temperature and process rather than portraying the fastest possible device.

These specification guidelines allow designers to design systems more efficiently since the devices used will behave as documented. Unspecified guardbands no longer need to be added by the designer to ensure system reliability.

Power Dissipation—Test Philosophy

In an effort to reduce confusion about measuring power dissipation capacitance, C_{PD}, a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison.

The following is a list of different types of logic functions, along with the input setup conditions under which the C_{PD} was measured for each type of device. By understanding how the device was exercised during C_{PD} measurements, the designer can understand whether the C_{PD} specified for that particular device reflects the total power dissipation capacitance for either the entire device or for just a certain stage of that device. For example, from the following list, it is apparent that the C_{PD} value specified for a counter reflects the internal capacitance for the entire device, since the entire device is being exercised during measurement. On the other hand, the C_{PD} value specified for an octal line driver reflects the internal capacitance for only one of eight stages, since only one input was being switched during test. Therefore the octal's overall power dissipation should be calculated for each of the eight stages, individually.

During the C_{PD} measurements, each output that is being switched should be loaded with the standard 50 pF and 500Ω load. All device measurements are made with V_{DD} = 5.0V at 25°C, with TRI-STATE® outputs enabled.

Gates/Buffers/ Line Drivers:	Switch one input. Bias the remaining inputs such that one output switches.
Latches:	Switch the Enable and D inputs such that the latch toggles.
Flip-Flops:	Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-flop.
Decoders:	Switch one address pin which changes two outputs.
Multiplexers:	Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.
Counters:	Switch the clock pin with other inputs biased such that the device counts.
Shift Registers:	Switch the clock pin with other inputs biased such that the device shifts.
Transceivers:	Switch one data input. For bidirectional devices enable only one direction.
Parity Generator:	Switch one input.
Priority Encoders:	Switch the lowest priority input.

AC Loading and Waveforms

LOADING CIRCUIT

Figure 1 shows the AC loading circuit used in characterizing and specifying propagation delays of all FACT devices ('AC and 'ACT) unless otherwise specified in the data sheet of a specific device.

AC Loading and Waveforms (Continued)

The use of this load, which is equivalent to the FAST® (Fairchild Advanced Schottky TTL) test jig, differs somewhat from previous (HCMOS) practice. This provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance, allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the inloading to be expected in avarage applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the FACT product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

The 500Ω resistor to ground can be a high frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high impedance probe. Alternately, the 500Ω resistor to ground can simply be a 450Ω resistor feeding into a 50Ω coaxial cable leading to a sampling scope input connector, with the internal 50Ω termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See *Figure 1*.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50Ω termination for the pulse generator that supplies the input signal.

Shown in *Figure 1* is a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500Ω resistors and the 2 × V_{DD} supply voltage establish a quiescent HIGH level.

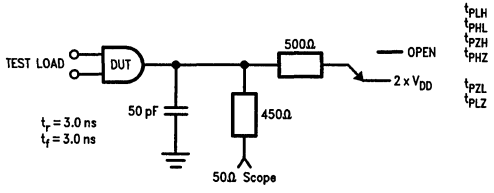


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FIGURE 1a. AC Loading Circuit for AC, ACT, ACQ, ACTQ

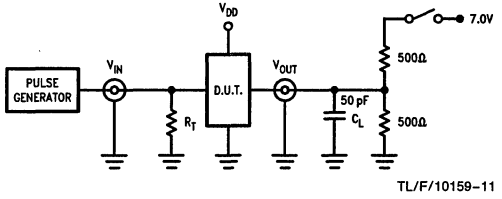

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FIGURE 1b. AC Loading Circuit for FCT, FCTA

Test Conditions

Figures 2a and *2b* describe the input signal voltage levels to be used when testing FACT circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0V for a logic LOW to 3.0V for a logic HIGH for 'ACT devices and 0V to V_{DD} for 'AC devices. The DC parameters are normally tested with V_{IN} at guaranteed input levels, that is V_{IH} to V_{IL} (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 5.0V then dropping to a level corresponding to V_{IH} characteristics, and then raising again to the 5.0V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0V to V_{IL}, then returning to 0V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the FACT device.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output wave-

'ACxx, ACQxx Devices

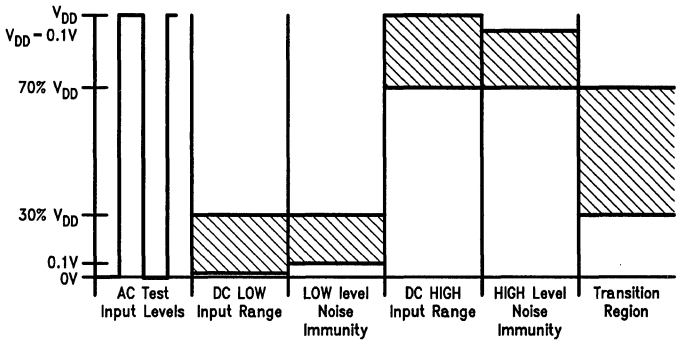

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FIGURE 2a. Test Input Signal Levels

Test Conditions (Continued)

'ACTxx, ACTQxx, FCTxx, FCTxxA Devices

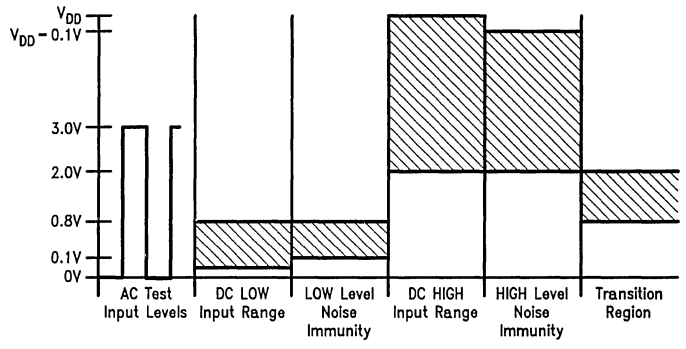

FIGURE 2b. Test Input Signal Levels

form transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{DD} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

Rise and Fall Times

Input signals should have rise and fall times of 3.0 ns and signal swing of 0V to 3.0V V_{DD} for 'ACT devices or 0V to V_{DD} for 'AC devices. Rise and fall times less than or equal to 1 ns should be used for testing f_{max} or pulse widths.

CMOS devices, including 4000 Series CMOS, HC, HCT and FACT families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, FACT devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a HIGH level to a LOW level, or from a LOW level to a HIGH level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2–3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the V_{DD} or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world because of this induced voltage.

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it recrosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have V_{DD} and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With FACT logic having gains as high as 100, it merely takes a 50 mV change in the input to generate a full 5V swing on the output.

Propagation Delays, f_{max}, Set and Hold Times

A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc. See *Figures 3, 4*, and *8*.

Enable and Disable Times

Figures 5, 6 and *11* show that the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from V_{OL} or V_{OH}, respectively. This change enhances the repeatability of measurements, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 0.3V of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 0.3V is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable times and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled. Note that the measurement points have been changed from the previous 10% and 90% points. This better reflects actual test points and does not change specification limits.

Waveforms

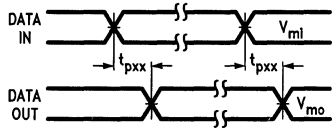

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FIGURE 3. Waveform for Inverting and Non-Inverting Functions for AC/ACT, ACQ/ACTQ

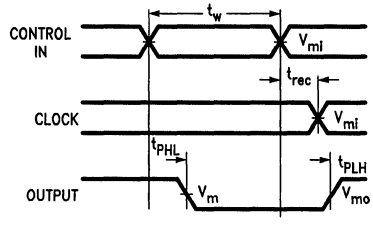

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FIGURE 4. Propagation Delay, Pulse Width and t_{rec} Waveforms for AC/ACT, ACQ/ACTQ

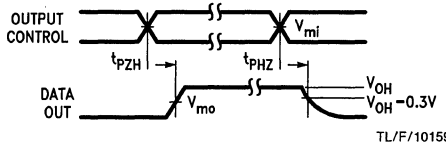

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FIGURE 5. TRI-STATE Output High Enable and Disable Times for AC/ACT, ACQ/ACTQ

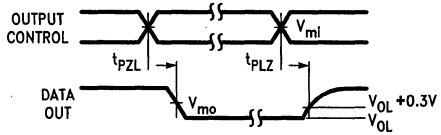

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FIGURE 6. TRI-STATE Output Low Enable and Disable Times for AC/ACT, ACQ/ACTQ

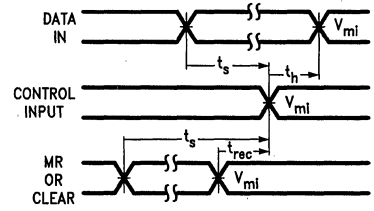

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FIGURE 7. Setup Time, Hold Time and Recovery Time for AC/ACT, ACQ/ACTQ

*V_{mi} = 50% V_{DD} for 'AC/'ACQ devices; 1.5V for 'ACT/'ACTQ devices
V_{mo} = 50% V_{DD} for 'AC/'ACT, 'ACQ/'ACTQ devices

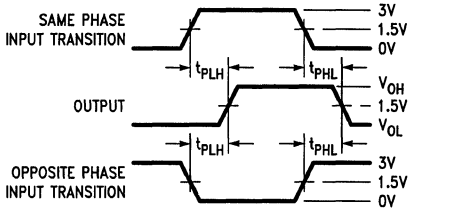

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FIGURE 8. Propagation Delay for FCT, FCTA

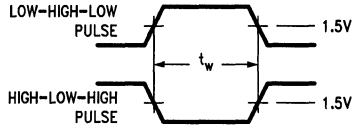

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FIGURE 9. Pulse Width for FCT, FCTA

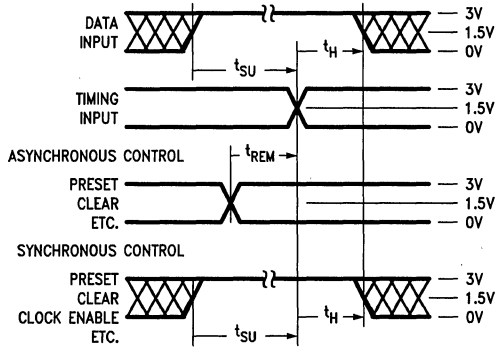

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FIGURE 10. Set-Up, Hold and Release Times for FCT, FCTA

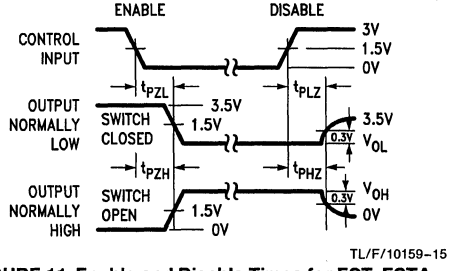

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FIGURE 11. Enable and Disable Times for FCT, FCTA

Note 1: Diagram shown for input Control Enable-LOW and input Control Disable-HIGH

Note 2: Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_o ≤ 50Ω; t_F ≤ 2.5 ns; t_R ≤ 2.5 ns

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FACT devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, which are near the device, are conductive and connected to ground.

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture or Equivalent
Tektronics Model 7854 Oscilloscope or Equivalent

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{DD} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT/ACTQ/FCT/FCTA devices and 0V LOW and 5V HIGH for AC/ACQ devices. Verify levels with a digital volt meter.

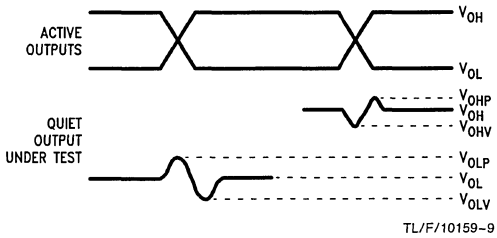

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FIGURE 12. Quiet Output Noise Voltage Waveforms

Note A. V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B. Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output LOW during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output HIGH during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

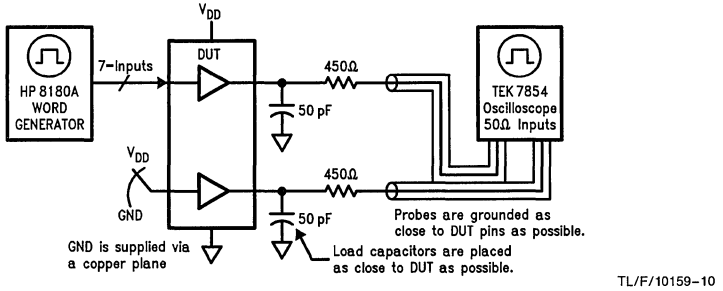

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FIGURE 13. Simultaneous Switching Test Circuit

Section 3

Design Considerations and Application Notes

Section 3 Contents

National Semiconductor

Design Considerations

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. National Semiconductor's advanced CMOS helps designers achieve these goals.

FACT™ (Fairchild Advanced CMOS Technology) logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a 50Ω transmission line drive capability (comparable to National Semiconductor's FAST bipolar technology family) to offer a complete family of 1.3-micron SSI, MSI, and LSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD, and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

There are six items of interest which need to be evaluated when implementing FACT devices in new designs:

- Interfacing—interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving—FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects—As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to system-generated problems.
- Board Layout—Prudent board layout will ensure that most noise effects are minimized.
- Power Supplies and Decoupling—Maximize ground and V_{DD} traces to keep V_{DD}/ground impedance as low as possible; full ground/V_{DD} planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.
- Electromagnetic Interference

Interfacing

FACT and FACT QS devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink 24 mA of current under worst case conditions. FACT FCT is guaranteed to sink 64 mA and source 15 mA. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive FAST®, ALS, AS, LS, HC and HCT devices.

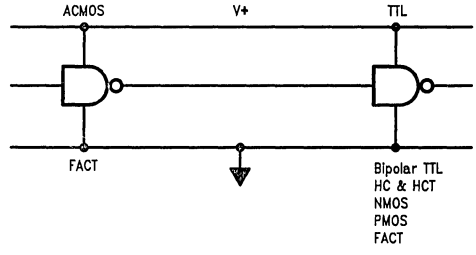


FIGURE 3-1. Interfacing FACT to NMOS, CMOS, and TTL

FACT devices can be directly driven by both NMOS and CMOS families, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1 μA per input.

Some older technologies, including all existing TTL families, will not be able to drive FACT AC/ACQ circuits directly; this is due to inadequate output HIGH level capability, which is guaranteed to 2.4V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be constructed employing a resistor pull-up to V_{DD} of approximately 4.7 kΩ, which is depicted in *Figure 3-2*. The correct HIGH level is seen by the CMOS device while not loading down the TTL driver.

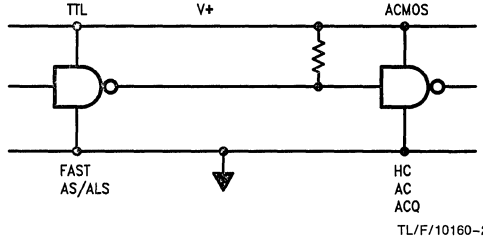


FIGURE 3-2. V_{IH} Pull-Up on TTL Outputs

Unfortunately, there will be designs where including a pull-up resistor will not be acceptable. In these cases, such as a terminated TTL bus, National Semiconductor has designed devices which offer thresholds that are TTL-compatible *(Figure 3-3)*.

Interfacing (Continued)

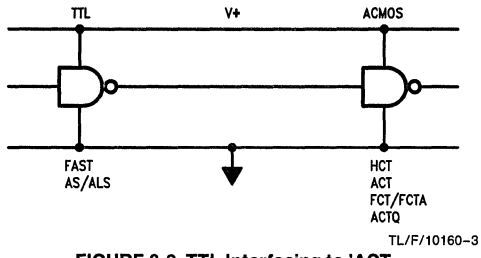


FIGURE 3-3. TTL Interfacing to 'ACT

ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using a F100124 or F100324 TTL-to-ECL translator and a F100125 or F100325 ECL-to-TTL translator in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to V_{DD} of approximately 4.7 kΩ).

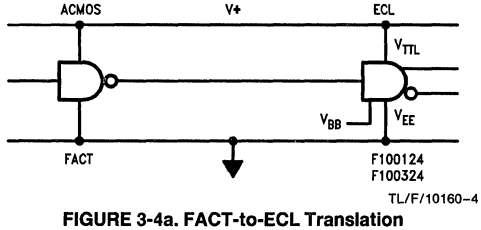


FIGURE 3-4a. FACT-to-ECL Translation

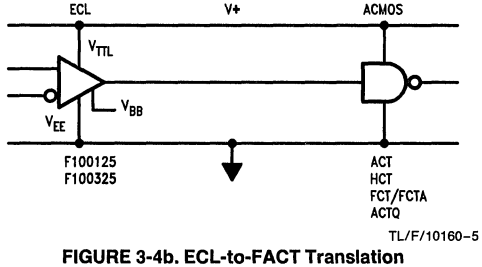


FIGURE 3-4b. ECL-to-FACT Translation

It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

Line Driving and Termination

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become more significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

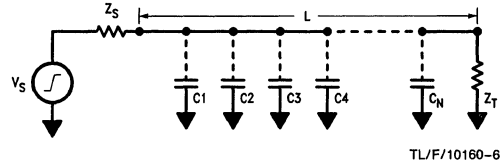
Of the many properties of transmission lines, two are of major interest to the system designer: Z'_o, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z'_o and t_{pde} can be calculated with:

$$Z'_o = \frac{Z_o}{\sqrt{1 + C_D/C_L}}$$

$$t_{pde} = t_{pd}\sqrt{1 + C_D/C_L}$$

where C_L = intrinsic line capacitance and C_D = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.



Length of Transmission Line = L

Distributed Load Capacitance per Unit Length = $C_D = \sum_{n=1}^{N} C_L/L$

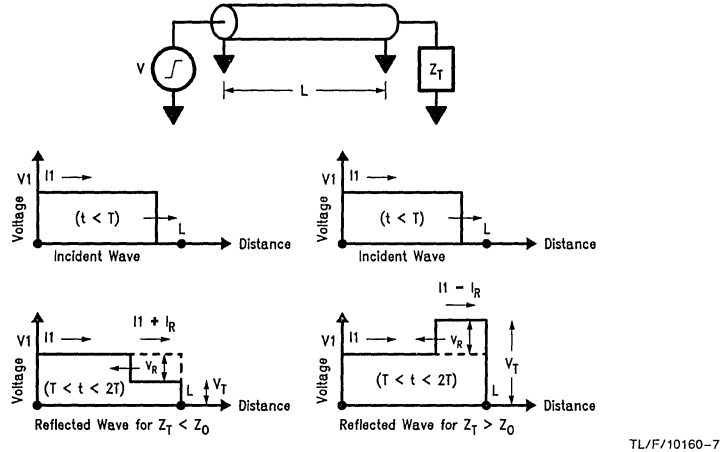
Characteristic Impedance of a Transmission Line Altered by Distributed Loading

$$= Z'_O = \sqrt{\frac{L_O}{C_O + C_D}} = \frac{Z_O}{\sqrt{1 + \frac{C_D}{C_O}}}$$

Effective Reflection Coefficient at Termination = $\rho = \frac{Z_T - Z'_O}{Z_T + Z'_O}$

FIGURE 3-5a. Transmission Line with Distributed Loading

Line Driving and Termination (Continued)



TL/F/10160–7

- Length of Transmission Line = L
- Delay of Transmission Line = T
- Time of Sample = t
- Incident Wave Current = I_1
- Incident Wave Voltage = V_1
- Reflected Wave Current = I_R
- Reflected Wave Voltage = V_R
- Characteristic Impedance of Line = Z_O
- Termination Impedance = Z_T
- Voltage at Termination = V_T

FIGURE 3-5b. Reflections Due to Impedance Mismatching

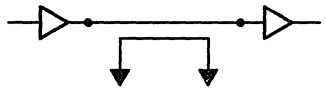
There are several termination schemes which may be used. Included are series, parallel, AC parallel, and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

SERIES TERMINATIONS

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line or especially for single point loads. Loads that are between the driver and the end of the line will receive a two-step waveform. The first step will be the incident wave, V_i. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor, and the impedance of the line according to the formula

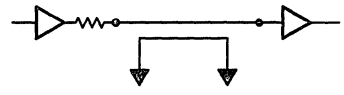
$$V_i = V_{DD} \cdot Z'_o/(Z'_o + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. Z_S for FACT is approximately 17Ω. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a



TL/F/10160–8

a. No Termination



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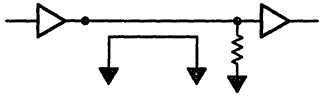
b. Series Termination



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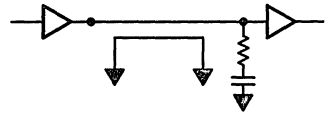
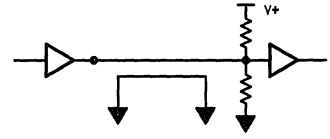
c. Parallel Termination



TL/F/10160–11

d. AC Parallel Termination



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e. Thevenin Termination

FIGURE 3-6a. Termination Schemes

Line Driving and Termination (Continued)

valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

PARALLEL TERMINATION

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{DD} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

AC PARALLEL TERMINATION

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The terminating effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

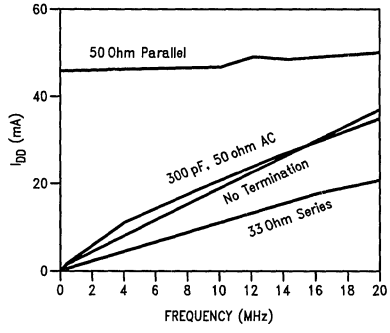
Thevenin Termination

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{DD} or ground, increasing power consumption.

- Parallel: Resistor = Z_o
- Thevenin: Resistor = $2 \times Z_o$
- Series: Resistor = $Z_o - Z_{out}$
- AC: Resistor = Z_o

  Capacitor = $C \geq \frac{3tr}{Z_o}$

Figure 3-6b. Suggested Termination Values



TL/F/10160–13

FIGURE 3-6c. FACT I_{DD} vs Termination

FACT circuits have been designed to drive 50Ω transmission lines over the full commercial temperature range and 75Ω transmission lines over the military temperature range. This is guaranteed by the FACT family's specified dynamic drive capability of 75 mA source and sink current. This ensures incident wave switching on 50Ω transmission lines and is consistent with the 3 ns rated edge transition time.

FACT and FACT QS devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT FCT/FCTA have very high DC sink current capability (64 mA, commercial temperature) making the output drive compatible with popular bus standards such as VMEbus™ and MULTIBUS®.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} for AC/ACQ devices are specified at 70% and 30% of V_{DD} respectively. The corresponding output levels, V_{OH} and V_{OL}, are specified to be within 0.1V of the rails, of which the output is sourcing or sinking 50 μA or less. These noise margins are outlined in *Figure 3-7*.

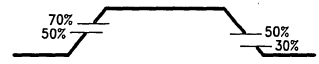


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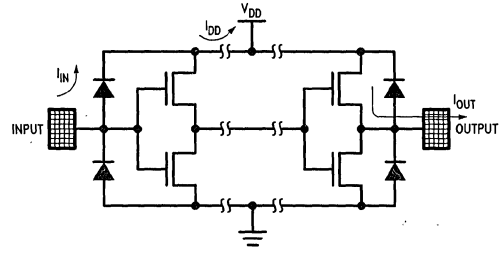
FIGURE 3-7. AC/ACQ Input Threshold

CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{DD} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 3-8 exemplifies the situation when power is removed. Any input driven above the V_{DD} pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{DD} or any output that is HIGH. Depending upon the system, this current, I_{IN}, can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line. Another possible solution would be to ensure that the output enable input is inactive, preventing the outputs from turning on and loading down the bus. This may be accomplished by hardwiring a 4.7 kΩ pull-up resistor to the V_{DD} pin of the FACT device.



TL/F/10160–15

FIGURE 3-8. Noise Effects

Noise Effects

FACT offers the best noise immunity of any competing technology available today. With input thresholds specified at 30% and 70% of V_{DD} and outputs that drive to within 100 mV of the rails, FACT AC/ACQ devices offer noise margins approaching 30% of V_{DD}. At 5V V_{DD}, FACT's specified input and output levels give almost 1.5V of noise margin for both ground- and V_{DD}-born noise. With realistic input thresholds closer to 50% of V_{DD}, the actual margins approach 2.5V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

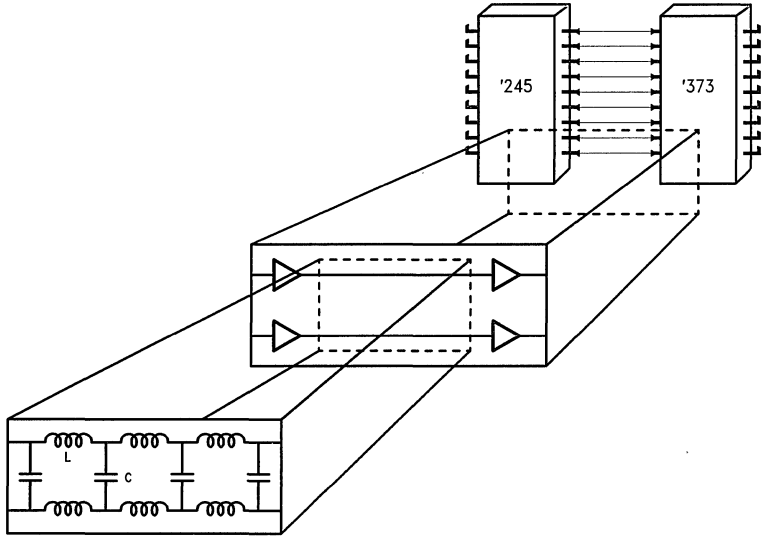
Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, *Figures 3-9b* and *3-9d*, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air (ϵ_r = 1.0) and epoxy glass (ϵ_r = 4.7). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, *Figures 3-9c* and *3-9e*, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in *Figures 3-10a* through *3-10f*, exemplify the outstanding immunity to everyday noise which can effect system reliability.

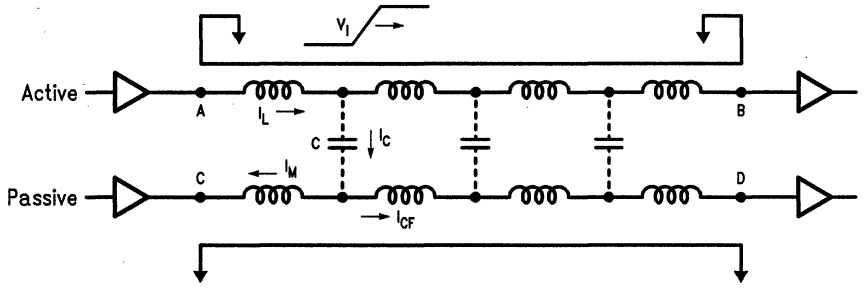


TL/F/10160–61

■ Two parallel signal lines provide mutual inductance and shunt capacitance

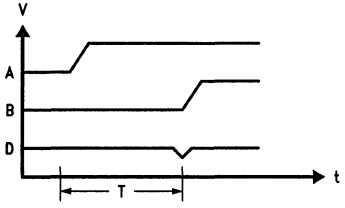
FIGURE 3-9a. Where Does Crosstalk Take Place?

Crosstalk (Continued)



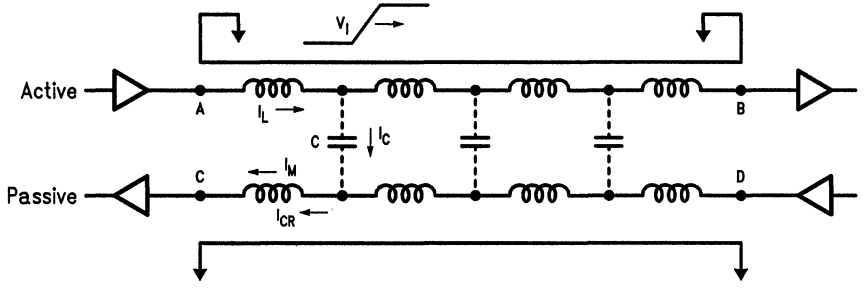
TL/F/10160–62

- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = I_C = -C dV_i/dt
- Mutually Induced Current = I_M = mI_L
- Forward Crosstalk Current = I_{CF}
- As the active signal, V_i, propagates from A to B a negative-going spike, V_f, propagates from C to D, coincident with V_i.



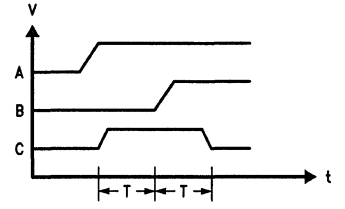
TL/F/10160–63

FIGURE 3-9b. Forward Crosstalk—Refresher



TL/F/10160–64

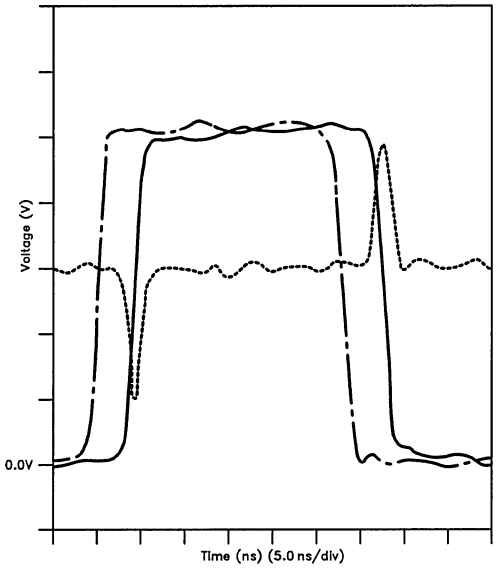
- Current through the Characteristic Inductance of Transmission Line = I_L
- Capacitively Coupled Current = I_C = -C dV_i/dt
- Mutually Induced Current = I_M = mI_L
- Reverse Crosstalk Current = I_{CR}
- As the active signal, V_i, propagates from A to B a positive pulse appears at C for a duration twice the coupled line delay T.



TL/F/10160–65

FIGURE 3-9c. Reverse Crosstalk—Refresher

Crosstalk (Continued)

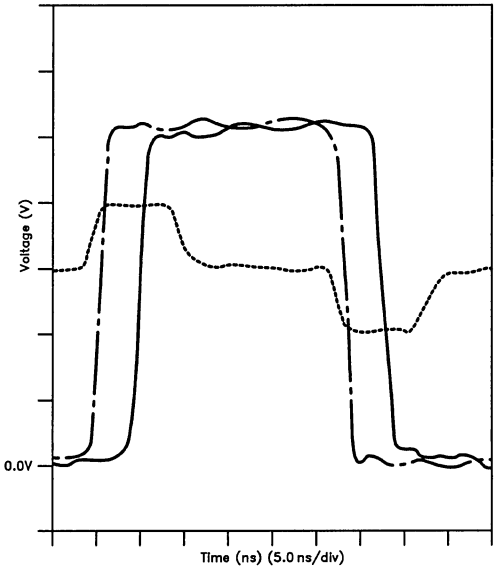


Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Forward Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

TL/F/10160–16

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

FIGURE 3-9d. Forward Crosstalk on PCB Traces



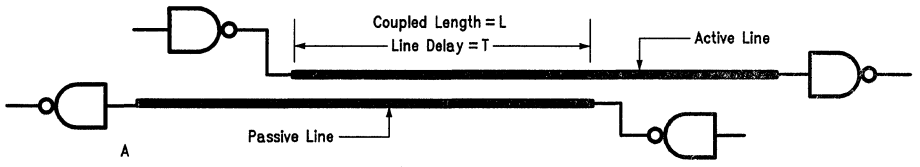
Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Reverse Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

TL/F/10160–17

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

FIGURE 3-9e. Reverse Crosstalk on PCB Traces

Crosstalk (Continued)



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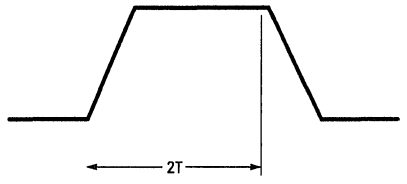
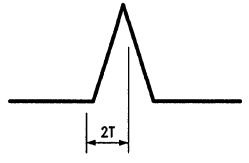
Noise Pulses at A:



For $T > t_r$ Noise Reaches Max Amplitude

TL/F/10160–19



For $T = 0.5\ t_r$ Noise Just Reaches Max at Peak

TL/F/10160–20

For $T < 0.5\ t_r$ Noise Never Reaches Full Amplitude

TL/F/10160–21

FIGURE 3-9f. Partially Coupled Lines

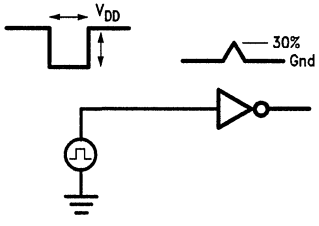


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FIGURE 3-10a. High Noise Margin

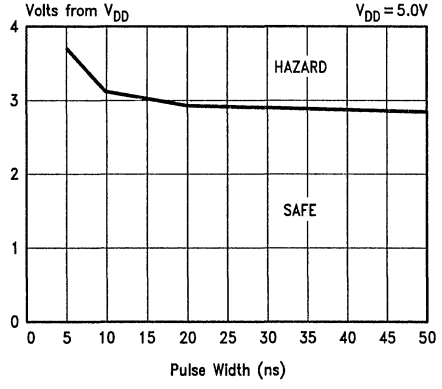

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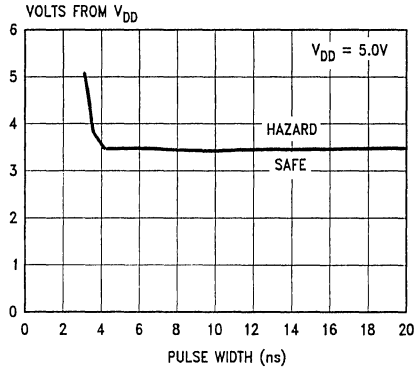
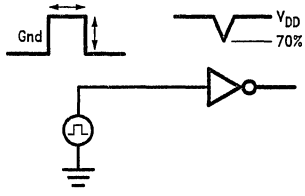
FIGURE 3-10b. FACT AC/ACQ High Noise Margin

Crosstalk (Continued)



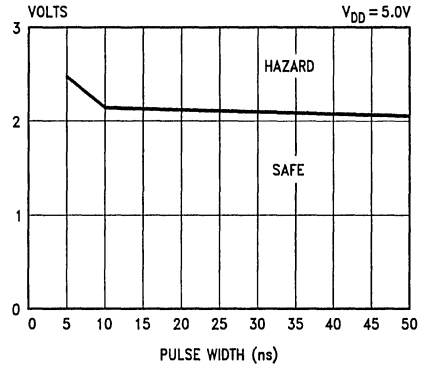
TL/F/10160–66

FIGURE 3-10c. FACT ACT/ACTQ/FCT/FCTA High Noise Margin



TL/F/10160–24

FIGURE 3-10d. Low Noise Margin



TL/F/10160–25

FIGURE 3-10e. FACT AC/ACQ Low Noise Margin

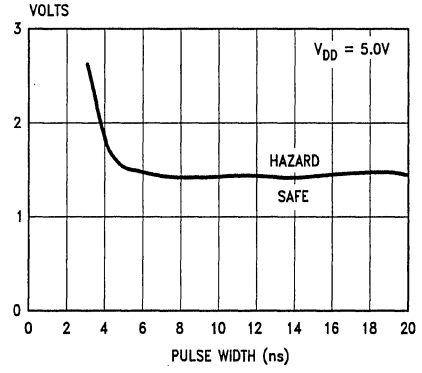


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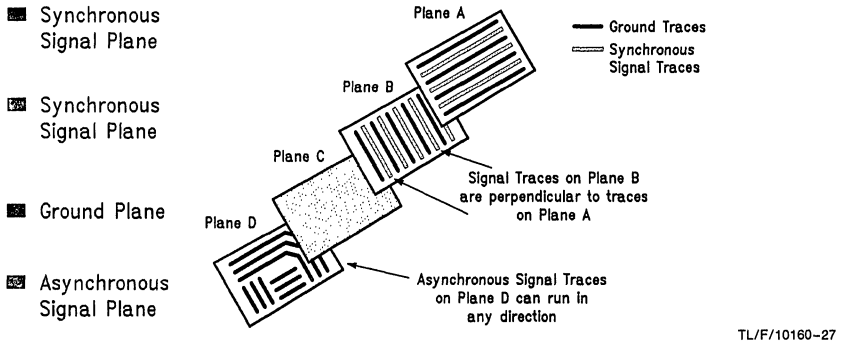
FIGURE 3-10f. FACT ACT/ACTQ/FCT/FCTA Low Noise Margin

With over 2.0V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

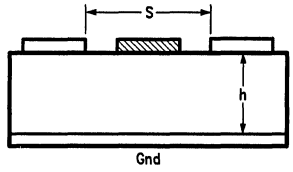
In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.



TL/F/10160–27

FIGURE 3-11a. Recommended Crosstalk—Avoidance Structure

Crosstalk (Continued)



- Minimize parallel trace lengths
- Maximize distance "S" between traces to minimize crosstalk
- Add ground trace between signal traces
- Minimize distance h to keep line impedance low

TL/F/10160–32

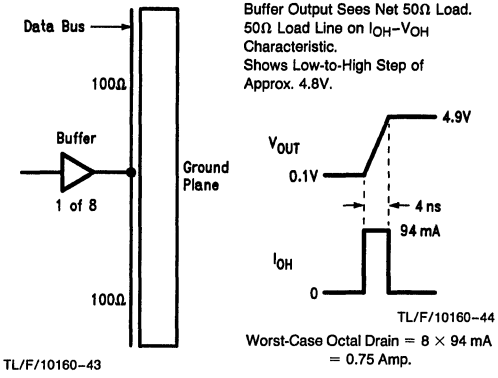
FIGURE 3-11b. PCB Layout Tips for Crosstalk Avoidance

Decoupling Requirements

National Semiconductor Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. *Figure 3-12* displays various V_{DD} and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 50Ω and 100Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{DD} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in *Figure 3-13* to calculate the amount of decoupling necessary. This circuit utilizes an 'AC240 driving a 100Ω bus from a point somewhere in the middle.

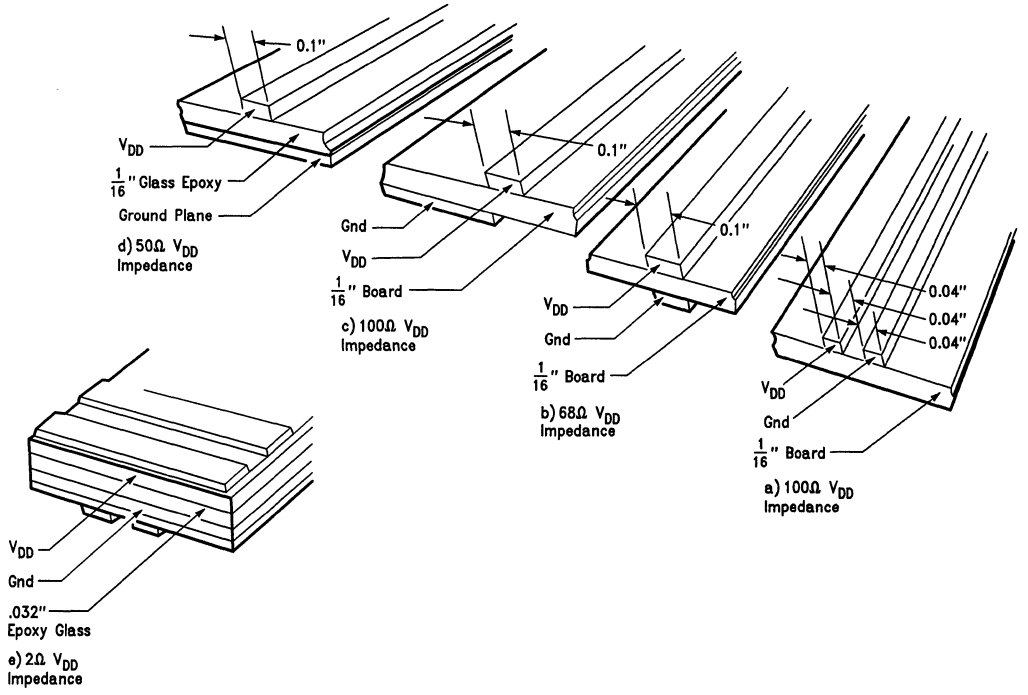


TL/F/10160–43

TL/F/10160–44

Worst-Case Octal Drain = 8 × 94 mA = 0.75 Amp.

FIGURE 3-13. Octal Buffer Driving a 100Ω Bus



TL/F/10160–42

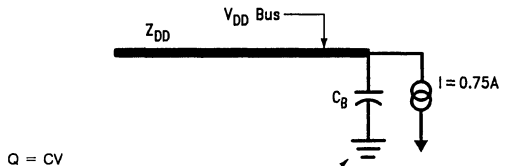
FIGURE 3-12. Power Distribution Impedances

Decoupling Requirements (Continued)

Being in the middle of the bus, the driver will see two 100Ω loads in parallel, or an effective impedance of 50Ω. To switch the line from rail to rail, a drive of 94 mA is needed; more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{DD} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in *Figure 3-14*.

In this example, if the V_{DD} droop is to be kept below 30 mV and the edge rate equals 4 ns, a 0.10 μF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.



$Q = CV$
$I = C\Delta V/\Delta t$
$C = I\Delta t/\Delta V$
$\Delta t = 4 \times 10^{-9}$

Bypass Capacitor
Specify V_{DD} Droop = 30 mV Max

TL/F/10160–45

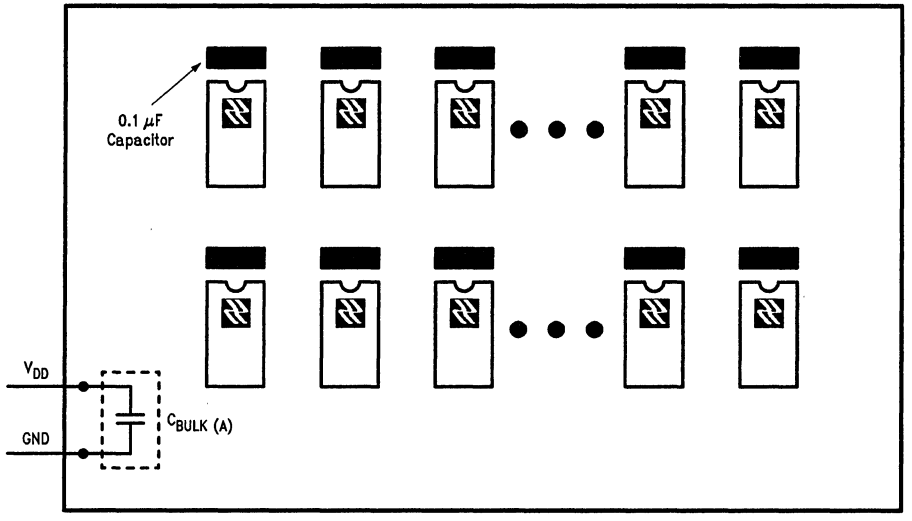
$$C = \frac{0.750 \times 4 \times 10^{-9}}{0.03} = 100 \times 10^{-9} = 0.100\ \mu F$$

Select $C_B \geq 0.10\ \mu F$

FIGURE 3-14. Formula for Calculating Decoupling Capacitors

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.



TL/F/10160–28

- Need to decouple board at the point of power supply entry
- This capacitor (A) will smooth low frequency bulk switching noise
- A large value electrolytic capacitor is typically used (50 μF–100 μF)

FIGURE 3-15. Board-Level Decoupling Capacitor

Electromagnetic Interference

One of the features of advanced CMOS is its fast output edge rates. For the first time a non-ECL logic family is capable of switching outputs at ECL speeds. In fact, advanced CMOS edge rates exceed that of ECL. ECL outputs typically swing 900 mV in 700 ps, translating into an edge rate of 1.3 V/ns. Advanced CMOS outputs, on the other hand, swing 5.0V in approximately 3.0 ns, translating into an edge rate of 1.6 V/ns. Logic families driving at these speeds, however, are more prone to generate higher levels of system noise. Electronic systems using advanced CMOS logic, as with any other high performance logic system, require a higher level of design considerations.

One element of system noise that will be discussed here is referred to as Electromagnetic Interference, or EMI. The level of EMI generated from a system can be greatly reduced with the use of proper Electromagnetic Compatibility (EMC) design techniques. These design considerations begin at the circuit board level and continue through the system level to the enclosures themselves; EMC needs to be a concern at the initial system design stage.

WHAT IS EMI/RFI?

Electromagnetic Interference, or EMI, is an electrical phenomenon where electric field energy and magnetic field energy are transmitted from one source to create interference of transmitted and/or received signals from another source. This may result in the information becoming distorted.

EMI can be an issue of emissions, that is, energy radiated from one system to another or within the same system. It can also be an issue of susceptibility, from high powered microwave signals or nuclear EMP (Electromagnetic Pulse)—an issue more applicable in the military arena than commercial. While this section will specifically address radiated energy, many comments may also apply to susceptibility.

SOURCES OF ELECTROMAGNETIC INTERFERENCE

EMI generation in an electronic system may result from several sources. All mediums of signal transmission—from the signal origin to its destination—are possible sources of radiated EMI. Understanding how each medium—including ICs, coaxial cables, and connectors—can radiate EMI is paramount in effective, high performance system design.

As *Figure 3-16* illustrates, EMI in a typical electronic circuit is generated by a current flowing in some current path configured within the circuit. These paths can be either V_{DD}-to-GND loops or output transmission lines. The propagating current pulse creates magnetic field energy, while the voltage drop across the loop area creates electric field energy. The current path material itself acts as an antenna radiating—or receiving—both the electric and magnetic fields.

EMI generation is a function of several factors. Transmitted signal frequency, duty cycle, edge rate, and output voltage swings are the major factors of the resultant EMI levels. *Figure 3-17* illustrates a generalized Fourier transformation of the transmitted signal from the time domain to the frequency domain. To think in terms of EMI, one must think in terms of the frequency domain. This illustration helps to realize the role of the time domain signal components in the frequency domain. Notice that as the signal's period decreases, duty cycle decreases, or rise/fall time decreases that the radiated bandwidth increases.

On the circuit level, in addition to the signal component factors mentioned earlier, radiating area, and the resultant antenna's radiating efficiency also play an important role in EMI generation. Also, current spikes, power line noise, and output ringing caused by outputs switching also contribute to the overall EMI. Good design techniques that moderate this noise will play a major role in minimizing radiated EMI.

OVERALL SYSTEM EMI

System EMI is a function of the current loop area. Some of the largest loop areas in a system consist of circuit board signal transmission lines, backplane transmission lines, and I/O cables. The current loop areas of the integrated circuit packages—V_{DD}-to-GND loops—are small in comparison to those of the transmission lines and I/O cables. Differences in IC package pinout schemes are much less noticeable in terms of overall system radiated EMI.

The formula used to model the maximum electric field is listed below. This formula takes into account the antenna dimension and efficiency as well as the basic signal components.

$$|E|_{Max} = \frac{1.32 \times 10^{-3} \bullet I \bullet A \bullet Freq^2}{D}\left[1 + \left(\frac{\lambda}{2\pi D}\right)^2\right]^{1/2} \frac{\mu V}{m}$$

where,

$|E|_{Max}$ is the maximum E-field in the plane of the loop

I is the current amplitude in milliamps

A is the antenna area in square cm

λ is the wavelength at the frequency of interest

D is the observation distance in meters

Freq is the frequency in MHz

and the perimeter of the loop $P \ll \lambda$.

Figures 3-18a and *3-18b* illustrate lab measurements of radiated emissions from a test board populated with FACT, FACT QS, and a competitor's ACMOS logic. The device under test is driving a similar device across 26 cm of printed circuit board trace.

At higher frequencies where, for example, quarter wavelengths approach the lengths of transmission lines common in typical backplanes and plug-in cards, FACT QS with its innovative noise supressions circuitry radiates substantially less EMI than other ACMOS logic.

CIRCUIT BOARD DESIGN CONSIDERATIONS

Original equipment manufacturers cannot afford to fail electromagnetic emissions tests. Since these tests are measured outside of the system, precautions to shield the enclosures, I/O cables, and connections are paramount. However, EMI within a system may also cause errors in data trans-

Electromagnetic Interference (Continued)

mission or unreliable system operation. Therefore, good EMC design techniques at the circuit board level are just as necessary.

Designing a system free of all EMI is an overwhelming task. However, considering the following design recommendations at the circuit board level forms a good foundation on which to design a system with good EMC.

- The use of multilayer printed circuit board is a virtual necessity. Two-sided printed circuit board and wire-wrap boards provide no shielding of EMI. Two-sided boards also do not allow the use of power and ground planes. Instead they require the use of high impedance power and ground traces. Planes provide impedances several orders of magnitude lower than that of traces, reducing transient voltage drops in the power distribution and return loops. As a result of these lower voltage drops, power supply induced EMI can also be reduced.
- In addition to the reduced impedance, these power and ground planes have an inherent EMI shielding effect that the large areas of copper provide. With the use of striplines or signal transmission lines sandwiched between the power and ground planes, the designer can take full advantage of the planes' shielding capabilities. To maximize this shielding effect, keep the power and ground plane areas as homogeneous as possible.
- Since plastic provides no EMI shielding, and sockets of any profile provide plenty of lead length, ICs should be soldered directly to the board. Solder power and ground pins directly to the power and ground planes, respectively. Minimize the IC and associated component lead lengths wherever possible.
- Minimizing the number of simultaneously switching outputs will also help to moderate the current pulse amplitude and output ringing.
- Terminating signal traces longer than 8 inches (typical) will minimize reflections and ringing due to those reflections.
- Avoid capacitively coupling signals from one transmission line to another—crosstalk—by avoiding long parallel signal transmission lines. If parallel transmission lines are unavailable, maximize the distance between the two lines, or insert a ground trace. Minimizing the spacing between the signal plane and ground plane will also help reduce crosstalk. For more details, see section on Crosstalk.

POWER SUPPLY DECOUPLING CONSIDERATIONS

Much of a system's radiated EMI may originate from the power supply itself. Propagation of power supply noise throughout a system is a very undersirable situation in any respect, including EMI. Suppression of this power supply noise is highly recommended. Decoupling the power supply at every level, from the system supply distribution network, down to the individual IC, is also a necessity when designing for low noise—and low EMI.

- On the system level, the use of a tantalum or aluminum electrolytic capacitor in the power supply distribution network is recommended.
- Decoupling the power supply at the point of entry onto the printed circuit board is also highly recommended. The use of a low equivalent series inductance, or ESL, multilayer ceramic capacitor, 50 μF to 100 μF, provides good low to medium frequency filtering and EMI suppression.
- To further suppress power supply noise and associated EMI throughout the circuit board itself, the use of a low ESL chip capacitor for each IC is highly recommended. Because the location of any transient noise on a power or ground plane would be impossible to predict, and the IC density of different circuit boards vary dramatically, every IC on these circuit boards should be adequately decoupled. A 0.10 μF chip capacitor, located as close to each ground pin as possible, will provide good high frequency power supply noise filtering and added EMI suppression.

BACKPLANE CONSIDERATIONS

The above discussion emphasized design techniques for printed circuit boards. However, because the backplane may, and usually does, consist of several long signal transmission lines, the same low noise design techniques should be used.

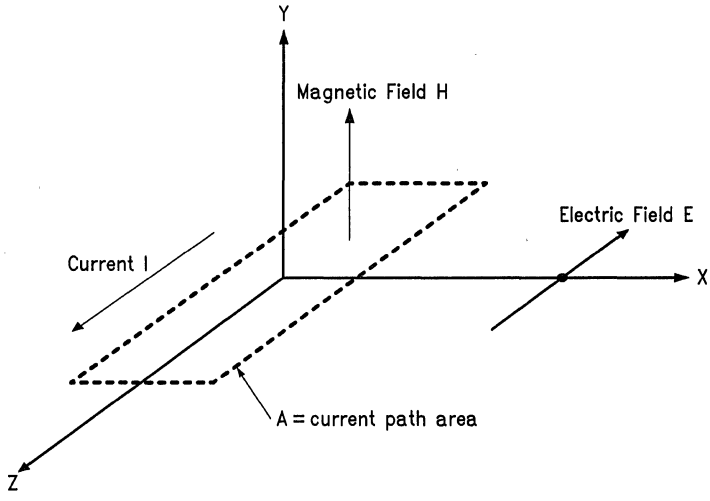
- Multilayer board techniques should also be applied to the backplane. If possible, these transmission lines should be shielded individually. This would allow for a denser parallel layout of transmission lines as well as providing good EMC.
- Use multiple ground and power connections from the backplane to the circuit boards' power and ground planes to minimize the connection impedance. This will help to further suppress any source of power supply generated EMI.

SYSTEM CONSIDERATIONS

One of the major sources of radiated system EMI are the edge connectors, I/O cables, and their associated connectors.

- Use care to ensure that, not only the cables are shielded and the shield properly grounded, but that the shield totally envelopes both the cable and its connectors. The shield should seat firmly into a grounded chassis and touch the chassis a full 360° around the connection. An open ended cable or an improperly grounded connector shield will be a prime suspect for out-of-spec EMI emissions and should be avoided. Use shielded coaxial cables whenever possible. If ribbon cable is preferred, shield all ribbon cables with commercially available ribbon cable shielding. Again, ensure that this shield is properly attached to the connector shield by a full 360°.
- In choosing or designing the enclosure for the system, minimize the number of openings in the enclosure. Since high performance logic now deals with smaller wavelengths than the older technologies, enclosure opening sizes should also be considered. Keep openings as small as possible. If openings are necessary (displays, controls, fans, etc.) there are commercially available accessories that offer good built-in EMI shielding.
- If access panels are necessary, ensure that these panels are properly sealed with some sort of shielding material (gaskets, copper brushes, etc.).
- Of course, the enclosure itself should be of a material that provides good shielding against electric fields.

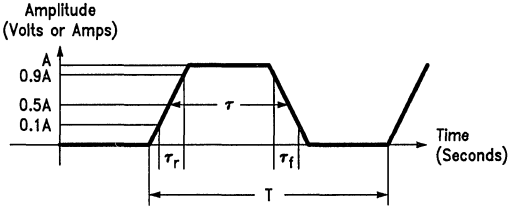
Electromagnetic Interference (Continued)



TL/F/10160–46

FIGURE 3-16. EMI is Generated by a Current Flowing along Some Path (Loop)

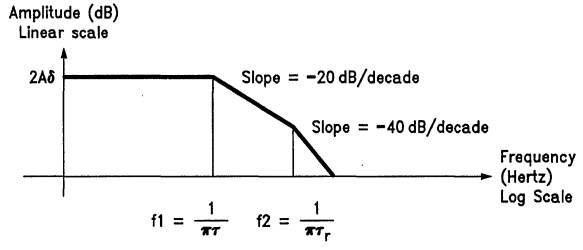
Time Domain: Trapezoidal Pulse Train



TL/F/10160–47

- τ = Pulse Width HIGH
- τ_r = Rise Time
- τ_f = Fall Time
- T = Period
- A = Amplitude

Frequency Domain: Worst-Case Upper Bound Approximation

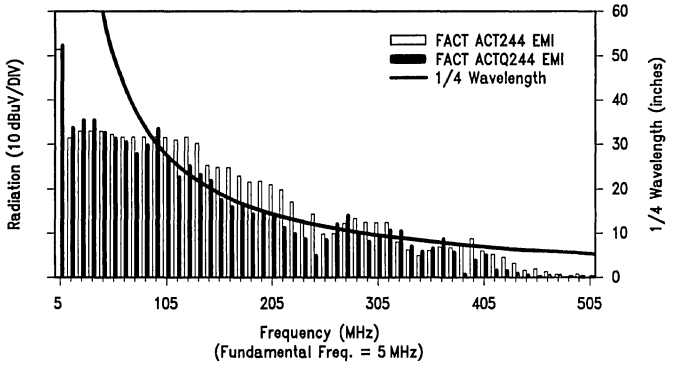


TL/F/10160–48

- f_1 = 1st Breakpoint
- f_2 = 2nd Breakpoint
- δ = Duty Cycle = τ/T

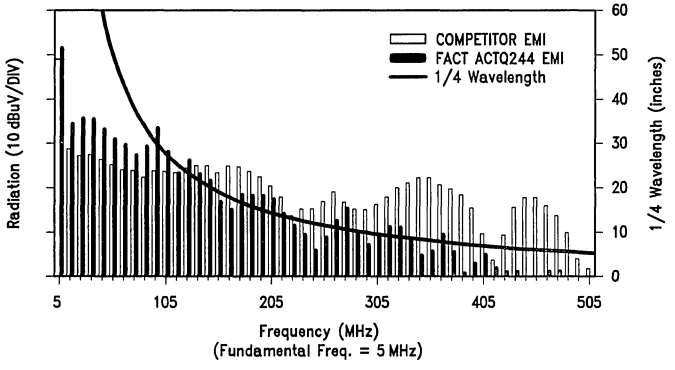
FIGURE 3-17. Time Domain to Frequency Domain Conversion

Electromagnetic Interference (Continued)



TL/F/10160–49

FIGURE 3-18a. FACT Radiation—ACTQ244 versus ACT244



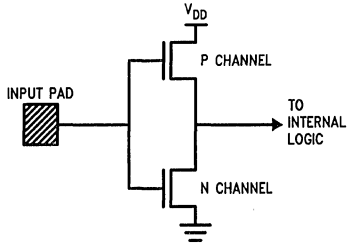
TL/F/10160–50

FIGURE 3-18b. FACT Radiation—ACTQ244 versus Competition

TTL-Compatible CMOS Designs Require Delta I_{DD} Consideration

The FACT product line is comprised of two types of advanced CMOS input circuits: 'AC/'ACQ and 'ACT/'ACTQ/'FCT/'FCTA devices. 'ACT/'ACTQ/'FCT/'FCTA indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As these 'ACT/'ACTQ/'FCT/'FCTA series are used to replace TTL, the I_{DDT} or Delta I_{DD} specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS. In many datasheets I_{DDT} or Delta I_{DD} are also referred to as I_{CCT} or Delta I_{CC}. There are no other differences.

It is important to understand the concept of Delta I_{DD} and how to use it within a design. First, consider where Delta I_{DD} initiates. Most CMOS input structures are of the totem pole type with an n-channel transistor in a series with a p-channel transistor as illustrated below.

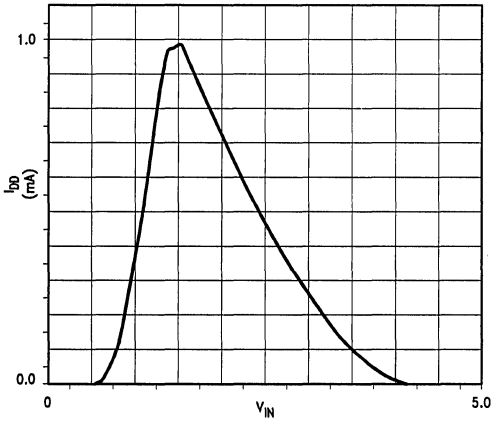


TL/F/10160–52

FIGURE 3-19. CMOS Input Structure

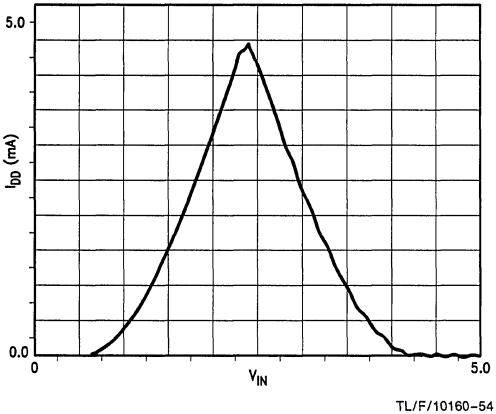
TTL-Compatible CMOS Designs Require Delta I_{DD} Consideration (Continued)

These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an ON transistor is approximately 4 kΩ while the resistance of an OFF transistor is generally greater than 500 MΩ. When the input to this structure is at either ground or V_{DD}, one transistor will be ON and one will be OFF. The total series resistance of this pair will be the combination of the two individual resistances, greater than 500 MΩ. The leakage current will then be less than 1 μA. When the input is between ground and V_{DD}, the resistance of the ON transistor will increase while the resistance of the OFF transistor will decrease. The net resistance will drop due to the much larger value of the OFF resistance. The total series resistance can be as low as 600Ω. This reduction in series resistance of the input structure will cause a corresponding increase in I_{DD} as current flows through the input structure. The following graph depicts typical I_{DD} variance with input voltage for an 'ACT device.



TL/F/10160–53

FIGURE 3-20. I_{DD} versus Input Voltage for 'ACT Devices



TL/F/10160–54

FIGURE 3-21. I_{DD} versus I_{IN} for 'AC Devices

The Delta I_{DD} specification is the increase in I_{DD}. For each input at V_{DD} − 2.1V (approx. TTL V_{OH} level), the Delta I_{DD} value should be added to the quiescent supply current to arrive at the circuit's worst-case static I_{DD} value.

Fortunately, there are several factors which tend to reduce the increase in I_{DD} per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. FAST logic outputs can drive 'ACT-type inputs down to 200 mV and up to 3.5V. Additionally, the typical I_{DD} increase per input will be less than the specified limit. As shown in the graph above, the I_{DD} increase at V_{DD} − 2.1V is less than 200 μA in the typical system. Experiments have shown that the I_{DD} of an 'ACT240 series device typically increases only 200 μA when all of the inputs are connected to a FAST device instead of ground or V_{DD}.

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta I_{DD} specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

Such is the case with parts that have a bidirectional pin, exemplified by the '245 Octal Transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for I_{DD} and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static I_{DD} specification orders of magnitude less than standard load currents. Most CMOS I_{DD} specifications are usually less than 100 μA. When conducting an I_{DD} test, greater care must be taken so that other currents will not mask the actual I_{DD} of the device. These currents are usually sourced from the inputs and outputs.

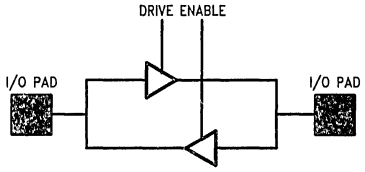
Since the static I_{DD} requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an I_{DD} test. Even a standard 500Ω load resistor will sink 10 mA at 5V, which is more than twice the I_{DD} level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during I_{DD} tests.

Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, I_{DD} can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly ON, and a conduction is created from V_{DD} to ground. This conduction path

Testing Advanced CMOS Devices with I/O Pins (Continued)

leads to the increased I_{DD} current seen in the I_{DD} vs V_{IN} curve. When the input is at either rail, the input structure no longer conducts. Most I_{DD} testing is done with all of the inputs tied to either V_{DD} or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual I_{DD} of the device under test which is being measured by the tester.

When testing the I_{DD} of a CMOS '245, problems can arise depending upon how the test is conducted. Note the structure of the '245's I/O pins illustrated below.



TL/F/10160–55

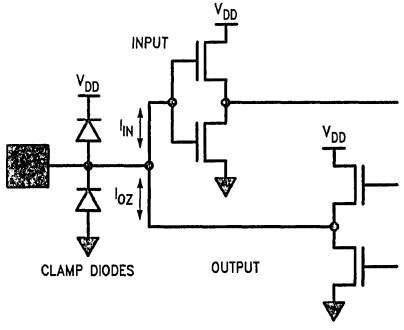
FIGURE 3-22. '245 I/O Structure

Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the I_{DD} of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from V_{DD} to ground. A simple rule to follow is to treat any output which is disabled as an input. This will help insure the integrity of an I_{DD} test.

Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted below.

The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined I_{IN} specification of the input and the I_{OZ} specification of the output. This combined leakage test is defined as IOZ_T. For FACT devices, I_{IN} is specified at ± 1 μA while I_{OZ} is specified at ± 5 μA. Combining these gives a limit of ± 6 μA for I/O pins. Usually, I/O pins will show leakages that are less than the I_{OZ} specification of the output alone.



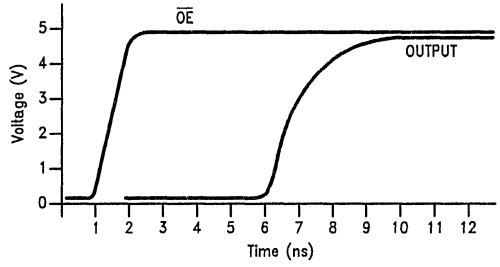
TL/F/10160–56

FIGURE 3-23. I/O Pin Internal Structure

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

Testing Disable Times of TRI-STATE® Outputs in a Transmission Line Environment

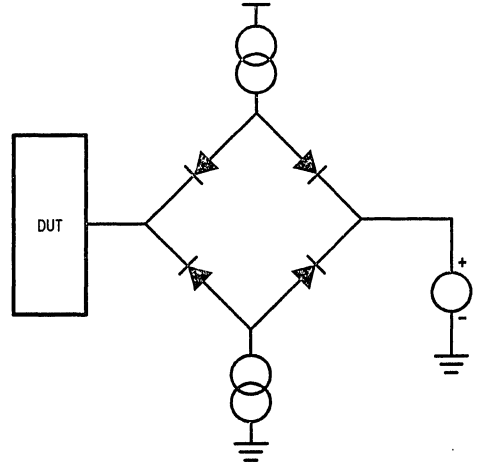
Traditionally, the disable time of a TRI-STATE buffer has been measured from the 50% point on the disable input, to the (V_{OL} + 0.3V) or (V_{OH} − 0.3V) point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown below.



TL/F/10160–57

FIGURE 3-24. Typical Bench TRI-STATE Waveform

ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. The following figure illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.



TL/F/10160–58

FIGURE 3-25. MCT Wheatstone Bridge Test Load

Testing Disable Times of TRI-STATE® Outputs in a Transmission Line Environment (Continued)

The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL}. When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the (V_{OL} + 0.3V) level or fallen to the (V_{OH} − 0.3V) level.

Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in *Figure 3-26.*

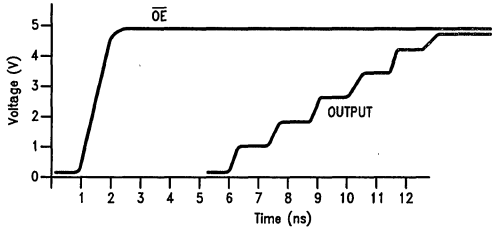


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FIGURE 3-26. Typical ATE TRI-STATE Waveform

Transmission line theory states the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of 50Ω to 60Ω, this voltage step can be as minimal as 250 mV. If the comparator was programmed to the disable measurement points, it would be looking for a step of approximately 575 mV at 5.5V V_{DD}. Three reflections of the current pulse would be required before the comparator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customer's incoming tests, even though the device meets specifications. The figure below graphically shows this stepout.

Point A represents the typical 50% measurement point on tester driven waveforms. Point B reprsents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become nonrepeatable.

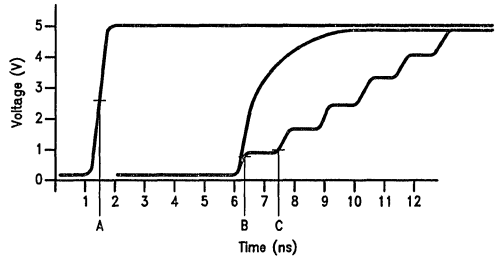

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FIGURE 3-27. Measurement Stepout

Understanding Latch-Up in Advanced CMOS Logic

National Semiconductor
Application Note 600

Latch-up has long been a bane to CMOS IC applications; its occurence and theory have been the subjects of numerous studies and articles. The applications engineer and systems designer, however, are not so much concerned with the theory and modeling of latch-up as they are with the consequences of latch-up and what has been done by the device designer and process engineer to render ICs resistant to latch-up.

Of equal interest are those precautions, if any, which must be observed to limit the liability of designs to latch-up.

WHAT IS LATCH-UP?

Latch-up is a failure mechanism of CMOS (and bipolar) integrated circuits characterized by excessive current drain coupled with functional failure, parametric failure and/or device destruction. It may be a temporary condition that terminates upon removal of the exciting stimulus, a catastrophic condition that requires the shutdown of the system to clear or a fatal condition that requires replacement of damaged parts. Regardless of the severity of the condition, latch-up is an undesirable but controllable phenomenon. In many cases, latch-up is avoidable.

The cause of the latch-up exists in all junction-isolated or bulk CMOS processes: parasitic PNPN paths. *Figure 1*, a basic CMOS cross section, shows the parasitic NPN and PNP bipolar transistors which most frequently participate in latch-up. The P+ sources and drains of the P-channel MOS devices act as the emitters (and sometimes collectors) of lateral PNP devices; the N-substrate is the base of this device and collector of a vertical NPN device. The P-well acts as the collector of the PNP and the base of the NPN. Finally, the N+ sources and drains of the N-channel MOS devices serve as the emitter of the NPN. The substrate is normally connected to V_{CC}, the most positive circuit voltage, via an N+ diffusion tap while the P-well is terminated at Gnd, the most negative circuit voltage, through a P+ diffusion. These power supply connections involve bulk or spreading resistance to all points of the substrate and P-well.

Normally, only a small leakage current flows between the substrate and P-well causing only a minute bias to be built up across the bulk due to the resistivity of the material. In this case the depletion layer formed around the reverse-biased PN junction between P-well and the substrate supports the majority of the V_{CC}-Gnd voltage drop. As long as the MOS source and drain junctions remain reverse-biased, CMOS is well behaved. In the presence of intense ionizing radiation, thermal or over-voltage stress, however, current can be injected into the PNP emitter-base junction, forward-biasing it and causing current to flow through the substrate and into the P-well. At this point, the NPN device turns on, increasing the base drive to the PNP. The circuit next enters a regenerative phase and begins to draw significant current from the external network thus causing most of the undesirable consequences of latch-up. Once established, a latch-up site, through the fields generated by the currents being conducted, may trigger similar action in both elements of the IC.

WHAT TO DO

As might be expected, latch-up is highly dependent on the characteristics of the bipolar devices involved in the latch-up loop. Device current gains, emitter efficiencies, minority carrier life times and the degree of NPN-PNP circuit coupling are all important factors relating to both the sensitivity of the particular latch-up device and to the severity of the failure once it has been excited. Layout geometry and process both contribute significantly to these parameters; CMOS, like other technologies, has been shrunk to provide more function per unit area, increasing susceptibility to latch-up. All major CMOS vendors have upgraded their processes and/or design rules to compensate for this increased susceptibility, some with more success than others. The lateral PNP is typically the weak link in the latch-up loop. As such, various devices can be exploited toward reducing the effectiveness of the PNP to participate in latch-up. Guard banding, device placement, the installation of pseudo-collectors between the P-channel devices and the P-well, and the use of a low resistivity substrate under an epitaxial layer are a few of the IC design tactics now being practiced to reduce the current gain or to control the action of the lateral PNP structures in state-of-the-art CMOS devices.

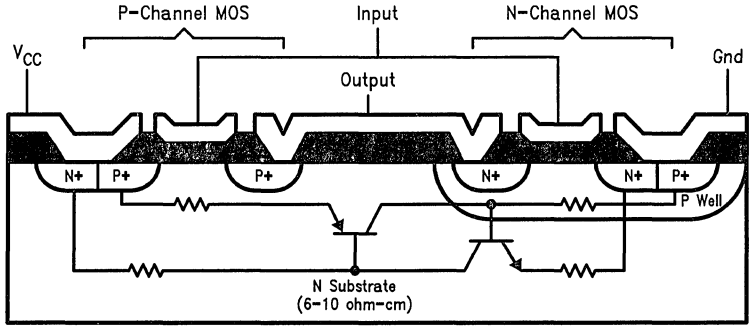

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FIGURE 1. Basic CMOS Inverter Cross Section with Latch-Up Circuit Model

Vendors of CMOS ICs have always been aware of the latch-up phenomenon and have considerably improved their designs and processes to reduce the danger of latch-up occuring under normal usage. Abnormal applications and misuse of CMOS ICs may still pose problems that the CMOS vendor has little control over. Hence, CMOS users must be aware of what they are doing and those measures which must be taken to reduce the susceptibility to latch-up. The use of CMOS at or beyond its rated maximum voltage range and the presence of inductive transients are applications-related situations which can trigger latch-up. Environment, including thermal stress, poorly regulated or noisy supplies and radiation incidence can also contribute to or cause latch-up. The system engineer must consider these situations when using CMOS in designs.

While latch-up is generally recognized as resulting from regenerative switching along a PNPN path, many designers incorrectly assume that this regenerative action places the device in a state that can only be recovered from if the system is powered down. The fact is that there is probably an equal, if not greater, chance that the regenerative switching, when encountered, will be non-sustaining (the condition, more accurately referred to as current amplification, will disappear when the triggering stimulus is removed); over-voltage applied to properly designed input protection networks is one example of controlled current amplification. For sustained latch-up to occur, the regeneration loop must have sufficient gain and the power source must be able to supply a minimum current. From this we can see that current-limited power supplies might be used to recover from or reduce the effects of latch-up. Another method uses current-limiting series resistors in the power connections of offending ICs in conjunction with storage capacitors shunting the devices. Normal switching current will be drawn from the capacitors while DC current will be limited by the resistors.

In the loop of positive current feedback formed by the parasitic PNP and NPN transistors of the latch-up structures, regenerative switching may result if sufficient loop gain is available. One must remember, though, that three conditions are necessary for latch-up to occur.

1) both parasitic bipolars must be biased into the active state;
2) the product of the parasitic bipolar transistor current gains ($B_{npn} \bullet B_{pnp}$) must be sufficient to allow regeneration, i.e., greater than or equal to one;
3) the terminal network must be capable of supplying a current greater than the holding current required by the PNPN path. In processes utilizing an epitaxial silicon, this current is usually in excess of 1A.

If any of these conditions is not met both during the initiation and in the steady state, then the latch-up condition is either non-sustaining or cannot be initiated. If the current to the latched structure is not limited, permanent damage may result. Again, any means to prevent any of these conditions from being satisfied will protect the circuit from exhibiting sustained latch-up.

The prevention of biasing the bipolars into the active region and the limiting of the current which may be supplied by the network are the two factors which system designers have under their control. Many of the protective measures long exercised in discrete and TTL designs may also be applied to CMOS designs to reduce susceptibility and prevent damage to these systems. Diode clamping of inductive loads, signal and supply level regulation, and sharing of large DC loads by several devices with suitable series limiting resistors to distribute thermal stress over a larger area or multiple ICs are all positive-preventive measures to exploit.

While we have been considering the CMOS device in a generic manner, there are two primary structures used in all CMOS ICs which have latch-up paths associated with them; these are the inverter or gate and the transmission switch. Both structures may be susceptible under the right conditions. While the CMOS inverter can exhibit latch-up independent of circuit configuration, the transmission switch usually has lower holding current, and thus, a lower threshold for latch-up, but is dependent on its external connections for latch-up to occur. *Figure 2* shows the lumped equivalent circuit of the inverter. Notice the shunting resistors across the base-emitter junctions of the bipolar transistors: these resistors divert base drive from the bipolars and as a result increase both the trigger current and holding current levels required for the structures to participate in latch-up. A further increase in these current levels can be achieved by further decreasing the shunt resistance. Diffusing all active components into an epitaxial silicon, under which would lie a substrate of substantially less resistivity, will have a dramatic effect on decreasing the shunt resistance, therefore increasing the trigger current and holding current levels required for latch-up.

THE CIRCUIT CONNECTION

As we have seen above, the external circuit connections are regular participants in the latch-up process. The current for latch-up comes from these connections and often the triggering mechanism is external to the latching device. All three classes of external connections (power, input and output) are important in latch-up. We will now look at how these connections relate to this process.

Current injection through the power terminals when the power supply voltage is beyond the maximum rated for the CMOS device can directly cause latch-up through base collector leakage or breakdown mechanisms. One aspect of high power supply voltages that is not often recognized is the effect of field-aiding lateral currents under the emitters of the PNP devices. This can effect a significant increase in the beta of these devices, making internally trigger latch-up much more prevalent. Again, the warning to the the system designer is to avoid using CMOS at maximum rated supply voltages unless precautions are taken to insure latch-up is unlikely or is at least acceptable and recoverable. Switching transients coupled onto power lines has become a problem

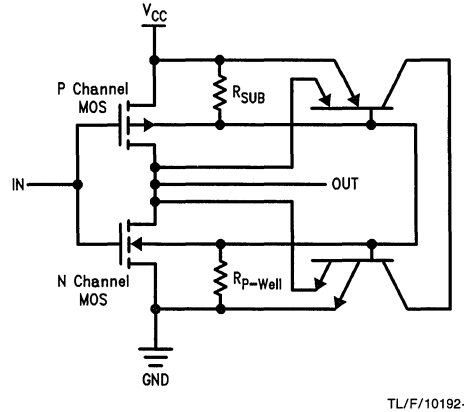

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FIGURE 2. CMOS Inverter with Parasitic Bipolars

now that CMOS has become a high-speed logic technology. Attention to power supply decoupling is now a necessity when designing with high-speed CMOS. Of course, CMOS processes incorporating an epitaxial silicon over a substrate of very low resistivity is less prone to latch-up under these conditions. These recommended precautions should be taken just the same.

Latch-up involving input terminals, next to gate oxide rupture, used to be one of the most common failure mechanisms of CMOS. Transients exceeding the power supply routinely caused either or both of these effects to occur. Fortunately, CMOS vendors have learned to make better input protection networks and have learned that proper placement of these components with respect to the rest of the chip circuitry is necessary to reduce susceptibility to latch-up. The system designer should review foreign input signals to CMOS systems and take precautions necessary to limit the severity of over/undershoot from these sources. Measures which could be used to reduce the possibility of latch-up induced by input signals are: proper termination of transmission lines driving CMOS, series current limiting resistors, AC coupling with DC restoration to the CMOS supplies, and the addition of Schottky diode clamps to the CMOS power rails. As an additional measure there are several CMOS circuits which have input protection networks that can handle overvoltage in one direction or the other and which are specifically designed to act as interface circuits between other logic families and CMOS. Judicious application of these will also aid in suppressing any tendencies of CMOS systems to latch-up.

Finally, attention to CMOS outputs, their loading and the stresses applied to them will also enable the designer to generate latch-up free systems. Historically, output terminals of CMOS have been least likely to cause latch-up though they can participate in latch-up once it is initiated. The normal mode of failure in this respect is, again, the application of voltages beyond the CMOS supplies or the maximum limit for the devices though excessive current has also been linked to latch-up failure at elevated temperatures. Inductive surges and transmission line reflections are the most likely sources of output latch-up in CMOS and should be attended to in the most applicable method, i.e., by clamping, termination or through dissipative measures.

WHAT WE HAVE DONE

National Semiconductor, as an important supplier of advanced CMOS to all segments of the industry, has made a commitment to provide IC designs which make use of state-of-the-art latch-up suppression techniques in an effort to support its customers before they need support. The three most important actions which we have taken to guard our customers from latch-up are in the areas of layout, power distribution and process design. These techniques, along with recognized good design practice, yield a product line that lives up to the intent of an advanced CMOS family. In brief review, National Semiconductor's attack on latch-up is summarized in the following.

Latch-Up Protection Geometries

Every FACT™ IC employs special geometries to isolate every input protection device and every output from active areas on the chip. In this way, structures which would normally participate in latch-up loops are decoupled and are thus less troublesome. All devices are scrutinized for potential latch-up sites and are protected by similar geometries where any risk is significant.

Power Distribution

Careful attention to on-chip power distribution and enhanced termination of P-wells and substrate is used by National Semiconductor to improve latch-up resistance. Our double metal process affords the advantage in maintaining low impedance distribution of power and ground potentials over the entire chip; the potential gradient-caused fields which often induce or enhance latch-up are thus minimized while functional performance is enhanced by cleaner on-chip power supplies.

Process Design

By design, the FACT process is better both in low latch-up susceptibility and in enhanced device performance. The most significant advancement of the FACT process has been the incorporation of an epitaxial silicon layer. *Figure 3* illustrates a modified version of *Figure 1*, utilizing an epitaxial layer of silicon to contain all of the active components of the CMOS circuit. This epitaxial layer allows the use of a separate layer of substrate silicon, of a resistivity some three orders of magnitude lower than the epitaxial layer. The effect is also modeled in *Figure 3*.

As illustrated, the resistivity of the epitaxial silicon, R_1, is on the order of 6 ohm-cm to 10 ohm-cm. The underlying substrate resistivity, R_2, is as low as 0.008 ohm-cm to 0.025 ohm-cm. The result is a parallel combination of resistivities, R_1 and R_2, that is equivalent to R_2. What has now happened is that the gain of the parasitic PNP-NPN circuit has been dramatically slashed. Under the same latch-up conditions described earlier, the introduction of the low resistivity substrate now means that at least 10 times more current is needed to trigger the parasitic PNP-NPN combination.

The active components within the epitaxial layer maintain the same performance characteristics as those of the active area illustrated in the non-epitaxial CMOS circuit of *Figure 1*. Therefore the introduction of the epitaxial layer to the FACT process does not reduce any AC, DC, functional or ESD performance. However, what we have is an advanced CMOS logic family that is now virtually latch-up immune.

Thus, through innovative and careful layout, attention to eliminating circuit situations which could be latch-up prone and by careful selection and maintenance of our advanced CMOS process, FACT sets the standard for latch-up resistance.

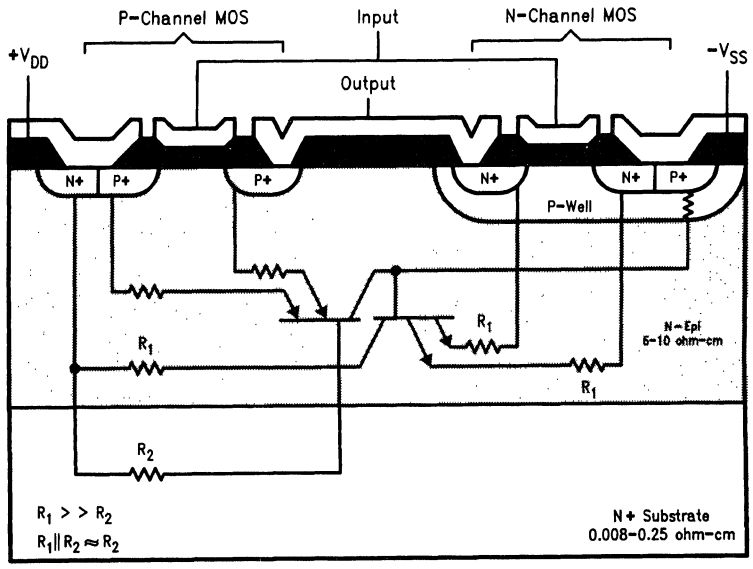

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FIGURE 3

Terminations for Advanced CMOS Logic

National Semiconductor
Application Note 610
Raghu Rao

INTRODUCTION

Advanced CMOS logic such as National Semiconductor's FACT (Fairchild Advanced CMOS Technology) logic, has extended CMOS performance to the level of advanced bipolar technologies. While high-performance design rules that are currently utilized for bipolar designs are also applicable to CMOS, power consumption becomes a new area of concern in high-performance system designs.

One advantage of using advanced CMOS logic is its low power consumption. However careless circuit design can increase power consumption, possibly by several orders of magnitude. A simple FACT gate typically consumes 625 μW/MHz of power; at 10 MHz, this translates to 6.25 mW. A 50Ω parallel termination on the line will use over 361 mW with a 50% duty cycle.

The use of high-performance system board design guidelines is important when designing with advanced CMOS families. Because of advanced CMOS logic edge rates (less than 3 ns–4 ns), many signal traces will exhibit transmission line characteristics.

A PCB trace begins to act as a transmission line when the propagation delay (t_{pd}) across the trace approaches one third of the driver's edge rate. For advanced CMOS, lines as short as 6 to 8 inches may exhibit these effects. This rule encompasses many traces on a standard PCB. With older CMOS technologies which have lower edge rates, this critical length is much longer: 18 inches for 74HC and 5 feet for CD4000 series and 74C devices. A transmission line terminating into a mismatched impedance could result in transient noise which adversely affects signal integrity.

The FACT family also features guaranteed line driving capability. The I_{OLD}/I_{OHD} specifications guarantee that a FACT device can drive incident wave voltage steps into line impedances as low as 50Ω. The I_{OLD} specifications do not guarantee incident wave switching into bipolar level inputs since the input low thresholds are 500 mV to 850 mV lower than CMOS. Due to the relatively linear behavior of the outputs below 1V, CMOS devices can drive incident voltages, adequate for bipolar inputs, into line impedances as low as 80Ω. For line impedances lower than 80Ω, termination can be used to provide adequate input levels. Thus besides reducing noise transients, terminations could also be used to interface between devices from different technologies.

Five possible termination schemes are presented with their impact on power dissipation and noise reduction. *Figure 1* illustrates these schemes.

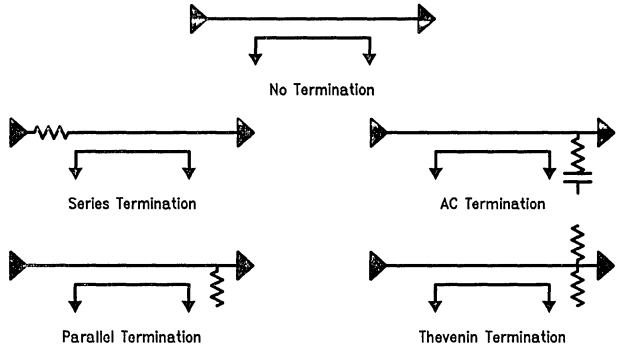

FIGURE 1. Termination Schemes

NO TERMINATION

No termination is the lowest cost option and features the easiest design. For line lengths 8 inches or less, this is often the best choice. For lines longer than 8 inches, transmission line effects (line delays and ringing) may exist. *Figure 2* illustrates the effect of a FACT device driving a 3-foot open-ended coaxial line. Clamp diodes at the inputs of most logic devices tend to reduce the ringing and overshoots. Often, these clamp diodes are sufficient to insure reliable system operation. *Figure 3* illustrates the impact of these diodes on the same 3-foot coaxial line. However, it is not uncommon to find logic devices like DRAMs, D-to-A converters and PLDs, that have no input clamp diodes.

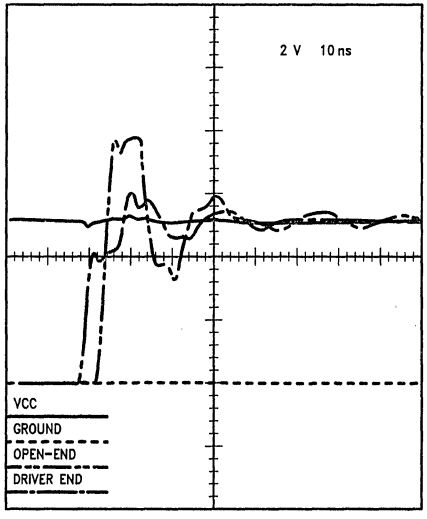

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FIGURE 2. Transmission Line Effects FACT Driving 3 Foot Open-Ended Coax

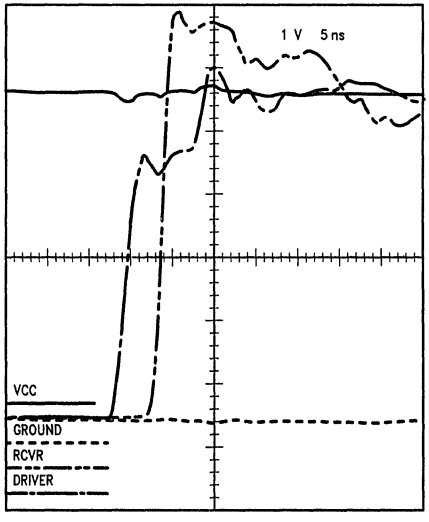

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FIGURE 3. Effects of Input Clamp Diodes FACT Driving FACT with no Termination

PARALLEL TERMINATION

Parallel termination provides an AC and DC current path back to the power supply for switching currents. While it effectively reduces ringing *(Figure 4)*, the DC path to ground or to V_{CC} will dissipate power. The power consumption for this type of a termination scheme has some important implications. For proper impedance matching the value of this terminating resistor should be equal to the characteristic impedance of the line.

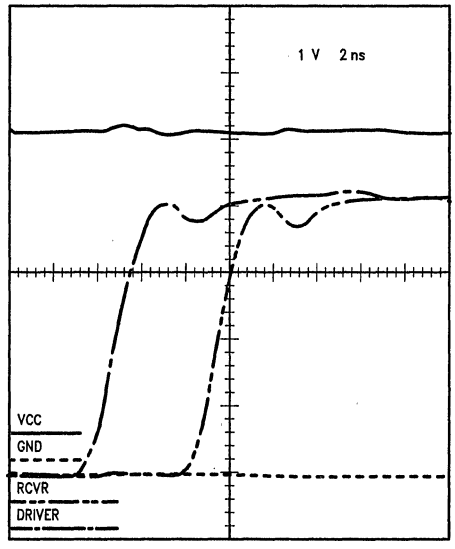

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FIGURE 4. FACT Driving FACT with Parallel Termination

The DC component to the power consumption is a function of the signal duty cycle. Signals with lower duty cycles will dissipate less DC power. Since the load seen by the driving device is resistive, not capacitive, load capacitance does not affect power consumption. Therefore, parallel termination dissipates less AC power. Because of this lower AC power at high frequencies, parallel terminations may consume less power than no termination. Depending upon the load capacitance, signal duty cycle, and line impedance, this frequency can be as low as 40 MHz.

There are drawbacks associated with parallel termination. The maximum DC current allowed into or out of any FACT output is 50 mA. This limits the allowable resistor values to greater than 100Ω. Even though this ringing may not be excessive, imperfect impedance matching may cause ringing on lines with an impedance less than 100Ω. However, because the high-power dissipation of this termination scheme negates the advantages of advanced CMOS logic, this is not an intended advanced CMOS application.

Parallel termination tends to unbalance CMOS outputs. Using a resistor to ground, the CMOS device will achieve a 0.0V output low voltage (V_{OL}). But due to the high DC load in the logic HIGH state, the output high voltage (V_{OH}) will be degraded *(Figure 4)*. This degraded high level output will be above the input high voltage (V_{IH}) of both CMOS and bipolar inputs due to the guaranteed dynamic current (V_{OHD}) specifications (75 mA @ 3.85V, V_{CC} = 5.5V). This lower V_{OH} level may cause an increase in I_{CC} if the driven device is CMOS; however, this increase should be minimal.

THEVENIN TERMINATION

Thevenin termination is similar to parallel termination, except that both pull-up and pull-down resistors are used. Power consumptions are also similar for both of these schemes. The difference is that the DC power consumption is a function of duty cycle and resistor ratios. If the resistors are matched, DC power consumption is not dependent upon duty cycle. One advantage Thevenin termination has over parallel termination is that lines with impedances as low as 50Ω can be terminated in their characteristic impedances. For proper impedance matching, the equivalent thevenin resistance should be the same as the line characteristic impedance.

Thevenin termination does not create unbalanced CMOS outputs, although it reduces the output swing *(Figure 5)*. This limited output swing may increase current consumption in a driven CMOS device however this increase is minimal.

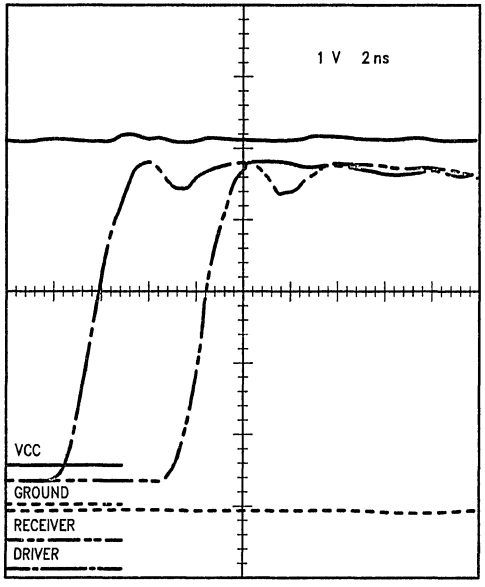

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FIGURE 5. FACT Driving FACT with Thevenin Termination

Busses using Thevenin termination should not be left floating. A floating bus level is determined by the ratio of the resistors. If this level is close to any input threshold, output oscillations and I_{CC} increase may occur. If the bus must be left floating, the resistor ratio should be chosen so that an adequate noise margin is insured. The bus could be left floating by either turning off the driver or by placing the bus in a high impedance state.

Other terminations which do not introduce DC current paths may be more suitable to CMOS systems. These include series and AC parallel terminations.

SERIES TERMINATION

Series termination works by limiting the current that is put into a line. While other termination circuits dissipate extra power, series termination reduces power consumption and dissipates less energy than no termination. This is a recommended termination scheme for the FACT family because of its low power dissipation.

Series termination assumes that any voltage step driven into a transmission line will double at the receiver. Therefore, the initial voltage step driven into the line is one-half of the receiver input voltage. The resistor value can be computed by $R_S = Z_O - R_D$, where R_S is the resistor value, Z_O is the line impedance and R_D is the driver resistance. *Figure 6* illustrates the waveforms associated with series termination.

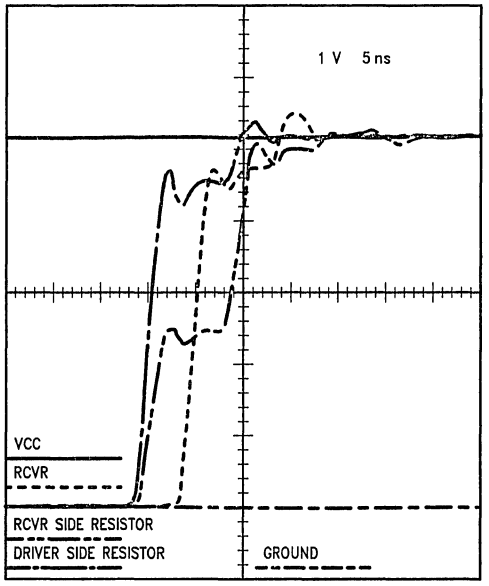

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FIGURE 6. FACT Driving FACT with Series Termination

While the device output produces a full output step, only half of that is driven into the line. At the receiver end, the edge doubles, thus recreating the full output swing. The initial step then reflects back, fixing the full output voltage applied on the entire line. A voltage plateau is created at the input to the line whose width will be twice the line t_{pd}.

Series termination is well suited for lines with a single driver receiver pair. Series termination limits the initial voltage step, which offers several benefits: reduced power consumption and decreased cross-coupled radiated noise.

One possible drawback to series termination is that any other receiver located near the driver will see the voltage plateau. Because the plateau level may be very close to the typical CMOS threshold (50% of V_{CC}), any such input could see multiple input switching. Combinatorial outputs may oscillate, or clocked inputs may experience multiple clocking.

One solution is to choose the resistor value that keeps the initial voltage step away from the input thresholds. Larger resistor values will require one or more reflections to settle out, while still maintaining valid V_{IN} levels at the inputs. Smaller values will generate overshoot and undershoot.

AC PARALLEL TERMINATION

AC Parallel termination is another technique which blocks the DC path to ground. A capacitor in series with the parallel termination resistor blocks the DC path, while maintaining the AC path. This is a highly recommended termination scheme for the FACT family because of its negligible DC power consumption.

After the initial voltage step, the capacitor will charge up to the rail voltage at a rate determined by the RC time constant of the circuit *(Figure 7)*.

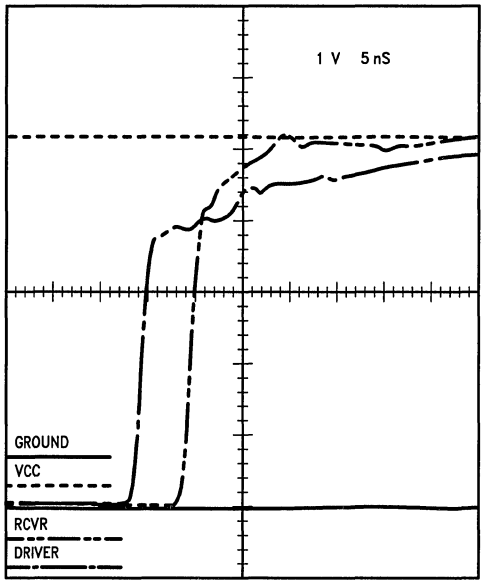

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FIGURE 7. FACT Driving FACT with AC Termination

The capacitor value needs to be carefully determined. If the RC time constant is too small, the RC circuit will act as an edge generator and will create overshooting and undershooting. While increasing the capacitor reduces overshoot, it also increases power consumption. As a rule, the RC time constant should be greater than 3 times the line delay.

When driving TTL-level inputs, the same threshold concerns arise as with no termination. The I_{OLD} current specifications guarantee incident wave switching into CMOS inputs on line impedances as low as 50Ω. For TTL-level inputs, this minimum line impedance rises to 80Ω. When the line impedance is less than 80Ω, a termination value greater than the line impedance will increase the amplitude of the initial voltage step; this can be used to guarantee incident wave switching into both TTL and CMOS-level inputs. Large resistor values will cause ringing on the line, but the amplitude should be small and not present any problems.

At lower frequencies, this termination capacitance increases the total signal trace impedance; therefore, it also increases the slope of the power consumption curve. At higher frequencies, the capacitor is unable to fully charge or discharge, and the slope of the curve falls off. At very high frequencies, AC parallel termination acts like a parallel resistor tied to an intermediate voltage supply, with the voltage level determined by the signal duty cycle. The slope of the power consumption curve is dependent on C_{PD} (Power dissipation capacitance) of the device. The power crossover point between no termination and AC termination may be as low as 15 MHz, depending upon the system capacitive loading and the signals' duty cycle.

POWER CONSUMPTION

The use of one of these termination schemes will affect the power consumption of the system. Power consumption depends upon the circuit used, signal frequency, device and signal trace loads, signal duty cycle, system V_{CC} and component values.

Figure 8 shows the power consumption of each type of termination circuit over a frequency range. For low frequency signals, termination circuits without DC components will usually use less power (no termination, series termination and AC parallel termination). At higher frequencies, parallel termination or AC termination may consume less power because of lower AC power consumption. The AC power consumption of these two termination schemes is a function of the device C_{PD}, while the AC power consumption of the other termination schemes is a function of both the device C_{PD} and the system capacitive loading (C_L). The AC power consumption of AC parallel termination at low frequencies also includes the termination capacitance. The signal used for these curves has a 50% duty cycle. The DC power consumption of the parallel termination will drop as duty cycles drops. For very low duty cycle signals, this scheme may consume the least amount of power.

For low frequencies, the slope of the AC parallel termination curve is greater than any other. This is because it is a function of the device C_{PD}, the capacitive loading (C_L), and the termination capacitance (C_T). But at higher frequencies where the pulse width is less than the RC time constant, the slope drops off. At some frequency less than that of parallel termination, AC parallel termination will use less power than using no termination. At some higher frequency, this circuit uses less power than series termination.

SUMMARY

With new advanced CMOS logic families, power consumption has become an important issue in high-performance systems. Because of the need to use termination, system designers need to be aware of how these circuits affect the power consumption of their systems. The power consumption of the termination scheme will vary, depending upon frequency, duty cycle, line impedance, loading and other factors *(Figure 8)*.

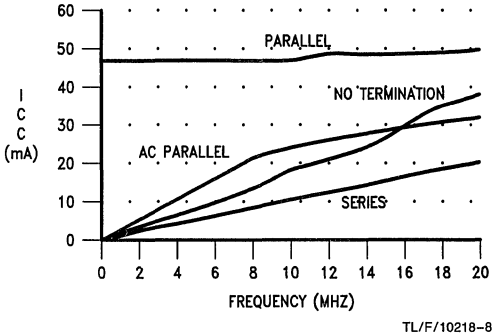

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FIGURE 8. Power Consumption

Power consumption is not the only concern when choosing a termination circuit. Part-count and board space are also important concerns. It is up to system designers to choose which, if any, termination circuit is best suited to their circuit. Table I shows the recommended values for the various termination schemes. It is highly recommended that the designer use these values as a starting point and adapt it for the most feasible and optimum results.

TABLE I. Recommended Termination Values

• Parallel:	Resistor = Z_O
• Thevenin:	Resistor = $2 \times Z_O$
• Series:	Resistor = $Z_O - Z_{OUT}$
• AC:	Resistor = Z_O
	Capacitor = $C \geq \frac{3td}{Z_O}$
• Active:	Resistor = $2 \times Z_O$

For additional information on terminations, refer to these National Semiconductor publications.

1. FAST Applications Handbook, 1987.

2. F100K ECL User's Handbook, 1986.

Understanding and Minimizing Ground Bounce

National Semiconductor
Application Note 640

As system designers begin to use high performance logic families to increase system performance, they may run into new problems which previously did not raise concern when lower performance devices were utilized. These problems can generally be avoided by following a few simple rules. This application note discusses the subject of ground bounce with respect to high performance CMOS logic families and offers a set of simple guidelines that will eliminate system problems due to this phenomenon.

Ground bounce has been a concern to some system designers for many years. Its effects can be found in most bipolar and CMOS logic families. However, ground bounce has recently become a major issue. Although new advanced CMOS logic families have edge rates comparable to advanced bipolar logic devices, CMOS outputs swing almost from rail to rail while bipolar outputs swing from ground to approximately 3.0V. These edge rates, coupled with the greater voltage swings found in today's advanced CMOS logic devices, tend to generate more ground bounce noise than their bipolar counterparts.

In 1982, National Semiconductor, formerly Fairchild Semiconductor, began to develop FACT™ (Fairchild Advanced CMOS Technology) logic incorporating more than three years of experience gained with FAST® (Fairchild Advanced Schottky TTL) logic into the groundwork. As a result, Fairchild was able to understand the important trade-offs associated with high performance in a logic family. In the bipolar world, these trade-offs were between speed and power; in the CMOS world, the trade-offs are between speed and ease of use. Utilizing experience gained from FAST products, the FACT family objectives were defined to provide the optimum solution, allowing greater system performance while minimizing system design problems. Using FACT devices does require more attention toward circuit design and board layout than older, slower technologies. The resulting advantages—low power and high performance—greatly outweigh these considerations.

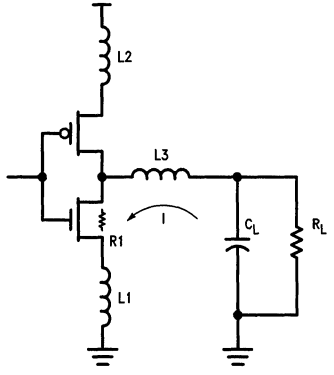
DEFINING GROUND BOUNCE

As edge rates and drive capability increase in advanced logic families, the effects of intrinsic electrical characteristics become more pronounced. One of these intrinsic electrical characteristics is the inductance found in all leadframe materials.

Figure 1a shows a simple circuit model for a CMOS device in a leadframe driving a standard test load. The inductor L1 represents the intrinsic inductance in the ground lead of the package; inductor L2 represents the intrinsic inductance in the power lead of the package; inductor L3 represents the intrinsic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

The three waveforms shown in *Figures 1b, c,* and *d* depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, and the inductors L1 and L3, and C_L, the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = -C_L \bullet dV/dt$)]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{GB} = L \bullet (dI/dt)$].

While these diagrams and figures are useful in explaining the origins of ground bounce, they are highly theoretical and idealistic. There are many second and third order effects which would need to be considered for a complete theoretical analysis. Considering these effects, though, would lead to highly complex second and third order differential equations which are difficult to solve. The purpose of this application note is to develop a fundamental understanding of ground bounce and to provide a useful set of design guide-



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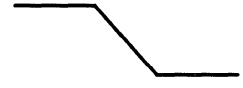
a. Output Model



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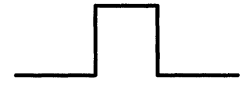
b. Output Voltage (V)



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c. $I = -C_L \bullet (dV/dt)$

TL/F/10232–4

d. $V_{GB} = L \bullet (dI/dt)$

FIGURE 1. Ground Bounce Circuit Model

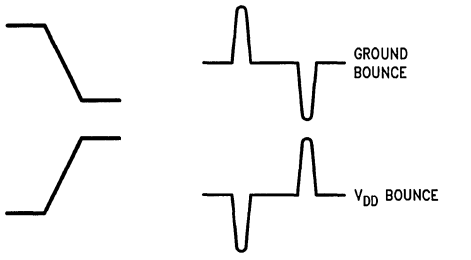
lines. Therefore, we will avoid these lengthy and complex theoretical discussions wherever possible.

In order to change the output from a HIGH to a LOW, current must flow to discharge the load capacitance. This current, as it changes, causes a voltage to be generated across the inductances in the circuit. The formula for the voltage across an inductor is $V = L \bullet (dI/dt)$. This induced voltage creates what is known as ground bounce. Because the inductor is between the external system ground and the internal device ground, the induced voltage causes the internal ground to be at a different potential than the external ground. This shift in potential causes the device inputs and outputs to behave differently than expected because they are referenced to the internal device ground, while the devices which are either driving into the inputs or being driven by the outputs are referenced to the external system ground. External to the device, ground bounce causes input thresholds to shift and output levels to change. This situation is very similar to that of large systems where voltages can develop across expansive ground networks.

OTHER CAUSES OF GROUND BOUNCE

Although this discussion is limited to ground bounce generated during HIGH-to-LOW transitions, it should be noted that the ground bounce is also generated during LOW-to-HIGH transitions. This ground bounce is created by the large gate capacitances associated with the output transistors on the die. Because these gate capacitances are larger than the gate capacitances of earlier-stage transistors, more current is generated when they switch. The output buffer stages of CMOS devices are inverters; thus their inputs are switching HIGH-to-LOW when their outputs are switching LOW-to-HIGH. It is the currents associated with switching these inputs to the output transistors that generate ground bounce when the outputs switch LOW-to-HIGH. This LOW-to-HIGH ground bounce has a much smaller amplitude and therefore does not present the same concern.

We should also note that everything discussed here concerning ground bounce can be applied to the opposite effect, V_{DD} bounce. V_{DD} bounce is the inverse of ground bounce. As one would expect, there is an intrinsic inductance in the V_{DD} lead as well as the ground lead. The internal V_{DD} potential will collapse toward ground at the beginning of a LOW-to-HIGH transition and then bounce above the external V_{DD} potential at the end of the transition.



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- V_{DD} bounce (droop) is the voltage drop across the package
- Inductance (to V_{DD}) is caused by charging load capacitances
- V_{DD} bounce is less of a concern than ground bounce because TTL-level inputs have greater high noise immunity

FIGURE 2. Ground Bounce/V_{DD} Bounce

In addition, V_{DD} bounce is generated during HIGH-to-LOW transitions for the same reasons that ground bounce is generated during LOW-to-HIGH transitions.

We will not discuss V_{DD} bounce in this application note because its effects parallel those of ground bounce, and the system problems of V_{DD} bounce are typically of less concern than ground bounce. This is because TTL inputs have a greater input high noise margin that input low noise margin. For CMOS driving TTL, the input high noise margin approaches 3.5V, and for CMOS driving CMOS, the input high noise margin approaches 2.5V. In either case, the input high noise margin is 3 to 5 times greater than any expected V_{DD} bounce.

CONTRIBUTING FACTORS OF GROUND BOUNCE

While our circuit diagrams shown above are useful for explaining the origins of ground bounce, they are too idealistic to be used for modeling. In the real world, there are many other variables which affect the actual shape and amplitude of the induced voltage. To develop an accurate model, the resistor must be replaced with a model of the actual transistor. In addition, the period where the transistors are turning on and off would need to be taken into account. Including these variables, plus others, would lead to highly complex differential equations that are nearly impossible to solve except by the most advanced computer programs. Since theoretical analysis of ground bounce is difficult to perform, we will use empirical data to develop an understanding of ground bounce and how it is effected.

There are several factors which affect ground bounce: the number of outputs switching simultaneously; the location of the output pin; the location and type of load on the line; the V_{DD} voltage; the device technology; and the output and ground inductances. Each of these factors play a critical role in the generation of ground bounce.

GROUND BOUNCE DEMONSTRATION BOARD

In order to evaluate ground bounce and the factors which affect it, Fairchild designed a board which allowed side-by-side evaluation of ground bounce under varying conditions.

Figure 3 shows the functional block diagram of the board. A counter generates the changing data lines by counting from 0 to 127. The counter can also be configured to count down from 127 to 0 so that V_{DD} bounce may be evaluated. This changing data is clocked into an 'AC374 and then passed into both another 'AC374 and an 'AC244. This was done for two reasons.

First, the noise generated by the first 'AC374 represents gound bounce generated by a lightly-loaded circuit. Secondly, being able to choose between either the 'AC374 or the 'AC244 to drive the system bus allows us to evaluate both devices under heavy load conditions. The quiet output from these two devices drives a line that is connected to the clock inputs of eight '74 D-type flip-flops and two inverter inputs. Each flip-flop is configured so that if a valid clock was encountered, the Q output will go from a "0" to a "1"; each flip-flop acts as qlitch catcher, detecting any ground bounce noise which violates the flip-flop clock thresholds. Devices from several common logic families are connected to this quiet output so that the effect on different technologies can be evaluated.

The seven other outputs of the 'AC374 or the 'AC244 drive a 7-bit data bus. This data bus is loaded with fourteen devices, which represents a typical heavily-loaded system bus and allows us to evaluate ground bounce under these conditions.

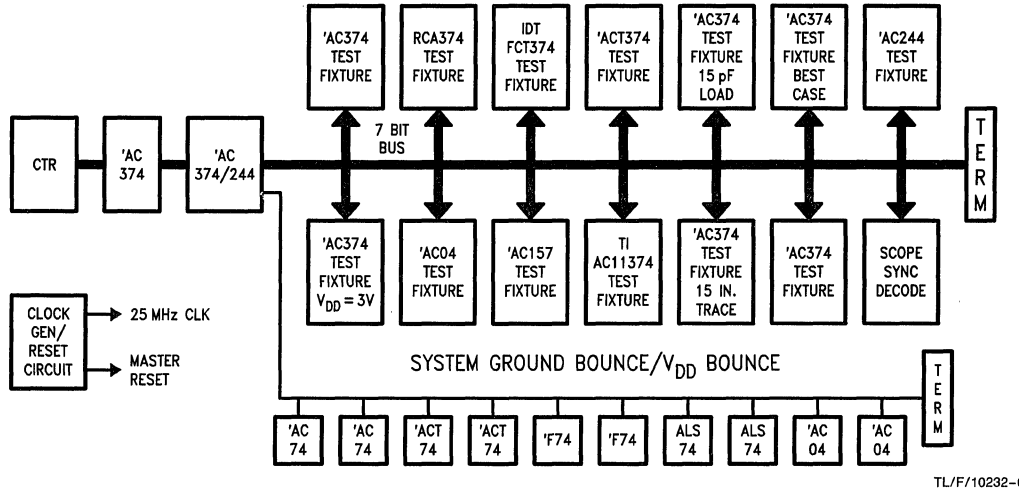

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FIGURE 3. Ground Bounce Demonstration Board Block Diagram

TABLE I. Critical Signal Statistics

Signal	Length	CO	LO	RO	# Loads	C_L	Termination Type	Termination Type
DATA BUS	30 Inch	107 pF	565 nH	1.3Ω	14	70 pF	PARALLEL	50Ω
CLOCK*	28 Inch	103 pF	445 nH	1.0Ω	16	80 pF	THEVENIN	71Ω/120Ω
GROUND BOUNCE	7.5 Inch	30 pF	117 nH	0.2Ω	10	50 pF	AC	26Ω/200Ω

• Clock generated from seven (7) stage ring oscillator ('AC240)—approximately 25 MHz

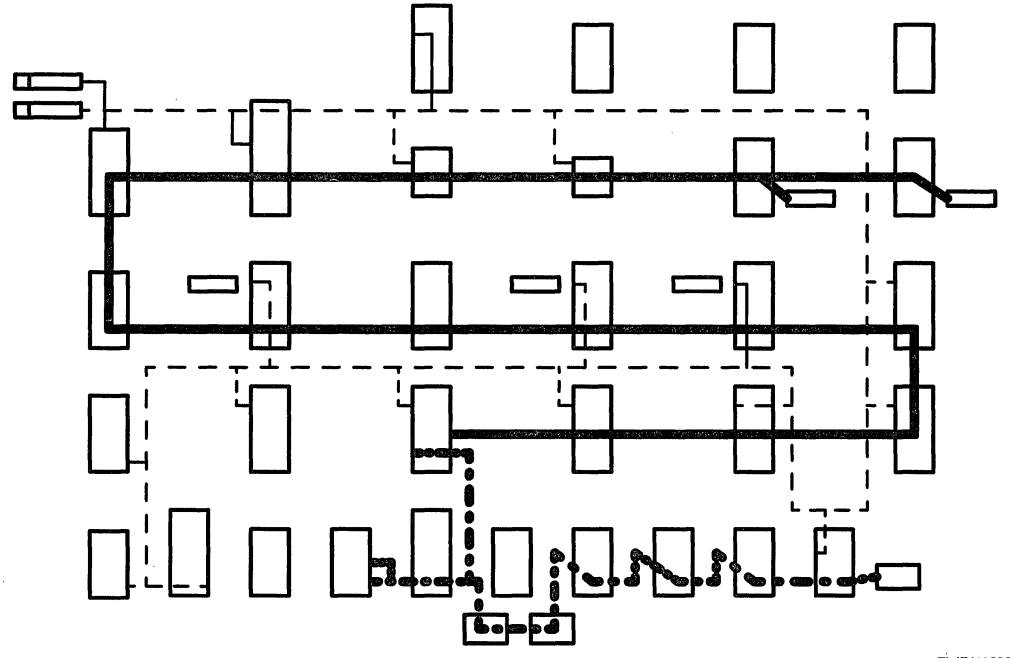

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FIGURE 4. Critical Signal Paths

Each device on the bus is configured equivalent to a standard test fixture. Conditions such as output loading, load placement, power supply voltage, and quiet output pin location were varied to compare ground bounce under different conditions. Also, some device locations were populated with different device types and devices from other logic families to evaluate ground bounce across technologies.

Table I lists the important electrical characteristics for the critical signal paths. *Figure 4* shows the physical layout of the board and the critical paths. This board was used to generate the data and waveforms presented in this application note unless otherwise noted.

LEAD INDUCTANCE

The impact of the ground inductance on ground bounce seems to be obvious. For a given dI/dt value, the greater the inductance, the greater the ground bounce. While this would imply that reducing the ground inductance should reduce the ground bounce, this is not always the case. The explanation is fairly straightforward.

Ground bounce tends to limit the available AC current in CMOS outputs by reducing the voltage across the output impedance, and therefore, reduces the current that will flow. When the ground lead inductance is reduced, a corresponding increase in the output edge rate of the device occurs. This is due to the fact that by reducing the inductance in the ground lead we have increased the available AC current. This greater dI/dt tends to reduce any improvement that the reduced ground inductance may have generated.

National tested FACT to investigate the effect of ground inductance on ground bounce. This was accomplished by assembling die from the same manufacturing lot in plastic DIPs; some were assembled using the standard pinout and some were assembled with the ground and power pads connected to the center pins. When the data was analyzed, it was found that the die assembled with center pin V_{DD} and ground averaged approximately 10%–15% less ground bounce than the die assembled with the standard pinouts. Along with the small reduction in ground bounce, they also exhibited somewhat faster edge rates with corresponding decreases in propagation delays.

OTHER PACKAGES

The inductance in the ground lead is not the only inductance in the package; all of the output pins have an associated inductance. The inductances in the outputs also contribute to ground bounce, especially any oscillatory effects. While just reducing the ground or V_{DD} does not significantly reduce ground bounce, reducing the inductance in both the power leads and the outputs does reduce ground bounce.

Figure 5 outlines the effect that packaging has on ground bounce. In order to make the comparison as valid as possible, die from the same wafer were used. This was necessary because the effect of process variations on ground bounce is greater than the effect of packaging. It can be seen that packages with smaller power and signal lead inductances tend to reduce ground bounce. It is important to note that the difference between CDIP and LCC package ground lead inductance is approximately one order of magnitude (20 nH versus 2 nH), yet the difference in ground bounce is less than 35%.

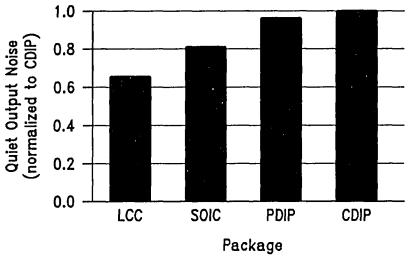

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FIGURE 5. Noise vs Package Configuration

Reducing the ground lead inductance is not "the" solution to ground bounce problems. While a small reduction in ground bounce can be realized, additional problems, like increased crosstalk, may occur. A better solution is to reduce the inductance in all leads. Smaller packages, such as SOIC and LCC/PLCC packages, do reduce ground bounce over both standard and center-V_{DD}/ground-pinned DIP packages.

NUMBER OF OUTPUTS SWITCHING

The number of outputs switching simultaneously affects the amplitude of ground bounce. For a simple model, treat the output impedances of each active output as resistors and inductors in parallel. For resistors of equal value in parallel, the formula for the net resistance is R/n, where R is the output impedance of each transistor, and n is the number of resistors. Therefore, as more outputs switch at the same time, the output resistance is reduced and more ground bounce will be generated.

Again, it is very difficult to model this effect so we will rely on empirical results for our analysis. *Figure 6* illustrates the effect of increasing the number of outputs switching at the same time. We can see that as the number goes up, the amplitude and duration of the ground bounce pulse also increases. Therefore, devices that have fewer outputs will have less ground bounce.

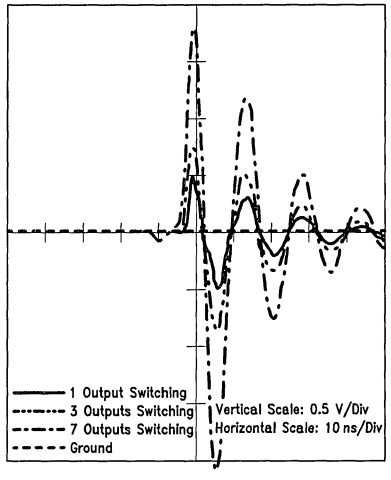

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FIGURE 6. Number of Outputs Switching

Figure 7 shows the ground bounce generated by an 'AC157 when three of the four outputs are switching with standard test loads. Here we see only 475 mV of noise on the worst-case pin (pin furthest from the ground pin). This amplitude of ground bounce is not what we would expect in an actual system. As we will discuss later, a test fixture lumped load creates much more ground bounce than distributed system loads.

OUTPUT LOAD

The type and value of the output loading is one of the major variables that affect the amplitude of the ground bounce. *Figures 8, 9* and *10* show the effects of varying the load capacitance in a standard test fixture.

In *Figure 8*, the ground bounce amplitude peaks for a load capacitance of approximately 60–70 pF, and then drops off as the capacitance is increased. This drop off is caused by the filtering effect of the larger capacitors.

For *Figure 9*, only the load capacitors on the active outputs were varied. The load on the quiet output was maintained at 50 pF. The amplitude of the ground bounce amplitude increased with increased capacitive loading. However, the slope of the curve drops off as the capacitance increases. This is due to the amount of energy that is discharged from the capacitor during the time that the output transistor is turning on.

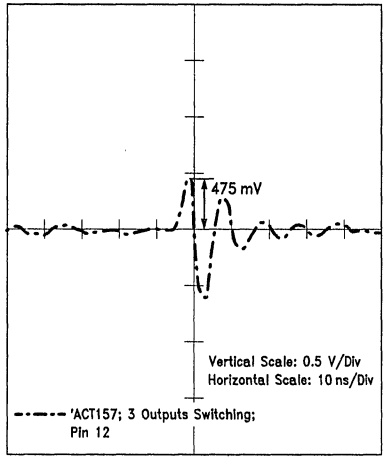

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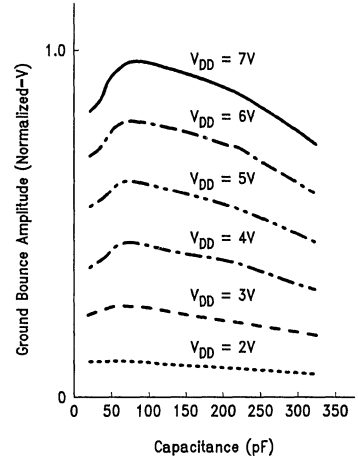
FIGURE 7. 'AC157 Quiet Output Noise

Smaller capacitors contain less energy than larger capacitors, and therefore, a larger change in the voltage across them will occur during the time that the output is turning on. Because of this, the size of the capacitance tends to limit the maximum amount of current sinking throughout the output and therefore, the amount of ground bounce. Larger capacitors, however, do not experience such a large change in voltage as the outputs turn on. For very large capacitances, there is almost no change in the voltage across them, and they behave much like a power supply. Under these conditions, the maximum amount of current that will sink through the outputs is limited by the outputs themselves. Increasing the capacitance does not increase the current and therefore, does not increase the ground bounce.

Figure 10 shows the effect of varying only the capacitive loading on the active output. Here, the filtering effect of the load can be observed clearly. As the load capacitance is increased, it filters the signal and reduces the amplitude of the ground bounce.

Because they generate more AC current during switching, capacitive loads tend to generate more ground bounce noise than resistive loads. Fortunately, most actual PCB traces will be long enough so that they react like an impedance and not lumped capacitive loads.



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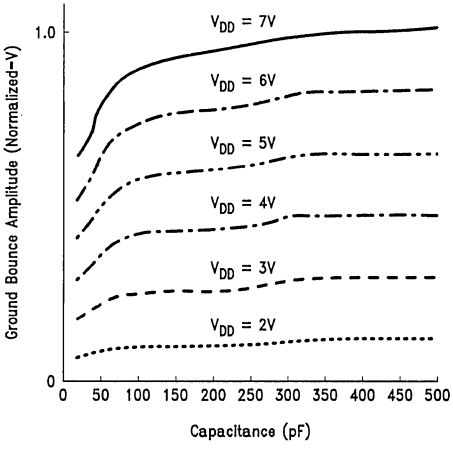
Quiet Output Switching Using 'AC241
7 Outputs Driving Lumped Capacitive Loads
Monitoring Pin 18.

FIGURE 8. Quiet Output Noise vs Capacitive Loading



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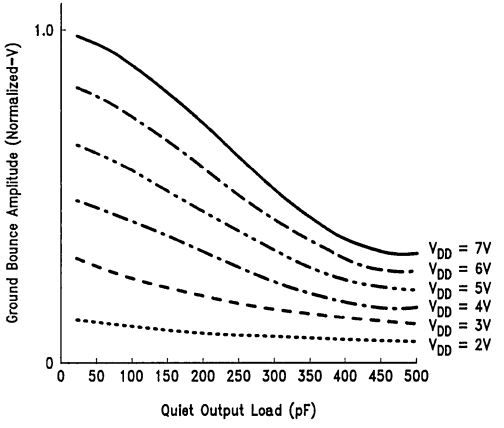
Quiet Output Switching with 'AC241
7 Outputs Driving Lumped Capacitive Loads
Monitoring Pin 18

FIGURE 9. Fixed Quiet Load

Figure 11 displays ground bounce when the device is loaded with standard 50 pF/500Ω test loads. Each load was connected directly to the output pin. Under these conditions, which are considered worst case, the measured ground bounce amplitude was 1.7V.



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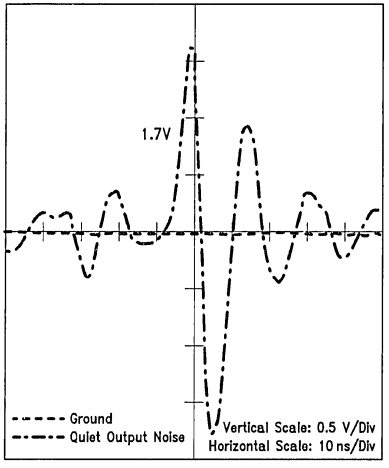
Ground Bounce Varying Quiet Output Load Only
Other 7 Loads are Standard 500Ω/50 pF

FIGURE 10. Fixed Active Load

Figure 12 illustrates what happens when the test load is moved away from the device output. A standard test load was connected to the output via 15 inches of circuit trace. The amplitude of the ground bounce was reduced to 1.1V. While this loading is closer to an actual system trace than a test load, it still generates more ground bounce noise because of the lumped load that is still on the line.



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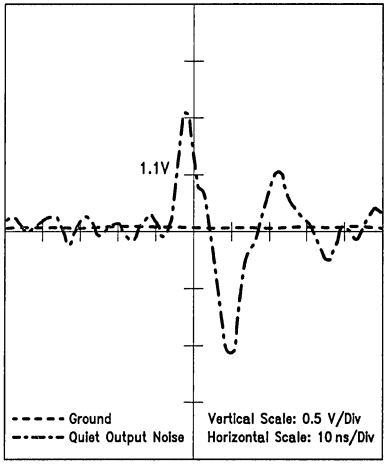
7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin

FIGURE 11. Standard Test Fixture



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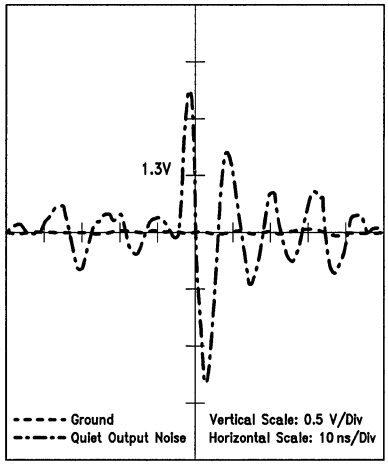
7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin
15″ PCB Trace Separating Load from Device

FIGURE 12. Test Fixture Emulating Transmission Line Effect

Figure 13 shows the ground bounce when the load capacitance is reduced to 5 pF. The ground bounce decreased to 1.3V. This circuit represents a short, lightly loaded line.

Figures 14 and *15* depict the ground bounce generated by the 'AC374 and 'AC244 driving the data bus on the board. This bus is over 30 inches long and has over 200 pF of capacitance load. The 'AC374 only generated 600 mV of ground bounce while the 'AC244 generated 500 mV. This circuit represents a typical system trace. These figures show the expected amplitudes of ground bounce in an actual system.

Figure 16 shows the ground bounce which was measured on a commercially available personal computer motherboard after a 'F244 was removed and replaced with an 'ACT244. For these results, the host processor was removed, and the inputs to the 'ACT244 were connected to



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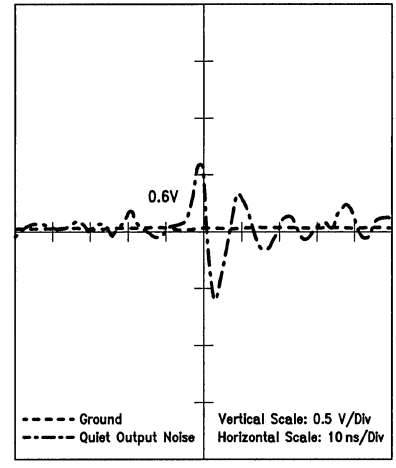
7 Outputs Switching V_{DD} = 5V
C_L = 5 pF
Worst-Case Output Pin
Open Circuit Output (5 pF Parasitic Capacitance)

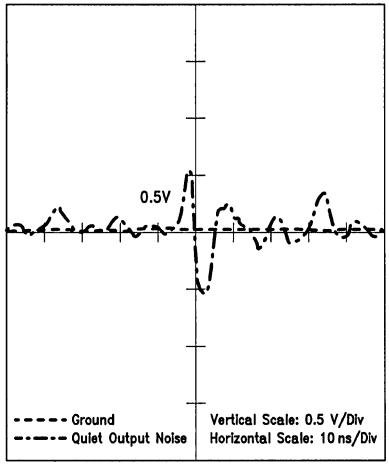
FIGURE 13. Reduced Output Loading



TL/F/10232–17

7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin;
Ten Loads on Quiet Output Heavy Load

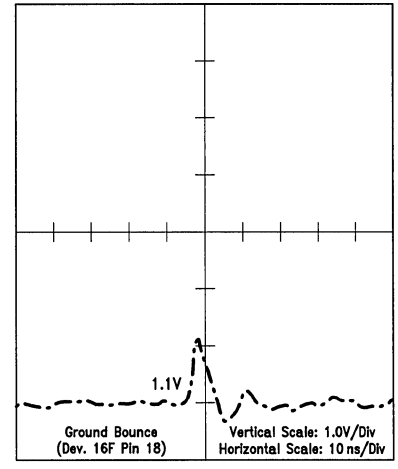
FIGURE 14. System Quiet Output Noise—'AC374



TL/F/10232–18

7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin;
Ten Loads on Quiet Output Heavy Load

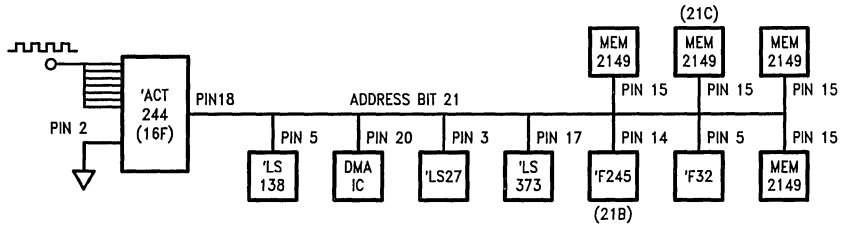
FIGURE 15. System Quiet Output Noise—'AC244



TL/F/10232–19

7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin
'AC244 Driving 10 Distributed Loads on an Unterminated Address Bus

FIGURE 16. Quiet Output Noise in Personal Computer Application



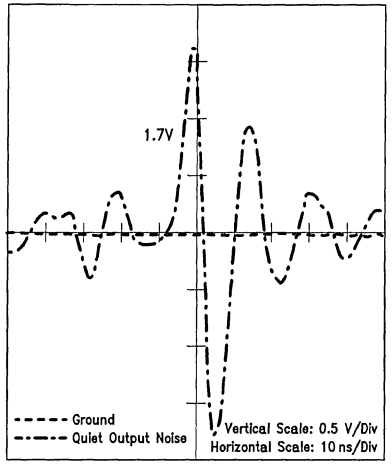
TL/F/10232–20

- Commercial PC Address Bus
- No Termination Resistors
- Approximately 50 pF Capacitance Loading
- Replaced 'F244 with 'ACT244
- With 7 Outputs Switching, Quiet Output Noise = 1.1V

FIGURE 17. PC Circuit Diagram

the board clock source. The logic diagram for this line is represented in *Figure 17*. An address bus driver was chosen because of the length of the line and the number of loads on it. Here, the ground bounce amplitude was 1.1V. We can see that this signal line is connected to devices of many different technologies and functions, including LS and memory products. After the host processor was replaced, the system exhibited no performance degradation due to the device replacement.

It can be seen from the previous figures that the type and location of the output loads have a major effect on ground bounce. It is also obvious that standard test loads generate the most ground bounce. Even reducing the capacitive load, or moving it away from the output still generates more noise than a typical application.



TL/F/10232–21

7 Output Switching V_{DD} = 5V

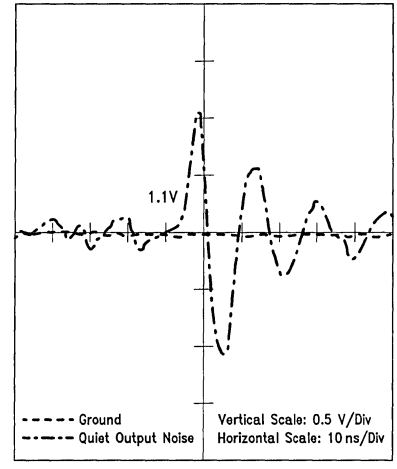
C_L = 50 pF

Standard Test Setup

FIGURE 18. Quiet Output Noise— Worst-Case Output Pin

OUTPUT PIN LOCATION

The location of the output pin with respect to the device ground also affects the magnitude of ground bounce. Tests have shown that outputs located closer to the ground lead generally have 30% to 50% less noise than pins further away. The effects of pin location are portrayed in *Figures 18* and *19. Figure 18* shows the ground bounce on the worst-case pin, which is the one farthest away from ground. *Figure 19* shows the ground bounce on the best-case pin, the one closest to ground. By choosing outputs close to ground, the amount of ground bounce may be reduced by nearly half.



TL/F/10232–22

7 Outputs Switching V_{DD} = 5V

C_L = 50 pF

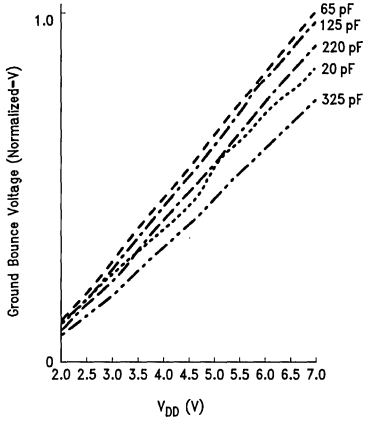
FIGURE 19. Quiet Output Noise— Best-Case Output Pin (Pin 9)

POWER SUPPLY VOLTAGE EFFECTS

The value of V_{DD} also affects the amplitude of the ground bounce. By reducing the V_{DD} level, not only is the output voltage swing reduced, but also the amount of current that the output can deliver. Both of these tend to reduce ground bounce.

Figure 20 tabulates the results of varying both V_{DD} and load capacitance. All of these numbers were taken on a standard test fixture. Note that while the amplitude of the ground bounce changes linearly with voltage, it is not merely the ratio of the voltage levels. Reducing the V_{DD} by 40% (from 5.0V to 3.0V) reduces the ground bounce by almost 60%. Since the amplitude of the ground bounce decreases faster than the input threshold, there is a net gain in the noise margin.

Figure 21 represents the same results taken on the ground bounce demo board. The ground bounce was measured with V_{DD} = 3.0V. The amount of ground bounce was reduced to 800 mV, even with standard test loads. It should be pointed out that 'ACXXX devices can be used in a 5V TTL system with a V_{DD} of 3.3V ±0.3V. Under these conditions, the outputs will still drive an incident wave on a 75Ω transmission line for the commercial temperature range and 100Ω for the military temperature range. With V_{DD} equal to 3.3V, FACT 'ACXXX devices have TTL-compatible inputs and outputs.



TL/F/10232–23

FIGURE 20. Quiet Output Noise vs Power Supply

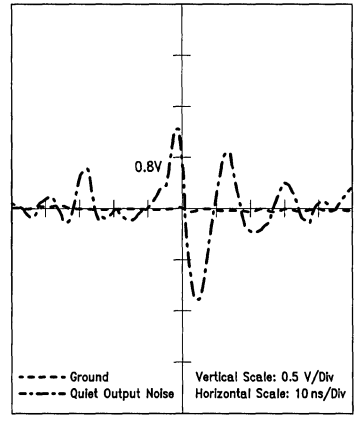
TEST FIXTURES VS REAL SYSTEMS

Because ground bounce is so dependent upon the load the device is driving, it has proven to be one characteristic of CMOS devices that does not correlate well between results taken on standard test fixtures and results seen in actual systems. This occurs for several reasons. First, the AC loading presented by standard text fixtures is not the same as the AC loading generated by a system load, and second, the standard test load creates a LCR tank circuit that tends to oscillate during edge transitions.

For these reasons, ground bounce data taken on test fixtures is useful for comparative analysis, but is not valid for predicting actual system performance.

AC LOADING EFFECTS

Standard text fixtures use 50 pF of capacitance and 500Ω of resistance to simulate a "typical load," as shown in *Figure 22*. It is possible to achieve good correlation between propagation delay data taken using these test loads and data taken in real systems. Unfortunately, this is not true for ground bounce. While this lumped load testing was adequate for older, slower technologies, it is not as useful for the newer, faster logic families. As edge rates go up, more and more circuit traces react like transmission lines, not lumped loads. For devices having edge rates of approximately 3 ns, traces longer than 6–8 inches will exhibit transmission line characteristics and cannot be treated as lumped loads.



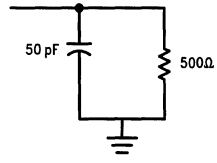
TL/F/10232–24

7 Outputs Switching V_{DD} = 5V

C_L = 50 pF

Worst-Case Output Pin

FIGURE 21. Quiet Output Noise—V_{DD} = 3.0V

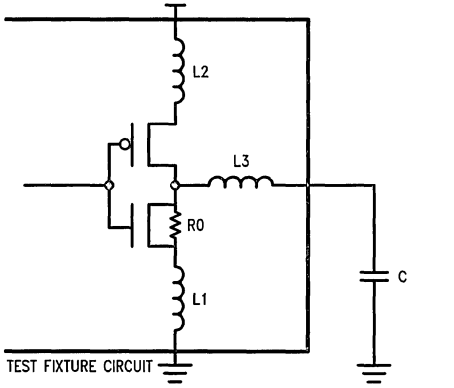


TL/F/10232–25

FIGURE 22. Standard Test Load

Figures 23a and *23b* are models of a capacitive load and a transmission line load, respectively. In *Figure 23a,* we replace the capacitor with a power supply. This simulates our circuit at the time when the output transistor has just turned on, and the full capacitor voltage is applied across the device. In *Figure 23b*, the transmission line is replaced with a resistor to the power supply. This simulates the AC characteristics of the transmission line.

Comparing the two figures, we notice that while the capacitive load applies the full voltage directly to the device output, the transmission line acts like an additional resistance between the voltage and the device output. Clearly, one would expect more current to flow with the capacitive load than with the resistive load. Since the output transistor turns on just as fast in both cases, the capacitive load will create a greater dI/dt, causing more voltage to be induced across the ground lead inductance. Because of this, standard test fixtures tend to generate two to three times more ground bounce noise than system printed circuit traces. This is still true for traces that may have more capacitance than the 50 pF lumped load used in standard test fixtures.



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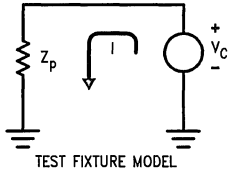

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FIGURE 23a. Test Fixture

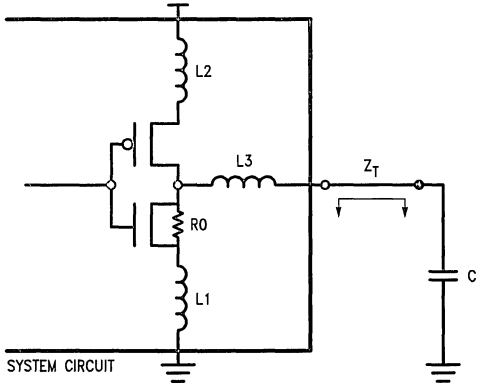
LCR TANK EFFECTS

Referring back to *Figure 1a*, notice the LCR tank circuit that is formed by the load capacitance, parasitic inductances and output resistance. Imagine each edge transition as a single impulse into this tank circuit; it would be expected to oscillate. Theoretically, the frequency of the oscillation should be somewhere in the range around 1.3 GHz. Typically, oscillations are observed in the frequency range of 100 MHz to 200 MHz. There are several reasons for this discrepancy.

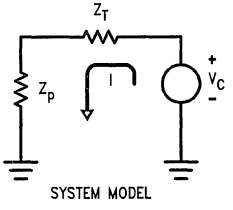
The output transistor does not behave like a pure resistance. The transistor tends to limit the available current to less than 160 mA to 180 mA. Additionally, there are other parasitic elements associated with the output transistor affecting the frequency of oscillation.

Because most circuit traces react like impedances and not capacitances, this type of oscillation is not seen when FACT devices drive typical circuit traces.

Figures 22 and *23* highlight the differences between ground bounce in a standard test fixture and in a comparable PCB trace. The results of the test fixture *(Figure 24)* are much greater than the results of the PCB circuit trace *(Figure 25)*. This is due to the greater current requirements caused by the lumped capacitive load versus a distributed load.

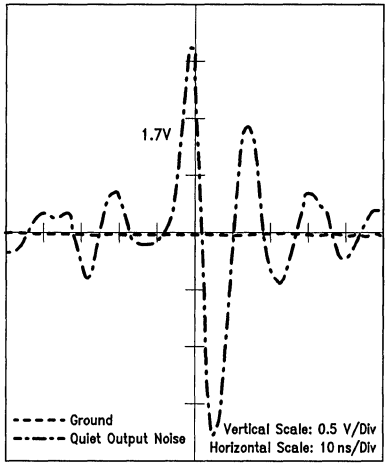


TL/F/10232–28



TL/F/10232–29

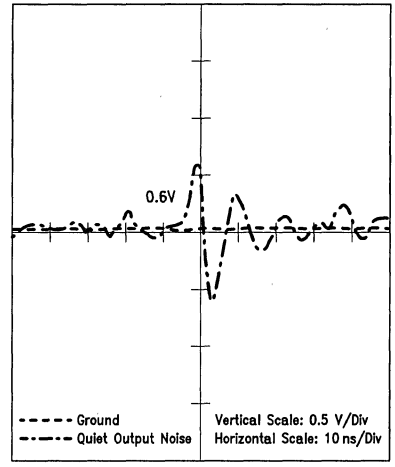
FIGURE 23b. System Models



TL/F/10232–30

7 Outputs Switching V_{DD} = 5V C_L = 50 pF
Worst Case Output Pin; Ten Loads on Quiet Output

FIGURE 24. Quiet Output—Standard Test Fixture



TL/F/10232–31

7 Outputs Switching V_{DD} = 5V; Heavy Load
Worst-Case Output Pin; Ten Loads on Quiet Output

FIGURE 25. Quiet Output Noise—System Bus

The difference in oscillation between a standard test fixture and a typical circuit trace is also shown. Even though the circuit trace has more capacitance than the test fixture, it is not lumped at the output, but distributed along the circuit trace.

For these reasons, ground bounce data taken on test fixtures is useful for comparative analysis, but is not valid for predicting actual system performance.

MANIFESTATIONS OF GROUND BOUNCE

The problems associated with ground bounce occur because the induced voltage across the ground leads creates a voltage differential between the external system ground and the internal device ground. This voltage affects both inputs and outputs, although differently.

The difference between the external and internal grounds must be taken into account to arrive at the actual input threshold. Noise on either the internal ground or V_{DD} will cause the input thresholds to change. CMOS input thresholds are generally 50% of the voltage across the input structure, i.e., if V_{DD} is 5.0V, then the input threshold will be 2.5V. Now, if the ground bounces positively 1.0V, the net voltage across the input structure will be reduced to 4.0V. This will cause the input threshold to shift up to 3.0V (1.0V of ground rise + 50% × 4.0V). Conversely, if the ground bounces negatively 1.0V, the input threshold will drop down to 2.0V (−1.0V + 50% × 6.0V). If during this time a quiet input is held between 2.0V and 3.0V, the input structure will detect a change of state.

Regarding the outputs, the effect is somewhat different. Any output that is LOW is essentially tied to the internal ground through a very low impedance: approximately 10–12Ω. Therefore, any output will tend to follow the internal ground as it shifts with respect to the external ground. This causes any LOW outputs to also shift with respect to external ground.

There are four predominant manifestations of ground bounce which we will discuss: 1) altered device states, where a device assumes a state that is not intended or expected, 2) undershoot noise on active signals, 3) propagation delay degradation, and 4) noise on quiet (static) outputs.

ALTERED DEVICE STATES

Of these four symptoms, the most critical is altered device states. Altered device states occur when a device assumes a state that is not intended or expected by the system designer. The results can range from glitches on the outputs to permanently-altered data in registers or counters. Ground bounce can cause these types of problems when it is great enough to cause an external signal to be sensed incorrectly in the device.

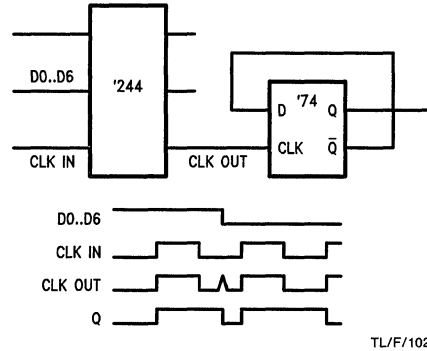


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FIGURE 26. Example of Ground Bounce

In CMOS devices, the input thresholds are generally a percentage of the voltage across the input structure. Generally, the input levels are 50% for CMOS level inputs and 30% for TTL-level inputs. As the internal ground and power levels shift with respect to the external power and ground planes, the input thresholds will also shift. If the shift is great enough to cause the input threshold to go above an external HIGH signal (so that the input signal looks LOW) or below an external LOW signal (so that the input looks HIGH), the input will detect a change of state. Depending upon the input type, several results can occur.

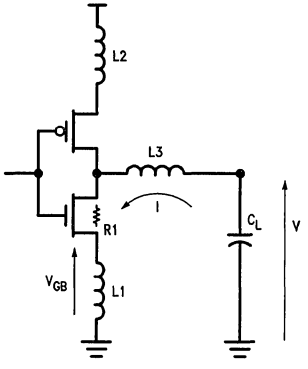
If the input is a synchronous one, such as the data input into a D-type flip-flop, then the device should not be affected. If the input is combinatorial, or the data input to a transparent latch, the output may glitch.

The effects may be more damaging if the input is asynchronous, such as a clock, preset, set, load, or clear. With these inputs, data in the internal counters or registers may be corrupted. Most likely, this type of data corruption can usually cause a system to fail, or generate invalid results.

FACT devices are characterized during initial device evaluation to ensure that the device will not exhibit this problem.

PROPAGATION DELAY DEGRADATION

Propagation delay degradation is a phenomenon familiar to most system designers. As more than one output on a single device is switched, the propagation delay, as measured to the input threshold level, will become longer. To understand how this happens with CMOS devices, consider *Figure 27*; any voltage developed across the inductor L1 will reduce the voltage across the output impedance R1. This, in turn reduces the current through R1. Since the rate of voltage change across the load capacitance is directly related to the current available, a decrease in current reduces the rate at which the output voltage changes, i.e., the edge rate slows down. This, in turn, slows down the propagation delay because more time is required for the output to go from one rail to the input threshold. As additional outputs are switching simultaneously, the voltage across the inductor increases, and the current available to charge or discharge the load capacitance will be less.



TL/F/10232–32

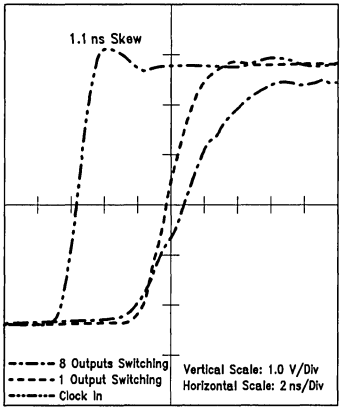
FIGURE 27. Output Model

Figure 28 illustrates the effects of multiple output switching on the propagation delay of a FACT device. Here we see that as more outputs switch, the edge rate of those outputs drops off.

While it is not possible to test this type of parameter in an ATE environment, National understands its importance to system designers. Since this type of measurement can be made in a bench environment, FACT devices are evaluated during initial device characterization to insure that this propagation delay degradation is less than 250 ps per additional output switched.

UNDERSHOOT ON ACTIVE SIGNALS

Undershoot noise on active signals is generally created by impedance mismatches in transmission lines. Yet, it can also be created by ground bounce. *Figure 29* shows the voltage that is generated across the inductor during the edge transition. While at the beginning of the transition the ground bounce is positive, at the end it is negative. This is due to the currents turning off as the output reaches the end of its voltage swing.



TL/F/10232–33

FIGURE 28. Propagation Delay vs Number of Outputs Switching

Unfortunately, the negative ground bounce occurs when the output is finishing its transition. The output will follow the internal ground as a quiet output would. This results in the output undershooting and then returning to ground.

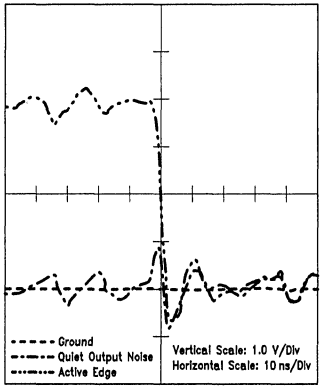


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FIGURE 29. Quiet Output Noise Concurrent with Active Edge

Undershoot amplitudes are generally slightly less than the associated ground bounce. This undershoot noise will generally not be a problem because most standard logic families have input structures, such as clamp diodes, that tend to damp it out. However, some specialized devices, exemplified by dynamic RAMs, may be sensitive to undershoots greater than −2.0V.

QUIET OUTPUT NOISE

Quiet, or static, output noise is usually the symptom of ground bounce that is first noticed by system designers. As pointed out earlier, quiet output noise occurs because LOW outputs tend to follow internal ground. If there is a shift between the external and internal grounds, it will appear as noise on a quiet output. The effects of this noise can range from noise on the output signals to system failure. If the noise is great enough to cross the input threshold on the next device on the line, this next device may react.

The reaction, of course, will depend upon the type of input. If the input is synchronous, the ground bounce noise will not propagate through the input into the device. If the input is combinatorial or asynchronous, output glitches or corrupted counters or registers may result. In order to predict the effects of this noise, it is necessary to consider some typical applications.

As shown earlier, ground bounce amplitude is dependent upon the number of outputs switching. Therefore, devices which have fewer outputs will have less noise. Because of this, our discussions will be limited to octal devices and their applications.

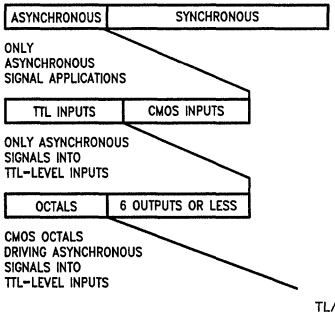

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FIGURE 30. Application Segments

SYNCHRONOUS DATA/ADDRESS BUSSES

One of the largest application segments for octal devices is driving/receiving data and address busses. In these bus applications, the receiver is usually synchronous and latches in the data on a clock edge. In *Figure 29*, notice that the quiet output noise exists only when the active outputs are switching. In addition, both quiet and active outputs achieve this stable and valid state within the propagation delay time specified in the FACT Data Book.

During the time that the data or address is latched in (when the data is expected to remain stable and valid) the quiet outputs are as stable and valid as the active outputs. Therefore, valid data will always be clocked in, and in these systems, no additional work is required to achieve maximum system performance and reliability.

ASYNCHRONOUS CONTROL LINES

A much smaller application segment is driving asynchronous signals. Octal devices, like the '240 series, offer eight buffers in a 20-pin package. This feature can be useful to the system designer trying to reduce board size and part count. It is in these applications that problems are most likely to occur. However, there are several factors that work in the designer's favor.

It is important to look at the type of input that is being driven. CMOS-level inputs have much greater low noise margins than TTL-level inputs. Standard CMOS inputs have input thresholds set to 50% of V_{DD}. This means that if V_{DD} equals 5.0V, there is 2.5V of low noise margin. Test results show that the ground bounce will never be this great in a system. In addition, as noted above, the actual ground bounce noise expected in a real system is less than the AC noise margins of most TTL families.

Finally, it is very important to note that the duration of the ground bounce noise spike is short (tyically 2–3 ns @ 0.8V). Typically, AC noise margins increase with decreasing pulse width. This is more pronounced in slower technologies. *Figure 31* shows the typical low level input noise thresholds of FAST, Schottky, and Low Power Schottky. For pulse width typically seen with ground bounce noise, the AC noise margins of FAST and Schottky approach 2.0V and 1.5V respectively. Even LS devices, which have the lowest input thresholds, have AC noise margins that exceed 2.0V for pulse

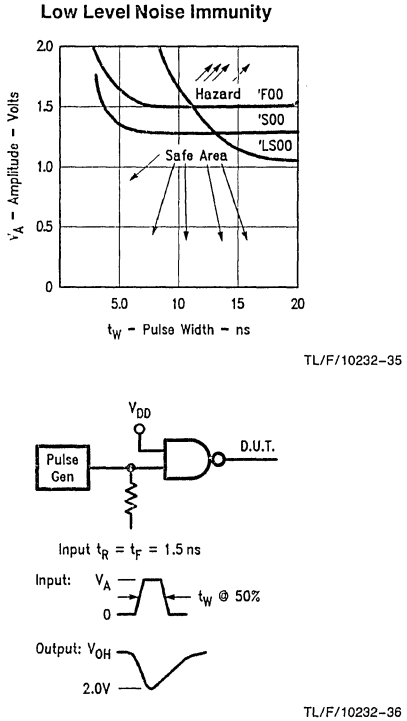

FIGURE 31. AC Noise Thresholds

widths as great as 8 ns. For ground bounce type noise pulses, with widths of 2–3 ns, the LS AC thresholds are well above 2.0V.

There are also several design techniques under the system designer's control which can be used to minimize ground bounce noise, thereby eliminating ground bounce-induced problems.

The first factor that should be considered, in many cases, is that the need for a buffer can be eliminated. This is due to the fact that all FACT logic devices feature the same 24 mA output stages. A quick example will help to clarify this. For the example, a divide-by-2 clock generator drives a clock onto a large processor board. *Figure 32a* shows the circuit built with ALS devices while *Figure 32b* shows the same circuit built with FACT devices. The difference is obvious: the ALS circuit required a buffer to drive the clock line because the 'ALS74 does not have enough output drive to drive the line. On the other hand the 'AC74 has the same drive capability as the 'AC240, so adding the buffer is redundant. In addition, the output of the 'AC74 is double buffered to isolate the internal logic from noise on the outputs. Removing an additional propagation delay gains performance advantages besides board space and part count savings. If it is not possible to remove the buffer, the designer can still insure minimum noise on the output. This can be accomplished with several methods, some of which are discussed here.

Board-level timing analysis may show that not all of the outputs can switch at the same time. Under these conditions, the worst-case ground bounce will be reduced *(Figure 6)*. As

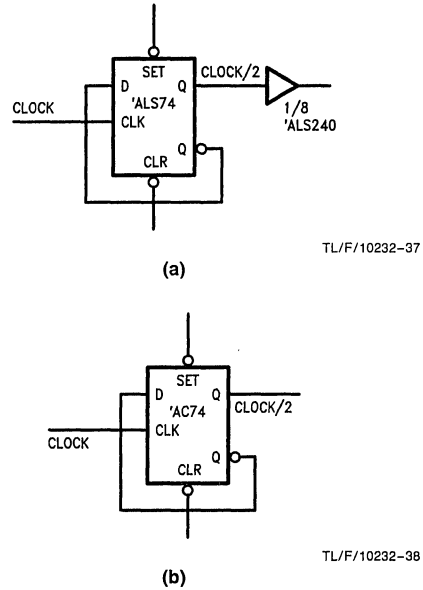

FIGURE 32. Example Circuits

mentioned earlier, outputs closer to the ground pin may have up to 50% less noise than outputs further away. Therefore, asynchronous lines should be driven from outputs closer to the device ground pin whenever possible.

Some other methods, which may be more difficult to implement, include reducing the power supply voltage or using two power supply voltages. Running the system V_{DD} lower (closer to 4.5V) will reduce the ground bounce noise levels of the CMOS devices while not affecting the input thresholds of the TTL devices. In addition, as we stated earlier, the V_{DD} value for the CMOS devices can be lowered to 3.3V. This reduces the ground bounce by 60% while maintaining TTL-compatible inputs and outputs. For a small number of CMOS devices, a standard zener diode regulated circuit may be used. For larger numbers of devices, a second (3.3V) power plane may be added.

Take a moment to summarize the material covered thus far. While at first glance, the problems associated with quiet output noise may seem to be the most precarious to system designers, there are many issues that affect them. First, a large percentage of the octal applications are synchronous busses. In these applications, quiet output noise will not be a problem.

It is the smaller segment of asynchronous applications that are most suspect. Fortunately, only octal devices generate enough ground bounce noise to be of serious concern. Secondly, if the inputs are CMOS, the input noise margins are greater than any ground bounce. If the inputs are TTL, the ground bounce will generally be less than the TTL AC input noise margins. Additionally, designers have several techniques available to reduce the ground bounce. These include: a) use logic devices that provide buffer-type drive capability, thereby eliminating the need for these octal buffers (all FACT devices have the same 24 mA outputs); b) do not have all of the outputs on an octal device switch simultaneously; c) select outputs closer to the ground pin for driv-

ing asynchronous inputs, and d) reduce the V_{DD} level. Any or all of these may be used to eliminate the possibility of system failures due to quiet output noise in the small number of octal applications where these problems might occur. Most applications require no special precautions.

The major points of concern regarding ground bounce:

Ground bounce occurs because of the parasitic inductances found in all conductors.

Ground bounce causes shifts in input thresholds and noise on outputs.

There are many factors which affect the amplitude of the ground bounce:

- Number of outputs switching simultaneously: More outputs mean more ground bounce.
- Type of output load: Lumped capacitive loads generate 2 to 3 times more gorund bounce than system traces. Increasing the capacitive load increases ground bounce to approximately 60–70 pF. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: Outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: Lowering V_{DD} reduces the ground bounce.
- Test fixtures: Standard test fixtures generate 30 to 50% more ground bounce than a typical system since they use capacitive loads which increase the AC load and form LCR tank circuits that oscillate.

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degradation. FACT devices are characterized not to degrade more than 250 ps per additional output switching.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise: FACT's worst case quiet output noise has been measured to be around 500–1100 mV in real system applications.

DESIGN RULES

From this, we can develop a simple set of rules that will protect any system from problems associated with ground bounce. This set of design rules listed below is recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines. These guidelines are the same ones as those they have been using for years for the advanced bipolar logic families.

Use multi-layer boards with V_{DD} and ground planes, with the device power pins soldered directly to the planes, to insure the lowest power line impedances possible.

Use decoupling capacitors for every device, usually 0.10 μF should be adequate. These capacitors should be located as close to the ground pin as possible.

Avoid using sockets or wirewrap boards.

Avoid connecting capacitors directly to the outputs.

In addition, observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce.

Use caution when driving asynchronous TTL-level inputs from CMOS octal outputs.

Use caution when running control lines (set, reset, load, clock, chip select) which are glitch sensitive through the same device that drive data or address lines.

While it is desirable to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

Locate these outputs as close to the ground pin as possible.

Use the lowest V_{DD} as possible or split the power supply.

Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Ground bounce is an unwanted noise source that is found in most logic families available today. Due to increased edge rates and voltage swings, ground bounce can be more of a problem with new Advanced CMOS logic families. National, with the vast experience in high performance logic design gained from its leadership position with the FAST family, defined FACT logic so that high performance problems, as exemplified by ground bounce, were minimized while not sacrificing performance. By following the simple design guidelines outlined, designers can use FACT logic to maximize system performance while ensuring their systems are free from the problems associated with ground bounce.

Dynamic Threshold for Advanced CMOS Logic

National Semiconductor
Application Note 680
Ray Mentzer

INTRODUCTION

Most users of digital logic are quite familiar with the threshold specifications found on family logic data sheets. Designers using products with TTL level input thresholds will see numbers like V_{IH} = 2.0V and V_{IL} = 0.8V. These threshold guarantees are static, a part's response to these levels during switching transients can be undesirable. Through the course of this paper the reader should gain an understanding for the difference between a static threshold and a dynamic threshold. This paper will also discuss how various products respond dynamically, how dynamic thresholds are tested, and specified. Lastly, this paper will look at how FACT Quiet Series™ has addressed and specified dynamic threshold characteristics.

WHAT IS A DYNAMIC THRESHOLD?

If National Semiconductor were able to package its I.C.'s in "ideal" packages, then dynamic and static thresholds would be one and the same. However, our package, like that of all our competitors, is not "ideal" and has a finite amount of inductance associated with each signal lead. As will be shown later, it is the inductance in the power leads which are the primary cause for the non-ideality.

To understand the phenomena of dynamic thresholds the properties of ground bounce must first be examined. *Figure 1* is a representation for a 74XX00 product which includes package inductance. *Figure 2a* shows an output pulldown making an HL/ZL transition. In discharging the load capacitor a current I_C equaling C*dv/dt flows into the chip, this current is approximated versus time in *Figure 2b*. The changing current, I_C, generates a voltage across the ground inductor represented in *Figure 2c* through the equation L*di/dt. It is the voltage across the ground inductor, commonly known as ground bounce, which is the cause for static and dynamic thresholds to differ.

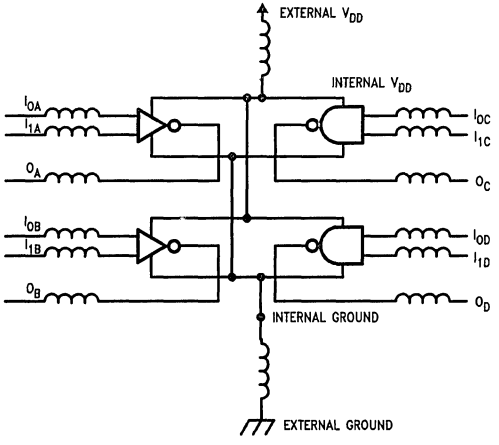

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FIGURE 1. A Typical "00" 2-Input Quad NAND Gate

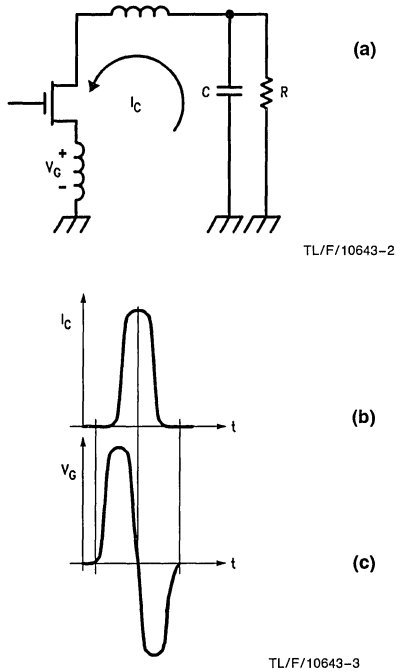

FIGURE 2

The threshold of an IC is referenced to its internal ground. Therefore, voltages induced on the ground inductor are reflected directly as a change in threshold with respect to external ground. *Figure 3* shows the effects of ground bounce on an input threshold. If when the threshold is moving it crosses the input voltage levels, a problem area exists. However, having the threshold cross the input level does not necessarily induce a product failure. The threshold must cross the input level for a period of time for a false switch to occur. (*Figure 4* shows the voltage time relationship). Note that in the high speed technologies two things have come together, faster delays and output edge rates, generally meaning larger di/dt's, and an ability to react to narrower pulses.

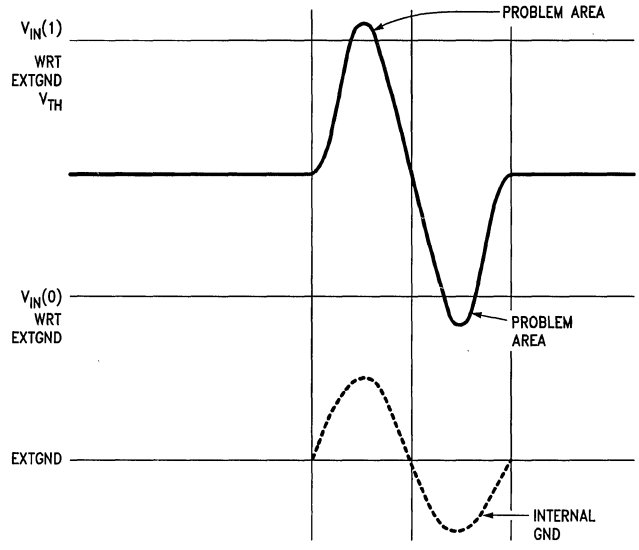

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FIGURE 3

V_{IL} Noise Rejection

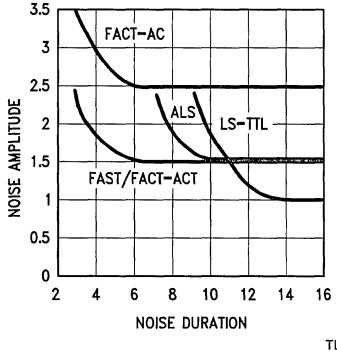

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FIGURE 4

In the example discussed above, ground bounce was outlined as the cause for the threshold change. For bipolar TTL technologies, this is the only noise source of concern since the threshold is created by a V_{BE} stack referenced to ground. As V_{DD} changes in a bipolar circuit, the threshold will change logarithmically as the currents in the transistors change, i.e., a 1V change in V_{DD} creates approximately a 34 mV shift in threshold. CMOS thresholds are set up as a percentage of V_{DD} and track linearly with V_{DD} changes. Therefore, a noise spike on V_{DD} from an LH/ZH transition generates dynamic threshold characteristics which must be considered along with those of the HL/ZL edges. In this example let internal ground bounce to a 1V peak; the bipolar threshold will peak to approximately 2.5V while the CMOS circuit will peak to $((V_{th}/V_{DD}*(V_{DD} - V_{bounce}) + 1.0V) = ((0.3*(4.0) + 1.0) = 2.2V$. Consider a negative bounce of 1V on the internal V_{DD} bus, the threshold delta for the bipolar product will be negligible, but the CMOS chip's threshold will change as follows: $((V_{th}/V_{DD}*(V_{DD} - V_{bounce})) = (0.3*(4)) = 1.2V$.

HOW ARE DYNAMIC THRESHOLDS SPECIFIED?

A circuits dynamic threshold characteristics are quantified with the specifications V_{IHD} and V_{ILD}, where the "D" appendage stands for "dynamic". The definitions are as below,

- V_{IHD}— The minimum HIGH input level such that normal switching/functional characteristics are observed during output transients.
- V_{ILD}— The maximum LOW input level such that normal switching/functional characteristics are observed during output transients.

HOW ARE DYNAMIC THRESHOLDS CHARACTERIZED?

The characterization of dynamic thresholds requires some planning for each product. The test will vary depending upon which edge will generate the supply noise; i.e., is the edge an LH or a ZL? Is the test for a data or control pin? This section discusses the planning process for testing an ACQ244, ACQ374, and an FCT534. From this discussion the reader should be able to test other products and understand the FACT Quiet Series dynamic noise specifications.

Test Fixturing/Setup: Dynamic threshold tests are sensitive to the test configuration. The same considerations used to measure AC propagation delays should be exercised. National Semiconductor uses the same fixturing for both AC propagation delay and noise testing. The inputs for this test are driven with a word generator running at 1 MHz which has been deskewed such that no more than 150 ps exists between channels. FACT Quiet Series specifies V_{IHD}/V_{ILD} at 25°C with V_{DD} at 5.0V. For CMOS, true worst case exists where ground bounce is maximized, at cold temp high V_{DD}. Bipolar circuits are not as straightforward; the threshold has a temperature coefficient tracking its V_{BE} stack which can change nearly a volt from −55°C to +125°C. The temperature and V_{DD} that create worst case bounce may not induce worst case V_{IHD}/V_{ILD}.

Each product subject to V_{IHD}/V_{ILD} testing will have multiple test possibilities. Through the case studies below, the reader should gain an understanding for some of the test tradeoffs.

Case 1: Product = ACTQ244 test data pins with LH/HL transitions.

The algorithm for this test is as follows. Maximize the number of outputs switching, N, in this case 8. N − 1 of the inputs will be transitioning to and from nonthreshold levels, 0V–3V. The last input will transition from 3V to V_{ILD} or from 0V to V_{IHD}. *Figure 5* shows the four combinations of tests. It should be noted that values of V_{ILD} and V_{IHD} that induce failure will vary as a function of the test pin. This is due mostly to voltage drops on the internal power bussing. As a result, pins farthest from the ground pin, and sometimes the V_{CC} pin, are likely to be worst case pins.

Case 2: Product = ACTQ244 test data pins with ZL/ZH transitions.

This test will ramp the enable pin from 3V–0V while holding the input under test at threshold, i.e., have all outputs transitioning ZL, with N − 1 inputs at 0V and the input under test at V_{ILD}. The other tests are as follows, N − 1 transitioning ZL pin under test (PUT) at V_{IHD}, all outs going ZH PUT at V_{IHD}, and N − 1 a ZH switch and PUT at V_{ILD}.

Case 3: Product = ACTQ244 test OE pin with HL/LH transitions.

V_{ILD} is the parameter to check here. Data inputs should be switching 0V–3V while the OE pin is being stepped up from 0V to V_{ILD}. While testing the OE pin with an LH output transition, the standard 50 pF, 500Ω load should be used. When testing with an HL on the output, the TRI-STATE® ZL/LZ 500Ω to V_{CC} * 2 should be used. Without the pullup resistor, failure cannot be detected. The LZ and HZ edges create supply noise by switching off currents being sourced or sunk by the device. With standard AC loading, their transients are much less than those of the other edges. Therefore, V_{IHD} for the chip is guaranteed by the data pins.

The test cases discussed in cases 1–3 are all possible test methods, note there are other possible combinations. In practice National has found that tests done in conjunction with HL transitions are worst case, i.e., case 1, and will guarantee V_{ILD} and V_{IHD} for the chip.

Case 4: Product = ACTQ374

This class of function, the non-inverting register, will have very good data and clock pin dynamic threshold characteristics. For instance, take the worst case bounce where all output are transitioning HL. To accomplish this, all inputs are LOW on the active edge of clock. If a V_{IHD} test of the clock were performed, the positive ground bounce at some level of V_{IHD} will stimulate one, if not multiple, false clocks to occur. A failure is not detected because the false clock or clocks merely regenerated an existing low output. The positive ground bounce had the effect of making the logic low data look lower. Always associated with positive bounce is negative bounce, which on an HL transition occurs later. If this negative bounce is able to switch the internal data gate, setup and hold times have been violated and again failure is not detected. Reference *Figure 6* for a representation of this scenario.

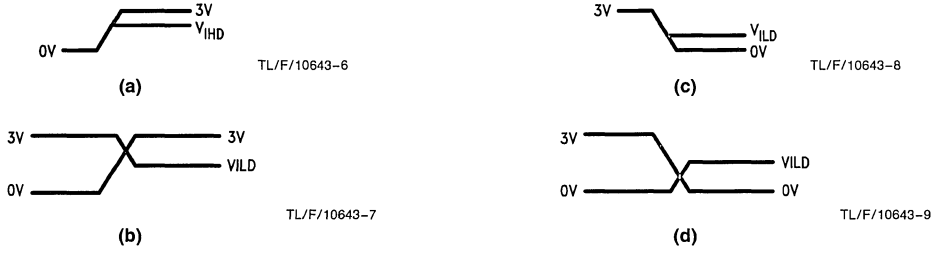
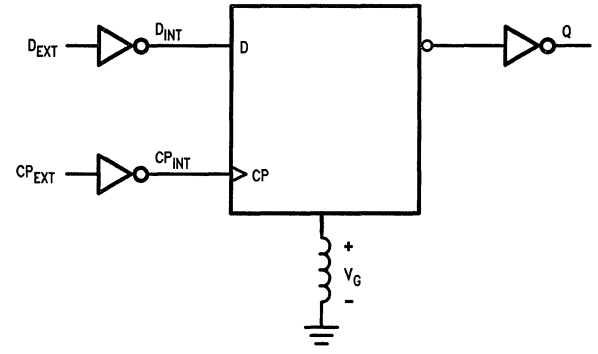


FIGURE 5



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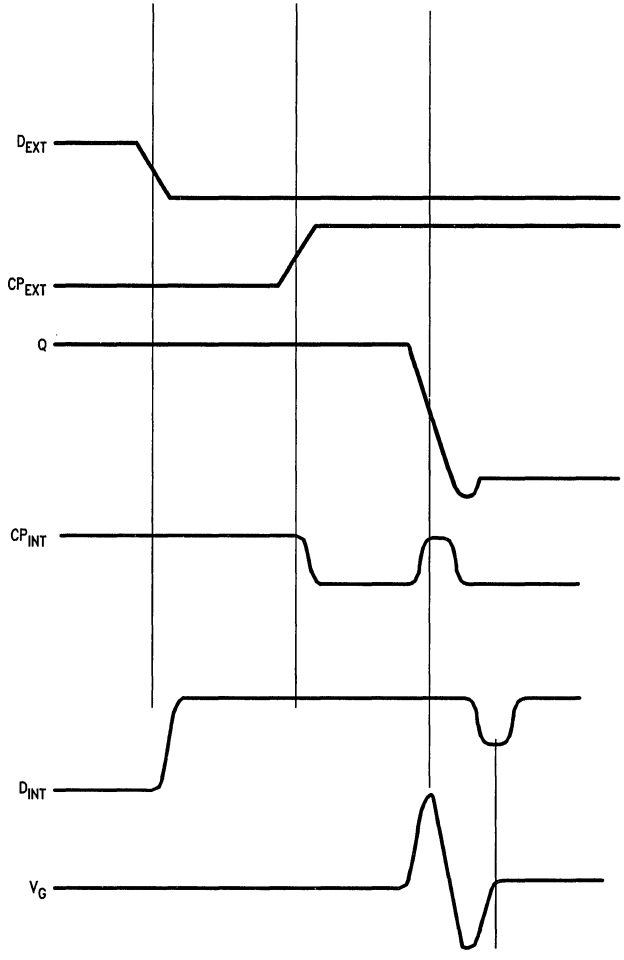
(a)



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(b)

FIGURE 6

The most rigorous test for the non-inverting flop will be to have clock held at V_{IHD}, data at a hard HIGH, and all outputs are transitioning ZL.

Case 5: Product = FCTQ534

The inverting products, as this one is, inherently have poorer V_{IHD}/V_{ILD} characteristics than the non-inverting. While testing a 240 is straightforward, the 534 testing and results require further consideration. While the output is transitioning, both data and clock are HIGH. If data is held at a hard HIGH and clock lowered, false clocks occur, but a failure is not detected. The reverse is also true, as data is lowered, the data gate changes, but no clocks occur. However, as both data and clock HIGH levels are lowered simultaneously a window of V_{IHD} failure will be observed.

Figure 7 plots this "window of failure". This plot will be examined by sweeping from right to left. It can be seen that for clock V_{IHD} levels down to approximately 2.6V, proper data continues to clock out for data levels down to 1.5V, the static threshold value. For all V_{IHD} voltages of the clock below 2.6V, false clocking exists. If data is raised high enough, no internal data changes occur and therefore no product test failures. A data is lowered, internal data pulses down (*Figure 8*). The initial internal pulses may not cause device failure either because the voltage has not dropped to a valid logic level or because setup and hold times to the master latch have not been satisified, but eventually failures are observed. It is interesting to note that were the FCT534 to have a more positive hold time, its hold time is slightly negative, the data voltage inducing failure would be much lower.

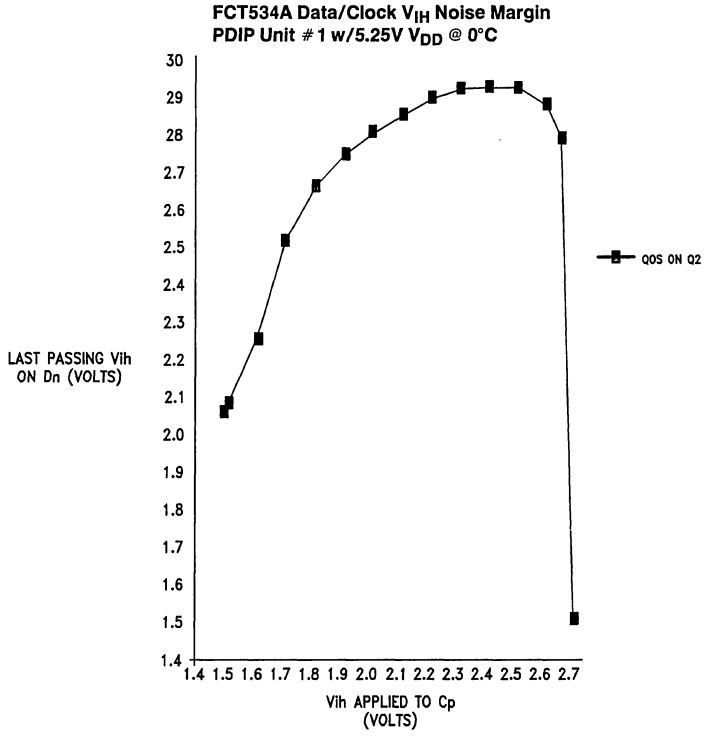

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FIGURE 7

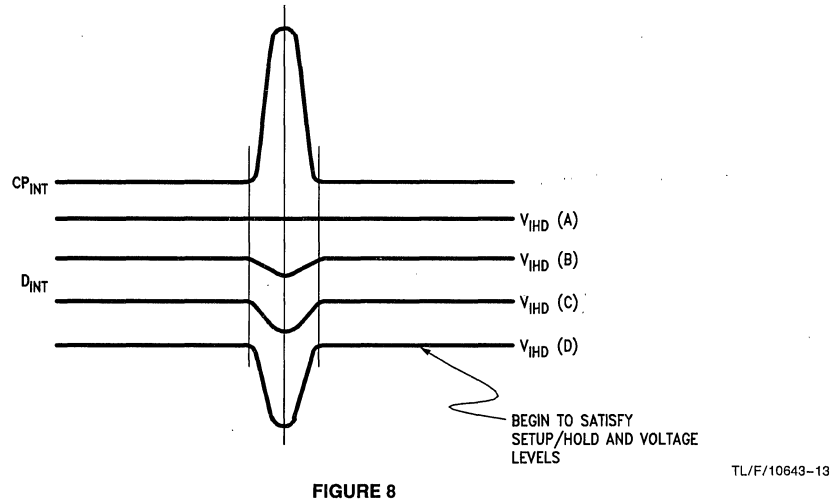


FIGURE 8

The implication of the data in *Figure 7* is that if the high voltage levels droop down to approximately 2.9V on data and 2.6V on clock simultaneously, a system failure is possible. How can these conditions exist at the same time? The temperature of *Figure 7* is 0°C, if the inputs are driven by TTL drivers at a V_{DD} = 4.5V, 2.6V V_{OH}'s are possible. However, the V_{DD} of the plot is 5.25, assuming the driver TTL chips are on the V_{DD} bus, the HIGH levels will be greater than 2.6V. There is another variable to be considered before stating that no problem exists: what termination scheme is being used? If both data and clock signals come from transmission lines using either parallel or thevenin termination, HIGH voltage levels below 2.6V are possible. If either or both of the signals are unterminated, series terminated, or AC terminated then functionality is assured. In summary, a problem may exist if this parts data and clock pins are driven by parallel or thevenin terminated transmission lines while the V_{DD} bus is at 5.25V and the junction temperature is 0°C.

HOW DO DYNAMIC THRESHOLD PROBLEMS MANIFEST THEMSELVES?

There are three main modes of failure during dynamic threshold testing. Firstly, the part can malfunction through a state change. Also possible are oscillations, glitches, AC delay changes, and slew rate degradation. One octal register tested recently was seen to exhibit metastable type characteristics. Failure criteria are as follows.

- On a LOW output the LOW level will not rise above a TTL threshold LOW, 0.8V, after the transition of the output.
- On a HIGH output the HIGH level will not drop below a CMOS threshold HIGH, 3.5V @ V_{DD} = 5.0V, after the transition of the output.
- If the natural ringing, other than initial switching rail bounce, of the output violates the previous two criteria then the ringing amplitude will be noted. Failure is then defined as a 100 mV movement in the output toward the threshold from the peak ringing amplitude, (*Figure 9*).
- Gross failures will include functional state changes, oscillations, AC delay changes, and slew rates effects.

HOW DO DYNAMIC THRESHOLD PROBLEMS AFFECT DIFFERENT FUNCTIONS?

All the products discussed thus far pass the FACT Quiet Series dynamic threshold limits of V_{IHD} = 2.2V and V_{ILD} = 0.8V, which are specified as being tested singularly. The case of the FCTQ534 represents one where much effort was required to observe the failure mode. There are classes of product that will display clock V_{IHD} failures readily. These would be products which toggle the outputs independent of data. The most common functions in the list would be counters and shift registers. If the 74XXX299 clock pin were tested, the initial clock edge would shift data inducing ground bounce. If the clock V_{IHD} is low enough, it will be that observed false clocks will continue until all outputs are in the same logic state as the serial data pin.

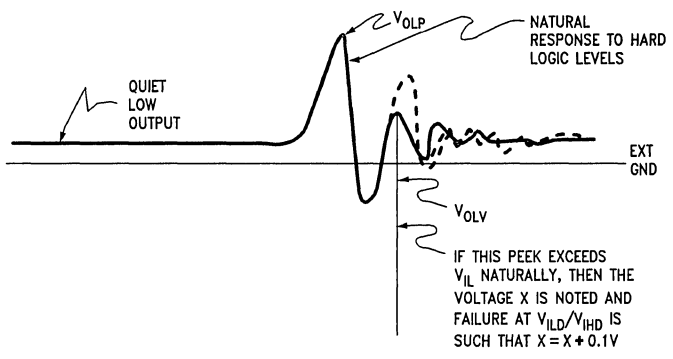


FIGURE 9

WHAT DOES FACT QUIET SERIES DO TO ADDRESS DYNAMIC THRESHOLDS?

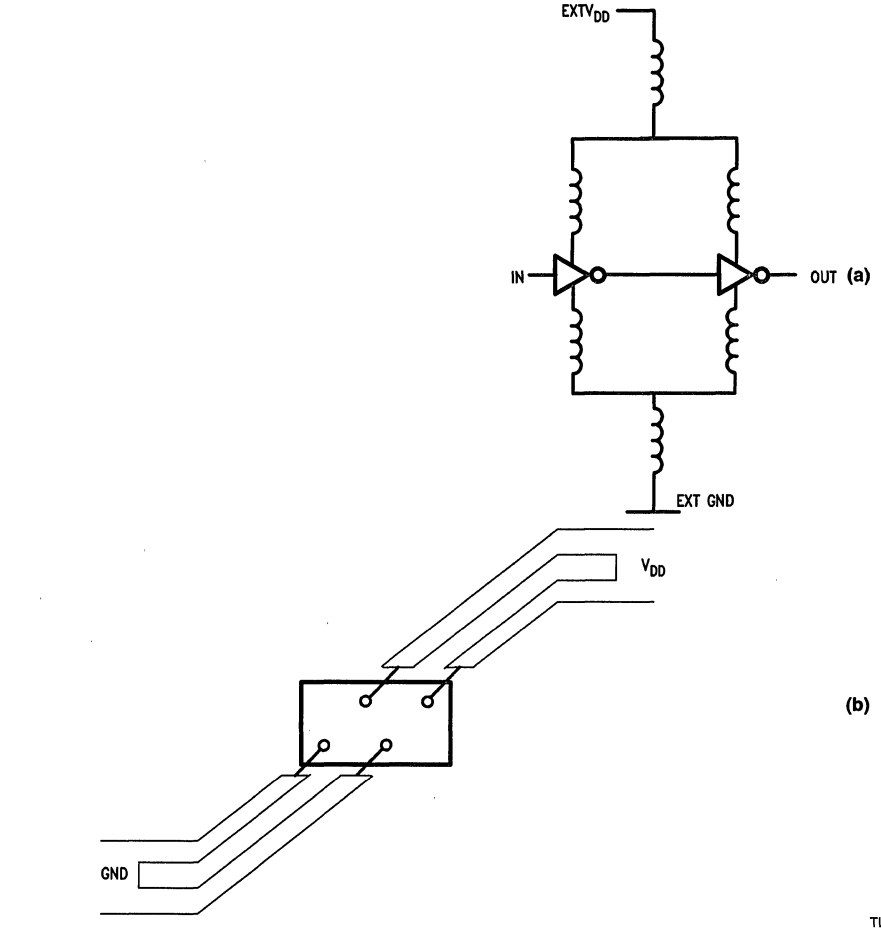
The Quiet Series product utilizes two technical innovations to accomplish its performance. First, by using a split ground bus configuration, input and output grounds are given a degree of isolation. Schematically this is shown in *Figures 10a* and *b*. The ground bus for inputs stages and outputs sections are separated on chip and only connected by the common inductance near the shoulder of the package and a mutual inductance between the leadframe fingers. Note, the V_{DD} input and output V_{DD} busses are electrically shorted on chip by the substrate resistance. The leadframe inductance forms a voltage divider such that the input only sees a percentage of the output ground noise. Secondly, a proprietary GTO™ technology, shown in *Figure 10c*, is used to shape the output edge. This then yields an output voltage waveform shown in *Figure 10d*. The soft turn on of the output attenuates the dv/dt, and therefore the di/dt presented to the ground inductance, yielding a reduction in the ground noise.

HOW DOES NATIONAL COMPARE WITH OTHER VENDORS?

The characteristics of National Semiconductor's FACT Quiet Series ensure superior dynamic threshold performance in conventional corner pinned packaging. The split power rail technology used to isolate inputs and outputs addresses a noise issue which goes unresolved in multiple power pin ACL logic families, and most single pin families. The same split rail technology is used in the FACT FCT and FCTA logic lines. Referencing the FCT534 already discussed, *Figure 11* shows one of the dramatic differences created by the Quiet Series technology.

SUMMARY

With the new advanced CMOS technologies, the specifications and characteristics for dynamic thresholds need to be considered along with the other variables that impact the choice of a device type or family. This applications note has discussed the theories of test philosophy, failure criteria, and the root causes of dynamic thresholds. This information should provide the systems designer the tools to analyze any impact to design performance.


EXTV$_{DD}$
IN
OUT
(a)
EXT GND
V$_{DD}$
(b)
GND
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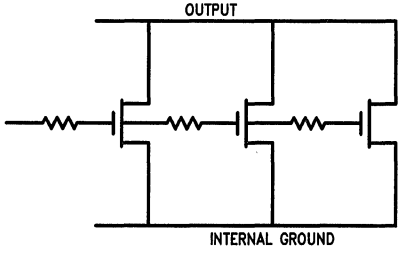
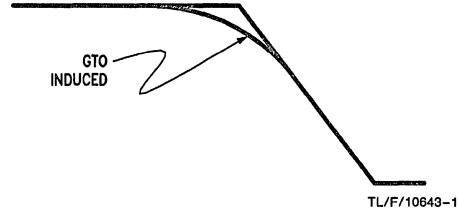

OUTPUT
INTERNAL GROUND
TL/F/10643–16
(c)


GTO
INDUCED
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(d)

FIGURE 10

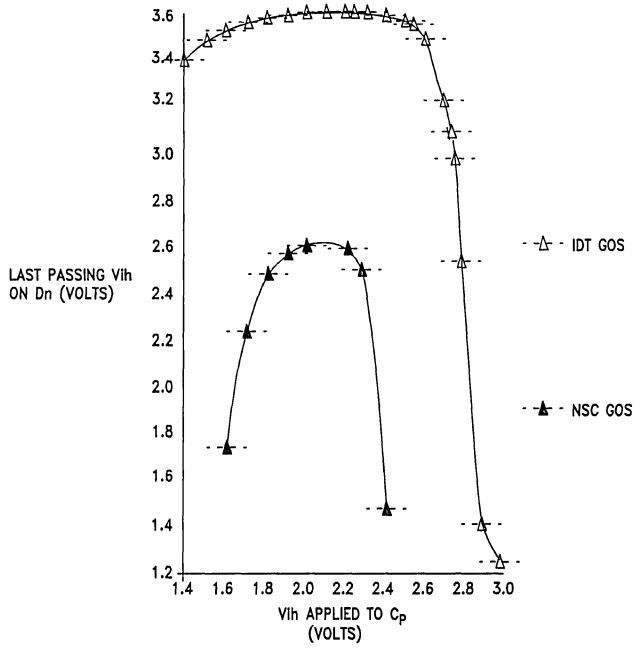

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FIGURE 11. 'FCT534A Data/Clock V_{IH} Noise Margin IDT #5 (PDIP) vs NSC #2 (CDIP) 5.0V V_{DD} @ Room

Design Innovations Address Advanced CMOS Logic Noise Considerations

National Semiconductor
Application Note 690
Michael L. Gilbert

UNDERSTANDING THE FUNDAMENTALS OF NOISE

Today's electronic system designers are becoming increasingly more familiar with the issues involved in migrating to high-speed logic. One key issue is total system noise.

Noise in an electronic system can be described according to its source. The first category is system-generated noise, i.e., noise generated from the printed board up, such as power distribution and decoupling noise, crosstalk noise, electromagnetic interference (EMI), and transmission line reflections. System noise is a function of signal characteristics such as edge rate, voltage swing, and frequency. This type of noise can be minimized by strictly adhering to proper printed circuit board design practice commonplace in the design of ECL-based systems. The system designer can do more to control this type of noise than device-generated noise.

Device-generated noise is the second category, i.e., noise that is generated at the integrated circuit level such as simultaneous switching noise, or ground bounce, device undershoot, and dynamic input threshold shift. System designers may use techniques that minimize the level of device-generated noise. Device-generated noise is more effectively minimized by the IC designer and manufacturer. In some asynchronous applications, such as the distribution of timing signals, use of inherently lower-noise ICs can be critical.

CONTROLLING SYSTEM-GENERATED NOISE IS CRITICAL

The power distribution network is a key source of system noise. High-performance logic switches large amounts of current in a short amount of time and almost always requires multiple-plane printed circuit boards with separate power and ground planes instead of traces. Due to their high impedance, power and ground traces may generate too large of a power supply droop for low noise systems.

In addition, the logic's switching-current demand also requires bypass capacitors for each device, located as close to power or ground pin as possible. Usually a 0.1 μF ceramic chip capacitor provides adequate decoupling. Including power supply decoupling at every step of the system design is critical for a high-performance, low-noise system. Power supply noise is easily coupled and radiated throughout the system.

Crosstalk is another system noise. If not addressed during system design, it can create problems in high-performance systems. Crosstalk refers to the noise created when a signal on an "active" trace is coupled onto an adjacent parallel "quiet" signal trace.

Forward crosstalk manifests itself as a negative voltage spike on the adjacent quiet trace and results from mutual inductance effects. Its amplitude and duration are generally much less than reverse crosstalk. Reverse crosstalk is noise on the quiet trace resulting from a combination of capacitively-coupled and mutually-induced energy from the active signal trace. Its amplitude and duration are determined by the active signal's edge rate and the length of adjacent parallel traces. The faster the edge or the closer the adjacent traces, the higher the crosstalk amplitude. The longer the adjacent traces run, the longer the duration of the reverse crosstalk. Reverse crosstalk travels in the direction opposite to the active signal's propagation and lasts for twice the one-way delay time of the signal trace.

Crosstalk control methods include minimizing the coupled trace length and maximizing the distance between the two adjacent traces. If board area does not allow large spaces between lines, the insertion of a ground trace between the two adjacent traces also minimizes crosstalk.

Proper termination of all adjacent traces is important in minimizing crosstalk. Reflections are also propagating signals and will create crosstalk. Terminating adjacent transmission lines will eliminate the reflected signal.

Electromagnetic Interference (EMI) is another type of system noise. EMI is the radiation of energy outside the system. Whenever an electric charge is accelerated, electromagnetic waves result. The efficiency of this process is mainly determined by the geometry of the charge paths. The most significant charge paths in a system are the printed circuit board signal traces, power supplies, and I/O cables. The largest and most plentiful charge paths, they are also leading sources of EMI.

The EMI bandwidth is a function of the signal frequency, amplitude, edge rate, duty cycle, edge discontinuity, and ringing. These characteristics of high-performance logic, especially advanced CMOS logic, can cause signal traces and I/O cables to radiate more noise than ever before. The higher frequencies generated as a result of these characteristics will radiate more efficiently from signal lines because of their shorter wavelengths.

Addressing the characteristics of a signal that may create EMI is critical to reducing EMI, or achieving electromagnetic compatibility (EMC). Reliable solutions to EMC include proper shielding and grounding of all cables as well as proper termination of all signal traces. Adhering to other system design guidelines for power supply decoupling and crosstalk can also minimize EMI. Some of the output edge control techniques discussed later will also minimize EMI by directly effecting several key signal characteristics.

The last major form system noise is reflections on the transmission line and the resultant ringing. Ringing observed on signal traces has two sources: one is system-generated; the other, device-generated. The two are often confused. It is important to note that improperly terminated transmission lines will create ringing caused by reflections, i.e., system-generated noise.

Reflections are caused by mismatches in impedance from driver to transmission line or from transmission line to receiver/termination. The magnitude of these reflections is related to the length of the transmission line and the impedance along the line. Transmission line impedances and driver/receiver I/O impedances seldom match. Most often

these impedances are orders of magnitude different. With the edge rates of today's advanced CMOS logic, transmission lines of approximately 20 centimeters (8 inches) or longer will most probably need some type of termination.

Choosing the right termination scheme is important. When designing with low-power advanced CMOS, do not select a termination that will dissipate several tens of milliamperes. Popular bipolar terminations such as a DC parallel termination (resistor to ground) or a Thevenin (voltage divider) termination (resistors to both rails) draw large amounts of DC current. Effective termination schemes that preserve low CMOS power consumption are a series resistor (for a single driver/receiver pair) or an AC parallel termination (resistor in series with a capacitor to ground) for distributed multiple loads.

Device-generated ringing is due to the parasitic LCR tank circuits in the IC and its load. The stimulus for this type of ringing is an overshoot or undershoot in the output signal. This ringing is minimized by slowing the output edge rate with higher loads or by improvements in IC circuitry.

WHAT IS DEVICE-GENERATED NOISE?

Device-generated noise includes dynamic threshold shift, ground bounce, and output undershoot.

The first type of device-generated noise is dynamic threshold shift. System designers are very familiar with DC input threshold requirements, namely V_{IH} (Input Voltage HIGH) and V_{IL} (Input Voltage LOW). For TTL-based logic, these levels are typically 2.0V and 0.8V, respectively. For CMOS-based logic, these levels are typically 70% and 30% of V_{DD}, respectively and are measured and guaranteed in a static (DC) mode only. Switching any part of the device-under-test is an invalid condition. In a real-life situation the IC is dynamic and so are the input thresholds.

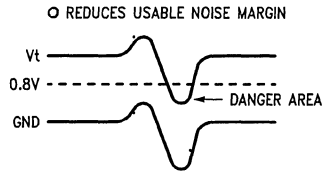

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FIGURE 1. Dynamic Threshold

Dynamic input threshold shifts arise when one or several of the inputs are toggled, generating noise on the device's on-chip power rails. The input threshold voltage is proportional to the power supply voltage. Any fluctuation of these rails, such as ground bounce and/or undershoot, will create fluctuations of the input threshold. *Figure 1* illustrates a negative excursion on the internal ground of an IC. The input threshold tracks this excursion and crosses through the static LOW input level. This creates an unwanted change of state on the output when the threshold falls below the input level. In this case, an undershoot caused by bounce on the chip ground causes a normally valid input level to create an invalid output state.

Dynamic threshold shifts may create problems on synchronizing inputs should the device's output noise be great enough to cause the device's threshold voltage to shift across the input voltage level. On TTL-compatible inputs, dynamic threshold shifts could substantially reduce an already low noise margin.

In addition to causing erroneous changes in state, the output may begin to go into a high-frequency oscillation as input voltage levels approach the dynamic threshold. Regardless of whether the input in question is a synchronizing input, this high frequency oscillation will increase chip heating. Should this situation continue, device reliability could be effected.

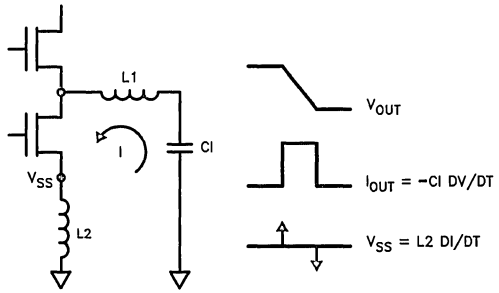

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FIGURE 2. Ground Bounce Model

The second type of device-generated noise is ground bounce or simultaneous switching noise. Ground bounce or V_{OLP} (Voltage Output LOW, Peak) and undershoot or V_{OLV} (Voltage Output LOW, Valley) are names given to noise levels associated with the output of a logic device. While these two issues are not new to logic, they are of greater concern with advanced logic families. Since advanced CMOS outputs switch rail to rail at high speed and into heavy loads, performance and design concerns have risen in this area.

Similary, V_{DD} droop and overshoot are also device-generated noise issues. However, since both affect the logic HIGH level and since using CMOS outputs to drive TTL inputs provides much higher noise margin than the logic LOW level, this discussion focuses on low-level noise margin issues.

As the model in *Figure 2* illustrates, ground bounce is the voltage induced on the device ground inductance by current as it quickly discharges from a capacitive load, sinking into the output's N-channel transistor. The greater the amount and rate of discharge that is created by multiple simultaneously switching outputs, the greater the ground bounce level. Essentially there are more current sources sinking current into the same ground inductor.

Device undershoot or V_{OLV} (Voltage Output LOW, Valley) is simply a function of the LCR tank circuit at the output. As edge rates increase, undershoot and subsequent ringing increase. Undershoot also decreases as the capacitive load on the output increase and/or as the inductance of the output decreases. Therefore, advanced CMOS logic devices driving one or two other advanced CMOS logic devices will have more undershoot than an advanced CMOS device driving a heavily loaded bus. For this reason, in most systems undershoot levels are much less than those observed in test fixture environments. Also, improper bus termination may appear to worsen undershoot. In fact it is the energy of the reflected wave that increases the undershoot and not the device itself. Most undershoot levels in excess of 2.0V are the result of some mismatched impedance along the transmission line and can be eliminated with proper termination.

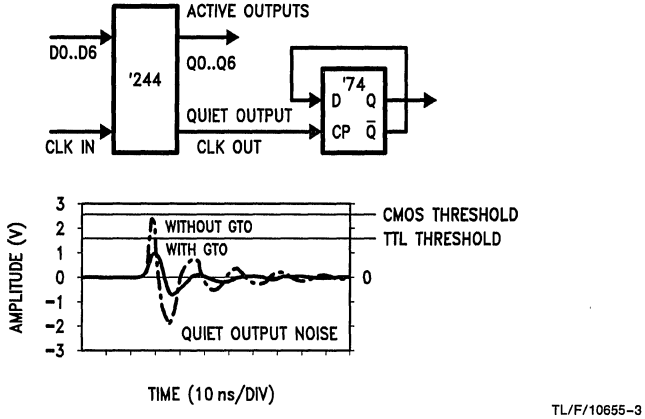

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FIGURE 3. Example of Ground Bounce

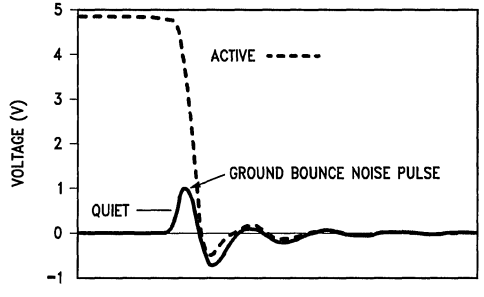

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FIGURE 4. Location of Bounce Pulse

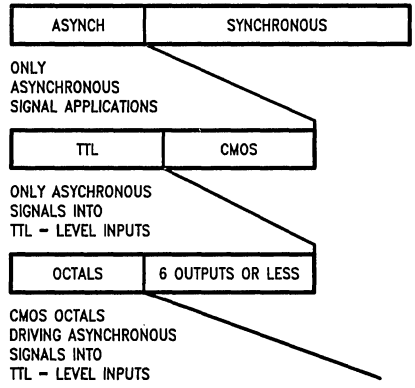


FIGURE 5. Application Segments

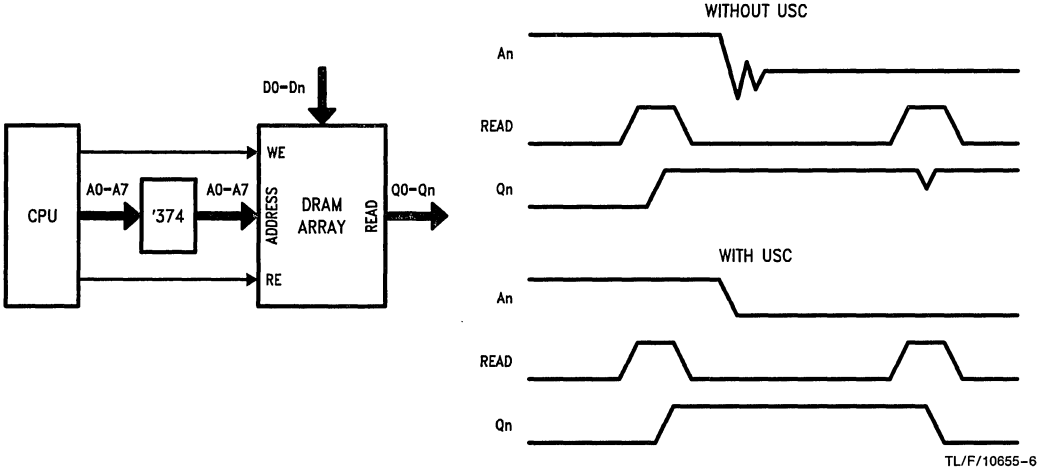


FIGURE 6. Example of Undershoot

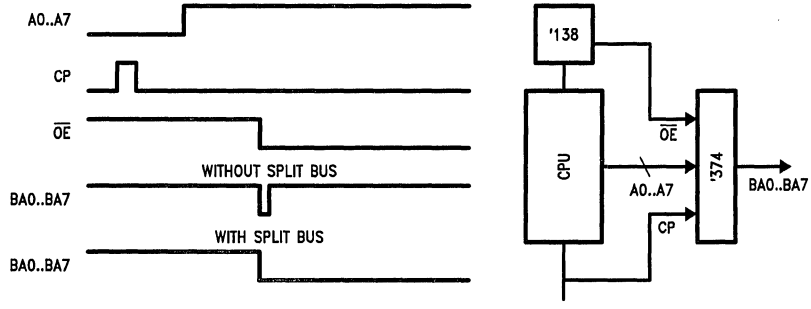


FIGURE 7. Example of Dynamic Threshold Shift

WHERE CAN DEVICE-GENERATED NOISE AFFECT SYSTEM PERFORMANCE?

An integrated circuit ground inductor's di/dt is determined by the number of outputs switching and the capacitive load on each output. In a system, transmission line effects will reduce the effective capacitive load the output may actually drive. In a test fixture, the load is made up of low-dissipation factor chip capacitors soldered directly to the output pins. In a system, a finite physical distance separates the various capacitive loads from each other as well as the driver's output. The net effect of capacitance distributed along the transmission line is to lower the effective impedance of the transmission line. As a result, ground bounce in a system is typically 50% less than test fixture measurements. Test fixture measurements of ground bounce should only be used for comparative analysis and characterization.

The magnitude of system ground bounce and the segment of applications where that bounce may present problems is very small. Ground bounce occurs concurrently with the transition of the active outputs of the device. Ground bounce on quiet output(s) driving synchronous signals—such as data and address lines—are not of concern since these signals will not be synchronized or sampled until long after ground bounce has settled out. See *Figure 4.*

However, while asynchronous signals, such as resets, presets, latch enables, and clock lines, typically number far fewer than synchronous signals in a system they may be more susceptible to ground bounce.

Since substantial ground bounce voltage levels are only achieved with six or more outputs switching simultaneously in the same package, device with eight or more bits, i.e., octals, are the primary focus of ground bounce.

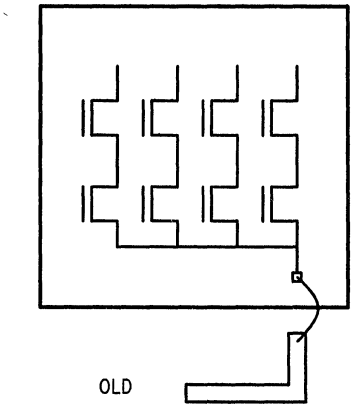
Also, noise signals, such as ground bounce, driven into CMOS-level inputs generally have no effect due to the higher amount of energy needed to switch CMOS inputs. Typical voltage levels needed to switch full CMOS inputs are 3.0V for approximately 2.0 ns; ground bounce levels in a system or a test fixture do not reach this level. However, ground bounce on asynchronous signals into TTL-input levels may cause system errors. Typically TTL inputs need only 1.7V of noise of 2.0 ns to switch (e.g. FAST® and ALS).

For these reasons, the small segment of applications where ground bounce noise may compound with system noise levels and possibly affect system performance is where advanced CMOS octals drive asynchronous signals into TTL-level inputs. See *Figure 5.* Since the mechanisms are similar, shifts in dynamic threshold are also a possible concern in this small segment.

Undershoot, either on quiescent low or high-to-low switching outputs, can create noise problems in some systems by generating excess ringing on the signal line. As stated earlier, ringing also adds to EMI and crosstalk noise. Additionally, most devices driven by logic devices have clamp diodes on their inputs that will limit the input voltage excursions. However, as devices such as DRAMs, DACs, and PLDs have no protection and are sensitive to negative voltage excursions on the input, system faults or damage to these devices, caused by latch-up, may result. The use of series resistors can safeguard against such faults.

The system designer may further minimize ground bounce and undershoot effects by choosing surface mount technology (SMT). SMT package inductance on the order of 2 nH to 4 nH can reduce ground bounce and undershoot by as much as 25%, without the board area penalty incurred by larger non-standard pinout. Also, if the design allows, placing asynchronous signal lines on pins closest to the ground pin will minimize the noise on these lines—as much as 20% less noise than pins furthest from ground.

If device-generated noise is still a critical issue in the system design, National Semiconductor Corporation has implemented several design improvements that greatly minimize device-generated noise. The result is an extension to the FACT™ line—FACT Quiet Series or FACT QS.



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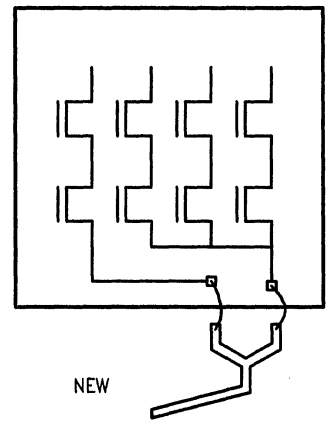

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FIGURE 8. Split Ground Bus Structure

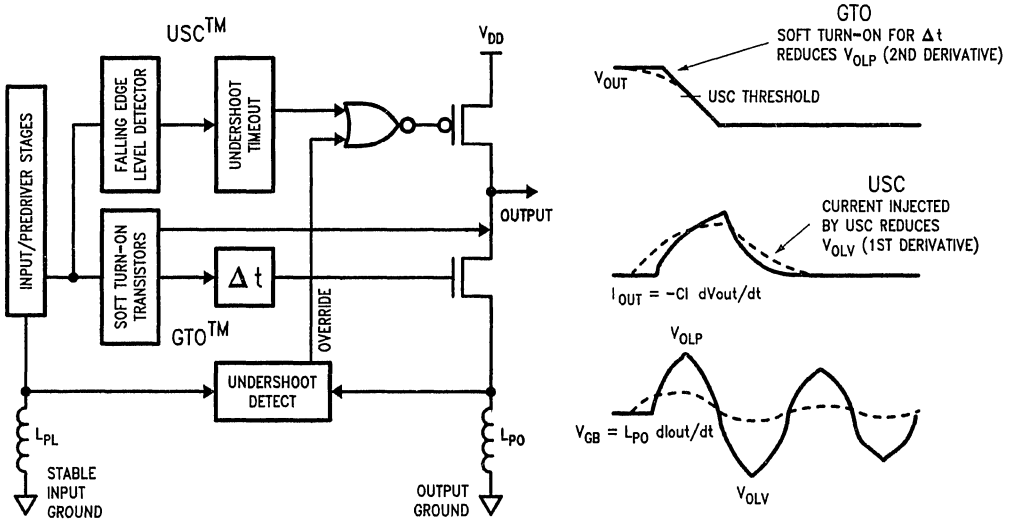

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FIGURE 9. National Semiconductor's Proprietary Noise Control Circuitry

DESIGN INNOVATIONS RESOLVE DEVICE NOISE ISSUES

FACT Quiet Series implements patented technological breakthroughs in device-generated noise suppression as well as several major performance improvements. Design improvements include a split ground bus and leadframe, a graduated output N-channel turn-on circuit, and an output undershoot correction circuit.

The first design improvement, a split ground bus and leadframe, addresses dynamic threshold shift. Since the cause of threshold shift is noise on the IC ground bus created by simultaneous output switching, separating the output and input ground buses virtually eliminates dynamic threshold shift.

FACT QS has separate on-chip ground buses for the input transistors and for the remainder of the internal gates, including the output transistors. FACT QS goes one step further to isolate output noise from the inputs by implementing a split leadframe for the ground pin. *Figure 8* illustrates the change in the ground bus structure. Note that the split leadframe joins just prior to exiting the cavity. Standard pinout, package quality, and reliability are maintained using this technique.

Resulting from output noise, dynamic threshold shifts are worst-case under conditions of multiple simultaneously switching outputs. Values of dynamic thresholds on advanced CMOS without the split ground bus and leadframe range from 0.3V to 0.7V.

The result of the split ground bus and leadframe is a dynamic threshold equivalent to the static threshold. For FACT ACTQ logic, typical dynamic threshold is 1.4V for a logic low. In this way, output switching noise becomes inconsequent to the input using split ground bussing. National Semiconductor's FACT QS, FACT FCT and FACT FCTA logic lines all incorporate split ground bus and leadframe improvements.

A second design improvement, a graduated output N-channel turn-on circuit (GTO™), greatly reduces ground bounce. As *Figure 2* illustrated, ground bounce is a function of the output waveshape, d^2v/dt^2. Reducing package and chip inductance does have some effect in reducing ground bounce, but the reduction in ground bounce is not linear with inductance reduction. Package inductances may change by an order of magnitude, yet ground bounce is reduced only by as much as 25%.

Second order effects, such as increases in di/dt as output reactance is decreased, cause ground bounce reductions to flatten as inductance is reduced. The cost of reducing inductance on dual-in-line packages is an increased number of power and ground pins, increased package size, and a non-standard pinout. Package pinout changes have negligible effect on surface mount devices where inductance is low to begin with.

The greater reduction in ground bounce is found by rounding the transition point on the high-to-low edge, or waveshaping. *Figure 9* illustrates the effect of output waveshaping on ground bounce. This waveshaping is actually achieved by combining several design techniques. The two most notable are the slow decay of the load capacitance charge through a soft turn-on circuit prior to the actual transition, and the delaying of the actual turn-on of the large N-channel output transistor.

Since ground bounce levels are more substantial on the high-to-low transition, the low-to-high transition remains unchanged. In addition, design considerations were taken to ensure the integrity of the high-to-low edge rate, and thereby maintain device AC performance.

Ground bounce on advanced CMOS logic without output waveshaping is on the order of 2.0V to 3.0V V_{OLP} in a test fixture environment. In the same environment, FACT QS, with the GTO circuitry, provides V_{OLP} performance in the range of 1.0V to 1.3V. In a system, 30% to 50% lower V_{OLP}s should result.

The third design improvement, undershoot corrector circuitry (USC™), reduces output undershoot, both on the switching and quiescent (at ground) outputs. Undershoot is also a matter of di/dt. As output edge rates speed up and voltage swings increase, undershoot increases. Undershoot also increases as the number of simultaneously switching outputs increases. The result, V_{OLV}, can be seen on both the switching edges as well as outputs quiescent at ground.

The undershoot correction circuit works by limiting negative di/dt excursions. The first part of this two-stage circuit senses a high-to-low edge. At a predetermined point on that edge, the undershoot corrector is turned on. The corrector simply activates a P-channel transistor which sources current into the output. This softens the di/dt that occurs when the load is depleted of charge. An internal RC timer controls the duration and decay of the correction.

Should the RC timer time out before undershoot is fully resolved, a differential amplifier, sensing that the output voltage is still below the input ground, keeps the current source turned on.This two-stage design is more reliable because of the time required for the current injector to turn on after the output goes negative.

Because USC operation is affected by package inductance, plastic DIP packages react differently than ceramic DIP packages. Similarly, surface mount devices have a different correction level. As ground bounce and undershoot decrease with decreasing inductance, the need for undershoot correction also decreases with decreasing inductance.

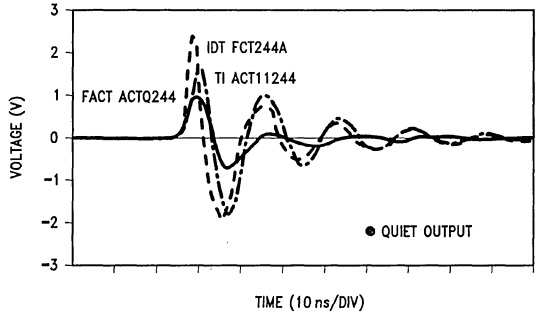

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FIGURE 10. ACMOS Comparison

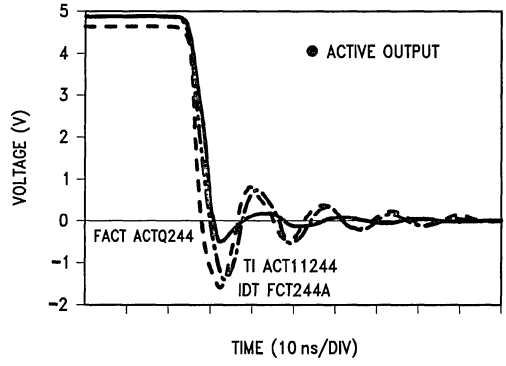

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FIGURE 11. ACMOS Comparison

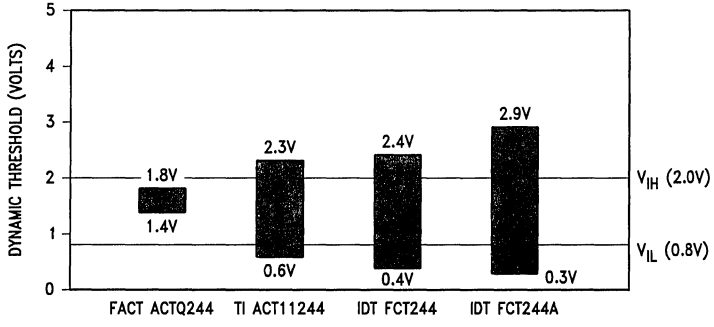

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FIGURE 12. ACMOS Dynamic Threshold Comparison

OUTPUT CONTROL CIRCUITRY RESULTS IN LOWER NOISE

Figures 10 and *11* compare three major ACMOS product lines. These ACMOS manufacturers have different levels of noise suppression. All measurements were taken using an industry-accepted fixture and methodology.

FACT QS is manufactured on a smaller geometry CMOS process than standard FACT products. Because of the use of this technology, FACT QS AC speeds are faster than standard FACT. Propagation delays as well as set-up and hold times are also specified identically to or faster than standard FACT.

DESIGN IMPROVEMENTS GO BEYOND NOISE

In addition to improvements which reduce device-generated noise, FACT QS also incorporates design improvements for greatly enhanced performance and reliability. These parameters include specification of output pin-to-pin propagation delay skew, higher electrostatic discharge (ESD) immunity, and higher latchup immunity, than standard FACT products.

Pin-to-pin skew becomes an issue as high-performance logic is designed into clock distribution and other timing-sensitive applications. Since, part-to-part skews are not effected by variations in V_{DD} or temperature, the only variable that could effect part-to-part skew is processing variations from one device to another. Part-to-part skews may be interpreted by subtracting the 25°C, 5.0V − V_{DD} propagation delay minimum specification from the maximum specification on most advanced CMOS logic data sheets.

Guaranteed ACMOS logic pin-to-pin skew specifications are unique to National Semiconductor's FACT QS product line. For clock distribution applications where all outputs transition to the same state simultaneously, output skew is typically less than 500 ps, with worst case being 1.0 ns. For bus applications where outputs can transition to either state simultaneously, typical skew is less than 800 ps, with worst case being 1.0 ns.

Another performance improvement is higher ESD immunity. Process improvements for FACT QS have improved ESD immunity to 8,000V or better. ESD is specified at 6,000V typical, with worst case being at 4,000V minimum. MIL Class 3 (4,000V or more) is guaranteed.

A third performance improvement in National's FACT QS is a higher latch-up immunity specification. As with standard FACT, the implementation of epitaxial silicon in the FACT process essentially eliminated latch-up possibility. The currents needed to latch-up devices manufactured on the FACT processes are typically in excess of 1A. FACT QS latchup immunity is tested to 300 mA on the inputs and up to 1A on the outputs. Latchup immunity is specified at 300 mA minimum at +125°C.

REFERENCES AND BIBLIOGRAPHY

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"FACT™ Advanced CMOS Logic Databook", National Semiconductor Corporation, 1989.

"Terminations for Advanced CMOS Logic", Applications Note 610, National Semiconductor Corporation, May 1989.

J.L. Norman Violette, Donald R.J. White, and Michael F. Violette, *Electromagnetic Compatibility Handbook,* Van Nostrand Reinhold Co., New York, 1987.

Section 4

Advanced CMOS Datasheets

Section 4 Contents

Section 4 Contents (Continued)

Section 4 Contents (Continued)

National Semiconductor

54AC/74AC00 • 54ACT/74ACT00
Quad 2-Input NAND Gate

General Description

The 'AC/'ACT00 contains four 2-input NAND gates.

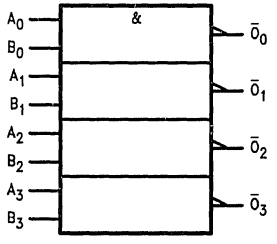
Features

- Outputs source/sink 24 mA
- 'ACT00 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC00: 5962-87549
  - — 'ACT00: 5962-87699

Ordering Code: See Section 8

Logic Symbol

IEEE/IEC



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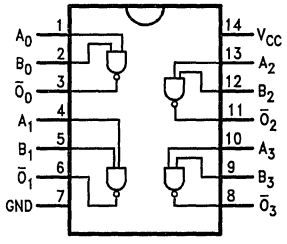
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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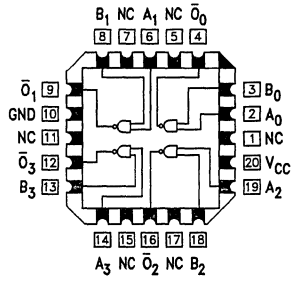
Pin Assignment for LCC



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Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	2.0	7.0	9.5	1.0	11.0	2.0	10.0	ns	2-3,4
		5.0	1.5	6.0	8.0	1.0	8.5	1.5	8.5		
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.0	1.0	9.0	1.0	8.5	ns	2-3,4
		5.0	1.5	4.5	6.5	1.0	7.0	1.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.5	5.5	9.0	1.0	9.5	1.0	9.5	ns	2-3,4
t_{PHL}	Propagation Delay	5.0	1.5	4.0	7.0	1.0	8.0	1.0	8.0	ns	2-3,4

Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC02•54ACT/74ACT02
Quad 2-Input NOR Gate

General Description

The 'AC02/'ACT02 contains four, 2-input NOR gates.

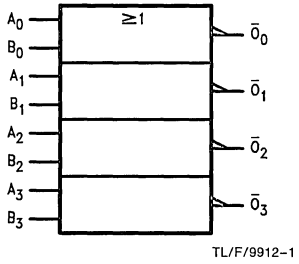
The information on the ACT02 is Preliminary Information Only.

Features

- Outputs source/sink 24 mA
- 'ACT02 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — AC02: 5962-87612

Ordering Code: See Section 8

Logic Symbol



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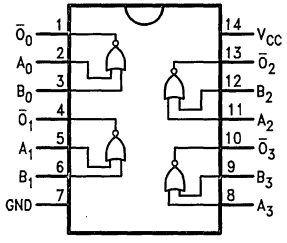
Connection Diagrams



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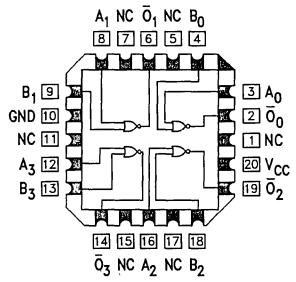


TL/F/9912–2

Pin Names	Description
A_n, B_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.76		I_{OH} −24 mA
		5.5		4.86	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.5	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5		I_{OL} 24 mA
		5.5		0.36	0.5		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	5.0	7.5	1.0	9.0	1.0	8.0	ns	2-3,4
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		
t_{PHL}	Propagation Delay	3.3	1.5	5.0	7.5	1.0	9.0	1.0	8.0	ns	2-3,4
		5.0	1.5	4.5	6.5	1.0	7.5	1.0	7.0		

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	6.0	8.5			1.0	9.0	ns	2-3,4
t_{PHL}	Propagation Delay	5.0	1.0	6.5	9.5			1.0	10.0	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC04 • 54ACT/74ACT04
Hex Inverter

General Description

The 'AC/'ACT04 contains six inverters.

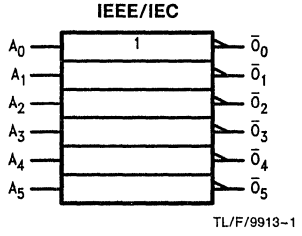
The information for the ACT04 is preliminary information only.

Features

- Outputs source/sink 24 mA
- 'ACT04 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'AC04: 5962–87609

Ordering Code: See Section 8

Logic Symbol



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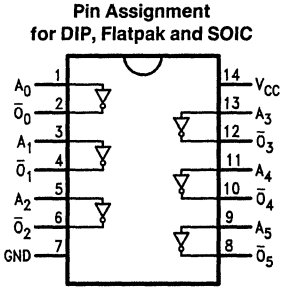
Connection Diagrams



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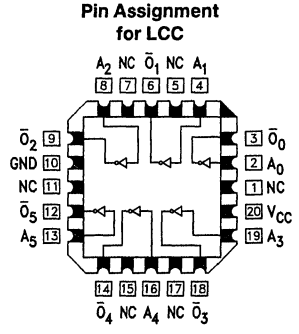


TL/F/9913–2

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	4.5	9.0	1.0	11.0	1.0	10.0	ns	2-3,4
		5.0	1.5	4.0	7.0	1.0	8.5	1.0	7.5		
t_{PHL}	Propagation Delay	3.3	1.5	4.5	8.5	1.0	10.0	1.0	9.5	ns	2-3,4
		5.0	1.5	3.5	6.5	1.0	7.5	1.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	6.0	8.5			1.0	9.0	ns	2-3,4
t_{PHL}	Propagation Delay	5.0	1.0	5.5	8.0			1.0	8.5	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC08 • 54ACT/74ACT08
Quad 2-Input AND Gate

General Description

The 'AC/'ACT08 contains four, 2-input AND gates.

The information for the ACT08 is preliminary information only.

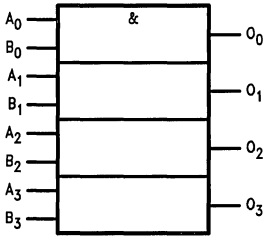
Features

- Outputs source/sink 24 mA
- 'ACT08 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'AC08: 5962-87615

Ordering Code: See Section 8

Logic Symbols

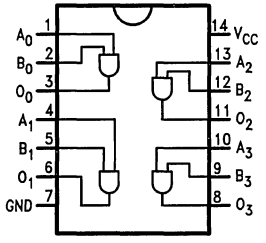
IEEE/IEC



TL/F/9914–1

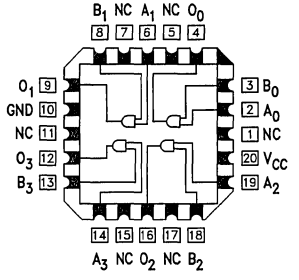
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9914–3

Pin Assignment for LCC



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Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms.

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	7.5	9.5	1.0	12.5	1.0	10.0	ns	2-3, 4
		5.0	1.5	5.5	7.5	1.0	9.0	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	11.5	1.0	9.0	ns	2-3, 4
		5.0	1.5	5.5	7.0	1.0	8.5	1.0	7.5		

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics: See Section 2 for waveforms.

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	6.5	9.0			1.0	10.0	ns	2-3, 4
t_{PHL}	Propagation Delay	5.0	1.0	6.5	9.0			1.0	10.0	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	20.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC10 • 54ACT/74ACT10
Triple 3-Input NAND Gate

General Description

The 'AC/'ACT10 contains three, 3-input NAND gates.

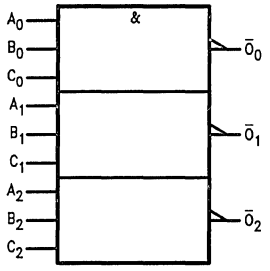
The information for the ACT10 is Preliminary Information only.

Features

- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
  — 'AC10: 5962-87610

Ordering Code: See Section 8

Logic Symbol



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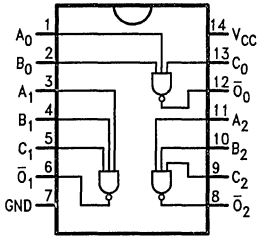
Connection Diagrams



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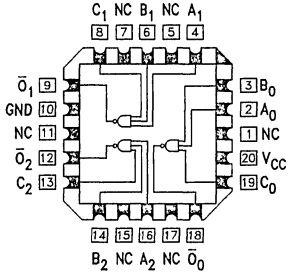

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Pin Names	Description
A_n, B_n, C_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.5	0.44		12 mA
		4.5		0.36	0.5	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	6.0	9.5	1.0	11.0	1.0	10.5	ns	2-3,4
		5.0	1.5	4.5	7.0	1.0	8.5	1.0	8.0		
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.5	1.0	10.0	1.0	10.0	ns	2-3,4
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	6.5	9.0			1.0	10.0	ns	2-3,4
t_{PHL}	Propagation Delay	5.0	1.0	6.5	9.0			1.0	9.5	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	25.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC11
Triple 3-Input AND Gate

General Description

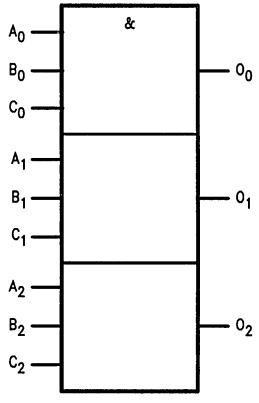
The 'AC11 contains three 3-input AND gates.

Features

- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
  — 'AC11: 5962-87611

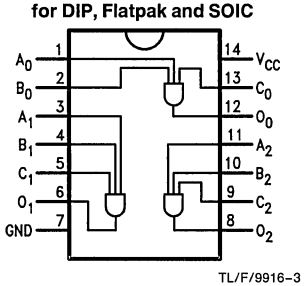
Ordering Code: See Section 8

Logic Symbol

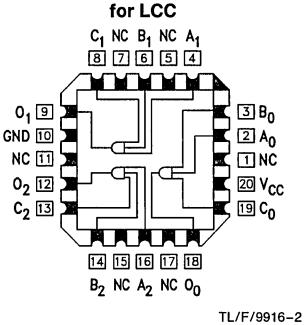


TL/F/9916–1

Connection Diagrams



TL/F/9916–3



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Pin Names	Description
A_n, B_n, C_n	Inputs
O_n	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46	V	I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.5	0.44	V	I_{OL} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	5.5	9.5	1.0	11.0	1.0	10.0	ns	2-3, 4
		5.0	1.5	4.0	8.0	1.0	8.5	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.5	5.5	8.5	1.0	10.5	1.0	9.5	ns	2-3, 4
		5.0	1.5	4.0	7.0	1.0	8.0	1.0	7.5		

*Voltage Range 3.3 is 3.3V ±0.3V

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	20.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC14
Hex Inverter with Schmitt Trigger Input

General Description

The 'AC14 contains six inverter gates each with a Schmitt trigger input. The 'AC14 contains six logic inverters which accept standard CMOS input signals and provide standard CMOS output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The 'AC14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

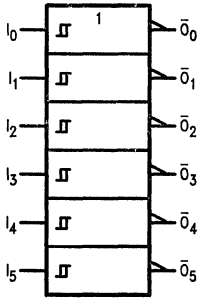
Features

- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
  — 'AC14: 5962-87624

Ordering Code: See Section 8

Logic Symbol

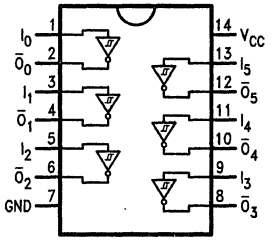
IEEE/IEC



TL/F/9917-1

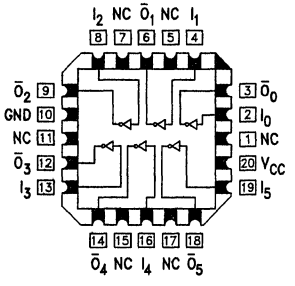
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9917-2

Pin Assignment for LCC



TL/F/9917-3

Function Table

Input	Output
A	$\overline{O}$
L	H
H	L

Pin Names	Description
I_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
V_{t+}	Maximum Positive Threshold	3.0		2.2	2.2	2.2	V	T_A = Worst Case
		4.5		3.2	3.2	3.2		
		5.5		3.9	3.9	3.9		
V_{t-}	Minimum Negative Threshold	3.0		0.5	0.5	0.5	V	T_A = Worst Case
		4.5		0.9	0.9	0.9		
		5.5		1.1	1.1	1.1		

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
$V_{h(max)}$	Maximum Hysteresis	3.0		1.2	1.2	1.2	V	T_A = Worst Case
		4.5		1.4	1.4	1.4		
		5.5		1.6	1.6	1.6		
$V_{h(min)}$	Minimum Hysteresis	3.0		0.3	0.3	0.3	V	T_A = Worst Case
		4.5		0.4	0.4	0.4		
		5.5		0.5	0.5	0.5		
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	9.5	13.5	1.0	16.0	1.5	15.0	ns	2-3,4
		5.0	1.5	7.0	10.0	1.0	12.0	1.5	11.0		
t_{PHL}	Propagation Delay	3.3	1.5	7.5	11.5	1.0	14.0	1.5	13.0	ns	2-3,4
		5.0	1.5	6.0	8.5	1.0	10.0	1.5	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	25.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC20
Dual 4-Input NAND Gate

General Description

The 'AC20 contains four 4-input NAND gates.

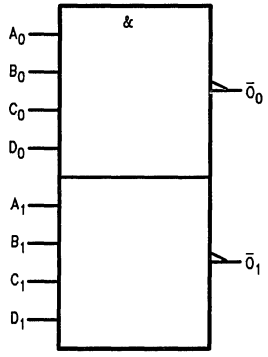
Features

- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
  — 'AC20: 5962-87613

Ordering Code: See Section 8

Logic Symbol

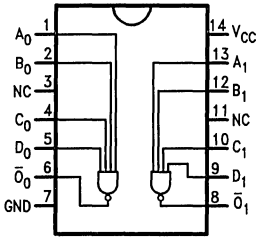
IEEE/IEC



TL/F/9918–1

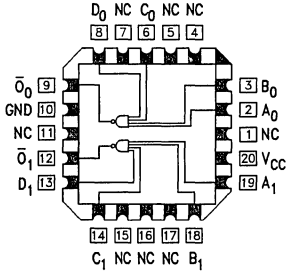
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9918–3

Pin Assignment for LCC



TL/F/9918–2

Pin Names	Description
A_m, B_n, C_n, D_n	Inputs
$\overline{O}_n$	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.5	0.44		12 mA
		4.5		0.36	0.5	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note : I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	2.0	6.0	8.5	1.0	11.0	1.5	10.0	ns	2-3,4
		5.0	1.5	5.0	7.0	1.0	8.5	1.0	8.0		
t_{PHL}	Propagation Delay	3.3	1.5	5.0	7.0	1.0	10.5	1.0	9.0	ns	2-3,4
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC32 • 54ACT/74ACT32
Quad 2-Input OR Gate

General Description

The 'AC/'ACT32 contains four, 2-input OR gates.

The information for the ACT32 is Preliminary information only.

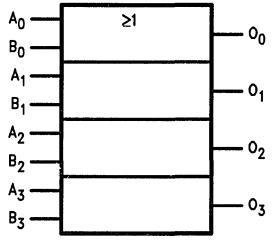
Features

- Outputs source/sink 24 mA
- 'ACT32 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'AC32: 5962-87614

Ordering Code: See Section 8

Logic Symbol

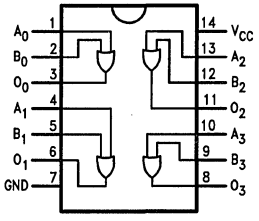
IEEE/IEC



TL/F/9919–1

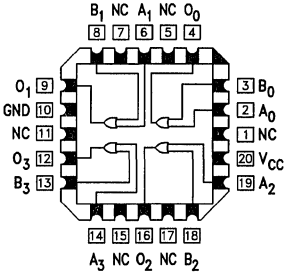
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9919–3

Pin Assignment for LCC



TL/F/9919–2

Pin Names	Description
A_n, B_n	Inputs
O_n	Outputs

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.5	7.0	9.0	1.0	12.0	1.5	10.0	ns	2-3, 4
		5.0	1.5	5.5	7.5	1.0	9.0	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	11.5	1.0	9.0	ns	2-3, 4
		5.0	1.5	5.0	7.0	1.0	8.5	1.0	7.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	6.5	9.0			1.0	10.0	ns	2-3, 4
t_{PHL}	Propagation Delay	5.0	1.0	6.5	9.0			1.0	10.0	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.3V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	20.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC74 • 54ACT/74ACT74
Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

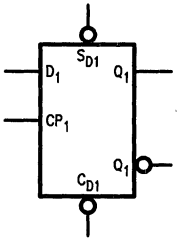
Asynchronous Inputs:
LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Output source/sink 24 mA
- 'ACT74 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC74: 5962-88520
  - — 'ACT74: 5962-87525

Ordering Code: See Section 8

Logic Symbols



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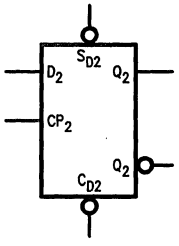
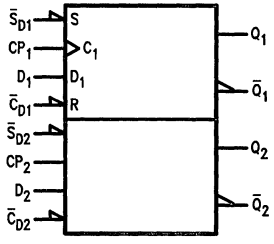


TL/F/9920–2

IEEE/IEC

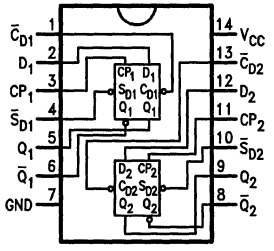


TL/F/9920–3

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

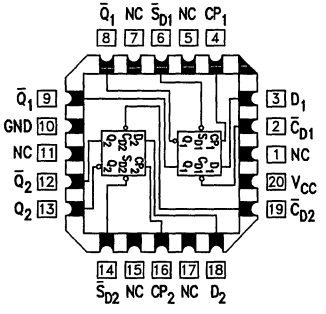
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9920–4

Pin Assignment for LCC



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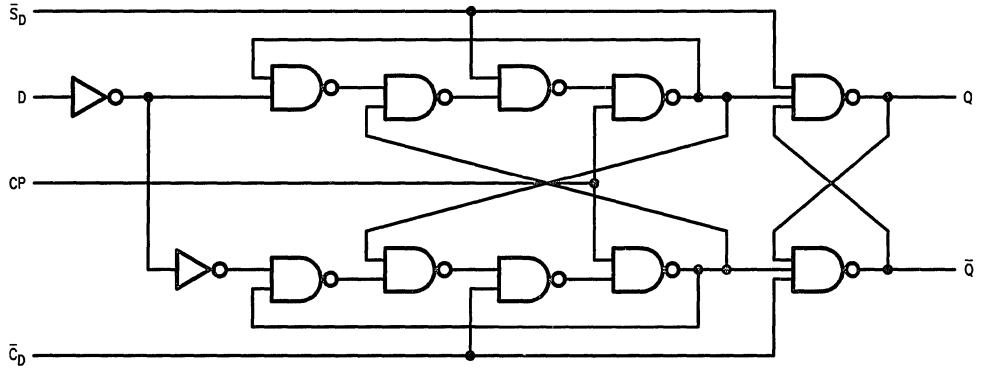
Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous Q($\overline{Q}$) before LOW-to-HIGH Transition of Clock

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74AC $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74ACT $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	100	125		70		95		MHz	
		5.0	140	160		95		125			
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	3.5	8.0	12.0	1.0	13.0	2.5	13.0	ns	2-3, 4
		5.0	2.5	6.0	9.0	1.0	9.5	2.0	10.0		
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3	4.0	10.5	12.0	1.0	14.0	3.5	13.5	ns	2-3, 4
		5.0	3.0	8.0	9.5	1.0	10.5	2.5	10.5		
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	4.5	8.0	13.5	1.0	17.5	4.0	16.0	ns	2-3, 4
		5.0	3.5	6.0	10.0	1.0	12.0	3.0	10.5		
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3	3.5	8.0	14.0	1.0	13.5	3.5	14.5	ns	2-3, 4
		5.0	2.5	6.0	10.0	1.0	10.0	2.5	10.5		

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP_n	3.3	1.5	4.0	5.0	4.5	ns	2-7
		5.0	1.0	3.0	4.0	3.0		
t_h	Hold Time, HIGH or LOW D_n to CP_n	3.3	−2.0	0.5	0.5	0.5	ns	2-7
		5.0	−1.5	0.5	0.5	0.5		
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3	3.0	5.5	8.0	7.0	ns	2-3
		5.0	2.5	4.5	5.5	5.0		
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3	−2.5	0	0.5	0	ns	2-3, 7
		5.0	−2.0	0	0.5	0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		85		125		MHz	
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	5.5	9.5	1.0	11.5	2.5	10.5	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	3.0	6.0	10.0	1.0	12.5	3.0	11.5	ns	2-3, 4
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	4.0	7.5	11.0	1.0	14.0	4.0	13.0.	ns	2-3, 4
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	3.5	6.0	10.0	1.0	12.0	3.0	11.5	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP_n	5.0	1.0	3.0	4.0	3.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP_n	5.0	−0.5	1.0	1.0	1.0	ns	2-7
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	7.0	6.0	ns	2-3
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	0	0.5	0	ns	2-3, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	35.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC86
Quad 2-Input Exclusive-OR Gate

General Description

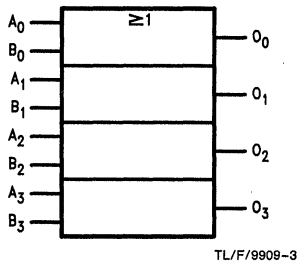
The 'AC86 contains four, 2-input exclusive-OR gates.

Features

- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
  — 'AC86: 5962-89550

Ordering Code: See Section 8

Logic Symbol



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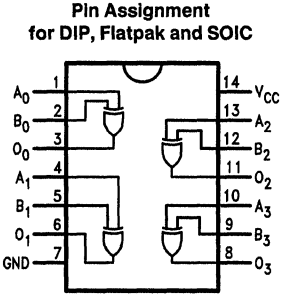
Connection Diagrams



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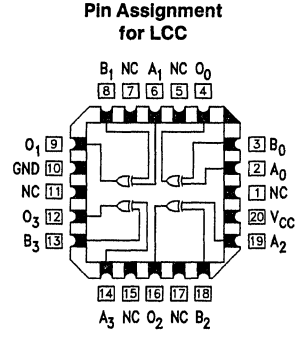

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Pin Names	Description
A_0–A_3	Inputs
B_0–B_3	Inputs
O_0–O_3	Outputs

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = 0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25°C	74AC	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = 25°C$	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE®							V_I (OE) = V_{IL}, V_{IH} $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80	40	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay Inputs to Outputs	3.3	2.0	6.0	11.5	1.0	14.0	1.5	12.5	ns	2-3, 4
		5.0	1.5	4.5	8.5	1.0	10.0	1.0	9.5		
t_{PLH}	Propagation Delay Inputs to Outputs	3.3	2.0	6.5	11.5	1.0	14.0	1.5	12.5	ns	2-3, 4
		5.0	1.5	4.5	8.5	1.0	10.0	1.0	9.0		

*Voltage Range 3.3V is 3.3V ±0.3V
Voltage Range 5.0V is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	35	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC109 • 54ACT/74ACT109
Dual $\overline{JK}$ Positive Edge-Triggered Flip-Flop

General Description

The 'AC/'ACT109 consists of two high-speed completely independent transition clocked $\overline{JK}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $\overline{JK}$ design allows operation as a D flip-flop (refer to 'AC/'ACT74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level

LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level

Clear and Set are independent of clock

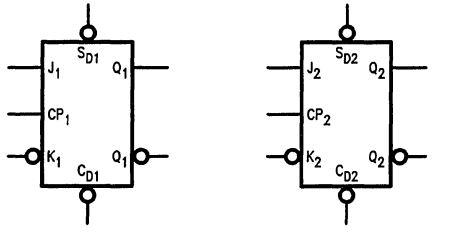
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

- Outputs source/sink 24 mA
- 'ACT109 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC109: 5962-89551
  - — 'ACT109: 5962-88534

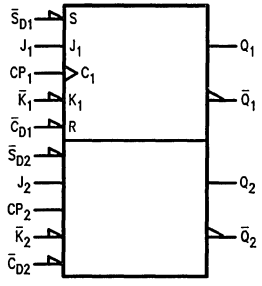
Ordering Code: See Section 8

Logic Symbols



TL/F/9923–1 TL/F/9923–2

IEEE/IEC

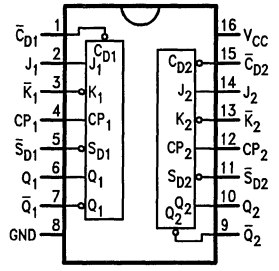


TL/F/9923–7

Pin Names	Description
$J_1, J_2, \overline{K}_1, \overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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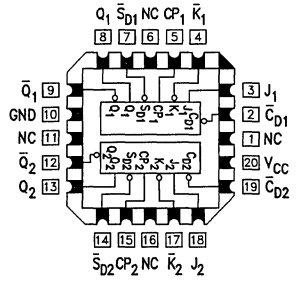
Pin Assignment for LCC



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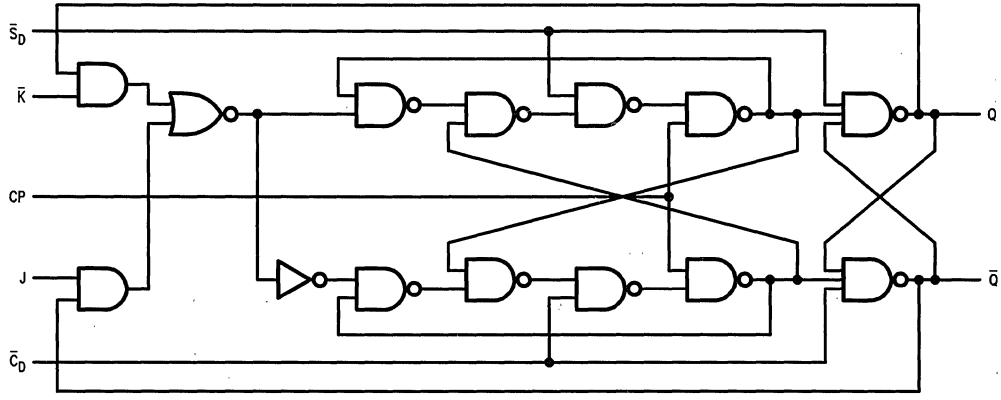
Truth Table (each half)

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	L	L	L	H
H	H	⌐	H	L	Toggle	
H	H	⌐	L	H	Q_0	$\overline{Q}_0$
H	H	⌐	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
⌐ = LOW-to-HIGH Transition
X = Immaterial
$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW-to-HIGH Transition of Clock

Logic Diagram (one half shown)



TL/F/9923–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = −55°C to +125°C	54AC T_A = −40°C to +85°C	74AC Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		
		5.5		4.86	4.7		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.5	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5		
		5.5		0.36	0.5		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	125 150	150 175		65 95		100 125		MHz	
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	4.0 2.5	8.0 6.0	13.5 10.0	1.0 1.0	17.5 12.0	3.5 2.0	16.0 10.5	ns	2-3, 4
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	3.0 2.0	8.0 6.0	14.0 10.0	1.0 1.0	13.5 10.0	3.0 1.5	14.5 10.5	ns	2-3, 4
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	3.0 2.5	8.0 6.0	12.0 9.0	1.0 1.0	13.0 9.5	2.5 2.0	13.0 10.0	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	3.0 2.0	10.0 7.5	12.0 9.5	1.0 1.0	14.0 10.5	3.0 2.0	13.5 10.5	ns	2-3, 4

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements : See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	3.5 2.0	6.5 4.5	8.0 5.5	7.5 5.0	ns	2-7
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	−1.5 −0.5	0 0.5	0 0.5	0 0.5	ns	2-7
t_w	Pulse Width $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3 5.0	2.0 2.0	4.0 3.5	8.0 5.5	4.5 3.5	ns	2-3
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	3.3 5.0	−2.5 −1.5	0 0	0.5 0.5	0 0	ns	2-3, 7

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		85		125		MHz	
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	4.0	7.0	11.0	1.0	14.0	3.5	13.0	ns	2-3, 4
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	3.0	6.0	10.0	1.0	12.0	2.5	11.5	ns	2-3, 4
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	5.5	9.5	1.0	11.5	2.0	10.5	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	6.0	10.0	1.0	12.5	2.0	11.5	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0.5	2.0	2.5	2.5	ns	2-7
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0	2.0	2.0	2.0	ns	2-7
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	3.0	5.0	7.0	6.0	ns	2-3
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP_n	5.0	−2.5	0	0.5	0	ns	2-3, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	35.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC125 • 54ACT/74ACT125
Quad Buffer with TRI-STATE® Outputs

General Description

The 'AC/'ACT125 contains four independent non-inverting buffers with TRI-STATE outputs.

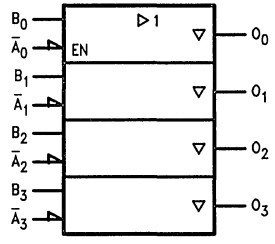
Features

- Outputs source/sink 24 mA
- 'ACT125 has TTL-compatible outputs

Ordering Code: See Section 8

Logic Symbol

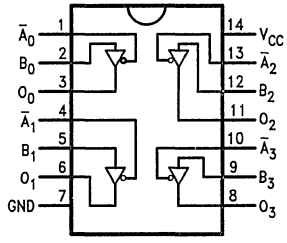
IEEE/IEC



TL/F/10692–1

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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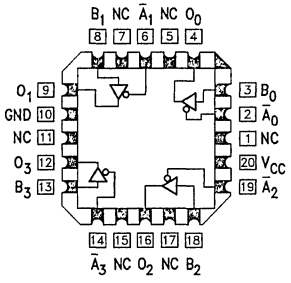
Pin Assignment for LCC and PCC



TL/F/10692–3

Pin Names	Description
$\overline{A}_n$, B_n	Inputs
O_n	Outputs

Function Table

Inputs		Output
A_n	B_n	O_n
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
X = Immaterial

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note : I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V‡
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

‡May be measured per the JEDEC Alternate Method.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3	1.0	6.5	9.0			1.0	10.0	ns	2–3, 4
		5.0	1.0	5.5	7.0			1.0	7.5		
t_{PHL}	Propagation Delay Data to Output	3.3	1.0	6.5	9.0			1.0	10.0	ns	2–3, 4
		5.0	1.0	5.0	7.0			1.0	7.5		
t_{PZH}	Output Enable Time	3.3	1.0	6.0	10.5			1.0	11.0	ns	2–5
		5.0	1.0	5.0	7.0			1.0	8.0		
t_{PZL}	Output Enable Time	3.3	1.0	7.5	10.0			1.0	11.0	ns	2–6
		5.0	1.0	5.5	8.0			1.0	8.5		
t_{PHZ}	Output Disable Time	3.3	1.0	7.5	10.0			1.0	10.5	ns	2–5
		5.0	1.0	6.5	9.0			1.0	9.5		
t_{PLZ}	Output Disable Time	3.3	1.0	7.5	10.5			1.0	11.5	ns	2–6
		5.0	1.0	6.5	9.0			1.0	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.0	6.5	9.0			1.0	10.0	ns	2–3, 4
t_{PHL}	Propagation Delay Data to Output	5.0	1.0	7.0	9.0			1.0	10.0	ns	2–3, 4
t_{PZH}	Output Enable Time	5.0	1.0	6.0	8.5			1.0	9.5	ns	2–5
t_{PZL}	Output Enable Time	5.0	1.0	7.0	9.5			1.0	10.5	ns	2–6
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	9.5			1.0	10.5	ns	2–5
t_{PLZ}	Output Disable Time	5.0	1.0	7.5	10.0			1.0	10.5	ns	2–6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC138 • 54ACT/74ACT138
1-of-8 Decoder/Demultiplexer

General Description

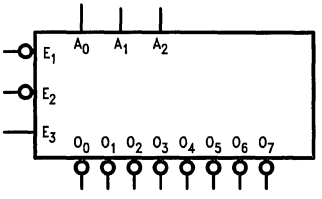
The 'AC/'ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'AC/'ACT138 devices or a 1-of-32 decoder using four 'AC/'ACT138 devices and one inverter.

Features

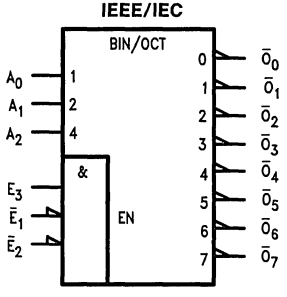
- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- 'ACT138 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC138: 5962-87622
  - — 'ACT138: 5962-87554

Ordering Code: See Section 8

Logic Symbol



TL/F/9925–1

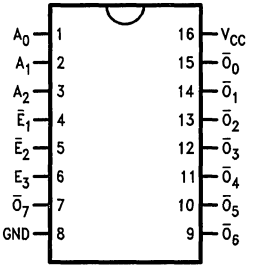


TL/F/9925–7

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

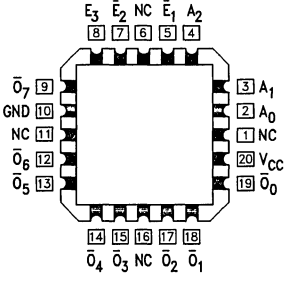
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9925–2

Pin Assignment for LCC



TL/F/9925–3

Functional Description

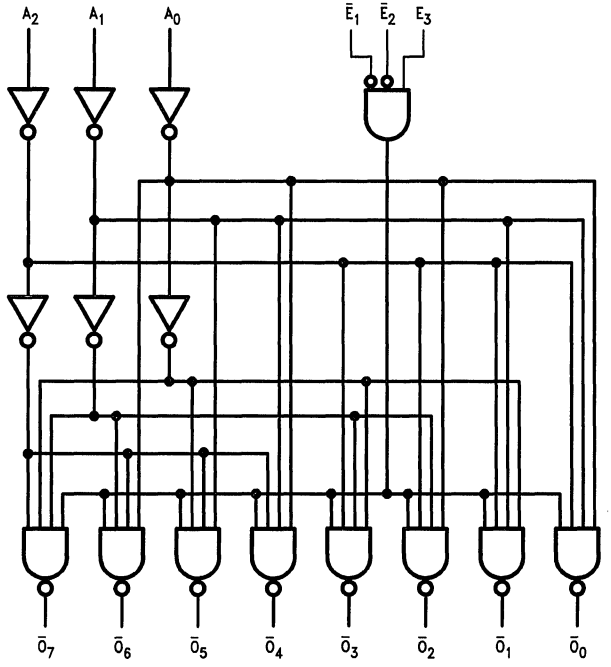
The 'AC/'ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The 'AC/'ACT138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'AC/'ACT138 devices and one inverter (see *Figure 1*). The 'AC/'ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

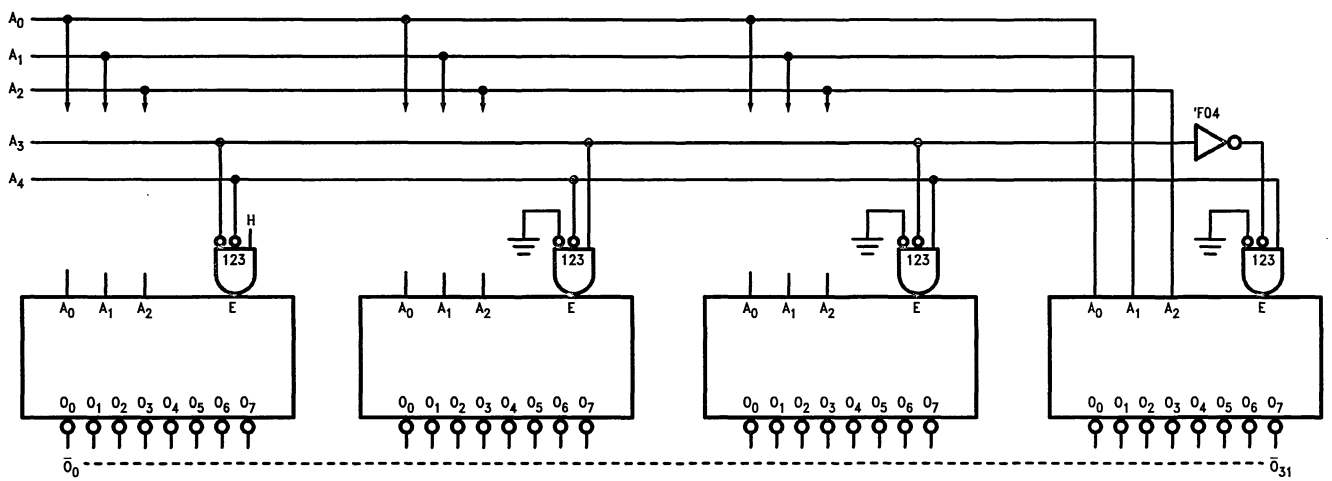
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9925–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



TL/F/9925–5

FIGURE 1. Expansion to 1-of-32 Decoding

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = −55°C to +125°C	54AC T_A = −40°C to +85°C	74AC	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.5	8.5	13.0	1.0	16.0	1.5	15.0	ns	2-3, 4
		5.0	1.5	6.5	9.5	1.0	12.0	1.5	10.5		
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.5	8.0	12.5	1.0	15.0	1.5	14.0	ns	2-3, 4
		5.0	1.5	6.0	9.0	1.0	11.5	1.5	10.5		
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3	1.5	11.0	15.0	1.0	16.5	1.5	16.0	ns	2-3, 4
		5.0	1.5	8.0	11.0	1.0	13.0	1.5	12.0		
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3	1.5	9.5	13.5	1.0	15.5	1.5	15.0	ns	2-3, 4
		5.0	1.5	7.0	9.5	1.0	12.0	1.5	10.5		
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	3.3	1.5	11.0	15.5	1.0	17.0	1.5	16.5	ns	2-3, 4
		5.0	1.5	8.0	11.0	1.0	13.5	1.5	12.5		
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	3.3	1.5	8.5	13.0	1.0	15.0	1.5	14.0	ns	2-3, 4
		5.0	1.5	6.0	8.0	1.0	11.0	1.0	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.5	7.0	10.5	1.0	12.5	1.5	11.5	ns	2-3, 4
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.5	6.5	10.5	1.0	12.5	1.5	11.5	ns	2-3, 4
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	2.5	8.0	11.5	1.0	13.5	2.0	12.5	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	2.0	7.5	11.5	1.0	12.5	2.0	12.5	ns	2-3, 4
t_{PLH}	Propagation Delay E_3 to $\overline{O}n$	5.0	2.5	8.0	12.0	1.0	14.0	2.0	13.0	ns	2-3, 4
t_{PHL}	Propagation Delay E_3 to $\overline{O}n$	5.0	2.0	6.5	10.5	1.0	12.0	1.5	11.5	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC139 • 54ACT/74ACT139
Dual 1-of-4 Decoder/Demultiplexer

General Description

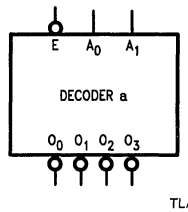
The 'AC/'ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'AC/'ACT139 can be used as a function generator providing all four minterms of two variables.

Features

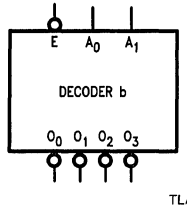
- Multifunction capability
- Two completely independent 1-of-4 decoders
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- 'ACT139 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - —'AC139: 5962-87623
  - —'ACT139: 5962-87553

Ordering Code: See Section 8

Logic Symbols



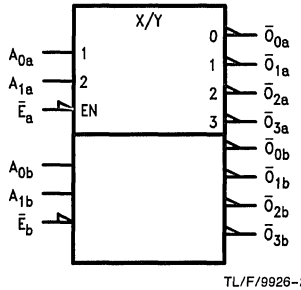
TL/F/9926–8



TL/F/9926–1

Pin Names	Description
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs
$\overline{O}_0$–$\overline{O}_3$	Outputs

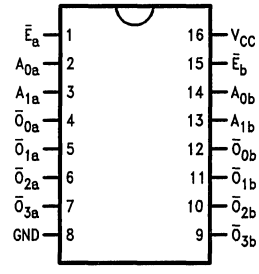
IEEE/IEC



TL/F/9926–2

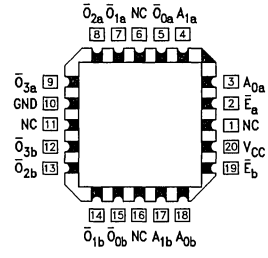
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9926–3

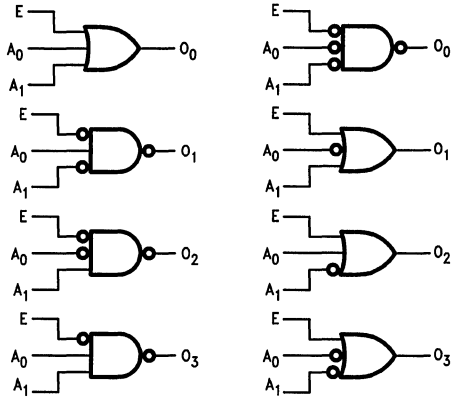
Pin Assignment for LCC



TL/F/9926–4

Functional Description

The 'AC/'ACT139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0–A_1) and provides four mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_3$). Each decoder has an active-LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'AC/'ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in *Figure a*, and thereby reducing the number of packages required in a logic network.



TL/F/9926–6

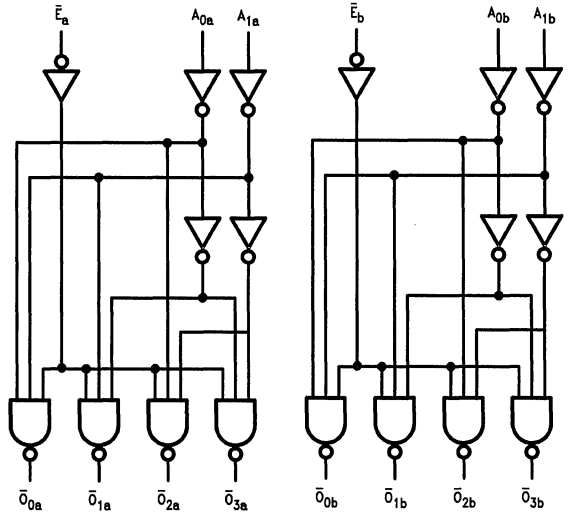
FIGURE a. Gate Functions (Each Half)

Truth Table

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} + 0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} + 0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'AC Devices
V_{IN} from 30% to 70% of V_{CC}
V_{CC} @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'ACT Devices
V_{IN} from 0.8V to 2.0V
V_{CC} @ 4.5V, 5.5V 125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	$I_{OUT} = -50\ \mu A$
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*$V_{IN} = V_{IL}$ or V_{IH}
		3.0		2.56	2.4	2.46		-12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} -24 mA
		5.5		4.86	4.7	4.76		-24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*$V_{IN} = V_{IL}$ or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3	4.0	8.0	11.5	1.0	14.5	3.5	13.0	ns	2-3, 4
		5.0	3.0	6.5	8.5	1.0	11.0	2.5	9.5		
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3	3.0	7.0	10.0	1.0	12.5	2.5	11.0	ns	2-3, 4
		5.0	2.5	5.5	7.5	1.0	10.0	2.0	8.5		
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.3	4.5	9.5	12.0	1.0	14.5	3.5	13.0	ns	2-3, 4
		5.0	3.5	7.0	8.5	1.0	11.0	3.0	10.0		
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.3	4.0	8.0	10.0	1.0	12.5	3.0	11.0	ns	2-3, 4
		5.0	2.5	6.0	7.5	1.0	10.0	2.5	8.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.5	6.0	8.5	1.0	12.0	1.5	9.5	ns	2-3, 4
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.5	6.0	9.5	1.0	11.0	1.5	10.5	ns	2-3, 4
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	5.0	2.5	7.0	10.0	1.0	12.5	2.0	11.0	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	5.0	2.0	7.0	9.5	1.0	12.0	1.5	10.5	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC151 • 54ACT/74ACT151
8-Input Multiplexer

General Description

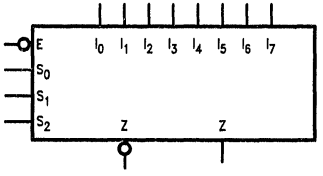
The 'AC/'ACT151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The 'AC/'ACT151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

- Outputs source/sink 24 mA
- 'ACT151 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - —'AC151: 5962-87691
  - —'ACT151: 5962-88756

Ordering Code: See Section 8

Logic Symbol



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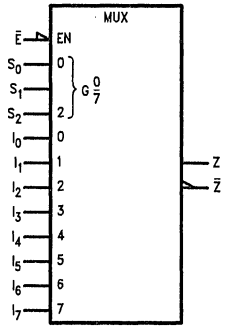
IEEE/IEC

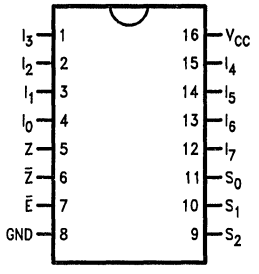


TL/F/9927–6

Pin Names	Description
I_0–I_7	Data Inputs
S_0–S_2	Select Inputs
$\bar{E}$	Enable Input
Z	Data Output
$\bar{Z}$	Inverted Data Output

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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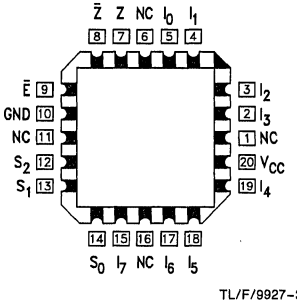
Pin Assignment for LCC



TL/F/9927–3

Truth Table

Inputs				Outputs	
$\bar{E}$	S_2	S_1	S_0	$\bar{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\bar{I}_0$	I_0
L	L	L	H	$\bar{I}_1$	I_1
L	L	H	L	$\bar{I}_2$	I_2
L	L	H	H	$\bar{I}_3$	I_3
L	H	L	L	$\bar{I}_4$	I_4
L	H	L	H	$\bar{I}_5$	I_5
L	H	H	L	$\bar{I}_6$	I_6
L	H	H	H	$\bar{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

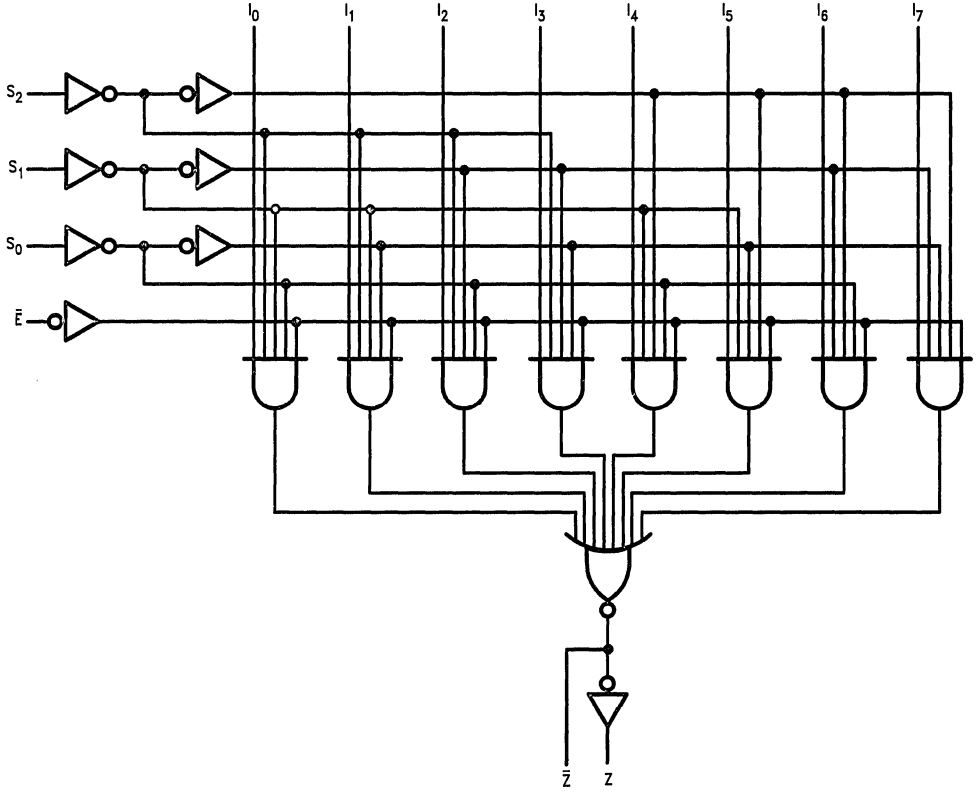
Functional Description

The 'AC/'ACT151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet S_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

The 'AC/'ACT151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the 'AC/'ACT151 can provide any logic function of four variables and its complement.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3 5.0	3.0 2.5	11.5 8.5	18.0 13.0	1.0 1.0	22.0 15.5	3.0 2.0	20.0 15.0	ns	2-3,4
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3 5.0	2.5 2.0	12.0 8.5	18.0 13.0	1.0 1.0	22.0 15.5	2.5 1.5	20.0 15.0	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3 5.0	2.5 2.0	8.0 6.0	13.0 10.0	1.0 1.0	15.5 12.0	2.0 1.5	14.0 11.0	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3 5.0	1.5 1.5	8.5 6.5	13.0 10.0	1.0 1.0	15.5 12.0	1.5 1.5	14.0 11.0	ns	2-3,4
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3 5.0	2.5 1.5	9.5 7.0	14.0 10.5	1.0 1.0	16.0 12.0	2.0 1.5	15.5 11.0	ns	2-3,4
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3 5.0	2.5 1.5	9.5 7.0	15.0 11.0	1.0 1.0	18.0 13.0	2.0 1.5	16.0 12.0	ns	2-3,4

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z	5.0	3.5	12.5	15.5	1.0	19.5	3.0	17.0	ns	2-3,4
t_{PHL}	Propagation Delay S_n to Z	5.0	3.5	12.5	15.5	1.0	20.0	3.0	16.5	ns	2-3,4
t_{PLH}	Propagation Delay S_n to $\overline{Z}$	5.0	3.5	12.5	15.0	1.0	19.5	3.0	16.5	ns	2-3,4
t_{PHL}	Propagation Delay S_n to $\overline{Z}$	5.0	4.0	12.5	16.5	1.0	20.0	3.5	18.5	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{E}$ to Z	5.0	2.5	6.0	9.5	1.0	12.0	2.5	10.0	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{E}$ to Z	5.0	2.5	6.0	9.0	1.0	12.5	2.5	10.0	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}$	5.0	2.5	6.0	8.5	1.0	12.0	2.5	9.5	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$	5.0	3.0	6.5	10.0	1.0	12.5	2.5	10.5	ns	2-3,4
t_{PLH}	Propagation Delay I_n to Z	5.0	3.5	7.5	11.5	1.0	15.0	3.0	12.5	ns	2-3,4
t_{PHL}	Propagation Delay I_n to Z	5.0	3.5	8.0	12.0	1.0	16.0	3.0	13.5	ns	2-3,4
t_{PLH}	Propagation Delay I_n to $\overline{Z}$	5.0	3.5	8.0	12.0	1.0	15.0	3.0	13.0	ns	2-3,4
t_{PHL}	Propagation Delay I_n to $\overline{Z}$	5.0	4.0	8.0	12.5	1.0	16.0	3.0	14.0	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	70.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC153 • 54ACT/74ACT153
Dual 4-Input Multiplexer

General Description

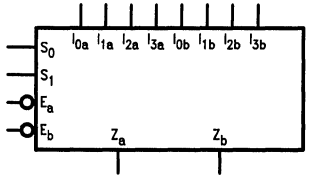
The 'AC/'ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'AC/'ACT153 can act as a function generator and generate any two functions of three variables.

Features

- Outputs source/sink 24 mA
- 'ACT153 has TTL-compatible inputs
- Standard Military Drawings (SMD)
  - — 'AC153: 5962-87625
  - — 'ACT153: 5962-87698

Ordering Code: See Section 8

Logic Symbols



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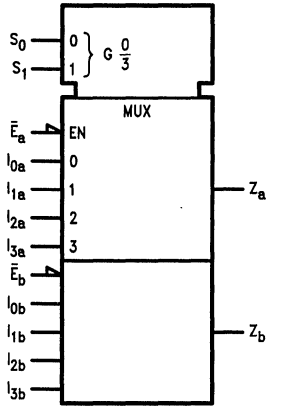
IEEE/IEC



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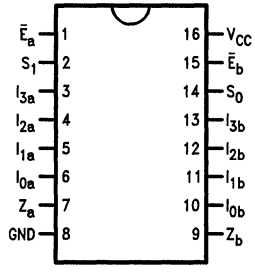
Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{E}_a$	Side A Enable Input
$\overline{E}_b$	Side B Enable Input
Z_a	Side A Output
Z_b	Side B Output

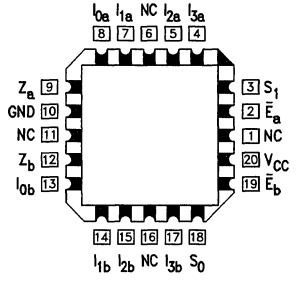
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9928–3

Pin Assignment for LCC



TL/F/9928–4

Functional Description

The 'AC/'ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs indepedently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs Z_a, Z_b) are forced LOW. The 'AC/'ACT153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet S_0 + I_{3a} \bullet S_1 \bullet S_0)$$

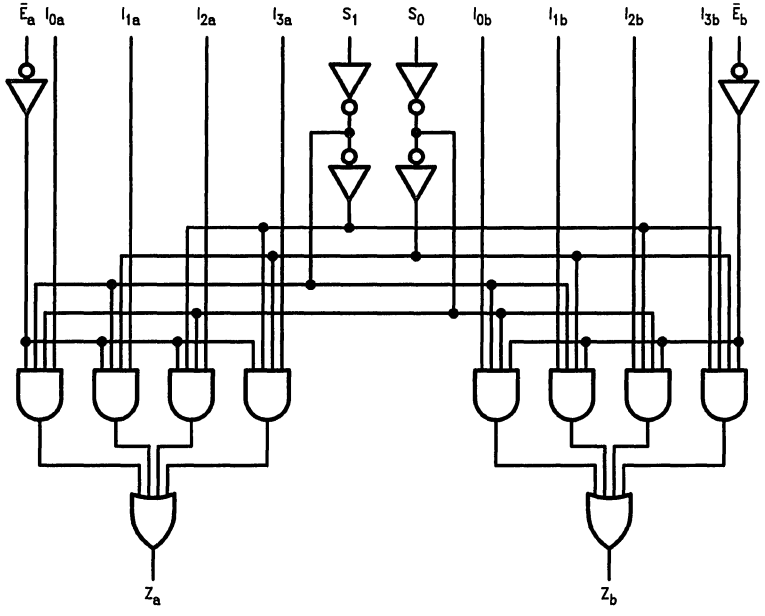
$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet S_0 + I_{3b} \bullet S_1 \bullet S_0)$$

Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9928–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3	2.5	9.5	15.0	1.0	19.5	2.5	17.5	ns	2-3,4
		5.0	2.0	6.5	11.0	1.0	14.0	2.0	12.5		
t_{PHL}	Propagation Delay S_n to Z_n	3.3	3.0	8.5	14.5	1.0	18.0	2.5	16.5	ns	2-3,4
		5.0	2.5	6.5	11.0	1.0	13.5	2.0	12.0		
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	3.3	2.5	8.0	13.5	1.0	16.5	2.0	16.0	ns	2-3,4
		5.0	1.5	5.5	9.5	1.0	12.5	1.5	11.0		
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	3.3	2.5	7.0	11.0	1.0	14.0	2.0	12.5	ns	2-3,4
		5.0	2.0	5.0	8.0	1.0	10.0	1.5	9.0		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	2.5	7.5	12.5	1.0	16.0	2.0	14.5	ns	2-3,4
		5.0	1.5	5.5	9.0	1.0	11.5	1.5	10.5		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.5	7.0	11.5	1.0	14.5	1.5	13.0	ns	2-3,4
		5.0	1.5	5.0	8.5	1.0	10.5	1.5	10.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	3.0	7.0	11.5	1.0	15.0	2.0	13.5	ns	2-3,4
t_{PHL}	Propagation Delay S_n to Z_n	5.0	3.0	7.0	11.5	1.0	14.5	2.5	13.5	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	2.0	6.5	10.5	1.0	13.5	2.0	12.5	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	3.0	6.0	9.5	1.0	11.5	2.5	11.0	ns	2-3,4
t_{PLH}	Propagation Delay I_n to Z_n	5.0	2.5	5.5	9.5	1.0	12.5	2.0	11.0	ns	2-3,4
t_{PHL}	Propagation Delay I_n to Z_n	5.0	2.0	5.5	9.5	1.0	12.0	2.0	11.0	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	65.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC157 • 54ACT/74ACT157
Quad 2-Input Multiplexer

General Description

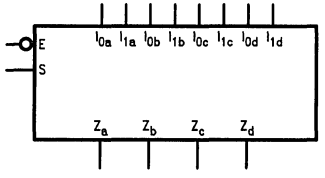
The 'AC/'ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The 'AC/'ACT157 can also be used as a function generator.

Features

- Outputs source/sink 24 mA
- 'ACT157 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC157: 5962-89539
  - — 'ACT157: 5962-89688

Ordering Code: See Section 8

Logic Symbols



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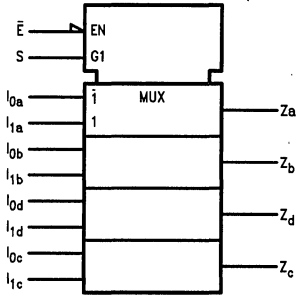
IEEE/IEC

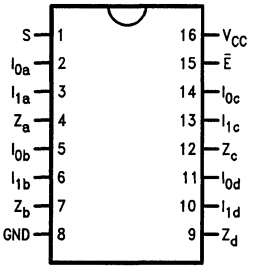


TL/F/9929–2

Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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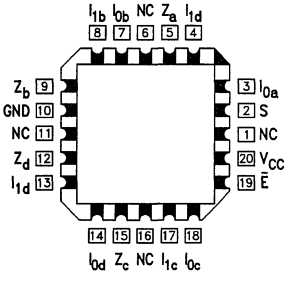
Pin Assignment for LCC



TL/F/9929–4

Functional Description

The 'AC/'ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'AC/'ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

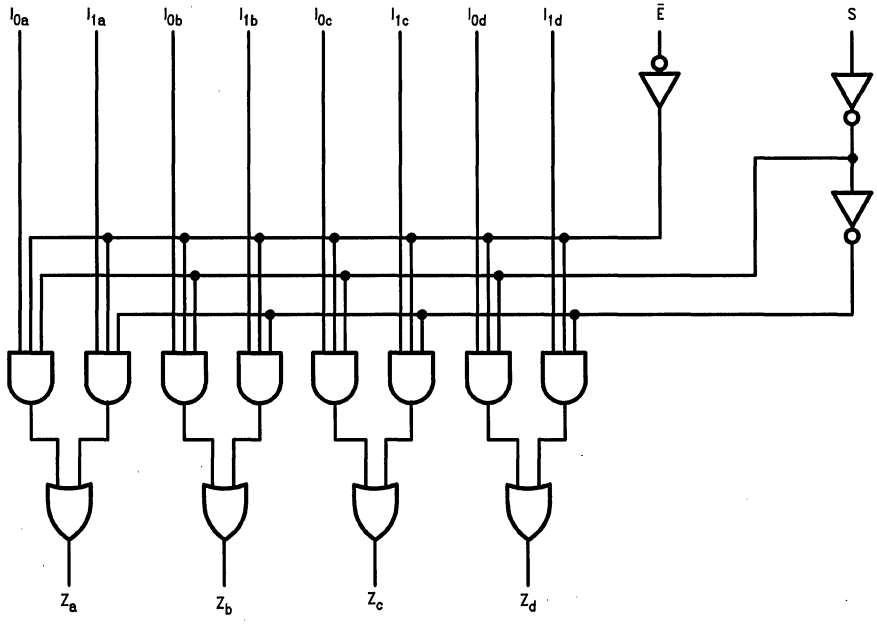
A common use of the 'AC/ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/'ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/9929–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms.

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	3.3	1.5	7.0	11.5	1.0	16.0	1.5	13.0	ns	2-3, 4
		5.0	1.5	5.5	9.0	1.0	12.0	1.5	10.0		
t_{PHL}	Propagation Delay S to Z_n	3.3	1.5	6.5	11.0	1.0	14.0	1.5	12.0	ns	2-3, 4
		5.0	1.5	5.0	8.5	1.0	11.5	1.0	9.5		
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	3.3	1.5	7.0	11.5	1.0	16.0	1.5	13.0	ns	2-3, 4
		5.0	1.5	5.5	9.0	1.0	12.0	1.5	10.0		
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	3.3	1.5	6.5	11.0	1.0	14.0	1.5	12.0	ns	2-3, 4
		5.0	1.5	5.5	9.0	1.0	11.5	1.0	9.5		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.5	1.0	11.0	1.0	9.0	ns	2-3, 4
		5.0	1.5	4.0	6.5	1.0	9.0	1.0	7.0		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.0	1.0	11.0	1.0	9.0	ns	2-3, 4
		5.0	1.5	4.0	6.5	1.0	9.0	1.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms.

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	5.0	2.0	5.5	9.0	1.0	11.5	1.5	10.0	ns	2-3, 4
t_{PHL}	Propagation Delay S to Z_n	5.0	2.0	5.5	9.5	1.0	11.5	2.0	10.5	ns	2-3, 4
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	5.0	1.5	6.0	10.0	1.0	12.0	1.5	11.5	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	5.0	1.5	5.0	8.5	1.0	10.0	1.0	9.0	ns	2-3, 4
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.5	4.0	7.0	1.0	8.5	1.0	8.5	ns	2-3, 4
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.5	4.5	7.5	1.0	9.0	1.0	8.5	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC158 • 54ACT/74ACT158
Quad 2-Input Multiplexer

General Description

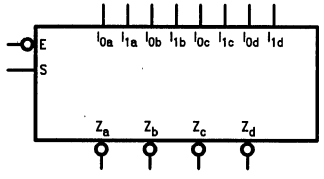
The 'AC/'ACT158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'AC/'ACT158 can also be used as a function generator.

Features

- Outputs source/sink 24 mA
- 'ACT158 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC158: 5962-89729
  - — 'ACT158: 5962-88755

Ordering Code: See Section 8

Logic Symbols



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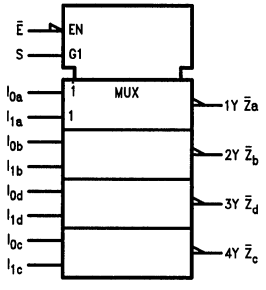
IEE/IEC



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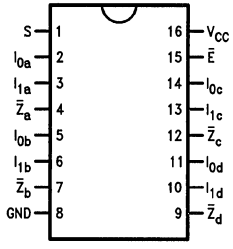
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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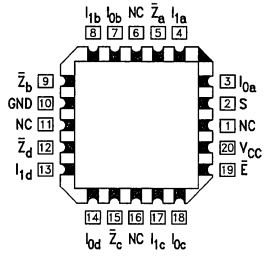
Pin Assignment for LCC



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Pin Names	Description
I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
$\overline{Z}_a$–$\overline{Z}_d$	Inverted Outputs

Functional Description

The 'AC/'ACT158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The 'AC/'ACT158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

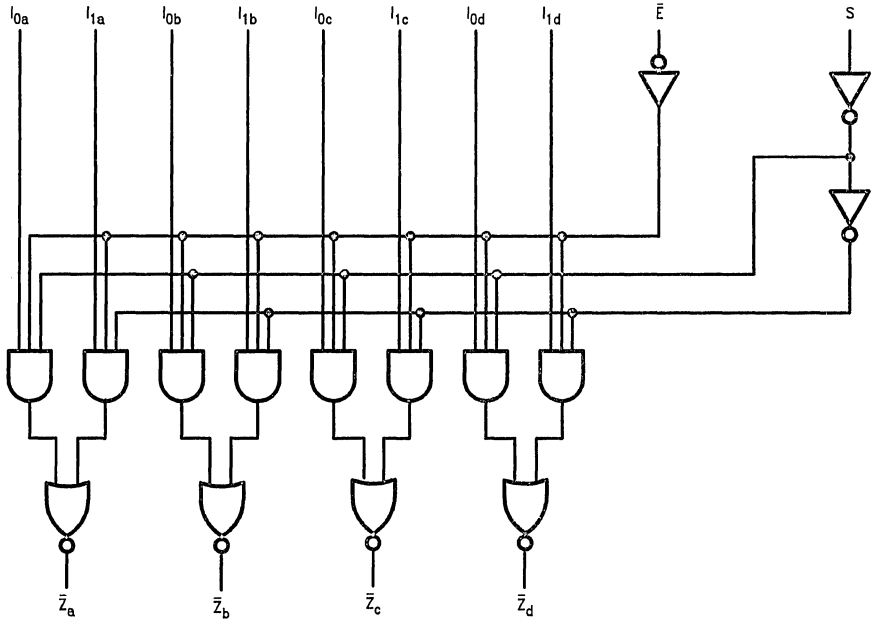
A common use of the 'AC/'ACT158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/'ACT158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms.

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3	1.5	7.0	11.5	1.0	14.0	1.5	12.5	ns	2-3, 4
		5.0	1.5	5.5	9.0	1.0	11.0	1.0	9.5		
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3	1.5	7.0	11.5	1.0	14.0	1.5	12.5	ns	2-3, 4
		5.0	1.5	5.5	9.0	1.0	11.0	1.5	10.0		
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	3.3	1.5	7.5	12.0	1.0	15.0	1.5	13.0	ns	2-3, 4
		5.0	1.5	6.0	9.5	1.0	12.0	1.5	10.5		
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	3.3	1.5	7.0	11.0	1.0	14.0	1.5	12.0	ns	2-3, 4
		5.0	1.5	5.5	8.5	1.0	10.0	1.0	9.5		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3	1.5	5.5	9.0	1.0	11.0	1.5	10.0	ns	2-3, 4
		5.0	1.5	4.0	7.0	1.0	8.5	1.0	7.5		
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3	1.5	5.0	8.0	1.0	10.0	1.0	8.5	ns	2-3, 4
		5.0	1.5	4.0	6.5	1.0	7.5	1.0	6.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms.

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	2.5	6.0	9.5	1.0	12.0	2.0	11.0	ns	2-3, 4
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.5	5.5	9.0	1.0	11.5	1.5	10.0	ns	2-3, 4
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	5.0	1.5	5.5	9.5	1.0	11.0	1.5	10.5	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	5.0	1.5	5.5	9.5	1.0	11.0	1.5	10.5	ns	2-3, 4
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.5	4.5	8.0	1.0	9.5	1.0	8.5	ns	2-3, 4
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.5	4.0	6.5	1.0	8.0	1.0	7.5	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC161 • 54ACT/74ACT161
Synchronous Presettable Binary Counter

General Description

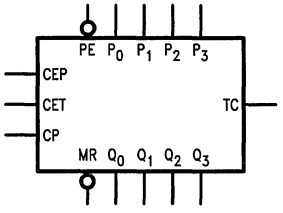
The 'AC/'ACT161 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW.

Features

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT161 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'AC161: 5962-89561

Ordering Code: See Section 8

Logic Symbols



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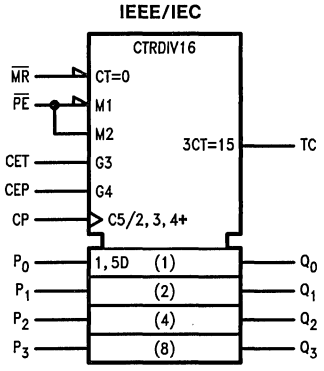
IEEE/IEC



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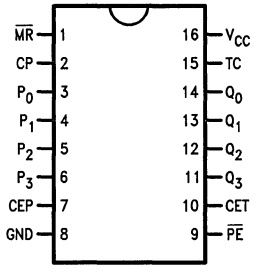
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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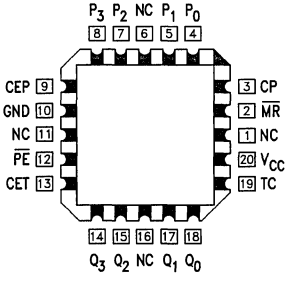
Pin Assignment for LCC



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Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$	Asynchronous Master Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Inputs
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Functional Description

The 'AC/'ACT161 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Five control inputs—Master Reset, Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT161 use D-type edge-triggered flip-flops and changing the $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in *Figure 2* are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle requires 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs O_0–O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces O_0–O_3 to the High Z state but does not prevent counting, loading or resetting.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

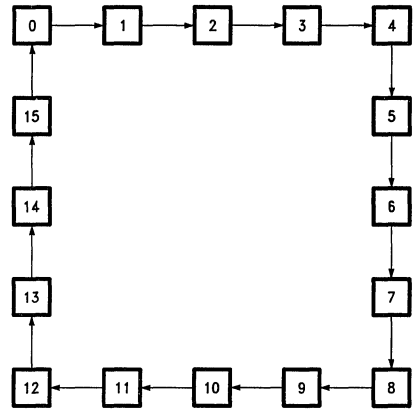
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

Mode Select Table

$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐‾)
X	X	X	Reset (Clear)
L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	Count (Increment)
H	L	X	No Change (Hold)
H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



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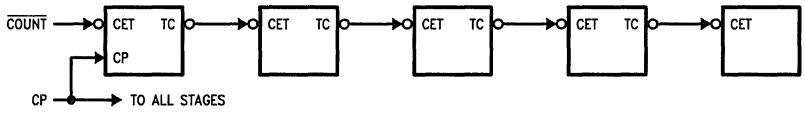

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FIGURE 1. Multistage Counter with Ripple Carry

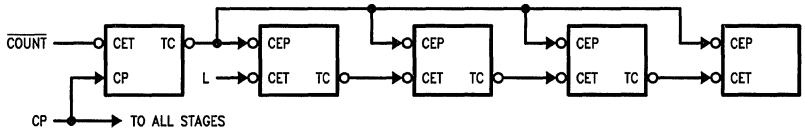

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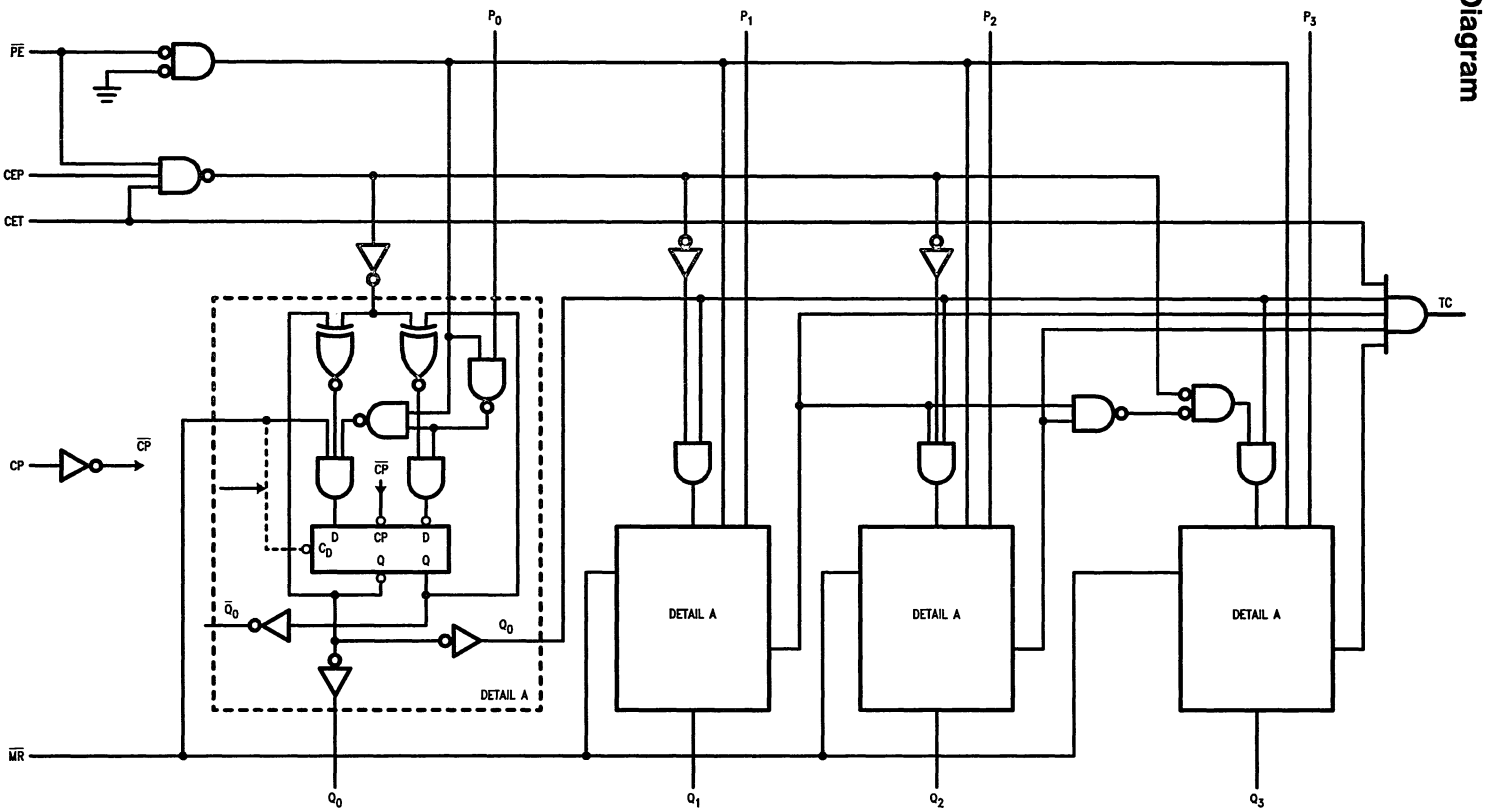
FIGURE 2. Multistage Counter with Lookahead Carry

Block Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.5	0.44		12 mA
		4.5		0.36	0.5	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	111 167		55 80		60 95		MHz	
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.0 5.0	12 9.0	1.0 1.0	15.0 11.0	1.5 1.0	13.5 9.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	7.0 5.0	12 9.5	1.0 1.0	15.0 11.0	1.5 1.5	13 10	ns	2-3,4
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9 6	15 10.5	1.0 1.0	18.5 13.0	2.5 1.5	16.5 11.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	8.5 6.5	14 11	1.0 1.0	17.5 13.0	2.5 2.0	15.5 11.5	ns	2-3,4
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	5.5 3.5	9.5 6.5	1.0 1.0	13.0 8.5	1.5 1.0	11 7.5	ns	2-3,4
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	6.5 5	11 8.5	1.0 1.0	14.5 11.0	2.0 1.5	12.5 9.5	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	2.0 1.5	6.5 5.5	12 9.5	1.0 1.0	14.5 10.5	1.5 1.5	13.5 10	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	3.3 5.0	3.5 2.5	10 8.5	15 13	1.0 1.0	18.5 14.0	3.0 2.5	17.5 13.5	ns	2-3,4

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	6.0 3.5	13.5 8.5	16.0 10.5	16 10.5	ns	2-7
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −4.0	−1 0	0.5 1.5	−0.5 0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	6.5 4.0	11.5 7.5	15.0 10.5	14 8.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−6.0 −3.5	0 0.5	−1.0 0.0	0 1	ns	2-7
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.0 2.0	6.0 4.5	7.5 5.5	7 5	ns	2-7
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−3.5 −2	0 0	2.0 2.0	0 0.5	ns	2-7
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	2.0 2.0	3.5 2.5	5.0 5.0	4 3	ns	2-3
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	2.0 2.0	4.0 3.0	5.0 5.0	4.5 3.5	ns	2-3
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	3.0 2.5	5.5 4.5	5.0 5.0	7.5 6.0	ns	2-3
t_{rec}	Recovery Time $\overline{MR}$ to CP		−2 −1	−0.5 0	1.5 2.0	0 0.5	ns	2-3,7

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	115	125				100		MHz	
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	5.5	9.5			1.5	10.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	6.0	10.5			1.5	11.5	ns	2-3,4
t_{PLH}	Propagation Delay CP to TC	5.0	2.0	7.0	11.0			1.5	12.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to TC	5.0	1.5	8.0	12.5			1.5	13.5	ns	2-3,4
t_{PLH}	Propagation Delay CET to TC	5.0	1.5	5.5	8.5			1.5	10.0	ns	2-3,4
t_{PHL}	Propagation Delay CET to TC	5.0	1.5	6.5	9.5			1.5	10.5	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.5	6.0	10.0			1.5	11.0	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	5.0	2.5	8.0	13.5			2.0	14.5	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	9.5		11.5	ns	2-3,4
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0		0	ns	2-3,4
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5		9.5	ns	2-3,4
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5		−0.5	ns	2-3,4
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		6.5	ns	2-3,4
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0		0	ns	2-3,4
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0		3.5	ns	2-3
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0		3.5	ns	2-3
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	3.0	3.0		7.5	ns	2-3
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0		0.5	ns	2-3,7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC163 • 54ACT/74ACT163
Synchronous Presettable Binary Counter

General Description

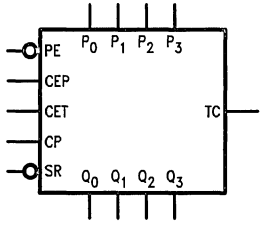
The 'AC/'ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Features

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT163 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'AC163: 5962-89582

Ordering Code: See Section 8

Logic Symbols



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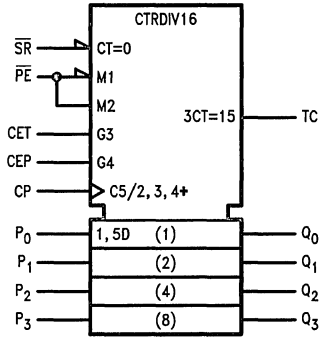
IEEE/IEC



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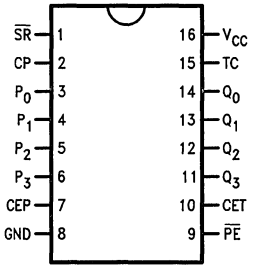
Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{SR}$	Synchronous Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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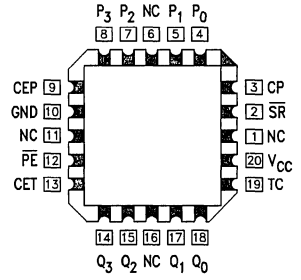
Pin Assignment for LCC



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Functional Description

The 'AC/'ACT163 counts in modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: synchronous reset, parallel load, count-up and hold. Four control inputs—Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle ($\overline{CET}$)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{SR}$ HIGH, CEP and $\overline{CET}$ permit counting when both are HIGH. Conversely, a LOW signal on either CEP or $\overline{CET}$ inhibits counting.

The 'AC/'ACT163 uses D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and $\overline{CET}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when $\overline{CET}$ is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and $\overline{CET}$ inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in *Figure 2* are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{CEP}$, $\overline{CET}$, and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs O_0–O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces O_0–O_3 to the High Z state but does not prevent counting, loading or resetting.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

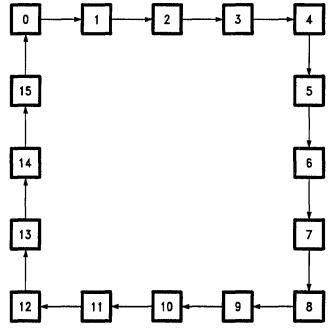
$\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CET}$

Mode Select Table

$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



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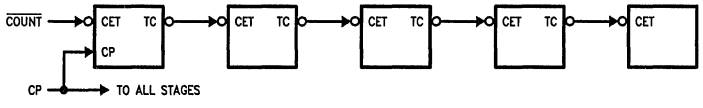

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FIGURE 1

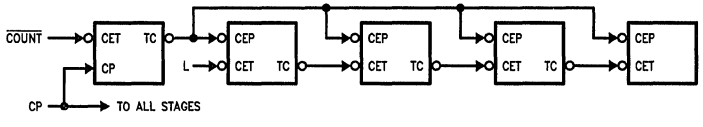

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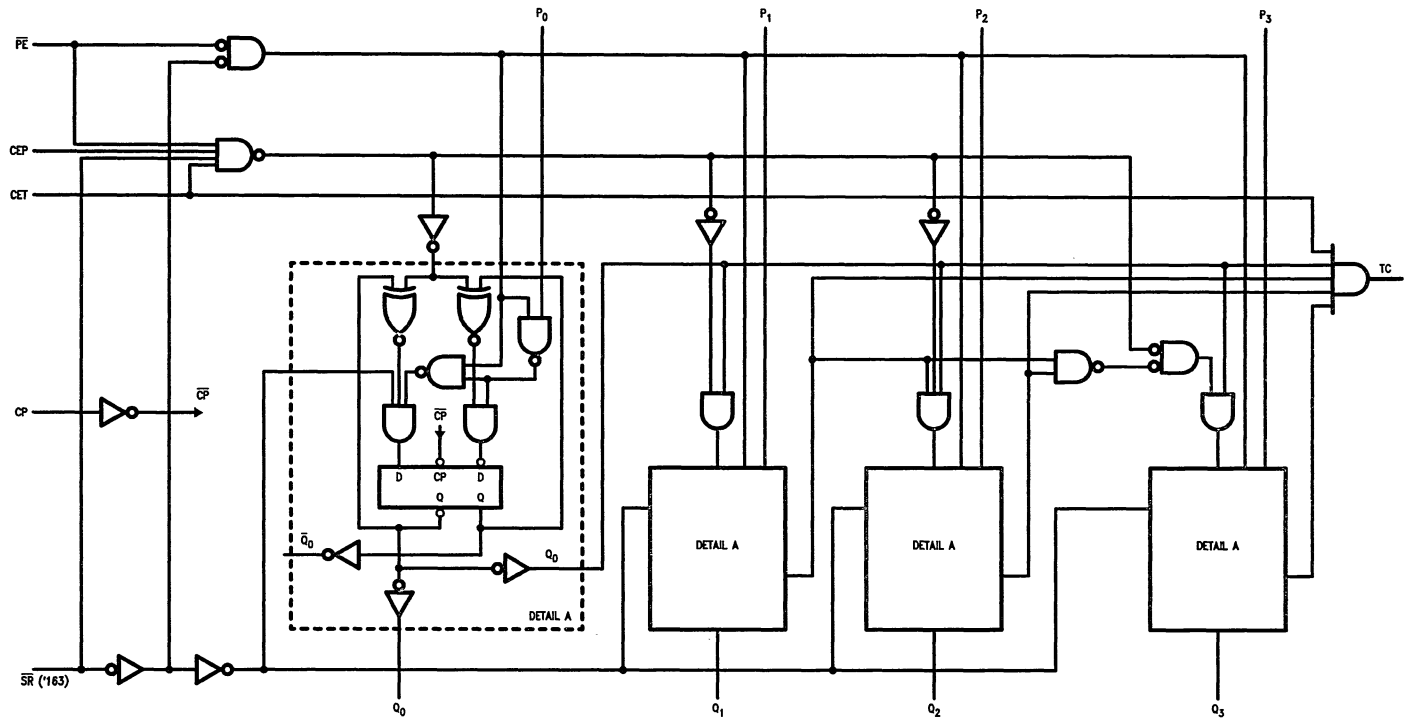
FIGURE 2

Block Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	70 110	95 140		55 90		60 95		MHz	
t_{PLH}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.5 5.5	12.5 9.0	1.0 1.0	13.5 9.5	1.5 1.0	13.5 9.5	ns	2-3,4
t_{PHL}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	12.0 9.5	1.0 1.0	12.5 9.5	1.5 1.5	13.0 10.0	ns	2-3,4
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9.5 7.0	15.0 10.5	1.0 1.0	16.5 11.0	2.5 1.5	16.5 11.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	11.0 8.0	14.0 11.0	1.0 1.0	15.0 11.0	2.5 2.0	15.5 11.5	ns	2-3,4
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	7.5 5.5	9.5 6.5	1.0 1.0	11.0 7.5	1.5 1.0	11.0 7.5	ns	2-3,4
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	8.5 6.0	11.0 8.5	1.0 1.0	12.0 9.0	2.0 1.5	12.5 9.5	ns	2-3,4

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0	13.5 8.5	17.0 11.0	16.0 10.5	ns	2-7
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0	−1.0 0	−0.5 0	−0.5 0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0	14.0 9.5	17.0 12.0	16.5 11.0	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5	−1.0 −0.5	−0.5 0	−0.5 0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0	11.5 7.5	16.0 9.5	14.0 8.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.0	−1.0 −0.5	−0.5 0	−0.5 0	ns	2-7
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5	8.0 5.5	7.0 5.0	ns	2-7
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0	0 0	0 0.5	0 0.5	ns	2-7
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5	5.0 5.0	4.0 3.0	ns	2-3
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0	5.0 5.0	4.5 3.5	ns	2-3

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	140				105		MHz	
t_{PLH}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	5.5	10.0			1.5	11.0	ns	2-3,4
t_{PHL}	Propagation Delay, CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	6.0	11.0			1.5	12.0	ns	2-3,4
t_{PLH}	Propagation Delay CP to TC	5.0	2.5	7.0	11.5			2.0	13.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to TC	5.0	3.0	8.0	13.5			2.0	15.0	ns	2-3,4
t_{PLH}	Propagation Delay CET to TC	5.0	2.0	5.5	9.0			1.5	10.5	ns	2-3,4
t_{PHL}	Propagation Delay CET to TC	5.0	2.0	6.0	10.0			2.0	11.0	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	10.0		12.0	ns	2-7
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0.5		0.5	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	4.0	10.0		11.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	−5.5	−0.5		−0.5	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5		10.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5		0	ns	2-7
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		6.5	ns	2-7
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0		0.5	ns	2-7
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.5		3.5	ns	2-3
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5		3.5	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC169•54ACT/74ACT169
4-Stage Synchronous Bidirectional Counter

General Description

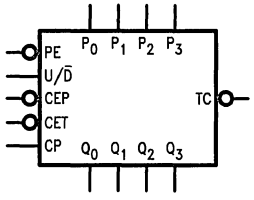
The 'AC/'ACT169 is fully synchronous 4-stage up/down counter. The 'AC/'ACT169 is a modulo-16 binary counter. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

Features

- Synchronous counting and loading
- Built-In lookahead carry capability
- Presettable for programmable operation
- Outputs source/sink 24 mA
- 'ACT has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbol



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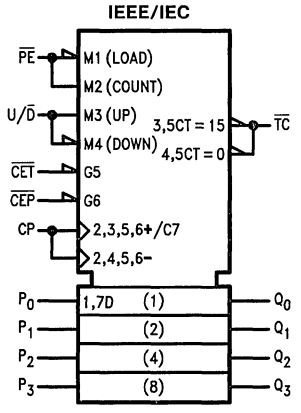

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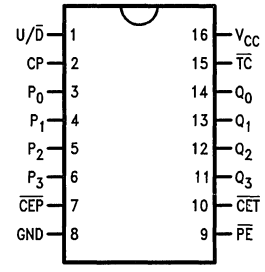
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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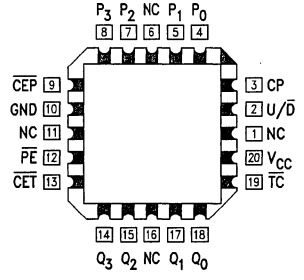
Pin Assignment for LCC



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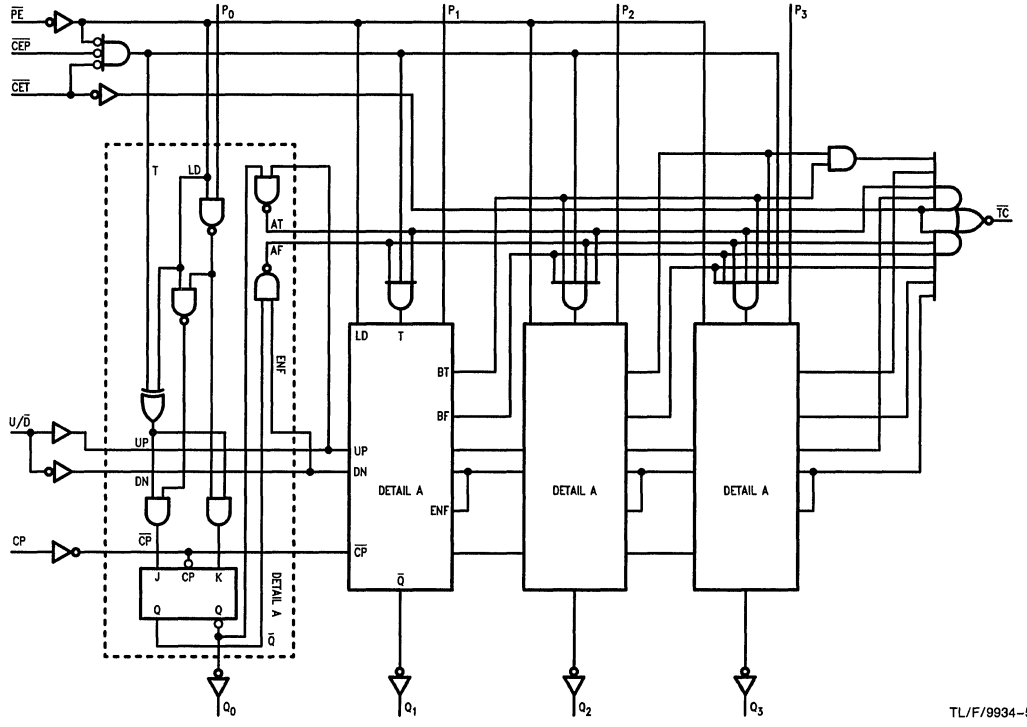
Pin Names	Description
$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up-Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC/'ACT169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0–P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. If an illegal state occurs, the 'AC169 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$

2) Up: $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 Q_3 \bullet (Up) \bullet \overline{CET}$

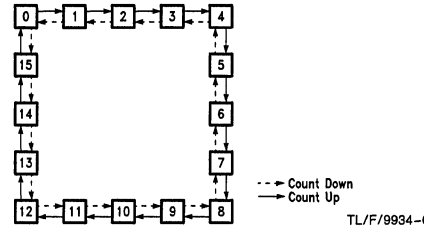
3) Down: $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Down) \bullet \overline{CET}$

Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (P_n to Q_n)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	75 100	118 154		55 75		65 90		MHz	
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	2.5 1.5	9.5 7.0	13.0 10.0	1.0 1.0	15.0 12.0	2.0 1.5	14.5 11.0	ns	2-3,4
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	2.5 1.5	10.5 7.5	14.5 11.0	1.0 1.0	16.5 13.0	2.0 1.5	16.0 12.0	ns	2-3,4
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	4.5 3.0	13.5 9.5	18.0 13.0	1.0 1.0	22.0 16.0	3.5 2.0	22.0 14.0	ns	2-3,4
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	3.5 2.5	13.5 9.5	18.0 13.0	1.0 1.0	22.0 16.0	3.0 2.0	20.5 14.5	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	3.5 3.0	11.0 8.0	15.0 10.5	1.0 1.0	18.5 13.0	3.0 2.5	16.5 12.0	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	3.0 2.0	9.5 7.0	12.5 9.0	1.0 1.0	16.0 11.0	2.5 1.5	14.5 10.0	ns	2-3,4
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0	3.5 2.5	11.0 8.0	15.0 10.5	1.0 1.0	18.5 13.0	3.0 2.0	17.0 12.0	ns	2-3,4
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0	2.5 1.5	10.0 7.0	13.5 9.5	1.0 1.0	16.5 12.0	2.0 1.5	15.5 10.5	ns	2-3,4

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms.

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	3.0 1.5	4.5 2.5	7.0 4.5	5.0 2.5	ns	2-7
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	1.5 0.5	0.5 1.5	2.0 2.5	0.5 1.5	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	7.5 4.5	10.5 7.0	13.5 9.0	12.5 8.0	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	4.5 2.0	0 0.5	0.5 2.5	0 1.0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0	10.0 6.5	13.5 9.5	12.0 8.0	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	6.0 4.0	0 0.5	0.5 2.5	0 1.0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0	5.5 3.5	8.5 6.5	6.5 4.0	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 1.5	0 0.5	0.5 2.0	0 0.5	ns	2-7
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	7.0 4.5	10.0 6.5	13.0 9.0	11.5 7.5	ns	2-7
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	7.0 4.0	0 0.5	0.5 2.0	0 0.5	ns	2-7
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	3.0 3.0	5.0 5.0	4.0 3.0	ns	2-3

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	90					90		MHz	
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	5.0	2.0	6.5	9.0			2.0	10.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	5.0	2.0	6.5	9.0			2.0	10.5	ns	2-3,4
t_{PLH}	Propagation Delay CP to $\overline{TC}$	5.0	3.0	9.0	11.5			3.0	14.0	ns	2-3,4
t_{PHL}	Propagation Delay CP to $\overline{TC}$	5.0	3.0	9.0	11.5			3.0	14.0	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	5.0	2.5	7.5	10.0			2.5	11.5	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	5.0	2.5	7.5	10.0			2.5	11.5	ns	2-3,4
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	5.0	2.5	8.0	10.5			2.5	12.0	ns	2-3,4
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	5.0	2.5	8.0	10.5			2.5	12.0	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	5.0		2.5		2.5	ns	2-7
t_h	Hold Time, HIGH or LOW P_n to CP	5.0		1.5		1.5	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	5.0		7.0		7.0	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	5.0		0		0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	5.0		7.0		7.0	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	5.0		0		0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0		6.0		6.0	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0		0.5		0.5	ns	2-7
t_s	Setup Time, HIGH or LOW $U/\overline{D}$ to CP	5.0		7.0		7.0	ns	2-7
t_h	Hold Time, HIGH or LOW $U/\overline{D}$ to $\overline{CP}$	5.0		0.5		0.5	ns	2-7
t_w	CP Pulse Width, HIGH or LOW	5.0		4.0		4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC174 • 54ACT/74ACT174
Hex D Flip-Flop with Master Reset

General Description

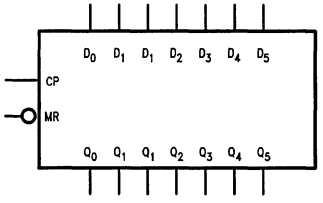
The 'AC/'ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

- Outputs source/sink 24 mA
- 'ACT174 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC174: 5962-87626
  - — 'ACT174: 5962-87757

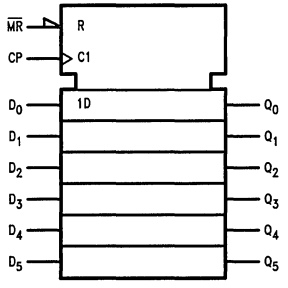
Ordering Code: See Section 8

Logic Symbols



TL/F/9935–1

IEEE/IEC

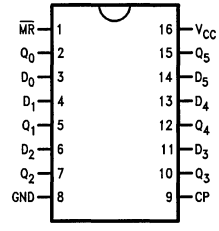


TL/F/9935–2

Pin Names	Description
D_0–D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_5	Outputs

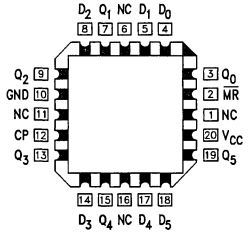
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9935–3

Pin Assignment for LCC



TL/F/9935–4

Functional Description

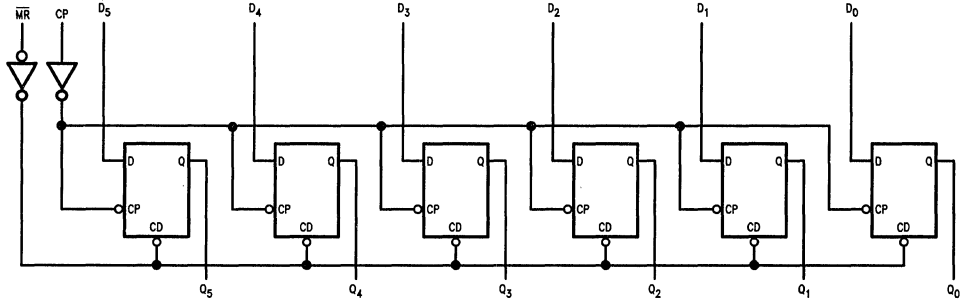
The 'AC/'ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 'AC/'ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	⌐	H	H
H	⌐	L	L
H	L	X	Q

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/9935–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	90 100	100 125		65 90		70 100		MHz	
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	2.0 1.5	9.0 6.0	11.5 8.5	1.0 1.0	14.0 10.5	1.5 1.0	12.5 9.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	2.0 1.5	8.5 6.0	11.0 8.0	1.0 1.0	13.0 10.0	1.5 1.0	12.0 9.0	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	2.5 1.5	9.0 7.0	11.5 9.0	1.0 1.0	13.5 11.0	2.0 1.5	12.5 10.5	ns	2-3,4

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.5 2.0	6.5 5.0	7.5 5.5	7.0 5.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	1.0 0.5	3.0 3.0	3.0 3.0	3.0 3.0	ns	2-7
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	7.0 5.0	ns	2-3
t_w	CP Pulse Width	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	7.0 5.0	ns	2-3
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0	2.5 2.0	3.0 2.0	2.5 2.0	ns	2-3,7

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	165	200		95		140		MHz	
t_{PLH}	Propagation Delay CP to Q_n	5.0	1.5	7.0	10.5	1.0	12.5	1.5	11.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to Q_n	5.0	1.5	7.0	10.5	1.0	13.0	1.5	11.5	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.5	6.5	9.5	1.0	12.0	1.5	11.0	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	0.5	1.5	3.0	1.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0	2.0	2.0	2.0	ns	2-7
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	1.5	3.0	5.0	3.5	ns	2-3
t_w	CP Pulse Width, HIGH OR LOW	5.0	1.5	3.0	5.0	3.5	ns	2-3
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	−1.0	0.5	1.0	0.5	ns	2-3,7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	85.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC175 • 54ACT/74ACT175
Quad D Flip-Flop

General Description

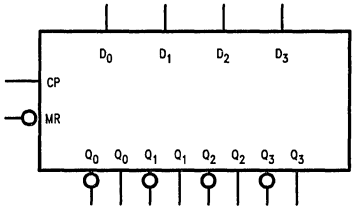
The 'AC/'ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset
- True and complement output
- Outputs source/sink 24 mA
- 'ACT175 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC175: 5962-89552
  - — 'ACT175: 5962-89693

Ordering Code: See Section 8

Logic Symbols



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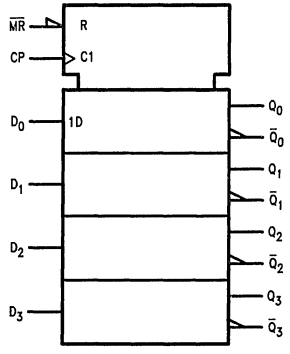
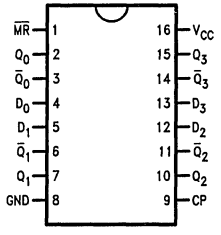
IEEE/IEC



TL/F/9936-2

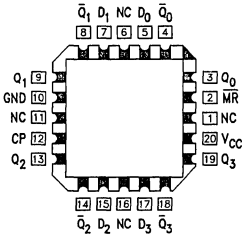
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9936-3

Pin Assignment for LCC



TL/F/9936-4

Pin Names	Description
D_0–D_3	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

Functional Description

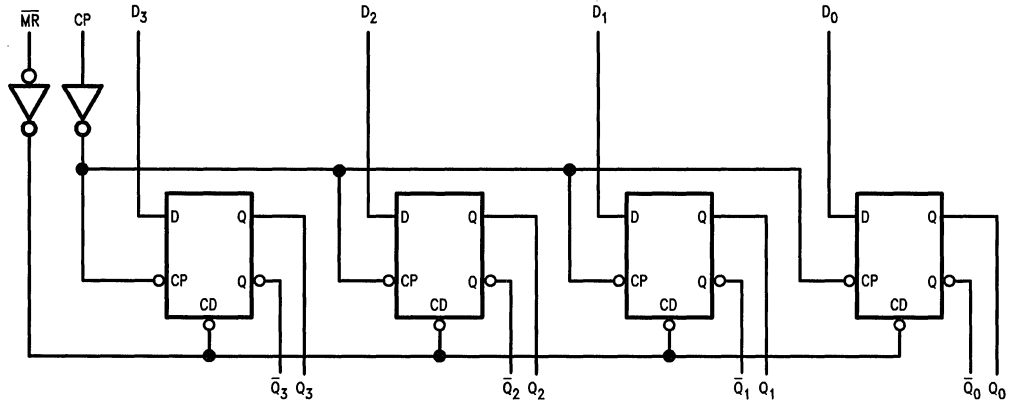
The 'AC/'ACT175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'AC/'ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs	Outputs	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



TL/F/9936–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	149	214		95		139		MHz	
		5.0	187	244		95		187			
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3	2.0	9.5	12.0	1.0	15.0	2.0	13.5	ns	2-3,4
		5.0	1.5	7.0	9.0	1.0	11.5	1.0	9.5		
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3	2.5	8.5	13.0	1.0	14.5	2.0	14.5	ns	2-3,4
		5.0	1.5	6.0	9.5	1.0	10.5	1.5	10.5		
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	3.3	3.0	7.5	12.5	1.0	13.5	2.5	13.5	ns	2-3,4
		5.0	2.0	5.5	9.0	1.0	10.5	1.5	10.0		
t_{PHL}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	3.3	3.0	8.5	11.0	1.0	15.0	2.5	12.5	ns	2-3,4
		5.0	2.0	6.0	8.5	1.0	11.0	1.5	9.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	2.0	4.5	5.0	4.5	ns	2-7
		5.0	1.0	3.0	3.5	3.0		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	1.0	1.0	2.0	1.0	ns	2-7
		5.0	1.0	1.0	2.5	1.0		
t_w	CP Pulse Width HIGH or LOW	3.3	2.5	4.5	6.0	4.5	ns	2-3
		5.0	2.0	3.5	5.0	3.5		
t_w	$\overline{MR}$ Pulse Width, LOW	3.3	2.5	4.5	5.5	5.0	ns	2-3
		5.0	2.0	3.5	5.0	3.5		
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3	−2.0	0	1.5	0	ns	2-3,7
		5.0	−1.0	0	1.5	0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	175	236		95		145		MHz	
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	2.0	6.0	10.0	1.0	11.5	1.5	11.0	ns	2-3,4
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	2.0	7.0	11.0	1.0	12.5	1.5	12.0	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	5.0	2.0	6.0	9.5	1.0	11.5	1.5	10.5	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	5.0	2.0	5.5	9.5	1.0	11.0	1.5	10.5	ns	2-3,4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s (H) t_s (L)	Setup Time D_n to CP	5.0	3.0 3.0	2.0 2.5	3.5 3.5	2.0 2.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.0	1.5	1.0	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0	4.0	3.0	5.0	3.5	ns	2-3
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	4.0	3.0	5.0	4.0	ns	2-3
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0	0	0	1.5	0	ns	2-3,7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC191
Up/Down Counter with Preset and Ripple Clock

General Description

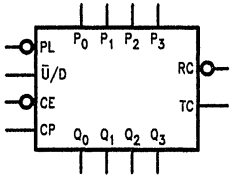
The 'AC191 is a reversible modulo 16 binary counter. It features synchronous counting and asynchronous presetting. The preset feature allows the 'AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

Features

- High speed—133 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable
- Outputs source/sink 24 mA

Ordering Code: See Section 8

Logic Symbols



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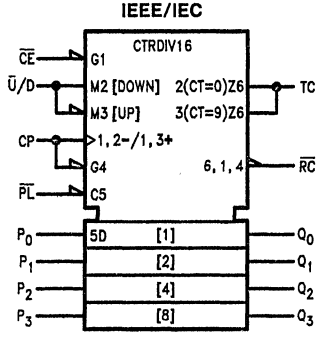

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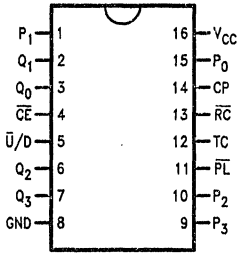
Pin Names	Description
$\overline{CE}$	Count Enable Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input
$\overline{U}/D$	Up/Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output
TC	Terminal Count Output

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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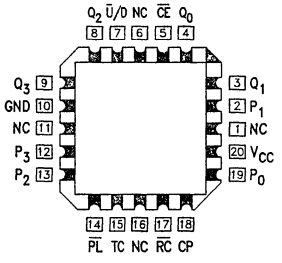
Pin Assignment for LCC



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Functional Description

The 'AC191 is a synchronous up/down counter. The 'AC191 is organized as a 4-bit binary counter. It contains four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Load inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 15 in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, $\overline{RC}$ output wil go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in *Figures A* and *B*. In *Figure A*, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in *Figure B*. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in *Figure C* avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of *Figures A* and *B* doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

Mode Select Table

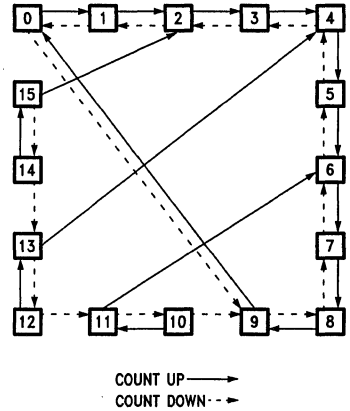
Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	↗	Count Up
H	L	H	↗	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ Truth Table

Inputs				Outputs
$\overline{PL}$	$\overline{CE}$	TC*	CP	$\overline{RC}$
H	L	H	⊓	⊓
H	H	X	X	H
H	X	L	X	H
L	X	X	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

State Diagram



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Functional Description (Continued)

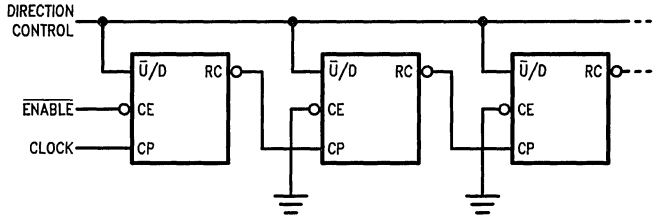

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FIGURE A. N-Stage Counter Using Ripple Clock

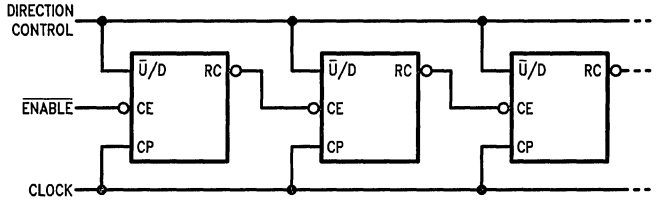

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FIGURE B. Synchronous N-Stage Counter Using Ripple Carry/Borrow

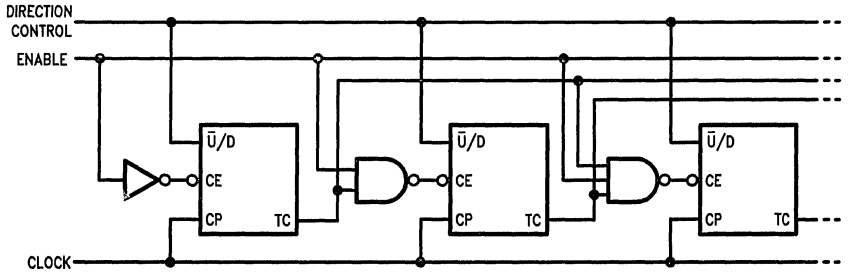

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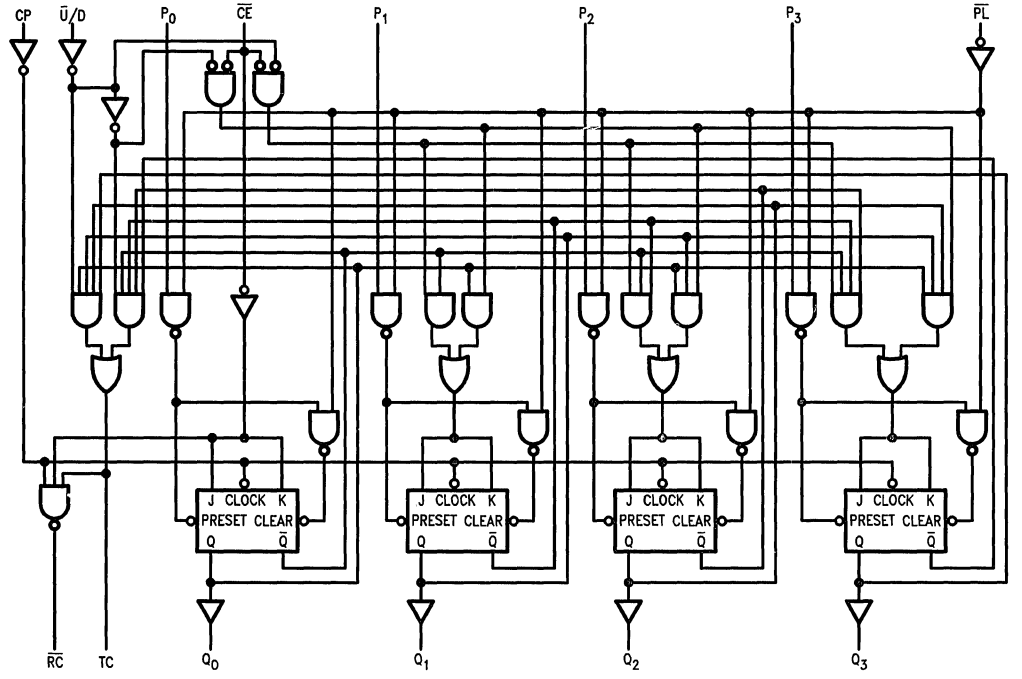
FIGURE C. Synchronous N-Stage Counter with Parallel Gated Carry/Borrow

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46	V	I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44	V	I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 90	105 133		55 80		65 85		MHz	
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	2.0 1.5	8.5 6.0	15.0 11.0	1.0 1.0	16.5 12.0	1.5 1.5	16.0 12.0	ns	2-3,4
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	2.5 1.5	8.5 6.0	14.5 10.5	1.0 1.0	16.0 12.0	2.0 1.5	16.0 11.5	ns	2-3,4
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.5 2.5	10.5 7.5	18.0 12.0	1.0 1.0	19.5 14.0	2.5 1.5	20.0 14.0	ns	2-3,4
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	4.0 2.5	10.5 7.5	17.5 12.5	1.0 1.0	19.0 14.5	3.0 2.0	19.0 13.5	ns	2-3,4
t_{PLH}	Propagation Delay CP to $\overline{RC}$	3.3 5.0	2.5 2.0	7.5 5.5	12.0 9.5	1.0 1.0	14.0 10.5	2.0 1.0	13.5 10.5	ns	2-3,4
t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.5	1.0 1.0	12.5 9.5	2.0 1.0	12.5 9.5	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0	2.5 1.5	7.0 5.0	12.0 8.5	1.0 1.0	14.0 10.0	1.5 1.0	13.5 9.5	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0	2.0 1.5	6.5 5.0	11.0 8.0	1.0 1.0	12.5 9.5	1.5 1.0	12.5 9.0	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	3.3 5.0	2.5 1.5	6.5 5.0	12.5 9.0	1.0 1.0	14.5 11.0	2.0 1.0	14.5 10.0	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{U}/D$ to $\overline{RC}$	3.3 5.0	2.5 1.5	7.0 5.0	12.0 8.5	1.0 1.0	15.0 11.0	2.0 1.0	13.5 10.0	ns	2-3,4
t_{PLH}	Propagation Delay $\overline{U}/D$ to TC	3.3 5.0	2.0 1.5	7.0 5.0	11.5 8.5	1.0 1.0	14.0 13.5	1.5 1.0	13.5 9.5	ns	2-3,4
t_{PHL}	Propagation Delay $\overline{U}/D$ to TC	3.3 5.0	2.0 1.5	6.5 5.0	11.0 8.5	1.0 1.0	13.5 10.0	1.5 1.0	12.5 9.5	ns	2-3,4
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.0	2.5 2.0	8.0 5.5	13.5 9.5	1.0 1.0	16.5 11.5	2.0 1.0	15.5 10.5	ns	2-3,4

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms (Continued)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay P_n to Q_n	3.3	2.5	7.5	13.0	1.0	15.5	1.5	14.5	ns	2-3,4
		5.0	1.5	5.5	9.5	1.0	10.5	1.0	10.5		
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3	3.5	9.5	14.5	1.0	18.0	2.5	17.5	ns	2-3,4
		5.0	2.0	5.5	9.5	1.0	12.5	1.0	10.5		
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3	3.0	8.0	13.5	1.0	15.5	2.0	15.5	ns	2-3,4
		5.0	2.0	6.0	10.0	1.0	11.5	1.5	11.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3	1.0	3.0	4.0	3.0	ns	2-7
		5.0	0.5	2.0	3.0	2.5		
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3	−1.5	0.5	1.5	1.0	ns	2-7
		5.0	−0.5	1.0	2.0	1.0		
t_s	Setup Time, LOW $\overline{CE}$ to CP	3.3	3.0	6.0	9.0	7.0	ns	2-7
		5.0	1.5	4.0	6.0	4.5		
t_h	Hold Time, LOW $\overline{CE}$ to CP	3.3	−4.0	−0.5	0	−0.5	ns	2-7
		5.0	−2.5	0	0.5	0		
t_s	Setup Time, HIGH or LOW $\overline{U}/D$ to CP	3.3	4.0	8.0	10.5	9.0	ns	2-7
		5.0	2.5	5.5	7.5	6.5		
t_h	Hold Time, HIGH or LOW $\overline{U}/D$ to CP	3.3	−5.0	0	0	0	ns	2-7
		5.0	−3.0	0.5	1.0	0.5		
t_w	$\overline{PL}$ Pulse Width, LOW	3.3	2.0	3.5	5.0	4.0	ns	2-3
		5.0	1.0	1.0	5.0	1.0		
t_w	CP Pulse Width, LOW	3.3	2.0	3.5	6.0	4.0	ns	2-3
		5.0	2.0	3.0	6.0	4.0		
t_{rec}	Recovery Time $\overline{PL}$ to CP	3.3	−0.5	0	1.5	0	ns	2-3,7
		5.0	−1.0	0	1.0	0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	75.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC240 • 54ACT/74ACT240
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

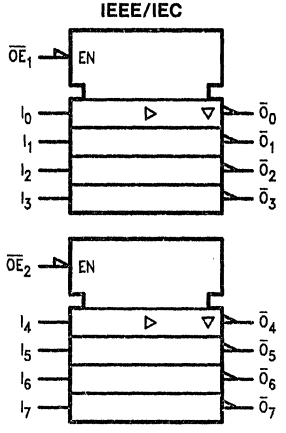
The 'AC/'ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- Inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT240 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC240: 5962-87550
  - — 'ACT240: 5962-87759

Ordering Code: See Section 8

Logic Symbol



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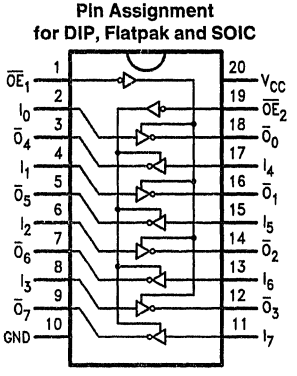
Connection Diagrams



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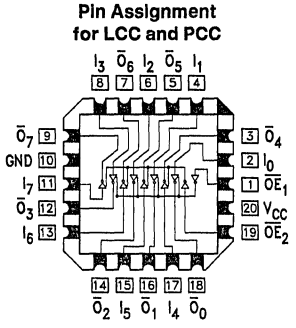


TL/F/9941–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = −55°C to +125°C	54AC T_A = −40°C to +85°C	74AC Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	2.46	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76	I_{OH} −24 mA
		5.5		4.86	4.7	4.76	−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	0.44	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44	I_{OL} 24 mA
		5.5		0.36	0.50	0.44	24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3	1.5	6.0	8.0	1.0	11.0	1.0	9.0	ns	2-3,4
		5.0	1.5	4.5	6.5	1.0	8.5	1.0	7.0		
t_{PHL}	Propagation Delay Data to Output	3.3	1.5	5.5	8.0	1.0	10.5	1.0	8.5	ns	2-3,4
		5.0	1.5	4.5	6.0	1.0	8.0	1.0	6.5		
t_{PZH}	Output Enable Time	3.3	1.5	6.0	10.5	1.0	11.5	1.0	11.0	ns	2-5
		5.0	1.5	5.0	7.0	1.0	9.0	1.0	8.0		
t_{PZL}	Output Enable Time	3.3	1.5	7.0	10.0	1.0	13.0	1.0	11.0	ns	2-6
		5.0	1.5	5.5	8.0	1.0	10.5	1.0	8.5		
t_{PHZ}	Output Disable Time	3.3	1.5	7.0	10.0	1.0	12.5	1.0	10.5	ns	2-5
		5.0	1.5	6.5	9.0	1.0	10.5	1.0	9.5		
t_{PLZ}	Output Disable Time	3.3	1.5	7.5	10.5	1.0	13.5	1.0	11.5	ns	2-6
		5.0	1.5	6.5	9.0	1.0	11.0	1.0	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V
*Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.5	6.0	8.5	1.0	9.5	1.5	9.5	ns	2-3,4
t_{PHL}	Propagation Delay Data to Output	5.0	1.5	5.5	7.5	1.0	9.0	1.5	8.5	ns	2-3,4
t_{PZH}	Output Enable Time	5.0	1.5	7.0	8.5	1.0	10.0	1.0	9.5	ns	2-5
t_{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.0	11.5	1.5	10.5	ns	2-6
t_{PHZ}	Output Disable Time	5.0	2.0	8.0	9.5	1.0	11.0	2.0	10.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	2.5	6.5	10.0	1.0	11.5	2.0	10.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC241 • 54ACT/74ACT241
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC/'ACT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

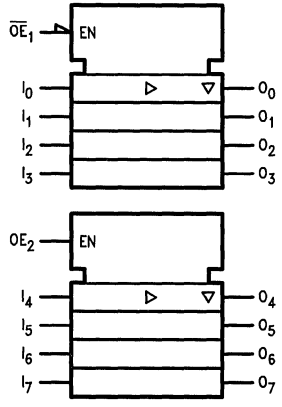
Features

- Non-inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT241 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC241: 5962-87551
  - — 'ACT241: 5962-89847

Ordering Code: See Section 8

Logic Symbol

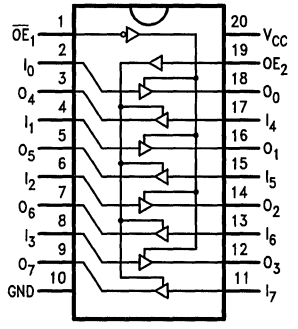
IEEE/IEC



TL/F/9942–2

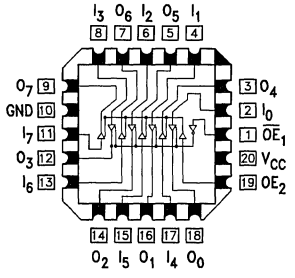
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9942–1

Pin Assignment for LCC and PCC



TL/F/9942–3

Pin Names	Description
$\overline{OE}_1$,	TRI-STATE Output Enable Input
OE_2	TRI-STATE Output Enable Input (Active HIGH)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE_2	I_n	
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74AC $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74ACT $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3	1.5	6.0	9.0	1.0	12.0	1.5	10.0	ns	2-3, 4
		5.0	1.5	5.0	7.0	1.0	9.5	1.0	7.5		
t_{PHL}	Propagation Delay Data to Output	3.3	1.5	6.0	9.0	1.0	11.5	1.0	10.5	ns	2-3, 4
		5.0	1.5	4.5	7.0	1.0	9.0	1.0	7.5		
t_{PZH}	Output Enable Time	3.3	1.5	6.5	12.5	1.0	13.0	1.0	13.0	ns	2-5
		5.0	1.5	5.5	9.0	1.0	10.0	1.0	9.5		
t_{PZL}	Output Enable Time	3.3	1.5	7.0	12.0	1.0	13.0	1.5	13.0	ns	2-6
		5.0	1.5	5.5	9.0	1.0	10.0	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	2.0	8.0	12.0	1.0	13.0	2.0	12.5	ns	2-5
		5.0	1.5	6.5	10.0	1.0	11.5	1.0	10.5		
t_{PLZ}	Output Disable Time	3.3	1.5	7.0	12.5	1.0	13.0	1.0	13.5	ns	2-6
		5.0	1.5	6.0	10.0	1.0	11.5	1.0	10.5		

*Voltage Range 3.3 is 3.3V ±3.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.5	6.5	9.0	1.0	10.0	1.5	10.0	ns	2-3, 4
t_{PHL}	Propagation Delay Data to Output	5.0	1.5	7.0	9.0	1.0	10.0	1.5	10.0	ns	2-3, 4
t_{PZH}	Output Enable Time	5.0	1.5	6.0	9.0	1.0	11.5	1.0	10.0	ns	2-5
t_{PZL}	Output Enable Time	5.0	1.5	7.0	10.0	1.0	12.5	1.5	11.0	ns	2-6
t_{PHZ}	Output Disable Time	5.0	1.5	8.0	10.5	1.0	12.5	1.5	11.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	2.0	7.0	10.5	1.0	12.5	1.5	11.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC244 • 54ACT/74ACT244
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC/'ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

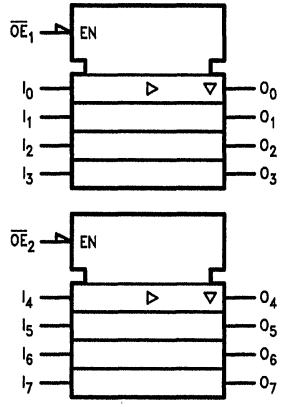
Features

- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT244 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC244: 5962-87552
  - — 'ACT244: 5962-87760

Ordering Code: See Section 8

Logic Symbol

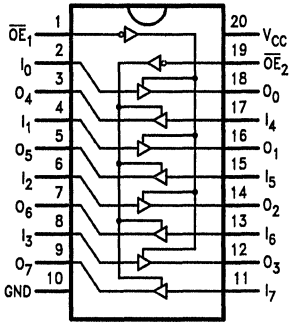
IEEE/IEC



TL/F/9943–1

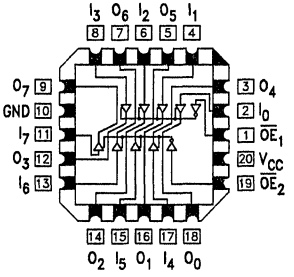
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9943–2

Pin Assignment for LCC and PCC



TL/F/9943–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, V_{GND} $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	6.5 5.0	9.0 7.0	1.0 1.0	12.5 9.5	1.5 1.0	10.0 7.5	ns	2-3,4
t_{PHL}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	6.5 5.0	9.0 7.0	1.0 1.0	12.0 9.0	2.0 1.0	10.0 7.5	ns	2-3,4
t_{PZH}	Output Enable Time	3.3 5.0	2.0 1.5	6.0 5.0	10.5 7.0	1.0 1.0	11.5 9.0	1.5 1.5	11.0 8.0	ns	2-5
t_{PZL}	Output Enable Time	3.3 5.0	2.5 1.5	7.5 5.5	10.0 8.0	1.0 1.0	13.0 10.5	2.0 1.5	11.0 8.5	ns	2-6
t_{PHZ}	Output Disable Time	3.3 5.0	3.0 2.5	7.0 6.5	10.0 9.0	1.0 1.0	12.5 10.5	1.5 1.0	10.5 9.5	ns	2-5
t_{PLZ}	Output Disable Time	3.3 5.0	2.5 2.0	7.5 6.5	10.5 9.0	1.0 1.0	13.0 11.0	2.5 2.0	11.5 9.5	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	2.0	6.5	9.0	1.0	10.0	1.5	10.0	ns	2-3,4
t_{PHL}	Propagation Delay Data to Output	5.0	2.0	7.0	9.0	1.0	10.0	1.5	10.0	ns	2-3,4
t_{PZH}	Output Enable Time	5.0	1.5	6.0	8.5	1.0	9.5	1.0	9.5	ns	2-5
t_{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns	2-6
t_{PHZ}	Output Disable Time	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	2.5	7.5	10.0	1.0	11.5	2.0	10.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC245 • 54ACT/74ACT245 Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

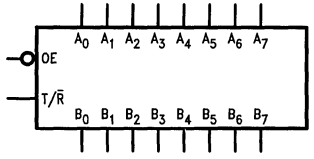
The 'AC/'ACT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

- Noninverting buffers
- Bidirectional data path
- A and B outputs source/sink 24 mA
- 'ACT245 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC245: 5962-87758
  - — 'ACT245: 5962-87663

Ordering Code: See Section 8

Logic Symbols



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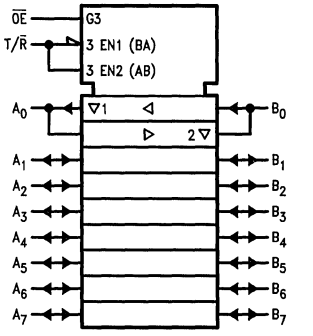

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Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A TRI-STATE Inputs or TRI-STATE Outputs
B_0–B_7	Side B TRI-STATE Inputs or TRI-STATE Outputs

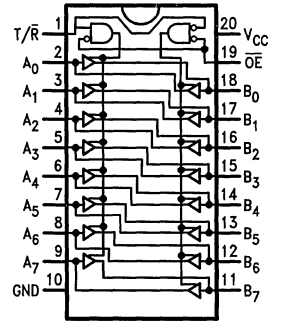
Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

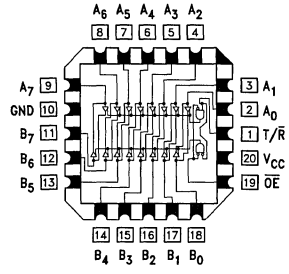
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9944–3

Pin Assignment for LCC and PCC



TL/F/9944–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		
		5.5		4.86	4.7	4.76		I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	11.5	1.0	9.0	ns	2-3,4
		5.0	1.5	3.5	6.5	1.0	8.5	1.0	7.0		
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.5	5.0	8.5	1.0	10.0	1.0	9.0	ns	2-3,4
		5.0	1.5	3.5	6.0	1.0	7.5	1.0	7.0		
t_{PZH}	Output Enable Time	3.3	2.5	7.0	11.5	1.0	13.5	2.0	12.5	ns	2-5
		5.0	1.5	5.0	8.5	1.0	10.0	1.0	9.0		
t_{PZL}	Output Enable Time	3.3	2.5	7.5	12.0	1.0	14.5	2.0	13.5	ns	2-6
		5.0	1.5	5.5	9.0	1.0	10.5	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	2.0	6.5	12.0	1.0	13.5	1.0	12.5	ns	2-5
		5.0	1.5	5.5	9.0	1.0	10.5	1.0	10.0		
t_{PLZ}	Output Disable Time	3.3	2.0	7.0	11.5	1.0	14.0	1.5	13.0	ns	2-6
		5.0	1.5	5.5	9.0	1.0	10.5	1.0	10.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.5	4.0	7.5	1.0	9.0	1.5	8.0	ns	2-3,4
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.5	4.0	8.0	1.0	10.0	1.0	9.0	ns	2-3,4
t_{PZH}	Output Enable Time	5.0	1.5	5.0	10.0	1.0	12.0	1.5	11.0	ns	2-5
t_{PZL}	Output Enable Time	5.0	1.5	5.5	10.0	1.0	13.0	1.5	12.0	ns	2-6
t_{PHZ}	Output Disable Time	5.0	1.5	5.5	10.0	1.0	12.0	1.0	11.0	ns	2-5
t_{PLZ}	Output Disable Time	5.0	2.0	5.0	10.0	1.0	12.0	1.5	11.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC251 • 54ACT/74ACT251
8-Input Multiplexer with TRI-STATE® Output

General Description

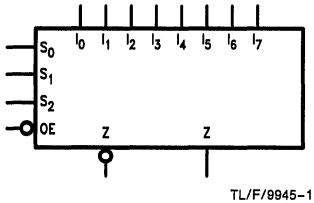
The 'AC/'ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

Features

- Multifunctional capability
- On-chip select logic decoding
- Inverting and noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT251 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC251: 5962-87692
  - — 'ACT251: 5962-89599

Ordering Code: See Section 8

Logic Symbols



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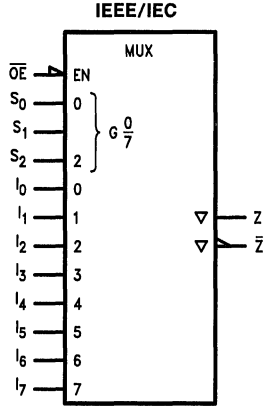
IEEE/IEC

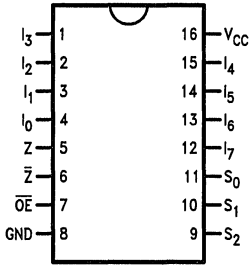


TL/F/9945–2

Pin Names	Description
S_0–S_2	Select Inputs
$\overline{OE}$	TRI-STATE Output Enable Input
I_0–I_7	Multiplexer Inputs
Z	TRI-STATE Multiplexer Output
$\overline{Z}$	Complementary TRI-STATE Multiplexer Output

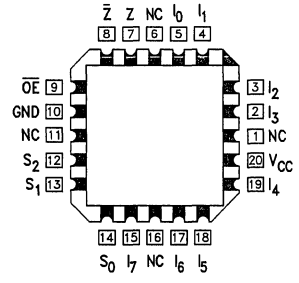
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9945–3

Pin Assignment for LCC



TL/F/9945–4

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

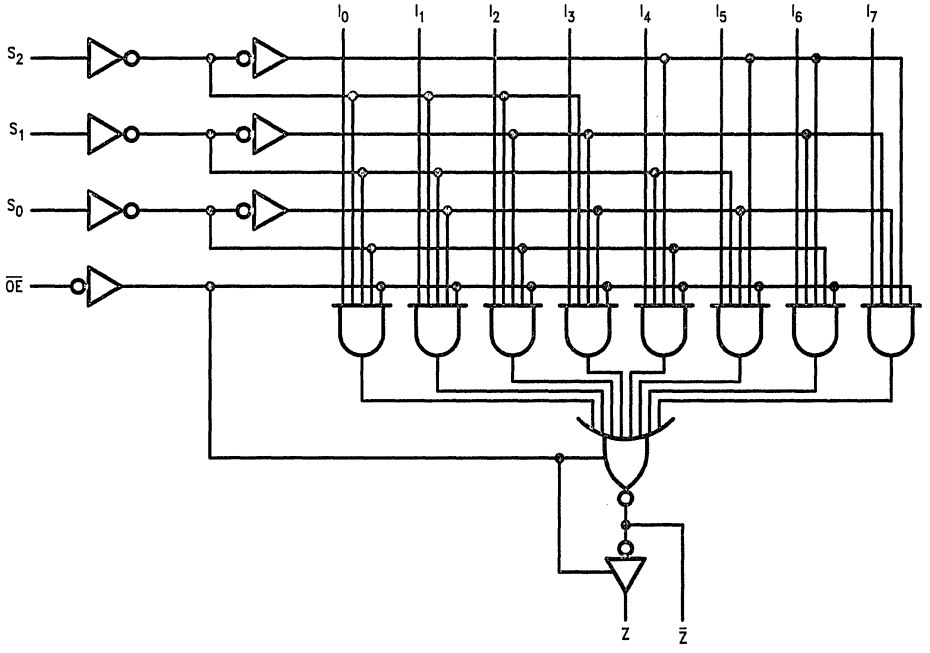
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

Truth Table

Inputs				Outputs	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/9945–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		I_{OH} −24 mA
		5.5		4.86	4.7		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50		I_{OL} 24 mA
		5.5		0.36	0.50		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.5	11.5	17.5	1.0	21.0	1.5	19.0	ns	2-3,4
		5.0	1.5	8.5	12.5	1.0	15.5	1.5	13.5		
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.5	11.0	17.5	1.0	21.0	1.5	19.0	ns	2-3,4
		5.0	1.5	8.0	12.5	1.0	15.5	1.5	13.5		
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.5	10.0	14.0	1.0	17.0	1.5	15.5	ns	2-3,4
		5.0	1.5	7.0	10.0	1.0	12.0	1.5	11.0		
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.5	9.0	14.0	1.0	16.5	1.5	15.5	ns	2-3,4
		5.0	1.5	6.5	10.0	1.0	12.0	1.5	11.0		
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	7.5	11.0	1.0	13.0	1.5	12.0	ns	2-5
		5.0	1.5	5.5	8.0	1.0	10.0	1.5	9.0		
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	7.5	11.0	1.0	13.0	1.5	12.0	ns	2-6
		5.0	1.5	5.5	8.0	1.0	10.0	1.5	9.0		
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	8.5	11.5	3.5	14.0	1.5	13.0	ns	2-5
		5.0	1.5	7.0	9.5	2.5	11.0	1.5	10.0		
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.5	7.0	11.0	4.0	13.0	1.5	12.0	ns	2-6
		5.0	1.5	5.5	8.0	3.0	10.0	1.5	8.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	2.5	7.0	15.5	1.0	18.5	2.0	17.0	ns	2-3,4
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	2.5	7.5	16.5	1.0	19.5	2.5	18.5	ns	2-3,4
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	2.5	5.5	12.0	1.0	14.0	2.0	13.0	ns	2-3,4
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	2.5	6.5	12.5	1.0	15.0	2.5	14.0	ns	2-3,4
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.5	5.0	8.5	1.0	10.0	1.5	9.0	ns	2-5
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.5	4.5	8.5	1.0	10.0	1.5	9.5	ns	2-6
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	2.0	6.0	12.0	1.0	13.5	2.0	13.0	ns	2-5
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.5	4.5	8.5	1.0	9.5	1.5	9.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	70.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC253 • 54ACT/74ACT253
Dual 4-Input Multiplexer with TRI-STATE® Outputs

General Description

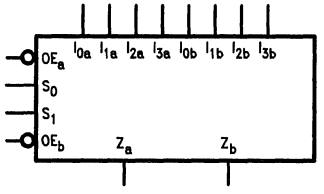
The 'AC/'ACT253 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

Features

- Multifunction capability
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT253 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC253: 5962-87693
  - — 'ACT253: 5962-87761

Ordering Code: See Section 8

Logic Symbols



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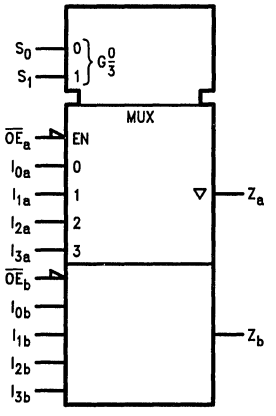
IEEE/IEC



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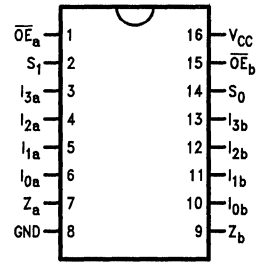
Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	TRI-STATE Outputs

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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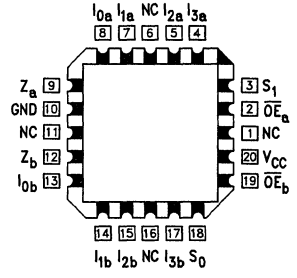
Pin Assignment for LCC



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Functional Description

The 'AC/'ACT253 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

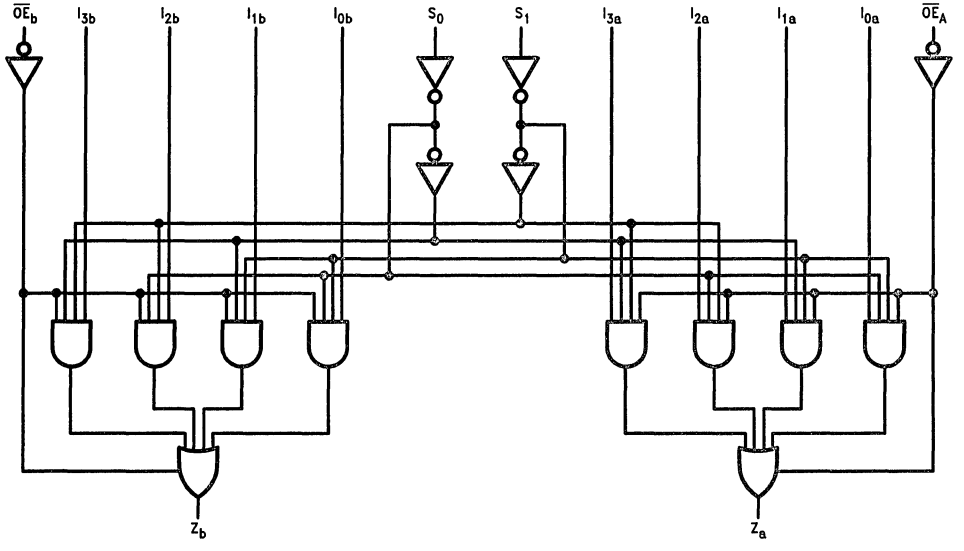
Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/9946–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3	2.0	8.5	15.5	1.0	19.5	2.0	17.5	ns	2-3,4
		5.0	2.0	6.5	11.0	1.0	13.5	1.5	12.5		
t_{PHL}	Propagation Delay S_n to Z_n	3.3	2.5	9.5	16.0	1.0	20.0	2.0	18.0	ns	2-3,4
		5.0	2.0	7.0	11.5	1.0	15.0	1.5	13.0		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.5	7.0	14.5	1.0	19.0	1.5	17.0	ns	2-3,4
		5.0	1.5	5.5	10.0	1.0	13.0	1.5	11.5		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	2.0	7.5	13.0	1.0	16.0	1.5	15.0	ns	2-3,4
		5.0	1.5	5.5	9.5	1.0	12.0	1.5	11.0		
t_{PZH}	Output Enable Time	3.3	1.5	4.5	8.0	1.0	9.5	1.0	8.5	ns	2-5
		5.0	1.5	3.5	6.0	1.0	7.0	1.0	6.5		
t_{PZL}	Output Enable Time	3.3	1.5	5.0	8.0	1.0	10.0	1.0	9.0	ns	2-6
		5.0	1.5	3.5	6.0	1.0	7.5	1.0	7.0		
t_{PHZ}	Output Disable Time	3.3	2.0	5.5	9.5	1.0	11.0	1.5	10.0	ns	2-5
		5.0	2.0	5.0	8.0	1.0	9.5	1.5	8.5		
t_{PLZ}	Output Disable Time	3.3	1.5	5.0	8.0	1.0	9.5	1.0	9.0	ns	2-6
		5.0	1.5	4.0	7.0	1.0	8.0	1.0	7.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	2.0	7.0	11.5	1.0	14.5	2.0	13.0	ns	2-3,4
t_{PHL}	Propagation Delay S_n to Z_n	5.0	3.0	7.5	13.0	1.0	16.0	2.5	14.5	ns	2-3,4
t_{PLH}	Propagation Delay I_n to Z_n	5.0	2.5	5.5	10.0	1.0	12.0	2.0	11.0	ns	2-3,4
t_{PHL}	Propagation Delay I_n to Z_n	5.0	3.5	6.5	11.0	1.0	13.5	3.0	12.5	ns	2-3,4
t_{PZH}	Output Enable Time	5.0	2.0	4.5	7.5	1.0	9.5	1.5	8.5	ns	2-5
t_{PZL}	Output Enable Time	5.0	2.0	5.0	8.0	1.0	9.5	1.5	9.0	ns	2-6
t_{PHZ}	Output Disable Time	5.0	3.0	6.0	9.5	1.0	11.0	2.5	10.0	ns	2-5
t_{PLZ}	Output Disable Time	5.0	2.5	4.5	7.5	1.0	9.0	2.0	8.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC257•54ACT/74ACT257
Quad 2-Input Multiplexer with TRI-STATE® Outputs

General Description

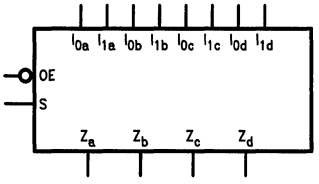
The 'AC/'ACT257 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

Features

- Multiplexer expansion by tying outputs together
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT257 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC257: 5962-88703
  - — 'ACT257: 5962-89689

Ordering Code: See Section 8

Logic Symbols



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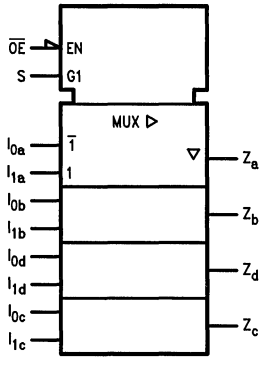
IEEE/IEC



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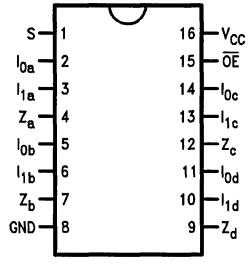
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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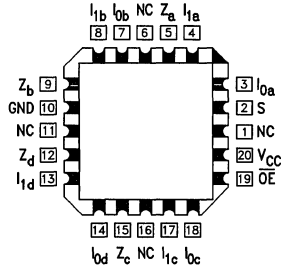
Pin Assignment for LCC



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Pin Names	Description
S	Common Data Select Input
$\overline{OE}$	TRI-STATE Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
Z_a–Z_d	TRI-STATE Multiplexer Outputs

Functional Description

The 'AC/'ACT257 is quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

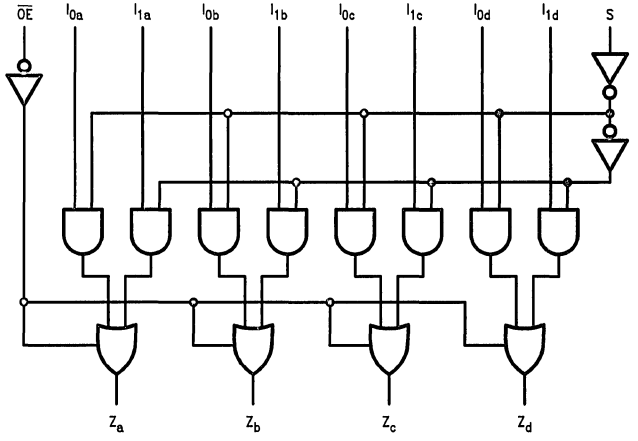
When the Output Enable ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.5	5.0	8.5	1.0	11.0	1.0	9.0	ns	2-3,4
		5.0	1.5	4.0	6.0	1.0	8.0	1.0	7.0		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.5	6.0	8.5	1.0	11.0	1.0	9.0	ns	2-3,4
		5.0	1.5	4.5	6.0	1.0	8.5	1.0	7.0		
t_{PLH}	Propagation Delay S to Z_n	3.3	1.5	7.0	10.5	1.0	14.5	1.5	11.5	ns	2-3,4
		5.0	1.5	5.0	7.5	1.0	11.0	1.0	8.5		
t_{PHL}	Propagation Delay S to Z_n	3.3	1.5	7.5	10.5	1.0	14.5	1.5	11.5	ns	2-3,4
		5.0	1.5	5.5	7.5	1.0	11.0	1.0	8.5		
t_{PZH}	Output Enable Time	3.3	1.5	6.5	9.5	1.0	13.0	1.0	10.5	ns	2-5
		5.0	1.5	5.0	7.5	1.0	10.0	1.0	8.5		
t_{PZL}	Output Enable Time	3.3	1.5	5.5	9.0	1.0	11.0	1.0	10.0	ns	2-6
		5.0	1.5	5.0	8.5	1.0	9.5	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	1.5	5.5	10.0	1.0	13.0	1.0	11.0	ns	2-5
		5.0	1.5	5.0	9.0	1.0	11.0	1.0	10.0		
t_{PLZ}	Output Disable Time	3.3	1.5	5.5	9.0	1.0	10.5	1.0	10.0	ns	2-6
		5.0	1.5	5.0	8.0	1.0	9.5	1.0	9.0		

*Voltage Range 3.3 is 3.0V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.5	5.0	7.0	1.0	8.0	1.0	7.5	ns	2-3,4
t_{PHL}	Propagation Delay I_n to Z_n	5.0	2.0	6.0	7.5	1.0	9.5	1.5	8.5	ns	2-3,4
t_{PLH}	Propagation Delay S to Z_n	5.0	2.0	7.0	9.5	1.0	11.0	1.5	10.5	ns	2-3,4
t_{PHL}	Propagation Delay S to Z_n	5.0	2.5	7.0	10.5	1.0	11.5	2.0	11.5	ns	2-3,4
t_{PZH}	Output Enable Time	5.0	2.0	6.0	8.0	1.0	9.5	1.5	9.0	ns	2-5
t_{PZL}	Output Enable Time	5.0	2.0	6.0	8.0	1.0	9.5	1.5	9.0	ns	2-6
t_{PHZ}	Output Disable Time	5.0	2.5	6.5	9.0	1.0	10.5	1.5	10.0	ns	2-5
t_{PLZ}	Output Disable Time	5.0	2.0	6.0	7.5	1.0	9.0	1.5	8.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC258 • 54ACT/74ACT258
Quad 2-Input Multiplexer with TRI-STATE® Outputs

General Description

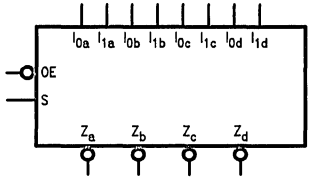
The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

Features

- Multiplexer expansion by tying outputs together
- Inverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT258 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'ACT258: 5962-88704

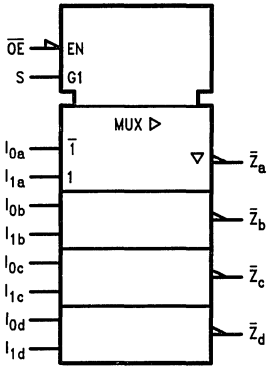
Ordering Code: See Section 8

Logic Symbols



TL/F/9950–1

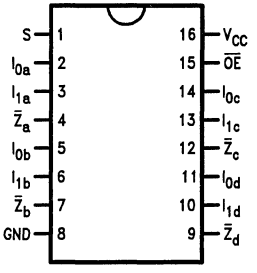
IEEE/IEC



TL/F/9950–2

Connection Diagrams

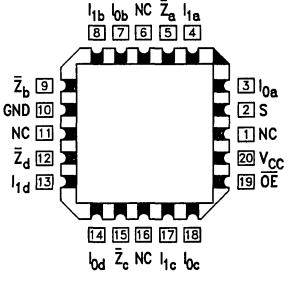
Pin Assignment for DIP, Flatpak and SOIC



TL/F/9950–3

Pin Names	Description
S	Common Data Select Input
$\overline{OE}$	TRI-STATE Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
$\overline{Z}_a$–$\overline{Z}_d$	TRI-STATE Inverting Data Outputs

Pin Assignment for LCC



TL/F/9950–4

Functional Description

The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'AC/'ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$\overline{Z}_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z}_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$\overline{Z}_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

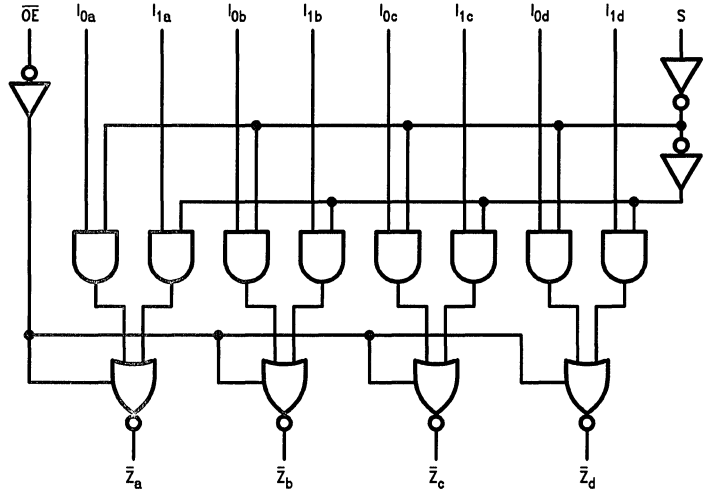
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



TL/F/9950–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3	2.0	6.0	9.5	1.0	12.0	1.5	11.0	ns	2-3, 4
		5.0	1.5	4.5	7.5	1.0	9.5	1.0	8.5		
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3	2.0	5.0	8.5	1.0	10.5	1.5	9.5	ns	2-3, 4
		5.0	1.5	4.0	6.5	1.0	7.5	1.0	7.0		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3	3.0	7.5	12.0	1.0	15.0	2.5	14.0	ns	2-3, 4
		5.0	2.0	6.0	9.5	1.0	11.5	1.5	10.5		
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3	2.5	7.5	11.5	1.0	14.0	2.0	13.0	ns	2-3, 4
		5.0	1.5	5.5	9.0	1.0	10.5	1.5	10.0		
t_{PZH}	Output Enable Time	3.3	2.5	6.0	9.5	1.0	11.5	2.0	10.5	ns	2-5
		5.0	1.5	4.5	7.5	1.0	9.0	1.5	8.5		
t_{PZL}	Output Enable Time	3.3	2.0	5.5	9.0	1.0	10.5	1.5	10.0	ns	2-6
		5.0	1.5	5.5	7.0	1.0	8.5	1.0	8.0		
t_{PHZ}	Output Disable Time	3.3	2.5	5.5	10.0	1.0	11.5	2.0	11.0	ns	2-5
		5.0	2.0	5.5	8.5	1.0	9.5	1.5	9.0		
t_{PLZ}	Output Disable Time	3.3	2.0	5.5	9.0	1.0	10.5	2.0	10.0	ns	2-6
		5.0	1.5	5.0	7.0	1.0	8.5	1.5	8.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	2.0	6.5	8.5	1.0	10.5	1.5	9.5	ns	2-3, 4
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	2.0	5.5	7.5	1.0	9.0	1.5	8.0	ns	2-3, 4
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	3.0	7.5	10.5	1.0	13.0	2.0	11.5	ns	2-3, 4
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.5	7.0	9.5	1.0	12.0	1.5	11.0	ns	2-3, 4
t_{PZH}	Output Enable Time	5.0	2.0	6.5	8.5	1.0	10.5	1.5	9.5	ns	2-5
t_{PZL}	Output Enable Time	5.0	2.0	6.5	8.5	1.0	10.0	1.5	9.5	ns	2-6
t_{PHZ}	Output Disable Time	5.0	1.5	7.0	9.0	1.0	10.5	1.0	10.0	ns	2-5
t_{PLZ}	Output Disable Time	5.0	2.0	6.0	8.0	1.0	10.0	1.5	9.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	55.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC273
Octal D Flip-Flop

General Description

The 'AC273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

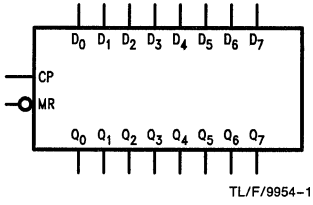
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- See '377 for clock enable version
- See '373 for transparent latch version
- See '374 for TRI-STATE version
- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
  — 'AC273: 5962-87756

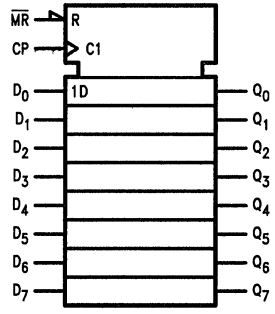
Ordering Code: See Section 8

Logic Symbols



TL/F/9954–1

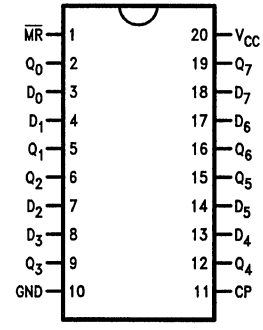
IEEE/IEC



TL/F/9954–2

Connection Diagrams

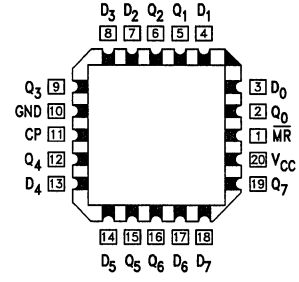
Pin Assignment for DIP, Flatpak and SOIC



TL/F/9954–3

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

Pin Assignment for LCC



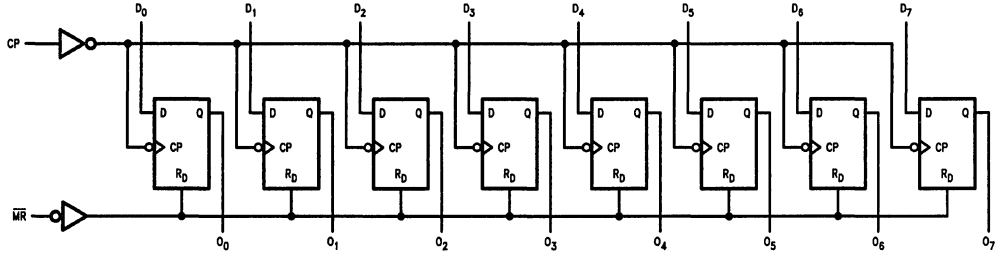
TL/F/9954–4

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/9954–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5 to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
f_{max}	Maximum Clock Frequency	3.3	90	125		75		75		MHz	
		5.0	140	175		90		125			
t_{PLH}	Propagation Delay Clock to Output	3.3	4.0	7.0	12.5	1.0	15.0	3.0	14.0	ns	2-3, 4
		5.0	3.0	5.5	9.0	1.0	11.0	2.5	10.0		
t_{PHL}	Propagation Delay Clock to Output	3.3	4.0	7.0	13.0	1.0	16.0	3.5	14.5	ns	2-3, 4
		5.0	3.0	5.0	10.0	1.0	11.5	2.5	11.0		
t_{PHL}	Propagation Delay $\overline{MR}$ to Output	3.3	4.0	7.0	13.0	1.0	16.0	3.5	14.0	ns	2-3, 4
		5.0	3.0	5.0	10.0	1.0	11.5	2.5	10.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF Typ	74AC $T_A = +25°C$, $C_L = 50$ pF Guaranteed Minimum	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
t_s	Setup Time, HIGH or LOW Data to CP	3.3	3.5	5.5	8.0	6.0	ns	2-7
		5.0	2.5	4.0	5.0	4.5		
t_h	Hold Time, HIGH or LOW Data to CP	3.3	−2.0	0	0	0	ns	2-7
		5.0	−1.0	1.0	1.0	1.0		
t_w	Clock Pulse Width HIGH or LOW	3.3	3.5	5.5	6.5	6.0	ns	2-3
		5.0	2.5	4.0	5.0	4.5		
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	3.3	2.0	5.5	10.0	6.0	ns	2-3
		5.0	1.5	4.0	6.5	4.5		
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3	1.5	3.5	6.0	4.5	ns	2-3, 7
		5.0	1.0	2.0	4.0	3.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC280
9-Bit Parity Generator/Checker

General Description

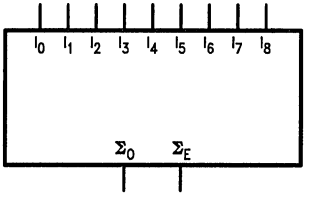
The 'AC280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

Features

- 9-bit width for memory applications

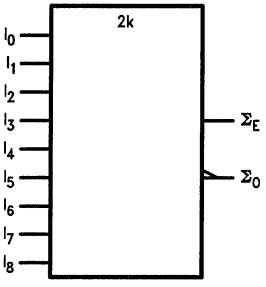
Ordering Code: See Section 8

Logic Symbols



TL/F/9955–1

IEEE/IEC

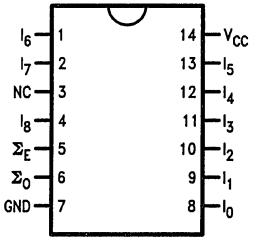


TL/F/9955–4

Pin Names	Description
I_0–I_8	Data Inputs
Σ_O	Odd Parity Output
Σ_E	Even Parity Output

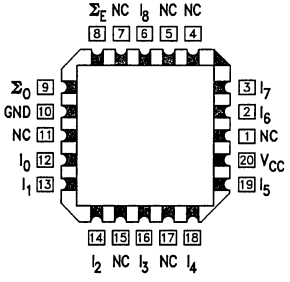
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/9955–2

Pin Assignment for LCC



TL/F/9955–3

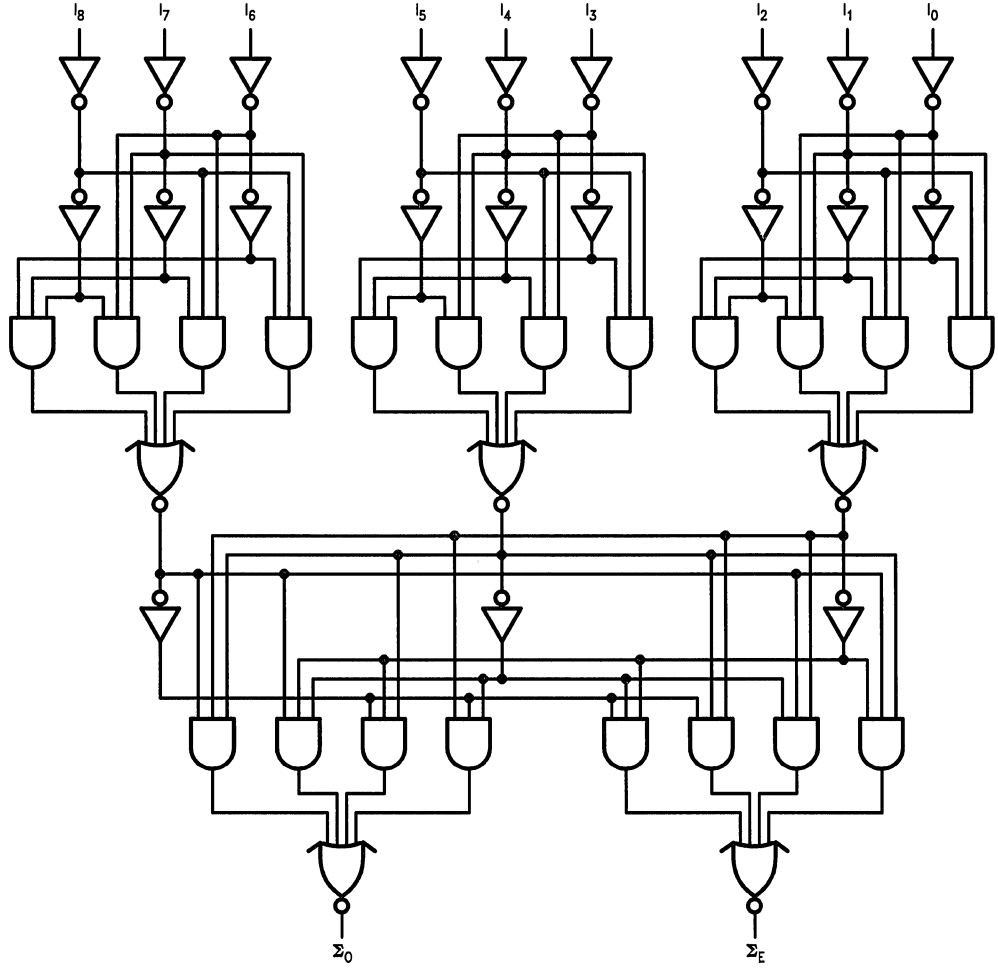
Truth Table

Number of HIGH Inputs I_0–I_8	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level

L = LOW Voltage Level

Logic Diagram



TL/F/9955–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} + 0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} + 0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'AC Devices
V_{IN} from 30% to 70% of V_{CC}
V_{CC} @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'ACT Devices
V_{IN} from 0.8V to 2.0V
V_{CC} @ 4.5V, 5.5V 125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$	74AC $T_A = -55°C$ to $+125°C$	54AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.76		
		5.5		4.86	4.76		I_{OH} −24 mA
							I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50		
		5.5		0.36	0.50		I_{OL} 24 mA
							I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74 AC @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	5.0	10.5	17.0	1.0	20.0	4.0	18.5	ns	2-3, 4
t_{PHL}	I_n to Σ_E	5.0	3.0	7.5	13.0	1.5	14.5	2.0	14.5		
t_{PLH}	Propagation Delay	3.3	5.0	12.0	17.0	1.0	20.0	4.0	18.5	ns	2-3, 4
t_{PHL}	I_n to Σ_O	5.0	3.0	8.5	13.0	1.5	14.5	2.0	14.5		

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	75.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC299 • 54ACT/74ACT299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

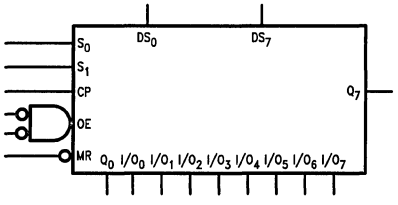
The 'AC/'ACT299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0, Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT299 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC299: 5962-88754
  - — 'ACT299: 5962-88771

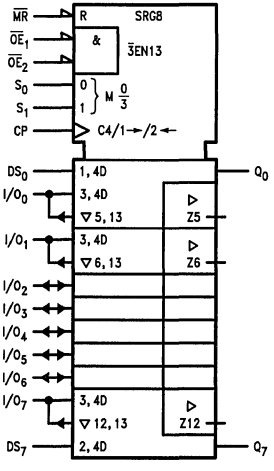
Ordering Code: See Section 8

Logic Symbols



TL/F/9893–1

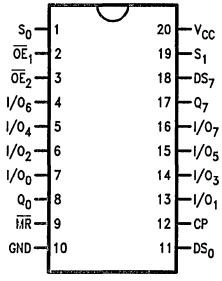
IEEE/IEC



TL/F/9893–4

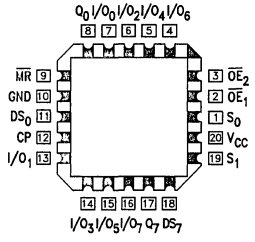
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9893–2

Pin Assignment for LCC



TL/F/9893–3

Pin Names	Description
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I/O_0–I/O_7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q_0, Q_7	Serial Outputs

Functional Description

The 'AC/'ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Truth Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

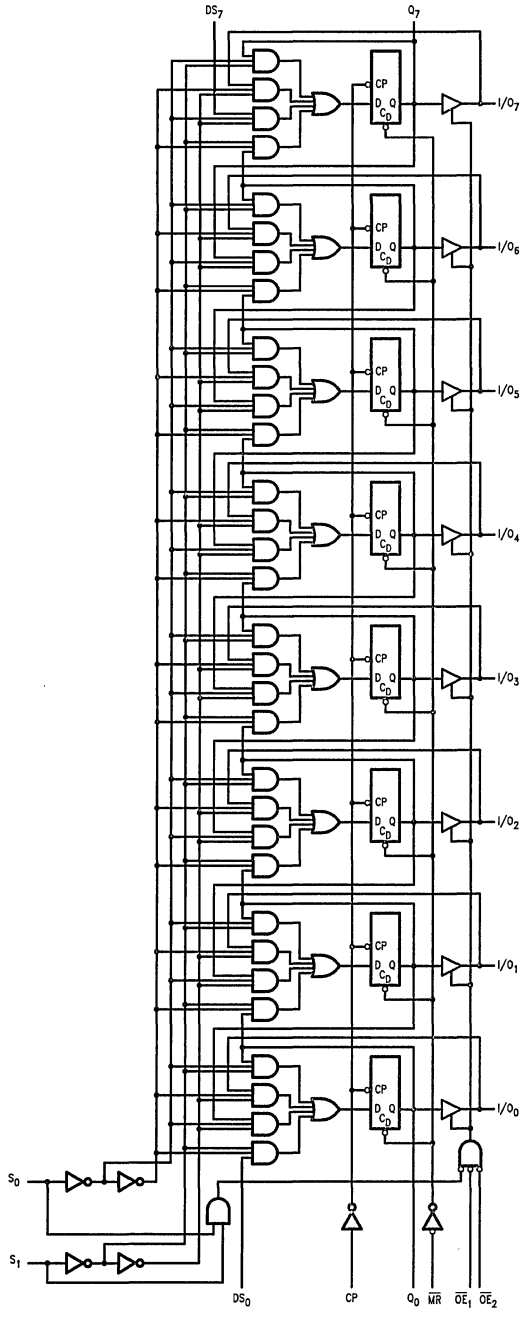
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Truth Table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	↗	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↗	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↗	Shift Left, $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Logic Diagram



TL/F/9893–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
(Unless Otherwise Specified)	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.0V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics For 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.7	3.76		I_{OH} −12 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
								I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.50	0.44		I_{OH} 12 mA
		5.5		0.36	0.50	0.44		I_{OH} 24 mA
								24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I(OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; threshold on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

DC Electrical Characteristics For 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = 25°C$ Typ	74AC $T_A = 25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			57	86	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

*All outputs loaded; threshold on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Electrical Characteristics For 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = 25°C$ Typ	74ACT $T_A = 25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5	0.0001	3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.5V
C_{PD}	Power Dissipation Capacitance	170	pF	V_{CC} = 5.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	3.3 5.0	90 130	124 173		70 80		80 105		MHz	
t_{PLH}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	3.3 5.0	8.5 5.5	14.0 9.5	20.5 14.0	1.0 1.0	25.5 17.5	7.0 4.5	22.0 15.0	ns	2–3, 4
t_{PHL}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	3.3 5.0	8.5 5.5	14.5 10.0	21.5 14.5	1.0 1.0	26.5 18.0	7.0 5.0	23.0 16.0	ns	2–3, 4
t_{PLH}	Propagation Delay $\overline{CP}$ to I/O_n	3.3 5.0	9.0 6.0	14.5 10.0	20.5 14.5	1.0 1.0	24.5 17.0	7.5 5.0	22.5 16.0	ns	2–3, 4
t_{PHL}	Propagation Delay $\overline{CP}$ to I/O_n	3.3 5.0	10.0 6.5	16.0 11.0	23.0 16.0	1.0 1.0	26.5 18.5	8.5 6.0	24.5 17.5	ns	2–3, 4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	3.3 5.0	9.0 5.5	15.5 10.5	22.5 15.5	1.0 1.0	27.0 18.5	7.5 5.0	25.0 17.0	ns	2–3, 4
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	3.3 5.0	9.0 5.5	15.0 10.0	21.5 15.0	1.0 1.0	26.5 18.0	7.5 5.0	24.0 16.5	ns	2–3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0	7.0 4.5	12.0 8.5	18.0 12.5	1.0 1.0	22.0 15.0	6.0 4.0	19.5 13.5	ns	2–5
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0	7.0 5.0	12.5 8.0	18.0 12.5	1.0 1.0	23.5 16.0	6.0 4.0	20.5 14.0	ns	2–6
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0	6.5 3.5	13.0 9.5	18.5 14.0	1.0 1.0	22.5 17.0	5.5 3.0	19.5 15.0	ns	2–5
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0	5.5 3.5	11.5 8.0	17.0 12.5	1.0 1.0	21.5 16.0	4.5 2.0	19.0 13.5	ns	2–6

*Voltage Range 3.3 is 3.3V ±0.3V.
Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	3.0 2.0	8.0 5.0	9.5 7.0	8.5 5.5	ns	2–7
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	−3.0 −1.5	0.5 1.0	2.0 2.5	0.5 1.0	ns	2–7
t_s	Setup Time, HIGH or LOW I/O_n to CP	3.3 5.0	2.0 1.0	5.5 3.5	6.0 4.0	6.0 4.0	ns	2–7
t_h	Hold Time, HIGH or LOW I/O_n to CP	3.3 5.0	−2.0 −1.0	0 1.0	1.5 2.0	0 1.0	ns	2–7
t_s	Setup Time, HIGH or LOW DS_0 or DS_7 to CP	3.3 5.0	2.5 1.5	6.5 4.0	7.5 5.0	7.0 4.5	ns	2–7
t_h	Hold Time, HIGH or LOW DS_0 or DS_7 to CP	3.3 5.0	−2.0 −1.0	0 1.0	1.5 1.5	0.5 1.0	ns	2–7
t_w	CP Pulse Width, LOW	3.3 5.0	3.5 2.0	4.5 3.5	5.5 5.0	5.0 3.5	ns	2–3
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	4.0 2.0	4.5 3.5	5.5 5.0	5.0 3.5	ns	2–3
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0.5	1.5 1.5	2.5 2.5	1.5 1.5	ns	2–3, 7

*Voltage Range 3.3 is 3.3V ±0.3V
*Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0	120	170		70		110		MHz	
t_{PLH}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	8.5	12.5	1.0	15.5	3.0	14.0	ns	2–3, 4
t_{PHL}	Propagation Delay CP to Q_0 or Q_7 (Shift Left or Right)	5.0	4.0	9.0	13.5	1.0	16.0	3.5	15.0	ns	2–3, 4
t_{PLH}	Propagation Delay CP to I/O_n	5.0	4.5	8.5	12.5	1.0	15.0	4.5	13.5	ns	2–3, 4
t_{PHL}	Propagation Delay CP to I/O_n	5.0	5.0	9.5	15.0	1.0	18.0	4.5	16.5	ns	2–3, 4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0	4.0	14.0	15.0	1.0	18.0	4.0	18.0	ns	2–3, 4
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	5.0	4.0	13.0	14.5	1.0	17.5	3.5	17.5	ns	2–3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	5.0	2.5	8.0	12.0	1.0	14.0	1.5	13.0	ns	2–5
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	5.0	2.0	8.0	12.0	1.0	14.5	1.5	13.5	ns	2–6
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	2.5	2.0	8.5	12.5	1.0	14.5	2.0	13.5	ns	2–5
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	2.0	2.5	8.0	11.5	1.0	14.0	2.0	12.5	ns	2–6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	6.5	5.5	ns	2–7
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	−2.0	1.0	1.5	1.0	ns	2–7
t_s	Setup Time, HIGH or LOW I/O_n to CP	5.0	1.5	4.0	4.5	4.5	ns	2–7
t_h	Hold Time, HIGH or LOW I/O_n to CP	5.0	−1.0	1.0	1.5	1.0	ns	2–7
t_s	Setup Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	1.5	4.5	5.5	5.0	ns	2–7
t_h	Hold Time, HIGH or LOW DS_0 or DS_7 to CP	5.0	−1.0	1.0	1.5	1.0	ns	2–7
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	5.0	4.5	ns	2–3
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	2.0	3.5	5.0	3.5	ns	2–3
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	1.5	1.5	1.5	ns	2–3, 7

*Voltage Range 5.0 is 5.0V ±0.5V.

National Semiconductor

54ACT/74ACT323
8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

General Description

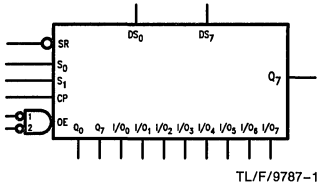
The 'ACT323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbols



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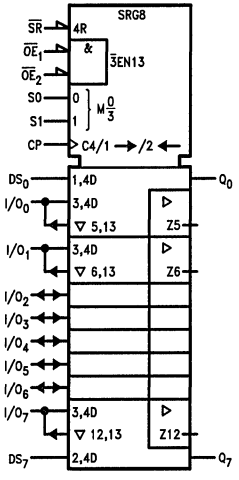

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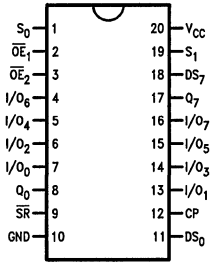
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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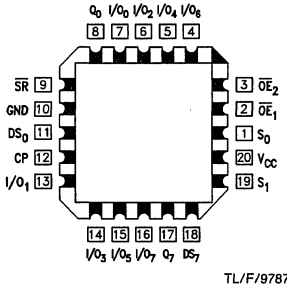
Pin Assignment for LCC



TL/F/9787–3

Pin Name	Description
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{SR}$	Synchronous Reset Input
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I/O_0–I/O_7	Multiplexed Parallel Data Inputs or TRI-STATE Parallel Data Outputs
Q_0, Q_7	Serial Outputs

Functional Description

The 'ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP.

Mode Select Table

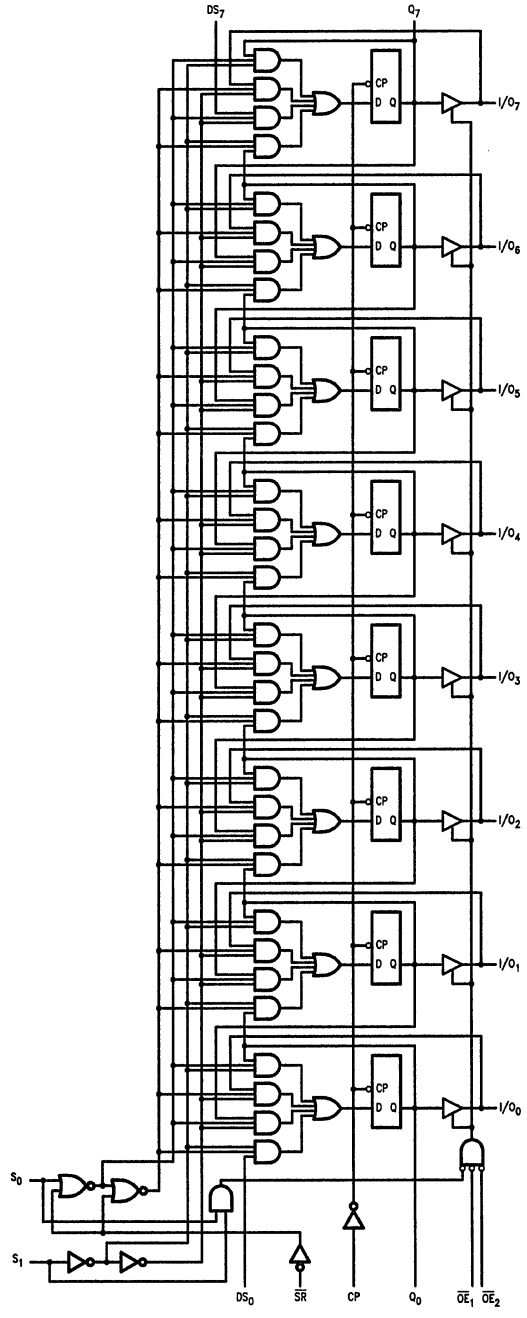
Inputs				Response
$\overline{SR}$	S_1	S_0	CP	
L	X	X	⌐	Synchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics For 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} −24 mA −24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	$V_{I/O}$ = V_{CC} or GND V_{IN} = V_{IH}, V_{IL}
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = 25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0	120	125		95		110		MHz	
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	12.5	1.0	16.5	4.0	14.0	ns	2-3, 4
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	13.5	1.0	17.0	4.5	15.0	ns	2-3, 4
t_{PLH}	Propagation Delay CP to I/O_n	5.0	5.0	8.5	12.5	1.0	16.5	4.5	14.5	ns	2-3, 4
t_{PHL}	Propagation Delay CP to I/O_n	5.0	6.0	10.0	14.5	1.0	18.0	5.0	16.0	ns	2-3, 4
t_{PZH}	Output Enable Time	5.0	3.5	7.5	11.0	1.0	15.0	3.0	12.5	ns	2-5
t_{PZL}	Output Enable Time	5.0	3.5	7.5	11.5	1.0	15.5	3.0	13.0	ns	2-6
t_{PHZ}	Output Disable Time	5.0	4.0	8.5	12.5	1.0	15.5	3.0	13.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	3.0	8.0	11.5	1.0	15.0	2.5	12.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = 25°C$, $C_L = 50$ pF, $V_{CC} = +5.0V$		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF, $V_{CC} = +5.0V$	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $V_{CC} = +5.0V$	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	6.0	5.0	ns	2-7
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0	1.5	1.5	1.5	ns	2-7
t_s	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	1.0	4.0	4.5	4.5	ns	2-7
t_h	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	0	1.0	1.0	1.0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	1.0	2.5	3.0	2.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	0	1.0	1.0	1.0	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	5.0	4.5	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	170	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACT/74ACT367
Hex Buffer with TRI-STATE® Outputs

General Description

The 'ACT367 contains six independent non-inverting buffers with TRI-STATE outputs.

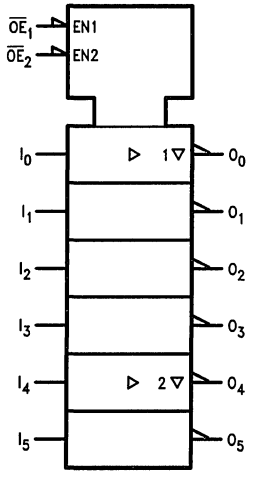
Features

- Outputs source/sink 24 mA
- 'ACT has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbol

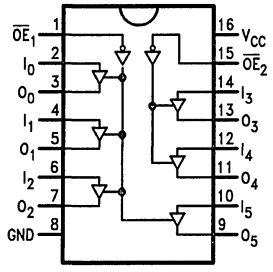
IEEE/IEC



TL/F/10691–1

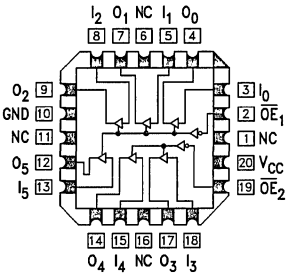
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/10691–2

Pin Assignment for LCC and PCC



TL/F/10691–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active LOW)
I_n	Input
O_n	Output

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

Function Table

Inputs		Outputs
$\overline{OE}$	I	O
L	L	H
L	H	L
H	X	Z

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V††
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C

††May be measured per the JEDEC alternate method.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	6.5	9.0			1.0	10.0	ns	2-3, 4
t_{PHL}	Propagation Delay	5.0	1.0	6.5	9.0			1.0	10.0	ns	2-3, 4
t_{PZH}	Output Enable Time	5.0	1.0	8.0	10.5			1.0	11.0	ns	2-5
t_{PZL}	Output Enable Time	5.0	1.0	9.5	12.0			1.0	13.0	ns	2-6
t_{PHZ}	Output Disable Time	5.0	1.0	9.5	12.0			1.0	13.0	ns	2-5
t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.5			1.0	11.5	ns	2-6

*Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACT/74ACT368
Hex Inverter Buffer with TRI-STATE® Outputs

General Description

The 'ACT368 contains six independent inverting buffers with TRI-STATE outputs.

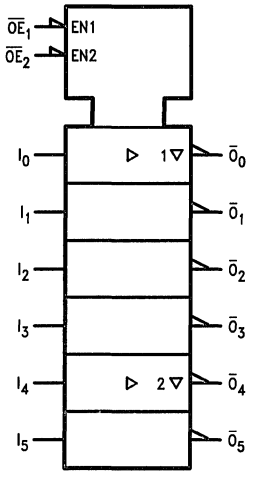
Features

- Outputs source/sink 24 mA
- 'ACT has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbols

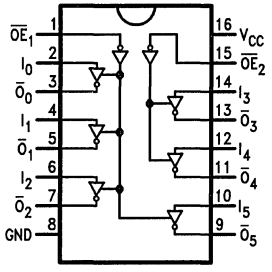
IEE/IEC



TL/F/10690–1

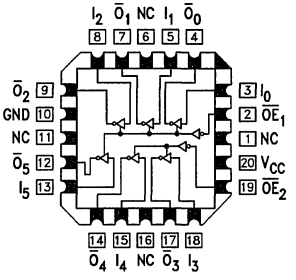
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/10690–2

Pin Assignment for LCC and PCC



TL/F/10690–3

Function Table

Inputs		Output
$\overline{OE}$	I	$\overline{O}$
L	L	H
L	H	L
H	X	Z

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active LOW)
	Input
$\overline{O}_n$	Output

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$ ††
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

††May be measured per the JEDEC Alternate Method.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	6.5	9.0			1.0	10.0	ns	2–3, 4
t_{PHL}	Propagation Delay	5.0	1.0	6.0	9.0			1.0	10.0	ns	2–3, 4
t_{PZH}	Output Enable Time	5.0	1.0	8.0	10.0			1.0	11.0	ns	2–5
t_{PZL}	Output Enable Time	5.0	1.0	8.0	12.0			1.0	13.0	ns	2–6
t_{PHZ}	Output Disable Time	5.0	1.0	9.0	12.0			1.0	13.0	ns	2–5
t_{PLZ}	Output Disable Time	5.0	1.0	8.5	11.0			1.0	12.0	ns	2–6

*Voltage Range 5.0 is 5.0V ±0.5V.

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC373 • 54ACT/74ACT373
Octal Transparent Latch with TRI-STATE® Outputs

General Description

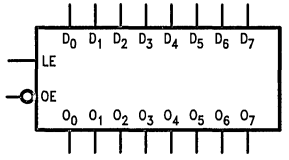
The 'AC/'ACT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Features

- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT373 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - '—' 'AC373: 5962-87555
  - '—' 'ACT373: 5962-87556

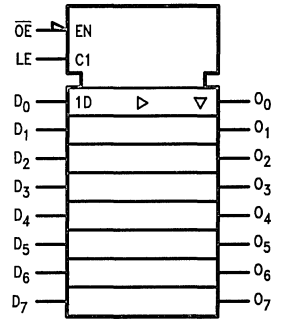
Ordering Code: See Section 8

Logic Symbols



TL/F/9958–1

IEEE/IEC

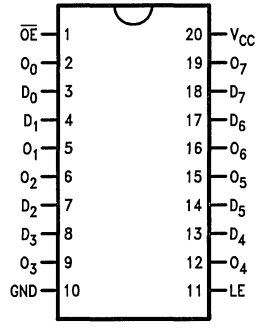


TL/F/9958–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

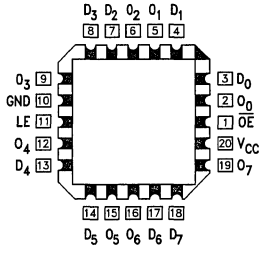
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9958–3

Pin Assignment for LCC



TL/F/9958–4

Functional Description

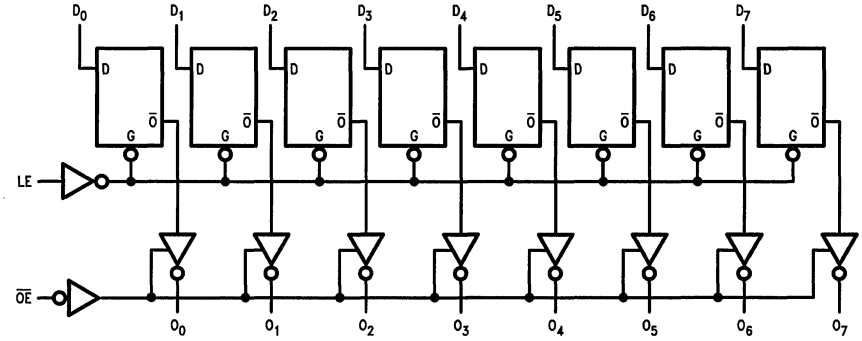
The 'AC/'ACT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/9958–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded, thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3	1.5	10.0	13.5	1.0	16.5	1.5	15.0	ns	2-3, 4
		5.0	1.5	7.0	9.5	1.0	11.5	1.5	10.5		
t_{PHL}	Propagation Delay D_n to O_n	3.3	1.5	9.5	13.0	1.0	16.0	1.5	14.5	ns	2-3, 4
		5.0	1.5	7.0	9.5	1.0	11.5	1.5	10.5		
t_{PLH}	Propagation Delay LE to O_n	3.3	1.5	10.0	13.5	1.0	16.5	1.5	15.0	ns	2-3, 4
		5.0	1.5	7.5	9.5	1.0	12.0	1.5	10.5		
t_{PHL}	Propagation Delay LE to O_n	3.3	1.5	9.5	12.5	1.0	15.0	1.5	14.0	ns	2-3, 4
		5.0	1.5	7.0	9.5	1.0	11.0	1.5	10.5		
t_{PZH}	Output Enable Time	3.3	1.5	9.0	11.5	1.0	14.0	1.0	13.0	ns	2-5
		5.0	1.5	7.0	8.5	1.0	10.5	1.0	9.5		
t_{PZL}	Output Enable Time	3.3	1.5	8.5	11.5	1.0	13.5	1.0	13.0	ns	2-6
		5.0	1.5	6.5	8.5	1.0	10.0	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	1.5	10.0	12.5	1.0	16.0	1.0	14.5	ns	2-5
		5.0	1.5	8.0	11.0	1.0	13.5	1.0	12.5		
t_{PLZ}	Output Disable Time	3.3	1.5	8.0	11.5	1.0	13.0	1.0	12.5	ns	2-6
		5.0	1.5	6.5	8.5	1.0	10.5	1.0	10.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3	3.5	5.5	6.5	6.0	ns	2-7
		5.0	2.0	4.0	5.0	4.5		
t_h	Hold Time, HIGH or LOW D_n to LE	3.3	−3.0	1.0	1.0	1.0	ns	2-7
		5.0	−1.5	1.0	1.0	1.0		
t_w	LE Pulse Width, HIGH	3.3	4.0	5.5	6.5	6.0	ns	2-3
		5.0	2.0	4.0	5.0	4.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	2.5	8.5	10.0	1.0	12.5	1.5	11.5	ns	2-3, 4
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.0	8.0	10.0	1.0	12.5	1.5	11.5	ns	2-3, 4
t_{PLH}	Propagation Delay LE to O_n	5.0	2.5	8.5	11.0	1.0	12.5	2.0	11.5	ns	2-3, 4
t_{PHL}	Propagation Delay LE to O_n	5.0	2.0	8.0	10.0	1.0	11.5	1.5	11.5	ns	2-3, 4
t_{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.0	11.5	1.5	10.5	ns	2-5
t_{PZL}	Output Enable Time	5.0	2.0	7.5	9.0	1.0	11.0	1.5	10.5	ns	2-6
t_{PHZ}	Output Disable Time	5.0	2.5	9.0	11.0	1.0	14.0	2.5	12.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	1.5	7.5	8.5	1.0	11.0	1.0	10.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	3.0	7.0	8.5	8.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0	0	1.0	1.0	ns	2-7
t_w	LE Pulse Width, HIGH	5.0	2.0	7.0	8.5	8.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC374 • 54ACT/74ACT374
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

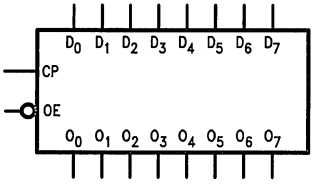
The 'AC/'ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- See '273 for reset version
- See '377 for clock enable version
- See '373 for transparent latch version
- See '574 for broadside pinout version
- See '564 for broadside pinout version with inverted outputs
- 'ACT374 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC374: 5962-87694
  - — 'ACT374: 5962-87631

Ordering Code: See Section 8

Logic Symbols



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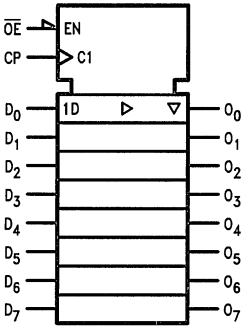
IEEE/IEC



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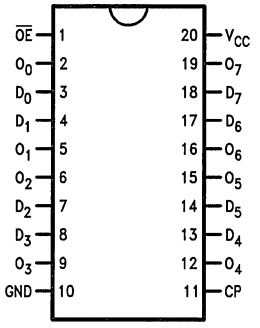
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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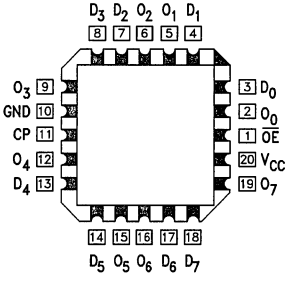
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Pin Assignment for LCC and PCC



TL/F/9959–4

Functional Description

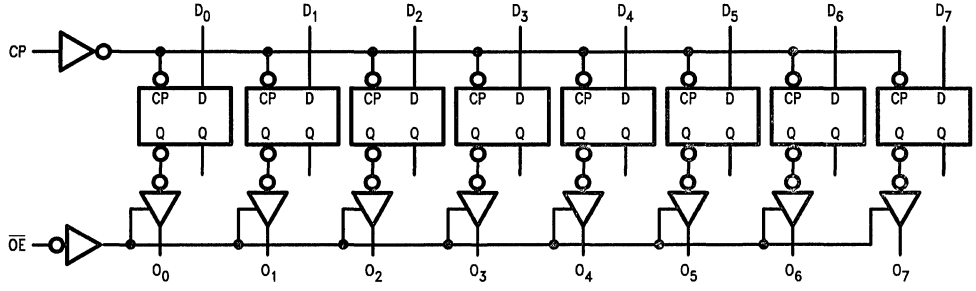
The 'AC/'ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐‾	L	H
L	⌐‾	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐‾ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	60 100	110 155		60 95		60 100		MHz	
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0	3.0 2.5	11.0 8.0	13.5 9.5	1.0 1.0	16.5 12.0	1.5 1.5	15.5 10.5	ns	2-3, 4
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0	2.5 2.0	10.0 7.0	12.5 9.0	1.0 1.0	15.0 11.0	2.0 1.5	14.0 10.0	ns	2-3, 4
t_{PZH}	Output Enable Time	3.3 5.0	3.0 2.0	9.5 7.0	11.5 8.5	1.0 1.0	14.0 10.5	1.5 1.0	13.0 9.5	ns	2-5
t_{PZL}	Output Enable Time	3.3 5.0	2.5 2.0	9.0 6.5	11.5 8.5	1.0 1.0	14.0 10.5	1.5 1.0	13.0 9.5	ns	2-6
t_{PHZ}	Output Disable Time	3.3 5.0	3.0 2.0	10.5 8.0	12.5 11.0	1.0 1.0	16.0 12.5	2.0 2.0	14.5 12.5	ns	2-5
t_{PLZ}	Output Disable Time	3.3 5.0	2.0 1.5	8.0 6.5	11.5 8.5	1.0 1.0	13.0 10.5	1.0 1.0	12.5 10.0	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0	5.5 4.0	6.5 5.0	6.0 4.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 0	1.0 1.5	1.0 1.5	1.0 1.5	ns	2-7
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	4.0 2.5	5.5 4.0	6.5 5.0	6.0 4.5	ns	2-3

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	100	160		70		90		MHz	
t_{PLH}	Propagation Delay CP to O_n	5.0	2.0	8.5	10.0	1.0	12.0	2.0	11.5	ns	2-3, 4
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	8.0	9.5	1.0	11.5	1.5	11.0	ns	2-3, 4
t_{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.0	11.5	1.5	10.5	ns	2-5
t_{PZL}	Output Enable Time	5.0	1.5	8.0	9.0	1.0	11.5	1.5	10.5	ns	2-6
t_{PHZ}	Output Disable Time	5.0	1.5	8.5	11.5	1.0	13.0	1.0	12.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	1.5	7.0	8.5	1.0	11.0	1.0	10.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	5.0	8.5	5.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5	1.5	1.5	ns	2-7
t_w	CP Pulse Width, HIGH or LOW	5.0	2.5	5.0	8.5	5.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	80.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC377 • 54ACT/74ACT377
Octal D Flip-Flop with Clock Enable

General Description

The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

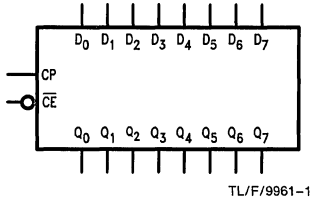
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- 'ACT377 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC377: 5962-88702
  - — 'ACT377: 5962-87697

Ordering Code: See Section 8

Logic Symbols



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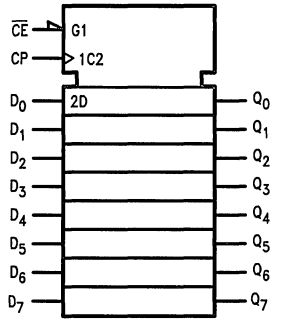
IEEE/IEC



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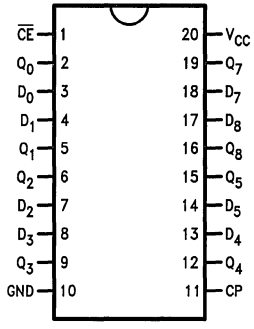
Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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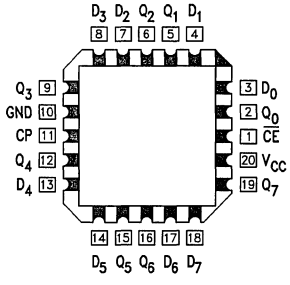
Pin Assignment for LCC



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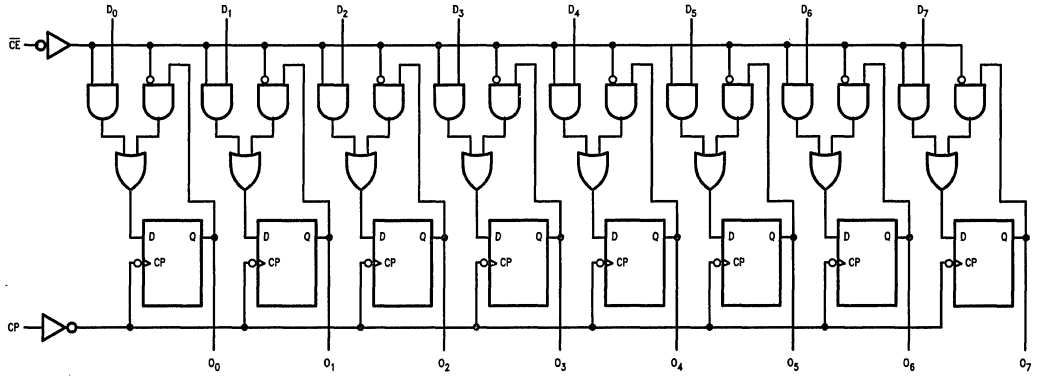
Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load '1'	⌐	L	H	H
Load '0'	⌐	L	L	L
Hold (Do Nothing)	⌐	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175		75 95		75 125		MHz	
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	3.0 2.0	8.0 6.0	13.0 9.0	1.0 1.0	14.0 10.0	1.5 1.5	14.0 10.0	ns	2-3, 4
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	3.5 2.5	8.5 6.5	13.0 10.0	1.0 1.0	15.0 11.0	2.0 1.5	14.5 11.0	ns	2-3, 4

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	3.5 2.5	5.5 4.0	7.5 6.0	6.0 4.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−2.0 −1.0	0 1.0	1.5 2.5	0 1.0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0	4.0 2.5	6.0 4.0	9.5 6.0	7.5 4.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0	−3.5 −2.0	0 1.0	1.0 2.0	0 1.0	ns	2-7
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0	6.5 5.0	6.0 4.5	ns	2-3

*Voltage Range 3.3 is 3.0V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	140	175		85		125		MHz	
t_{PLH}	Propagation Delay CP to Q_n	5.0	3.0	6.5	9.0	1.0	11.0	2.5	10.0	ns	2-3, 4
t_{PHL}	Propagation Delay CP to Q_n	5.0	3.5	7.0	10.0	1.0	12.0	2.5	11.0	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.5	4.5	7.0	5.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−1.0	1.0	1.0	1.0	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	5.0	2.5	4.5	7.0	5.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	5.0	−1.0	1.0	1.0	1.0	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	5.5	4.5	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	90.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC378
Parallel D Register with Enable

General Description

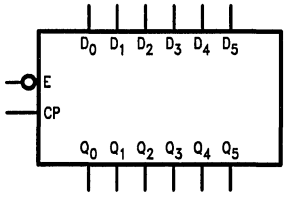
The 'AC378 is a 6-bit register with a buffered common Enable. This device is similar to the 'AC174, but with common Enable rather than common Master Reset.

Features

- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high-speed termination effects

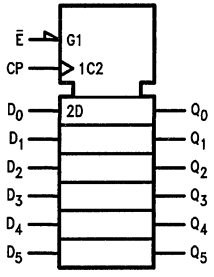
Ordering Code: See Section 8

Logic Symbols



TL/F/10231–1

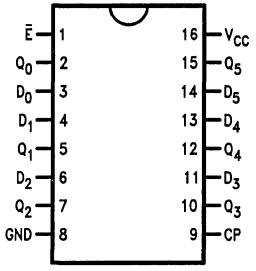
IEEE/IEC



TL/F/10231–4

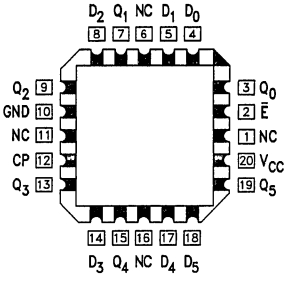
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/10231–2

Pin Assignment for LCC



TL/F/10231–3

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D_0–D_5	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q_0–Q_5	Outputs

Functional Description

The 'AC378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q inputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

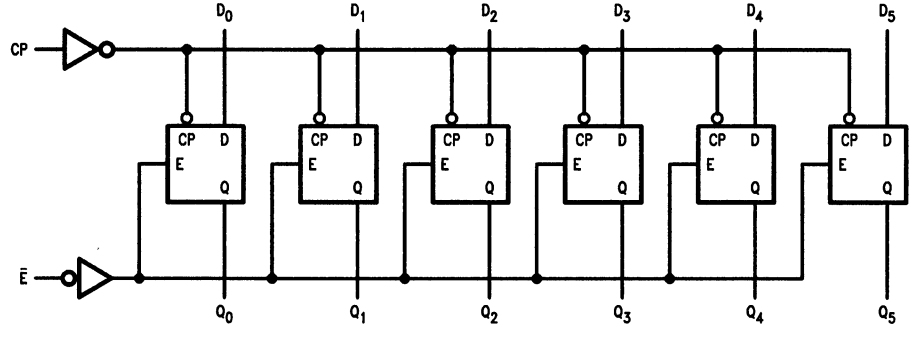
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

Truth Table

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	⌐	X	No Change
L	⌐	H	H
L	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/10231–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.5	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.5	0.44		I_{OL} 24 mA
		5.5		0.36	0.5	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			54AC T_A = −55°C to +125°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3	125	160		95		110		MHz	
		5.0	160	200		95		145			
t_{PLH}	Propagation Delay CP to Q_n	3.3	2.5	8.5	11.0	1.5	12.0	2.5	12.5	ns	2–3, 4
		5.0	1.5	6.0	8.0	1.5	9.0	1.5	9.0		
t_{PHL}	Propagation Delay CP to Q_n	3.3	2.5	8.0	10.5	1.5	12.0	2.5	11.0	ns	2–3, 4
		5.0	1.5	5.5	7.5	1.5	7.5	1.5	8.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		54AC T_A = −55°C to +125°C, C_L = 50 pF	74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3	1.5	3.0	4.0	3.5	ns	2–7
		5.0	1.0	2.0	4.0	2.5		
t_h	Hold Time, HIGH or LOW D_n to CP	3.3	1.0	2.0	4.0	2.0	ns	2–7
		5.0	1.0	2.0	4.0	2.0		
t_s	Setup Time, HIGH or LOW, $\overline{E}$ to CP	3.3	0	2.0	2.5	2.0	ns	2–7
		5.0	0	2.0	2.5	2.0		
t_h	Hold Time, HIGH or LOW, $\overline{E}$ to CP	3.3	1.0	2.0	4.0	2.0	ns	2–7
		5.0	1.0	2.0	4.0	2.0		
t_w	CP Pulse Width HIGH or LOW	3.3	3.0	4.5	6.5	5.5	ns	2–3
		5.0	2.0	3.5	6.5	4.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	28	pF	V_{CC} = 5.0V

National Semiconductor

54ACT/74ACT399
Quad 2-Port Register

General Description

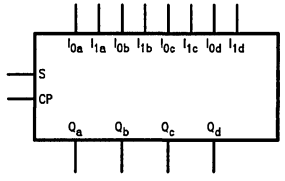
The 'ACT399 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flop on the rising edge of the clock.

Features

- Select inputs from two data sources
- Fully positive edge-triggered operation
- Outputs source/sink 24 mA
- 'ACT399 has TTL-compatible inputs

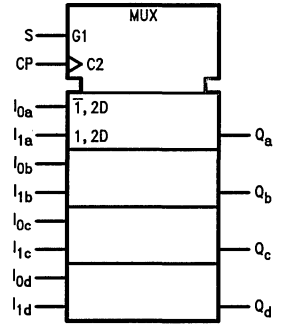
Ordering Code: See Section 8

Logic Symbols



TL/F/9789–1

IEEE/IEC

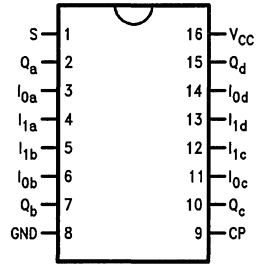


TL/F/9789–5

Pin Names	Description
S	Common Select Input
CP	Clock Pulse Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
Q_a–Q_d	Register True Outputs

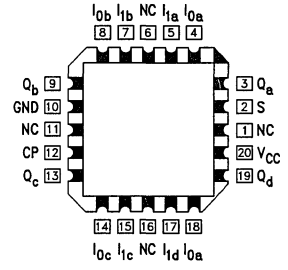
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9789–3

Pin Assignment for LCC



TL/F/9789–2

Functional Description

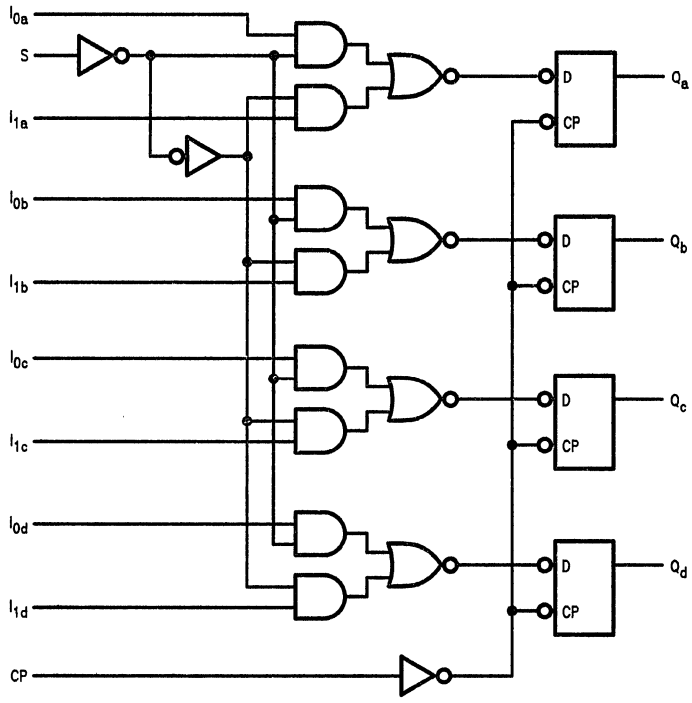
The 'ACT399 is a high-speed quad 2-port register. It selects four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation.

Function Table

Inputs				Outputs	
S	I_0	I_1	CP	Q	$\overline{Q}$
L	L	X	↗	L	H
L	H	X	↗	H	L
H	X	L	↗	L	H
H	X	H	↗	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/9789–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	+175°C
PDIP	+140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.85	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or Ground

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for the 54ACT device is identical to the 74ACT device at 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54ACT T_A, V_{CC} = Mil, $C_L = 50$ pF		74ACT T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Input Clock Frequency	5.0	165	160		90		160		MHz	
t_{PLH}	Propagation Delay CP to Q	5.0	1.5	7.0	8.0		10.0	1.5	8.5	ns	2–3, 4
t_{PHL}	Propagation Delay CP to Q	5.0	2.0	6.0	9.0		10.0	2.0	9.5	ns	2–3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW I_n to CP	5.0	3.0	2.5	3.5	2.5	ns	2–7
t_h	Hold Time, HIGH or LOW I_n to CP	5.0	0	1.0	3.0	1.0	ns	2–7
t_s	Setup Time, HIGH or LOW S to CP	5.0	3.0	4.0	6.0	4.0	ns	2–7
t_h	Hold Time, HIGH or LOW S to CP	5.0	−1.0	0.5	2.5	0.5	ns	2–7
t_w	CP Pulse Width HIGH or LOW	5.0	5.5	3.5	5.0	3.5	ns	2–3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	30	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC520 • 54ACT/74ACT520
8-Bit Identity Comparator

General Description

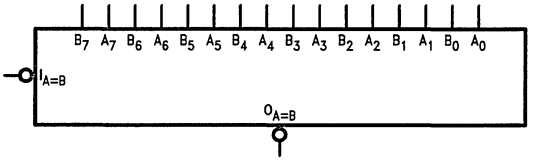
The 'AC/'ACT520 are expandable 8-bit comparators. They compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

Features

- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- 'ACT520 has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbols



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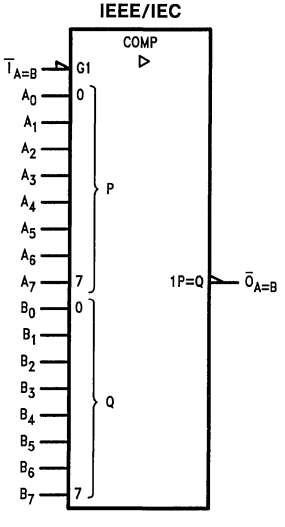
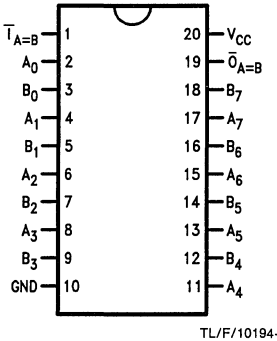


TL/F/10194–4

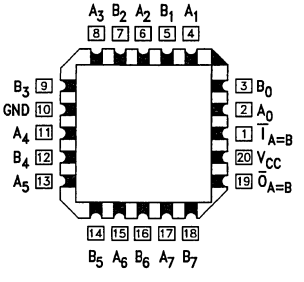
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10194–2

Pin Assignment for LCC



TL/F/10194–3

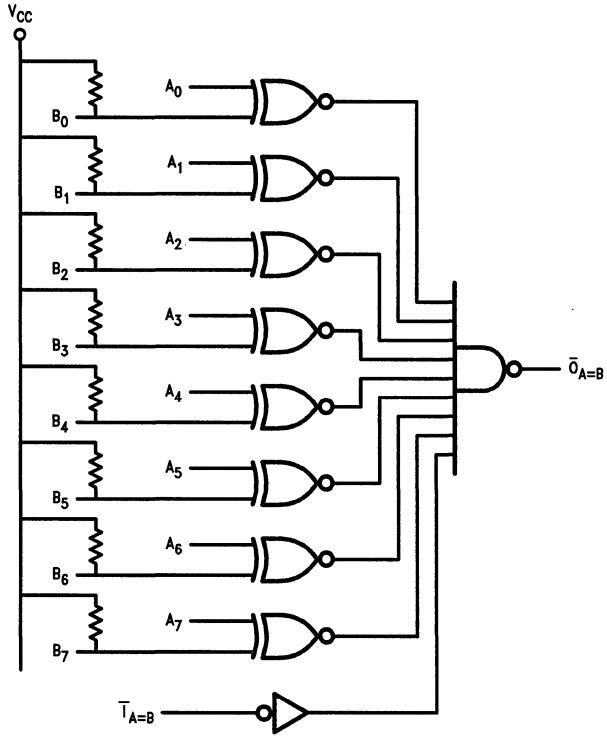
Pin Names	Description
A_0–A_7	Word A Inputs
B_0–B_7	Word B Inputs
$T_{A=B}$	Expansion or Enable Input
$\overline{O}_{A=B}$	Identity Output

Truth Table

Inputs		Outputs
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Logic Diagram



TL/F/10194–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3	4.0	7.5	11.5	1.0	14.0	3.0	13.0	ns	2–3, 4
		5.0	2.5	5.5	8.5	1.5	10.5	2.0	9.5		
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3	4.5	8.0	12.0	1.0	15.0	3.5	13.5	ns	2–3, 4
		5.0	3.0	5.5	9.0	1.5	11.0	2.5	10.0		
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.5	5.5	8.5	1.0	10.0	2.5	9.5	ns	2–3, 4
		5.0	2.5	4.5	6.5	1.5	7.5	2.0	7.0		
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.5	5.5	8.5	1.0	10.5	2.5	9.5	ns	2–3, 4
		5.0	2.5	4.5	6.5	1.5	8.0	2.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	5.5	8.5	1.5	12.0	2.5	9.5	ns	2–3, 4
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	6.0	10.0	1.5	12.0	2.5	11.5	ns	2–3, 4
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.0	4.0	6.0	1.5	8.5	2.0	6.5	ns	2–3, 4
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.5	5.0	7.5	1.5	9.0	2.0	8.5	ns	2–3, 4

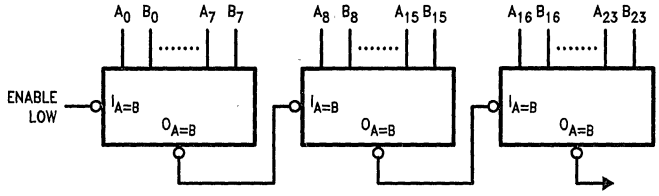
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0V

Applications

Ripple Expansion



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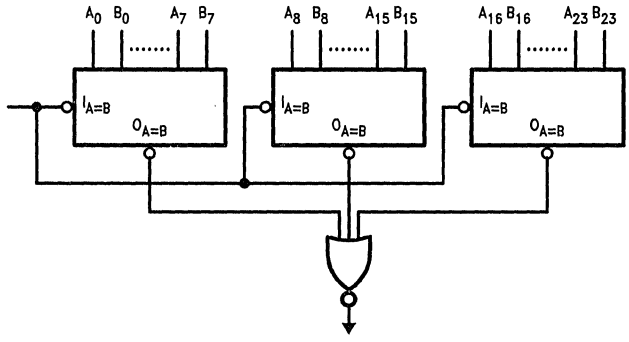
Parallel Expansion



TL/F/10194–7

National Semiconductor

54AC/74AC521 • 54ACT/74ACT521
8-Bit Identity Comparator

General Description

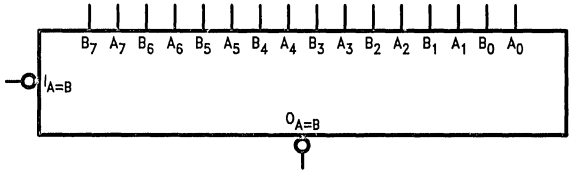
The 'AC/'ACT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

Features

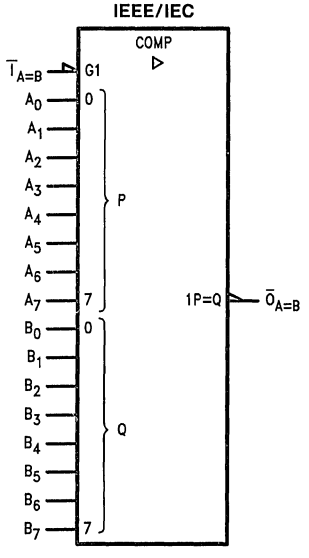
- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- 'ACT521 has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbols



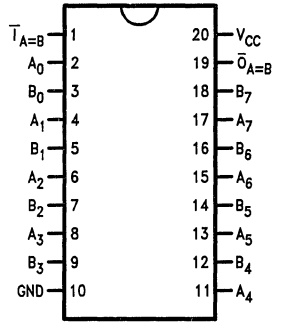
TL/F/9964–1



TL/F/9964–4

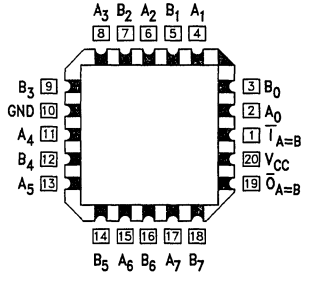
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9964–2

Pin Assignment for LCC



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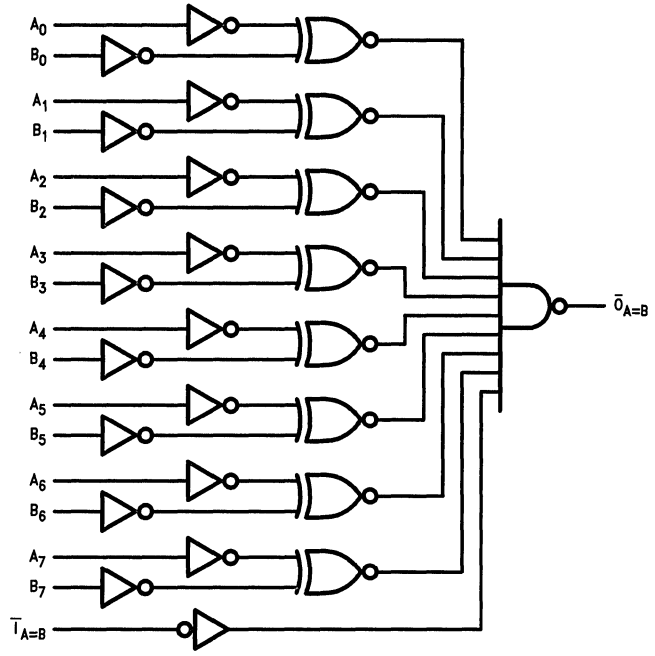
Pin Names	Description
A_0–A_7	Word A Inputs
B_0–B_7	Word B Inputs
$\overline{T}_{A=B}$	Expansion or Enable Input
$\overline{O}_{A=B}$	Identity Output

Truth Table

Inputs		Outputs
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3	3.5	7.0	11.0	1.0	15.0	3.0	12.0	ns	2-3, 4
		5.0	2.5	5.0	8.0	1.5	10.5	2.0	9.0		
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3	4.5	7.5	11.5	1.0	15.0	3.5	12.5	ns	2-3, 4
		5.0	3.0	5.5	8.5	1.5	10.5	2.5	9.0		
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.0	5.5	8.0	1.0	10.5	2.5	9.0	ns	2-3, 4
		5.0	2.5	4.0	6.0	1.5	8.0	2.0	7.0		
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3	3.0	5.5	8.0	1.0	10.5	2.5	9.0	ns	2-3, 4
		5.0	2.0	4.0	6.0	1.5	8.0	2.0	7.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	5.5	9.0	1.5	11.0	2.5	9.5	ns	2-3, 4
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0	3.0	6.0	10.0	1.5	12.0	2.5	11.0	ns	2-3, 4
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.0	4.0	6.5	1.5	7.5	2.0	7.0	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0	2.5	5.0	7.5	1.5	8.5	2.0	8.0	ns	2-3, 4

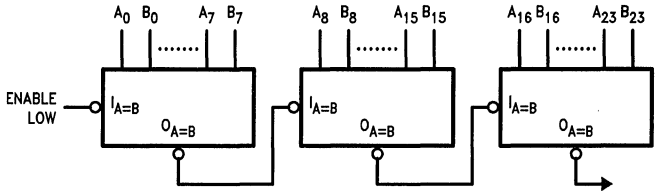
*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0V$

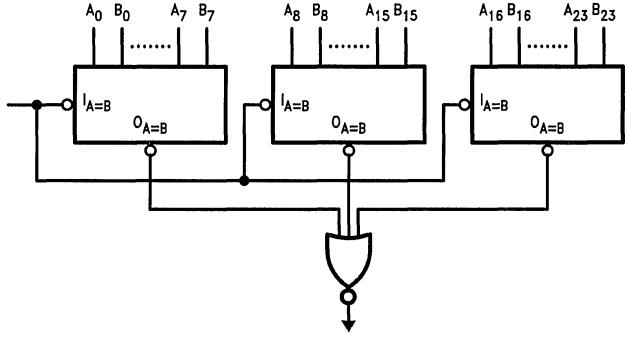
Applications

Ripple Expansion



TL/F/9964–6

Parallel Expansion



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National Semiconductor

54ACT/74ACT534
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

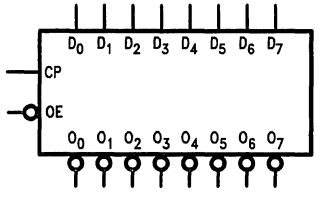
The 'ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'ACT534 is the same as the 'ACT374 except that the outputs are inverted.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT534 has TTL-compatible inputs
- Inverted output version of 'ACT374

Ordering Code: See Section 8

Logic Symbols



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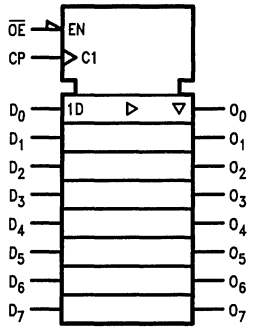
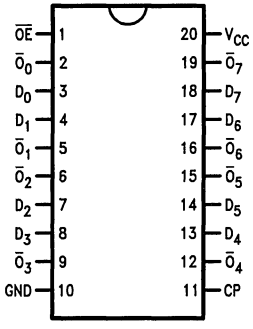
IEEE/IEC



TL/F/9965–2

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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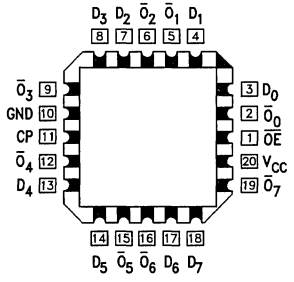
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

Pin Assignment for LCC



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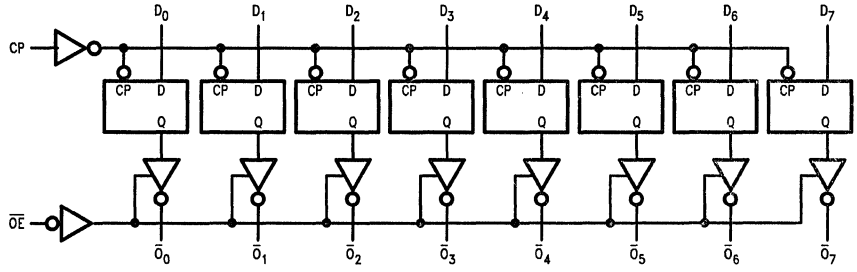
Functional Description

The 'ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



TL/F/9965–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs			Output
CP	OE	D	$\overline{O}$
⌐	L	H	L
⌐	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
Z = High Impedance
$\overline{O}_0$ = Value stored from previous clock cycle

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		100		85		120		MHz	
t_{PLH}	Propagation Delay CP to $\overline{Q}_n$	5.0	2.5	6.5	11.5	1.0	14.0	2.0	12.5	ns	2-3, 4
t_{PHL}	Propagation Delay CP to $\overline{Q}_n$	5.0	2.0	6.0	10.5	1.0	13.0	2.0	12.0	ns	2-3, 4
t_{PZH}	Output Enable Time	5.0	2.5	6.5	12.0	1.0	14.0	2.0	12.5	ns	2-5
t_{PZL}	Output Enable Time	5.0	2.0	6.0	11.0	1.0	13.0	2.0	11.5	ns	2-6
t_{PHZ}	Output Disable Time	5.0	1.5	7.0	12.5	1.0	14.5	1.0	13.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	1.5	5.5	10.5	1.0	11.5	1.0	10.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	3.5	5.0	4.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−1.0	1.0	3.0	1.5	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	3.5	5.0	3.5	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC540
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC540 is an octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

These devices are similar in function to the 'AC240 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

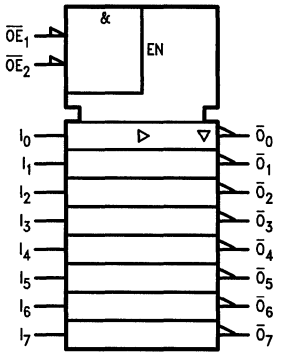
Features

- TRI-STATE inverting outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24 mA

Ordering Code: See Section 8

Logic Symbol

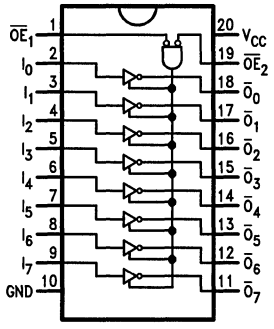
IEEE/IEC



TL/F/9966–1

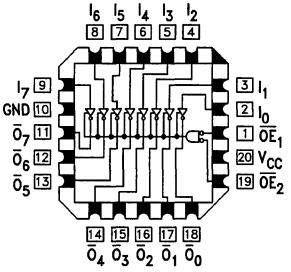
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9966–3

Pin Assignment for LCC



TL/F/9966–2

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3	1.5	5.5	7.5	1.0	9.0	1.0	8.0	ns	2-3, 4
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		
t_{PHL}	Propagation Delay Data to Output	3.3	1.5	5.0	7.0	1.0	8.0	1.0	7.5	ns	2-3, 4
		5.0	1.5	4.0	5.5	1.0	6.5	1.0	6.0		
t_{PZH}	Output Enable Time	3.3	3.0	8.5	11.0	1.0	13.0	2.5	12.0	ns	2-5
		5.0	2.0	6.5	8.5	1.0	10.0	2.0	9.5		
t_{PZL}	Output Enable Time	3.3	2.5	7.5	10.0	1.0	12.0	2.0	11.0	ns	2-6
		5.0	2.0	6.0	7.5	1.0	9.0	1.5	8.5		
t_{PHZ}	Output Disable Time	3.3	2.5	8.5	13.0	1.0	15.5	1.5	14.0	ns	2-5
		5.0	1.5	7.5	10.5	1.0	12.0	1.0	11.0		
t_{PLZ}	Output Disable Time	3.3	2.5	7.0	10.0	1.0	12.0	2.0	11.0	ns	2-6
		5.0	1.5	6.0	8.0	1.0	10.0	1.5	9.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	30.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC541
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'AC541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The 'AC541 is a noninverting option of the 'AC540.

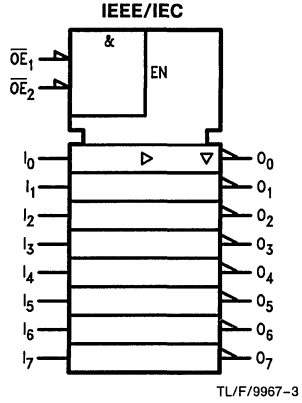
This device is similar in function to the 'AC244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

Features

- TRI-STATE outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24 mA
- 'AC540 provides inverted outputs
- Standard Military Drawing (SMD)
  — 'AC541: 5962-88706

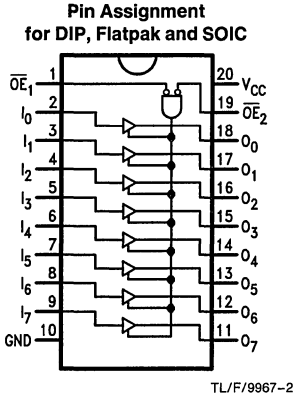
Ordering Code: See Section 8

Logic Symbol

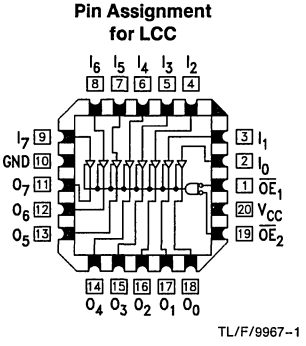


TL/F/9967–3

Connection Diagrams



TL/F/9967–2



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Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$	74AC $T_A = -55°C$ to $+125°C$	54AC $T_A = -40°C$ to $+85°C$	74AC	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

†Maximum test duration 2.0 ms, one output loaded at a time.

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC	54AC	74AC	Units	Conditions
			T_A = +25°C	T_A = −55°C to +125°C	T_A = −40°C to +85°C		
			Typ	Guaranteed Limits			
I_{OZ}	Maximum TRI-STATE® Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC			54AC		74AC		Units	Fig. No.
			T_A = +25°C C_L = 50 pF			T_A = −55°C to +125°C C_L = 50 pF		T_A = −40°C to +85°C C_L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3	2.0	5.5	8.0	1.0	10.0	1.5	9.0	ns	2–3, 4
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		
t_{PHL}	Propagation Delay Data to Output	3.3	2.0	5.5	8.0	1.0	9.5	1.5	8.5	ns	2–3, 4
		5.0	1.5	4.0	6.0	1.0	7.0	1.0	6.5		
t_{PZH}	Output Enable Time	3.3	3.0	8.0	11.5	1.0	13.5	3.0	12.5	ns	2–5
		5.0	2.0	6.0	8.5	1.0	10.0	1.5	9.5		
t_{PZL}	Output Enable Time	3.3	2.5	7.0	10.0	1.0	12.5	2.5	11.5	ns	2–6
		5.0	1.5	5.5	7.5	1.0	9.0	1.0	8.5		
t_{PHZ}	Output Disable Time	3.3	3.5	9.0	12.5	1.0	15.0	2.5	14.0	ns	2–5
		5.0	2.0	7.0	9.5	1.0	12.0	1.0	10.5		
t_{PLZ}	Output Disable Time	3.3	2.5	6.5	9.5	1.0	11.0	2.0	10.5	ns	2–6
		5.0	2.0	5.5	7.5	1.0	9.0	1.0	8.5		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	30.0	pF	V_{CC} = 5.0V

National Semiconductor

54ACT/74ACT563
Octal Latch with TRI-STATE® Outputs

General Description

The 'ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

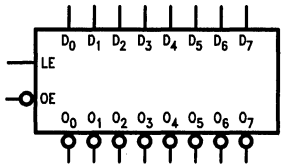
The 'ACT563 device is functionally identical to the 'ACT573, but with inverted outputs.

Features

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT573 but with inverted outputs
- Outputs source/sink 24 mA
- 'ACT563 has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbols



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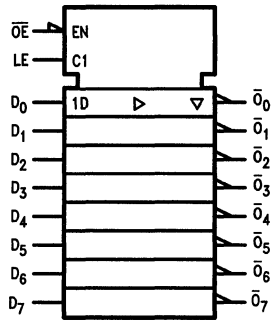
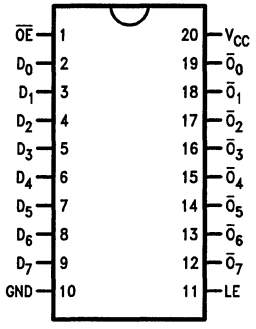
IEEE/IEC



TL/F/9970–2

Connection Diagrams

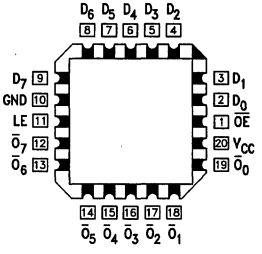
Pin Assignment for DIP, Flatpak and SOIC



TL/F/9970–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Latch Outputs

Pin Assignment for LCC



TL/F/9970–4

Functional Description

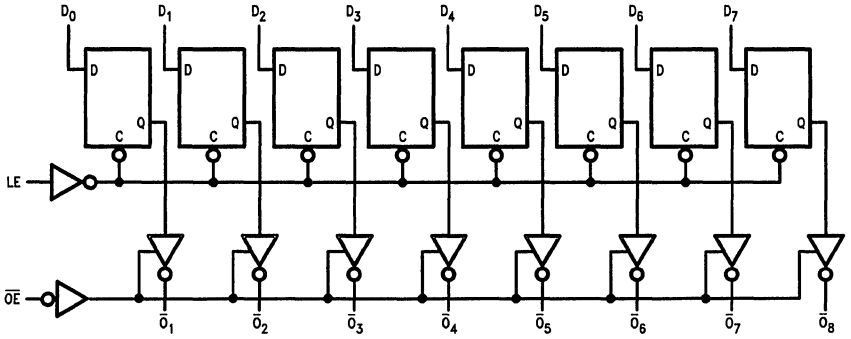
The 'ACT563 contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High-Z
H	H	L	H	Z	High-Z
H	H	H	L	Z	High-Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/9970–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	5.0	3.0	7.0	11.5	1.0	14.5	2.5	12.5	ns	2-3,4
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	5.0	3.0	6.0	10.0	1.0	12.0	2.5	11.0	ns	2-3,4
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	5.0	3.0	6.5	10.5	1.0	12.5	2.5	11.5	ns	2-3,4
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0	2.5	5.5	9.5	1.0	11.5	2.0	10.5	ns	2-3,4
t_{PZH}	Output Enable Time	5.0	2.5	5.5	9.0	1.0	11.5	2.0	10.0	ns	2-5
t_{PZL}	Output Enable Time	5.0	2.0	5.5	8.5	1.0	11.0	2.0	9.5	ns	2-6
t_{PHZ}	Output Disable Time	5.0	3.5	6.5	10.5	1.0	12.0	2.5	11.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	2.0	4.5	8.0	1.0	9.5	1.0	8.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	1.5	4.0	4.5	4.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−2.0	0	1.5	0	ns	2-7
t_w	LE Pulse Width, HIGH	5.0	2.0	3.0	5.0	3.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	50.0	pF	V_{CC} = 5.0V

National Semiconductor

54ACT/74ACT564
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

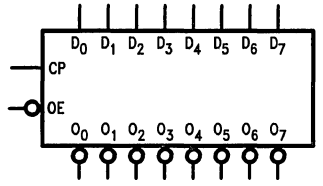
The 'ACT564 device is functionally identical to the 'ACT574, but with inverted outputs.

Features

- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT574 but with inverted outputs
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT564 has TTL-compatible inputs

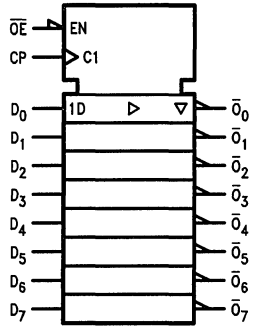
Ordering Code: See Section 8

Logic Symbols



TL/F/9972–1

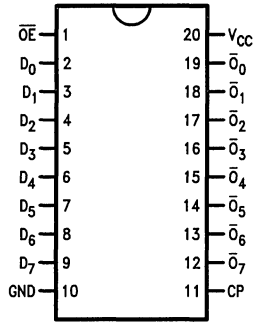
IEEE/IEC



TL/F/9972–2

Connection Diagrams

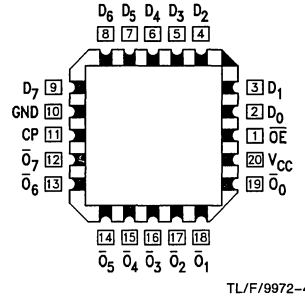
Pin Assignment for DIP, Flatpak and SOIC



TL/F/9972–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

Pin Assignment for LCC



TL/F/9972–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85	90		65		75		MHz	
t_{PLH}	Propagation Delay, CP to $\overline{O}_n$	5.0	2.0	6.5	10.5	1.0	12.5	1.5	11.5	ns	2-3,4
t_{PHL}	Propagation Delay, CP to $\overline{O}_n$	5.0	1.5	6.0	9.5	1.0	11.5	1.5	10.5	ns	2-3,4
t_{PZH}	Output Enable Time	5.0	1.5	5.5	9.0	1.0	10.5	1.5	9.5	ns	2-5
t_{PZL}	Output Enable Time	5.0	1.5	5.5	8.5	1.0	10.5	1.0	9.5	ns	2-6
t_{PHZ}	Output Disable Time	5.0	1.5	7.0	10.5	1.0	12.5	1.5	11.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	1.5	5.0	8.0	1.0	9.5	1.0	8.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	2.5	3.5	3.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	2.5	1.0	ns	2-7
t_w	LE Pulse Width, HIGH or LOW	5.0	2.5	3.0	5.0	3.5	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACT/74ACT573
Octal Latch with TRI-STATE® Outputs

General Description

The 'ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

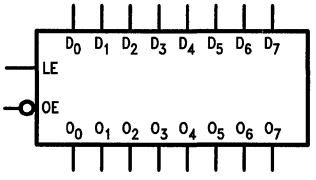
The 'ACT573 is functionally identical to the 'ACT373 but has inputs and outputs on opposite sides.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT373
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT573 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'ACT573: 5962-87664

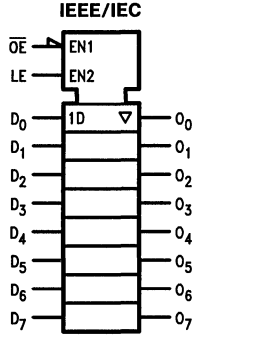
Ordering Code: See Section 8

Logic Symbols



TL/F/9973–1

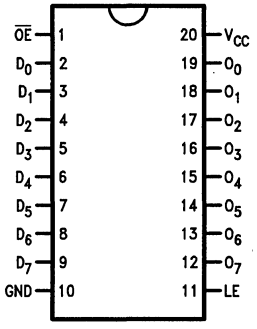
IEEE/IEC



TL/F/9973–2

Connection Diagrams

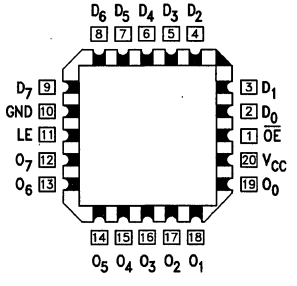
Pin Assignment for DIP, Flatpak and SOIC



TL/F/9973–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

Pin Assignment for LCC



TL/F/9973–4

Functional Description

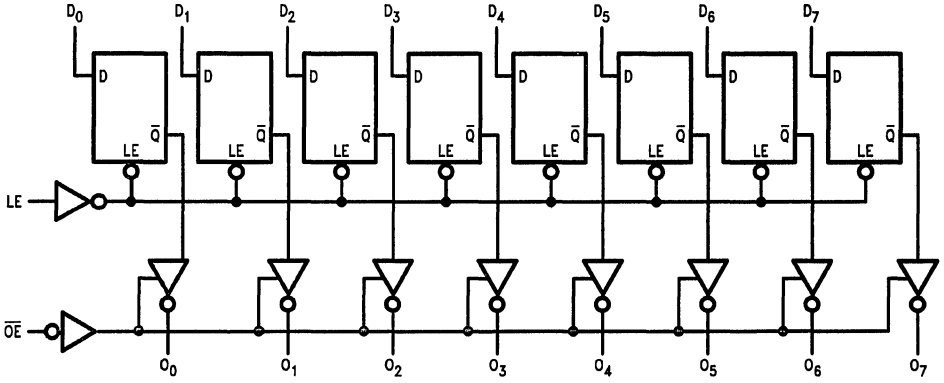
The 'ACT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



TL/F/9973–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_m to O_n	5.0	2.5	6.0	10.5	1.0	13.5	2.0	12.0	ns	2-3,4
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.5	6.0	10.5	1.0	13.5	2.0	12.0	ns	2-3,4
t_{PLH}	Propagation Delay LE to O_n	5.0	3.0	6.0	10.5	1.0	13.0	2.5	12.0	ns	2-3,4
t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	5.5	9.5	1.0	12.0	2.0	10.5	ns	2-3,4
t_{PZH}	Output Enable Time	5.0	2.0	5.5	10.0	1.0	11.5	1.5	11.0	ns	2-5
t_{PZL}	Output Enable Time	5.0	1.5	5.5	9.5	1.0	11.0	1.5	10.5	ns	2-6
t_{PHZ}	Output Disable Time	5.0	2.5	6.5	11.0	1.0	13.5	1.5	12.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	1.5	5.0	8.5	1.0	10.5	1.0	9.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	1.5	3.0	4.5	3.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−1.5	0	1.0	0	ns	2-7
t_w	LE Pulse Width, HIGH	5.0	2.0	3.5	5.0	4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	25.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC574 • 54ACT/74ACT574
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'AC/'ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

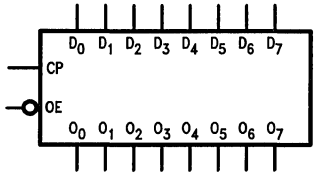
The 'AC/'ACT574 is functionally identical to the 'AC/'ACT374 except for the pinouts.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'AC/'ACT374
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT574 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'ACT574: 5962-89601

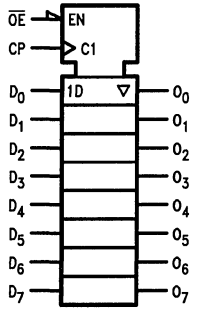
Ordering Code: See Section 8

Logic Symbols



TL/F/9910–1

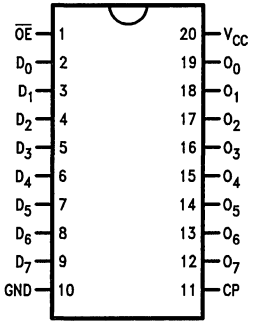
IEEE/IEC



TL/F/9910–4

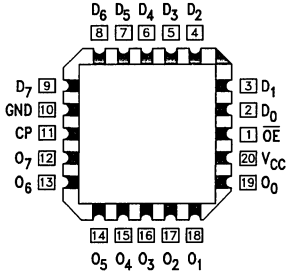
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9910–2

Pin Assignment for LCC



TL/F/9910–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Functional Description

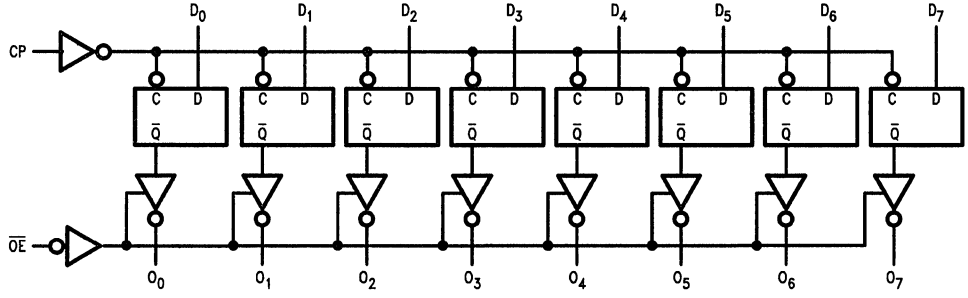
The 'AC/'ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/9910–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- (Unless Otherwise Specified) (AC) 2.0V to 6.0V
- (ACT) 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'AC Devices
V_{IN} from 30% to 70% of V_{CC}
V_{CC} @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'ACT Devices
V_{IN} from 0.8V to 2.0V
V_{CC} @ 4.5V, 5.5V 125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25°C	74AC T_A = −55°C to +125°C	54AC T_A = −40°C to +85°C	74AC Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		
		5.5		4.86	4.7		
		3.0		2.46			I_{OH} −24 mA
		4.5		3.76			
		5.5		4.76			I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50		
		5.5		0.36	0.50		
		3.0		0.44			I_{OL} 24 mA
		4.5		0.44			
		5.5		0.44			I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
					±1.0		

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = 25°C$ Typ	74AC $T_A = 25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = 25°C$ Typ	74ACT $T_A = 25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	3.3 5.0	75 95	112 153		55 80		60 85		MHz	
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0	3.5 2.0	8.5 6.0	13.5 9.5	1.0 1.0	16.5 11.5	3.5 2.0	15.0 11.0	ns	2-3, 4
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0	3.5 2.0	7.5 5.5	12.0 8.5	1.0 1.0	15.0 10.5	3.5 2.0	13.5 9.5	ns	2-3, 4
t_{PZH}	Output Enable Time	3.3 5.0	2.5 2.0	7.0 5.0	11.0 8.5	1.0 1.0	13.0 9.5	2.5 2.0	12.0 9.0	ns	2-5
t_{PZL}	Output Enable Time	3.3 5.0	3.0 2.0	6.5 5.0	10.5 8.0	1.0 1.0	12.5 9.5	3.0 1.5	11.5 9.0	ns	2-6
t_{PHZ}	Output Disable Time	3.3 5.0	3.5 2.0	7.5 6.0	12.0 9.5	1.0 1.0	14.0 11.0	2.5 1.5	13.0 10.5	ns	2-5
t_{PLZ}	Output Disable Time	3.3 5.0	2.0 1.0	5.5 4.5	9.0 7.5	1.0 1.0	10.5 9.0	1.5 1.0	10.0 8.5	ns	2-6

*Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-Up Time, HIGH or LOW D_n to CP	3.3 5.0	0.5 0	2.5 1.5	3.0 2.0	3.0 2.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−0.5 0	1.5 1.5	1.5 1.5	1.5 1.5	ns	2-7
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.0	6.0 4.0	7.5 5.5	7.0 5.0	ns	2-3

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	5.0	100	110		70		85		ns	
t_{PLH}	Propagation Delay CP to O_n	5.0	2.5	7.0	11.0	1.0	13.5	2.0	12.0	ns	2-3, 4
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	6.5	10.0	1.0	12.5	1.5	11.0	ns	2-3, 4
t_{PZH}	Output Enable Time	5.0	2.0	6.4	9.5	1.0	11.0	1.5	10.0	ns	2-5
t_{PZL}	Output Enable Time	5.0	2.0	6.0	9.0	1.0	11.0	1.5	10.0	ns	2-6
t_{PHZ}	Output Disable Time	5.0	2.0	7.0	10.5	1.0	12.0	1.5	11.5	ns	2-5
t_{PLZ}	Output Disable Time	5.0	2.0	5.5	8.5	1.0	10.0	1.5	9.0	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-Up Time, HIGH or LOW D_n to CP	5.0	1.5	2.5	3.5	2.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	2.0	1.0	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	3.0	5.0	4.0	ns	2-3

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC646 • 54ACT/74ACT646
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

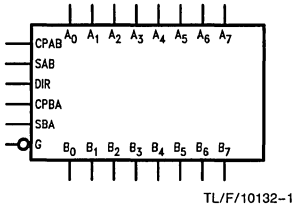
The 'AC/'ACT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1-4.*

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- TRI-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- 'ACT646 has TTL compatible inputs
- Standard Military Drawing (SMD)
  — 'AC646: 5962-89682

Ordering Code: See Section 8

Logic Symbols



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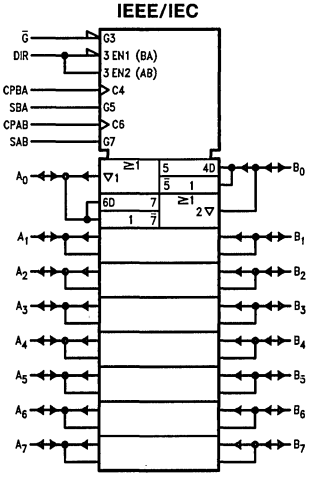

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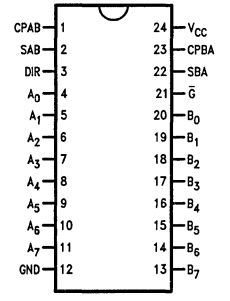
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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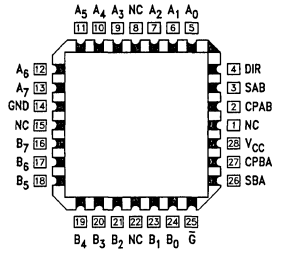
Pin Assignment for LCC and PCC



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Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

Real Time Transfer A-Bus to B-Bus

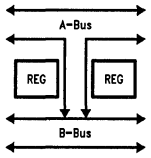

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FIGURE 1

Real Time Transfer B-Bus to A-Bus

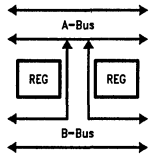

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FIGURE 2

Storage from Bus to Register

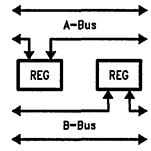

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FIGURE 3

Transfer from Register to Bus

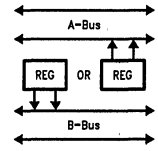

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FIGURE 4

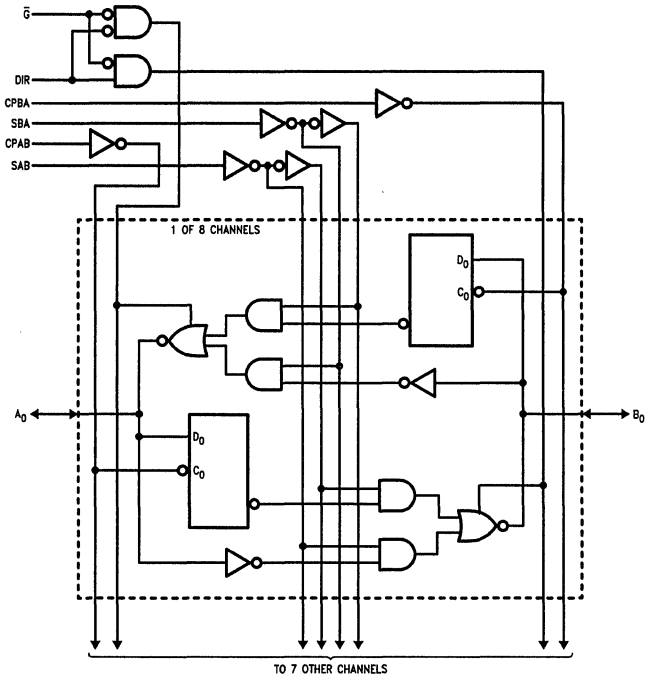
Function Table

Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↗	X	X	X			Clock A_n Data into A Register
H	X	X	↗	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↗	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↗	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↗	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↗	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	4.0 2.5	10.5 7.5	16.5 12.0	1.0 1.0	20.0 14.0	3.0 2.0	18.5 13.0	ns	2-3, 4
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	3.0 2.0	9.5 6.5	14.5 10.5	1.0 1.0	17.5 12.0	2.5 1.5	16.0 11.5	ns	2-3, 4
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	2.5 1.5	7.5 5.0	12.0 8.0	1.0 1.0	15.0 10.0	2.0 1.0	13.5 9.0	ns	2-3, 4
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.5 1.5	7.5 5.0	12.5 9.0	1.0 1.0	14.5 9.5	1.5 1.0	13.5 9.5	ns	2-3, 4
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3 5.0	2.0 1.5	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.5 1.5	15.5 11.0	ns	2-3, 4
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3 5.0	1.5 1.5	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.5 1.5	15.0 11.0	ns	2-3, 4
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.5	1.0 1.0	13.0 9.5	2.0 1.5	12.5 9.0	ns	2-5
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.5 1.5	7.5 5.5	12.5 9.0	1.0 1.0	15.5 11.0	2.0 1.5	14.0 10.0	ns	2-6
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	3.0 2.0	8.0 6.5	12.5 10.0	1.0 1.0	14.0 11.5	2.5 2.0	13.5 11.0	ns	2-5
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	2.0 1.5	7.5 6.0	12.0 9.5	1.0 1.0	13.5 11.0	2.0 1.5	13.5 10.5	ns	2-6
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	2.0 1.5	6.5 5.0	11.0 7.5	1.0 1.0	14.5 10.5	1.5 1.0	12.0 8.5	ns	2-5
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	2.5 1.5	7.0 5.0	11.5 8.0	1.0 1.0	16.0 12.5	2.0 1.0	13.0 9.0	ns	2-6
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	2.5 1.5	7.5 5.5	11.5 9.5	1.0 1.0	14.5 12.0	1.5 1.5	12.5 10.0	ns	2-5
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.5 1.5	7.5 5.5	12.0 9.5	1.0 1.0	16.5 12.0	1.5 1.5	13.5 10.5	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW Bus to Clock	3.3 5.0	2.0 1.5	5.0 4.0	6.0 4.5	5.5 4.5	ns	2-7
t_h	Hold Time, HIGH or LOW Bus to Clock	3.3 5.0	−1.5 −0.5	0 0.5	1.5 2.0	0 1.0	ns	2-7
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.5	5.0 5.0	4.5 3.5	ns	2-3

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	5.0	6.0	12.0	14.5			3.0	16.0	ns	2-3, 4
t_{PHL}	Propagation Delay Clock to Bus	5.0	6.0	12.0	14.5			3.5	16.0	ns	2-3, 4
t_{PLH}	Propagation Delay Bus to Bus	5.0	4.5	8.5	10.5			2.5	11.5	ns	2-3, 4
t_{PHL}	Propagation Delay Bus to Bus	5.0	5.0	8.5	10.5			2.0	11.5	ns	2-3, 4
t_{PLH}	Propagation Delay SBA or SAB to A_n to B_n (w/A_n or B_n HIGH or LOW)	5.0	5.0	9.5	11.5			2.5	12.5	ns	2-3, 4
t_{PHL}	Propagation Delay SBA or SAB to A_n to B_n (w/A_n or B_n HIGH or LOW)	5.0	5.0	9.5	11.5			2.5	12.5	ns	2-3, 4
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	5.0	6.0	9.0	11.0			1.5	12.0	ns	2-5
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	5.0	5.0	9.0	11.0			3.0	12.0	ns	2-6
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	7.5	10.5	13.0			4.5	14.5	ns	2-5
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	5.0	5.5	10.0	12.5			3.0	14.0	ns	2-6
t_{PZH}	Enable Time DIR to A_n or B_n	5.0	5.5	6.5	10.5			1.5	11.5	ns	2-5
t_{PZL}	Enable Time DIR to A_n or B_n	5.0	4.0	6.5	10.5			3.0	11.5	ns	2-6
t_{PHZ}	Disable Time DIR to A_n or B_n	5.0	5.5	8.5	12.5			4.5	13.5	ns	2-5
t_{PLZ}	Disable Time DIR to A_n or B_n	5.0	4.0	8.5	12.5			3.0	13.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW BUS to Clock	5.0	2.5	7.0		8.0	ns	2-7
t_h	Hold Time, HIGH or LOW Bus to Clock	5.0	0	2.5		2.5	ns	2-7
t_w	Clock Pulse Width HIGH or LOW	5.0	4.5	7.0		8.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	60.0	pF	V_{CC} = 5.0V

National Semiconductor

54AC/74AC648
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

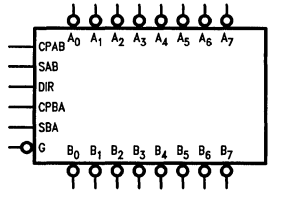
The 'AC648 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1* thru *4* (See Page 2).

Features

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- TRI-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Inverted data to output

Ordering Code: See Section 8

Logic Symbols



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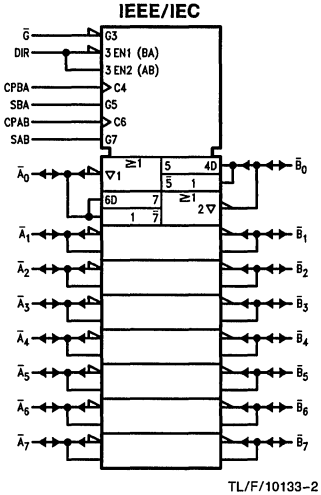

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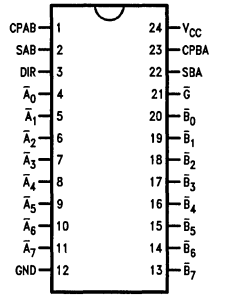
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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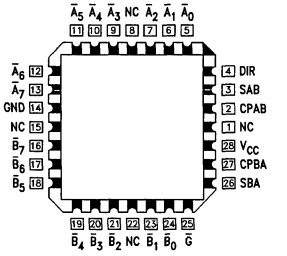
Pin Assignment for LCC and PCC



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Pin Names	Description
$\overline{A}_0$–$\overline{A}_7$	Data Register A Inputs, Data Register A TRI-STATE Outputs
$\overline{B}_0$–$\overline{B}_7$	Data Register B Inputs, Data Register B TRI-STATE Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

Function Table

Inputs						Data I/O*		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock A_n Data into A Register
H	X	X	↑	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↑	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↑	X	H			Clock B_n Data into B Register and Output to A_n

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
↑ = LOW-to-HIGH Transition

Real Time Transfer A-Bus to B-Bus

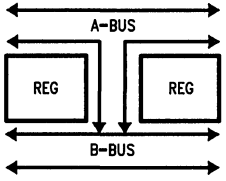

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FIGURE 1

Real Time Transfer B-Bus to A-Bus

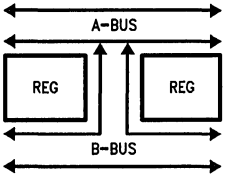

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FIGURE 2

Storage from Bus to Register

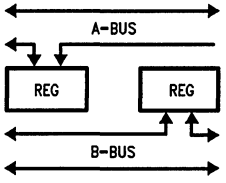

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FIGURE 3

Transfer from Register to Bus

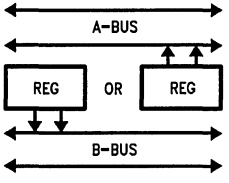

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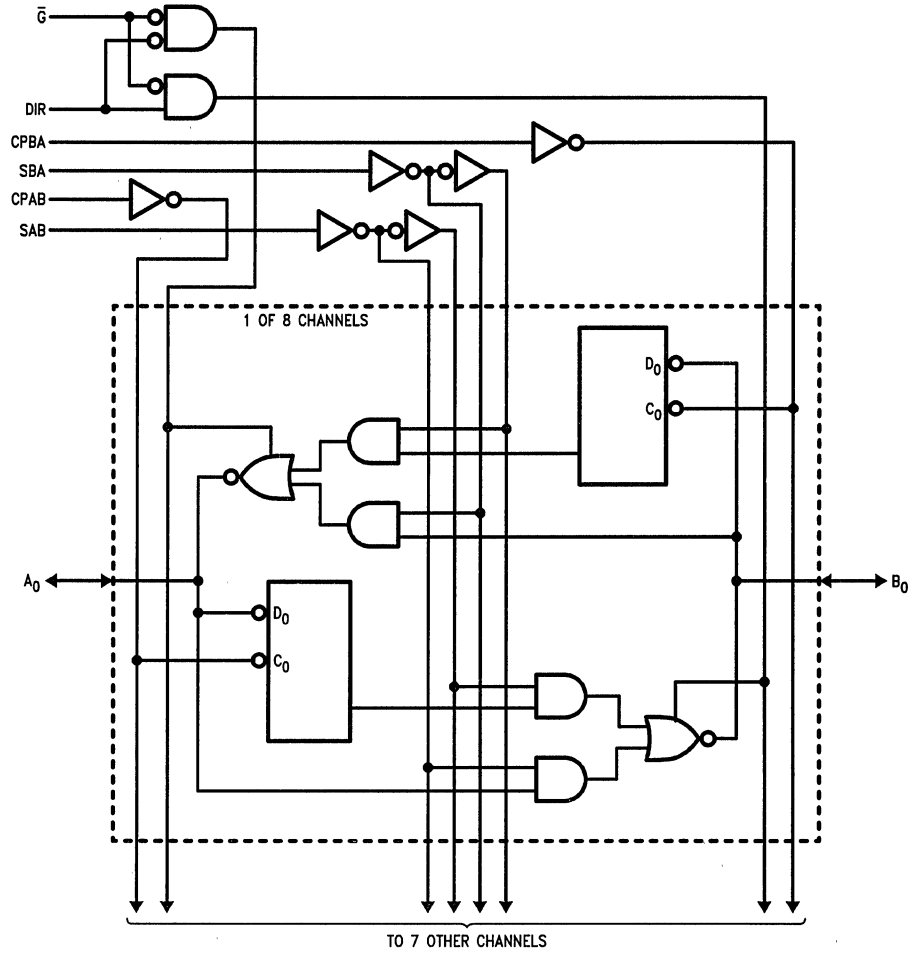
FIGURE 4

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PLH}	Propagation Delay Clock to Bus	3.3	1.5	10.0	15.5			1.5	17.0	ns	2-3, 4
		5.0	1.5	7.0	11.0			1.5	12.0		
t_{PHL}	Propagation Delay Clock to Bus	3.3	1.5	8.5	13.5			1.5	14.5	ns	2-3, 4
		5.0	1.5	6.0	10.5			1.5	11.5		
t_{PLH}	Propagation Delay Bus to Bus	3.3	1.5	6.0	10.0			1.5	11.0	ns	2-3, 4
		5.0	1.5	4.0	7.0			1.0	7.5		
t_{PHL}	Propagation Delay Bus to Bus	3.3	1.5	5.5	9.0			1.5	10.0	ns	2-3, 4
		5.0	1.5	3.5	7.5			1.0	8.0		
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (with A_n or B_n HIGH or LOW)	3.3	1.5	7.5	12.5			1.5	14.0	ns	2-3, 4
		5.0	1.5	5.5	9.0			1.5	10.0		
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (with A_n or B_n HIGH or LOW)	3.3	1.5	7.5	12.5			1.5	14.0	ns	2-3, 4
		5.0	1.5	5.5	9.5			1.5	10.5		
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3	1.5	6.5	11.0			1.0	11.5	ns	2-5
		5.0	1.5	5.0	8.0			1.0	9.0		
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3	1.5	7.0	11.0			1.0	12.5	ns	2-6
		5.0	1.5	5.0	8.0			1.0	9.0		
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3	1.5	7.5	12.0			1.0	13.0	ns	2-5
		5.0	1.5	6.0	10.0			1.0	11.0		
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3	1.5	7.0	11.5			1.0	12.5	ns	2-6
		5.0	1.5	5.5	9.0			1.0	10.0		
t_{PZH}	Enable Time DIR to A_n or B_n	3.3	1.5	6.0	12.5			1.0	14.0	ns	2-5
		5.0	1.5	4.5	9.5			1.0	10.5		
t_{PZL}	Enable Time DIR to A_n or B_n	3.3	1.5	6.5	13.0			1.5	14.5	ns	2-6
		5.0	1.5	4.5	9.0			1.0	10.5		
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3	1.5	7.0	11.5			1.0	13.5	ns	2-5
		5.0	1.5	5.5	9.0			1.0	10.0		
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3	1.5	7.0	13.5			1.5	15.0	ns	2-6
		5.0	1.5	5.0	9.5			1.0	10.0		

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, Bus to Clock	3.3 5.0	2.0 1.5	3.0 2.0		3.5 2.0	ns	2-7
t_h	Hold Time, HIGH or LOW, Bus to Clock	3.3 5.0	−1.5 −0.5	0 1.0		0 1.0	ns	2-7
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.0		4.0 3.0	ns	2-3

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	65.0	pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT705 Arithmetic Logic Unit for Digital Signal Processing Applications

General Description

The 'ACT705 is a high-speed arithmetic processing integrated circuit which is packaged in an 84-pin leadless chip carrier. It features separate input buses that provide data and instruction codes to a high-speed single-cycle 16-bit ALU and an 8-bit by 8-bit parallel multiplier/accumulator.

The ALU is a 16-bit parallel design which supports sixteen arithmetic and logic functions, as well as carry-in/out and borrow-in/out. The multiplier/accumulator, which offers a full 16-bit product, provides for unsigned, signed, mixed mode and imaginary number multiplication. Product accumulation with sum and difference arithmetic is available in each multiplier operating mode.

The 16-bit results of the ALU and multiplier/accumulator are multiplexed to a single set of TRI-STATE® output buffers. The two ALU and multiplier/accumulator carry-out bits, as well as the 4-bit status field indicating ALU and multiplier/accumulator error conditions make up the remaining six bits of the entire 22-bit output.

Features

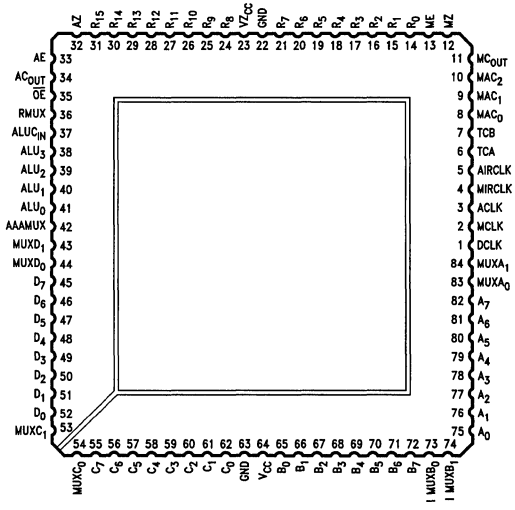
- 84-pin, PCC, CPGA
- Outputs source/sink 8 mA
- 'ACT705 has TTL-compatible inputs
- High throughput achieved with high degree of parallelism in the architecture
- Pipelined stages
- High-speed 16-bit ALU and an 8 x 8 complex multiplier
- 16-bit full ALU performs sixteen Boolean and arithmetic functions with carry-in and carry-out
- 8 x 8 parallel multiplier supports unsigned, signed, complex or mixed mode multiplications, produces 16-bit result with carry-out
- Separate data and instruction buses allow instruction fetches in parallel with execution—single cycle operation
- Accepts 8- or 16-bit data and delivers a 16-bit output
- Data register bank configured to accept a combination of 8- or 16-bit data
- Separate clocks for ALU instruction, multiplier instruction, data, ALU accumulator and multiplier accumulator registers
- Clustered clock pins for ease of board design
- 16-bit ALU/accumulator with feedback to ALU input
- Status of accumulator inputs is monitored: conditions monitored include twos complement overflow, underflow or equal-to-zero

Applications

- Voice-band signal processing
- Discrete Fourier transform applications
  - — FIR filters
  - — IIR filters
- Fast Fourier transform applications
  - — Spectrum analysis
  - — Speech recognition

Connection Diagram

Pin Assignment for PCC



TL/F/10135–1

National Semiconductor

54ACT/74ACT715•LM1882
Programmable Video Sync Generator

General Description

The 'ACT715/LM1882 is a 20-pin TTL-input compatible device capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The device is capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

The 'ACT715/LM1882 makes no assumptions concerning the system architecture. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

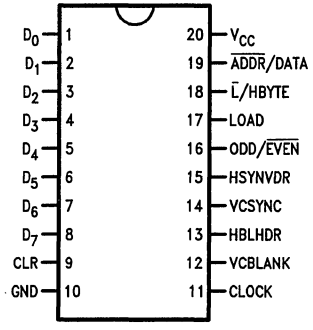
Features

- Maximum Input Clock Frequency > 100 MHz
- Interlaced and non-interlaced formats available
- Separate or composite horizontal and vertical Sync and Blank signals available
- Complete control of pulse width via register programming
- All inputs are TTL compatible
- 8 mA drive on all outputs
- Default RS170/NTSC values mask programmed into registers
- Orderable as linear device LM1882CN or LM1882CM

Ordering Code: See Section 8

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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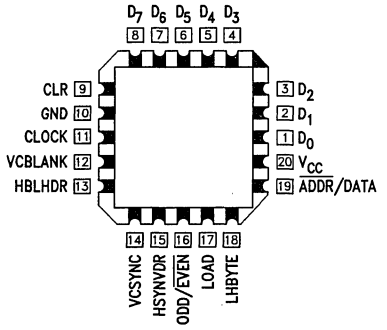
Pin Assignment for LCC



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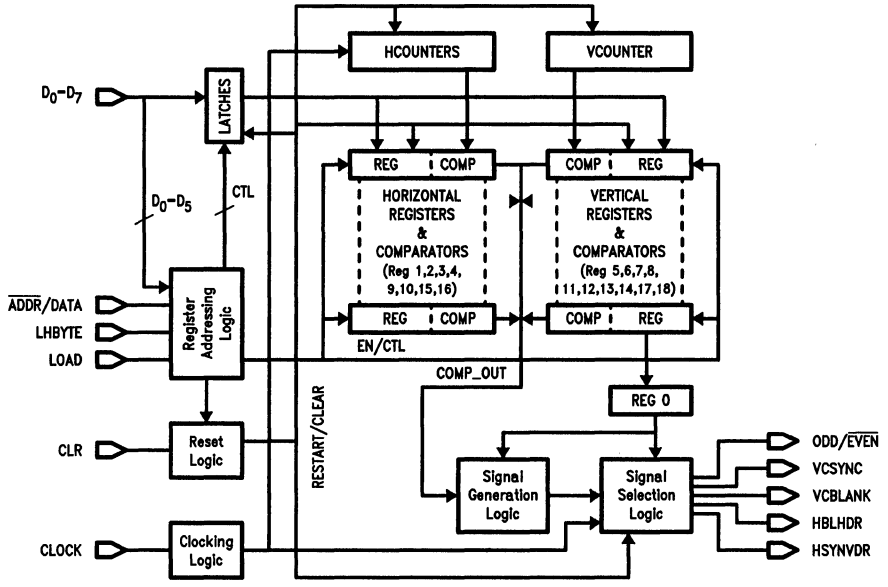
Logic Block Diagram



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Pin Description

There are a Total of 13 inputs and 5 outputs on the 'ACT715/LM1882.

Data Inputs D0–D7: The Data Input pins connect to the Address Register and the Data Input Register.

ADDR/DATA: The ADDR/DATA signal is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus.

L/HBYTE: The L/HBYTE signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the Data Registers. A 1 on this pin when an ADDR/DATA is a 0 enables Auto-Load Mode.

LOAD: The Load control pin loads data into the Address or Data Registers on the rising edge. ADDR/DATA and L/HBYTE data is loaded into the device on the falling edge of the clock. The Load pin has been implemented as a Schmitt trigger input for better noise immunity.

CLOCK: System Clock input from which all timing is derived. The clock pin has been implemented as a Schmitt trigger for better noise immunity.

CLR: The Clear pin is an asynchronous input that initializes the device when it is high. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators and registers. The clear pin has been implemented as a Schmitt trigger for better noise immunity.

ODD/EVEN: Output that identifies if display is in odd (HIGH) or even (LOW) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation this input is always HIGH. Data can be serially scanned out on this pin during test mode.

VCSYNC: Outputs Vertical or Composite Sync signal based on value of the Status Register.

VCBLANK: Outputs Vertical or Composite Blanking signal based on value of the Status Register.

HBLHDR: Outputs Horizontal Blanking signal, Horizontal Gating signal or cursor position based on value of the Status Register.

HSYNVDR: Outputs Horizontal Sync signal, Vertical Gating signal or Vertical Interrupt signal based on value of Status Register.

Register Description

All of the data registers are 12 bits wide. Width's of all pulses are defined by specifying the start count and end count of all pulses. Horizontal pulses are specified with-respect-to the number of clock pulses per line and vertical pulses are specified with-respect-to the number of lines per frame.

REG0—STATUS REGISTER

The Status Register controls the mode of operation, the signals that are output and the polarity of these outputs.

Bits 0–2

B_2	B_1	B_0	VCBLANK	VCSYNC	HBLHDR	HSYNVDR
0	0	0	CBLANK	CSYNC	HGATE	VGATE
0	0	1	VBLANK	CSYNC	HBLANK	VGATE
0	1	0	CBLANK	VSYNC	HGATE	HSYNC
0	1	1	VBLANK	VSYNC	HBLANK	HSYNC
1	0	0	CBLANK	CSYNC	CURSOR	VINT
1	0	1	VBLANK	CSYNC	HBLANK	VINT
1	1	0	CBLANK	VSYNC	CURSOR	HSYNC
1	1	1	VBLANK	VSYNC	HBLANK	HSYNC

Register Description (Continued)

Bits 3–4

B_4	B_3	Mode of Operation
0	0	Interlaced Double Serration and Equalization
0	1	Non Interlaced Double Serration
1	0	Illegal State
1	1	Non Interlaced Single Serration and Equalization

Bits 5–8

Bits 5 through 8 control the polarity of the outputs. A value of zero in these bit locations indicates a pulse active LOW. A value of 1 indicates an active HIGH pulse.

B5— VCBLANK Polarity

B6— VCSYNC Polarity

B7— HBLHDR Polarity

B8— HSYNVDR Polarity

Bits 9–11

Bits 9 through 11 enable several different features of the device.

B9— Enable Equalization/Serration Pulses (0)
Disable Equalization/Serration Pulses (1)

B10— Disable System Clock (0)
Enable System Clock (1)

B11— Disable Counter Test Mode (0)
Enable Counter Test Mode (1)

HORIZONTAL INTERVAL REGISTERS

The Horizontal Interval Registers determine the number of clock cycles per line and the characteristics of the Horizontal Sync and Blank pulses.

REG1— Horizontal Front Porch

REG2— Horizontal Sync Pulse End Time

REG3— Horizontal Blanking Width

REG4— Horizontal Interval Width # of Clocks per Line

VERTICAL INTERVAL REGISTERS

The Vertical Interval Registers determine the number of lines per frame, and the characteristics of the Vertical Blank and Sync Pulses.

REG5— Vertical Front Porch

REG6— Vertical Sync Pulse End Time

REG7— Vertical Blanking Width

REG8— Vertical Interval Width # of Lines per Frame

EQUALIZATION AND SERRATION PULSE SPECIFICATION REGISTERS

These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.

REG 9— Equalization Pulse Width End Time

REG10— Serration Pulse Width End Time

REG11— Equalization/Serration Pulse Vertical Interval Start Time

REG12— Equalization/Serration Pulse Vertical Interval End Time

VERTICAL INTERRUPT SPECIFICATION REGISTERS

These Registers determine the width of the Vertical Interrupt signal if used.

REG13— Vertical Interrupt Activate Time

REG14— Vertical Interrupt Deactivate Time

CURSOR LOCATION REGISTERS

These 4 registers determine the cursor position location, or they generate separate Horizontal and Vertical Gating signals.

REG15— Horizontal Cursor Position Start Time

REG16— Horizontal Cursor Position End Time

REG17— Vertical Cursor Position Start Time

REG18— Vertical Cursor Position End Time

Signal Specification

HORIZONTAL SYNC AND BLANK SPECIFICATIONS

All horizontal signals are defined by a start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This limitation is imposed because during interlace operation this value is internally divided by 2 in order to generate serration and equalization pulses at 2 × the horizontal frequency. Horizontal signals will change on the falling edge of the CLOCK signal. Signal specifications are shown below.

Horizontal Period (HPER) = REG(4) × ckper

Horizontal Blanking Width = [REG(3) − 1] × ckper

Horizontal Sync Width = [REG(2) − REG(1)] × ckper

Horizontal Front Porch = [REG(1) − 1] × ckper

VERTICAL SYNC AND BLANK SPECIFICATION

All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the Vertical Registers in terms of lines per field. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical Blank will change on the leading edge of HBLANK. Vertical Sync will change on the leading edge of HSYNC.

Vertical Frame Period (VPER) = REG(8) × hper

Vertical Field Period (VPER/n) = REG(8) × hper/n

Vertical Blanking Width = [REG(7) − 1] × hper/n

Vertical Syncing Width = [REG(6) − REG(5)] × hper/n

Vertical Front Porch = [REG(5) − 1] × hper/n

where n = 1 for noninterlaced
n = 2 for interlaced

COMPOSITE SYNC AND BLANK SPECIFICATION

Composite Sync and Blank signals are created by logically ANDing (ORing) the active LOW (HIGH) signals of the corresponding vertical and horizontal components of these signals. The Composite Sync signal may also include serration and/or equalization pulses. The serration pulse interval occurs in place of the Vertical Sync interval. Equalization puls-

Signal Specification (Continued)

es occur preceding and/or following the serration pulses. The width and location of these pulses can be programmed through the registers shown below.

Horizontal Equalization PW = [REG(9) − REG(1)] × ckper

Horizontal Serration PW = [REG(4)/n + REG(1) − REG(10)] × ckper

Where n = 1 for noninterlaced single serration/equalization
n = 2 for noninterlaced double serration/equalization
n = 2 for interlaced operation

HORIZONTAL AND VERTICAL GATING SIGNALS

Horizontal and Vertical Gating Signals are available for use when Composite Sync and Blank signals are selected and the value of bit 2 of the status register is 0. The Vertical Gating signal will change in the same manner as that specified for the Vertical Blank.

Horizontal Gating Signal Width = [REG(16) − REG(15)] × ckper

Vertical Gating Signal Width = [REG(18) − REG(17)] × hper

CURSOR POSITION AND VERTICAL INTERRUPT

The Cursor Position and Vertical Interrupt signal are available when Composite Sync and Blank signals are selected and bit 2 of the Status Register is set to the value of 1. The cursor position generates a single pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active LOW (HIGH) signals specified by the registers used for generating Horizontal and Vertical Gating signals. The Vertical Interrupt signal generates a pulse during the vertical interval specified. The Vertical Interrupt signal will change in the same manner as that specified for the Vertical Blanking signal.

Horizontal Cursor Width = [REG(16) − REG(15)] × ckper

Vertical Cursor Width = [REG(18) − REG(17)] × hper

Vertical Interrupt Width = [REG(14) − REG(13)] × hper

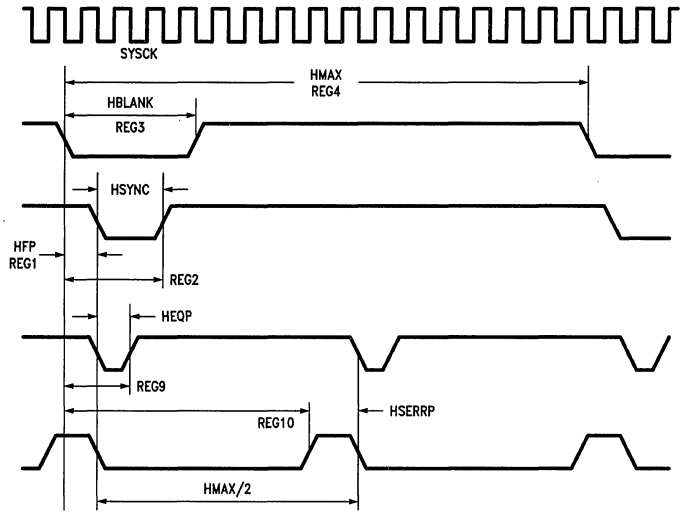

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FIGURE 1. Horizontal Waveform Specification

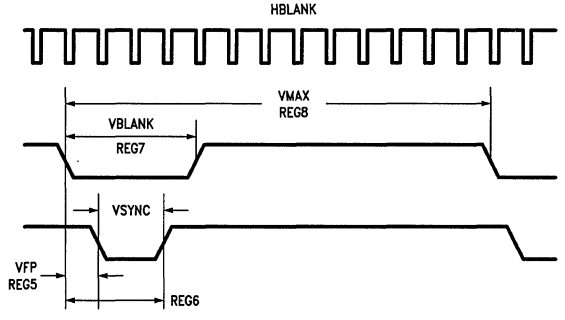

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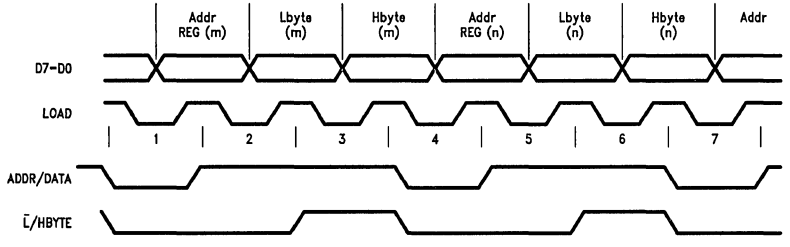
FIGURE 2. Vertical Waveform Specification

Addressing Logic

The register addressing logic is composed of two blocks of logic. The first is the address register and counter (ADDRCNTR), and the second is the address decode (ADDRDEC).

ADDRCNTR LOGIC

Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 Load cycles (19 Address and 38 Data cycles). Auto Addressing requires that only the initial register value be specified. The Auto Load sequence would require only 39 Load cycles to completely program all registers (1 Address and 38 Data). In the auto load sequence the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the time the High Byte is written the address counter is incremented by 1. The counter has been implemented to loop on the initial value loaded into the address register. For example: If a value of 0 was written into the address register then the counter would count from 0 to 18 before resetting back to 0. If a value of 15 was written into the address register then the counter would count from 15 to 18 before looping back to 15. If a value greater than or equal to 18 is placed into the address register the counter will continuously loop on this value. Auto addressing is initiated on the falling edge of load when ADDRDATA is 0 and LHBYTE is 1. Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDRDATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto Incrementing is disabled on the falling edge of load after ADDRDATA and LHBYTE goes low.



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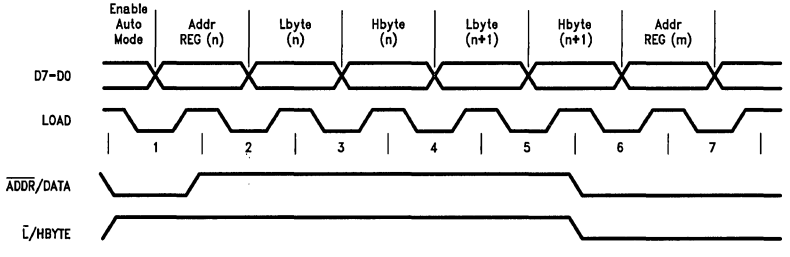
Manual Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Manual Addressing	Load Address m
2	Enable Lbyte Data Load	Load Lbyte m
3	Enable Hbyte Data Load	Load Hbyte m
4	Enable Manual Addressing	Load Address n
5	Enable Lbyte Data Load	Load Lbyte n
6	Enable Hbyte Data Load	Load Hbyte n



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Auto Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Auto Addressing	Load Start Address n
2	Enable Lbyte Data Load	Load Lbyte (n)
3	Enable Hbyte Data Load	Load Hbyte (n); Inc Counter
4	Enable Lbyte Data Load	Load Lbyte (n+1)
5	Enable Hbyte Data Load	Load Hbyte (n+1); Inc Counter
6	Enable Manual Addressing	Load Address

Addressing Logic (Continued)

ADDRDEC LOGIC

The ADDRDEC logic decodes the current address and generates the enable signal for the appropriate register. The enable values for the registers and counters change on the falling edge of LOAD. Since the data registers are disabled at this time any overlap of enable signals will not cause register data to change. The following Addresses are used by the device.

Address 0 Status Register REG0
Address 1–18 Data Registers REG1–REG18
Address 19–21 Unused
Address 22/54 Restart Vector (Restarts Device)
Address 23/55 Clear Vector (Zeros All Registers)
Address 24–31 Unused
Address 32–50 Register Scan Addresses
Address 51–53 Counter Scan Addresses
Address 56–63 Unused

At any given time only one register at most is selected. It is possible to have no registers selected.

VECTORED CLEAR ADDRESS

Addresses 23 (17H) or 55 (37H) is used to clear all registers simultaneously. This function may be desirable to use prior to loading new data into the Data or Status Registers. This address is read into the device in a similar fashion as all of the other registers.

VECTORED RESTART ADDRESS

The function of addresses 22 (16H) or 54 (36H) are similar to that of the CLR pin except that the programming of the registers is not affected. It is recommended but not required that this address is read after the initial device configuration load sequence.

SCAN MODE LOGIC

A scan mode is available in the ACT715/LM1882 that allows the user to non-destructively verify the contents of the registers. Scan mode is invoked through reading a scan address into the address register. The scan address of a given register is defined by the Data register address + 32. The internal Clocking signal is disabled when a scan address is read. Disabling the clock freezes the device in it's present state. Data can then be serially scanned out of the data registers through the ODD/EVEN Pin. The value of the two horizontal counters and 1 vertical counter can also be scanned out by using address numbers 51–53.

Normal device operation can be resumed by latching in a non-scan address. As the scanning of the registers is a non-destructive scan, the device will resume correct operation from the point at which it was halted.

RS170 Default Register Values

The tables below show the values programmed for the RS170 Format and how they compare against the actual EIA RS170 Specifications. The default signals that will be displayed are CSYNC, CBLANK, HDRIVE and VDRIVE. The device initially starts at the beginning of the odd field of interlace. All signals have active low pulses and the clock is disabled at power up. Registers 13 and 14 are not involved in the actual signal information. If the Vertical Interrupt was selected a pulse indicating the active lines would be displayed.

Reg	D Value	H	Register Description
REG0	0	000	Status Register
REG1	23	017	HFP End Time
REG2	91	05B	HSYNC Pulse End Time
REG3	157	09D	HBLANK Pulse End Time
REG4	910	38E	Total Horizontal Clocks
REG5	7	007	VFP End Time
REG6	13	00D	VSYNC Pulse End Time
REG7	41	029	VBLANK Pulse End Time
REG8	525	20D	Total Vertical Lines
REG9	57	038	Equalization Pulse End Time
REG10	410	19A	Serration Pulse Start Time
REG11	1	001	Pulse Interval Start Time
REG12	19	013	Pulse Interval End Time
REG13	41	029	Vertical Interrupt Activate Time
REG14	526	20E	Vertical Interrupt Deactivate Time
REG15	911	38F	Horizontal Drive Start Time (1)
REG16	92	05C	Horizontal Drive End Time
REG17	1	001	Vertical Drive Start Time
REG18	21	015	Vertical Drive End Time

	Rate	Period
Input Clock	14.31818 MHz	69.841 ns
Line Rate	15.73426 kHz	63.556 μs
Field Rate	59.94 Hz	16.683 ms
Frame Rate	29.97 Hz	33.367 ms

Signal	Width	μs	%H	Specification (μs)
HFP	22 Clocks	1.536		1.5 ±0.1
HSYNC Width	68 Clocks	4.749	7.47	4.7 ±0.1
HBLANK Width	156 Clocks	10.895	17.15	10.9 ±0.2
HDRIVE Width	91 Clocks	6.356	10.00	0.1H ±0.005H
HEQP Width	34 Clocks	2.375	3.74	2.3 ±0.1
HSERR Width	68 Clocks	4.749	7.47	4.7 ±0.1
HPER IOD	910 Clocks	63.556	100	

RS170 Default Register Values (Continued)

Signal	Width	μs	%V	Specification
VFP	3 Lines	190.67		6 EQP Pulses
VSYNC Width	3 Lines	190.67		6 Serration Pulses
VBLANK Width	20 Lines	1271.12	7.62	0.075V ± 0.005V
VDRIVE Width	11.0 Lines	699.12	4.20	0.04V ± 0.006V
VEQP Intrvl	9 Lines		3.63	9 Lines/Field
VPERIOD (field)	262.5 Lines	16.683 ms		16.683 ms/Field
VPERIOD (frame)	525 Lines	33.367 ms		33.367 ms/Frame

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source or Sink Current (I_O) ±15 mA

DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND}) ±20 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'ACT/LM1882 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74ACT/LM1882 −40°C to +85°C
- 54ACT/LM1882 −55°C to +125°C

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'AC Devices
V_{IN} from 30% to 70% of V_{CC}
V_{CC} @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'ACT/LM1882 Devices
V_{IN} from 0.8V to 2.0V
V_{CC} @ 4.5V, 5.5V 125 mV/ns

DC Characteristics For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF		54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4		4.4	V	$I_{OUT} = -50$ μA
		5.5	5.49	5.4		5.4	V	
		4.5		3.86		3.76	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		4.86		4.76	V	$I_{OH} = -8$ mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1		0.1	V	$I_{OUT} = 50$ μA
		5.5	0.001	0.1		0.1	V	
		4.5		0.36		0.44	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		0.36		0.44	V	$I_{OH} = +8$ mA
I_{OLD}	Minimum Dynamic Output Current	5.5				32.0	mA	$V_{OLD} = 1.65V$

*All outputs loaded; thresholds on input associated with input under test.

DC Characteristics

For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified) (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF		54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OHD}	Minimum Dynamic Output Current	5.5				−32.0	mA	$V_{OHD} = 3.85V$
I_{IN}	Maximum Input Leakage Current	5.5		±0.1		±1.0	μA	$V_I = V_{CC}$, GND
I_{CC}	Supply Current Quiescent	5.5		8.0		80	μA	$V_{IN} = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6			1.5	mA	$V_{IN} = V_{CC} - 2.1V$

Note 1: Test Load 50 pF, 500Ω to Ground.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$, $C_L = 50$ pF			54ACT/LM1882 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT/LM1882 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{MAXI}	Interlaced f_{MAX} (HMAX/2 is ODD)	5.0	170	190				150		MHz	
f_{MAX}	Non-Interlaced f_{MAX} (HMAX/2 is EVEN)	5.0	190	220				175		MHz	
t_{PLH1} t_{PHL1}	Clock to Any Output	5.0	4.0	13.0	15.5			3.5	18.5	ns	2–3, 4
t_{PLH2} t_{PHL2}	Clock to ODDEVEN (Scan Mode)	5.0	4.5	15.0	17.0			3.5	20.5	ns	2–3, 4
t_{PLH3}	Load to Outputs	5.0	4.0	11.5	16.0			3.0	19.5	ns	2–3, 4

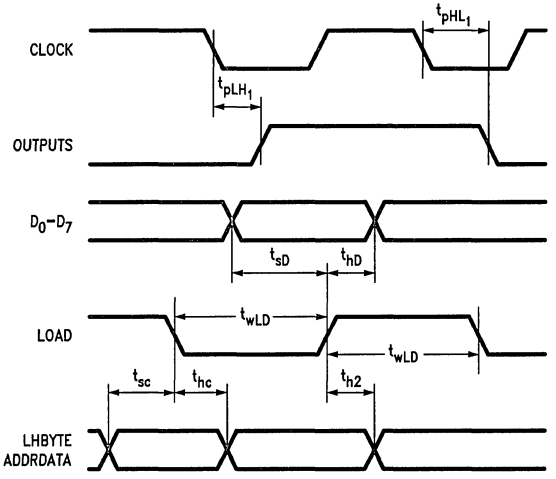
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	17.0	pF	$V_{CC} = 5.0V$

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$		54ACT/LM1882 $T_A = -55°C$ to $+125°C$	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units	Fig. No.
			Typ	Guaranteed Minimums				
	Control Setup Time							
t_{sc}	ADDR/DATA to LOAD−	5.0	3.0	4.0		4.5	ns	2–7
t_{sc}	L/HBYTE to LOAD−		3.0	4.0		4.5	ns	2–7
	Data Setup Time							
t_{sd}	D7–D0 to LOAD+	5.0	2.0	4.0		4.5	ns	2–7
	Control Hold Time							
t_{hc}	LOAD− to ADDR/DATA	5.0	0	1.0		1.0	ns	2–7
	LOAD− to L/HBYTE		0	1.0		1.0	ns	2–7
	Data Hold Time							
t_{hd}	LOAD+ to D7–D0	5.0	1.0	2.0		2.0	ns	2–7
t_{rec}	LOAD+ to CL− (Note 1)	5.0	5.5	7.0		8.0	ns	2–3, 7
	Pulse Width							
t_{wld-}	Load Low	5.0	3.0	5.5		5.5	ns	2–3
t_{wld+}	Load High	5.0	3.0	5.0		7.5	ns	2–3
t_{wclr}	CLR Pulse Width HIGH	5.0	5.5	6.5		9.5	ns	2–3
t_{wck}	CLOCK Width (High or Low)	5.0	2.5	3.0		3.5	ns	2–3

Note 1: Removal of Vectored Reset to Clock.



TL/F/10137–6

FIGURE 3. AC Specifications

National Semiconductor

54ACT/74ACT818
8-Bit Diagnostic Register

General Description

The 'ACT818 is a high-speed, general-purpose pipeline register with an on-board diagnostic register for performing serial diagnostics and/or writable control store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the diagnostic register to operate as a right-shift-only register. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with 'ACT818 diagnostic pipeline registers. The loop can be used to scan in a complete test routine starting point (Data, Address, etc.). Then after a specified number of machine cycles it scans out the results to be inspected for the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

Features

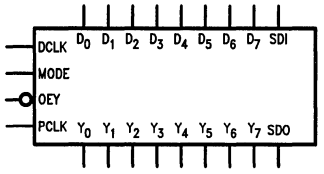
- On-line and off-line system diagnostics
- Swaps the contents of diagnostic register and output register
- Diagnostic register and diagnostic testing
- Cascadable for wide control words as used in microprogramming
- Edge-triggered D registers
- Outputs source/sink 24 mA
- 'ACT818 has TTL-compatible inputs
- 'ACT818 is functionally- and pin-compatible to AMD Am29818 and MMI 74S818

Applications

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/serial-parallel converter

Ordering Code: See Section 8

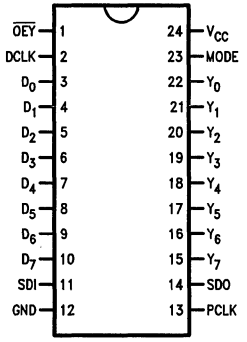
Logic Symbol



TL/F/9801–3

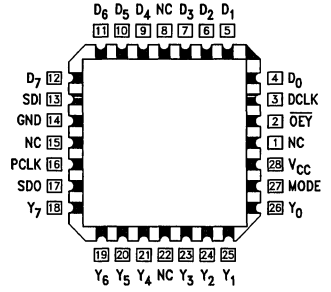
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9801–1

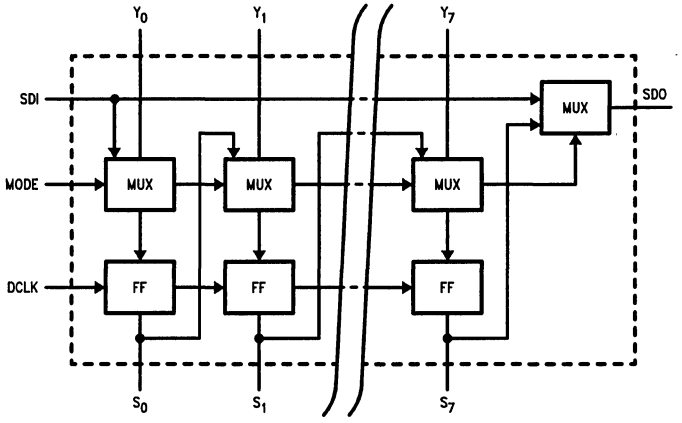
Pin Assignment for LCC and PCC



TL/F/9801–2

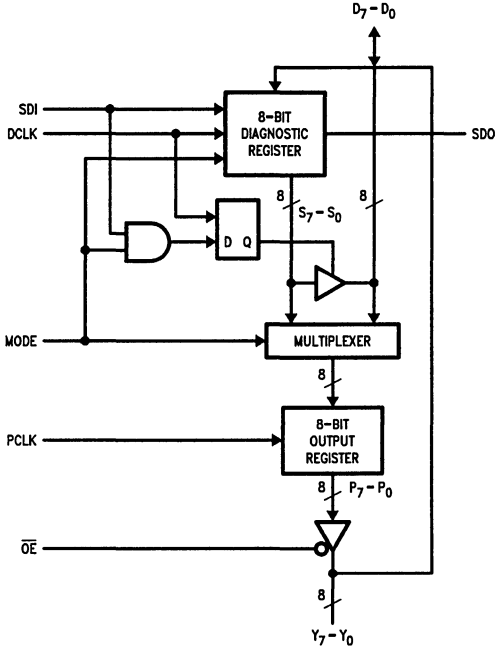
Pin Names	Description
D_0–D_7	Data Inputs
SDI	Serial Data Input
DCLK	Diagnostics Clock
MODE	Control Input
PCLK	Pipeline Register Clock
$\overline{OEY}$	Output Enable Input
SDO	Serial Data Output
Y_0–Y_7	Data Outputs

Diagnostic Register



TL/F/9801–4

Block Diagram



TL/F/9801–5

Functional Description

Data transfers into the diagnostic register occur on the LOW-to-HIGH transition of DCLK. Mode and SDI determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. Mode selects whether the data source is the data input or the diagnostic register output. Because of the independence of the clock inputs, data can be shifted in the diagnostic register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously, as long as no setup or hold times are violated. This simultaneous operation is legal.

Function Table

Inputs				Outputs			Operation
SDI	MODE	DCLK	PCLK	SDO	Diagnostic Reg.	Pipeline Reg.	
X	L	⌐‾	X	S7	SI<SI − 1, SO<SD_I	NA	Serial Shift; D_7–D_0 Disabled
X	L	X	⌐‾	S7	NA	PI<DI	Normal Load Pipeline Register
L	H	⌐‾	X	L	SI<YI	NA	Load Diagnostic Register from Y; DI Disabled
X	H	X	⌐‾	SDI	NA	PI<SI	Load Pipeline Register from Diagnostic Register
H	H	⌐‾	X	H	Hold	NA	Hold Diagnostic Register; DI Enabled

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐‾ = LOW-to-HIGH Clock Transition

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V_{OUT} = 0.1V or V_{CC} − 0.1V
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±10.0	±1.0	μA	V_{IN} = V_{CC}
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$\overline{OE}$ = V_{IH} V_{OUT} = 0V, V_{CC}
I_{CC}	Maximum Quiescent Supply Current	5.5		1.0			mA	V_{IN} = V_{CC} or GND
I_{CCT}	Maximum Additional I_{CC}/Input	5.5			1.6	1.5	mA	V_{IN} = V_{CC} − 2.1V V_{CC} = 5.5V
V_{OH}	Minimum HIGH Level Output Voltage, Y_0–Y_7 Outputs	4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V V	*V_{IN} = V_{IL} or V_{IH} I_{OH} = −24 mA I_{OH} = −24 mA
	Minimum HIGH Level Output Voltage, D_0–D_7, SDO Outputs	4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V V	I_{OH} = −8 mA I_{OH} = −8 mA
V_{OL}	Maximum LOW Level Output Voltage, Y_0–Y_7 Outputs	4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V V	*V_{IN} = V_{IL} or V_{IH} I_{OL} = 24 mA I_{OL} = 24 mA
	Maximum LOW Level Output Voltage, D_0–D_7, SDO Outputs	4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V V	I_{OL} = 8 mA I_{OL} = 8 mA
I_{OLD}	Minimum Dynamic Output Current, Y_0–Y_7 Outputs	5.5			50	75	mA	V_{OLD} = 1.65V Max

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OHD}	Minimum Dynamic Output Current, Y_0–Y_7 Outputs	5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{OLD}	Minimum Dynamic Output Current, D_0–D_7, SDO Outputs (Note 1)	5.5			32	32	mA	V_{OLD} = 1.65V Max
I_{OHD}	Minimum Dynamic Output Current, D_0–D_7, SDO Outputs (Note 1)	5.5			−32	−32	mA	V_{OHD} = 3.85V Min

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Test load 50 pF, 500Ω to ground.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay PCLK to Y	5.0	3.0	6.0	9.0	1.5	10.5	2.5	9.5	ns	2–3, 4
t_{PLH}	Propagation Delay PCLK to Y	5.0	3.0	6.5	9.0	1.5	11.0	2.5	10.0	ns	2–3, 4
t_{PHL}	Propagation Delay MODE to SDO	5.0	4.0	8.0	11.0	1.5	13.0	3.5	12.0	ns	2–3, 4
t_{PLH}	Propagation Delay MODE to SDO	5.0	4.0	8.0	11.5	1.5	14.0	4.0	12.5	ns	2–3, 4
t_{PHL}	Propagation Delay SDI to SDO	5.0	3.5	7.5	10.5	1.5	12.5	3.0	12.0	ns	2–3, 4
t_{PLH}	Propagation Delay SDI to SDO	5.0	3.5	7.5	10.5	1.5	13.0	3.5	12.0	ns	2–3, 4
t_{PHL}	Propagation Delay DCLK to SDO	5.0	4.5	9.0	12.5	1.5	15.5	4.0	14.0	ns	2–3, 4
t_{PLH}	Propagation Delay DCLK to SDO	5.0	4.5	9.5	13.0	1.5	16.0	4.0	14.5	ns	2–3, 4
t_{PZL}	Output Enable Time $\overline{OEY}$ to Y_n	5.0	2.5	6.0	9.0	1.5	11.0	2.5	10.0	ns	2–6
t_{PLZ}	Output Disable Time $\overline{OEY}$ to Y_n	5.0	1.5	5.5	8.0	1.5	9.5	1.0	9.0	ns	2–6
t_{PZL}	Output Enable Time DCLK to D_n	5.0	3.0	8.0	12.0	1.5	15.0	3.0	13.5	ns	2–6
t_{PLZ}	Output Disable Time DCLK to D_n	5.0	2.0	8.5	11.0	1.5	13.0	1.5	12.0	ns	2–6
t_{PZH}	Output Enable Time $\overline{OEY}$ to Y_n	5.0	3.0	8.0	10.0	1.5	12.0	2.5	11.0	ns	2–5
t_{PHZ}	Output Disable Time $\overline{OEY}$ to Y_n	5.0	2.5	9.0	11.0	1.5	13.0	2.0	11.5	ns	2–5
t_{PZH}	Output Enable Time DCLK to D_n	5.0	3.0	6.5	11.5	1.5	14.0	3.0	13.0	ns	2–5
t_{PHZ}	Output Disable Time DCLK to D_n	5.0	3.0	7.5	12.0	1.5	14.0	2.0	13.0	ns	2–5

*Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time D to PCLK	5.0	1.0	4.0	6.0	5.0	ns	2–7
t_h	Hold Time D to PCLK	5.0	0.0	1.0	1.5	1.0	ns	2–7
t_s	Setup Time MODE to PCLK	5.0	2.5	4.5	6.5	5.5	ns	2–7
t_h	Hold Time MODE to PCLK	5.0	−1.0	0.0	0.5	0.0	ns	2–7
t_s	Setup Time Y to DCLK	5.0	0.5	2.5	3.5	2.5	ns	2–7
t_h	Hold Time Y to DCLK	5.0	0	1.0	2.0	1.5	ns	2–7
t_s	Setup Time MODE to DCLK	5.0	2.0	4.0	5.0	4.0	ns	2–7
t_h	Hold Time MODE to DCLK	5.0	−0.5	1.0	1.5	1.0	ns	2–7
t_s	Setup Time SDI to DCLK	5.0	2.0	3.5	5.5	4.5	ns	2–7
t_h	Hold Time SDI to DCLK	5.0	−0.5	1.0	1.5	1.0	ns	2–7
t_s	Setup Time DCLK to PCLK	5.0	6.0	9.0	12.0	10.5	ns	2–7
t_s	Setup Time PCLK to DCLK	5.0	6.0	11.0	12.5	11.5	ns	2–7
t_w	Pulse Width PCLK HIGH or LOW	5.0	2.0	3.0	4.5	3.0	ns	2–3
t_w	Pulse Width DCLK HIGH or LOW	5.0	2.0	3.0	4.5	3.0	ns	2–3

Note 1: Test load 50 pF, 500Ω to ground.

*Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	20	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC821 • 54ACT/74ACT821
10-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

The 'AC/'ACT821 is a 10-bit D flip-flop with TRI-STATE outputs arranged in a broadside pinout.

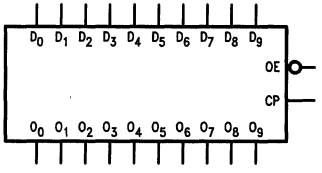
The 'AC/'ACT821 is functionally identical to the AM29821.

Features

- TRI-STATE outputs for bus interfacing
- Noninverting outputs
- Outputs source/sink 24 mA
- 'ACT821 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'ACT821: 5962-88705

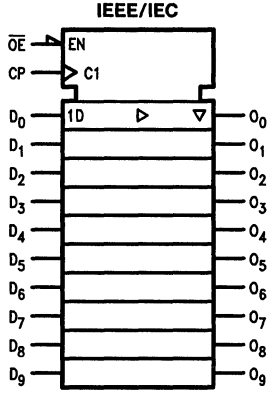
Ordering Code: See Section 8

Logic Symbols



TL/F/10139–1

IEEE/IEC



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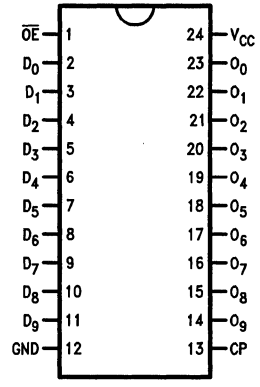
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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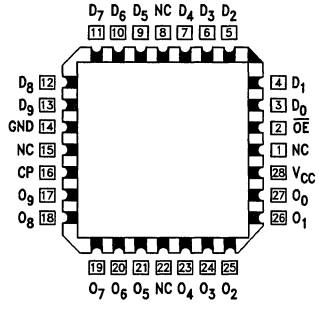
Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	Data Outputs
$\overline{OE}$	Output Enable Input
CP	Clock Input

Pin Assignment for LCC



TL/F/10139–4

Functional Description

The 'AC/'ACT821 consists of ten D-type edge-triggered flip-flops. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

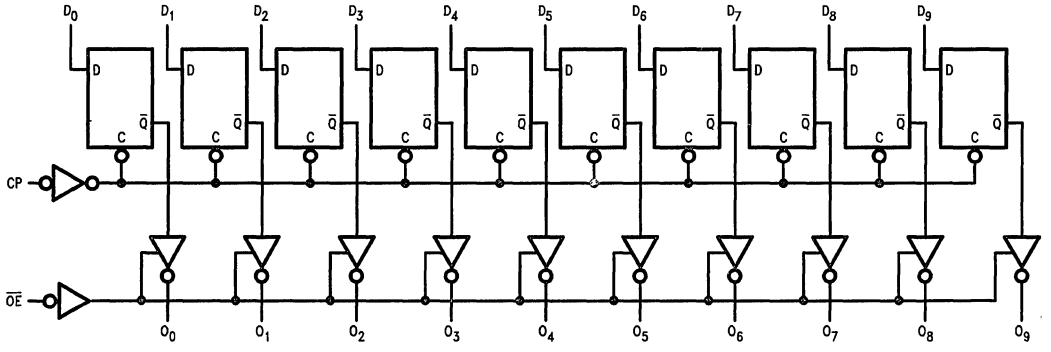
The 'AC/'ACT821 is functionally and pin compatible with the AM29821.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	⌐	L	L	Z	High Z
H	⌐	H	H	Z	High Z
L	⌐	L	L	L	Load
L	⌐	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
Z = HIGH Impedance
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE® Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	110 120	145 160		95 100		100 110		MHz	
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0	3.0 2.0	8.0 6.0	13.0 9.5	1.0 1.0	16.0 11.5	3.0 2.0	15.0 10.5	ns	2-3, 4
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0	3.0 2.0	8.0 5.5	13.0 9.5	1.0 1.0	16.0 11.5	3.0 2.0	15.0 10.5	ns	2-3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.0 4.5	11.0 8.0	1.0 1.0	13.0 10.0	2.5 1.5	12.0 9.0	ns	2-5
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.5 5.0	11.0 8.0	1.0 1.0	13.5 10.0	2.5 1.5	12.0 9.0	ns	2-6
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.5 5.0	10.5 8.0	1.0 1.0	12.0 10.0	2.5 1.5	11.0 8.5	ns	2-5
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0	2.5 1.5	6.0 4.5	10.5 8.0	1.0 1.0	12.0 10.0	2.5 1.5	11.0 8.5	ns	2-6

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −1.0	1.5 1.5	2.5 2.5	1.5 1.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −1.0	3.5 3.5	4.0 4.0	4.0 4.0	ns	2-7
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.0 4.0	6.0 5.0	5.5 4.0	ns	2-3

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	150		85		110		MHz	
t_{PLH}	Propagation Delay CP to O_n	5.0	2.0	6.0	9.5	1.0	11.5	1.5	10.5	ns	2-3, 4
t_{PHL}	Propagation Delay CP to O_n	5.0	2.5	6.0	9.5	1.0	11.5	2.0	10.5	ns	2-3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	7.0	10.5	1.0	12.5	2.0	11.5	ns	2-5
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	7.0	10.5	1.0	13.0	2.0	12.0	ns	2-6
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	7.5	12.0	1.0	13.5	1.0	13.0	ns	2-5
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	7.0	10.5	1.0	12.5	1.0	11.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.5	2.0	4.0	2.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	2.0	3.0	2.5	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0	3.0	4.5	6.0	5.5	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	35.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACT/74ACT823
9-Bit D Flip-Flop

General Description

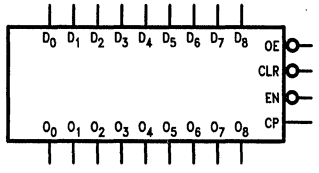
The 'ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The 'ACT823 offers noninverting outputs and is fully compatible with AMD's Am29823.

Features

- Outputs source/sink 24 mA
- TRI-STATE® outputs for bus interfacing
- Inputs and outputs are on opposite sides
- 'ACT823 has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbols



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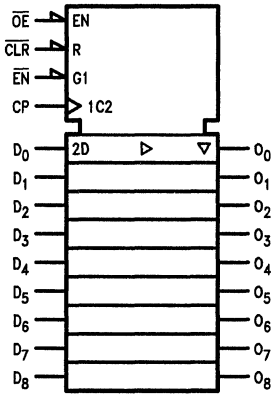
IEEE/IEC



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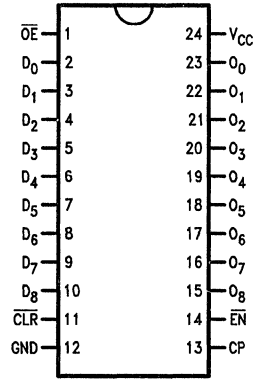
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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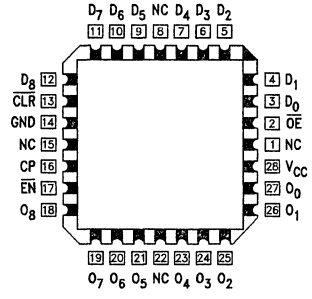
Pin Assignment for LCC



TL/F/9894–4

Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

Functional Description

The 'ACT823 consists of nine D-type edge-triggered flip-flops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These devices are ideal for parity bus interfacing in high performance systems.

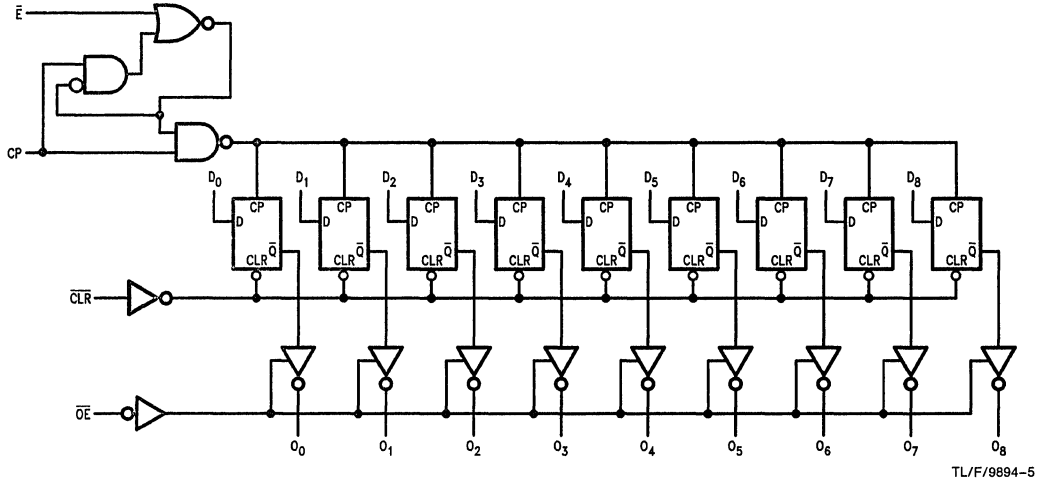
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	↗	L	L	Z	High Z
H	X	L	↗	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 4.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level	4.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50pF$			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	158		95		109		MHz	
t_{PLH}	Propagation Delay CP to O_n	5.0	1.5	5.5	9.5	1.0	12.0	1.5	10.5	ns	2-3, 4
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	5.5	9.5	1.0	12.0	1.5	10.5	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0	2.5	8.0	13.5	1.0	18.0	2.0	15.5	ns	2-3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	11.5	1.5	11.5	ns	2-5
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.0	6.5	11.0	1.0	12.0	1.5	12.0	ns	2-6
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.5	11.0	1.0	13.5	1.5	12.0	ns	2-5
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	12.0	1.5	11.5	ns	2-6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D to CP	5.0	0.5	2.5	4.0	2.5	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	2.5	3.0	2.5	ns	2-7
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	2.0	4.0	2.5	ns	2-7
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	1.0	3.0	1.0	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	4.5	6.0	5.5	ns	2-3
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	3.0	5.5	7.0	5.5	ns	2-3
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5	3.5	4.5	4.0	ns	2-3, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACT/74ACT825
8-Bit D Flip-Flop

General Description

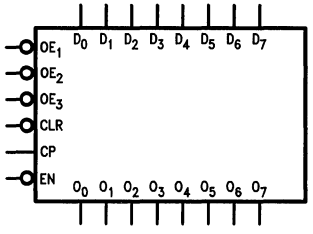
The 'ACT825 is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The 'ACT825 has noninverting outputs and is fully compatible with AMD's Am29825.

Features

- Outputs source/sink 24 mA
- Inputs and outputs are on opposite sides
- 'ACT825 has TTL-compatible inputs

Ordering Code: See Section 8

Logic Symbols



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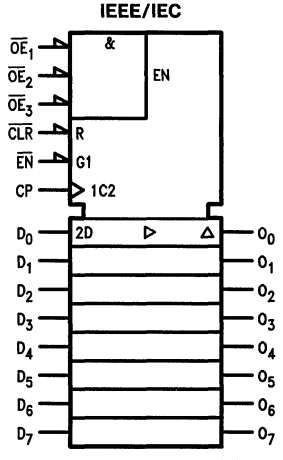
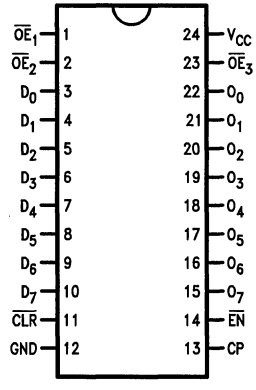
IEEE/IEC



TL/F/9895–3

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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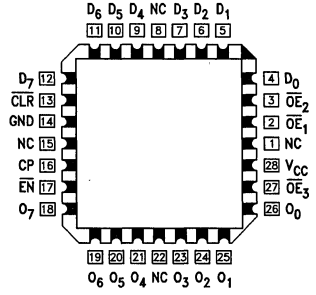
Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output Enables
$\overline{EN}$	Clock Enable
$\overline{CLR}$	Clear
CP	Clock Input

Pin Assignment for LCC



TL/F/9895–4

Functional Description

The 'ACT825 consists of eight D-type edge-triggered flip-flops. These devices have TRI-STATE® outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}_1$, $\overline{OE}_2$ and $\overline{OE}_3$ LOW, the contents of the flip-flops are available at the outputs. When one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the outputs go to the high impedance state.

Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The 'ACT825 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

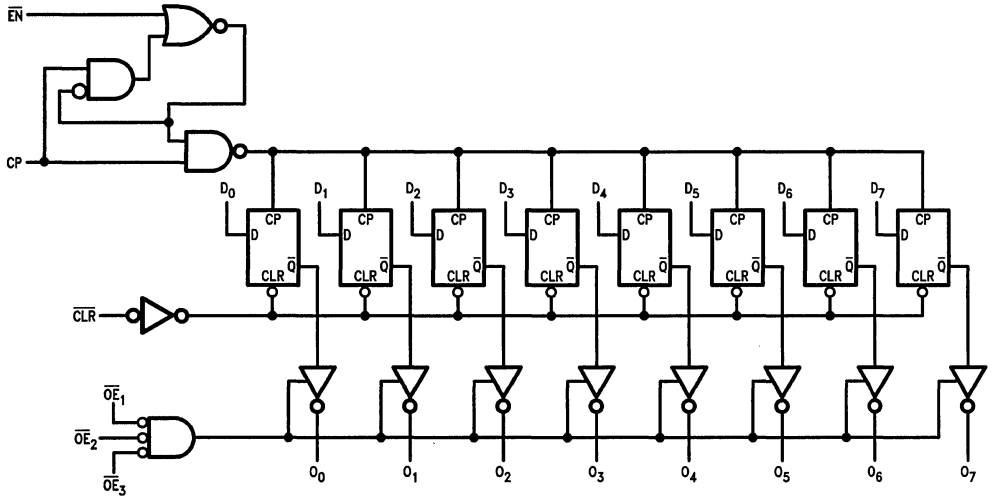
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D_n	Q	O	
H	X	L	↗	L	L	Z	High-Z
H	X	L	↗	H	H	Z	High-Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/9895–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to 7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) +0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current Per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74AC/ACT −40°C to +85°C
- 54AC/ACT −55°C to +125°C

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'AC Devices
V_{IN} from 30% to 70% of V_{CC}
V_{CC} @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'ACT Devices
V_{IN} from 0.8V to 2.0V
V_{CC} @ 4.5V, 5.5V 125 mV/ns

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} −2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	158		95		109		MHz	
t_{PLH}	Propagation Delay CP to O_n	5.0	1.5	5.5	9.5	1.0	11.5	1.5	10.5	ns	2–3, 4
t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	5.5	9.5	1.0	11.5	1.5	10.5	ns	2–3, 4
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0	2.5	8.0	13.5	1.0	18.0	2.0	15.5	ns	2–3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	11.5	1.5	11.5	ns	2–5
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.0	6.5	11.0	1.0	12.5	1.5	12.0	ns	2–6
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.5	11.0	1.0	13.5	1.5	12.0	ns	2–5
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.5	6.0	10.5	1.0	13.0	1.5	11.5	ns	2–6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	0.5	2.5	4.0	2.5	ns	2–7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	2.5	3.0	2.5	ns	2–7
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	2.0	4.0	2.5	ns	2–7
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	0	1.0	3.0	1.0	ns	2–7
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	4.5	6.0	5.5	ns	2–3
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	3.0	5.5	7.0	5.5	ns	2–3
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5	3.5	4.5	4.0	ns	2–3, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACT/74ACT841
10-Bit Transparent Latch with TRI-STATE® Outputs

General Description

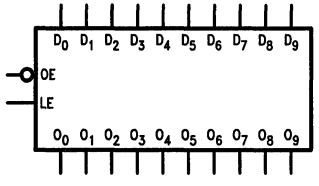
The 'ACT841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'ACT841 is a 10-bit transparent latch, a 10-bit version of the 'ACT373.

Features

- 'ACT841 has TTL-compatible inputs
- Outputs source/sink 24 mA
- Non-inverting TRI-STATE outputs

Ordering Code: See Section 8

Logic Symbols



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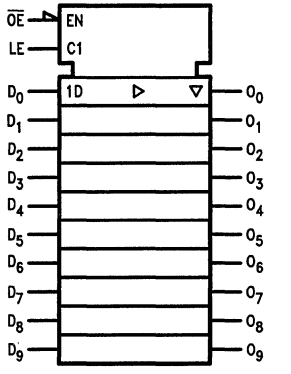
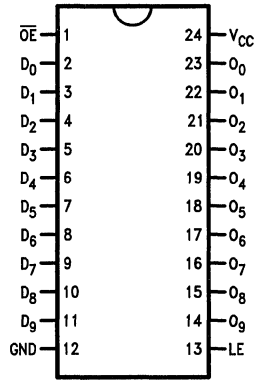


TL/F/10156–2

Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	TRI-STATE Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable

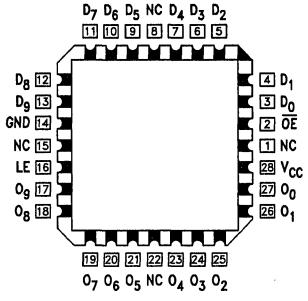
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10156–3

Pin Assignment for LCC



TL/F/10156–4

Functional Description

The ACT841 consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

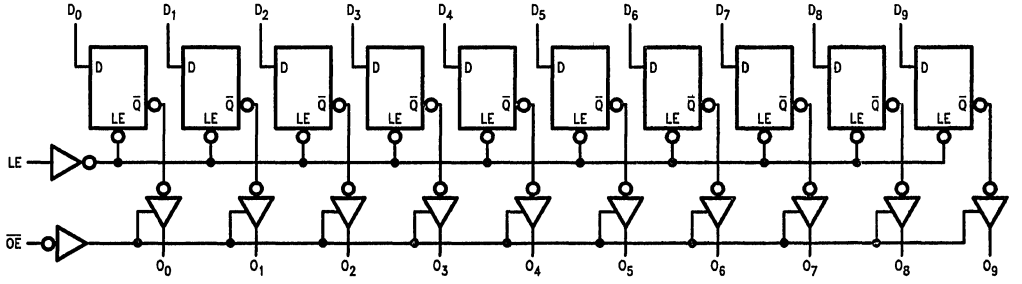
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/10156–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate progagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	μA	V_I = V_{CC} − 2.1V

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74ACT $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	2.0	5.5	9.5	1.0	11.0	2.0	10.0	ns	2–3, 4
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.0	5.5	9.5	1.0	11.0	2.0	10.0	ns	2–3, 4
t_{PLH}	Propagation Delay LE to O_n	5.0	2.0	5.5	9.0	1.0	11.0	2.0	10.0	ns	2–3, 4
t_{PHL}	Propagation Delay LE to O_n	5.0	2.0	5.5	9.0	1.0	11.0	2.0	10.0	ns	2–3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.0	5.5	9.5	1.0	11.0	2.0	10.5	ns	2–5, 6
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.0	5.5	9.5	1.0	11.0	2.0	10.5	ns	2–5, 6
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	2.0	6.0	10.5	1.0	12.0	2.0	11.0	ns	2–5, 6
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	2.0	6.0	10.5	1.0	12.0	2.0	11.0	ns	2–5, 6

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	−0.5	0.5	3.0	1.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0.5	2.0	2.0	2.0	ns	2-7
t_w	LE Pluse Width, HIGH	5.0	2.0	3.5	5.0	3.5	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC843 • 54ACT/74ACT843
8-Bit Transparent Latch

General Description

The 'AC/'ACT843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths.

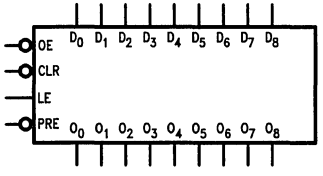
The 'AC/'ACT843 is functionally and pin compatible with AMD's Am29843.

Features

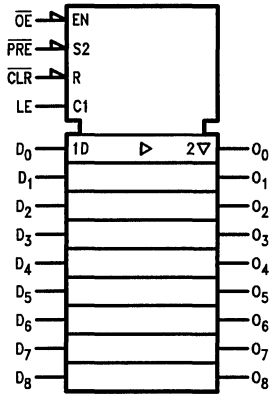
- 'ACT843 has TTL-compatible inputs
- TRI-STATE® outputs for bus interfacing

Ordering Code: See Section 8

Logic Symbols



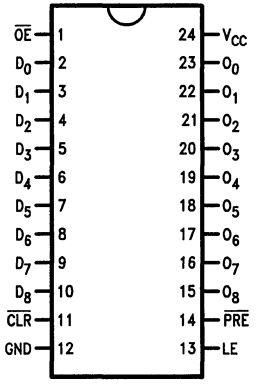
TL/F/9800–1



TL/F/9800–3

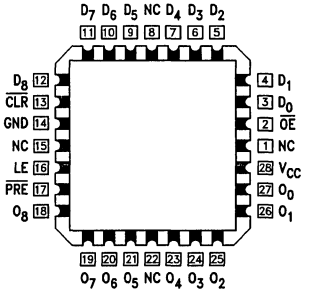
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9800–2

Pin Assignment for LCC



TL/F/9800–4

Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

Functional Description

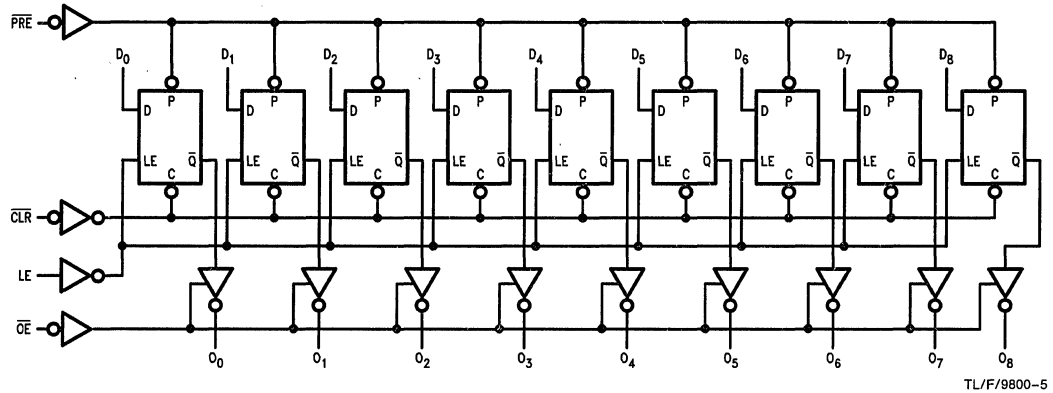
The 'AC/'ACT843 consists of nine D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. In addition to the LE and $\overline{OE}$ pins, the 'AC/'ACT843 has a Clear ($\overline{CLR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

Function Tables

Inputs					Internal	Outputs	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O	
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Clear/High Z
H	L	H	L	X	H	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/9800–5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} +0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} +0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} +0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} +0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46		−12 mA
		4.5		3.86	3.7	3.76	V	I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44		12 mA
		4.5		0.36	0.50	0.44	V	I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$ Typ	74AC $T_A = +25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3	3.5	6.5	12.0	1.0	14.0	2.5	13.0	ns	2–3, 4
		5.0	2.0	4.5	8.5	1.0	10.0	1.5	9.0		
t_{PHL}	Propagation Delay D_n to O_n	3.3	4.0	7.0	12.0	1.0	14.0	3.0	13.0	ns	2–3, 4
		5.0	2.5	5.0	8.5	1.0	10.0	1.5	9.0		
t_{PLH}	Propagation Delay LE to O_n	3.3	3.5	6.5	12.0	1.0	14.0	2.5	13.0	ns	2–3, 4
		5.0	2.0	4.5	8.5	1.0	10.0	1.5	9.0		
t_{PHL}	Propagation Delay LE to O_n	3.3	4.0	7.0	12.0	1.0	14.0	3.0	13.0	ns	2–3, 4
		5.0	2.5	5.0	8.5	1.0	10.0	1.5	9.0		
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	3.3	5.5	8.5	19.0	1.0	23.5	4.5	21.5	ns	2–3, 4
		5.0	3.5	6.0	13.0	1.0	16.0	2.5	14.5		
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3	7.5	11.0	21.5	1.0	26.5	6.0	24.0	ns	2–3, 4
		5.0	5.0	7.5	15.0	1.0	19.0	4.0	17.0		
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3	3.5	6.0	11.0	1.0	13.0	3.0	12.0	ns	2–5, 6
		5.0	2.0	4.5	8.0	1.0	10.0	1.5	9.0		
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3	4.0	6.5	11.0	1.0	13.0	2.5	12.0	ns	2–5, 6
		5.0	2.0	5.0	8.0	1.0	10.0	1.5	9.0		
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3	4.0	6.5	10.5	1.0	12.0	3.5	11.0	ns	2–5, 6
		5.0	3.0	5.0	8.0	1.0	9.0	2.5	8.5		
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3	3.0	6.0	10.5	1.0	12.0	2.5	11.0	ns	2–5, 6
		5.0	2.0	4.5	8.0	1.0	9.0	1.5	8.5		
t_{PHL}	Propagation Delay $\overline{PRE}$ to O_n	3.3	4.5	7.0	12.5	1.0	15.0	3.5	13.5	ns	2–3, 4
		5.0	3.0	5.0	9.0	1.0	10.5	2.0	9.5		
t_{PLH}	Propagation Delay $\overline{CLR}$ to O_n	3.3	4.5	7.0	12.5	1.0	15.0	3.5	13.5	ns	2–3, 4
		5.0	3.0	5.0	9.0	1.0	10.5	2.0	9.5		

*Voltage Range 3.3 is 3.3V ±0.3V

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3	0	3.0	3.5	3.5	ns	2–7
		5.0	−0.5	1.5	2.0	2.0		
t_h	Hold Time, HIGH or LOW D_n to LE	3.3		2.0	2.0	2.0	ns	2–7
		5.0	−0.5	2.5	2.5	2.5		
t_w	LE Pulse Width, HIGH	3.3	1.5	3.0	3.5	3.0	ns	2–3
		5.0	1.5	3.0	3.0	3.0		
t_w	$\overline{PRE}$ Pulse Width, LOW	3.3	5.0	12.0	16.0	14.5	ns	2–3
		5.0	3.0	8.5	11.0	10.0		
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3	5.5	14.0	18.5	16.5	ns	2–3
		5.0	4.0	10.0	13.0	12.0		
t_{rec}	$\overline{PRE}$ Recovery Time	3.3	1.0	3.0	3.5	3.0	ns	2–3,7
		5.0	0	1.5	1.5	1.5		
t_{rec}	$\overline{CLR}$ Recovery Time	3.3	0	1.5	2.5	1.5	ns	2–3,7
		5.0	−0.5	0.5	1.5	0.5		

*Voltage Range 3.3 is 3.3V ±0.3V

*Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	2.5	5.5	9.5	1.0	11.0	2.0	10.0	ns	2–3, 4
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.5	5.5	9.5	1.0	11.0	2.0	10.0	ns	2–3, 4
t_{PLH}	Propagation Delay LE to O_n	5.0	2.5	5.5	9.0	1.0	11.0	2.0	10.0	ns	2–3, 4
t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	5.5	9.0	1.0	11.0	2.0	10.0	ns	2–3, 4
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	5.0	2.5	6.5	14.0	1.0	17.5	2.0	16.0	ns	2–3, 4
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0	2.5	7.5	15.5	1.0	19.0	2.0	17.5	ns	2–3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	5.5	9.5	1.0	11.0	2.0	10.5	ns	2–5, 6
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	2.5	5.5	9.5	1.0	11.0	2.0	10.5	ns	2–5, 6
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	2.5	6.0	10.5	1.0	12.0	2.0	11.0	ns	2–5, 6
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	2.5	6.0	10.5	1.0	12.0	2.0	11.0	ns	2–5, 6
t_{PHL}	Propagation Delay $\overline{PRE}$ to O_n	5.0	2.5	6.0	10.5	1.0	12.5	2.0	11.0	ns	2–3, 4
t_{PLH}	Propagation Delay $\overline{CLR}$ to O_n	5.0	2.5	5.5	9.5	1.0	11.5	2.0	10.5	ns	2–3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	−0.5	0.5	1.0	1.0	ns	2–7
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0.5	2.0	2.0	2.0	ns	2–7
t_w	LE Pulse Width, HIGH	5.0	2.0	3.5	3.5	3.5	ns	2–3
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	5.0	8.5	11.0	10.0	ns	2–3
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	5.5	9.5	12.5	11.0	ns	2–3
t_{rec}	$\overline{PRE}$ Recovery Time	5.0	0.5	2.0	2.0	2.0	ns	2–3, 7
t_{rec}	$\overline{CLR}$ Recovery Time	5.0	−0.5	1.0	1.0	1.0	ns	2–3, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	44	pF	V_{CC} = 5.0V

National Semiconductor

54ACT/74ACT845
8-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The 'ACT845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple $\overline{OE}$ controls.

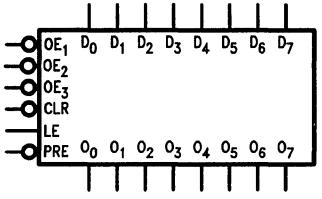
The 'ACT845 is functionally and pin compatible with AMD's Am29845.

Features

- 'ACT845 has TTL-compatible inputs

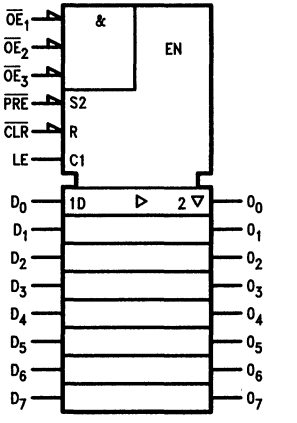
Ordering Code: See Section 8

Logic Symbols



TL/F/9896-3

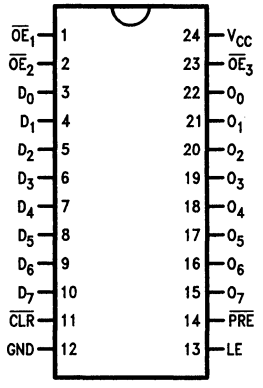
Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$–$\overline{OE}_3$	Output Enables
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset



TL/F/9896-5

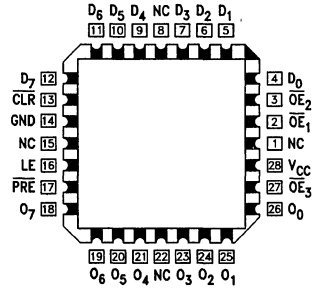
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9896-1

Pin Assignment for LCC



TL/F/9896-2

Functional Description

The 'ACT845 consists of eight D latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition.

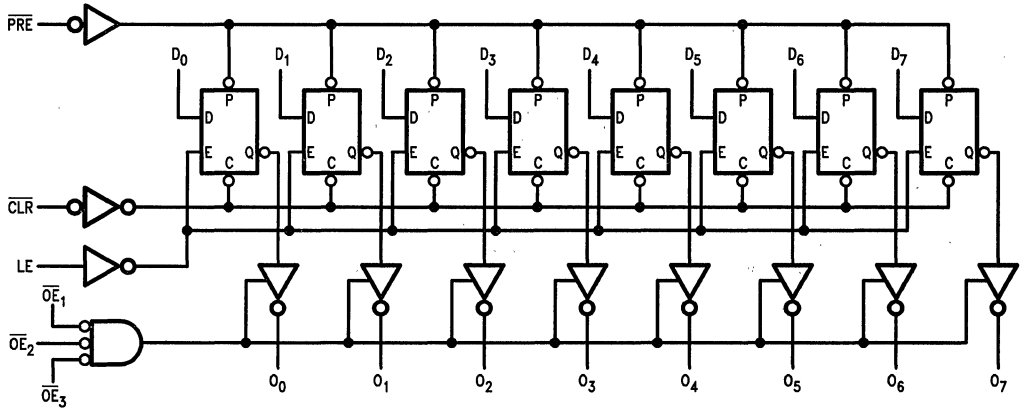
On the LE HIGH-to-LOW transition, the data that meets the setup times is latched Data appears on the bus when the Output Enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) are LOW. When any one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the bus output is in the high impedance state.

Function Table

Inputs					Internal	Output	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}_n$	LE	D	Q	O	
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Clear/High Z
H	L	H	L	X	H	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/9896–4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) −0.5V to +7.0V

DC Input Diode Current (I_{IK})
- $V_I = -0.5V$ −20 mA
- $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V_I) −0.5V to V_{CC} +0.5V

DC Output Diode Current (I_{OK})
- $V_O = -0.5V$ −20 mA
- $V_O = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) −0.5V to V_{CC} +0.5V

DC Output Source or Sink Current (I_O) ±50 mA

DC V_{CC} or Ground Current
Per Output Pin (I_{CC} or I_{GND}) ±50 mA

Storage Temperature (T_{STG}) −65°C to +150°C

Junction Temperature (T_J)
- CDIP 175°C
- PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 'AC 2.0V to 6.0V
- 'ACT 4.5V to 5.5V

Input Voltage (V_I) 0V to V_{CC}

Output Voltage (V_O) 0V to V_{CC}

Operating Temperature (T_A)
- 74ACT −40°C to +85°C
- 54ACT −55°C to +125°C

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'AC Devices
V_{IN} from 30% to 70% of V_{CC}
V_{CC} @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)
'ACT Devices
V_{IN} from 0.8V to 2.0V
V_{CC} @ 4.5V, 5.5V 125 mV/ns

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	74ACT T_A = 25°C		54ACT T_A = −55°C to +125°C	74ACT T_A = −40°C to +85°C	Units (V)	V_{CC}	Conditions
		Typ	Guaranteed Limits					
V_{IH}	Minimum High Level Input Voltage	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	4.5 5.5	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	4.5 5.5	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	4.5 5.5	I_{OUT} = −50 μA
			3.86 4.86	3.70 4.70	3.76 4.76	V	4.5 5.5	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	4.5 5.5	I_{OUT} = 50 μA
			0.36 0.36	0.50 0.50	0.44 0.44	V	4.5 5.5	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current		±0.1	±1.0	±1.0	μA	5.5	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current		±0.5	±10.0	±5.0	μA	5.5	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	0.6		1.6	1.5	mA	5.5	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current			50	75	mA	5.5	V_{OLD} = 1.65V Max
I_{OHD}				−50	−75	mA	5.5	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current		8.0	160	80	μA	5.5	V_{IN} = V_{CC} or Ground

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	V_{CC}* (V)	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max			
t_{PLH}	Propagation Delay D_n to O_n	2.0	5.5	9.5			2.0	10.0	ns	5.0	2–3, 4
t_{PHL}	Propagation Delay D_n to O_n	2.0	5.5	9.5			2.0	10.0	ns	5.0	2–3, 4
t_{PLH}	Propagation Delay LE to O_n	2.0	5.5	9.0			2.0	10.0	ns	5.0	2–3, 4
t_{PHL}	Propagation Delay LE to O_n	2.0	5.5	9.0			2.0	10.0	ns	5.0	2–3, 4
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	2.0	6.5	14.0			2.0	16.0	ns	5.0	2–3, 4
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	2.0	7.5	15.5			2.0	17.5	ns	5.0	2–3, 4
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	2.0	5.5	9.5			2.0	10.5	ns	5.0	2–5
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	2.0	5.5	9.5			2.0	10.5	ns	5.0	2–6
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	2.0	6.0	10.5			2.0	11.0	ns	5.0	2–5
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	2.0	6.0	10.5			2.0	11.0	ns	5.0	2–6
t_{PHL}	Propagation Delay $\overline{PRE}$ to O_n	2.0	6.0	10.5			2.0	11.0	ns	5.0	2–3, 4
t_{PLH}	Propagation Delay $\overline{CLR}$ to O_n	2.0	5.5	9.5			2.0	10.5	ns	5.0	2–3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	V_{CC}* (V)	Fig. No.
		Typ	Guaranteed Minimum					
t_s	Setup Time, HIGH or LOW D_n to LE	−0.5	0.5		1.0	ns	5.0	2–7
t_h	Hold Time, HIGH or LOW D_n to LE	0.5	2.0		2.0	ns	5.0	2–7
t_w	LE Pulse Width, HIGH	2.0	3.5		3.5	ns	5.0	2–3
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	8.5		10.0	ns	5.0	2–3
t_w	$\overline{CLR}$ Pulse Width, LOW	5.5	9.5		11.0	ns	5.0	2–3
t_{rec}	$\overline{PRE}$ Recovery Time	0.5	2.0		2.0	ns	5.0	2–3, 7
t_{rec}	$\overline{CLR}$ Recovery Time	0	1.0		1.0	ns	5.0	2–3, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

National Semiconductor

54AC/74AC899 • 54ACT/74ACT899
9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

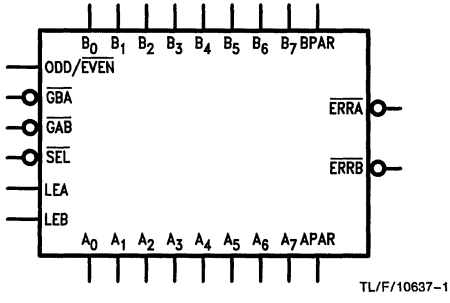
The 'AC/'ACT899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. The 'AC/'ACT899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

Features

- Latchable transceiver with output sink of 24 mA
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enable for A-to-B and B-to-A directions
- Select pin for ODD/$\overline{\text{EVEN}}$ parity
- $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in system applications in place of the '534 and '280
- May be used in system applications in place of the '657 and '373 (no need to change T/$\overline{\text{R}}$ to check parity)
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

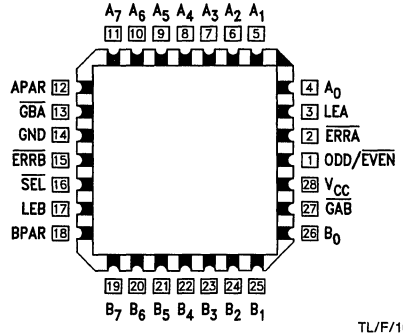
Logic Symbol



TL/F/10637–1

Connection Diagram

Pin Assignment for PCC



TL/F/10637–2

Pin Names	Description
A_0–A_7	A Bus Data Inputs/Data Outputs
B_0–B_7	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ Parity Select, Active LOW for EVEN Parity
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output Enables for A or B Bus, Active LOW
$\overline{\text{SEL}}$	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The 'AC/'ACT899 has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

— Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select ($\overline{\text{SEL}}$) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by $\overline{\text{ERRB}}$ ($\overline{\text{ERRA}}$).

— Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is HIGH. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).

— Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table below).

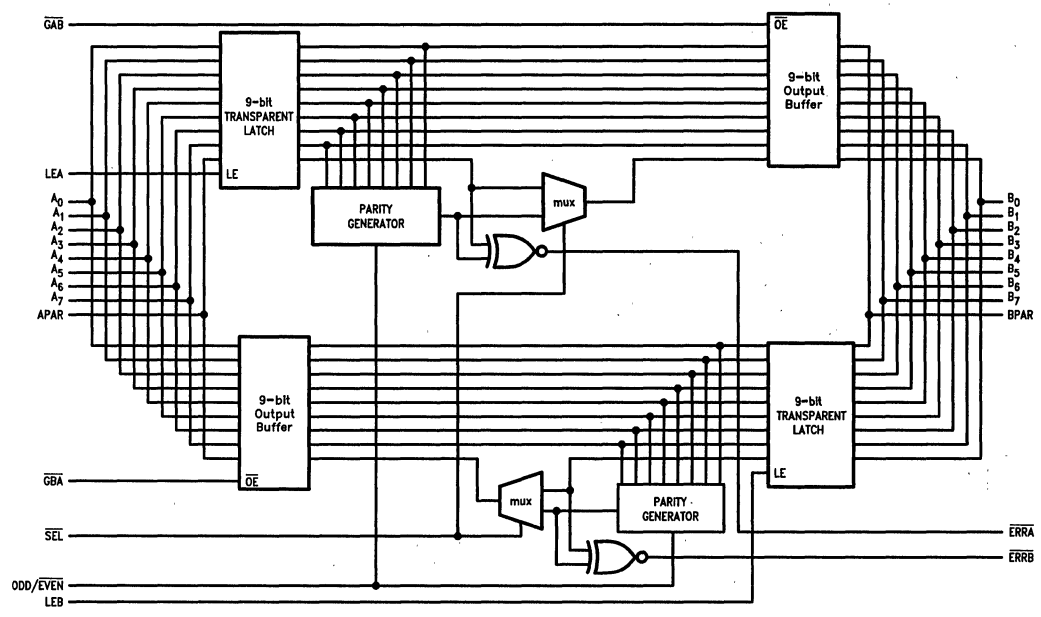
Function Table

Inputs					Operation
$\overline{\text{GAB}}$	$\overline{\text{GBA}}$	$\overline{\text{SEL}}$	LEA	LEB	
H	H	X	X	X	Busses A and B are TRI-STATE®.
H	L	L	L	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$ (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	L	H	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
H	L	L	X	L	Generates parity from B latch data based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against latched BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	X	H	BPAR/B[0:7] → APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	H	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
L	H	L	H	L	Generates parity for A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	L	H	H	Generates parity from A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.
L	H	L	L	X	Generates parity from A latch data based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against latched APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	L	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	H	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Note 1: O/$\overline{\text{E}}$ = ODD/$\overline{\text{EVEN}}$

Functional Block Diagram



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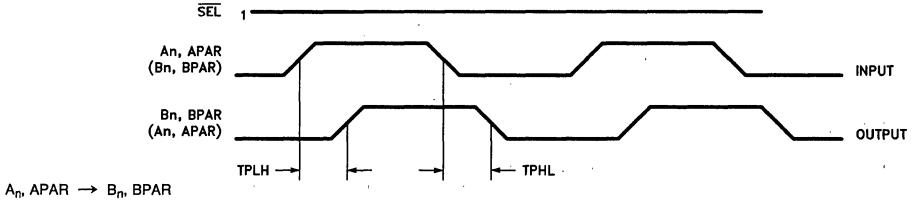
AC Path



A_n, APAR → B_n, BPAR
(B_n, BPAR → A_n, APAR)

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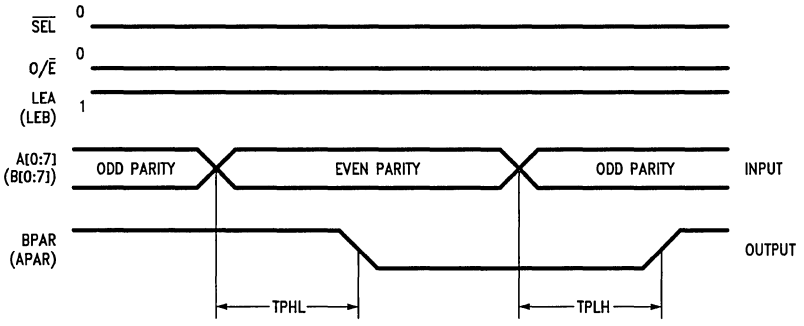
FIGURE 1

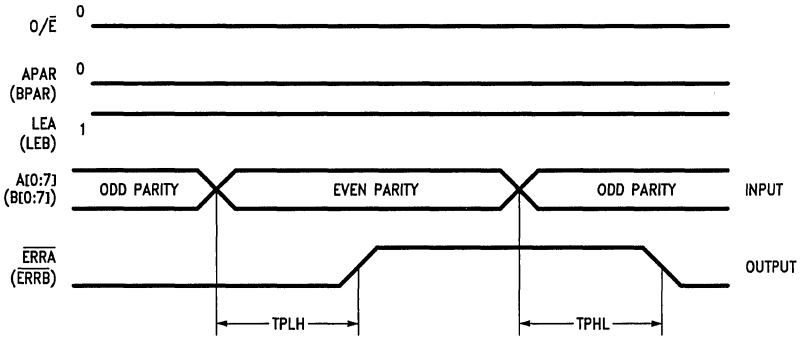
AC Path (Continued)



$A_n \rightarrow$ BPAR
($B_n \rightarrow$ APAR)

TL/F/10637–5

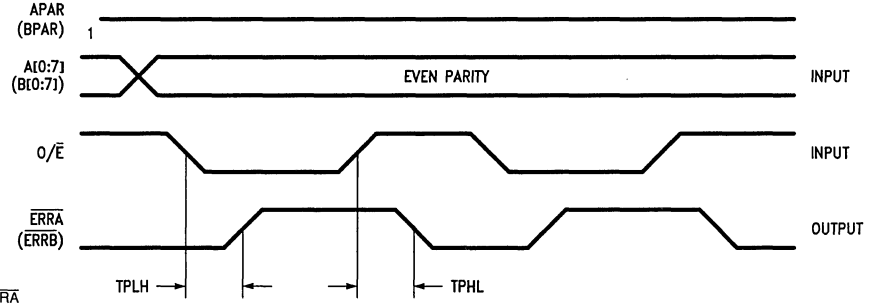
FIGURE 2



$A_n \rightarrow \overline{ERRA}$
($B_n \rightarrow \overline{ERRB}$)

TL/F/10637–6

FIGURE 3

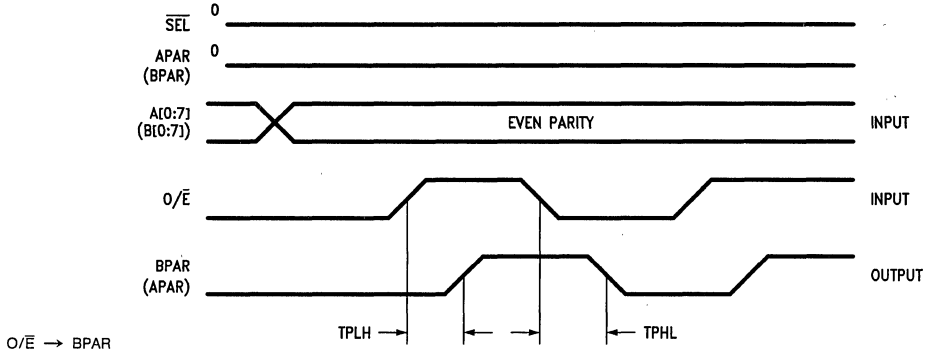


$O/\overline{E} \rightarrow \overline{ERRA}$
$O/\overline{E} \rightarrow \overline{ERRB}$

TL/F/10637–7

FIGURE 4

AC Path (Continued)



TL/F/10637–8

FIGURE 5

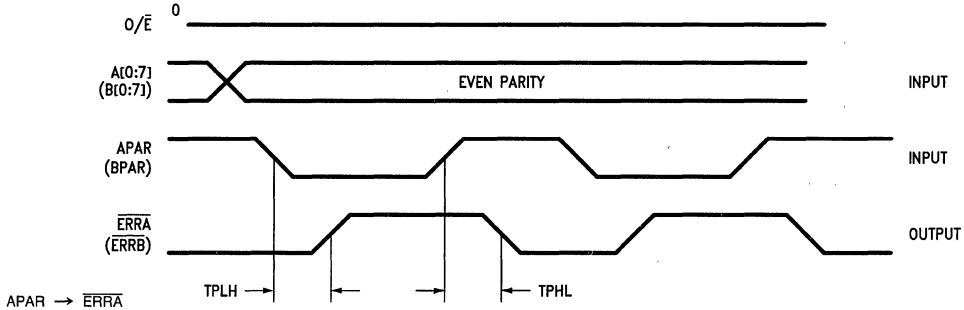


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FIGURE 6

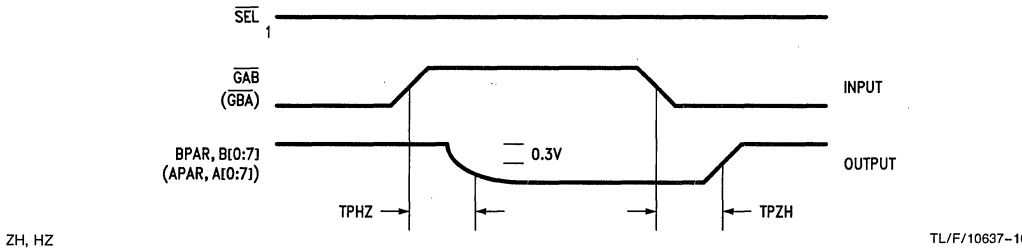

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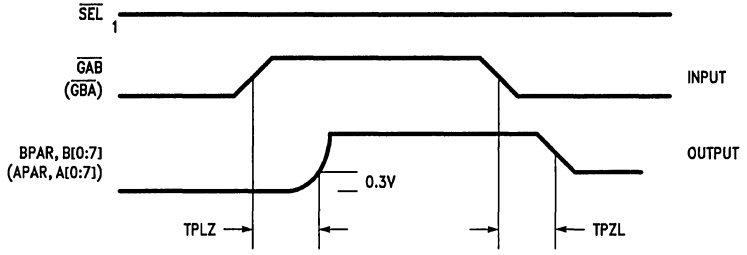
FIGURE 7

AC Path (Continued)



ZL, LZ

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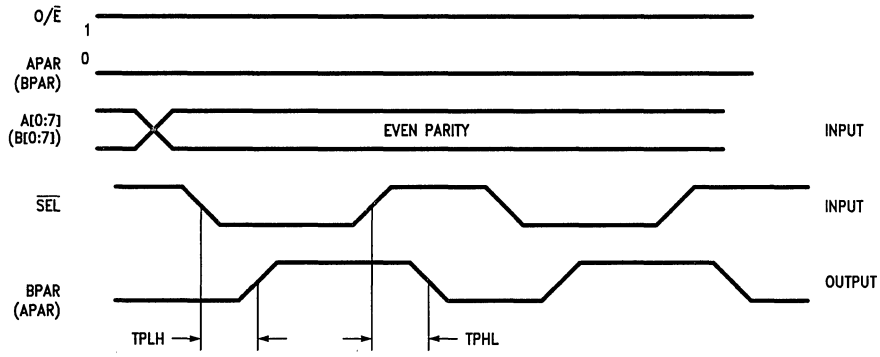
FIGURE 8



SEL → BPAR
(SEL → APAR)

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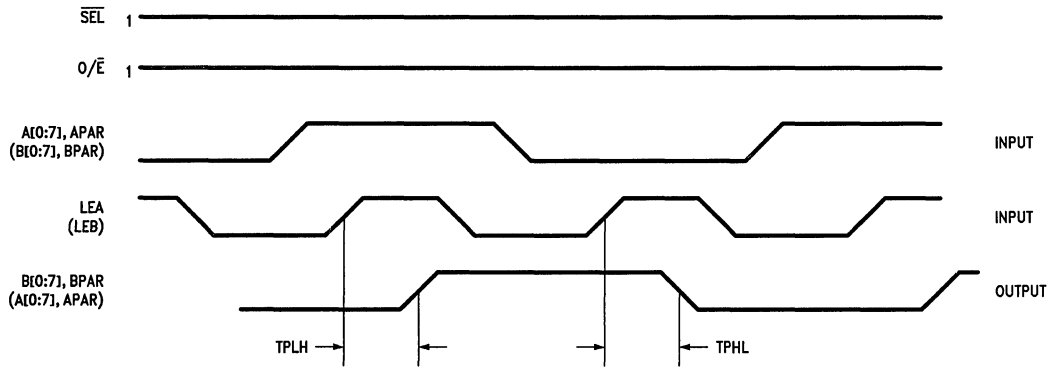
FIGURE 9

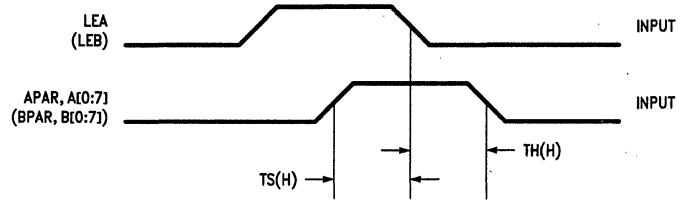


LEA → BPAR, B[0:7]
(LEB → APAR, A[0:7])

TL/F/10637–13

FIGURE 10

AC Path (Continued)



TS(H), TH(H)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

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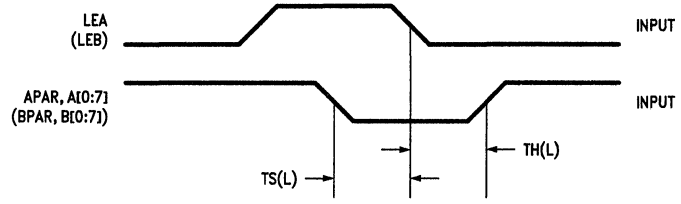
FIGURE 11



TS(L), TH(L)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

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FIGURE 12

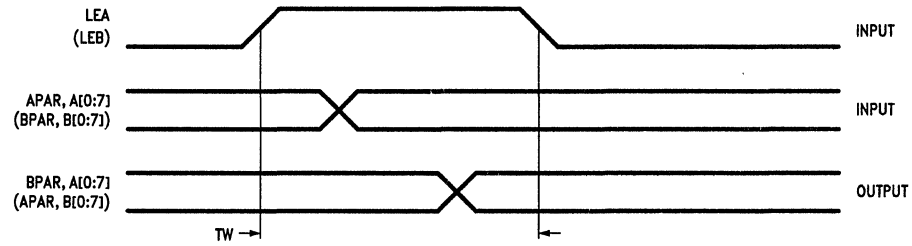

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FIGURE 13

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND (Note)

*Maximum of 9 outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND

*Maximum of 9 outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note)

*Maximum of 9 outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to B_n, A_n	3.3 5.0	2.5 1.5	12.0 7.0	15.0 10.0			2.5 1.5	15.5 10.5	ns	1
t_{PLH} t_{PHL}	Propagation Delay APAR, BPAR to BPAR, APAR	3.3 5.0	2.5 1.5	9.5 5.5	12.0 8.0			2.5 1.5	12.5 8.5	ns	1
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to BPAR, APAR	3.3 5.0	3.0 2.0	13.5 8.0	16.5 11.0			3.0 2.0	17.0 11.5	ns	2
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$	3.3 5.0	2.5 1.5	12.5 7.5	15.5 10.5			2.5 1.5	16.5 11.0	ns	3
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	3.3 5.0	2.5 1.5	12.5 7.5	15.5 10.5			2.5 1.5	16.5 11.0	ns	4
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to APAR, BPAR	3.3 5.0	3.0 2.0	12.5 7.5	15.5 10.5			3.0 2.0	16.5 11.0	ns	5
t_{PLH} t_{PHL}	Propagation Delay APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	3.3 5.0	2.0 1.5	12.5 7.5	15.5 10.5			2.0 1.5	16.5 11.0	ns	6
t_{PLH} t_{PHL}	Propagation Delay $\overline{SEL}$ to APAR, BPAR	3.3 5.0	2.0 1.5	10.0 6.0	12.5 8.5			2.0 1.5	13.5 9.0	ns	9
t_{PLH} t_{PHL}	Propagation Delay LEB, LEA to A_n, B_n	3.3 5.0	4.0 2.5	12.0 7.0	15.5 10.5			4.0 2.5	16.5 11.0	ns	10, 11
t_{PLH} t_{PHL}	Propagation Delay LEB, LEA to APAR, BPAR	3.3 5.0	3.0 2.0	13.5 8.0	17.0 11.5			3.0 2.0	18.0 12.0	ns	10, 11
t_{PLH} t_{PHL}	Propagation Delay LEB, LEA to $\overline{ERRA}$, $\overline{ERRB}$	3.3 5.0	4.0 2.5	13.5 8.0	17.0 11.5			4.0 2.5	18.0 12.0	ns	12
t_{PZH} t_{PZL}	Output Enable Time $\overline{GBA}$, $\overline{GAB}$ to A_n, B_n	3.3 5.0	3.0 2.0	12.5 7.5	15.5 10.5			3.0 2.0	16.5 11.0	ns	7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{GBA}$, $\overline{GAB}$ to APAR, BPAR	3.3 5.0	2.5 1.5	10.5 6.0	13.5 9.0			2.5 1.5	14.0 9.5	ns	7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{GBA}$, $\overline{GAB}$ to A_n, B_n	3.3 5.0	1.5 1.0	11.0 6.5	14.0 9.5			1.5 1.0	14.0 9.5	ns	7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{GBA}$, $\overline{GAB}$ to APAR, BPAR	3.3 5.0	1.5 1.0	11.0 6.5	14.0 9.5			1.5 1.0	14.0 9.5	ns	7, 8

*Voltage Range 5.0 is 5.0V ±0.5V.
Voltage Range 3.3 is 3.3V ±0.3V.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF	54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW A_n, B_n, PAR to LEA, LEB	3.3 5.0	3.0 3.0		3.0 3.0	ns	11, 12
t_h	Hold Time, HIGH or LOW A_n, B_n, PAR to LEA, LEB	3.3 5.0	2.0 1.5		2.0 1.5	ns	11, 12
t_w	Pulse Width for LEA, LEB	3.3 5.0	4.0 4.0		4.0 4.0	ns	13

*Voltage Range 5.0 is 5.0V ±0.5V.
Voltage Range 3.3 is 3.3V ±0.3V.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to B_n, A_n	5.0	2.5	7.5	11.5			2.5	12.0	ns	1
t_{PLH} t_{PHL}	Propagation Delay APAR, BPAR to BPAR , APAR	5.0	1.5	6.0	8.5			1.5	9.0	ns	1
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to BPAR, APAR	5.0	2.5	8.5	12.0			2.5	12.5	ns	2
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{ERRA}$, $\overline{ERRB}$	5.0	2.0	8.0	11.5			2.0	12.0	ns	3
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to $\overline{ERRA}$, $\overline{ERRB}$	5.0	2.0	8.0	11.5			2.0	12.0	ns	4
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to APAR, BPAR	5.0	2.5	8.0	11.5			2.5	12.0	ns	5
t_{PLH} t_{PHL}	Propagation Delay APAR, BPAR to $\overline{ERRA}$, $\overline{ERRB}$	5.0	1.5	7.5	10.5			1.5	11.5	ns	6
t_{PLH} t_{PHL}	Propagation Delay $\overline{SEL}$ to APAR, BPAR	5.0	1.5	6.5	9.0			1.5	9.5	ns	9
t_{PLH} t_{PHL}	Propagation Delay LEB to A_n, B_n	5.0	2.5	7.0	10.5			2.5	11.0	ns	10, 11
t_{PLH} t_{PHL}	Propagation Delay LEA to APAR, BPAR	5.0	2.0	8.0	11.5			2.0	12.0	ns	10, 11
t_{PLH} t_{PHL}	Propagation Delay LEA, LEB to $\overline{ERRA}$, $\overline{ERRB}$	5.0	2.5	8.0	11.5			2.5	12.0	ns	12
t_{PZH} t_{PZL}	Output Enable Time $\overline{GBA}$ or $\overline{GAB}$ to A_n, B_n	5.0	2.5	7.0	10.5			2.5	11.0	ns	7, 8
t_{PZH} t_{PZL}	Output Enable Time $\overline{GBA}$ or $\overline{GAB}$ to BPAR or APAR	5.0	1.5	6.0	9.0			1.5	9.5	ns	7, 8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{GBA}$ or $\overline{GAB}$ to A_n, B_n	5.0	1.5	6.5	9.5			1.5	9.5	ns	7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{GBA}$ or $\overline{GAB}$ to BPAR, APAR	5.0	1.5	6.5	9.5			1.5	9.5	ns	7, 8

*Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF	54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW A_n, B_n, PAR to LEA, LEB	5.0	3.0		3.0	ns	11, 12
t_h	Hold Time, HIGH or LOW A_n, B_n, PAR to LEA, LEB	5.0	1.5		1.5	ns	11, 12
t_w	Pulse Width for LEB, LEA	5.0	4.0		4.0	ns	13

*Voltage Range 5.0 = 5.0V ±0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	210	pF	V_{CC} = 5.0V

National Semiconductor

ADVANCE INFORMATION

54AC/74AC2525 • 54AC/74AC2526
Minimum Skew Clock Driver

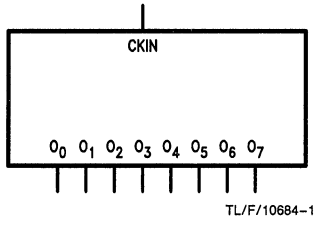
The 'AC2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications. The 2525 is designed to distribute a single clock to eight separate receivers with low skew across all outputs during both the TPLH and TPHL transitions. The AC2526 is similar to the AC2525 but contains a multiplexed clock input to allow for systems with dual clock speeds or systems where a separate test clock has been implemented.

Features

- Ideal for signal generation and clock distribution
- Guaranteed pin to pin and part to part skew
- Multiplexed clock input ('2526)
- Guaranteed 2000V minimum ESD protection
- 24 mA output drive capability

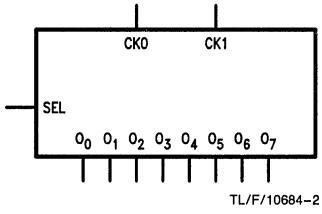
Logic Symbols

'AC2525



TL/F/10684–1

'AC2526

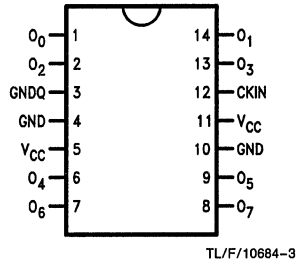


TL/F/10684–2

Connection Diagrams

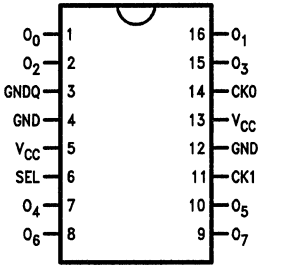
Pin Assignment for DIP, Flatpak and SOIC

'AC2525



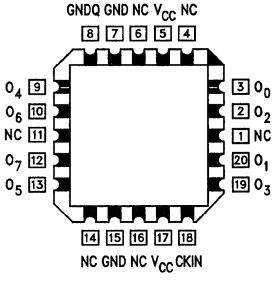
TL/F/10684–3

'AC2526

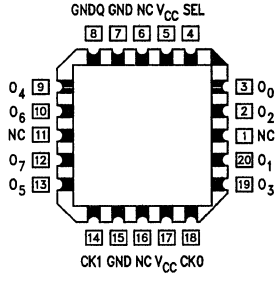


TL/F/10684–4

Pin Assignment for LCC



TL/F/10684–5



TL/F/10684–6

National Semiconductor

54AC/74AC2708•54ACT/74ACT2708
64 x 9 First-In, First-Out Memory

General Description

The 'AC/'ACT2708 is an expandable first-in, first-out memory organized as 64 words by 9 bits. An 85 MHz shift-in and 60 MHz shift-out typical data rate makes it ideal for high-speed applications. It uses a dual port RAM architecture with pointer logic to achieve the high speed with negligible fall-through time.

Separate Shift-In (SI) and Shift-Out (SO) clocks control the use of synchronous or asynchronous write or read. Other controls include a Master Reset ($\overline{MR}$) and Output Enable ($\overline{OE}$) for initializing the internal registers and allowing the data outputs to be TRI-STATE®. Input Ready (IR) and Output Ready (OR) signal when the FIFO is ready for I/O operations. The status flags HF and FULL indicate when the FIFO is full, empty or half full.

The FIFO can be expanded to provide different word lengths by tying off unused data inputs.

Features

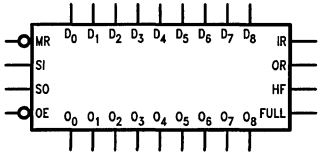
- 64-words by 9-bit dual port RAM organization
- 85 MHz shift-in, 60 MHz shift-out data rate, typical
- Expandable in word width only
- 'ACT2708 has TTL-compatible inputs
- Asynchronous or synchronous operation
- Asynchronous master reset
- Outputs source/sink 8 mA
- TRI-STATE outputs
- Full ESD protection
- Input and output pins directly in line for easy board layout
- TRW 1030 work-alike operation

Applications

- High-speed disk or tape controllers
- A/D output buffers
- High-speed graphics pixel buffer
- Video time base correction
- Digital filtering

Ordering Code: See Section 8

Logic Symbol

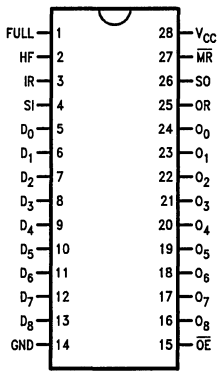


TL/F/10144–1

Pin Names	Description
D_0–D_8	Data Inputs
$\overline{MR}$	Master Reset
$\overline{OE}$	Output Enable Input
SI	Shift-In
SO	Shift-Out
IR	Input Ready
OR	Output Ready
HF	Half Full Flag
FULL	Full Flag
O_0–O_8	Data Outputs

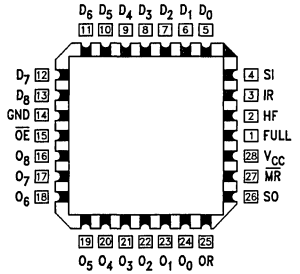
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



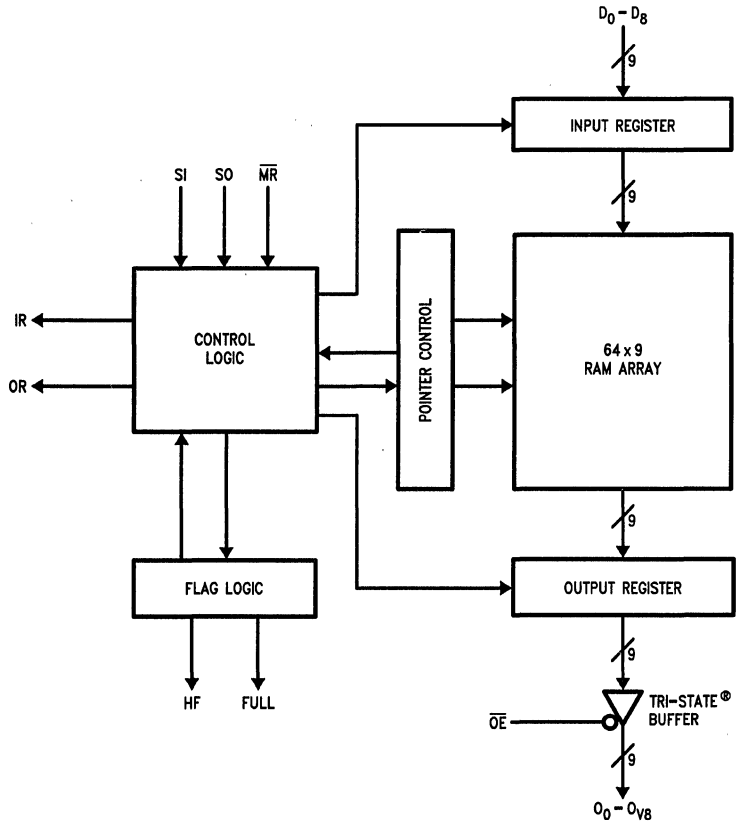
TL/F/10144–2

Pin Assignment for LCC



TL/F/10144–3

Block Diagram



TL/F/10144–4

Functional Description

INPUTS

Data Inputs (D_0–D_8)

Data inputs for 9-bit wide data are TTL-compatible. Word width can be reduced by trying unused inputs to ground and leaving the corresponding outputs open.

Reset ($\overline{MR}$)

Reset is accomplished by pulsing the $\overline{MR}$ input LOW. During normal operation $\overline{MR}$ is HIGH. A reset is required after power up to guarantee correct operation. On reset, the data outputs go LOW, IR goes HIGH, OR goes LOW, FH and FULL go LOW. During reset, both internal read and write pointers are set to the first location in the array.

Shift-In (SI)

Data is written into the FIFO by pulsing SI HIGH. When Shift-In goes HIGH, the data is loaded into an internal data latch. Data setup and hold times need to be adhered to with respect to the falling edge of SI. The write cycle is complete after the falling edge of SI. The shift-in is independent of any ongoing shift-out operation. After the first word has been written into the FIFO, the falling edge of SI makes HF go HIGH, indicating a non-empty FIFO. The first data word appears at the output after the falling edge of SI. After half the memory is filled, the next rising edge of SI makes FULL go HIGH indicating a half-full FIFO. When the FIFO is full, any further shift-ins are disabled.

When the FIFO is empty and $\overline{OE}$ is LOW, the falling edge of the first SI will cause the first data word just shifted-in to appear at the output, even though SO may be LOW.

Shift-Out (SO)

Data is read from the FIFO by the Shift-Out signal provided the FIFO is not empty. SO going HIGH causes OR to go LOW indicating that output stage is busy. On the falling edge of SO, new data reaches the output after propagation delay t_D. If the last data has been shifted-out of the memory, OR continues to remain LOW, and the last word shifted-out remains on the output pins.

Output Enable ($\overline{OE}$)

$\overline{OE}$ LOW enables the TRI-STATE output buffers. When $\overline{OE}$ is HIGH, the outputs are in a TRI-STATE mode.

OUTPUTS

Data Outputs (O_0–O_8)

Data outputs are enabled when $\overline{OE}$ is LOW and in the TRI-STATE condition when $\overline{OE}$ is HIGH.

Input Ready (IR)

IR HIGH indicates data can be shifted-in. When SI goes HIGH, IR goes LOW, indicating input stage is busy. IR stays LOW when the FIFO is full and goes HIGH after the falling edge of the first shift-out.

Output Ready (OR)

OR HIGH indicates data can be shifted-out from the FIFO. When SO goes HIGH, OR goes LOW, indicating output stage is busy. OR is LOW when the FIFO is reset or empty and goes HIGH after the falling edge of the first shift-in.

Half-Full (HF)

This status flag along with the FULL status flag indicates the degree of fullness of the FIFO. On reset, HF is LOW; it rises on the falling edge of the first SI. The rising edge of the SI pulse that fills up the FIFO makes HF go LOW. Going from the empty to the full state with SO LOW, the falling edge of the first SI causes HF to go HIGH, the rising edge of the 33rd SI causes FULL to go HIGH, and the rising edge of the 64th SI causes HF to go LOW.

When the FIFO is full, HF is LOW and the falling edge of the first shift-out causes HF to go HIGH indicating a "non-full" FIFO.

Full Flag (FULL)

This status flag along with the HF status flag indicates the degree of fullness of the FIFO. On reset, FULL is LOW. When half the memory is filled, on the rising edge of the next SI, the FULL flag goes HIGH. It remains set until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. The FULL flag then goes LOW on the rising edge of the next SO.

Status Flags Truth Table

HF	FULL	Status Flag Condition
L	L	Empty
L	H	Full
H	L	<32 Locations Filled
H	H	≥32 Locations Filled

H = HIGH Voltage Level
L = LOW Voltage Level

Reset Truth Table

Inputs			Outputs				
$\overline{MR}$	SI	SO	IR	OR	HF	FULL	O_0–O_8
H	X	X	X	X	X	X	X
L	X	X	H	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

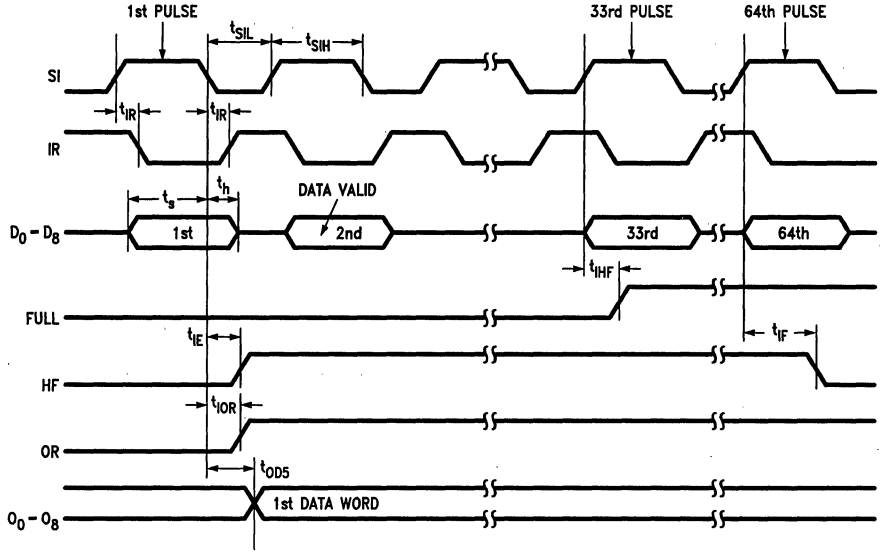
Functional Description (Continued)

MODES OF OPERATION

Mode 1: Shift In Sequence for FIFO Empty to Full

Sequence of Operation

1. Input Ready is initially HIGH; HF and FULL flags are LOW. The FIFO is empty and prepared for valid data. OR is LOW indicating that the FIFO is not yet ready to output data.
2. Shift-In is set HIGH, and data is loaded into the FIFO. Data has to be settled t_S before the falling edge of SI and held t_h after.
3. Input Ready (IR) goes LOW propagation delay t_{IR} after SI goes HIGH: input stage is busy.
4. Shift-In is set LOW; IR goes HIGH indicating the FIFO is ready for additional data. Data just shifted-in arrives at output propagation delay t_{OD5} after SI falls. OR goes HIGH propagation delay t_{IOR} after SI goes LOW, indicating the FIFO has valid data on its outputs. HF goes HIGH propagation delay t_{IE} after SI falls, indicating the FIFO is no longer empty.
5. The process is repeated through the 64th data word. On the rising edge of the 33rd SI, FULL flag goes HIGH propagation delay t_{IHF} after SI, indicating a half-full FIFO. HF goes LOW propagation delay t_{IF} after the rising edge of the 64th pulse indicating that the FIFO is full. Any further shift-ins are disabled.



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Note: SO and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH.

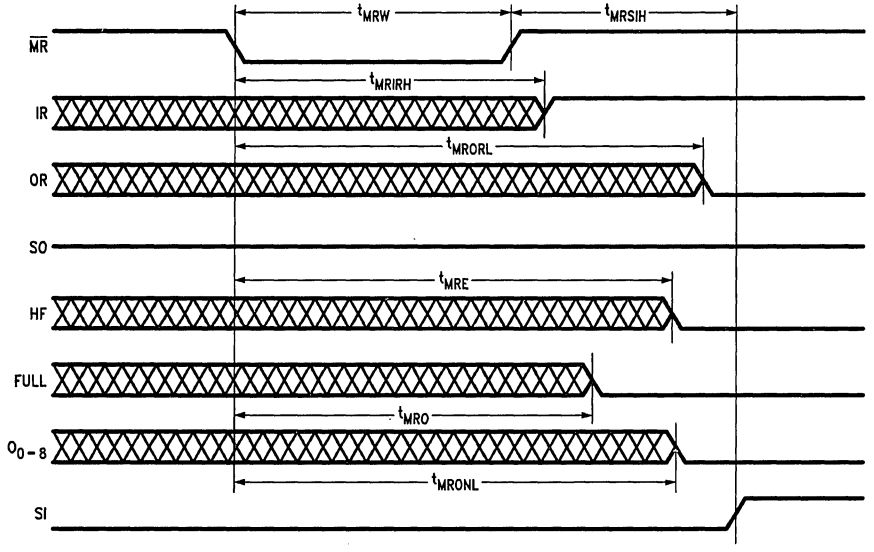
FIGURE 1. Modes of Operation Mode 1

Functional Description (Continued)

Mode 2: Master Reset

Sequence of Operation

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ($\overline{MR}$) HIGH.
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of $\overline{MR}$. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times t_{MRE} and t_{MRO} respectively after the falling edge of $\overline{MR}$. OR falls recovery time t_{MRORL} after $\overline{MR}$ falls. Data at outputs goes LOW recovery time t_{MRONL} after $\overline{MR}$ goes LOW.
5. Shift-In can be taken HIGH after a minimum recovery time t_{MRSIH} after $\overline{MR}$ goes HIGH.



TL/F/10144–6

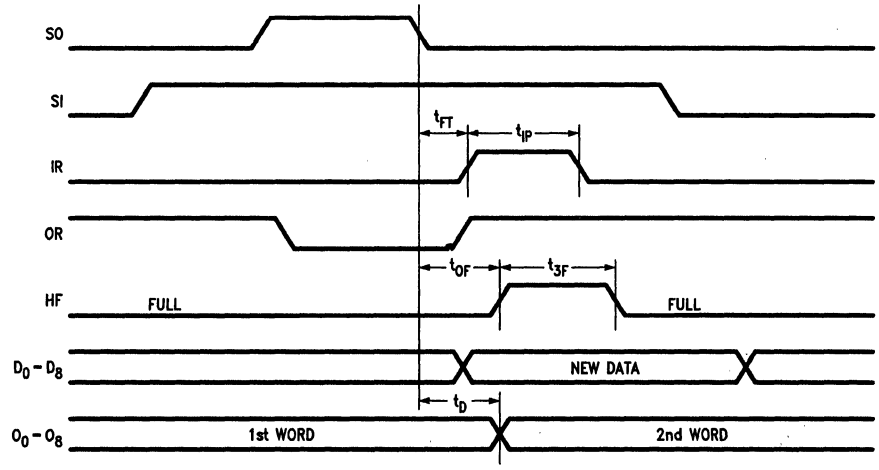
FIGURE 2. Mode of Operation Mode 2

Functional Description (Continued)

Mode 3: With FIFO Full, Shift-In is Held HIGH in Anticipation of an Empty Location

Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay t_D. New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH one fall-through time, t_{FT}, after the falling edge of SO. Also, HF goes HIGH one t_{OF} after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width t_{IP} after rising and shifting new data in. Also, HF returns LOW pulse width t_{3F} after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation



TL/F/10144–7

Note: $\overline{MR}$ and FULL are HIGH; $\overline{OE}$ is LOW.

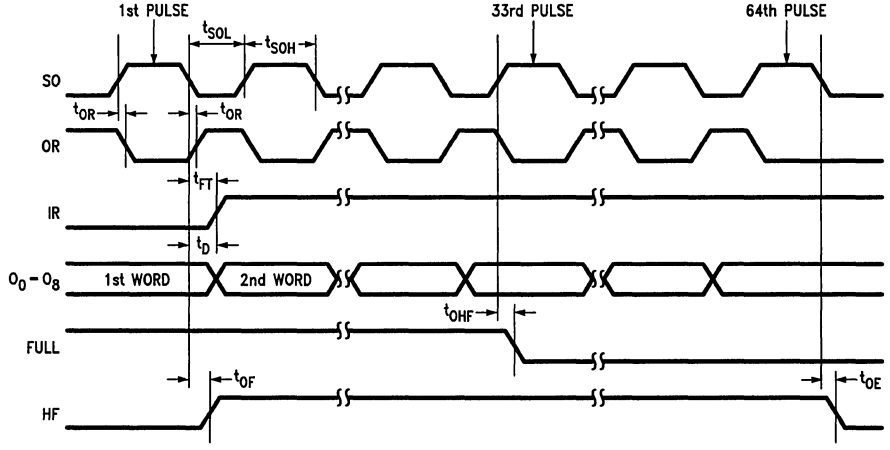
FIGURE 3. Modes of Operation Mode 3

Functional Description (Continued)

Mode 4: Shift-Out Sequence, FIFO Full to Empty

Sequence of Operation

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW one propagation delay, t_{OR}, after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output one propagation delay, t_D, after SO falls; OR goes HIGH one propagation delay, t_{OR}, after SO falls and HF rises one propagation delay, t_{OF}, after SO falls. IR rises one fall-through time, t_{FT}, after SO falls.
4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay, t_{OHF}, after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay, t_{OE}, after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.



TL/F/10144–8

Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; D_0–D_8 are immaterial.

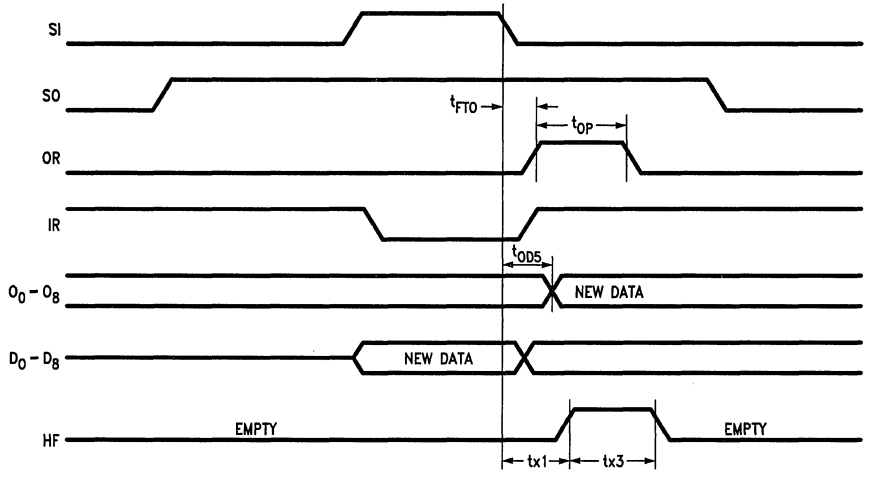
FIGURE 4. Modes of Operation Mode 4

Functional Description (Continued)

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

Sequence of Operation

1. FIFO is initially empty; Shift-Out goes HIGH.
2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay t_{X1} after the falling edge of SI.
3. OR rises a fall-through time of t_{FTO} after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output one propagation delay, t_{OD5}, after the falling edge of Shift-In.
5. OR goes LOW pulse width t_{OP} after rising and HF goes LOW pulse width t_{X3} after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.



TL/F/10144–9

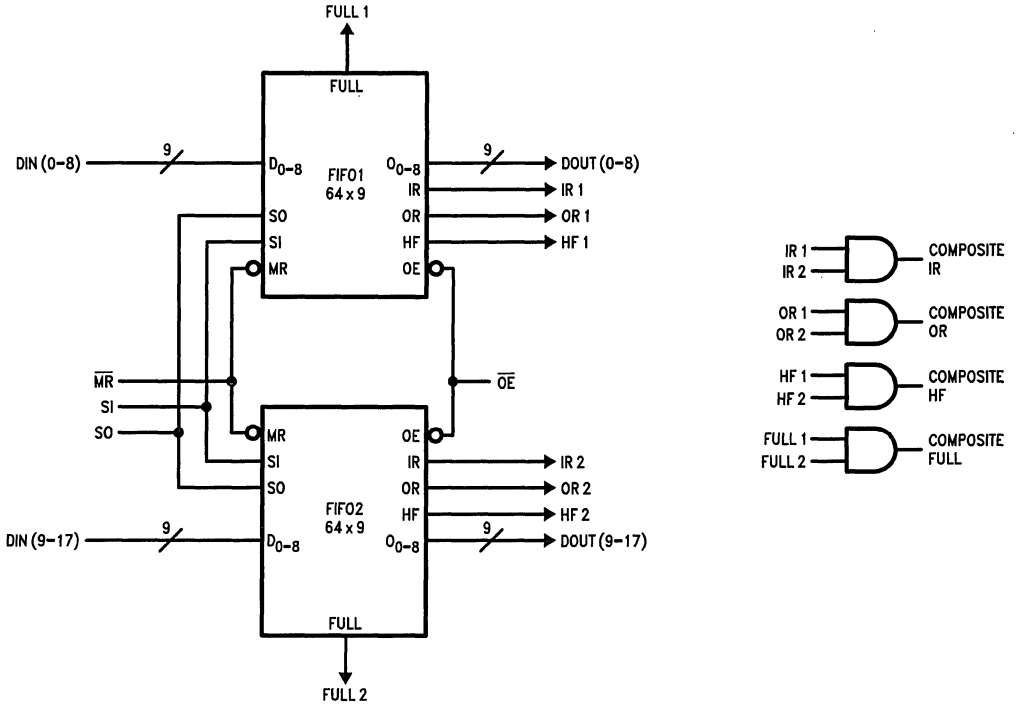
Note: FULL is LOW; $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage t_{DOF} after OR is HIGH.

FIGURE 5. Modes of Operation Mode 5

FIFO Expansion

Word Width Expansion

Word width can be increased by connecting the corresponding input control signals of multiple devices. Flags can be monitored to obtain a composite signal by ANDing the corresponding flags.



TL/F/10144–10

Note: AND the corresponding flags to obtain a composite signal.

FIGURE 6. Word Width Expansion—64 x 18 FIFO

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±32 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±32 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Device

Symbol	Parameter	V_{CC} (V)	74AC T_A = 25°C		54AC T_A = −55°C to +125°C	74AC T_A = −40° to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} −0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −4 mA
		4.5		3.86	3.7	3.76		I_{OH} −8 mA
		5.5		4.86	4.7	4.76		−8 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 4 mA
		4.5		0.36	0.50	0.44		I_{OL} 8 mA
		5.5		0.36	0.50	0.44		8 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC} GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0		V_I(OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'AC Family Device (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = 25°C$ Typ	74AC $T_A = 25°C$ Guaranteed Limits	54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°$ to $+85°C$	Units	Conditions
I_{OLD}	†Minimum Dynamic Output Current	5.5			32	32	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−32	−32	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	$V_{IN} = V_{CC}$ or GND
I_{CCD}	Supply Current 20 MHz Loaded	5.5	125	150		150	mA	f = 20 MHz (Note 2)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

Note 2: Test load 50 pF, 500Ω to ground.

DC Electrical Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT $T_A = 25°C$ Typ	54ACT $T_A = 25°C$ Guaranteed Limits	54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} −0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8		V_{OUT} = 0.1V or V_{CC} −0.1V
V_{OH}	Minimum High Level	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −8 mA −8 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.32 0.32	0.40 0.40	0.37 0.37	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 8 mA 8 mA
I_{IN}	Maximum Input	5.5		±0.1	+1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6	1.0	1.6	1.5	mA	$V_I = V_{CC}$ −2.1V
I_{OLD}	†Maximum Dynamic	5.5			32	32	mA	V_{OLD} = 1.65V
I_{OHD}	Output Current	5.5			−32	−32	mA	V_{OHD} = 3.85V
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160	80	μA	$V_{IN} = V_{CC}$ or GND
I_{CCD}	Supply Current 20 MHz Loaded	5.5	125	150		150	mA	f = 20 MHz (Note 2)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Notes: I_{CC} limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.
When $\overline{MR}$ is low with SO High, I_{CC} > 1.5 mA.

Note 2: Test load 50 pF, 500Ω to ground.

AC Characteristics: See Section 2 for waveforms

Symbol	Parameter	*V_{CC} (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay, t_{IR} SI to IR	3.3	2.5	8.5	16.5	1.0	20.0	2.0	18.5	ns	1
		5.0	1.5	5.5	11.5	1.5	15.0	1.0	12.5		
t_{PHL}	Propagation Delay, t_{IR} SI to IR	3.3	2.5	7.0	14.0	1.0	20.0	2.0	16.0	ns	1
		5.0	1.5	5.0	10.0	1.5	15.0	1.0	11.0		
t_{PLH}	Propagation Delay, t_{IHF} SI to > HF	3.3	4.5	12.0	23.5	1.0	30.0	4.5	27.0	ns	1
		5.0	3.0	8.0	15.5	1.5	20.0	3.0	18.0		
t_{PHL}	Propagation Delay, t_{IF} SI to Full Condition	3.3	5.0	11.5	22.0	1.0	28.0	5.0	25.0	ns	1
		5.0	3.5	8.0	15.0	2.0	20.0	3.5	17.0		
t_{PLH}	Propagation Delay, t_{IE} SI to Not Empty	3.3	4.5	11.5	23.5	1.0	29.0	4.5	26.5	ns	1
		5.0	3.0	8.0	15.5	1.5	20.0	3.0	17.5		
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	3.3	4.5	13.5	30.5	1.0	39.0	4.5	34.5	ns	1
		5.0	3.0	9.0	20.0	1.5	26.0	3.0	23.0		
t_{PLH}	Propagation Delay t_{MRIRH} $\overline{MR}$ to IR	3.3	3.5	10.5	21.5	1.0	26.0	3.5	23.5	ns	2
		5.0	2.5	7.5	14.5	1.5	18.0	2.0	16.0		
t_{PHL}	Propagation Delay, t_{MRORL} $\overline{MR}$ to OR	3.3	7.5	18.5	35.5	1.0	45.0	7.5	41.0	ns	2
		5.0	6.0	12.0	23.0	3.0	31.0	6.0	26.5		
t_{PHL}	Propagation Delay t_{MRO} $\overline{MR}$ to Full Flag	3.3	4.0	9.0	18.0	1.0	24.0	4.0	21.5	ns	2
		5.0	2.5	6.5	12.5	1.5	17.0	2.0	15.0		
t_{PHL}	Propagation Delay t_{MRE} $\overline{MR}$ to HF Flag	3.3	8.5	20.0	39.5	1.0	49.0	8.5	44.5	ns	2
		5.0	7.0	13.5	26.0	4.0	33.0	6.5	29.5		
t_{PHL}	Propagation Delay, t_{MRONL} $\overline{MR}$ to O_n, LOW	3.3	3.5	9.5	19.5	1.0	25.0	3.5	21.5	ns	2
		5.0	2.0	7.0	14.0	1.5	18.0	2.0	15.5		
t_W	IR Pulse Width, t_{IP}	3.3	17.0	37.5	69.0		87.0	17.0	79.5	ns	3
		5.0	15.0	22.0	40.5		53.0	14.5	48.0		
t_W	HF Pulse Width t_{3F}	3.3	18.0	40.0	71.5		92.0	18.0	84.0	ns	3
		5.0	16.0	23.0	42.0		56.0	15.5	50.5		
t_{PLH}	Propagation Delay, t_D SO to Data Out	3.3	7.0	20.5	41.5	1.0	55.0	7.0	47.5	ns	3, 4
		5.0	5.5	13.5	26.0	3.5	37.0	5.0	31.0		
t_{PHL}	Propagation Delay, t_D SO to Data Out	3.3	7.0	22.5	43.5	1.0	55.0	7.0	50.5	ns	3, 4
		5.0	5.5	14.5	28.0	3.5	37.0	5.5	32.5		
t_{PHL}	Propagation Delay, t_{OHF} SO to < HF	3.3	4.0	9.0	17.5	1.0	23.0	4.0	20.5	ns	4
		5.0	2.5	6.5	12.0	1.5	16.0	2.0	14.0		
t_{PLH}	Propagation Delay, t_{OF} SO to Not Full	3.3	5.5	14.5	29.0	1.0	36.0	5.5	33.0	ns	3, 4
		5.0	4.0	10.0	19.0	2.5	24.0	4.0	22.0		
t_{PLH}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	3.3	3.0	8.5	17.0	1.0	22.0	3.0	19.5	ns	4
		5.0	2.0	5.5	12.0	1.5	18.0	1.5	13.0		

*Voltage Range 3.3 is 3.3V ± 0.3V

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: See Section 2 for waveforms (Continued)

Symbol	Parameter	*V_{CC} (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay, t_{OE} SO to Empty	3.3	4.0	10.5	20.5	1.0	26.0	3.5	23.5	ns	4
		5.0	2.5	7.0	14.0	1.5	19.0	2.0	16.0		
t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	3.3	7.5	22.5	44.5	1.0	60.0	7.0	53.5	ns	5
		5.0	6.0	15.5	30.0	4.5	39.0	5.5	35.0		
t_{PHL}	Propagation Delay, t_{OD5} SI to New Data Out	3.3	7.5	21.5	42.0	1.0	60.0	7.0	48.5	ns	5
		5.0	6.0	14.5	28.5	4.5	39.0	5.5	33.0		
t_{PLH}	Propagation Delay, t_{X1} SI to HF	3.3	4.0	11.5	23.0	1.0	29.0	3.5	26.0	ns	5
		5.0	2.5	8.0	15.5	1.5	20.0	2.0	17.5		
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	3.3	4.0	15.5	30.5	1.0	39.0	4.0	34.5	ns	5
		5.0	3.0	10.5	20.0	2.5	26.0	2.5	23.0		
t_W	OR Pulse Width, t_{OP}	3.3	13.0	23.5	42.0		54.0	12.0	48.5	ns	5
		5.0	10.0	13.5	25.5		34.0	9.0	29.5		
t_W	HF Pulse Width, t_{X3}	3.3	15.0	27.0	49.5		63.0	14.0	57.0	ns	5
		5.0	12.0	16.0	30.0		40.0	11.0	34.5		
t_{PLH}	Fall-Through Time, t_{FT} SO to IR	3.3	6.5	19.0	37.0	1.0	47.0	6.0	42.5	ns	5
		5.0	5.0	12.5	24.0	4.0	31.0	4.5	27.5		
t_{PZL}	Output Enable $\overline{OE}$ to O_n	3.3	2.5	7.0	14.0	1.0	21.0	2.0	16.0	ns	2-6
		5.0	1.5	5.0	10.0	1.5	15.0	1.0	11.0		
t_{PLZ}	Output Disable $\overline{OE}$ to O_n	3.3	2.0	4.5	9.0	1.0	17.0	1.5	9.5	ns	2-6
		5.0	1.0	3.5	7.0	1.5	13.0	1.0	7.5		
t_{PZH}	Output Enable $\overline{OE}$ to O_n	3.3	2.5	7.5	16.5	1.0	21.0	2.0	18.5	ns	2-7
		5.0	1.5	5.5	11.5	1.5	15.0	1.0	13.0		
t_{PHZ}	Output Disable $\overline{OE}$ to O_n	3.3	2.0	6.5	13.0	1.0	17.0	1.5	13.5	ns	2-7
		5.0	1.0	5.0	10.0	1.5	13.0	1.0	11.0		
f_{SI}	Maximum SI Clock Frequency	3.3	35.0			20.0		30.0		MHz	
		5.0	60.0			45.0		50.0			
f_{SO}	Maximum SO Clock Frequency	3.3	25.0			15.0		20.0		MHz	
		5.0	45.0			30.0		35.0			

*Voltage Range 3.3 is 3.3V ± 0.3V

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: See Section 2 for waveforms (Continued)

Symbol	Parameter	*V_{CC} (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay, t_{IR} SI to IR	5.0	2.0	6.5	11.0			1.5	12.5	ns	1
t_{PHL}	Propagation Delay, t_{IR} SI to IR	5.0	2.0	6.5	11.0			1.5	12.0	ns	1
t_{PLH}	Propagation Delay, t_{IHF} SI to > HF	5.0	4.0	10.5	17.0			4.0	19.5	ns	1
t_{PHL}	Propagation Delay, t_{IF} SI to Full Condition	5.0	4.5	10.5	16.5			4.5	19.5	ns	1
t_{PLH}	Propagation Delay, t_{IE} SI to Not Empty	5.0	4.0	10.0	15.5			4.0	17.5	ns	1
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	5.0	4.0	13.5	16.5			4.0	19.0	ns	1
t_{PLH}	Propagation Delay t_{MRIRH} $\overline{MR}$ to IR	5.0	3.0	8.5	13.5			3.0	15.5	ns	2
t_{PHL}	Propagation Delay, t_{MRORL} $\overline{MR}$ to OR	5.0	7.0	16.5	25.5			7.0	29.0	ns	2
t_{PHL}	Propagation Delay, t_{MRO} $\overline{MR}$ to Full Flag	5.0	3.5	9.0	14.0			3.5	16.0	ns	2
t_{PHL}	Propagation Delay, t_{MRE} $\overline{MR}$ to HF Flag	5.0	8.0	17.5	27.5			8.0	30.5	ns	2
t_{PHL}	Propagation Delay, t_{MRONL} $\overline{MR}$ to O_n, LOW	5.0	3.0	9.0	15.0			3.0	17.0	ns	2
t_W	IR Pulse Width, t_{IP}	5.0	16.5	28.0	43.0			16.5	51.5	ns	3
t_W	HF Pulse Width, t_{3F}	5.0	17.5	30.0	46.5			17.5	56.0	ns	3
t_{PLH}	Propagation Delay, t_D SO to Data Out	5.0	6.5	18.5	27.0			6.5	31.0	ns	3, 4
t_{PHL}	Propagation Delay, t_D SO to Data Out	5.0	6.5	18.5	29.5			6.5	34.5	ns	3, 4
t_{PHL}	Propagation Delay, t_{OHF} SO to < HF	5.0	3.5	8.5	13.5			3.5	15.5	ns	4
t_{PLH}	Propagation Delay, t_{OF} SO to Not Full	5.0	5.0	12.5	19.5			5.0	22.0	ns	3, 4
t_{PLH}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	5.0	2.5	7.0	11.5			2.5	13.5	ns	4

*Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: See Section 2 for waveforms (Continued)

Symbol	Parameter	*V_{CC} (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay, t_{OE} SO to Empty	5.0	3.5	9.5	15.5			3.0	17.5	ns	4
t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	5.0	7.0	19.0	30.5			6.0	35.5	ns	5
t_{PHL}	Propagation Delay, t_{OD5} SI to New Data Out	5.0	7.0	19.0	29.5			6.0	34.5	ns	5
t_{PLH}	Propagation Delay, t_{X1} SI to HF	5.0	3.5	10.0	16.0			2.5	18.0	ns	5
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	5.0	3.5	13.5	21.0			1.5	24.0	ns	5
t_W	OR Pulse Width, t_{OP}	5.0	12.5	17.0	26.0			12.5	30.5	ns	5
t_W	HF Pulse Width, t_{X3}	5.0	14.5	20.5	30.5			14.5	36.5	ns	5
t_{PLH}	Fall-Through Times, t_{FT} SO to IR	5.0	6.0	15.0	23.5			2.5	28.0	ns	5
t_{PZL}	Output Enable $\overline{OE}$ to O_n	5.0	2.0	6.5	11.0			1.5	12.0	ns	2-6
t_{PLZ}	Output Disable $\overline{OE}$ to O_n	5.0	1.5	5.0	8.5			1.5	9.5	ns	2-6
t_{PZH}	Output Enable $\overline{OE}$ to O_n	5.0	2.0	7.0	12.0			1.5	13.0	ns	2-5
t_{PHZ}	Output Disable $\overline{OE}$ to O_n	5.0	1.5	7.0	12.0			1.5	13.0	ns	2-5
f_{SI}	Maximum SI Clock Frequency	5.0	55	85				45		MHz	
f_{SO}	Maximum SO Clock Frequency	5.0	42	60				35		MHz	

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	*V_{CC} (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
$t_W(H)$	SI Pulse Width, t_{SIH}	3.3 5.0	9.0 5.5	16.5 10.5	11.0 9.0	20.5 12.5	ns	1
$t_W(L)$	SI Pulse Width, t_{SIL}	3.3 5.0	8.5 6.5	16.0 12.0	26.0 14.0	19.5 14.5	ns	1
t_S	Setup Time, HIGH or LOW, D_n to SI	3.3 5.0	−2.0 −1.5	1.0 1.0	2.0 0.0	1.0 1.0	ns	1
t_H	Hold Time, HIGH or LOW, D_n to SI	3.3	1.0 1.0	5.5 4.0	7.0 7.0	6.0 4.5	ns	1
t_W	$\overline{MR}$ Pulse Width, t_{MRW}	3.3 5.0	13.0 8.5	26.0 16.0	34.0 22.0	30.5 20.0	ns	2
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	3.3 5.0	4.5 3.0	8.0 6.0	11.0 8.0	9.5 7.0	ns	2
$t_W(H)$	SO Pulse Width, t_{SOH}	3.3 5.0	4.0 2.5	7.5 5.5	24.0 15.0	8.5 6.5	ns	4
$t_W(L)$	SO Pulse Width, t_{SOL}	3.3 5.0	10.0 6.0	18.0 12.0	23.0 16.0	21.0 14.0	ns	4

*Voltage Range 3.3 is 3.3V ± 0.3V
*Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements

Symbol	Parameter	*V_{CC} (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
$t_W(H)$	SI Pulse Width, t_{SIH}	5.0	3.5	6.5		7.5	ns	1
$t_W(L)$	SI Pulse Width, t_{SIL}	5.0	6.0	10.0		12.0	ns	1
t_S	Setup Time, HIGH or LOW, D_n to SI	5.0	1.0	3.5		4.5	ns	1
t_H	Hold Time, HIGH or LOW, D_n to SI	5.0	1.5	3.5		4.5	ns	1
t_W	$\overline{MR}$ Pulse Width, t_{MRW}	5.0	13.0	20.0		24.5	ns	2
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	5.0	4.5	7.5		8.5	ns	2
$t_W(H)$	SO Pulse Width, t_{SOH}	5.0	7.5	6.5		8.0	ns	4
$t_W(L)$	SO Pulse Width, t_{SOL}	5.0	9.0	14.0		17.0	ns	4

*Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT2725
512 x 9 First In, First Out Memory (FIFO)

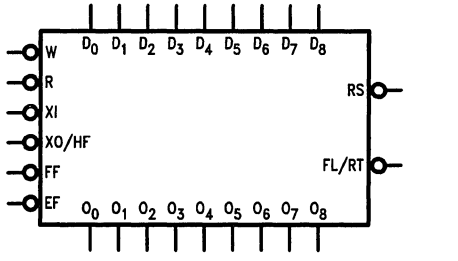
General Description

The 512 x 9 FIFO is a first-in, first-out dual port memory capable of asynchronous, simultaneous read and write. Other important features are: expansion capability in both the word depth and bit width, half-full flag capability in the single device mode, empty and full warning flags, ring pointers for fall-through time; it is suited for high-speed applications.

Features

- First-in, first-out dual port memory
- 512 x 9 organization
- Low power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by word depth and/or bit width
- Half-full flag capability in single device mode
- Empty and full warning flags
- Auto retransmit capability
- Outputs source/sink 8 mA
- 'ACT2725 has TTL-compatible inputs
- Pin and functionality compatible with IDT7201A

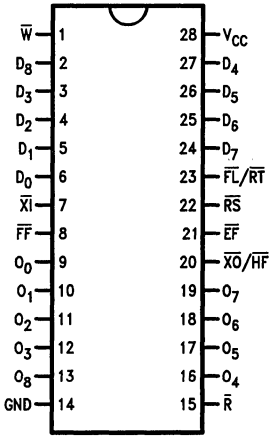
Logic Symbol



TL/F/10138–3

Connection Diagram

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10138–1

Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{XI}$	Expansion In
$\overline{XO}/\overline{HF}$	Expansion Out, Half-Full Flag
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag
$\overline{RS}$	Reset
$\overline{FL}/\overline{RT}$	First Load/Retransmit

4

National Semiconductor

ADVANCE INFORMATION

54ACT/74ACT2726
512 x 9 Bidirectional First In, First Out Memory (BIFIFO)

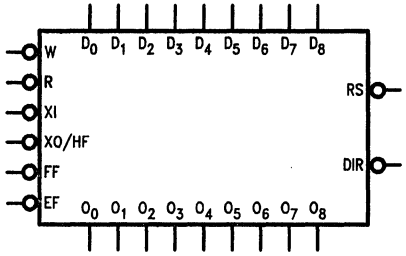
General Description

The 512 x 9 FIFO is a first-in, first-out dual port memory capable of asynchronous, simultaneous read and write. Other important features are: expansion capability in both the word depth and bit width, half-full flag capability in the single device mode, empty and full warning flags, and ring pointers for zero fall-through time. There are two sets of bidirectional ports, each 9 bits wide, through which data flow can be controlled. A direction pin (DIR) controls the direction of the data: when the DIR is HIGH, A is the input port and B is the output port. When the DIR is LOW, the input port is B and output port is A. It is suited for high-speed applications.

Features

- First-in, first-out bidirectional memory
- 512 x 9 organization
- Low power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by word depth and/or bit width
- Half-full flag capability in single device mode
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Outputs source/sink 8 mA
- 'ACT2726 has TTL-compatible inputs

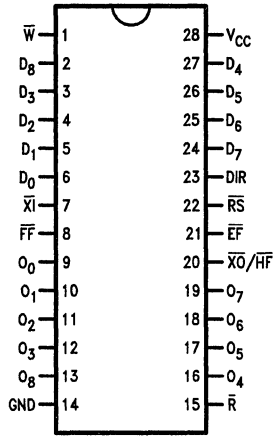
Logic Symbol



TL/F/10656–1

Connection Diagram

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10656–2

Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{XI}$	Expansion In
$\overline{XO}/\overline{HF}$	Expansion Out, Half-Full Flag
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag
$\overline{RS}$	Reset
DIR	Direction

Section 5

Quiet Series Datasheets

Section 5 Contents

National Semiconductor

54ACQ/74ACQ153 • 54ACTQ/74ACTQ153
Quiet Series Dual 4-Input Multiplexer

General Description

The 'ACQ/'ACTQ153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'ACQ/'ACTQ153 can act as a function generator and generate any two functions of three variables.

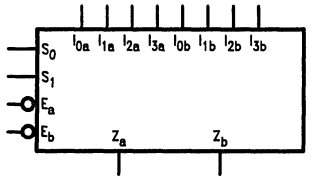
Features

- Outputs source/sink 24 mA
- 'ACTQ153 has TTL-compatible inputs
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity

The information for the 'ACQ153 is advanced information only.

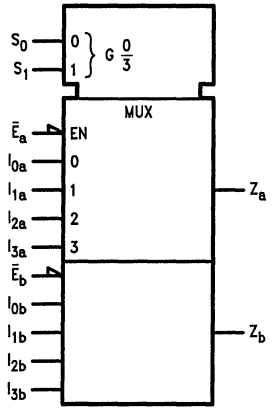
Ordering Code: See Section 8

Logic Symbols



TL/F/10244–1

IEEE/IEC

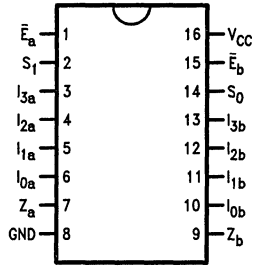


TL/F/10244–2

Pin Names	Description
I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\bar{E}_a$	Side A Enable Input
$\bar{E}_b$	Side B Enable Input
Z_a	Side A Output
Z_b	Side B Output

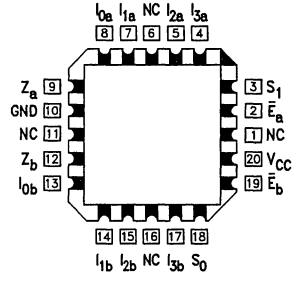
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10244–3

Pin Assignment for LCC



TL/F/10244–4

Functional Description

The 'ACQ/'ACTQ153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs indepedently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The 'ACQ/'ACTQ153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

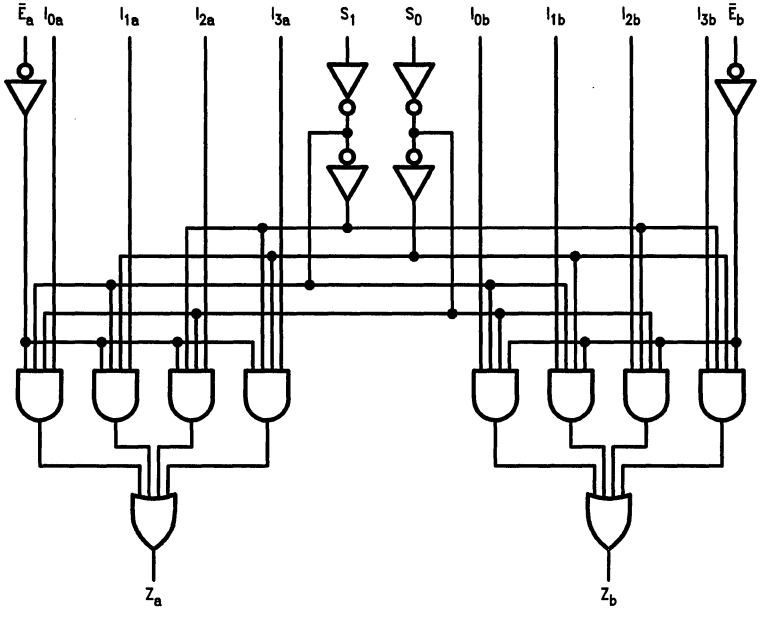
$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



TL/F/10244–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ T_A = +25°C		54ACTQ T_A = −55°C to +125°C	74ACTQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4		I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.70	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1		I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ		Guaranteed Limits			
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{IHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Curent	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5			V	*Figures 1, 2* (Note 2, 3)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2			V	*Figures 1, 2*
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	†Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of Data Inputs defined as (n). n − 1 Data Inputs are driven 0V to 5V. One Data Input @ V_{IN} = GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V ('ACTQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	3.0	7.0	11.5			2.0	13.5	ns	2-3, 4
t_{PHL}	Propagation Delay S_n to Z_n	5.0	3.0	7.0	11.5			2.5	13.5	ns	2-3, 4
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	2.0	6.5	10.5			2.0	12.5	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	3.0	6.0	9.5			2.5	11.0	ns	2-3, 4
t_{PLH}	Propagation Delay I_n to Z_n	5.0	2.5	5.5	9.5			2.0	11.0	ns	2-3, 4
t_{PHL}	Propagation Delay I_n to Z_n	5.0	2.0	5.5	9.5			2.0	11.0	ns	2-3, 4

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	65.0	pF	V_{CC} = 5.0V

National Semiconductor

54ACQ/74ACQ240 • 54ACTQ/74ACTQ240 Quiet Series Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

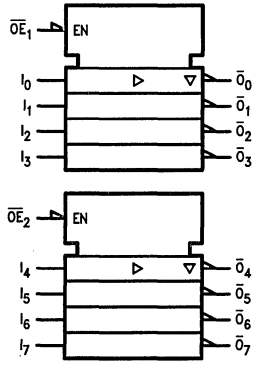
Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'ACT240
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbol

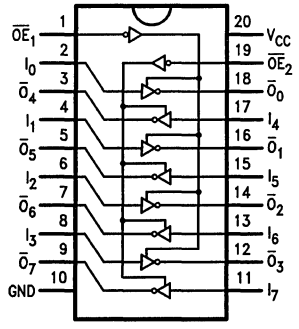
IEEE/IEC



TL/F/10234–1

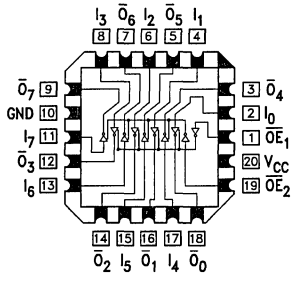
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10234–2

Pin Assignment for LCC and PCC



TL/F/10234–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C		54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND (Note 1)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n − 1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5			V	*Figures 1, 2* (Note 2, 3)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of Data Inputs defined as (n). n−1 Data Inputs are driven 0V to 3V. One Data Input @ V_{IN} = GND.

Note 4: Max number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF Min	74ACQ Typ	74ACQ Max	54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	54ACQ Max	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	74ACQ Max	Units	Fig. No.
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	7.0 5.0	10.0 6.5			2.0 1.5	10.5 7.0	ns	2–3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3 5.0	2.5 1.5	8.0 5.5	12.0 8.0			2.5 1.5	12.5 8.5	ns	2–5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.5 6.0	13.5 9.0			1.0 1.0	14.0 9.5	ns	2–5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3 5.0		1.0 0.5	1.5 1.0				1.5 1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3 ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	5.0	1.5	5.5	7.0	1.5	9.0	1.5	7.5	ns	2–3, 4
t_{PZL}, t_{PZH}	Output Enable Time	5.0	1.5	6.5	8.5	1.5	11.0	1.5	9.0	ns	2–5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	7.0	9.5	1.5	10.0	1.0	10.0	ns	2–5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	70	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACQ/74ACQ241 • 54ACTQ/74ACTQ241 Quiet Series Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

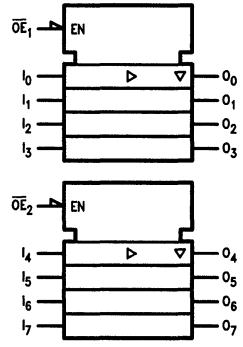
Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT241
- 4 kV minimum ESD immunity ('ACTQ)

Ordering Code: See Section 8

Logic Symbol

IEE/IEC



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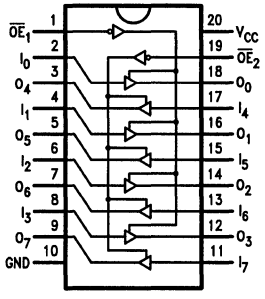
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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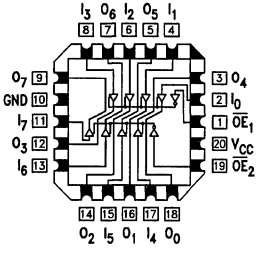
Pin Assignment for LCC and PCC



TL/F/10642–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C	74ACQ T_A = −55°C to +125°C	54ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.7		I_{OH} −12 mA
		5.5		4.86	4.7		I_{OH} −24 mA
					2.46		I_{OH} −24 mA
					3.76		I_{OH} −24 mA
					4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.50	V	*V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.50		I_{OL} 12 mA
		5.5		0.36	0.50		I_{OL} 24 mA
					0.44		I_{OL} 24 mA
					0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND (Note 1)
					±1.0		V_I = V_{CC}, GND (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n−1 Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits			
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case DIP package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n−1 Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: *See Section 2 for Waveforms*

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF			54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	3.3	2.0	6.5	9.0			2.0	9.5	ns	2-3, 4
		5.0	1.5	4.5	6.0			1.5	6.5		
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.0	13.0			2.5	13.5	ns	2-5, 6
		5.0	1.5	5.5	8.5			1.5	9.0		
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	8.5	14.5			1.0	15.0	ns	2-5, 6
		5.0	1.0	5.5	9.5			1.0	10.0		
t_{OSHL}, t_{OSLH}	Output to Output Skew **Data to Output	3.3		1.0	1.5				1.5	ns	
		5.0		0.5	1.0				1.0		

*Voltage Range 5.0 is 5.0V ±0.5V.
Voltage Range 3.3 is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	5.0	1.5	5.0	6.5	1.5	8.0	1.5	7.0	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	5.0	1.5	6.5	9.0	1.5	10.5	1.5	9.5	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	7.0	10.0	1.5	9.5	1.0	10.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew **Data to Output	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	70	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACQ/74ACQ244 • 54ACTQ/74ACTQ244 Quiet Series Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

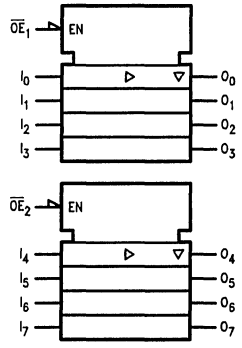
Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT244
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbol

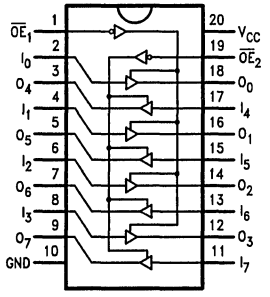
IEE/IEC



TL/F/10235–1

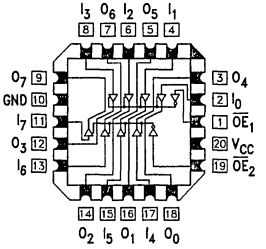
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10235–2

Pin Assignment for LCC and PCC



TL/F/10235–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C Typ	74ACQ T_A = +25°C Guaranteed Limits	54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND (Note 1)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND (Note 1)

*All outputs loaded thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50$ μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	$I_{OUT} = 50$ μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−50	−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)

*All outputs loaded thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	7.0 5.0	9.0 6.0			2.0 1.5	9.5 6.5	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3 5.0	2.5 1.5	8.0 6.5	12.0 8.0			2.5 1.5	12.5 8.5	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	9.0 7.5	13.5 9.0			1.0 1.0	14.0 9.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3 5.0		1.0 0.5	1.5 1.0				1.5 1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

Voltage Range 3.3 is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	5.0	1.5	5.5	6.5	1.5	9.0	1.5	7.0	ns	2-7
t_{PZL}, t_{PZH}	Output Enable Time	5.0	1.5	7.0	8.5	1.5	10.5	1.5	9.0	ns	2-7
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	9.5	1.5	10.5	1.0	10.0	ns	2-3
t_{OSHL}, t_{OSLH}	Output to Output Skew ** Data to Output	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	70	pF	V_{CC} = 5.0V

National Semiconductor

54ACQ/74ACQ245 • 54ACTQ/74ACTQ245 Quiet Series Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

The 'ACQ/'ACTQ245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

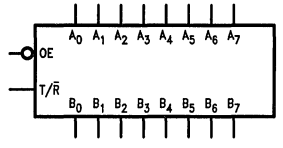
The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'ACT245
- 4 kV minimum ESD immunity ('ACQ)

Ordering Code: See Section 8

Logic Symbols



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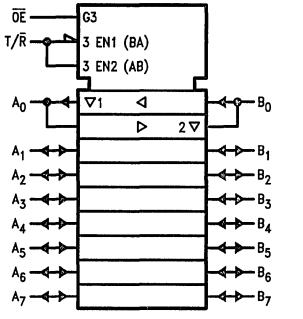
IEEE/IEC



TL/F/10236–2

Pin Names	Description
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A TRI-STATE Inputs or TRI-STATE Outputs
B_0–B_7	Side B TRI-STATE Inputs or TRI-STATE Outputs

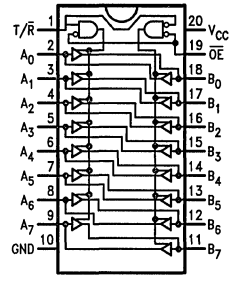
Truth Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

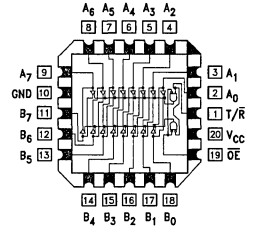
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10236–3

Pin Assignment for LCC and PCC



TL/F/10236–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C		54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.6	±11.0	±6.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2,3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). n−1 Data Inputs are driven 0V to 3V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF			54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	7.5 5.0	10.0 6.5			2.0 1.5	10.5 7.0	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3 5.0	3.0 2.0	8.5 6.0	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.5 7.5	14.5 9.5			1.0 1.0	15.0 10.0	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	3.3 5.0		1.0 0.5	1.5 1.0				1.5 1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	5.0	1.5	5.5	7.0	1.5	9.0	1.5	7.5	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.0	9.0	1.5	12.0	2.0	9.5	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.0	11.5	1.0	10.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Output	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	80.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACQ/74ACQ273 • 54ACTQ/74ACTQ273
Quiet Series Octal D Flip-Flop

General Description

The 'AC/'ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

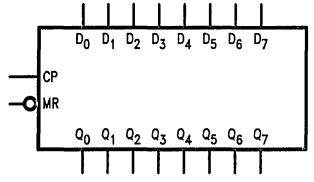
Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered common clock and asynchronous master reset
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT273
- 4 kV minimum ESD immunity

The information for the ACQ273 is Advanced Information only.

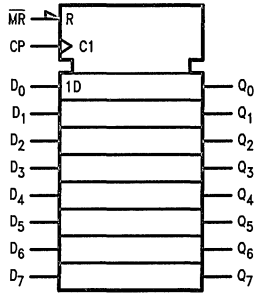
Ordering Code: See Section 8

Logic Symbols



TL/F/10585–1

IEEE/IEC



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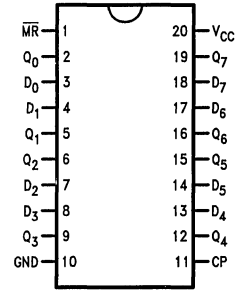
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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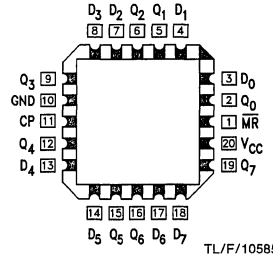
Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

Pin Assignment for LCC



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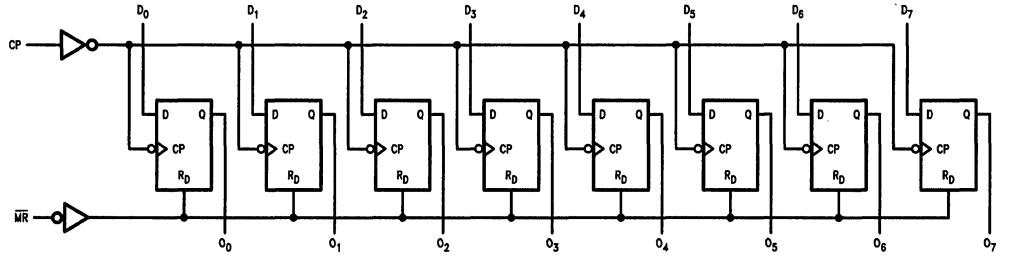
Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/10585–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$ 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$ 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ T_A = +25°C		54ACTQ T_A = −55°C to +125°C	74ACTQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.7	3.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA
		5.5		4.86	4.7	4.76		
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} −24 mA
		5.5		0.36	0.50	0.44		
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). n − 1 Data inputs are driven 0V to 3V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	125	189		85		110		MHz	
t_{PHL}, t_{PLH}	Propagation Delay Clock to Output	5.0	1.5	6.5	8.5	1.5	10.0	1.5	9.0	ns	2-3, 4
t_{PHL}	Propagation Delay $\overline{MR}$ to Output	5.0	1.5	7.0	9.0	1.5	11.0	1.5	9.5	ns	2-3, 4
t_{OSHL}, t_{OSLH}	Output to Output Skew** Data to Ouput	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW Data to CP	5.0	1.0	3.5	5.0	3.5	ns	2-7
t_h	Hold Time, HIGH or LOW Data to CP	5.0	−0.5	1.5	2.0	1.5	ns	2-7
t_w	Clock Pulse Width HIGH or LOW	5.0	2.0	4.0	5.0	4.0	ns	2-3
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	5.0	1.5	4.0	5.0	4.0	ns	2-3
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0.5	3.0		3.0	ns	2-3, 7

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACQ/74ACQ373 • 54ACTQ/74ACTQ373 Quiet Series Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

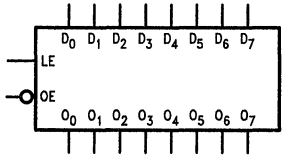
The 'ACQ/'ACTQ373 utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch up immunity
- Eight latches in a single package
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT373
- 4 kV minimum ESD immunity ('ACQ)

Ordering Code: See Section 8

Logic Symbols



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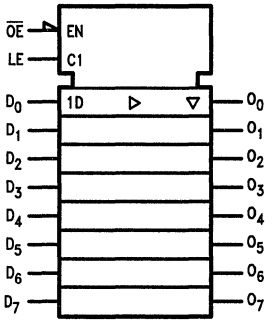
IEEE/IEC

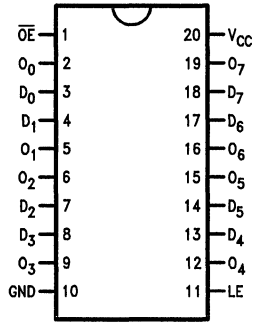


TL/F/10237–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

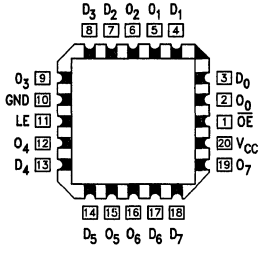
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10237–3

Pin Assignment for LCC and PCC



TL/F/10237–4

Functional Description

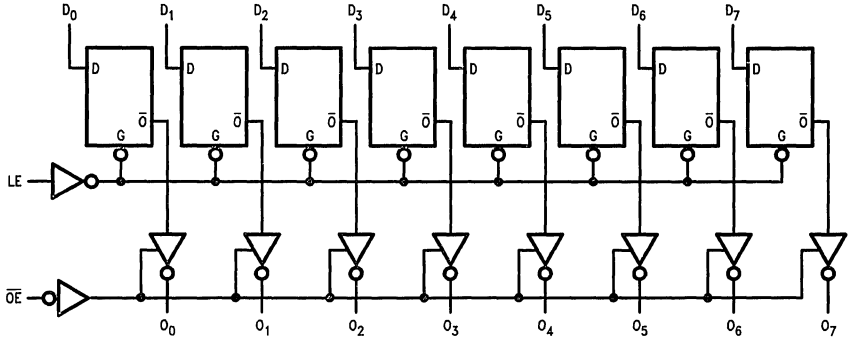
The 'ACQ/'ACTQ373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latchup Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C		54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND (Note 1)

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I(OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Maximum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6	1.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5		50		75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5		−50		−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	8.0	160.0		80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	3.3	2.5	8.0	10.5			2.5	11.0	ns	2-3, 4
		5.0	1.5	5.5	7.0			1.5	7.5		
t_{PLH}, t_{PLH}	Propagation Delay LE to O_n	3.3	2.5	8.0	12.0			2.5	12.5	ns	2-3, 4
		5.0	2.0	6.0	8.0			2.0	8.5		
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.5	13.0			2.5	13.5	ns	2-5, 6
		5.0	1.5	6.5	8.5			1.5	9.0		
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.0	14.5			1.0	15.0	ns	2-5, 6
		5.0	1.0	6.5	9.5			1.0	10.0		
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	3.3		1.0	1.5				1.5	ns	
		5.0		0.5	1.0				1.0		

*Voltage Range 5.0 is 5.0V ±0.5V.
Voltage Range 3.3 is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$ $C_L = 50$ pF		54ACQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	0 0	3.0 3.0		3.0 3.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0	1.5 1.5		1.5 1.5	ns	2-7
t_w	LE Pulse Width, HIGH	3.3 5.0	2.0 2.0	4.0 4.0		4.0 4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V.
Voltage Range 3.3 is 3.3V ±0.3V.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	5.0	2.0	6.5	7.5	1.5	10.5	2.0	8.0	ns	2-3, 4
t_{PLH}, t_{PLH}	Propagation Delay LE to O_n	5.0	2.5	7.0	8.5	1.5	11.5	2.5	9.0	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.0	9.0	1.5	11.0	2.0	9.5	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.5	10.5	1.0	10.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.
Voltage Range 3.3 is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	0	3.0	3.5	3.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0	1.5	1.5	1.5	ns	2-7
t_w	LE Pulse Width, HIGH	5.0	2.0	4.0	5.0	4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V
*Voltage Range 3.3 is 3.3V ±0.3V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	44.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACQ/74ACQ374 • 54ACTQ/74ACTQ374 Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

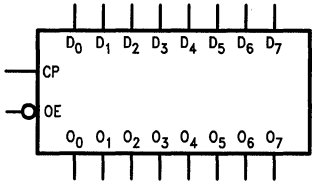
The 'ACQ/'ACTQ374 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT374
- 4 kV minimum ESD immunity

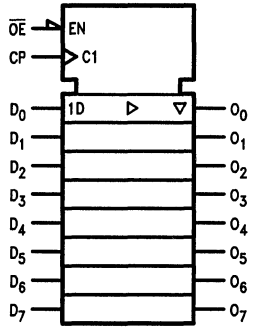
Ordering Code: See Section 8

Logic Symbols



TL/F/10238–1

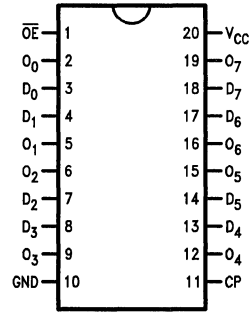
IEEE/IEC



TL/F/10238–2

Connection Diagrams

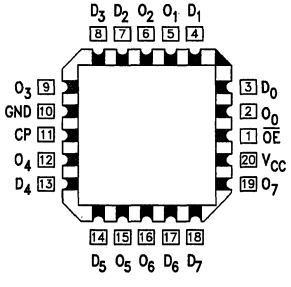
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10238–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Pin Assignment for LCC and PCC



TL/F/10238–4

Functional Description

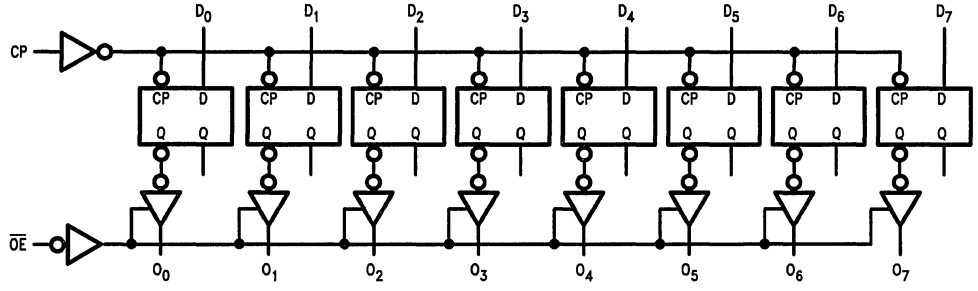
The 'ACQ/'ACTQ374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C		54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±50	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1* and *2* (Notes 2 and 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1* and *2* (Notes 2 and 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2 and 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2 and 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n − 1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1* and *2* (Notes 2 and 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1* and *2* (Notes 2 and 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2 and 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2 and 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF			54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	75 90					70 85		MHz	
t_{PLH}, t_{PHL}	Propagation Delay CP to O_n	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	9.5 8.0	14.5 9.5			1.0 1.0	15.0 10.0	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to O_n	3.3 5.0		1.0 0.5	1.5 1.0				1.5 1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF		54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	0 0	3.0 3.0		3.0 3.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 2.0	1.5 1.5		1.5 1.5	ns	2-7
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	4.0 4.0		4.0 4.0	ns	2-3

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85			95		80		MHz	
t_{PLH}, t_{PHL}	Propagation Delay CP to O_n	5.0	2.0	7.0	9.0	2.0	11.5	2.0	9.5	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.5	9.0	2.0	11.5	2.0	9.5	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.5	10.5	1.0	10.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to O_n	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	0	3.0	3.5	3.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5	2.0	1.5	ns	2-7
t_w	CP Pulse Width, HIGH or LOW	5.0	2.0	4.0	5.0	4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	42.0	pF	$V_{CC} = 5.0V$

National Semiconductor

ADVANCE INFORMATION

54ACQ/74ACQ377 • 54ACTQ/74ACTQ377
Quiet Series Octal D Flip-Flop with Clock Enable

General Description

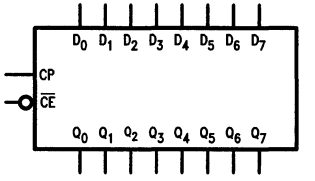
The 'ACQ/'ACTQ377 has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is low. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

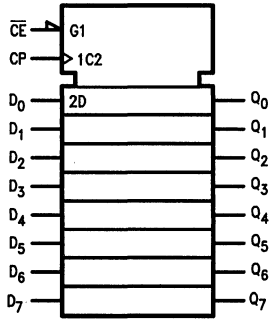
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT377
- 4 kV minimum ESD immunity

Logic Symbols



TL/F/10151–1

IEEE/IEC

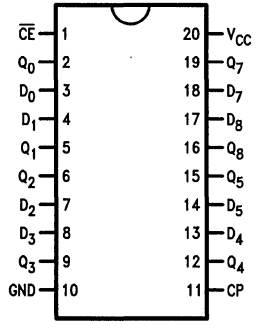


TL/F/10151–2

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

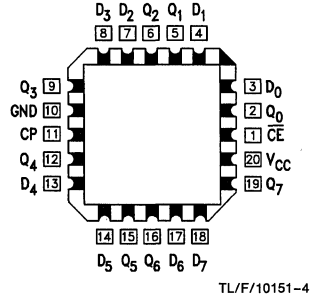
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10151–3

Pin Assignment for LCC



TL/F/10151–4

National Semiconductor

54ACQ/74ACQ533 • 54ACTQ/74ACTQ533 Quiet Series Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

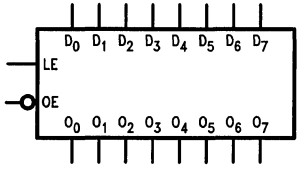
The 'ACQ/'ACTQ533 utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch up immunity
- Eight latches in a single package
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Inverted version of the 'ACQ/'ACTQ373
- 4 kV minimum ESD immunity

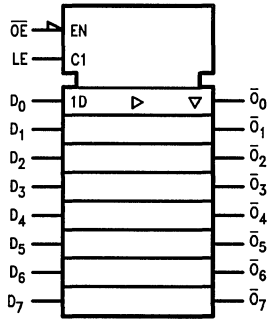
Ordering Code: See Section 8

Logic Symbols



TL/F/10630–1

IEEE/IEC

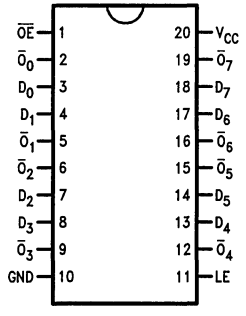


TL/F/10630–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Latch Outputs

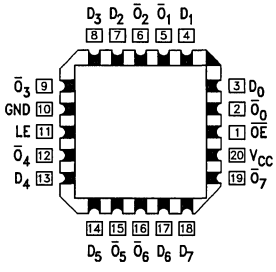
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10630–3

Pin Assignment for LCC



TL/F/10630–4

Functional Description

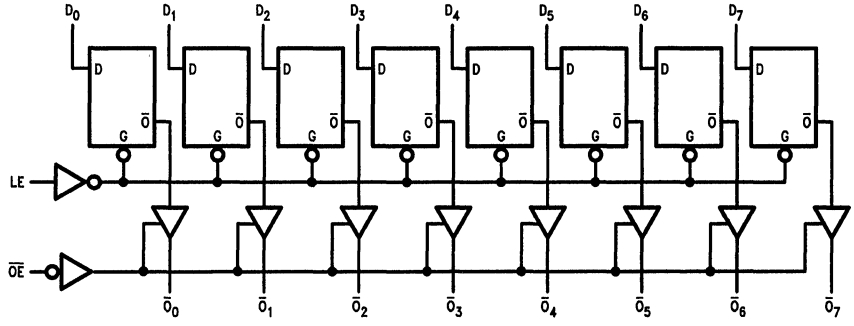
The 'ACQ/'ACTQ533 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	$\overline{O}_n$
X	H	X	Z
H	L	L	H
H	L	H	L
L	L	X	$\overline{O}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
$\overline{O}_0$ = Previous $\overline{O}_0$ before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/10630–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latchup Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C		54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		2.56	2.4	2.46	V	−12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
								*V_{IN} = V_{IL} or V_{IH}
		3.0		0.36	0.50	0.44	V	12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND (Note 1)

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	3.3	2.5	8.5	11.5			2.5	12.0	ns	2-3, 4
		5.0	1.5	5.5	7.5			1.5	8.0		
t_{PLH}, t_{PLH}	Propagation Delay LE to O_n	3.3	2.5	2.5	13.0			2.5	13.5	ns	2-3, 4
		5.0	2.0	6.0	8.5			2.0	9.0		
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.5	13.0			2.5	13.5	ns	2-5, 6
		5.0	1.5	6.0	8.5			1.5	9.0		
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.0	14.5			1.0	15.0	ns	2-5, 6
		5.0	1.0	6.5	9.5			1.0	10.0		
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	3.3		1.0	1.5				1.5	ns	
		5.0		0.5	1.0				1.0		

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$ $C_L = 50$ pF		54ACQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	0 0	3.0 3.0		3.0 3.0	ns	2-7
t_H	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0	1.5 1.5		1.5 1.5	ns	2-7
t_W	LE Pulse Width, HIGH	3.3 5.0	2.0 2.0	4.0 4.0		4.0 4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V.
Voltage Range 3.3 is 3.3V ±0.3V.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	5.0	2.0	6.0	8.0			2.0	8.5	ns	2-3, 4
t_{PLH}, t_{PLH}	Propagation Delay LE to O_n	5.0	2.5	7.0	9.0			2.5	9.5	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.0	9.0			2.0	9.5	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0			1.0	10.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to LE	5.0	0	3.0		3.0	ns	2-7
t_H	Hold Time, HIGH or LOW D_n to LE	5.0	0	1.5		1.5	ns	2-7
t_W	LE Pulse Width, HIGH	5.0	2.0	4.0		4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACQ/74ACQ534•54ACTQ/74ACTQ534
Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'ACQ/'ACTQ534 is the same as the 'ACQ/'ACTQ374 except that the outputs are inverted.

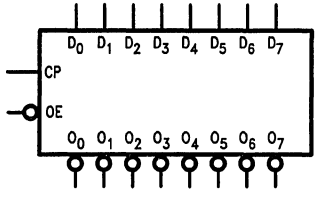
The 'ACQ/'ACTQ534 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Inverted output version of the 'ACQ/'ACTQ374
- Faster prop delays than the standard 'ACT534
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbols



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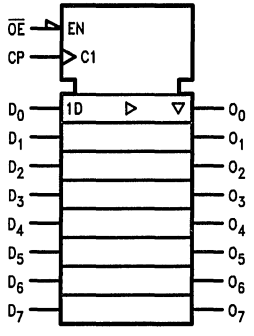
IEEE/IEC



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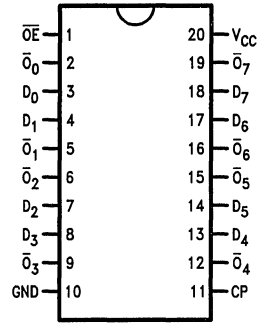
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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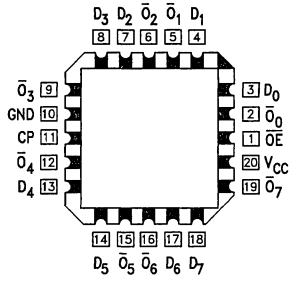
Pin Assignment for LCC



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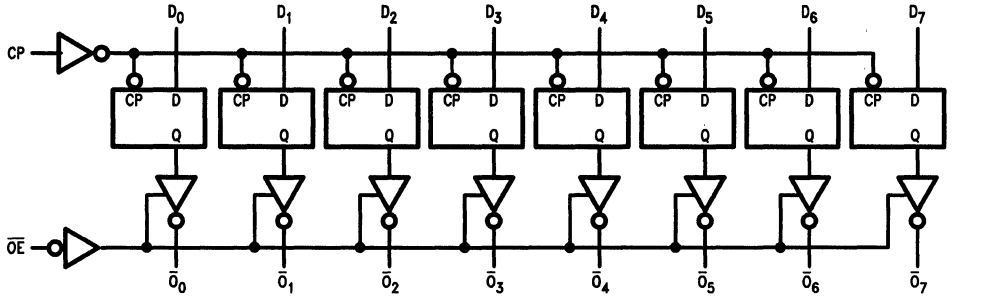
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

Functional Description

The 'ACQ/'ACTQ534 consists of eight D-type flip-flops with individual inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs			Output
CP	OE	D	$\overline{O}$
⌐	L	H	L
⌐	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
Z = High Impedance
$\overline{O}_0$ = Value stored from previous clock cycle

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C		54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IH}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Note 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5			V	*Figures 1, 2* (Note 2, 3)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of Data Inputs defined as (n). n−1 Data Inputs are driven 0V to 3V. One Data Input @ V_{IN} = GND.

Note 4: Max number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF			54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	75 90					70 85		MHz	
t_{PHL}, t_{PLH}	Propagation Delay CP to $\overline{Q}_n$	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	9.5 8.0	14.5 9.5			1.0 1.0	15.0 10.0	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to $\overline{Q}_n$	3.3 5.0		1.0 0.5	1.5 1.0				1.5 1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V, Voltage Range 3.3 is 3.3V ± 0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF		54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	1.0 1.0	3.0 3.0		3.0 3.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0	1.5 1.5		1.5 1.5	ns	2-7
t_w	CP Pulse Width HIGH or LOW	3.3 3.3	2 2	4.0 4.0		4.0 4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V, Voltage Range 3.3 is 3.3V ± 0.3V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85					80		MHz	
t_{PHL}, t_{PLH}	Propagation Delay CP to $\overline{Q}_n$	5.0	2.0	7.0	9.0			2.0	9.5	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.0	9.0			2.0	9.5	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0			1.0	10.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to $\overline{Q}_n$	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	3.0		3.0	ns	2-7
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5		1.5	ns	2-7
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0		4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

National Semiconductor

ADVANCE INFORMATION

54ACQ/74ACQ543 • 54ACTQ/74ACTQ543 Quiet Series Octal Registered Transceiver with TRI-STATE® Outputs

General Description

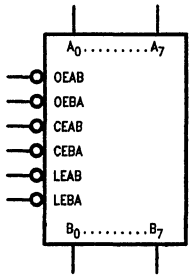
The ACQ/ACTQ543 is a non-inverting octal transceiver containing two sets of D-type registers for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

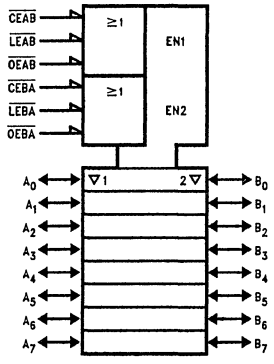
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- 8-bit octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back registers for storage
- Outputs source/sink 24 mA
- 4 kV minimum ESD immunity

Logic Symbols



TL/F/10154-1

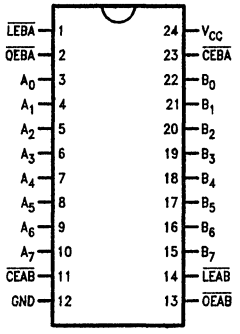
IEEE/IEC



TL/F/10154-4

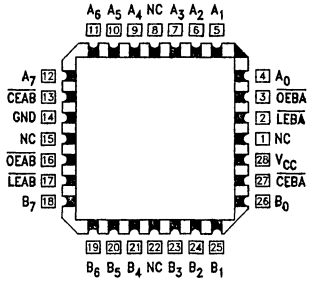
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/10154-2

Pin Assignment for LCC and PCC



TL/F/10154-3

National Semiconductor

ADVANCE INFORMATION

54ACQ/74ACQ544 • 54ACTQ/74ACTQ544 Quiet Series Octal Registered Transceiver with TRI-STATE® Outputs

General Description

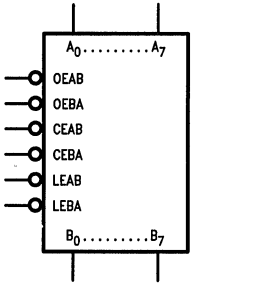
The ACQ/ACTQ544 is an inverting octal transceiver containing two sets of D-type registers for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow. The '544 inverts data in both directions.

The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

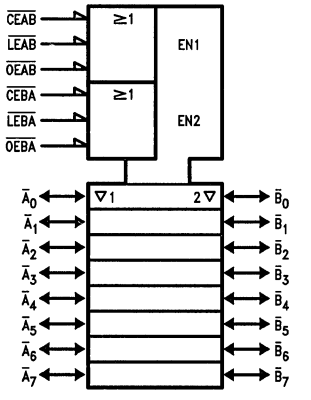
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- 8-bit inverting octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back registers for storage
- Outputs source/sink 24 mA
- 4 kV minimum ESD immunity
- 300 mil slim PDIP/SOIC

Logic Symbols



TL/F/10685–1

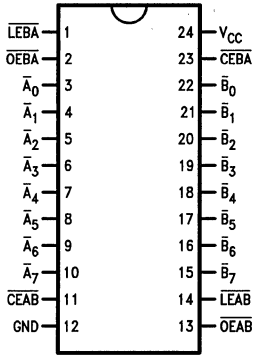
IEEE/IEC



TL/F/10685–4

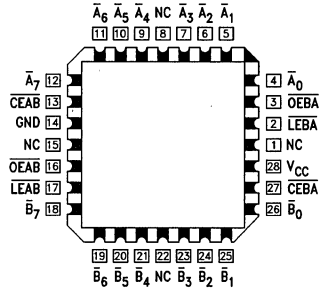
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/10685–2

Pin Assignment for LCC and PCC



TL/F/10685–3

National Semiconductor

54ACQ/74ACQ563 • 54ACTQ/74ACTQ563
Quiet Series Octal Latch with TRI-STATE® Outputs

General Description

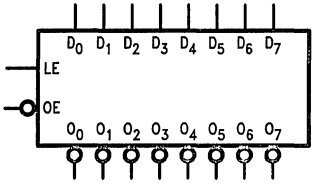
The 'ACQ/'ACTQ563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The 'ACQ/'ACTQ563 is functionally identical to the 'ACQ/'ACTQ573, but with inverted outputs. The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Outputs source/sink 24 mA
- Faster prop delays than standard ACT563
- Functionally identical to the ACQ/ACTQ573 but with inverted outputs
- 4 kV minimum ESD immunity

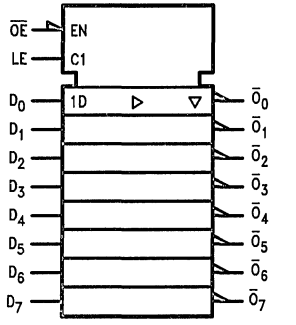
Ordering Code: See Section 8

Logic Symbols



TL/F/10631–1

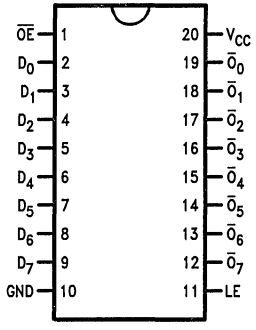
IEEE/IEC



TL/F/10631–2

Connection Diagrams

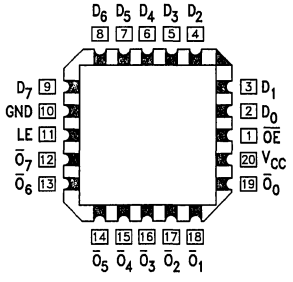
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10631–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Latch Outputs

Pin Assignment for LCC



TL/F/10631–4

Functional Description

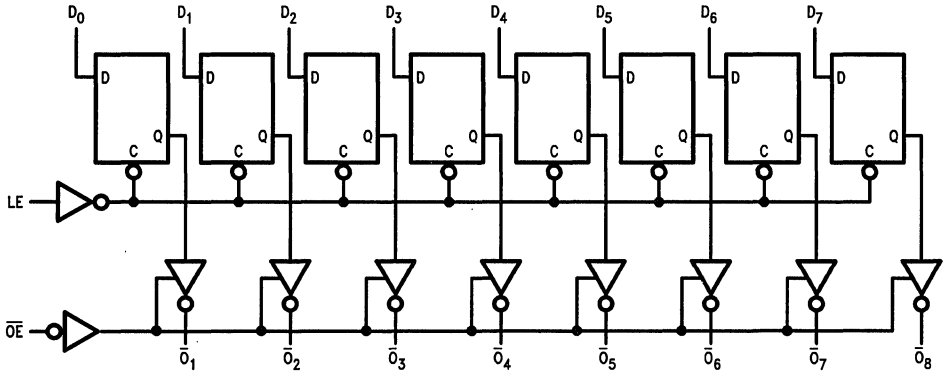
The 'ACQ/'ACTQ563 contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High-Z
H	H	L	H	Z	High-Z
H	H	H	L	Z	High-Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/10631–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latchup Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C	74ACQ	54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ		54ACQ	74ACQ	Units	Conditions
			$T_A = +25°C$		$T_A = -55°C$ to $+125°C$	$T_A = -40°C$ to $+85°C$		
			Typ	Guaranteed Limits				
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND (Note 2)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I(OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @5.5V V_{CC}.
I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Maximum number of Data Inputs (n) switching. (n−1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = − 50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} − 24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1		I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND (Note 1)
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2			V	*Figures 1, 2* (Note 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching; 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF			54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	3.3	2.5	8.5	11.5			2.5	12.0	ns	2-3, 4
		5.0	1.5	5.5	7.5			1.5	8.0		
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	3.3	2.5	8.5	13.0			2.5	13.5	ns	2-3, 4
		5.0	2.0	6.0	8.5			2.0	9.0		
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.5	13.0			2.5	13.5	ns	2-5, 6
		5.0	1.5	6.0	8.5			1.5	9.0		
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.0	14.5			1.0	15.0	ns	2-5, 6
		5.0	1.0	6.5	9.5			1.0	10.0		
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	3.3		1.0	1.5				1.5	ns	
		5.0		0.5	1.0				1.0		

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF		54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to LE	3.3	0	3.0		3.0	ns	2-7
		5.0	0	3.0		3.0		
t_H	Hold Time, HIGH or LOW D_n to LE	3.3	0	1.5		1.5	ns	2-7
		5.0	0	1.5		1.5		
t_W	LE Pulse Width, HIGH	3.3	2.0	4.0		4.0	ns	2-3
		5.0	2.0	4.0		4.0		

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3V is 3.3 ±0.3V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	5.0	2.0	6.0	8.0			2.0	8.5	ns	2-3, 4
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	7.0	9.0			2.5	9.5	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.0	9.0			2.0	9.5	ns	2-5, 6
t_{PHZ}, t_{PHL}	Output Disable Time	5.0	1.0	8.0	10.0			1.0	10.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to LE	5.0	0	3.0		3.0	ns	2-7
t_H	Hold Time, HIGH or LOW D_n to LE	5.0	0	1.5		1.5	ns	2-7
t_W	LE Pulse Width, HIGH	5.0	2.0	4.0		4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	42	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACQ/74ACQ564 • 54ACTQ/74ACTQ564 Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

General Description

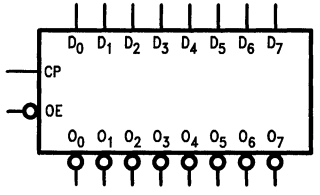
The 'ACTQ564 is a high speed octal D-type flip-flop with buffered common clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the low-to-high clock (CP) transition. The 'ACQ/'ACTQ564 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with μP's
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'ACT564
- 4 kV minimum ESD immunity

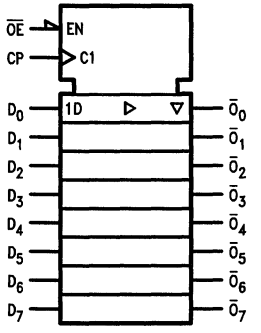
Ordering Code: See Section 8

Logic Symbols



TL/F/10632–1

IEEE/IEC



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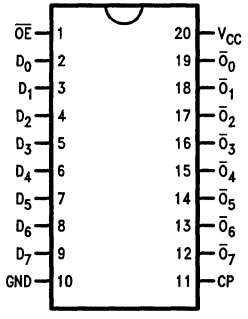
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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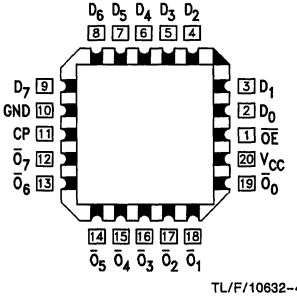
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

Pin Assignment for LCC and PCC



TL/F/10632–4

Functional Description

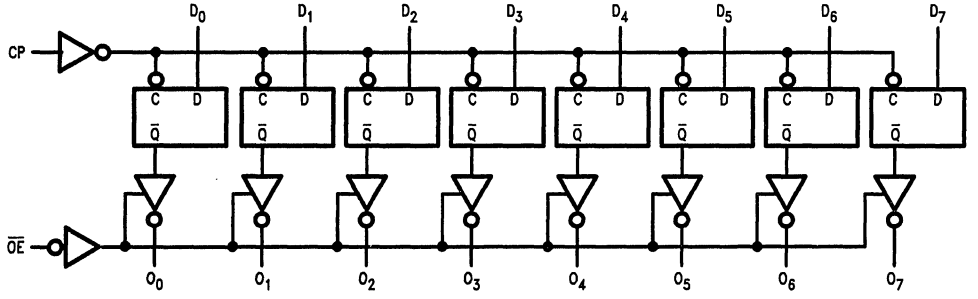
The 'ACQ/'ACTQ564 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	H	Z	Load
H	⌐	H	L	Z	Load
L	⌐	L	H	H	Data Available
L	⌐	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C		54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND (Note 1)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1* and *2* (Notes 2 and 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1* and *2* (Notes 2 and 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2 and 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2 and 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: *Max number of outputs defined as (n).* Data inputs are driven 0V to 5V. One output @ GND

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50$ μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	$I_{OUT} = 50$ μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5			V	*Figures 1* and *2* (Notes 2 and 3)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2			V	*Figures 1* and *2* (Notes 2 and 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2 and 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2 and 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
f_{max}	Maximum Clock Frequency	3.3 5.0	75 90					70 85		MHz	
t_{PLH}, t_{PHL}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-3, 4
t_{PZH}, t_{PZL}	Output Enable Time	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-5, 6
t_{PHZ}, t_{PHL}	Output Disable Time	3.3 5.0	1.0 1.0	9.5 8.0	14.5 9.5			1.0 1.0	15.0 10.0	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to $\overline{O}_n$	3.3 5.0		1.5 0.5	1.0 1.0				1.5 1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

Voltage Range 3.3 is 3.3V ±0.3V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF		54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	0 0	3.0 3.0		3.0 3.0	ns	2-7
t_H	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0	1.5 1.5		1.5 1.5	ns	2-7
t_W	LE Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	4.0 4.0		4.0 4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V.
Voltage Range 3.3 is 3.3V ±0.3V.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85					80		MHz	
t_{PLH}, t_{PHL}	Propagation Delay CP to $\overline{O}_n$	5.0	2.0	7.0	9.0			2.0	9.5	ns	2-3, 4
t_{PZH}, t_{PZL}	Output Enable Time	5.0	2.0	7.0	9.0			2.0	9.5	ns	2-5, 6
t_{PHZ}, t_{PHL}	Output Disable Time	5.0	1.0	8.0	10.0			1.0	10.5	ns	2-5, 6
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to $\overline{O_n}$	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to CP	5.0	0	3.0		3.0	ns	2-7
t_H	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5		1.5	ns	2-7
t_W	LE Pulse Width, HIGH or LOW	5.0	2.0	4.0		4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACQ/74ACQ573 • 54ACTQ/74ACTQ573
Quiet Series Octal Latch with TRI-STATE® Outputs

General Description

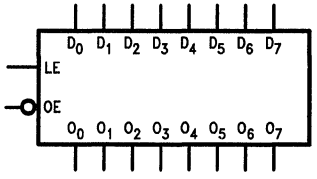
The 'ACQ/'ACTQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The 'ACQ/'ACTQ573 is functionally identical to the 'ACQ/'ACTQ373 but with inputs and outputs on opposite sides of the package. The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching raise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Outputs source/sink 24 mA
- Faster prop delays than standard 'ACT573
- 4 kV minimum ESD immunity

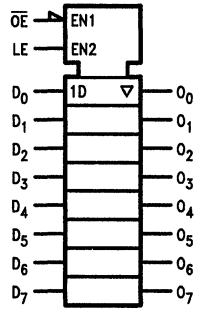
Ordering Code: See Section 8

Logic Symbols



TL/F/10633–1

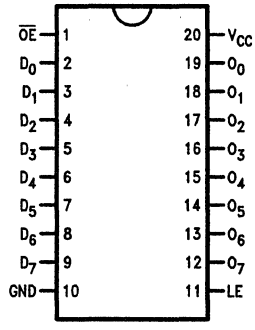
IEEE/IEC



TL/F/10633–2

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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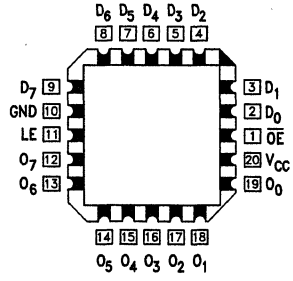
Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

Pin Assignment for LCC



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Functional Description

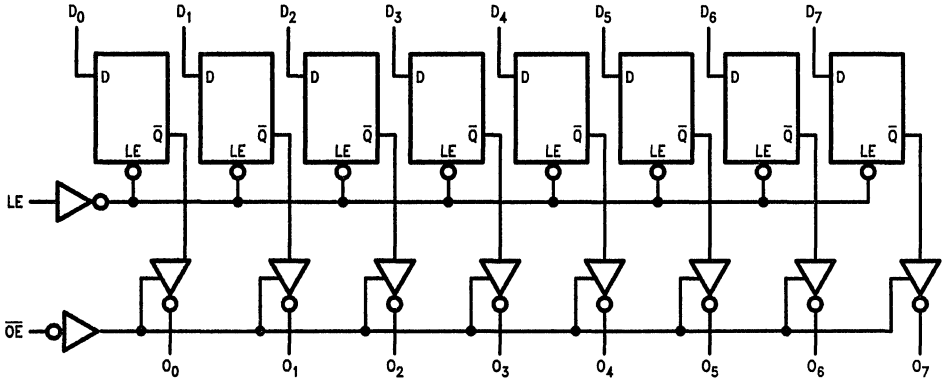
The 'ACQ/'ACTQ573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latchup Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C		54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND (Note 1)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65\ V_{Max}$
I_{OHD}		5.5			−50	−75	mA	$V_{OHD} = 3.85\ V_{Min}$
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Curent	5.5		±0.5	±11.0	±5.0	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Note 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50\ \mu A$
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	$I_{OUT} = 50\ \mu A$
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n − 1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF Min	Typ	Max	54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Min	Max	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Min	Max	Units	Fig. No.
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	3.3	2.5	8.5	10.5			2.5	11.0	ns	2-3, 4
		5.0	1.5	5.5	7.0			1.5	7.5		
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	3.3	2.5	8.5	12.0			2.5	12.5	ns	2-3, 4
		5.0	2.0	6.0	8.0			2.0	8.5		
t_{PZL}, t_{PZH}	Output Enable Time	3.3	2.5	8.5	13.0			2.5	13.5	ns	2-5, 6
		5.0	1.5	6.0	8.5			1.5	9.0		
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3	1.0	9.0	14.5			1.0	15.0	ns	2-5, 6
		5.0	1.0	6.0	9.5			1.0	10.0		
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	3.3		1.0	1.5				1.5	ns	
		5.0		0.5	1.0				1.0		

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL} or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF		54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	0 0	3.0 3.0		3.0 3.0	ns	2-7
t_H	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0	1.5 1.5		1.5 1.5	ns	2-7
t_W	LE Pulse Width, HIGH	3.3 5.0	2.0 2.0	4.0 4.0		4.0 4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	5.0	2.0	6.5	7.5			2.0	8.0	ns	2-3, 4
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	7.0	8.5			2.5	9.0	ns	2-3, 4
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.0	9.0			2.0	9.5	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0			1.0	10.5	ns	2-5, 6
t_{OSHL} t_{OSLH}	Output to Output Skew** D_n to O_n	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL} or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to LE	5.0	0	3.0		3.0	ns	2-7
t_H	Hold Time, HIGH or LOW D_n to LE	5.0	0	1.5		1.5	ns	2-7
t_W	LE Pulse Width, HIGH	5.0	2.0	4.0		4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	42.0	pF	$V_{CC} = 5.0V$

National Semiconductor

54ACQ/74ACQ574 • 54ACTQ/74ACTQ574 Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ574 is a high-speed, low-power octal D-type flip-flop with a buffered Common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH clock (OP) transition.

'ACQ/'ACTQ574 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

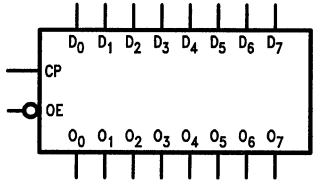
The 'ACQ/'ACTQ574 is functionally identical to the 'ACTQ374 but with different pin-out.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of the package allowing easy interface with microprocessors
- Functionally identical to the 'ACQ/ACTQ374
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT574
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

Logic Symbols



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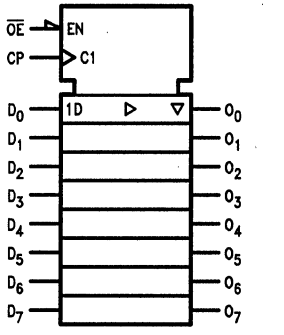
IEEE/IEC



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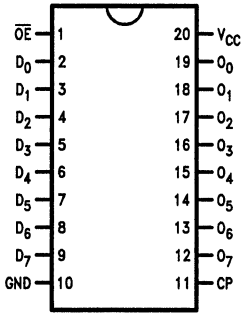
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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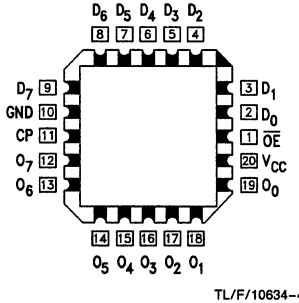
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

Pin Assignment for LCC and PCC



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Functional Description

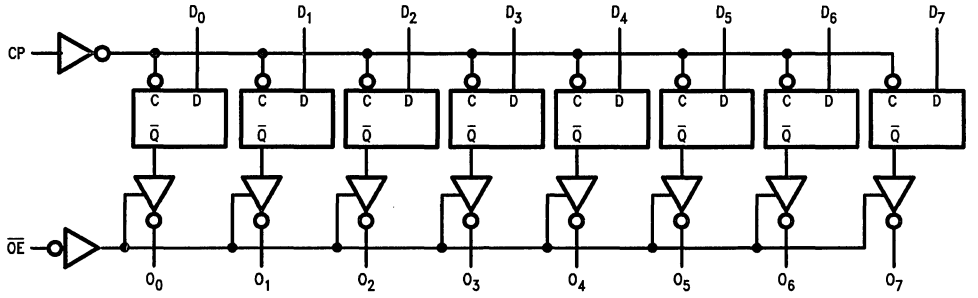
The 'ACQ/'ACTQ574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	L	Z	Load
H	⌐	H	H	Z	Load
L	⌐	L	L	L	Data Available
L	⌐	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Electrical Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C		54ACQ T_A = −55°C to +125°C	74ACQ T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15	3.15		
		5.5	2.75	3.85	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35	1.35		
		5.5	2.75	1.65	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4	4.4		
		5.5	5.49	5.4	5.4	5.4		
		3.0		2.56	2.4	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7	3.76		I_{OH} −24 mA
		5.5		4.86	4.7	4.76		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1	0.1		
		5.5	0.001	0.1	0.1	0.1		
		3.0		0.36	0.50	0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA
		4.5		0.36	0.50	0.44		I_{OL} 24 mA
		5.5		0.36	0.50	0.44		24 mA

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

DC Electrical Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$		54ACQ $T_A = -55°C$ to $+125°C$	74ACQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND (Note 1)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I(OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 1, 2* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Maximum number of data inputs (n) switching. (n−1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). f = 1 MHz.

DC Electrical Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.85 4.86	3.70 4.70	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±10.0	±5.0	μA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	†Maximum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	160.0	80.0	μA	V_{IN} = V_{CC} or GND (Note 1)
V_{OLP}	Maximum High Level Output Noise	5.0	1.1	1.5			V	*Figures 1, 2* (Notes 2, 3)
V_{OLV}	Maximum Low Level Output Noise	5.0	−0.6	−1.2			V	*Figures 1*, 2 (Notes 2, 3)
V_{IHD}	Maximum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n−1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF			54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	75 90					70 85		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	3.0 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-3,4
t_{PZH} t_{PZL}	Output Enable Time	3.3 5.0	3.0 2.0	9.5 6.5	13.0 8.5			3.0 2.0	13.5 9.0	ns	2-5,6
t_{PHZ} t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	9.5 8.0	14.5 9.5			1.0 1.0	15.0 10.0	ns	2-5,6
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to $\overline{O}_n$	3.3 5.0		1.0 0.5	1.5 1.0				1.5 1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$, $C_L = 50$ pF		54ACQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	0 0	3.0 3.0		3.0 3.0	ns	2-7
t_H	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0	1.5 1.5		1.5 1.5	ns	2-7
t_W	LE Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	4.0 4.0		4.0 4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85					80		MHz	
t_{PLH}, t_{PHL}	Propagation Delay CP to $\overline{O}_n$	5.0	2.0	7.0	9.0			2.0	9.5	ns	2-3, 4
t_{PZH}, t_{PZL}	Output Enable Time	5.0	20	7.0	9.0			2.0	9.5	ns	2-5, 6
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0			1.0	10.5	ns	2-7
t_{OSHL}, t_{OSLH}	Output to Output Skew** CP to $\overline{O}_n$	5.0		0.5	1.0				1.0	ns	

*Voltage Range 5.0 is 5.0V ±0.5V.

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$, $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_S	Setup Time, HIGH or LOW D_n to CP	5.0	0	3.0		3.0	ns	2-7
t_H	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5		1.5	ns	2-7
t_W	LE Pulse Width, HIGH or LOW	5.0	2.0	4.0		4.0	ns	2-3

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.0V$

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ADVANCE INFORMATION

54ACQ/74ACQ646 • 54ACTQ/74ACTQ646 Quiet Series Octal Transceiver/Register with TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA).

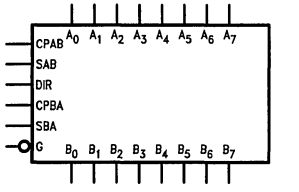
The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Independent registers for A and B busses
- Multiplexed real-time and stored data transfers
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT646
- 4 kV minimum ESD immunity

The information on the ACQ646 is Advanced Information only.

Logic Symbols



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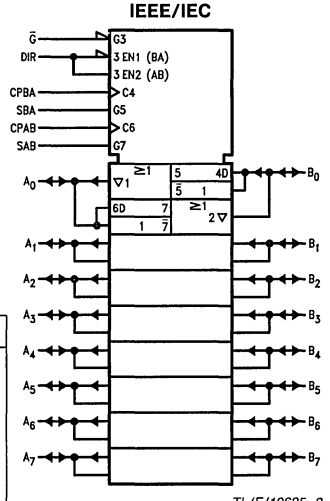

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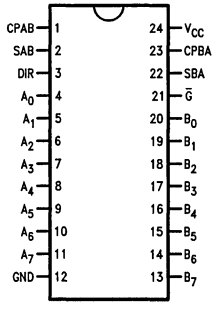
Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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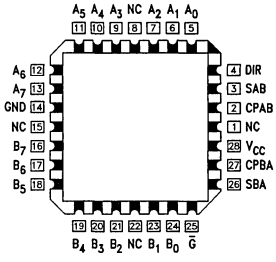
Pin Assignment for LCC and PCC



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ADVANCE INFORMATION

54ACQ/74ACQ657 • 54ACTQ/74ACTQ657 Quiet Series Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

General Description

The 'ACQ/'ACTQ657 contains eight non-inverting buffers with TRI-STATE outputs and an 8-bit parity generator/checker. Intended for bus oriented applications, the device combines the '245 and the '280 functions in one package.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

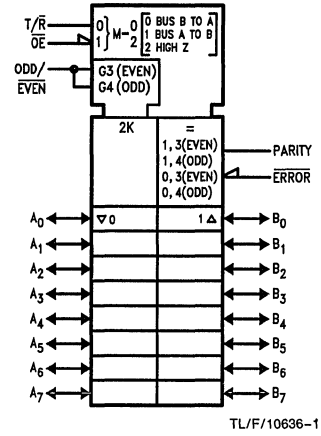
The Information on the ACQ657 is Advanced Information only.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Combines the '245 and the '280 functions in one package
- 300 mil 24-pin slim dual-in-line package
- Outputs source/sink 24 mA
- 4 kV minimum ESD immunity

Logic Symbols

IEEE/IEC



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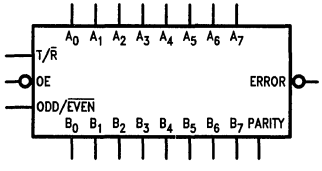

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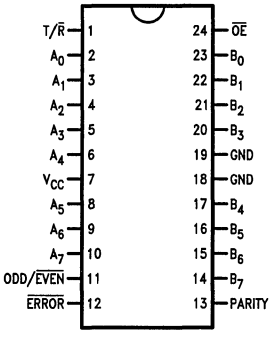
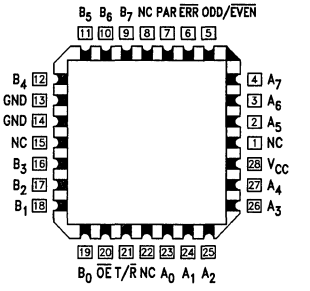
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/10636-2

Pin Assignment for LCC and PLCC



TL/F/10636-3

Pin Names	Description
A_0–A_7	Data Inputs/TRI-STATE Outputs
B_0–B_7	Data Inputs/TRI-STATE Outputs
T/$\overline{R}$	Transmit/Receive Input
$\overline{OE}$	Enable Input
PARITY	Parity Input/TRI-STATE Output
ODD/$\overline{EVEN}$	ODD/$\overline{EVEN}$ Parity Input
$\overline{ERROR}$	Error Output

National Semiconductor

ADVANCE INFORMATION

54ACQ/74ACQ821
Quiet Series 10-Bit D Flip-Flop with TRI-STATE® Outputs

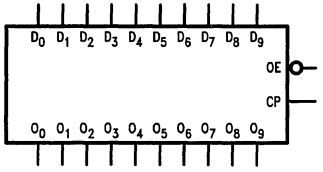
General Description

The 'ACQ821 is a 10-bit D flip-flop with non-inverting TRI-STATE outputs arranged in a broadside pinout. The ACQ821 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

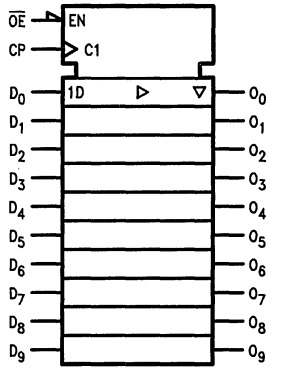
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Non-inverting TRI-STATE outputs for bus interfacing
- 4 kV minimum ESD immunity
- Outputs source/sink 24 mA
- Functionally identical to the AM29821

Logic Symbols



TL/F/10686–1

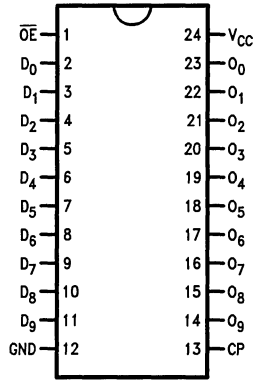
IEEE/IEC



TL/F/10686–2

Connection Diagrams

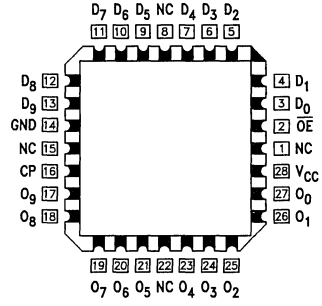
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10686–3

Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	Data Outputs
$\overline{OE}$	Output Enable Input
CP	Clock Input

Pin Assignment for LCC



TL/F/10686–4

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National Semiconductor

ADVANCE INFORMATION

54ACTQ/74ACTQ827 Quiet Series 10-Bit Buffer/Line Driver with TRI-STATE® Outputs

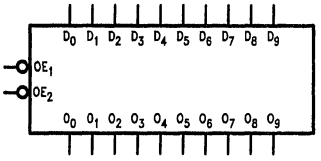
General Description

The 'ACTQ827 10-bit bus buffer provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility. The 'ACTQ827 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ feature GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- Functionally and pin-compatible to AMD's AM29827
- 'ACTQ827 has TTL-compatible inputs
- 4 kV minimum ESD immunity

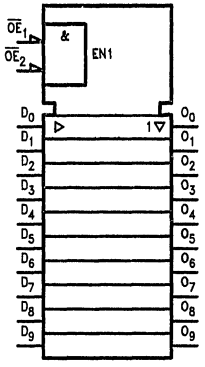
Logic Symbols



TL/F/10687–1

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs

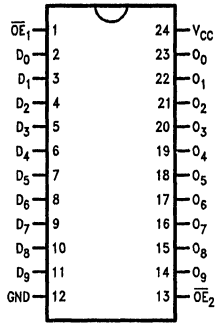
IEEE/IEC



TL/F/10687–2

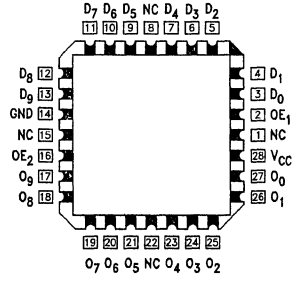
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10687–3

Pin Assignment for LCC



TL/F/10687–4

National Semiconductor

ADVANCE INFORMATION

54ACTQ/74ACTQ841 Quiet Series 10-Bit Transparent Latch with TRI-STATE® Outputs

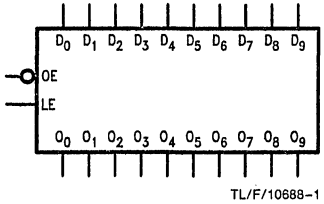
General Description

The 'ACTQ841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The '841 is a 10-bit transparent latch, a 10-bit version of the '373. The 'ACTQ841 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance, FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

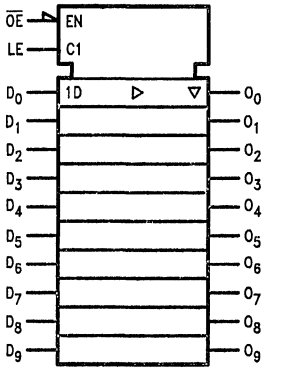
Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- 'ACTQ841 has TTL-compatible inputs
- 4 kV minimum ESD immunity

Logic Symbols



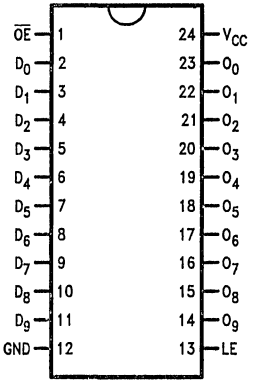
TL/F/10688–1



TL/F/10688–2

Connection Diagrams

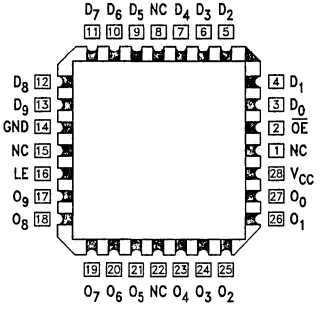
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10688–3

Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	TRI-STATE Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable

Pin Assignment for LCC



TL/F/10688–4

National Semiconductor

ADVANCE INFORMATION

54ACTQ/74ACTQ843
Quiet Series 8-Bit Transparent Latch

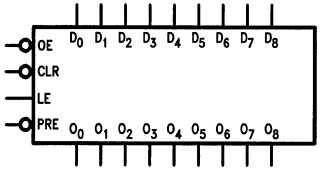
General Description

The 'ACTQ843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths. The 'ACTQ843 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

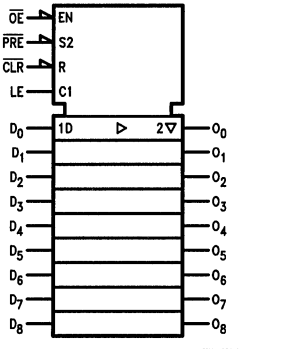
Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on oppostie sides of package for easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- 'ACTQ843 has TTL-compatible inputs
- Functionally and pin-compatible to AMD's AM29843
- 4 kV minimum ESD immunity
- 'ACT843 has TTL-compatible inputs
- TRI-STATE® outputs for bus interfacing

Logic Symbols



TL/F/10689–1

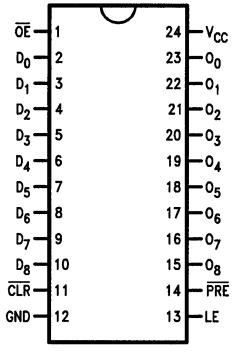


TL/F/10689–4

Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

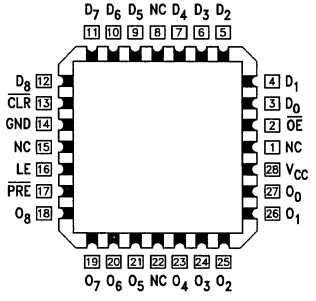
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10689–2

Pin Assignment for LCC



TL/F/10689–3

Section 6

FCT Series Datasheets

Section 6 Contents

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT138
1-of-8 Decoder/Demultiplexer

General Description

The 'FCT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'FCT138 devices or a 1-of-32 decoder using four 'FCT138 devices and one inverter.

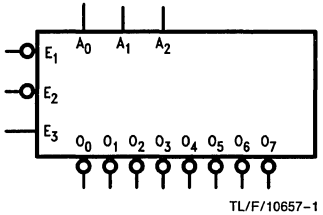
FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

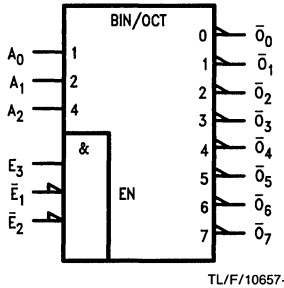
- NSC 54FCT/74FCT138 is pin and functionally equivalent to IDT 54FCT/74FCT138
- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military Product compliant to MIL-STD 883 and Standard Military Drawing #5962-87654

Logic Symbol



TL/F/10657–1

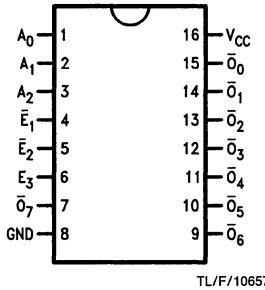
IEEE/IEC



TL/F/10657–4

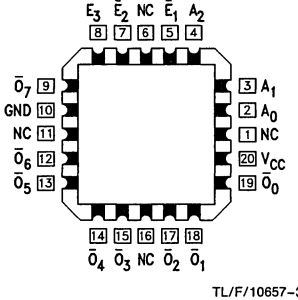
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10657–2

Pin Assignment for LCC



TL/F/10657–3

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

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National Semiconductor

54FCT/74FCT240
Inverting Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'FCT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

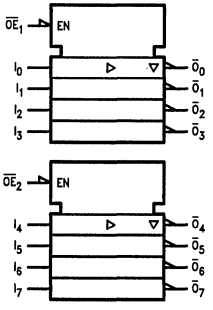
Features

- NSC 54FCT/74FCT240 is pin and functionally equivalent to IDT 54FCT/74FCT240
- Inverting TRI-STATE outputs
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (commercial), 48 mA (military)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883 and standard military drawing #5962-87655

Ordering Code: See Section 8

Logic Symbol

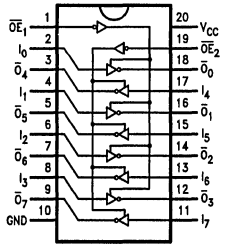
IEEE/IEC



TL/F/10239–1

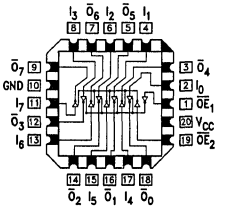
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10239–2

Pin Assignment for LCC



TL/F/10239–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Table

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}1$	I	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}2$	I	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 74FCT: −0.5V to 7.0V
- 54FCT: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.55	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	5.0	mA	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND f_i = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	5.0	1.5	8.0	1.5	9.0	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	7.0	1.5	10.0	1.5	10.5	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	9.5	1.5	12.5	ns	2-11

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f = 1.0 MHz

Symbol	Parameter (Note)	Typ	Max	Units	Condition
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.
C_{OUT} for 74FCT only.

National Semiconductor

54FCT/74FCT241
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'FCT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

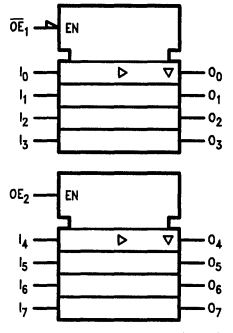
Features

- NSC 54FCT/74FCT241 is pin and functionally equivalent to IDT 54FCT/74FCT241
- Non-inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (Com), 48 mA (Mil)
- CMOS power levels
- ESD immunity ≥4 kV typical
- Military product compliant to MIL-STD 883

Ordering Code: See Section 8

Logic Symbol

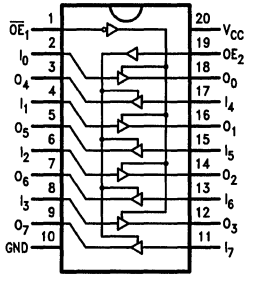
IEEE/IEC



TL/F/10659–1

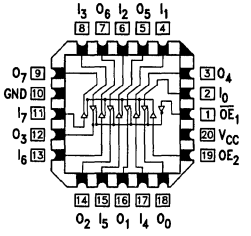
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10659–2

Pin Assignment for LCC



TL/F/10659–3

Pin Names	Description
$\overline{OE}_1$,	TRI-STATE Output Enable Input
OE_2	TRI-STATE Output Enable Input (Active HIGH)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE_2	I	
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 74FCT: −0.5V to 7.0V
- 54FCT: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditons shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq$ 0.2V f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditons shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.55	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	5.5	mA	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0		f_i = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	9.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.
Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	4.0	1.5	6.5	1.5	9.0	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	8.0	1.5	12.5	ns	2-10
t_{PHZ} t_{PLZ}	Output Disable Time	4.5	1.5	7.0	1.5	11.5	ns	2-10

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.

C_{OUT} for 74FCT only.

National Semiconductor

54FCT/74FCT244
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'FCT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

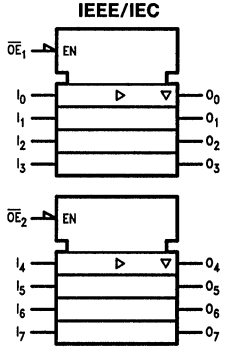
FACT FCT and GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT244 is pin and functionally equivalent to IDT 54FCT/74FCT244
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (commercial) and 48 mA (military)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883C and standard military drawing #5962-87630

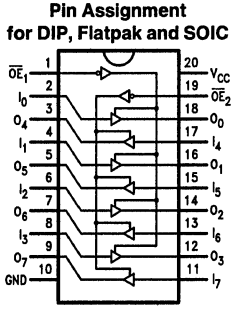
Ordering Code: See Section 8

Logic Symbol

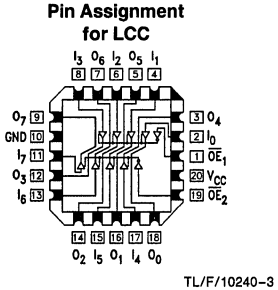


TL/F/10240–1

Connection Diagrams



TL/F/10240–2



TL/F/10240–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to 7.0V
- 74FCT: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditons shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_D = V_{CC}$ V_D = 2.7V (Note 2) V_D = 0.5V (Note 2) V_D = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditons shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.55	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_1$ = $\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	5.5	mA	V_{CC} = Max Outputs Open $\overline{OE}_1$ = $\overline{OE}_2$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0		f_i = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	9.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}_1$ = $\overline{OE}_2$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.
Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	4.5	1.5	6.5	1.5	9.0	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	6.0	1.5	8.0	1.5	10.5	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	5.0	1.5	7.0	1.5	12.5	ns	2-11

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.
C_{OUT} for 74FCT only.

National Semiconductor

54FCT/74FCT245
Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

The 'FCT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

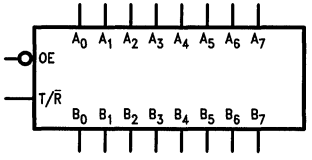
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC54FCT/74FCT245 is pin and functionally equivalent to IDT54FCT/74FCT245
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity.
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (commercial) and 48 mA (military)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883 and Standard Military Drawing #5962-87629

Ordering Code: See Section 8

Logic Symbols



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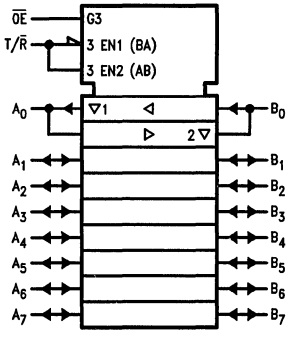
Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A TRI-STATE Inputs or TRI-STATE Outputs
B_0–B_7	Side B TRI-STATE Inputs or TRI-STATE Outputs

IEEE/IEC



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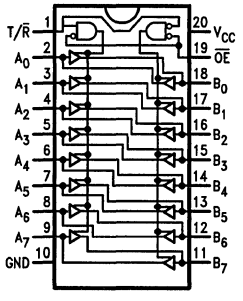
Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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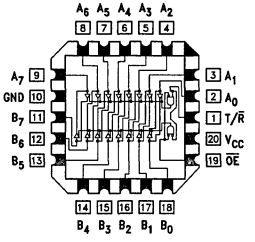
Pin Assignment for LCC and PCC



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to 7.0V
- 74FCT: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current (except I/O Pins)			5.0 5.0	µA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IH}	Input High Current (I/O Pins Only)			15 15	µA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current (except I/O Pins)			−5.0 −5.0	µA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{IL}	Input Low Current (I/O Pins Only)			−15 −15	µA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	µA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2) V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 µA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 µA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 µA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 µA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_i = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_A = \overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $T/\overline{R} = \overline{OE}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0		f_i = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	10.0		(Note 5) V_{CC} = Max Outputs Open $T/\overline{R} = \overline{OE}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.
Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	5.0	1.5	7.0	1.5	7.5	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B	6.0	1.5	9.5	1.5	10.0	ns	2-8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to A or B	6.0	1.5	7.5	1.5	10.0	ns	2-11
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B	6.0	1.5	9.5	1.5	10.0	ns	2-11
t_{PHZ} t_{PLZ}	Output Enable Time T/$\overline{R}$ to A or B	6.0	1.5	7.5	1.5	10.0	ns	2-11

Note: Minimum limits guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f = 1.0 MHz

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.
C_{OUT} for 74FCT245 only.

National Semiconductor

54FCT/74FCT273
Octal D Flip-Flop

General Description

The 'FCT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

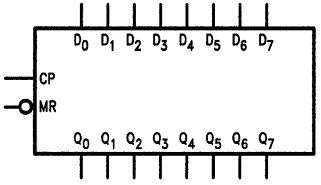
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Features

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- TTL input and output level compatible
- TTL levels accept CMOS levels
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- NSC 54/74FCT273 is pin and functionally equivalent to IDT 54/74FCT273

Ordering Code: See Section 8

Logic Symbols



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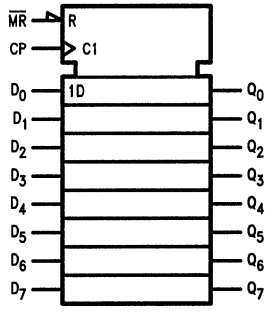
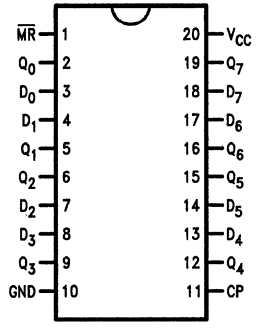
IEEE/IEC



TL/F/10146–2

Connection Diagrams

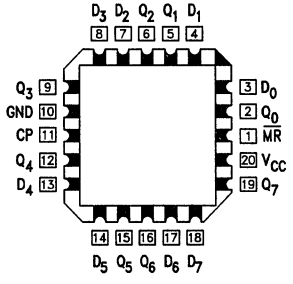
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10146–3

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

Pin Assignment for LCC



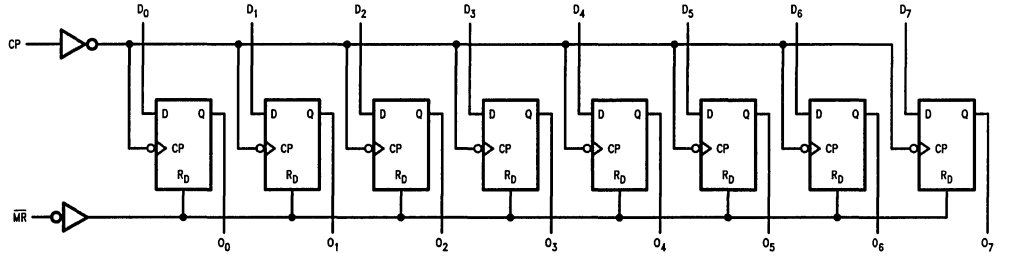
TL/F/10146–4

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5 to +7.0V
- 74FCT: −0.5 to +7.0V

Temperature Under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75 to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCT/74FCT			Units	Conditions	
		Min	Typ	Max			
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min	I_{OL} = 300 μA
			0.3	0.5		$V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 48 mA (Mil)
			0.3	0.5			I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} Max Outputs Open $\overline{MR} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$ $V_{IN} \leq 0.2V$
V_H	Input Hysteresis on Clock Only		200		mV		
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open $\overline{MR} = V_{CC}$	$V_{IN} \geq V_{CC}$ $V_{IN} \leq 0.2V$
			1.8	6.0		f_I = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{MR} = V_{CC}$	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8		f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Curent for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$			
		Typ	Min	Max	Min	Max		
t_{PHL} t_{PLH}	Propagation Delay Clock to Output	7.0	2.0	13.0			ns	2-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	8.0	2.0	13.0			ns	2-8
t_{SU}	Setup Time HIGH or LOW Data to CP	3.0	3.0				ns	2-10
t_h	Hold Time HIGH or LOW Data to CP	1.0	2.0				ns	2-10
t_w	Clock Pulse Width HIGH or LOW	4.0	7.0				ns	2-9
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	4.0	7.0				ns	2-9
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.0	4.0				ns	2-10

Note 1: Minimum limits are guaranteed but not tested on Propagation Delays.

Capacitance $T_A = 25°C, f = 1.0\ MHz$

Symbol	Parameter	Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

Note: This parameter is guaranteed by characterization data and not tested.

National Semiconductor

54FCT/74FCT373
Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'FCT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

FACT FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

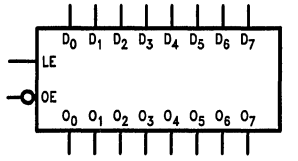
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT373 is pin and functionally equivalent to IDT 54FCT/74FCT373
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (commercial) and 32 mA (military)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883 and standard military drawing #5962-87644

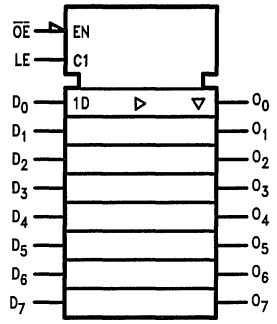
Ordering Code: See Section 8

Logic Symbols



TL/F/10242-1

IEEE/IEC

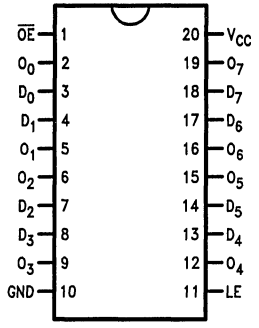


TL/F/10242-2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

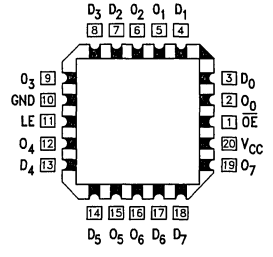
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10242-3

Pin Assignment for LCC



TL/F/10242-4

Functional Description

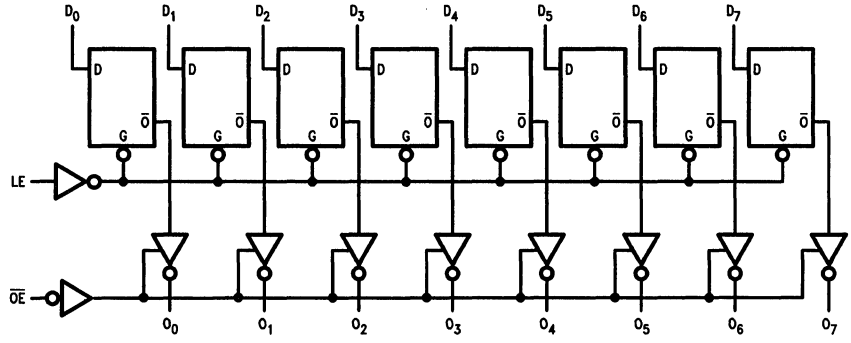
The 'FCT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_n

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_n = Previous O_n before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/10242–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to +7.0V
- 74FCT: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	V_O = V_{CC} V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.50 0.50		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 μA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq$ 0.2V f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V (Continued)

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.45	mA/MHz	V_{CC} = Max Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)	1.5		4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} f_i = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$ V_{IN} = 3.4V V_{IN} = GND
		1.8		5.0			
		3.0		8.0		(Note 5) V_{CC} = Max $\overline{OE}$ = GND LE = V_{CC} f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$ V_{IN} = 3.4V V_{IN} = GND
		5.0		14.5			
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duratioin not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	5.0	1.5	8.0	1.5	8.5	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	7.0	1.5	12.0	1.5	13.5	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	7.5	1.5	10.0	ns	2-11
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	9.0	2.0	13.0	2.0	15.0	ns	2-8
t_{SU}	Set Up Time High or Low D_n to LE	1.0	2.0		2.0		ns	2-10
t_H	Hold Time High or Low D_n to LE	1.0	1.5		3.0		ns	2-10
t_W	LE Pulse Width High or Low	5.0	6.0		6.0		ns	2-9

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f = 10 MHz

Symbol	Parameter (Note)	Typ	Max	Units	Condition
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.

C_{OUT} for 74FCT only.

National Semiconductor

54FCT/74FCT374
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

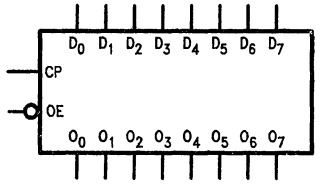
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT374 is pin and functionally equivalent to IDT 54FCT/74FCT374
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (commercial) and 32 mA (military)
- CMOS power levels
- ESD immunity ≥ 4kV typ
- Military product compliant to MIL-STD 883 and standard military drawing #5962-87628

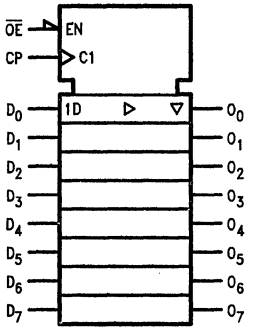
Ordering Code: See Section 8

Logic Symbols



TL/F/10243–1

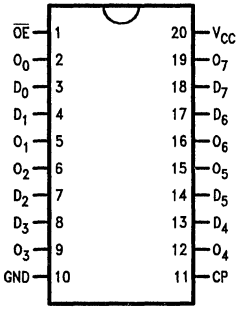
IEEE/IEC



TL/F/10243–2

Connection Diagrams

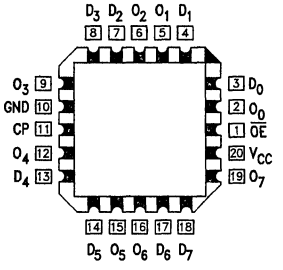
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10243–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Pin Assignment for LCC



TL/F/10243–4

Functional Description

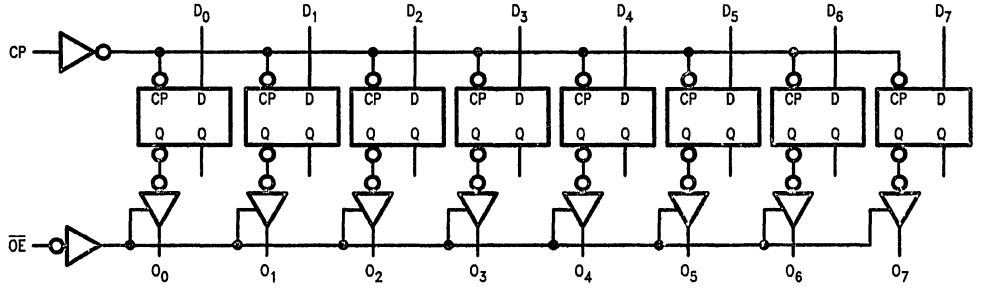
The 'FCT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐‾	L	H
L	⌐‾	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐‾ = LOW-to-HIGH Transition

Logic Diagram



TL/F/10243–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to 7.0V
- 74FCT: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	µA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	µA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	µA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 µA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 µA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 µA	
			GND 0.3 0.3	0.2 0.50 0.50		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 µA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq$ 0.2V f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	V_{CC} = Max Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_i = 5 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_P to O_n	6.6	2.0	10.0	2.0	11.0	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	9.0	1.5	12.5	1.5	14.0	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	8.0	1.5	8.0	ns	2-11
t_{SU}	Set Up Time High or Low D_n to C_P	1.0	2.0		2.5		ns	2-10
t_H	Hold Time High or Low D_n to C_P	0.5	2.0		2.5		ns	2-10
t_w	C_P Pulse Width High or Low	4.0	7.0		7.0		ns	2-9

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance $T_A = +25°C, f = 1.0$ MHz

Symbol	Parameter (Note 1)	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note 1: This parameter is measured at characterization but not tested.

C_{OUT} for 74FCT only.

National Semiconductor

54FCT377/74FCT377
Octal D Flip-Flop with Clock Enable

General Description

The FCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

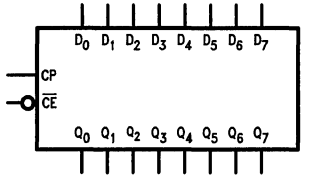
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT377 is pin and functionally equivalent to IDT 54FCT/74FCT377
- Ideal for addressable register applications
- Clock enables for address and data synchronization applications
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883 and Standard Military Drawing # 5962-87627

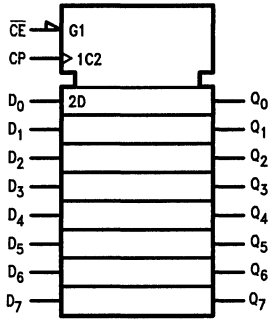
Ordering Code: See Section 8

Logic Symbols



TL/F/10661–1

IEEE/IEC

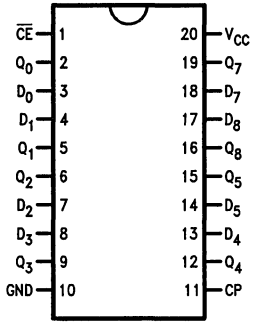


TL/F/10661–2

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

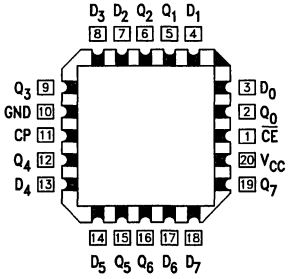
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10661–3

Pin Assignment for LCC



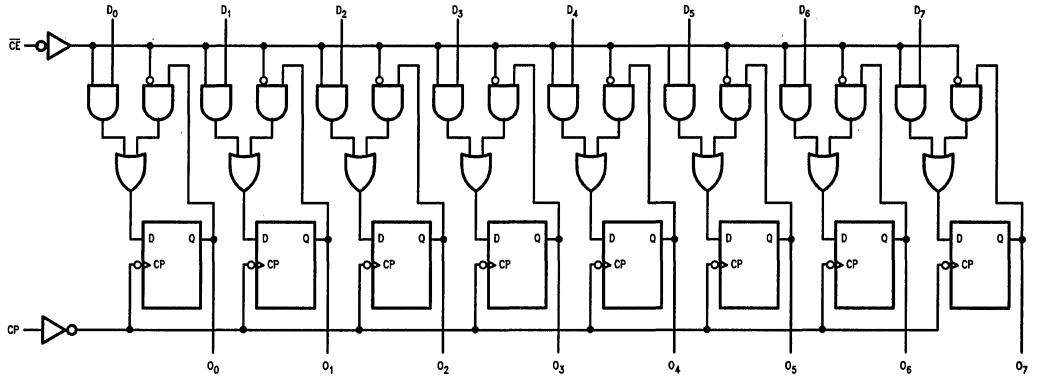
TL/F/10661–4

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load '1'	⌐	L	H	H
Load '0'	⌐	L	L	L
Hold (Do Nothing)	⌐	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



TL/F/10661–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to +7.0V
- 74FCT: −0.5V to +7.0V

Temperature Under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC}	V_{CC}			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA
		2.4	4.3				I_{OH} = −12 mA (Mil)
		2.4	4.3				I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 μA
			0.3	0.5			I_{OL} = 32 mA (Mil)
			0.3	0.5			I_{OL} = 48 mA (Com)

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.30	mA/MHz	V_{CC} = Max Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0		$\overline{CE}$ = GND f_I = 5 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	9.0		(Note 5) V_{CC} = Max Outputs Open f_{CP} = 10 MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8		$\overline{CE}$ = GND f_I = 2.5 MHz Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs HIGH

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.4 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT $T_A = 25°C$ $V_{CC} = 5.0V$	74FCT $T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		54FCT $T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$		Units	Fig. No.
		Typ	Min (Note)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_P to $\overline{O}_n$	7.0	2.0	13.0	2.0	13.0	ns	2-8
t_{SU}	Set Up Time HIGH or LOW D_n to C_P	1.0	2.5		4.0		ns	2-10
t_H	Hold Time HIGH or LOW D_n to C_P	1.0	2.0		2.0		ns	2-10
t_{SU}	Set Up Time HIGH or LOW $\overline{CE}$ to C_P	1.5	4.0		4.5		ns	2-10
t_H	Hold Time HIGH or LOW $\overline{CE}$ to C_P	3.0	1.5		2.0		ns	2-10
t_W	Clock Pulse Width, LOW	4.0	7.0		7.0		ns	2-9

Note: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance $T_A = +25°C$, f = 1.0 MHz

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.
C_{OUT} for 74FCT only.

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT521
8-Bit Identity Comparator

General Description

The 'FCT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

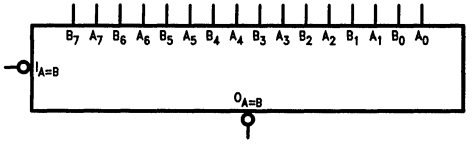
FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

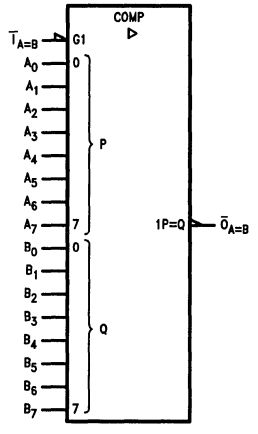
- NSC 54FCT/74FCT521 is pin and functionally equivalent to IDT 54FCT/74FCT521
- Expandable to any word length
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



TL/F/10662-1

IEEE/IEC

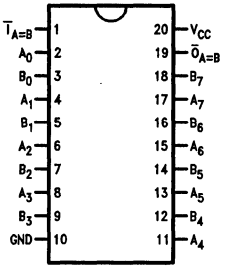


TL/F/10662-4

Pin Names	Description
A_0–A_7	Word A Inputs
B_0–B_7	Word B Inputs
$T_{A=B}$	Expansion or Enable Input
$\overline{O}_{A=B}$	Identity Output

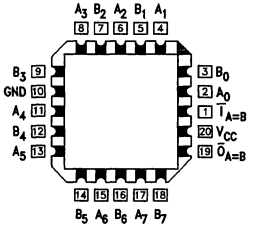
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10662-2

Pin Assignment for LCC



TL/F/10662-3

National Semiconductor

54FCT/74FCT533
Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'FCT533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance. FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance. The 'FCT533 is the same as the 'FCT373, except that the outputs are inverted.

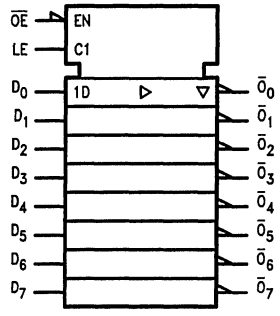
Features

- NSC 54FCT/74FCT533 is pin and functionally equivalent to IDT 54FCT/74FCT533
- TRI-STATE outputs for bus interfacing
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- ESD immunity 4 kV typ
- Military product compliant to MIL-STD 883 and Standard Military Drawing #5962-88651

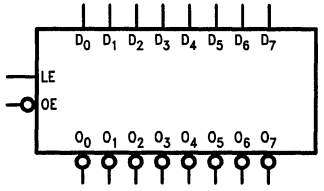
Ordering Code: See Section 8

Logic Symbols

IEEE/IEC



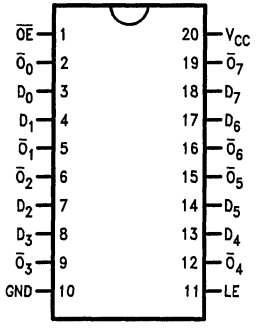
TL/F/10664–1



TL/F/10664–4

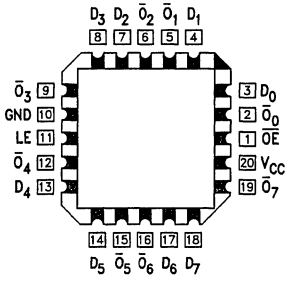
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/10664–2

Pin Assignment for LCC



TL/F/10664–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

Function Table

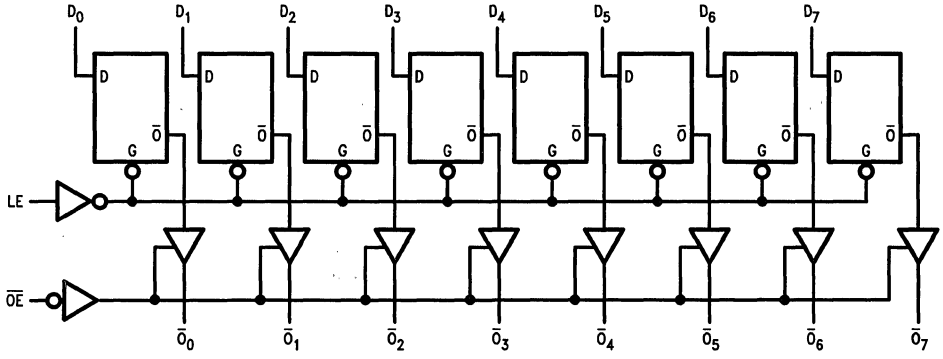
Inputs			Output
LE	$\overline{OE}$	D	$\overline{O}$
H	L	H	L
H	L	L	H
L	L	X	$\overline{O}_n$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Logic(0) or logic(1) must be valid Input Level
O_n = Previous $\overline{O}_n$ before high to low transition of latch enable.

Functional Description

The 'FCT533 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent and the latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW the latch contents are presented inverted at the outupts $\overline{O}_7$–$\overline{O}_0$. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



TL/F/10664–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Voltage with respect to GND (V_{TERM})
- 54FCT: −0.5V to +7.0V
- 74FCT: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C.

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum HIGH Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	V_O = V_{CC} V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_{IN} = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC}	V_{CC}			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA
		2.4	4.3				I_{OH} = −12 mA (Mil)
		2.4	4.3				I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 μA
			0.3	0.50			I_{OL} = 32 mA (Mil)
			0.3	0.50			I_{OL} = 48 mA (Com)

DC Characteristics for FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C. (Continued)

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} f_I = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5			V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on LE Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz. Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0V$	T_A, V_{CC} = Com $R_L = 500\Omega$ $C_L = 50$ pF		T_A, V_{CC} = Mil $R_L = 500\Omega$ $C_L = 50$ pF			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	6.0	1.5	10.0	1.5	8.5	ns	2–8
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	9.0	2.0	13.0	2.0	9.5	ns	2–8
t_{PZH} t_{PZL}	Output Enable Time	8.0	1.5	11.0	1.5	12.5	ns	2–11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	7.0	1.5	8.5	ns	2–11
t_S	Set Up Time High or Low D_n to LE	1.0	2.0		2.0		ns	2–10
t_H	HOLD Time High or Low D_n to LE	1.0	1.5		3.0		ns	2–10
t_W	LE Pulse Width High or Low	5.0	6.0		6.0		ns	2–9

Note 1: Minimum limits are guaranteed but not tested on Propagation Delays

Capacitance ($T_A = +25C, f = 1.0$ MHz)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{in}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{out}	Output Capacitance	8	12	pF	$V_{out} = 0V$

Note: This parameter is measured at characterization but not tested
C_{OUT} for 74FCT only.

National Semiconductor

54FCT/74FCT534
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

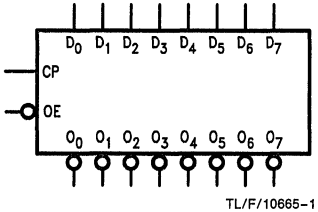
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance. The 'FCT534 is the same as the 'FCT374 except that the outputs are inverted.

Features

- NSC 54/74FCT534 is pin and functionally equivalent to IDT 54/74FCT534
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD-883

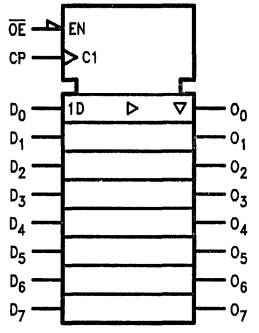
Ordering Code: See Section 8

Logic Symbols



TL/F/10665–1

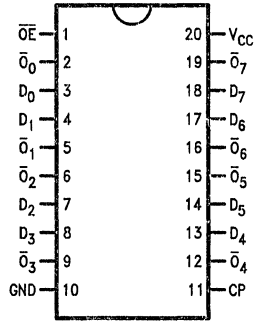
IEEE/IEC



TL/F/10665–2

Connection Diagrams

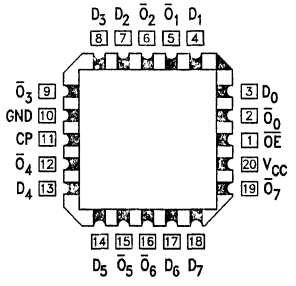
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10665–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

Pin Assignment for LCC

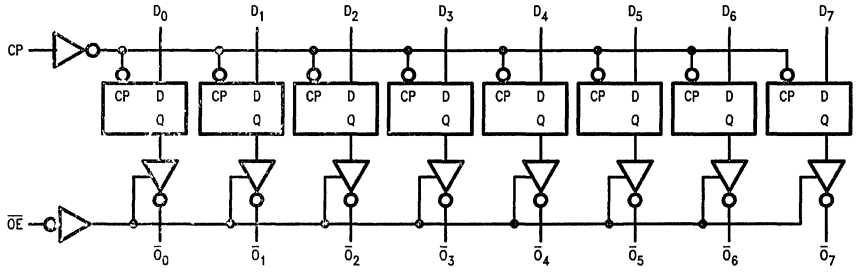


TL/F/10665–4

Functional Description

The 'FCT534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



TL/F/10665–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs			Output
CP	OE	D	$\overline{O}$
⌐⌐	L	H	L
⌐⌐	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐⌐ = LOW-to-HIGH Clock Transition
Z = High Impedance
$\overline{O}_0$ = Value stored from previous clock cycle

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to +7.0V
- 74FCT: −0.5V to +7.0V

Temperature Under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.5 0.5		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_I = 5 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHz f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Numbers of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.
Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Mil C_L = 50 pF		T_A V_{CC} = Com C_L = 50 pF			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_P to $\overline{On}$	6.5	1.5	10.0			ns	2-9
t_{PZH} t_{PZL}	Output Enable Time	9.0	1.5	12.5			ns	2-11
t_{PHZ} t_{PHL}	Output Disable Time	6.0	1.5	8.0			ns	2-11
t_s	Set Up Time High or Low Dn to CP	1.0	2.0				ns	2-10
t_h	Hold Time High or Low Dn to CP	0.5	1.5				ns	2-10
t_w	CP Pulse Width High or Low	4.0	7.0				ns	2-9

Note 1: Minimum limits guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f_I = 1.0 MHz

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.
C_{OUT} for 74FCT only.

National Semiconductor

54FCT540
Inverting Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'FCT540 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

The FACT540 is functionally equivalent to the FCT240 while providing broadside pinout.

The FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features undershoot corrector and a split ground bus for superior performance.

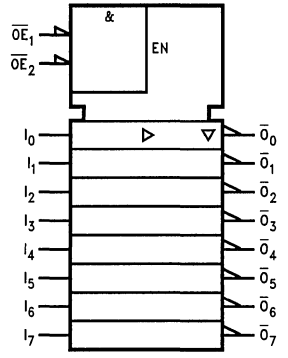
Features

- NSC 54FCT540 is pin and functionally equivalent to IDT 54FCT540
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA
- CMOS power levels
- 2 kV minimum ESD immunity
- Military product compliant to MIL-STD 883 and Standard Military Drawing #5962-89767

Ordering Code: See Section 8

Logic Symbol

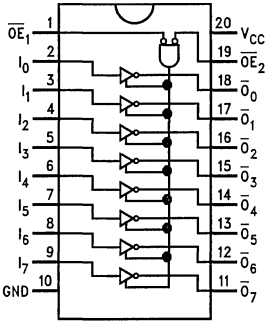
IEEE/IEC



TL/F/10695–1

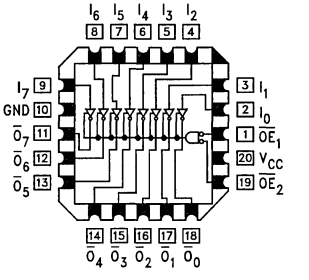
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10695–2

Pin Assignment for LCC



TL/F/10695–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I_n	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
54FCT −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
54FCT −65°C to +135°C

Storage Temperature (T_{STG})
54FCT −65°C to +150°C

Power Dissipation (P_T) 0.5W

DC Output Current (I_{OUT}) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
54FCT 4.5V to 5.5V

Input Voltage 0V to V_{CC}

Output Voltage 0V to V_{CC}

Operating Temperature (T_A)
54FCT −55°C to +125°C

Junction Temperature (T_J)
CDIP 175°C
PDIP 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCT Min	54FCT Typ	54FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8 V_{HC} 2.4 2.4	3.0 V_{CC} 4.3 4.3		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	 I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND GND 0.3 0.3	0.2 0.2 0.55 0.55	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	 I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ $f_I = 0$	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	54FCT			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.35	0.4	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)			5.5	mA	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND f_i = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				6.0			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT $T_A = +25°C$ $V_{CC} = 5.0V$	74FCT $T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		54FCT $T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$		Units	Fig. No.
		Typ	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	5.0			1.5	9.5	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	7.0			1.5	12.5	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0			1.5	9.5	ns	2-11

Capacitance $T_A = +25°C, f = 1.0\ MHz$

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	8	pF	$V_{IN} = 0V$

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT541
Non-Inverting Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'FCT541 is a non-inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

The FCT541 is functionally equivalent to the FCT 241 with the exception of packaging, inputs and outputs are on the opposite side of the package.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features undershoot corrector and split ground bus for superior performance.

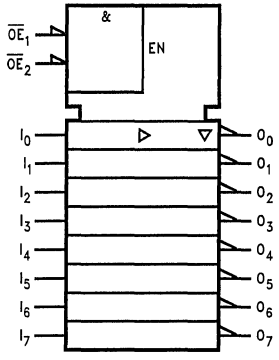
Features

- NSC 54FCT541 is pin and functionally equivalent to IDT 54FCT541
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA
- CMOS power levels
- 2 kV minimum ESD immunity
- Military product compliant to MIL-STD 883 and standard military drawing #5962-89766

Ordering Code: See Section 8

Logic Symbol

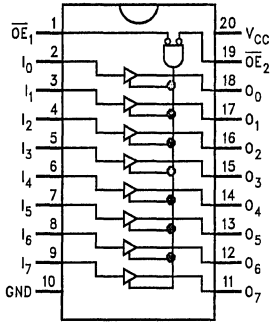
IEEE/IEC



TL/F/10696–1

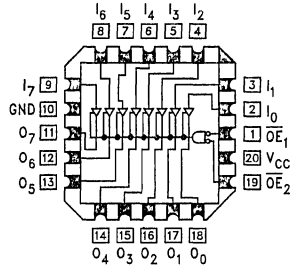
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10696–2

Pin Assignment for LCC



TL/F/10696–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I_n	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
54FCT −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
54FCT −65°C to +135°C

Storage Temperature (T_{STG})
54FCT −65°C to +150°C

Power Dissipation (P_T) 0.5W

DC Output Current (I_{OUT}) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
54FCT 4.5V to 5.5V

Input Voltage 0V to V_{CC}

Output Voltage 0V to V_{CC}

Operating Temperature (T_A)
54FCT −55°C to +125°C

Junction Temperature (T_J)
CDIP 175°C
PDIP 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	54FCT Min	54FCT Typ	54FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	V_O = V_{CC} V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max V_{IN} ≥ V_{HC}, V_{IN} ≤ 0.2V f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	54FCT			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.35	0.40	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)			5.5	mA	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND f_i = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
				6.0			V_{IN} = 3.4V V_{IN} = GND
						(Note 5) V_{CC} = Max $\overline{OE}_A$ = $\overline{OE}_B$ = GND f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
							V_{IN} = 3.4V

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT $T_A = +25°C$ $V_{CC} = 5.0V$	74FCT $T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		54FCT $T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$		Units	Fig. No.
		Typ	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	5.0			1.5	9.0	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	7.0			1.5	12.5	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0			1.5	9.5	ns	2-11

Capacitance $T_A = +25°C, f = 1.0\ MHz$

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	8	pF	$V_{IN} = 0V$

Note: This parameter is measured at characterization but not tested.

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT543
Octal Registered Transceiver

General Description

The 'FCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

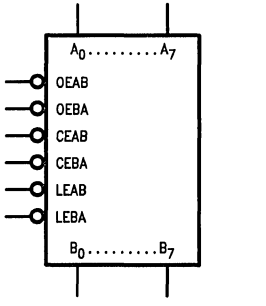
FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

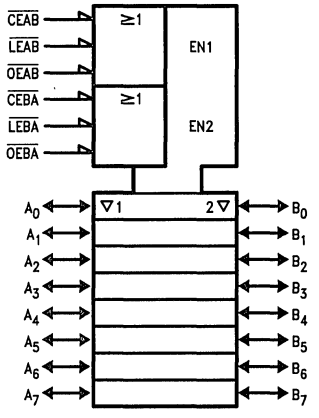
- NSC 54FCT/74FCT543 is pin and functionally equivalent to IDT 54FCT/74FCT543
- Back to back registers for storage
- Separate controls for data flow in each direction
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (com), 48 mA (mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



TL/F/10666–1

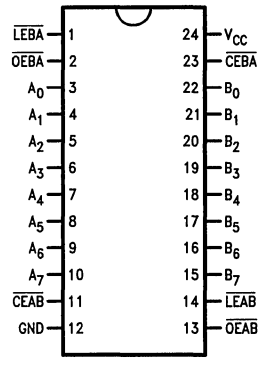
IEEE/IEC



TL/F/10666–2

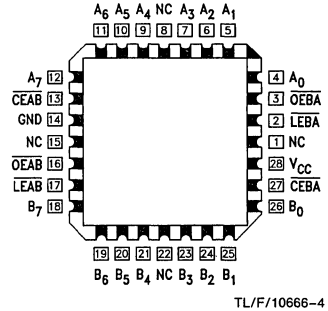
Connection Diagrams

Pin Assignment for DIP and SOIC



TL/F/10666–3

Pin Assignment for LCC



TL/F/10666–4

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT544
Octal Registered Transceiver

General Description

The 'FCT544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The 'FCT544 inverts data in both directions.

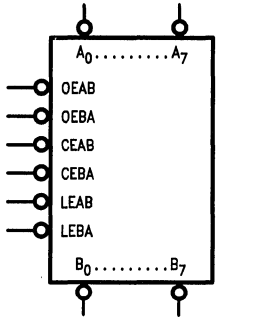
FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

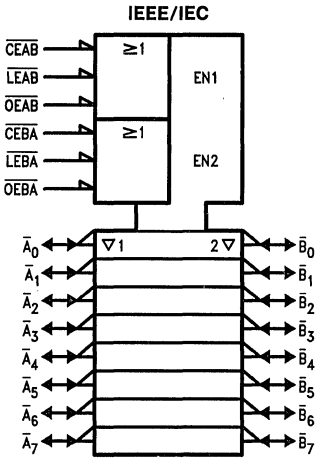
Features

- NSC 54FCT/74FCT544 is pin and functionally equivalent to IDT 54FCT/74FCT544
- Back to back registers for storage
- Separate controls for data flow in each direction
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (com), 48 mA (mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



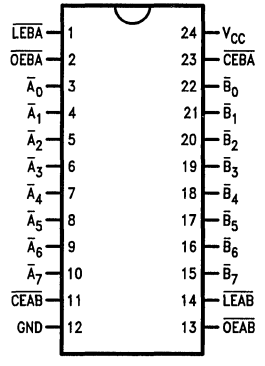
TL/F/10668–1



TL/F/10668–2

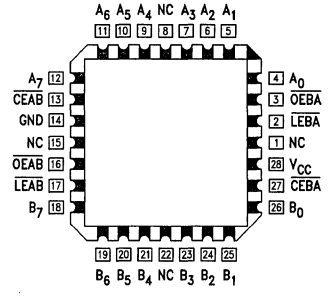
Connection Diagrams

Pin Assignment for DIP and SOIC



TL/F/10668–3

Pin Assignment for LCC



TL/F/10668–4

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
$\overline{A}_0$–$\overline{A}_7$	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
$\overline{B}_0$–$\overline{B}_7$	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

National Semiconductor

54FCT/74FCT563
Octal Latch with TRI-STATE® Outputs

General Description

The 'FCT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

FACT FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

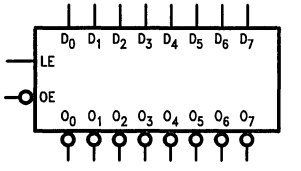
The 'FCT563 device is functionally identical to the 'FCT573, but with inverted outputs.

Features

- Inputs and outputs on opposite side of package allow easy interface with microprocessors
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD-883

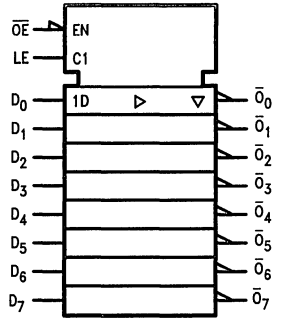
Ordering Code: See Section 8

Logic Symbols



TL/F/10670–1

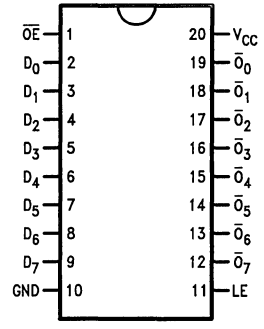
IEEE/IEC



TL/F/10670–2

Connection Diagrams

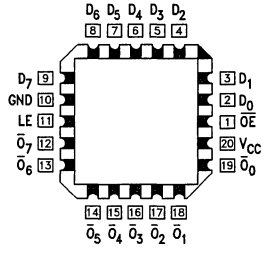
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10670–3

Pin Names	Description
D_0-D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$-$\overline{O}_7$	TRI-STATE Latch Outputs

Pin Assignment for LCC



TL/F/10670–4

Functional Description

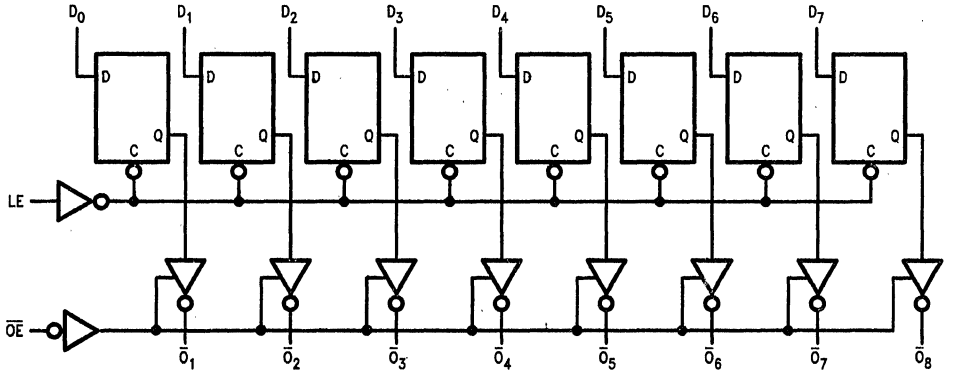
The 'FCT563 contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the TRI-STATE mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs	Function
$\overline{OE}$	LE	D	O	
H	X	X	Z	High-Z
L	H	L	H	Transparent
L	H	H	L	Transparent
L	L	X	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/10670–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to +7.0V
- 74FCT: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0	μA	V_{CC} = Max	$V_I = V_{CC}$
				5.0			V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2)
				−5.0			V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0	μA	V_{CC} = Max	$V_O = V_{CC}$
				10.0			V_O = 2.7V (Note 2)
				−10.0			V_O = 0.5V (Note 2)
				−10.0			V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0			V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC}	V_{CC}		V	V_{CC} = Min; $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA
		2.4	4.3				I_{OH} = −12 mA (Mil)
		2.4	4.3				I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min; $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA
			0.3	0.50			I_{OL} = 32 mA (Mil)
			0.3	0.50			I_{OL} = 48 mA (Com)

DC Characteristics for FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0		LE = V_{CC} f_I = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		LE = V_{CC} f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on LE Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL inputs High
N_T = Number of Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_I = Input Frequency
N_I = Number of Inputs at f_I
All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.
Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		T_A = 25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	5.0	1.5	8.0			ns	2-8
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	9.0	2.0	13.0			ns	2-8
t_{PZL} t_{PZH}	Output Enable Time	7.0	1.5	12.0			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	7.5			ns	2-11
t_S	Set Up Tme High or Low D_n to LE	1.0	2.0	—			ns	2-11
t_H	Hold Time High or Low D_n to LE	1.0	1.5	—			ns	2-10
t_W	LE Pulse Width High or Low	5.0	6.0	—			ns	2-9

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f = 1.0 MHz

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.
C_{OUT} for 74FCT only.

National Semiconductor

54FCT/74FCT564
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

FACT FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

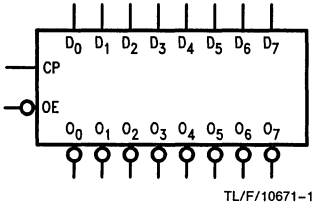
The 'FCT564 device is functionally identical to the 'FCT574, but with inverted outputs.

Features

- NSC 54FCT/74FCT564 is pin and functionally equivalent to IDT 54FCT/74FCT564
- TRI-STATE outputs for bus-oriented applications
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883

Ordering Code: See Section 8

Logic Symbols



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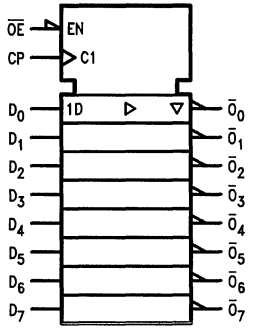
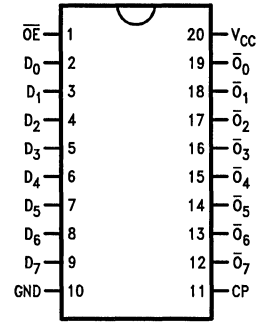
IEEE/IEC



TL/F/10671–2

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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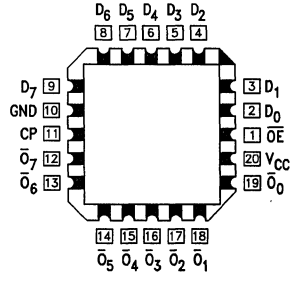
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

Pin Assignment for LCC



TL/F/10671–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with respect to GND (V_{TERM})
- 54FCT: −0.5V to 7.0V
- 74FCT: −0.5 to 7.0V

Temperature Under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} 5.0V ±5%, T_A = 0°C to +70°; Mil: V_{CC} = 5.0V ±10% T_A = 55°C +125°C V_{HC} = V_{CC} −0.2V

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	V_O = V_{CC} V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.50 0.50		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = 300 μA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C +125°C; V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHZ f_I = 5 MHz 50% Duty Cycle One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHz 50% Duty Cycle f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	6.6	2.0	10.0			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	9.0	1.5	12.5			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Timed	6.0	1.5	8.0			ns	2-11
t_S	Set-Up Time High or Low D_n to CP	1.0	2.0	—			ns	2-10
t_H	HOLD Time High or Low D_n to CP	0.5	2.0	—			ns	2-10
t_W	CP Pulse Width High or Low	4.0	7.0	—			ns	2-9

Note: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.
C_{OUT} for 74FCT only.

National Semiconductor

54FCT/74FCT573
Octal Latch with TRI-STATE® Outputs

General Description

The 'FCT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

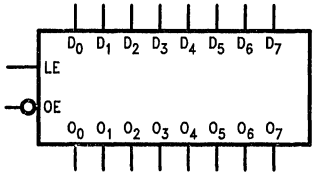
The 'FCT573 is functionally identical to the 'FCT373 but has inputs and outputs on opposite sides.

Features

- NSC 54/74FCT573 is pin and functionally equivalent to IDT 54/74FCT573
- TRI-STATE outputs for bus interfacing
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military Product compliant to MIL-STD-883 and Standard Military Drawing #5962-88639

Ordering Code: See Section 8

Logic Symbols



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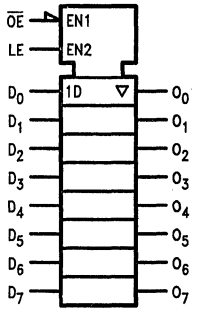
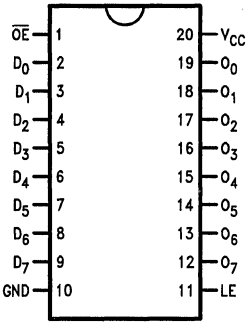
IEEE/IEC



TL/F/10672–2

Connection Diagrams

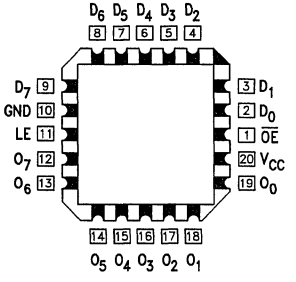
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10672–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

Pin Assignment for LCC



TL/F/10672–4

Functional Description

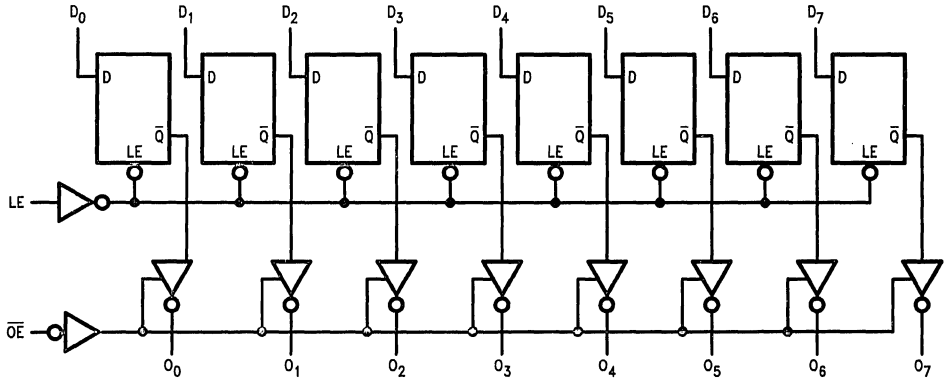
The FCT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, and the latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the latch contents are presented inverted at the outputs $\overline{O}_7$–$\overline{O}_0$. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



TL/F/10672–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to +7.0V
- 74FCT: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 54FCT: −65°C to +135°C
- 74FCT: −55°C to +125°C

Storage Temperature (T_{STG})
- 54FCT: −65°C to +150°C
- 74FCT: −55°C to +125°C

Power Dissipation (P_T): 0.5W

DC Ouput Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC}	V_{CC}			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA
		2.4	4.3				I_{OH} = −12 mA (Mil)
		2.4	4.3				I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA
			0.3	0.50			I_{OL} = 32 mA (Mil)
			0.3	0.50			I_{OL} = 48 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	V_{CC} = Max Outputs Open One Input Toggling 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	74FCT Min	74FCT Typ	74FCT Max	Units	Conditions	
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND, LE = V_{CC} f_{CP} = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND, LE = V_{CC} f_{CP} = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL inputs High
N_T = Number of Inputs at D_H
I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.
Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54/74FCT T_A = +25°C, V_{CC} = 5.0V Typ	74FCT T_A, V_{CC} = Com, R_L = 500Ω, C_L = 50 pF Min (Note)	74FCT Max	54FCT T_A, V_{CC} = Mil, R_L = 500Ω, C_L = 50 pF Min	54FCT Max	Units	Fig. No.
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	5.0	1.5	8.0	1.5	8.5	ns	2-8
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	9.0	2.0	13.0	2.0	15.0	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	7.0	1.5	12.0	1.5	13.5	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	7.5	1.5	10.0	ns	2-11
t_S	Setup Time High or Low, D_n to LE	1.0	2.0		2.0		ns	2-10
t_H	Hold Time High or Low, D_n to LE	1.0	1.5		1.5		ns	2-10
t_W	LE Pulse Width High or Low	5.0	6.0		6.0		ns	2-9

Note: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	10	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.

C_{OUT} for 74FCT only.

National Semiconductor

54FCT/74FCT574
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

FACT FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

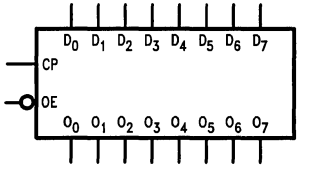
The 'FCT574 is functionally identical to the 'FCT374 except for the pinouts.

Features

- NSC 54FCT/74FCT574 is pin and functionally equivalent to IDT 54FCT/74FCT574
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity.
- Input clamp diodes to limit bus reflections.
- TTL/CMOS input and output level compatible.
- I_{OL} = 48 mA (Com) and 32 mA (Mil)
- CMOS power levels
- ESD immunity ≥ 4kV typ
- Military Product compliant to MIL-STD 883

Ordering Code: See Section 8

Logic Symbols



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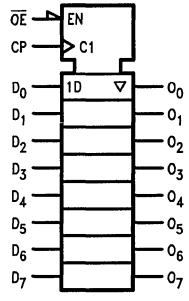
IEEE/IEC



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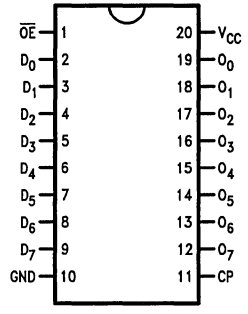
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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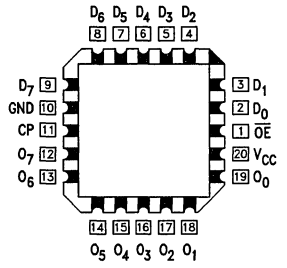
Pin Assignment for LCC



TL/F/10673–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

Functional Description

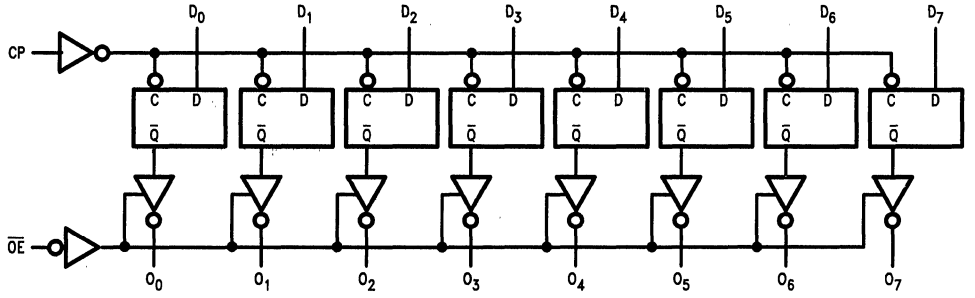
The 'FCT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	L	Z	Load
H	⌐	H	H	Z	Load
L	⌐	L	L	L	Data Available
L	⌐	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/10673–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCT: −0.5V to +7.0V
- 74FCT: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCT: −55°C to +125°C
- 54FCT: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum ratings conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCT: 4.5V to 5.5V
- 74FCT: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCT: −55°C to +125°C
- 74FCT: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} −0.2V

Symbol	Parameter	54FCT/74FCT Min	54FCT/74FCT Typ	54FCT/74FCT Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	V_O = V_{CC} V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage		2.8	3.0	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
			V_{HC}	V_{CC}		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA
			2.4	4.3			I_{OH} = −12 mA (Mil)
			2.4	4.3			I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 μA
			0.3	0.5			I_{OL} = 32 mA (Mil)
			0.3	0.5			I_{OL} = 48 mA (Com)

DC Characteristics for 'FCT Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} −0.2V (Continued)

Symbol	Parameter	74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHz f_I = 5.0 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHz f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I_{CCD} = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I_C/I_{CC} limits.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCT/74FCT	74FCT		54FCT		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$		$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$			
		Typ	Min (Note)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	6.6	2.0	10.0	2.0	11.0	ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	9.0	1.5	12.5	1.5	14.0	ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	6.0	1.5	8.0	1.5	8.0	ns	2-11
t_{SU}	Set-Up Time High or Low D_n to CP	1.0	2.0		3.5		ns	2-10
t_H	Hold Time High or Low D_n to CP	0.5	2.0		2.0		ns	2-10
t_W	CP Pulse Width High or Low	4.0	7.0		7.0		ns	2-9

Note: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance ($T_A = +25°C, f = 1.0$ MHz)

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured during characterization but not tested.
C_{OUT} for 74FCT only.

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT646
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

The 'FCT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA).

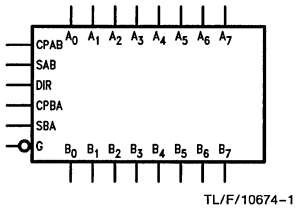
FACT™ FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT646 is pin and functionally equivalent to IDT 54FCT/74FCT646
- Independent registers for A and B buses multiplexed real time and stored time
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (Com), 48 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD-883

Logic Symbols



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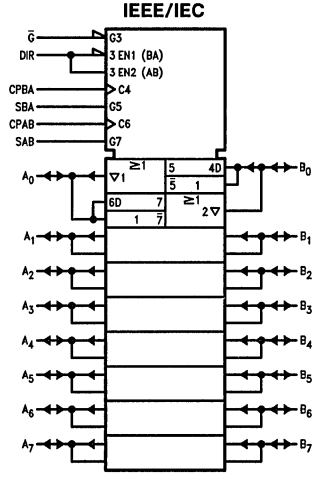
IEEE/IEC

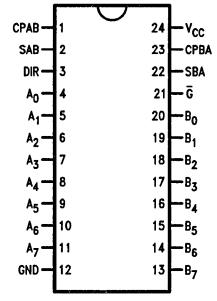


TL/F/10674–2

Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

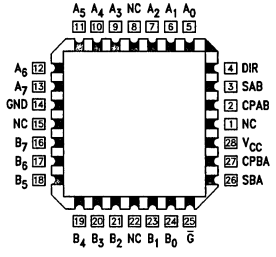
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10674–3

Pin Assignment for LCC and PCC



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Section 7

FCT A and B Series Datasheets

Section 7 Contents

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT138A
1-of-8 Decoder/Demultiplexer

General Description

The 'FCT138A is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'FCT138A devices or a 1-of-32 decoder using four 'FCT138A devices and one inverter.

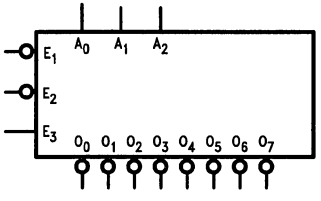
FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

- NSC 54FCT/74FCT138A is pin and functionally equivalent to IDT 54FCT/74FCT138A
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbol



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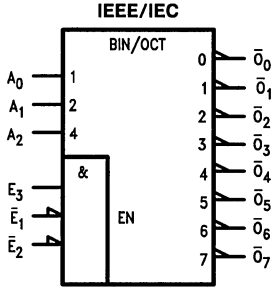
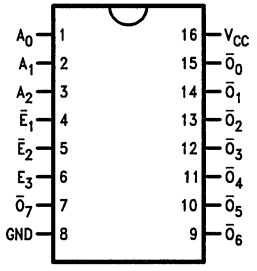


TL/F/10658–4

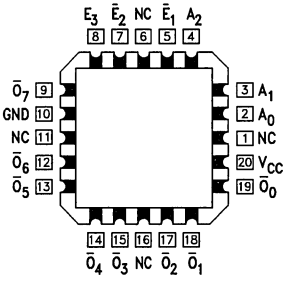
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10658–2

Pin Assignment for LCC



TL/F/10658–3

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

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National Semiconductor

54FCT/74FCT240A
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

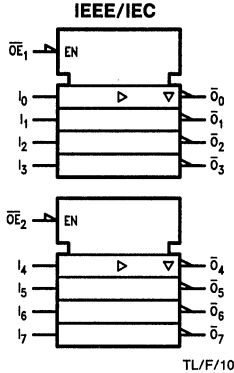
The 'FCT240A is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- NSC 54/74FCT240A is pin and functionally equivalent to IDT 54/74FCT240A
- Inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up immunity
- I_{OL} = 64 mA (commercial) and 48 mA (military)
- Electrostatic discharge protection ≥ 2 kV
- Military product compliant to MIL-STD 883C
- Inherently radiation tolerant

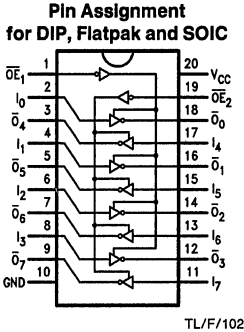
Ordering Code: See Section 8

Logic Symbol

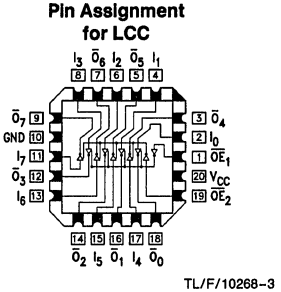


TL/F/10268–1

Connection Diagrams



TL/F/10268–2



TL/F/10268–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs
$\overline{OE}1$	D	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}2$	D	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to 7.0V
- 74FCTA: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq$ 0.2V, f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND f_i = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note 1)	Max	Min (Note 1)	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	3.5	1.5	4.8			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	4.8	1.5	6.2			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	4.3	1.5	5.6			ns	2-11

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f = 1.0 MHz

Symbol	Parameter (Note)	Typ	Max	Units	Condition
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT241A
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'FCT241A is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

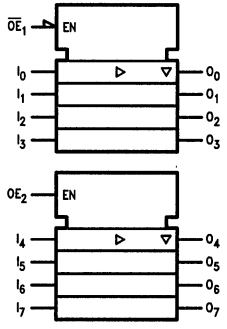
Features

- NSC 54/74FCT241A is pin and functionally equivalent to IDT 54/74FCT241A
- Non-inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- 'FCT241A has TTL-compatible inputs
- Military product compliant to MIL-STD-883C
- Inherently radiation tolerant
- I_{OL} = 64 mA (Comm) and 48 mA (Mil)
- TTL input and output level compatible
- High current latch up

Ordering Code: See Section 8

Logic Symbol

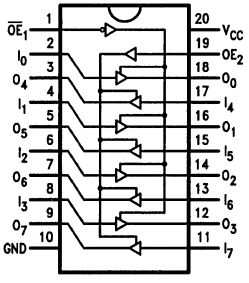
IEEE/IEC



TL/F/10269–1

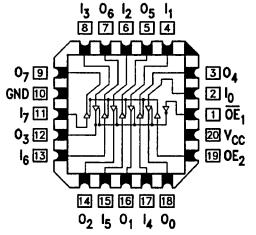
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10269–2

Pin Assignment for LCC



TL/F/10269–3

Pin Names	Description
$\overline{OE}_1$,	TRI-STATE Output Enable Input
OE_2	TRI-STATE Output Enable Input (Active HIGH)
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	D	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
OE_2	D	
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 74FCTA: −0.5V to 7.0V
- 54FCTA: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditons shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ $f_I = 0$	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditons shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0		f_i = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$			
		Typ	Min (Note 1)	Max	Min (Note 1)	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	3.0	1.5	4.8			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	4.0	1.5	6.2			ns	2-10
t_{PHZ} t_{PLZ}	Output Disable Time	3.0	1.5	5.6			ns	2-10

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance ($T_A = +25°C$, f = 1.0 MHz)

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT244A
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

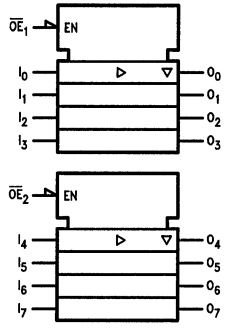
The 'FCT244A is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

Features

- NSC 54/74FCT244A is pin and functionally equivalent to IDT 54/74FCT244A
- TRI-STATE outputs drive lines or buffer memory address registers
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up immunity
- I_{OL} = 64 mA (commercial) and 48 mA (military)
- Electrostatic discharge protection ≥ 2 kV
- Military product compliant to MIL-STD 883C
- Inherently radiation tolerant

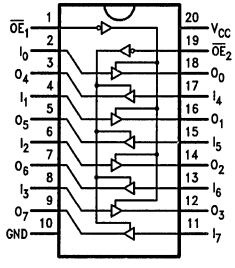
Ordering Code: See Section 8

Logic Symbol

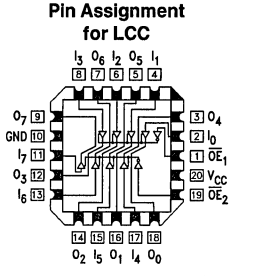


TL/F/10270–1

Connection Diagrams



TL/F/10270–2



TL/F/10270–3

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Inputs
I_0–I_7	Inputs
O_0–O_7	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	D	
L	L	L
L	H	H
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	D	
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to 7.0V
- 74FCTA: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditons shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCTA/74FCTA Min	54FCTA/74FCTA Typ	54FCTA/74FCTA Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2) V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditons shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0		f_i = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50$ pF		$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50$ pF			
		Typ	Min (Note 1)	Max	Min (Note 1)	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	3.1	1.5	4.8			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	3.8	1.5	6.2			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	3.3	1.5	5.6			ns	2-11

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance ($T_A = +25°C$, f = 1.0 MHz)

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT245A
Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

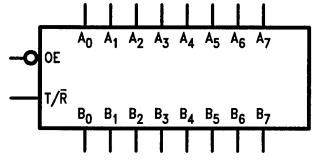
The 'FCT245A contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

Features

- NSC 54/74FCT245A is pin and functionally equivalent to IDT 54/74FCT245A
- Non-inverting buffers
- Bidirectional data path
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up immunity
- I_{OL} = 64 mA (commercial) and 48 mA (military)
- Electrostatic discharge protection ≥ 2 kV
- Military product compliant to MIL-STD 883C
- Inherently radiation tolerant

Ordering Code: See Section 8

Logic Symbols



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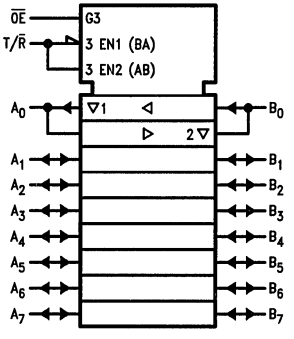
IEEE/IEC



TL/F/10271–2

Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

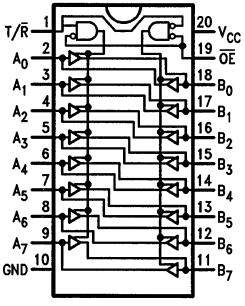
Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

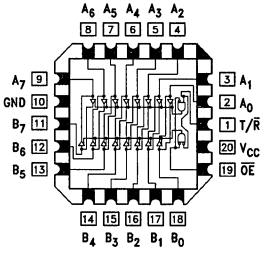
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10271–3

Pin Assignment for LCC



TL/F/10271–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to 7.0V
- 74FCTA: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current (except I/O Pins)			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IH}	Input High Current (I/O Pins Only)			15 15	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current (except I/O Pins)			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{IL}	Input Low Current (I/O Pins Only)			−15 −15	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCT/74FCT			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} = Max Outputs Open $T/\overline{R}$ = GND or V_{CC} $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $T/\overline{R} = \overline{OE}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0		f_I = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $T/\overline{R} = \overline{OE}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA $T_A = +25°C$ $V_{CC} = 5.0V$	74FCTA $T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		54FCTA $T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$		Units	Fig. No.
		Typ	Min (Note 2)	Max	Min (Note 2)	Max		
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	3.3	1.5	4.6			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B	4.8	1.5	6.2			ns	2-8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to A or B	4.5	1.5	5.0			ns	2-11
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B (Note 1)	4.8	1.5	6.2			ns	2-11
t_{PHZ} t_{PLZ}	Output Enable Time T/$\overline{R}$ to A or B (Note 1)	4.5	1.5	5.0			ns	2-11

Note 1: This parameter is guaranteed but not tested.

Note 2: Minimum limits guaranteed but not tested on propagation delays.

Capacitance $T_A = +25°C$, f = 1.0 MHz

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT273A Octal D Flip-Flop

General Description

The 'FCT273A has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

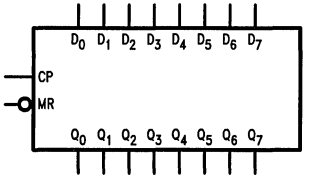
FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features NSC correction and split ground bus for superior performance.

Features

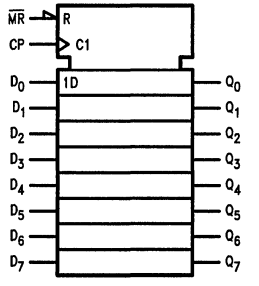
- NSC 54FCT/74FCT273A is pin and functionally equivalent to IDT 54FCT/74FCT273A
- Ideal buffer for MOS microprocessor or memory
- Buffered common clock
- Buffered, asynchronous master reset
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



TL/F/10660–1

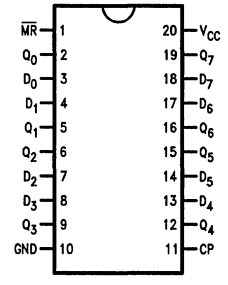
IEEE/IEC



TL/F/10660–2

Connection Diagrams

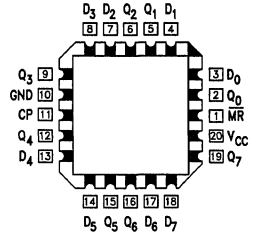
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10660–3

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

Pin Assignment for LCC



TL/F/10660–4

National Semiconductor

54FCT/74FCT373A
Octal Transparent Latch with TRI-STATE® Outputs

General Description

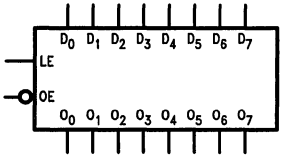
The 'FCT373A consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Features

- NSC 54/74FCT373A pin and functionally equivalent to IDT 54/74FCT373A
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- TTL input and output level compatible
- High current latch up immunity
- I_{OL} = 48 mA (commercial) and 32 mA (military)
- Military product compliant to MIL-STD 883

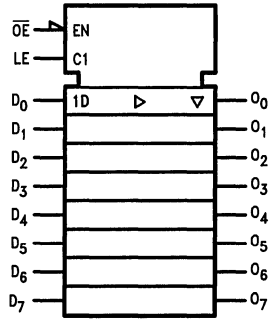
Ordering Code: See Section 8

Logic Symbols



TL/F/10618–1

IEEE/IEC

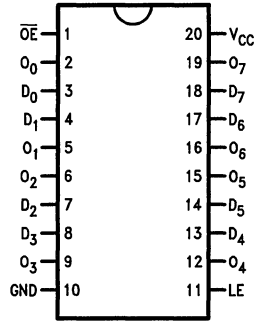


TL/F/10618–2

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

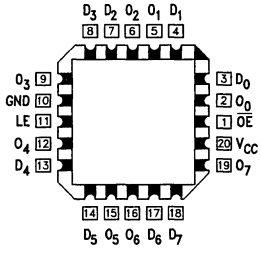
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10618–3

Pin Assignment for LCC



TL/F/10618–4

Functional Description

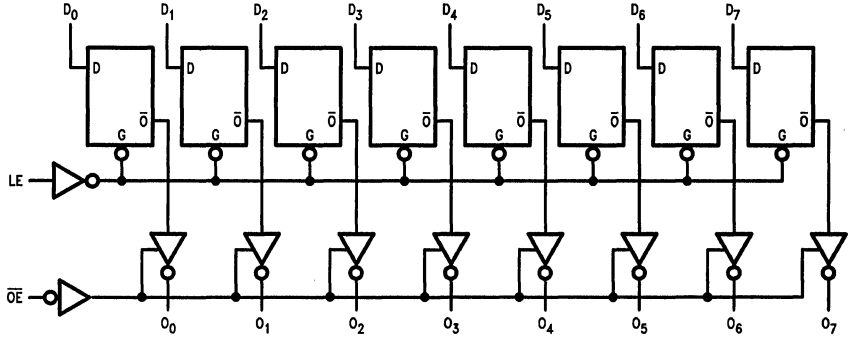
The 'FCT373A contains eight D-type latches with TRI-STATE outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH to Low transition of Latch Enable

Logic Diagram



TL/F/10618–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCTA circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2) V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.50 0.50		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ $f_I = 0$	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0		f_i = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max $\overline{OE}$ = GND LE = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} =$ Com $R_L = 500\Omega$ $C_L = 50$ pF		$T_A, V_{CC} =$ Mil $R_L = 500\Omega$ $C_L = 50$ pF			
		Typ	Min (Note 1)	Max	Min (Note 1)	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	4.0	1.5	5.2			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	6.5			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	4.0	1.5	5.5			ns	2-11
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	7.0	2.0	8.5			ns	2-8
t_{SU}	Set Up Time High or Low D_n to LE	1.0	2.0				ns	2-10
t_H	Hold Time High or Low D_n to LE	1.0	1.5				ns	2-10
t_W	LE Pulse Width High or Low	4.0	5.0				ns	2-9

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance $T_A = +25°C, f = 1.0$ MHz

Symbol	Parameter (Note 1)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT374A
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

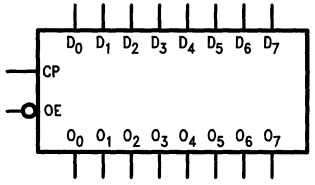
The 'FCT374A is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- NSC 54/74FCT374A is pin and functionally equivalent to IDT 54/74FCT374A
- Buffered positive edge triggered clock
- TRI-STATE outputs for bus-oriented applications
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up immunity
- I_{OL} = 48 mA (commercial) and 32 mA (military)
- Electrostatic discharge protection ≥ 2 kV
- Inherently radiation tolerant

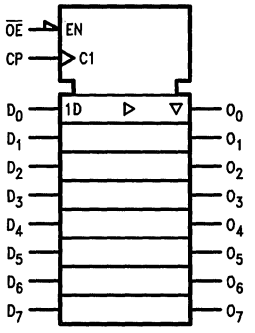
Ordering Code: See Section 8

Logic Symbols



TL/F/10264–1

IEEE/IEC

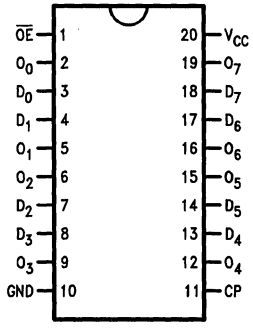


TL/F/10264–2

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

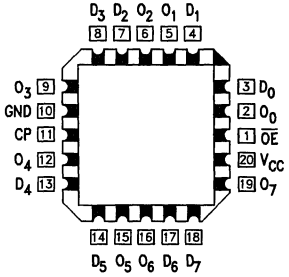
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10264–3

Pin Assignment for LCC



TL/F/10264–4

Functional Description

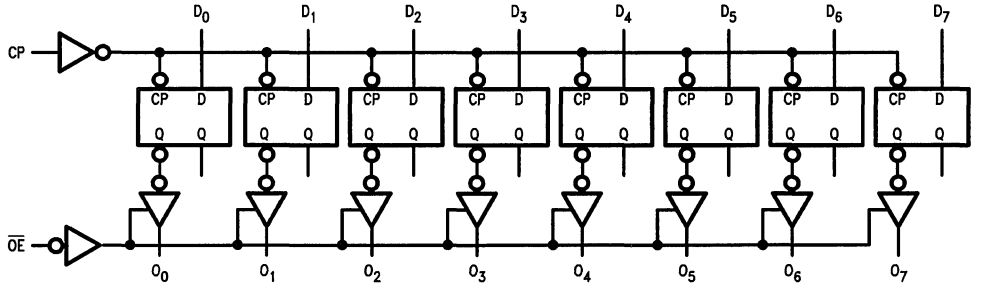
The 'FCT374A consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition

Logic Diagram



TL/F/10264–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to 7.0V
- 74FCTA: −0.5V to 7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$.

Symbol	Parameter	54FCTA/74FCTA Min	54FCTA/74FCTA Typ	54FCTA/74FCTA Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.50 0.50		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_i = 5.0 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			2.0	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.75	7.8		(Note 5) V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			6.0	16.8			V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$			
		Typ	Min (Note 1)	Max	Min (Note 1)	Max		
t_{PLH} t_{PHL}	Propagation Delay C_P to O_n	4.5	2.0	6.5			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	6.5			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	4.0	1.5	5.5			ns	2-11
t_{SU}	Set Up Time High or Low D_n to C_P	1.0	2.0				ns	2-10
t_H	Hold Time High or Low D_n to C_P	0.5	1.5				ns	2-10
t_w	C_P Pulse Width High or Low	4.0	5.0				ns	2-9

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance $T_A = +25°C, f = 1.0\ MHz$

Symbol	Parameter (Note)	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.

National Semiconductor

ADVANCE INFORMATION

54FCT377A/74FCT377A
Octal D Flip-Flop with Clock Enable

General Description

The FCT377A has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

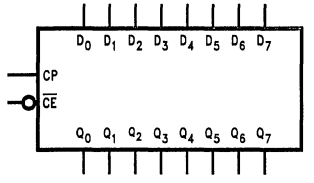
FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot corrector in addition to a split ground bus for superior performance.

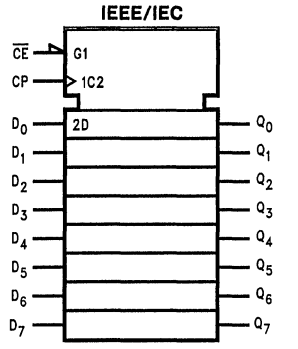
Features

- NSC 54FCT/74FCT377A is pin and functionally equivalent to IDT 54FCT/74FCT377A
- Ideal for addressable register applications
- Clock enables for address and data synchronization applications
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV.
- Military product compliant to MIL-STD 883

Logic Symbols



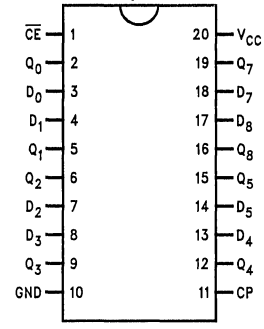
TL/F/10697–1



TL/F/10697–2

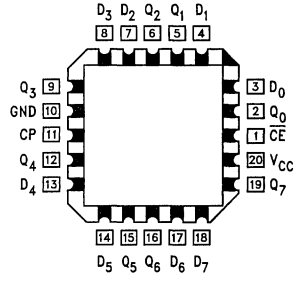
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10697–3

Pin Assignment for LCC



TL/F/10697–4

Pin Names	Description
D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT521A
8-Bit Identity Comparator

General Description

The 'FCT521A is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

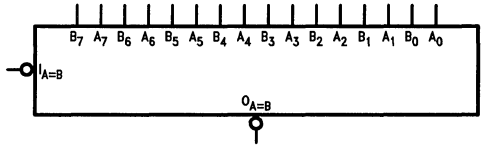
FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

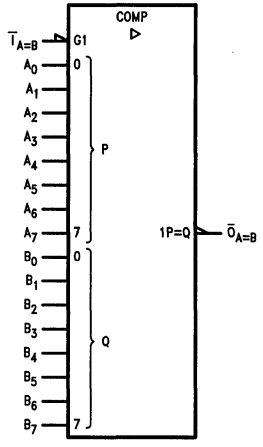
- NSC 54FCT/74FCT521A is pin and functionally equivalent to IDT 54FCT/74FCT521A
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



TL/F/10663–1

IEEE/IEC

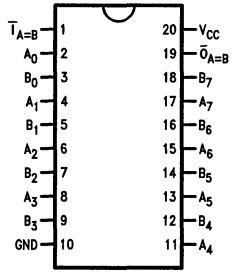


TL/F/10663–3

Pin Names	Description
A_0–A_7	Word A Inputs
B_0–B_7	Word B Inputs
$T_{A=B}$	Expansion or Enable Input
$\overline{O}_{A=B}$	Identity Output

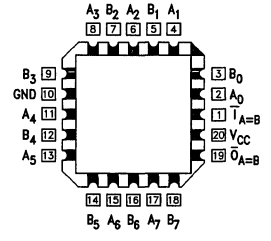
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10663–2

Pin Assignment for LCC



TL/F/10663–4

National Semiconductor

54FCT/74FCT533A
Octal Transparent Latch with TRI-STATE® Outputs

General Description

The 'FCT533A consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. The 'FCT533A is the same as the 'FCT373A, except that the outputs are inverted.

FACT FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

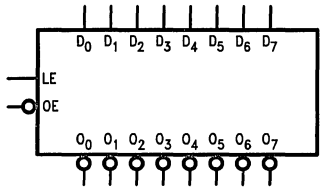
FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

- NSC 54FCT/74FCT533A is pin and functionally equivalent to IDT 54FCT/74FCT533A
- TRI-STATE outputs for bus interfacing
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD 883
- Inherently radiation tolerant

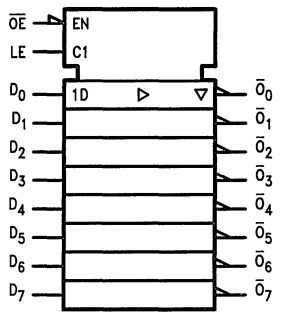
Ordering Code: See Section 8

Logic Symbols



TL/F/10638–4

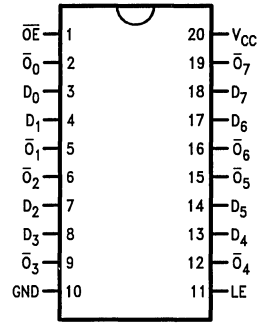
IEEE/IEC



TL/F/10638–1

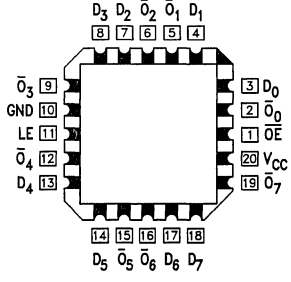
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



TL/F/10638–2

Pin Assignment for LCC



TL/F/10638–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

Function Table

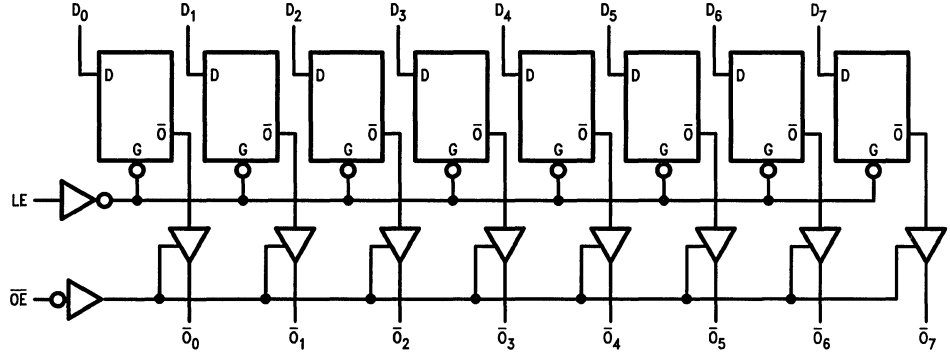
Inputs			Output
LE	$\overline{OE}$	D	$\overline{O}$
H	L	H	L
H	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Logic(0) or logic(1) must be valid Input Level

Functional Description

The 'FCT533A contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent and the latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW the latch contents are presented inverted at the outupts $\overline{O}_7$–$\overline{O}_0$. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



TL/F/10638–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Voltage with respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C.

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum HIGH Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0	μA	V_{CC} = Max	$V_I = V_{CC}$
				5.0			V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2)
				−5.0			V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0	μA	V_{CC} = Max	$V_O = V_{CC}$
				10.0			V_O = 2.7V (Note 2)
				−10.0			V_O = 0.5V (Note 2)
				−10.0			V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_{IN} = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC}	V_{CC}			V_{CC} = Min	I_{OH} = −300 μA
		2.4	4.3			$V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −12 mA (Mil)
		2.4	4.3				I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min	I_{OL} = 300 μA
			0.3	0.50		$V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 32 mA (Mil)
			0.3	0.50			I_{OL} = 48 mA (Com)

DC Characteristics for FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C. (Continued)

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} f_I = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5			V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	4.0	1.5	5.2			ns	2–8
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	7.0	2.0	8.5			ns	2–8
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	6.5			ns	2–11
t_{PHZ} t_{PLZ}	Output Disable Time	4.0	1.5	5.5			ns	2–11
t_S	Set Up Time High or Low D_n to LE	1.0	2.0				ns	2–10
t_H	HOLD Time High or Low D_n to LE	1.0	1.5				ns	2–10
t_W	LE Pulse Width High or Low	4.0	5.0				ns	2–9

Minimum limits are guaranteed but not tested on Propagation Delays

Capacitance (T_A = +25C, f = 1.0 MHz)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{in}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{out}	Output Capacitance	8	12	pF	V_{out} = 0V

Note: This parameter is measured at characterization but not tested

National Semiconductor

54FCT/74FCT534A
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

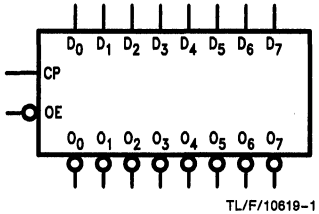
The 'FCT534A is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'FCT534A is the same as the 'FCT374A except that the outputs are inverted.

Features

- NSC 54/74FCT534A is pin and functionally equivalent to IDT 54/74FCT534A
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- Military product compliant to MIL-STD-883

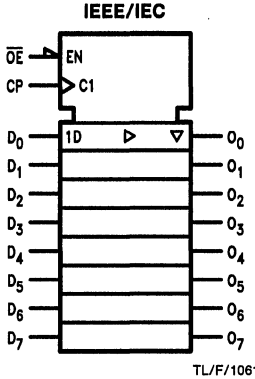
Ordering Code: See Section 8

Logic Symbols



TL/F/10619–1

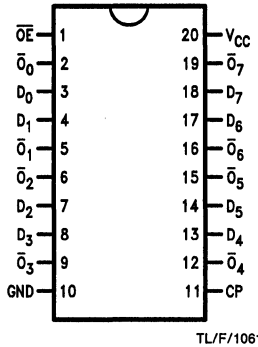
IEEE/IEC



TL/F/10619–2

Connection Diagrams

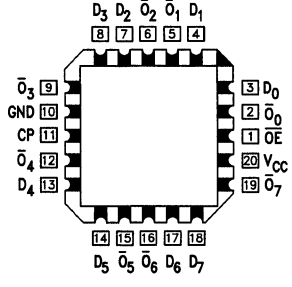
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10619–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

Pin Assignment for LCC

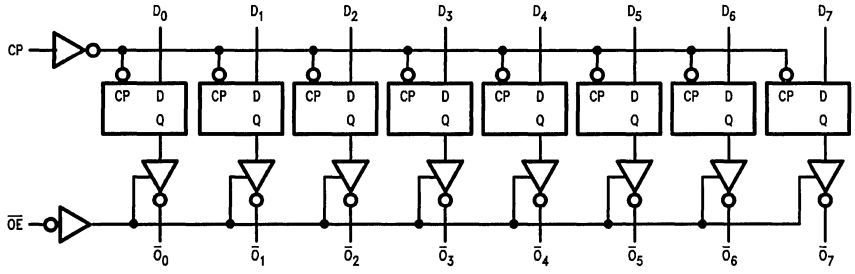


TL/F/10619–4

Functional Description

The 'FCT534A consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



TL/F/10619–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs			Output
CP	OE	D	$\overline{O}$
⌐‾	L	H	L
⌐‾	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐‾ = LOW-to-HIGH Clock Transition
Z = High Impedance
$\overline{O}_0$ = Value stored from previous clock cycle

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature Under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	V_O = V_{CC} V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.5 0.5		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 μA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)
V_H	Input Hysteresis on Clock Only		200		mV		

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V.

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.40	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz $\overline{OE}$ = GND f_I = 5 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHz f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Numbers of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		T_A = +25°C, V_{CC} = 5.0V	T_A, V_{CC} = Mil, C_L = 50 pF		T_A V_{CC} = Com, C_L = 50 pF			
		Typ	Min (Note 1)	Max	Min (Note 1)	Max		
t_{PLH} t_{PHL}	Propagation Delay C_P to $\overline{On}$	4.5	1.5	6.5			ns	2-9
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	6.5			ns	2-11
t_{PHZ} t_{PHL}	Output Disable Time	4.0	1.5	5.5			ns	2-11
t_s	Set Up Time High or Low Dn to CP	1.0	2.0				ns	2-10
t_h	Hold Time High or Low Dn to CP	1.0	1.5				ns	2-10
t_w	CP Pulse Width High or Low	4.0	5.0				ns	2-9

Note 1: Minimum limits guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f_I = 1.0 MHz

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT543A
Octal Registered Transceiver

General Description

The FCT543A octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

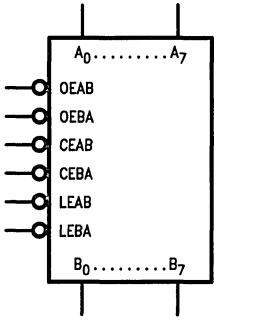
FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

- NSC 54FCT/74FCT543A is pin and functionally equivalent to IDT 54FCT/74FCT543A
- Speed controls for data flow in each direction
- Back to back latched transceiver
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (com), 48 mA (mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product complaint to MIL-STD 883

Ordering Code: See Section 8

Logic Symbols



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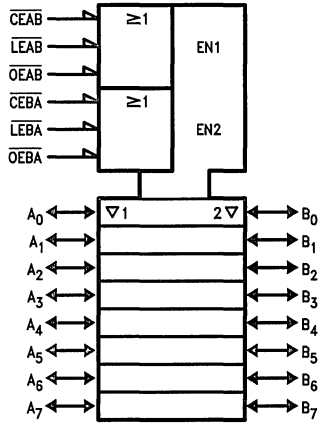

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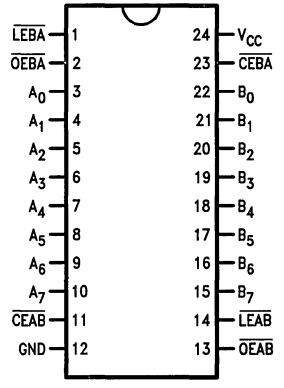
Connection Diagrams

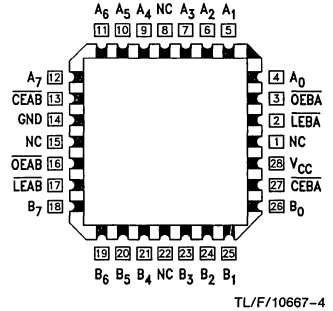
Pin Assignment for DIP and SOIC



TL/F/10667–3

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

Pin Assignment for LCC



TL/F/10667–4

Functional Description

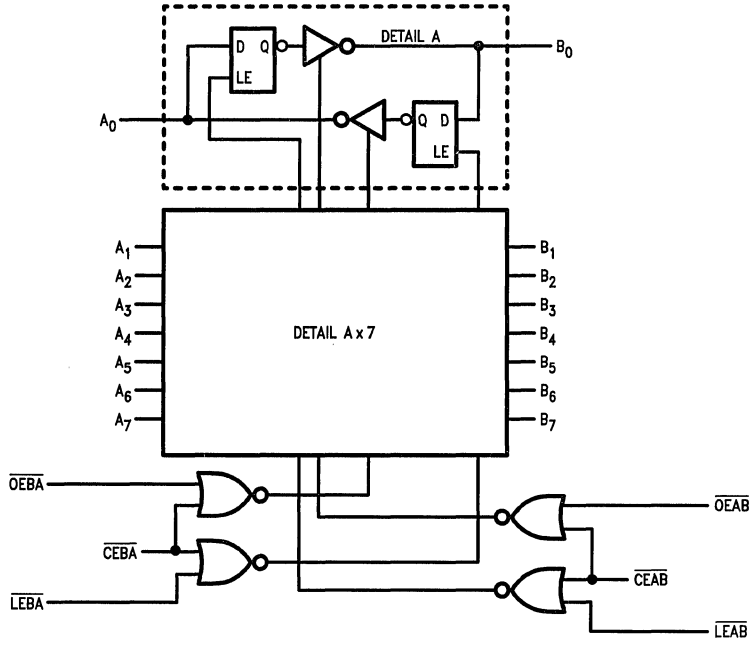
The FCT543A contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or take data from B_0–B_7, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Input			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEB}$ and $\overline{OEBA}$

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Device

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCTA/74FCTA Min	54FCTA/74FCTA Typ	54FCTA/74FCTA Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input Current (Except I/O Pins)			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current (Except I/O Pins)			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{IH}	Input High Currents (I/O Pins)			15 15	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V
I_{IL}	Input Low Currents (I/O Pins)			−15 −15	μA	V_{CC} = Max	V_I = 0.5V V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.55 0.55		V_{CC} = Min $V_{IN} = V_{IL}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	

DC Characteristics for 'FCTA Family Device

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} −0.2V (Continued)

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	0.2	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.55	mA/MHz	V_{CC} = Max Outputs Open $\overline{CEAB}$ & $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open t_{CP} = 10 MHz 50% Duty Cycle $\overline{CEAB}$ & $\overline{OEAB}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0		$\overline{CEBA}$ = V_{CC} f_{CP} = $\overline{LEAB}$ = 10 MHz One Bit Toggling at f_i = 5 MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	16.5		(Note 5) V_{CC} = Max Outputs Open t_{CP} = 10 MHz 50% Duty Cycle $\overline{CEAB}$ & $\overline{OEAB}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	21.75		$\overline{CEBA}$ = V_{CC} f_{CP} = $\overline{LEAB}$ = 10 MHz f_i = 2.5 MHz Eight Bits Toggling at f_i = 5 MHz 50% Duty Cycle	V_{IN} = 3.4 V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in millamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA $T_A = +25°C$ $V_{CC} = 5.0V$	74FCTA $T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		54FCTA $T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$		Units	Fig. No.
		Typ	Min (Note)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n		1.5	6.5			ns	2-8
t_{PLH} t_{PLH}	Propagation Delay $\overline{LEAB}$ to A_n, $\overline{LEAB}$ to B_n		1.5	8			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n		2	9			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n		2	7.5			ns	2-11
t_{SU}	Set Up Time High or Low A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$		2				ns	2-10
t_H	Hold Time		2				ns	2-10

Note: Minimum propagation delays are guaranteed but not listed.

Capacitance $T_A = +25°C, f = 1.0\ MHz$

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT544A
Octal Registered Transceiver

General Description

The 'FCT544A octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The 'FCT544A inverts data in both directions.

FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

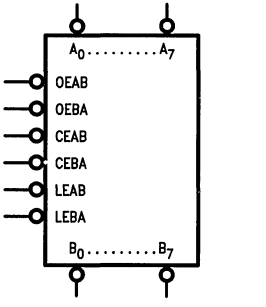
FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

- NSC 54FCT/74FCT544A is pin and functionally equivalent to IDT 54FCT/74FCT544A
- Back to back registers for storage separate controls for data flow in each direction
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (Com), 48 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Ordering Code: See Section 8

Logic Symbols



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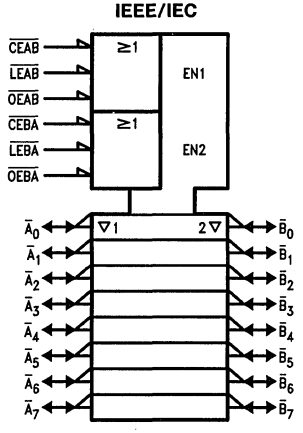
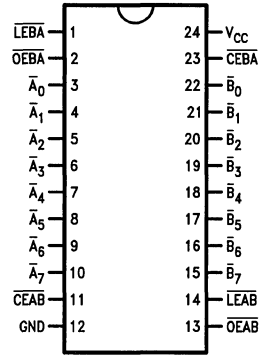
IEEE/IEC



TL/F/10669–2

Connection Diagrams

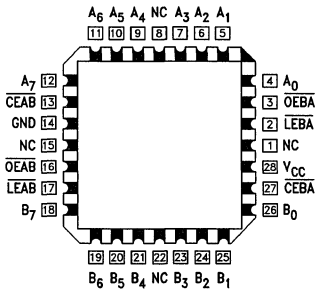
Pin Assignment for DIP and SOIC



TL/F/10669–3

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
$\overline{A}_0$–$\overline{A}_7$	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
$\overline{B}_0$–$\overline{B}_7$	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

Pin Assignment for LCC



TL/F/10669–4

Functional Description

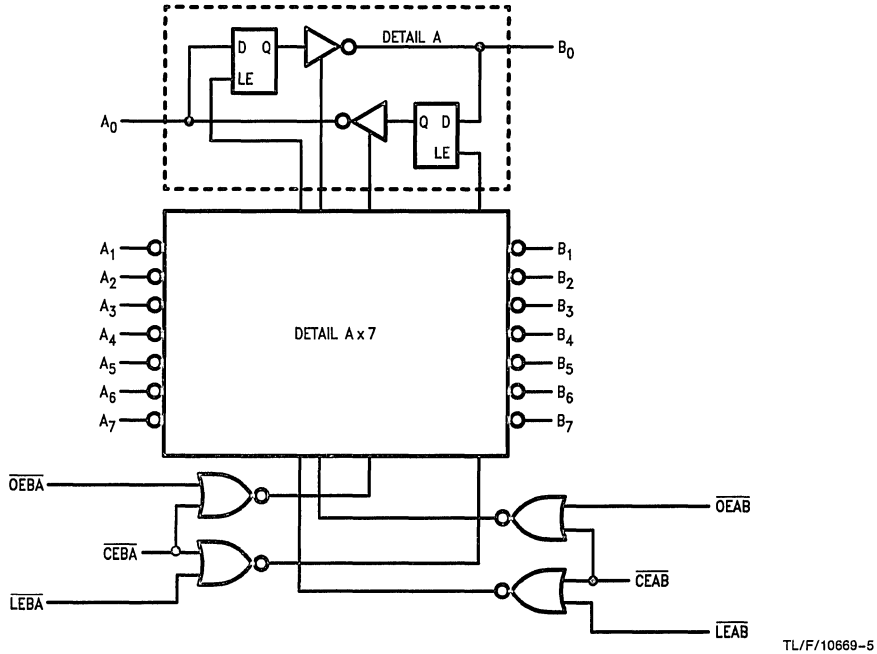
The 'FCT544A contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from $\overline{A}_0$–$\overline{A}_7$ or take data from $\overline{B}_0$–$\overline{B}_7$, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ outputs.

Data I/O Control Table

Input			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High-Z
X	H	X	Latched	
L	L	X	Transparent	
X	X	H		High-Z
L	X	L		Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Logic Diagram



TL/F/10669–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 54FCTA: −65°C to +135°C
- 74FCTA: −55°C to +125°C

Storage Temperature (T_{STG})
- 54FCTA: −65°C to +150°C
- 74FCTA: −55°C to +125°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C.

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current (Except I/O Pins)			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current (Except I/O Pins)			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{IH}	Input High Currents (I/O Pins)			15 15	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Currents (I/O Pins)			−15 −15	μA	V_{CC} = MAx	V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8 V_{HC} 2.4 2.4	3.0 V_{CC} 4.3 4.3		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND GND 0.3 0.3	0.2 0.2 0.55 0.55	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_L = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq$ 0.2V f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C.

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.3	mA/MHz	V_{CC} = Max Outputs Open $\overline{CEAB} + \overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{CEAB} + \overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC}. $f_{CP} = \overline{LEAB}$ = 10 MHz One Bit Toggling at f_1 = 5 MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	16.5		(Note 5) V_{CC} = Max Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{CEAB} + \overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC}. $f_{CP} = \overline{LEAB}$ = 10 MHz Eight Bits Toggling at f_i = 5 MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	21.75			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of Inputs at D_H
I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note 1)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n		1.5	7.0			ns	2-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEAB}$ to A_n, $\overline{LEAB}$ to B_n		1.5	8.0			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n		1.5	9			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{CEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{OEAB}$ to A_n or B_n		1.5	7.5			ns	2-11
t_{SU}	Setup Time High or Low A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$		2				ns	2-10
t_H	Hold Time High or Low A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$		2				ns	2-10

Note 1: Minimum propagation delays are guaranteed but not tested.

Capacitance T_A = +25°C, f = 1.0 MHz

Symbol	Parameter (Note)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT563A
Octal Latch with TRI-STATE® Outputs

General Description

The 'FCT563A is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The 'FCT563A device is functionally identical to the 'FCT573A, but with inverted outputs.

FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

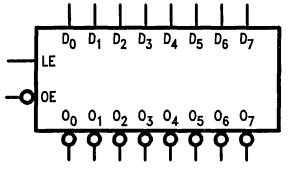
FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

- Inputs and outputs on opposite side of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD-883
- Inherently radiation tolerant

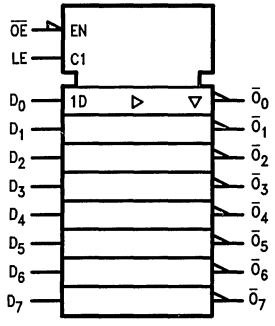
Ordering Code: See Section 8

Logic Symbols



TL/F/10639–1

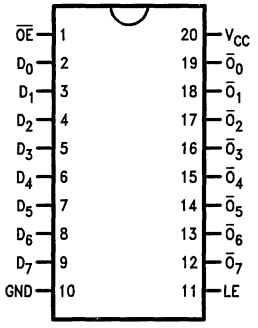
IEEE/IEC



TL/F/10639–2

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



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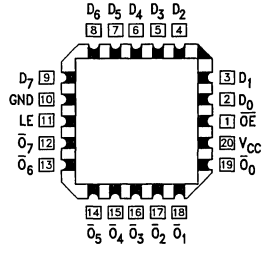
Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Latch Outputs

Pin Assignment for LCC



TL/F/10639–4

Functional Description

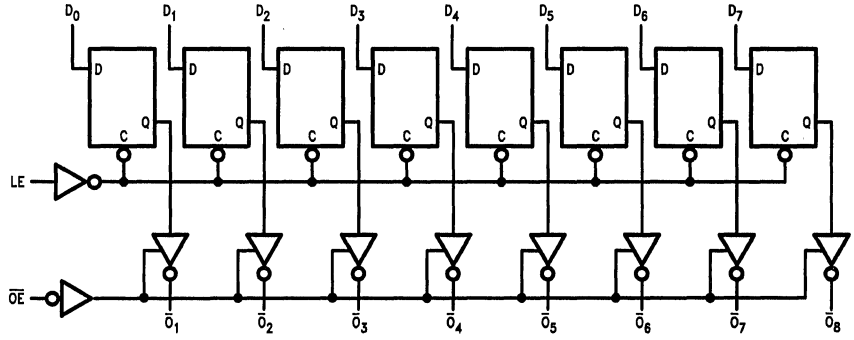
The 'FCT563A contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the TRI-STATE mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Outputs	Function
$\overline{OE}$	LE	D	O	
H	X	X	Z	High-Z
L	H	L	H	Transparent
L	H	H	L	Transparent
L	L	X	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



TL/F/10639–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0	μA	V_{CC} = Max	$V_I = V_{CC}$
				5.0			V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2)
				−5.0			V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0	μA	V_{CC} = Max	$V_O = V_{CC}$
				10.0			V_O = 2.7V (Note 2)
				−10.0			V_O = 0.5V (Note 2)
				−10.0			V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0			V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC}	V_{CC}		V	V_{CC} = Min; $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA
		2.4	4.3				I_{OH} = −12 mA (Mil)
		2.4	4.3				I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min; $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA
			0.3	0.50			I_{OL} = 32 mA (Mil)
			0.3	0.50			I_{OL} = 48 mA (Com)

DC Characteristics for FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0		LE = V_{CC} f_I = 10 MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5		LE = V_{CC} f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		T_A = 25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	4.0	1.5	5.2			ns	2-8
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	7.0	2.0	8.5			ns	2-8
t_{PZL} t_{PZH}	Output Enable Time	5.5	1.5	6.5			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	4.0	1.5	5.5			ns	2-11
t_S	Set Up Tme High or Low D_n to LE	1.0	2.0				ns	2-10
t_H	Hold Time High or Low D_n to LE	1.0	1.5				ns	2-10
t_W	LE Pulse Width High or Low	4.0	5.0				ns	2-9

Minimum limits are guaranteed but not tested on propagation delays.

Capacitance T_A = +25°C, f = 1.0 MHz

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT564A
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT564A is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'FCT564A device is functionally identical to the 'FCT574A, but with inverted outputs.

FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

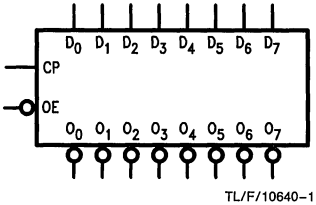
FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

- TRI-STATE outputs for bus-oriented applications
- Useful as input or output port for microprocessors
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD-883
- Inherently radiation tolerant

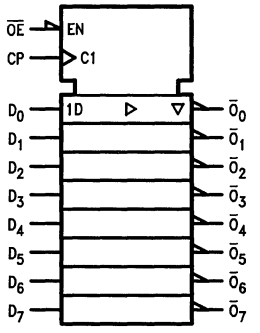
Ordering Code: See Section 8

Logic Symbols



TL/F/10640–1

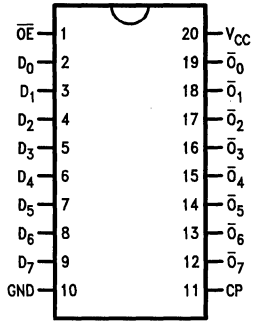
IEEE/IEC



TL/F/10640–2

Connection Diagrams

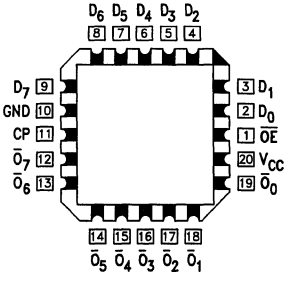
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10640–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	TRI-STATE Outputs

Pin Assignment for LCC



TL/F/10640–4

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with respect to GND (V_{TERM})
- 54FCTA: −0.5V to 7.0V
- 74FCTA: −0.5 to 7.0V

Temperature Under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5w

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} 5.0V ±5%, T_A = 0°C to +70°; Mil: V_{CC} = 5.0V ±10% T_A = 55°C +125°C V_{HC} = V_{CC} −0.2V

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	V_I = V_{CC} V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	V_O = V_{CC} V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
		V_{HC} 2.4 2.4	V_{CC} 4.3 4.3			V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
			GND 0.3 0.3	0.2 0.50 0.50		V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = 300 μA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V +5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C +125°C; V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHZ f_I = 5 MHz 50% Duty Cycle One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CP} = 10 MHz 50% Duty Cycle f_I = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND
V_H	Input Hysteresis on Clock Only		200		mV		

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		T_A = +25°C V_{CC} = 5.0V	T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF			
		Typ	Min (Note)	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{O}_n$	4.5	2.0	6.5			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	6.5			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Timed	4.0	1.5	5.5			ns	2-11
t_S	Set-Up Time High or Low D_n to CP	1.0	2.0				ns	2-10
t_H	HOLD Time High or Low D_n to CP	1.0	1.5				ns	2-10
t_W	CP Pulse Width High or Low	4.0	5.0				ns	2-9

Note: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT573A
Octal Latch with TRI-STATE® Outputs

General Description

The 'FCT573A is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

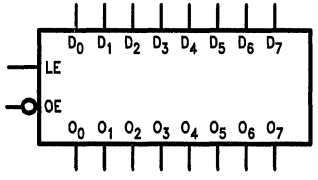
The 'FCT573A is functionally identical to the 'FCT373A but has inputs and outputs on opposite sides.

Features

- NSC 54/74FCT573A is pin and functionally equivalent to IDT 54/74FCT573A
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- TRI-STATE outputs for bus interfacing
- Military product compliant to MIL-STD-883
- TTL input and output level compatible
- TTL inputs accept CMOS levels

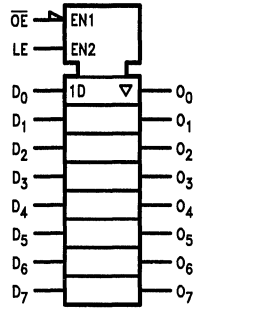
Ordering Code: See Section 8

Logic Symbols



TL/F/10641–1

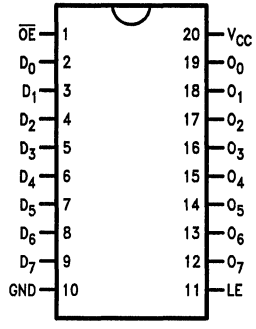
IEEE/IEC



TL/F/10641–2

Connection Diagrams

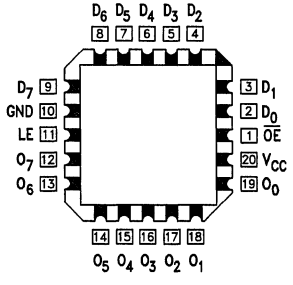
Pin Assignment for DIP, Flatpak and SOIC



TL/F/10641–3

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

Pin Assignment for LCC



TL/F/10641–4

Functional Description

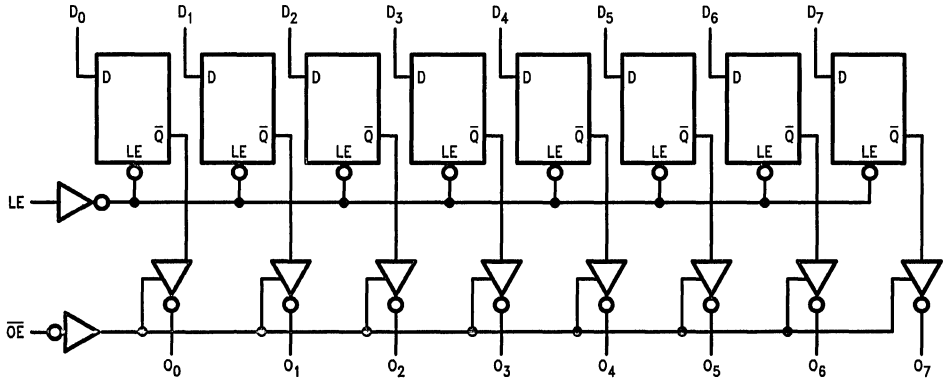
The FCT573A contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, and the latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the latch contents are presented inverted at the outputs $\overline{O}_7$–$\overline{O}_0$. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 54FCTA: −65°C to +135°C
- 74FCTA: −55°C to +125°C

Storage Temperature (T_{STG})
- 54FCTA: −65°C to +150°C
- 74FCTA: −55°C to +125°C

Power Dissipation (P_T): 0.5W

DC Ouput Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Doide Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8	3.0		V	V_{CC} = 3V; $V_{IN} = 0.2V$ or V_{HC}; I_{OH} = −32 μA	
		V_{HC}	V_{CC}			V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA
		2.4	4.3				I_{OH} = −12 mA (Mil)
		2.4	4.3				I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND	0.2	V	V_{CC} = 3V; $V_{IN} = 0.2V$ or V_{HC}; I_{OL} = 300 μA	
			GND	0.2		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA
			0.3	0.50			I_{OL} = 32 mA (Mil)
			0.3	0.50			I_{OL} = 48 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_I = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.45	mA/MHz	V_{CC} = Max Outputs Open One Input Toggling 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} − 0.2V

Symbol	Parameter	54FCTA/74FCTA Min	54FCTA/74FCTA Typ	54FCTA/74FCTA Max	Units	Conditions	
I_C	Total Power Supply Current (Note 6)		1.5	4.5	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND, LE = V_{CC} f_{CP} = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	5.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	8.0		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND, LE = V_{CC} f_{CP} = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	14.5			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL inputs High
N_T = Number of Inputs at D_H
I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_i = Input Frequency
N_i = Number of Inputs at f_i
All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54/74FCTA T_A = +25°C V_{CC} = 5.0V	74FCTA T_A, V_{CC} = Com R_L = 500Ω C_L = 50 pF		54FCTA T_A, V_{CC} = Mil R_L = 500Ω C_L = 50 pF		Units	Fig. No.
		Typ	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	4.0	1.5	5.2			ns	2-8
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	7.0	2.0	8.5			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	6.5			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	4.0	1.5	5.5			ns	2-11
t_S	Setup Time High or Low, D_n to LE	1.0	2.0				ns	2-10
t_H	Hold Time High or Low, D_n to LE	1.0	1.5				ns	2-10
t_W	LE Pulse Width High or Low	4.0	5.0				ns	2-9

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	10	pF	V_{OUT} = 0V

Note: This parameter is measured at characterization but not tested.

National Semiconductor

54FCT/74FCT574A
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT574A is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

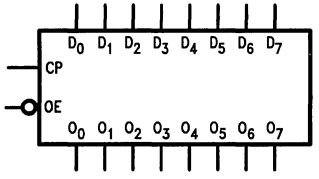
The 'FCT574A is functionally identical to the 'FCT374A except for the pinouts.

Features

- NSC 54/74FCT574A is pin and functionally equivalent to IDT54/74FCT574A
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'FCT374A
- TRI-STATE outputs for bus-oriented applications
- 'FCT574A has TTL-compatible inputs
- I_{OL} = 48 mA (Comm) and 32 mA (Mil)
- TTL inputs accept CMOS levels

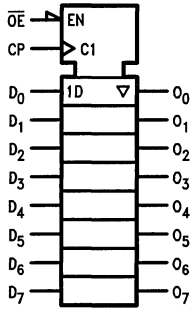
Ordering Code: See Section 8

Logic Symbols



TL/F/10150–1

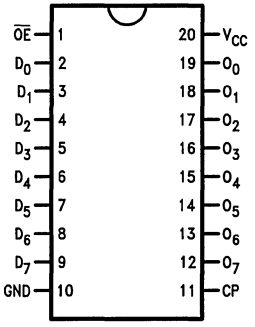
IEEE/IEC



TL/F/10150–4

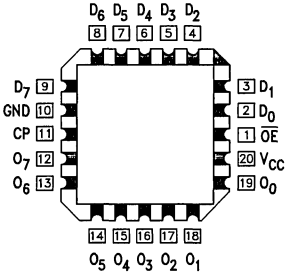
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10150–2

Pin Assignment for LCC



TL/F/10150–3

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Outputs

7

Functional Description

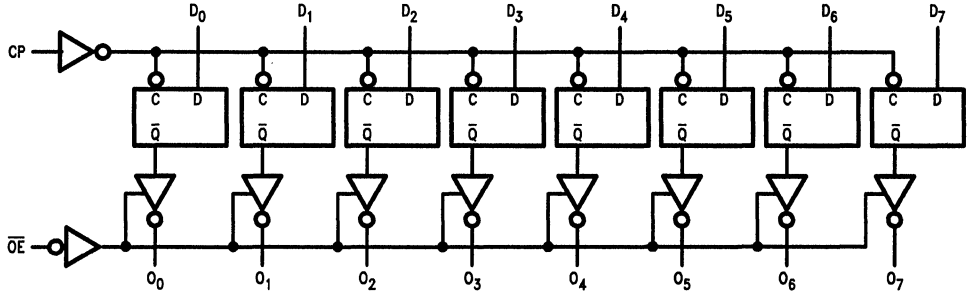
The 'FCT574A consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_N	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	↗	L	L	Z	Load
H	↗	H	H	Z	Load
L	↗	L	L	L	Data Available
L	↗	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↗ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



TL/F/10150–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: 0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCTA/74FCTA Min	54FCTA/74FCTA Typ	54FCTA/74FCTA Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_O = V_{CC}$ V_O = 2.7V (Note 2) V_O = 0.5V (Note 2) V_O = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage		2.8	3.0	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA	
			V_{HC} 2.4 2.4	V_{CC} 4.3 4.3		V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND GND 0.3 0.3	0.2 0.2 0.5 0.5	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA	
						V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 300 μA I_{OL} = 32 mA (Mil) I_{OL} = 48 mA (Com)

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10%, T_A = −55°C to +125°C, V_{HC} = V_{CC} −0.2V (Continued)

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ f_i = 0	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.15	0.25	mA/MHz	V_{CC} = Max Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_i = 5.0 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			1.8	6.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	7.8		(Note 5) V_{CC} = Max Outputs Open $\overline{OE}$ = GND f_{CD} = 10 MHz f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq 0.2V$
			5.0	16.8			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics: See Section 2 for Waveforms

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$			
		Typ	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	4.5	2.0	6.5			ns	2-8
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	6.5			ns	2-11
t_{PHZ} t_{PLZ}	Output Disable Time	4.0	1.5	5.5			ns	2-11
t_{SU}	Set-Up Time High or Low D_n to CP	1.0	2.0				ns	2-10
t_H	Hold Time High or Low D_n to CP	0.5	1.5				ns	2-10
t_W	CP Pulse Width High or Low	4.0	5.0				ns	2-9

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

Capacitance ($T_A = +25°C, f = 1.0$ MHz)

Symbol	Parameter (Note 1)	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	6	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT646A
Octal Transceiver/Register with TRI-STATE® Outputs

General Description

The FCT646A consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA).

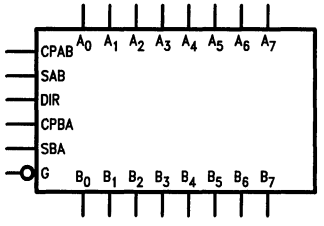
FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

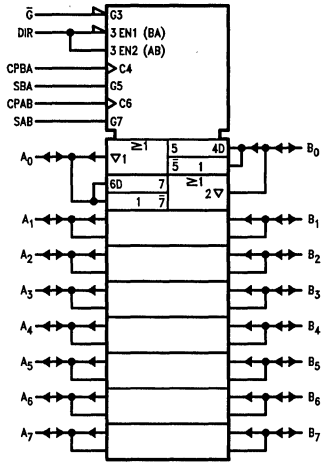
- NSC 54FCT/74FCT646A is pin and functionally equivalent to IDT 54FCT/74FCT646A
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 64 mA (Com), 48 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



TL/F/10675–1

IEEE/IEC

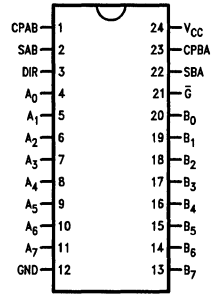


TL/F/10675–2

Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

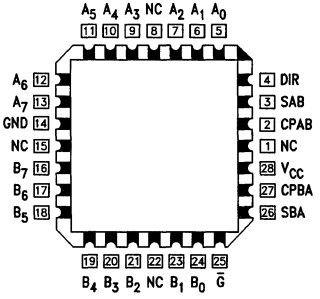
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10675–3

Pin Assignment for LCC and PCC



TL/F/10675–4

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT821A • 54FCT/74FCT821B
10-Bit D Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT821A/B is a 10-bit D flip-flop with TRI-STATE outputs arranged in a broadside pinout.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

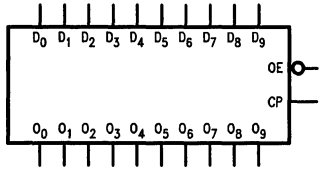
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

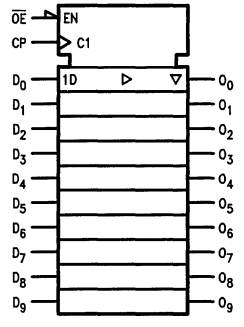
- NSC 54FCT/74FCT821A/B is pin and functionally equivalent to IDT 54FCT/74FCT821A/B
- High-speed parallel registers with positive edge-triggered D-type flip-flops for ringing suppression
- Buffered common clock enable ($\overline{EN}$) and asynchronous clear input ($\overline{CLR}$)
- Input clamp diodes for ringing suppression
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (COM), 32 mA (MIL)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883
- TRI-STATE outputs for bus interfacing
- Noninverting outputs

Logic Symbols



TL/F/10677–1

IEEE/IEC

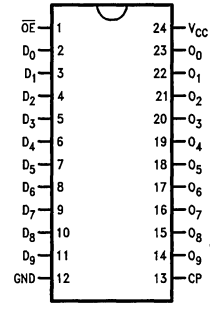


TL/F/10677–2

Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	Data Outputs
$\overline{OE}$	Output Enable Input
CP	Clock Input

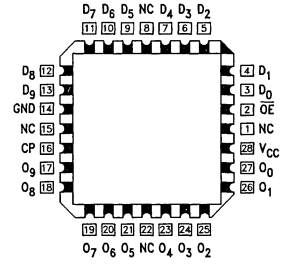
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10677–3

Pin Assignment for LCC



TL/F/10677–4

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT823A • 54FCT/74FCT823B
9-Bit D Flip-Flop

General Description

The 'FCT823A/B is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

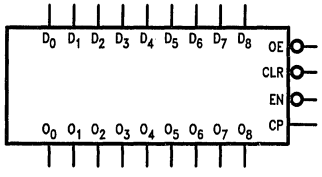
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT823A/B is pin and functionally equivalent to IDT 54FCT/74ACT823A/B
- High speed parallel registers with positive edge-triggered D-type flip-flop
- Buffered common clock enable ($\overline{EN}$) and asynchronous clear input (CLR)
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD 883

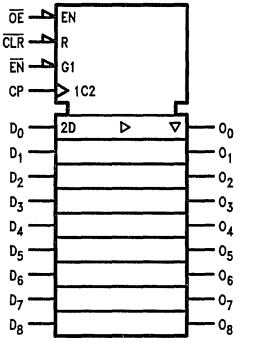
Logic Symbols



TL/F/10678–1

Pin Names	Description
D_0–D_8	Data Inputs
O_0–O_8	Data Outputs
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

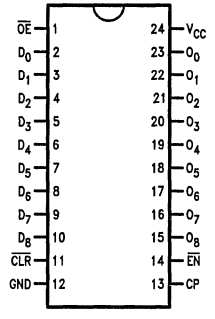
IEEE/IEC



TL/F/10678–2

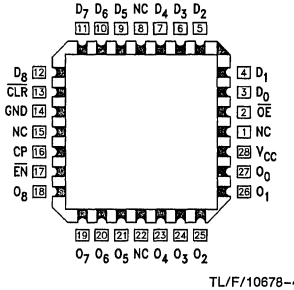
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10678–3

Pin Assignment for LCC



TL/F/10678–4

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT825A • 54FCT/74FCT825B
8-Bit D Flip-Flop

General Description

The 'FCT825A/B is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multiuse control of the interface.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

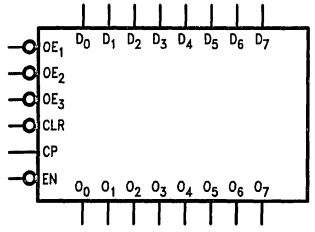
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

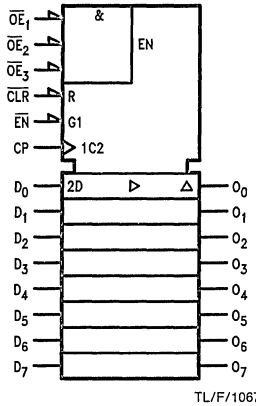
- NSC 54FCT/74FCT825A/B is pin and functionally equivalent to IDT 54FCT/74FCT825A/B
- High-speed parallel registers with positive edge-triggered D-type flip flops
- Buffered common clock enable ($\overline{EN}$) and asynchronous Clear input ($\overline{CLR}$)
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



TL/F/10679–1

IEEE/IEC

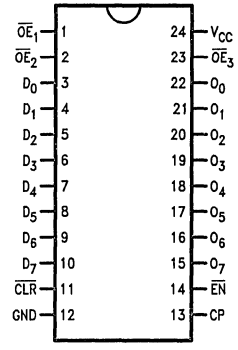


TL/F/10679–2

Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output Enables
$\overline{EN}$	Clock Enable
$\overline{CLR}$	Clear
CP	Clock Input

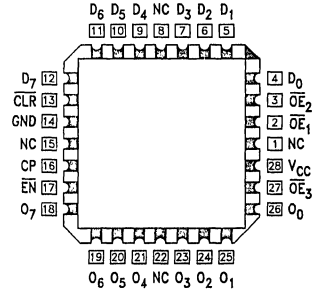
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10679–3

Pin Assignment for LCC



TL/F/10679–4

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT827A • 54FCT/74FCT827B 10-Bit Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'FCT827A/B 10-bit bus buffer provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

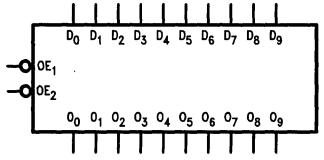
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

- NSC 54FCT/74FCT827A/B is pin and functionally equivalent to IDT 54FCT/74FCT827A/B
- High Speed parallel registers with positive edge-triggered D-type flip-flops
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

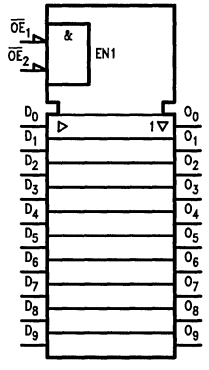
Logic Symbols



TL/F/10680–1

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs

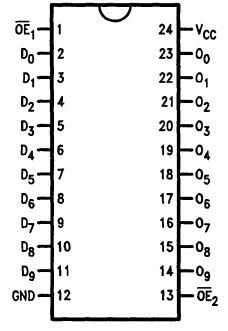
IEEE/IEC



TL/F/10680–2

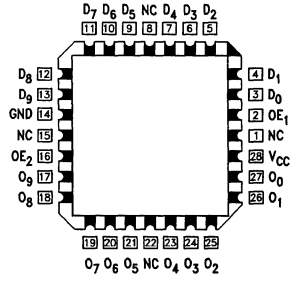
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10680–3

Pin Assignment for LCC



TL/F/10680–4

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT841A•54FCT/74FCT841B
10-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'FCT841A/B is a 10-bit transparent latch, a 10-bit version of the FCT373A.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

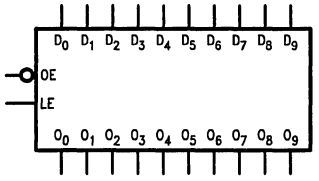
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

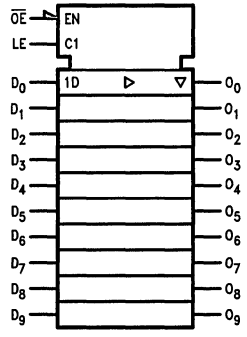
Features

- NSC 54FCT/74FCT841A/B is pin and functionally equivalent to IDT 54FCT/74FCT841A/B
- High Speed parallel latches
- Buffered common latch enable, clear and preset input
- Input clamp diodes to limit bus reflections
- TIL/CMOS input and output level compatible
- I_{OL} = 48 mA (com), 32 mA (mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



TL/F/10681–1

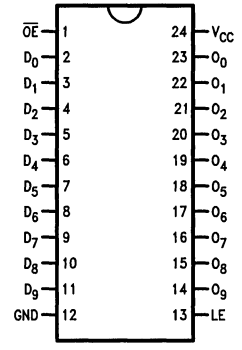


TL/F/10681–2

Pin Names	Description
D_0–D_9	Data Inputs
O_0–O_9	TRI-STATE Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable

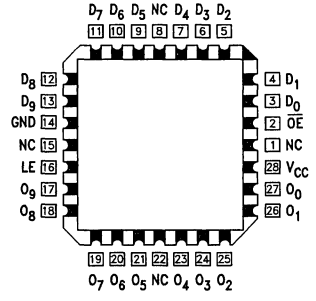
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10681–3

Pin Assignment for LCC



TL/F/10681–4

7

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT843A • 54FCT/74FCT843B
9-Bit Transparent Latch

General Description

The 'FCT843A/B bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

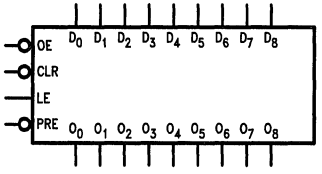
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

Features

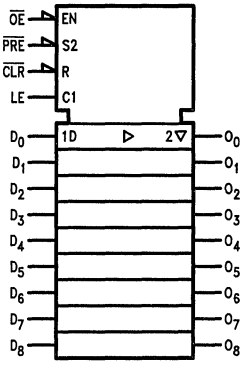
- NSC 54FCT/74FCT843A/B is pin and functionally equivalent to IDT 54FCT/74FCT843A/B
- High Speed parallel latches
- Buffered common latch enable, clear and preset inputs
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Logic Symbols



TL/F/10682–1

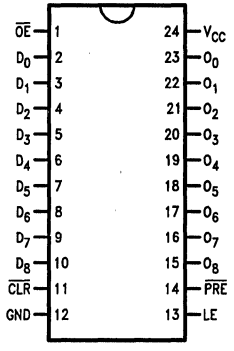
Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset



TL/F/10682–4

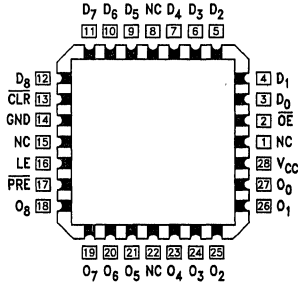
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10682–2

Pin Assignment for LCC



TL/F/10682–3

National Semiconductor

ADVANCE INFORMATION

54FCT/74FCT845A • 54FCT/74FCT845B
8-Bit Transparent Latch with TRI-STATE® Outputs

General Description

The 'FCT845A/B bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple $\overline{OE}$ controls.

FACT™ FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

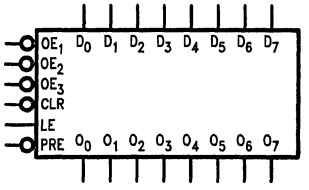
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

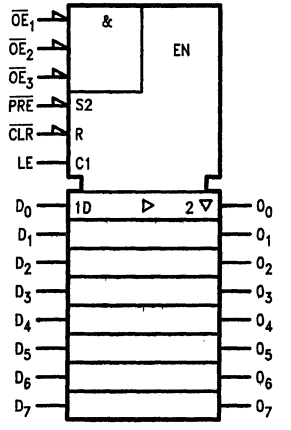
Features

- NSC 54FCT/74FCT845A/B is pin and functionally equivalent to IDT 54FCT/74FCT845A/B
- High speed parallel latches
- Buffered common latch enable, clear and preset input
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I_{OL} = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD 883

Logic Symbols



TL/F/10683–1

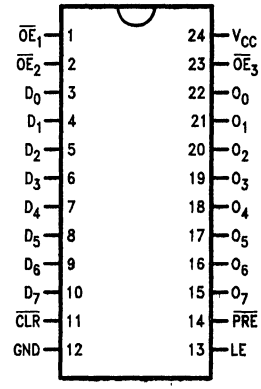


TL/F/10683–2

Pin Names	Description
D_0–D_7	Data Inputs
O_0–O_7	Data Outputs
$\overline{OE}_1$–$\overline{OE}_3$	Output Enables
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

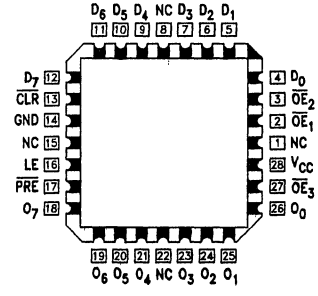
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/10683–3

Pin Assignment for LCC



TL/F/10683–4

7

National Semiconductor

54FCT/74FCT899A
9-Bit Latchable Transceiver with Parity Generator/Checker

General Description

The 'FCT899A is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. It has a guaranteed current sinking capability of 24 mA at the A-bus and 64 mA at the B-bus.

The 'FCT899A features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/$\overline{\text{EVEN}}$ parity, and separate error signal output pins for checking parity.

FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

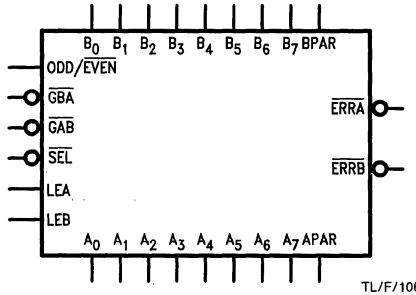
FACT FCTA features undershoot correction and split ground bus for superior performance.

Features

- Latchable transceiver with output sink of 24 mA at the A-bus and 64 mA at the B-bus
- Option to select generate parity and check or "feed-through" data/parity in directions A-to-B or B-to-A
- Independent latch enables for A-to-B and B-to-A directions
- Select pin for ODD/$\overline{\text{EVEN}}$ parity
- $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ output pins for parity checking
- Ability to simultaneously generate and check parity
- CMOS power levels
- Guaranteed 4000V min ESD protection

Ordering Code: See Section 8

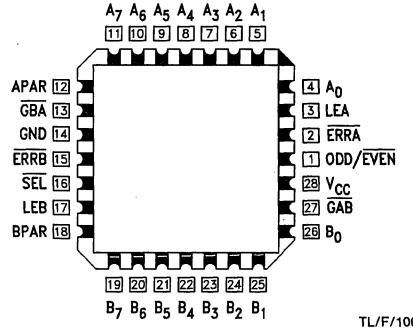
Logic Symbol



TL/F/10693–1

Connection Diagram

Pin Assignment for PCC



TL/F/10693–2

Pin Names	Description
A_0–A_7	A Bus Data Inputs/Data Outputs
B_0–B_7	B Bus Data Inputs/Data Outputs
APAR, BPAR	A and B Bus Parity Inputs
ODD/$\overline{\text{EVEN}}$	ODD/$\overline{\text{EVEN}}$ Parity Select, Active LOW for EVEN Parity
$\overline{\text{GBA}}$, $\overline{\text{GAB}}$	Output Enables for A or B Bus, Active LOW
$\overline{\text{SEL}}$	Select Pin for Feed-Through or Generate Mode, LOW for Generate Mode
LEA, LEB	Latch Enables for A and B Latches, HIGH for Transparent Mode
$\overline{\text{ERRA}}$, $\overline{\text{ERRB}}$	Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs

Functional Description

The 'FCT899A has three principal modes of operation which are outlined below. These modes apply to both the A-to-B and B-to-A directions.

— Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select ($\overline{\text{SEL}}$) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by $\overline{\text{ERRB}}$ ($\overline{\text{ERRA}}$).

— Bus A (B) communicates to Bus B (A) in a feed-through mode if $\overline{\text{SEL}}$ is HIGH. Parity is still generated and checked as $\overline{\text{ERRA}}$ and $\overline{\text{ERRB}}$ in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).

— Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table below).

Function Table

Inputs					Operation
$\overline{\text{GAB}}$	$\overline{\text{GBA}}$	$\overline{\text{SEL}}$	LEA	LEB	
H	H	X	X	X	Busses A and B are TRI-STATE®.
H	L	L	L	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$ (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	L	H	H	Generates parity from B[0:7] based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
H	L	L	X	L	Generates parity from B latch data based on O/$\overline{\text{E}}$. Generated parity → APAR. Generated parity checked against latched BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	X	H	BPAR/B[0:7] → APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$.
H	L	H	H	H	BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as $\overline{\text{ERRB}}$. Generated parity also fed back through the A latch for generate/check as $\overline{\text{ERRA}}$.
L	H	L	H	L	Generates parity for A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	L	H	H	Generates parity from A[0:7] based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.
L	H	L	L	X	Generates parity from A latch data based on O/$\overline{\text{E}}$. Generated parity → BPAR. Generated parity checked against latched APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	L	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$.
L	H	H	H	H	APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as $\overline{\text{ERRA}}$. Generated parity also fed back through the B latch for generate/check as $\overline{\text{ERRB}}$.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Note 1: O/$\overline{\text{E}}$ = ODD/$\overline{\text{EVEN}}$

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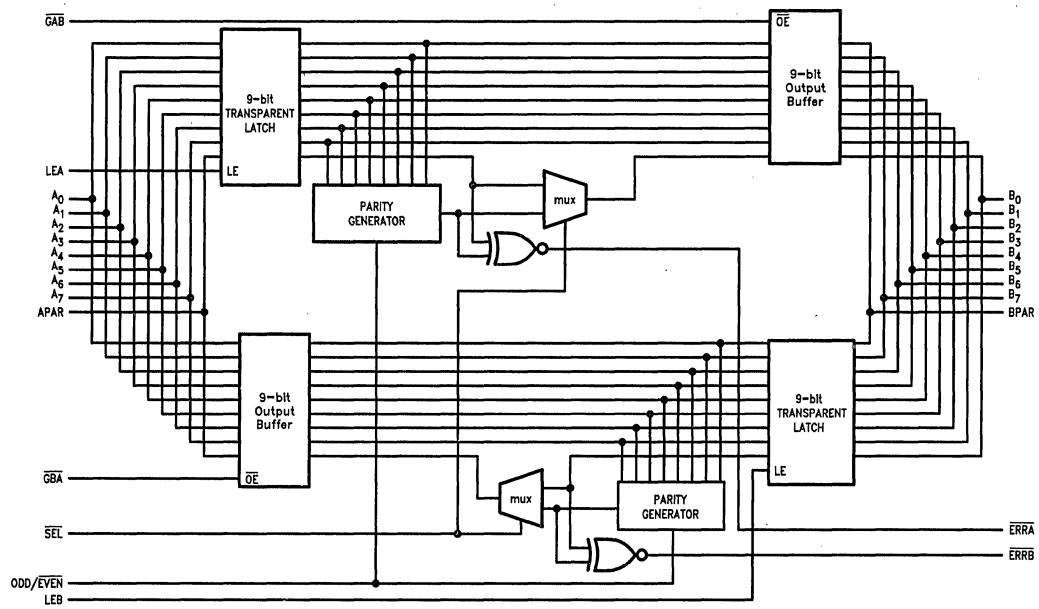
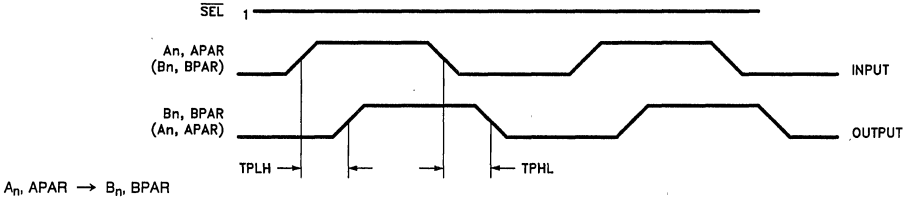
Functional Block Diagram



TL/F/10693–3

AC Path

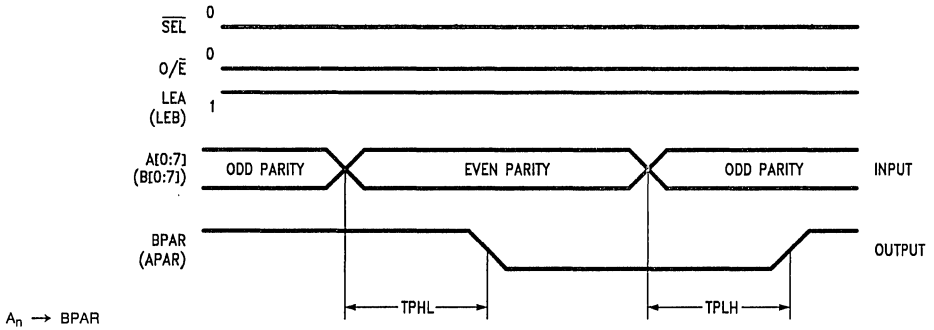


A_n, APAR → B_n, BPAR
(B_n, BPAR → A_n, APAR)

TL/F/10693–4

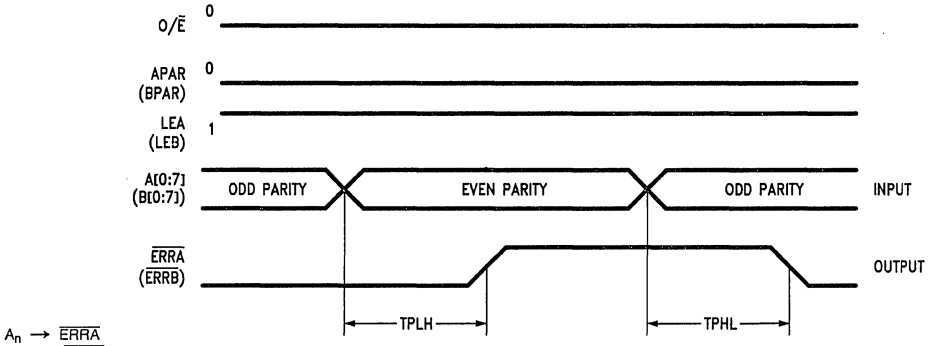
FIGURE 1

AC Path (Continued)



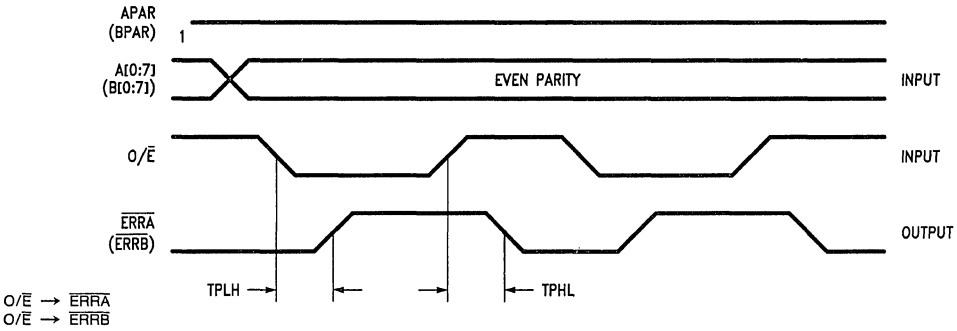
TL/F/10693–5

FIGURE 2



TL/F/10693–6

FIGURE 3



TL/F/10693–7

FIGURE 4

AC Path (Continued)

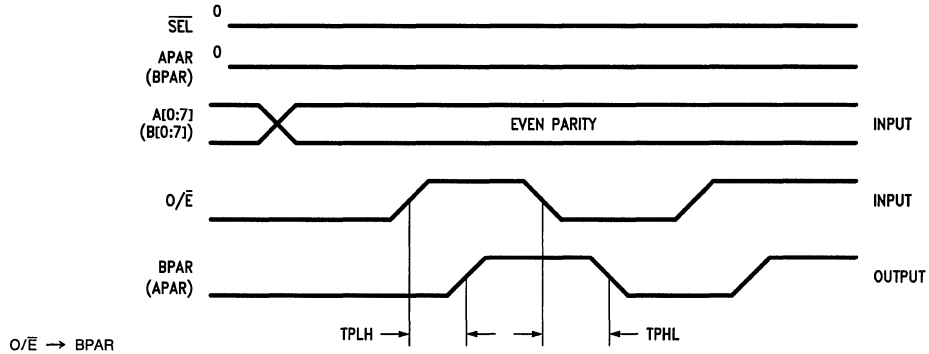


FIGURE 5

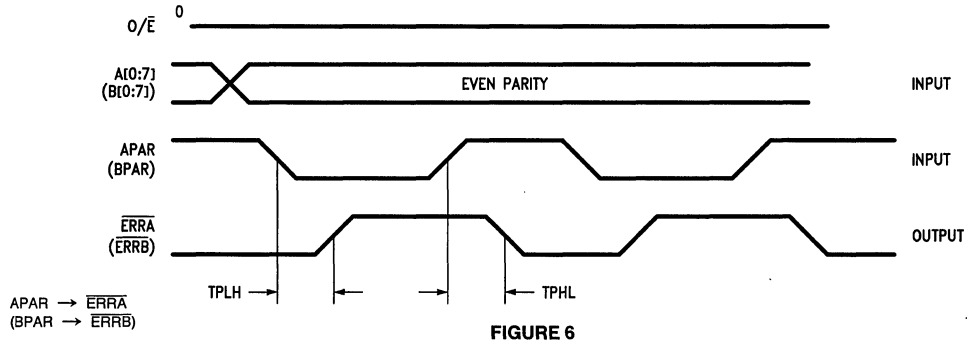


FIGURE 6

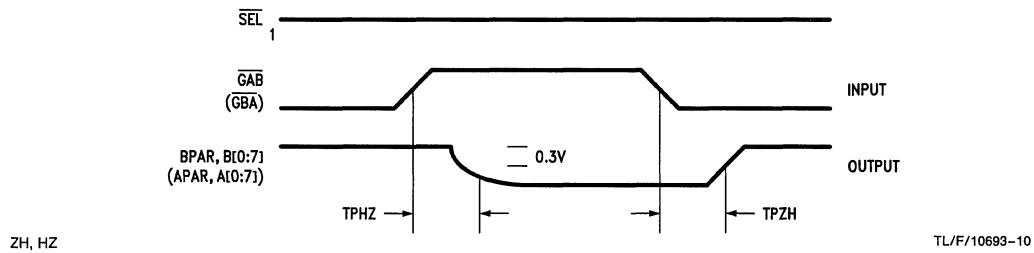
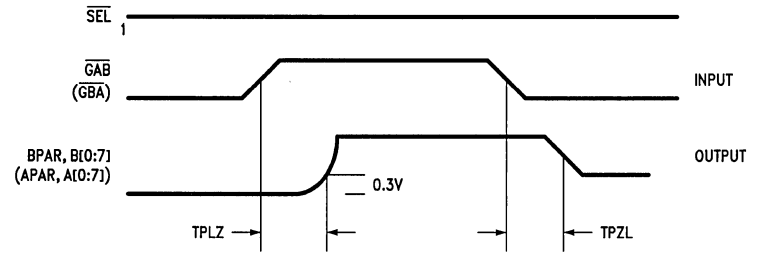


FIGURE 7

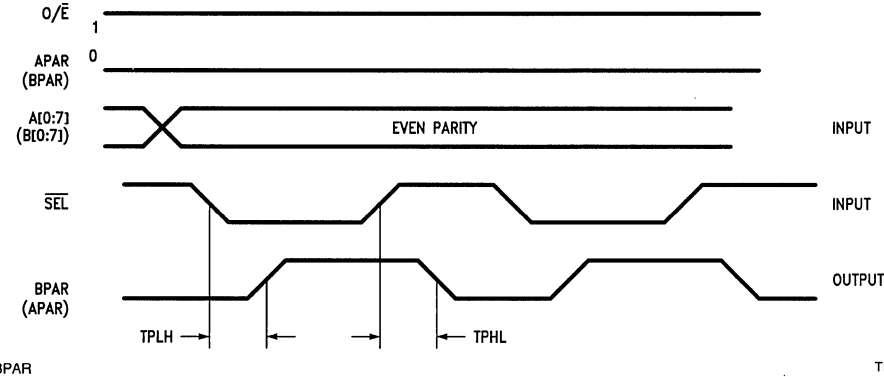
AC Path (Continued)



ZL, LZ

TL/F/10693–11

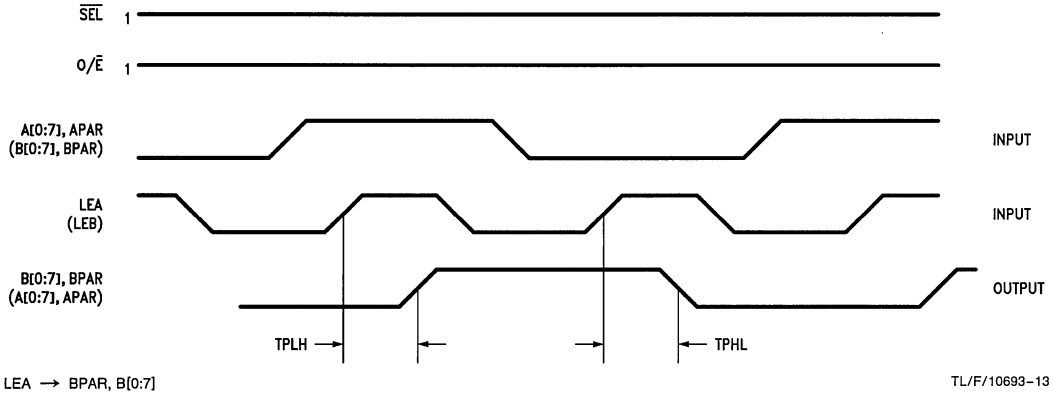
FIGURE 8



SEL → BPAR
(SEL → APAR)

TL/F/10693–12

FIGURE 9

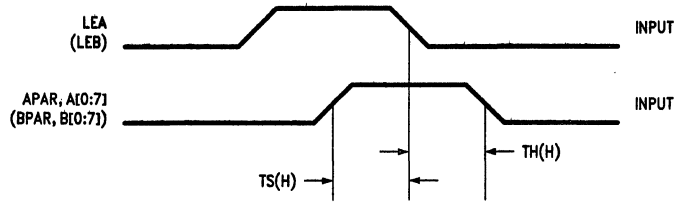


LEA → BPAR, B[0:7]
(LEB → APAR, A[0:7])

TL/F/10693–13

FIGURE 10

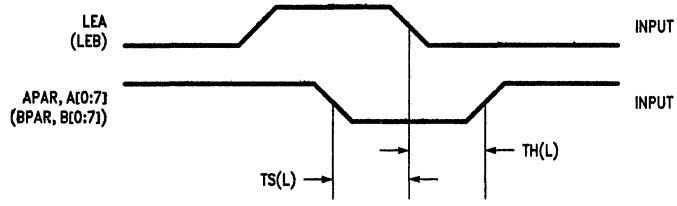
AC Path (Continued)



TS(H), TH(H)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

TL/F/10693–14

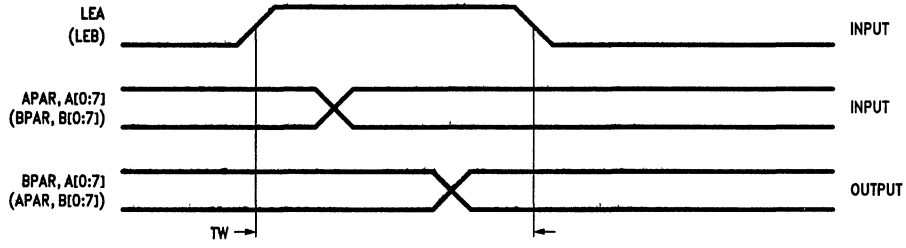
FIGURE 11



TS(L), TH(L)
LEA → APAR, A[0:7]
(LEB → BPAR, B[0:7])

TL/F/10693–15

FIGURE 12



TL/F/10693–16

FIGURE 13

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V_{TERM})
- 54FCTA: −0.5V to +7.0V
- 74FCTA: −0.5V to +7.0V

Temperature under Bias (T_{BIAS})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +135°C

Storage Temperature (T_{STG})
- 74FCTA: −55°C to +125°C
- 54FCTA: −65°C to +150°C

Power Dissipation (P_T): 0.5W

DC Output Current (I_{OUT}): 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

Supply Voltage (V_{CC})
- 54FCTA: 4.5V to 5.5V
- 74FCTA: 4.75V to 5.25V

Input Voltage: 0V to V_{CC}

Output Voltage: 0V to V_{CC}

Operating Temperature (T_A)
- 54FCTA: −55°C to +125°C
- 74FCTA: −0°C to +70°C

Junction Temperature (T_J)
- CDIP: 175°C
- PDIP: 140°C

DC Characteristics for 'FCTA Family Devices

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} 5.0V ±10% T_A = −55°C to +125°C, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	54FCTA/74FCTA Min	Typ	Max	Units	Conditions	
V_{IH}	Minimum High Level Input Voltage	2.0			V		
V_{IL}	Maximum Low Level Input Voltage			0.8	V		
I_{IH}	Input High Current			5.0 5.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2)
I_{IL}	Input Low Current			−5.0 −5.0	μA	V_{CC} = Max	V_I = 0.5V (Note 2) V_I = GND
I_{OZ}	Maximum TRI-STATE Current			10.0 10.0 −10.0 −10.0	μA	V_{CC} = Max	$V_I = V_{CC}$ V_I = 2.7V (Note 2) V_I = 0.5V (Note 2) V_I = GND
V_{IK}	Clamp Diode Voltage		−0.7	−1.2	V	V_{CC} = Min; I_N = −18 mA	
I_{OS}	Short Circuit Current	−60	−120		mA	V_{CC} = Max (Note 1); V_O = GND	
V_{OH}	Minimum High Level Output Voltage	2.8 V_{HC} 2.4 2.4	3.0 V_{CC} 4.3 4.3		V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OH} = −32 μA V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	 I_{OH} = −300 μA I_{OH} = −12 mA (Mil) I_{OH} = −15 mA (Com)
V_{OL}	Maximum Low Level Output Voltage		GND GND 0.3 0.3	0.2 0.2 0.55 0.55	V	V_{CC} = 3V; V_{IN} = 0.2V or V_{HC}; I_{OL} = 300 μA V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	 I_{OL} = 300 μA I_{OL} = 48 mA (Mil) I_{OL} = 64 mA (Com)
I_{CC}	Maximum Quiescent Supply Current		0.001	1.5	mA	V_{CC} = Max $V_{IN} \geq V_{HC}$, $V_{IN} \leq 0.2V$ $f_I = 0$	
ΔI_{CC}	Quiescent Supply Current; TTL Inputs HIGH		0.5	2.0	mA	V_{CC} = Max V_{IN} = 3.4V (Note 3)	

DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C; Mil: V_{CC} = 5.0V ±10% T_A = −55°C to +125°C, V_{HC} = V_{CC} −0.2V (Continued)

Symbol	Parameter	54FCTA/74FCTA			Units	Conditions	
		Min	Typ	Max			
I_{CCD}	Dynamic Power Supply Current (Note 4)		0.25	0.40	mA/MHz	V_{CC} = Max Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq$ 0.2V
I_C	Total Power Supply Current (Note 6)		1.5	4.0	mA	V_{CC} = Max Outputs Open f_i = 10 MHz One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq$ 0.2V
			1.8	5.0			V_{IN} = 3.4V V_{IN} = GND
			3.0	6.5		(Note 5) V_{CC} = Max Outputs Open f_i = 2.5 MHz Eight Bits Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq$ 0.2V
			5.0	14.5			V_{IN} = 3.4V V_{IN} = GND

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

Note 6: $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs High

N_T = Number of Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All Currents are in milliamps and all frequencies are in megahertz.

AC Electrical Characteristics

Symbol	Parameter	54FCTA/74FCTA	74FCTA		54FCTA		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = 5.0V$	$T_A, V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50\ pF$		$T_A, V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50\ pF$			
		Typ	Min	Max	Min	Max		
t_{PHL} t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	10.0	2.5	11.0			ns	1
t_{PHL} t_{PLH}	Propagation Delay APAR to BPAR or BPAR to APAR	11.0	1.5	8.0			ns	1
t_{PHL} t_{PLH}	Propagation Delay A to BPAR or B to APAR $\overline{SEL} = 0$	13.0	2.5	11.5			ns	2
t_{PHL} t_{PLH}	Propagation Delay A to $\overline{ERRA}$ or B to $\overline{ERRB}$	13.0	2.0	11.0			ns	3
t_{PHL} t_{PLH}	Propagation Delay ODD/$\overline{EVEN}$ to ERRA, ERRB or APAR, BPAR	13.0	2.0	11.0			ns	4, 5
t_{PHL} t_{PLH}	Propagation Delay $\overline{SEL}$ to APAR or BPAR	10.5	1.5	8.5			ns	9
t_{PHL} t_{PLH}	Propagation Delay LEA/LEB to B/A or BPAR/APAR	11.0	2.0	11.0			ns	10, 11
t_{PZL} t_{PZH}	Output Enable Delay	9.5	1.5	10.0			ns	7, 8
t_{PHZ} t_{PLZ}	Output Disable Enable	11.0	1.5	8.5			ns	7, 8
t_{SET}	Setup Time A to LEA or B to LEB	3.0	3.0				ns	11, 12
t_{HOLD}	Hold Time A to LEA, B to LEB	1.5	1.5				ns	11, 12
t_W	Pulse Width LEA or LEB	5.0	4.0				ns	13

Section 8

Ordering Information and Physical Dimensions

Section 8 Contents

National Semiconductor

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74AC/ACT XXX P C QR

Temperature Range Family
- 74AC = Commercial FACT™
- 54AC = Military FACT
- 74ACT = Commercial TTL-Compatible FACT
- 54ACT = Military TTL-Compatible FACT
- 74ACQ = Commercial Quiet Series
- 54ACQ = Military Quiet Series
- 74ACTQ = Commercial Quiet Series TTL-Compatible
- 54ACTQ = Military Quiet Series TTL-Compatible
- 74FCT = Commercial FCT TTL-Compatible
- 54FCT = Military FCT TTL-Compatible
- 74FCTXXXA = Commercial FCT A-Speed TTL-Compatible
- 54FCTXXXA = Military FCT A-Speed TTL-Compatible
- 74FCTXXXB = Commercial FCT B-Speed TTL-Compatible
- 54FCTXXXB = Military FCT B-Speed TTL-Compatible

Device Type

Package Code
- P = Plastic DIP
- SP = Slim Plastic DIP
- D = Ceramic DIP
- SD = Slim Ceramic DIP
- F = Flatpak
- L = Leadless Ceramic Chip Carrier (LCC)
- Q = Plastic Leaded Chip Carrier (PCC)
- S = Small Outline (SOIC)

Temperature Range
- C = Commercial JEDEC AC/ACQ/ACT/ACTQ (−40°C to +85°C) FCT, FCTXXXA (0°C to +70°C)
- J = Commercial EIAJ AC/ACQ/ACT/ACTQ (−40°C to +85°C)
- M = Military (−55°C to +125°C)

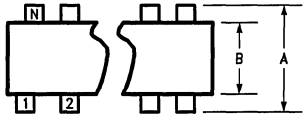
Special Variations
- X = Devices shipped in 13″ reels
- QR = Commercial grade device with burn-in
- QB = Military grade device with environmental and burn-in processing shipped in tubes

For most current packaging information, contact Product Marketing.

JEDEC-EIAJ Small Outline Package Comparison

	Dim	14 Pin		16 Pin		20 Pin		24 Pin	
		Min	Max	Min	Max	Min	Max	Min	Max
JEDEC	A	0.228 (5.80)	0.245 (6.20)	0.228 (5.80)	0.245 (6.20)	0.393 (10.0)	0.420 (10.65)	0.393 (10.0)	0.420 (10.65)
	B	0.149 (3.80)	0.158 (4.00)	0.149 (3.80)	0.158 (4.00)	0.291 (7.40)	0.300 (7.60)	0.291 (7.40)	0.300 (7.60)
EIAJ	A	0.300 (7.62)	0.350 (8.89)	0.300 (7.62)	0.350 (8.89)	0.300 (7.62)	0.350 (8.89)	0.300 (7.62)	0.350 (8.89)
	B	0.198 (5.02)	0.245 (6.22)	0.198 (5.02)	0.245 (6.22)	0.198 (5.02)	0.245 (6.22)	0.198 (5.02)	0.245 (6.22)

Units: Inch (mm)

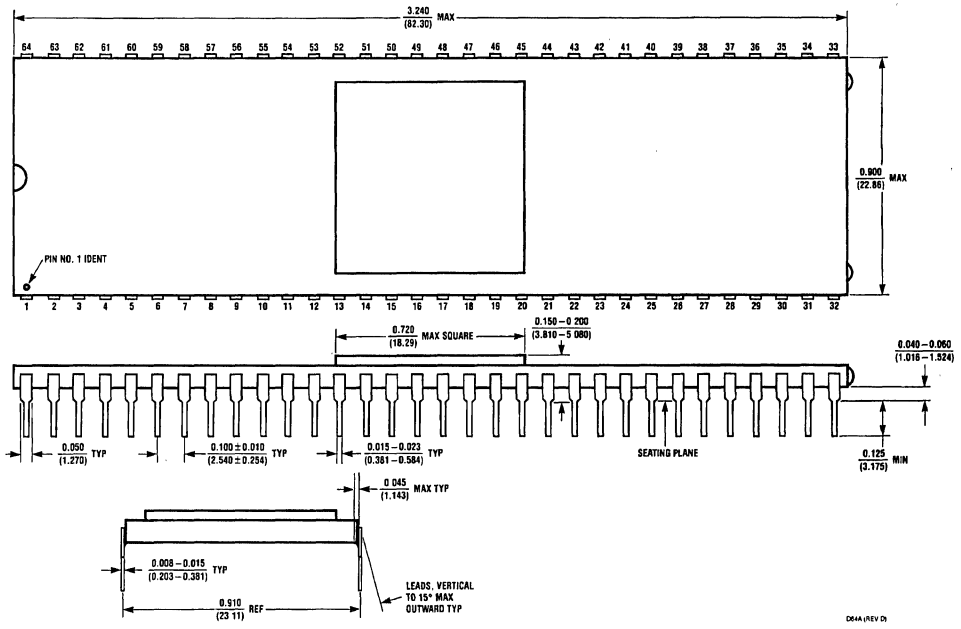


TL/F/10162–2

National Semiconductor

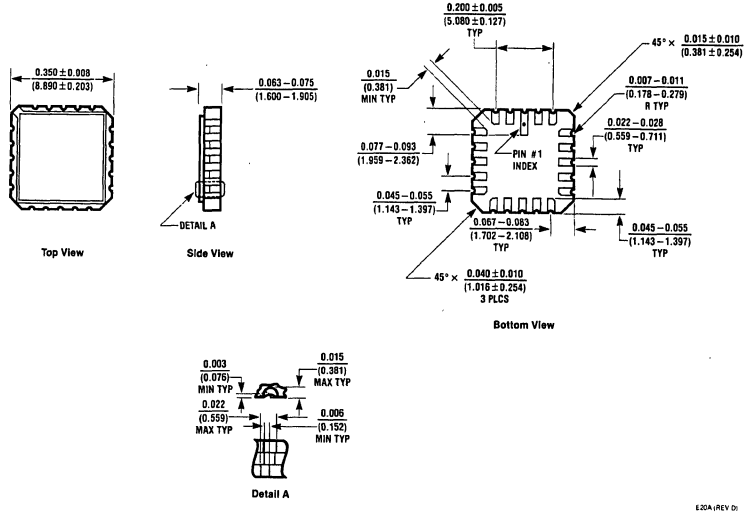
All dimensions are in inches (millimeters)

64 Lead Side Brazed Ceramic Dual-In-Line Package (D)
NS Package Number D64A

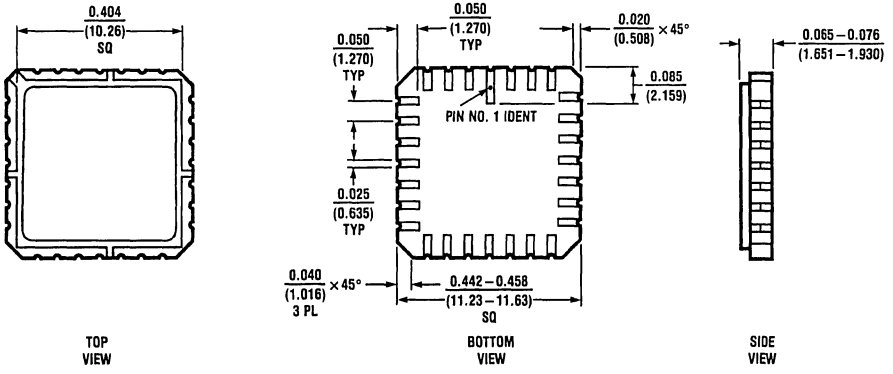


Note: FACT™ Product Shipped WITHOUT Protective Silicon "Bumpers".

20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

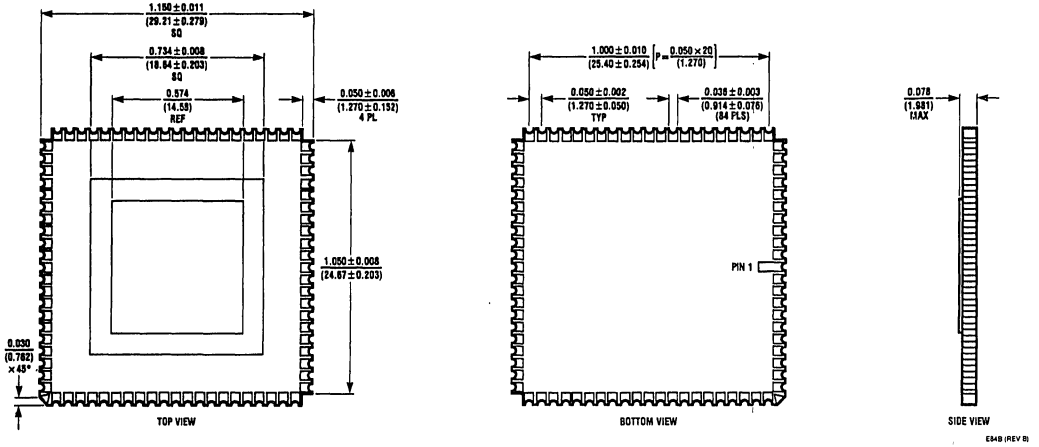


28 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



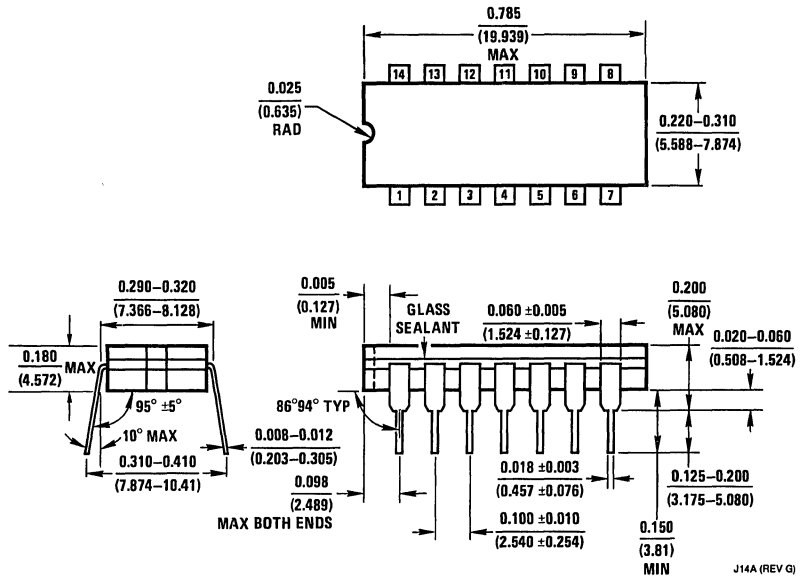
E28A (REV C)

84 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E84B

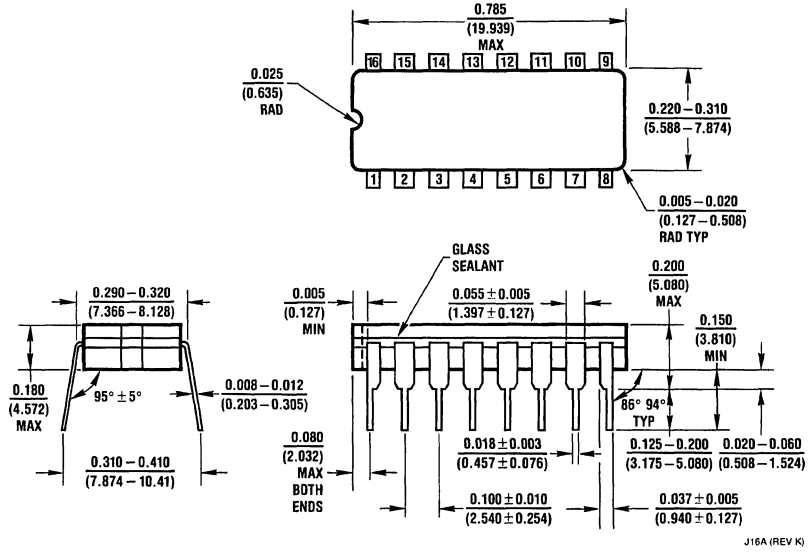


E84B (REV B)

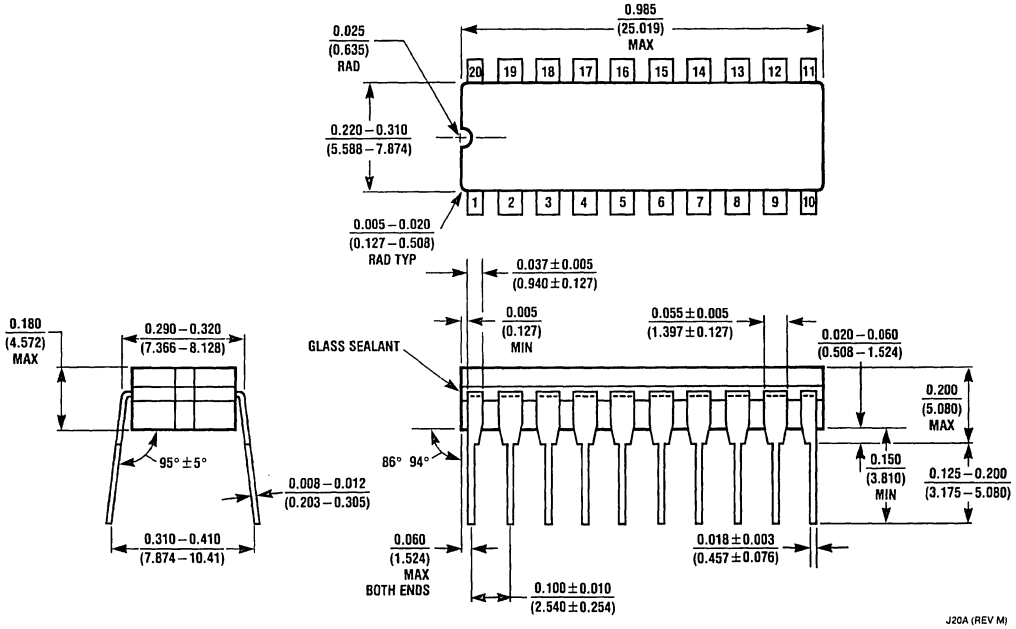
14 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J14A



16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

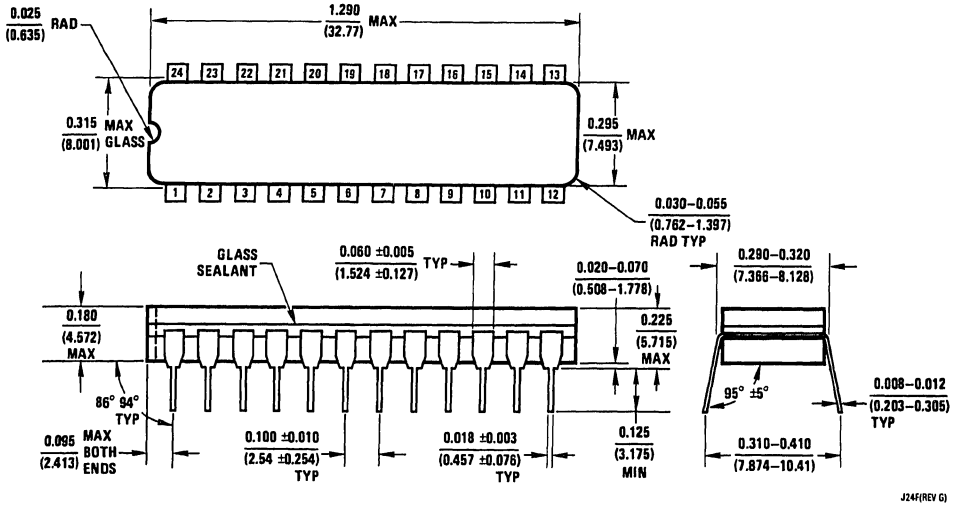


20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



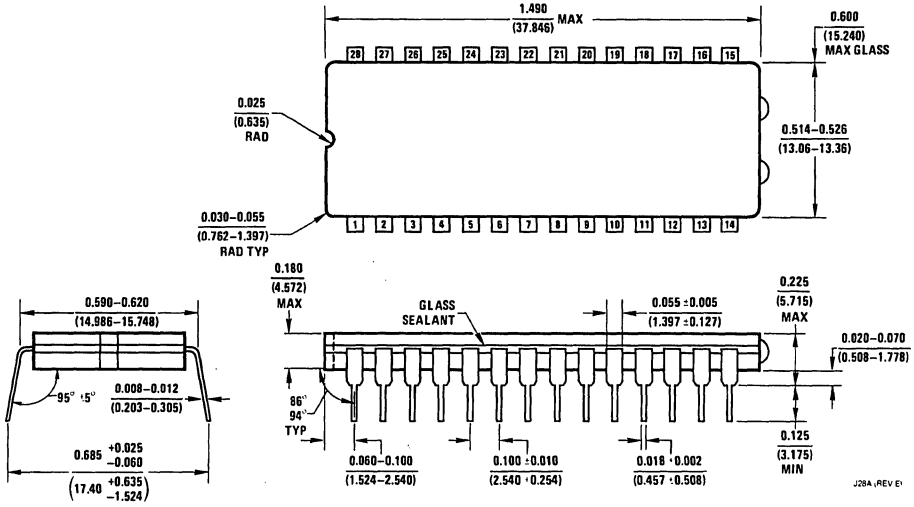
J20A (REV M)

24 Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F



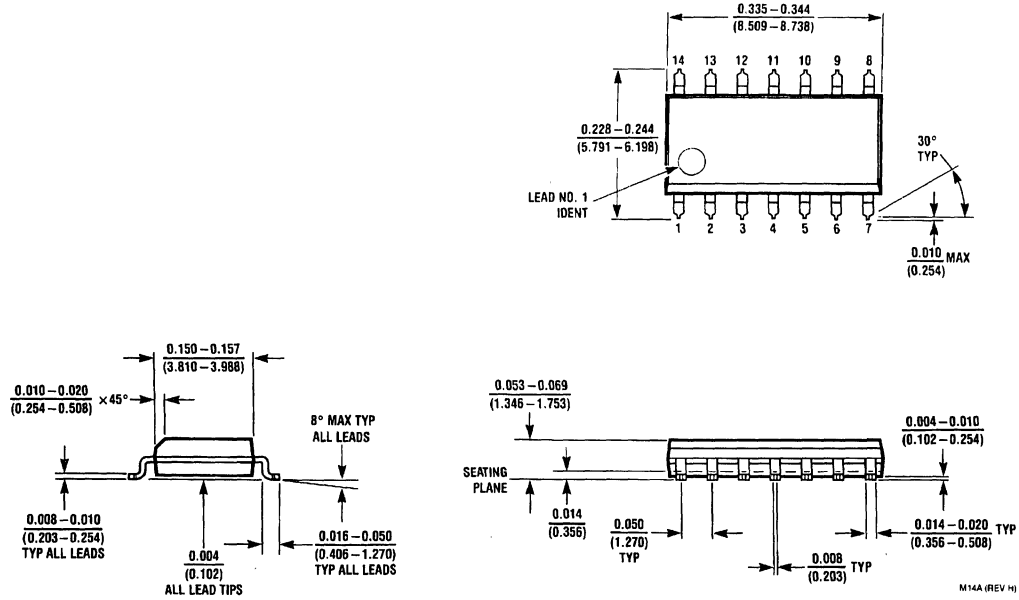
J24F(REV G)

28 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J28A

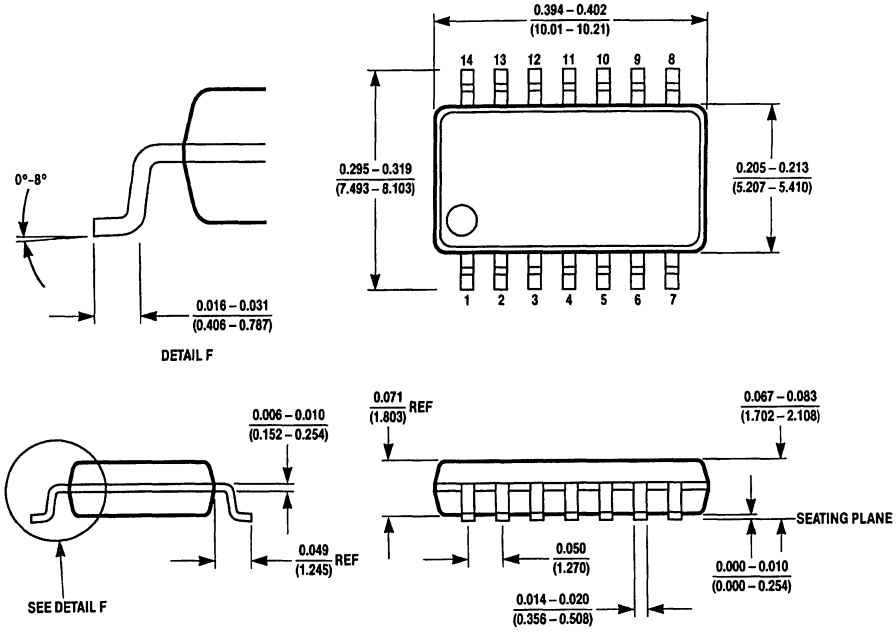


Note: FACT™ Product Shipped WITHOUT Protective Silicon "Bumpers".

14 Lead Small Outline Integrated Circuit (S)
NS Package Number M14A

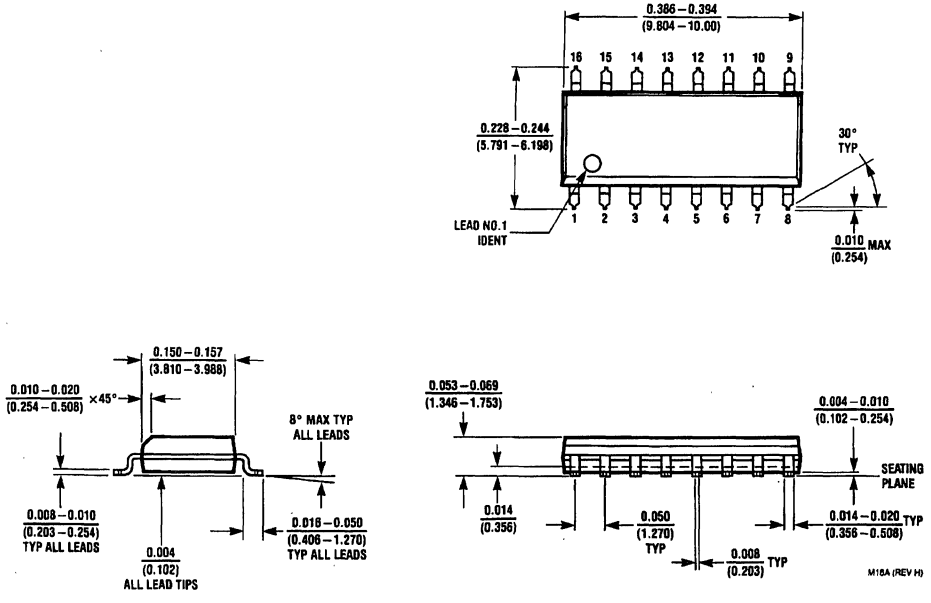


14 Lead Small Outline Package - EIAJ (SJ)
NS Package Number M14D



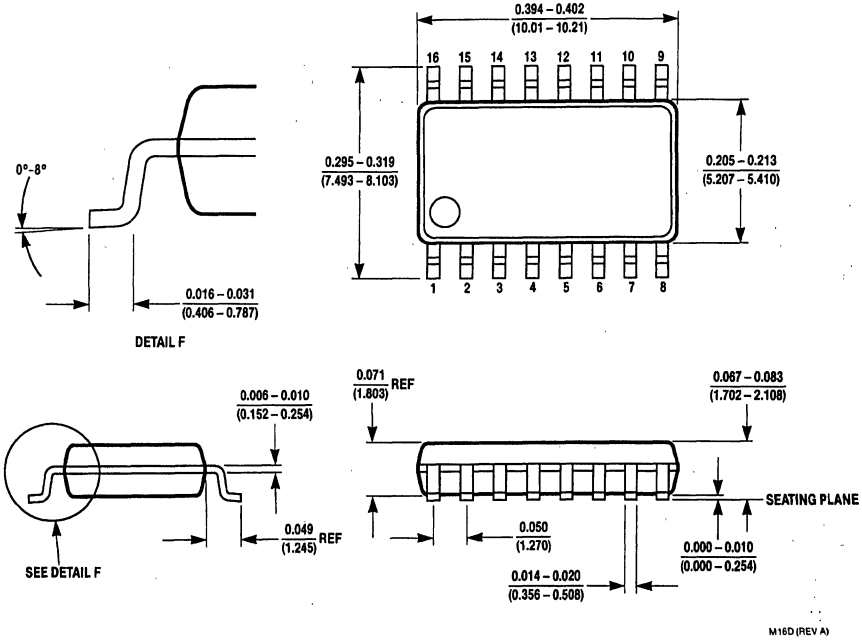
M14D (REV A)

16 Lead Small Outline Integrated Circuit (S)
NS Package Number M16A

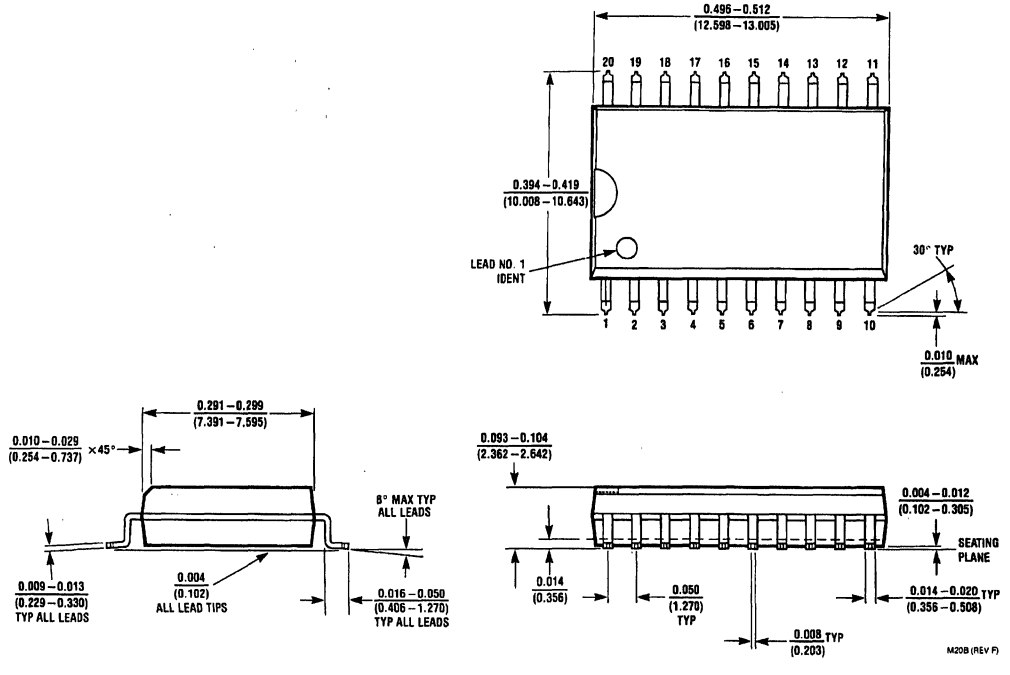


M16A (REV H)

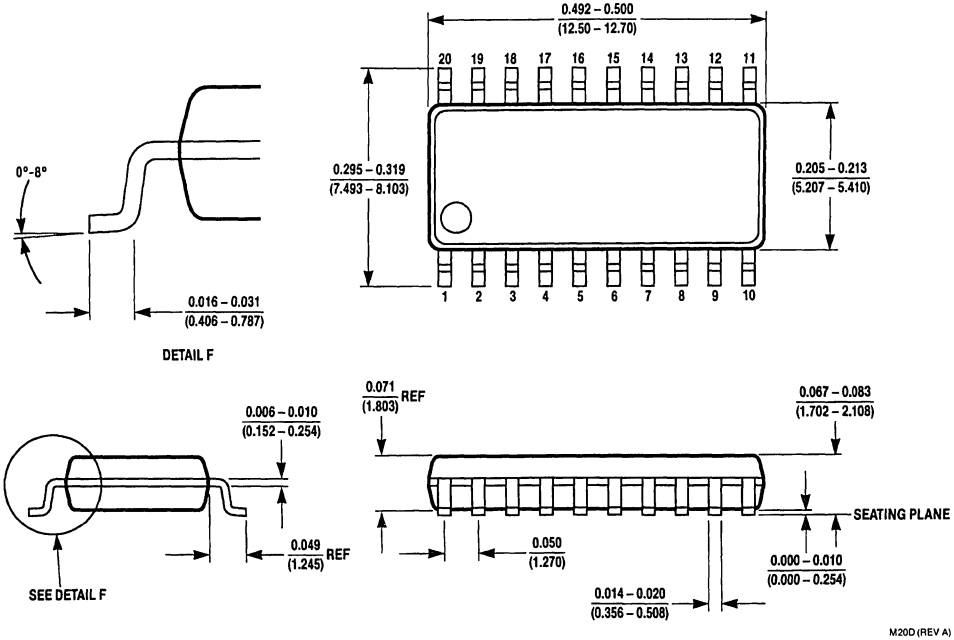
16 Lead Small Outline Package - EIAJ (SJ)
NS Package Number M16D



20 Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

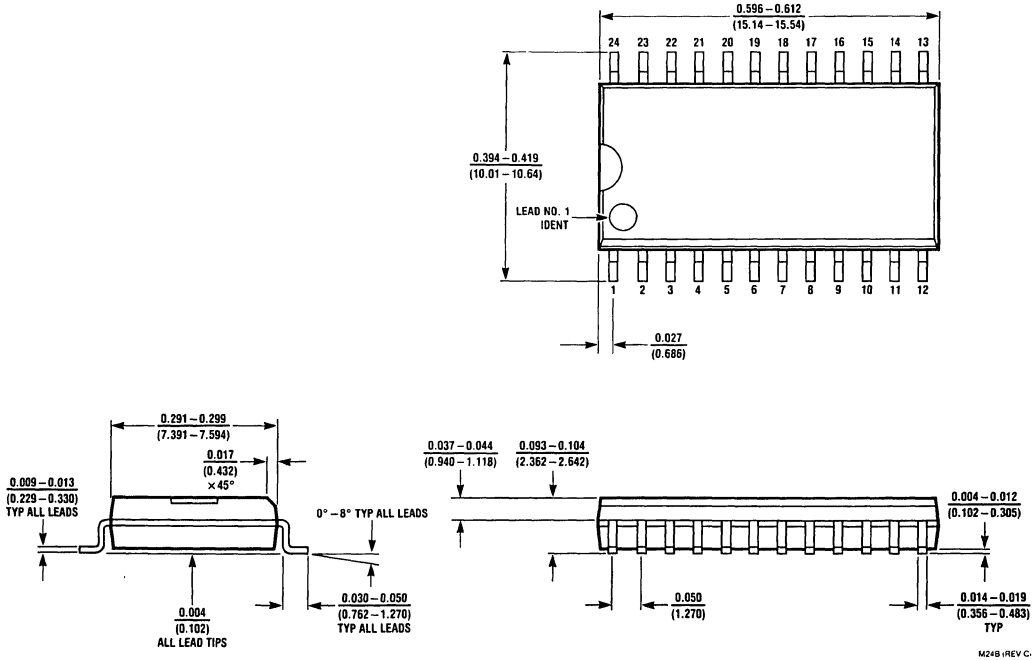


20 Lead Small Outline Package - EIAJ (SJ)
NS Package Number M20D



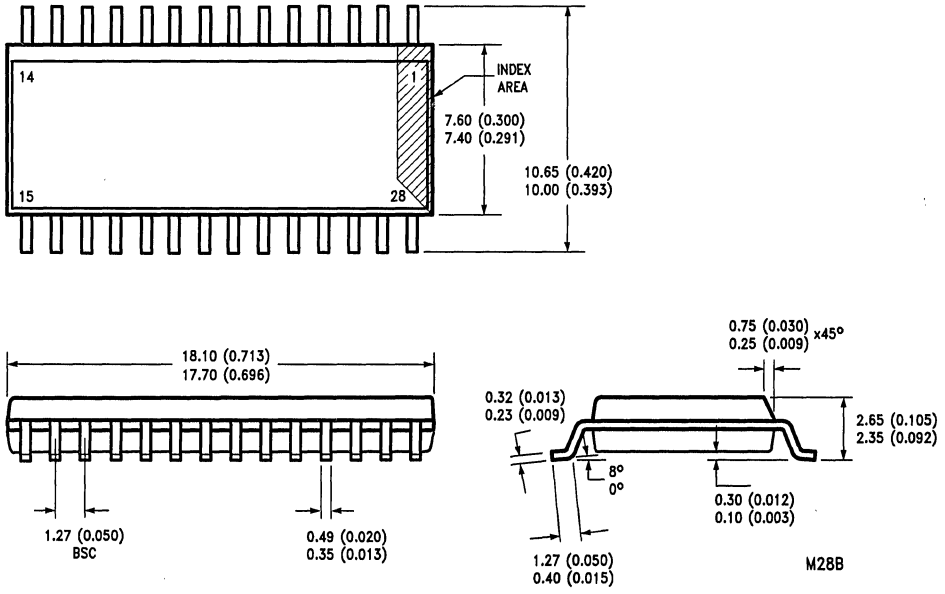
M20D (REV A)

24 Lead Small Outline Integrated Circuit (S)
NS Package Number M24B

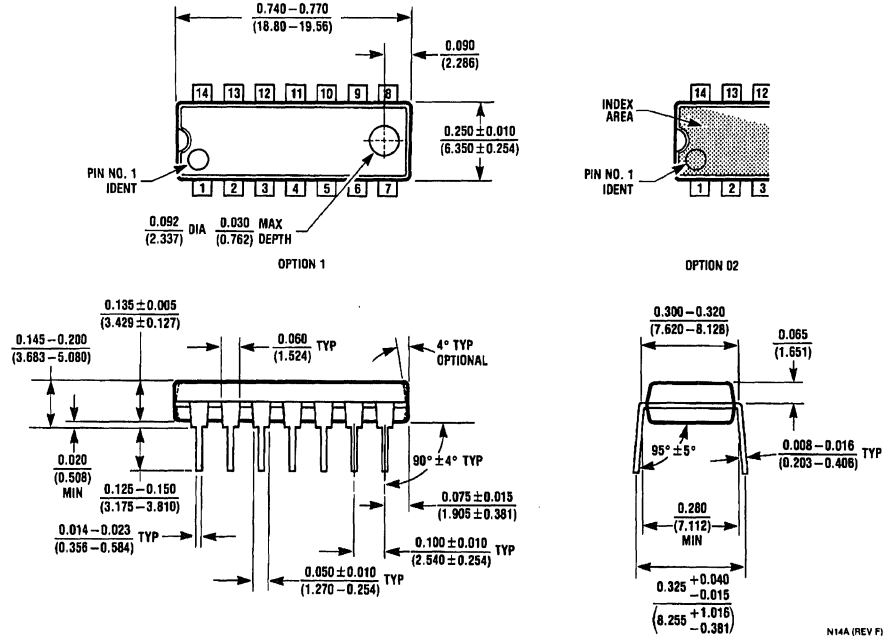


M24B (REV C)

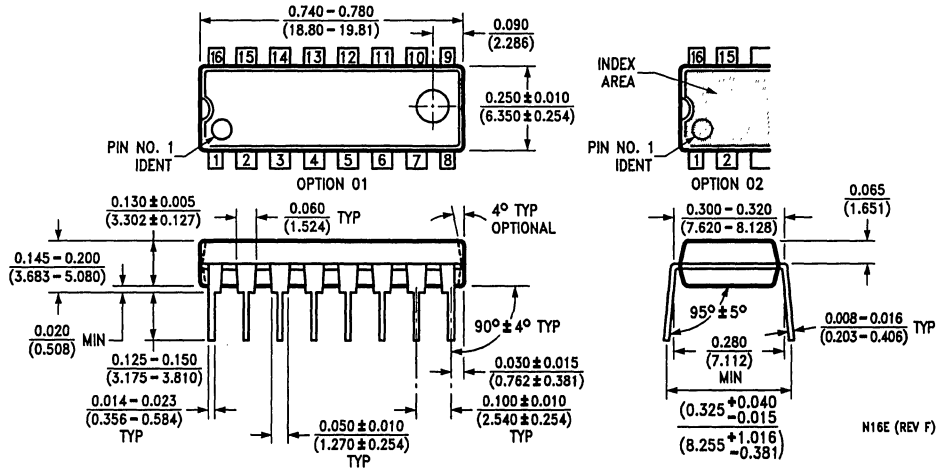
28 Lead Small Outline Integrated Circuit (S)
NS Package Number M28B



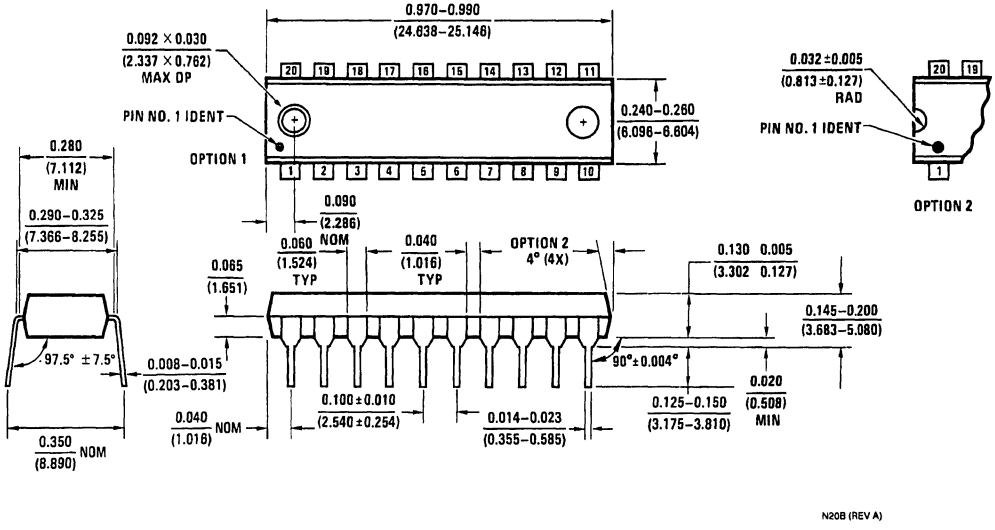
14 Lead Plastic Dual-In-Line Package (P)
NS Package Number N14A



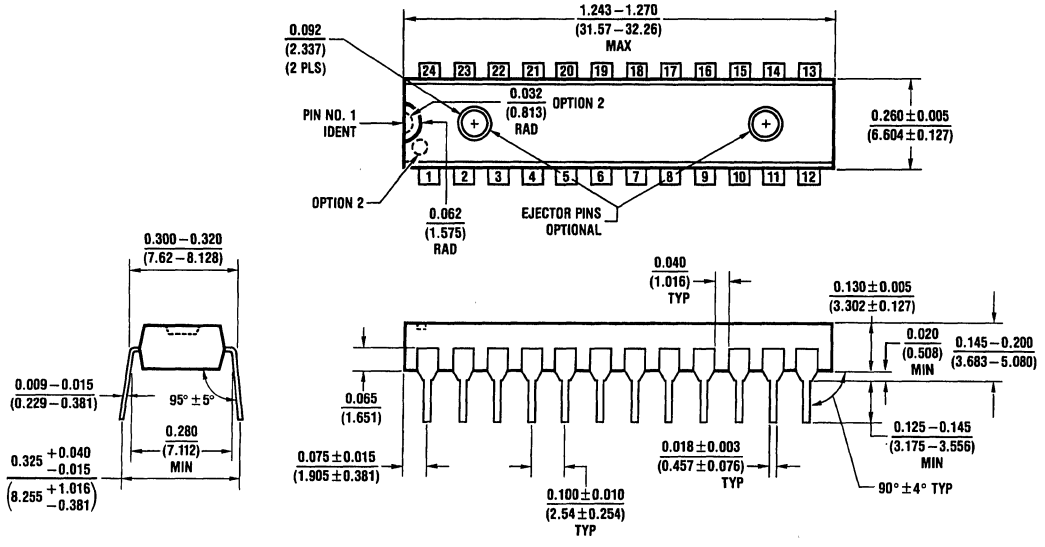
16 Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E



20 Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

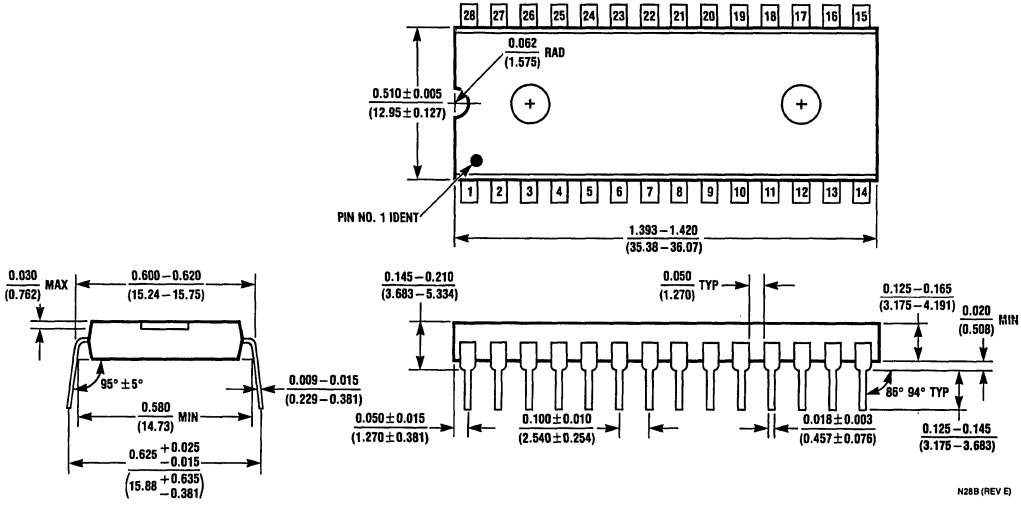


24 Lead Plastic Slim (0.300" Wide) Dual-In-Line Package (SP)
NS Package Number N24C



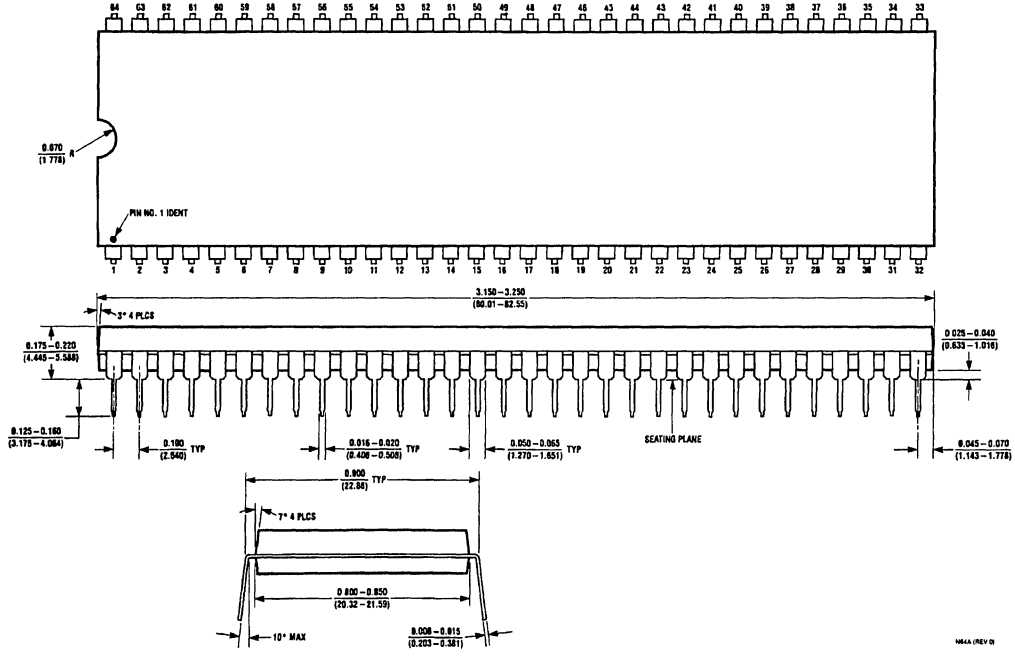
N24C (REV F)

28 Lead Plastic Dual-In-Line Package (P)
NS Package Number N28B

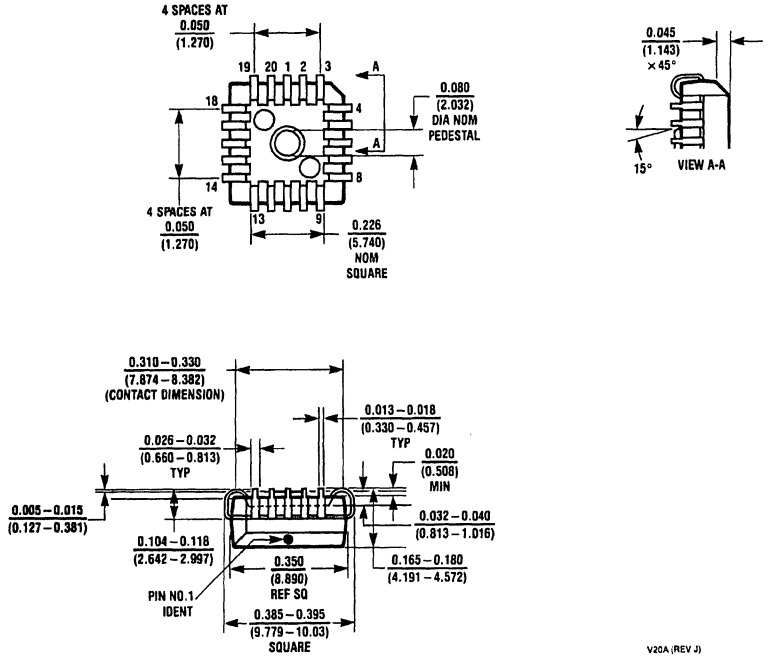


N28B (REV E)

64 Lead Plastic Dual-In-Line Package (P)
NS Package Number N64A

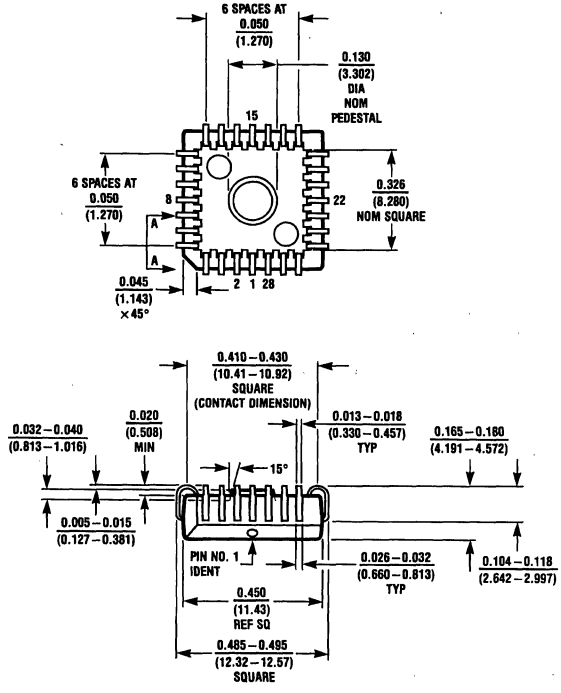


20 Lead Plastic Chip Carrier (Q)
NS Package Number V20A



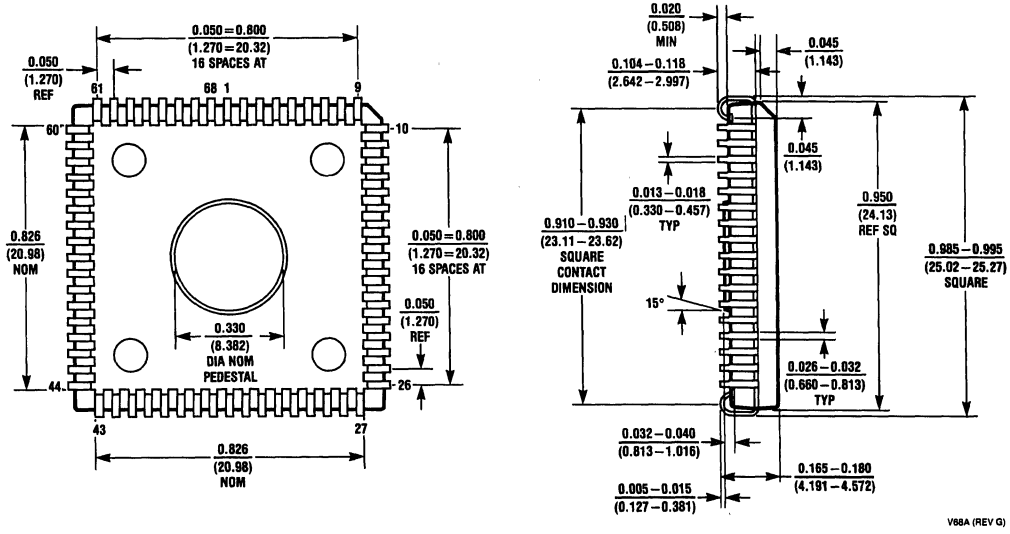
V20A (REV J)

28 Lead Plastic Chip Carrier (Q)
NS Package Number V28A



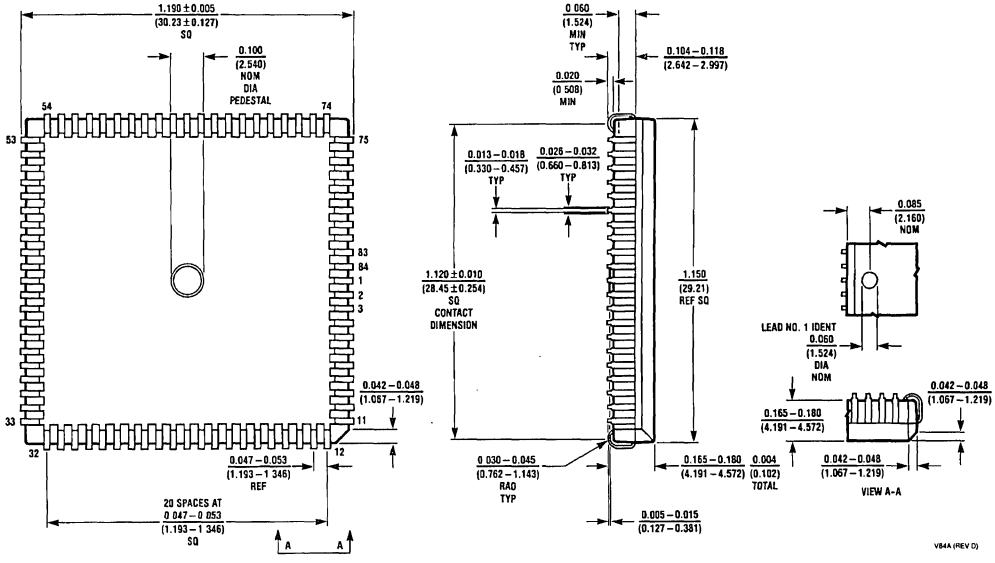
V28A (REV G)

68 Lead Plastic Chip Carrier (Q)
NS Package Number V68A

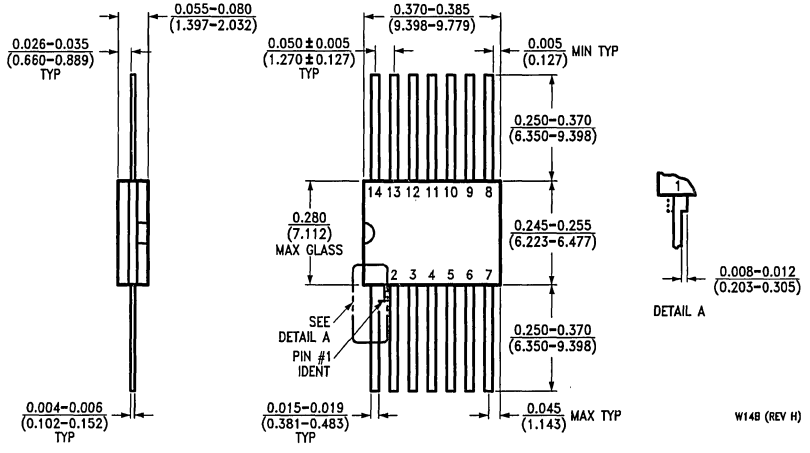


V68A (REV G)

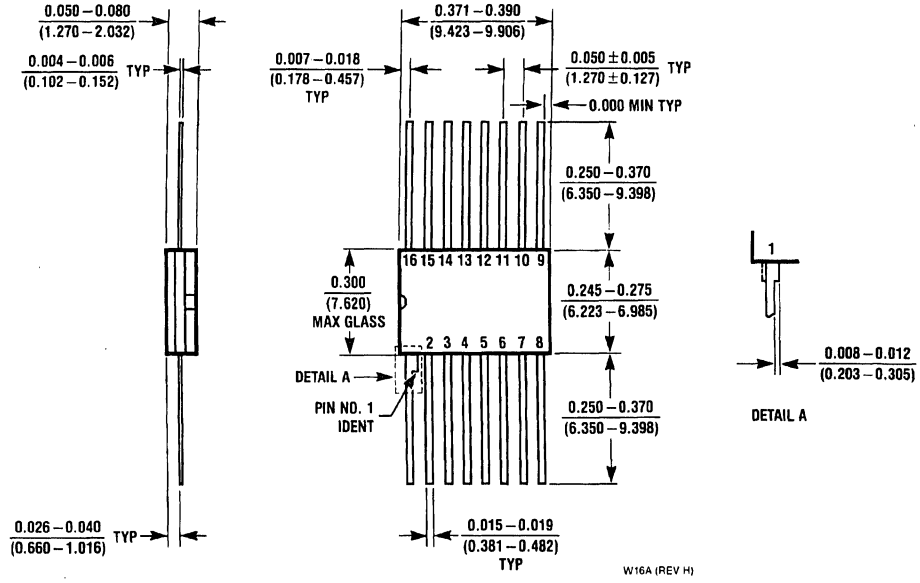
84 Lead Plastic Chip Carrier (Q)
NS Package Number V84A



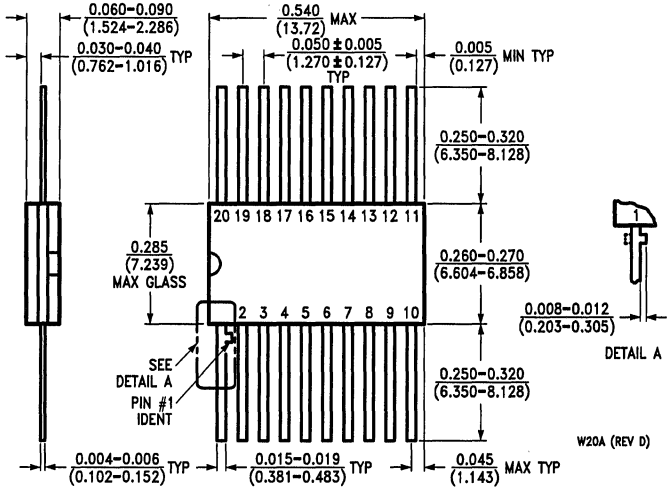
14 Lead Ceramic Flatpak (F)
NS Package Number W14B



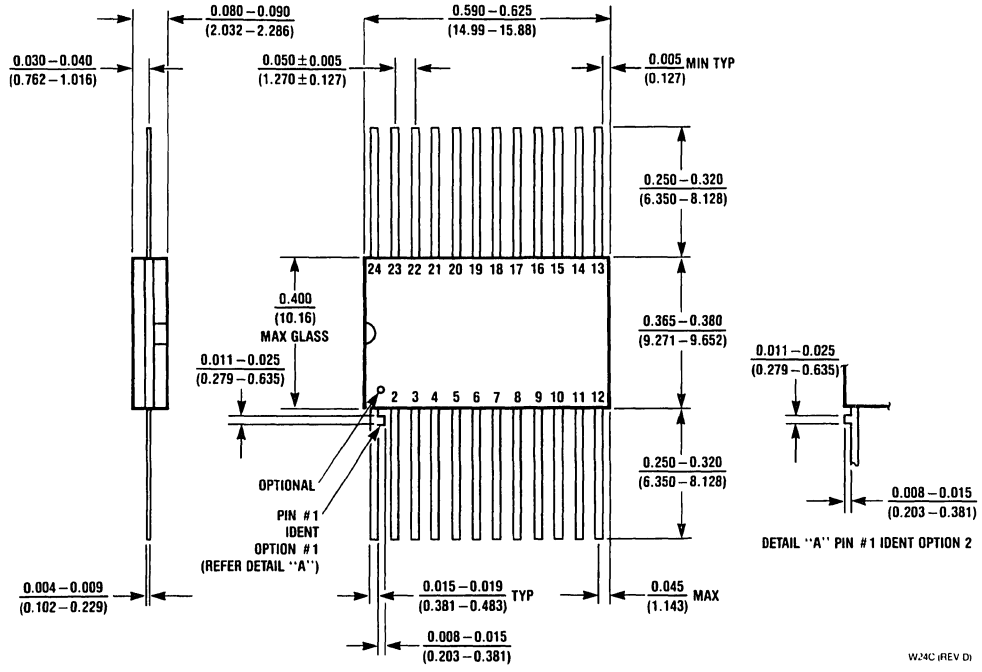
16 Lead Ceramic Flatpak (F)
NS Package Number W16A



20 Lead Ceramic Flatpak (F)
NS Package Number W20A



24 Lead Ceramic Flatpak (F)
NS Package Number W24C



NOTES

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