400043 Rev. 1

National Semiconductor Corporation

Linear Databook 3

- *Audio Circuits*
- *Radio Circuits*
- *Video Circuits*
- *Motion Control*
- *Special Functions*
- *Surface Mount*

Rev. 1

Linear 3 Databook

National Semiconductor

Linear Databook 3

1988 Edition

General Information

TRADEMARKS

Following is the most current list of National Semiconductor Corporation's trademarks and registered trademarks.

AbuseableTM
AnadigTM
ANS-R-TRANTM
APPSTM
Auto-Chem DeflasherTM
BI-FETTM
BI-FET IITM
BI-LINETM
BIPLANTM
BLCTM
BLXTM
Brite-LiteTM
BTLTM
CheckTrackTM
CIMTM
CIMBUSTM
Clock✓ChekTM
COMBOTM
COMBO ITM
COMBO IITM
COPSTM microcontrollers
Datachecker®
DENSPAKTM
DIBTM
Digitalker®
DISCERNTM
DISTILLTM
DNRTM
DPVMTM
ELSTARTM
E-Z-LINKTM
5-Star ServiceTM
GENIXTM
GNXTM
HEX 3000TM
HPCTM
ICMTM
INFOCHEXTM
Integral ISETM
IntelisplayTM
ISETM
ISE/06TM
ISE/08TM
ISE/16TM
ISE32TM
KeyScanTM
LMCMOSTM
M2CMOSTM
MacrobusTM
MacrocomponentTM
Meat✓ChekTM
MicrobusTM data bus
MICRO-DACTM
μtalkerTM
MicrotalkerTM
MICROWIRETM
MICROWIRE/PLUSTM
MOLETM
MSTTM
Naked-8TM
National®
NAX 800TM
Nitride PlusTM
Nitride Plus OxideTM
NMLTM
NOBUSTM
NSC800TM
NSX-16TM
NS-XC-16TM
NURAMTM
OXISSTM
P2CMOSTM
Perfect WatchTM
Pharma✓ChekTM
PLANTM
PolycraftTM
POSitalkerTM
Power & ControlTM
QUAD3000TM
QUIKLOOKTM
RATTM
RTX16TM
SABRTM
Script✓ChekTM
SCXTM
SERIES/800TM
Series 3000TM
Series 32000®
Shelf✓ChekTM
SPIRETM
STARTM
Starlink™
STARPLEXTM
STARPLEX IITM
SuperChipTM
SuperScriptTM
SYS32TM
TapePakTM
TDSTM
TeleGateTM
The National Anthem®
Time✓ChekTM
TINATM
TLCTM
TrapezoidalTM
TRI-CODETM
TRI-POLYTM
TRI-SAFETM
TRI-STATE®
TURBOTRANSCEIVERTM
VIPTM
VR32TM
XMOSTM
XPUTM
Z STARTM
883B/RETSTM
883S/RETSTM

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LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Linear Products Introduction

National Semiconductor Corporation first established itself as the Linear Leader in 1967 with the introduction of the FIRST MONOLITHIC VOLTAGE REGULATOR . . . LM100. In the 20 years since, many of our products were firsts in performance and function. Today, this catalog spans the traditional areas of Op Amps, Voltage Regulators, Voltage References and Temperature Sensors, to Data Acquisition, Communication, Automotive, and Power Plus Control. National Semiconductor intends to remain a leader in the traditional product areas while forging ahead into VLSI solutions for analog problems and analog systems.

You can rely on National LINEAR to develop the most comprehensive product offering for use in the commercial, computer, automotive, telecommunication, industrial or military business segments. More than 1,000 basic LINEAR products (5400 options) allow design engineers to find the optimum Linear IC solution from National Semiconductor.

The Linear product line is presented in 3 Databooks. All sections are referenced and cross-indexed to provide quick and easy access. The technical information and basic product specifications are presented in data sheet format, including maximum ratings, electrical characteristics, performance curves and package information.

Additional application information is available as specific application notes or completely compiled in the LINEAR APPLICATIONS HANDBOOK. A product cross reference to the specific application note has been provided. This handbook and the 3-volume set of Linear Data Books represent a complete base of information to the National LINEAR product line.

National Semiconductor Corporation

Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advanced Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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National Semiconductor Corporation

CROSS REFERENCE BY PART NUMBER

A complete interchangeability list of Linear IC's offered by most Integrated Circuit Manufacturers are listed in this section and reference the nearest National Semiconductor Corp. direct replacement or recommended replacement with either an improved or functional replacement. The following notations are appended to assist you in finding the best option.

No reference note ..... "DIRECT REPLACEMENT"

Note (1) ..... "IMPROVED REPLACEMENT" Pin-for-Pin replacement with "SUPERIOR" Electrical Specifications.

Note (2) ..... "FUNCTIONAL REPLACEMENT" Similar device. Consult datasheet to determine the suitability for specific application.

Note (3) ..... "SIMILAR DEVICE" with superior performance. Consult datasheet to determine suitability of the replacement for specific application.

ANALOG DEVICES	NATIONAL	
AD0P07	LM607	(1)
ADDAC-08	DAC0800	
ADDAC-08	DAC0801	
ADDAC-08	DAC0802	
ADDAC80	DAC1280+	(1)
ADDAC85	DAC1280+	(1)
AD101A	LM101A	(1)
AD201A	LM201A	(1)
AD301A	LM301A	(1)
AD506	LH0022	(2)
AD509	LH0003	(2)
AD521	LM363	(2)
AD521	LH0036	(2)
AD524	LH0038	(2)
AD537	LM331	(2)
AD562	DAC1266	(3)
AD563	DAC1265	(3)
AD565A	DAC1265	
AD566A	DAC1266	
AD567	DAC1230	(2)
AD573	ADC1005	(2)
AD573	ADC1025	(2)
AD581	LM581	
AD581	LH0070	(1)
AD582	LF398	(2)
AD583	LF198	(3)
AD588	LM369	(2)
AD589M	LM385	(1)
AD589U	LM185	(1)
AD590	LM135	(2)
AD590	LM34	(3)
AD590	LM134	(2)
AD590	LM35	(3)
AD611K	LF411AC	(1)
AD611J	LF411C	(1)
AD614	LH0086	(2)
AD624	LH0038	(2)
AD650	LM331	(2)
AD651	LM331	(2)
AD654	LM331	(2)
AD673	ADC0841	(2)
AD741	LM741	
ADLH0032	LH0032	(2)
ADLH0033	LH0033	(2)
AD0042	LH0042	(2)
AD3542	LH0042	(2)
AD5035	LH0042	(2)
AD7502	LF13509	(2)
AD7516	CO4066B	(2)
AD7523	DAC0832	(2)
AD7523	DAC0831	(2)
AD7523	DAC0830	(2)
AD7524	DAC0830	(3)
AD7524	DAC0831	(3)
AD7524	DAC0832	(3)
AD7533	DAC1020	
AD7533	DAC1022	
AD7533	DAC1021	
AD7541A	DAC1218	(2)
AD7541A	DAC1219	(2)
AD7541	DAC1219	(1)
AD7541	DAC1218	(1)
AD7542	DAC1210	(2)
AD7542	DAC1209	(2)
AD7542	DAC1208	(2)
AD7545	DAC1209	(2)
AD7545	DAC1210	(2)
AD7545	DAC1208	(2)
AD7548	DAC1230	(2)
AD7548	DAC1232	(2)
AD7548	DAC1231	(2)
AD7552	ADC1225	(2)
AD7552	ADC1205	(2)
AD7571	ADC1005	(2)
AD7571	ADC1025	(2)
AD7575	ADC0820	(2)
AD7576	ADC0820	(2)
AD7578	ADC1225	(2)
AD7578	ADC1205	(2)
AD7820	ADC0820	

APEX	NATIONAL	
PA01	LM12	(2)
PA01	LH0101	(2)
PA07	LM12	(2)
PA10	LM12	(2)
PA10	LH0101	(2)
PA11	LM12	(2)
PA51	LM12	(2)
PA73	LM12	(2)

BURR-BROWN	NATIONAL	
SHC80	LF398	(2)
SHC85	LF398	(2)
HOS-100	LH0033	(2)
INA102	LH0038	(2)
SHC298A	LF398A	(1)
3507	LM6361	(2)
3533	LH0033	(2)
3542	LH0042	(2)
3550	LM6361	(2)
3551	LM6361	(2)
3553	LH0063	(2)
3554	LH0032	(2)
3571	LM675	(2)
3572	LH0021	(2)
3573	LM675	(2)
3606A6	LH0084	(2)
3606A6	LH0086	(2)
3626	LH0036	(2)
3629	LH0038	(2)

CTS	NATIONAL	
CTS0002	LH0002	(1)
CTS0004	LH0004	(1)
CTS0021	LH0021	(1)
CTS0024	LH0024	(1)
CTS0032	LH0032	(1)
CTS0033	LH0033	(1)
CTS0041	LH0041	(1)
CTS0042	LH0042	(1)
CTS2101A	LH2101A	(1)
CTS2111	LH2111	(1)

ELANTEC	NATIONAL	
ELH0002	LH0002	(1)
ELH0021	LH0021	(1)
ELH0032	LH0032	(1)
ELH0033	LH0033	(1)
ELH0041	LH0041	(1)
ELH0101	LH0101	(1)
EL2006C	LM6261	(2)
EL2006	LM6161	(2)
EHA2500	LM6161	(2)
EHA2502	LM6161	(2)
EHA2505	LM6361	(2)
EHA2510	LM6161	(2)
EHA2512	LM6161	(2)
EHA2515	LM6361	(2)
EHA2520	LM6164	(2)
EHA2522	LM6164	(2)
EHA2525	LM6364	(2)
EHA2600	LM6161	(2)
EHA2602	LM6161	(2)
EHA2605	LM6361	(2)
EHA2620	LM6164	(2)
EHA2622	LM6164	(2)
EHA2625	LM6364	(2)

EXAR	NATIONAL	
XR084M	LF147	(1)
XR084	LF347	(1)
XR146	LM146	(1)
XR246	LM246	(1)
XR346	LM346	(1)
XR-1001	MF4C-100	(1)
XR-1002	MF4C-50	(1)
XR1458	LM1458	(1)

FAIRCHILD	NATIONAL	
μA78XXKM	LM140K-XX	(1)
μ78LXXACH	LM78LXXACH	(1)
μ78XXUC	LM340T-XX	(1)
μ78XXUC	LM78XXCT	(1)
μA78LXXACLP	LM78LXXACZ	(1)
μA78LXXAWC	LM78LXXACZ	(1)
μ78MXXCKC	LM78XXCK	(1)
μ78MXXCKC	LM78MXXCT	(1)
μA78MXXUC	LM341P-XX	(1)
μA78MXXCKC	LM78XXCT	(1)
μA78XXKC	LM340K-XX	(1)
μA79XXUC	LM79LXXACZ	(1)
μA79XXUC	LM79MXXCP	(1)
μA79XXCKC	LM79XXCT	(1)
μA79XXCKC	LM79MXXCP	(1)
μA79XXUC	LM79MXXCH	(1)
μA79XXUC	LM320T-XX	(1)
μA79XXCKC	LM79MXXCH	(1)
μA79XXCKC	LM79LXXACZ	(1)
μA79MXXAUC	LM320MP-XX	(1)
μA79XXKM	LM120K-XX	(1)
μA79XXKC	LM320K-XX	(1)
μA79XXUC	LM79XXCT	(1)
μA101A	LM101A	(1)
μA102	LM102	(1)
μA105HM	LM105H	(1)
μA107	LM107	(1)
μA108A	LM108A	(1)
μA108	LM108	(1)
μA109KM	LM109K STEEL	(1)
μA110	LM110	(1)
μA111	LM111	(1)
μA124	LM124	(1)
μA139	LM139	(1)
μA139A	LM139A	(1)
μA201A	LM201A	(1)
μA207	LM207	(1)
μA208	LM208	(1)
μA208A	LM208A	(1)
μA211	LM211	(1)
μA224	LM224	(1)
μA239	LM239	(1)
μA239A	LM239A	(1)
μA248	LM248	(1)
μA249	LM249	(1)
μA301A	LM301A	(1)
μA302	LM302	(1)
μA304HC	LM304H	(1)
μA305HC	LM305H	(1)
μA305AHC	LM305AH	(1)
μA307	LM307	(1)
μA308A	LM308A	(1)
μA308	LM308	(1)
μA309KC	LM309K STEEL	(1)
μA310	LM310	(1)
μA311	LM311	(1)
μA317KC	LM317K STEEL	(1)
μA317UC	LM317T	(1)
μA318	LM318	(1)
μA324	LM324	(1)
μA339	LM339	(1)
μA339A	LM339A	(1)
μA348	LM348	(1)
μA349	LM349	(1)
μA376TC	LM376N	(1)
μA555TC	LM555CN	(1)
μA556PC	LM556CN	(1)
μA709	LM709	(1)
μA709	LM709	(1)
μA710	LM710	(1)
μA710	LM710	(1)
μA711	LM711	(1)
μA714	LM607	(1)
μA723HM	LM723H	(1)
μA723HC	LM723CH	(1)
μA723DC	LM723CJ	(1)
μA723MJ	LM723J	(1)
μA723CJ	LM723CJ	(1)
μA723DM	LM723J	(1)
μA723PC	LM723CN	(1)
μA723CN	LM723CN	(1)
μA725	LM725	(1)
μA725	LM725	(1)
μA733CN	LM733CN	(1)
μA733	LM733	(1)
μA741	LM741	(1)
μA741	LM741	(1)
μA747	LM747	(1)
μA747	LM747	(1)
μA748	LM748	(1)
μA748	LM748	(1)
μA760	LM760	(1)
μA771B	LF411	(1)
μA771	LF351	(1)
μA771A	LF411	(1)
μA772B	LF412A	(1)
μA772	LF353	(1)
μA772A	LF412A	(1)
μA774	LF347	(1)
μA774B	LF347B	(1)
μA776	LM4250	(1)
μA1458	LM1458	(1)
μC1496P	LM1496N	(1)
μC1496G	LM1496H	(1)
μA1558	LM1558	(1)
μC1596G	LM1596H	(1)
TDA2310	LM381	(1)
μA2901	LM2901	(1)
μA2902	LM2902	(1)
TCA3089	LM3089N	(1)
μA3301	LM3301	(1)
μA3302	LM3302	(1)
μC4558CD	LM833CN	(1)
μA7392	LM1014	(1)

HARRIS	NATIONAL	
HA-OP07	LM607	(1)
HF-10	MF10	
HI-201	LF13201	
HI-300	AH5020	(2)
LM741	LM741	(1)
HA2400	LM604AM	(2)
HA2404	LM604AM	(2)
HA2405	LM604C	(2)
HA2406	LM604C	(2)
HA2500	LM6161	(2)
HA2502	LM6161	(2)
HA2505	LM6361	(2)
HA2510	LM6161	(2)
HA2512	LM6161	(2)
HA2515	LM6361	(2)
HA2520	LM6164	(2)
HA2520	LH0003	(1)
HA2522	LH0003	(1)
HA2522	LM6164	(2)
HA2525	LH0003	(1)
HA2525	LM6364	(2)
HA2530	LH0024	(2)
HA2535	LH0024	(2)
HA2540	LH0032	(2)
HA2541-5	LM6361	(2)
HA2541-2	LM6161	(2)
HA2542	LH0032	(2)
HA2542-2	LM6164	(2)
HA2542-5	LM6164	(2)
HA2600	LM6161	(2)
HA2602	LM6161	(2)
HA2605	LM6361	(2)
HA2620	LM6164	(2)
HA2622	LM6164	(2)
HA2625	LM6364	(2)
HA2640	LH0004	(1)
HA5033	LH0033	(1)
HA5162	LH0062	(2)
A5180	LH0052	(1)

HEWLETT PACKARD	NATIONAL	
HCTL-100	LM628	(3)

HITACHI	NATIONAL	
HA13421A	LM18293	(3)
HA17082	LF353	(1)
HA17082A	LF412	(1)
HA17084	LF347	(1)
HA17084A	LF347B	(1)
HA17094	LM2904	(1)
HA17301	LM3301	(1)
HA17324	LM324	(1)
HA17339	LM339	(1)
HA17358	LM358	(1)
HA17393	LM393	(1)
HA17458	LM1458	(1)
HA17741	LM741	(1)
HA17747	LM747	(1)
HA17901	LM2901	(1)
HA17902	LM2902	(1)
HA17903	LM2903	(1)

LINEAR TECHNOLOGY	NATIONAL	
REF-01	LM168	(1)
REF-01	LM368	(1)
LM129	LM129	
LM134	LM134	
LM185	LM185	
LM199	LM199	
LM234	LM234	
LM329	LM329	
LM334	LM334	
LM385	LM385	
LM399	LM399	
AD581	LM581	
AD581	LH0070	
LT1001	LM607A	(1)
LT1004C	LM385	
LT1004M	LM185	
LT1009M	LM136-2.5	
LT1009C	LM336-2.5	
LT1019C	LM368	(2)
LT1019M	LM168	(2)
LT1020	LP2951	(3)
LT1021M	LM169	(1)
LT1021C	LM369	(1)
LT1029M	LM136-5.0	
LT1029C	LM336-5.0	
LT1031	LH0070	

LSI COMPUTER	NATIONAL	
LS7261	LM621	(3)
LS7263	LM621	(3)

MICRA	NATIONAL	
MC0002	LH0002	(1)
MC0003	LH0003	(1)
MC0004	LH0004	(1)
MC0032	LH0032	(1)
MC0033	LH0033	(1)
MC0041	LH0041	(1)
MC0063	LH0063	(1)

MICRO POWER SYSTEMS	NATIONAL	
MPOP07	LM607	(1)
MP108	LM108	(1)
MP108A	LM108A	(1)
MP155A	LF155A	(1)
MP155	LF155	(1)
MP156	LF156	(1)
MP156A	LF156A	(1)
MP157	LF157	(1)
MP157A	LF157A	(1)
MP208A	LM208A	(1)
MP208	LM208	(1)
MP308	LM308	(1)
MP308A	LM308A	(1)
MP355A	LF355A	(1)
MP356A	LF356A	(1)
MP357A	LF357A	(1)
MP2108A	LH2108A	(1)
MP5010H	LM385	
MP5010L	LM385	
MP5010G	LM185	
MP5010H	LM185	
MP5010L	LM185	
MP5010G	LM385	

MOTOROLA	NATIONAL	
DAC-08	DAC0800	
DAC-08	DAC0802	
DAC-08	DAC0801	
MC78XXACT	LM340AT-XX	(1)
MC78XXCK	LM78XXCK	(1)
MC78LXXACP	LM78LXXACZ	(1)
MC78MXXCT	LM78XXCK	(1)
MC78MXXCT	LM341P-XX	(1)
MC78LXXACG	LM78LXXCH	(1)
LM78XXCT	LM78LXXCH	(1)
MC78MXXCT	LM78MXXCT	(1)
MC78XXCT	LM78XXCT	(1)
MC78LXXCP	LM78LXXACZ	(1)
MX78MXXCT	LM342P-XX	(1)
MC78LXXCG	LM78LXXACH	(1)
MC79XXCK	LM320K-XX	(1)
MC79MXXCKC	LM320MP-XX	(1)
MC79XXCK	LM79XXCK	(1)
MC79XXCKC	LM320T-XX	(1)
LM79XXCP	LM79XXCT	(1)
MC79XXCT	LM79MXXCH	(1)
MC79LXXCP	LM320LZ-XX	(1)
MC79LXXACG	LM320H-XX	(1)
MC79LXXCLP	LM320LZ-XX	(1)
MC79XXCT	LM79MXXCP	(1)
MC79LXXACP	LM79LXXACZ	(1)
MC79LXXCP	LM79LXXCZ	(1)
MC79XXCT	LM320T-XX	(1)
MC79XXCT	LM79XXCT	(1)
MC79XXCT	LM79LXXACZ	(1)
LM79XXCP	LM79LXXACZ	(1)
LM79XXCP	LM79MXXCH	(1)
LM79XXCP	LM79MXXCP	(1)
LM109K	LM109K STEEL	(1)
LM109H	LM109H	(1)
LM117H	LM117K STEEL	(1)
LM123K	LM123K STEEL	(1)
LM137H	LM137H	(1)
LM137K	LM137K STEEL	(1)
LM140K	LM140K-XX	(1)
LM150K	LM150K STEEL	(1)
LM285	LM285	
LM309H	LM309H	(1)
LM309H	LM309K	(1)
LM309K	LM309K STEEL	(1)
LM317H	LM317H	(1)
LM317LZ	LM317LZ	(1)
LM317T	LM317T	(1)
LM317KC	LM317T	(1)
LM317K	LM317K STEEL	(1)
LM323K	LM323K STEEL	(1)
LM330-XKC	LM330T-XX	(1)
LM337H	LM337H	(1)
LM337K	LM337K STEEL	(1)
LM337KC	LM337T	(1)
LM337T	LM337T	(1)
LM340T-XX	LM340T-XX	(1)
LM340T-XX	LM340K-XX	(1)
LM340-XXKC	LM340T-XX	(1)
LM350T	LM350T	(1)
LM350K	LM350K STEEL	(1)
LM350KC	LM350T	(1)
LM350KA	LM350K STEEL	(1)
LM385	LM385	
AD562A	DAC1266	(2)
AD563A	DAC1265	(2)
μPC741	LM741	
MC1408	DAC0806	
MC1408	DAC0808	
MC1408	DAC0807	
MC1414	LM1414	(1)
MC1436	LM343	(1)
MC1458	LM1458	(1)
MC1496	LM1446	
MC1508	DAC0808	
MC1514	LM1514	(1)
MC1536	LM143	(1)
MC1558	LM1558	(1)
MC1596G	LM1596CH	(1)
MC1709	LM709	(1)
MC1709	LM709	
MC1710	LM710	
MC1723CL	LM723CJ	(1)
MC1723CG	LM723CH	(1)
MC1723CP	LM723CN	(1)
MC1723CL	LM723CM	(1)
MC1723L	LM723J	(1)
MC1723G	LM723H	(1)
MC1733CG	LM723CH	(1)
MC1741	LM741	(1)
MC1741	LM741	
MC1747	LM747	(1)
MC1747	LM747	
MC1748	LM748	
LM2930-XKC	LM2930T-XX	(1)
MC3301	LM3301	(1)
MC3302	LM3302	(1)
MC3361	LM3361AN	(1)
MC3401	LM3401	(1)
MC3410	DAC1020	(2)
MC3412	DAC1265	(1)
MC3510	DAC1020	(2)
MC4741	LM348	(1)
MC14442	ADC0829	(2)
MC14444	ADC0830	(2)
MC34001A	LF411C	(1)
MC34001B	LF411C	(1)
MC34001	LF351	(1)
MC34002B	LF412C	(1)
MC34002	LF353	(1)
MC34002A	LF412A	(1)
MC34004B	LF347B	(1)
MC34004	LF347	(1)
MC34004B	LF147	(1)
MC34004	LF147	(1)
MC35001	LF411M	(1)
MC35001A	LF411M	(1)
MC35001B	LF411M	(1)
MC35002B	LF412M	(1)
MC35002	LF412M	(1)
MC35002A	LF412AM	(1)

MC145040	ADC0811	(2)
MC145041	ADC0811	

PRECISION-MONOLITHIC INC.	NATIONAL	
REF-01J	LM368-10	(1)
REF-01	LM369	(1)
AMP-01	LH0038	(2)
DAC-02	DAC1022	(2)
DAC-02	DAC1020	(2)
REF-02	LM368-5.0	(3)
DAC-02	DAC1021	(2)
DAC-03	DAC1020	(2)
DAC-03	DAC1022	(2)
BUF03	LH0033	(1)
DAC-03	DAC1021	(2)
OP05	LM607	(2)
DAC-05	DAC1020	(2)
DAC-05	DAC1021	(2)
DAC-05	DAC1022	(2)
SW06B	LF11333	
SW06G	LF13333	
SW06F	LF13333	
OP07	LM607	(1)
DAC-08	DAC0801	
DAC-08	DAC0800	
MUX-08E	LF13508	
DAC-08	DAC0802	
OP15	LF411	(1)
MUX-24E	LF13509	
REF-43	LM368-2.5	(1)
OP77	LM607	(1)
OP100	LH0052	(2)
DAC100	DAC1021	(2)
DAC100	DAC1020	(2)
DAC100	DAC1022	(2)
OP105/111	LH0052	(2)
PM108A	LM108A	(1)
PM108	LM108	(1)
PM139A	LM139A	(1)
PM139	LM139	(1)
PM155	LF155	(1)
PM155A	LF155A	(1)
PM156	LF156	(1)
PM156A	LF156A	(1)
PM157	LF157	(1)
PM157A	LF157A	(1)
SW201G	LF13201	
SW201B	LF11201	
SW201F	LF13201	
SW202B	LF11202	
SW202F	LF13202	
SW202G	LF13202	
PM208A	LM208A	(1)
PM208	LM208	(1)
OP215	LF412	(1)
PM308A	LM308A	(1)
PM308	LM308	(1)
DAC312	DAC1266	(2)
PM339A	LM339A	(1)
PM355	LF355	(1)
PM355A	LF355A	(1)
PM356A	LF356A	(1)
PM356	LF356	(1)
PM357A	LF357A	(1)
PM357	LF357	(1)
PM420	LF124	(1)
OPA501/3573	LH0101	(2)
PM725	LM725	(1)
PM-725	LM725	
PM741	LM741	(1)
PM-741	LM741	
PM-747	LM747	
PM747	LM747	(1)
DAC888	DAC0831	(2)
DAC888	DAC0832	(2)
DAC888	DAC0830	(2)
ADC910	ADC1005	(2)
ADC910	ADC1025	(2)
DAC0812	DAC1208	(2)
DAC0812	DAC1209	
DAC0812	DAC1210	
DAC1408	DAC0806	(2)
DAC1408	DAC0808	(2)
DAC1408	DAC0807	(2)
PM2108A	LH2108A	(1)
PM7533	DAC1021	
PM7533	DAC1020	
PM7533	DAC1022	
PM7541	DAC1219	
PM7541	DAC1218	

RAYTHEON	NATIONAL	
REF-01	LM369	(1)
REF-01T	LM368	(1)
REF-02	LM368-5.0	(3)
REF-03	LM368-2.5	(1)
LP365	LP365	
RC714	LM607	(1)
RC741	LM741	(1)
RC741	LM741	
RC747	LM747	
RC747	LM747	(1)
RC1458	LM1458	(1)
RC1558	LM1558	(1)

RCA/ INTERSIL/G.E.	NATIONAL	
CA081C	TL081C	(2)
CA081A	LF411C	(2)
CA081	LF411M	(2)
CA081B	LF411C	(2)
CA082C	TL082C	(2)
CA082B	LF412C	(2)
CA082	LF412M	(2)
CA082A	LF412C	(2)
CA084B	LF347B	(2)
CA084	LF147	(2)
CA084C	LF347	(2)
CA124	LM124	(1)
CA139	LM139	(1)
CA139A	LM139A	(1)
CA158	LM158	(1)
CA158A	LM158A	(1)
DG201	LF11201	
DG211	LF13201	
DG212	LF13202	
CA224	LM224	(1)
CA239	LM239	(1)
CA239A	LM239A	(1)
CA258	LM258	(1)
CA258A	LM258A	(1)
CA301A	LM301A	(1)
CA307	LM307	(1)
CA311	LM311	(1)
CA324	LM324	(1)
CA339A	LM339A	(1)
CA339	LM339	(1)
CA358A	LM358A	(1)
CA358	LM358	(1)
CA741	LM741	
CA741	LM741	(1)
CA747	LM747	(1)
CA747	LM747	
CA748	LM748	(1)
μA748	LM748	
CA748	LM748	
ADC0801	ADC0801	
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
CA1458	LM1458	(1)
CA1558	LM1558	(1)
CA3105	LM675	(2)
CA3290	LF393	(2)
CA3401	LM3401	(1)
IH5009	AH5009	
IH5010	AH5010	
IH5011	AH5011	
IH5012	AH5012	
IH6108	LF13508	
IH6208	LF13509	
ICL7114	ADC1205	(2)
ICL7114	ADC1225	(2)
AD7520	DAC1021	
AD7520	DAC1020	
AD7520	DAC1022	
AD7521	DAC1221	
AD7521	DAC1220	
AD7521	DAC1222	
AD7530	DAC1020	(3)
AD7530	DAC1021	(3)
AD7530	DAC1022	(3)
AD7531	DAC1220	
AD7531	DAC1221	
AD7531	DAC1222	
AD7533	DAC1020	
AD7533	DAC1021	
AD7533	DAC1022	
AD7541	DAC1219	
AD7541	DAC1218	
ICL7650	LMC668	(1)
ICL8069	LM385-1.2	
ICL8069	LM313	
ICH8530	LH0101	(2)

SAMSUNG	NATIONAL	
LM741	LM741	

SGS	NATIONAL	
L78M12CV	LM341P-12	(1)
L78M15CV	LM341P-15	(1)
L78S12CV	LM340T-12	(1)
L78S05CV	LM340T-5.0	(1)
L78S15CV	LM340T-15	(1)
L78M05CV	LM341P-5.0	(1)
LM117K	LM117K	(1)
L123CB	LM723CN	(1)
L272	LM18272	
L293	LM18293	
L298	LM18298	
LM317T	LM317T	(1)
LM317K	LM317K	(1)
LM748	LM748	
TDA2310	LM381	
LM2930A	LM2930T-5.0	(1)
LM2931A	LM2931AT-5.0	(1)
TCA3089	LM3089	
L7805CT	LM7805CK	(1)

L7815CV	LM7815CT	(1)
L7905ACV	LM320T-5.0	(1)
L7905CT	LM7905CK	(1)
L7905CV	LM7905CT	(1)
L7912CT	LM7912CK	(1)
L7912ACV	LM320T-12	(1)
L7915CT	LM7915CK	(1)
L7915ACV	LM320T-15	(1)

SIEMENS	**NATIONAL**	
TCA365	LH0101	(1)

SIGNETICS	**NATIONAL**	
DAC-08	DAC0802	
DAC-08	DAC0801	
DAC-08	DAC0800	
78LXXACS	LM78XXACZ	(1)
78LXXADB	LM78XXACH	(1)
78LXXCDB	LM78LXXCH	(1)
78LXXCS	LM78LXXCZ	(1)
78XXCU	LM78XXCT	(1)
78XXDA	LM78XXCK	(1)
79XXDA	LM79XXCK	(1)
79XXCU	LM79XXCT	(1)
LM109DB	LM109H	(1)
TBA120S-4	TBA120SIV	
TBA120S-3	TBA120SIII	
TBA120S-2	TBA120SII	
LF198	LF198	
LF298	LF298	
LM309DA	LM309K	(1)
LM309DB	LM309H	(1)
LM340XXLL	LM340TXX	(1)
LM340XXDA	LM340KXX	(1)
LF398	LF398	
NE529	LM361	(1)
SE529	LM161	(1)
SE532	LM158	(1)
SA532	LM2904	(1)
NE532	LM358	(1)
SA534	LM2902	(1)
NE555N	LM555CN	
SE567	LM567	(2)
μA723CN	LM723CN	(1)
μA723CL	LM723CH	(1)
μA723L	LM723H	(1)
μA723CF	LM723CJ	(1)
μA723F	LM723J	(1)
μA741	LM741	
μA747	LM747	
ADC0801	ADC0801	
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
ADC0805	ADC0805	
MC1408	DAC0808	
MC1408	DAC0807	
MC1408	DAC0806	
MC1496N	LM1496N	
MC1508	DAC0808	
MC1596K	LM1596H	
NE4558D	LM833CM	(2)
NE4558N	LM833CN	(2)
NE4558	LM833	(2)
NE5034	ADC0841	(2)
SE5118	DAC0830	(2)
NE5118	DAC0830	(2)
NE5410	DAC1020	(2)
SE5410	DAC1020	(2)
NE5532P	LM833CN	(2)
NE5532	LM833	
NE5532N	LM833CN	(2)

SILICON GENERAL	**NATIONAL**	
SG101	LM101A	(1)
SG101A	LM101A	(1)
SG107	LM107	(1)
SG124	LM124	(1)
SG201	LM201A	(1)
SG201A	LM201A	(1)
SG207	LM207	(1)
SG224	LM224	(1)
SG301A	LM301A	(1)
SG307	LM307	(1)
SG324	LM324	(1)
SG741	LM741	(1)
SG741	LM741	(1)
SG1173	LM675	(2)
SG1436	LM343	(1)
SG1536	LM143	(1)
SG3173	LM675	(2)

SILICONIX	**NATIONAL**
DG201	LF13201
DG202	LF13202
DG211	LF13201
DG212	LF13202
DG508	LF13508
DG509	LF13509

SPRAGUE	**NATIONAL**
UDN22933	LM18293

TELEDYNE	**NATIONAL**	
TP0032	LH0032	(1)
TP0033	LH0033	(1)

TEXAS INSTRUMENTS	**NATIONAL**	
μA78XXCKC	LM78XXCT	(1)
μA78LXXACL	LM78LXXACZ	(1)
μA78MXXCKD	LM78MXXCP	(1)
μA79MXXCKD	LM79MXXCP	(1)
μA79XXCKC	LM79XXCT	(1)
TL061A	LF441	(1)
TL061B	LF441A	(1)
TL061	LF441	(1)
TL062A	LF442	(1)
TL062B	LF442	(1)
TL062	LF442	(1)
TL064A	LF444	(1)
TL064	LF444	(1)
TL071B	LF411	(1)
TL071A	LF411	(1)
TL071	LF351	(1)
TL072	LF353	(1)
TL072A	LF412	(1)
TL072B	LF412	(1)
TL074	LF347	(1)
TL074A	LF347B	(1)
TL081B	LF411	(1)
TL081	TL081	(1)
TL081A	LF411	(1)
TL082B	LF412	(1)
TL082A	LF412	(1)
TL082	TL082	(1)
TL084A	LF347B	(1)
TL084	LF347	(1)
TL087	LF411A	(1)
TL088	LF411A	(1)
TLC274BI	LMC660AI	(2)
TLC274BM	LMC660AM	(2)
TLC274M	LMC660AM	(2)
TLC274AC	LMC660AI	(2)
TLC274BC	LMC660AI	(2)
TLC274AM	LMC660AM	(2)
TLC274I	LMC660AI	(2)
TLC274C	LMC660C	(2)
TLC274AI	LMC660AI	(2)
TL288	LF412A	(1)
LM317KC	LM317T	(1)
TL487N	LM3915N	(2)
TL489N	LM3914N	(2)
TL490N	LM3914N	(2)
TL491N	LM3914N	(2)
TL520	ADC0848	(2)
TL521	ADC0848	(2)
TL522	ADC0848	(2)
TL530	ADC0830B	
TL531	ADC0830C	
TL532	ADC0829B	
TLC532A	ADC0829B	(2)
TLC533A	ADC0829C	(2)
TL533	ADC0829C	
TLC540	ADC0811	(2)
TLC541	ADC0811	
TLC549	ADC0831	(2)
μA709	LM709	
μA723CN	LM723CN	(1)
μA723CJ	LM723CJ	(1)
μA723MJ	LM723J	(1)
μA733CN	LM733CN	
μA741	LM741	
μA747	LM747	
ADC0801	ADC0801	
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
ADC0805	ADC0805	
ADC0808	ADC0808	
ADC0809	ADC0809	
ADC0831	ADC0831	
ADC0832	ADC0832	
ADC0834	ADC0834	
ADC0838	ADC0838	
RC4558	LM833	
RV4558D	LM833CM	
RC4558D	LM833CM	

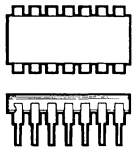
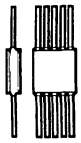
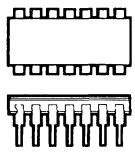
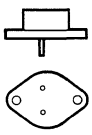
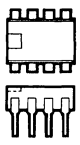
THOMSON	**NATIONAL**	
LM105H	LM105H	(1)
LM109K	LM109K STEEL	(1)
LM117K	LM117K STEEL	(1)
LM117H	LM117H	(1)
LM123K	LM123K STEEL	(1)
LM134	LM134	
LM135	LM135	
LM137K	LM137K STEEL	(1)
LM137H	LM137H	(1)
LM138K	LM138K STEEL	(1)
LF198	LF198A	(1)
LM234	LM234	
LM235	LM235	
LF298	LF298	
LM305H	LM305H	(1)
LM309H	LM309H	(1)
LM309K	LM309K STEEL	(1)

LM317K	LM317K STEEL	(1)
LM317H	LM317H	(1)
LM323K	LM323K STEEL	(1)
LM334	LM334	
LM335A	LM335A	
LM335	LM335	
LM337H	LM337H	(1)
LM337K	LM337K STEEL	(1)
LM338K	LM338K STEEL	(1)
LF398	LF398A	(1)
μA741	LM741	
μA748	LM748	
TBC0136	LM336	
μA7805CK	LM7805KC	(1)
μA7805MK	LM140K-5.0	(1)
μA7812MK	LM140K-12	(1)
μA7812CK	LM7812KC	(1)
μA7815CK	LM7815KC	(1)
μA7815MK	LM140K-15	(1)
μA7905MK	LM120K-5.0	(1)
μA7905CK	LM7905KC	(1)
μA7912MK	LM120K-12	(1)
μA7912CK	LM7912KC	(1)
μA7915MK	LM120K-15	(1)
μA7915CK	LM7915KC	(1)

TOSHIBA	**NATIONAL**	
TA7504	LM741	
TA75339	LM2901	(1)
TA75358	LM2904	(1)
TA75393	LM2903	(1)
TA75902	LM2902	(1)

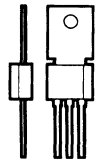
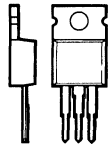
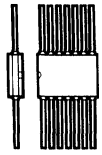
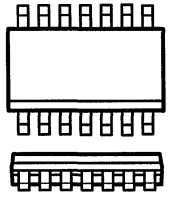
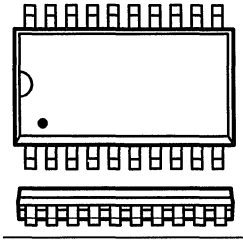
UNITRODE	**NATIONAL**
L293	LM18293
L298	LM18298

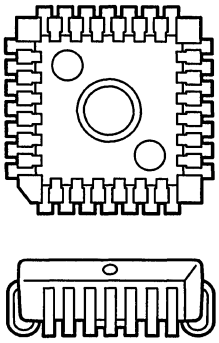
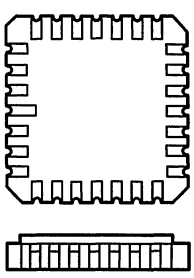
Industry Package Cross-Reference Guide

	NSC	Signetics	Fairchild	Motorola	TI	RCA	Hitachi	NEC	LTC
 4/16 Lead Glass/Metal DIP	D	I	D	L		D	C	D	D
 Glass/Metal Flat Pack	F	Q	F	F	F, S	K	F		Q
 TO-99, TO-100, TO-5	H	T, K, L, DB	H	G	L	S*, V1**		A	H
 8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	F	R, D	U	J		G	D	J, J8
 TO-3 (Steel)	K			KS					K
TO-3 (Aluminum)	KC	DA	K	K	K				
 8-, 14- and 16-Lead Plastic DIP	N	V, A, B	T, P	P	P, N	E	P	C	N, N8

*With dual-in-line formed leads

**With radically formed leads

		NSC	Signetics	Fairchild	Motorola	TI	RCA	Hitachi	NEC	LTC
	TO-202 (D-40, Durawatt)	P					KD			
	TO-220 3- & 5-Lead	T	U	U		KC		T	H	T
	TO-220 11-, 15- & 23-Lead	T								
	Low Temperature Glass Hermetic Flat Pack	W		F	F	W				
	TO-92 (Plastic)	Z	S	W	P	LP			H	Z
	SO (Narrow Body)	M	D	S	D	D	M	MP	G	S
	SO (Wide Body)	WM				DW				

	NSC	Signetics	Fairchild	Motorola	TI	RCA	Hitachi	NEC	LTC
 PCC	V	A	Q	FN	FN	Q	CP	L	
 LCC Leadless Ceramic Chip Carrier	E	G	L1	U	FK/ FG/FH	BJ	CG	K	

Linear 1 Databook
Selection Guides

Voltage Regulators

Operational Amplifiers

Buffers

Voltage Comparators

Instrumentation Amplifiers

National Semiconductor Corporation

Voltage Regulators Definition of Terms

Current-Limit Sense Voltage: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

Feedback Sense Voltage: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

Input Voltage Range: The range of dc input voltages over which the regulator will operate within specifications.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

Maximum Power Dissipation: The maximum total device dissipation for which the regulator will operate within specifications.

Output-Input Voltage Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

Output Noise Voltage: The RMS ac voltage at the output with constant load and no inut ripple, measured over a specified frequency range.

Output Voltage Range: The range of regulated output voltages over which the specifications apply.

Output Voltage Scale Factor: The output voltage obtained for a unit value of resistance between the adjustment terminal and ground.

Quiescent Current: That par of input current to the regulator that is not delivered to the load.

Ripply Rejection: The line regulation for ac inupt signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

Standby Current Drain: That part of the operating current of the regulator which does not contribute to the load current. (See Quiescent Current)

Temperature Stability: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Thermal Regulation: Percentage change in output voltage for a given change in power dissipation over a specified time period.

National Semiconductor Corporation

Voltage Regulators Selection Guide

Adjustable Positive Voltage Regulators

Amps	Device	Output Voltage	Package	Page
10.0	LM196K	1.25V–15V	TO-3	
	LM396K	1.25V–15V	TO-3	
5.0	LM138K	1.2V–32V	TO-3	
	LM338K	1.2V–32V	TO-3	
3.0	LM150K	1.2V–33V	TO-3	
	LM350K, T	1.2V–33V	TO-3, TO-220	
1.5	LM117K	1.2V–37V	TO-3	
	LM117HVK	1.2V–57V	TO-3	
	LM2941CT	5.0V–24V	TO-220	
	LM317K, T	1.2V–37V	TO-3, TO-220	
	LM317HVK	1.2V–57V	TO-3	
0.5	LM117H	1.2V–37V	TO-39	
	LM117HVH	1.2V–57V	TO-39	
	LM317H	1.2V–57V	TO-39	
	LM317HVH	1.2V–37V	TO-39	
	LM317MP	1.2V–37V	TO-202	
0.1	LM317LZ, M	1.2V–37V	TO-92, SO-8	
	LM2931CT	3.0V–24V	TO-220, 5-LEAD	
	LP2951CN, J, H, M	1.24V–29V	DIP, CERDIP, HEADER, SO-8	

Adjustable Negative Voltage Regulators

Amps	Device	Output Voltage	Package	Page
3.0	LM133K	−1.2V – −32V	TO-3	
	LM333K, T	−1.2V – −32V	TO-3, TO-220	
1.5	LM137K	−1.2V – −37V	TO-3	
	LM137HVK	−1.2V – −47V	TO-3	
	LM337K, T	−1.2V – −37V	TO-3, TO-220	
	LM337HVK	−1.2V – −47V	TO-3	
0.5	LM137H	−1.2V – −37V	TO-39	
	LM137HVH	−1.2V – −47V	TO-39	
	LM337H	−1.2V – −37V	TO-39	
	LM337HVH	−1.2V – −47V	TO-39	
	LM337MP	−1.2V – −37V	TO-202	
0.1	LM337LZ, M	−1.2V – −37V	TO-92, SO-8	

Fixed Positive Voltage Regulators

Amps	Device	Output Voltage	Package	Page
3.0	LM123K	5V	TO-3	
	LM2943CT*	5V	TO-220	
	LM323K	5V	TO-3	
1.0	LM109K	5V	TO-3	
	LM140AK	5V, 12V, 15V	TO-3	
	LM140K	5V, 12V, 15V	TO-3	
	LM2940CT	5V, 12V, 15V	TO-220	
	LM309K	5V	TO-3	
	LM340AK, T	5V, 12V, 15V	TO-3, TO-220	
	LM340K, T	5V, 12V, 15V	TO-3, TO-220	
	LM78xxCK, T	5V, 12V, 15V	TO-3, TO-220	
0.5	LM2984CT	5V, 12V, 15V	TO-220, TO-202	
	LM341T, P	5V, 12V, 15V	TO-220, TO-202	
	LM78MxxCT	5V, 12V, 15V	TO-220	
0.2	LM109H	5V	TO-39	
	LM309H	5V	TO-39	
	LM342P	5V, 12V, 15V	TO-202	
0.15	LM2930T	5V, 8V	TO-220	
0.1	LM140LAH	5V, 12V, 15V	TO-39	
	LM2931Z, T	5V	TO-92, TO-220	
	LM340LZ, H	5V, 12V, 15V	TO-92, TO-39	
	LM78LxxACZ, H, M	5V, 12V, 15V	TO-92, TO-39, SO-8	
	LP2950CZ	5V	TO-92	

*Future Product

Fixed Negative Voltage Regulators

Amps	Device	Output Voltage	Package	Page
3.0	LM145K	−5V, −5.2V	TO-3	
	LM345K	−5V, −5.2V	TO-3	
1.5	LM120K	−5V, −12V, −15V	TO-3	
	LM320K, T	−5V, −12V, −15V	TO-3, TO-220	
	LM79xxCT, K	−5V, −12V, −15V	TO-3, TO-220	
0.5	LM320MP	−5V, −12V, −15V	TO-220	
	LM79MxxCP, K	−5V, −12V, −15V	TO-202, TO-3	
0.2	LM120H	−5V, −12V, −15V	TO-39	
	LM320H	−5V, −12V, −15V	TO-39	
0.1	LM320LZ	−5V, −12V, −15V	TO-92	
	LM79LxxACZ, M	−5V, −12V, −15V	TO-92, SO-8	

*The LM320 has better electrical characteristics than the LM79xx.

LM100 Series +55°C to +150°C
LM300 Series 0°C to +125°C

Low Dropout Regulators

Amps	Device	Output Voltage	Package	Page
0.100	LM2931T, Z LP2950CZ LP2951N, J, H	5V, ADJ 5V ADJ	TO-220, TO-92 TO-92 DIP, CERDIP, HEADER	
0.150	LM2930T	5V, 8V	TO-220	
0.500	LM2984CT	TRIPLE 5V + WATCHDOG	TO-220, 11-LEAD	
0.750	LM2925T LM2935T	5V WITH DELAYED RESET DUAL 5V	TO-220, 5-LEAD TO-220, 5-LEAD	
1.5	LM2940CT LM2941CT*	5V, 12V, 15V ADJ	TO-220 TO-220, 5-LEAD	
3.0	LM2943CT*	5V	TO-220	

*Future Product

National Semiconductor Corporation

Operational Amplifiers Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

National Semiconductor Corporation

General Purpose Operational Amplifier Selection Guide

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Military Temperature Range (−55°C to +125°C) Specs at T_A = 25°C (Note 1)								
LH0044A	0.025	15	0.4	0.06	3	±3	±20	
LM607A	0.025	2	1.8	0.7	1.5	*	±22	
LH0044	0.05	30	0.4	0.06	4	±3	±20	
LM607B	0.05	3	1.8	0.7	1.5	*	±22	
LM11	0.3	0.05	*	0.3	0.6	*	±20	
LF411A	0.5	0.2	4	15	2.8	±6	±22	
LF441A	0.5	0.05	1	1	0.2	±6	±22	
LH0052	0.5	0.003	1	3	3.5	±5	±22	
LM108A	0.5	2	1	0.3	0.4	±2	±20	
LF412A	1	0.2	4	15	5.6	±6	±22	Dual BiFet
LF442A	1	0.05	1	1	0.4	±6	±22	Dual BiFet
LH0004	1	100	*	*	0.15	±5	±45	
LM604A	1	40	7	2	8	4	36	Multiplexed OA
LF155A	2	0.05	2.5	5	4	±5	±22	
LF156A	2	0.05	5	12	7	±5	±22	
LF157A	2	0.05	25	50	7	±5	±22	Minimum Gain of 5
LF411	2	0.2	4	15	3.4	±6	±18	
LMC660A	2	0.02	1.5	1.7	2.2	5	15	Quad CMOS
LM10	2	20	*	*	0.4	(Note 4)		OA + Reference
LM101A	2	75	1	0.5	3	±3	±22	
LM107	2	75	1	0.5	3	±3	±22	
LM108	2	2	1	0.3	0.4	±2	±20	
LM112	2	2	1	0.2	0.6	±2	±20	Compensated LM108
LM124A	2	50	*	*	3	3	32	Quad
LM158A	2	50	*	*	1.2	3	32	Dual
LP124	2	4	0.1	0.05	0.13	3	32	Quad
LH0020	2.5	250	*	*	5	±5	±22	
LF412	3	0.2	4	15	6.8	±6	±22	Dual
LM741A	3	80	1.5	0.7	2.8	±3	±22	
LH0022	4	0.01	1	3	3.5	±5	±22	
LF155	5	0.1	2.5	5	4	±5	±22	

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Military Temperature Range (−55°C to +125°C) Specs at T_A = 25°C (continued)								
LF156	5	0.1	5	12	7	±5	±22	
LF157	5	0.1	20	50	7	±5	±22	Minimum Gain of 5
LF147	5	0.2	4	13	11	±6	±22	Quad BiFet
LF412	5	0.2	4	15	6.8	±6	±18	Dual BiFet
LF442	5	0.1	1	1	0.5	±6	±18	Dual BiFet
LF444A	5	0.1	1	1	0.80	±6	±22	Quad BiFet
LH0086	5	0.5	3	10	15.5	±8	±18	Programmable Gain OA
LM124	5	150	*	*	3	3	32	Quad
LM143	5	20	1	2.5	4	±4	±40	
LM144	5	20	1	2.5	4	±4	±40	Minimum Gain of 10
LM146	5	100	1.2	0.4	2	±1.5	±22	(Note 5)
LM148	5	100	1	0.5	3.6	±5	±22	Quad
LM149	5	100	4	2	3.6	±5	±22	Minimum Gain of 5, Quad
LM158	5	150	*	*	1.2	3	32	Dual
LM192	5	150	*	*	2	3	32	Comparator and Op Amp
LM741	5	500	*	0.5	2.8	±3	±22	
LM1558	5	500	*	*	5	±3	±22	Dual
LM4250	5	50	0.2	0.2	0.1	±1	±18	(Note 5)
LH0042	20	0.025	1	3	3.5	±5	±22	

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Industrial Temperature Range (−25°C to +85°C) (Note 1)								
LMC669B	0.025	0.1	*	*	6	±8	±22	Autozero Block
LH0044B	0.05	30	0.4	0.06	4	±3	±20	
LH0044C	0.05	30	0.4	0.06	4	±3	±20	
LMC669C	0.05	0.1	*	*	6	±8	±22	Autozero Block
LM208A	0.5	2	1	0.3	0.6	±2	±20	
LH0052C	1	0.005	1	3	3.8	±5	±22	
LMC660A	2	0.02	1.5	1.7	2.2	5	15	Quad CMOS
LM10B(L)	2	20	*	*	0.4	(Note 4)		Op Amp and Reference
LM201A	2	75	1	0.5	3	±3	±22	
LM207	2	75	1	0.5	3	±3	±22	
LM208	2	2	1	0.3	0.6	±2	±20	
LM212	2	2	1	0.3	0.6	±2	±20	Compensated LM208
LM224A	3	80	*	*	2	3	32	Quad

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Industrial Temperature Range (−25°C to +85°C) (continued)								
LM258A	3	80	*	*	1.2	3	32	Dual
LF255	5	0.1	2.5	5	4	±5	±22	
LF256	5	0.1	5	12	7	±5	±22	
LF257	5	0.1	20	50	7	±5	±22	Minimum Gain of 5
LM224	5	150	*	*	2	3	32	Quad
LM258	5	150	*	*	1.2	3	32	Dual
LM292	5	250	*	*	2	3	32	Comparator and Op Amp
LH0020C	6	500	*	*	6	±5	±22	
LH0022C	6	0.025	1	3	4	±5	±22	
LM246	6	250	0.5	0.4	2.5	±2	±18	(Note 5)
LM248	6	200	1	0.5	4.5	±5	±18	Quad
LM249	6	200	4	2	4.5	±5	±18	Minimum Gain of 5, Quad
LH0086C	10	0.5	3	10	15.5	±8	±18	Programmable Gain 1 to 200
LH0042C	20	0.05	1	3	4	±5	±22	

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Commercial Temperature Range (0°C to +70°C) (Notes 1 and 2)								
LMC668A	0.005	0.06	1	2.5	3.5	*	18	Commutating Autozero
LMC668	0.01	0.06	1	2.5	3.5	*	18	Commutating Autozero
LMC669B	0.025	0.1	*	*	6	±8	±22	Autozero Block
LM607A	0.025	2	1.8	0.7	1.5	*	±22	
LMC669C	0.05	0.1	*	*	6	±8	±22	Autozero Block
LM607B	0.05	3	1.8	0.7	1.5	*	±22	
LM607	0.15	10	1.8	0.7	1.8	*	±22	
LF411A	0.5	0.2	4	15	2.8	±6	±22	
LF441A	0.5	0.05	1	1	0.2	±6	±22	
LM308A	0.5	7	1	0.3	0.8	±2	±20	
LM11C	0.6	0.1	*	0.3	0.8	*	±20	
LF412A	1	0.2	4	15	5.6	±6	±22	Dual
LF442A	1	0.05	1	1	0.4	±6	±22	Dual
LM604A	1	40	5	3	9	4	36	Multiplexed Op Amp
LF355A	2	0.05	2.5	5	4	±5	±22	
LF356A	2	0.05	5	12	10	±5	±22	
LF357A	2	0.05	20	50	10	±5	±22	Minimum Gain of 5

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Commercial Temperature Range (0°C to +70°C) (continued)								
LF411	2	0.2	4	15	3.4	±6	±22	
LF412	3	0.2	4	15	6.8	±6	±22	Dual
LM324A	3	100	*	*	3	3	32	Quad
LM358A	3	100	*	*	2	3	32	Dual
LM604	3	60	5	7	9	4	36	Multiplexed Op Amp
LM741E	3	80	1.5	0.7	2.8	±3	±22	
LM10C(L)	4	30	*	*	0.5	(Note 4)		OA and Reference
LP324	4	10	0.1	0.05	0.15	3	32	
LF347B	5	0.2	4	13	11	±6	±22	Quad
LF355B	5	0.1	2.5	5	4	±5	±22	
LF356B	5	0.1	5	12	4	±5	±22	
LF357B	5	0.1	20	50	7	±5	±22	
LF441	5	0.1	1	1	0.25	±6	±22	
LF442	5	0.1	1	1	0.5	±6	±22	Dual
LM11CL	5	0.2	*	0.3	0.8	*	±20	
LM392	5	250	*	*	2	3	32	
LM833	5	1000	10	5	8	*	±18	Dual Low Noise
LMC660	6	0.02	1.5	1.7	2.7	5	15	Quad CMOS
LM346	6	250	0.5	0.4	2.5	±1.5	±22	(Note 5)
LM348	6	200	1	0.5	4.5	±5	±18	
LM349	6	200	4	2	4.5	±5	±18	
LM741C	6	500	1.5	0.5	2.8	±3	±18	
LM1458	6	500	*	*	5.6	±3	±18	
LM4250C	6	75	0.2	0.2	0.1	±1	±18	(Note 5)
LM324	7	250	*	*	3	3	32	
LM358	7	250	*	*	2	3	32	
LM301A	7.5	250	1	0.5	3	±3	±18	
LM307	7.5	250	1	0.5	3	±3	±18	
LM308	7.5	7	1	0.3	0.8	±2	±18	
LM312	7.5	7	1	0.2	0.8	±2	±18	Compensated LM308
LM343	8	40	1	2.5	5	±4	±34	
LM344	8	40	1	2.5	5	±4	±34	Minimum Gain of 10
LF347	10	0.2	4	13	11	±6	±18	Quad BiFet
LF351	10	0.2	4	13	3.4	±6	±18	
LF353	10	0.2	4	13	6.8	±6	±18	Dual BiFet
LF355	10	0.2	2.5	5	4	±5	±18	
LF356	10	0.2	5	12	10	±5	±18	
LF357	10	0.2	20	50	10	±5	±18	Minimum Gain of 5

General Purpose Operational Amplifier Selection Guide (Continued)

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Commercial Temperature Range (0°C to +70°C) (continued)								
LF444	10	0.1	1	1	1	±6	±18	Quad BiFet
LF13741	15	0.2	1	0.5	4	*	±18	
TL081C	15	0.2	4	13	2.8	±6	±18	
TL082C	15	0.2	4	13	5.6	±6	±18	Dual BiFet

Part #	V_{OS} mV (Max)	I_B nA (Max)	GBW MHz (Typ)	Slew Rate V/μs (Typ)	Supply Current (Note 3) mA (Max)	Supply Voltage		Special Features
						Min V	Max V	
Automotive Temperature Range (−40°C to +85°C)								
LM604	3	60	7	3	9	4	36	Multiplexed Op Amp
LP2902	4	20	0.1	0.05	0.15	3	26	Quad
LM2902	7	250	*	*	3	3	26	Quad
LM2904	7	250	*	*	2	3	26	Quad
LM2924	7	250	*	*	2	3	26	Comparator Plus Op Amp

*Not Specified.

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: Those looking for a commercial part should also look at the Industrial Temp Range guide as many Hybrids are listed there.

Note 3: Supply current is for all amplifiers in a package.

Note 4: The LM10 has 2 versions: one a high voltage part, good to 45V and a low voltage part, good to 7V. Refer to the datasheet for more information.

Note 5: The LM146 and LM4250 are programmable amplifiers. The data shown is for $V_S = \pm 15V$ and $I_{SET} = 10\ \mu A$. Refer to the datasheets for more information.

National Semiconductor Corporation

Low I_{BIAS} Selection Guide

≤5 pA	≤20 pA	≤50 pA	≤100 pA	≤200 pA	≤500 pA	≤ 1 nA
T_A = 25°C						
LH0022	LMC668	LH0032A	LH0032	LF401A	LH4101	LH4104
LH0022C	LMC660	LF155A/156A	LF155/156	LF401	LH0032C	
LH0042		LF157A	LF157	LF400A	LH0086	
LH0042C		LF355A/356A	LF255/256	LF400	LH0086C	
LH0052		LF357A	LF257	TL081		
LH0052C		LF441A	LF355B/356B	LH0032AC		
LH0062		LF442A	LF357B	LF351		
		LF444A	LF441	LF411A/411		
		LM11	LF442	LF355/356		
			LF444	LF357		
			LM11C	LF147/347B/347		
			LH0062C	LF353		
				LF412A/412		
				LF13741		
				LM11CL		

Note: Datasheet should be referred to for conditions and more detailed information.

National Semiconductor Corporation

High Speed Operational Amplifier Selection Guide

Part #	Slew Rate V/μs (Typ)	GBW MHz (Typ)	V_{OS} mV (Max)	I_S mA (Max) (Note 2)	Notes
GBW ≥ 4 MHz, T_A = 25°C					
LH0024	500	70	8	15	
LH0032	500	70	15	22	FET Input
LM6361	300	50	20	6.8	
LM6364	300	175	9	6.8	Min Gain of 5
LM6365	300	725	7	6.8	Min Gain of 25
LH4101	250	40	15	40	Medium Power JFET
LF400	70	16	2.5	12	Fast Settling JFET
LF401	70	16	0.5	12	Precision Fast Settling JFET
LH0003	70	30	3	3	
LH0062	70	15	15	12	FET Input
LM318	70	15	10	10	
LF357	50	20	10	10	Min Gain of 5, JFET
LH4104	40	16	10	25	Medium Power Fast Settling JFET
LM359	30	30	*	22	Dual Current Mode (Norton) Amp
LF411	15	4	2	3.4	JFET
LF412	15	4	3	6.8	Dual JFET
LF347	13	4	10	11	Quad JFET
LF351	13	4	10	3.4	JFET
LF353	13	4	10	6.8	Dual JFET
LF356	12	4.5	10	10	JFET
LM833	7	15	5	8	Dual Low Noise

*Not specified.

Note 1: Datasheet should be referred to for conditions and more detailed information. Many versions with better DC specs are available in addition to those listed above.

Note 2: Supply current is for all amplifiers in a package.

National Semiconductor Corporation

Medium and High Power Operational Amplifier Selection Guide ($\geq$ 0.1A Output)

Part #	I_{OUT} A (Typ)	V_{OS} mV (Max)	I_S mA (Max)	Slew Rate V/μS (Typ)	PBW kHz (Typ)
LH4104	0.1	10	25	40	*
LH4101	0.1	15	40	250	*
LH0041	0.2	6	4	1	20
LH0061	0.5	15	15	25	1000
LH0021	1.0	6	4	1	20
LH0101A	2	3	35	10	300
LH0101	2	10	35	10	300
LM675	3	10	50	8	*
LM12(L)	(Note 2)	7	80	9	60
LM12C(L)	(Note 2)	15	120	9	60

*Not Specified

Note 1: Refer to Datasheet for conditions and more detailed information.

Note 2: I_{OUT} for the LM12 is dependent on the amount of power dissipated in the output transistor. The datasheet should be referred to, to determine amount of current available.

National Semiconductor Corporation

Special Amplifier Selection Guide

LH0045	Two Wire Transmitter
LH0082	20 MHz Transimpedance Amplifier
LH0086	Programmable Gain Operational Amplifier
LM359	Dual Current Mode (Norton) Amplifier
LM2900, 3900, 3301, 3401	Quad Current Mode (Norton) Amplifier
LM3080	Operational Transconductance Amplifier
LM13600	Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers
13700	Improved Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers
LM604	4 In, 1 Out Multiplexed Op Amp

Note: Refer to the datasheet for specifications.

National Semiconductor Corporation

Buffers
Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental.

$$\%\ \text{harmonic distortion} = \frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

National Semiconductor Corporation

Buffers Selection Guide (Notes 1 and 2)

Device Type	−3 dB MHz (Typ)	V_{OS} mV (Max)	I_S mA (Max)	Voltage Gain (Typ)	V_{OUT} V (Min)	S. R. V/μs (Typ)	I_{OUT} mA (Typ)
LM110, 210, 310	20	7.5	5.5	0.9999	±10	3.0	10
LH4001	25	500	10	0.97	±10	125	200
LH0002	30	±30	10	0.97	±10	100	200
LH0033	100	20	24	0.98	±9	1400	100
LH4002	200	50	35	0.85	±3	1250	40
LH0063	200	±50	65	0.93	±10	2400	250

*Not specified

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: 200°C Temp Range Parts are available. Consult local sales office for information.

National Semiconductor Corporation

Voltage Comparators Definition of Terms

Input Bias Current: The average of the two input currents.

Input Offset Current: The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

Input Offset Voltage: The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

Input Voltage Range: The range of voltage on the input terminals (common-mode) over which the offset specifications apply.

Logic Threshold Voltage: The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

Negative Output Level: The negative DC output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

Output Leakage Current: The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

Output Resistance: The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

Output Sink Current: The maximum negative current that can be delivered by the comparator.

Positive Output Level: The high output voltage level with a given load and the input drive equal to or greater than a specified value.

Power Consumption: The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

Response Time: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Saturation Voltage: The low-output voltage level with the input drive equal to or greater than a specified value.

Strobe Current: The current out of the strobe terminal when it is at the zero logic level.

Strobe Output Level: The DC output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

Strobe "ON" Voltage: The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

Strobe "OFF" Voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

Strobe Release Time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

Supply Current: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

Voltage Gain: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

National Semiconductor Corporation

Voltage Comparators Selection Guide

	Response Time (Typ) ns	V_{OS} mV(Max)	I_S mA(Max)	I_B nA(Max)	Comments
T_A = 25°C (Notes 1 and 2)					
LM361	12	5	25	30,000	High Speed w/Strobes
LM360	16	5	32	20,000	High Speed, Complementary Outputs
LM306	40	5	10	25,000	High Speed, High Drive
LM319	80	8	12.5	1000	High Speed Dual
LF311	200	10	7.5	0.15	FET Input
LM311	200	10	7.5	300	General Purpose Single
LM339	1300	5	2	400	General Purpose Quad
LM392	1300	10	1	400	One Comparator Plus One Op Amp
LM393	1300	5	2.5	250	General Purpose Dual
LM2903	1300	5	2.5	250	Automotive Dual
LM2901	1300	7	2	400	Automotive Quad
LP365	4000	9	0.30	200	Programmable Quad
LP311	4000	10	0.3	150	Low Power Single
LP339	5000	9	0.1	40	Low Power Quad

*Not Specified

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: This selection guide should be used to select for Response Time required. Industrial and Military Temperature Range types are available. The DC specs are for the lowest Commercial Grade available.

National Semiconductor Corporation

Instrumentation Amplifiers Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V2^2 + V3^2 + V4^2 + \ldots)^{1/2}\,(100\%)}{V1}$$

where V1 is the rms amplitude of the fundamental and V2, V3, V4, . . . are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).

National Semiconductor Corporation

Instrumentation Amplifiers Selection Guide

Part Number	Gain Error (Max)	Gain Linearity (Typ)	CMRR dB (Min)	I_B nA (Max)
		$T_A = 25°C$		
LH0036 μ Power	3%	0.03%	46	125
LH0038	3%	0.0001%	86	100
LH0084	0.3%	0.005%	80	0.500
LM363	2.5%	0.01%	90	10

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Linear 2 Databook
Selection Guides

Active Filters

Analog Switches/Multiplexers

Analog-to-Digital Converters

Digital-to-Analog Converters

Sample and Hold

Temperature Sensors

Voltage References

National Semiconductor Corporation

Active Filters
Definition of Terms

f_{CLK}: the switched capacitor filter external clock frequency.

f_o: center of frequency of the second order function complex pole pair. f_o is measured at the bandpass output of each ½ MF10, and it is the frequency of the bandpass peak occurrence.

Q: quality factor of the 2nd order function complex pole pair. Q is also measured at the bandpass output of each ½ MF10 and it is the ratio of f_o over the −3 dB bandwidth of the 2nd order bandpass filter. The value of Q is not measured at the lowpass or highpass outputs of the filter, but its value relates to the possible amplitude peaking at the above outputs.

H_{OBP}: the gain in (V/V) of the bandpass output at $f = f_o$.

H_{OLP}: the gain in (V/V) of the lowpass output of each ½ MF10 at $f \rightarrow 0$ Hz.

H_{OHP}: the gain in (V/V) of the highpass output of each ½ MF10 as $f \rightarrow f_{CLK}/2$.

Q_Z: the quality factor of the 2nd order function complex zero pair, if any. (Q_Z is a parameter used when an allpass output is sought and unlike Q it cannot be directly measured).

f_Z: the center frequency of the 2nd order function complex zero pair, if any. If f_Z is different from f_o, and if the Q_Z is quite high it can be observed as a notch frequency at the allpass output.

f_{notch}: the notch frequency observed at the notch output(s) of the MF10.

H_{ON_1}: the notch output gain as $f \rightarrow 0$ Hz.

H_{ON_2}: the notch output gain as $f \rightarrow f_{CLK}/2$.

National Semiconductor Corporation

Active Filter Selection Guide

Device #	Type	Function	Max Order	Max Freq Accuracy	Freq Range	Typ. Q Accuracy	Max F x Q
MF10 (S, T)	Universal	Universal	4th	±0.6%	0.1–30 kHz	±2%	200 kHz
MF8 (T)	Bandpass	Chebyshev Butterworth	4th	±1.0%	0.1–20 kHz	±2%	5 MHz
MF6 (S, T)	Lowpass	Butterworth	6th	±1.0	0.1–20 kHz	N/A	N/A
MF5 (S)	Universal	Universal	2nd	±1.0%	0.1–30 kHz	±6%	200 kHz
MF4 (S)	Lowpass	Butterworth	4th	±0.6%	0.1–20 kHz	N/A	N/A
*LMF100	Universal	Universal	4th	±0.6%	40 kHz	±2%	1.8 MHz
*LMF60	Lowpass	Butterworth	6th	±0.6%	40 kHz	N/A	N/A

S Surface Mount Available

T Extended Temperature Available

* Advance Information

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Analog Switch Definition of Terms

R_{ON}: Resistance between the output and the input of an addressed channel.

I_S: Current at any switch input. This is leakage current when the switch is ON.

I_D: Current at any switch input going into the switch. This is leakage current when the switch is OFF.

C_S: Capacitance between any open terminal "S" and ground.

C_D: Capacitance between any open terminal "D" and ground.

$I_D - I_S$: Leakage current that flows from the closed switch into the body. This leakage is the difference between the current I_D going into the switch and the current I_S going out of the switch.

t_{RAN}: Delay time when switching from one address state to another.

t_{ON}: Delay time between the 50% points of an enable input and the switch ON condition.

t_{OFF}: Delay time between the 50% points of the enable input and the switch OFF condition.

National Semiconductor Corporation

Analog Switch/Multiplexer Selection Guide

Part Number	Function	Logic Input	V_S (Typ)	T_{ON}/T_{OFF} ns (Typ)	R_{ON} Ω
AH5011	QUAD SPST	TTL, CMOS	—	150/300	100
AH5012		TTL, CMOS	—	150/300	150
CD4016		CMOS	±7.5	20/40	850
CD4066		CMOS	±7.5	25/50	280
LF11201/LF13201		TTL	±15	90/500	200
LF11202/LF13202		TTL	±15	90/500	200
LF11331/LF13331		TTL	±15	90/500	200
LF11332/LF13332		TTL	±15	90/500	200
LF11333/LF13333		TTL	±15	90/500	200
MM74HC4016		CMOS	±12	5/8	40
AH5020	DUAL SPDT	TTL, CMOS	—	150/300	150
CD4053	TRIPLE SPDT	CMOS	±7.5	160/75	300
MM74HC4053		CMOS	±6.0	15/16	40
AH5009	4-CHANNEL	TTL, CMOS	—	150/300	100
AH5010		TTL, CMOS	—	150/300	150
CD4052	4-CHANNEL	CMOS	±7.5	160/75	300
CD4529B	DIFFERENTIAL	CMOS	±7.5	50	350
LF13509		TTL, CMOS	±18	1600/200	350
MM74HC4052		CMOS	±6.0	15/16	40
CD4051	8-CHANNEL	CMOS	±7.5	160/75	300
CD4529B		CMOS	±7.5	50	350
LF13508		TTL, CMOS	±18	1600/200	350
MM74HC4051		CMOS	±6.0	15/16	40

National Semiconductor Corporation

Definition Of Terms A/D Converters

Conversion Time: The time required for a complete measurement by an analog-to-digital converter.

DC Common-Mode Error: This specification applies to ADCs with differential inputs. It is the change in the output code that occurs when the analog voltages on the two inputs are changed by an equal amount. It is expressed in LSBs.

Differential Nonlinearity: Ideally, any two adjacent digital codes correspond to measured analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. For example, a DAC with a 1.5 LSB output change for a 1 LSB digital code change exhibits ½ LSB differential non-linearity. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB will lead to a non-monotonic transfer function in a DAC and missing codes in an ADC.

Gain Error (Full Scale Error): For an ADC, the difference (usually expressed in LSBs) between the input voltage that should ideally produce a full scale output code and the actual input voltage that produces that code. For DACs, it is the difference between the output voltage (or current) with full scale input code and the ideal voltage (or current) that should exist with a full scale input code.

Gain Temperature Coefficient (Full Scale Temperature Coefficient): Change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

Integral Nonlinearity (Linearity Error): Worst case deviation from the line between the endpoints (zero and full scale). Can be expressed as a percentage of full scale or in fractions of an LSB.

LSB (Least-Significant Bit): In a binary coded system this is the bit that carries the smallest value or weight. Its value is the full scale voltage (or current) divided by 2^n, where n is the resolution of the converter.

Missing Codes: When an incremental increase or decrease in input voltage causes the converter to increment or decrement its numeric output by more than one LSB the converter is said to exhibit "missing codes". If there are missing codes, there is a numeric value on the output on the converter which cannot be reached by any input voltage value.

Monotonicity: A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction (or remains constant) for each increase in the input code. The converse is true for decreasing codes.

MSB (Most Significant Bit): In a binary coded system this is the bit that has the largest value or weight. Its value is one half of full scale.

Multiplying DAC: In a sense, every DAC is a multiplying DAC since the output voltage (or current) is equal to the reference voltage times a constant determined by the digital input code divided by 2^n (n is the number of bits of resolution). In a two quadrant multiplying DAC the reference voltage or the digital input code can change the output voltage polarity. If both the reference voltage and the digital code change the output voltage polarity four quadrant multiplication exists.

Offset Error (Zero Error): In a DAC, this is the output voltage that exists when the input digital code is set to give an ideal output of zero volts. In the case of an ADC, this is the difference between the ideal input voltage (½ LSB) and the actual input voltage that is needed to make the transition from zero to 1 LSB. All the digital codes in the transfer curve are offset by the same value. Many converters allow nulling of offset with an external potentiometer. Offset error is usually expressed in LSBs.

Power Supply Rejection (Power Supply Sensitivity): The sensitivity of a converter to changes in the dc power supply voltages.

Quantizing Error: The error inherent in all A/D conversions. Since even an "ideal" converter has finite resolution, any analog voltage that falls between two adjacent output codes will result in an output code that is inaccurate by up to ½ LSB.

Ratiometric Operation: Many A/D applications require a stable and accurate reference voltage against which the input voltage is compared. This approach results in an **absolute conversion**. Some applications, however, use transducers or other signal sources whose output voltages are proportional to some external reference. In these **ratiometric** applications, the reference for the signal source should be connected to the reference input of the converter. Thus, any variations in the source reference voltage will also change the converter reference voltage and produce an accurate conversion.

Resolution: The smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of analog levels is equal to 2^n. As an example, a 12-bit converter divides the analog signal into $2^{12} = 4096$ discrete voltage (or current) levels.

Settling Time: The time from a change in input code until a DAC's output signal remains within ± ½ LSB (or some other specified tolerance) of the final value.

National Semiconductor Corporation

A/D Converter Selection Guide

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range*			Package	Comments
							M	I	C		
A/D CONVERTER											
ADC0800	8	±2 LSB	50 μs	±5V	TTL, TRI-STATE	+5, −12	•		•	18-Pin DIP	
ADC0801	8	±¼ LSB	110 μs	5V	TTL, TRI-STATE	+5	•	•		20-Pin DIP	Differential Input
ADC0802	8	±½ LSB	110 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Differential Input
ADC0803	8	±½ LSB	110 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Differential Input
ADC0804	8	±1 LSB	110 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Differential Input
ADC0805	8	±1 LSB	110 μs	5V	TTL, TRI-STATE	+5		•		20-Pin DIP	Ratiometric Operation
ADC0808	8	±½ LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•		28-Pin DIP 28-Pin PCC	8-Channel MUX
ADC0809	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5		•		28-Pin DIP 28-Pin PCC	8-Channel MUX
ADC0811B	8	±½ LSB	32 μs	5V	TTL	+5		•	•	20-Pin DIP 20-Pin PCC	11-Channel Serial I/O
ADC0811C	8	±1 LSB	32 μs	5V	TTL	+5		•	•	20-Pin DIP 20-Pin PCC	11-Channel Serial I/O
ADC0816	8	±½ LSB	100 μs	5V	TTL, TRI-STATE	+5	•	•		40-Pin DIP	16-Channel MUX
ADC0817	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5		•		40-Pin DIP	16-Channel MUX
ADC0819B	8	±½ LSB	16 μs	5V	TTL	+5		•	•	28-Pin DIP 28-Pin PCC	19-Channel Serial I/O
ADC0819C	8	±1 LSB	16 μs	5V	TTL	+5		•	•	28-Pin DIP 28-Pin PCC	19-Channel Serial I/O
ADC0820B	8	±½ LSB	1.2 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Built-In Track and Hold Function
ADC0820C	8	±1 LSB	1.2 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin SO 20-Pin PCC	Built-In Track and Hold Function

A/D Converter Selection Guide (Continued)

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range*			Package	Comments
							M	I	C		
A/D CONVERTER (Continued)											
ADC0829B	8	±½ LSB	100 μs	5V	TTL, TRI-STATE	+5		•		28-Pin DIP	Additional Digital Input Capability
ADC0829C	8	±1 LSB	100 μs	5V	TTL, TRI-STATE	+5		•		28-Pin DIP	Additional Digital Input Capability
ADC0831B	8	±½ LSB	32 μs	5V	TTL	+5		•	•	8-Pin DIP	Serial I/O
ADC0831C	8	±1 LSB	32 μs	5V	TTL	+5		•	•	8-Pin DIP	Serial I/O
ADC0832B	8	±½ LSB	32 μs	5V	TTL	+5		•	•	8-Pin DIP	2-Channel Serial I/O
ADC0832C	8	±1 LSB	32 μs	5V	TTL	+5		•	•	8-Pin DIP	2-Channel Serial I/O
ADC0833B	8	±½ LSB	32 μs	5V	TTL	+5		•	•	14-Pin DIP	4-Channel Serial I/O
ADC0833C	8	±1 LSB	32 μs	5V	TTL	+5		•	•	14-Pin DIP	4-Channel Serial I/O
ADC0834B	8	±½ LSB	32 μs	5V	TTL	+5		•	•	14-Pin DIP	4-Channel Serial I/O
ADC0834C	8	±1 LSB	32 μs	5V	TTL	+5		•	•	14-Pin DIP	4-Channel Serial I/O
ADC0838B	8	±½ LSB	32 μs	5V	TTL	+5		•	•	20-Pin DIP 20-Pin PCC	8-Channel Serial I/O
ADC0838C	8	±1 LSB	32 μs	5V	TTL	+5		•	•	20-Pin DIP 20-Pin PCC	8-Channel Serial I/O
ADC0841B	8	±½ LSB	40 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP 20-Pin PCC	Differential Input, Internal Clock
ADC0841C	8	±1 LSB	40 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP 20-Pin PCC	Differential Input, Internal Clock
ADC0844B	8	±½ LSB	40 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	4-Channel MUX, Internal Clock
ADC0844C	8	±1 LSB	40 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	4-Channel MUX, Internal Clock
ADC0848B	8	±½ LSB	40 μs	5V	TTL, TRI-STATE	+5		•	•	28-Pin DIP 28-Pin PCC	8-Channel MUX, Internal Clock
ADC0848C	8	±1 LSB	40 μs	5V	TTL, TRI-STATE	+5		•	•	28-Pin DIP 28-Pin PCC	8-Channel MUX, Internal Clock
ADC1001C	10	±1 LSB	200 μs	5V	TTL, TRI-STATE	+5		•	•	20-Pin DIP	8-Bit Bus Compatible, Differential Input
ADC1005B	10	±½ LSB	50 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin PCC	8-Bit Bus Compatible, Differential Input

A/D Converter Selection Guide (Continued)

Part No.	Resolution (Bits)	Absolute Accuracy (Max)	Conversion Time	Input Voltage Range	Output Logic Levels	Supplies (V)	Temperature Range*			Package	Comments
							M	I	C		
A/D CONVERTER (Continued)											
ADC1005C	10	±1 LSB	50 μs	5V	TTL, TRI-STATE	+5	•	•	•	20-Pin DIP 20-Pin PCC	8-Bit Bus Compatible, Differential Input
ADC1021C	10	±1 LSB	200 μs	5V	TTL, TRI-STATE	+5		•	•	24-Pin DIP	Differential Input
ADC1025B	10	±½ LSB	50 μs	5V	TTL, TRI-STATE	+5	•	•	•	24-Pin DIP 28-Pin PCC	Differential Input
ADC1025C	10	±1 LSB	50 μs	5V	TTL, TRI-STATE	+5	•	•	•	24-Pin DIP 28-Pin PCC	Differential Input
ADC1205B	12+sign	±½ LSB	100 μs	±5V	TTL, TRI-STATE	+5, ±5		•	•	24-Pin DIP	8-Bit Bus Compatible, Differential Input
ADC1205C	12+sign	±1 LSB	100 μs	±5V	TTL, TRI-STATE	+5, ±5		•	•	24-Pin DIP	8-Bit Bus Compatible, Differential Input
ADC1210	12	±¾ LSB	200 μs	10.2V	CMOS	+5 to ±15	•	•		24-Pin DIP	
ADC1211	12	±2 LSB	200 μs	10.2V	CMOS	+5 to ±5	•	•		24-Pin DIP	
ADC1225B	12+sign	±½ LSB	100 μs	±5V	TTL, TRI-STATE	+5, ±5		•	•	28-Pin DIP	Differential Input
ADC1225C	12+sign	±1 LSB	100 μs	±5V	TTL, TRI-STATE	+5, ±5		•	•	28-Pin DIP	Differential Input
ADC3511	3½-Digit	0.05%	200 ms	2V	TTL, TRI-STATE	+5			•	24-Pin DIP	Integrating μP Compatible
ADC3711	3¾-Digit	0.05%	400 ms	2V	TTL, TRI-STATE	+5			•	24-Pin DIP	Integrating μP Compatible
LM131	V-F	0.01%	N/A	V_{CC} − 2V	Open Collector	+5 to +40	•	•	•	8-Pin DIP or TO-99 Can	Voltage-to-Frequency Converter 100 kHz Max
DIGITAL VOLTMETER											
ADD3501	3½-Digit	0.05%	200 ms	2V	7-Segment LED Drive	+5			•	28-Pin DIP	3½-Digit LED DVM
ADD3701	3½-Digit	0.05%	400 ms	2V	7-Segment LED Drive	+5			•	28-Pin DIP	3¾-Digit LED DVM

*Temperature ranges: "M" is −55°C to +125°C ambient; "I" is −40°C to +85°C or −25°C to +85°C; "C" is 0°C to +70°C.

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Definition of Terms D/A Converters

Conversion Time: The time required for a complete measurement by an analog-to-digital converter.

DC Common-Mode Error: This specification applies to ADCs with differential inputs. It is the change in the output code that occurs when the analog voltages on the two inputs are changed by an equal amount. It is expressed in LSBs.

Differential Nonlinearity: Ideally, any two adjacent digital codes correspond to measured analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. For example, a DAC with a 1.5 LSB output change for a 1 LSB digital code change exhibits ½ LSB differential non-linearity. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB will lead to a non-monotonic transfer function in a DAC and missing codes in an ADC.

Gain Error (Full Scale Error): For an ADC, the difference (usually expressed in LSBs) between the input voltage that should ideally produce a full scale output code and the actual input voltage that produces that code. For DACs, it is the difference between the output voltage (or current) with full scale input code and the ideal voltage (or current) that should exist with a full scale input code.

Gain Temperature Coefficient (Full Scale Temperature Coefficient): Change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

Integral Nonlinearity (Linearity Error): Worst case deviation from the line between the endpoints (zero and full scale). Can be expressed as a percentage of full scale or in fractions of an LSB.

LSB (Least-Significant Bit): In a binary coded system this is the bit that carries the smallest value or weight. Its value is the full scale voltage (or current) divided by 2^n, where n is the resolution of the converter.

Monotonicity: A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction (or remains constant) for each increase in the input code. The converse is true for decreasing codes.

MSB (Most Significant Bit): In a binary coded system this is the bit that has the largest value or weight. Its value is one half of full scale.

Multiplying DAC: In a sense, every DAC is a multiplying DAC since the output voltage (or current) is equal to the reference voltage times a constant determined by the digital input code divided by 2^n (n is the number of bits of resolution). In a two quadrant multiplying DAC the reference voltage or the digital input code can change the output voltage polarity. If both the reference voltage and the digital code change the output voltage polarity, four quadrant multiplication exists.

Offset Error (Zero Error): In a DAC, this is the output voltage that exists when the input digital code is set to give an ideal output of zero volts. In the case of an ADC, this is the difference between the ideal input voltage (½ LSB) and the actual input voltage that is needed to make the transition from zero to 1 LSB. All the digital codes in the transfer curve are offset by the same value. Many converters allow nulling of offset with an external potentiometer. Offset error is usually expressed in LSBs.

Power Supply Rejection (Power Supply Sensitivity): The sensitivity of a converter to changes in the dc power supply voltages.

Quantizing Error: The error inherent in all A/D conversions. Since even an "ideal" converter has finite resolution, any analog voltage that falls between two adjacent output codes will result in an output code that is inaccurate by up to ½ LSB.

Ratiometric Operation: Many A/D applications require a stable and accurate reference voltage against which the input voltage is compared. This approach results in an **absolute conversion**. Some applications, however, use transducers or other signal sources whose output voltages are proportional to some external reference. In these **ratiometric** applications, the reference for the signal source should be connected to the reference input of the converter. Thus, any variations in the source reference voltage will also change the converter reference voltage and produce an accurate conversion.

Resolution: The smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of analog levels is equal to 2^n. As an example, a 12-bit converter divides the analog signal into $2^{12} = 4096$ discrete voltage (or current) levels.

Settling Time: The time from a change in input code until a DAC's output signal remains within ± ½ LSB (or some other specified tolerance) of the final value.

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D/A Converter Selection Guide

Part No.	Resolution (Bits)	Linearity @ 25°C % (Max)	Settling Time (+½ LSB)	Supplies (V)	Temperature Range*			Package	Comments
					M	I	C		
ADC0852	8	0.19		5		•	•	8-Pin DIP	DAC, Comparator, Serial Input
ADC0854	8	0.19		5		•	•	14-Pin DIP	DAC, Comparator, Serial Input
DAC0800	8	0.19	100 ns	±5 to ±15	•		•	16-Pin DIP 16-Pin S.O.	High-Speed Multiplying
DAC0801	8	0.39	100 ns	±5 to ±15	•		•	16-Pin DIP 16-Pin S.O.	High-Speed Multiplying
DAC0802	8	0.10	100 ns	±5 to ±15	•		•	16-Pin DIP 16-Pin S.O.	High-Speed Multiplying
DAC0806	8	0.78	150 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	Multiplying
DAC0807	8	0.39	150 ns	±5 to ±15			•	16-Pin DIP 16-Pin S.O.	Multiplying
DAC0808	8	0.19	150 ns	±5 to ±15	•		•	16-Pin DIP 16-Pin S.O.	Multiplying
DAC0830	8	0.05	1 μs	5 to 15	•	•	•	20-Pin DIP 20-Pin S.O. 20-Pin PCC	μP Compatible 4-Quadrant Multiplying
DAC0831	8	0.10	1 μs	5 to 15			•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC0832	8	0.20	1 μs	5 to 15		•	•	20-Pin DIP 20-Pin S.O. 20-Pin PCC	μP Compatible 4-Quadrant Multiplying
DAC1000	10	0.05	500 ns	5 to 15	•	•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1001	10	0.1	500 ns	5 to 15			•	24-Pin DIP	μP Compatible Double Buffered
DAC1002	10	0.2	500 ns	5 to 15	•	•	•	24-Pin DIP	μP Compatible Double Buffered
DAC1006	10	0.05	500 ns	5 to 15	•	•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1007	10	0.1	500 ns	5 to 15		•	•	20-Pin DIP	μP Compatible Double Buffered
DAC1008	10	0.2	500 ns	5 to 15	•	•	•	20-Pin DIP	μP Compatible Double Buffered

D/A Converter Selection Guide (Continued)

Part No.	Resolution (Bits)	Linearity @ 25°C % (Max)	Settling Time (+½ LSB)	Supplies (V)	Temperature Range*			Package	Comments
					M	I	C		
DAC1020	10	0.05	500 ns	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1021	10	0.1	500 ns	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1022	10	0.2	500 ns	5 to 15	•	•	•	16-Pin DIP	4-Quadrant Multiplying
DAC1208	12	0.012	1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1209	12	0.024	1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1210	12	0.05	1 μs	5 to 15		•	•	24-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1218	12	0.012	1 μs	5 to 15		•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1219	12	0.024	1 μs	5 to 15		•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1220	12	0.05	500 ns	5 to 15	•	•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1221	12	0.1	500 ns	5 to 15			•	18-Pin DIP	4-Quadrant Multiplying
DAC1222	12	0.2	500 ns	5 to 15	•	•	•	18-Pin DIP	4-Quadrant Multiplying
DAC1230	12	0.012	1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1231	12	0.024	1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1232	12	0.05	1 μs	5 to 15		•	•	20-Pin DIP	μP Compatible 4-Quadrant Multiplying
DAC1265A	12	0.006	200 ns	±15	•		•	24-Pin DIP	High-Speed
DAC1265	12	0.012	200 ns	±15	•		•	24-Pin DIP	High-Speed
DAC1266A	12	0.006	200 ns	±12 to ±15	•		•	24-Pin DIP	High-Speed
DAC1266	12	0.012	200 ns	±12 to ±15	•		•	24-Pin DIP	High-Speed

*Ambient temperature range for "M" is −55°C to +125°C, "I" is −25°C to +85°C or −40°C to +85°C, "C" 0°C to +70°C.

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Sample and Hold Definition of Terms

Acquisition Time: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Time: The delay required between "Hold" command and an input analog transition, so that the transition does not affect the held output.

Dynamic Sampling Error: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold Settling Time: The time required for the output to settle within 1 mV of final value after the "hold" logic command.

Hold Step: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (DC) analog input voltage. Logic swing is 5V.

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Sample and Hold Selection Guide

	LF198A	LF398A	LF198	LF398	LF298	Units
Accuracy Gain/Offset Error	0.01	0.01	0.02	0.02	0.02	% Max
Offset Voltage	2	3	5	10	5	mV Max
Droop Rate (25°C)						
C_S = 1000 pF	30	30	30	30	30	mV/sec
C_S = 10000 pF	3	3	3	3	3	
Acquisition Time (25°C)						
C_S = 1000 pF	4	4	4	4	4	μs
C_S = 10000 pF	20	20	20	20	20	
Aperture Time (25°C)	25	25	25	25	25	ns
Temperature Range	−55 to +125	0 to +70	−55 to +125	0 to +70	−25 to +85	°C
Comment	Low Drift	Low Drift	General Purpose	General Purpose	Low Drift	

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Temperature Sensor Selection Guide

Part	Temp. Range	*Accuracy	Output Scale
LM34A	−50°F to +300°F	±2.0°F	10 mV/°F
LM34	−50°F to +300°F	±3.0°F	10 mV/°F
LM34CA	−40°F to +230°F	±2.0°F	10 mV/°F
LM34C	−40°F to +230°F	±3.0°F	10 mV/°F
LM34D	+32°F to +212°F	±4.0°F	10 mV/°F
LM35A	−55°C to +150°C	±1.0°C	10 mV/°C
LM35	−55°C to +150°C	±1.5°C	10 mV/°C
LM35CA	−40°C to +110°C	±1.0°C	10 mV/°C
LM35C	−40°C to +110°C	±1.5°C	10 mV/°C
LM35D	0°C to +100°C	±2.0°C	10 mV/°C
LM134-3	−55°C to +125°C	±3.0°C	$I_{SET} \propto$ °k
LM134-6	−55°C to +125°C	±6.0°C	$I_{SET} \propto$ °k
LM234-3	−25°C to +100°C	±3.0°C	$I_{SET} \propto$ °k
LM234-6	−25°C to +100°C	±6.0°C	$I_{SET} \propto$ °k
LM135A	−55°C to +150°C	±1.3°C	10 mV/°k
LM135	−55°C to +150°C	±2.0°C	10 mV/°k
LM235A	−40°C to +125°C	±1.3°C	10 mV/°k
LM235	−40°C to +125°C	±2.0°C	10 mV/°k
LM335A	−40°C to +100°C	±2.0°C	10 mV/°k
LM335	−40°C to +100°C	±4.0°C	10 mV/°k
LM3911	−25°C to +85°C	±10.0°C	10 mV/°k (or °F)

***Note:** Accuracy is measured over T(Min) to T(Max) uncalibrated

Note: The LM134/234/334 3-Terminal Adjustable current sources Datasheet can be found in Linear 1, Section 1.

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Voltage Reference Selection Guide

Shunt Type

Reverse Breakdown Voltage (V_R)	Device	Operating Temp. Range*	Voltage Tolerance Max, $T_A = 25°C$	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance (Typ)
				ppm/°C (Max)	Over Range		
1.22	LM113-2	M	±1%	50 (Typ)	−55°C to +125°C	500 μA to 20 mA	0.8
1.22	LM113-1	M	±2%	50 (Typ)	−55°C to +125°C	500 μA to 20 mA	0.8
1.22	LM113	M	±5%	100 (Typ)	−55°C to +125°C	500 μA to 20 mA	0.8
1.22	LM313	C	±5%	100 (Typ)	0°C to +70°C	500 μA to 20 mA	0.8
1.235	LM185BX-1.2	M	±1%	30	−55°C to +125°C	10 μA to 20 mA	1
1.235	LM185BY-1.2	M	±1%	50	−55°C to +125°C	10 μA to 20 mA	1
1.235	LM185-1.2	M	±1%	150	−55°C to +125°C	10 μA to 20 mA	1
1.235	LM285BX-1.2	I	±1%	30	−40°C to +85°C	10 μA to 20 mA	1
1.235	LM285BY-1.2	I	±1%	50	−40°C to +85°C	10 μA to 20 mA	1
1.235	LM285-1.2	I	±1%	150	−40°C to +85°C	10 μA to 20 mA	1
1.235	LM385BX-1.2	C	±1%	30	0°C to +70°C	15 μA to 20 mA	1
1.235	LM385BY-1.2	C	±1%	50	0°C to +70°C	15 μA to 20 mA	1
1.235	LM385B-1.2	C	±1%	150	0°C to +70°C	15 μA to 20 mA	1
1.235	LM385-1.2	C	+2%, −2.4%	150	0°C to +70°C	15 μA to 20 mA	1
1.24 to 5.3 (Adj.)	LM185B	M	±1%	150	−55°C to +125°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM185BX	M	±1%	50	−55°C to +125°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM185BY	M	±1%	50	−55°C to +125°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM285BX	I	±1%	30	−40°C to +85°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM285BY	I	±1%	50	−40°C to +85°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM285	I	±2%	150	−40°C to +85°C	10 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM385BX	C	±1%	30	0°C to +70°C	13 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM385BY	C	±1%	50	0°C to +70°C	13 μA to 20 mA	0.3
1.24 to 5.3 (Adj.)	LM385	C	±2%	150	0°C to +70°C	13 μA to 20 mA	0.3
2.49	LM136A	M	±1%	72	−55°C to +125°C	400 μA to 10 mA	0.4
2.49	LM136	M	±2%	72	−55°C to +125°C	400 μA to 10 mA	0.4
2.49	LM236A	I	±1%	72	−25°C to +85°C	400 μA to 10 mA	0.4
2.49	LM236	I	±2%	72	−25°C to +85°C	400 μA to 10 mA	0.4
2.49	LM336	I	±4%	54	0°C to +70°C	400 μA to 10 mA	0.4
2.49	LM336B	C	±2%	54	0°C to +70°C	400 μA to 10 mA	0.4
2.5	LM185BX-2.5	M	±1.5%	30	−55°C to +125°C	20 μA to 20 mA	1
2.5	LM185BY-2.5	M	±1.5%	50	−55°C to +125°C	20 μA to 20 mA	1
2.5	LM185B-2.5	M	±1.5%	150	−55°C to +125°C	20 μA to 20 mA	1
2.5	LM285BX-2.5	I	±1.5%	30	−40°C to +85°C	20 μA to 20 mA	1
2.5	LM285BY-2.5	I	±1.5%	50	−40°C to +85°C	20 μA to 20 mA	1
2.5	LM285-2.5	I	±1.5%	150	−40°C to +85°C	20 μA to 20 mA	1
2.5	LM385BX-2.5	C	±1.5%	30	0°C to +70°C	20 μA to 20 mA	1
2.5	LM385BY-2.5	C	±1.5%	50	0°C to +70°C	20 μA to 20 mA	1
2.5	LM385B-2.5	C	±1.5%	150	0°C to +70°C	20 μA to 20 mA	1
2.5	LM385-2.5	C	±3%	150	0°C to +70°C	20 μA to 20 mA	1

Shunt Type (Continued)

Reverse Breakdown Voltage (V_R)	Device	Operating Temp. Range*	Voltage Tolerance Max, T_A = 25°C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance (Typ)
				ppm/°C (Max)	Over Range		
5.0	LM136A	M	±1%	72	−55°C to +125°C	400 μA to 10 mA	0.8
5.0	LM136	M	±2%	72	−55°C to +125°C	400 μA to 10 mA	0.8
5.0	LM236A	I	±1%	72	−25°C to +85°C	400 μA to 10 mA	0.8
5.0	LM236	I	±2%	72	−25°C to +85°C	400 μA to 10 mA	0.8
5.0	LM336B	C	±2%	54	0°C to +70°C	400 μA to 10 mA	0.8
5.0	LM336	C	±4%	54	0°C to +70°C	400 μA to 10 mA	0.8
6.9	LM129A	M	+3%, −2%	10	−55°C to +125°C	600 μA to 15 mA	0.6
6.9	LM129B	M	+3%, −2%	20	−55°C to +125°C	600 μA to 15 mA	0.6
6.9	LM129C	M	+3%, −2%	50	−55°C to +125°C	600 μA to 15 mA	0.6
6.9	LM329B	C	±5%	50	0°C to +70°C	600 μA to 15 mA	0.8
6.9	LM329C	C	±5%	20	0°C to +70°C	600 μA to 15 mA	0.8
6.9	LM329D	C	±5%	100	0°C to +70°C	600 μA to 15 mA	0.8
6.95	LM199A	M	±2%	0.5	−55°C to +125°C	500 μA to 10 mA	0.5
6.95	LM199A-20	M	Same as LM199A with 20 ppm guaranteed long term drift.				
6.95	LM199	M	±2%	1.0	−55°C to +125°C	500 μA to 10 mA	0.5
6.95	LM299A	I	±2%	0.5	−25°C to +85°C	500 μA to 10 mA	0.5
6.95	LM299A-20	I	Same as LM299A with 20 ppm guaranteed long term drift.				
6.95	LM299	I	±2%	1	−25°C to +85°C	500 μA to 10 mA	0.5
6.95	LM399A	C	±5%	1	0°C to +70°C	500 μA to 10 mA	0.5
6.95	LM399A-50	C	Same as LM399A with 50 ppm guaranteed long term drift.				
6.95	LM399	C	±5%	2	0°C to +70°C	500 μA to 10 mA	0.5
6.95	LM3999	C	±5%	5	0°C to +70°C	600 μA to 10 mA	0.6

*C (Commercial) = 0°C to 70°C, I (Industrial) = −25°C to +85°C for the LM236 and LM299, I = −40°C to +85°C for all others.
M (Military) = −55°C to +125°C

Current References

Output Current Range	Device	Operating Temperature Range	Set Current Error			Operating Voltage Range	Set Current Temperature Dependence*
			2 μA to 10 μA	10 μA to 1 mA	1 mA to 5 mA		
2 μA to 10 mA	LM134	−55°C to +125°C	±8%	±3%	±5%	1V to 40V	0.96T to 0.104T
2 μA to 10 mA	LM134-3	−55°C to +125°C	N/A	±1%	N/A	1V to 40V	0.98T to 0.102T
2 μA to 10 mA	LM134-6	−55°C to +125°C	N/A	±2%	N/A	1V to 40V	0.97T to 0.103T
2 μA to 10 mA	LM234	−25°C to +100°C	±8%	±3%	±5	1V to 40V	0.96T to 0.104T
2 μA to 10 mA	LM234-3	−25°C to +100°C	N/A	±1%	N/A	1V to 40V	0.98T to 0.102T
2 μA to 10 mA	LM234-6	−25°C to +100°C	N/A	±2%	N/A	1V to 40V	0.97T to 0.103T
2 μA to 10 mA	LM334	0°C to +70°C	±12%	±6%	±8%	1V to 40V	0.96T to 0.104T

*Set current changes linearly with temperature at a rate of 0.33%/°C.

Series Type (Buffered Output)

Output Voltage	Device	Oper. Temp. Range*	Voltage Tolerance Max, T_A = 25°C	Temperature Drift		Load Reg. ppm/mA	Over Current Range	Quiescent Current (mA)
				ppm/°C (Max)	Over Range			
2.5	LM368Y-2.5	C	±0.2%	20	0°C to +70°C	25	0 mA to +10 mA	0.55
2.5	LM368-2.5	C	±0.2%	30	0°C to +70°C	25	0 mA to +10 mA	0.55
5.0	LM168BY-5.0	M	±0.05%	10	−55°C to +125°C	10	−10 mA to +10 mA	0.35
5.0	LM268BY-5.0	I	±0.05%	15	−40°C to +85°C	10	−10 mA to +10 mA	0.35
5.0	LM368BY-5.0	C	±0.1%	20	0°C to +70°C	10	−10 mA to +10 mA	0.35
5.0	LM368-5.0	C	±0.1%	30	0°C to +70°C	10	−10 mA to +10 mA	0.35
10	LM169B	M	±0.05%	3	−55°C to +125°C	8	−10 mA to +10 mA	1.8
10	LM168BY-10	M	±0.05%	10	−55°C to +125°C	10	−10 mA to +10 mA	0.35
10	LH0070-2	M	±0.05%	8	−40°C to +85°C	60	0 to 5 mA	5
10	LM169	M	±0.05%	5	−55°C to +125°C	8	−10 mA to +10 mA	1.8
10	LM581U	M	±0.05%	10	−55°C to +125°C	50	0 mA to 5 mA	1.8
10	LH0070-0	M	±0.1%	40	−40°C to +85°C	60	0 mA to 5 mA	5
10	LM581T	M	±0.1%	10	−55°C to +125°C	50	0 mA to 5 mA	1.8
10	LH0070-1	M	±0.1%	20	−40°C to +85°C	60	0 mA to 5 mA	5
10	LM581S	M	±0.3%	30	−55°C to +125°C	50	0 mA to 5 mA	1.8
10	LM268BY-10	I	±0.05%	15	−40°C to +85°C	10	−10 mA to +10 mA	0.35
10	LM581L	C	±0.05%	5	0°C to +70°C	50	0 mA to 5 mA	1.8
10	LM369C	C	±0.05%	10	0°C to +70°C	8	−10 mA to +10 mA	1.8
10	LM369	C	±0.05%	5	0°C to +70°C	8	−10 mA to +10 mA	1.8
10	LM369B	C	±0.05%	3	0°C to +70°C	8	−10 mA to +10 mA	1.8
10	LM581K	C	±0.1%	10	0°C to +70°C	50	0 mA to 5 mA	1.8
10	LM368Y-10	C	±0.1%	20	0°C to +70°C	10	−10 mA to +10 mA	0.35
10	LM368-10	C	±0.1%	30	0°C to +70°C	10	−10 mA to +10 mA	0.35
10	LM369D	C	±0.1%	30	0°C to +70°C	8	−10 mA to +10 mA	2
10	LM581J	C	±0.3%	30	0°C to +70°C	50	0 mA to 5 mA	1.8
10.24	LH0071-2	M	±0.05%	8	−40°C to +85°C	60	0 mA to 5 mA	5
10.24	LH0071-1	M	±0.1%	20	−40°C to +85°C	60	0 mA to 5 mA	5
10.24	LH0071-0	M	±0.1%	30	−40°C to +85°C	60	0 mA to 5 mA	5

*C (Commercial) = 0°C to 70°C, I (Industrial) = −40°C to +85°C, M (Military) = −55°C to +125°C

Low Current Reference Diodes

Output Voltage	Device	Operating Temp. Range*	Voltage Tolerance Max, T_A = 25°C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance (Typ)
				ppm/°C (Max)	Over Range		
3.0	LM103-3.0	M	±10%	−1700	−55°C to +125°C	10 μA to 10 mA	25
3.3	LM103-3.3	M	±10%	−1500	−55°C to +125°C	10 μA to 10 mA	25
3.6	LM103-3.6	M	±10%	−1400	−55°C to +125°C	10 μA to 10 mA	25
3.9	LM103-3.9	M	±10%	−1300	−55°C to +125°C	10 μA to 10 mA	25

*M (Military) = −55°C to +125°C

"Reference Grade" Voltage Regulators*

Output Voltage	Device	Operating Temperature Range	Voltage Tolerance Max, T_A = 25°C	Output Variation Over Operating Range	Load Reg. ppm/mA	Line Reg. ppm/V	Output Current (Max)	Quiescent Current
Adjustable:	LP2951	−55°C to +150°C	±0.5%	±0.5%	100	42	100 mA	120 μA
1.235V to 30V	LP2951AC	−40°C to +125°C	±0.5%	±0.5%	100	42	100 mA	120 μA
	LP2951C	−40°C to +125°C	±1%	±1%	200	83	100 mA	120 μA
Programmable:	LH0075	−55°C to +125°C	±0.5%	±0.14% (Typ)	15	200	200 mA	8 mA
5V, 6V, 10V, 12V, 15V	LH0075C	0°C to +70°C	±1%	±0.3% (Typ)	25	400	200 mA	10 mA
Programmable								
−5V, −6V, −10V	LH0076	−55°C to +125°C	±0.5%	±0.14% (Typ)	15	200	200 mA	15 mA
−10V, −15V	LH0076C	0°C to +70°C	±1%	±0.3% (Typ)	25	400	200 mA	15 mA
5V	LP2950AC	−40°C to +125°C	±0.5%	±0.5%	100	42	100 mA	120 μA
5V	LP2950C	−40°C to +125°C	±1%	±1%	200	83	100 mA	120 μA

*For more information on these circuits, refer to the Voltage Regulator section of the Databook.

Section 1

Audio Circuits

Section 1 Contents

***Devices Not Covered In Last Publication**

National Semiconductor Corporation

Audio Circuits Definition of Terms

Amplifier

Class A

A class A transistor audio amplifier refers to an amplifier with a single output device that has a collector flowing for the full 360° of the input cycle.

Class B

The most common type of audio amplifier that basically consists of two output devices each of which conducts for 180° of the input cycle.

Class C

In a class C amplifier the collector current flows for less than 180°. Although highly efficient, high distortion results and the load is frequently tuned to minimize this distortion (primarily used in R.F. power amplifiers).

Class D

A switching or sampling amplifier with extremely high efficiency (approaching 100%). The output devices are used as switches, voltage appearing across them only while they are off, and current flowing only when they are saturated.

Crossover Distortion

Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current allowing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for I/Cs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion for negative going transition through zero at the higher audio frequencies.

Dolby B

Dolby B is a simplified version of the Dolby A professional quality noise reduction system. The amplitude of low level signals over a selected frequency range is increased prior to recording to enhance them above tape noise. On playback the original levels are restored causing a corresponding reduction in the audible tape noise. The major difference with Dolby A which used four frequency bands, is the use of a single variable frequency band with a cut-off frequency that increases in the presence of high level high frequency signals.

Dolby Level

Because of the complementary nature of the Dolby B noise reduction system, the audio channel between the encoder and the decoder must have a fixed gain such that the decoding signal level is within 2 dB of the encoding signal level. Also if recordings are interchangeable the signals in the noise reduction system must be related to the levels in the audio channel. Dolby level provides this reference and corresponds to a specified tape flux density when recorded with a 400 Hz tone. For reel to reel and eight track cartridge tapes this is 185 nWb/m, and for cassettes Dolby level is 200 nWb/m.

Large-Signal Voltage Gain

The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Resistance

The ratio of the change in output voltage to the change in output current with the output around zero.

Output Voltage Swing

The peak output voltage swing, referred to zero, that can be obtained without clipping.

Power Bandwidth

The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 6 dB below the rated output. For example, an amplifier rated at 60 watts with $\leq$0.25% THD, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30 watts.

Power Supply Rejection

The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Slew Rate

The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Supply Current

The current required from the power supply to operate the amplifier with no load and the output at zero.

Thermal Resistance (R_{TH})

An analogy for heat transfer where the ability of a heat conductive system to transfer heat is described in similar terms to those used in an electrical system for power dissipated in a resistor with a given applied voltage. The thermal resistance is given by the temperature differential established when a given amount of power is being dissipated ($\theta = T1 - T2/P_D$) with units of °C/watt.

National Semiconductor Corporation

Audio Selection Guide

PREAMPLIFIERS

	Application			Package	Voltage Range	Equivalent Input Noise	THD	PSR	Input Coupling	Notes
	Portable	Home	Auto							
LM381	•	•		14 Pin DIP	9V–40V	0.5 μV	0.1%	120 dB	AC	Stereo
LM382	•	•	•	14 Pin DIP	9V–40V	0.8 μV	0.1%	120 dB	AC	Stereo
LM387	•	•	•	8 Pin DIP	9V–30V	0.65 μV	0.1%	110 dB	AC	Stereo
LM1818	•	•	•	20 Pin DIP	3.5V–18V	0.85 μV	0.05%	85 dB	AC	Tape System
LM1837	•	•	•	18 Pin DIP	4V–18V	0.6 μV†	0.03%	105 dB	DC	Autoreverse
LM1897	•	•	•	16 Pin DIP	4V–18V	0.6 μV†	0.03%	105 dB	DC	Few Externals
LM833 (Note 1)		•	•	8 Pin DIP 8 Pin SO	±5V–±15V	0.5 μV	0.002%	100 dB	DC	Low Noise Dual Op Amp
LM837 (Note 1)		•	•	14 Pin DIP 14 Pin SO	±5V–±15V	0.5 μV	0.002%	100 dB	DC	Low Noise Quad Op Amp Drives 600Ω Load

†CCIR/ARM in DIN circuit referred to unity gain at 2 kHz.

Note 1: Data sheet in Linear 1.

AUDIO POWER AMPLIFIERS

	Application			Package	Power*			@ Voltage	Bridgeable	THD*	Input Noise*	Single/ Dual	Notes
	Portable	Home	Auto		8Ω	4Ω	2Ω						
LM380		•		8 Pin DIP 14 Pin DIP	2.5W			18V		0.2%		Single	See AN-69
LM383	•		•	5 Pin TO-220		5.5W	8.6W	14.4V	Yes	0.2%	2 μV	Single	Protected
LM384		•		14 Pin DIP	5.5W			22V		0.25%		Single	Fixed Gain
LM386	•	•		8 Pin DIP 8 Pin SO		0.33W		6V		0.2%		Single	4V Operation
LM388	•			14 Pin DIP	2.2W			12V	Yes	0.1%		Single	Minimum Externals
LM389	•			18 Pin DIP		0.33W		6V		0.2%		Single	Includes Transistor Array
LM390	•			14 Pin DIP		1W		6V	Yes	0.2%		Single	Battery Operation
LM391		•		16 Pin DIP				60V–100V		0.01%	3 μV	Single	Power Driver
LM1877	•	•	•	14 Pin DIP	3W			20V		0.05%	2.5 μV	Dual	6V–24V
LM2877	•	•	•	11 Pin SIP	4.5W			20V		0.07%	2.5 μV	Dual	Single-In-Line Package
LM1895	•	•	•	8 Pin DIP		1.1W		6V		0.2%	1.4 μV	Single	Low AM Radiation
LM2895	•	•	•	11 Pin SIP		4.3W		12V		0.15%	1.4 μV	Single	3V–15V

AUDIO POWER AMPLIFIERS (Continued)

	Application			Package	Power*			@ Voltage	Bridgeable	THD*	Input Noise*	Single/ Dual	Notes
	Portable	Home	Auto		8Ω	4Ω	2Ω						
LM1896	•	•	•	14 Pin DIP		1.1W		6V	Yes	0.1%	1.4 μV	Dual	Low AM Radiation
LM2896	•	•	•	11 Pin SIP		2.5W		9V	Yes	0.1%	1.4 μV	Dual	No Pops
LM2002	•		•	5 Pin TO-220		5.2W	8W	14.4V	Yes	0.1%	2 μV	Single	Protected
LM2878		•		11 Pin SIP	5.5W			22V	Yes	0.15%	2.5 μV	Dual	6V–32V
LM831	•			16 Pin DIP 20 Pin SO	0.44W			3V	Yes	0.2%	1.3 μV	Dual	1.8V–6V
LM12 (Note 1)		•		TO-3	50W	85W		±30V		0.01%		Single	Power Op Amp
LM675 (Note 1)		•		5 Pin TO-220	20W			±25V			3 μV	Single	Power Op Amp
LM1875		•		5 Pin TO-220	20W			±25V		0.015%	3 μV	Single	Low Crossover Distortion
LM2005			•	11 Pin TO-220		20W		14.4V	Yes	0.3%	1.5 μV	Dual	Protected
LM2879		•		11 Pin TO-220	8W			28V	Yes	0.05%	2.5 μV	Dual	6V–32V

*Note that all values shown are typical. Please refer to data sheets for test conditions.

Note 1: Data sheet in Linear 1.

AUDIO CONTROLS

	Application			Package	Voltage Range	Volume Control Range	Signal to Noise	THD	Separation	Notes
	Portable	Home	Auto							
LM1035/ LM1036	•	•	•	20 Pin DIP	8V–18V	80 dB	80 dB	0.05%	75 dB	Dual DC Controlled Tone/Volume/Balance
LM1037	•	•	•	18 Pin DIP	5V–30V		100 dB	0.04%	100 dB	DC Audio Switch
LM1038	•	•	•	18 Pin DIP	5V–30V		100 dB	0.04%	100 dB	BCD Logic Control
LM13600 (Note 1)	•	•	•	16 Pin DIP	±2V–±18V			0.5%	100 dB	Transconductance Amplifiers
LM13700 (Note 1)	•	•	•	16 Pin SO						
LM3080 (Note 1)	•	•	•	8 Pin DIP	±2V–±18V					Transconductance Amplifier
LM1040	•	•	•	24 Pin DIP	9V–16V	75 dB	80 dB	0.06%	75 dB	Dual DC Controlled Tone/Volume/Balance Stereo Enhancement
LMC835		•	•	28 Pin DIP	±2.5V–±8V		114 dB	*		7 Band Graphic Equalizer MICROWIRE™ Controlled
LMC1992/ LMC1993 (Note 2)		•	•	28 Pin DIP	7V–15V	80 dB	105 dB	0.03%	95 dB	Stereo Volume/ Tone/Fade/Select MICROWIRE™ Controlled

*Distortion determined by external op amps.

Note 1: Data sheet in Linear 1.

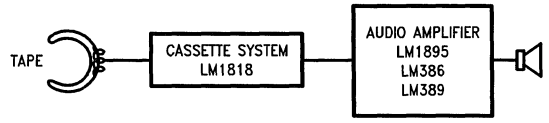
Note 2: LMC1992 selects 4 inputs.
LMC1993 selects 3 inputs and has a loudness control.

NOISE REDUCTION

	Application			Package	Voltage Range	NR Type	NR Effect*	Encoding Required	Single/ Dual/	Decode S/N*	Notes
	Portable	Home	Auto								
LM1131	•	•	•	18 Pin DIP	7V–20V	Dolby	10 dB	Yes	Dual	90 dB	DC Switched
LM1894	•	•	•	14 Pin DIP, SO	4.5V–18V	DNR	12 dB	No	Dual	76 dB	NSC System
LM1112	•	•	•	16 Pin DIP	6V–20V	Dolby	10 dB	Yes	Single	83 dB	
LM1141	•	•	•	28 Pin DIP, Quad	5V–16V	Dolby		Yes	Single		Dolby B/C
LM832	•			14 Pin DIP, SO	1.5V–9V	DNR	12 dB	No	Dual	76 dB	NSC System

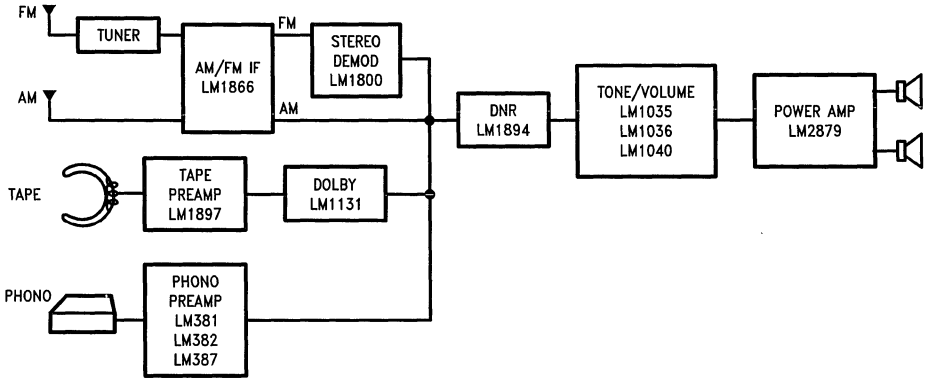
*Note that all values shown are typical. Please refer to data sheets for test conditions.

Monaural Cassette Player



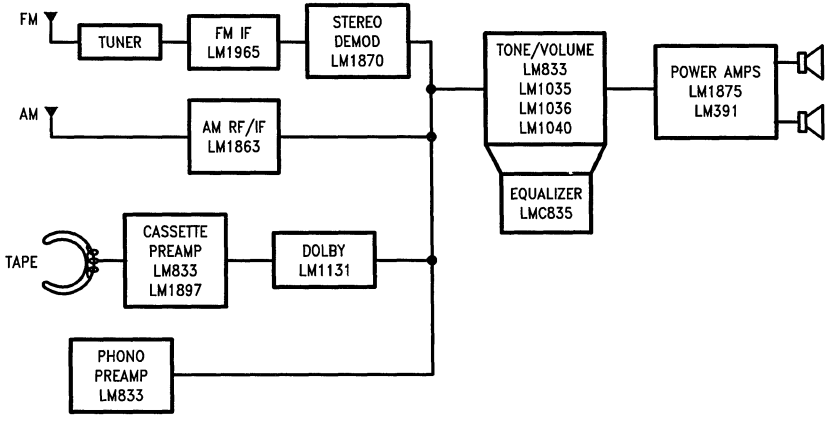
TL/XX/0013–1

Home Stereo System (Audio Power < 10W)



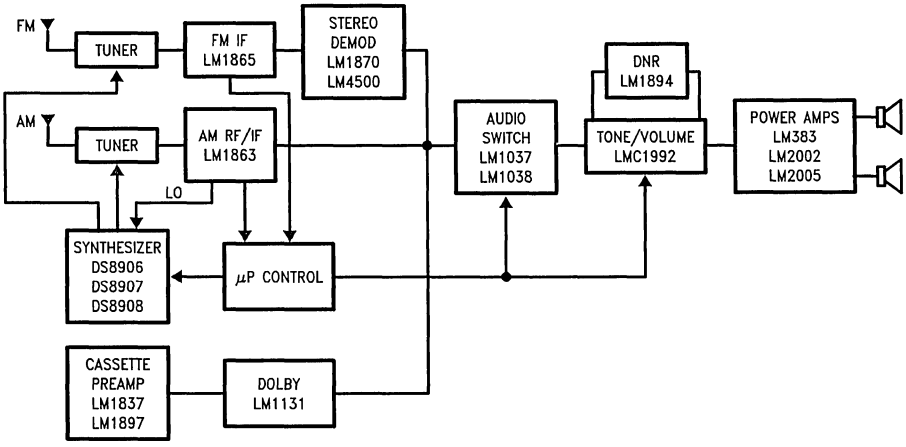
TL/XX/0013–2

Home Component Stereo (Audio Power > 10W)



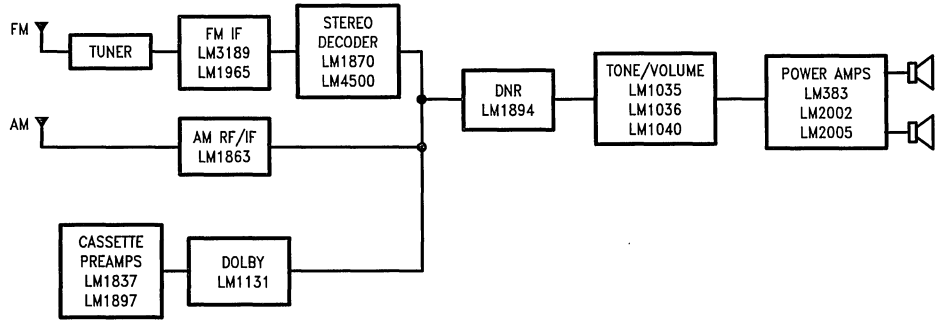
TL/XX/0013–3

Automotive Radio (Electronically Tuned)



TL/XX/0013–4

Auto Radio (Manually Tuned)



TL/XX/0013–5

National Semiconductor Corporation

LM377 Dual 2 Watt Audio Amplifier

General Description

The LM377 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, and AM-FM stereo receivers, etc.

The LM377 will deliver 2W/channel into 8 or 16Ω loads. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown. For more information, see AN-125.

Features

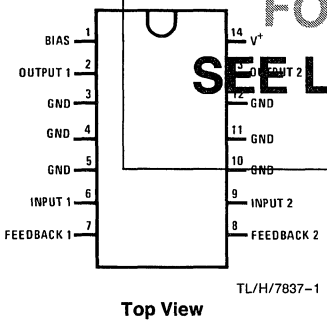
- A_{VO} typical 90 dB
- 2W per channel
- 70 dB ripple rejection
- 75 dB channel separation
- Internal stabilization
- Self centered biasing
- 3 MΩ input impedance
- 10–26V operation
- Internal current limiting
- Internal thermal protection

Applications

- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Connection Diagram

Dual-In-Line Package



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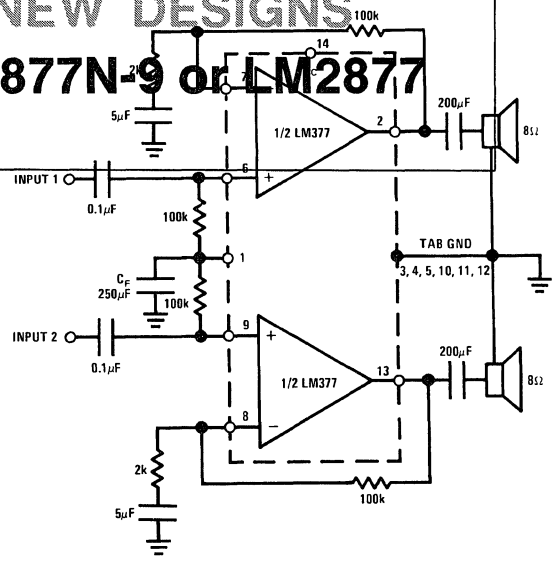
Top View

Order Number LM377N
See NS Package Number N14A

Typical Application

Simple Stereo Amplifier



TL/H/7837–2

National Semiconductor Corporation

LM378 Dual 4 Watt Audio Amplifier

General Description

The LM378 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, and AM-FM stereo receivers, etc.

The LM378 will deliver 4W channel into 8 or 16Ω loads. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown. For more information see AN-125.

Features

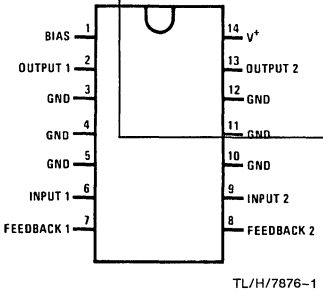
- A_{VO} typical 90 dB
- 4W per channel
- 70 dB ripple rejection
- 75 dB channel separation
- Internal stabilization
- Self centered biasing
- 3 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Application

- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Connection Diagram

Dual-In-Line Package



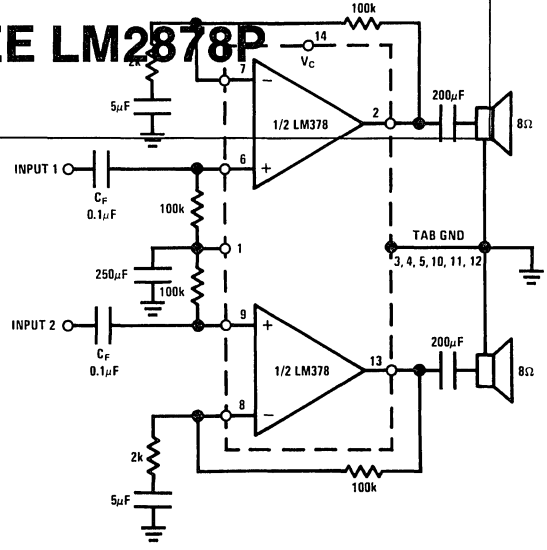
TL/H/7876–1

Top View

Order Number LM378N
See NS Package Number N14A

Typical Application

Simple Stereo Amplifier



TL/H/7876–2

National Semiconductor Corporation

LM380 Audio Power Amplifier

General Description

The LM380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self centering to one half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

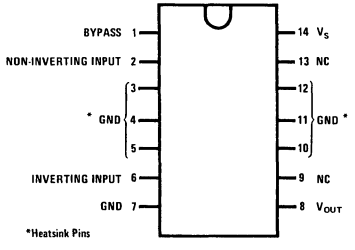
Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters, etc.

A selected part for more power on higher supply voltages is available as the LM384. For more information see AN-69.

Features

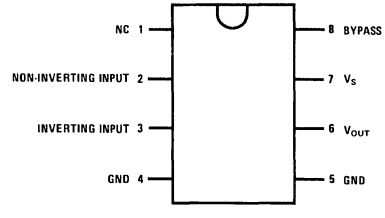
- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package

Connection Diagrams (Dual-In-Line Packages, Top View)



TL/H/6977–1

Order Number LM380N
See NS Package Number N14A

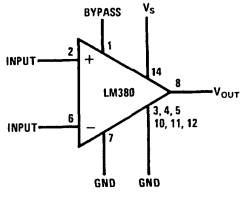


TL/H/6977–2

Order Number LM380N-8
See NS Package Number N08E

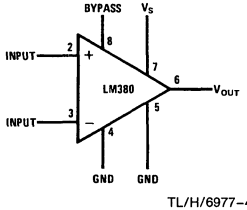
Block and Schematic Diagrams

LM380N

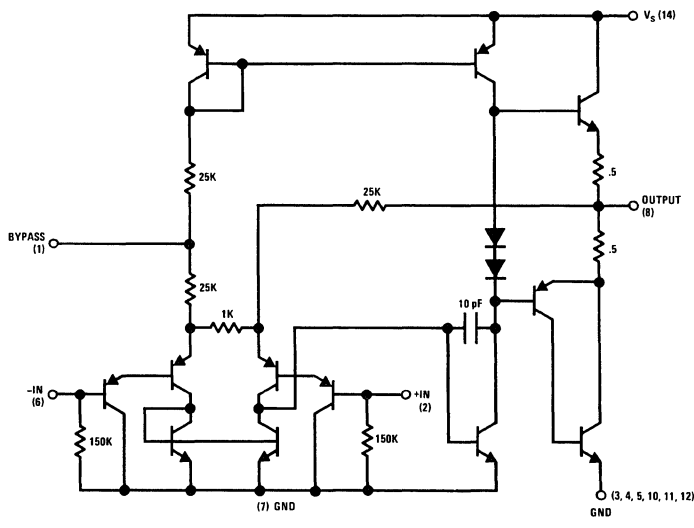


TL/H/6977–3

LM380N-8



TL/H/6977–4



TL/H/6977–5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	22V
Peak Current	1.3A
Package Dissipation 14-Pin DIP (Notes 6 and 7)	8.3W
Package Dissipation 8-Pin DIP (Notes 6 and 7)	1.67W
Input Voltage	±0.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	+260°C
ESD rating to be determined	

Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$P_{OUT(RMS)}$	Output Power	$R_L = 8\Omega$, THD = 3% (Notes 3, 4)	2.5			W
A_V	Gain		40	50	60	V/V
V_{OUT}	Output Voltage Swing	$R_L = 8\Omega$		14		V_{p-p}
Z_{IN}	Input Resistance			150k		Ω
THD	Total Harmonic Distortion	(Notes 4, 5)		0.2		%
PSRR	Power Supply Rejection Ratio	(Note 2)		38		dB
V_S	Supply Voltage		10		22	V
BW	Bandwidth	$P_{OUT} = 2W$, $R_L = 8\Omega$		100k		Hz
I_Q	Quiescent Supply Current			7	25	mA
V_{OUTQ}	Quiescent Output Voltage		8	9.0	10	V
I_{BIAS}	Bias Current	Inputs Floating		100		nA
I_{SC}	Short Circuit Current			1.3		A

Note 1: V_S = 18V and T_A = 25°C unless otherwise specified.

Note 2: Rejection ratio referred to the output with C_{BYPASS} = 5 μF.

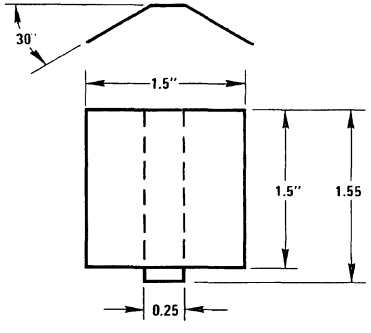
Note 3: With device Pins 3, 4, 5, 10, 11, 12 soldered into a $1/16$" epoxy glass board with 2 ounce copper foil with a minimum surface of 6 square inches.

Note 4: C_{BYPASS} = 0.47 μfd on Pin 1.

Note 5: The maximum junction temperature of the LM380 is 150°C.

Note 6: The package is to be derated at 15°C/W junction to heat sink pins for 14-pin pkg; 75°C/W for 8-pin.

Heat Sink Dimensions

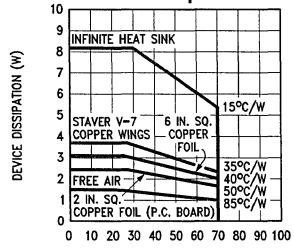


Staver Heat Sink #V-7
Staver Company
41 Saxon Ave.
P.O. Drawer H
Bayshore, NY 11706
Tel: (516) 666-8000
Copper Wings
2 Required
Soldered to
Pins 3, 4, 5,
10, 11, 12
Thickness 0.04
Inches

TL/H/6977–6

Typical Performance Characteristics

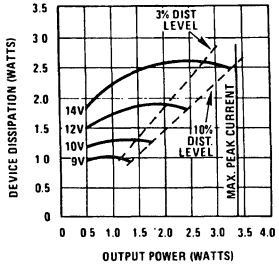
Maximum Device Dissipation vs Ambient Temperature



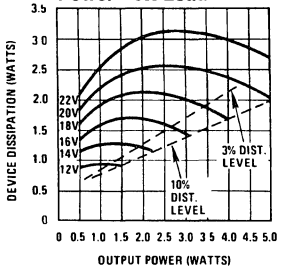
Note: 2 oz. copper foil, single-sided PC board.

TL/H/6977–12

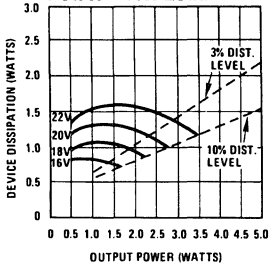
Device Dissipation vs Output Power—4Ω Load



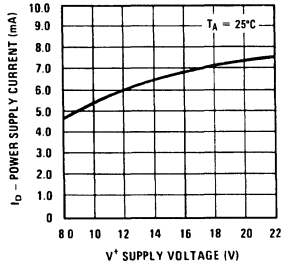
Device Dissipation vs Output Power—8Ω Load



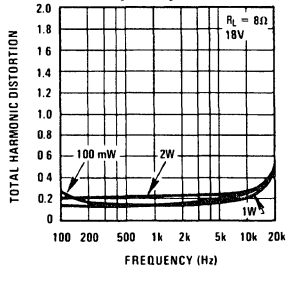
Device Dissipation vs Output Power—16Ω Load



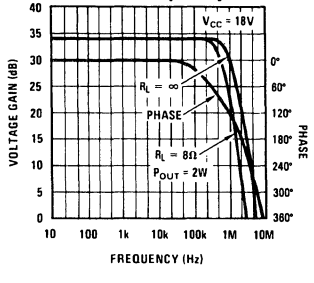
Power Supply Current vs Supply Voltage



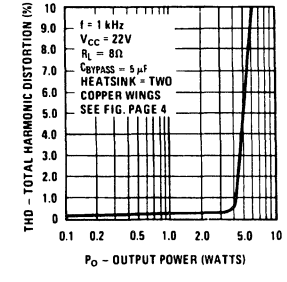
Total Harmonic Distortion vs Frequency



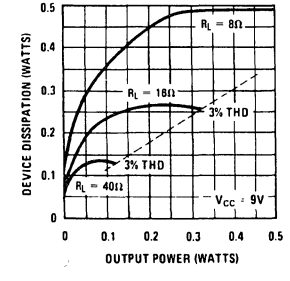
Output Voltage Gain and Phase vs Frequency



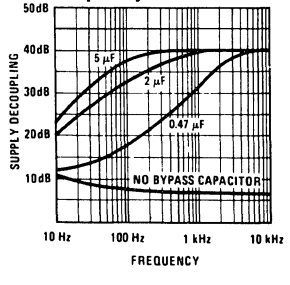
Total Harmonic Distortion vs Output Power



Device Dissipation vs Output Power



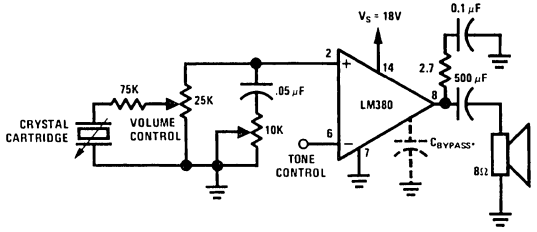
Supply Decoupling vs Frequency



TL/H/6977–7

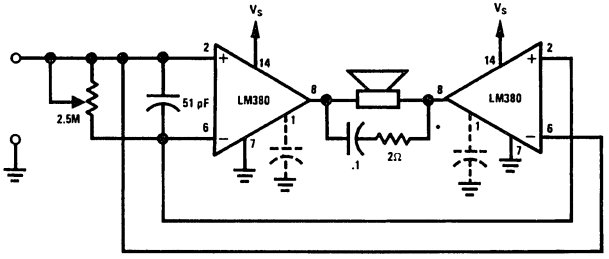
Typical Applications

Phono Amplifier



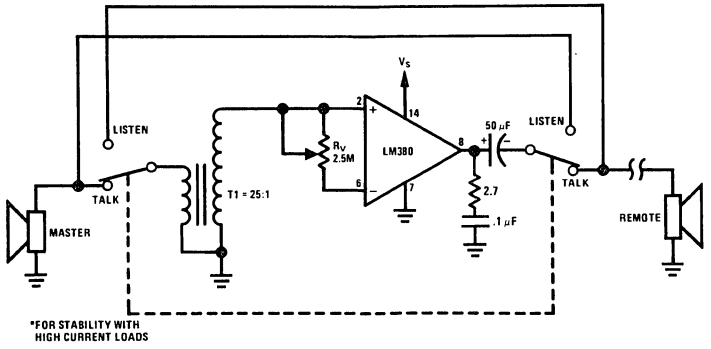
TL/H/6977–8

Bridge Amplifier



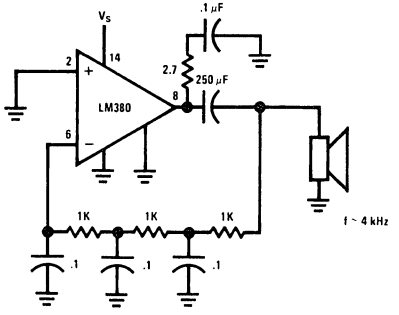
TL/H/6977–9

Intercom



TL/H/6977–10

Phase Shift Oscillator



TL/H/6977–11

National Semiconductor Corporation

LM381/LM381A Low Noise Dual Preamplifier

General Description

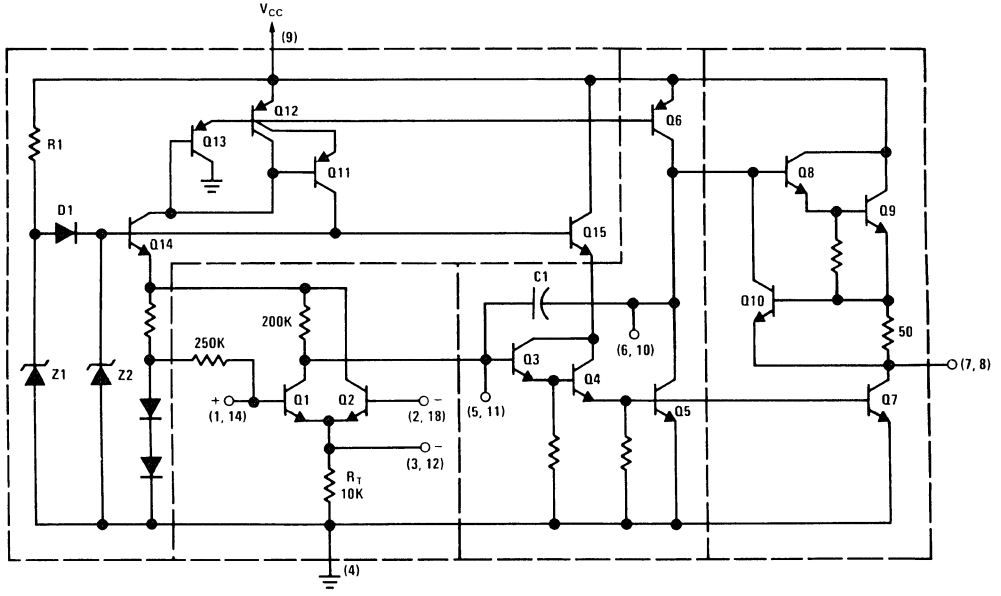
The LM381/LM381A is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 120 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (112 dB), large output voltage swing (V_{CC} − 2V) p-p, and wide power bandwidth (75 kHz, 20 Vp-p). The LM381/LM381A operates from a single supply across the wide range of 9V to 40V.

Either differential input or single ended input configurations may be selected. The amplifier is internally compensated with the provision for additional external compensation for narrow band applications. For additional information see AN-64, AN-104.

Features

- Low noise — 0.5 μV total input noise
- High gain — 112 dB open loop
- Single supply operation
- Wide supply range 9V–40V
- Power supply rejection — 120 dB
- Large output voltage swing (V_{CC} − 2V)p-p
- Wide bandwidth 15 MHz unity gain
- Power bandwidth 75 kHz, 20 Vp-p
- Internally compensated
- Short circuit protected

Schematic Diagram



TL/H/7841–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+40V
Power Dissipation (Note 1)	1.56 W
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

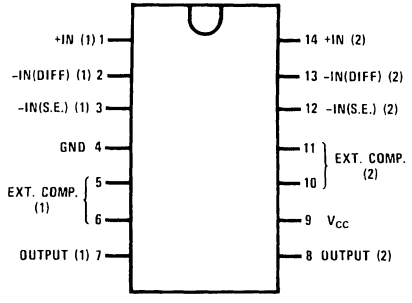
Electrical Characteristics $T_A = 25°C$, $V_{CC} = 14V$, unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
Voltage Gain	Open Loop (Differential Input), f = 100 Hz		160,000		V/V
	Open Loop (Single Ended), f = 100 Hz		320,000		V/V
Supply Current	V_{CC} 9V to 40V, $R_L = \infty$		10		mA
Input Resistance (Positive Input)			100		kΩ
(Negative Input)			200		kΩ
Input Current (Negative Input)			0.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak-to-Peak		$V_{CC} - 2$		V
Unity Gain Bandwidth			15		MHz
Power Bandwidth	20 V_{PP} (V_{CC} = 24V)		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio	f = 1 kHz		120		dB
Channel Separation	f = 1 kHz		60		dB
Total Harmonic Distortion	60 dB Gain, f = 1 kHz		0.1		%
Total Equivalent Input Noise	$R_S = 60\Omega$, 10–10,000 Hz (Single Ended Input, Flat Gain Circuit, A_V = 1000)				
LM381A			0.5	0.7	μVrms
LM381			0.5	1.0	μVrms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Connection Diagram

Dual-In-Line Package



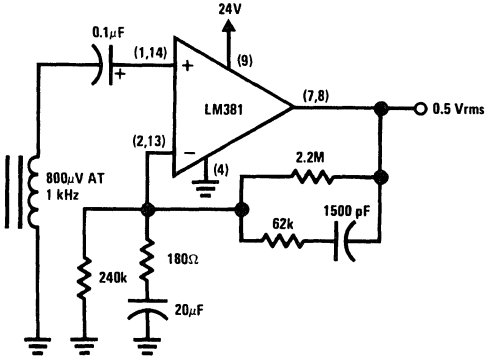
TL/H/7841–2

Top View

Order Number LM381N or LM381AN
See NS Package Number N14A

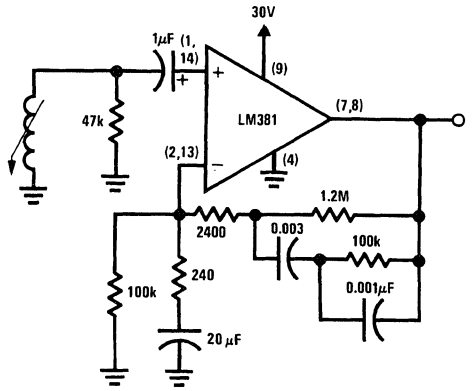
Typical Applications

Typical Tape Playback Amplifier



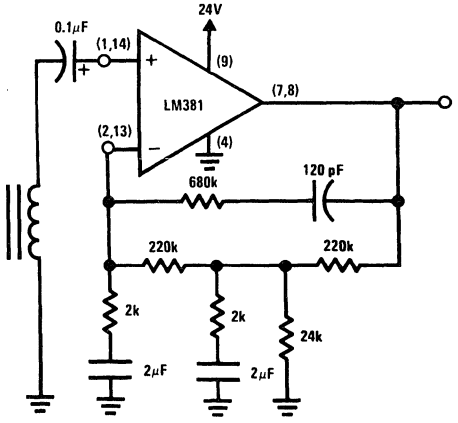
TL/H/7841–3

Typical Magnetic Phono Preamp



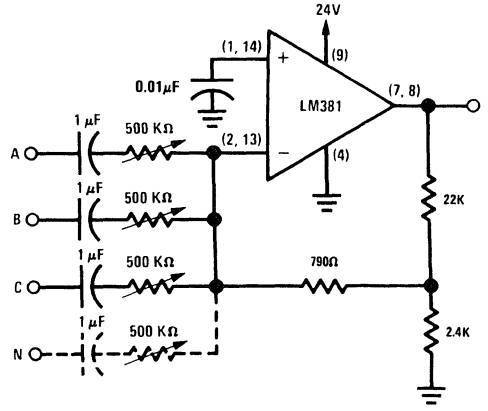
TL/H/7841–4

Two-Pole Fast Turn-On NAB Tape Preamp



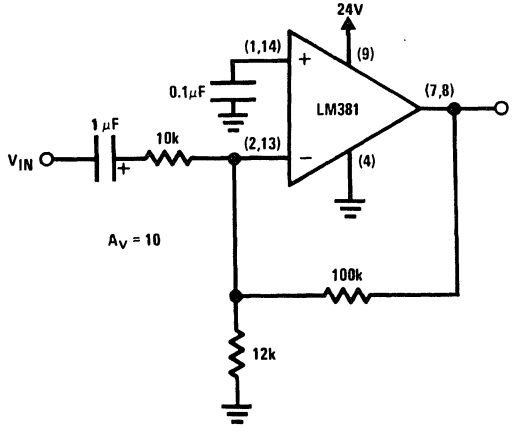
TL/H/7841–5

Audio Mixer



TL/H/7841–6

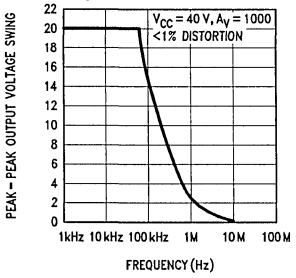
Ultra-Low Distortion Amplifier
(A_V = 10, THD < 0.05%, V_{OUT} = 3 V_{RMS})



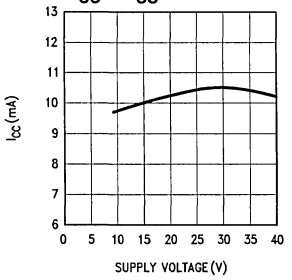
TL/H/7841–7

Typical Performance Characteristics

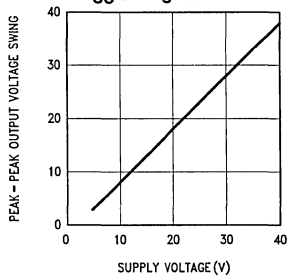
Large Signal Frequency Response



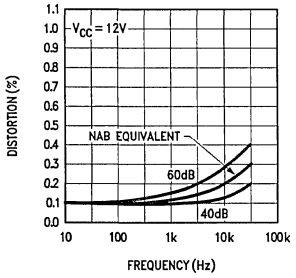
V_{CC} vs I_{CC}



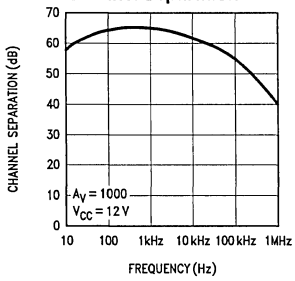
P-P Output Voltage V_{CC} Swing vs



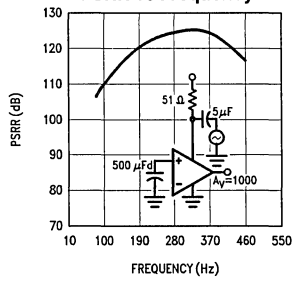
% Distortion



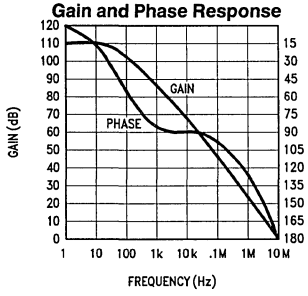
Channel Separation



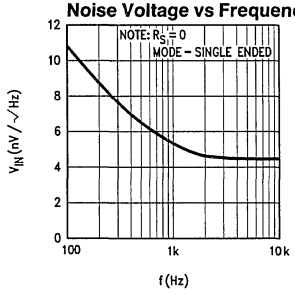
PSRR vs Frequency



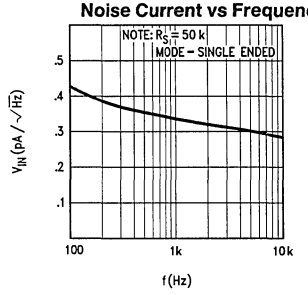
Gain and Phase Response



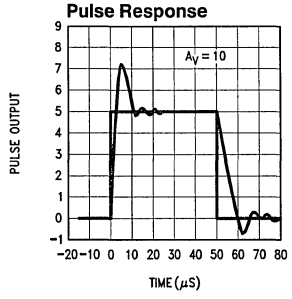
Noise Voltage vs Frequency



Noise Current vs Frequency



Pulse Response



TL/H/7841–8

National Semiconductor Corporation

LM382 Low Noise Dual Preamplifier

General Description

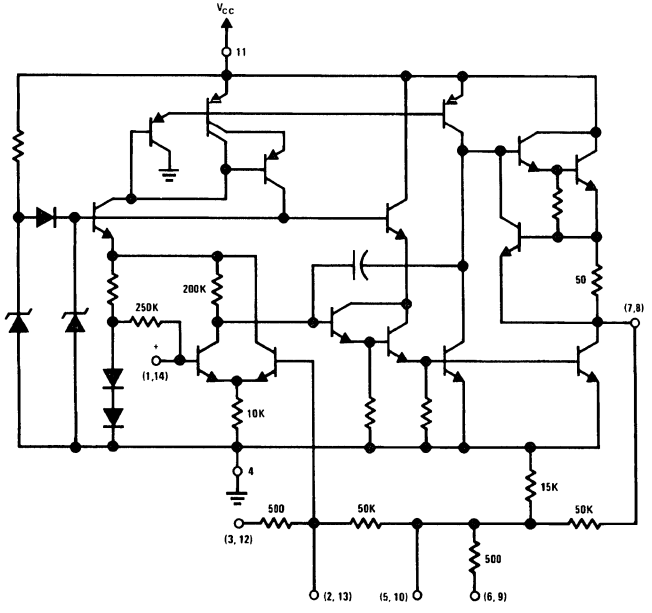
The LM382 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 120 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (100 dB), and wide power bandwidth (75 kHz, 20 Vp-p). The LM382 operates from a single supply across the wide range of 9V to 40V.

A resistor matrix is provided on the chip to allow the user to select a variety of closed loop gain options and frequency response characteristics such as flat-band, NAB or RIAA equalization. The circuit is supplied in the 14 lead dual-in-line package.

Features

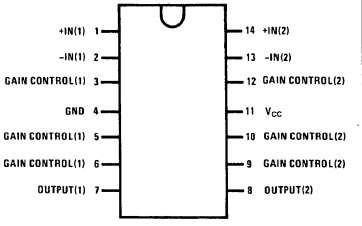
- Low noise — 0.8 μV total equivalent input noise
- High gain — 100 dB open loop
- Single supply operation
- Wide supply range 9V to 40V
- Power supply rejection — 120 dB
- Large output voltage swing
- Wide bandwidth — 15 MHz unity gain
- Power bandwidth — 75 kHz, 20 Vp-p
- Internally compensated
- Short circuit protected

Schematic and Connection Diagrams



TL/H/7842–1

Dual-In-Line Package



TL/H/7843–2

Top View

Order Number LM382N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

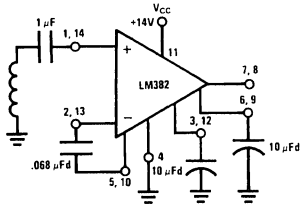
Supply Voltage	+40V
Power Dissipation (Note 1)	1.56 W
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+260°C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = 14V$, unless otherwise stated.

Parameter	Conditions	Min	Typ	Max	Units
Voltage Gain	Open Loop, f = 100 Hz		100,000		V/V
Supply Current	V_{CC} 9V to 40V, $R_L = \infty$		10	20	mA
Output DC Voltage			6		V
Input Resistance (Positive Input)			100		kΩ
(Negative Input)			200		kΩ
Input Current (Negative Input)			0.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak-to-Peak, R_L = 10k		12		V
Unity Gain Bandwidth			15		MHz
Power Bandwidth	20 Vp-p (V_{CC} = 24V)		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio	f = 1 kHz		120		dB
Channel Separation	f = 1 kHz	40	60		dB
Total Harmonic Distortion	60 dB Gain, f = 1 kHz		0.1	0.3	%
Total Equivalent Input Noise	R_S = 600Ω, 100–10,000 Hz (Flat Response Circuit)		0.8	1.2	μVrms

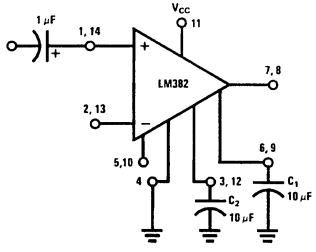
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Typical Applications



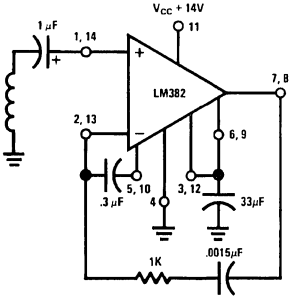
TL/H/7842-3

Tape Preamp (NAB Equalization)



TL/H/7842-5

Flat Response — Fixed Gain Configuration



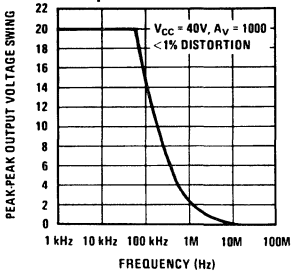
TL/H/7842-4

Phono Preamp (RIAA Equalization)

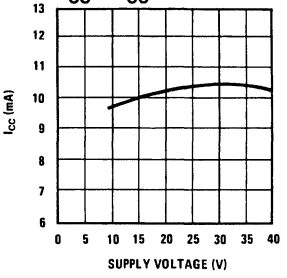
Capacitor	Gain
C1 Only	40 dB
C2 Only	55 dB
C1 & C2	80 dB

Typical Performance Characteristics

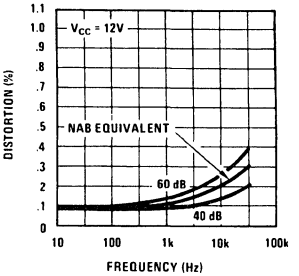
Large Signal Frequency Response



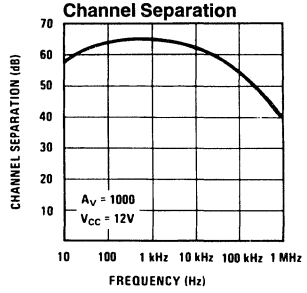
V_{CC} vs I_{CC}



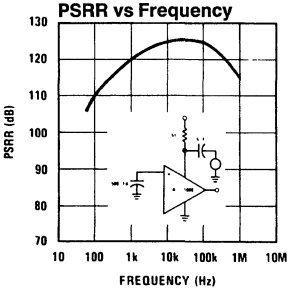
% Distortion



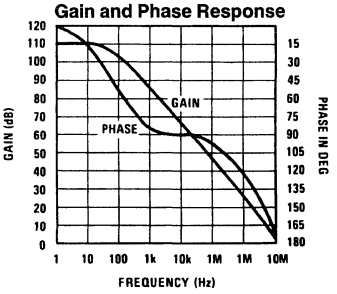
Channel Separation



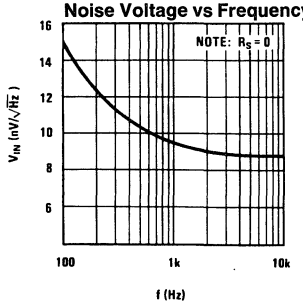
PSRR vs Frequency



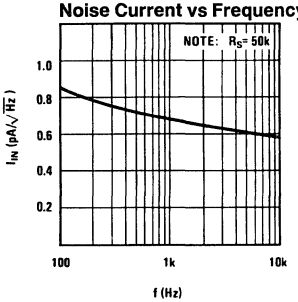
Gain and Phase Response



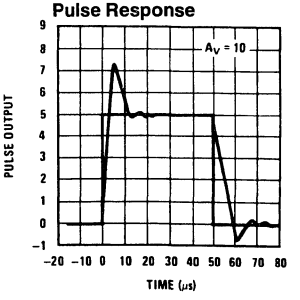
Noise Voltage vs Frequency



Noise Current vs Frequency



Pulse Response



TL/H/7842–6

National Semiconductor Corporation

LM383/LM383A 7 Watt Audio Power Amplifier

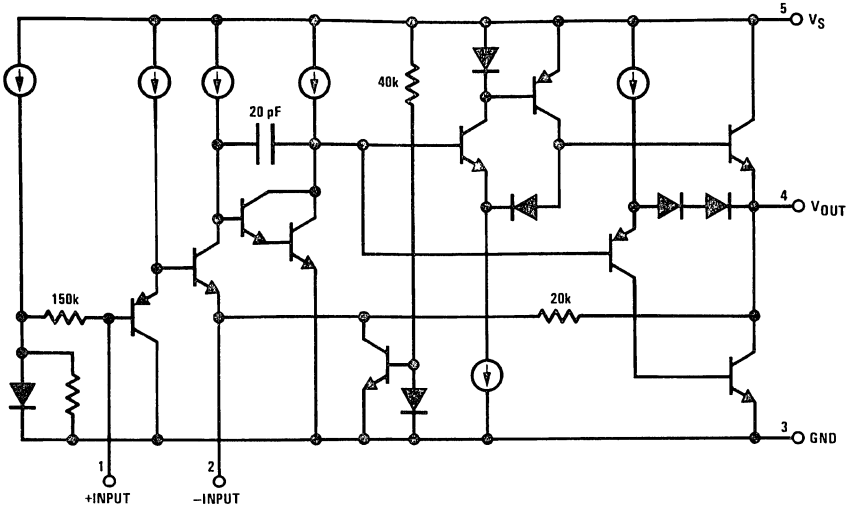
General Description

The LM383 is a cost effective, high power amplifier suited for automotive applications. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The LM383 is current limited and thermally protected. High voltage protection is available (LM383A) which enables the amplifier to withstand 40V transients on its supply. The LM383 comes in a 5-pin TO-220 package.

Features

- High peak current capability (3.5A)
- Large output voltage swing
- Externally programmable gain
- Wide supply voltage range (5V–20V)
- Few external parts required
- Low distortion
- High input impedance
- No turn-on transients
- High voltage protection available (LM383A)
- Low noise
- AC short circuit protected

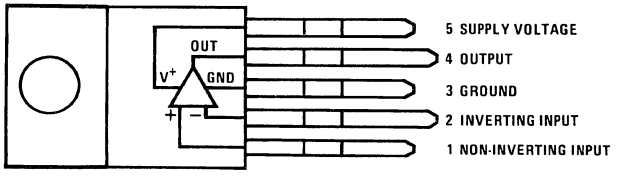
Equivalent Schematic



TL/H/7145–1

Connection Diagram

Plastic Package



TL/H/7145–2

Order Number LM383T or LM383AT
See NS Package Number T05B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Peak Supply Voltage (50 ms)	
LM383A (Note 2)	40V
LM383	25V
Operating Supply Voltage	20V
Output Current	
Repetitive	3.5A
Non-repetitive	4.5A
Input Voltage	±0.5V
Power Dissipation (Note 3)	15W
Operating Temperature	0°C to +70°C
Storage Temperature	−60°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics V_S = 14.4V, T_{TAB} = 25°C, A_V = 100 (40 dB), R_L = 4Ω, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
DC Output Level		6.4	7.2	8	V
Quiescent Supply Current	Excludes Current in Feedback Resistors		45	80	mA
Supply Voltage Range		5		20	V
Input Resistance			150		kΩ
Bandwidth	Gain = 40 dB		30		kHz
Output Power	V_S = 13.2V, f = 1 kHz				
	R_L = 4Ω, THD = 10%		4.7		W
	R_L = 2Ω, THD = 10%		7.2		W
	V_S = 13.8V, f = 1 kHz				
	R_L = 4Ω, THD = 10%		5.1		W
	R_L = 2Ω, THD = 10%		7.8		W
	V_S = 14.4V, f = 1 kHz				
	R_L = 4Ω, THD = 10%	4.8	5.5		W
	R_L = 2Ω, THD = 10%	7	8.6		W
	R_L = 1.6Ω, THD = 10%		9.3		W
	V_S = 16V, f = 1 kHz				
	R_L = 4Ω, THD = 10%		7		W
	R_L = 2Ω, THD = 10%		10.5		W
	R_L = 1.6Ω, THD = 10%		11		W
THD	P_o = 2W, R_L = 4Ω, f = 1 kHz		0.2		%
	P_o = 4W, R_L = 2Ω, f = 1 kHz		0.2		%
Ripple Rejection	R_S = 50Ω, f = 100 Hz	30	40		dB
	R_S = 50Ω, f = 1 kHz		44		dB
Input Noise Voltage	R_S = 0, 15 kHz Bandwidth		2		μV
Input Noise Current	R_S = 100 kΩ, 15 kHz Bandwidth		40		pA

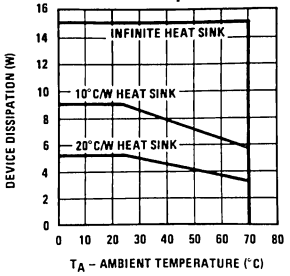
Note 1: A 0.2 μF capacitor in series with a 1Ω resistor should be placed as close as possible to pins 3 and 4 for stability.

Note 2: The LM383 shuts down above 25V.

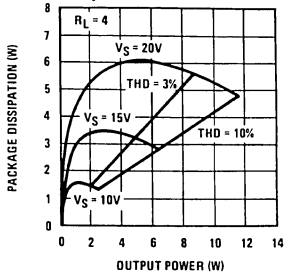
Note 3: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 4°C/W junction to case.

Typical Performance Characteristics

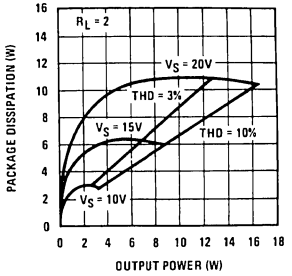
Device Dissipation vs Ambient Temperature



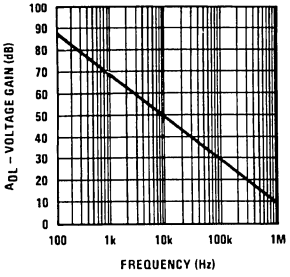
Power Dissipation vs Output Power



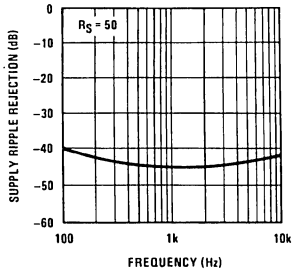
Power Dissipation vs Output Power



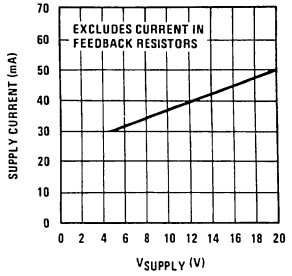
Open Loop Gain vs Frequency



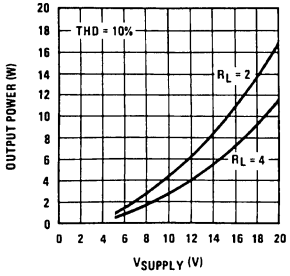
Supply Ripple Rejection vs Frequency



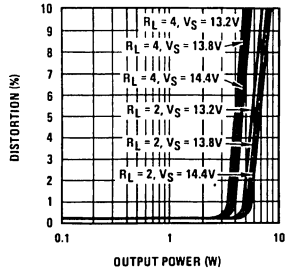
Supply Current vs Supply Voltage



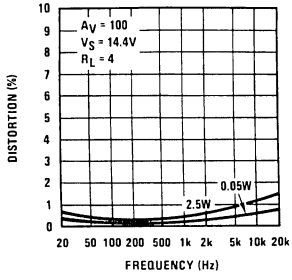
Output Power vs Supply Voltage



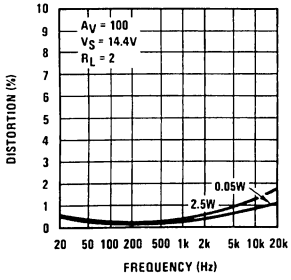
Distortion vs Output Power



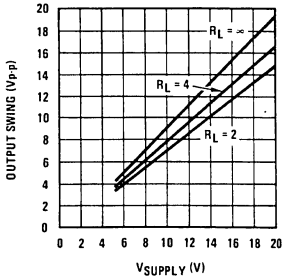
Distortion vs Frequency



Distortion vs Frequency



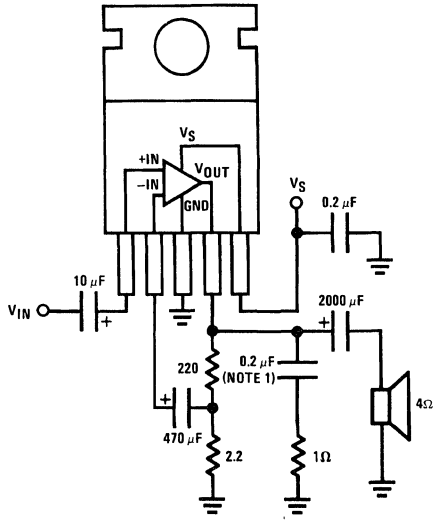
Output Swing vs Supply Voltage



TL/H/7145–4

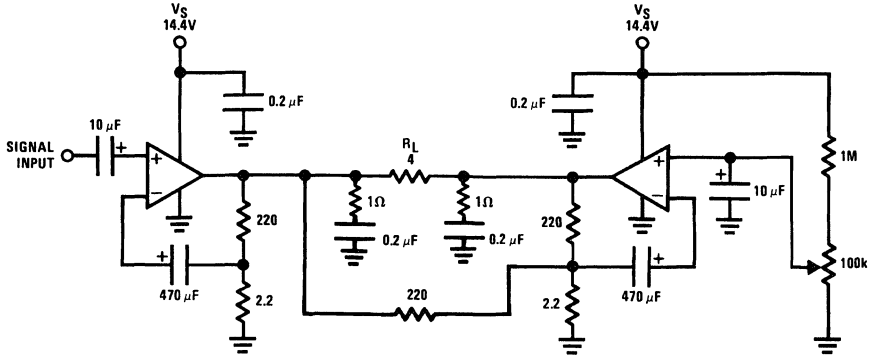
Typical Applications

Single Amplifier



TL/H/7145–3

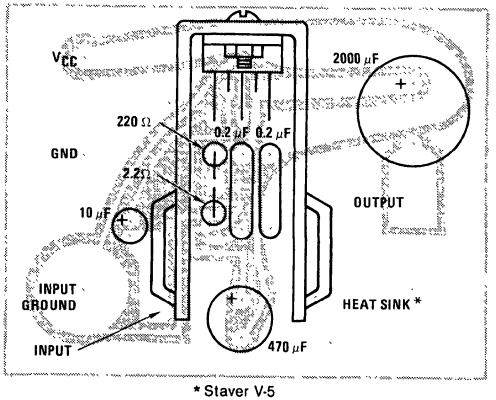
16W Bridge Amplifier



TL/H/7145–5

Component Layout

Single Amplifier
V_S = 20V
R_L = 4Ω



* Staver V-5

Heatsink from:
Staver Company
41 Saxon Ave.
P.O. Drawer H
Bay Shore, NY 11706
Tel: (516) 666-8000

TL/H/7145–6

National Semiconductor Corporation

LM384 5 Watt Audio Power Amplifier

General Description

The LM384 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self-centering to one half the supply voltage.

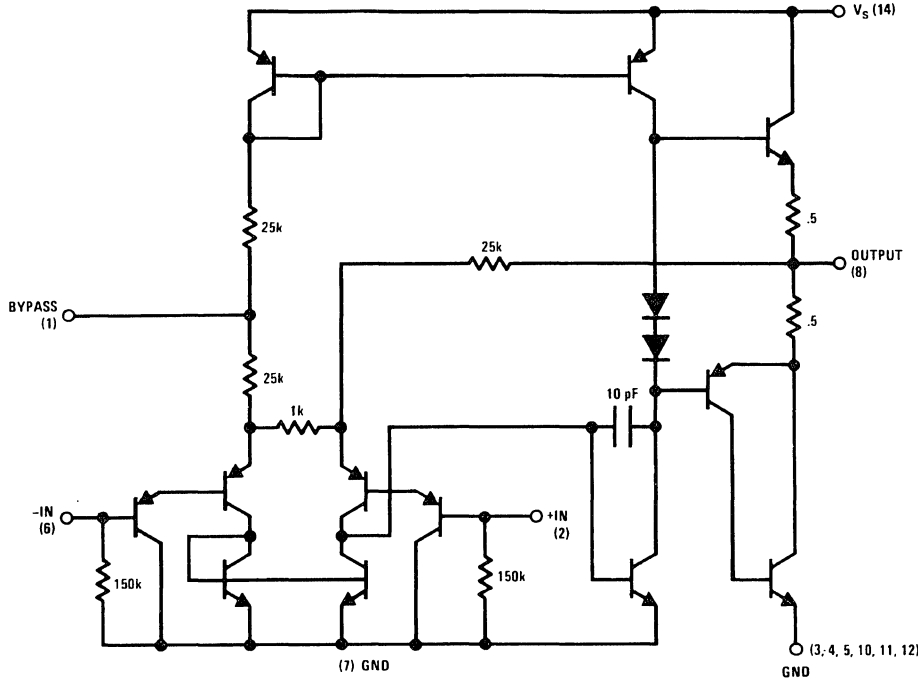
The output is short-circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, sound projector systems, etc. See AN-69 for circuit details.

Features

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one half of the supply voltage
- Standard dual-in-line package

Schematic Diagram



TL/H/7843–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	28V
Peak Current	1.3A
Power Dissipation (See Notes 3 and 4)	1.67W
Input Voltage	±0.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Z_{IN}	Input Resistance			150		kΩ
I_{BIAS}	Bias Current	Inputs Floating		100		nA
A_V	Gain		40	50	60	V/V
P_{OUT}	Output Power	THD = 10%, R_L = 8Ω	5	5.5		W
I_Q	Quiescent Supply Current			8.5	25	mA
$V_{OUT\,Q}$	Quiescent Output Voltage			11		V
BW	Bandwidth	P_{OUT} = 2W, R_L = 8Ω		450		kHz
V^+	Supply Voltage		12		26	V
I_{SC}	Short Circuit Current (Note 5)			1.3		A
$PSRR_{RTO}$	Power Supply Rejection Ratio (Note 2)			31		dB
THD	Total Harmonic Distortion	P_{OUT} = 4W, R_L = 8Ω		0.25	1.0	%

Note 1: V^+ = 22V and T_A = 25°C operating with a Staver V7 heat sink for 30 seconds.

Note 2: Rejection ratio referred to the output with C_{BYPASS} = 5 μF, freq = 120 Hz.

Note 3: The maximum junction temperature of the LM384 is 150°C.

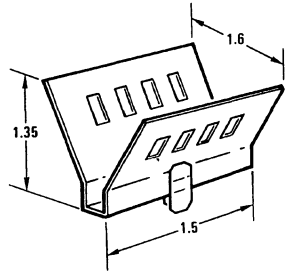
Note 4: The package is to be derated at 15°C/W junction to heat sink pins.

Note 5: Output is fully protected against a shorted speaker condition at all voltages up to 22V.

Heat Sink Dimensions

Staver Company
41 Saxon Ave.
P.O. Drawer H
Bay Shore, N.Y.
Tel: (516) 666-8000

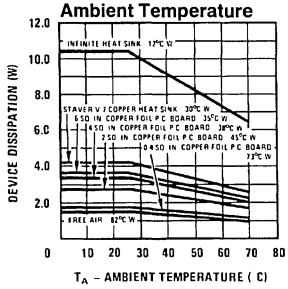
Staver "V7" Heat Sink



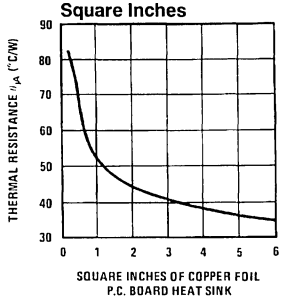
TL/H/7843–4

Typical Performance Characteristics

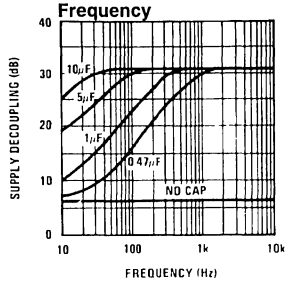
Device Dissipation vs Ambient Temperature



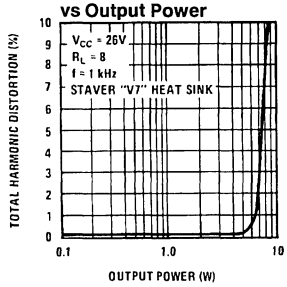
Thermal Resistance vs Square Inches



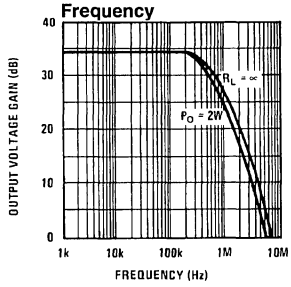
Supply Decoupling vs Frequency



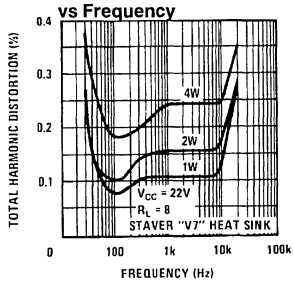
Total Harmonic Distortion vs Output Power



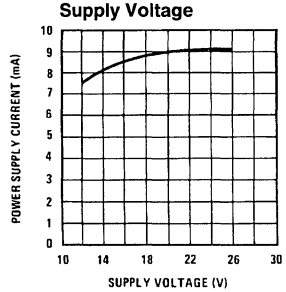
Output Voltage Gain vs Frequency



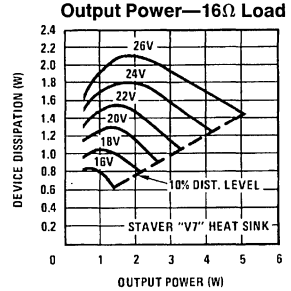
Total Harmonic Distortion vs Frequency



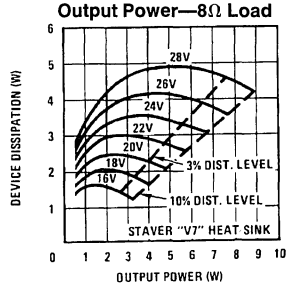
Power Supply Current vs Supply Voltage



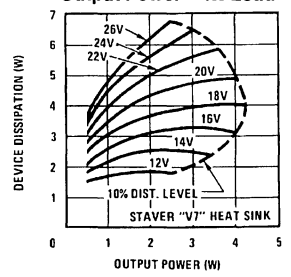
Device Dissipation vs Output Power—16Ω Load



Device Dissipation vs Output Power—8Ω Load

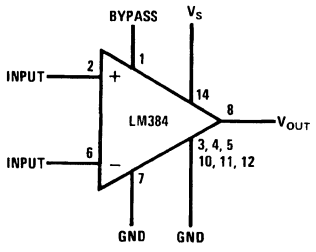


Device Dissipation vs Output Power—4Ω Load



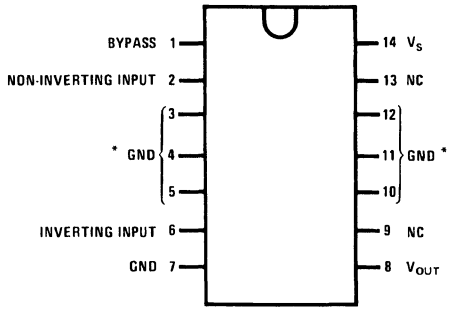
TL/H/7843–5

Block and Connection Diagrams



TL/H/7843-1

Dual-In-Line Package



*Heatsink Pins

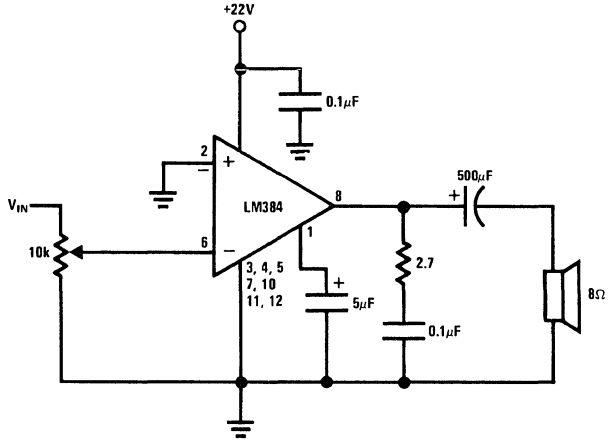
TL/H/7843-2

Top View

Order Number LM384N
See NS Package Number N14A

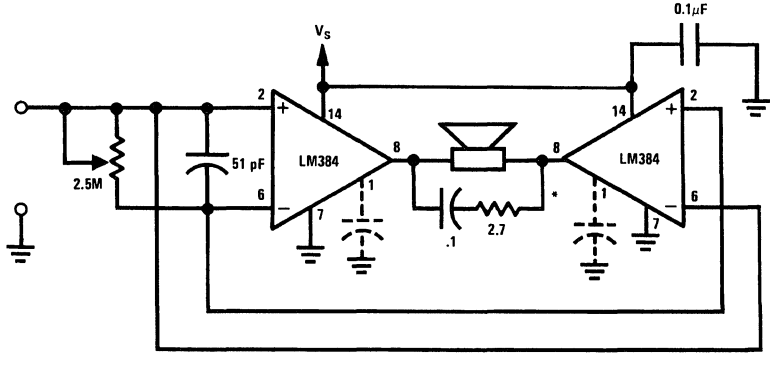
Typical Applications

Typical 5W Amplifier



TL/H/7843-6

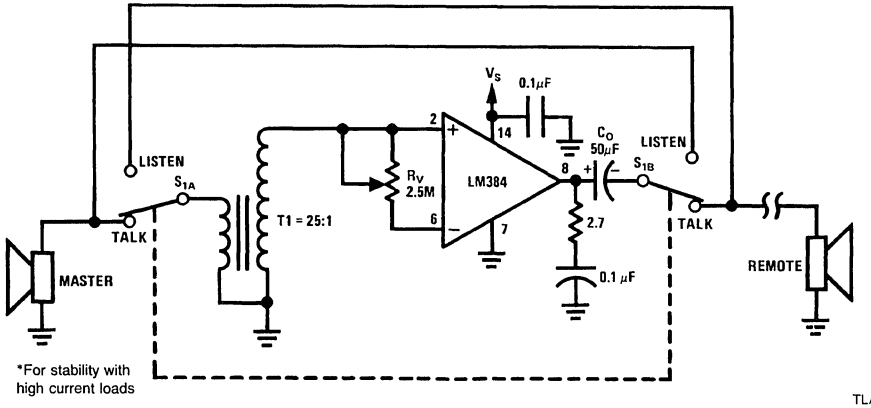
Bridge Amplifier



TL/H/7843-7

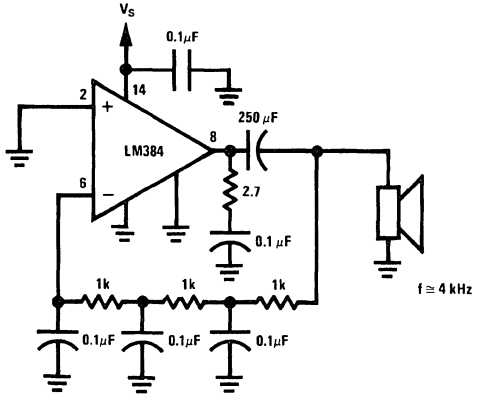
Typical Applications (Continued)

Intercom



TL/H/7843–8

Phase Shift Oscillator



TL/H/7843–9

National Semiconductor Corporation

LM386 Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

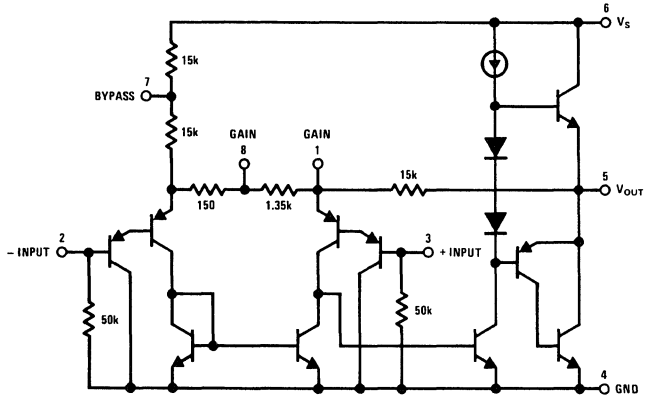
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range — 4V–12V or 5V–18V
- Low quiescent current drain — 4 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Eight pin dual-in-line package

Applications

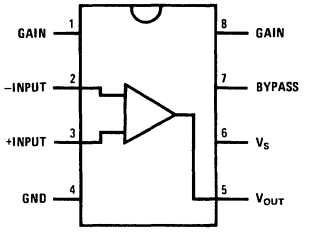
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



TL/H/6976–1

Dual-In-Line and Small Outline Packages



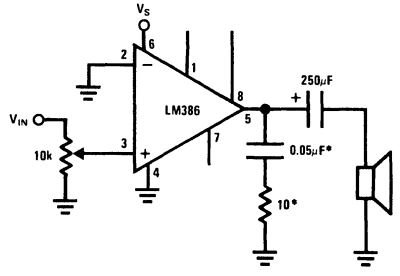
TL/H/6976–2

Top View

Order Number LM386M-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A or N08E

Typical Applications

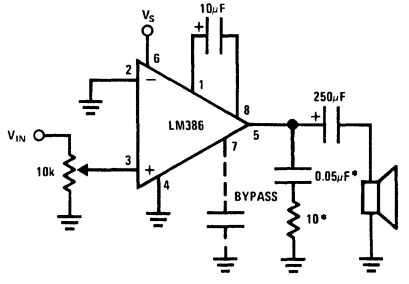
Amplifier with Gain = 20
Minimum Parts



TL/H/6976–3

*Required for LM386N-4 only.

Amplifier with Gain = 200



TL/H/6976–4

*Required for LM386N-4 only.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 1) (LM386N-4)	1.25W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260°C
Small Outline Package	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 μF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW f = 1 kHz, Pins 1 and 8 Open		0.2		%
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 μF Pins 1 and 8 Open, Referred to Output		50		dB
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and 1) a thermal resistance of 80°C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170°C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

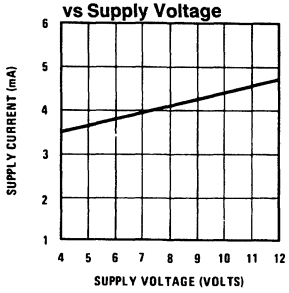
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

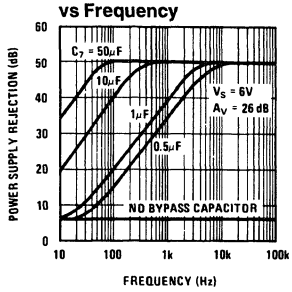
When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Typical Performance Characteristics

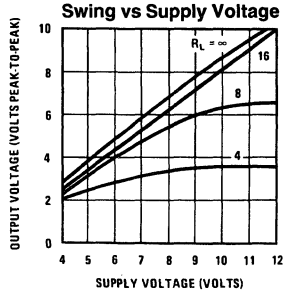
Quiescent Supply Current vs Supply Voltage



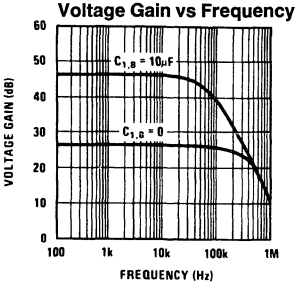
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



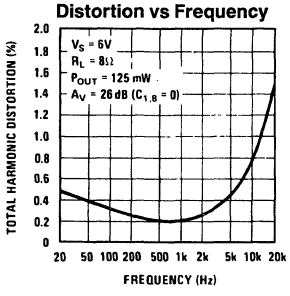
Peak-to-Peak Output Voltage Swing vs Supply Voltage



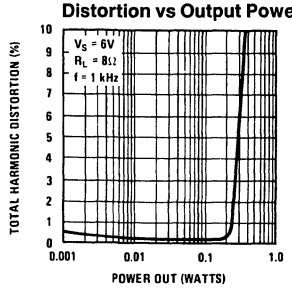
Voltage Gain vs Frequency



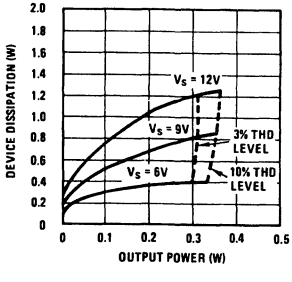
Distortion vs Frequency



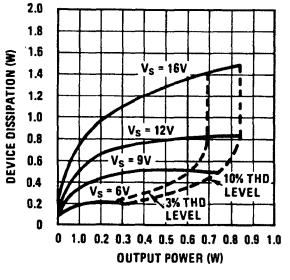
Distortion vs Output Power



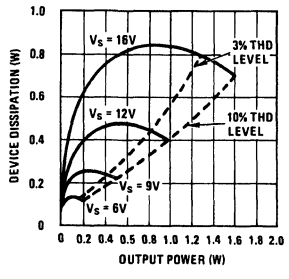
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



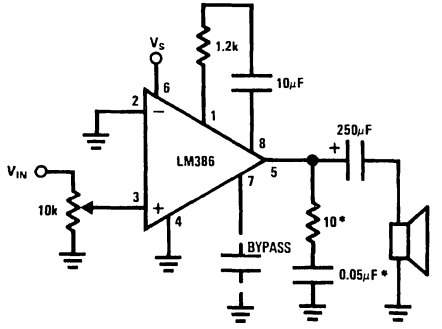
Device Dissipation vs Output Power—16Ω Load



TL/H/6976–5

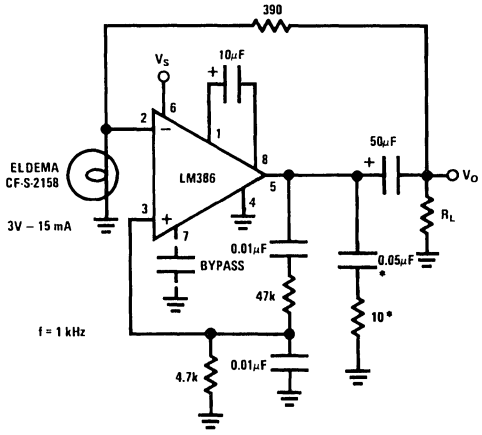
Typical Applications (Continued)

Amplifier with Gain = 50



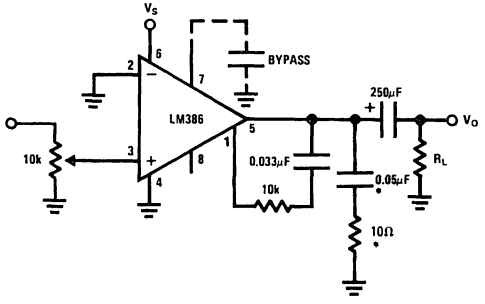
TL/H/6976-6

Low Distortion Power Wienbridge Oscillator



TL/H/6976-7

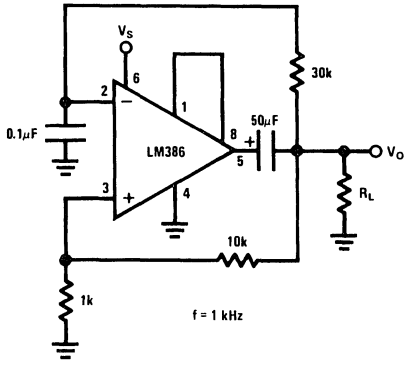
Amplifier with Bass Boost



TL/H/6976-8

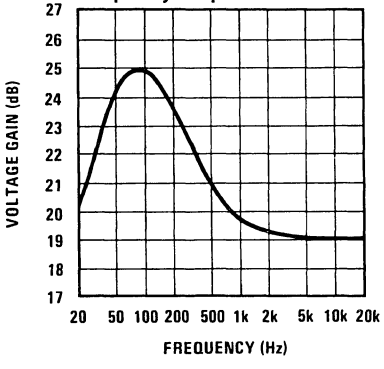
*Required for LM386N-4 only.

Square Wave Oscillator



TL/H/6976-9

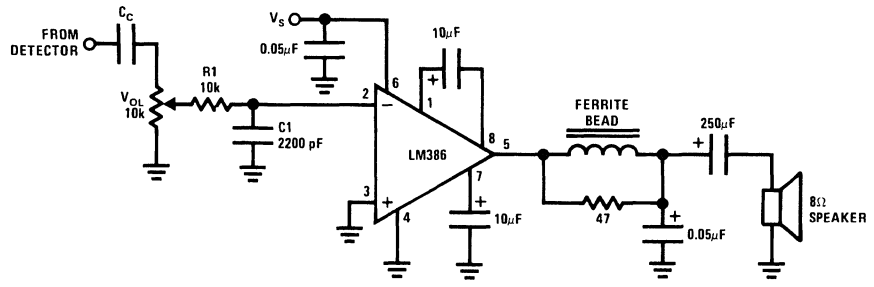
Frequency Response with Bass Boost



TL/H/6976-10

Typical Applications (Continued)

AM Radio Power Amplifier



TL/H/6976–11

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

National Semiconductor Corporation

LM387/LM387A Low Noise Dual Preamplifier

General Description

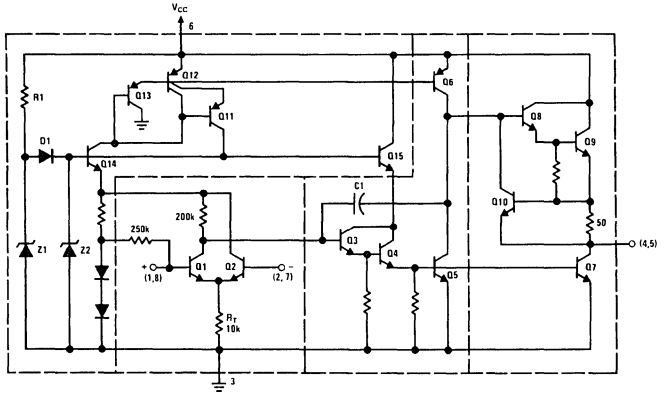
The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110 dB supply rejection and 60 dB channel separation. Other outstanding features include high gain (104 dB), large output voltage swing (V_{CC} − 2V)p-p, and wide power bandwidth (75 kHz, 20 Vp-p). The LM387A is a selected version of the LM387 that has lower noise in a NAB tape circuit, and can operate on a larger supply voltage. The LM387 operates from a single supply across the wide range of 9V to 30V, the LM387A operates on a supply of 9V to 40V.

The amplifiers are internally compensated for gains greater than 10. The LN387, LM387A is available in an 8-lead dual-in-line package. The LM387, LM387A is biased like the LM381. See AN-64 and AN-104.

Features

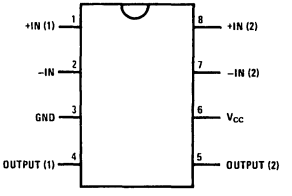
- Low noise — 1.0 μV total input noise
- High gain — 104 dB open loop
- Single supply operation
- Wide supply range LM387 — 9 to 30V
  LM387A — 9 to 40V
- Power supply rejection — 110 dB
- Large output voltage swing (V_{CC} − 2V)p-p
- Wide bandwidth 15 MHz unity gain
- Power bandwidth 75 kHz, 20 Vp-p
- Internally compensated
- Short circuit protected
- Performance similar to LM381

Schematic and Connection Diagrams



TL/H/7845-1

Dual-In-Line Package

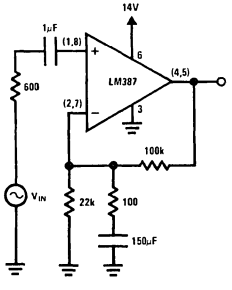


TL/H/7845-2

Top View

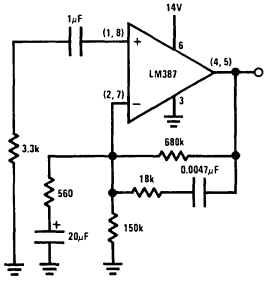
Order Number LM387N or LM387AN
See NS Package Number N08E

Typical Applications



TL/H/7845-3

FIGURE 1. Flat Gain Circuit (A_V = 1000)



TL/H/7845-4

FIGURE 2. NAB Tape Circuit

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage
- LM387 +30V
- LM387A +40V

Power Dissipation (Note 1) 1.5W
Operating Temperature Range 0°C to +70°C
Storage Temperature Range −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) 260°C

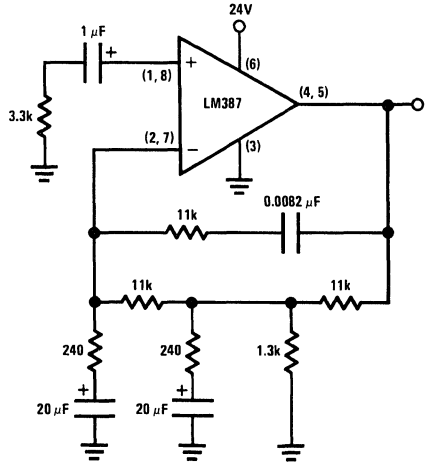
Electrical Characteristics $T_A = 25°C$, $V_{CC} = 14V$, unless otherwise stated

Parameter	Conditions	Min	Typ	Max	Units
Voltage Gain	Open Loop, f = 100 Hz		160,000		V/V
Supply Current	LM387, V_{CC} 9V–30V, $R_L = \infty$ LM387A, V_{CC} 9V–40V, $R_L = \infty$		10 10		mA mA
Input Resistance Positive Input Negative Input		50	 100 200		 kΩ kΩ
Input Current Negative Input			0.5	3.1	μA
Output Resistance	Open Loop		150		Ω
Output Current	Source Sink		8 2		mA mA
Output Voltage Swing	Peak-to-Peak		$V_{CC}-2$		V
Unity Gain Bandwidth			15		MHz
Large Signal Frequency Response	20 Vp-p ($V_{CC} > 24V$), THD ≤ 1%		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio Input Referred	f = 1 kHz		110		dB
Channel Separation	f = 1 kHz	40	60		dB
Total Harmonic Distortion	60 dB Gain, f = 1 kHz		0.1	0.5	%
Total Equivalent Input Noise (Flat Gain Cricuit)	10 Hz–10,000 Hz LM387 *Figure 1*		1.0	1.2	μVrms
Output Noise NAB Tape Playback Circuit Gain of 37 dB	Unweighted LM387A *Figure 2*		400	700	μVrms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

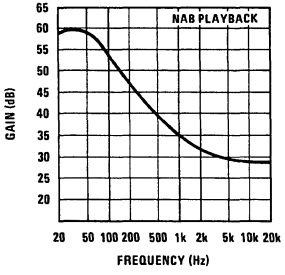
Typical Applications (Continued)

Two-Pole Fast Turn-ON NAB Tape Preamplifier



TL/H/7845–5

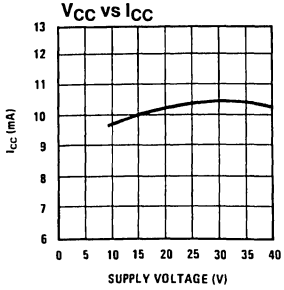
Frequency Response of NAB Circuit of Figure 2



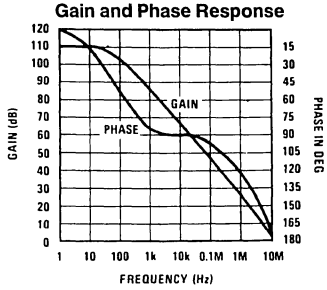
TL/H/7845–6

Typical Performance Characteristics

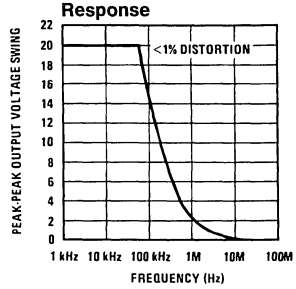
V_{CC} vs I_{CC}



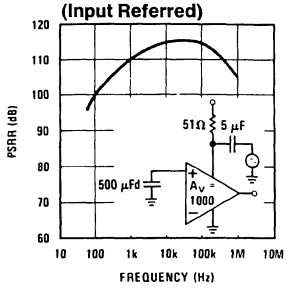
Gain and Phase Response



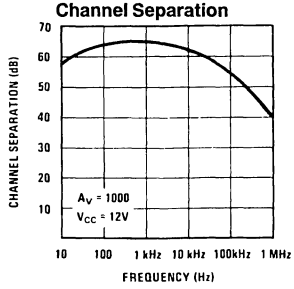
Large Signal Frequency Response



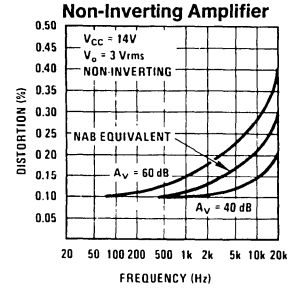
PSRR vs Frequency (Input Referred)



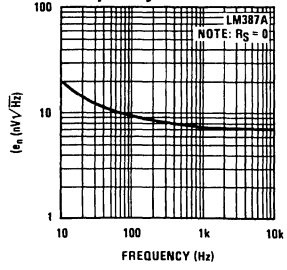
Channel Separation



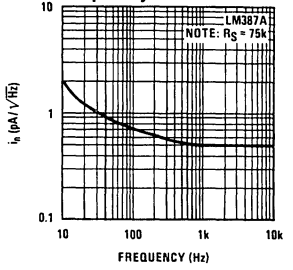
Distortion vs Frequency Non-Inverting Amplifier



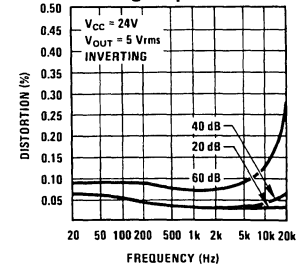
Noise Voltage vs Frequency



Noise Current vs Frequency



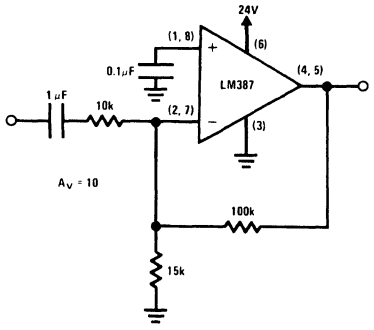
Distortion vs Frequency Inverting Amplifier



TL/H/7845–7

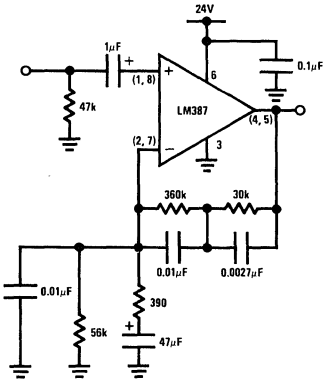
Typical Applications (Continued)

Inverting Amplifier Ultra-Low Distortion



TL/H/7845–8

Typical Magnetic Phono Preamplifier



TL/H/7845–9

National Semiconductor Corporation

LM388 1.5 Watt Audio Power Amplifier

General Description

The LM388 is an audio amplifier designed for use in medium power consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 2 and 6 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage.

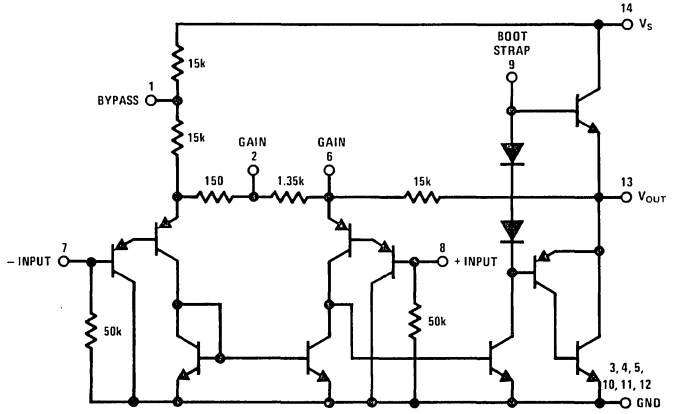
Features

- Minimum external parts
- Wide supply voltage range
- Excellent supply rejection
- Ground referenced input
- Self-centering output quiescent voltage
- Variable voltage gain
- Low distortion
- Fourteen pin dual-in-line package
- Low voltage operation, 4V

Applications

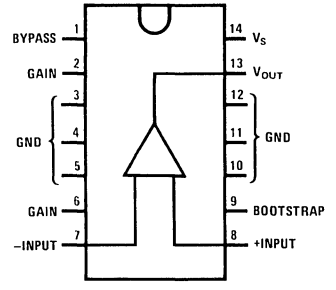
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Lamp drivers
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



TL/H/7846–1

Dual-In-Line Package



TL/H/7846–2

Top View

Order Number LM388N-1
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	15V
Package Dissipation 14-Pin DIP (Note 1)	8.3W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics T_A = 25°C, *(Figure 1)*

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_S	Operating Supply Voltage LM388		4		12	V
I_Q	Quiescent Current LM388	V_{IN} = 0 V_S = 12V		16	23	mA
P_{OUT}	Output Power (Note 2) LM388N-1	R1 = R2 = 180Ω, THD = 10% V_S = 12V, R_L = 8Ω V_S = 6V, R_L = 4Ω	 1.5 0.6	 2.2 0.8		 W W
A_V	Voltage Gain	V_S = 12V, f = 1 kHz 10 μF from Pins 2 to 6	23	26 46	30	dB dB
BW	Bandwidth	V_S = 12V, Pins 2 and 6 Open		300		kHz
THD	Total Harmonic Distortion	V_S = 12V, R_L = 8Ω, P_{OUT} = 500 mW, f = 1 kHz, Pins 2 and 6 Open		0.1	1	%
PSRR	Power Supply Rejection Ratio (Note 3)	V_S = 12V, f = 1 kHz, C_{BYPASS} = 10 μF, Pins 2 and 6 Open, Referred to Output		50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	V_S = 12V, Pins 7 and 8 Open		250		nA

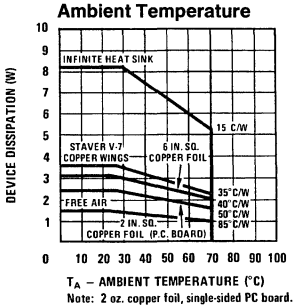
Note 1: Pins 3, 4, 5, 10, 11, 12 at 25°C. Derate at 15°C/W above 25°C case.

Note 2: The amplifier should be in high gain for full swing on higher supplies due to input voltage limitations.

Note 3: If load and bypass capacitor are returned to V_S *(Figure 2)*, rather than ground *(Figure 1)*, PSRR is typically 30 dB.

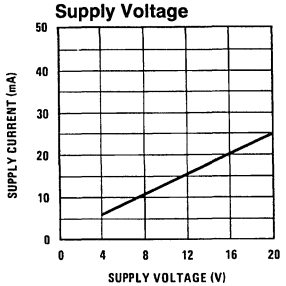
Typical Performance Characteristics

Maximum Device Dissipation vs Ambient Temperature

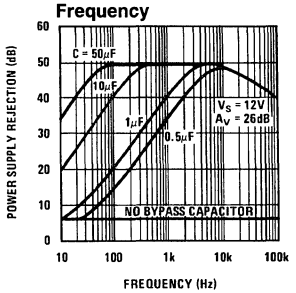


Note: 2 oz. copper foil, single-sided PC board.

Quiescent Supply Current vs Supply Voltage



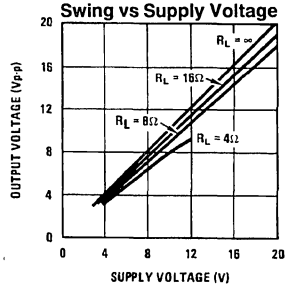
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



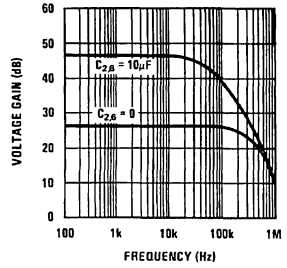
TL/H/7846–5

Typical Performance Characteristics (Continued)

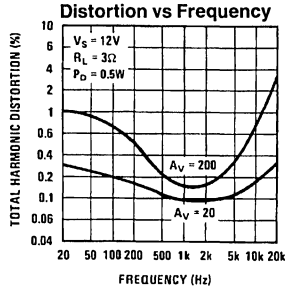
Peak-to-Peak Output Voltage Swing vs Supply Voltage



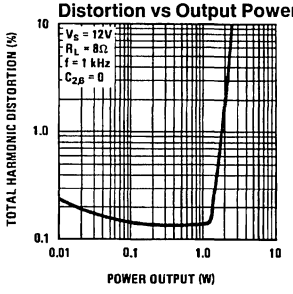
Voltage Gain vs Frequency



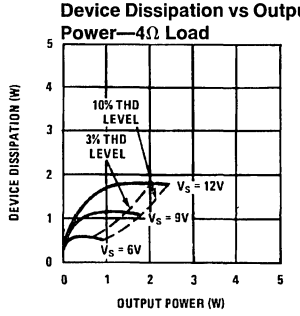
Distortion vs Frequency



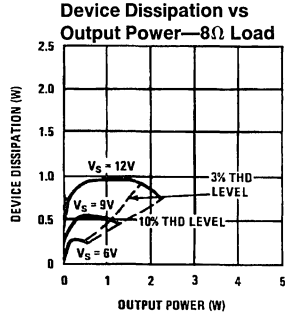
Distortion vs Output Power



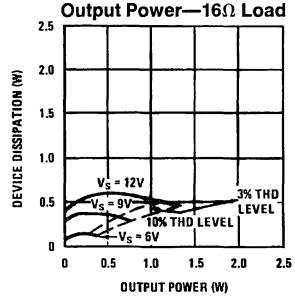
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



Device Dissipation vs Output Power—16Ω Load



TL/H/7846–6

Application Hints

GAIN CONTROL

To make the LM388 a more versatile amplifier, two pins (2 and 6) are provided for gain control. With pins 2 and 6 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pins 2 to 6, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pins 2 to 6 then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 6 to ground, as in *Figure 7*.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 6 to 13 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 2

Application Hints (Continued)

is open. If pins 2 and 6 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9 V/V.

INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor . The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM388 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM388 with higher gains (bypassing the 1.35 kΩ resistor between pins 2 and 6) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

BOOTSTRAPPING

The base of the output transistor of the LM388 is brought out to pin 9 for Bootstrapping. The output stage of the amplifier during positive swing is shown in *Figure 3* with its external circuitry.

R1 + R2 set the amount of base current available to the output transistor. The maximum output current divided by beta is the value required for the current in R1 and R2:

$$(R1 + R2) = \beta_O \frac{(V_S/2) - V_{BE}}{I_{O\,MAX}}$$

Good design values are $V_{BE} = 0.7V$ and $\beta_O = 100$.

Example: 1 watt into 8Ω load with $V_S = 12V$.

$$I_{O\,MAX} = \sqrt{\frac{2\,P_O}{R_L}} = 500\ mA$$

$$(R1 + R2) = 100\left(\frac{(12/2) - 0.7}{0.5}\right) = 1060\Omega$$

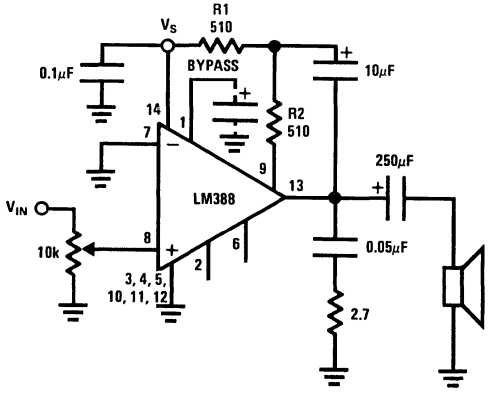
To keep the current in R2 constant during positive swing capacitor C_B is added. As the output swings positive C_B lifts R1 and R2 above the supply, maintaining a constant voltage across R2. To minimize the value of C_B, R1 = R2. The pole due to C_B and R1 and R2 is usually set equal to the pole due to the output coupling capacitor and the load. This gives:

$$C_B \cong \frac{4C_c}{\beta_O} \cong \frac{C_c}{25}$$

Example: for 100 Hz pole and $R_L = 8\Omega$; $C_c = 200\ \mu F$ and $C_B = 8\ \mu F$, if R1 is made a diode and R2 increased to give the same current, C_B can be decreased by about a factor of 4, as in *Figure 4*.

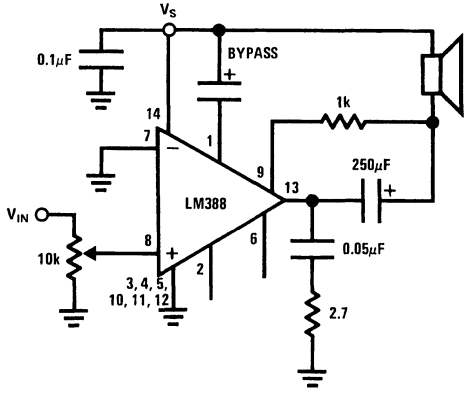
For reduced component count the load can replace R1. The value of (R1 + R2) is the same, so R2 is increased. Now C_B is both the coupling and the bootstrapping capacitor (see *Figure 2*).

Typical Applications



TL/H/7846–3

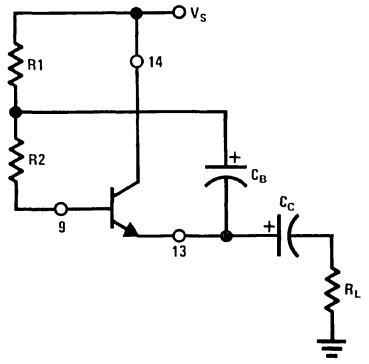
FIGURE 1. Load Returned to Ground (Amplifier with Gain = 20)



TL/H/7846–4

FIGURE 2. Load Returned to V_S (Amplifier with Gain = 20)

Typical Applications (Continued)



TL/H/7846-7

FIGURE 3

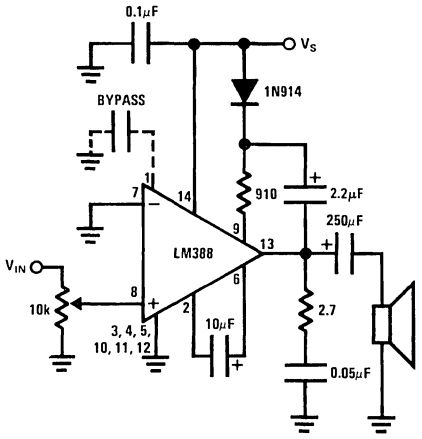


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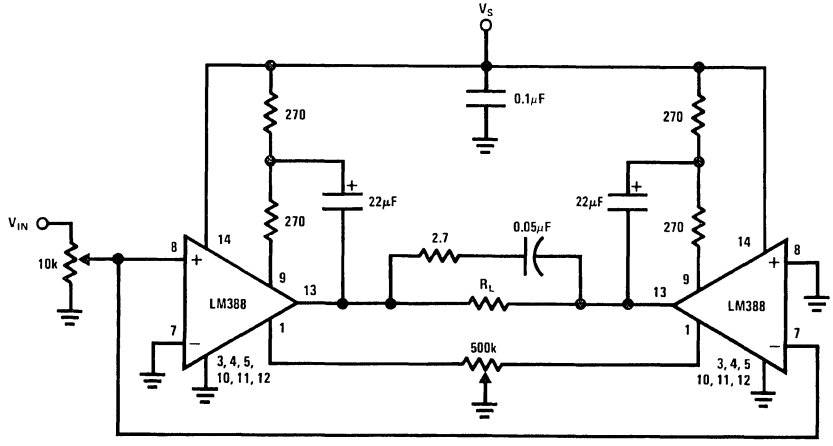
FIGURE 4. Amplifier with Gain = 200 and Minimum C_B



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V_S = 6V R_L = 4Ω P_O = 1.0W
V_S = 12V R_L = 8Ω P_O = 4W

FIGURE 5. Bridge Amp

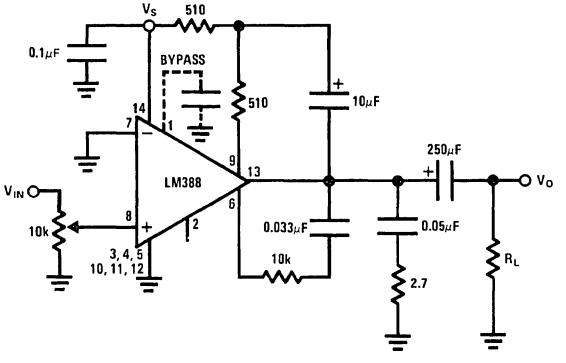

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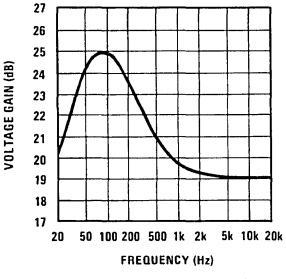
FIGURE 6a. Amplifier with Bass Boost



TL/H/7846-11

FIGURE 6b. Frequency Response with Bass Boost

Typical Applications (Continued)

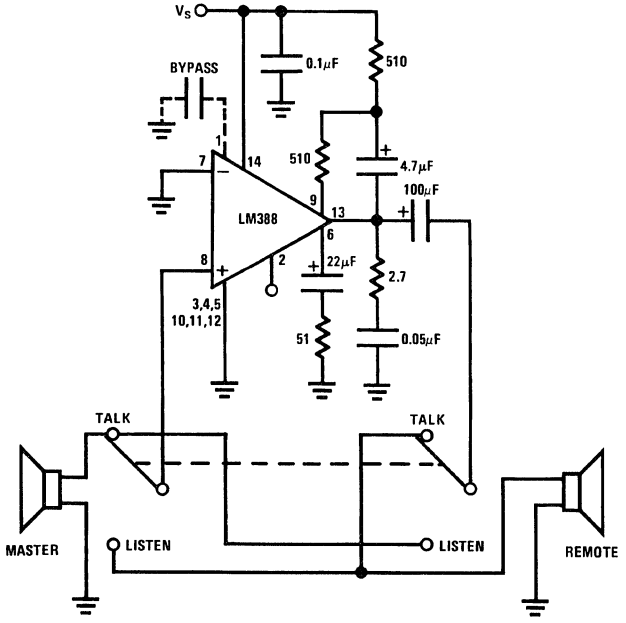


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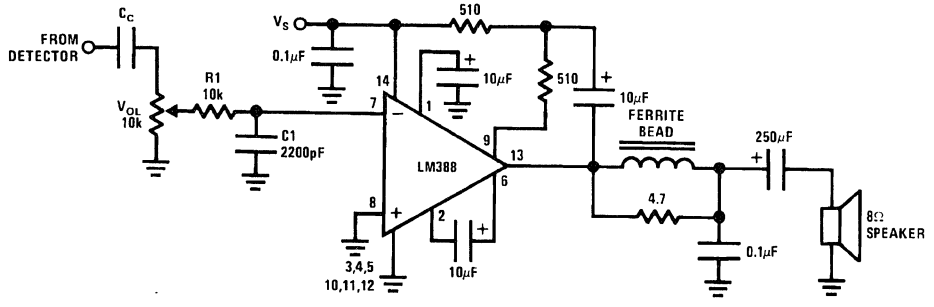
FIGURE 7. Intercom



TL/H/7846–13

FIGURE 8. AM Radio Power Amplifier

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

National Semiconductor Corporation

LM389 Low Voltage Audio Power Amplifier with NPN Transistor Array

General Description

The LM389 is an array of three NPN transistors on the same substrate with an audio power amplifier similar to the LM386.

The amplifier inputs are ground referenced while the output is automatically biased to one half the supply voltage. The gain is internally set at 20 to minimize external parts, but the addition of an external resistor and capacitor between pins 4 and 12 will increase the gain to any value up to 200.

The three transistors have high gain and excellent matching characteristics. They are well suited to a wide variety of applications in DC through VHF systems.

Features

Amplifier

- Battery operation
- Minimum external parts
- Wide supply voltage range
- Low quiescent current drain
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion

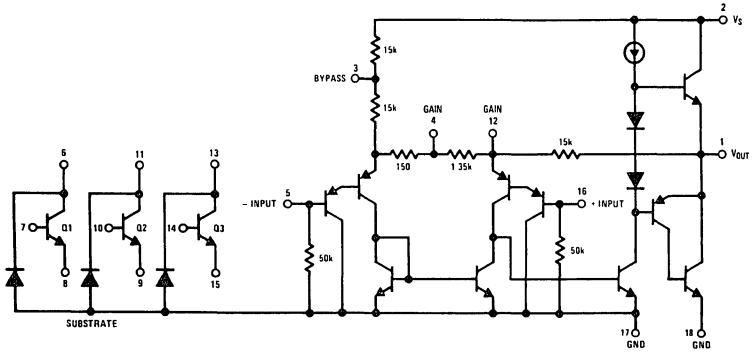
Transistors

- Operation from 1 μA to 25 mA
- Frequency range from DC to 100 MHz
- Excellent matching

Applications

- AM-FM radios
- Portable tape recorders
- Intercoms
- Toys and games
- Walkie-talkies
- Portable phonographs
- Power converters

Equivalent Schematic and Connection Diagrams



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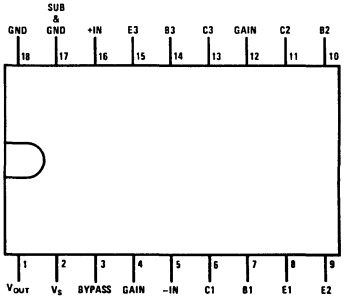
Dual-In-Line Package



TL/H/7847–2

Order Number LM389N
See NS Package Number N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	15V
Package Dissipation (Note 1)	1.89W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Collector to Emitter Voltage, V_{CEO}	12V
Collector to Base Voltage, V_{CBO}	15V
Collector to Substrate Voltage, V_{CIO} (Note 2)	15V
Collector Current, I_C	25 mA
Emitter Current, I_E	25 mA
Base Current, I_B	5 mA
Power Dissipation (Each Transistor) $T_A \leq +70°C$	150 mW

Electrical Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLIFIER						
V_S	Operating Supply Voltage		4		12	V
I_Q	Quiescent Current	$V_S = 6V$, $V_{IN} = 0V$		6	12	mA
P_{OUT}	Output Power (Note 3)	THD = 10% $V_S = 6V$, $R_L = 8\Omega$ $V_S = 9V$, $R_L = 16\Omega$	250	325 500		mW mW
A_V	Voltage Gain	$V_S = 6V$, f = 1 kHz 10 μF from Pins 4 to 12	23	26 46	30	dB dB
BW	Bandwidth	$V_S = 6V$, Pins 4 and 12 Open		250		kHz
THD	Total Harmonic Distortion	$V_S = 6V$, $R_L = 8\Omega$, $P_{OUT} = 125$ mW, f = 1 kHz, Pins 4 and 12 Open		0.2	3.0	%
PSRR	Power Supply Rejection Ratio	$V_S = 6V$, f = 1 kHz, $C_{BYPASS} = 10$ μF, Pins 4 and 12 Open, Referred to Output	30	50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	$V_S = 6V$, Pins 5 and 16 Open		250		nA
TRANSISTORS						
V_{CEO}	Collector to Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$	12	20		V
V_{CBO}	Collector to Base Breakdown Voltage	$I_C = 10$ μA, $I_E = 0$	15	40		V
V_{CIO}	Collector to Substrate Breakdown Voltage	$I_C = 10$ μA, $I_E = I_B = 0$	15	40		V
V_{EBO}	Emitter to Base Breakdown Voltage	$I_E = 10$ μA, $I_C = 0$	6.4	7.1	7.8	V
H_{FE}	Static Forward Current Transfer Ratio (Static Beta)	$I_C = 10$ μA $I_C = 1$ mA $I_C = 10$ mA	100	100 275 275		
h_{oe}	Open-Circuit Output Admittance	$I_C = 1$ mA, $V_{CE} = 5V$, f = 1.0 kHz		20		μmho
V_{BE}	Base to Emitter Voltage	$I_E = 1$ mA		0.7	0.85	V
$\lvert V_{BE1} - V_{BE2} \rvert$	Base to Emitter Voltage Offset	$I_E = 1$ mA		1	5	mV
V_{CESAT}	Collector to Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		0.15	0.5	V
C_{EB}	Emitter to Base Capacitance	$V_{EB} = 3V$		1.5		pF
C_{CB}	Collector to Base Capacitance	$V_{CB} = 3V$		2		pF
C_{CI}	Collector to Substrate Capacitance	$V_{CI} = 3V$		3.5		pF
h_{fe}	High Frequency Current Gain	$I_C = 10$ mA, $V_{CE} = 5V$, f = 100 MHz	1.5	5.5		

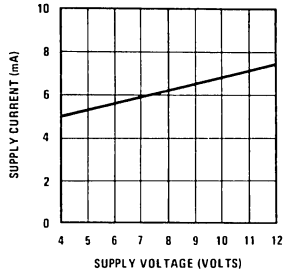
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 66°C/W junction to ambient.

Note 2: The collector of each transistor is isolated from the substrate by an integral diode. Therefore, the collector voltage should remain positive with respect to pin 17 at all times.

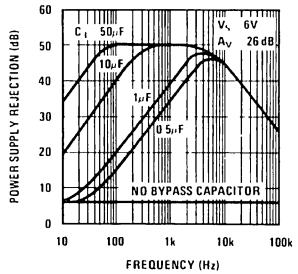
Note 3: If oscillation exists under some load conditions, add 2.7Ω and 0.05 μF series network from pin 1 to ground.

Typical Amplifier Performance Characteristics

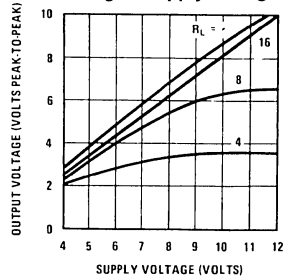
Quiescent Supply Current vs Supply Voltage



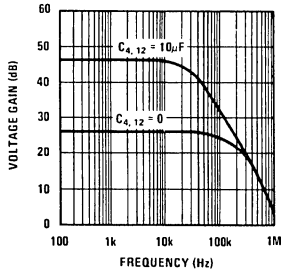
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



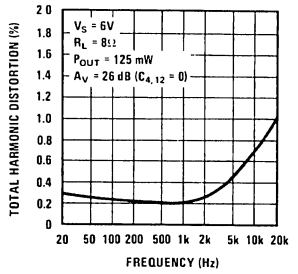
Peak-to-Peak Output Voltage Swing vs Supply Voltage



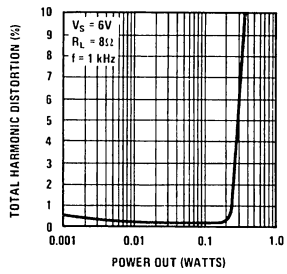
Voltage Gain vs Frequency



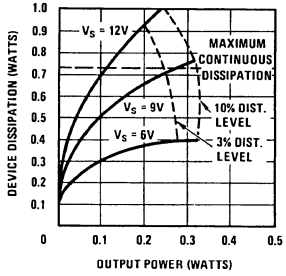
Distortion vs Frequency



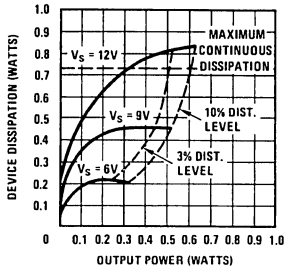
Distortion vs Output Power



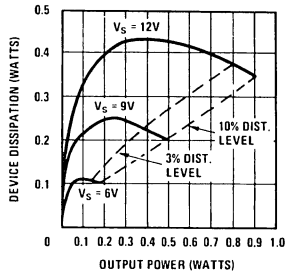
Device Dissipation vs Output Power—4Ω Load



Device Dissipation vs Output Power—8Ω Load



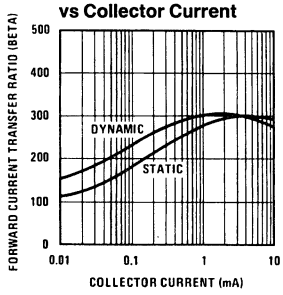
Device Dissipation vs Output Power—16Ω Load



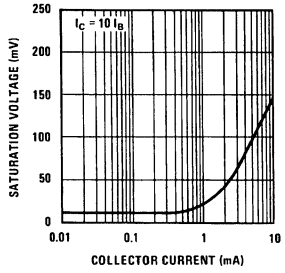
TL/H/7847–3

Typical Transistor Performance Characteristics

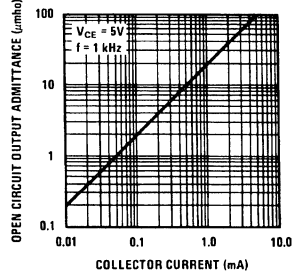
Forward Current Transfer Ratio vs Collector Current



Saturation Voltage vs Collector Current



Open Circuit Output Admittance vs Collector Current



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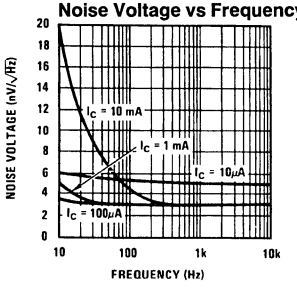
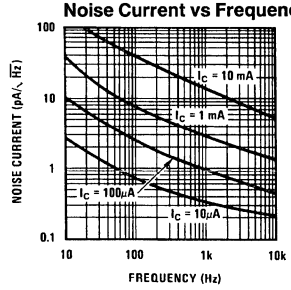
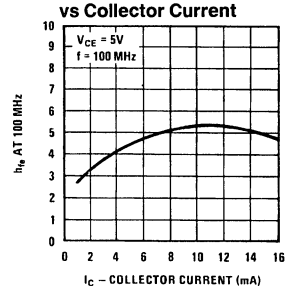
Noise Voltage vs Frequency



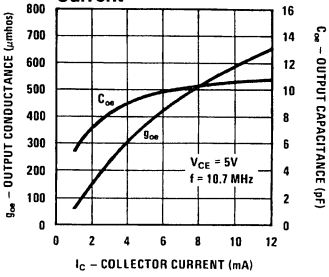
Noise Current vs Frequency



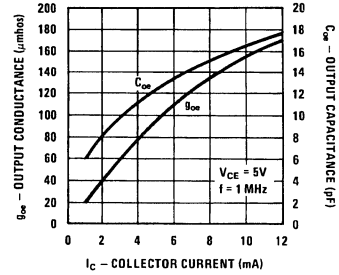
High Frequency Current Gain vs Collector Current



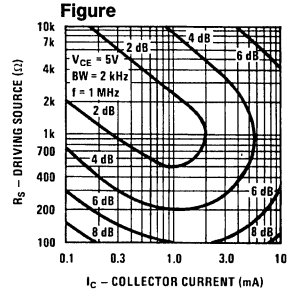
g_{oe} and C_{oe} vs Collector Current



g_{oe} and C_{oe} vs Collector Current



Contours of Constant Noise Figure



TL/H/7847–5

Application Hints

Gain Control

To make the LM389 a more versatile amplifier, two pins (4 and 12) are provided for gain control. With pins 4 and 12 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 4 to 12, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pin 4 to 12, then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 12 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 12 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 4 is open. If pins 4 and 12 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9V/V.

Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM389 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM389 with higher gains (bypassing the 1.35 kΩ resistor between pins 4 and 12) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance of the driven input.

Supplies and Grounds

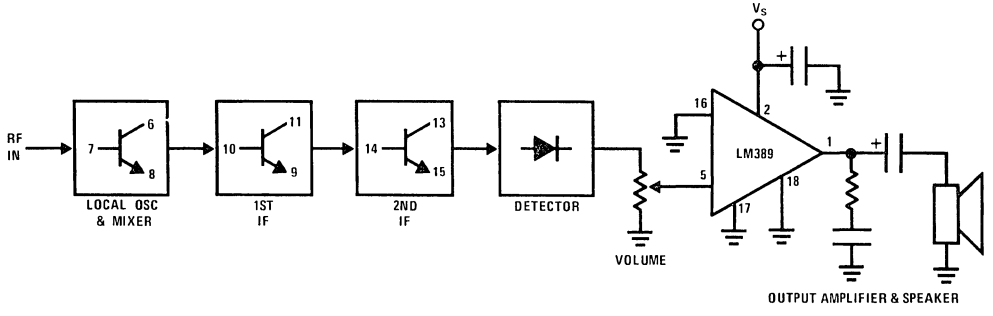
The LM389 has excellent supply rejection and does not require a well regulated supply. However, to eliminate possible high frequency stability problems, the supply should be decoupled to ground with a 0.1 μF capacitor. The high current ground of the output transistor, pin 18, is brought out separately from small signal ground, pin 17. If the two ground leads are returned separately to supply then the parasitic resistance in the power ground lead will not cause stability problems. The parasitic resistance in the signal ground can cause stability problems and it should be minimized. Care should also be taken to insure that the power dissipation does not exceed the maximum dissipation of the package for a given temperature. There are two ways to mute the LM389 amplifier. Shorting pin 3 to the supply voltage, or shorting pin 12 to ground will turn the amplifier off without affecting the input signal.

Transistors

The three transistors on the LM389 are general purpose devices that can be used the same as other small signal transistors. As long as the currents and voltages are kept within the absolute maximum limitations, and the collectors are never at a negative potential with respect to pin 17, there is no limit on the way they can be used.

For example, the emitter-base breakdown voltage of 7.1V can be used as a zener diode at currents from 1 μA to 5 mA. These transistors make good LED driver devices, V_{SAT} is only 150 mV when sinking 10 mA.

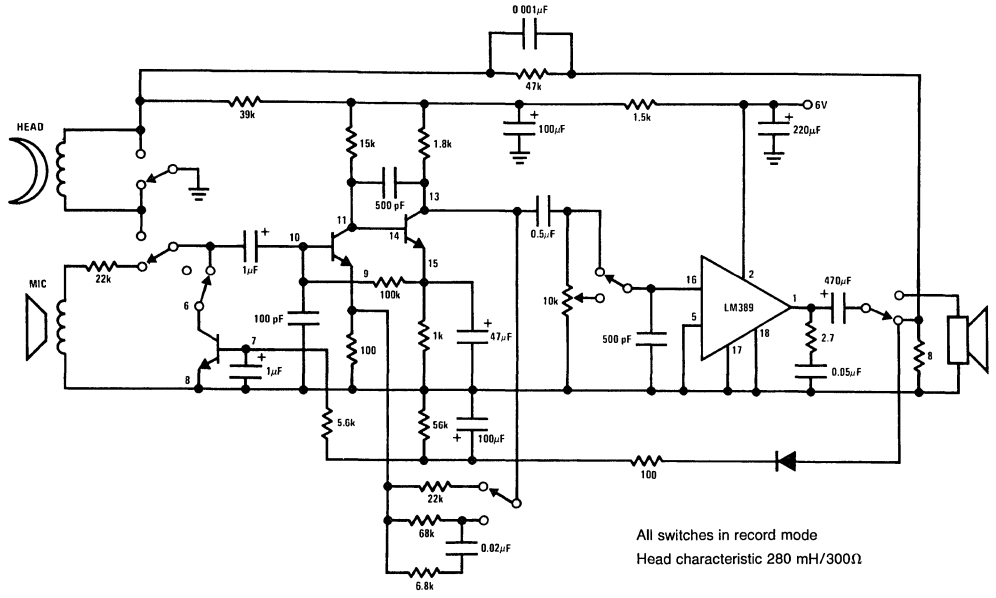
In the linear region, these transistors have been used in AM and FM radios, tape recorders, phonographs and many other applications. Using the characteristic curves on noise voltage and noise current, the level of the collector current can be set to optimize noise performance for a given source impedance. Some of the circuits that have been built are shown in *Figures 1–7*. This is by no means a complete list of applications, since that is limited only by the designers imagination.



TL/H/7847–6

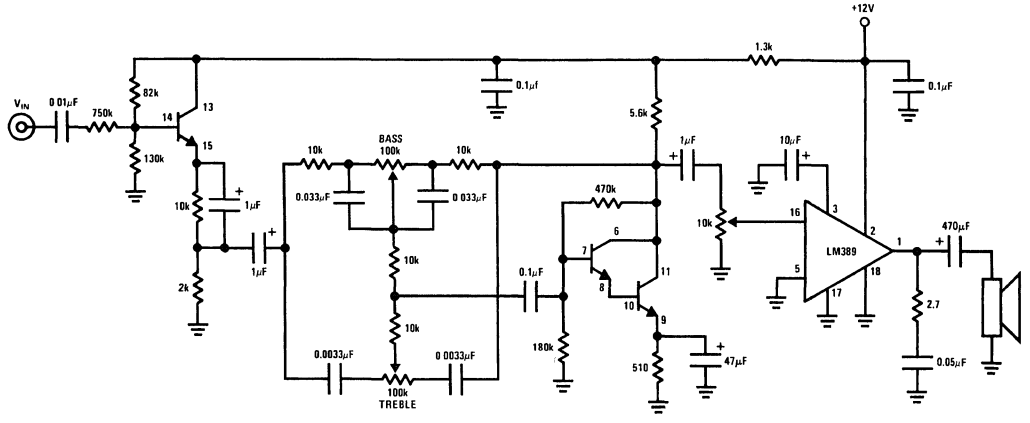
FIGURE 1. AM Radio

Application Hints (Continued)



TL/H/7847–7

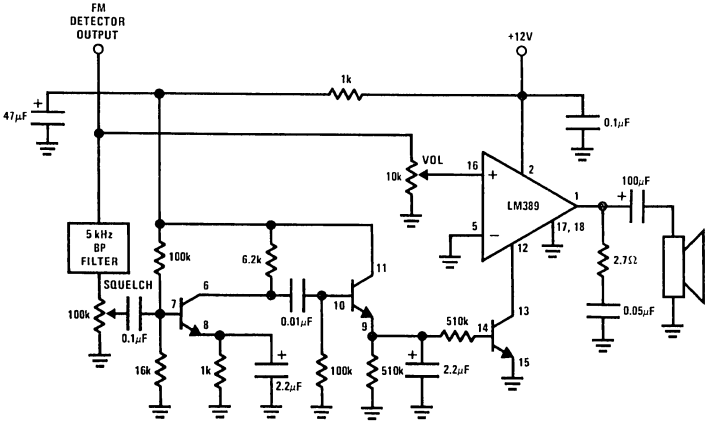
FIGURE 2. Tape Recorder



TL/H/7847–8

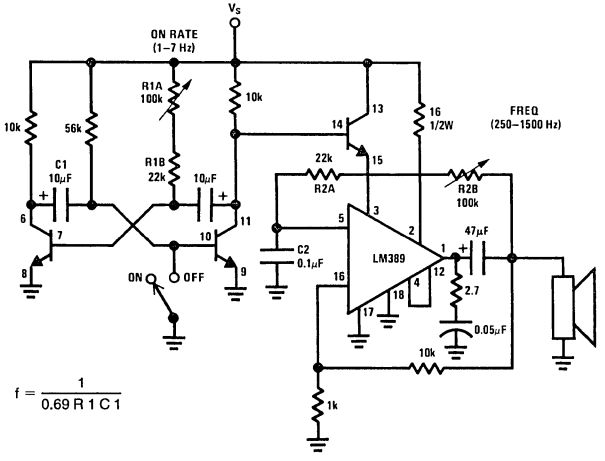
FIGURE 3. Ceramic Phono Amplifier with Tone Controls

Application Hints (Continued)



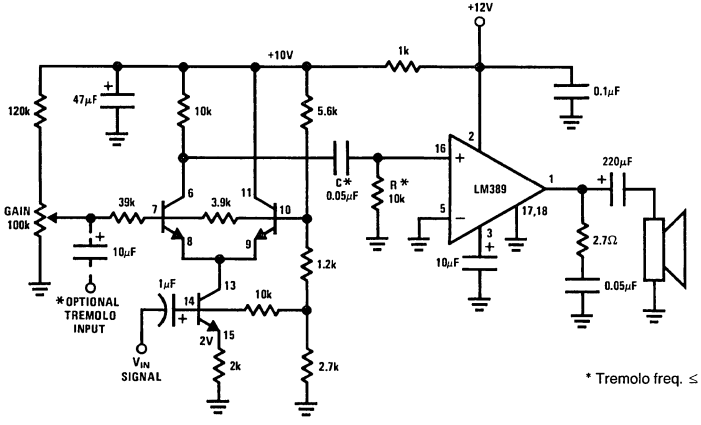
TL/H/7847–9

FIGURE 4. FM Scanner Noise Squelch Circuit



TL/H/7847–10

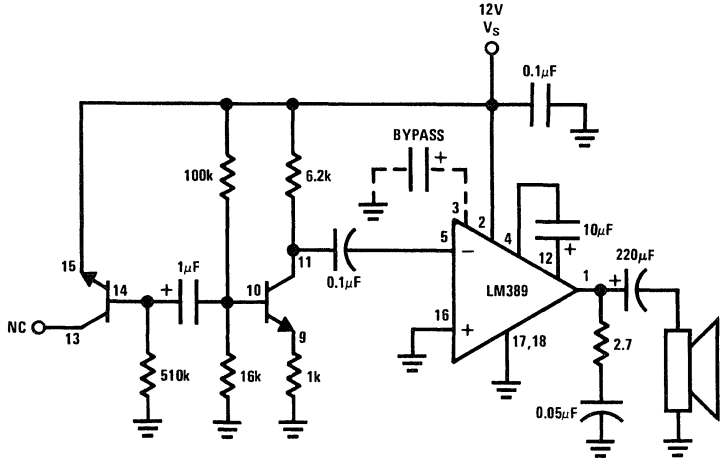
FIGURE 5. Siren



TL/H/7847–11

FIGURE 6. Voltage-Controlled Amplifier or Tremolo Circuit

Application Hints (Continued)



TL/H/7847–12

FIGURE 7. Noise Generator Using Zener Diode

National Semiconductor Corporation

LM390 1 Watt Battery Operated Audio Power Amplifier

General Description

The LM390 Power Audio Amplifier is optimized for 6V, 7.5V, 9V operation into low impedance loads. The gain is internally set at 20 to keep the external part count low, but the addition of an external resistor and capacitor between pins 2 and 6 wil increase the gain to any value up to 200. The inputs are ground referenced while the output is automatically biased to one half the supply voltage.

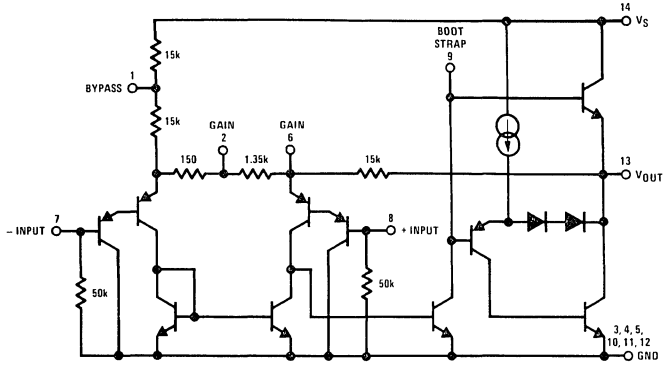
Features

- Battery operation
- 1W output power
- Minimum external parts
- Excellent supply rejection
- Ground referenced input
- Self-centering output quiescent voltage
- Variable voltage gain
- Low distortion
- Fourteen pin dual-in-line package

Applications

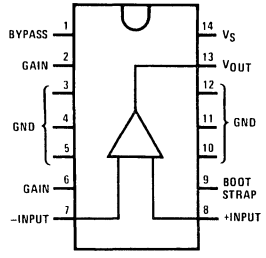
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Lamp drivers
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



TL/H/7848–1

Dual-In-Line Package



TL/H/7848–2

Order Number LM390N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	10V
Package Dissipation 14-Pin DIP (Note 1)	8.3W
Input Voltage	±0.4V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics T_A = 25°C, *(Figure 1)*

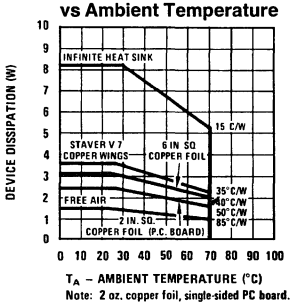
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_S	Operating Supply Voltage		4		9	V
I_Q	Quiescent Current	V_S = 6V, V_{IN} = 0		10	20	mA
P_{OUT}	Output Power	V_S = 6V, R_L = 4Ω, THD = 10%	0.8	1.0		W
A_V	Voltage Gain	V_S = 6V, f 1 kHz 10 μF from Pin 2 to 6	23	26 46	30	dB dB
BW	Bandwidth	V_S = 6V, Pins 2 and 6 Open		300		kHz
THD	Total Harmonic Distortion	V_S = 6V, R_L = 4Ω, P_{OUT} = 500 mW f = 1 kHz, Pins 2 and 6 Open		0.2	1	%
PSRR	Power Supply Rejection Ratio	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 μF, Pins 2 and 6 Open, Referred to Output (Note 2)		50		dB
R_{IN}	Input Resistance		10	50		kΩ
I_{BIAS}	Input Bias Current	V_S = 6V, Pins 7 and 8 Open		250		nA

Note 1: Pins 3, 4, 5, 10, 11, 12 at 25°C. Derate at 15°C/W above 25°C case.

Note 2: If load and bypass capacitor are returned to V_S *(Figure 2)*, rather than ground *(Figure 1)*, PSRR is typically 30 dB.

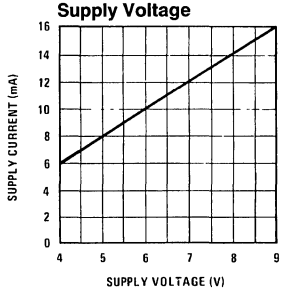
Typical Performance Characteristics

Maximum Device Dissipation vs Ambient Temperature

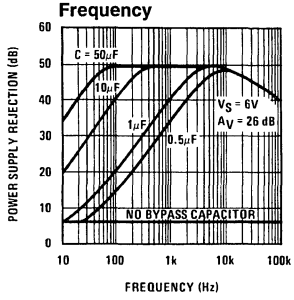


Note: 2 oz. copper foil, single-sided PC board.

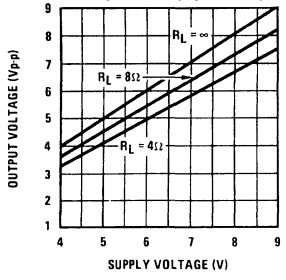
Quiescent Supply Current vs Supply Voltage



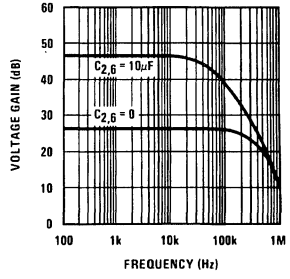
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



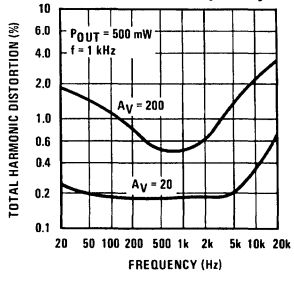
Peak-to-Peak Output Voltage Swing vs Supply Voltage



Voltage Gain vs Frequency



Distortion vs Frequency



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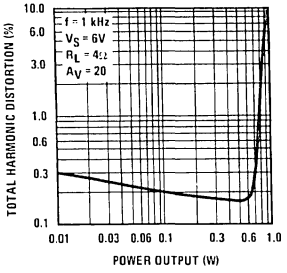
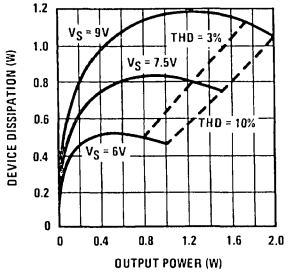
Typical Performance Characteristics (Continued)

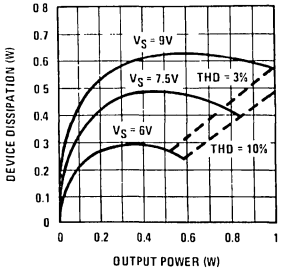
Distortion vs Output Power



Device Dissipation vs Output Power 4Ω Load



Device Dissipation vs Output Power 8Ω Load



TL/H/7848–6

Application Hints

Gain Control

To make the LM390 a more versatile amplifier, two pins (2 and 6) are provided for gain control. With pins 2 and 6 open, the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 2 to 6, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. A low frequency pole in the gain response is caused by the capacitor working against the external resistor in series with the 150Ω internal resistor. If the capacitor is eliminated and a resistor connects pin 2 to 6 then the output dc level may shift due to the additional dc gain. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 6 to ground, as in *Figure 7*.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 6 to 13 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 2 is open. If pins 2 and 6 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9 V/V.

Input Biasing

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM390 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM390 with higher gains (bypassing the 1.35 kΩ resistor between pins 2 and 6) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

Bootstrapping

The base of the output transistor of the LM390 is brought out to pin 9 for Bootstrapping. The output stage of the amplifier during positive swing is shown in *Figure 3* with its external circuitry.

R1 + R2 set the amount of base current available to the output transistor. The maximum output current divided by beta is the value required for the current in R1 and R2:

$$(R1 + R2) = \beta_O \frac{(V_S/2) - V_{BE}}{I_{O\,MAX}}$$

Good design values are $V_{BE} = 0.7V$ and $\beta_O = 100$.

Example 0.8 watt into 4Ω load with $V_S = 6V$.

$$I_{O\,MAX} = \sqrt{\frac{2\,P_O}{R_L}} = 632\ mA$$

$$(R1 + R2) = 100\left(\frac{(6/2) - 0.7}{0.632}\right) = 364\Omega$$

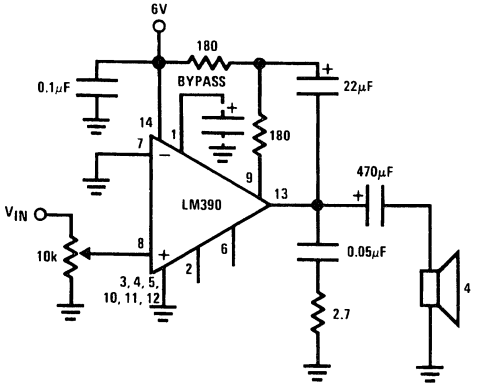
To keep the current in R2 constant during positive swing capacitor C_B is added. As the output swings positive C_B lifts R1 and R2 above the supply, maintaining a constant voltage across R2. To minimize the value of C_B, R1 = R2. The pole due to C_B and R1 and R2 is usually set equal to the pole due to the output coupling capacitor and the load. This gives:

$$C_B \cong \frac{4C_c}{\beta_O} \cong \frac{C_c}{25}$$

Example: for 100 Hz pole and $R_L = 4\Omega$; $C_c = 400\ \mu F$ and $C_B = 16\ \mu F$, if R1 is made a diode and R2 increased to give the same current, C_B can be decreased by about a factor of 4, as in *Figure 4*.

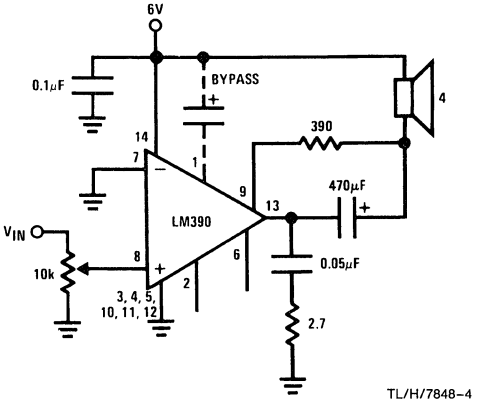
For reduced component count the load can replace R1. The value of (R1 + R2) is the same, so R2 is increased. Now C_B is both the coupling and the bootstrapping capacitor (see *Figure 2*).

Typical Applications



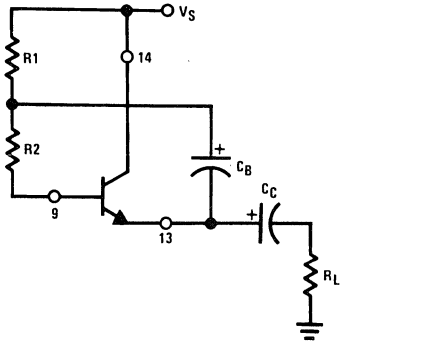
TL/H/7848–3

FIGURE 1. Load Returned to Ground (Amplifier with Gain = 20)



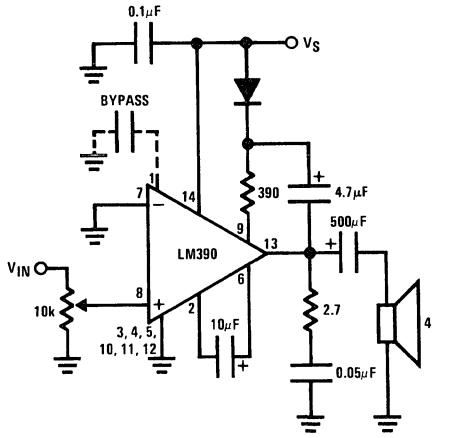
TL/H/7848–4

FIGURE 2. Load Returned to Supply (Amplifier with Gain = 20)



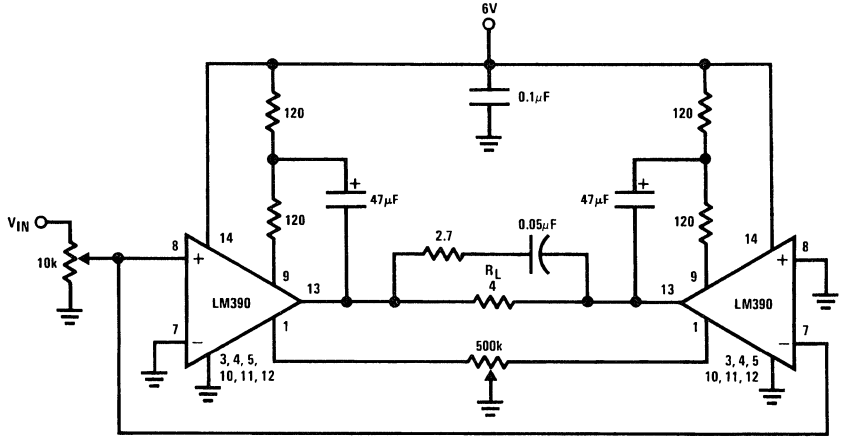
TL/H/7848–7

FIGURE 3



TL/H/7848–8

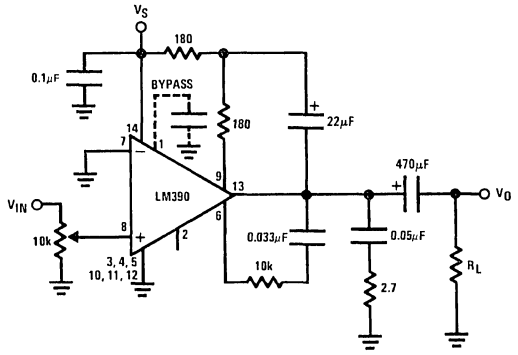
FIGURE 4. Amplifier with Gain = 200 and Minimum C_B



TL/H/7848–9

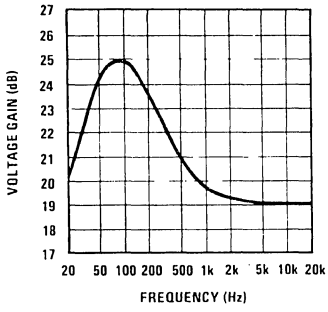
FIGURE 5. 2.5W Bridge Amplifier

Typical Applications (Continued)



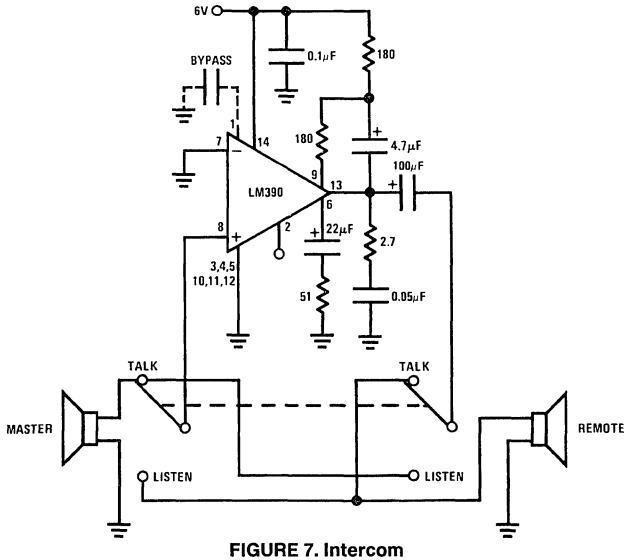
TL/H/7848–10

FIGURE 6(a). Amplifier with Bass Boost



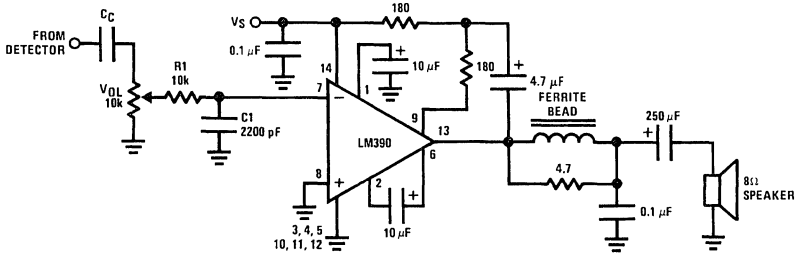
TL/H/7848–11

FIGURE 6(b). Frequency Response with Bass Boost



TL/H/7848–12

FIGURE 7. Intercom



TL/H/7848–13

FIGURE 8. AM Radio Power Amplifier

Note 1: Twist supply lead and supply ground very tightly.

Note 2: Twist speaker lead and ground very tightly.

Note 3: Ferrite bead is Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 4: R1C1 band limits input signals.

Note 5: All components must be spaced very close to IC.

National Semiconductor Corporation

LM391 Audio Power Driver

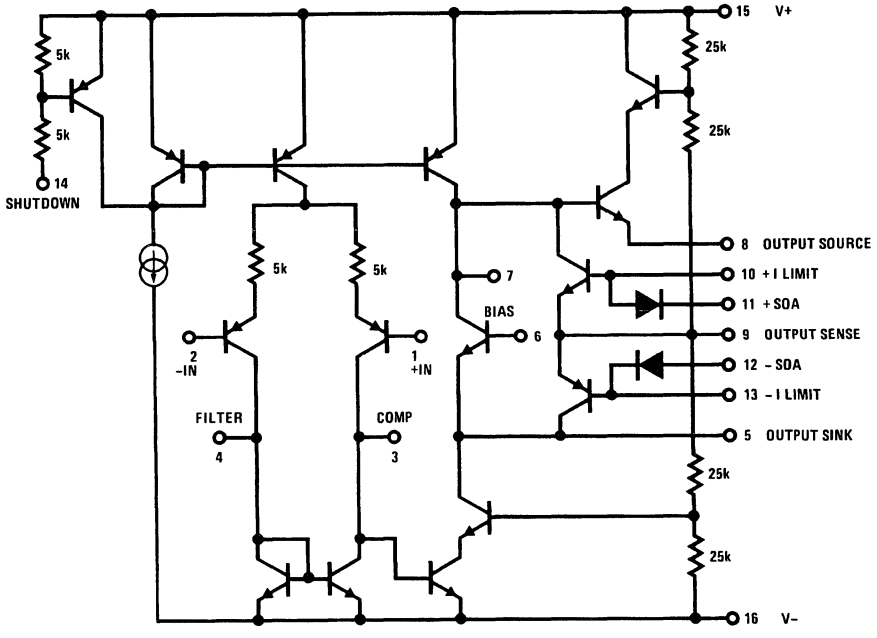
General Description

The LM391 audio power driver is designed to drive external power transistors in 10 to 100 watt power amplifier designs. High power supply voltage operation and true high fidelity performance distinguish this IC. The LM391 is internally protected for output faults and thermal overloads; circuitry providing output transistor protection is user programmable.

Features

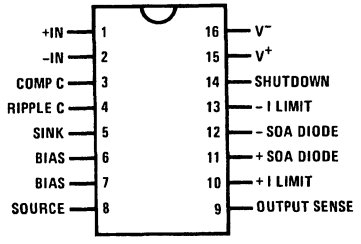
■ High Supply Voltage	±50V max
■ Low Distortion	0.01%
■ Low Input Noise	3 μV
■ High Supply Rejection	90 dB
■ Gain and Bandwidth Selectable	
■ Dual Slope SOA Protection	
■ Shutdown Pin	

Equivalent Schematic and Connection Diagram



TL/H/7146-1

Dual-In-Line Package



TL/H/7146-2

Top View

Order Number LM391N-100
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
LM391N-100	±50V or +100V
Input Voltage	Supply Voltage less 5V
Shutdown Current (Pin 14)	1 mA
Package Dissipation (Note 1)	1.39W
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temp. (Soldering, 10 sec.)	260°C

Electrical Characteristics $T_A = 25°C$ (The following are for $V^+ = 90\%\ V^+_{MAX}$ and $V^- = 90\%\ V^-_{MAX}$.)

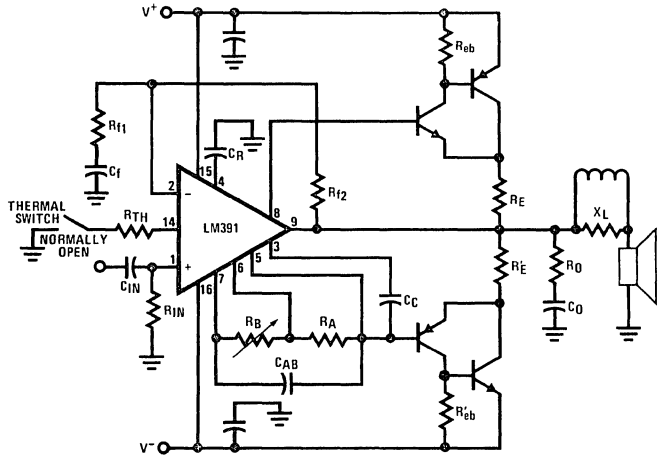
Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current LM391N-100	Current in Pin 15 $V_{IN} = 0$		 5	 6	mA
Output Swing	Positive Negative	$V^+ - 7$ $V^- + 7$	$V^+ - 5$ $V^- + 5$		V V
Drive Current	Source (Pin 8) Sink (Pin 5)	5 5			mA mA
Noise (20 Hz–20 kHz)	Input Referred		3		μV
Supply Rejection	Input Referred	70	90		dB
Total Harmonic Distortion	f = 1 kHz f = 20 kHz		0.01 0.10	 0.25	% %
Intermodulation Distortion	60 Hz, 7 kHz, 4:1		0.01		%
Open Loop Gain	f = 1 kHz	1000	5500		V/V
Input Bias Current			0.1	1.0	μA
Input Offset Voltage			5	20	mV
Positive Current Limit V_{BE}	Pin 10–9		650		mV
Negative Current Limit V_{BE}	Pin 9–13		650		mV
Positive Current Limit Bias Current	Pin 10		10	100	μA
Negative Current Limit Bias Current	Pin 13		10	100	μA

Pin 14 Current Comments

Minimum pin 14 current required for shutdown is 0.5 mA, and must not exceed 1 mA.
Maximum pin 14 current for amplifier not shut down is 0.05 mA.
The typical shutdown switch point current is 0.2 mA.

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Typical Applications

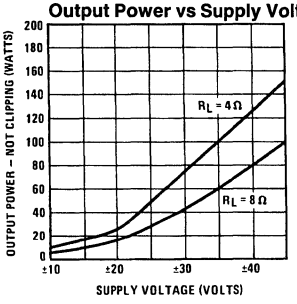


TL/H/7146–3

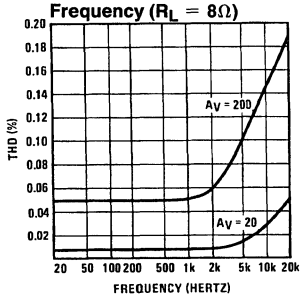
FIGURE 1. LM391 with External Components—Protection Circuitry Not Shown

Typical Performance Characteristics

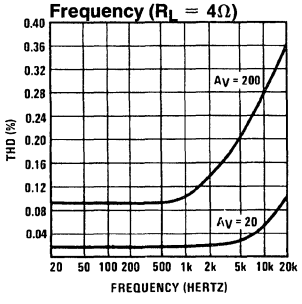
Output Power vs Supply Voltage



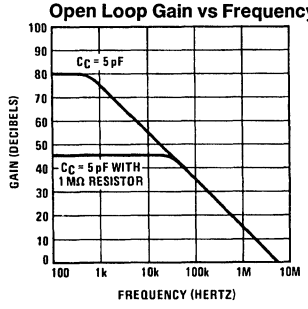
Total Harmonic Distortion vs Frequency ($R_L = 8\Omega$)



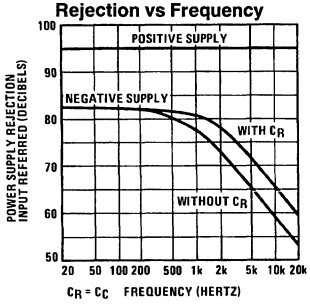
Total Harmonic Distortion vs Frequency ($R_L = 4\Omega$)



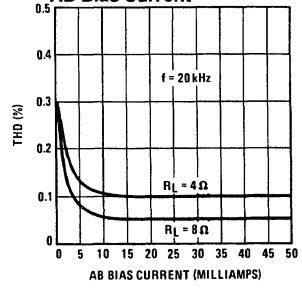
Open Loop Gain vs Frequency



Input Referred Power Supply Rejection vs Frequency



Total Harmonic Distortion vs AB Bias Current



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Pin Descriptions

Pin No.	Pin Name	Comments
1	+ Input	Audio input
2	− Input	Feedback input
3	Compensation	Sets the dominant pole
4	Ripple Filter	Improves negative supply rejection
5	Sink Output	Drives output devices and is emitter of AB bias V_{BE} multiplier
6	BIAS	Base of V_{BE} multiplier
7	BIAS	Collector of V_{BE} multiplier
8	Source Output	Drives output devices
9	Output Sense	Biases the IC and is used in protection circuits
10	+ Current Limit	Base of positive side protection circuit transistor
11	+ SOA Diode	Diode used for dual slope SOA protection
12	− SOA Diode	Diode used for dual slope SOA protection
13	− Current Limit	Base of negative side protection circuit transistor
14	Shutdown	Shuts off amplifier when current is pulled out of pin
15	V+	Positive supply
16	V−	Negative supply

External Components (Figure 1)

Component	Typical Value	Comments
C_{IN}	1 μF	Input coupling capacitor sets a low frequency pole with R_{IN}. $f_L = \frac{1}{2\pi R_{IN} C_{IN}}$
R_{IN}	100k	Sets input impedance and DC bias to input.
R_{f_2}	100k	Feedback resistor; for minimum offset voltage at the output this should be equal to R_{IN}.
R_{f_1}	5.1k	Feedback resistor that works with R_{f_2} to set the voltage gain. $A_V = 1 + \frac{R_{f_2}}{R_{f_1}}$
C_f	10 μF	Feedback capacitor. This reduces the gain to unity at DC for minimum offset voltage at the output. Also sets a low frequency pole with R_{f_1}. $f_L = \frac{1}{2\pi R_{f_1} C_f}$
C_C	5 pF	Compensation capacitor. Sets gain bandwidth product and a high frequency pole. $GBW = \frac{1}{2\pi 5000 C_C}$, $f_h = \frac{GBW}{A_V}$ Max f_h for stable design $\approx$ 500 kHz.
R_A	3.9k	AB bias resistor.
R_B	10k	AB bias potentiometer. Adjust to set bias current in the output stage.
C_{AB}	0.1 μF	Bypass capacitor for bias. This improves high frequency distortion and transient response.
C_R	5 pF	Ripple capacitor. This improves negative supply rejection at midband and high frequencies. C_R, if used, must equal C_C.
R_{eb}	100Ω	Bleed resistor. This removes stored charge in output transistors.
R_O	2.7Ω	Output compensation resistor. This resistor and C_O compensate the output stage. This value will vary slightly for different output devices.
C_O	0.1 μF	Output compensation capacitor. This works with R_O to form a zero that cancels f_β of the output power transistors.
R_E	0.3Ω	Emitter degeneration resistor. This resistor gives thermal stability to the output stage quiescent current. IRC PW5 type.
R_{TH}	39k	Shutdown resistor. Sets the amount of current pulled out of pin 14 during shutdown.
C_2, C'_2	1000 pF	Compensation capacitors for protection circuitry.
X_L	10$\Omega \| 5$ μH	Used to isolate capacitive loads, usually 20 turns of wire wrapped around a 10Ω, 2W resistor.

Application Hints

GENERALIZED AUDIO POWER AMP DESIGN

Givens: Power Output
Load Impedance
Input Sensitivity
Input Impedance
Bandwidth

The power output and load impedance determine the power supply requirements. Output signal swing and current are found from:

$$V_{Opeak} = \sqrt{2\,R_L\,P_O} \quad (1)$$

$$I_{Opeak} = \sqrt{\frac{2\,P_O}{R_L}} \quad (2)$$

Add 5 volts to the peak output swing (V_{OP}) for transistor voltage to get the supplies, i.e., $\pm$ (V_{OP} + 5V) at a current of I_{peak}. The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions.

$$\text{max supplies} \approx \pm(V_{Opeak} + 5)\,(1 + \text{regulation})\,(1.1) \quad (3)$$

The input sensitivity and output power specs determine the required gain.

$$A_V \geq \frac{\sqrt{P_O\,R_L}}{V_{IN}} = \frac{V_{ORMS}}{V_{INRMS}} \quad (4)$$

Normally the gain is set between 20 and 200; for a 25 watt, 8 ohm amplifier this results in a sensitivity of 710 mV and 71 mV, respectively. The higher the gain, the higher the THD, as can be seen from the characteristics curves. Higher gain also results in more hum and noise at the output.

The desired input impedance is set by R_{IN}. Very high values can cause board layout problems and DC offsets at the output. The bandwidth requirements determine the size of C_f and C_C as indicated in the external component listing.

The output transistors and drivers must have a breakdown voltage greater than the voltage determined by equation (3). The current gain of the drive and output device must be high enough to supply I_{Opeak} with 5 mA of drive from the LM391. The power transistors must be able to dissipate approximately 40% of the maximum output power; the drivers must dissipate this amount divided by the current gain of the outputs. See the output transistor selection guide, Table A.

To prevent thermal runaway of the AB bias current the following equation must be valid:

$$\theta_{JA} \leq \frac{R_E\,(\beta_{MIN} + 1)}{V_{CEQMAX}\,(K)} \quad (5)$$

where:

θ_{JA} is the thermal resistance of the driver transistor, junction to ambient, in °C/W.

R_E is the emitter degeneration resistance in ohms.

β_{min} is that of the output transistor.

V_{CEQMAX} is the highest possible value of one supply from equation (3).

K is the temperature coefficient of the driver base-emitter voltage, typically 2 mV/°C.

Often the value of R_E is to be determined and equation (5) is rearranged to be:

$$R_E \geq \frac{\theta_{JA}\,(V_{CEQMAX})\,K}{\beta_{MIN} + 1} \quad (6)$$

The maximum average power dissipation in each output transistor is:

$$\overline{P_{DMAX}} = 0.4\,P_{OMAX} \quad (7)$$

The power dissipation in the driver transistor is:

$$\overline{P_{DRIVER(MAX)}} = \frac{\overline{P_{DMAX}}}{\beta_{MIN}} \quad (8)$$

Heat sink requirements are found using the following formulas:

$$\theta_{JA} \leq \frac{T_{JMAX} - T_{AMAX}}{P_D} \quad (9)$$

$$\theta_{SA} \leq \theta_{JA} - \theta_{JC} - \theta_{CS} \quad (10)$$

where:

T_{jMAX} is the maximum transistor junction temperature.

T_{AMAX} is the maximum ambient temperature.

θ_{JA} is thermal resistance junction to ambient.

θ_{SA} is thermal resistance sink to ambient.

θ_{JC} is thermal resistance junction to case.

θ_{CS} is thermal resistance case to sink, typically 1°C/W for most mountings.

Application Hints (Continued)

PROTECTION CIRCUITRY

The protection circuits of the LM391 are very flexible and should be tailored to the output transistor's safe operating area. The protection V-I characteristics, circuitry, and resistor formulas are described below. The diodes from the output to each supply prevent the output voltage from exceeding the supplies and harming the output transistors. The output will do this if the protection circuitry is activated while driving an inductive load.

TURN-ON DELAY

It is often desirable to delay the turn-ON of the power amplifier. This is easily implemented by putting a resistor in series with a capacitor from pin 14 to ground. The value of the resistor is set to limit the current to less than 1 mA (the absolute maximum). This resistor with the capacitor gives a time constant of RC. The turn-ON delay is approximately 2 time constants.

Example:

Amplifier with maximum supply of 30V, like the 20W, 8Ω example in the data sheet, requiring a delay of 1 second.

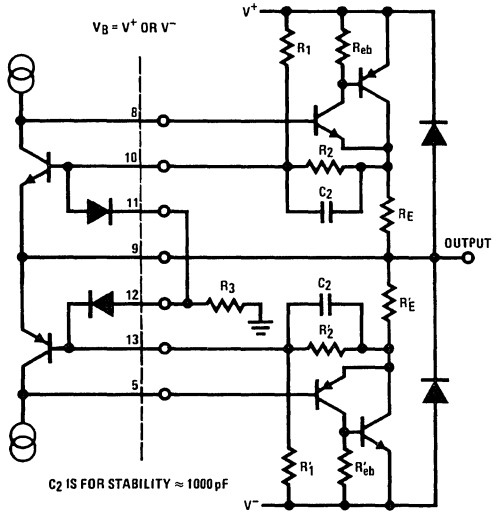
Time delay = 2 RC

$$R = \frac{\text{Max } V^+}{1\text{ mA}}$$

So:

R = 30k. Solving for C gives 16.7 μF. Use C = 20 μF with a 30V rating.

Protection Circuitry with External Components



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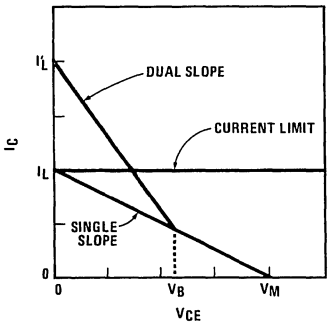
Protection Characteristics



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Protection Circuit Resistor Formulas ($V_B = V^+$)

Type of Protection	R_E, R'	R_1, R'_1	R_2, R'_2	R_3, R'_3
Current Limit	$R_E = \frac{\phi}{I_L}$	Not Required	Short	Not Required
Single Slope SOA Protection	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2\left(\frac{V_M - \phi}{\phi}\right)$	1 kΩ	Not Required
Dual Slope SOA Protection ($V_B = V^+$)	$R_E = \frac{\phi}{I_L}$	$R_1 = R_2\left(\frac{V_M - \phi}{\phi}\right)$	1 kΩ	$R_3 = R_2\left[\frac{V^+}{I'_L R_E - \phi} - 1\right]$

Note: ϕ is the current limit V_{BE} voltage, 650 mV. Assumptions: $V^+ >> \phi$, $V_M >> \phi$. V^+ is the load supply voltage. V_M is the maximum rated V_{CE} of the output transistors.

Application Hints (Continued)

TRANSIENT INTERMODULATION DISTORTION

There has been a lot of interest in recent years about transient intermodulation distortion. Matti Otala of University of Oulu, Oulu, Finland has published several papers on the subject. The results of these investigations show that the open loop pole of the power amplifier should be above 20 kHz.

To do this with the LM391 is easy. Put a 1 MΩ resistor from pin 3 to the output and the open loop gain is reduced to about 46 dB. Now the open loop pole is at 30 kHz. The current in this resistor causes an offset in the input stage that can be cancelled with a resistor from pin 4 to ground. The resistor from pin 4 to ground should be 910 kΩ rather than 1 MΩ to insure that the shutdown circuitry will operate correctly. The slight difference in resistors results in about 15 mV of offset. The 40W, 8Ω amplifier schematic shows the hookup of these two resistors.

BRIDGE AMPLIFIER

A switch can be added to convert a stereo amplifer to a single bridge amplifer. The diagram below shows where the switch and one resistor are added. When operating in the bridge mode the output load is connected between the two outputs, the input is V_{IN} #1, and V_{IN} #2 is disconnected.

OSCILLATIONS & GROUNDING

Most power amplifiers work the first time they are turned on. They also tend to oscillate and have excess THD. Most oscillation problems are due to inadequate supply bypassing and/or ground loops. A 10 μF, 50V electrolytic on each power supply will stop supply-related oscillations. However, if the signal ground is used for these bypass caps the THD is usually excessive. The signal ground must return to the power supply alone, as must the output load ground. All other grounds—bypass, output R-C, protection, etc., can tie together and then return to supply. This ground is called high frequency ground. On the 40W amplifier schematic all the grounds are labeled.

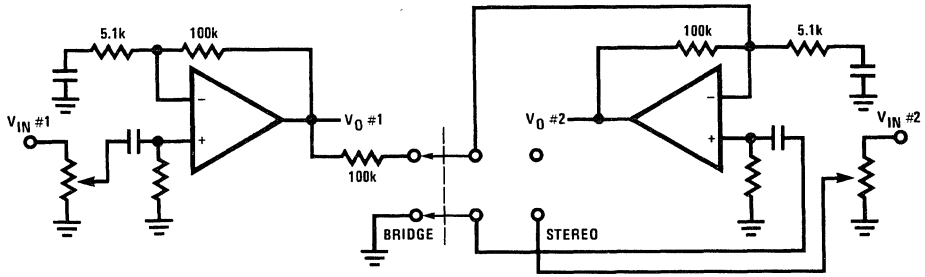
Capacitive loads can cause instabilities, so they are isolated from the amplifier with an inductor and resistor in the output lead.

AB BIAS CURRENT

To reduce distortion in the output stage, all the transistors are biased ON slightly. This results in class AB operation and reduces the crossover (notch) distortion of the class B stage to a low level, (see performance curve, THD vs AB bias). The potentiometer, R_B, from pins 6–7 is adjusted to give about 25 mA of current in the output stage. This current is usually monitored at the supply or by measuring the voltage across R_E.

Typical Applications (Continued)

Bridge Circuit Diagram



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Output Transistors Selection Guide

Table A.

Power Output	Driver Transistor		Output Transistor	
	PNP	NPN	PNP	NPN
20W @ 8Ω 30W @ 4Ω	MJE711 MJE171 D43C8	MJE721 MJE181 D42C8	TIP42A 2N6490	TIP41A 2N6487
40W @ 8Ω 60W @ 4Ω	MJE712 MJE172 D43C11	MJE722 MJE182 D42C11	2N5882	2N5880

Application Hints (Continued)

A 20W, 8Ω; 30W, 4Ω AMPLIFIER

Givens:

Power Output	20W into 8Ω 30W into 4Ω
Input Sensitivity	1V Max
Input Impedance	100k
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

20W/8Ω $V_{OP} = 17.9V$ $I_{OP} = 2.24A$

30W/4Ω $V_{OP} = 15.5V$ $I_{OP} = 3.87A$

Therefore the supply required is:

±23V @ 2.24A, reducing to . . .

±21V @ 3.87A

With 15% regulation and high line we get ±29V from equation (3).

Sensitivity and equation (4) set minimum gain:

$$A_V \geq \frac{\sqrt{20 \times 8}}{1} = 12.65$$

We will use a gain of 20 with resulting sensitivity of 632 mV.

Letting R_{IN} equal 100k gives the required input impedance. For low DC offsets at the output we let $R_{f_2} = 100k$. Solving for R_{f_1} gives:

$$R_{f_2} = 100k$$

$$R_{f_1} = \frac{100k}{20 - 1} = 5.26k; \text{ use } 5.1k$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole gives 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = \frac{20}{5} = 4 \text{ Hz}$$

$$f_h = 20k \times 5 = 100 \text{ kHz}$$

Solving for C_f:

$$C_f \geq \frac{1}{2\pi R_{f_1} f_L} = 7.8\ \mu F; \text{ use } 10\ \mu F$$

The recommended value for C_C is 5 pF for gains of 20 or larger. This gives a gain-bandwidth product of 6.4 MHz and a resulting bandwidth of 320 kHz, better than required.

The breakdown voltage requirement is set by the maximum supply; we need a minimum of 58V and will use 60V. We must now select a 60V power transistor with reasonable beta at I_{Opeak}, 3.87A. The TIP42, TIP41 complementary pair are 60V, 60W transistors with a minimum beta of 30 at 4A. The driver transistor must supply the base drive given 5 mA drive from the LM391. The MJE711, MJE721 complementary driver transistors are 60V devices with a minimum beta of 40 at 200 mA. The driver transistors should be much faster (higher f_T) than the output transistors to insure that the R-C on the output will prevent instability.

To find the heat sink required for each output transistor we use equations (7), (9), and (10):

$$\overline{P_D} = 0.4\,(30) = 12W \quad (7)$$

$$\theta_{JA} \leq \frac{150°C - 55°C}{12} = 7.9°C/W \text{ for } T_{AMAX} = 55°C \quad (9)$$

$$\theta_{SA} \leq 7.9 - 2.1 - 1.0 = 4.8°C/W \quad (10)$$

If both transistors are mounted on one heat sink the thermal resistance should be halved to 2.4°C/W.

The maximum average power dissipation in each driver is found using equation (8):

$$\overline{P_{DRIVER(MAX)}} = \frac{12}{30} = 400 \text{ mW}$$

Using equation (9):

$$\theta_{JA} \leq \frac{155 - 55}{0.4} = 237°C/W$$

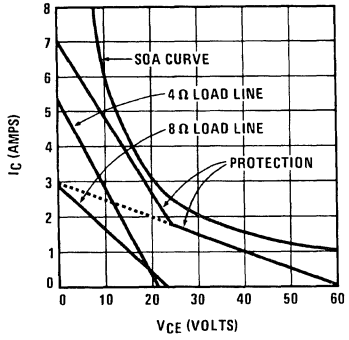
Application Hints (Continued)

Since the free air thermal resistance of the MJE711, MJE721 is 100°C/W, no heat sink is required. Using this information and equation (6) we can find the minimum value of R_E required to prevent thermal runaway.

$$R_E \geq \frac{100\ (30)\ (0.002)}{30 + 1} = 0.19\Omega \qquad (6)$$

We must now use the SOA data on the TIP42, TIP41 transistors to set up the protection circuit. Below is the SOA curve with the 4Ω and 8Ω load lines. Also shown are the desired protection lines. Note the value of V_B is equal to the supply voltage, so we use the formulas in the table.

D.C. SOA of TIP42, TIP41 Transistors



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The data points from the curve are:

$$V_M = 60V,\ V_B = 23V,\ I_L = 3A,\ I_L' = 7A$$

Using the dual slope protection formulas:

$$R_E = \frac{0.65}{3} = 0.22\Omega$$

$$R_2 = 1k$$

$$R_1 = 1k\left(\frac{60 - 0.65}{0.65}\right) \approx 91k$$

$$R_3 = 1k\left(\frac{23}{7(0.22) - 0.65} - 1\right) \approx 24k$$

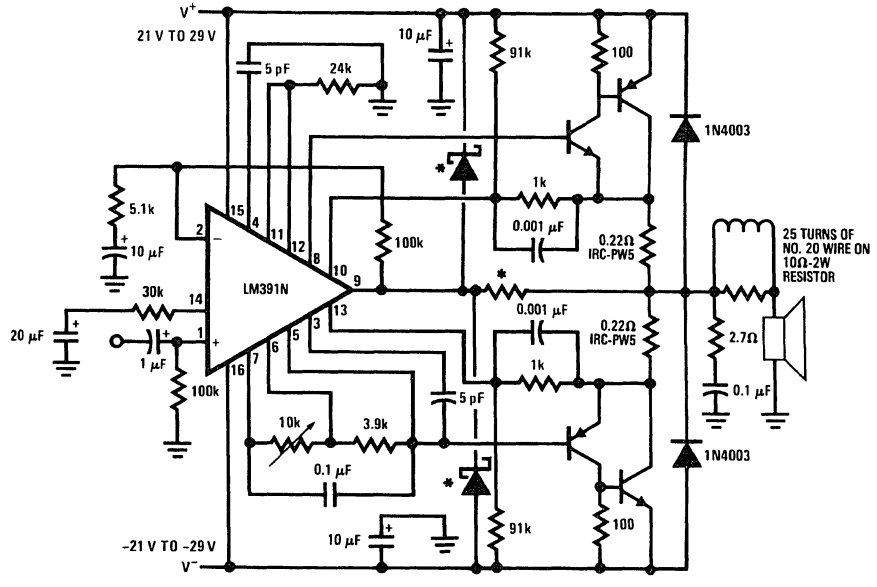
Note that an R_E of 0.22Ω satisfies equation (6). The final schematic of this amplifier is below. If the output is shorted the current will be 1.8A and V_{CE} is 23V. Since the input is AC, the average power is:

$$\text{short } \overline{P_D} = \tfrac{1}{2}(1.8)\ (23) \approx 21W$$

This power is greater than was used in the heat sink calculations, so the transistors will overheat for long-duration shorts unless a larger heat sink is used.

Typical Applications (Continued)

20W-8Ω, 30W-4Ω Amplifier with 1 Second Turn-ON Delay



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*Additional protection for LM391N; Schottky diodes and R ≅ 100Ω.

Application Hints (Continued)

A 40W/8Ω, 60W/4Ω AMPLIFIER

Given:

Power Output	40W/8Ω 60W/4Ω
Input Sensitivity	1V Max
Input Impedance	100k
Bandwidth	20 Hz–20 kHz ± 0.25 dB

Equations (1) and (2) give:

40W/8Ω $V_{OPeak} = 25.3V$ $I_{OPeak} = 3.16A$

60W/4Ω $V_{OPeak} = 21.9V$ $I_{OPeak} = 5.48A$

Therefore the supply required is:

±30.3V @ 3.16A, reducing to . . .

±26.9V @ 5.48A

With 15% regulation and high line we get ±38.3V using equation (3).

The minimum gain from equation (4) is:

$$A_V \geq 18$$

We select a gain of 20; resulting sensitivity is 900 mV.

The input impedance and bandwidth are the same as the 20 watt amplifier so the components are the same.

$R_{f_1} = 5.1k$ $R_{IN} = 100k$ $C_C = 5\ pF$

$R_{f_2} = 100k$ $C_f = 10\ \mu F$

The maximum supplies dictate using 80V devices. The 2N5882, 2N5880 pair are 80V, 160W transistors with a minimum beta of 40 at 2A and 20 at 6A. This corresponds to a minimum beta of 22.5 at 5.5A (I_{Opeak}). The MJE712, MJE722 driver pair are 80V transistors with a minimum beta of 50 at 250 mA. This output combination guarantees I_{Opeak} with 5 mA from the LM391.

Output transistor heat sink requirements are found using equations (7), (9), and (10):

$$\overline{P_D} = 0.4\,(60) = 24W \qquad (7)$$

$$\theta_{JA} \leq \frac{200 - 55}{24} = 6.0°C/W \text{ for } T_{AMAX} = 55°C \qquad (9)$$

$$\theta_{SA} \leq 6.0 - 1.1 - 1.0 = 3.9°C/W \qquad (10)$$

For both output transistors on one heat sink the thermal resistance should be 1.9°C/W.

Now using equation (8) we find the power dissipation in the driver:

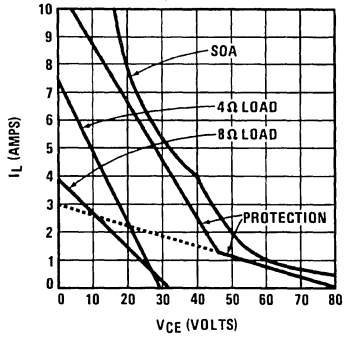
$$\overline{P_{DRIVER}} = \frac{24}{20} = 1.2W \qquad (8)$$

$$\theta_{JA} \leq \frac{150 - 55}{1.2} = 79°C/W \qquad (9)$$

Since a heat sink is required on the driver, we should investigate the output stage thermal stability at the same time to optimize the design. If we find a value of R_E that is good for the protection circuitry, we can then use equation (5) to find the heat sink required for the drivers.

The SOA characteristics of the 2N5882, 2N5880 transistors are shown in the following curve along with a desired protection line.

SOA 2N5882, 2N5880



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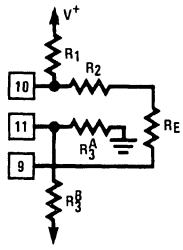
The desired data points are:

$V_M = 80V$ $V_B = 47V$ $I_L = 3A$ $I_L' = 11A$

Since the break voltage is not equal to the supply, we will use two resistors to replace R_3 and move V_B.

Circuit Used



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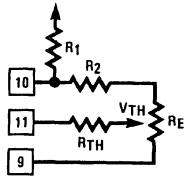
Thevenin Equivalent



Where: $R_{TH} = R_3^A \parallel R_3^B$

$$V_{TH} = V^- \left[\frac{R_3^A}{R_3^A + R_3^B}\right]$$

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Application Hints (Continued)

The formulas for R_E, R_1, and R_2 do not change:

$$R_E = \frac{0.65}{3A} = 0.22\Omega$$

$$R_2 = 1k \qquad R_1 = 1k\frac{80 - 0.65}{0.65} = 120k$$

The formula for R_3 now gives R_{TH} when the V^+ in the formula becomes V_B.

$$R_{TH} = R_2\left[\frac{V_B}{I_L R_E - \phi} - 1\right]$$

$$= 1k\left[\frac{47}{11\,(0.22) - 0.65} - 1\right] = 25.55k$$

V_{TH} is the additional voltage added to the supply voltage to get V_B.

$$V_{TH} = -(V_B - V^+) = -(47 - 30) = -17V$$

Now we must find R_3^A and R_3^B using the Thevenin formulas. Putting V_{TH}, V^-, and R_{TH} into the appropriate formulas reduces to:

$$R_3^B = 0.76\,R_3^A \qquad \text{and} \qquad 25.55k = R_3^A \,||\, R_3^B$$

The easiest way to solve these equations is to iterate with standard values. If we guess $R_3^A = 62k$, then $R_3^B = 47.12k$; use 47k. The Thevenin impedance comes out 26.7k, which is close enough to 25.55k.

Now we will use equation (5) to determine the heat sinking requirements of the drivers to insure thermal stability:

$$\theta_{JA} \le \frac{0.22\,(20 + 1)}{40\,(0.002)} \approx 57°C/W \qquad (5)$$

This value is lower than we got with equation (9), so we will use it in equation (10):

$$\theta_{SA} \le 57 - 6 - 1 = 50°C/W \qquad (10)$$

This is the required heat sink for each driver. For low TIM we add the 1 MΩ resistor from pin 3 to the output and a 910k resistor from pin 4 to ground. The complete schematic is shown below.

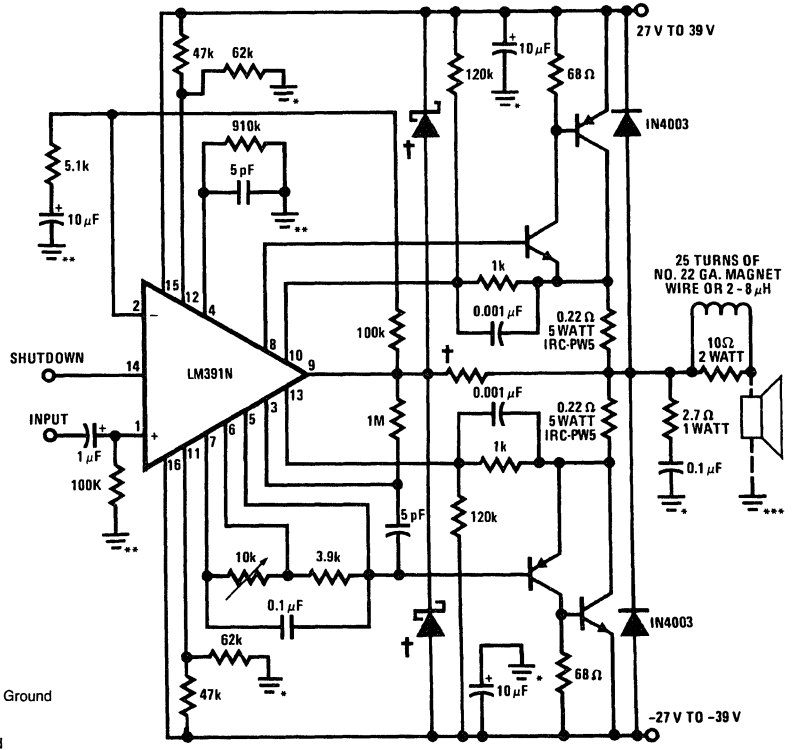
If the output is shorted, the transistor voltage is about 28V and the current is 5A. Therefore the average power is:

$$\text{short } \overline{PD} = \tfrac{1}{2}(28)\,5 = 70W$$

This is much larger than the power used to calculate the heat sinks and the output transistors will overheat if the output is shorted too long.

Typical Applications (Continued)

40W-8Ω, 60W-4Ω Amplifier



*High Frequency Ground

**Input Ground

***Speaker Ground

Note: All Grounds Should be Tied Together Only at Power Supply Ground.

†Additional protection for LM391N; Schottky diodes and R ≅ 100Ω.

TL/H/7146–13

National Semiconductor Corporation

LM831 Low Voltage Audio Power Amplifier

General Description

The LM831 is a dual audio power amplifier optimized for very low voltage operation. The LM831 has two independent amplifiers, giving stereo or higher power bridge (BTL) operation from two- or three-cell power supplies.

The LM831 uses a patented compensation technique to reduce high-frequency radiation for optimum performance in AM radio applications. This compensation also results in lower distortion and less wide-band noise.

The input is direct-coupled to the LM831, eliminating the usual coupling capacitor. Voltage gain is adjustable with a single resistor.

Features

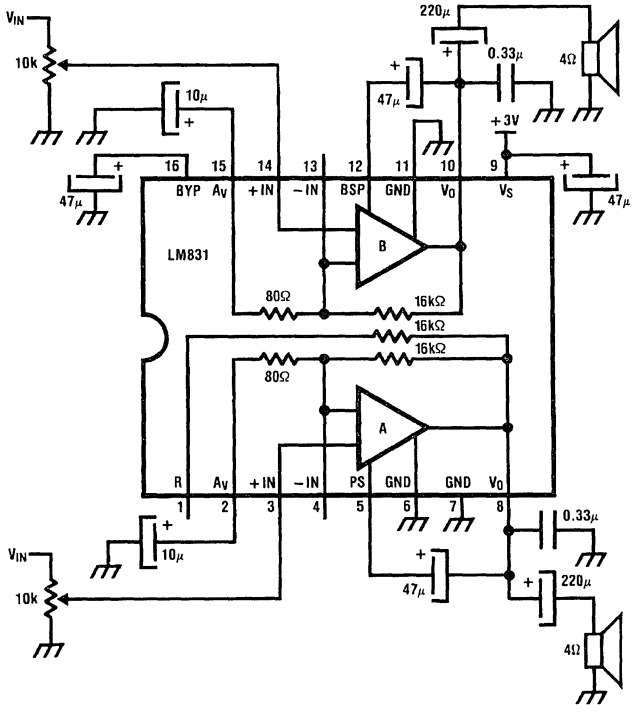
- Low voltage operation, 1.8V to 6.0V
- High power, 440 mW, 8Ω, BTL, 3V
- Low AM radiation
- Low noise
- Low THD

Applications

- Portable tape recorders
- Portable radios
- Headphone stereo
- Portable speakers

Typical Application

Dual Amplifier with Minimum Parts



TL/H/6754–1

A_V = 46 dB, BW = 250 Hz to 35 kHz

P_{OUT} = 220 mW/Ch, R_L = 4Ω

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_S	7.5V
Input Voltage, V_{IN}	±0.4V
Power Dissipation (Note 1), P_D	1.4W
Operating Temperature (Note 1), T_{opr}	−40°C to +85°C
Storage Temperature, T_{stg}	−65°C to +150°C
Junction Temperature, T_j	+150°C
Lead Temp. (Soldering, 10 sec.), T_L	+260°C

Electrical Characteristics

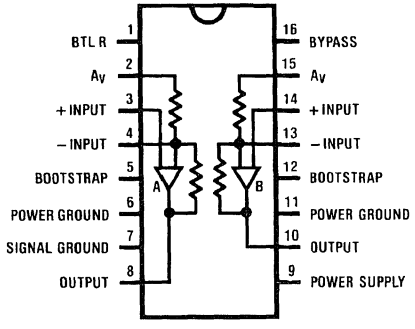
Unless otherwise specified, T_A = 25°C, V_S = 3V, f = 1 kHz, test circuit is dual or BTL amplifier with minimum parts.

Symbol	Parameter	Conditions	Typ	Tested Limit	Unit (Limit)
V_S	Operating Voltage		3 3	1.8 6	V(Min) V(Max)
I_Q	Supply Current	V_{IN} = 0, Dual Mode V_{IN} = 0, BTL Mode	5 6	10 15	mA (Max) mA (Max)
V_{OS}	Output DC Offset	V_{IN} = 0, BTL Mode	10	50	mV (Max)
R_{IN}	Input Resistance		25	15 35	k (Min) k (Max)
A_V	Voltage Gain	V_{IN} = 2.25 mV_{rms}, f = 1 kHz, Dual Mode	46	44 48	dB (Min) dB (Max)
PSRR	Supply Rejection	V_S = 3V + 200 mV_{rms} @ f = 1 kHz	46	30	dB (Min)
P_{OD}	Power Out	V_S = 3V, R_L = 4Ω, 10% THD, Dual Mode	220	150	mW (Min)
P_{ODL}	Power Out Low, V_S	V_S = 1.8V, R_L = 4Ω, 10% THD, Dual Mode	45	10	mW (Min)
P_{OB}	Power Out	V_S = 3V, R_L = 8Ω, 10% THD, BTL Mode	440	300	mW (Min)
P_{OBL}	Power Out Low, V_S	V_S = 1.8V, R_L = 8Ω, 10% THD, BTL Mode	90	20	mW (Min)
Sep	Channel Separation	Referenced to V_O = 200 mV_{rms}	52	40	dB (Min)
I_B	Input Bias Current		1	2	μA (Max)
E_{n0}	Output Noise	Wide Band (250 ~ 35 kHz)	250	500	μV (Max)
THD	Distortion	V_S = 3V, P_O = 50 mW, f = 1 kHz, Dual	0.25	1	% (Max)

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Connection Diagram

Dual-In-Line Package



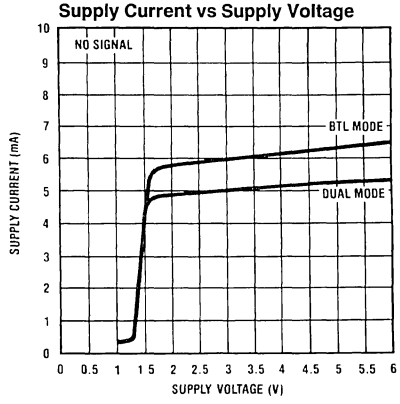
TL/H/6754–2

Top View

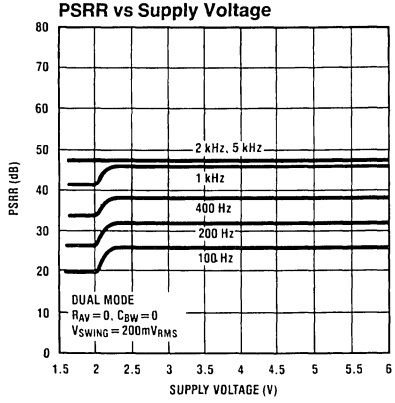
Order Number LM831N
See NS Package Number N16E

Typical Performance Characteristics

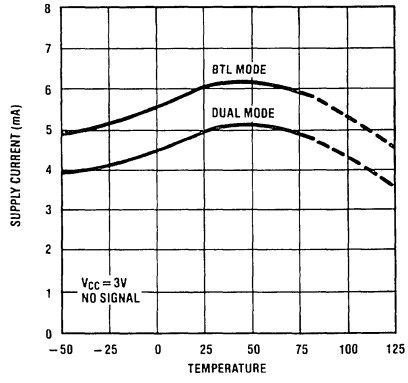
Supply Current vs Supply Voltage



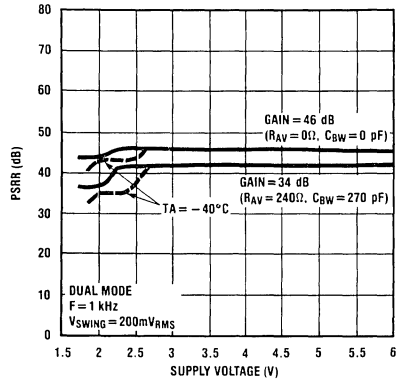
PSRR vs Supply Voltage



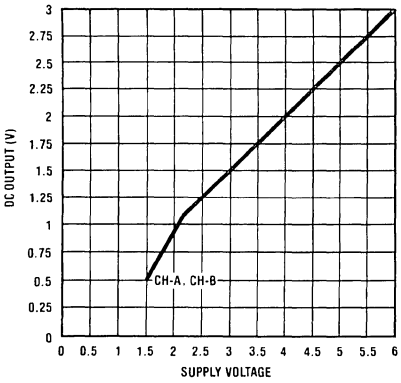
Supply Current vs Temperature



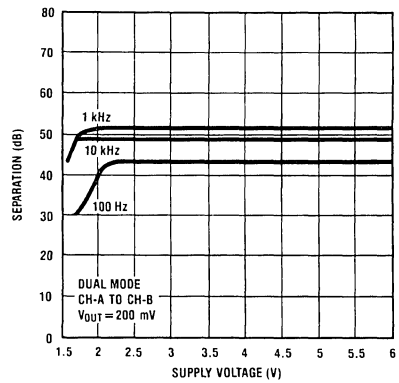
PSRR vs Supply Voltage



DC Output vs Supply Voltage



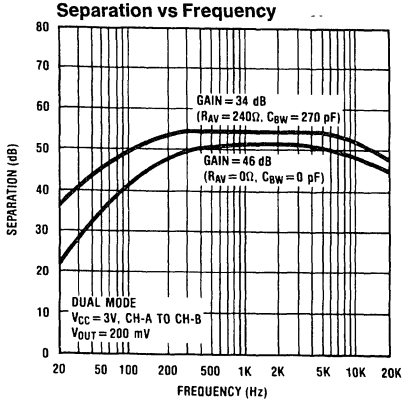
Separation vs Supply Voltage



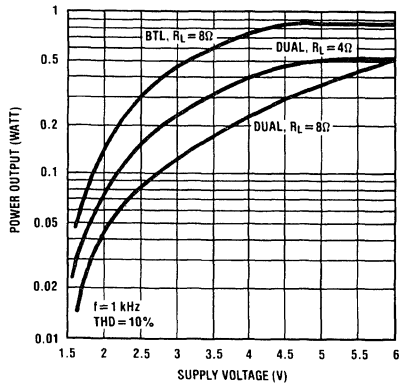
TL/H/6754–4

Typical Performance Characteristics (Continued)

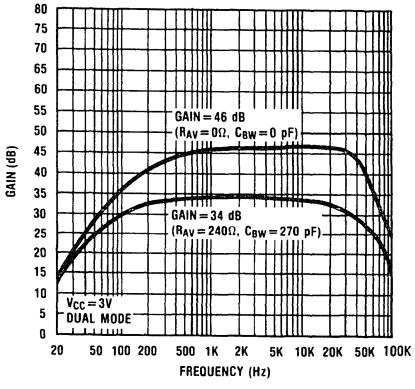
Separation vs Frequency



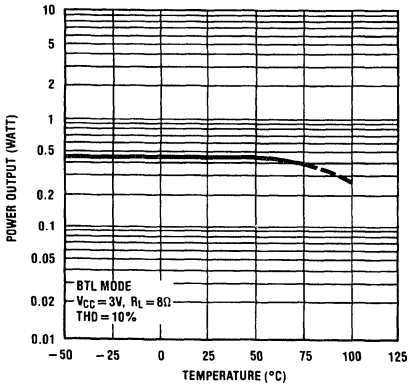
Power Output vs Supply Voltage



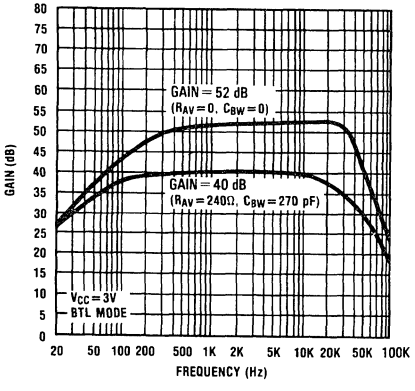
Gain vs Frequency



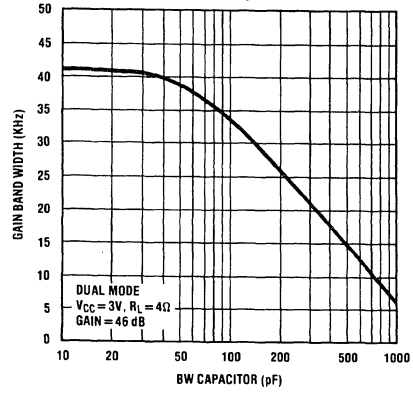
Power Output vs Temperature



Gain vs Frequency



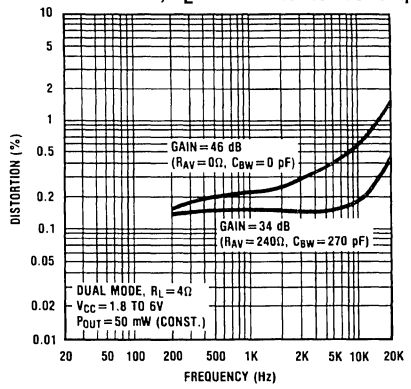
Bandwidth vs BW Capacitance



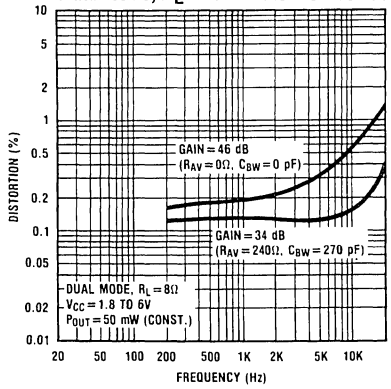
TL/H/6754–5

Typical Performance Characteristics (Continued)

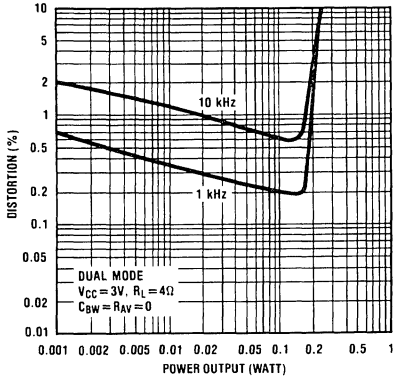
Dual Mode, R_L = 4Ω Distortion vs Frequency



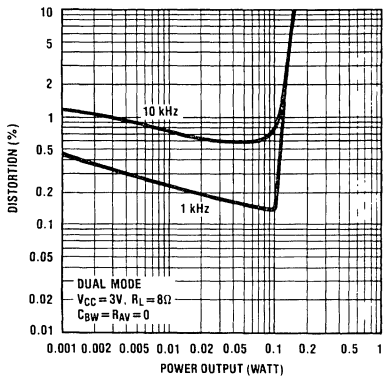
Dual Mode, R_L = 8Ω Distortion vs Frequency



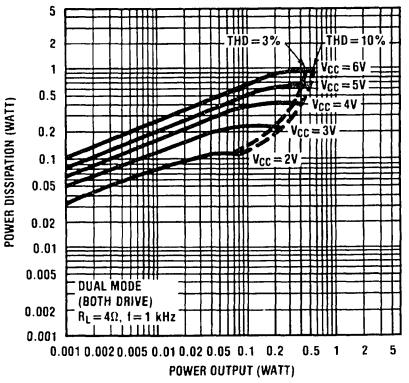
Distortion vs Power Output (Note 2)



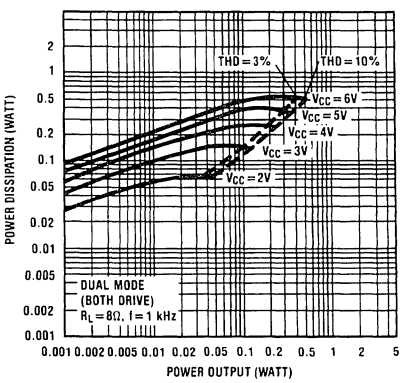
Distortion vs Power Output (Note 2)



Power Dissipation vs Power Output



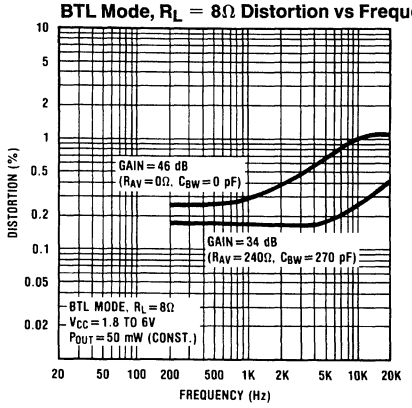
Power Dissipation vs Power Output



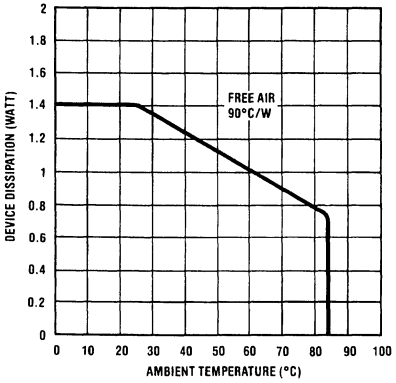
TL/H/6754–6

Typical Performance Characteristics (Continued)

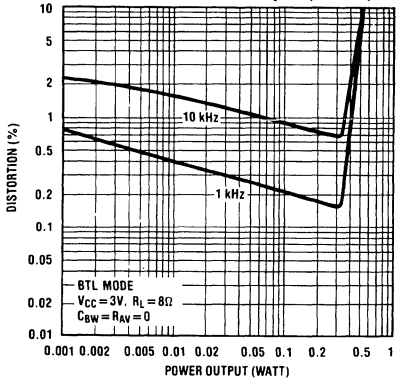
BTL Mode, $R_L = 8\Omega$ Distortion vs Frequency



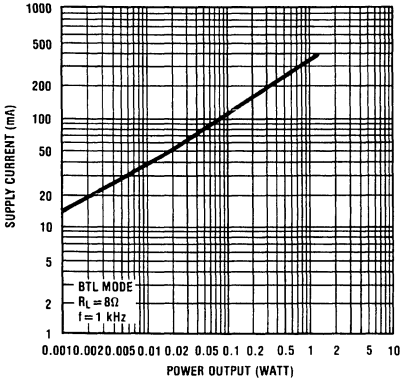
Device Dissipation vs Ambient Temperature



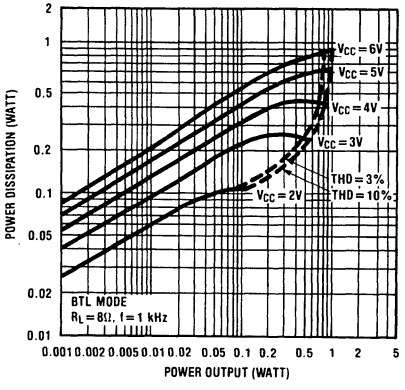
Distortion vs Power Output (Note 2)



Supply Current vs Power Output



Power Dissipation vs Power Output

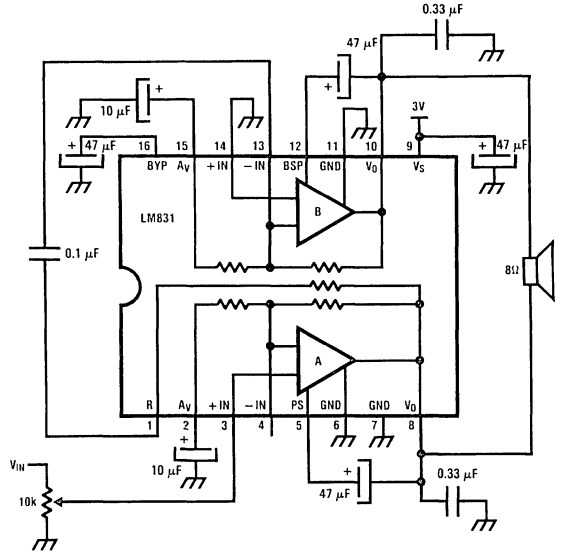


Note 2: 1 kHz curve is measured with 400 Hz–30 kHz Filter.

TL/H/6754–7

Typical Applications

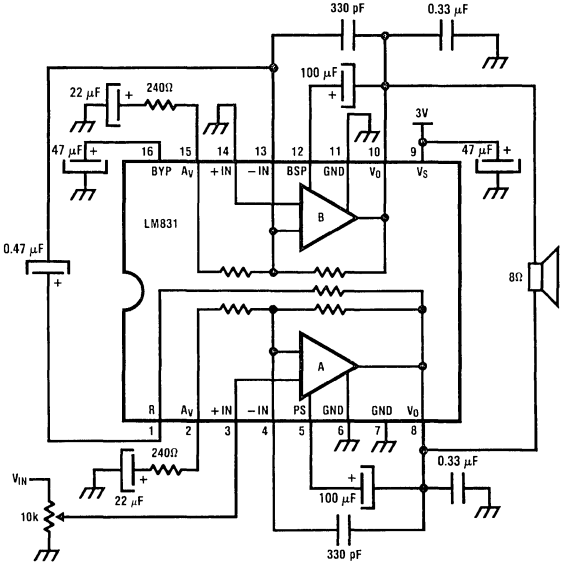
BTL Amplifier with Minimum Parts



TL/H/6754–8

A_V = 52 dB, BW = 250 Hz to 25 kHz
P_{OUT} = 440 mW, R_L = 8Ω

BTL Amplifier for Hi-Fi Quality

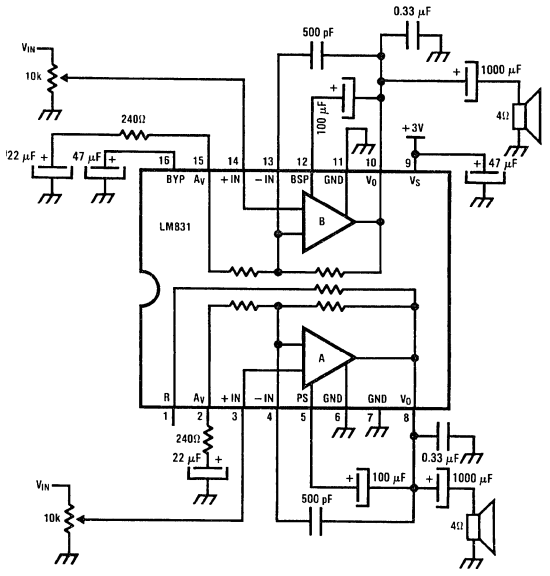


TL/H/6754–9

A_V = 40 dB, BW = 20 Hz to 20 kHz
P_{OUT} = 440 mW, R_L = 8Ω
(Dynamic Range Over 80 dB)

Typical Applications (Continued)

Dual Amplifier for Hi-Fi Quality



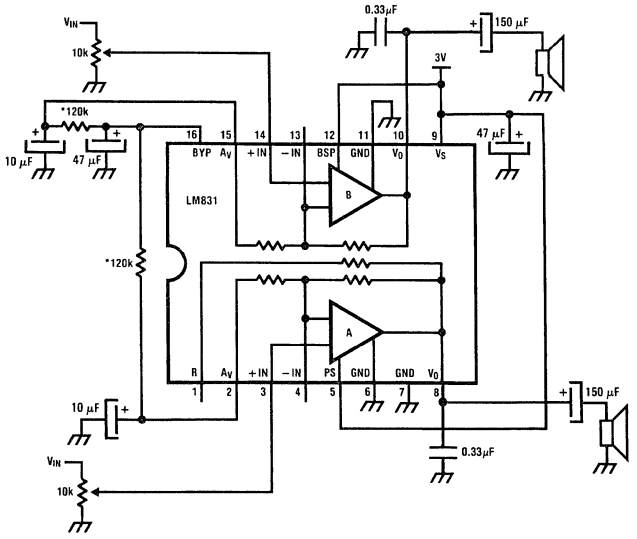
TL/H/6754–10

A_V = 34 dB, BW = 50 Hz to 20 kHz

P_{OUT} = 220 mW/Ch, R_L = 4Ω

(Dynamic Range Over 80 dB)

Low-Cost Power Amplifier (No Bootstrap)



TL/H/6754–11

P_{OUT} = 150 mW/Ch, BW = 300 Hz to 35 kHz

BTL Mode is also possible

*For 3-cell applications, the 120k resistor should be changed to 20K.

LM831 Circuit Description Refer to the external component diagram and equivalent schematic.

The power supply is applied to Pin 9 and is filtered by resistor R_1 and capacitor C_{BY} on Pin 16. This filtered voltage at Pin 16 is used to bias all of the LM831 circuits except the power output stage. Resistor R_0 generates a biasing current that sets the output DC voltage for optimum output power for any given supply voltage.

Feedback is provided to the input transistor Q_1 emitter by R_6 and R_7.

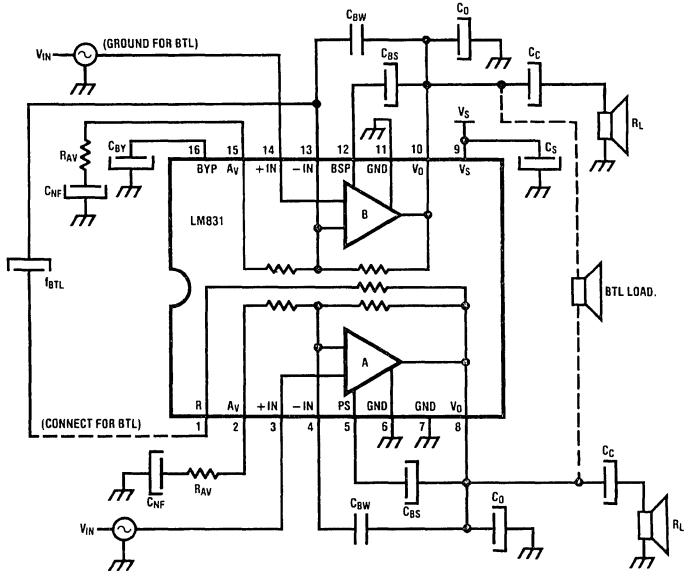
The capacitor C_{NF} on Pin 2 provides unity DC gain for maximum DC accuracy.

Q_2 provides voltage gain and the rest of the devices buffer the output load from Q_2's collector.

Bootstrapping of Pin 5 by C_{BS} allows maximum output swing and improved supply rejection.

R_5 is provided for bridge (BTL) operation.

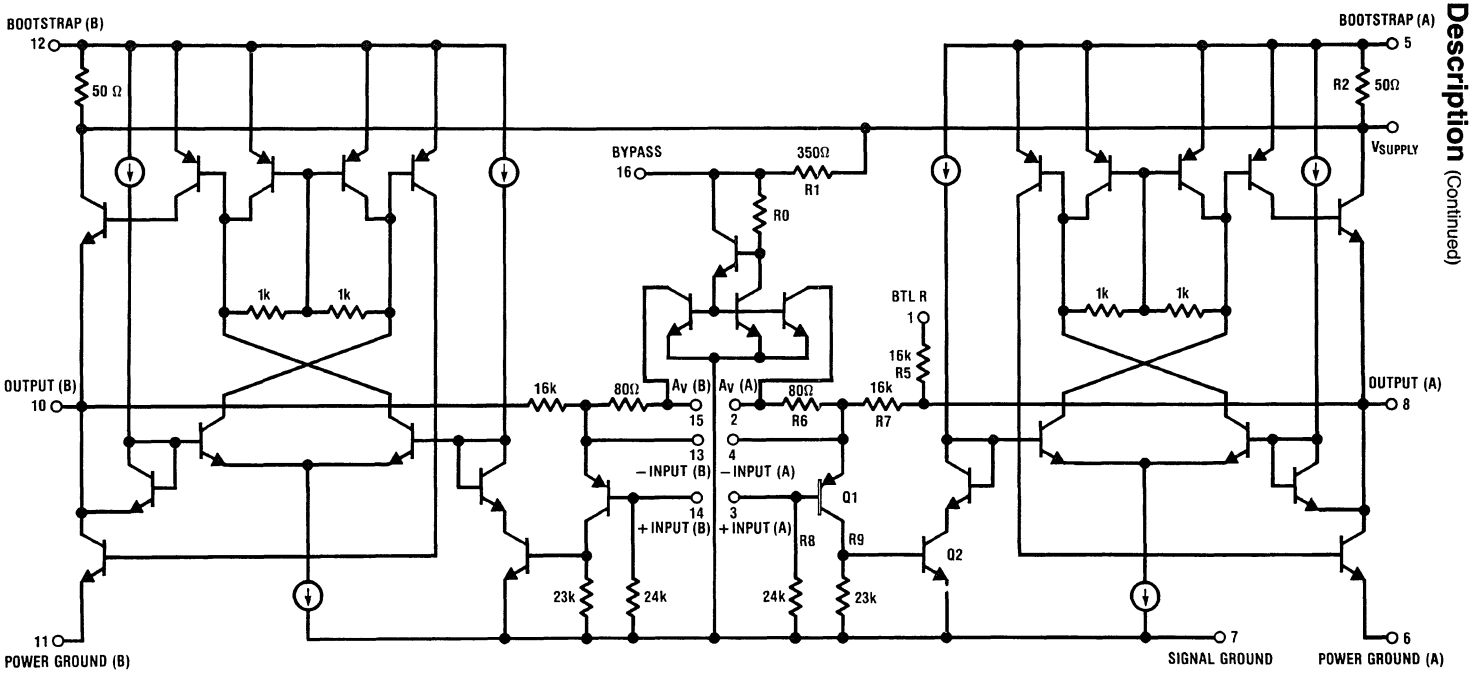
External Component Diagram



TL/H/6754–12

LM831 Circuit Description (Continued)

LM831 Equivalent Schematic



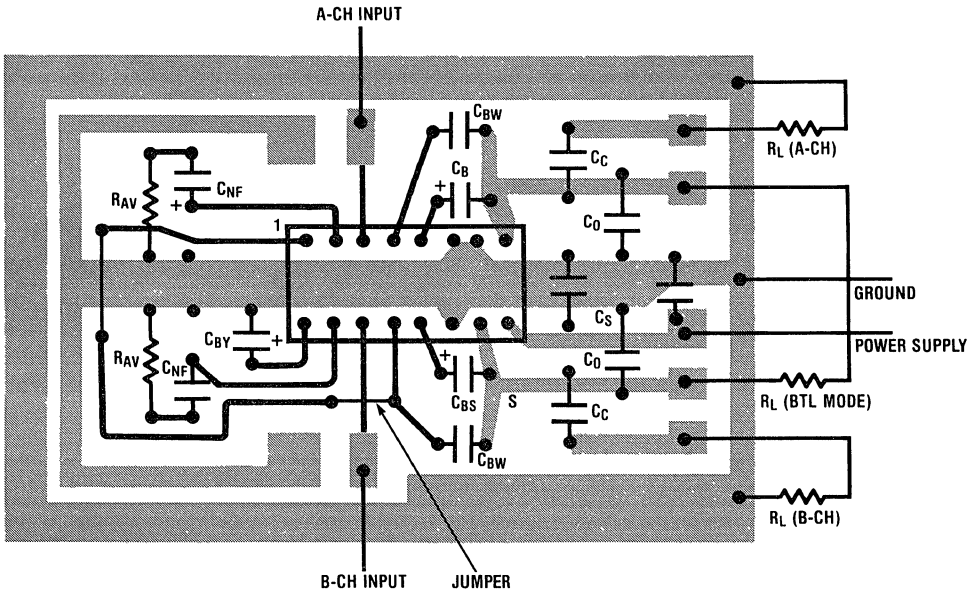
TL/H/6754–13

External Components (Refer to External Component Diagram)

Component	Comments	Min	Max
C_O	Required to stabilize output stage.	0.33 μF	1 μF
C_c	Output coupling capacitors for Dual Mode. Sets a low-frequency pole in the frequency response. $f_L = \frac{1}{2\pi C_c R_L}$	100 μF	10,000 μF
C_{BS}	Bootstrap capacitors. Sets a low-frequency pole in the power BW. Recommended value is $C_{BS} = \frac{1}{10 \bullet 2\pi \bullet f_L \bullet R_L}$	22 μF or (short Pins 4 & 12 to 9)	470 μF
C_S	Supply bypass. Larger values improve low-battery performance by reducing supply ripple.	47 μF	10,000 μF
C_{BY}	Filters the supply for improved low-voltage operation. Also sets turn-on delay.	47 μF	470 μF
C_{NF}	Sets a low-frequency response. Also affects turn-on delay. $f_L = \frac{1}{2\pi \bullet C_{NF} \bullet (R_{AV} + 80)}$ In BTL Mode, C_{NF} on Pin 15 can be reduced without affecting the frequency response. However, the turn-on "POP" will be worsened.	10 μF	100 μF
C_{BTL}	Used only in the Bridge Mode. Connects the output of the first amplifier to the inverting input of the other through an internal resistor. Sets a low-frequency pole in one-half the frequency response. $f_L = \frac{1}{2\pi \bullet C_{BTL} \bullet 16k}$	0.1 μF	1 μF
C_{BW}	Improves clipping waveform and sets the high-frequency bandwidth. Works with an internal 16k resistor. (This equation applies for $R_{AV} \neq 0$. For 46 dB application, see BW–C_{BW} curve.) $f_H = \frac{1}{2\pi \bullet C_{BW} \bullet 16k}$	See table below	
R_{AV}	Used to reduce the gain and improve the distortion and signal to noise. If this is desired, C_{BW} must also be used.	See table below	

Typical A_V	R_{AV}	C_{BW}	
		Min	Max
46 dB	Short	Open	4700 pF
40 dB	82	100 pF	4700 pF
34 dB	240	270 pF	4700 pF
28 dB	560	500 pF	4700 pF

Printed Circuit Layout for LM831N (Foil Side View) Refer to External Component Diagram



TL/H/6754–14

Note: Power ground pattern should be as wide as possible. Supply bypass capacitor should be as close to the IC as possible. Output compensation capacitors should also be close to the IC.

National Semiconductor Corporation

DNR® DYNAMIC NOISE REDUCTION SYSTEM

LM832 Dynamic Noise Reduction System DNR®

General Description

The LM832 is a stereo noise reduction circuit for use with audio playback systems. The DNR system is noncomplementary, meaning it does not require encoded source material. The system is compatible with virtually all prerecorded tapes and FM broadcasts. Psychoacoustic masking, and an adaptive bandwidth scheme allow the DNR to achieve 10 dB of noise reduction. DNR can save circuit board space and cost because of the few additional components required.

The LM832 is optimized for low voltage operation with input levels around 30 mVrms.

For higher input levels use the LM1894.

Features

- Low voltage battery operation
- Non-complementary noise reduction, "single ended"
- Low cost external components, no critical matching
- Compatible with all prerecorded tapes and FM
- 10 dB effective tape noise reduction CCIR/ARM weighted
- Wide supply range, 1.5V to 9V
- 150 mVrms input overload
- No royalty requirements
- Cascade connection for 17 dB noise reduction

Applications

- Headphone stereo
- Microcassette players
- Radio cassette players
- Automotive radio/tape players

Application Circuit

Order Number LM832M See NS Package M14A
Order Number LM832N See NS Package N14A

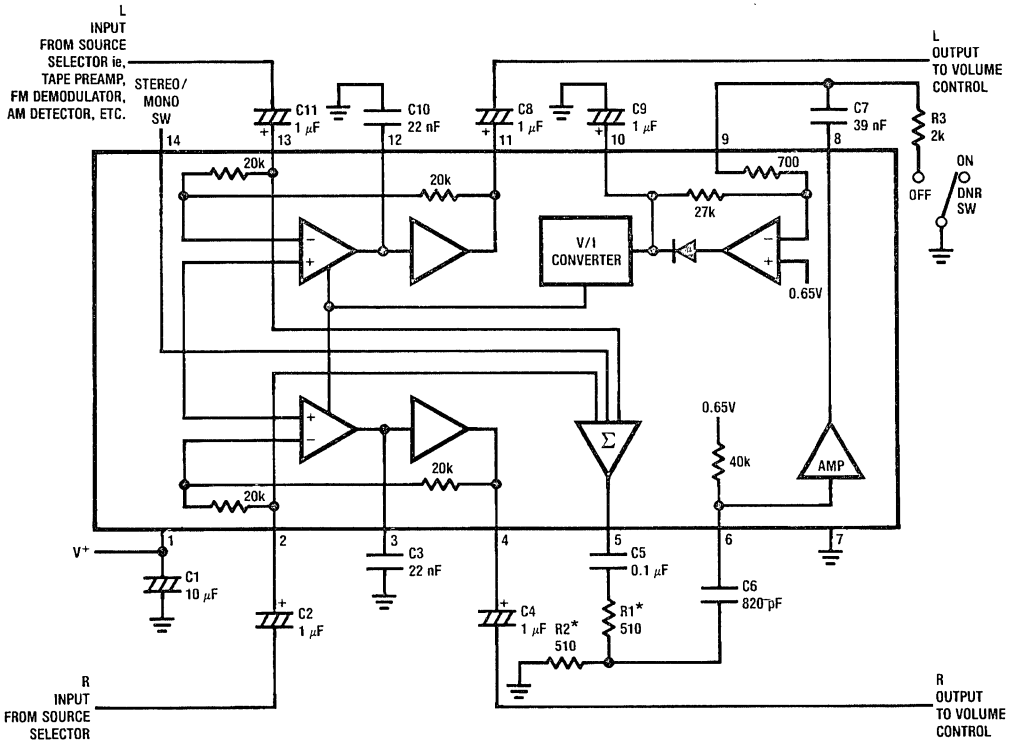


FIGURE 1. Component Hook-up for Stereo DNR System

TL/H/5176–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	10V
Power Dissipation (Note 1)	1.2W
Input Voltage	1.7 Vpp
Storage Temperature	−65 to +150°C
Operating Temperature (Note 1)	−40 to +85°

Soldering Information

- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effects on Products Reliability" for other methods of soldering surface mount devices."

DC Electrical Characteristics $T_A = 25°C$ $V_{CC} = 3.0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OP}	Operating Voltage	Supply Voltage for Normal Operation	1.5	3.0	9.0	V
$I_{CC}(1)$	Supply Current (1)	Pin 9 to GND 0.1 μF, BW = Min, Note 2		2.5	4.0	mA
$I_{CC}(2)$	Supply Current (2)	DC GND Pin 9 with 2k, BW = Max, Note 2		5.0	8.0	mA
$V_{IN}(1)$	Input Voltage (1)	Pin 2, Pin 13	0.20	0.36	0.5	V
$V_{IN}(2)$	Input Voltage (2)	Pin 6	0.50	0.65	0.8	V
$V_{IN}(3)$	Input Voltage (3)	Pin 9	0.50	0.65	0.8	V
$V_{OUT}(1)$	Output Voltage (1)	Pin 4, Pin 11	0.20	0.35	0.50	V
$V_{OUT}(2)$	Output Voltage (2)	Pin 5 Stereo Mode	0.15	0.28	0.40	V
$V_{OUT}(3)$	Output Voltage (3)	Pin 5 Monaural Mode, DC Ground Pin 14	0.10	0.20	0.30	V
$V_{OUT}(4)$	Output Voltage (4)	Pin 8	0.25	0.40	0.60	V
$V_{OUT}(5)$	Output Voltage (5)	Pin 10 BW = Max, Note 2	1.00	1.27	1.50	V
$V_{OUT}(6)$	Output Voltage (6)	Pin 10 BW = Min, Note 2	0.50	0.65	0.75	V
V_{OS}	Output DC Shift	Pin 4, PIN 11; Change BW Min to Max		1.0	3.0	mV

AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MAIN SIGNAL PATH (Note 3)						
A_V	Voltage Gain	V_{IN} = 30 mVrms, f = 1 kHz, BW = Max, Note 2	−1.0	0.0	+1.0	dB
C.B.	Channel Balance	V_{IN} = 30 mVrms, f = 1 kHz, BW = Max, Note 2	−1.0	0	+1.0	dB
f_{MIN}	Min Bandwidth	0.1 μF between Pin 9 - GND	600	1000	1500	Hz
f_{MAX}	Max Bandwidth	DC Ground Pin 9 with 2k	24	30	46	kHz
THD	Distortion	V_{IN} = 30 mVrms, f = 1 kHz, BW = Max, Note 2		0.07	0.5	%
MV_{IN}	Max Input Voltage	THD = 3%, f = 1 kHz, BW = Max Note 2	120	150		mVrms
S/N	Signal to Noise	REF = 30 mVrms, BW = Max, CCIR/ARM	60	68		dB
Z_{IN}	Input Impedance	Pin 2, Pin 13	14	20	26	kΩ
C.S.	Channel Separation	Ref = 30 mVrms, f = 1 kHz, BW = Max, Note 2	40	68		dB
P_{SRR}	P_{SRR}	V_{RIPPLE} = 50 mVrms, f = 100 Hz	40	55		dB
CONTROL PATH						
$A_V$sum(1)	Summing Amp Gain (1)	V_{IN} = 30 mVrms at R and L, f = 1 kHz	−3.0	−1.5	0.0	dB
$A_V$sum(2)	Summing Amp Gain (2)	DC Ground Pin 14, f = 1 kHz	−9.0	−6.0	−3.0	dB
A_V 1st	Gain Amp Gain	Pin 6 to Pin 8	25	30	35	dB
Z_{IN} 1st	Input Impedance	Pin 6	28	40	52	kΩ
A_{VPKD}	Peak Detector Gain	AC In, DC Out; Pin 9 to Pin 10	25	30	35	V/V
Z_{INPKD}	Input Impedance	Pin 9	500	800	1100	Ω
V_{RPKD}	Output DC Change	Pin 10, Change BW Min to Max	0.5	0.62	0.8	V

Note 1: For operation in ambient temperature above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance junction to ambient, as follows: LM832N −90° c/w, LM832M-115° c/w.

Note 2: To force the DNR system into maximum bandwidth, connect a 2k resistor from pin 9 to GND. AC ground pin 9 or pin 6 to select minimum bandwidth. To change minimum and maximum bandwidth, see Application Hints.

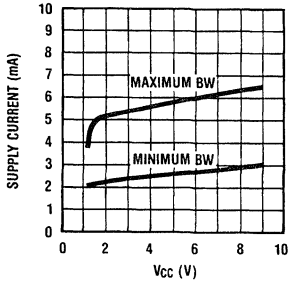
Note 3: The maximum noise reduction CCIR/ARM weighted is about 14 dB. This is accomplished by changing the bandwidth from maximum to minimum. In actual operation, minimum bandwidth is not selected, a nominal minimum bandwidth of about 2 kHz gives 10 dB of noise reduction. See Application Hints.

External Component Guide (See *Figure 1*)

P/N	Recommended Value	Purpose	Effect		Remarks
			Smaller	Larger	
C1	10 μF	Power supply decoupling	Poor supply rejection	Better supply rejection	Do not use less than 10 μF
C2,C11	1 μF	Input coupling capacitor	Increases frequency of low-frequency roll-off	Reduces frequency of low-frequency roll-off	DC voltage at pin 2 and pin 13 is 0.35V $f=\frac{1}{2\pi C_2 R_{IN}}$
C3,C10	22 nF for Stereo, 15 nF for mono	Establishment of Min and Max Bandwidth	Bandwidth becomes wider	Bandwidth becomes narrower	See Note 4
C4,C8	1 μF	Output coupling capacitor	Increases frequency of low-frequency roll-off	Reduces frequency of low-frequency roll-off	DC voltage at pin 4 and pin 11 is 0.35V $f=\frac{1}{2\pi C_4 R_{LOAD}}$
C5	0.1 μF	Works with R1 and R2 to set one of the low-frequency corners in control path	Some high frequency program material may be attenuated	Bandwidth may increase due to low-frequency inputs, causing "Breathing"	$f=\frac{1}{2\pi C_5(R1+R2)}=1.6$ kHz See Note 4
C6	820 pF	Works with input resistance of pin 6 to set one of the low-frequency corners in the control path	Same as above	Same as above	$f=\frac{1}{2\pi C_6 R_{PIN6}}=4.8$ kHz See Note 4
C7	39 nF	Works with input resistance of pin 9 to form part of control path frequency weighing	Same as above	Same as above	$f=\frac{1}{2\pi C_7 R_{PIN7}}=4.8$ kHz See Note 4
C9	1 μF	Sets attack time	Reduces attack and decay time	Increases attack and decay time	See Note 4
R1,R2	$R_1+R_2=1$ kΩ	This voltage divider sets control path sensitivity	—	—	Sensitivity should be set for maximum noise reduction and minimum audible frequency program effect on high
R3	•2 kΩ	Sets gain amp load when DNR is OFF	Loads gain amp output, may cause distortion	Max bandwidth will be reduced	

Note 4: The values of the control path filter components (C5, C6, C7, C9, R1, R2) and the integrating capacitors (C3, C10) should not be changed from the recommended values unless the characteristics of the noise or program material differ substantially from that of FM or tape sources. Failure to use the correct values may result in degraded performance, and therefore the application may not be approved for DNR trademark usage. Please contact National Semiconductor for more information and technical assistance.

Typical Performance Characteristics



TL/H/5176–2

FIGURE 2. Supply current vs supply voltage

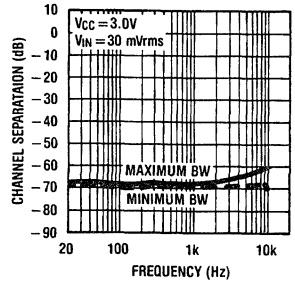


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FIGURE 3. Channel separation vs frequency

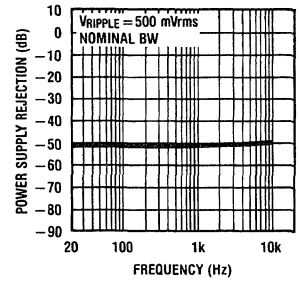

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FIGURE 4. Power supply rejection ratio vs frequency

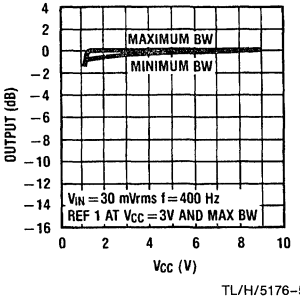

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FIGURE 5. Output level change vs supply voltage

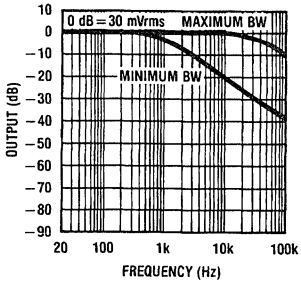

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FIGURE 6. Output level vs frequency

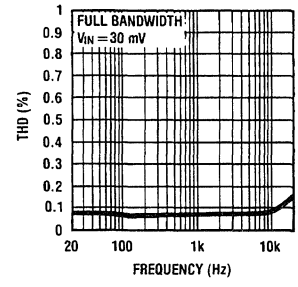

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FIGURE 7. THD vs frequency

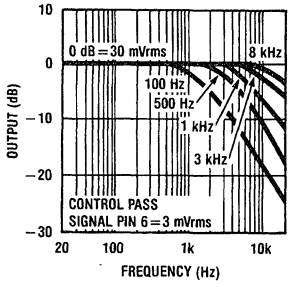

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FIGURE 8. Output vs frequency and control path signal

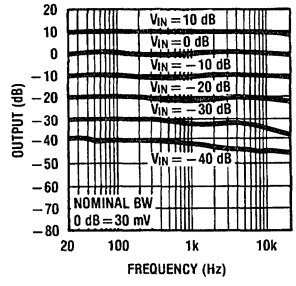

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FIGURE 9. Frequency response for various input levels

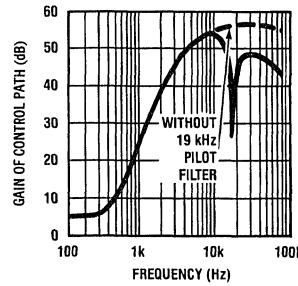

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FIGURE 10. Gain of control path vs frequency

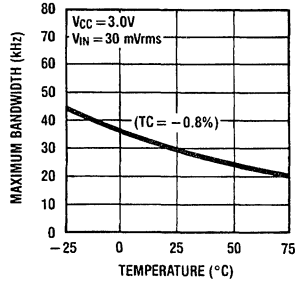

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FIGURE 11. Change in main signal path maximum bandwidth vs temperature

Circuit Operation

The LM832 has two signal paths, a main signal path and a bandwidth control path. The main path is an audio low pass filter comprised of a g_m block with a variable current, and a unity gain buffer. As seen in *Figure 1*, DC feedback constrains the low frequency gain to $A_v = -1$. Above the cutoff frequency of the filter, the output decreases at −6 dB/oct due to the action of the 0.022 μF capacitor.

The purpose of the control path is to generate a bandwidth control signal which replicates the ear's sensitivity to noise in the presence of a tone. A single control path is used for both channels to keep the stereo image from wandering. This is done by adding the right and left channels together in the summing amplifier of *Figure 1*. The R1, R2 resistor divider adjusts the incoming noise level to slightly open the bandwidth of the low pass filter. Control path gain is about 60dB and is set by the gain amplifier and peak detector gain. This large gain is needed to ensure the low pass filter bandwidth can be opened by very low noise floors. The capacitors between the summing amplifier output and the peak detector input determine the frequency weighting as shown in the typical performance curves. The 1 μF capacitor at pin 10, in conjunction with internal resistors, sets the attack and decay times. The voltage is converted into a proportional current which is fed into the g_m blocks. The bandwidth sensitivity to g_m current is 70 Hz/μA. In FM stereo applications a 19 kHz pilot filter is inserted between pin 8 and pin 9 as shown in *Figure 16*.

Normal methods of evaluating the frequency response of the LM 832 can be misleading if the input signal is also applied to the control path. Since the control path includes a frequency weighting network, a constant amplitude but varying frequency input signal will change the audio signal path bandwidth in a non-linear fashion. Measurements of the audio signal path frequency response will therefore be in error since the bandwidth will be changing during the measurement. See *Figure 9* for an example of the misleading results that can be obtained from this measurement approach. Although the frequency response is always flat below a single high-frequency pole, the lower curves do not resemble single pole responses at all.

A more accurate evaluation of the frequency response can be seen in *Figure 8*. In this case the main signal path is frequency swept while, the control path has a constant frequency applied. It can be seen that different control path frequencies each give a distinctive gain roll-off.

PSYCHOACOUSTIC BASICS

The dynamic noise reduction system is a low pass filter that has a variable bandwidth of 1 kHz to 30 kHz, dependent on music spectrum. The DNR system operates on three principles of psychoacoustics.

1. Music and speech can mask noise. In the absence of source material, background noise can be very audible. However, when music or speech is present, the human ear is less able to distinguish the noise—the source material is said to mask the noise. The degree of masking is dependent on the amplitude and spectral content (frequencies) of the source material, but in general multiple tones around 1 kHz are capable of providing excellent masking of noise over a very wide frequency range.

2. The ear cannot detect distortion for less than 1 ms. On a transient basis, if distortion occurs in less than 1 ms, the ear acts as an integrator and is unable to detect it. Because of this, signals of sufficient energy to mask noise open the bandwidth to 90% of the maximum value in less than 1 ms. Reducing the bandwidth to within 10% of its minimum value is done in about 60 ms: long enough to allow the ambience of the music to pass through, but not so long as to allow the noise floor to become audible.

3. Reducing the audio bandwidth reduces the audibility of noise. Audibility of noise is dependent on noise spectrum, or how the noise energy is distributed with frequency. Depending on the tape and the recorder equalization, tape noise spectrum may be slightly rolled off with frequency on a per octave basis. The ear sensitivity on the other hand greatly increases between 2 kHz and 10 kHz. Noise in this region is extremely audible. The DNR system low pass filters this noise. Low frequency music will not appreciably open the DNR bandwidth, thus 2 kHz to 20 kHz noise is not heard.

Application Hints

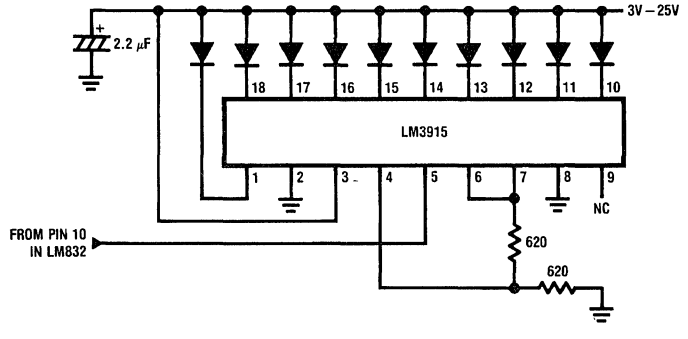
The DNR system should always be placed before tone and volume controls as shown in *Figure 1*. This is because any adjustment of these controls would alter the noise floor seen by the DNR control path. The sensitivity resistors R1 and R2 may need to be switched with the input selector, depending on the noise floors of different sources, i.e., tape, FM, phono. To determine the value of R1 and R2 in a tape system for instance; apply tape noise (no program material) and adjust the ratio of R1 and R2 to slightly open the bandwidth of the main signal path. This can easily be done by viewing the capacitor voltage of pin 10 with an oscilloscope, or by using the circuit of *Figure 12*. This circuit gives an LED display of the voltage on the peak detector capacitor. Adjust the values of R1 and R2 (their sum is always 1 kΩ) to light the LEDs of pin 1 and pin 18. The LED bar graph does not indicate signal level, but rather instantaneous bandwidth of the two filters; it should not be used as a signal-level indicator. For greater flexibility in setting the bandwidth sensitivity, R1 and R2 could be replaced by a 1 kΩ potentiometer.

To change the minimum and maximum value of bandwidth, the integrating capacitors, C3 and C10, can be scaled up or down. Since the bandwidth is inversely proportional to the capacitance, changing this 0.022 μF capacitor to 0.015 μF will change the typical bandwidth from 1 kHz–30 kHz to 1.5 kHz–44 kHz. With C3 and C10 set at 0.022 μF, the maximum bandwidth is typically 30 kHz. A double pole double throw switch can be used to completely bypass DNR.

The capacitor on pin 10 in conjunction with internal resistors sets the attack and decay times. The attack time can be altered by changing the size of C9. Decay times can be decreased by paralleling a resistor with C9, and increased by increasing the value of C9.

When measuring the amount of noise reduction of DNR in a cassette tape system, the frequency response of the cassette should be flat to 10 kHz. The CCIR weighting network has substantial gain to 8 kHz and any additional roll-off in the cassette player will reduce the benefits of DNR noise reduction. A typical signal-to-noise measurement circuit is shown in *Figure 13*. The DNR system should be switched from maximum bandwidth to nominal bandwidth with tape noise as a signal source. The reduction in measured noise is the signal-to-noise ratio improvement.

Application Hints (Continued)



TL/H/5176–12

FIGURE 12. Bar Graph Display of Peak Detector Voltage

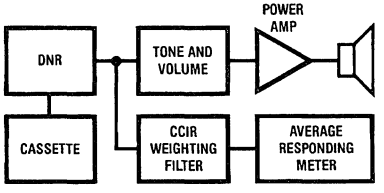


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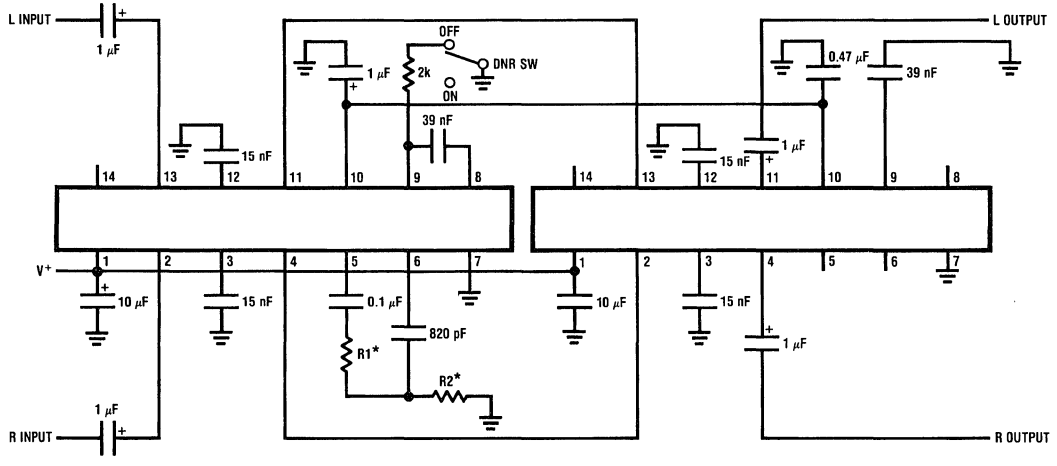
FIGURE 13. Technique for Measuring S/N Improvement of the DNR System

CASCADE CONNECTION

Additional noise reduction can be obtained by cascading the DNR filters. With two filters cascaded the rolloff is 12 dB per octave. For proper operating bandwidth the capacitors on pin 3 and 12 are changed to 15 nF. The resulting noise reduction is about 17 dB.

Figure 15 shows the monaural cascade connection. Note that pin 14 is grounded so only the pin 2 input is fed to the summing amp and therefore the control path.

Figure 14 shows the stereo cascade connection. Note that pin 14 is open circuit as in normal stereo operation.

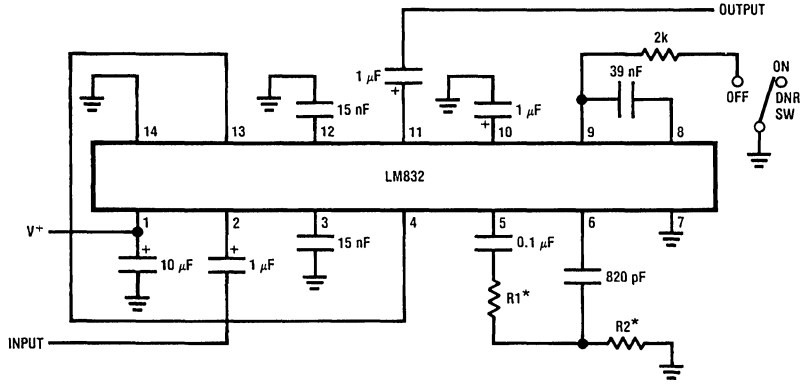


*R1 + R2 = 1 kΩ (refer to application hints)

TL/H/5176–14

FIGURE 14. Stereo Cascade Connection

Application Hints (Continued)



*R1 + R2 = 1 kΩ (refer to application hints)

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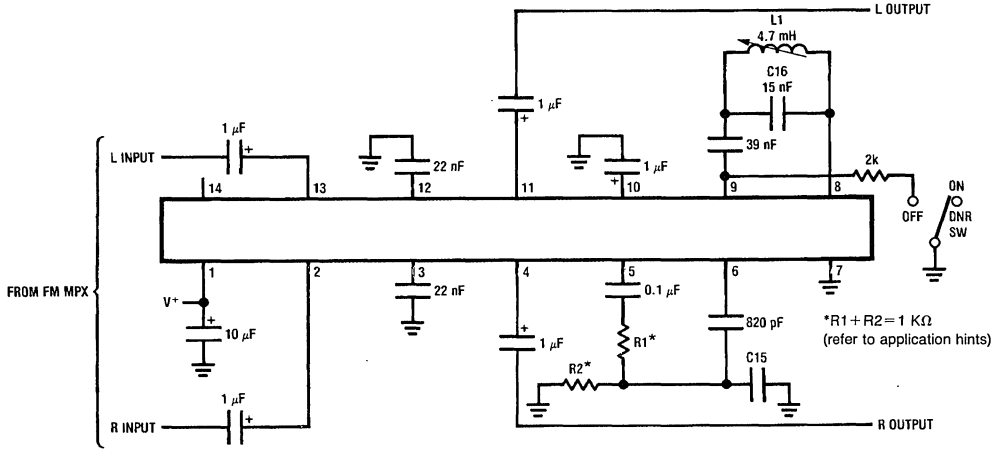
FIGURE 15. Monaural Cascade Connection

FM STEREO

When using the DNR system with FM stereo as the audio source, it is important to eliminate the ultrasonic frequencies that accompany the audio. If the radio has a multiplex filter to remove the ultrasonics there will be no problem.

This filtering can be done at the output of the demodulator, before the DNR system, or in the DNR system control path.

Standard audio multiplex filters are available for use at the output of the demodulator from several filter companies. *Figure 16* shows the additional components L1, C15 and C16 that are added to the control path for FM stereo applications. The coil must be tuned to 19 kHz, the FM pilot frequency.



TL/H/5176–16

FIGURE 16. FM Stereo Application

FOR FURTHER READING

Tape Noise Levels

1. "A Wide Range Dynamic Noise Reduction System" Blackmer, 'dB' Magazine, August-September 1972, Volume 6, #8.

2. "Dolby B-Type Noise Reduction System", Berkowitz and Gundry, Sert Journal, May-June 1974, Volume 8.

3. "Cassette vs Elcaset vs Open Reel", Toole, Audioscene Canada, April 1978.

4. "CCIR/ARM: A Practical Noise Measurement Method", Dolby, Robinson, Gundry, JAES, 1978.

Noise Masking

1. "Masking and Discrimination", Bos and De Boer, JAES, Volume 39, #4, 1966.

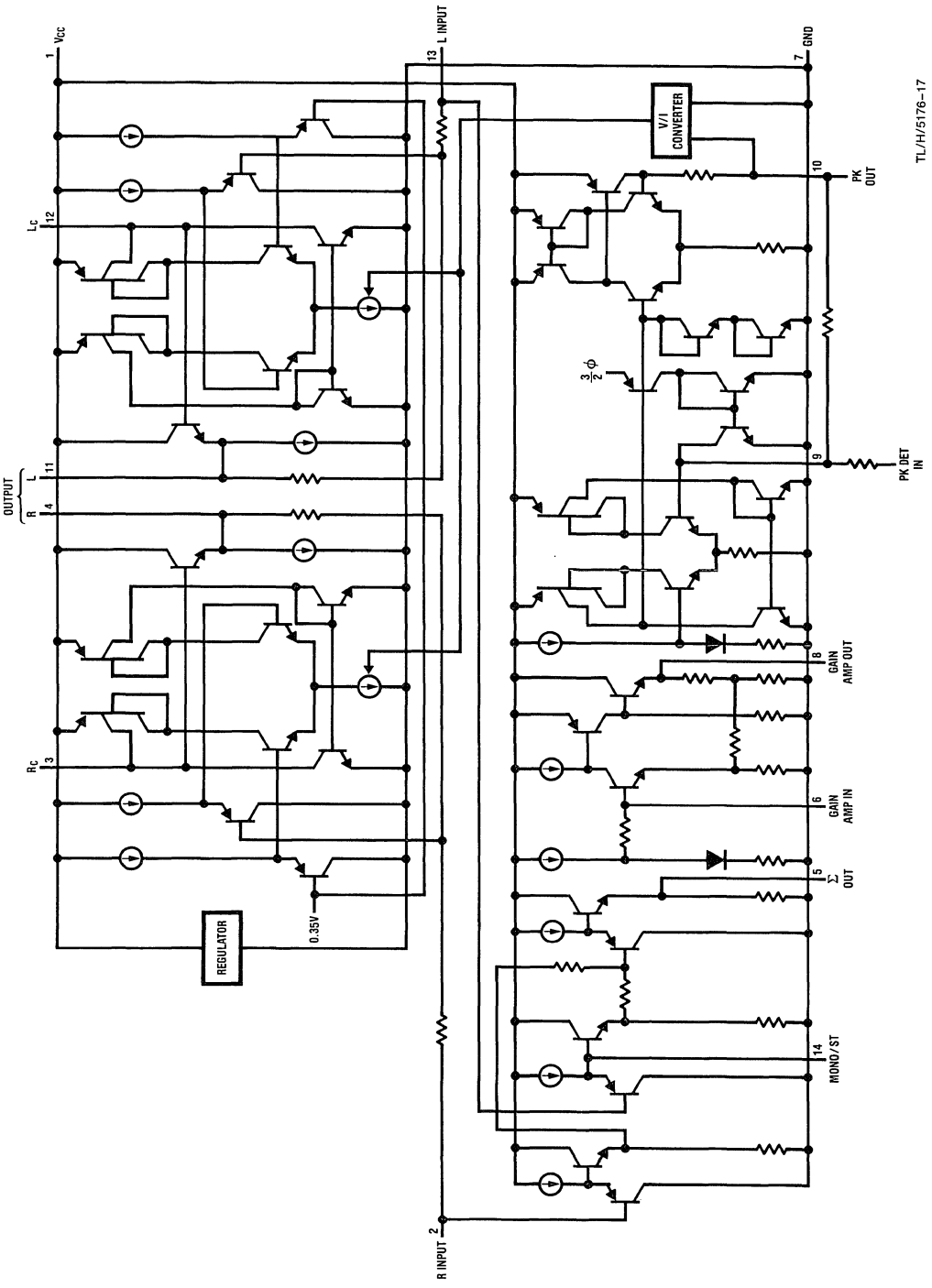
2. "The Masking of Pure Tones and Speech by White Noise", Hawkins and Stevens, JAES, Volume 22, #1, 1950.

3. "Sound System Engineering", Davis, Howard W. Sams and Co.

4. "High Quality Sound Reproduction", Moir, Chapman Hall, 1960.

5. "Speech and Hearing in Communication", Fletcher, Van Nostrand, 1953.

LM832 Simple Circuit Schematic



National Semiconductor Corporation

LM1035/LM1036 Dual DC Operated Tone/Volume/Balance Circuits

General Description

The LM1035/LM1036 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

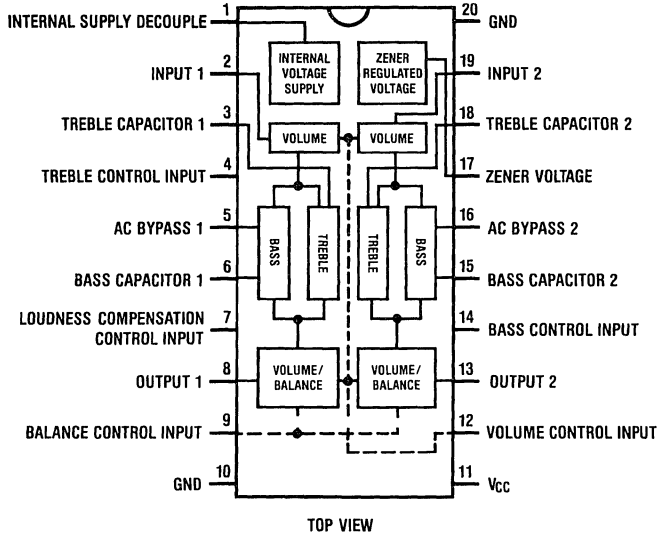
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 8V to 18V
- Large volume control range, 75 dB typical
- Tone control, ±15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 1 Vrms (0.3 Vrms for LM1036)
- High signal to noise, 80 dB typical for an input level of 1 Vrms (0.3 Vrms for LM1036)
- Few external components required

Block and Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5142–1

Order Number LM1035N or LM1036N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage
- LM1036 16V
- LM1035 20V

Control Pin Voltage (Pins 4, 7, 9, 12, 14) V_{CC}

Operating Temperature Range 0°C to +70°C
Storage Temperature Range −65°C to +150°C
Power Dissipation 1W
Lead Temp. (Soldering, 10 seconds) 260°C

Electrical Characteristics $V_{CC}=12V$, $T_A=25°C$ (unless otherwise stated)

Parameter	Conditions		Min	Typ	Max	Units
Supply Voltage Range	Pin 11	LM1036	9		16	V
		LM1035	8		18	V
Supply Current				35	45	mA
Zener Regulated Output	Pin 17					
Voltage				5.4		V
Current					5	mA
Maximum Output Voltage	Pins 8, 13; f = 1 kHz					
LM1036	$V_{CC}=9V$, Maximum Gain			0.8		Vrms
	$V_{CC}=12V$		0.8	1.0		Vrms
Maximum Output Voltage	Pins 8, 13; f = 1 kHz					
LM1035	$V_{CC}=8V$			1.3		Vrms
	$V_{CC}=12V$		2	2.5		Vrms
	$V_{CC}=18V$			3.5		Vrms
Maximum Input Voltage	Pins 2, 19; f = 1 kHz, $V_{CC}=9V$			1.1		Vrms
LM1036 (Note 1)	Flat Response, $V_{CC}=12V$		1.3	1.6		Vrms
	Gain = −10 dB					
Maximum Input Voltage	Pins 2, 19; f = 1 kHz		2	2.5		Vrms
LM1035 (Note 1)	Flat Response					
Input Resistance	Pins 2, 19; f = 1 kHz		20	30		kΩ
Output Resistance	Pins 8, 13; f = 1 kHz			20		Ω
Maximum Gain	V(Pin 12) = V(Pin 17); f = 1 kHz		−2	0	2	dB
Volume Control Range	f = 1 kHz	LM1036	70	75		dB
		LM1035	70	80		dB
Gain Tracking	f = 1 kHz					
Channel 1–Channel 2	0 dB through −40 dB			1	3	dB
	−40 dB through −60 dB			2		dB
Balance Control Range	Pins 8, 13; f = 1 kHz			1		dB
				−26	−20	dB
Bass Control Range	f = 40 Hz, $C_b=0.39\ \mu F$					
(Note 2)	V(Pin 14) = V(Pin 17)		12	15	18	dB
	V(Pin 14) = 0V		−12	−15	−18	dB
Treble Control Range	f = 16 kHz, $C_t=0.01\ \mu F$					
(Note 2)	V(Pin 4) = V(Pin 17)		12	15	18	dB
	V(Pin 4) = 0V		−12	−15	−18	dB
Total Harmonic Distortion	f = 1 kHz, $V_{IN}=0.3$ Vrms					
LM1036	Gain = 0 dB			0.06	0.3	%
	Gain = −30 dB			0.03		%
Total Harmonic Distortion	f = 1 kHz, $V_{IN}=1$ Vrms			0.05	0.2	%
LM1035	Maximum Gain					

Electrical Characteristics $V_{CC}=12V$, $T_A=25°C$ (unless otherwise stated) (Continued)

Parameter	Conditions		Min	Typ	Max	Units
Channel Separation	f = 1 kHz, Maximum Gain	LM1036	60	75		dB
		LM1035		75		dB
Signal/Noise Ratio LM1036	Unweighted 100 Hz–20 kHz Maximum Gain, 0 dB = 0.3 Vrms CCIR/ARM (Note 3)			80		dB
	Gain = 0 dB, V_{IN} = 0.3 Vrms		75	79		dB
	Gain = −20 dB, V_{IN} = 1.0 Vrms			72		dB
Signal/Noise Ratio LM1035	Unweighted 100 Hz–20 kHz Maximum Gain, 0 dB = 1 Vrms CCIR/ARM (Note 3)			80		dB
	Gain = 0 dB		76	80		dB
	Gain = −20 dB			64		dB
Output Noise Voltage at Minimum Gain	CCIR/ARM (Note 3)	LM1036		10	16	μV
		LM1035		25	35	μV
Supply Ripple Rejection	200 mVrms, 1 kHz Ripple	LM1036	35	50		dB
		LM1035		40		dB
Control Input Currents	Pins 4, 7, 9, 12, 14 (V = 0V)			−0.6	−2.5	μA
Frequency Response	−1 dB (Flat Response 20 Hz–16 kHz)			250		kHz

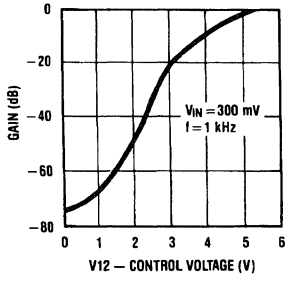
Note 1: The maximum permissible input level is dependent on tone and volume settings. See Application Notes.

Note 2: The tone control range is defined by capacitors C_b and C_t. See Application Notes.

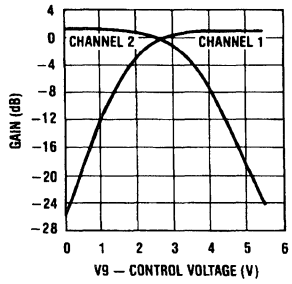
Note 3: Gaussian noise, measured over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz and an average-responding meter.

Typical Performance Characteristics

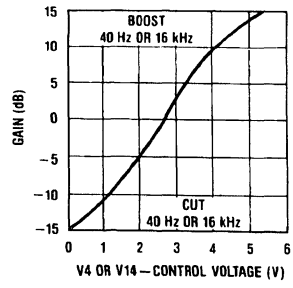
Volume Control Characteristics



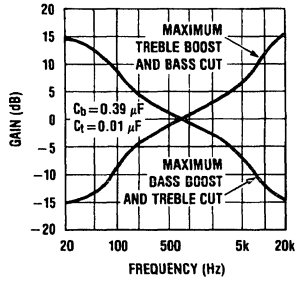
Balance Control Characteristic



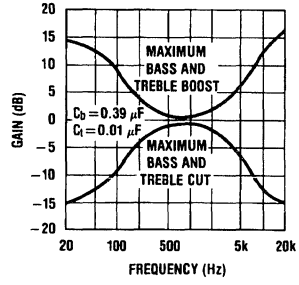
Tone Control Characteristic



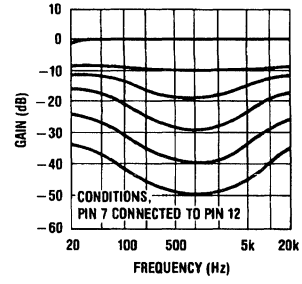
Tone Characteristic (Gain vs Frequency)



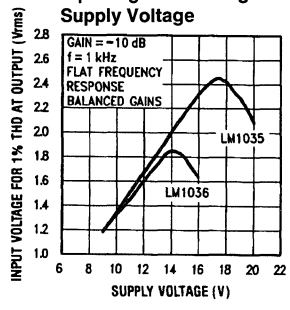
Tone Characteristic (Gain vs Frequency)



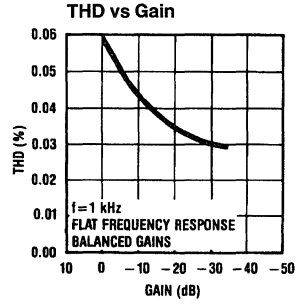
Loudness Compensated Volume Characteristic



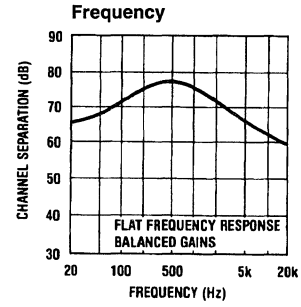
Input Signal Handling vs Supply Voltage



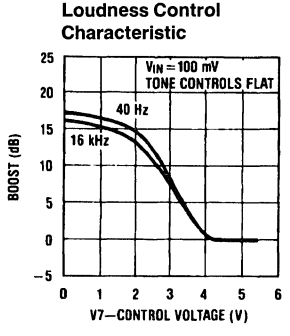
THD vs Gain



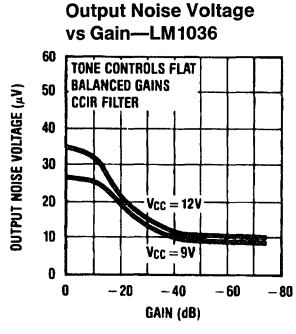
Channel Separation vs Frequency



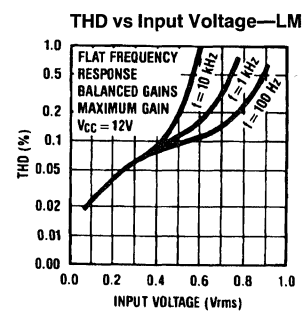
Loudness Control Characteristic



Output Noise Voltage vs Gain—LM1036



THD vs Input Voltage—LM1036



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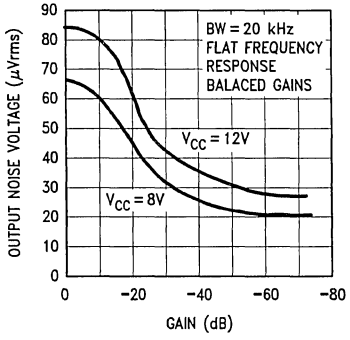
Typical Performance Characteristics (Continued)

Output Noise Voltage vs Gain—LM1035



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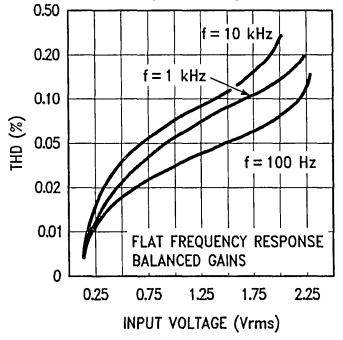
THD vs Input Voltage—LM1035



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Application Notes

TONE RESPONSE

The maximum boost and cut can be optimized for individual applications by selection of the appropriate values of C_t (treble) and C_b (bass).

The tone responses are defined by the relationships:

$$\text{Bass Response} = \frac{1+\frac{0.00065(1-a_b)}{j\omega C_b}}{1+\frac{0.00065a_b}{j\omega C_b}}$$

$$\text{Treble Response} = \frac{1+j\omega 5500(1-a_t)C_t}{1+j\omega 5500a_tC_t}$$

Where $a_b = a_t = 0$ for maximum bass and treble boost respectively and $a_b = a_t = 1$ for maximum cut.

For the values of C_b and C_t of 0.39 μF and 0.01 μF as shown in the Application Circuit, 15 dB of boost or cut is obtained at 40 Hz and 16 kHz.

ZENER VOLTAGE

A zener voltage (pin 17 = 5.4V) is provided which may be used to bias the control potentiometers. Setting a DC level of one half of the zener voltage on the control inputs, pins 4, 9, and 14, results in the balanced gain and flat response condition. Typical spread on the zener voltage is ±100 mV and this must be taken into account if control signals are used which are not referenced to the zener voltage. If this is the case, then they will need to be derived with similar accuracy.

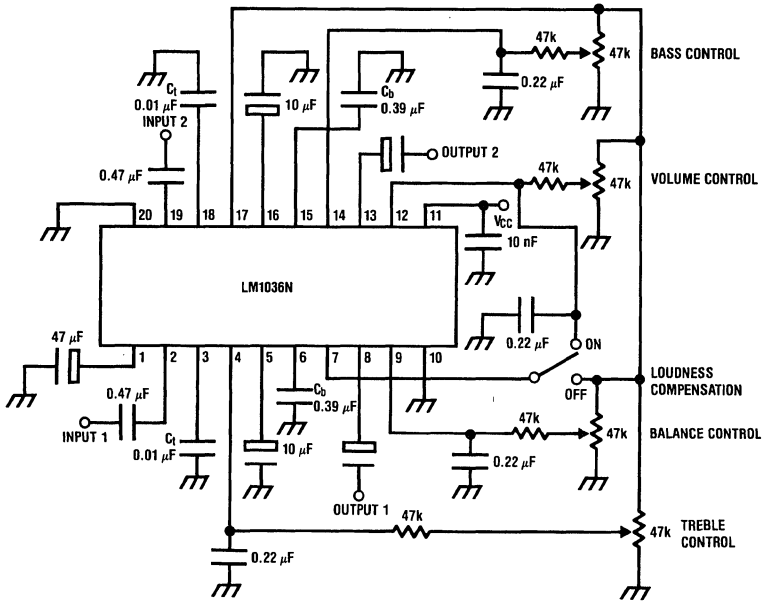
LOUDNESS COMPENSATION

A simple loudness compensation may be effected by applying a DC control voltage to pin 7. This operates on the tone control stages to produce an additional boost limited by the maximum boost defined by C_b and C_t. There is no loudness compensation when pin 7 is connected to pin 17. Pin 7 can be connected to pin 12 to give the loudness compensated volume characteristic as illustrated without the addition of further external components. (Tone settings are for flat response, C_b and C_t as given in Application Circuit.) Modification to the loudness characteristic is possible by changing the capacitors C_b and C_t for a different basic response or, by a resistor network between pins 7 and 12 for a different threshold and slope.

SIGNAL HANDLING

The volume control function of the LM1036 is carried out in two stages, controlled by the DC voltage on pin 12, to improve signal handling capability and provide a reduction of output noise level at reduced gain. The first stage is before the tone control processing and provides an initial 15 dB of gain reduction, so ensuring that the tone sections are not overdriven by large input levels when operating with a low volume setting. Any combination of tone and volume settings may be used provided the output level does not exceed 1 Vrms, V_{CC} = 12V (0.8 Vrms, V_{CC} = 9V). At reduced gain (< −6 dB) the input stage will overload if the input level exceeds 1.6 Vrms, V_{CC} = 12V (1.1 Vrms, V_{CC} = 9V). As there is volume control on the input stages, the inputs may be operated with a lower overload margin than would otherwise be acceptable, allowing a possible improvement in signal to noise ratio.

Application Circuit



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Applications Information

OBTAINING MODIFIED RESPONSE CURVES

The LM1036 is a dual DC controlled bass, treble, balance and volume integrated circuit ideal for stereo audio systems.

In the various applications where the LM1036 can be used, there may be requirements for responses different to those of the standard application circuit given in the data sheet. This application section details some of the simple variations possible on the standard responses, to assist the choice of optimum characteristics for particular applications.

TONE CONTROLS

Summarizing the relationship given in the data sheet, basically for an increase in the treble control range C_t must be increased, and for increased bass range C_b must be reduced.

Figure 1 shows the typical tone response obtained in the standard application circuit. (C_t=0.01 µF, C_b=0.39 µF). Response curves are given for various amounts of boost and cut.

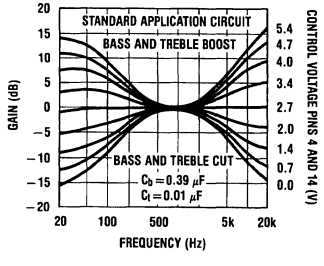

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FIGURE 1. Tone Characteristic (Gain vs Frequency)

Figures 2 and *3* show the effect of changing the response defining capacitors C_t and C_b to 2Ct, C_b/2 and 4C_t, C_b/4 respectively, giving increased tone control ranges. The values of the bypass capacitors may become significant and affect the lower frequencies in the bass response curves.

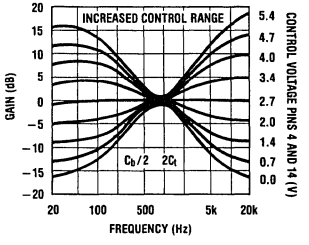

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FIGURE 2. Tone Characteristic (Gain vs Frequency)

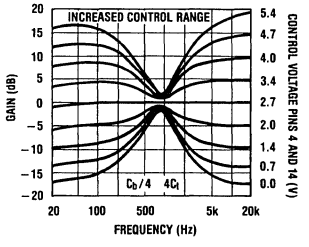

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FIGURE 3. Tone Characteristic (Gain vs Frequency)

Applications Information (Continued)

Figure 4 shows the effect of changing C_t and C_b in the opposite direction to $C_t/2$, $2C_b$ respectively giving reduced control ranges. The various results corresponding to the different C_t and C_b values may be mixed if it is required to give a particular emphasis to, for example, the bass control. The particular case with $C_b/2$, C_t is illustrated in *Figure 5*.

Restriction of Tone Control Action at High or Low Frequencies

It may be desired in some applications to level off the tone responses above or below certain frequencies for example to reduce high frequence noise.

This may be achieved for the treble response by including a resistor in series with C_t. The treble boost and cut will be 3 dB less than the standard circuit when $R = X_C$.

A similar effect may be obtained for the bass response by reducing the value of the AC bypass capacitors on pins 5 (channel 1) and 16 (channel 2). The internal resistance at these pins is 1.3 kΩ and the bass boost/cut will be approximately 3 dB less with X_C at this value. An example of such modified response curves is shown in *Figure 6*. The input coupling capacitors may also modify the low frequency response.

It will be seen from *Figures 2* and *3* that modifying C_t and C_b for greater control range also has the effect of flattening the tone control extremes and this may be utilized, with or without additional modification as outlined above, for the most suitable tone control range and response shape.

Other Advantages of DC Controls

The DC controls make the addition of other features easy to arrange. For example, the negative-going peaks of the output amplifiers may be detected below a certain level, and used to bias back the bass control from a high boost condition, to prevent overloading the speaker with low frequency components.

LOUDNESS CONTROL

The loudness control is achieved through control of the tone sections by the voltage applied to pin 7; therefore, the tone and loudness functions are not independent. There is normally 1 dB more bass than treble boost (40 Hz–16 kHz) with loudness control in the standard circuit. If a greater difference is desired, it is necessary to introduce an offset by means of C_t or C_b or by changing the nominal control voltage ranges.

Figure 7 shows the typical loudness curves obtained in the standard application circuit at various volume levels ($C_b = 0.39\ \mu F$).

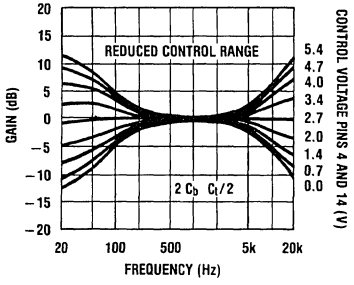

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FIGURE 4. Tone Characteristic (Gain vs Frequency)

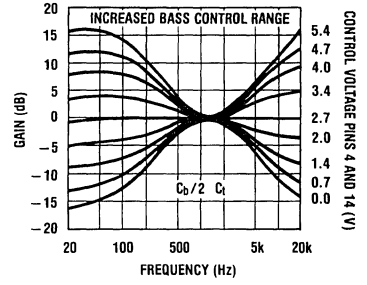

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FIGURE 5. Tone Characteristic (Gain vs Frequency)

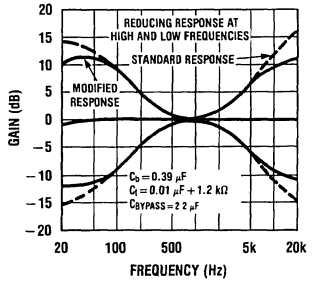

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FIGURE 6. Tone Characteristic (Gain vs Frequency)

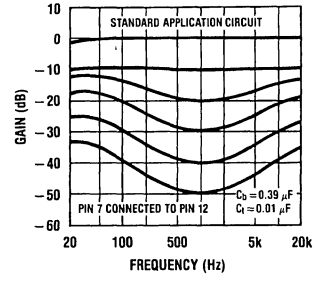

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FIGURE 7. Loudness Compensated Volume Characteristic

Applications Information (Continued)

Figures 8 and *9* illustrate the loudness characteristics obtained with C_b changed to $C_b/2$ and $C_b/4$ respectively, C_t being kept at the nominal 0.01 μF. These values naturally modify the bass tone response as in *Figures 2* and *3*.

With pins 7 (loudness) and 12 (volume) directly connected, loudness control starts at typically −8 dB volume, with most of the control action complete by −30 dB.

Figures 10 and *11* show the effect of resistively offsetting the voltage applied to pin 7 towards the control reference voltage (pin 17). Because the control inputs are high impedance, this is easily done and high value resistors may be used for minimal additional loading. It is possible to reduce the rate of onset of control to extend the active range to −50 dB volume control and below.

The control on pin 7 may also be divided down towards ground bringing the control action on earlier. This is illustrated in *Figure 12*, With a suitable level shifting network between pins 12 and 7, the onset of loudness control and its rate of change may be readily modified.

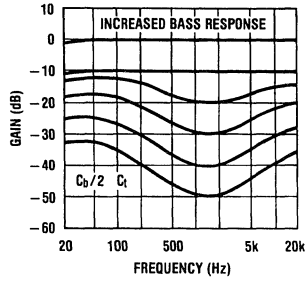

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FIGURE 8. Loudness Compensated Volume Characteristic

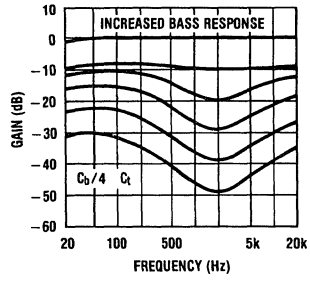

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FIGURE 9. Loudness Compensated Volume Characteristic

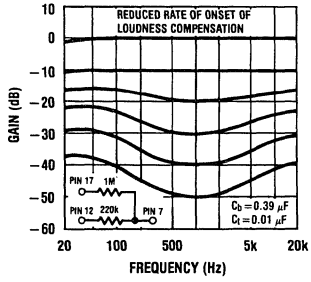

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FIGURE 10. Loudness Compensated Volume Characteristic

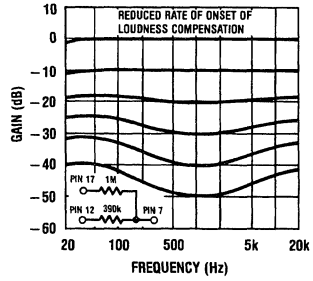

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FIGURE 11. Loudness Compensated Volume Characteristic

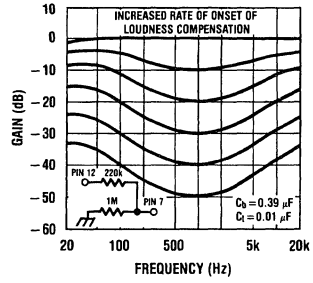

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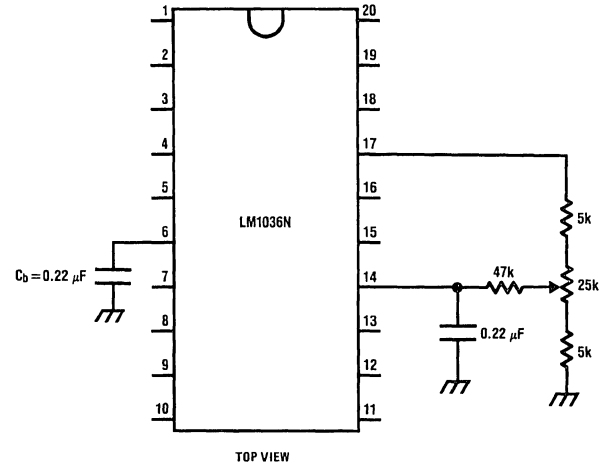
FIGURE 12. Loudness Compensated Volume Characteristic

Applications Information (Continued)

When adjusted for maximum boost in the usual application circuit, the LM1036 cannot give additional boost from the loudness control with reducing gain. If it is required, some additional boost can be obtained by restricting the tone control range and modifying C_t, C_b, to compensate. A circuit illustrating this for the case of bass boost is shown in *Figure 13*. The resulting responses are given in *Figure 14* showing the continuing loudness control action possible with bass boost previously applied.

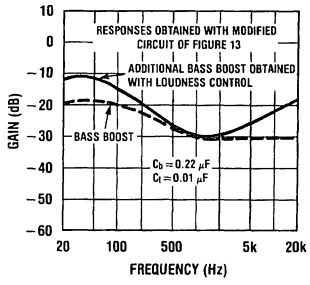
USE OF THE LM1036 ABOVE AUDIO FREQUENCIES

The LM1036 has a basic response typically 1 dB down at 250 kHz (tone controls flat) and therefore by scaling C_b and C_t, it is possible to arrange for operation over a wide frequency range for possible use in wide band equalization applications. As an example *Figure 15* shows the responses obtained centered on 10 kHz with $C_b = 0.039\ \mu F$ and $C_t = 0.001\ \mu F$.



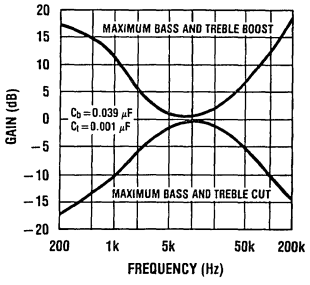
TL/H/5142–16

FIGURE 13. Modified Application Circuit for Additional Bass Boost with Loudness Control



TL/H/5142–17

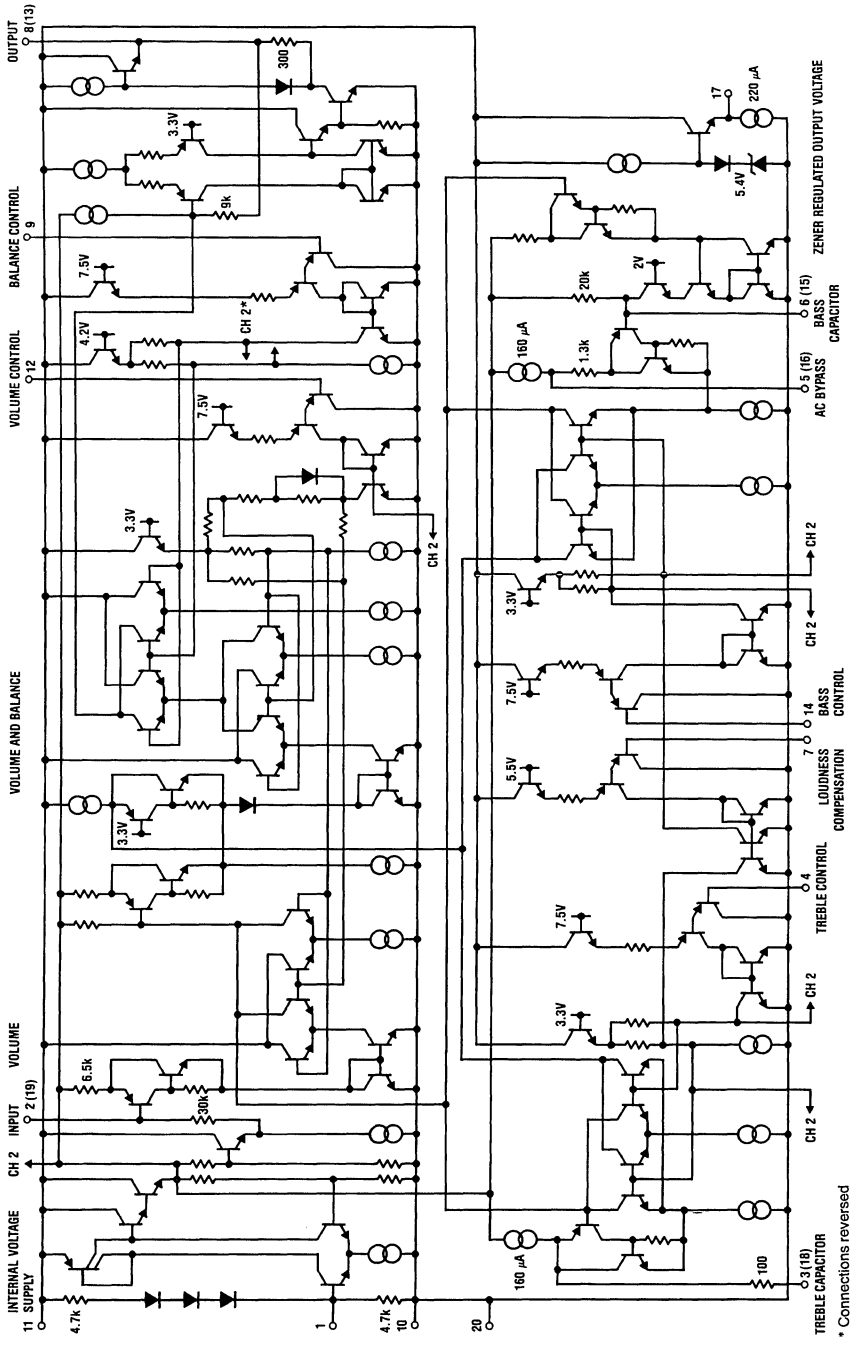
FIGURE 14. Loudness Compensated Volume Characteristic



TL/H/5142–18

FIGURE 15. Tone Characteristic (Gain vs Frequency)

Simplified Schematic Diagram (One Channel)



TL/H/5142–19

National Semiconductor Corporation

LM1037 Dual Four-Channel Analog Switch

General Description

The LM1037 is a dual, electronically controlled, analog switch with an internal muting facility. Any one of four stereo signal sources may be selected by means of four control inputs.

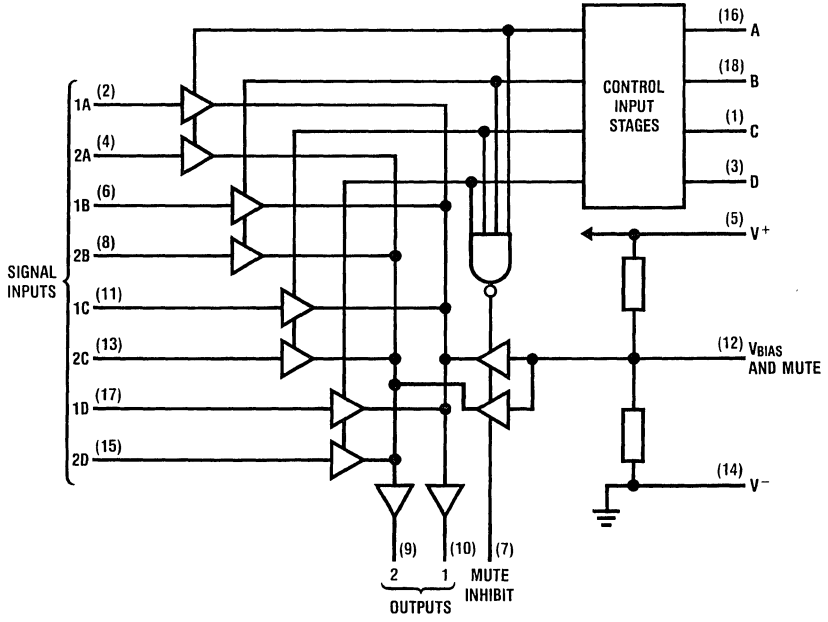
Its features make it ideal for stereo source selection in audio equipment and for use in a wide range of industrial, automotive, multiplexing or sampling applications.

An additional pin is included to allow parallel connection of two or more integrated circuits.

Features

- Wide supply voltage range, 5V–28V
- Low distortion, 0.04% typical
- Low noise, typically 5 μV
- High input impedance
- Low output impedance
- TTL compatible control inputs
- Very low control current

Block Diagram



TL/H/5199–1

Order Package Number LM1037N
See NS Package N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

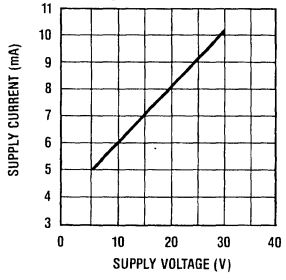
Supply Voltage	28V
Pin 7 Input Current	5 mA
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (Note 1)	1.3W
Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics $V_S = 12V$, $T_A = 25°C$

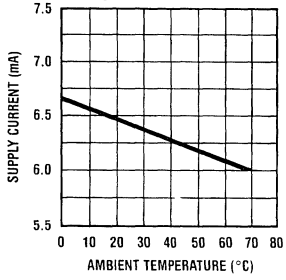
Parameter	Conditions	Typical	Tested Limit (Note 7)	Design Limit (Note 8)	Units (Limits)
Supply Voltage			28		$V_{(max)}$
Supply Voltage				5	$V_{(min)}$
Supply Current	$V_{SUPPLY} = 12V$	6.4	8.5		$mA_{(max)}$
	$V_{SUPPLY} = 28V$	10	14		$mA_{(max)}$
Voltage Gain		0	±0.7		dB
Signal Handling (Notes 2, 6)	$V_{SUPPLY} = 12V$	3.0	2.8		$Vrms_{(min)}$
Small-Signal Bandwidth		300			kHz
Distortion THD	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	0.04	0.1		$\%_{(max)}$
Noise Voltage at Output (Note 3)	CCIR/ARM $R_S = 0\Omega$	5		20	$\mu V_{(max)}$
Channel Separation (Note 4)	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−95		−70	$dB_{(min)}$
Relative Output in Muted State	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−90	−70		$dB_{(min)}$
Output Impedance		10			Ω
Signal Input Impedance		30			MΩ
Logic Low Input Level				0.8	$V_{(max)}$
Logic High Input Level				2.0	$V_{(min)}$
Logic High Input Level				V_{SUPPLY}	$V_{(max)}$

Typical Performance Characteristics ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

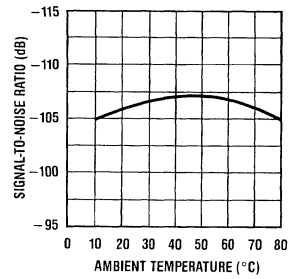
Supply Current vs Supply Voltage



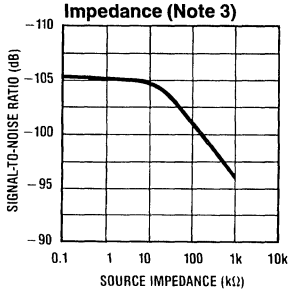
Supply Current vs Temperature



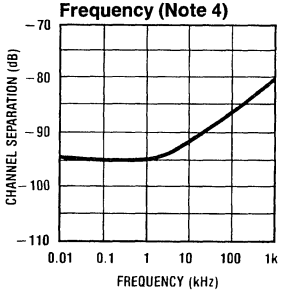
Signal-to-Noise vs Temperature (Note 3)



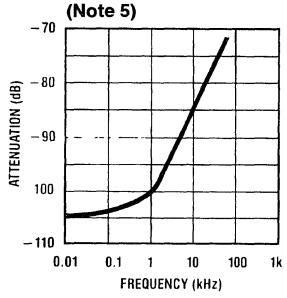
Signal-to-Noise vs Source Impedance (Note 3)



Channel Separation vs Frequency (Note 4)



Attenuation of Unselected Inputs vs Frequency (Note 5)



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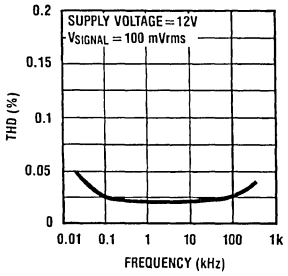
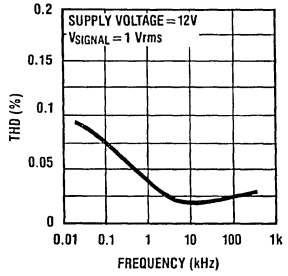
Typical Performance Characteristics (Continued) ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

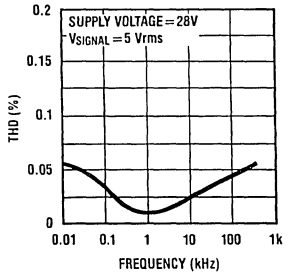
Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency



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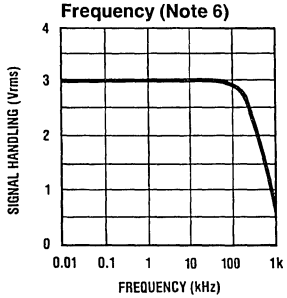
Signal Handling vs Frequency (Note 6)



TL/H/5199–4

Note 1: Above $T_A = 25°C$ derate based on T_J max = 150°C and $\theta_{JA} = 90°C/W$.

Note 2: The instantaneous maximum voltage difference between any two input pins of one channel is 9.6V. Voltages in excess of this level may cause increased distortion and degraded channel separation.

Note 3: Gaussian noise, monitored over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz, and an average-responding meter. Signal to noise ratios are referenced to 1V rms input signal.

Note 4: The level of output signal of a selected undriven amplifier with respect to the output level of a selected driven amplifier. For test purposes, signal is applied to only one input and all other inputs are decoupled to eliminate stray pick-up through external components. Channel separation is then defined as the ratio of signal levels of the two output pins.

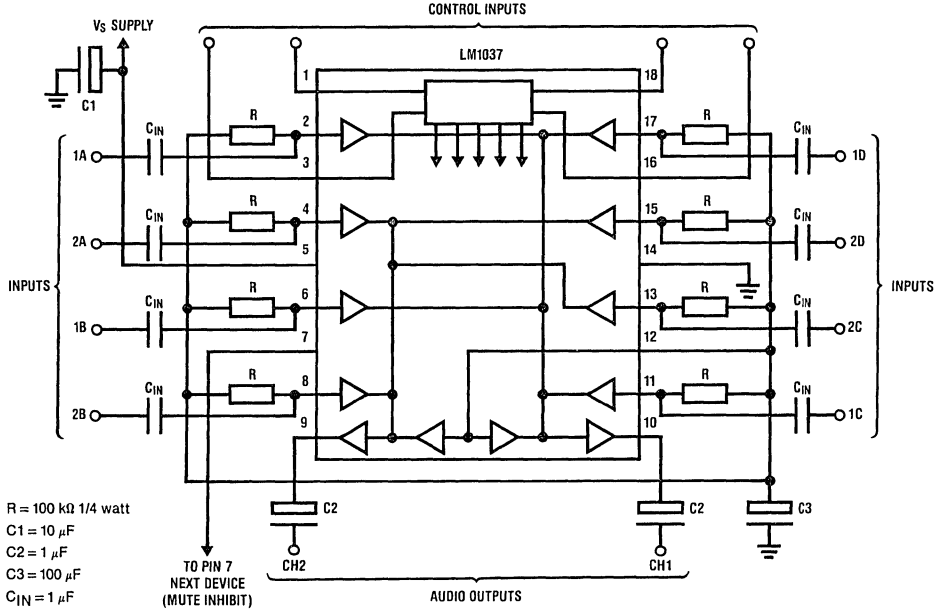
Note 5: For test purposes, signals are connected to three unselected input pins of one channel group and all other inputs are decoupled to eliminate stray pick-up through external components.

Note 6: Supply voltage 12V; signal handling defined at 1% distortion, 1 kHz.

Note 7: Guaranteed and 100% production tested.

Note 8: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Application



TL/H/5199–5

Truth Tables

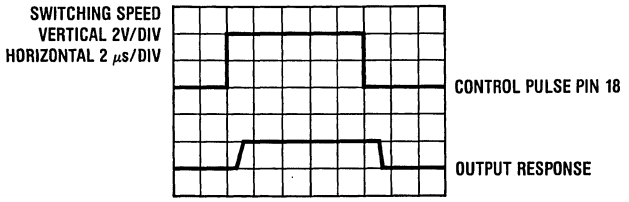
LM1037

Channel selection is achieved by the application of DC voltages to the control pins. Unselected control pins should be held low.

DC Control Pin in HIGH State	Input Pair Switched to Output Pins (10, 9)	
16	A	(2,4)
18	B	(6,8)
1	C	(11,13)
3	D	(17,15)
None	Mute	(12)

Low switching level (V_L) < 0.8V

High switching level (V_H) > 2.0V and up to V_{SUPPLY}



TL/H/5199–6

2 DEVICES CONNECTED IN PARALLEL

To increase the channel switching capacity, two or more devices can be connected together by the direct coupling of the mute inhibit pin 7 and the output pins 9 and 10. Only one output capacitor is required for each common output.

	DC Control Pin in HIGH State	Input Pair Switched to Output Pins (10,9)	
Device Number 1	16	A	(2,4)
	18	B	(6,8)
	1	C	(11,13)
	3	D	(17,15)
Device Number 2	16	A	(2,4)
	18	B	(6,8)
	1	C	(11,13)
	3	D	(17,15)
	None	Mute	(12)

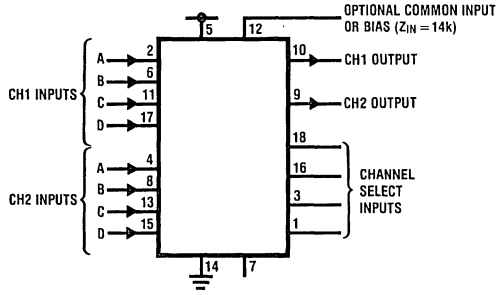
Pin Function Description

Device Pins	Description
Pin 16—Inputs A Select Pin 18—Inputs B Select Pin 1—Inputs C Select Pin 3—Inputs D Select	A high input level selects the corresponding channel. Only one channel should be selected at a time. Unselected channels should have their select inputs at a low level. Open circuit pins represent a high input level.
Pins 2, 6, 11, 17— Inputs for Output 1 (Pin 10) Pins 4, 8, 13, 15— Inputs for Output 2 (Pin 9)	Two sets of four high impedance channel inputs for the connection of signals to be switched.
Pin 12—Mute Bias Level	The DC level at this pin is applied to the outputs when no input is selected and pin 7 is open. The level is internally set by a 25 kΩ and 33 kΩ potential divider at 0.6 V_S. This level may be adjusted by means of external resistors. Pin 12 may also be used as an additional common input in which case this signal is present on both outputs when no control input is applied.
Pin 7—Mute Inhibit Input	With this pin unconnected and no channel selection input is present; the mute level at pin 12 is applied to the outputs. With pin 7 grounded and no channel selection input present, the device output emitter-followers are disabled allowing parallel connection to other device outputs. This pin is a current input and any current applied should be limited to 5 mA maximum. Pin 7 of several devices may be directly connected for parallel operation.
Pin 9—Output 2 Pin 10—Output 1	These are common output pins for each channel. There are three possible output conditions: 1) Signal selected from 1 of 4 inputs. 2) Mute level output. 3) Device not selected—internal 6 kΩ pull-down resistors to ground.
Pin 5	Positive supply voltage.
Pin 14	Negative or ground supply voltage.

Application Hints

The basic circuit arrangement with minimum external components for use with DC coupled signals is shown in *Figure 1*. This arrangement may be used in a normal signal selection system or in the feedback path of DC coupled amplifiers for example to make a simple dual programmable power supply. By switching feedback connections dual programmable gain or frequency response amplifiers may be obtained.

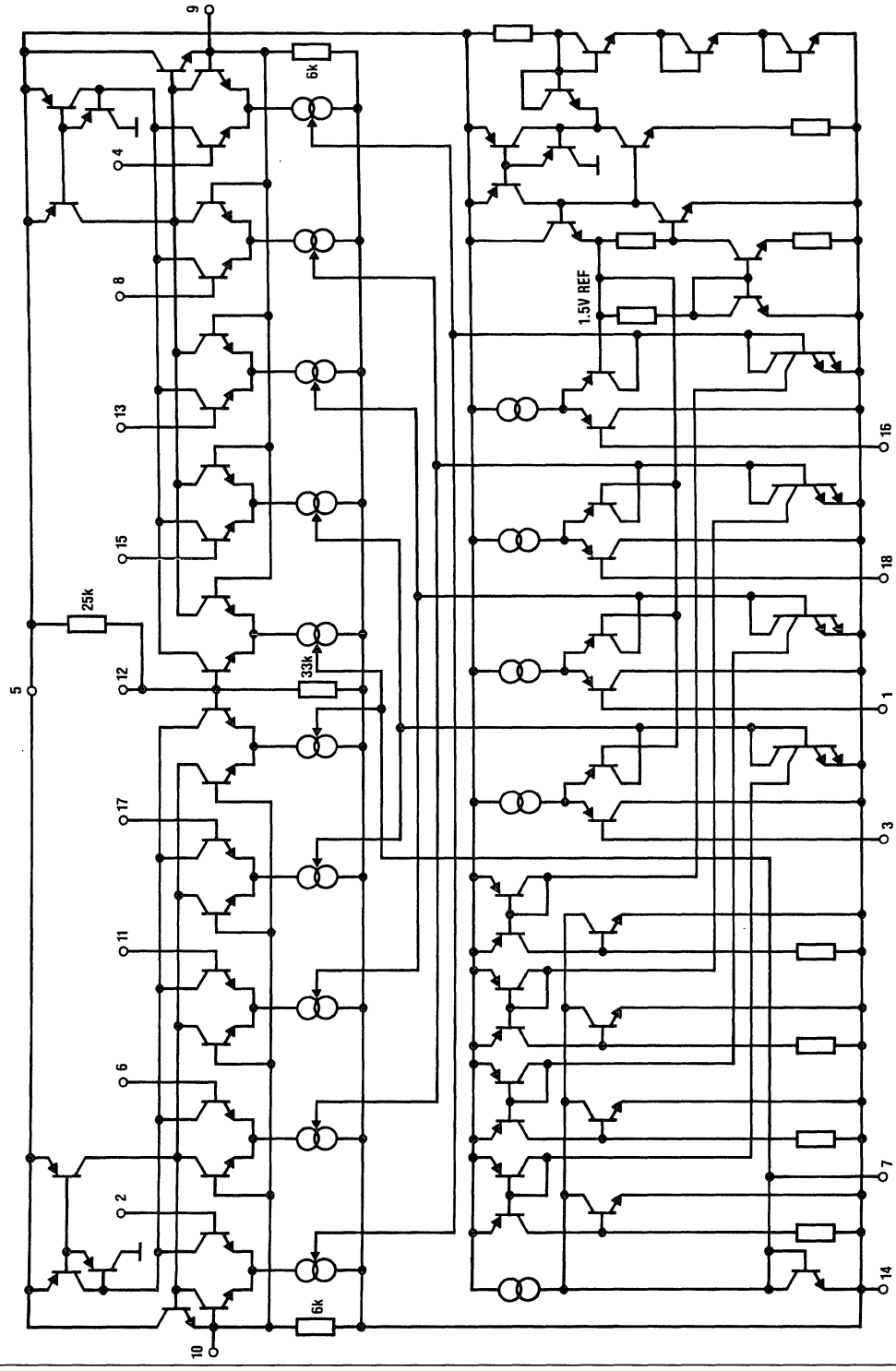
For switching between signal sources in stereo systems the LM1037 may be connected as shown in the typical application circuit. The input bias is obtainable from pin 12 or an alternative source may be used. If split supply operation is required, pin 12 may be grounded and the signals referenced to ground.



DC coupled signals $1.2V < V_{IN} < V_S - 1V$

FIGURE 1

Simplified Circuit Schematic (All signal and control inputs are Darlington connected)



TL/H/5199–15

National Semiconductor Corporation

LM1038 Dual Four-Channel Analog Switch

General Description

The LM1038 is a dual, electronically controlled, four-channel analog switch with an internal muting facility.

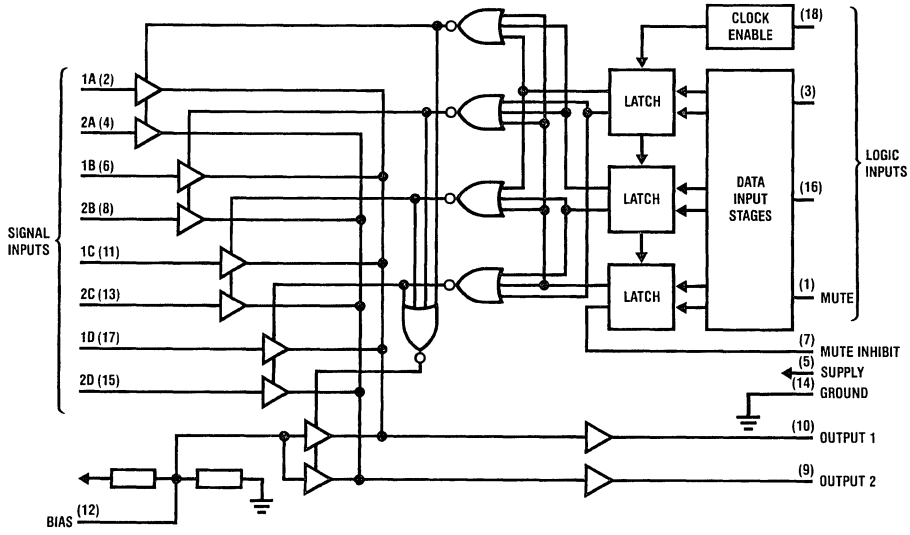
Its features make it ideal for stereo source selection in audio equipment and for use in a wide range of industrial, automotive, multiplexing or sampling applications.

Channel selection is achieved via two logic data pins with clock enabled latches. Muting is also selectable under clock control.

Features

- Wide supply voltage range, 5V-28V
- Low distortion, 0.04% typical
- High input impedance
- Low output impedance
- TTL compatible control Inputs
- Very low control current
- 2 control pins accept BCD input pulses
- Clock enable input may be strobed from a bus

Block Diagram



TL/H/5200–1

Order Number LM1038N
See NS Package Number N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

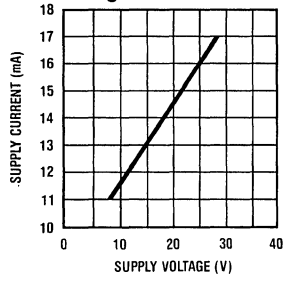
Supply Voltage	28V
Pin 7 Input Current	5 mA
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (Note 1)	1.3W
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics $V_S = 12V$, $T_A = 25°C$.

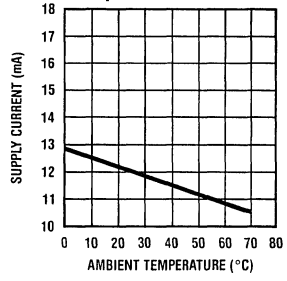
Parameter	Conditions	Typ	Tested Limit (Note 7)	Design Limit (Note 8)	Units (Limits)
Supply Voltage			28		$V_{(max)}$
Supply Voltage				5	$V_{(min)}$
Supply Current	$V_{SUPPLY} = 12V$	12	17		$mA_{(max)}$
	$V_{SUPPLY} = 28V$	17	28		$mA_{(max)}$
Voltage Gain		0	±0.7		dB
Signal Handling (Notes 2, 6)	$V_{SUPPLY} = 12V$	3.0	2.8		$Vrms_{(MIN)}$
Small-Signal Bandwidth		300			kHz
Distortion THD	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	0.04	0.1		$\%_{(max)}$
Noise Voltage at Output (Note 3)	CCIR/ARM $R_S = 0\Omega$	5		20	$\mu V_{(max)}$
Channel Separation (Note 4)	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−95		−70	$dB_{(min)}$
Relative Output in Muted State	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−90	−70		$dB_{(min)}$
Output Impedance		10			Ω
Signal Input Impedance		30			MΩ
Logic Low Input Level				0.8	$V_{(max)}$
Logic High Input Level				2.0	$V_{(min)}$
Logic High Input Level				V_{SUPPLY}	$V_{(max)}$

Typical Performance Characteristics ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

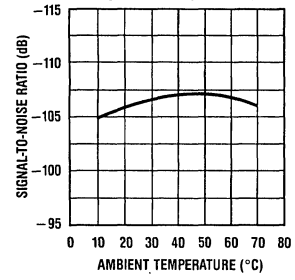
Supply Current vs Supply Voltage



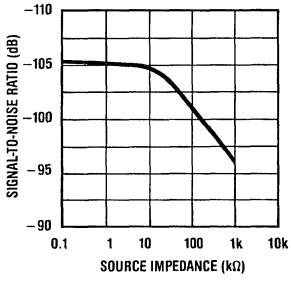
Supply Current vs Temperature



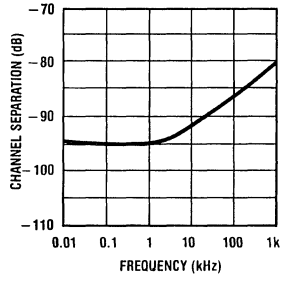
Signal-to-Noise vs Temperature (Note 3)



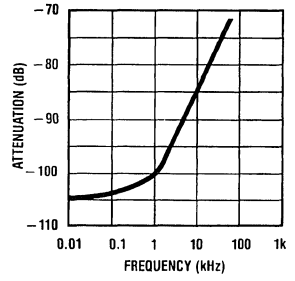
Signal-to-Noise vs Source Impedance (Note 3)



Channel Separation vs Frequency (Note 4)



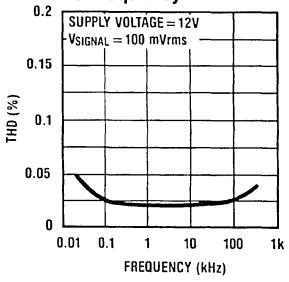
Attenuation of Unselected Inputs vs Frequency (Note 5)



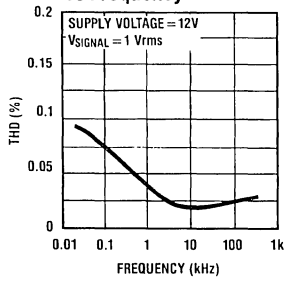
TL/H/5200–2

Typical Performance Characteristics (Continued) ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

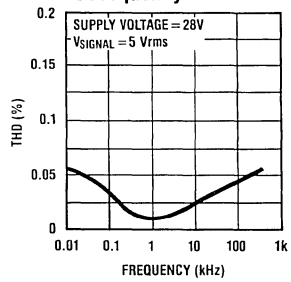
Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency

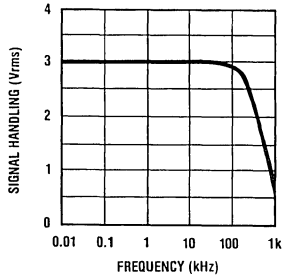


Total Harmonic Distortion vs Frequency



TL/H/5200–3

Signal Handling vs Frequency (Note 6)



TL/H/5200–4

Note 1: Above $T_A = 25°C$ derate based on T_J max = 150°C and $\theta_{JA} = 90°C/W$.

Note 2: The instantaneous maximum voltage difference between any two input pins of one channel is 9.6V. Voltages in excess of this level may cause increased distortion and degraded channel separation.

Note 3: Gaussian noise, monitored over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz, and an average responding meter. Signal-to-noise ratios are referenced to a 1 Vrms input signal.

Note 4: The level of output signal of a selected undriven amplifier with respect to the output level of a selected driven amplifier. For test purposes, signal is applied to only one input and all other inputs are decoupled to eliminate stray pick-up through external components. Channel separation is then defined as the ratio of signal levels of the two output pins.

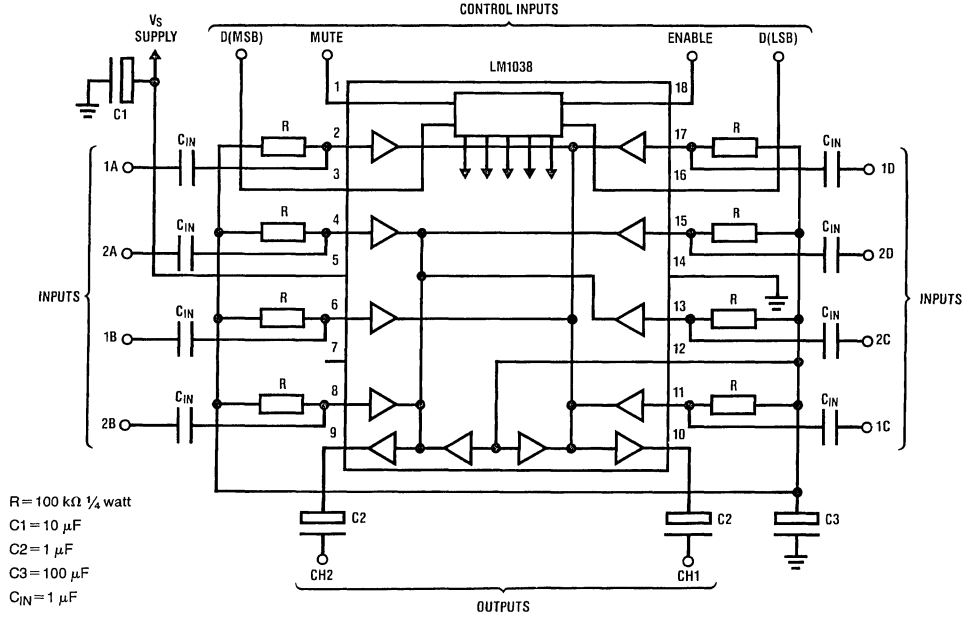
Note 5: For test purposes, signals are connected to three unselected input pins of one channel group and all other inputs are decoupled to eliminate stray pick-up through external components.

Note 6: Supply voltage 12V; signal handling defined at 1% distortion, 1 kHz.

Note 7: Guaranteed and 100% production tested.

Note 8: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Application



R = 100 kΩ ¼ watt
C1 = 10 µF
C2 = 1 µF
C3 = 100 µF
C_{IN} = 1 µF

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Truth Table

Logic Inputs				Input Pin Selected	
Latch Enable Pin 18	Mute Pin 1	Channel Select Data Pin 3	Pin 16	Output 1 Pin 10	Output 2 Pin 9
1	0	0	0	D Pin 17	D Pin 15
1	0	0	1	A Pin 2	A Pin 4
1	0	1	0	B Pin 6	B Pin 8
1	0	1	1	C Pin 11	C Pin 13
1	1	X	X	Pin 12 Mute Bias	
0	X	X	X	Inputs Previously Selected are Retained	

Low (0) < 0.8V
High (1) > 2.0V, up to V_{SUPPLY}

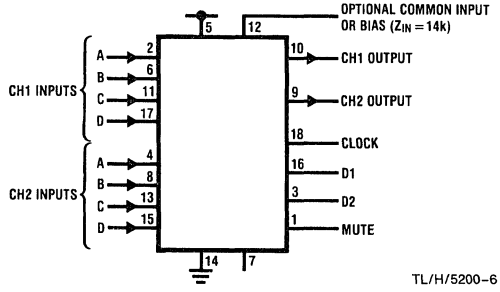
Pin Function Description

Device Pins	Description
Pin 1—Mute	A high level on this input will select the muted condition (outputs = pin 12 voltage) if the latch enable input is low provided pin 7 (mute enable) is open.
Pin 3—Channel Address (MSB) Pin 16—Inputs (LSB)	Binary information on these pins selects the required channel if the mute select input, pin 1, is low.
Pin 18—Latch Enable	With a high level on this pin the data on the channel select pins controls the channel enabled. When the input is low the channel select data is latched. The mute input pin 1 is also controlled by this input. A minimum enable pulse width of typically 3 μs is required.
Pins 2, 6, 11, 17— Inputs for Output 1 (Pin 10) Pins 4, 8, 13, 15— Inputs for Output 2 (Pin 9)	Two sets of four high impedance channel inputs for the connection of signals to be switched.
Pin 12—Mute Bias Level	The DC level at this pin is applied to the outputs when the mute input, pin 1, is activated. The level is internally set by a 25 kΩ and 33 kΩ potential divider to 0.6 V_S. This level may be adjusted by means of external resistors. Pin 12 may also be used as an additional common signal input.
Pin 7—Mute Inhibit	This is a current input and any control current into this pin must be externally limited to 5 mA maximum. With this pin open the mute input, pin 1, is enabled. With a current into this pin the mute facility is disabled and with no signal channel selected the output emitter-followers are disabled.
Pin 9—Output 2 Pin 10—Output 1	These are common output pins for each channel. There are three possible output conditions: 1) Signal selected from 1 of 4 inputs. 2) Mute level output. 3) Device not selected—internal 6 kΩ pull-down resistors to ground.
Pin 5	Positive supply voltage.
Pin 14	Negative or ground supply voltage.

Application Hints

The basic circuit arrangement with minimum external components for use with DC coupled signals is shown in *Figure 1*. This arrangement may be used in a normal signal selection system or in the feedback path of DC coupled amplifiers for example to make a simple dual programmable power supply. By switching feedback connections dual programmable gain or frequency response amplifiers may be obtained.

For switching between signal sources in stereo systems the LM1038 may be connected as shown in the typical application circuit. The input bias is obtainable from pin 12 or an alternative source may be used. If split supply operation is required, pin 12 may be grounded and the signals referenced to ground.



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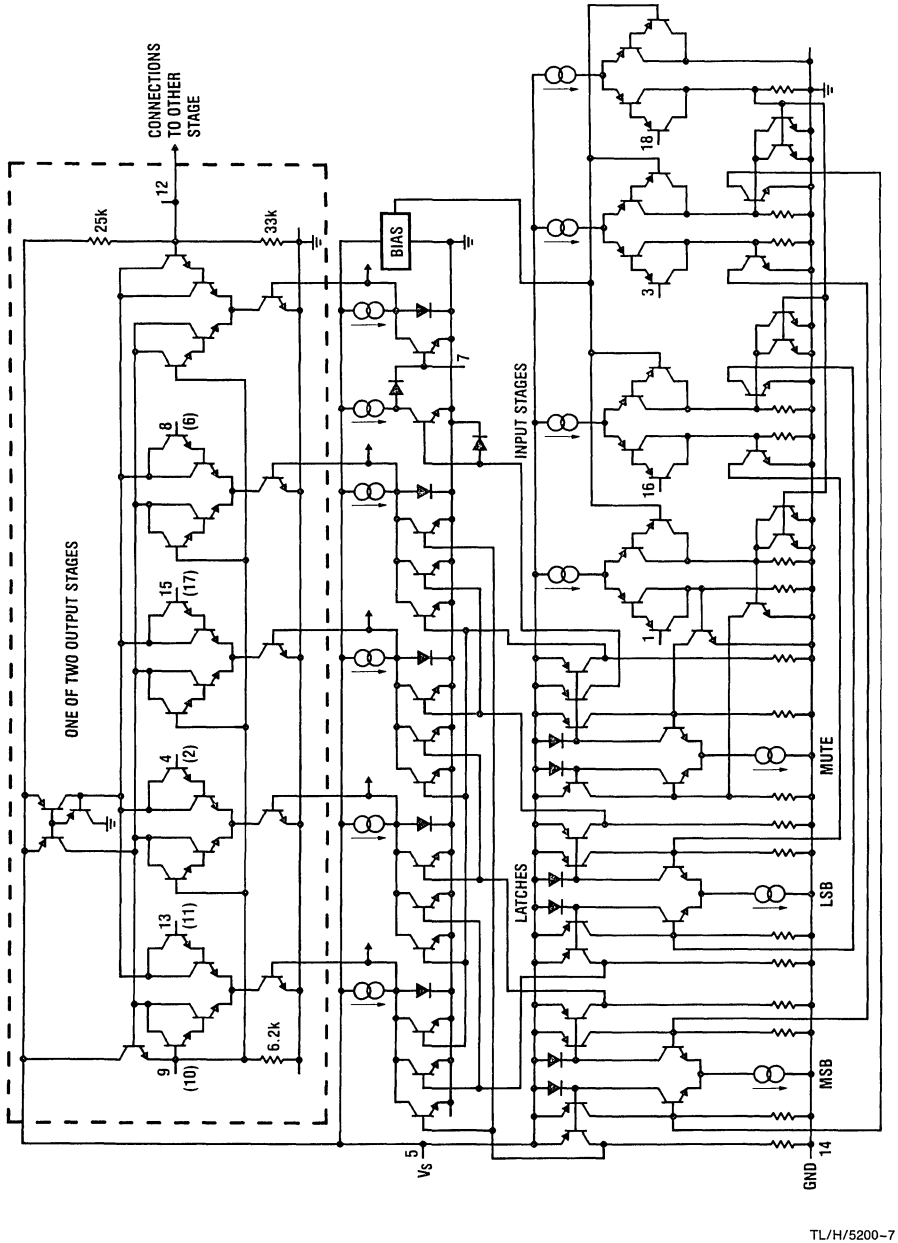
DC coupled signals $1.2V < V_{IN} < V_S - 1V$

FIGURE 1

Equivalent Schematic Diagram



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National Semiconductor Corporation

LM1040 Dual DC Operated Tone/Volume/Balance Circuit with Stereo Enhancement Facility

General Description

The LM1040 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. A stereo enhancement facility is included whereby the apparent stereo separation of systems requiring closely spaced speakers may be improved. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

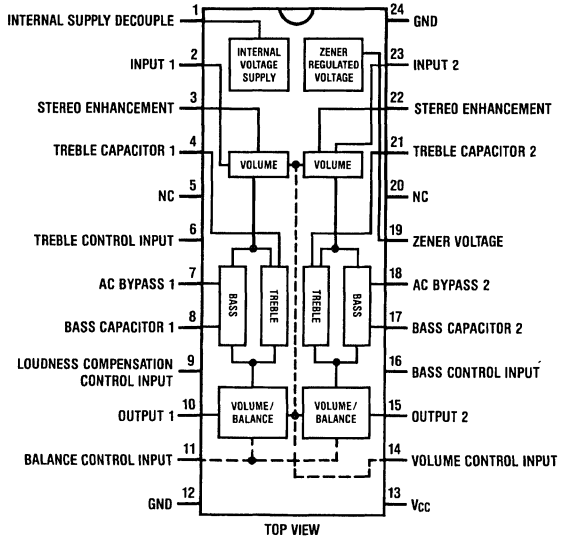
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 9V to 16V
- Large volume control range, 75 dB typical
- Tone control, ±15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 0.3 Vrms
- High signal to noise, 80 dB typical for an input level of 0.3 Vrms
- Few external components required

Block and Connection Diagrams

Dual-in-Line Package



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Order Number LM1040N
See NS Package Number N24A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	16V
Control Pin Voltage (Pins 6, 9, 11, 14, 16)	V_{CC}
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics $V_{CC}=12V$, $T_A=25°C$ (unless otherwise stated)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range	Pin 13	9		16	V
Supply Current			35	45	mA
Zener Regulated Output Voltage Current	Pin 19		 5.4	 5	 V mA
Maximum Output Voltage	Pins 10, 15; f = 1 kHz V_{CC} = 9V, Maximum Gain V_{CC} = 12V	 0.8	 0.8 1.0		 Vrms Vrms
Maximum Input Voltage (Note 1)	Pins 2, 23; f = 1 kHz, V_{CC} = 9V Flat Response, V_{CC} = 12V Gain = −10 dB	 1.3	1.1 1.6		Vrms Vrms
Input Resistance	Pins 2, 23; f = 1 kHz	20	30		kΩ
Output Resistance	Pins 10, 15; f = 1 kHz		20		Ω
Maximum Gain	V(Pin 14) = V(Pin 19); f = 1 kHz	−2	0	2	dB
Volume Control Range	f = 1 kHz	70	75		dB
Gain Tracking Channel 1-Channel 2	f = 1 kHz 0 dB through −40 dB −40 dB through −60 dB		 1 2	 3	 dB dB
Balance Control Range	Pins 10, 15; f = 1 kHz		1 −26	 −20	dB dB
Bass Control Range (Note 2)	f = 40 Hz, C_b = 0.39 μF V(Pin 16) = V(Pin 19) V(Pin 16) = 0V	 12 −12	 15 −15	 18 −18	 dB dB
Treble Control Range (Note 2)	f = 16 kHz, C_t = 0.01 μF V(Pin 6) = V(Pin 19) V(Pin 6) = 0V	 12 −12	 15 −15	 18 −18	 dB dB
Total Harmonic Distortion	f = 1 kHz, V_{IN} = 0.3 Vrms Gain = 0 dB Gain = −30 dB		 0.06 0.03	 0.3	 % %
Channel Separation	f = 1 kHz, Maximum Gain	60	75		dB
Signal/Noise Ratio	Unweighted 100 Hz-20 kHz Maximum Gain, 0 dB = 0.3 Vrms CCIR/ARM (Note 3) Gain = 0 dB, V_{IN} = 0.3 Vrms Gain = −20 dB, V_{IN} = 1.0 Vrms	 75	80 79 72	 	dB dB dB
Output Noise Voltage at Minimum Gain	CCIR/ARM (Note 3)		10		μV
Supply Ripple Rejection	200 mVrms, 1 kHz Ripple	35	−50		dB
Control Input Currents	Pins 6, 9, 11, 14, 16 (V = 0V)		−0.6	−2.5	μA
Frequency Response	−1 dB (Flat Response 20 Hz−16 kHz)		250		kHz

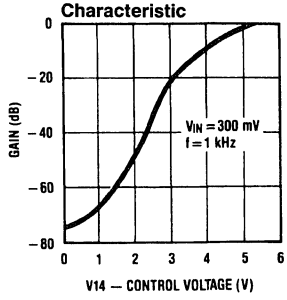
Note 1: The maximum permissible input level is dependent on tone and volume settings. See Application Notes.

Note 2: The tone control range is defined by capacitors C_b and C_t. See Application Notes.

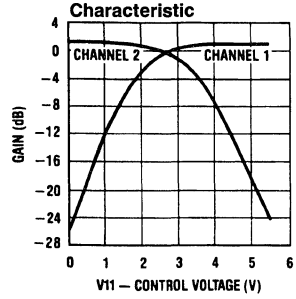
Note 3: Gaussian noise, measured over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz and an average-responding meter.

Typical Performance Characteristics

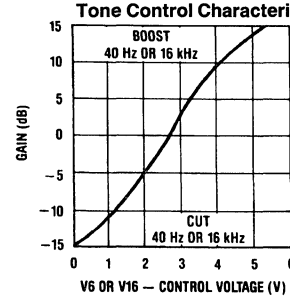
Volume Control Characteristic



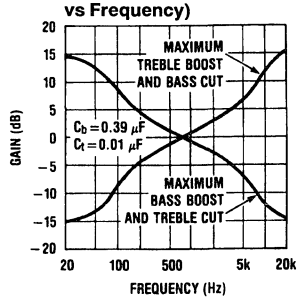
Balance Control Characteristic



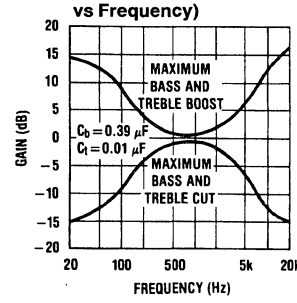
Tone Control Characteristic



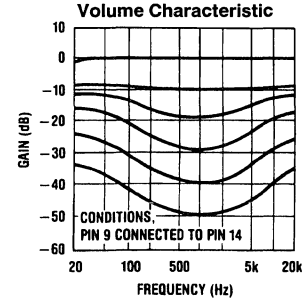
Tone Characteristic (Gain vs Frequency)



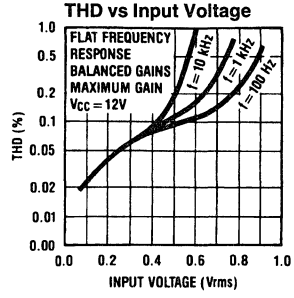
Tone Characteristic (Gain vs Frequency)



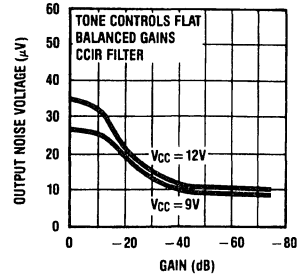
Loudness Compensated Volume Characteristic



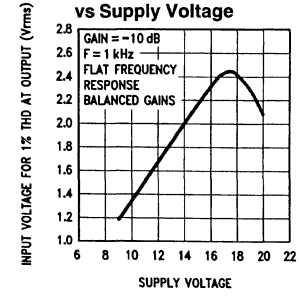
THD vs Input Voltage



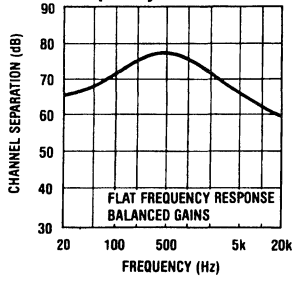
Output Noise Voltage vs Gain



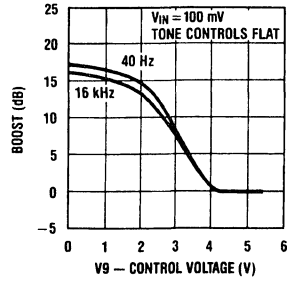
Input Signal Handling vs Supply Voltage



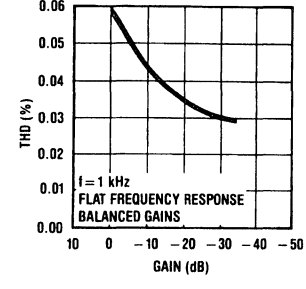
Channel Separation vs Frequency



Loudness Control Characteristic



THD vs Gain



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Application Notes

TONE RESPONSE

The maximum boost and cut can be optimized for individual applications by selection of the appropriate values of C_t (treble) and C_b (bass).

The tone responses are defined by the relationships:

$$\text{Bass Response} = \frac{1 + \dfrac{0.00065(1 - a_b)}{j\omega C_b}}{1 + \dfrac{0.00065 a_b}{j\omega C_b}}$$

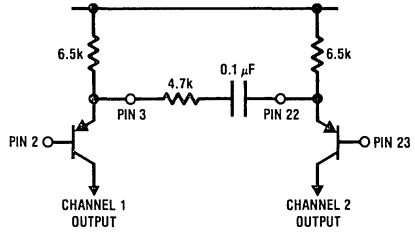
$$\text{Treble Response} = \frac{1 + j\omega 5500(1 - a_t)C_t}{1 + j\omega 5500 a_t C_t}$$

Where $a_b = a_t = 0$ for maximum bass and treble boost respectively and $a_b = a_t = 1$ for maximum cut.

For the values of C_b and C_t of 0.39 μF and 0.01 μF as shown in the Application Circuit, 15 dB of boost or cut is obtained at 40 Hz and 16 kHz.

STEREO ENHANCEMENT

When stereo system speakers need to be closer than optimum because of equipment/cabinet limitations, an improved stereo effect can be obtained using a modest amount of phase—reversed interchannel cross-coupling. In the LM1040 the input stage transistor emitters are brought out to facilitate this. The arrangement is shown below in basic form.



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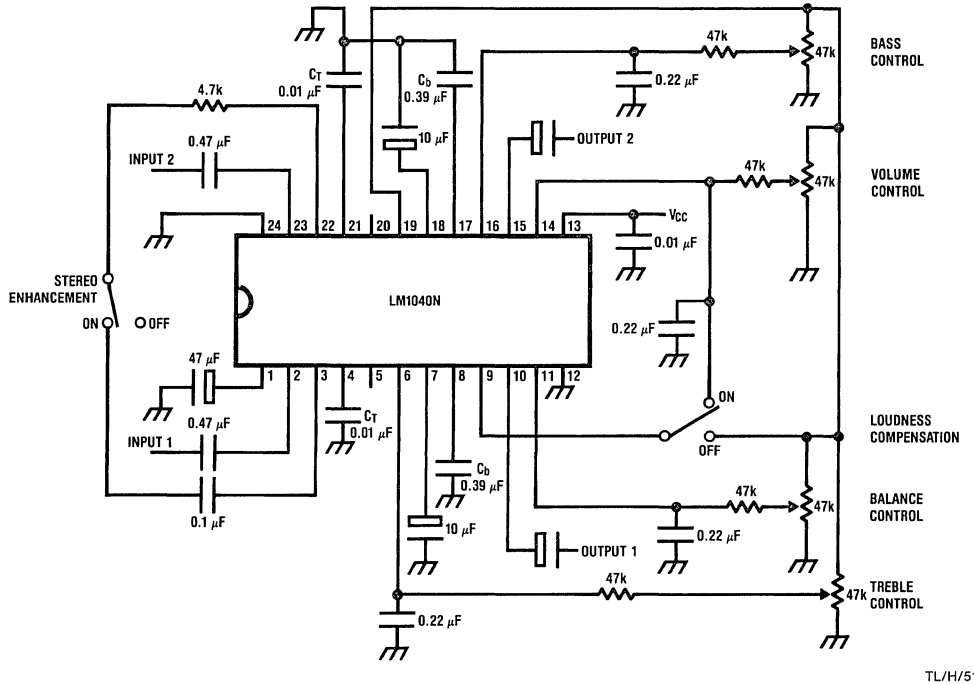
With a monophonic source, the emitters have the same signal and the resistor and capacitor connected between them have no effect. With a stereo signal each transistor works in the grounded base mode for stereo components, generating an in-phase signal from the opposite channel. As the normal signals are inverted at this point, the appropriate phase-reversed cross-coupling is achieved. An effective level of coupling of 60% can be obtained using 4.7k in conjunction with the internal 6.5k emitter resistors. At low frequencies, speakers become less directional and it becomes desirable to reduce the enhancement effect. With a 0.1 μF coupling capacitor, as shown, roll-off occurs below 330 Hz. The coupling components may be varied for alternative responses.

Application Circuit



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Application Notes (Continued)

ZENER VOLTAGE

A zener voltage (pin 19 = 5.4V) is provided which may be used to bias the control potentiometers. Setting a DC level of one half of the zener voltage on the control inputs, pins 6, 11, and 16, results in the balanced gain and flat response condition. Typical spread on the zener voltage is ±100 mV and this must be taken into account if control signals are used which are not referenced to the zener voltage. If this is the case, then they will need to be derived with similar accuracy.

LOUDNESS COMPENSATION

A simple loudness compensation may be effected by applying a DC control voltage to pin 9. This operates on the tone control stages to produce an additional boost limited by the maximum boost defined by C_b and C_t. There is no loudness compensation when pin 9 is connected to pin 19. Pin 9 can be connected to pin 14 to give the loudness compensated volume characteristic as illustrated without the addition of further external components. (Tone settings are for flat response, C_b and C_t as given in Application Circuit.) Modification to the loudness characteristic is possible by changing the capacitors C_b and C_t for a different basic response or, by a resistor network between pins 9 and 14 for a different threshold and slope.

SIGNAL HANDLING

The volume control function of the LM1040 is carried out in two stages, controlled by the DC voltage on pin 14, to improve signal handling capability and provide a reduction of output noise level at reduced gain. The first stage is before the tone control processing and provides an initial 15 dB of gain reduction, so ensuring that the tone sections are not overdriven by large input levels when operating with a low volume setting. Any combination of tone and volume settings may be used provided the output level does not exceed 1 Vrms, V_{CC} = 12V(0.7 Vrms, V_{CC} = 9V). At reduced gain (< −6 dB) the input stage will overload if the input level exceeds 1.6 Vrms, V_{CC} = 12V (1.1 Vrms, V_{CC} = 9V). As there is volume control on the input stages, the inputs may be operated with a lower overload margin than would otherwise be acceptable, allowing a possible improvement in signal to noise ratio.

Applications Information

OBTAINING MODIFIED RESPONSE CURVES

The LM1040 is a dual DC controlled bass, treble, balance and volume integrated circuit ideal for stereo audio systems.

In the various applications where the LM1040 can be used, there may be requirements for responses different to those of the standard application circuit given in the data sheet. This application section details some of the simple variations possible on the standard responses, to assist the choice of optimum characteristics for particular applications.

TONE CONTROLS

Summarizing the relationship given in the data sheet, basically for an increase in the treble control range C_t must be increased, and for increased bass range C_b must be reduced.

Figure 1 shows the typical tone response obtained in the standard application circuit. (C_t = 0.01 µF, C_b = 0.39 µF). Response curves are given for various amounts of boost and cut.

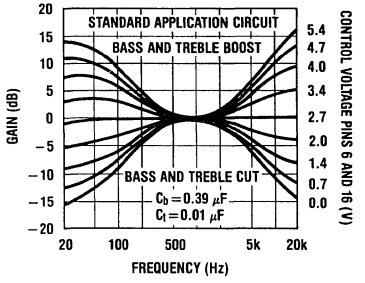

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FIGURE 1. Tone Characteristic (Gain vs Frequency)

Figures 2 and *3* show the effect of changing the response defining capacitors C_t and C_b to 2Ct, $C_b/2$ and $4C_t$, $C_b/4$ respectively, giving increased tone control ranges. The values of the bypass capacitors may become significant and affect the lower frequencies in the bass response curves.

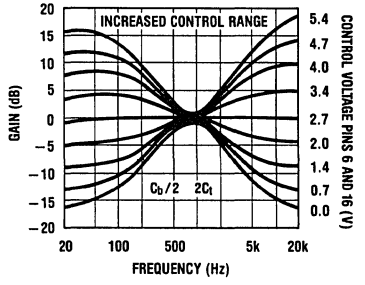

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FIGURE 2: Tone Characteristic (Gain vs Frequency)

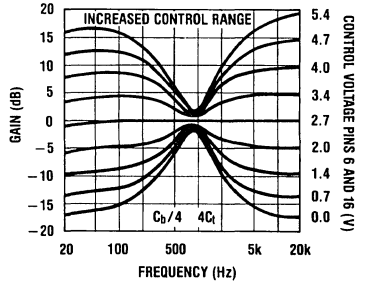

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FIGURE 3: Tone Characteristic (Gain vs Frequency)

Applications Information (Continued)

Figure 4 shows the effect of changing C_t and C_b in the opposite direction to $C_t/2$, $2C_b$ respectively giving reduced control ranges. The various results corresponding to the different C_t and C_b values may be mixed if it is required to give a particular emphasis to, for example, the bass control. The particular case with $C_b/2$, C_t is illustrated in *Figure 5.*

RESTRICTION OF TONE CONTROL ACTION AT HIGH OR LOW FREQUENCIES

It may be desired in some applications to level off the tone responses above or below certain frequencies for example to reduce high frequency noise.

This may be achieved for the treble response by including a resistor in series with C_t. The treble boost and cut will be 3 dB less than the standard circuit when $R = X_C$.

A similar effect may be obtained for the bass response by reducing the value of the AC bypass capacitors on pins 7 (channel 1) and 18 (channel 2). The internal resistance at these pins is 1.3 kΩ and the bass boost/cut will be approximately 3 dB less with X_C at this value. An example of such modified response curves is shown in *Figure 6*. The input coupling capacitors may also modify the low frequency response.

It will be seen from *Figures 2* and *3* that modifying C_t and C_b for greater control range also has the effect of flattening the tone control extremes and this may be utilized, with or without additional modification as outlined above, for the most suitable tone control range and response shape.

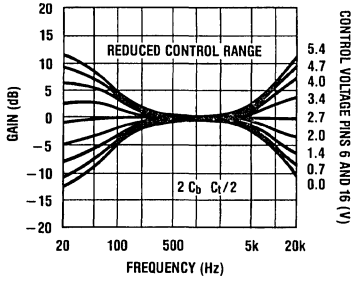
OTHER ADVANTAGES OF DC CONTROLS

The DC controls make the addition of other features easy to arrange. For example, the negative-going peaks of the output amplifiers may be detected below a certain level, and used to bias back the bass control from a high boost condition; to prevent overloading the speaker with low frequency components.

LOUDNESS CONTROL

The loudness control is achieved through control of the tone sections by the voltage applied to pin 9; therefore, the tone and loudness functions are not independent. There is normally 1 dB more bass than treble boost (40 Hz−16 kHz) with loudness control in the standard circuit. If a greater difference is desired, it is necessary to introduce an offset by means of C_t or C_b or by changing the nominal control voltage ranges.

Figure 7 shows the typical loudness curves obtained in the standard application circuit at various volume levels ($C_b = 0.39\ \mu F$).



TL/H/5147–8

FIGURE 4. Tone Characteristic (Gain vs Frequency)

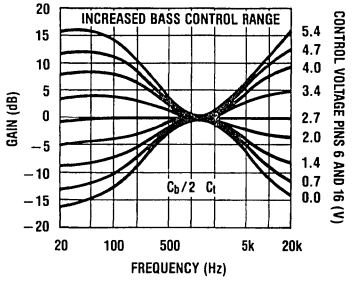


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FIGURE 5. Tone Characteristic (Gain vs Frequency)

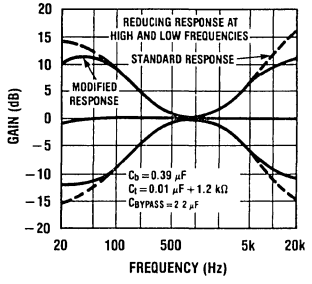

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FIGURE 6. Tone Characteristic (Gain vs Frequency)

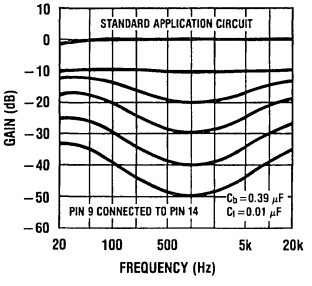

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FIGURE 7. Loudness Compensated Volume Characteristic

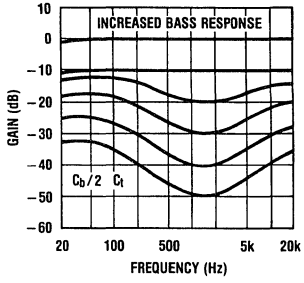
Applications Information (Continued)

Figures 8 and *9* illustrate the loudness characteristics obtained with C_b changed to $C_b/2$ and $C_b/4$ respectively, C_t being kept at the nominal 0.01 μF. These values naturally modify the bass tone response as in *Figures 2* and *3*.

With pins 9 (loudness) and 14 (volume) directly connected, loudness control starts at typically −8 dB volume, with most of the control action complete by −30 dB.

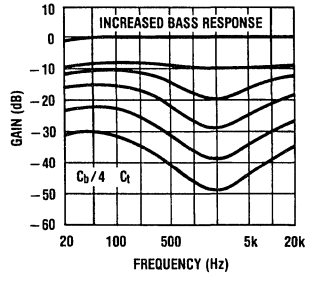
Figures 10 and *11* show the effect of resistively offsetting the voltage applied to pin 9 towards the control reference voltage (pin 19). Because the control inputs are high impedance, this is easily done and high value resistors may be used for minimal additional loading. It is possible to reduce the rate of onset of control to extend the active range to −50 dB volume control and below.

The control on pin 9 may also be divided down towards ground bringing the control action on earlier. This is illustrated in *Figure 12*. With a suitable level shifting network between pins 14 and 9, the onset of loudness control and its rate of change may be readily modified.



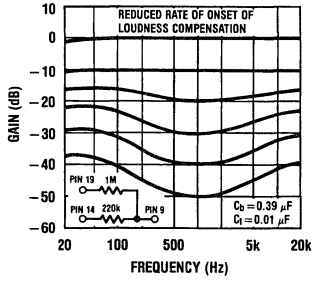
TL/H/5147–12

FIGURE 8. Loudness Compensated Volume Characteristic



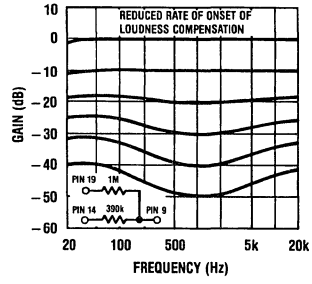
TL/H/5147–13

FIGURE 9. Loudness Compensated Volume Characteristic



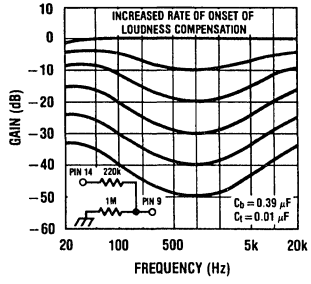
TL/H/5147–14

FIGURE 10. Loudness Compensated Volume Characteristic



TL/H/5147–15

FIGURE 11. Loudness Compensated Volume Characteristic



TL/H/5147–16

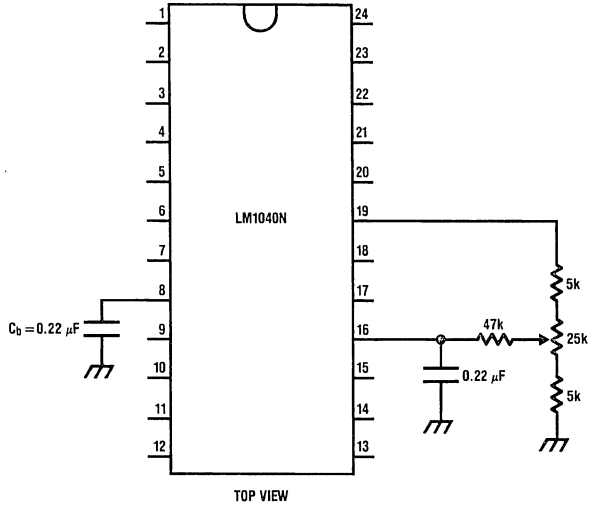
FIGURE 12. Loudness Compensated Volume Characteristic

Applications Information (Continued)

When adjusted for maximum boost in the usual application circuit, the LM-1040 cannot give additional boost from the loudness control with reducing gain. If it is required, some additional boost can be obtained by restricting the tone control range and modifying C_t, C_b, to compensate. A circuit illustrating this for the case of bass boost is shown in *Figure 13*. The resulting responses are given in *Figure 14* showing the continuing loudness control action possible with bass boost previously applied.

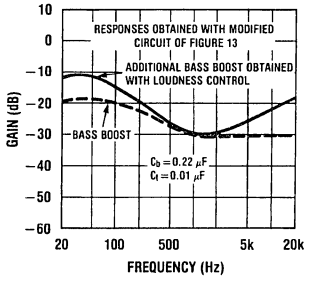
USE OF THE LM1040 ABOVE AUDIO FREQUENCIES

The LM1040 has a basic response typically 1 dB down at 250 kHz (tone controls flat) and therefore by scaling C_b and C_t, it is possible to arrange for operation over a wide frequency range for possible use in wide band equalization applications. As an example *Figure 15* shows the responses obtained centered on 10 kHz with $C_b = 0.039\ \mu F$ and $C_t = 0.001\ \mu F$.



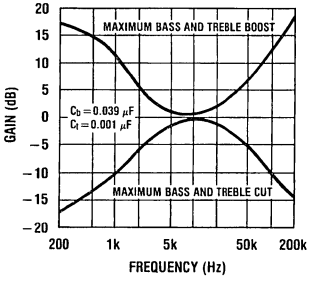
TL/H/5147–17

FIGURE 13. Modified Application Circuit for Additional Bass Boost with Loudness Control



TL/H/5147–18

FIGURE 14. Loudness Compensated Volume Characteristic



TL/H/5147–19

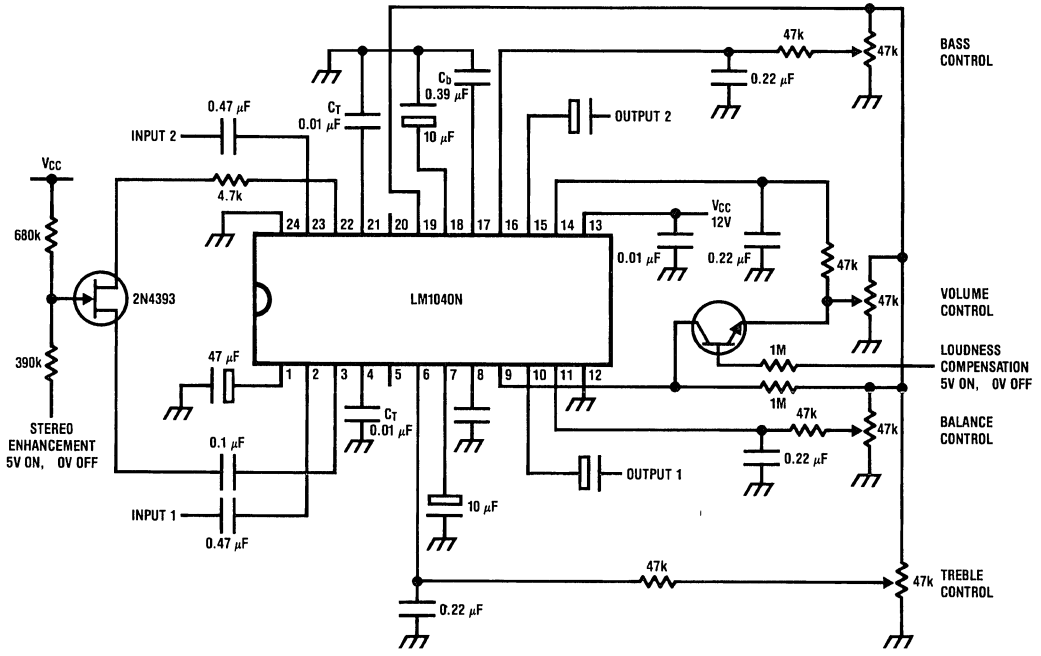
FIGURE 15. Tone Characteristic (Gain vs Frequency)

Applications Information (Continued)

DC CONTROL OF STEREO ENHANCEMENT AND LOUDNESS CONTROL

Figure 16 shows a possible circuit if electronic control of these functions is required. the typical DC level at pins 3 and 22 is 7.5V (V_{CC} = 12V), with the input signal superimposed, and this can be used to bias a FET switch as shown to save components. For switching with a 0V−5V signal a low-threshhold FET is required when using a 12V supply. With larger switching levels this is less critical.

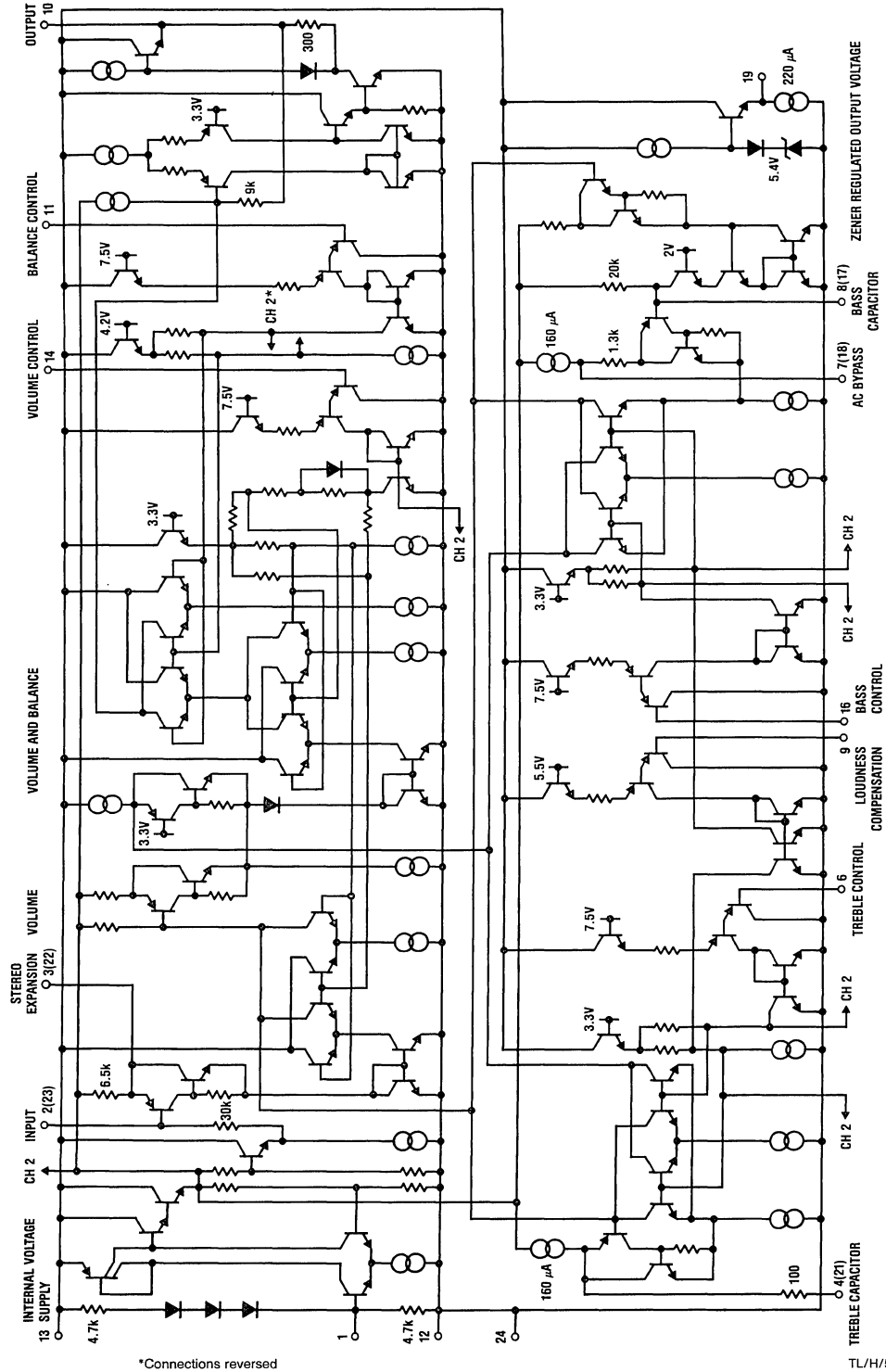
The high impedance PNP base input of the loudness control pin 9 is readily switched with a general purpose NPN transistor.



TL/H/5147–20

FIGURE 16. Application Circuit with Electronic Switching

Simplified Schematic Diagram (One Channel)



National Semiconductor Corporation

LM1112A/LM1112B/LM1112C
Dolby® B-Type Noise Reduction Processor

General Description

The LM1112 is a monolithic integrated circuit specifically designed to realize the Dolby B-type noise reduction system.

It is a replacement for the LM1111 and the Signetics NE-645/648 but with improved performance figures.

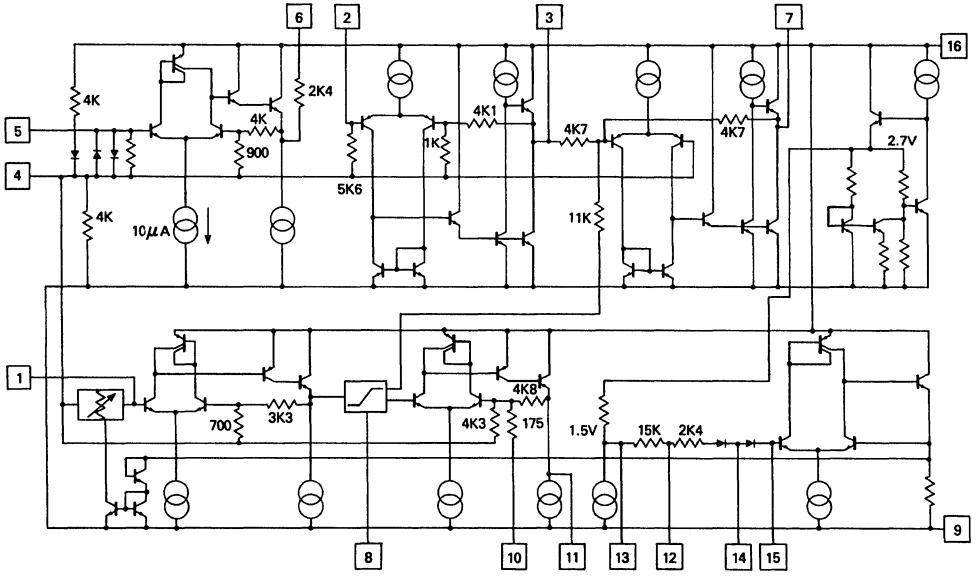
Features

- Very high signal/noise ratio, 74 dB encode (CCIR/ARM)
- Wide supply voltage range, 6V to 20V
- Very close matching to standard Dolby characteristics
- Audible switch-on transients greatly reduced
- Improved temperature performance
- Reduced number of precision external components
- Improved transient stability
- Input protection diodes

Available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.

Dolby and the double-D symbol are registered trademarks of Dolby Laboratories Licensing Corporation.

Schematic Diagram



TL/H/7876–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage 24V

Operating Temperature Range −20°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) 260°C

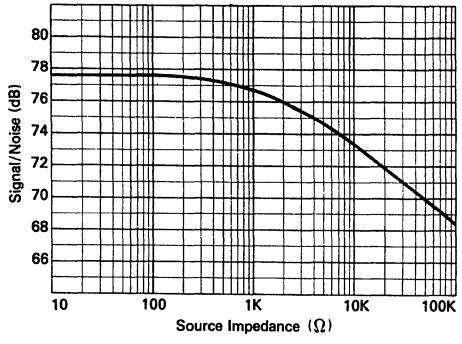
Electrical Characteristics V_S = 12V, T_A = 25°C. 0 dB refers to Dolby level which is 580 mVrms at pin 3.

Parameter	Conditions	LM1112A			LM1112B			LM1112C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		6		20	6		20	6		20	V
Supply Current			15	20		15	20		15	20	mA
Voltage Gain (Pin 5–3)	1 kHz Pins 6 and 12 Connected	24.5	25.5	26.5	24.5	25.5	26.5	24	25.5	27	dB
(Pin 5–6)	1 kHz Pin 6 Open		14.7			14.7			14.7		dB
(Pin 3–7)	1 kHz (Noise Reduction Out)	−0.5	0	0.5	−0.5	0	0.5	−1	0	1	dB
Distortion	1 kHz, 0 dB		0.03	0.1		0.03	0.1		0.03	0.1	%
	10 kHz, +10 dB		0.2			0.2			0.2		%
Signal Handling	1 kHz, 0.3% Distortion										
	V_S = 6V		8.5			8.5			8.5		dB
	V_S = 12V	13	15.5		13	15.5		13	15.5		dB
	V_S = 18V		19			19			19		dB
Signal/Noise Ratio at Pin 7 (Note 1)	Pins 6 and 2 Connected										
Encode Mode (CCIR/ARM) NR In	R_S = 10k	71.5	74		71	74		70	74		dB
	R_S = 1k		77			77			77		dB
NR Out	R_S = 10k		83			83			83		dB
Decode Mode (CCIR/ARM)	R_S = 10k		83			83			83		dB
Encode Characteristics	Input to Pin 5 10 kHz, 0 dB	0	0.5	1.0	−0.2	0.5	1.2	−0.5	0.5	1.5	dB
	1.3 kHz, −20 dB	−16.2	−15.7	−15.2	−16.7	−15.7	−14.7	−17.2	−15.7	−14.2	dB
	5 kHz, −20 dB	−17.3	−16.8	−16.3	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	3 kHz, −30 dB	−21.7	−21.2	−20.7	−22.2	−21.2	−20.2	−22.7	−21.2	−19.7	dB
	5 kHz, −30 dB	−22.3	−21.8	−21.3	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	10 kHz, −30 dB	−24.0	−23.5	−23.0	−24.5	−23.5	−22.5	−25.0	−23.5	−22.0	dB
	10 kHz, −40 dB	−30.1	−29.6	−29.1	−30.3	−29.6	−28.9	−30.6	−29.6	−28.6	dB
Input Resistance	Pin 5	45	65	80	45	65	80	45	65	80	kΩ
	Pin 2	4.3	5.6	6.9	4.3	5.6	6.9	4.3	5.6	6.9	kΩ
Output Resistance	Pin 6	1.8	2.4	3.0	1.8	2.4	3.0	1.8	2.4	3.0	kΩ
	Pin 3		30	45		30	45		30	45	Ω
	Pin 7		30	45		30	45		30	45	Ω
PSRR	f = 120 Hz		40			40			40		dB
Load Impedance Pin 3		5			5			5			kΩ
Pin 7		5			5			5			kΩ

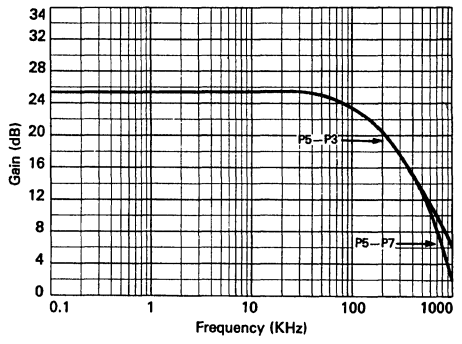
Note 1: Gaussian noise, measured over a period of 50 ms with a CCIR filler and an average responding meter.

Typical Performance Characteristics

Signal/Noise Ratio vs Source Impedance Encode Mode (CCIR/ARM)

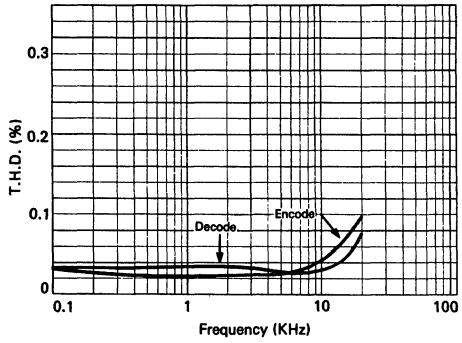


Gain vs Frequency (NR OFF)

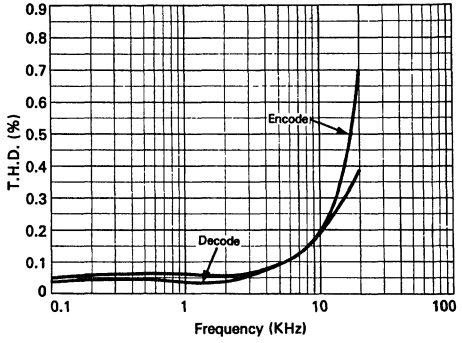


TL/H/7876–2

Total Harmonic Distortion — 0 dB Level

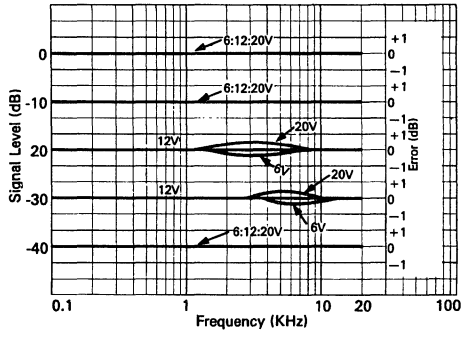


Total Harmonic Distortion — +10 dB Level

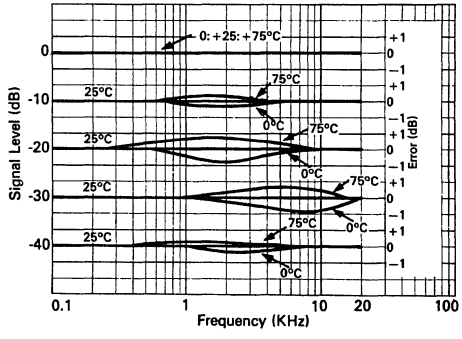


TL/H/7876–3

Back to Back Response Error vs Frequency and Supply Voltage (Standard Dolby Encoder)



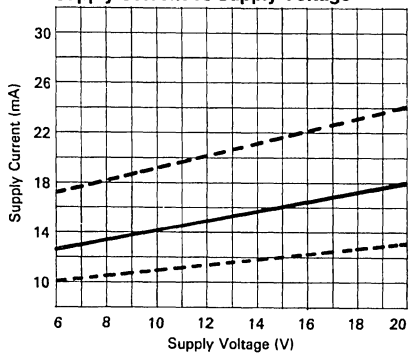
Back to Back Response vs Frequency and Temperature (Encoder Temperature 25°C)



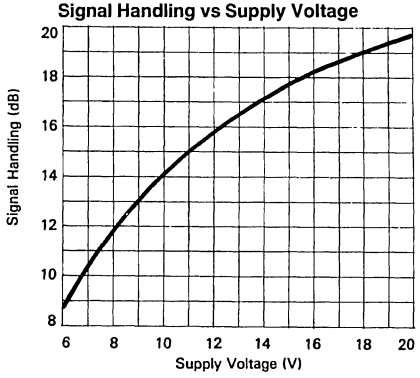
TL/H/7876–4

Typical Performance Characteristics (Continued)

Supply Current vs Supply Voltage



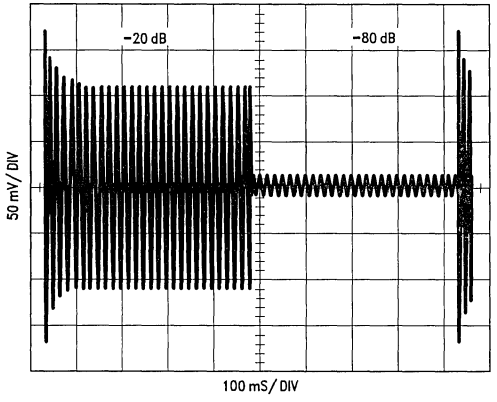
Signal Handling vs Supply Voltage



TL/H/7876–5

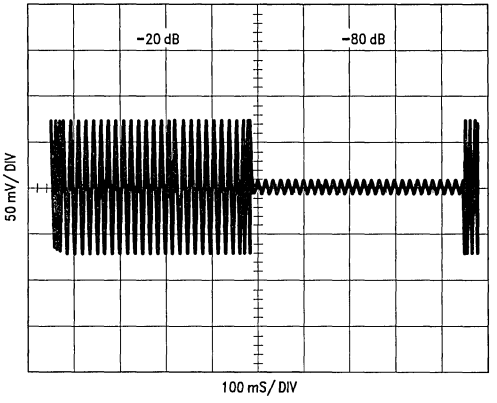
TRANSIENT RESPONSE TO ABRUPT LEVEL CHANGE (Measured at pin 7)

(a) Encode (f = 5 kHz)



TL/H/7876–6

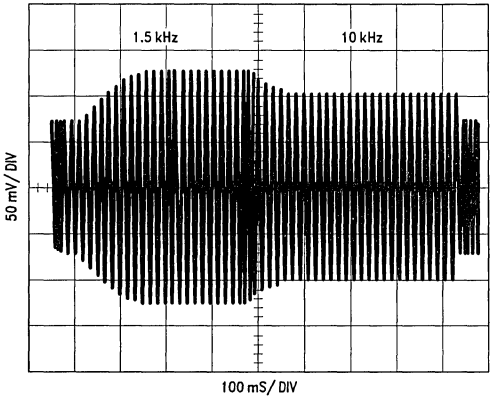
(b) Encoded and Decoded (f = 5 kHz)



TL/H/7876–7

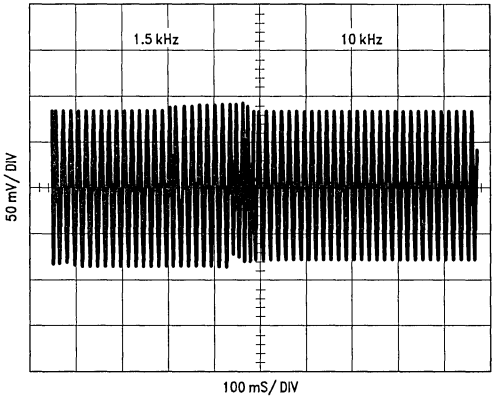
TRANSIENT RESPONSE TO ABRUPT FREQUENCY CHANGE (Measured at pin 7)

(a) Encode (−20 dB)



TL/H/7876–8

(b) Encoded and Decoded (−20 dB)

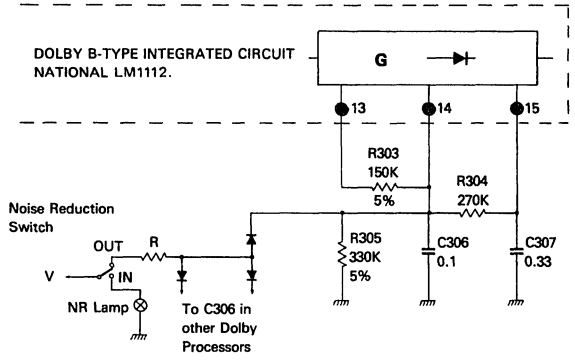


TL/H/7876–9

ELECTRICAL NOISE REDUCTION SWITCH

In place of the normal mechanical noise reduction on/off switch, the circuit below is often used to permit electrical NR control. When using this circuit, the following points should be noted:

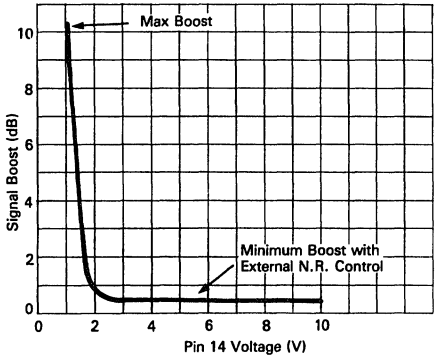
1. Signal boost is reduced by increasing DC voltage on Pin 14 (see curve). A voltage of approximately 3V is adequate to achieve NR OFF.
2. Supply current may be significantly increased by high pin 14 forced voltages. Values for V and R should thus be chosen such that pin 14 voltage is 3V–4V.
3. When electrical NR switching is used, signal level is slightly affected by the minimum value of the internal variable impedance. (At 10 kHz–10 dB, a residual boost of approximately 0.4 dB remains.) This is not the case for mechanical NR switching.



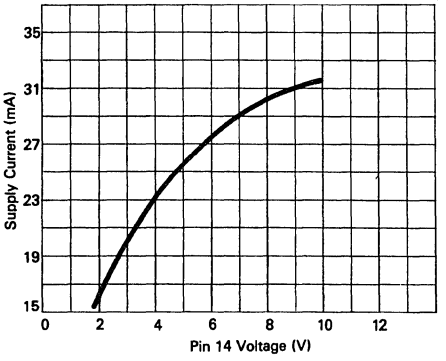
TL/H/7876–10

Note 1: Where not otherwise specified, component tolerances are ±10%.

Signal Boost vs Pin 14 Control Voltage (Encode, 10 kHz)

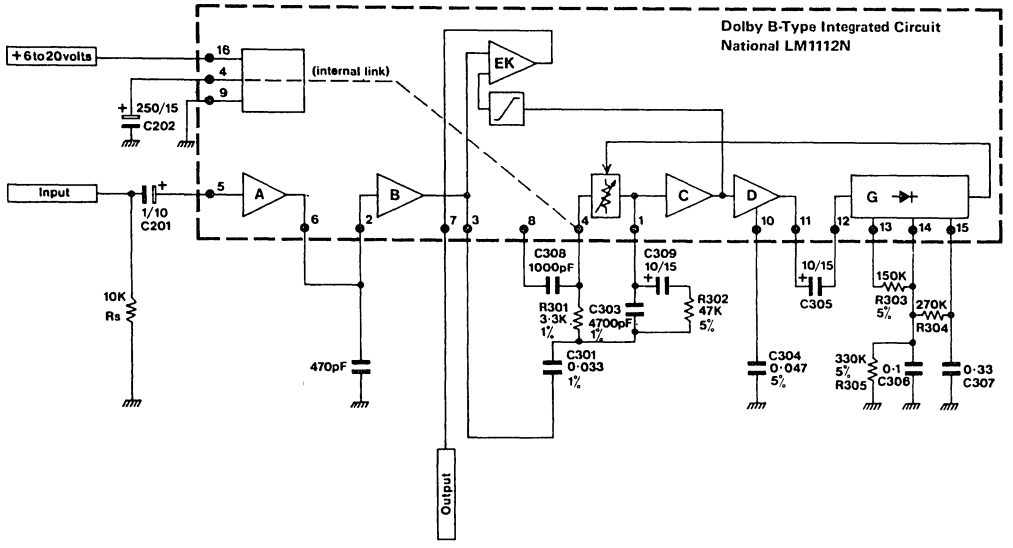


Supply Current vs Pin 14 Control Voltage (V_S = 12V) (Encode, 10 kHz)



TL/H/7876–11

Test Circuit (Encode)



TL/H/7876–12

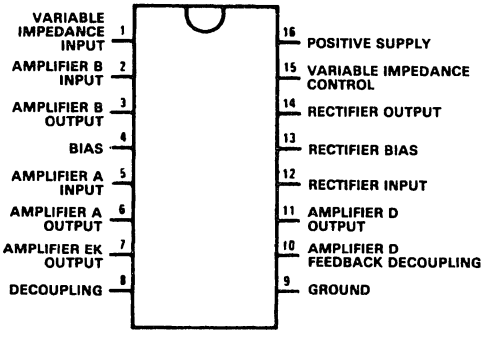
Note 1: 1 nF capacitors from pin 3 and pin 7 to ground may be required on older devices.

Note 2: Where not otherwise specified, component tolerances are ±10%.

Note 3: For LM1112AN use 2% components for C304, R303, R305. (5% components may cause errors up to +0.3 dB.)

Connection Diagram

Dual-In-Line Package



TL/H/7876–13

Order Number LM1112AN, LM1112BN or LM1112CN
See NS Package Number N16E

National Semiconductor Corporation

LM1131A/LM1131B/LM1131C
Dual Dolby® B-Type Noise Reduction Processor

General Description

The LM1131 is a monolithic integrated circuit specifically designed to realize the Dolby B-Type noise reduction system.

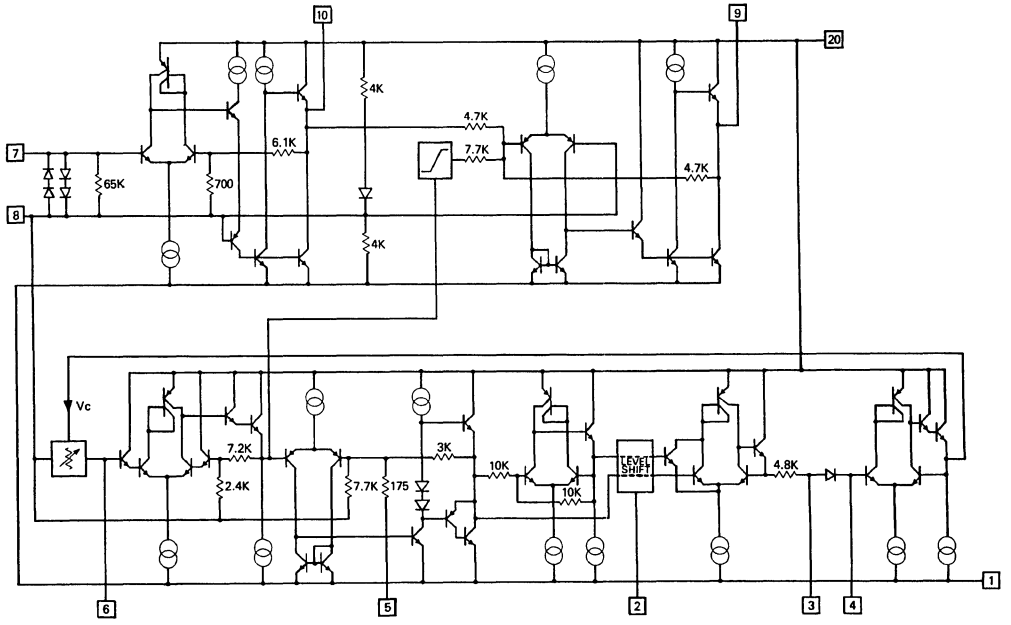
The circuit includes two completely separate noise reduction processors and will operate in both encode and decode modes. It is ideal for stereo applications in compact equipment or for mono applications in 3-head equipment where two processors with very closely matched internal gains are required.

Features

- Stereo Dolby noise reduction with one IC
- Wide supply voltage range, 5V–20V
- Very high signal/noise ratio, 79 dB encode, 90 dB decode (CCIR/ARM)
- Very close gain matching for 3-head recorders
- Close matching to standard Dolby characteristics
- Very low temperature drift of Dolby characteristics
- High signal handling capability, $> +20$ dB (V_S = 20V)
- Full-wave rectifier in both channels
- Operates with both single and split supply voltages
- Excellent transient response characteristics
- Minimal input switch-on transients
- Reduced number of external components per channel
- Improved input protection

Available to licensees of Dolby Laboratories Licensing Corporation, San Francisco, from whom licensing and application information must be obtained.

Schematic Diagram (1 channel shown only)



TL/H/6858–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	24V
Operating Temperature Range	−20°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics

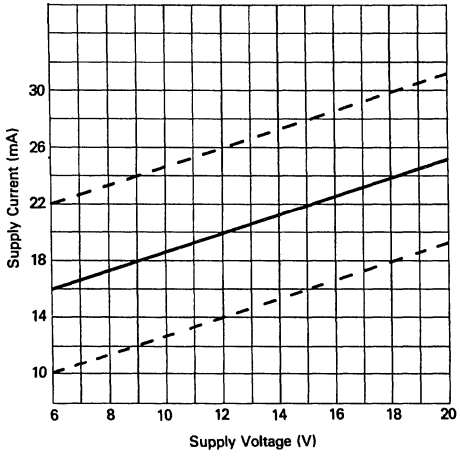
V_S = 12V, T_A = 25°C unless otherwise specified. 0 dB refers to Dolby level and is 580 mV, measured at TP1 and TP2.

Parameter	Conditions	LM1131A			LM1131B			LM1131C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		5		20	5		20	5		20	V
Supply Current			20			20		20			mA
Voltage Gain											
(Pins 7-10 and 14-11)	1 kHz Decode	19.2	19.7	20.2	18.7	19.7	20.7	18.2	19.7	21.2	dB
(Pins 10-9 and 11-12)	1 kHz Decode	−0.5	0	0.5	−0.5	0	0.5	−1.0	0	1.0	dB
Difference in Voltage	1 kHz Noise	−0.2	0	0.2	−0.5	0	0.5	−1.0	0	1.0	dB
Gain between Channels	Reduction OFF										
Crosstalk between Channels	1 kHz, 0 dB	−60	−90		−60	−90		−60	−90		dB
Signal/Noise Ratio at Pins 9 and 12	(Note 1)										
Encode	R_S = 10 kΩ	77	79		75.5	79		74	79		dB
	R_S = 1 kΩ		82			82			82		dB
Decode	R_S = 10 kΩ		90			90			90		dB
	R_S = 1 kΩ		92			92			92		dB
Encode Characteristics	10 kHz, 0 dB	0	0.5	1.0	0.2	0.5	1.2	−0.5	0.5	1.5	dB
	1.3 kHz, −20 dB	−16.2	−15.7	−15.2	−16.7	−15.7	−14.7	−17.2	−15.7	−14.2	dB
	5 kHz, −20 dB	−17.3	−16.8	−16.3	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	3 kHz, −30 dB	−21.7	−21.2	−20.7	−22.2	−21.2	−20.2	−22.7	−21.2	−19.7	dB
	5 kHz, −30 dB	−22.3	−21.8	−23.0	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	10 kHz, −40 dB	−30.1	−29.6	−29.1	−30.3	−29.6	−28.9	−30.6	−29.6	−28.6	dB
Variation in Encode Characteristics											
Temperature	0°C–70°C		< ±0.5			< ±0.5			< ±0.5		dB
Voltage	5V–20V		< ±0.2			< ±0.2			< ±0.2		dB
Distortion	1 kHz, 0 dB		0.03	0.1		0.03	0.1		0.03	0.2	%
	10 kHz, 10 dB		0.2			0.2			0.2		%
Signal Handling	1 kHz, Dist = 0.3%										
	V_S = 5V		6.5			6.5			6.5		dB
	V_S = 7V		10.5			10.5			10.5		dB
	V_S = 12V	14.0	16.0		14.0	16.0		14.0	16.0		dB
	V_S = 20V		21.0			21.0			21.0		dB
Input Resistance	Pins 7 and 14	45	65	80	45	65	80	45	65	80	kΩ
Output Resistance	Pins 9 and 12		30	55		30	55		30	55	Ω
	Pins 10 and 11		30	55		30	55		30	55	Ω

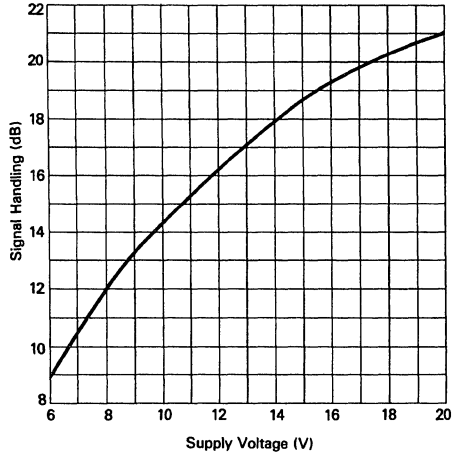
Note 1: Gaussian noise, measured over a period of 50 ms per channel, with a CCIR filter referenced to 2 kHz and an average-responding meter.

Typical Performance Characteristics

Supply Current vs Supply Voltage (1 kHz, 0 dB; NR ON)

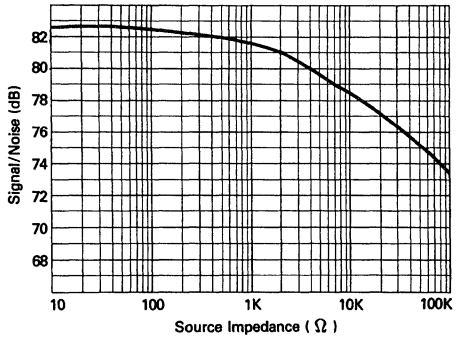


Signal Handling vs Supply Voltage

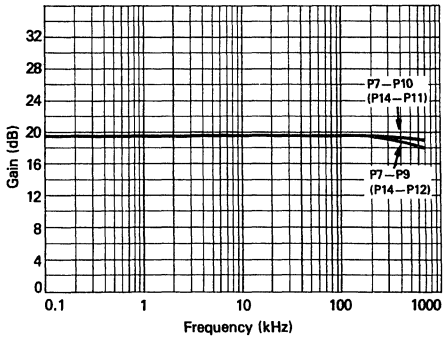


TL/H/6858–2

Signal to Noise Ratio vs Source Impedance Encode Mode (CCIR/ARM)

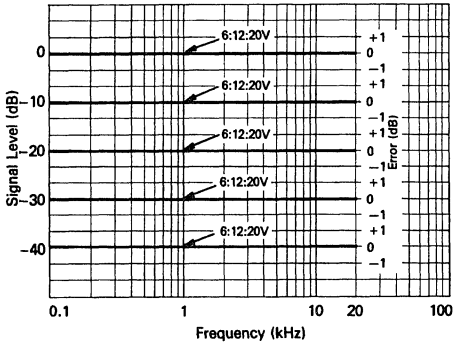


Gain vs Frequency (NR OFF)

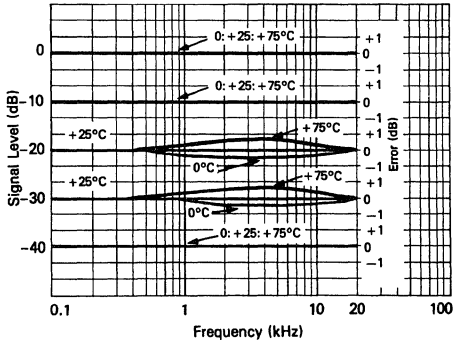


TL/H/6858–3

Back to Back Response Error vs Frequency and Supply Voltage (Standard Dolby Encoder)



Back to Back Response Error vs Frequency and Temperature (Encode Temperature + 25°C)



TL/H/6858–4

Application Notes

SUPPLY VOLTAGE

LM1131 may operate with either single or split supply voltages.

Single Supply Voltage

Pin 1 is connected to ground, pin 20 to V_S.

Pins 8 and 13 are internally generated reference voltages set to approximately half-supply. They should be connected together externally.

A 220 μF capacitor must be connected between pins 8 and 13 and ground. Device turn-on time is delayed by the rise time of pins 8 and 13.

Split Supply Voltages

Pin 1 is connected to the negative supply, pin 20 to the positive supply. Pins 8 and 13 are connected to 0V and no capacitor is required. Device turn-on time is delayed only by the rise times of the supply voltages.

SIGNAL GAIN AND FILTERING

It should be noted that LM1131 has only one internal preamplifier, AB, with no provision for interconnection of a low pass filter to remove bias or multiplex tones. In addition, main chain gain has been reduced by 6 dB in comparison with LM1112/LM1011.

If a low pass filter is required it should be connected at the input of the LM1131. Pre-adjustment of Dolby input level may then be performed, at the input of LM1131 if required.

NOISE REDUCTION SWITCH

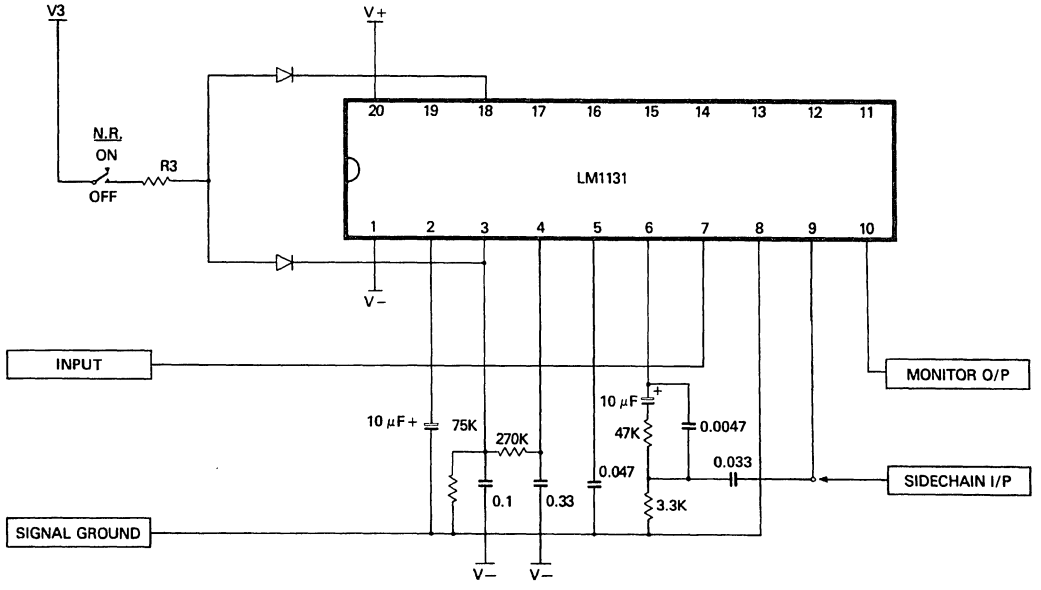
Noise reduction OFF is normally effected by means of a mechanical switch which open-circuits the sidechain input.

An alternative method which permits the control of NR OFF by means of a DC voltage is shown in *Figure 1*. The DC control voltage forces the internal impedance to a minimum value and heavily attenuates the sidechain input. When using this circuit the following points should be noted:

a) Signal boost in encode mode (signal cut in decode) is reduced by increasing DC voltages on pins 3 and 18. A voltage of approximately 3V above signal ground is adequate to achieve NR OFF.

b) Supply current may be increased significantly by high pin 3/18 forcing voltages. Thus, values for V3 and R3 should ideally be chosen such that pin 3/18 forced voltage is only 3V–5V greater than signal ground. Maximum permissible voltage on pin 3/18 is equal to supply voltage.

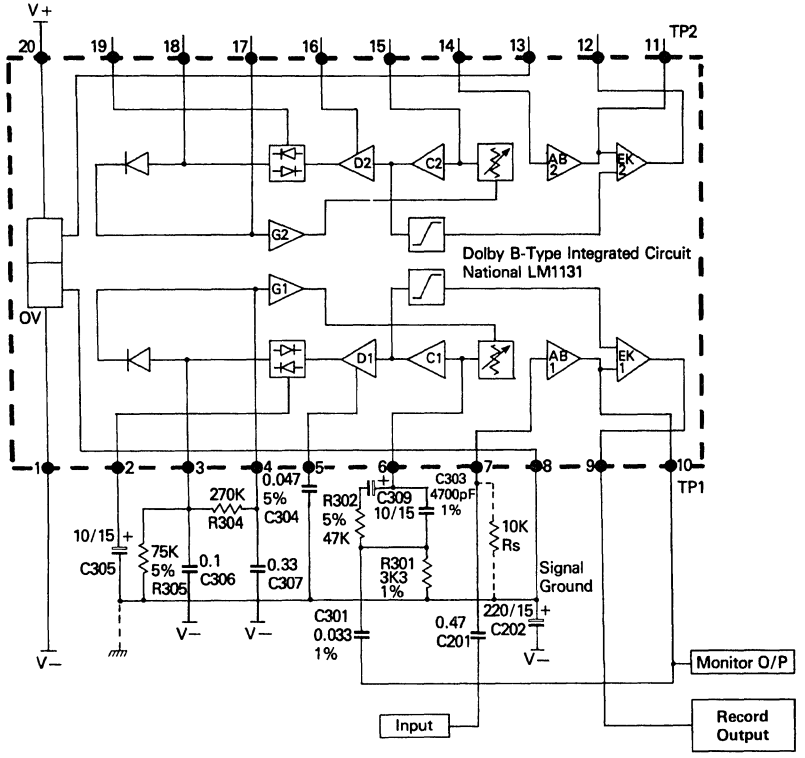
c) When electrical NR switching is used in this way, NR OFF signal level is slightly affected by the restriction that the internal variable impedance cannot achieve zero impedance. Thus, at 10 kHz–10 dB, a residual boost in encode (or cut in decode) of approximately 0.4 dB remains. At low frequencies this value reduces to insignificant levels. This is not the case for mechanical NR switching.



TL/H/6858–5

FIGURE 1. LM1131 Decode Processor with Electrical NR Switch (1 Channel Shown)

Test Circuit Encode Mode (components shown for channel 1 only)



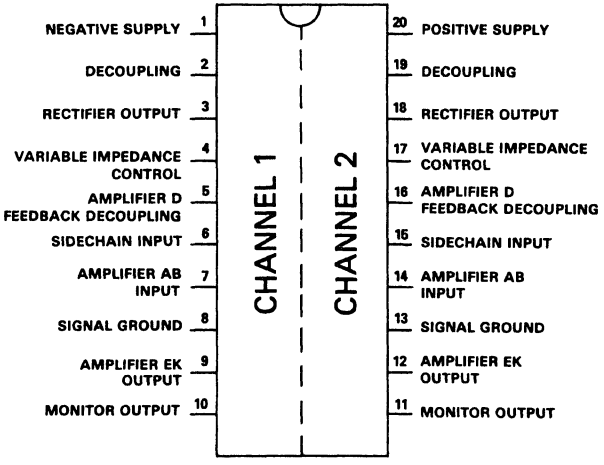
Note 1: Where not otherwise specified component tolerances are ±10%

Note 2: For LM1131AN use 2% components for C304, R303, R305. (5% components may cause errors up to ± 0.3 dB).

TL/H/6858–6

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/6858–7

Order Number LM1131AN, LM1131BN, LM1131CM or LM1131CN
See NS Package Number M20B or N20A

National Semiconductor Corporation

LM1141 Dolby B-C Type Noise Reduction Processor

General Description

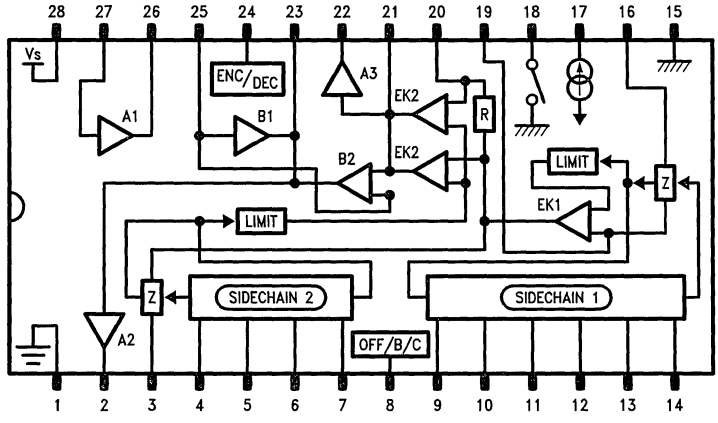
The LM1141 is a monolithic integrated circuit specifically designed to realise both Dolby B- and Dolby C-type noise reduction systems*. The circuit has a single input pin for Encode and Decode and includes all active components and switching internally to provide a single channel of a Dolby B- or Dolby C-type system. The low power consumption and compact package design make it ideal for use in automotive and portable Hi-Fi as well as quality cassette or tape sound systems.

*Available only to licensees of Dolby Laboratories Licensing Corporation. Dolby and the double D symbol are registered trademarks of Dolby Laboratories Licensing Corp.

Features

- Very low supply current (11.5 mA typ.)
- Wide supply voltage range, 5–16V
- Alternative Dolby levels, 245 mV or 580 mV
- Provision for MPX filter
- Very high signal to noise ratio, 66 dB typ. for encode, C mode CCIR/ARM
- 50 mV encode input sensitivity (30 mV decode)
- D.C.-controlled mode switching
- Minimal switching transients
- 28 pin DIP or QUAD packages available

Block Diagram



TL/H/9242–1

Order Number LM1141N or LM1141V
See NS Package Number N28B or V28A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, Vs 17V

Input Voltage, Encode/Decode Vs

Input Voltage, Switching +Vs + 0.5V
−Vs − 0.3V

Soldering Information
Dual-In-Line Package
Soldering (10 seconds) ..... 260°C
Plastic Chip Carrier Package
Vapor Phase (60 seconds) ..... 215°C
Infrared (15 seconds) ..... 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Temperature Range 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Package Dissipation @ T_A = 25°C (Note 1) LM1141N = 2.5W, LM1141V = 1.7W

ESD rating is to be determined.

Electrical Characteristics

Vs = 12V, T_A = 25°C unless otherwise stated.

0 dB refers to Dolby level which is 245 mV measured at Encode Output 1 with NR OFF.

Note: Encode input sensitivity = 50 mV, Decode input sensitivity = 30 mV

Parameter	Conditions	Test Limit Note 2		Design Limit Note 3			Units
		Min	Max	Min	Typ	Max	
Supply Voltage	Min Signal Handling = 12 dB at Encode O/P 1	5	16				V
Supply Current	Encode, NR OFF, No signal		16		11.5		mA
Voltage Gain (Note 4)	Encode O/P 1, NR OFF	12.5	15.1		13.8		dB
	Encode O/P 2, NR OFF	19.8	22.8		21.3		dB
	Decode O/P 1, NR OFF	16.9	19.5		18.2		dB
	Decode O/P 2, NR OFF	24.2	27.2		25.7		dB
Input Resistance	Encode/Decode Input	35	80		55		kΩ
Signal To Noise Ratio (Note 5)	Encode O/P 1 or 2, Rs = 5.6 kΩ C Mode			62	66		dB
	C.C.I.R./A.R.M B Mode			70	76		dB
	Decode O/P 1 or 2, Rs = 5.6 kΩ, NR OFF			78	84		dB
Signal handling	Enc O/P 1, Dec O/P 1, 1 kHz Vs = 5V, NR OFF, 1% T.H.D.	12			13		dB
	Enc O/P 2, Dec O/P 2, 1 kHz Vs = 9V, NR OFF, 1% T.H.D.	12			13		dB
Distortion (T.H.D.)	Encode O/P2, C Mode 0 dB, 1 kHz				0.05	0.15	%
	Decode O/P2, C Mode 0 dB, 1 kHz				0.04	0.15	%
Encode Characteristics	B Mode, 5 kHz, 0 dB			−1.2	0.3	1.8	dB
	B Mode, 1 kHz, −20 dB			2.7	4.2	5.7	dB
	B Mode, 5 kHz, −30 dB	6.7	9.7		8.2		dB
	B Mode, 1 kHz, −40 dB	4.7	7.7		6.2		dB
	C Mode, 10 kHz, −0 dB			−5.5	−3.5	−1.5	dB
	C Mode, 1 kHz, −20 dB			3.9	5.9	7.9	dB
	C Mode, 5 kHz, −30 dB	6.4	10.4		8.4		dB
	C Mode, 1 kHz, −40 dB	14.2	18.2		16.2		dB
Control Voltage	Encode Mode		0.8	0			V
	Decode Mode	2.0				Vs	V
	B Mode		0.8	0			V
	Off Mode	2.0	3.2		Open		V
	C Mode	4.6				Vs	V

Note 1: Above T_A = 25°C, derate with θ_{ja} = 50°C/W (LM1141N)
75°C/W (LM1141V)
Tj max = 150°C

Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 4: The resistors at the input and output of the MPX Filter are required to match the characteristic impedance of the filter block. The values shown correspond to the most commonly used filter for this application. Values should be checked for each individual application. If no filter is used, a 3.1 dB attenuation pad should be retained for correct operation of the processor.

Note 5: Gaussian noise, monitored over a period of 50 ms with a CCIR filter and an average-responding meter.

Pin Function Description

PIN 1. Negative supply voltage, −Vs.

PIN 2. High level decode (playback) output, (580 mV).

PIN 3. Connection to the variable impedance of sidechain 2. A capacitor is connected between this pin and signal ground to give a variable high pass filter characteristic, controlled by the sidechain.

PIN 4. A capacitor is connected between this pin and signal ground to provide pre-emphasis at amplifier D in sidechain 2.

PIN 5. A capacitor is connected between this pin and signal ground which decouples the feedback components of amplifier D of sidechain 2, and reduces system offsets.

PIN 6/7. Sidechain 2 transient response circuit.

PIN 8. Selects OFF, B or C mode depending on the d.c. voltage applied.

PIN 9/10. These pins are connected internally to low saturation switching transistors and externally to the transient response circuit of sidechain 1 in such a way that in C-mode the capacitor values are reduced.

PIN 11/12 Sidechain 1 transient response circuit.

PIN 13. A capacitor is connected between this pin and signal ground to provide pre-emphasis at amplifier D in sidechain 1.

PIN 14. A capacitor is connected between this pin and signal ground which decouples the feedback components of amplifier D of sidechain 1, and reduces the system offsets.

PIN 15. Signal ground, set internally to approximately half the supply voltage.

PIN 16. Connection to the variable impedance of sidechain 1. A capacitor is connected between this pin and signal ground to give a variable high pass filter characteristic, controlled by the sidechain.

PIN 17. A resistor is connected between this pin and −Vs. This sets up an accurate current required for correct maximum impedance filter characteristics.

PIN 18. This pin is connected internally to a low saturation switching transistor and is energised to switch on the Spectral Skewing circuit in C-mode.

PIN 19. The Spectral Skewing circuit is connected to this pin.

PIN 20. The Anti-Saturation circuit is connected to this pin.

PIN 21. Low level encode (record) output (245 mV).

PIN 22. High level encode (record) output (580 mV).

PIN 23. Low level decode (playback) output (245 mV).

PIN 24. Selects encode or decode mode depending on the d.c. voltage applied.

PIN 25. MPX filter output.

PIN 26. MPX filter input.

PIN 27. Signal input (encode and decode).

PIN 28. Positive supply voltage, +Vs.

Typical Applications

Selection of encode/decode and off/B/C is achieved by applying the required d.c voltage to the appropriate control pin. *Figures 1* and *2* show the relationship between the applied voltage and the mode selected.

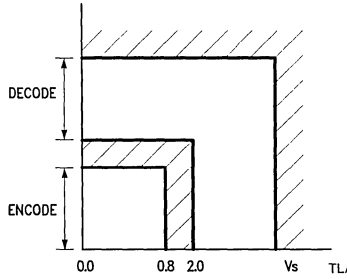
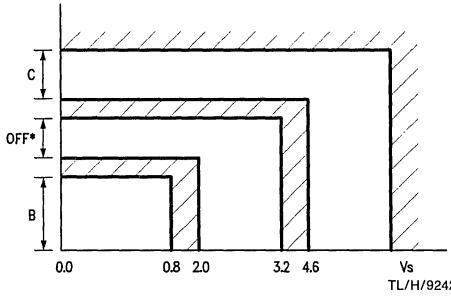


FIGURE 1. Pin 24 control voltage (V).



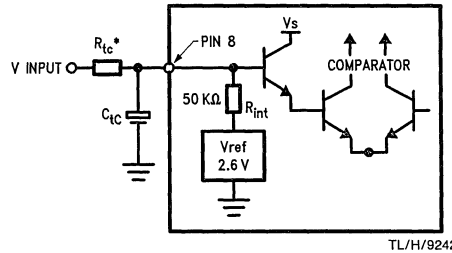
* Pin 8 open also gives Off mode.

FIGURE 2. Pin 8 control voltage (V).

Although audible switching pops have been reduced to a minimum, further improvement may be achieved by including an R-C time constant on the switching pins.

The values chosen for the R-C circuit connected to the OFF-B-C switching pin (8) are important in order that the switching circuitry functions correctly.

The internal configuration at pin 8 includes connection to a darlington input stage comparator and a 2.6V voltage reference via a resistor of value 50 kΩ, (see *Figure 3*) which allows selection of OFF mode when pin 8 is open-circuited, (See specification).



*R_{tc} max = 5 kΩ for 5V operation.

FIGURE 3

The capacitor C_{tc} affects the switching time when selecting OFF-mode (pin 8 open) from C mode. The discharge path is now via the 50 kΩ resistor to Vref, hence the switching time

Typical Applications (Continued)

is a function of $R_{int}C$. The Encode/Decode switching pin (24) is unaffected by the connection of a similar R-C network.

Connection of Supply Voltage

The device may be operated in either single ended or dual supply modes, since the internally generated bias voltage (pin 15) is approximately half the supply voltage.

For single supply applications a large electrolytic capacitor (200 μF) should be connected between pin 15 and $-$Vs.

For dual supply operation this capacitor is not required and pin 15 can be connected to 0v directly.

Sidechain Variable High Pass Filters

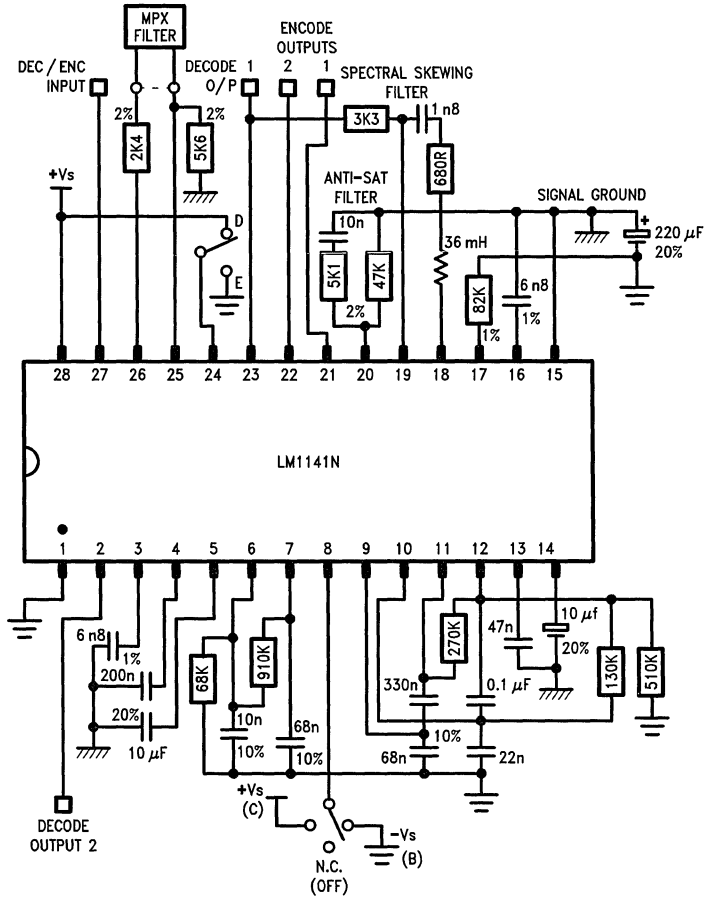
In encode mode the boost characteristics are controlled by the variable impedances of the sidechains in conjunction with external capacitors and a resistor forming a variable high pass filter.

The capacitors and the resistor (on pin 17 and common to both sidechains) must be accurate and of high stability (a tolerance of 1% is recommended).

Typical Connection Diagram for 5V to 9V Supply

(All external components 5% unless otherwise stated.)

*MPX Filter, See note 4 in General Notes.



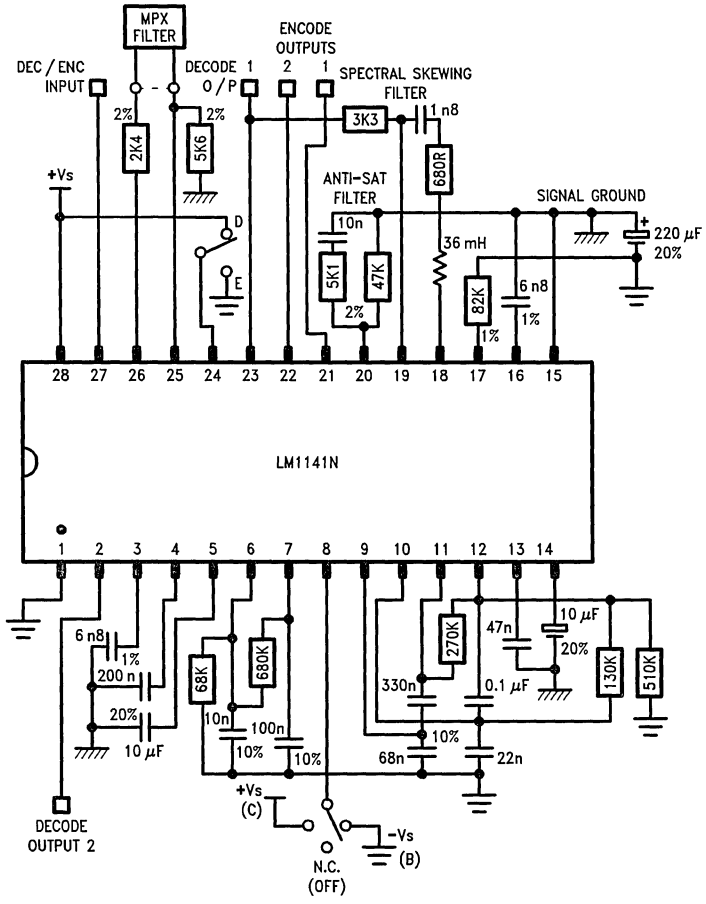
TL/H/9242–5

Device also available in 28 pin quad chip carrier package.

Typical Connection Diagram for 8V to 16V Supply

(All external components 5% unless otherwise stated.)

*MPX Filter, See note 4 in General Notes.



TL/H/9242–6

Device also available in 28 pin quad chip carrier package.

National Semiconductor Corporation

LM1818 Electronically Switched Audio Tape System

General Description

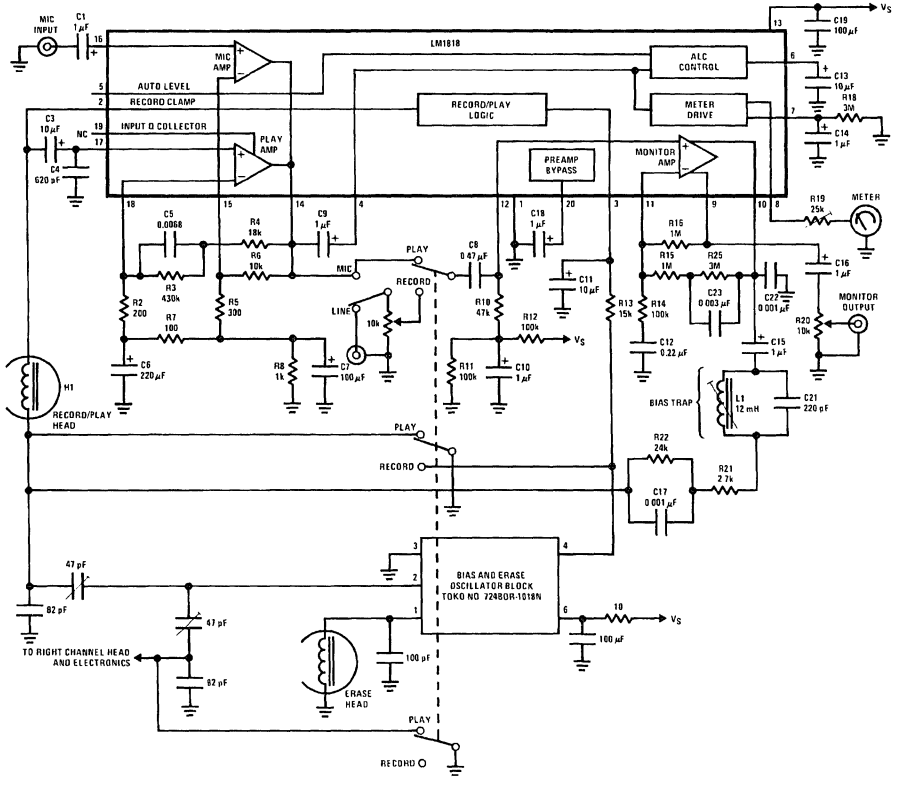
The LM1818 is a linear integrated circuit containing all of the active electronics necessary for building a tape recorder deck (excluding the bias oscillator). The electronic functions on the chip include: a microphone and playback preamplifier, record and playback amplifiers, a meter driving circuit, and an automatic input level control circuit. The IC features complete internal electronic switching between the record and playback modes of operation. The multipole switch used in previous systems to switch between record and playback modes is replaced by a single pole switch, thereby allowing for more flexibility and reliability in the recorder design.*

*Monaural operation, *Figure 9.*

Features

- Electronic record/play switching
- 85 dB power supply rejection
- Motional peak level meter circuitry
- Low noise preamplifier circuitry
- 3.5V to 18V supply operation
- Provision for external low noise input transistor

Typical Applications



TL/H/7894–1

FIGURE 1. Stereo Application Circuit (Left Channel Shown), V_S = 15V

Order Number LM1818N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	18V
Package Dissipation, (Note 1)	1560 mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	150°C
Minimum Voltage on Any Pin	−0.1 V_{DC}
Maximum Voltage on Pins 2 and 5	0.1 V_{DC}
Maximum Current Out of Pin 14	5 mA_{DC}
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics V_{CC} = 6V, T_A = 25°C, See Test Circuits *(Figures 2* and *3)*

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage Range		3.5		18	V_{DC}
Supply Current	Test Circuit *(Figure 2)*		5	12	mA
Turn-ON Time	Externally Programmable	50	400		ms
Playback Signal to Noise	DIN Eq. (3180 and 120 μs), 20–20 kHz, R_S = 0, Unweighted, V_{REF} = 1 mV at 400 Hz		74		dB
Record Signal to Noise	Flat Gain, 20–20 kHz, R_S = 0, ALC OFF, V_{REF} = 1 mV at 1 kHz, Unweighted		69		dB
Fast Turn-ON Charging Current	Pins 16 and 17		200		μA
Record and Playback Preamplifier Open Loop Voltage Gain	f = 100 Hz		100		dB
Preamplifier Input Impedance	Pin 16 or Pin 17		50		kΩ
Preamplifier Input Referred PSRR	1 kHz — Flat Gain		85		dB
Bias Voltage on Pin 18 in Play Mode or Pin 15 in Record Mode			0.5		V
Monitor Amplifier Input Bias Current	Pins 11 and 12		0.5		μA
Monitor Amplifier Open Loop Voltage Gain	Record or Playback, f = 100 Hz		80		dB
Monitor Output Current Capability	Pins 9 and 10, Source Current Available	400	750		μA
Monitor Amplifier Output Swing	R_L = 10k, AC Load	1.2	1.65		Vrms
THD, All Amplifiers	At 1 kHz, 40 dB Closed Loop Gain		0.05		%
Record-Playback Switching Time	As in Test Circuit		50		ms
Input ALC Range	ΔV_{IN} for ΔV_{OUT} = 8 dB		40		dB
Input Voltage on ALC Pin for Start of ALC Action			25		mVrms
ALC Input Impedance			2		kΩ
ALC Attack Time	C13 = 10 μF		7		ms
ALC Decay Time	R17 = ∞, C13 = 10 μF		30		sec
Meter Output Gain	100 mVrms at 1 kHz into Pin 4		800		mV_{DC}
Meter Output Current Capability		2			mA_{DC}

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

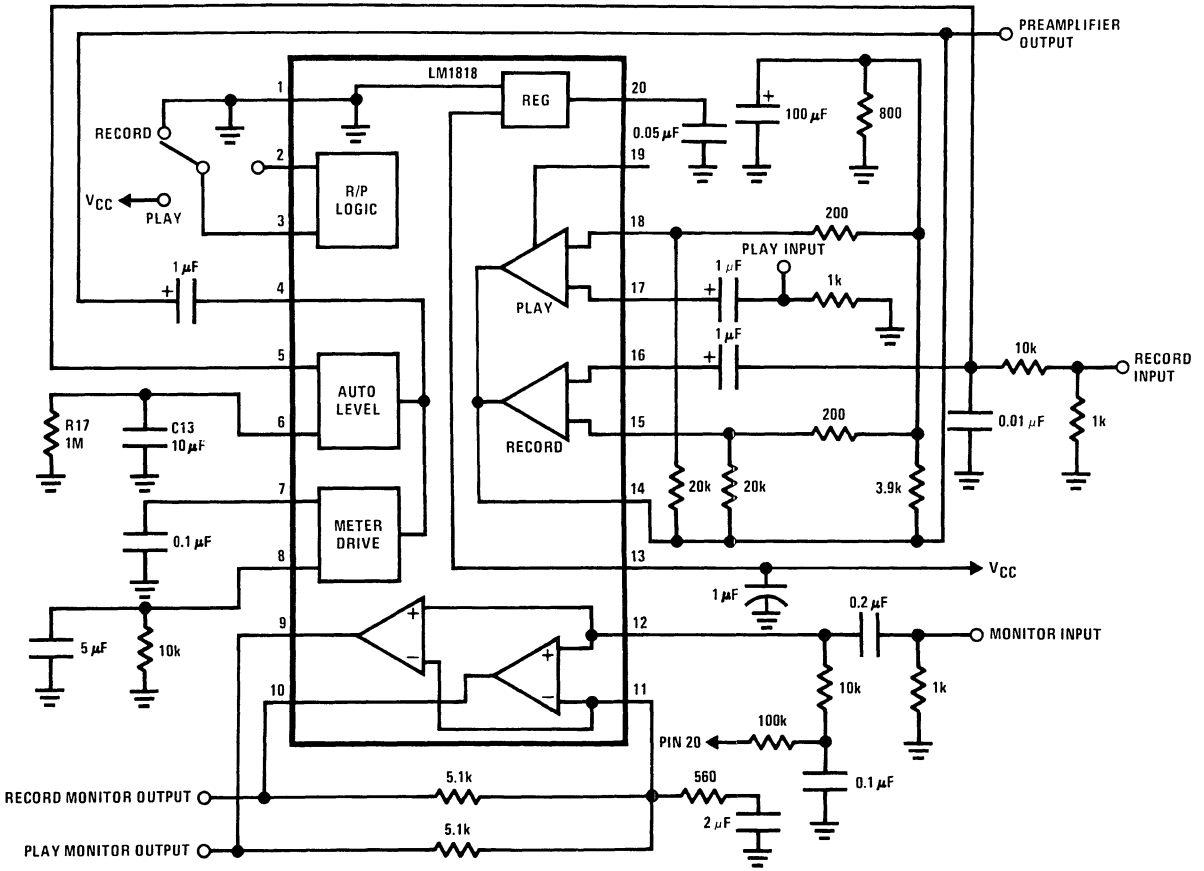


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FIGURE 2. General Test Circuit

Test Circuits (Continued)

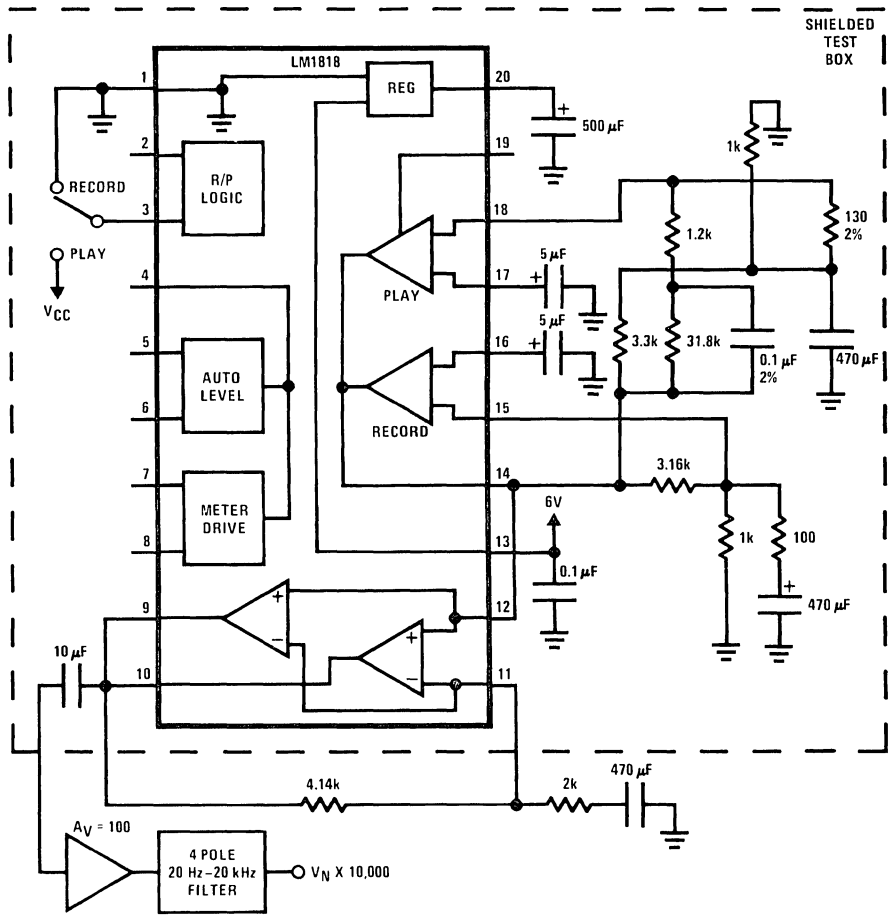

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FIGURE 3. Noise Test Circuit

Equivalent Schematic Diagram

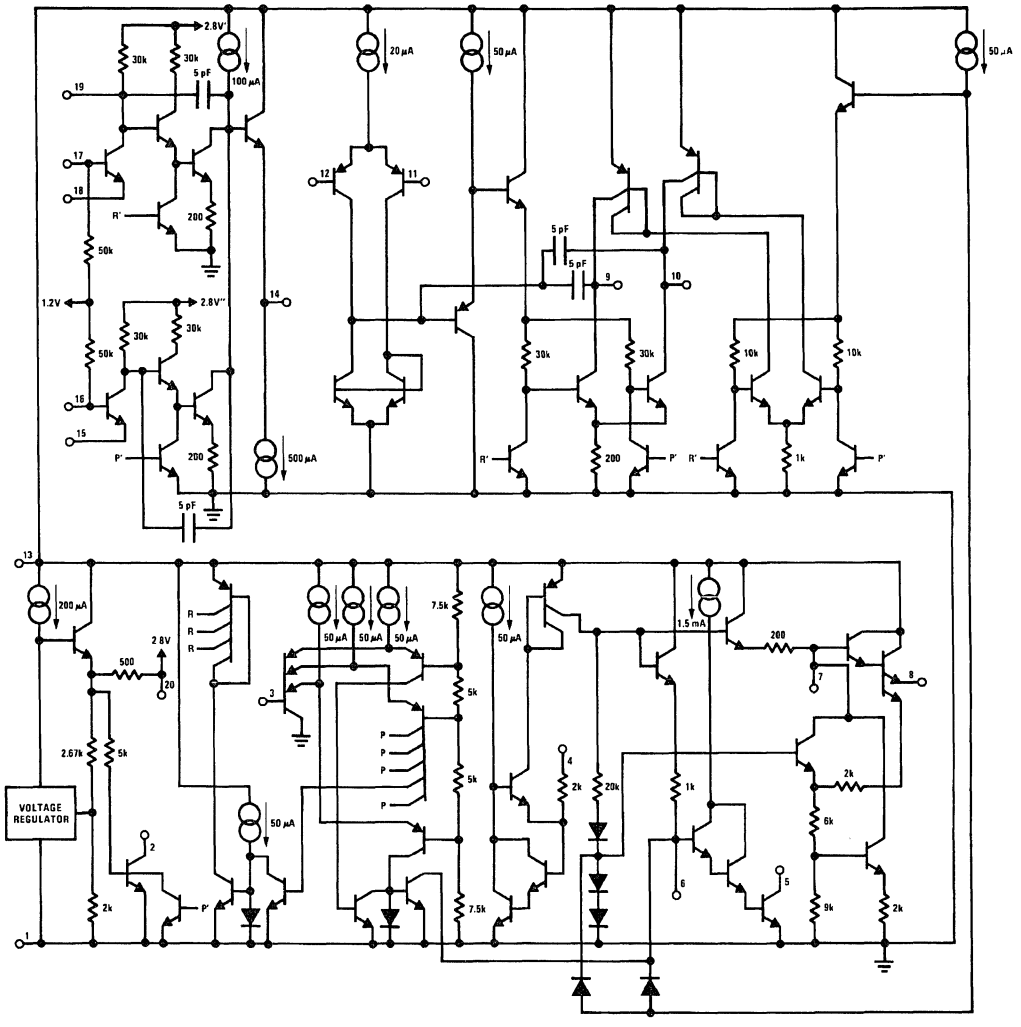

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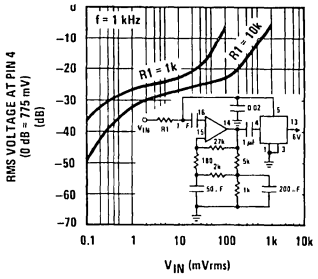
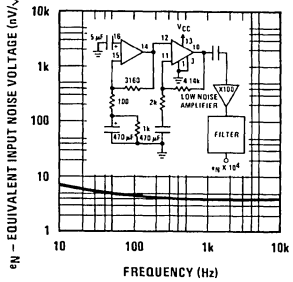
FIGURE 4

Typical Performance Characteristics

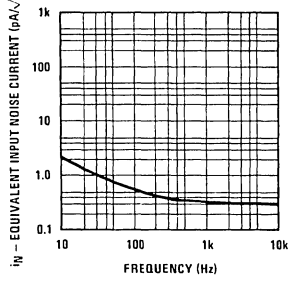
Automatic Level Control (ALC) Response Characteristic



Preamp Input Noise Voltage



Preamp Input Noise Current



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Application Hints

PREAMPLIFIERS *(Figure 5)*

There are 2 identical preamplifiers with 1 common output pin on the IC. One amplifies low level inputs such as a microphone in the record mode and another amplifies the signal from the playback head in the playback mode. The amplifiers use a common capacitor, C6, to set the low frequency pole of the closed loop responses. On the playback amplifier, the collector of the input device is made available so that an external low noise device can be connected in critical applications. When using an external low noise transistor, pins 17 and 18 of the IC are shorted together to ensure that the internal input transistor is turned OFF and the external transistor's collector is tied to pin 19. The input and feedback connections are now made to the external input transistor. The amplifiers are stable for all gains above 5 and have a typical open loop gain of 100 dB. R8 and R9 enable C6 to be quickly charged and set the DC gain. Internal biasing provides a DC voltage independent of temperature at pin 17 so that the preamplifier DC output will remain relatively constant with temperature. Supply decoupling is provided by an internal regulator. Additional decoupling can be added for the input stages by increasing the size of the capacitor on pin 20 of the IC. A fast charging circuit is connected to the preamplifiers' input capacitors (pins 16 and 17) to decrease the turn-ON time. Larger input capacitors decrease the noise by reducing the source impedance at lower frequencies where 1/f noise current produces an input noise voltage. The input resistance of the preamplifiers is typically 50 kΩ.

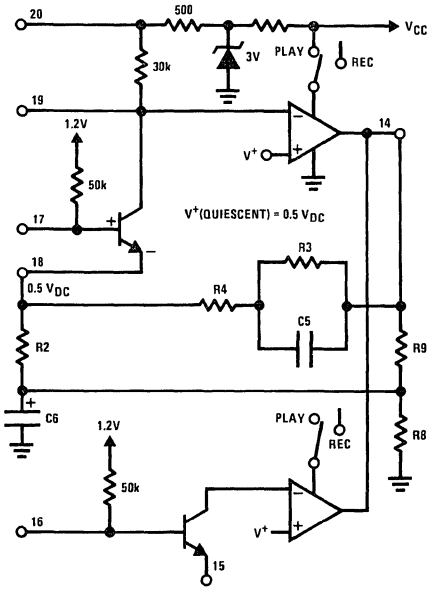

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FIGURE 5. Preamplifier

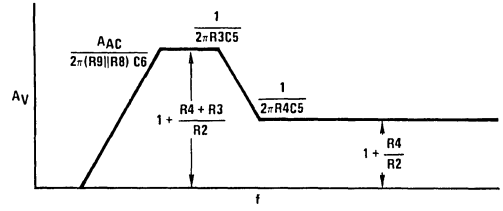
Quiescent DC Output Voltage

$$V_{DC} = \left(1 + \frac{R9}{R8}\right)(0.5 - 50 \times 10^{-6} R2) V \text{ if } R2 + R3 > 10\, R_E$$

where $R_E = \dfrac{R8R9}{R8 + R9}$

AC Voltage Gain

$$A_{AC} = \frac{R4 + \dfrac{R3}{1 + sC5R3}}{R2} + 1$$



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Application Hints (Continued)

MONITOR AND RECORD AMPLIFIERS *(Figure 6)*

The monitor and record amplifiers share common input and feedback connections but have separate outputs. During playback, the input signal is amplified and appears only at the playback monitor output. Because the outputs are separate, different feedback components can be used and, as a result, totally different responses can be set. The amplifiers are stable for all closed loop gains above 3 and have an open loop gain of typically 80 dB. The outputs are capable of supplying a minimum of 400 μA into a load and swing within 500 mV of either V_{CC} or ground. If more than 400 μA is needed to drive a load, an external pull-up resistor on the output of these amplifiers can increase the load driving capability.

AUTOMATIC LEVEL CONTROL—ALC *(Figure 7)*

The automatic level control provides a constant output level for a wide range of record source input levels. The ALC works on the varying impedance characteristic of a saturated transistor. The impedance of the saturated transistor forms a voltage divider with the source impedance of a series resistor (R1 in *Figure 9*). The input signal is decreased as the ALC transistor is increasingly forward biased. The ALC transistor will be forward biased when the preamplifiers's AC output (pin 14), coupled to the combination ALC-meter drive input (pin 4) reaches 40 mV peak (25 mVrms). The gain of the ALC loop is such that a preamp input signal increase of 10 dB will result in a 2 dB increase on the AC output of the preamplifier. If greater than 25 mVrms is desired at the output of the preamp, a series resistor can be added between the preamp output coupling capacitor and the ALC input (pin 4). The input impedance of the ALC circuit is 2 kΩ; therefore, if a 2 kΩ series resistor is added, ALC action will begin at 50 mVrms.

The ALC memory capacitor connected to pin 6 has the additional function of amplifier anti-pop control; for this reason, it is necessary that a capacitor be connected to pin 6 even if ALC is not used.

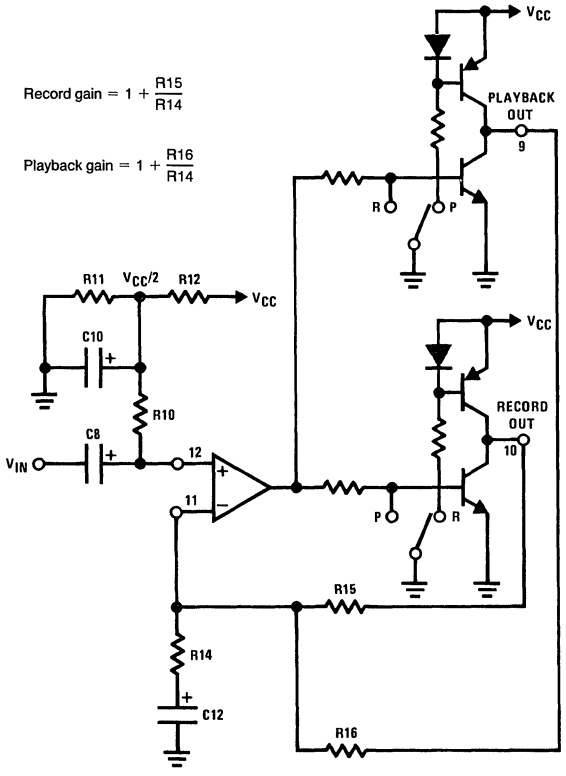

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FIGURE 6. Monitor Amplifier

Application Hints (Continued)

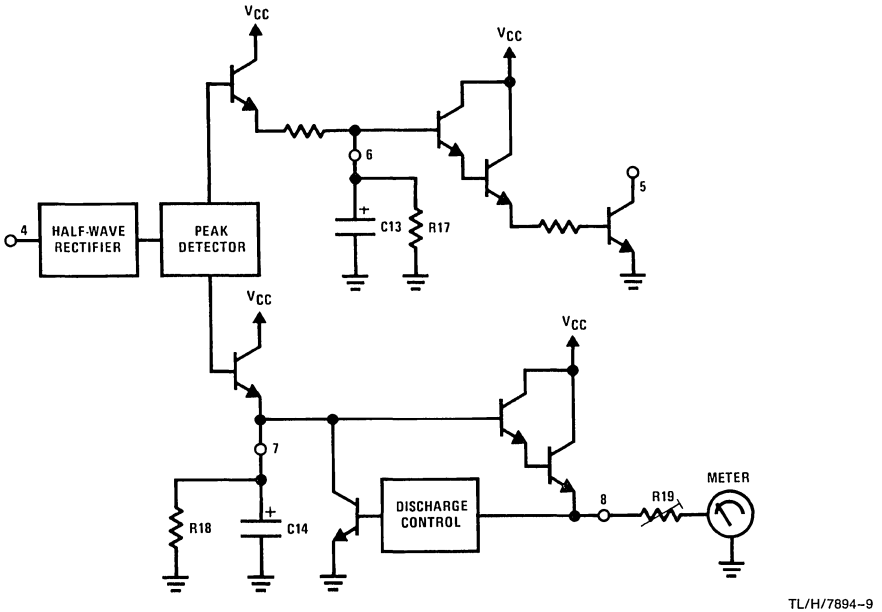

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FIGURE 7. Auto Level-Meter Circuit

METER DRIVING—MOTIONAL PEAK LEVEL RESPONSE *(Figure 7)*

The meter drive output (pin 8) is capable of supplying 1–2 mA at a filtered DC voltage that is typically equal to 10 times the RMS value of the signal applied to the ALC-meter drive input (pin 4). The RC network connected to pin 7 of the IC determines the memory constant of the meter circuit. It is therefore possible to store the peak input signal by giving this RC network a long time constant, or read the instantaneous signal level by giving this RC network a very short time constant (i.e., no capacitor). This memory capacitor is discharged within the integrated circuit at a discharge rate related to the DC level on the meter output pin. When the meter output pin is between 0 V_{DC} and 0.7 V_{DC} there is a 50 μA discharge current; when the pin is between 0.7V and 1.1V there is no internal discharge current; and when the voltage on pin 8 is greater than 1.1V there is a discharge equivalent to a 3.3k resistor across the memory capacitor. These different discharge rates allow the meter circuit to display fast, accurate responses on the lower portion of the meter display, slow responses in the higher portion of the meter display, and rapid discharge when the voltage is above the maximum reading the meter can display. The resistor in series with the meter can be adjusted such that the previously mentioned responses coincide with the proper points (0 VU and +3 VU) on the meter scale.

Application Hints (Continued)

Anti-Pop Circuitry *(Figure 8)*

The capacitor on pin 3 is used in a time delay system in conjunction with C13, the ALC capacitor, to suppress pops when switching between record and playback. *Figure 8* illustrates how this is done. The output amplifier, either record or playback, is shut off prior to switching and carefully rebiased after switching takes place. It is therefore required that a proper ratio is selected between the ALC capacitor and the logic input RC time constant. The ALC capacitor must be discharged to 0.7V within the time it takes the logic input capacitor to: 1) charge from $V_{CC}/2$ to 0.7 V_{CC} when switching from record to playback, or 2) discharge from $V_{CC}/2$ to 0.3 V_{CC} when switching from playback to record. These times would normally be similar; however, the ALC capacitor can be charged to a different initial value depending upon the input to the ALC circuit. The maximum value to which the ALC memory capacitor will normally charge is 3.2V, therefore, the maximum time allowed for discharging C13 is given by:

$$t1 = \frac{(C13 \times \Delta V)}{I_1} = C13\frac{(3.2V - 0.7V)}{350\ \mu A}$$

$$= C13 \times 7.2 \times 10^4$$

$$\text{If } C13 = 10\ \mu F,\ t1 = 72\ ms$$

It is now necessary to determine the minimum value for the R/P logic capacitor. This is done by computing the time between the 2 voltage switching points using the exponential equations for a single RC network.

$$t2 = R13\ C11\ \ln\left[\frac{V_{CC}}{0.3\ V_{CC}}\right] -$$

$$R13\ C11\ \ln\left[\frac{V_{CC}}{0.5\ V_{CC}}\right] = 0.51\ R13\ C11$$

To be sure that C13 is completely discharged, let t2 > t1.

$$R13\ C11 > \frac{t1}{0.51} = \frac{(72\ ms)}{0.51} = 141\ ms$$

$$\text{If } C11 = 10\ \mu F,\ R13 = 15\ k\Omega$$

R13 should be kept to a value less than 50 kΩ to insure that bias current existing from pin 3 does not cause an offset voltage above 200 mV. Typically this bias current is less than 3 μA.

Record Playback Switch

When the voltage on pin 3 of the IC is greater than 0.5 V_{CC}, the internal record-playback switch switches into the playback mode. During playback the record preamplifier remains partially biased but the input signal to this preamp does not appear at the preamplifier output. In addition, during the playback mode, the record monitor output (pin 9) is disabled and the ALC circuit operates to minimize the signal into the record preamp input. The meter circuit is operational in the playback as well as the record mode. Similarly, during the record mode, the playback preamp input is ignored and the playback monitor output is disabled. In addition, a pin is available to hold one side of the record head at ground potential while sinking up to 500 μA of AC bias and record current.

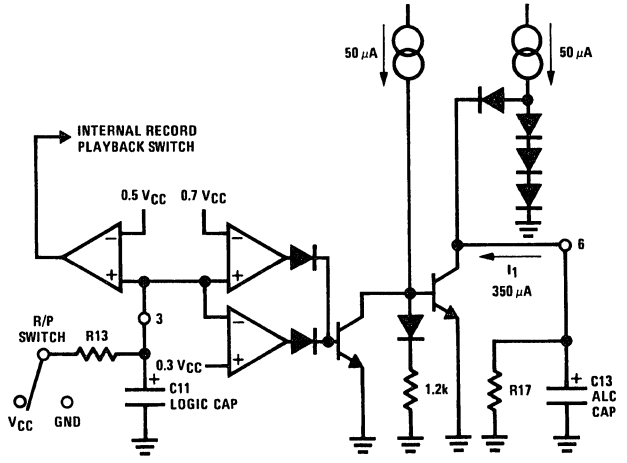

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FIGURE 8A. Anti-Pop Circuit

Application Hints (Continued)

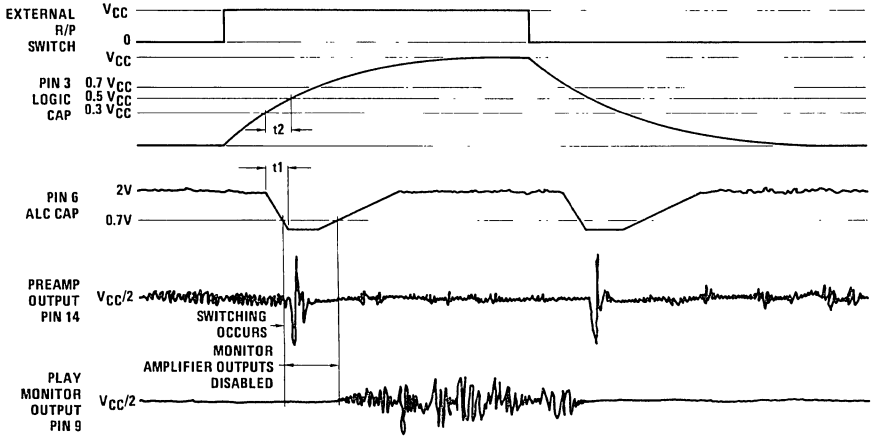

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FIGURE 8B. Waveform for Anti-Pop Circuit

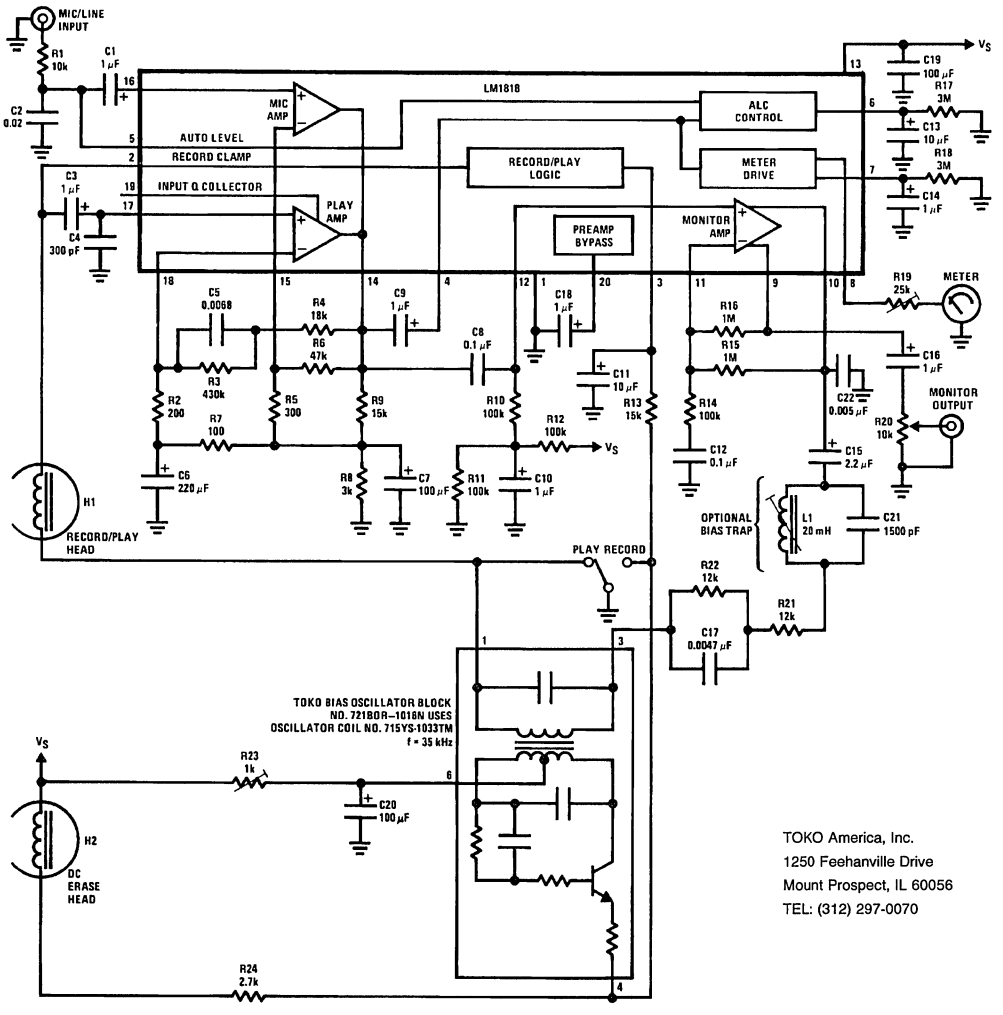
External Components (Refer to *Figure 9*, Monaural Application Circuit)

Component	External Component Function	Normal Range of Value
R1	Used in conjunction with varying impedance of pin 5, forming a resistor divider network to reduce input level in automatic level control circuit.	500Ω–20 kΩ
C2	Forms a noise reduction system by varying bandwidth as a function of the changing impedance on pin 5. With a small input signal, the bandwidth is reduced by R1 and C2. As the input level increases, so does the bandwidth.	0.01 μF–0.5 μF
C1, C3	Coupling capacitors. Because these are part of the source impedance, it is important to use the larger values to keep low frequency source impedance at a minimum.	0.5 μF–10 μF
C4	Radio frequency interference roll-off capacitor	100 pF–300 pF
R2 R3 R4 C5	Playback response equalization. C5 and R3 form a pole in the amplifier response at 50 Hz. C5 and R4 form a zero in the response at 1.3 kHz for 120 μs equalization and 2.3 kHz for 70 μs equalization.	50Ω–200Ω 47 kΩ–3.3 MΩ 2 kΩ–200 kΩ
R5 R6	Microphone preamplifier gain equalization	50Ω–200Ω 5 kΩ–200 kΩ
R7 R8 R9 C6 C7	DC feedback path. Provides a low impedance path to the negative input in order to sink the 50 μA negative input amplifier current. C6, R9, R7 and C7 provide isolation from the output so that adequate gain can be obtained at 20 Hz. This 2-pole technique also provides fast turn-ON settling time.	0–2 kΩ 200Ω–5 kΩ 1 kΩ–30 kΩ 200 μF–1000 μF 0–100 μF
C8	Preamplifier output to monitor amplifier input coupling	0.05 μF–1 μF
C9	ALC coupling capacitor. Note that ALC input impedance is 2 kΩ	0.1 μF–5 μF
R10 R11 R12 C10	These components bias the monitor amplifier output to half supply since the amplifier is unity gain at DC. This allows for maximum output swing on a varying supply.	10 kΩ–100 kΩ 10 kΩ–100 kΩ 10 kΩ–100 kΩ 1 μF–100 μF

External Components (Refer to *Figure 9*, Monaural Application Circuit) (Continued)

Component	External Component Function	Normal Range of Value
C11 R13	Exponentially falling or rising signal on pin 3 determines sequencing, time delay, and operational mode of the record/play anti-pop circuitry. See anti-pop diagram.	0–10 μF 0–50 kΩ
R14 R15 R16 C12	R16, R14 and C12 determine monitor amplifier response in the play mode. R15, R14 and C12 determine monitor amplifier response in the record mode.	1k–100k 30 kΩ–3 MΩ 30 kΩ–3 MΩ 0.1 μF–20 μF
C13 R17	Determines decay response on ALC characteristic and reduces amplifier pop	5 μF–20μF 100k–∞
C14 R18	Determines time constant of meter driving circuitry	0.1 μF–10 μF 100k–∞
R19	Meter sensitivity adjust	10 kΩ–100 kΩ
C15	Record output DC blocking capacitor	1 μF–10 μF
C16	Play output DC blocking capacitor	0.1 μF–10 μF
C17 R21 R22	Changes record output response to approximate a constant current output in conjunction with record head impedance resulting in proper recording equalization	500 pF–0.1μF 5 kΩ–100 kΩ 5 kΩ–100 kΩ
C18	Preamplifier supply decoupling capacitor. Note that large value capacitor will increase turn-ON time	0.1 μF–500 μF
C19	Supply decoupling capacitor	100 μF–1000 μF
C20	Decouples bias oscillator supply	10 μF–500μF
R23	Allows bias level adjustment	0–1 kΩ
R24	Adjusts DC erase current in DC erase machines (for AC erase, see "Stereo Application Circuit," *Figure 1*)	
L1 C21	Optional bias trap	1 mH–30 mH 100 pF–2000 pF
C22	Bias Roll-Off	0.001 μF–0.01 μF
H1	Record/play head	100Ω–500Ω; 70 mH–300 mH
H2	Erase head (DC type, AC optional)	10Ω–300Ω

Typical Applications (Continued)



TOKO America, Inc.
1250 Feehanville Drive
Mount Prospect, IL 60056
TEL: (312) 297-0070

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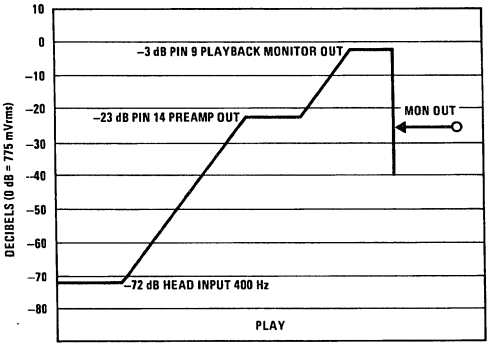
FIGURE 9A. Monaural Application Circuit

Typical Applications (Continued)



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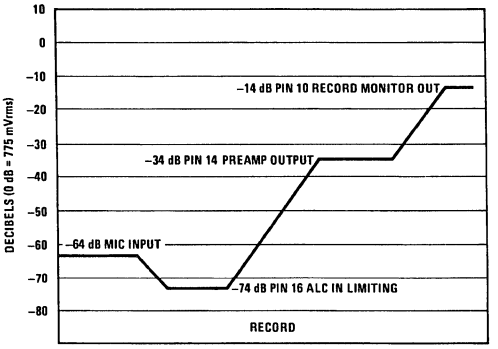

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FIGURE 9B. Level Diagram for Monaural Application Circuit

National Semiconductor Corporation

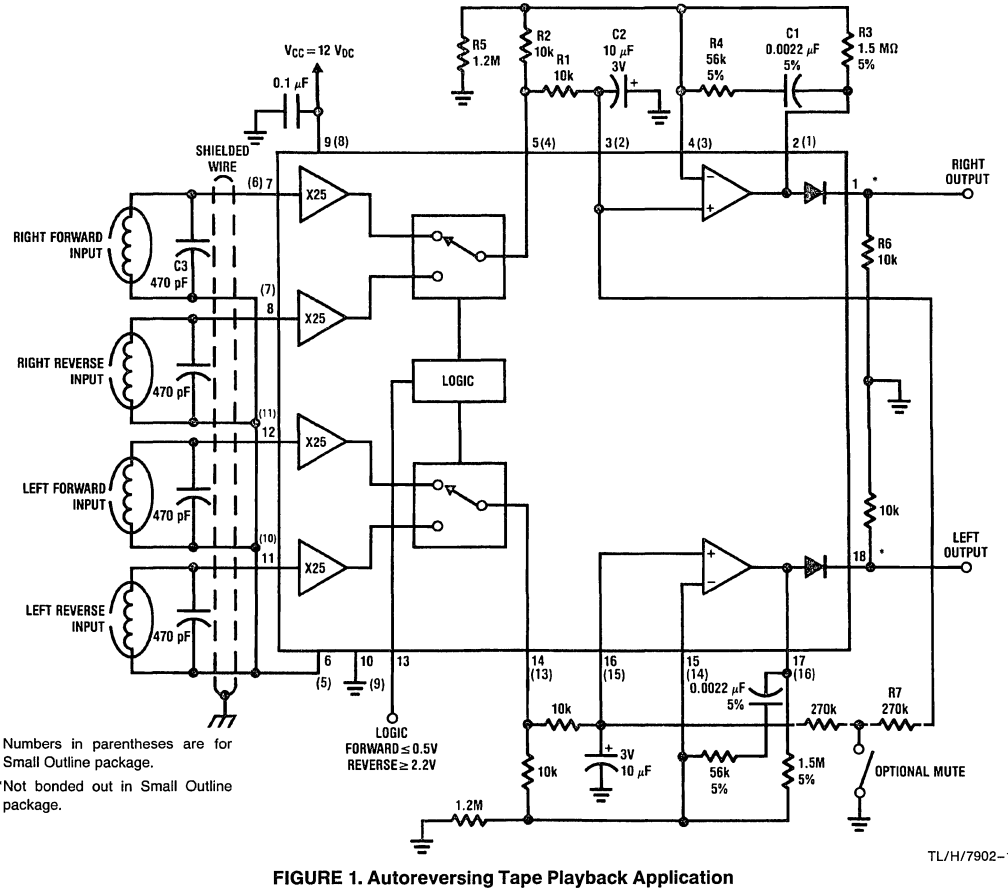
LM1837 Low Noise Preamplifier for Autoreversing Tape Playback Systems

General Description

The LM1837 is a dual autoreversing high gain tape preamplifier for applications requiring optimum noise performance. It has forward (left, right) and reverse (left, right) inputs which are selectable through a high impedance logic pin. It is an ideal choice for a tape playback amplifier when a combination of low noise, autoreversing, good power supply rejection, and no power-up transients are desired. The application also provides transient-free muting with a single pole grounding switch.

Features

- Programmable turn-on delay
- Transient-free power-up—no pops
- Transient-free muting
- Low noise—0.6 μV CCIR/ARM in a DIN circuit referenced to 1 kHz
- Low voltage battery operation −4V
- Wide gain bandwidth due to broadband two-amplifier approach—76 dB @ 20 kHz
- High power supply rejection—95 dB
- Low distortion—0.03%
- Fast slew rate—6V/μs
- Short circuit protection
- Internal diodes for diode switching applications
- Low cost external parts
- Excellent low frequency response
- Prevents "click" from being recorded onto the tape during power supply cycling in tape playback applications
- High impedance logic pin for forward/reverse switching



Numbers in parentheses are for Small Outline package.

*Not bonded out in Small Outline package.

FIGURE 1. Autoreversing Tape Playback Application

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	18V
Voltage on Pins 1 and 18	18V
Package Dissipation (Note 1)	1390 mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Minimum Voltage on Any Pin	−0.1 V_{DC}

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = 12V, see Test Circuit, *Figure 2*)

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage Range	R5 Removed from Circuit for Low Voltage Operation	4		18	V
Supply Current	V_{CC} = 12V		9	15	mA
Total Harmonic Distortion	f = 1 kHz, V_{IN} = 0.3 mV, Pins 2 and 17, *Figure 2*		0.03		%
THD + Noise (Note 2)	f = 1 kHz, V_{OUT} = 1V, Pins 2 and 17, *Figure 2*		0.10	0.25	%
Power Supply Rejection	Input Ref. f = 1 kHz, 1 Vrms	80	95		dB
Channel Separation (Note 3)	f = 1 kHz, Output = 1 Vrms,				dB
Left to Right	Output to Output	40	60		dB
Forward to Reverse		40	60		dB
Signal-to-Noise (Note 4)	Unweighted 32 Hz-12.74 kHz (Note 2)		58		dB
	CCIR/ARM (Note 5)		62		dB
	A Weighted		64		dB
	CCIR, Peak (Note 6)		52		dB
Noise	Output Voltage CCIR/ARM (Note 5)		120	200	μV
Input Amplifers					
Input Bias Current			0.5	2.0	μA
Input Impedance	f = 1 kHz	150			kΩ
AC Gain		27	28	29	dB
AC Gain Imbalance			±0.15	±0.5	dB
DC Output Voltage		2.1	2.5	2.9	V
DC Output Voltage Mismatch	Pins 5 and 14	−200	±30	200	mV
Output Source Current	Pins 5 and 14	2	10		mA
Output Sink Current	Pins 5 and 14	300	600		μA
Logic Level					
Forward				0.5	V
Reverse		2.2			V
Logic Pin Current			2	6	μA
DC Voltage Change at Pins 5 and 14	Change Logic State	−100	±20	100	mV

Electrical Characteristics (T_A = 25°C, V_{CC} = 12V, see Test Circuit, *Figure 2*) (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Output Amplifiers					
Closed Loop Gain	Stable Operation	5			V/V
Open Loop Voltage Gain	DC		100		dB
Gain Bandwidth Product			5		MHz
Slew Rate			6		V/μs
Input Offset Voltage			2	5	mV
Input Offset Current			20	100	nA
Input Bias Current			250	500	nA
Output Source Current	Pin 2 or 17	2	10		mA
Output Sink Current	Pin 2 or 17	400	900		μA
Outut Voltage Swing	Pin 2 or 17		11		Vp-p
Output Diode Leakage	Voltage on Pins 1 and 18 = 18V		0	10	μA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient (Dual-In-Line). Small Outline Thermal Resistance is 100°C/W.

Note 2: Measured with an average responding voltmeter using the filter circuit in *Figure 4*. This simple filter is approximately equivalent to a "brick wall" filter with a passband of 20 Hz to 20 kHz (see Application Hints). For 1 kHz THD the 400 Hz high pass filter on the distortion analyzer is used.

Note 3: Channel separation can be measured by applying the input signal through transformers to simulate a floating source (see Application Hints). Care must be taken to shield the coils from extraneous signals. Actual production test techniques at National simulate this floating source with a more complex op amp circuit.

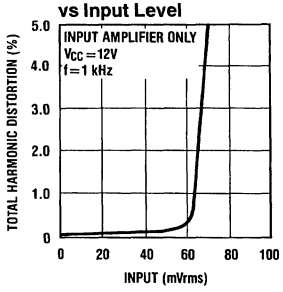
Note 4: The numbers are referred to an output level of 160 mV at pins 2 and 17 using the circuit of *Figure 2*. This corresponds to an input level of 0.3 mVrms at 333 Hz.

Note 5: Measured with an average responding voltmeter using the Dolby lab's standard CCIR filter having a unity gain reference at 2 kHz.

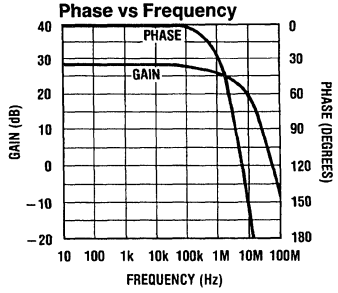
Note 6: Measured using the Rhode-Schwarz psophometer, model UPGR.

Typical Performance Characteristics

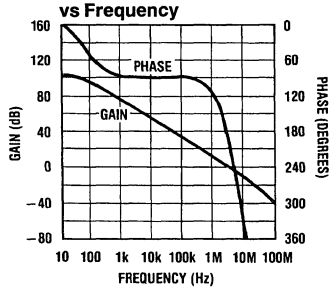
Input Amplifier THD vs Input Level



Input Amplifier Gain and Phase vs Frequency



Output Amplifier Open Loop Gain and Phase vs Frequency



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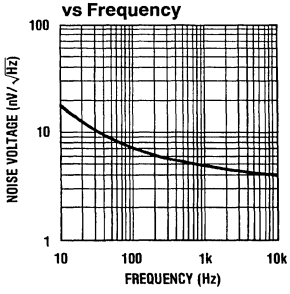
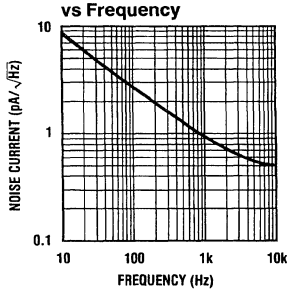
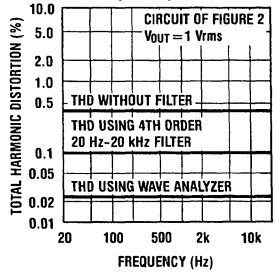
Spot Noise Voltage vs Frequency



Spot Noise Current vs Frequency



Total Harmonic Distortion vs Frequency



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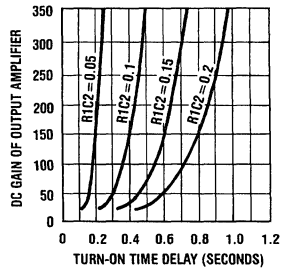
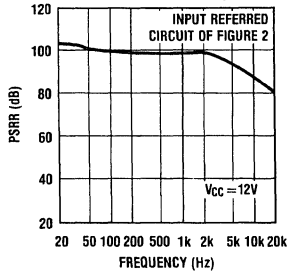
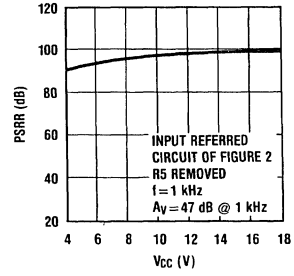
Turn-On Delay vs Component Values and Gain



PSRR vs Frequency



PSRR vs V_{CC}



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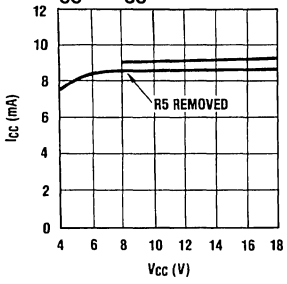
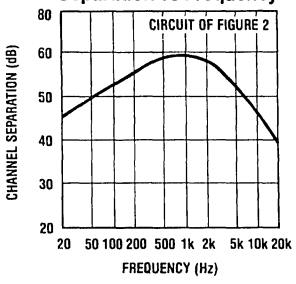
Typical Performance Characteristics (Continued)

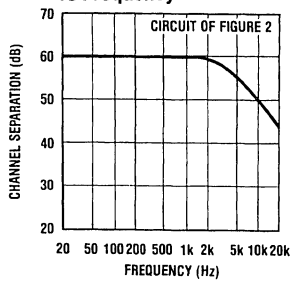
I_{CC} vs V_{CC}



Right to Left Channel Separation vs Frequency

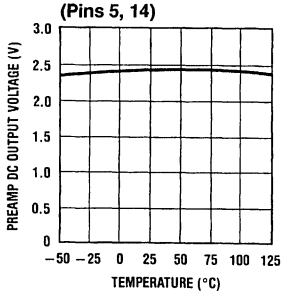


Forward to Reverse Channel Separation vs Frequency



TL/H/7902–5

Input Amplifier DC Output Voltage vs Temperature (Pins 5, 14)



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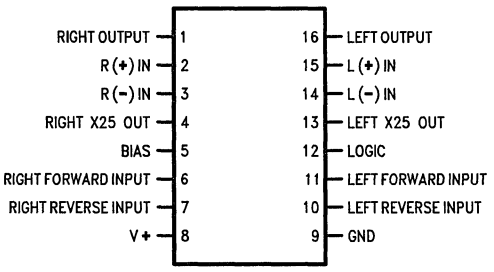
Connection Diagrams

Small Outline Package



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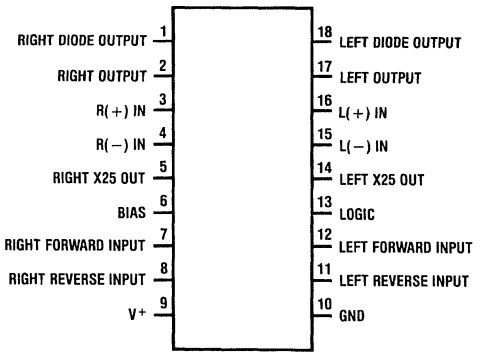
Order Number LM1837M
See NS Package Number M16B

Dual-In-Line Package



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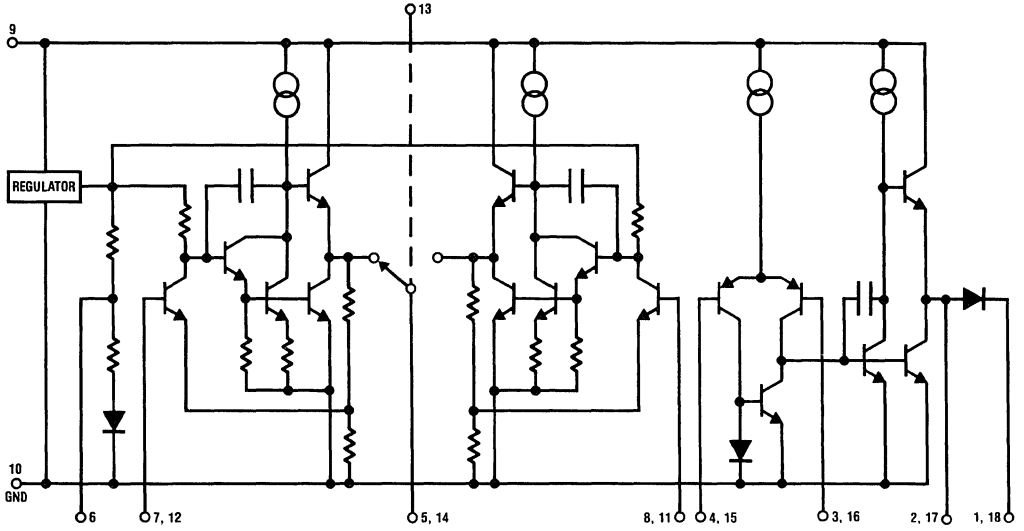
Top View

Order Number LM1837N
See NS Package Number N18A

External Components *(Figure 1)*

Component	Normal Range of Value and Function
R1, C2	2 kΩ–40 kΩ, 0.1 μF–10 μF (low leakage) Set turn-on delay and second amplifier's low frequency pole. Leakage current in C2 results in DC offset between the amplifier's inputs and therefore this current should be kept low. R1 is set equal to R2 such that any input offset voltage due to bias current is effectively cancelled. An input offset voltage is generated by the input offset current multiplied by the value of these resistors.
R2, R3	2 kΩ–40 kΩ, 500 kΩ–10 MΩ Sets the DC and low frequency gain of the output amplifier. The total input offset voltage will also be multiplied by the DC gain of this amplifier. It is therefore essential to keep the input offset voltage specification in mind when employing high DC gain in the output amplifier; i.e., 5 mV × 400 = 2V offset at the output.
R4, C1	10 kΩ–200 kΩ, 0.00047 μF–0.01 μF Set tape playback equalization characteristics in conjunction with R3 (calculations for the component values are included in the Application Hints section).
R6	2 kΩ–47 kΩ Biases the output diode when it is used in DC switching applications. This resistor can be excluded if diode switching is not desired.
C3	100 pF–1000 pF Often used to resonate with tape head in order to compensate for tape play-back losses including tape head gap and eddy current. For a typical cassette tape head, the resonant frequency selected is usually between 13 kHz and 17 kHz.
R5	100 kΩ–10 MΩ Increases the output DC bias voltage from the nominal 2.5V value (see Application Hints).
R7	Optionally used for tape muting. The use of this resistor can also provide "no-pop" turn-off if desired (see Application Hints).

Simplified Schematic



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Application Hints

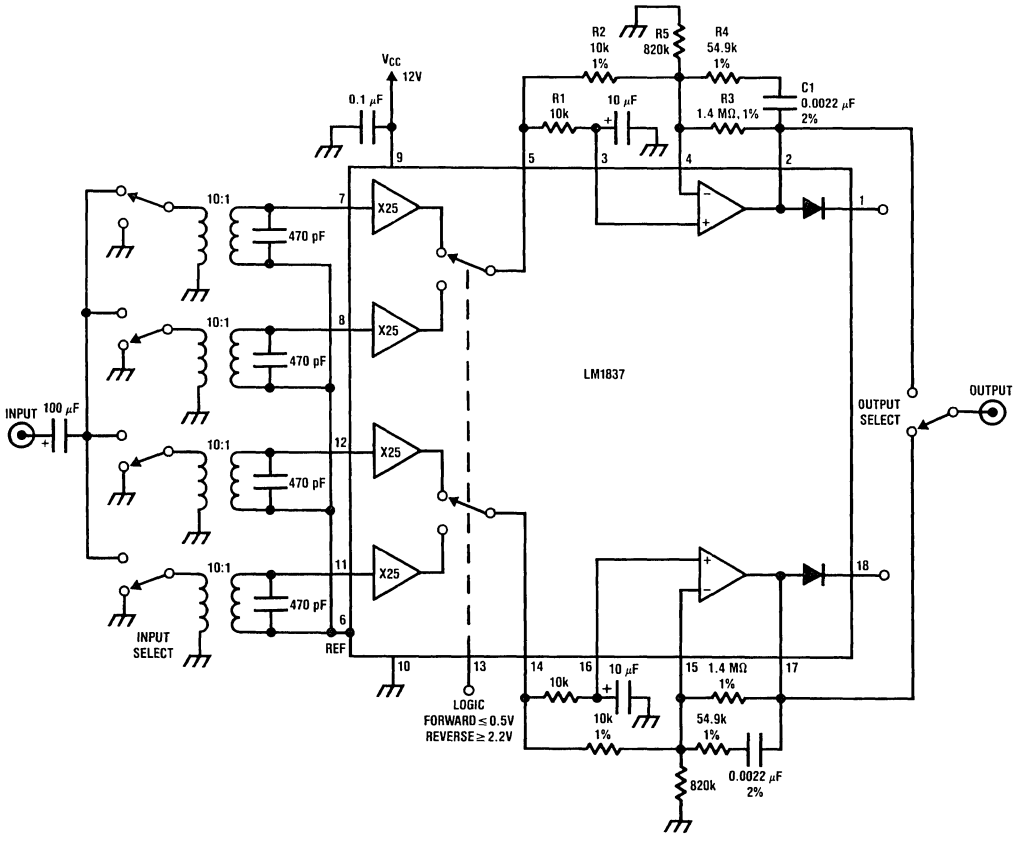

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FIGURE 2. General Test Circuit

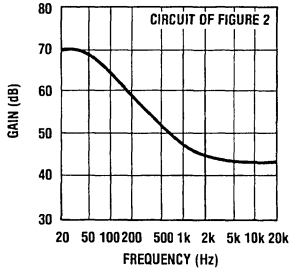

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FIGURE 3. Frequency Response of Test Circuit

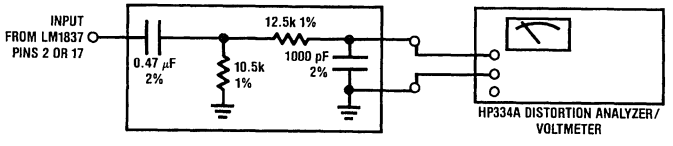

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FIGURE 4. Simple 32 Hz-12740 Hz Filter and Meter

Application Hints (Continued)

DISTORTION MEASUREMENT METHOD

In order to clearly interpret and compare specifications and measurements for low noise preamplifiers, it is necessary to understand several basic concepts of noise. An obvious example is the measurement of total harmonic distortion at very low input signal levels. Distortion analyzers provide outputs which allow viewing of the distortion products on an oscilloscope. The oscilloscope often reveals that the "distortion" being measured contains 1) distortion, 2) noise, and 3) 50 or 60 cycle AC line hum.

Line hum can be detected by using the "line sync" on the oscilloscope (horizontal sync selector). The triggering of a constant waveform indicates that AC line pick-up is present. This is usually the result of electro-magnetic coupling into the preamplifiers input or improper test equipment grounding, which simply must be eliminated before making further measurements!

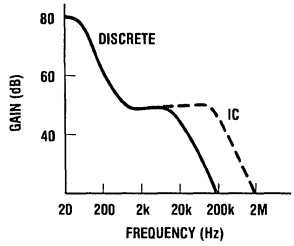
Input coupling problems can usually be corrected by any one of the following solutions: 1) shielding the source of the magnetic field (using mu metal or steel), 2) magnetically shielding the preamplifier, 3) physically moving the preamplifier far enough away from the magnetic field, or 4) using a high pass filter (f_o = 200 Hz–1 kHz) at the output of the preamplifier to prevent any line signal from entering the distortion analyzer. Ground loop problems can be solved by rearranging ground connections of the circuit and test equipment.

Separating noise from distortion products is necessary when it is desired to find the actual distortion and not the signal-to-noise ratio of an amplifier. The distortion produced by the LM1837 is predominantly a second harmonic. It is for this reason that the third and higher order harmonics can be filtered without resulting in any appreciable error in the measurement. The filter also reduces the amount of noise in the measured data. Another more tedious technique for measuring THD is to use a wave analyzer. Each harmonic is measured and then summed in an rms calculation. A typical curve is plotted for distortion vs frequency using this method. A typical curve is also included using a 20 Hz to 20 kHz 4th order filter.

To specify the distortion of the LM1837 accurately and also not require unusual or tedious measurements the following method is used. The output level is set to 1 Vrms at 1 kHz (approximately 5 mV at the input). The output is filtered with the circuit of *Figure 4* to limit the bandwidth of the noise and measured with a standard distortion analyzer. The analyzer has a filter that is switched in to remove line hum and ground loop pick-up as well as unrelated low frequency noise. The resulting measurement is fast and accurate.

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit to discrete preamplifier designs. Discrete transistor preamps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated in *Figure 5*.



TL/H/7902–13

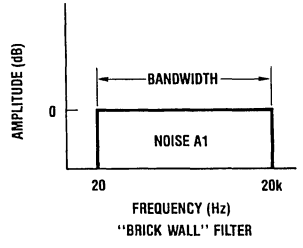
FIGURE 5

Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal-to-noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter.[1] A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to certain undesirable frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

The 32 Hz to 12740 Hz filter shown in *Figure 4* is a simple two pole, one zero filter, approximately equivalent to a "brick wall" filter of 20 Hz to 20 kHz. This approximation is absolutely valid if the noise has a flat energy spectrum over the frequencies involved. In other words a measurement of a noise source with constant spectral density through either of the two filters would result in the same reading. The output frequency response of the two filters is shown in *Figure 6*.

Application Hints (Continued)



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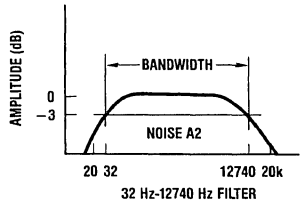

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FIGURE 6

Typical signal-to-noise figures are listed for several weighting filters which are commonly used in the measurement of noise. The shape of all weighting filters is similar with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown in *Figure 7*.

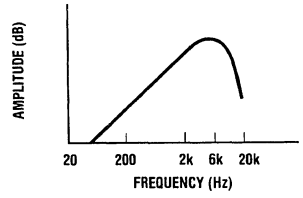

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FIGURE 7

In addition to noise filtering, differing meter types give different noise readings. Meter responses include: 1) rms reading, 2) average responding, 3) peak reading, and 4) quasi peak reading. Although theoretical noise analysis is derived using true rms (root mean square) based calculations, most actual measurement is taken with ARM (Average Responding Meter) test equipment.

Unless otherwise noted an average responding meter is used for all AC measurements in this data sheet.

BASIC CIRCUIT APPROACH

The LM1837 IC incorporates a two stage broadband design which minimizes noise, attains overall DC stability and prevents audible transients during turn-on.

The first stage consists of four direct coupled preamplifiers with internal gain of 25V/V (28 dB). Direct coupling to the tape head reduces input source impedance and external component cost by removing the input coupling capacitor. A typical input coupling capacitor of 1 μF has a reactance of 1.5 kΩ at 100 Hz. The resulting noise due to the amplifier's input noise current can dominate the noise voltage at the output of the playback system. The inputs of the amplifiers are biased from a common reference voltage that is temperature compensated to produce a quiescent DC voltage of 2.5V at the output of the first stage. The input stage bias current that flows through the tape head is kept below 2 μA in order to prevent any erasure of tape moving past the head. An added advantage of DC biasing is the prevention of large current transients during the charging of coupling capacitors at turn-on and turn-off. The outputs of the forward and reverse preamplifier are fed to the common output op amp through a logic controlled switch.

The second stage provides additional gain and proper equalization while preventing audible turn-on transients or "pops". The output (pin 2) is kept low until C2 charges through R1. When the voltage on C2 gets close to the DC voltage on pin 5, the output rises exponentially to its final DC value. The result is a transient-free turn-on characteristic.

Internal diodes are provided to facilitate electronic diode switching, popular in automotive applications.

The General Test Circuit illustrates the topography of the system. The components determining the overall frequency response are external due to the extreme sensitivity when matching a DIN equalization curve.

MUTE CIRCUIT AND LOGIC

The LM1837 can be muted with the addition of two resistors and a grounding switch, as shown in *Figure 1*. When the circuit is not muted the additional resistors have no effect on the AC performance. They *do* have an effect on the DC Q point however.

The difference in the DC output voltages of the input amplifiers is applied across the mute resistors (R7) and the positive input resistors (R1). This results in an additional offset at the input of the output amplifiers. To keep this offset to a minimum R7 should be as large as possible to achieve effective muting. Unmute voltage is the peak signal the preamplifier can swing without turning on the output amplifier under mute conditions:

$$\text{Unmute voltage} = V_{PIN\ 5,\ 14}\left[\frac{R5//R3}{R2 + R5//R3} - \frac{R7}{R1 + R7}\right]$$

Application Hints (Continued)

For example: The circuit in *Figure 1* has 2.5V DC at pins 5 and 14, so:

Unmute voltage =

$$2.5V\left[\frac{1.2M//1.5M}{10k + 1.2M//1.5M} - \frac{270k}{10k + 270K}\right] = 52.3\ mV$$

It may be necessary to slow the transition of the logic pin if the mute circuit is not used. The forward and reverse preamplifier output DC voltages can differ by ±100 mV. This rapid DC charge is gained up by the output amplifier and appears as a pop. The circuit of *Figure 8* will slow the DC transition.

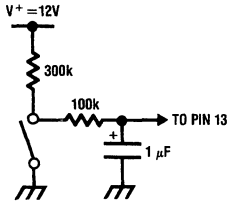

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FIGURE 8. Circuit to Slow Logic

DESIGN EQUATIONS

The overall gain of the circuit is given by:

$$A_V = 25\left[\frac{-R4R3}{R2(R3 + R4)}\right]\frac{\left(s + \frac{1}{R4C1}\right)}{\left(s + \frac{1}{(R3 + R4)C1}\right)} \quad (1)$$

Standard cassette tapes require equalization of 3180 μs (50 Hz) and 120 μs (1.3 kHz). These time constants result in an AC gain at 1 kHz given by:

$$A_V\,(1\ kHz) = 25\left(\frac{-R4R3}{R2(R3 + R4)}\right)1.663 \quad (2)$$

$$\left\{\begin{array}{c}3180\ \mu s\text{ or }50\ Hz\\ \text{and}\\ 120\ \mu s\text{ or }1326\ Hz\end{array}\right\}$$

Using the pole and zero locations of the transfer function, the two other equations needed to solve for the component values are:

$$R4 = \frac{1}{2\pi C1(1326\ Hz)} \quad (3)$$

$$R3 = \frac{1}{2\pi C1(50\ Hz)} - \frac{1}{2\pi C1(1326\ Hz)} = \frac{1}{2\pi C1(51.96)} \quad (4)$$

We can now solve for C1 as a function of R2, or:

$$A_V(1\ kHz) = -25\left\{\frac{\left[\frac{1}{2\pi C1(1326)}\right]\left[\frac{1}{2\pi C1(51.96)}\right]}{\left[R2\,\frac{1}{2\pi C1(50)}\right]}\right\} \quad (1.663)\ (5)$$

$$C1 = \frac{-4.80 \times 10^{-3}}{R2\,[A_V\,(1\ kHz)]} \quad (6)$$

When chromium dioxide is used, the defined time constants are 3180 μs and 70 μs. This changes equation (3) to:

$$R4 = \frac{1}{2\pi C1(2274\ Hz)} \quad (7)$$

The value of R3 is normally not changed. This results in an error of less than 0.2 dB in the low frequency response.

The output voltage of the LM1837 is set by the input amplifier DC voltage at pin 5 or 14, and by R3 and R5.

$$\text{Nominal } V_{OUT}\text{ (pin 2 or 17)} = 2.5\left(1 + \frac{R3}{R5}\right) \quad (8)$$

Pins 1 and 18 are biased 0.7V less than V_{OUT}(pin 2 or 17). When these diodes are used the output (pin 2 or 17) should be biased at one half the minimum operating supply voltage. Equation (8) can be rewritten to solve for R5.

$$R5 = \frac{2.5\ R3}{V_O - 2.5} \quad (9)$$

The output voltage of the LM1837 will vary from that given in equation (8) due to variations in the input amplifier DC voltage as well as the output amplifier input bias current, input offset current and input offset voltage. The following equation gives the worst-case variation in the output voltage in either forward or reverse state.

$$\Delta V_{OUT} = \pm\left[\Delta V_{PIN3}\left(1 + \frac{R3}{R5}\right) + \frac{R3}{R2}\left(\Delta I_{BIAS}\,(R1 - R2) + \frac{I_{OS}}{2}(R1 + R2) + V_{OS}\right)\right] \quad (10)$$

Using the worst-case values in the electrical characteristics reduces this to

$$\Delta V_{OUT} = \pm\left[0.4\left(1 + \frac{R3}{R5}\right) + \frac{R3}{R2}\left(200\ nA\,(R1 - R2) + 50\ nA\,(R1 + R2) + 5\ mV\right)\right] \quad (11)$$

Equation (10) does not incorporate the effect of mute resistors on the output voltage. The presence of mute resistors causes an additional offset

$$\Delta V_{OUT}(mute) = \pm\frac{\Delta V(pins\ 5–14)}{2(R1 + R7)} \times R1 \quad (12)$$

For the circuit in *Figure 1* worst-case:

$$\Delta V_{OUT}(mute) = \frac{400\ mV}{2(20k + 270k)} \times 1.5M = 1V$$

This means that the output pins 2 and 17 would differ by 1V. The trade off here is the amount of unmute voltage versus the DC accuracy of pins 2 and 17.

Application Hints (Continued)

The turn-on delay is set by R1 and C2; delay can be approximated by:

$$\text{Delay time } t = R1C2 \text{ Ln} \left(\frac{2.5}{V_{ODC}}\right)\left(\frac{R3}{R2}\right) \qquad (13)$$

EXAMPLE

If we desire a tape preamp with 100 mV output signal from a tape head with a nominal output of 0.5 mV at 1 kHz for standard ferric cassette tape, the external components are determined as follows. The value of R2 is arbitrarily set to 10 kΩ.

$$R1 = R2 = 10k$$

This minimizes errors due to the output amplifier bias currents.

$$C1 = \frac{-4.80 \times 10^{-3}}{10\ k\Omega\left[\frac{-100\ mV}{0.5\ mV}\right]} = 2400\ pF \rightarrow 0.0022\ \mu F$$

Use 0.0022 μF and determine:

$$R4 = \frac{1}{2\pi C1(1326)} = 54.6\ k\Omega \rightarrow 54.9\ k\Omega\ 1\%$$

$$R3 = \frac{1}{2\pi C1(51.96)} = 1.39\ M\Omega \rightarrow 1.4\ M\Omega\ 1\%$$

To bias the output amplifier output voltage at 6V (half supply):

$$R5 = \frac{2.5(1.4\ M\Omega)}{6 - 2.5} = 1\ M\Omega$$

The maximum variation in the output is found using equation (11):

$$\Delta V_{OUT} = \pm 1.9V$$

The low frequency response and turn-on delay determine the value of C2. For R1 = 10k and C2 = 10 μF the low frequency 3 dB point is 1.6 Hz and the turn-on delay is 0.4 seconds, from equation (12).

The complete circuit is shown in *Figure 2*. A circuit with 5% components and biased for a minimum supply of 10V is shown in *Figure 1*. If additional gain is needed R1 and R2 can be reduced without changing the frequency response of the circuit.

DIODE SWITCHING

The LM1837 has a diode in series with each output for source switching applications. The outputs of several functional blocks can be diode OR-connected as shown in *Figure 9*.

By removing the power supply from the FM demodulator, its output diode will be cut off by the LM1837 output DC voltage. R6 is used to bias ON the diode of the LM1837 when power is applied to it. When the output is taken from pin 1 or pin 18, the THD will be higher because of the current modulation in the diode.

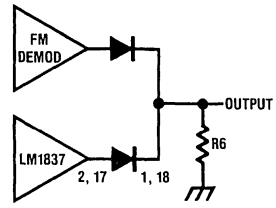

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FIGURE 9

CROSSTALK AND CHANNEL SEPARATION

When two signal sources share a common reference point which is separated from ground by a resistance, there will always be some amount of interchannel crosstalk (the reciprocal of channel separation) induced. The coupling method of *Figure 1* is examined to determine whether the induced crosstalk is acceptably low.

Figure 10 is the equivalent AC circuit for the connection scheme of *Figure 1*. R_B is the Thevenin resistance of the common bias point, R_{IN} is the preamplifier input resistance, Z_S is the impedance of the playback head, and V_{S7}, V_{S8}, V_{S11}, and V_{S12} are the open-circuit output voltages of the sources. If we set V_{S8}, V_{S11}, and V_{S12} equal to zero, we can define crosstalk for this circuit as V12/V7, where V7 and V12 are the AC signal voltages appearing at the two preamplifier inputs, assuming $R_B \ll R_{IN}/3$.

The crosstalk can be shown to be:

$$\frac{V12}{V7} = \frac{R_B}{R_B + Z_S + R_{IN}/3}$$

Since Z_S is dependent on the measurement frequency and the particular head used, we choose the worst-case condition and set $Z_S = 0$. The minimum value of R_{IN} is 150 kΩ, and $R_B \cong 100\Omega$. This yields a crosstalk figure of:

$$\frac{V12}{V7} = \frac{100}{50100} = -54\ dB$$

This is 14 dB better than the minimum guaranteed channel separation, so the connection method of *Figure 1* will provide acceptable crosstalk levels.

Reference 1: CCIR/ARM: A *Practical Noise Measurement Method;* by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

Application Hints (Continued)

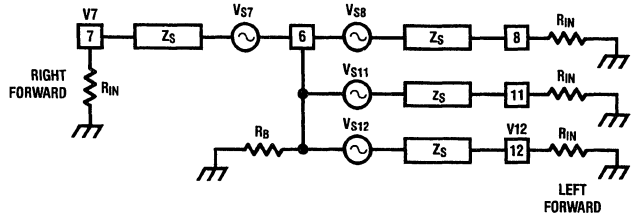

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FIGURE 10. AC Equivalent of *Figure 1*

National Semiconductor Corporation

LM1875 20 Watt Power Audio Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on ±25V supplies. Using an 8Ω load and ±30V supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of advanced circuit techniques and processing to achieve extremely low distortion levels even at high output power levels. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is internally compensated and stable for gains of 10 or greater.

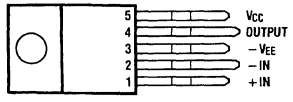
Features

- Up to 30 watts output power
- A_{VO} typically 90 dB
- Low distortion 0.015%, 1 kHz, 20 W
- Wide power bandwidth 70 kHz
- Short circuit protection
- Thermal protection with parole circuit
- High current capability 3A
- Wide supply range 20V-60V
- Internal protection diodes
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Connection Diagram



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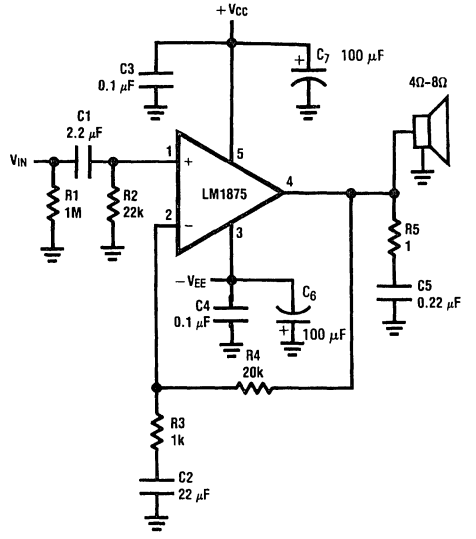
Front View

Order Number LM1875T
See NS Package Number T05B

Typical Applications



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	60V
Input Voltage	$-V_{EE}$ to V_{CC}
Operating Temperature	0°C to + 70°C
Storage Temperature	−65°C to + 150°C
Junction Temperature	150°C
Power Dissipation (Note 1)	30W
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics

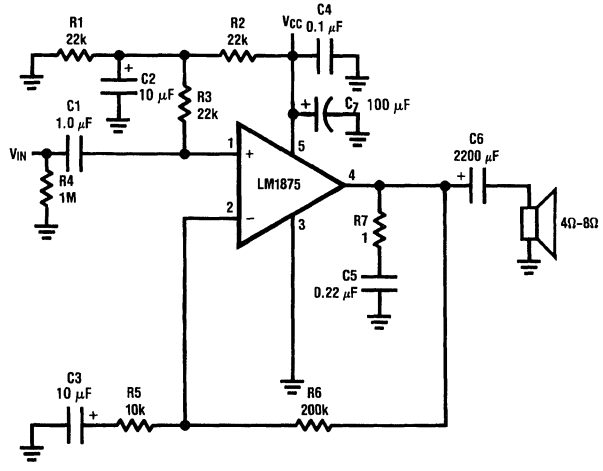
V_{CC} = +25V, $-V_{EE}$ = −25V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 20 (26 dB), f_o = 1 kHz, unless otherwise specified.

Parameter	Conditions	Typical	Tested Limits	Units
Supply Current	P_{OUT} = 0W	70	100	mA
DC Output Level		0		V
Output Power	THD = 1%	25		W
THD	P_{OUT} = 20W, f_o = 1 kHz	0.015		%
	P_{OUT} = 20W, f_o = 20 kHz	0.05	0.4	%
	P_{OUT} = 20W, R_L = 4Ω, f_o = 1 kHz	0.022		%
	P_{OUT} = 20W, R_L = 4Ω, f_o = 20 kHz	0.07	0.6	%
Offset Voltage		±1	±15	mV
Input Bias Current		±0.2	±2	μA
Input Offset Current		0	±0.5	μA
Gain-Bandwidth Product	f_o = 20 kHz	5.5		MHz
Open Loop Gain	DC	90		dB
PSRR	V_{CC}, 1 kHz, 1 Vrms	95	52	dB
	V_{EE}, 1 kHz, 1 Vrms	83	52	dB
Max Slew Rate	20W, 8Ω, 70 kHz BW	8		V/μs
Current Limit		4	3	A
Equivalent Input Noise Voltage	R_S = 600Ω, CCIR	3		μVrms

Note 1: Assumes T_{TAB} equal to 60°C max. For operation at higher tab temperatures and at ambient temperatures greater than 25°C, the LM1875 must be derated based on a maximum 150°C junction temperature. Thermal resistance depends upon device mounting techniques. θ_{JC} is typically 2° C/W. See Application Hints.

Typical Applications (Continued)

Typical Single Supply Operation



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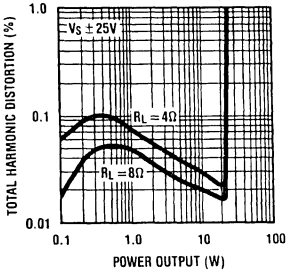
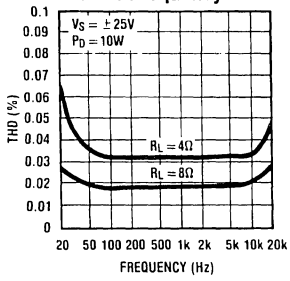
Typical Performance Characteristics

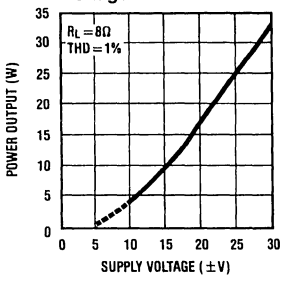
THD vs Power Output



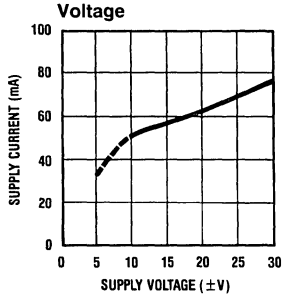
THD vs Frequency



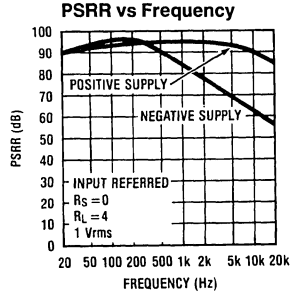
Power Output vs Supply Voltage



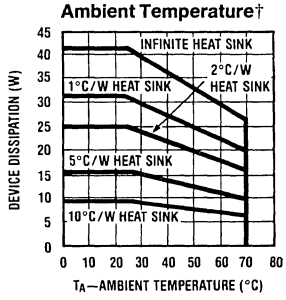
Supply Current vs Supply Voltage



PSRR vs Frequency

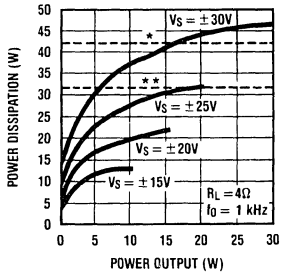


Device Dissipation vs Ambient Temperature†

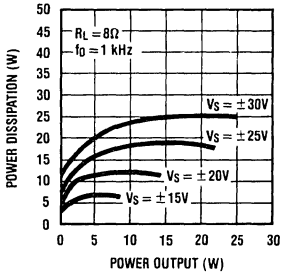


†ϕINTERFACE = 1°C/W.
See Application Hints.

Power Dissipation vs Power Output



Power Dissipation vs Power Output



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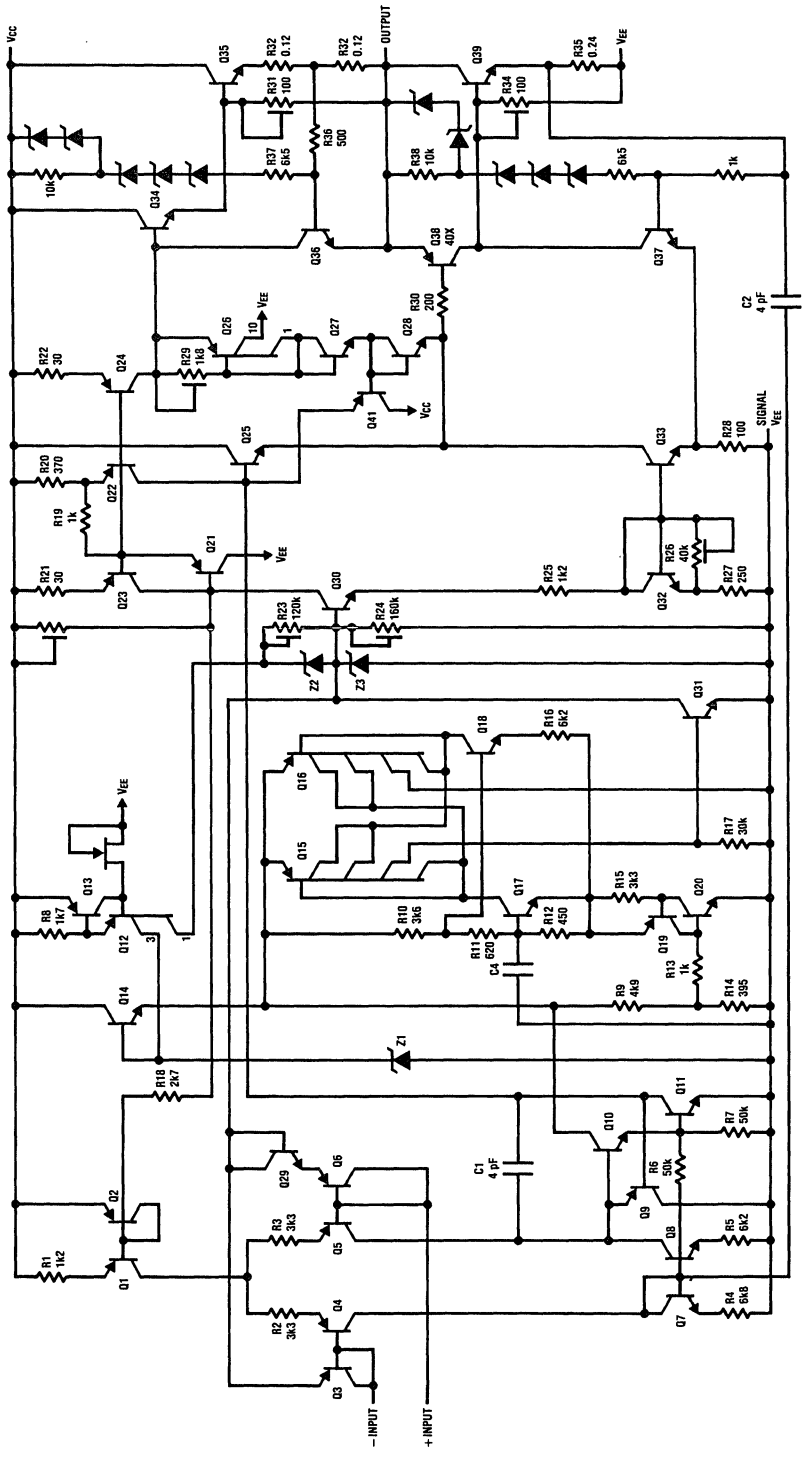
*Thermal shutdown with infinite heat sink

**Thermal shutdown with 1°C/W heat sink

Schematic Diagram



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Application Hints

STABILITY

The LM1875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM1875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

Proper layout of the printed circuit board is very important. While the LM1875 will be stable when installed in a board similar to the ones shown in this data sheet, it is sometimes necessary to modify the layout somewhat to suit the physical requirements of a particular application. When designing a different layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM1875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM1875 is no exception. If the output of the LM1875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM1875. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

DISTORTION

The preceding suggestions regarding circuit board grounding techniques will also help to prevent excessive distortion levels in audio applications. For low THD, it is also necessary to keep the power supply traces and wires separated from the traces and wires connected to the inputs of the LM1875. This prevents the power supply currents, which are large and nonlinear, from inductively coupling to the LM1875 inputs. Power supply wires should be twisted together and separated from the circuit board. Where these wires are soldered to the board, they should be perpendicular to the plane of the board at least to a distance of a couple of inches. With a proper physical layout, THD levels at 20 kHz with 10W output to an 8Ω load should be less than 0.05%, and less than 0.02% at 1 kHz.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic audio power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM1875 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM1875, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM1875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM1875 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

POWER DISSIPATION AND HEAT SINKING

The LM1875 must always be operated with a heat sink, even when it is not required to drive a load. The maximum idling current of the device is 100 mA, so that on a 60V power supply an unloaded LM1875 must dissipate 6W of power. The 54°C/W junction-to-ambient thermal resistance of a TO-220 package would cause the die temperature to rise 324°C above ambient, so the thermal protection circuitry will shut the amplifier down if operation without a heat sink is attempted.

Application Hints (Continued)

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM1875 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM1875, R_L is the load resistance, and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. The curves of "Power Dissipation vs Power Output" give a better representation of the behavior of the LM1875 with various power supply voltages and resistive loads. As an example, if the LM1875 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°C - 70°C}{19W} = 4.2°C/W.$$

Using $\theta_{JC} = 2°C/W$, the sum of the case-to-heat-sink interface thermal resistance and the heat-sink-to-ambient thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry.

If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM1875 and the heat sink. The heat sink thermal resistance must then be less than

4.2°C/W − 2°C/W − 1.6°C/W = 0.6°C/W.

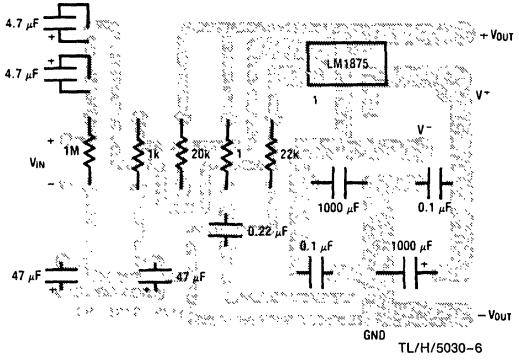
This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be reduced to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

Note: When using a single supply, maximum transfer of heat away from the LM1875 can be achieved by mounting the device directly to the heat sink (tab is at ground potential); this avoids the use of a mica or other type insulator.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load (usually considered to be a worst-case loudspeaker load) will be roughly that of the same amplifier driving the resistive part of that load. For example, a loudspeaker may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Component Layouts

Split Supply



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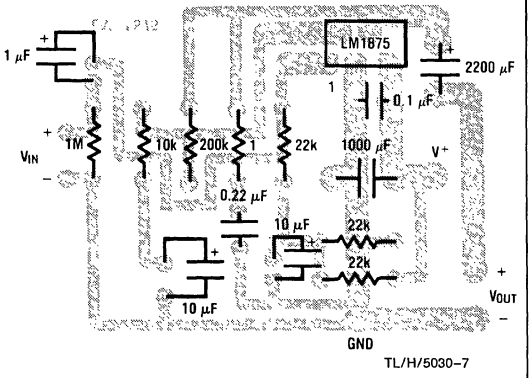
Single Supply



TL/H/5030–7

National Semiconductor Corporation

LM1877 Dual Power Audio Amplifier

General Description

The LM1877 is a monolithic dual power amplifier designed to deliver 2W/channel continuous into 8Ω loads. The LM1877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection, and output Q point centering. The LM1877 is internally compensated for all gains greater than 10.

Features

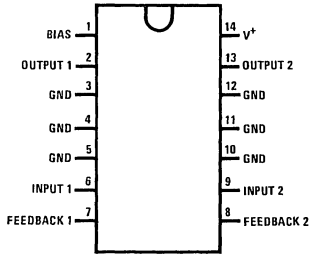
- 2W/channel
- −65 dB ripple rejection, output referred
- −65 dB channel separation, output referred
- Wide supply range, 6V–24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

Dual-In-Line Package



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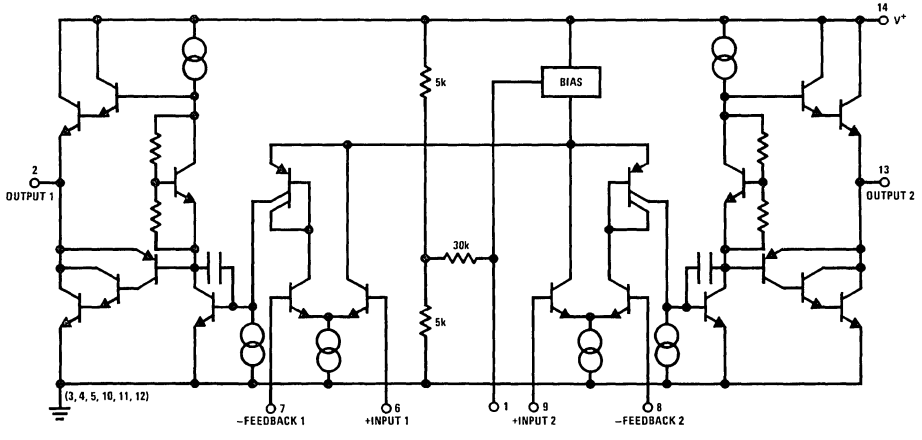
Top View

Order Number LM1877N-9
See NS Package Number N14A

Equivalent Schematic Diagram



TL/H/7913–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

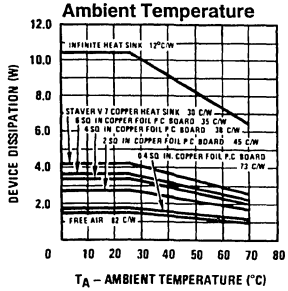
V_S = 20V, T_A = 25°C, (See Note 1) R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		25	50	mA
Output Power LM1877	THD = 10% V_S = 20V, R_L = 8Ω	2.0			W/Ch
Total Harmonic Distortion LM1877	f = 1 kHz, V_S = 14V				
	P_O = 50 mW/Channel		0.075		%
	P_O = 500 mW/Channel		0.045		%
	P_O = 1 W/Channel		0.055		%
Output Swing	R_L = 8Ω		V_S −6		Vp-p
Channel Separation	C_F = 50 μF, C_{IN} = 0.1 μF, f = 1 kHz, Output Referred				
	V_S = 20V, V_O = 4 Vrms	−50	−70		dB
	V_S = 7V, V_O = 0.5 Vrms		−60		dB
PSRR Power Supply Rejection Ratio	C_F = 50 μF, C_{IN} = 0.1 μF, f = 120 Hz, Output Referred				
	V_S = 20V, V_{RIPPLE} = 1 Vrms	−50	−65		dB
	V_S = 7V, V_{RIPPLE} = 0.5 Vrms		−40		dB
Noise	Equivalent Input Noise				
	R_S = 0, C_{IN} = 0.1 μF, BW = 20 Hz–20 kHz, Output Noise Wideband		2.5		μV
	R_S = 0, C_N = 0.1 μF, A_V 200		0.80		mV
Open Loop Gain	R_S = 0, f = 100 kHz, R_L = 8Ω		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	V_S = 20V	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

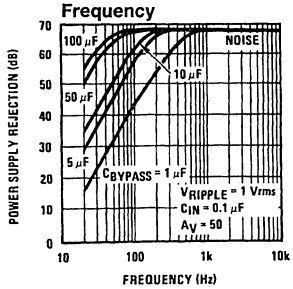
Note 1: For operation at ambient temperature greater than 25°C, the LM1877 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Typical Performance Characteristics

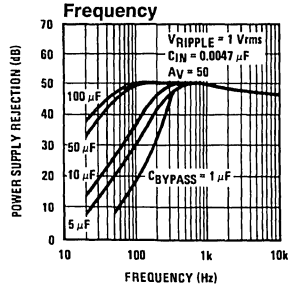
Device Dissipation vs Ambient Temperature



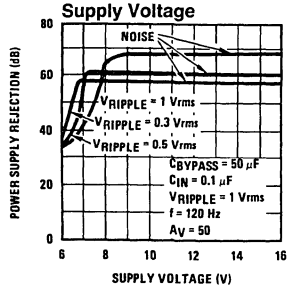
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



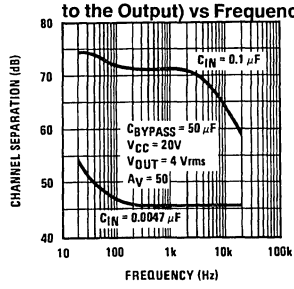
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



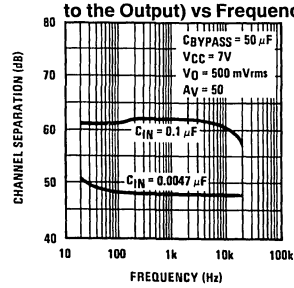
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



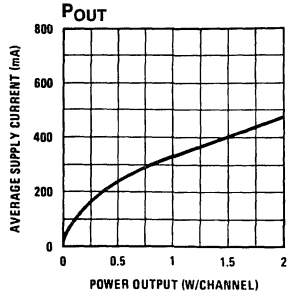
Channel Separation (Referred to the Output) vs Frequency



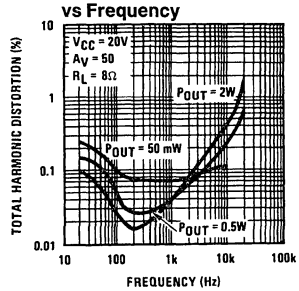
Channel Separation (Referred to the Output) vs Frequency



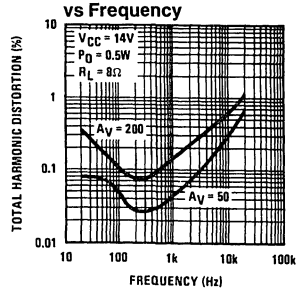
Average Supply Current vs P_{OUT}



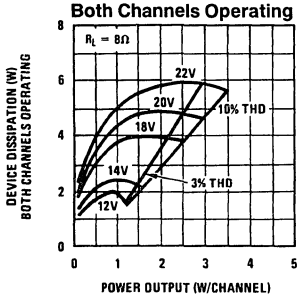
Total Harmonic Distortion vs Frequency



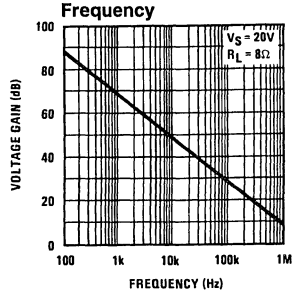
Total Harmonic Distortion vs Frequency



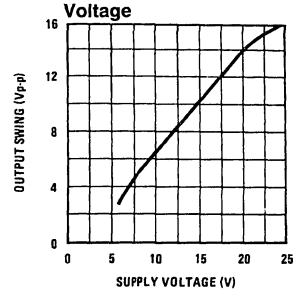
Power Dissipation (W) Both Channels Operating



Open Loop Gain vs Frequency



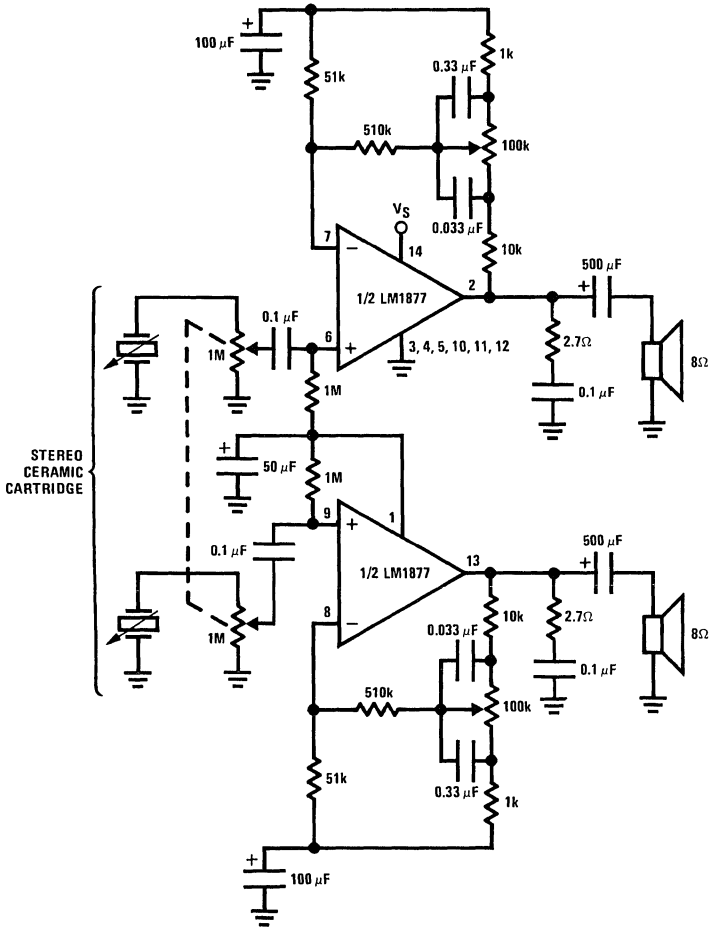
Output Swing vs Supply Voltage



TL/H/7913–3

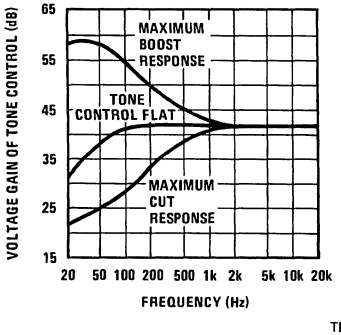
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control



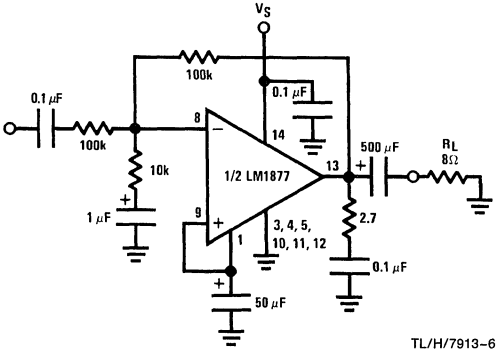
TL/H/7913–4

Frequency Response of Bass Tone Control



TL/H/7913–5

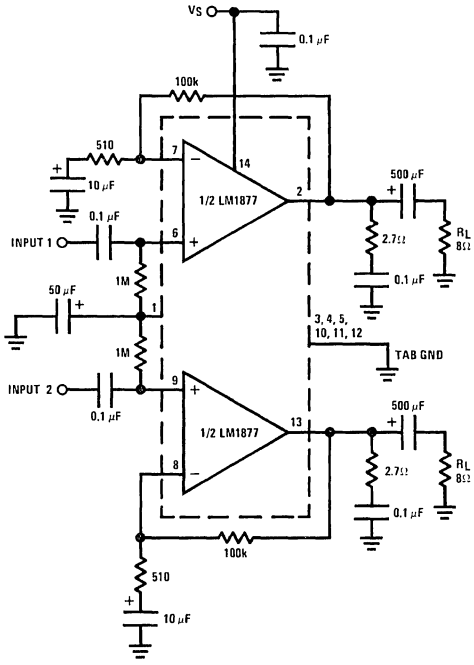
Inverting Unity Gain Amplifier



TL/H/7913–6

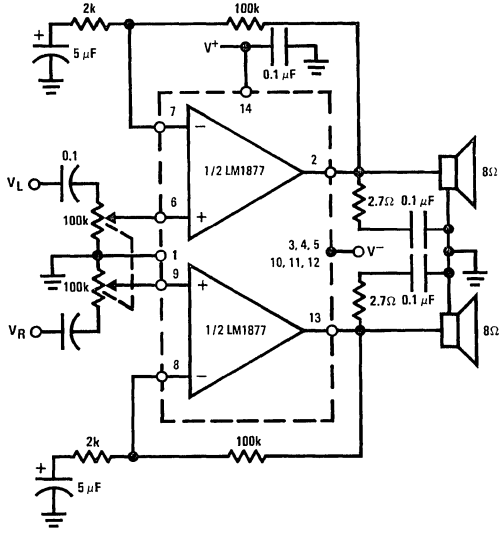
Typical Applications (Continued)

Stereo Amplifier with $A_V = 200$



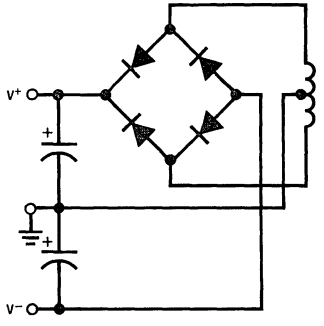
TL/H/7913–7

Non-Inverting Amplifier Using Split Supply



TL/H/7913–8

Typical Split Supply



TL/H/7913–9

National Semiconductor Corporation

DNR® DYNAMIC NOISE REDUCTION SYSTEM

LM1894 Dynamic Noise Reduction System DNR®

General Description

The LM1894 is a stereo noise reduction circuit for use with audio playback systems. The DNR system is non-complementary, meaning it does not require encoded source material. The system is compatible with virtually all prerecorded tapes and FM broadcasts. Psychoacoustic masking, and an adaptive bandwidth scheme allow the DNR to achieve 10 dB of noise reduction. DNR can save circuit board space and cost because of the few additional components required.

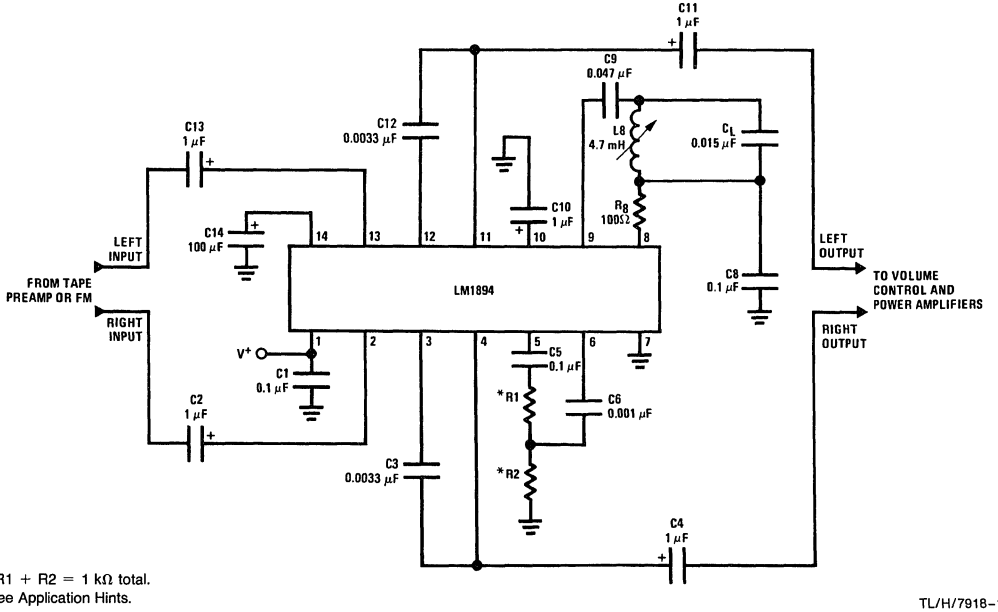
Features

- Non-complementary noise reduction, "single ended"
- Low cost external components, no critical matching
- Compatible with all prerecorded tapes and FM
- 10 dB effective tape noise reduction CCIR/ARM weighted
- Wide supply range, 4.5V to 18V
- 1 Vrms input overload

Applications

- Automotive radio/tape players
- Compact portable tape players
- Quality HI-FI tape systems
- VCR playback noise reduction
- Video disc playback noise reduction

Typical Application



*R1 + R2 = 1 kΩ total.
See Application Hints.

TL/H/7918–1

FIGURE 1. Component Hook-Up for Stereo DNR System

Order Number LM1894M or LM1894N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	20V
Input Voltage Range, V_{pk}	$V_S/2$
Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics

V_S = 8V, T_A = 25°C, V_{IN} = 300 mV at 1 kHz, circuit shown in *Figure 1* unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Range		4.5	8	18	V
Supply Current	V_S = 8V		17	30	mA
MAIN SIGNAL PATH					
Voltage Gain	DC Ground Pin 9, Note 2	−0.9	−1	−1.1	V/V
DC Output Voltage		3.7	4.0	4.3	V
Channel Balance	DC Ground Pin 9	−1.0		1.0	dB
Minimum Balance	AC Ground Pin 9 with 0.1 μF Capacitor, Note 2	675	965	1400	Hz
Maximum Bandwidth	DC Ground Pin 9, Note 2	27	34	46	kHz
Effective Noise Reduction	CCIR/ARM Weighted, Note 3		−10	−14	dB
Total Harmonic Distortion	DC Ground Pin 9		0.05	0.1	%
Input Headroom	Maximum V_{IN} for 3% THD AC Ground Pin 9		1.0		Vrms
Output Headroom	Maximum V_{OUT} for 3% THD DC Ground Pin 9		V_S − 1.5		Vp-p
Signal to Noise	BW = 20 Hz–20 kHz, re 300 mV				
	AC Ground Pin 9		79		dB
	DC Ground Pin 9		77		dB
	CCIR/ARM Weighted re 300 mV Note 4				
	AC Ground Pin 9	82	88		dB
	DC Ground Pin 9	70	76		dB
	CCIR Peak, re 300 mV, Note 5				
	AC Ground Pin 9		77		dB
	DC Ground Pin 9		64		dB
Input Impedance	Pin 2 and Pin 13	14	20	26	kΩ
Channel Separation	DC Ground Pin 9	−50	−70		dB
Power Supply Rejection	C14 = 100 μF, V_{RIPPLE} = 500 mVrms, f = 1 kHz	−40	−56		dB
Output DC Shift	Reference DVM to Pin 14 and Measuree Output DC Shift from Minimum to Maximum Bandwidth, Note 6.		4.0	20	mV

Electrical Characteristics

V_S = 8V, T_A = 25°C, V_{IN} = 300 mV at 1 kHz, circuit shown in *Figure 1* unless otherwise specified (Continued)

Parameter	Conditions	Min	Typ	Max	Units
CONTROL SIGNAL PATH					
Summing Amplifier Voltage Gain	Both Channels Driven	0.9	1	1.1	V/V
Gain Amplifier Input Impedance	Pin 6	24	30	39	kΩ
Voltage Gain	Pin 6 to Pin 8	21.5	24	26.5	V/V
Peak Detector Input Impedance	Pin 9	560	700	840	Ω
Voltage Gain	Pin 9 to Pin 10	30	33	36	V/V
Attack Time	Measured to 90% of Final Value with 10 kHz Tone Burst	300	500	700	μs
Decay Time	Measured to 90% of Final Value with 10 kHz Tone Burst	45	60	75	ms
DC Voltage Range	Minimum Bandwidth to Maximum Bandwidth	1.1		3.8	V

Note 1: For operation in ambient temperature above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 1) 80°C/W junction to ambient for the dual-in-line package, and 2) 105°C/W junction to ambient for the small outline package.

Note 2: To force the DNR system into maximum bandwidth, DC ground the input to the peak detector, pin 9. A negative temperature coefficient of −0.5%/°C on the bandwidth, reduces the maximum bandwidth at increased ambient temperature or higher package dissipation. AC ground pin 9 or pin 6 to select minimum bandwidth. To change minimum and maximum bandwidth, see Appliction Hints.

Note 3: The maximum noise reduction CCIR/ARM weighted is about 14 dB. This is accomplished by changing the bandwidth from maximum to minimum. In actual operation, minimum bandwidth is not selected, a nominal minimum bandwidth of about 2 kHz gives −10 dB of noise reduction. See Application Hints.

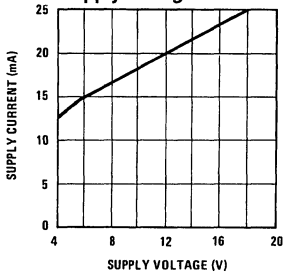
Note 4: The CCIR/ARM weighted noise is measured with a 40 dB gain amplifier between the DNR system and the CCIR weighting filter; it is then input referred.

Note 5: Measured using the Rhode-Schwartz psophometer.

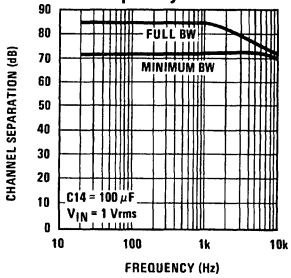
Note 6: Pin 10 is DC forced half way between the maximum bandwidth DC level and minimum bandwidth DC level. An AC 1 kHz signal is then applied to pin 10. Its peak-to-peak amplitude is V_{DC} (max BW) − V_{DC} (min BW).

Typical Performance Characteristics

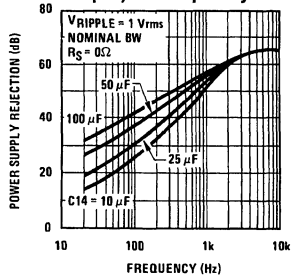
Supply Current vs Supply Voltage



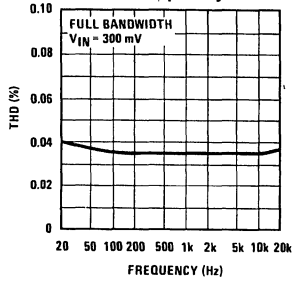
Channel Separation (Referred to the Output) vs Frequency



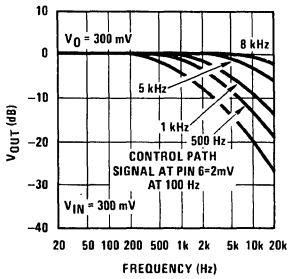
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



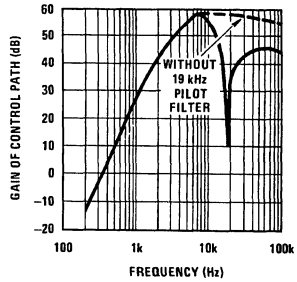
THD vs Frequency



−3 dB Bandwidth vs Frequency and Control Signal



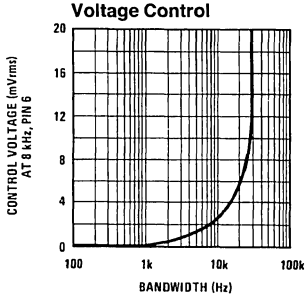
Gain of Control Path vs Frequency (with 10 kHz FM Pilot Filter)



TL/H/7918–2

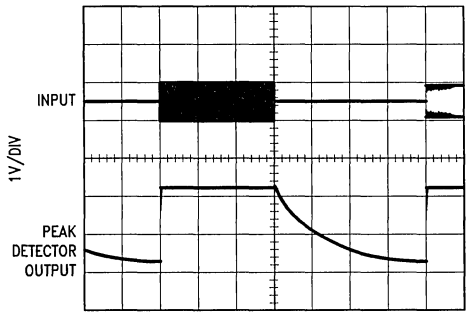
Typical Performance Characteristics (Continued)

Main Signal Path Bandwidth vs Voltage Control



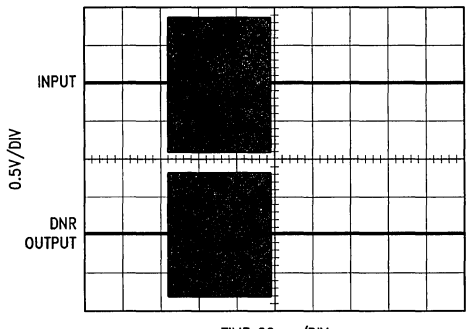
TL/H/7918–3

Peak Detector Response



TL/H/7918–4

Output Response



TL/H/7918–5

External Component Guide *(Figure 1)*

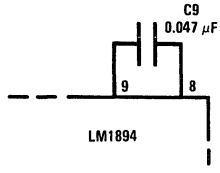
Component	Value	Purpose
C1	0.1 μF–100 μF	May be part of power supply, or may be added to suppress power supply oscillation.
C2, C13	1 μF	Blocks DC, pin 2 and pin 13 are at DC potential of $V_S/2$. C2, C13 form a low frequency pole with 20k R_{IN}. $f_L = \frac{1}{2\pi\ C2\ R_{IN}}$
C14	25 μF–100 μF	Improves power supply rejection.
C3, C12	0.0033 μF	Forms integrator with internal gm block and op amp. Sets bandwidth conversion gain of 33 Hz/μA of gm current.
C4, C11	1 μF	Output coupling capacitor. Output is at DC potential of $V_S/2$.
C5	0.1 μF	Works with R1 and R2 to attenuate low frequency transients which could disturb control path operation. $f_5 = \frac{1}{2\pi\ C5\ (R1 + R2)} = 1.6\ kHz$
C6	0.001 μF	Works with input resistance of pin 6 to form part of control path frequency weighting. $f_6 = \frac{1}{2\pi\ C6\ R1_{PIN\ 6}} = 5.3\ kHz$
C8	0.1 μF	Combined with L8 and C_L forms 19 kHz filter for FM pilot. This is only required in FM applications (Note 1).

External Component Guide (Figure 1)
(Continued)

Component	Value	Purpose
L8, C_L	4.7 mH, 0.015 μF	Forms 19 kHz filter for FM pilot. L8 is Toko coil CAN-1A185HM* (Note 1).
C9	0.047 μF	Works with input resistance of pin 9 to form part of control path frequency weighting. $f_9 = \frac{1}{2\pi\ C9\ R_{PIN\ 9}} = 4.8$ kHz
C10	1 μF	Set attack and decay time of peak detector.
R1, R2	1 kΩ	Sensitivity resistors set the noise threshold. Reducing attentuation causes larger signals to be peak detected and larger bandwidth in main signal path. Total value of R1 + R2 should equal 1 kΩ.
R8	100Ω	Forms RC roll-off with C8. This is only required in FM applications.

* Toko America Inc., 1250 Feehanville Drive, Mt. Prospect IL 60056

Note 1: When FM applications are not required, pin 8 and pin 9 hook-up as follows:



TL/H/7918–6

Circuit Operation

The LM1894 has two signal paths, a main signal path and a bandwidth control path. The main path is an audio low pass filter comprised of a gm block with a variable current, and an op amp configured as an integrator. As seen in *Figure 2*, DC feedback constrains the low frequency gain to $A_V = -1$. Above the cutoff frequency of the filter, the output decreases at −6 dB/oct due to the action of the 0.0033 μF capacitor.

The purpose of the control paths is to generate a bandwidth control signal which replicates the ear's sensitivity to noise in the presence of a tone. A single control path is used for both channels to keep the stereo image from wandering. This is done by adding the right and left channels together in the summing amplifier of *Figure 2*. The R1, R2 resistor divider adjusts the incoming noise level to open slightly the bandwidth of the low pass filter. Control path gain is about 60 dB and is set by the gain amplifier and peak detector gain. This large gain is needed to ensure the low pass filter bandwidth can be opened by very low noise floors. The capacitors between the summing amplifier output and the peak detector input determine the frequency weighting as shown in the typical performance curves. The 1 μF capacitor at pin 10, in conjunction with internal resistors, sets the attack and decay times. The voltage is converted into a proportional current which is fed into the gm blocks. The bandwidth sensitivity to gm current is 33 Hz/μA. In FM stereo applications at 19 kHz pilot filter is inserted between pin 8 and pin 9 as shown in *Figure 1*.

Figure 3 is an interesting curve and deserves some discussion. Although the output of the DNR system is a linear function of input signal, the −3 dB bandwidth is not. This is due to the non-linear nature of the control path. The DNR system has a uniform frequency response, but looking at the −3 dB bandwidth on a steady state basis with a single frequency input can be misleading. It must be remembered that a single input frequency can only give a single −3 dB bandwidth and the roll-off from this point must be a smooth −6 dB/oct.

A more accurate evaluation of the frequency response can be seen in *Figure 4*. In this case the main signal path is frequency swept, while the control path has a constant frequency applied. It can be seen that different control path frequencies each give a distinctive gain roll-off.

Psychoacoustic Basics

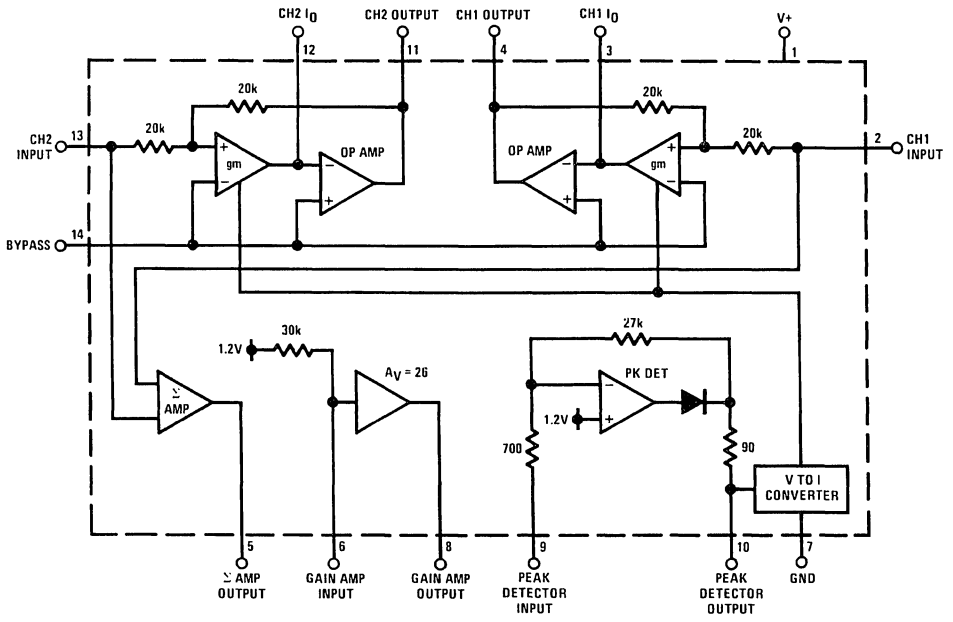
The dynamic noise reduction system is a low pass filter that has a variable bandwidth of 1 kHz to 30 kHz, dependent on music spectrum. The DNR system operates on three principles of psychoacoustics.

1. White noise can mask pure tones. The total noise energy required to mask a pure tone must equal the energy of the tone itself. Within certain limits, the wider the band of masking noise about the tone, the lower the noise amplitude need be. As long as the total energy of the noise is equal to or greater than the energy of the tone, the tone will be inaudible. This principle may be turned around; when music is present, it is capable of masking noise in the same bandwidth.

2. The ear cannot detect distortion for less than 1 ms. On a transient basis, if distortion occurs in less than 1 ms, the ear acts as an integrator and is unable to detect it. Because of this, signals of sufficient energy to mask noise open bandwidth to 90% of the maximum value in less than 1 ms. Reducing the bandwidth to within 10% of its minimum value is done in about 60 ms: long enough to allow the ambience of the music to pass through, but not so long as to allow the noise floor to become audible.

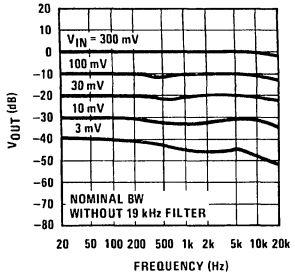
3. Reducing the audio bandwidth reduces the audibility of noise. Audibility of noise is dependent on noise spectrum, or how the noise energy is distributed with frequency. Depending on the tape and the recorder equalization, tape noise spectrum may be slightly rolled off with frequency on a per octave basis. The ear sensitivity on the other hand greatly increases between 2 kHz and 10 kHz. Noise in this region is extremely audible. The DNR system low pass filters this noise. Low frequency music will not appreciably open the DNR bandwidth, thus 2 kHz to 20 kHz noise is not heard.

Block Diagram



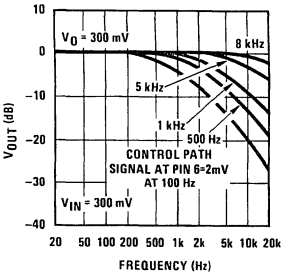
TL/H/7918–7

FIGURE 2



TL/H/7918–8

FIGURE 3. Output vs Frequency



TL/H/7918–9

FIGURE 4. −3 dB Bandwidth vs Frequency and Control Signal

Application Hints

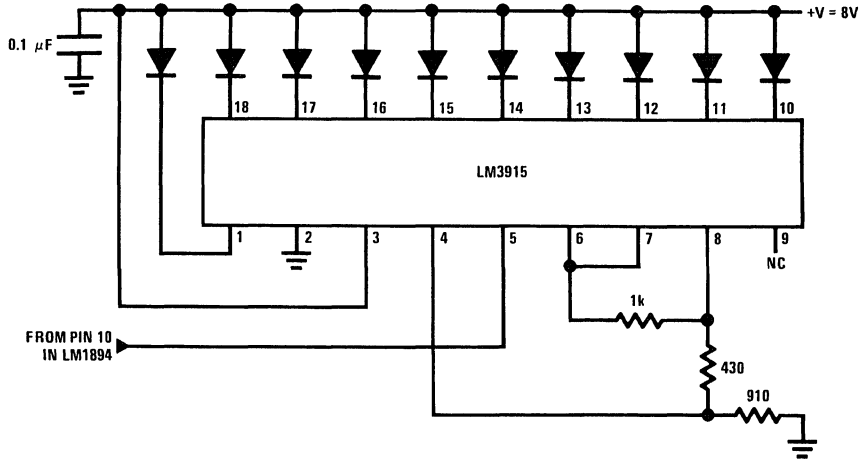
The DNR system should always be placed before tone and volume controls as shown in *Figure 1*. This is because any adjustment of these controls would alter the noise floor seen by the DNR control path. The sensitivity resistors R1 and R2 may need to be switched with the input selector, depending on the noise floors of different sources, i.e., tape, FM, phono. To determine the value of R1 and R2 in a tape system for instance; apply tape noise (no program material) and adjust the ratio of R1 and R2 to open slightly the bandwidth of the main signal path. This can easily be done by viewing the capacitor voltage of pin 10 with an oscilloscope, or by using the circuit of *Figure 5*. This circuit gives an LED display of the voltage on the peak detector capacitor. Adjust the values of R1 and R2 (their sum is always 1 kΩ) to light the LEDs of pin 1 and pin 18. The LED bar graph does not indicate signal level, but rather instantaneous bandwidth of the two filters; it should not be used as a signal-level indicator. For greater flexibility in setting the bandwidth sensitivity, R1 and R2 could be replaced by a 1 kΩ potentiometer.

To change the minimum and maximum value of bandwidth, the integrating capacitors, C3 and C12, can be scaled up or down. Since the bandwidth is inversely proportional to the capacitance, changing this 0.0039 μF capacitor to 0.0033 μF will change the typical bandwidth from 965 Hz–34 kHz to 1.1 kHz–40 kHz. With C3 and C12 set at 0.0033 μF, the maximum bandwidth is typically 34 kHz. A double pole double throw switch can be used to completely bypass DNR.

The capacitor on pin 10 in conjunction with internal resistors sets the attack and decay times. The attack time can be altered by changing the size of C10. Decay times can be decreased by paralleling a resistor with C10, and increased by increasing the value of C10.

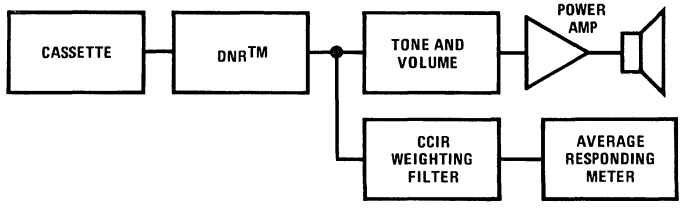
Application Hints (Continued)

When measuring the amount of noise reduction of the DNR system, the frequency response of the cassette should be flat to 10 kHz. The CCIR weighting network has substantial gain to 8 kHz and any additional roll-off in the cassette player will reduce the benefits of DNR noise reduction. A typical signal-to-noise measurement circuit is shown in *Figure 6*. The DNR system should be switched from maximum bandwidth to nominal bandwidth with tape noise as a signal source. The reduction in measured noise is the signal-to-noise ratio improvement.



TL/H/7918–10

FIGURE 5. Bar Graph Display of Peak Detector Voltage



TL/H/7918–11

FIGURE 6. Technique for Measuring S/N Improvement of the DNR System

Application Hints (Continued)

FOR FURTHER READING

Tape Noise Levels

1. "A Wide Range Dynamic Noise Reduction System", Blackmer, *'dB' Magazine,* August-September 1972, Volume 6, #8.

2. "Dolby B-Type Noise Reduction System", Berkowitz and Gundry, *Sert Journal,* May-June 1974, Volume 8.

3. "Cassette vs Elcaset vs Open Reel", Toole, *Audioscene Canada,* April 1978.

4. "CCIR/ARM: A Practical Noise Measurement Method", Dolby, Robinson, Gundry, *JAES,* 1978.

Noise Masking

1. "Masking and Discrimination", Bos and De Boer, *JAES,* Volume 39, #4, 1966.

2. "The Masking of Pure Tones and Speech by White Noise", Hawkins and Stevens, *JAES,* Volume 22, #1, 1950.

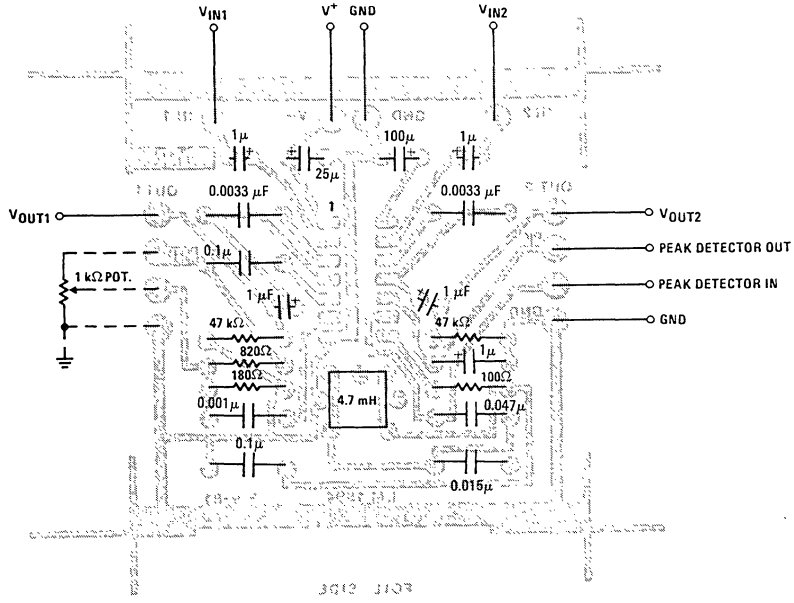
3. "Sound System Engineering", Davis Howard W. Sams and Co.

4. "High Quality Sound Reproduction", Moir, Chapman Hall, 1960.

5. "Speech and Hearing in Communication", Fletcher, Van Nostrand, 1953.

Printed Circuit Layout

DNR Component Diagram



TL/H/7918–12

National Semiconductor Corporation

LM1895/LM2895 Audio Power Amplifier

General Description

The LM1895 is a 6V audio power amplifier designed to deliver 1W into 4Ω. Utilizing a unique patented compensation scheme, the LM1895 is ideal for sensitive AM radio applications. This new circuit technique exhibits lower noise, lower distortion, and less AM radiation than conventional designs. The amplifier's supply range (3V–9V) is ideal for battery operation. The LM1895 is packaged in an 8-pin miniDIP for minimum PC board space. For higher supplies (V_S > 9V) the LM2895 is available in an 11-lead single-in-line package. The 11-lead package has been redesigned, resulting in a slightly degraded thermal characteristic shown in the figure Device Dissipation vs Ambient Temperature.

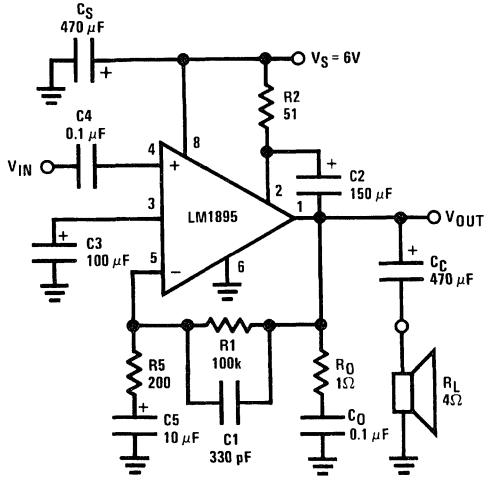
Features

- Guaranteed low crossover distortion
- Low AM radiation
- Low noise
- 3V, 4Ω, P_O = 250 mW
- Wide supply operation 3V–15V (LM2895)
- Low distortion
- No turn on "pop"
- Smooth waveform clipping
- 8-pin miniDIP (LM1895)
- 12V, 4Ω, P_O = 4W (LM2895)
- Tested for low crossover distortion

Applications

- Compact AM-FM radios
- Battery operated tape player amplifiers
- Line driver

Typical Applications



TL/H/7919–1

FIGURE 1. LM1895 with A_V = 500, BW = 5 kHz, AM Radio Application (V_{IN} = 4.2 mV for Full Power Output)

Order Number LM1895N or LM2895P
See NS Package Number N08E or P11A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage
- LM1895 $V_S = 12V$
- LM2895 $V_S = 18V$

Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

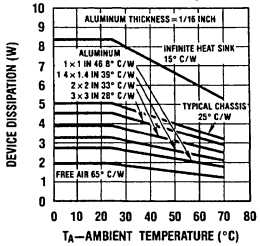
Unless otherwise specified, $T_A = 25°C$, $A_V = 200$ (46 dB). For the LM1895, $V_S = 6V$ and $R_L = 4\Omega$. For the LM2895, $T_{TAB} = 25°C$, $V_S = 12V$ and $R_L = 4\Omega$. Test circuit shown in *Figure 2*.

Parameter	Conditions	LM1895			LM2895			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Current	P_O = W		8	14		12	20	mA
Operating Supply Voltage		3		10	3		15	V
Output Power	THD = 10%, f = 1 kHz							
LM1895N	V_S = 6V, $R_L = 4\Omega$ } $T_A = 25°C$	0.9	1.1					W
	V_S = 9V, $R_L = 8\Omega$ } $T_A = 25°C$		1.1					W
LM2895P	V_S = 12V, $R_L = 4\Omega$ } $T_{TAB} = 25°C$				3.6	4.3		W
	V_S = 12V, $R_L = 8\Omega$ } $T_{TAB} = 25°C$					2.5		W
Distortion	f = 1 kHz							
	P_O = 50 mW		0.27			0.27		%
	P_O = 0.5W		0.20			0.20		%
	P_O = 1.0W					0.15		%
	f = 20 kHz, P_O = 100 mW, V_S = 3.6V			3.0			3.0	%
Crossover Distortion	f = 20 kHz, $R_L = 4\Omega$, P_O = 100 mW, V_{CC} = 3.6V			3			3	%
Power Supply Rejection Ratio (PSRR)	C_{BY} = 100 μF, f = 1 kHz, C_{IN} = 0.1 μF Output Referred, V_{RIPPLE} = 250 mV	40	52		40	52		dB
Noise	Equivalent Input Noise R_S = 0,							
	C_{IN} = 0.1 μF, BW = 20 −20 kHz		1.4			1.4		μV
	CCIR/ARM		1.4			1.4		μV
	Wideband		2.0			2.0		μV
DC Output Level		2.8	3.0	3.2	5.6	6.0	6.4	V
Input Impedance		50	150	350	50	150	350	kΩ
Input Offset Voltage			5			5		mV
Input Bias Current			120			120		nA

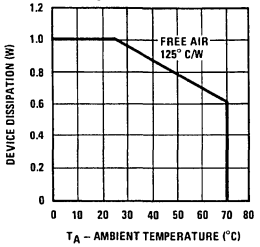
Note 1: For operation at ambient temperature greater than 25°C, the LM1895/LM2895 must be derated based on a maximum junction temperature using a thermal resistance which depends upon mounting techniques.

Typical Performance Characteristics

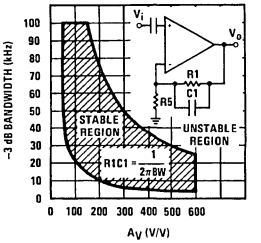
LM2895 Device Dissipation vs Ambient Temperature



LM1895 Maximum Device Dissipation vs Ambient Temperature



−3 dB Bandwidth vs Voltage Gain for Stable Operation



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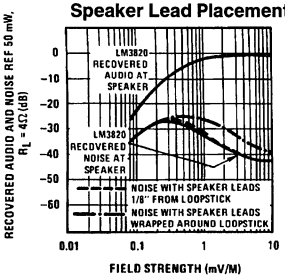
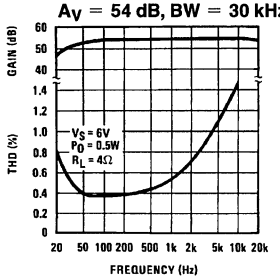
Typical Performance Characteristics (Continued)

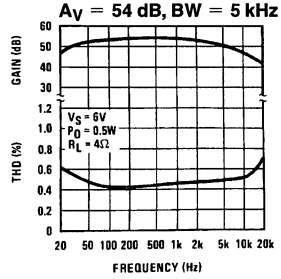
AM Recovered Audio and Noise vs Field Strength for Different Speaker Lead Placement



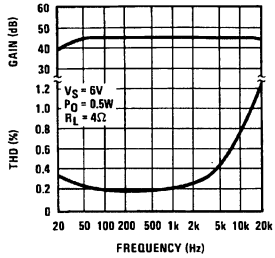
THD and Gain vs Frequency A_V = 54 dB, BW = 30 kHz



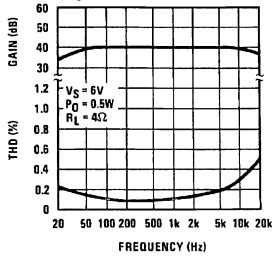
THD and Gain vs Frequency A_V = 54 dB, BW = 5 kHz



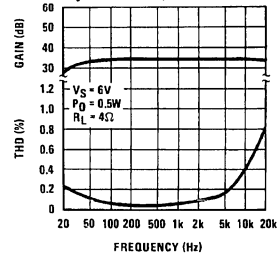
THD and Gain vs Frequency A_V = 46 dB, BW = 30 kHz



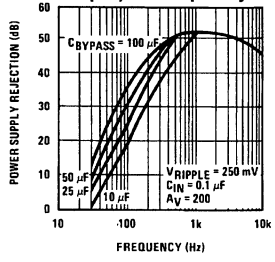
THD and Gain vs Frequency A_V = 40 dB, BW = 20 kHz



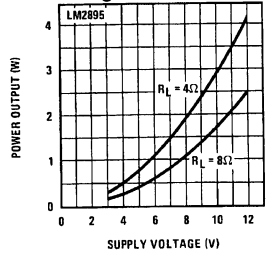
THD and Gain vs Frequency A_V = 34 dB, BW = 50 kHz



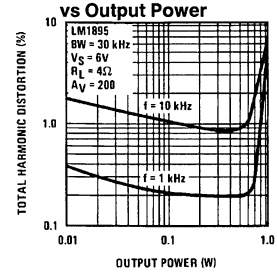
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



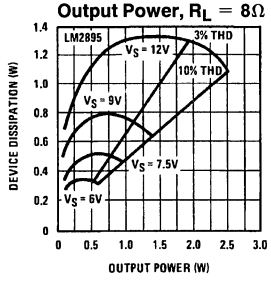
Power Output vs Supply Voltage



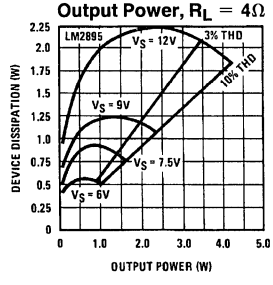
Total Harmonic Distortion vs Output Power



Power Dissipation vs Output Power, R_L = 8Ω

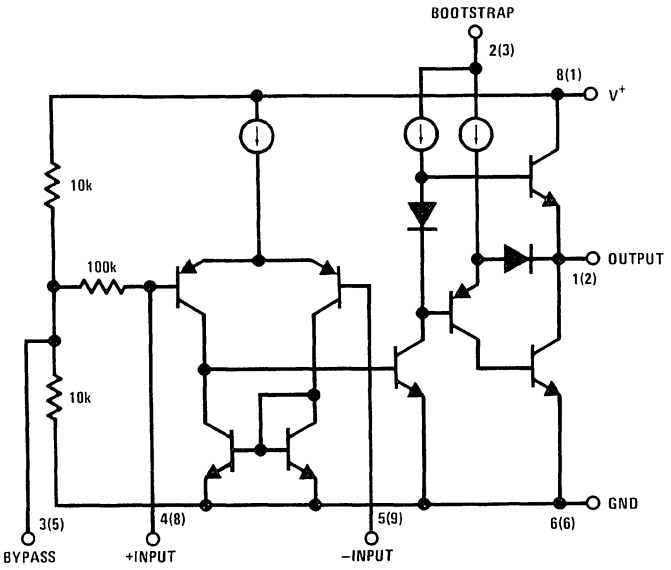


Power Dissipation vs Output Power, R_L = 4Ω



TL/H/7919–3

Equivalent Schematic



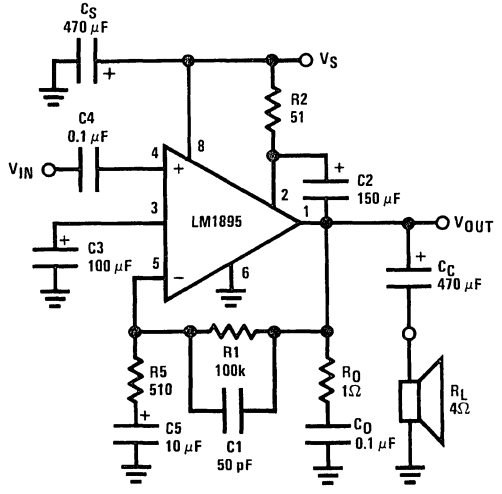
TL/H/7919–4

Pin 7 no connection on LM1895

Pins 4, 7, 10, 11 no connection on LM2895

( ) indicates pin number for LM2895

Typical Applications (Continued)



TL/H/7919–5

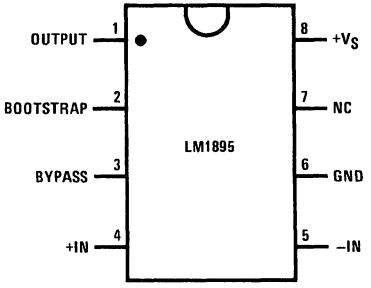
FIGURE 2. Amplifier with A_V = 200, BW = 30 kHz

External Components *(Figure 2)*

Components	Comments
1. R1, R5	Sets voltage gain, $A_V = 1 + R1/R5$
2. R2	Bootstrap resistor sets drive current for output stage and allows pin 2 to go above V_S
3. R_O	Works with C_O to stabilize output stage
4. C4	Input coupling capacitor. Pin 4 is at a DC potential of $V_S/2$. Low frequency pole set by: $f_L = \frac{1}{2\pi R_{IN}C4}$
5. C5	Feedback capacitor. Ensure unity gain at DC. Also a low frequency pole at: $f_L = \frac{1}{2\pi R5C5}$
6. C2	Bootstrap capacitor, used to increase drive to output stage. A low frequency pole is set by: $f_L = \frac{1}{2\pi R2C2}$
7. C1	Compensation capacitor. This stabilizes the amplifier and adjusts the bandwidth. See curve of bandwidth vs allowable gain
8. C3	Improves power supply rejection. (See Typical Performance Curves). Increasing C3 increases turn-on delay
9. C_C	Output coupling capacitor. Isolates pin 1 from the load. Low frequency pole set by: $f_L = \frac{1}{2\pi C_C R_L}$
10. C_O	Works with R_O to stabilize output stage
11. C_S	Provides power supply filtering

Connection Diagrams

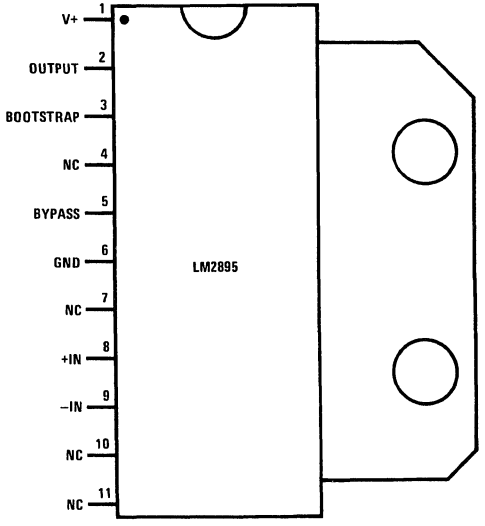
Dual-In-Line Package



TL/H/7919–6

Top View

Single-In-Line Package



TL/H/7919–7

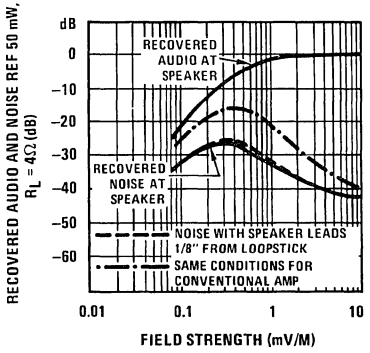
Top View

Application Hints

AM Radios

The LM1895/LM2895 have been designed to fill a wide range of audio power applications. A common problem with IC audio power amplifiers has been poor signal-to-noise performance when used in AM radio applications. In a typical radio application, the loopstick antenna is in close proximity to the audio amplifier. Current flowing in the speaker and power supply leads can cause electromagnetic coupling to the loopstick, resulting in system oscillation. In addition, most audio power amplifiers are not optimized for lowest noise because of compensation requirements. If noise from the audio amplifier radiates into the AM section, the sensitivity and signal-to-noise ratio will be degraded.

The LM1895 exhibits extremely low wideband noise due in part to an external capacitor C1 which is used to tailor the bandwidth. The circuit shown in *Figure 2* is capable of a signal-to-noise ratio in excess of 60 dB referred to 50 mW. Capacitor C1 not only limits the closed loop bandwidth, it also provides overall loop compensation. Neglecting C5 in *Figure 2*, the gain is:



TL/H/7919–8

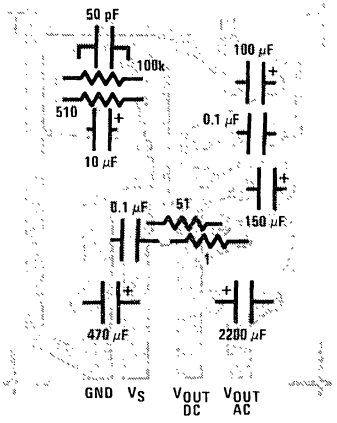
FIGURE 3. Improved AM Sensitivity Over Conventional Design

$$A_V(S) = \frac{S + A_V\omega_o}{S + \omega_o}$$

where $A_V = \frac{R1 + R5}{R5}$, $\omega_o = \frac{1}{R1C1}$

A curve of −3 dB BW (ω_o) vs A_V is shown in the Typical Performance Curves.

Figure 3 shows a plot of recovered audio as a function of field strength in μV/M. The receiver section in this example is an LM3820. The power amplifier is located about two inches from the loopstick antenna. Speaker leads run parallel to the loopstick and are 1/8 inch from it. Referenced to a 20 dB S/N ratio, the improvement in noise performance over conventional designs is about 10 dB. This corresponds to an increase in usable sensitivity of about 8.5 dB.



TL/H/7919–9

FIGURE 4. Printed Circuit Board Layout for LM1895

National Semiconductor Corporation

LM1896/LM2896 Dual Power Audio Amplifier

General Description

The LM1896 is a high performance 6V stereo power amplifier designed to deliver 1 watt/channel into 4Ω or 2 watts bridged monaural into 8Ω. Utilizing a unique patented compensation scheme, the LM1896 is ideal for sensitive AM radio applications. This new circuit technique exhibits lower wideband noise, lower distortion, and less AM radiation than conventional designs. The amplifier's wide supply range (3V–9V) is ideal for battery operation. For higher supplies (V_S > 9V) the LM2896 is available in an 11-lead single-in-line package. The LM2896 package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

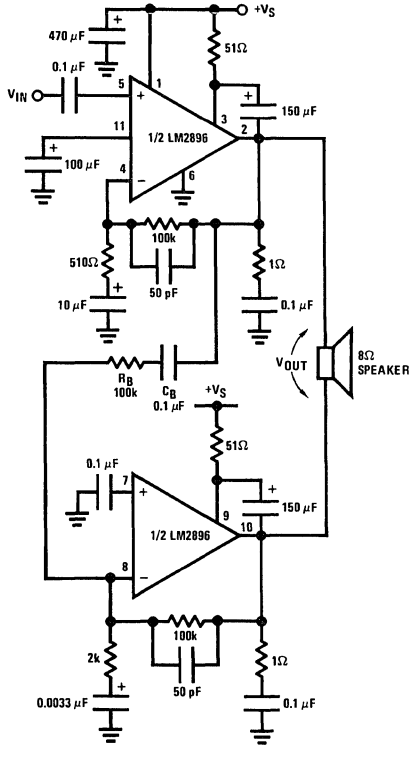
Features

- Low AM radiation
- Low noise
- 3V, 4Ω, stereo P_O = 250 mW
- Wide supply operation 3V–15V (LM2896)
- Low distortion
- No turn on "pop"
- Adjustable voltage gain and bandwidth
- Smooth waveform clipping
- P_O = 9W bridged, LM2896

Applications

- Compact AM-FM radios
- Stereo tape recorders and players
- High power portable stereos

Typical Applications



TL/H/7920–1

FIGURE 1. LM2896 in Bridge Configuration (A_V = 400, BW = 20 kHz)

Order Number LM1896N **Order Number LM2896P**
See NS Package Number N14A **See NS Package Number P11A**

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage
- LM1896 V_S = 12V
- LM2896 V_S = 18V

Operating Temperature (Note 1)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

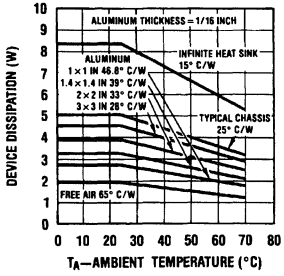
Unless otherwise specified, T_A = 25°C, A_V = 200 (46 dB). For the LM1896; V_S = 6V and R_L = 4Ω. For LM2896, T_{TAB} = 25°C, V_S = 12V and R_L = 8Ω. Test circuit shown in *Figure 2*.

Parameter	Conditions	LM1896			LM2896			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Current	P_O = 0W, Dual Mode		15	25		25	40	mA
Operating Supply Voltage		3		10	3		15	V
Output Power	THD = 10%, f = 1 kHz							
LM1896N-1	V_S = 6V, R_L = 4Ω Dual Mode, T_A = 25°C	0.9	1.1					W/ch
LM1896N-2	V_S = 6V, R_L = 8Ω Bridge Mode, T_A = 25°C		1.8	2.1				W
	V_S = 9V, R_L = 8Ω Dual Mode, T_A = 25°C		1.3					W/ch
LM2896P-1	V_S = 12V, R_L = 8Ω Dual Mode, T_{TAB} = 25°C				2.0	2.5		W/ch
LM2896P-2	V_S = 12V, R_L = 8Ω Bridge Mode, T_{TAB} = 25°C				7.2	9.0		W
	V_S = 9V, R_L = 4Ω Bridge Mode, T_{TAB} = 25°C					7.8		W
	V_S = 9V, R_L = 4Ω Dual Mode, T_{TAB} = 25°C					2.5		W/ch
Distortion	f = 1 kHz							
	P_O = 50 mW		0.09			0.09		%
	P_O = 0.5W		0.11			0.11		%
	P_O = 1W					0.14		%
Power Supply Rejection Ratio (PSRR)	C_{BY} = 100 μF, f = 1 kHz, C_{IN} = 0.1 μF Output Referred, V_{RIPPLE} = 250 mV	−40	−54		−40	−54		dB
Channel Separation	C_{BY} = 100 μF, f = 1 kHz, C_{IN} = 0.1 μF Output Referred	−50	−64		−50	−64		dB
Noise	Equivalent Input Noise R_S = 0, C_{IN} = 0.1 μF, BW = 20 − 20 kHz		1.4			1.4		μV
	CCIR/ARM		1.4			1.4		μV
	Wideband		2.0			2.0		μV
DC Output Level		2.8	3	3.2	5.6	6	6.4	V
Input Impedance		50	100	350	50	100	350	kΩ
Input Offset Voltage			5			5		mV
Voltage Difference between Outputs	LM1896N-2, LM2896P-2		10	20		10	20	mV
Input Bias Current			120			120		nA

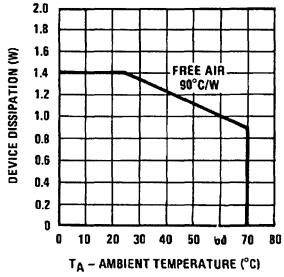
Note 1: For operation at ambient temperature greater than 25°C, the LM1896/LM2896 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon mounting techniques.

Typical Performance Curves

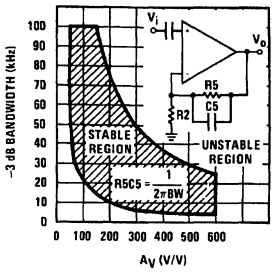
LM2896 Device Dissipation vs Ambient Temperature



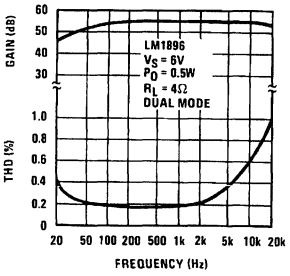
LM1896 Maximum Device Dissipation vs Ambient Temperature



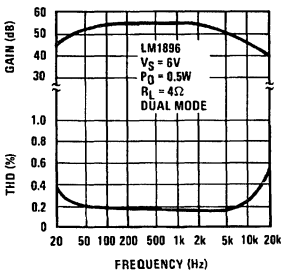
−3 dB Bandwidth vs Voltage Gain for Stable Operation



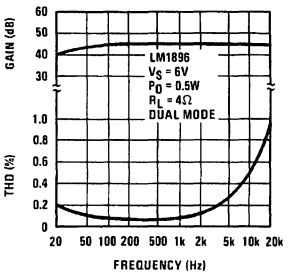
THD and Gain vs Frequency
A_V = 54 dB, BW = 30 kHz



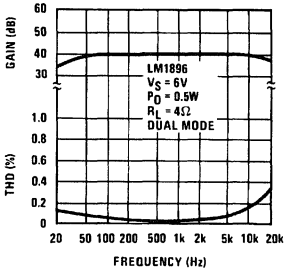
THD and Gain vs Frequency
A_V = 54 dB, BW = 5 kHz



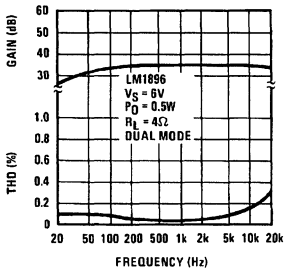
THD and Gain vs Frequency
A_V = 46 dB, BW = 50 kHz



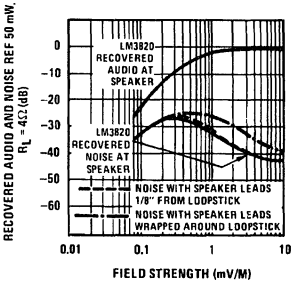
THD and Gain vs Frequency
A_V = 40 dB, BW = 20 kHz



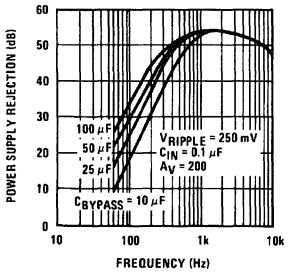
THD and Gain vs Frequency
A_V = 34 dB, BW = 50 kHz



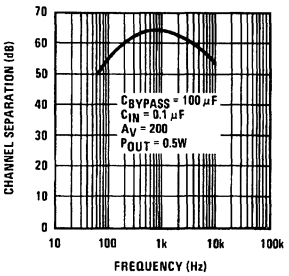
AM Recovered Audio and Noise vs Field Strength for Different Speaker Lead Placement



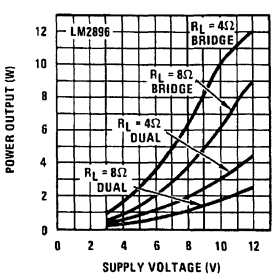
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



Channel Separation (Referred to the Output) vs Frequency



Power Output vs Supply Voltage



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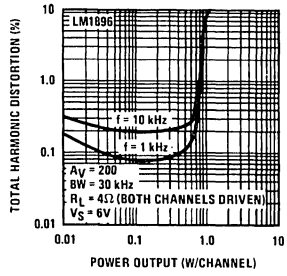
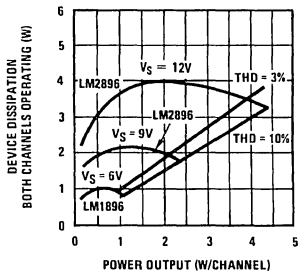
Typical Performance Curves (Continued)

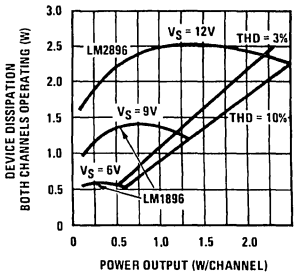
Total Harmonic Distortion vs Power Output



Power Dissipation vs Power Output $R_L = 4\Omega$



Power Dissipation vs Power Output $R_L = 8\Omega$



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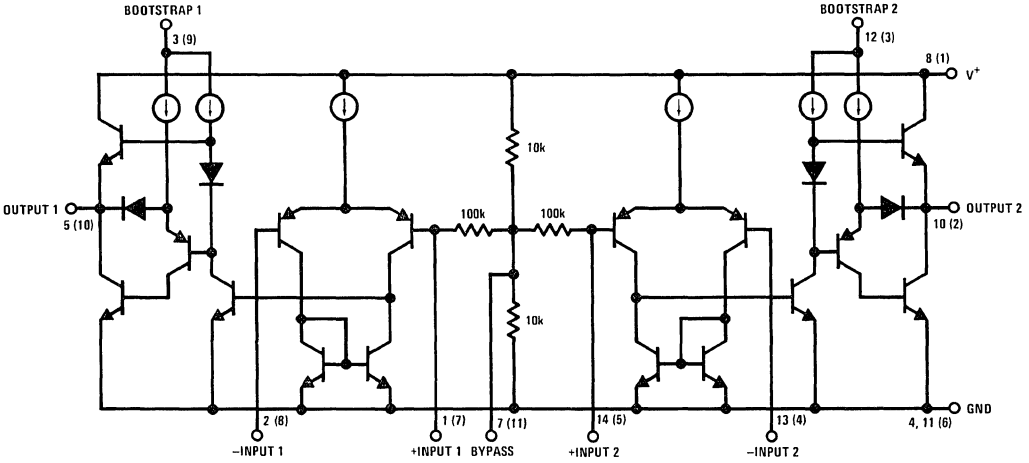
Equivalent Schematic



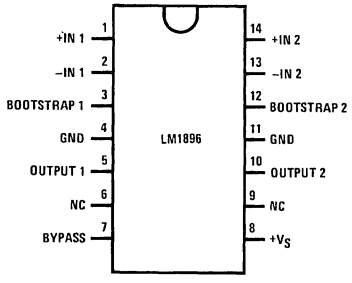
TL/H/7920–4

6, 9 No connection on LM1896

( ) indicates pin number for LM2896

Connection Diagrams

Dual-In-Line Package



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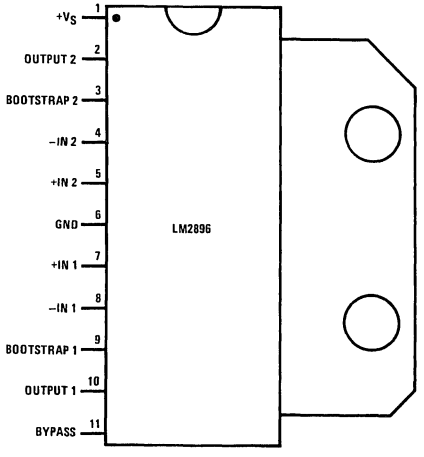
Top View

Single-In-Line Package



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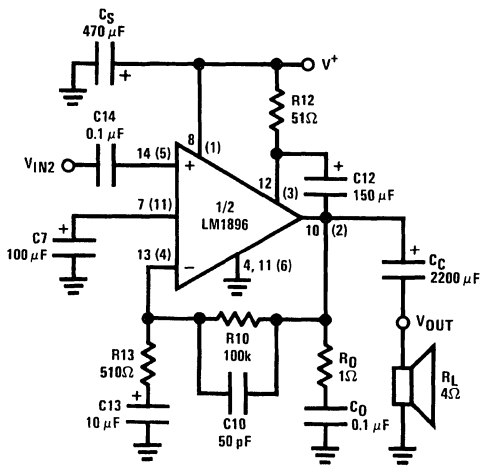
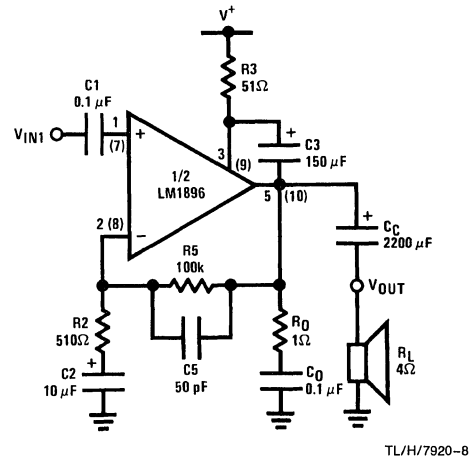
Top View

Typical Applications (Continued)



TL/H/7920–7



TL/H/7920–8

6, 9 No connection on LM1896

( ) Indicates pin number for LM2896

FIGURE 2. Stereo Amplifier with A_V = 200, BW = 30 kHz

External Components *(Figure 2)*

Components	Comments
1. R2, R5, R10, R13	Sets voltage gain, $A_V = 1 + R5/R2$ for one channel and $A_V = 1 + R10/R13$ for the other channel.
2. R3, R12	Bootstrap resistor sets drive current for output stage and allows pins 3 and 12 to go above V_S.
3. R_o	Works with C_o to stabilize output stage.
4. C1, C14	Input coupling capacitor. Pins 1 and 14 are at a DC potential of $V_S/2$. Low frequency pole set by: $f_L = \frac{1}{2\pi R_{IN} C1}$
5. C2, C13	Feedback capacitors. Ensure unity gain at DC. Also a low frequency pole at: $f_L = \frac{1}{2\pi R2C2}$
6. C3, C12	Bootstrap capacitors, used to increase drive to output stage. A low frequency pole is set by: $f_L = \frac{1}{2\pi R3C3}$
7. C5, C10	Compensation capacitor. These stabilize the amplifiers and adjust their bandwidth. See curve of bandwidth vs allowable gain.
8. C7	Improves power supply rejection (See Typical Performance Curves). Increasing C7 increases turn-on delay.
9. C_c	Output coupling capacitor. Isolates pins 5 and 10 from the load. Low frequency pole set by: $f_L = \frac{1}{2\pi C_c R_L}$
10. C_o	Works with R_o to stabilize output stage.
11. C_S	Provides power supply filtering.

Application Hints

AM Radios

The LM1896/LM2896 has been designed fo fill a wide range of audio power applications. A common problem with IC audio power amplifiers has been poor signal-to-noise performance when used in AM radio applications. In a typical radio application, the loopstick antenna is in close proximity to the audio amplifer. Current flowing in the speaker and power supply leads can cause electromagnetic coupling to the loopstick, resulting in system oscillation. In addition, most audio power amplifiers are not optimized for lowest noise because of compensation requirements. If noise from the audio amplifier radiates into the AM section, the sensitivity and signal-to-noise ratio will be degraded.

The LM1896 exhibits extremely low wideband noise due in part to an external capacitor C5 which is used to tailor the bandwidth. The circuit shown in *Figure 2* is capable of a signal-to-noise ratio in excess of 60 dB referred to 50 mW. Capacitor C5 not only limits the closed loop bandwidth, it also provides overall loop compensation. Neglecting C2 in *Figure 2*, the gain is:

$$A_V(S) = \frac{S + A_V\,\omega_o}{S + \omega_o}$$

$$\text{where } A_V = \frac{R2 + R5}{R2}, \quad \omega_o = \frac{1}{R5C5}$$

A curve of −3 dB BW (ω_o) vs A_V is shown in the Typical Performance Curves.

Figure 3 shows a plot of recovered audio as a function of field strength in μV/M. The receiver section in this example is an LM3820. The power amplifier is located about two inches from the loopstick antenna. Speaker leads run parallel to the loopstick and are 1/8 inch from it. Referenced to a 20 dB S/N ratio, the improvement in noise performance over conventional designs is about 10 dB. This corresponds to an increase in usable sensitivity of about 8.5 dB.

Bridge Amplifiers

The LM1896/LM2896 can be used in the bridge mode as a monaural power amplifier. In addition to much higher power output, the bridge configuration does not require output coupling capacitors. The load is connected directly between the amplifier outputs as shown in *Figure 4*.

Amp 1 has a voltage gain set by 1 + R5/R2. The output of amp 1 drives amp 2 which is configured as an inverting amplifier with unity gain. Because of this phase inversion in amp 2, there is a 6 dB increase in voltage gain referenced to V_i. The voltage gain in bridge is:

$$\frac{V_o}{V_i} = 2\left(1 + \frac{R5}{R2}\right)$$

C_B is used to prevent DC voltage on the output of amp 1 from causing offset in amp 2. Low frequency response is influenced by:

$$f_L = \frac{1}{2\pi\, R_B C_B}$$

Several precautions should be observed when using the LM1896/LM2896 in bridge configuration. Because the amplifiers are driving the load out of phase, an 8Ω speaker will appear as a 4Ω load, and a 4Ω speaker will appear as a 2Ω load. Power dissipation is twice as severe in this situation. For example, if V_S = 6V and R_L = 8Ω bridged, then the maximum dissipation is:

$$P_D = \frac{V_S^2}{20\,R_L} \times 2 = \frac{6^2}{20 \times 4} \times 2$$

$$P_D = 0.9 \text{ Watts}$$

This amount of dissipation is equivalent to driving two 4Ω loads in the stereo configuration.

When adjusting the frequency response in the bridge configuration, R5C5 and R10C10 form a 2 pole cascade and the −3 dB bandwidth is actually shifted to a lower frequency:

$$BW = \frac{0.707}{2\pi RC}$$

where R = feedback resistor

C = feedback capacitor

To measure the output voltage, a floating or differential meter should be used because a prolonged output short will over dissipate the package. *Figure 1* shows the complete bridge amplifier.

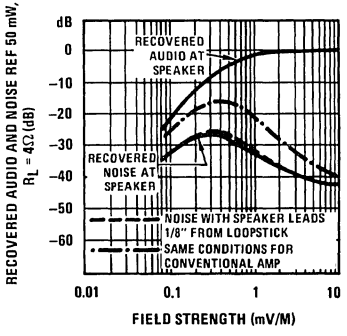


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FIGURE 3. Improved AM Sensitivity over Conventional Design

Application Hints (Continued)

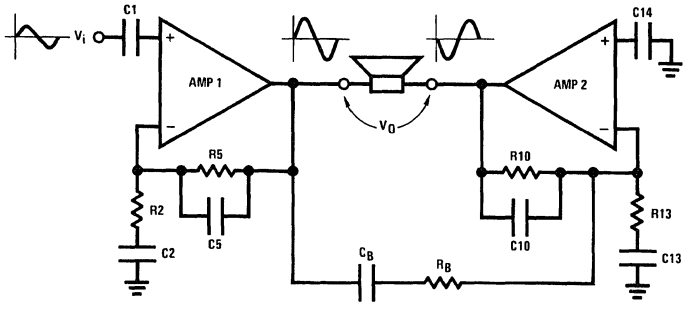

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Figure 4. Bridge Amplifier Connection

Printed Circuit Layout

Printed Circuit Board Layout

Figure 5 and *Figure 6* show printed circuit board layouts for the LM1896 and LM2896. The circuits are wired as stereo amplifiers. The signal source ground should return to the input ground shown on the boards. Returning the loads to power supply ground through a separate wire will keep the THD at its lowest value. The inputs should be terminated in less than 50 kΩ to prevent an input-output oscillation. This oscillation is dependent on the gain and the proximity of the bridge elements R_B and C_B to the (+) input. If the bridge mode is not used, do not insert R_B, C_B into the PCB.

To wire the amplifer into the bridge configuration, short the capacitor on pin 7 (pin 1 of the LM1896) to ground. Connect together the nodes labeled BRIDGE and drive the capacitor connected to pin 5 (pin 14 of the LM1896).

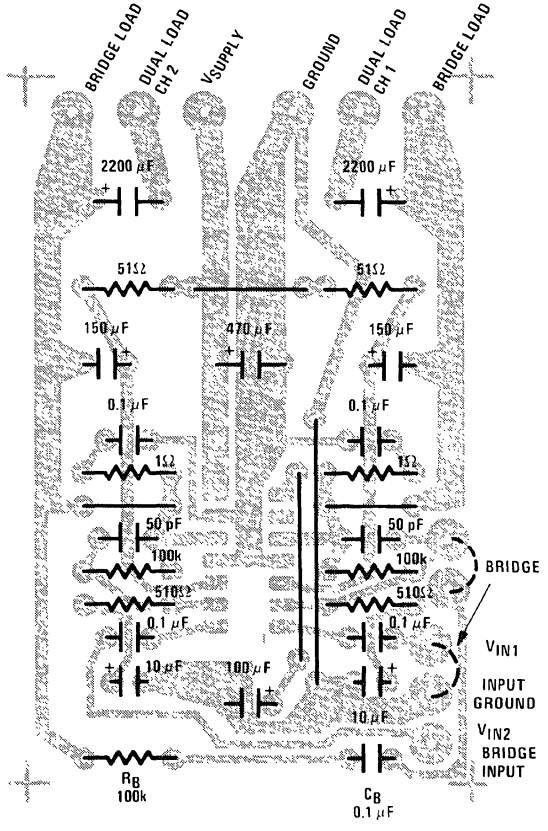

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FIGURE 5. Printed Circuit Board Layout for the LM1896

Printed Circuit Layout (Continued)

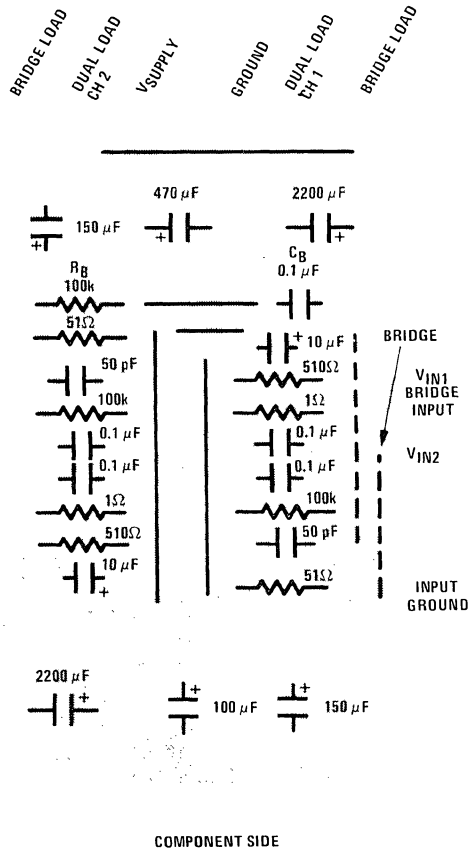

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FIGURE 6. Printed Circuit Board Layout for the LM2896

National Semiconductor Corporation

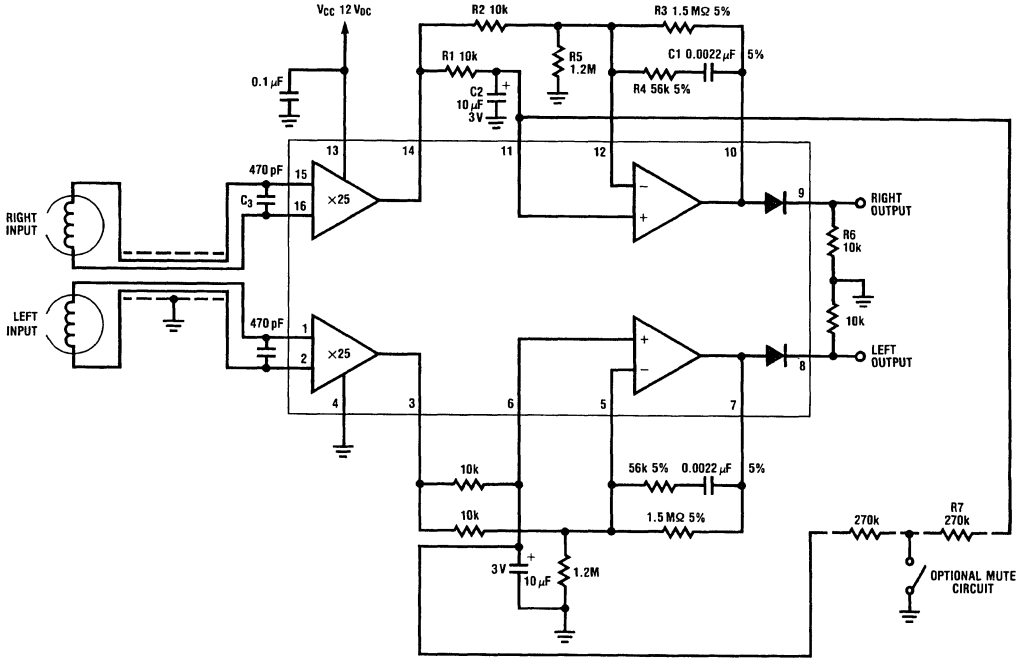
LM1897 Low Noise Preamplifier for Tape Playback Systems

General Description

The LM1897 is a dual high gain preamplifier for applications requiring optimum noise performance. It is an ideal choice for a tape playback amplifier when a combination of low noise, high gain, good power supply rejection, and no power up transients are desired. The application also provides transient-free muting with a single pole grounding switch.

Features

- Programmable turn-on delay
- Transient-free power up—no pops
- Transient-free muting
- Low noise—0.6 μV CCIR/ARM in a DIN circuit referenced to gain at 1 kHz
- Low Voltage Battery Operation 4V
- Wide gain bandwidth due to broadband two amplifier approach 76 dB @ 20 kHz
- High power supply rejection 105 dB
- Low distortion 0.03%
- Fast slew rate 6V/μs
- Short circuit protection
- Internal diodes for diode switching applications
- Low cost external parts
- Excellent low frequency response
- Prevents "click" from being recorded onto the tape during power supply cycling in tape playback applications



TL/H/7094–1

FIGURE 1. Typical Tape Playback Preamplifier Application

Order Number LM1897N
See NS Package Number N16E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	18V
Voltage on Pins 8 and 9	18V
Package Dissipation (Note 1)	715 mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Minimum Voltage On Any Pin	−0.1 V_{DC}
Lead Temperature (soldering, 10 sec.)	260°C

Electrical Characteristics (T_A = 25°C, V_{CC} = 12V, See Circuit—*Figure 2*)

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage Range	R_5 removed from circuit	4		18	V
Supply Current	V_{CC} = 12V		6	12	mA
Total Harmonic Distortion	f = 1 kHz, V_{IN} = 0.3 mV, Pins 7 & 10, *Figure 2*		0.03		%
THD + Noise (Note 2)	f = 1 kHz, V_{OUT} = 1V, Pins 7 & 10, *Figure 2*		0.10	0.25	%
Power Supply Rejection	Input Ref. f = 1 kHz, 1 V_{RMS}	85	105		dB
Channel Separation	f = 1 kHz, Output = 1 V_{RMS}, Output to Output	40	60		dB
Signal to Noise (Note 3)	Unweighted 32 Hz–12.74 kHz (Note 2)		58		dB
	CCIR/ARM (Note 4)		62		dB
	A Weighted		64		dB
	CCIR, Peak (Note 5)		52		dB
Noise	Output Voltage CCIR/ARM (Note 4)		120	200	μV
Input Amplifiers					
Input Bias Current			0.5	2.0	μA
Input Impedance	f = 1 kHz	50			kΩ
A.C. Gain		27	28	29	dB
A.C. Gain Imbalance			±0.15	±0.5	dB
D.C. Output Voltage		1.8	2.2	2.6	V
D.C. Output Voltage Mismatch	Pins 3 and 14	−200	±30	+200	mV
Output Source Current	Pins 3 and 14	2	10		mA
Output Sink Current	Pins 3 and 14	300	600		μA
Output Amplifiers					
Closed Loop Gain	Stable Operation	5			V/V
Open Loop Voltage Gain	D.C.		110		dB
Gain Bandwidth Product			5		MHz
Slew Rate			6		V/μs
Input Offset Voltage			2	5	mV
Input Offset Current			20	100	nA
Input Bias Current			250	500	nA
Output Source Current	Pin 7 or 10	2	10		mA
Output Sink Current	Pin 7 or 10	400	900		μA
Output Voltage Swing	Pin 7 or 10		11		V_{PP}
Output Diode Leakage	Voltage on Pins 8 and 9 = 18V		0	10	μA

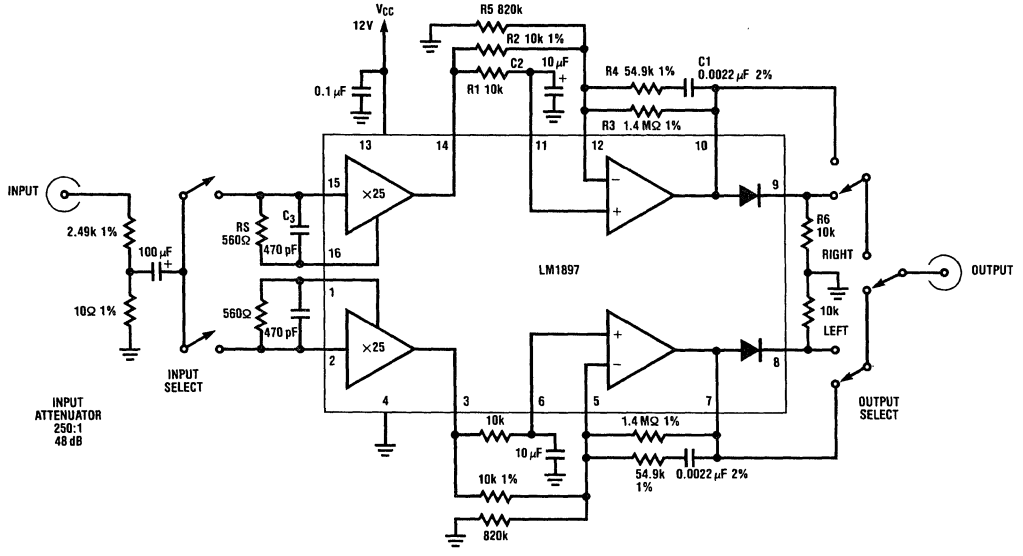
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/Watt junction to ambient.

Note 2: Measured with an average responding voltmeter using the filter circuit in *Figure 4*. This simple filter is approximately equivalent to a "brick wall" filter with a passband of 20 Hz to 20 kHz (see "Application Hints" section). For 1 kHz THD the 400 Hz high pass filter on the distortion analyzer is used.

Note 3: The numbers are referred to an output level of 160 mV at Pins 7 and 10 using the circuit of *Figure 2*. This corresponds to an input level of 0.3 mV RMS at 333 Hz.

Note 4: Measured with an average responding voltmeter using the Dolby lab's standard CCIR filter having a unity gain reference at 2 kHz.

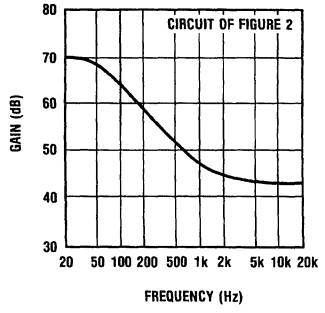
Note 5: Measured using the Rhode-Schwarz psophometer, model UPGR.



TL/H/7094–2

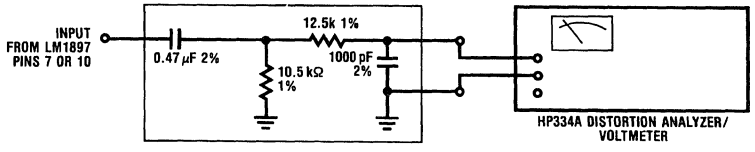
FIGURE 2. General Test Circuit

Gain vs. Frequency



TL/H/7094–3

FIGURE 3. Frequency Response of Test Circuit



TL/H/7094–4

FIGURE 4. Simple 32 Hz–12740 Hz Filter and Meter

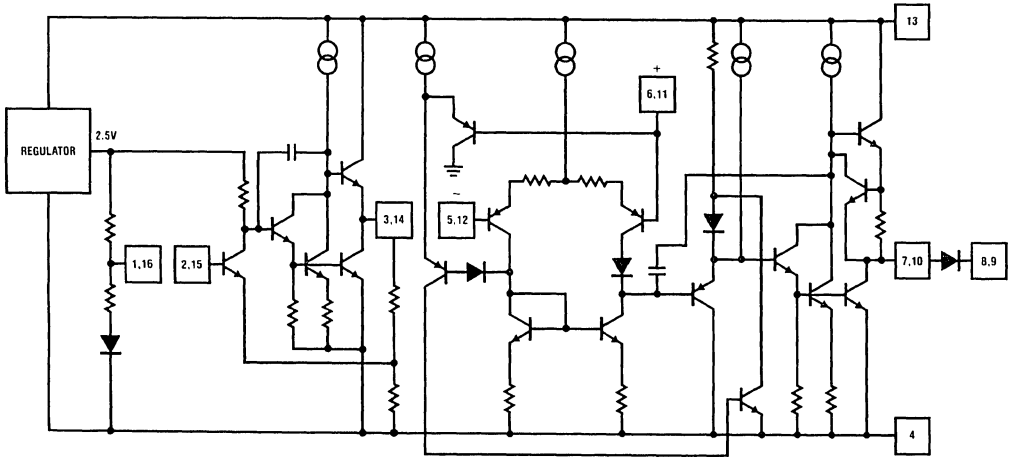


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FIGURE 5. Schematic Diagram

External Component	Component (Refer to *Figure 1*) External Component Function	Normal Range of Value
R_1,	Set turn-on delay and second amplifier's low frequency pole.	2 kΩ–40 kΩ
C_2	Leakage current in C_2 results in DC offset between the amplifier's inputs and therefore this current should be kept low. R_1 is set equal to R_2 such that any input offset voltage due to bias current is effectively cancelled. An input offset voltage is generated by the input offset current multiplied by the value of these resistors.	0.1 μF–10 μF (Low Leakage)
R_2	Set the DC and low frequency gain of the output amplifier. The total input offset voltage will also be multiplied by the DC gain of this amplifier. It is therefore essential to keep the input offset voltage specification in mind when employing high DC gain in the output amplifier; i.e. 5 mV × 400 = 2V offset at the output.	2 kΩ–40 kΩ
R_3		500 kΩ–10 MΩ
R_4	Set tape playback equalization characteristics in conjunction with R_3 (calculations for the component values are included in the Applications Hints section).	10 kΩ–200 kΩ
C_1		0.00047 μF–0.01 μF
R_6	Biases the output diode when it is used in DC switching applications. This resistor can be excluded if diode switching is not desired.	2 kΩ–47 kΩ
C_3	Often used to resonate with tape head in order to compensate for tape playback losses including tape head gap and eddy current. For a typical cassette tape head, the resonant frequency selected is usually between 13 and 17 kHz.	100 pF–1000 pF
R_5	Increases the output DC bias voltage from the nominal 2.2V value (See the Application Hints section).	100 kΩ–10 MΩ
R_7	Optionally used for tape muting. The use of this resistor can also provide "No Pop" turn-off if desired.	

Application Hints

DISTORTION MEASUREMENT METHOD

In order to clearly interpret and compare specifications and measurements for low noise preamplifiers, it is necessary to understand several basic concepts of noise. An obvious example is the measurement of total harmonic distortion at very low input signal levels. Distortion analyzers provide outputs which allow viewing of the distortion products on an oscilloscope. The oscilloscope often reveals that the "distortion" being measured contains 1) distortion, 2) noise, and 3) 50 or 60 cycle AC line hum.

Application Hints (Continued)

Line hum can be detected by using the "line sync" on the oscilloscope (horizontal sync selector). The triggering of a constant wave form indicates that AC line pickup is present. This is usually the result of electro-magnetic coupling into the preamplifier's input or improper test equipment grounding, which simply must be eliminated before making further measurements!

Input coupling problems can usually be corrected by any one of the following solutions: 1) shielding the source of the magnetic field (using mu metal or steel), 2) magnetically shielding the preamplifier, 3) physically moving the preamplifier far enough away from the magnetic field, or 4) using a high pass filter (f_0 = 200 Hz–1 kHz) at the output of the preamplifier to prevent any line signal from entering the distortion analyzer. Ground loop problems can be solved by rearranging ground connections of the circuit and test equipment.

Separating noise from distortion products is necessary when it is desired to find the actual distortion and not the signal-to-noise ratio of an amplifier. The distortion produced by the LM1897 is predominately a second harmonic. It is for this reason that the third and higher order harmonics can be filtered without resulting in any appreciable error in the measurement. The filter also reduces the amount of noise in the measured data. Another more tedious technique for measuring THD is to use a wave analyzer. Each harmonic is measured and then summed in an RMS calculation. A typical curve is plotted for distortion vs. frequency using this method. A typical curve is also included using a 20 Hz to 20 kHz 4th order filter.

To specify the distortion of the LM1897 accurately and also not require unusual or tedious measurements the following method is used. The output level is set to one volt RMS at 1 kHz (approximately 5 millivolts at the input). The output is filtered with the circuit of *Figure 4* to limit the bandwidth of the noise and measured with a standard distortion analyzer. The analyzer has a filter that is switched in to remove line hum and ground loop pick-up as well as unrelated low frequency noise. The resulting measurement is fast and accurate.

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit to discrete preamplifier designs. Discrete transistor preamps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated below.

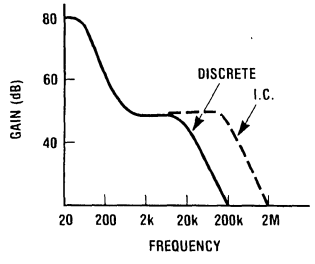

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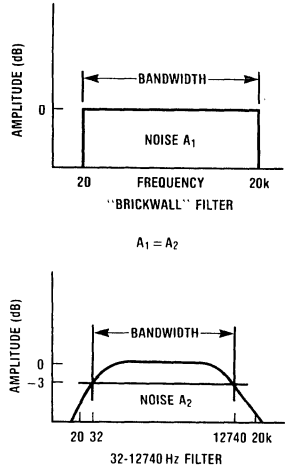
FIGURE 6

Integrated circuits have additional open loop gain allowing aditional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this additional bandwidth that can lead to erroneous signal to noise measurements if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth, (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter.[1] A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to certain undesirable frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

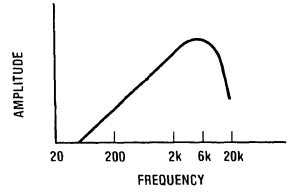
The 32 Hz to 12740 Hz filter shown in *Figure 4* is a simple two pole, one zero filter, approximately equivalent to a "brick wall" filter of 20 Hz to 20 kHz. This approximation is absolutely valid if the noise has a flat energy spectrum over the frequencies involved. In other words a measurement of a noise source with constant spectral density through either of the two filters would result in the same reading. The output frequency response of the two filters is shown is *Figure 7.*



TL/H/7094–7

FIGURE 7

Typical signal-to-noise figures are listed for several weighting filters which are commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown below.



TL/H/7094–8

FIGURE 8

Application Hints (Continued)

In addition to noise filtering, differing meter types give different noise readings. Meter responses include: 1) RMS reading, 2) average responding, 3) peak reading, and 4) quasi peak reading. Although theoretical noise analysis is derived using true RMS (root mean square) based calculations, most actual measurement is taken with ARM (Average Responding Meter) test equipment. Unless otherwise noted an average responding meter is used for all AC measurements in this data sheet.

BASIC CIRCUIT APPROACH

The LM1897 IC incorporates a two stage broadband design which minimizes noise, attains overall DC stability and prevents audible transients during turn-on.

The first stage is a direct coupled amplifier with an internal gain of 25 V/V (28 dB). Direct coupling to the tape head reduces input source impedance and external component cost by removing the input coupling capacitor. A typical input coupling capacitor of 1 μF has a reactance of 1.5 kΩ at 100 Hz. The resulting noise due to the amplifier's input noise current can dominate the noise voltage at the output of the playback system. The input of the amplifier is biased from a reference voltage that is temperature compensated to produce a quiescent DC voltage of 2.2V at the output of the first stage. The input stage bias current that flows through the tape head is kept below 2 μA in order to prevent any erasure of tape moving past the head. An added advantage of DC biasing is the prevention of large current transients during the charging of coupling capacitors at turn-on and turn-off.

The second stage provides additional gain and proper equalization while preventing audible turn-on transients or "pops". The output (Pin 10) is kept low until C2 charges through R1. When the voltage on C2 gets close to the DC voltage on Pin 14, the output rises exponentially to its final DC value. The result is a transient-free turn-on characteristic.

Internal diodes are provided to facilitate electronic diode switching popular in automotive applications.

The general test circuit illustrates the topography of the system. The components determining the overall frequency response are external due to the extreme sensitivity when matching a DIN equalization curve.

MUTE CIRCUIT

The LM1897 can be muted with the addition of two resistors and a grounding switch, as shown in *Figure 1*. When the circuit is not muted the additional resistors have no effect on the AC performance. They *do* have an effect on the DC Q point however.

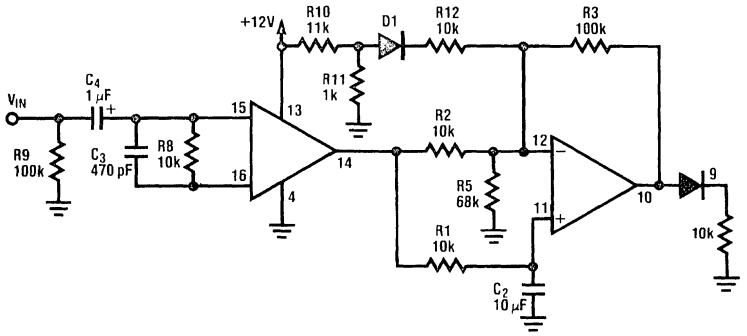
The difference in the DC output voltages of the input amplifiers is applied across the mute resistors (R7) and the positive input resistors (R1). This results in an additional offset at the input of the output amplifiers. To keep this offset to a minimum R7 should be as large as possible to achieve effective muting. In all cases R7 should be at least ten times R1. A typical value of R7 is 25 to 50 times R1.

CAPACITOR-COUPLED INPUT

The LM1897 is intended to be coupled directly to the signal source. Direct coupling permits faster turn-on and less low-frequency noise than would be possible with a capacitor-coupled input. However, there are some applications which require that the signal source be referred to ground and coupled to the input through a capacitor. *Figure 9* is an example of an LM1897 with a capacitor-coupled input. As shown, the circuit has a flat frequency response and is suitable for use as a microphone preamp.

R_8 provides a DC path for input bias current. The value of R_8 should be as low as possible without loading the source. A very large value of R_8 can cause excessive DC offset at the amplifier output. In order to avoid turn-on pops, the inverting input of the second amplifier must be at a higher voltage than the non-inverting input when V_{CC} is applied. R_{10}, R_{11}, R_{12}, and D_1 ensure that this condition will be met. If later stages in the playback system employ turn-on muting circuitry, these extra components may not be needed. The value of R_{10} depends on V_{CC} as defined by the following relationship:

$$R_{10} = (V_{CC} - 1) \times 1k$$



TL/H/7094–9

FIGURE 9. Microphone Preamplifier with Capacitor Coupled Input

Application Hints (Continued)

Design Equation

The overall gain of the circuit is given by:

$$A_V = 25\left[\frac{-R_4R_3}{R_2(R_3+R_4)}\right]\left(s+\frac{1}{R_4C_1}\right)\left(s+\frac{1}{(R_3+R_4)C_1}\right) \quad (1)$$

Standard cassette tapes require equalization of 3180 μs (50 Hz) and 120 μs (1.3kHz). These time constants result in an AC gain at 1 kHz given by:

$$A_V(1\text{ kHz}) = 25\left(\frac{-R_4R_3}{R_2(R_3+R_4)}\right)1.663\left\{\begin{array}{c}3180\ \mu s \text{ or } 50\text{ Hz}\\ \text{and}\\ 120\ \mu s \text{ or } 1326\text{ Hz}\end{array}\right\} \quad (2)$$

Using the pole and zero locations of the transfer function, the two other equations needed to solve for the component values are:

$$R_4 = \frac{1}{2\pi C_1(1326\text{ Hz})} \quad (3)$$

$$R_3 = \frac{1}{2\pi C_1(50\text{ Hz})} - \frac{1}{2\pi C_1(1326\text{ Hz})} = \frac{1}{2\pi C_1(51.96)} \quad (4)$$

We can now solve for C_1 as a function of R_2, or:

$$A_V(1\text{ kHz}) = -25\left\{\frac{\left[\frac{1}{2\pi C_1(1326)}\right]\left[\frac{1}{2\pi C_1(51.96)}\right]}{\left[R_2\frac{1}{2\pi C_1(50)}\right]}\right\}(1.663) \quad (5)$$

$$C_1 = \frac{-4.80\times10^{-3}}{R_2\,[A_V(1\text{ kHz})]} \quad (6)$$

When chromium dioxide tape is used, the defined time constants are 3180 μs and 70 μs. This changes equation (3) to:

$$R_4 = \frac{1}{2\pi C_1(2274\text{ Hz})} \quad (7)$$

The value of R_3 is normally not changed. This results in an error of less than 0.2 dB in the low frequency response.

The output voltage of the LM1897 is set by the input amplifier DC voltage at pin 3 or 14, and by R_3 and R_5.

$$\text{Nominal } V_{OUT} \text{ (pin 7 or 10)} = 2.2\left(1+\frac{R_3}{R_5}\right) \quad (8)$$

Pins 8 and 9 are biased 0.7 volts less than V_{OUT} (pin 7 or 10). When these diodes are used the output (pin 7 or 10) should be biased at one half the minimum operating supply voltage. Equation (8) can be rewritten to solve for R_5.

$$R_5 = \frac{2.2R_3}{V_O - 2.2} \quad (9)$$

The output voltage of the LM1897 will vary from that given in equation (8) due to variations in the input amplifier DC voltage as well as the output amplifier input bias current, input offset current and input offset voltage. The following equation gives the worst case variation in the output voltage.

$$\Delta V_{OUT} = \pm\left[\Delta V_{PIN\,3}\left(1+\frac{R_3}{R_5}\right)+\frac{R_3}{R_5}\left(\Delta I_{BIAS}(R_1-R_2)\right)+\frac{I_{OS}}{2}(R_1+R_2)+V_{OS}\right)\Big] \quad (10)$$

Using the worst case values in the electrical characteristics reduces this to

$$\Delta V_{OUT} = \pm\left[0.4\left(1+\frac{R_3}{R_5}\right)+\frac{R_3}{R_2}\left(200\text{ nA}(R_1-R_2)+50\text{ nA}(R_1+R_2)+5\text{ mV}\right)\right] \quad (11)$$

The turn-on delay is set by R_1 and C_2; delay can be approximated by:

$$\text{Delay Time } t = R_1C_2\ln\left(\frac{2.2}{V_{ODC}}\right)\left(\frac{R_3}{R_2}\right) \quad (12)$$

Example

If we desire a tape preamp with 100 mV output signal from a tape head with a nominal output of 0.5 mV at 1 kHz for standard ferric cassette tape, the external components are determined as follows. The value of R_2 is arbitrarily set to 10 kΩ.

$$R_1 = R_2 = 10\text{k}$$

This minimizes errors due to the output amplifier bias currents.

$$C_1 = \frac{-4.80\times10^{-3}}{10\text{ k}\Omega\left[\frac{-100\text{ mV}}{0.5\text{ mV}}\right]} = 2400\text{ pF} \longrightarrow 0.0022\ \mu\text{F}$$

Use 0.0022 μF and determine:

$$R_4 = \frac{1}{2\pi C_1(1326)} = 54.6\text{ k}\Omega \longrightarrow 54.9\text{ k}\Omega\ 1\%$$

$$R_3 = \frac{1}{2\pi C_1(51.96)} = 1.39\text{ M}\Omega \longrightarrow 1.4\text{ M}\Omega\ 1\%$$

To bias the output amplifier output voltage at 6 volts (half supply):

$$R_5 = \frac{2.2(1.4\text{ M}\Omega)}{6-2.2} = 811\text{ k}\Omega \longrightarrow 820\text{ k}\Omega$$

The maximum variation in the output voltage is found using equation (11):

$$\Delta V_{OUT} = \pm 1.9\text{V}$$

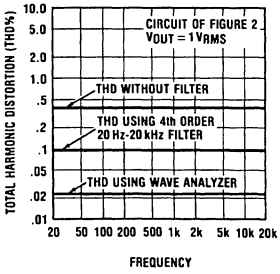
The low frequency response and turn-on delay determine the value of C_2. For R_1 = 10k and C_2 = 10μF the low frequency 3 dB point is 1.6 Hz and the turn-on delay is 0.4 seconds, from equation (12).

The complete circuit is shown in Figure 2. A circuit with 5% components and biased for a minimum supply of 10 volts is shown in Figure 1. If additional gain is needed R_1 and R_2 can be reduced without changing the frequency response of the circuit.

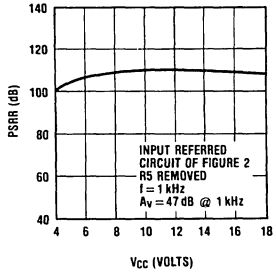
Reference 1: CCIR/ARM: *A Practical Noise Measurement Method;* by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

Typical Performance Characteristics

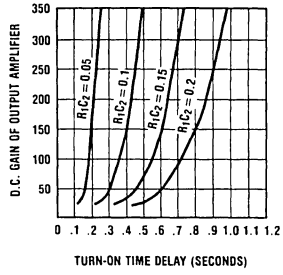
Total Harmonic Distortion vs Frequency



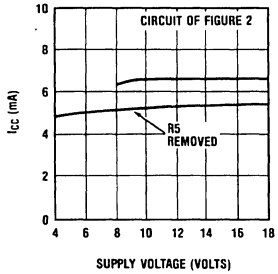
PSRR vs V_{CC}



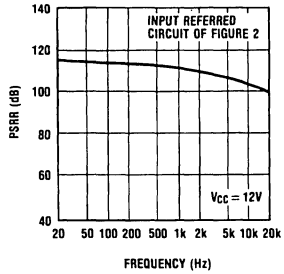
Turn On Delay vs Component Values and Gain



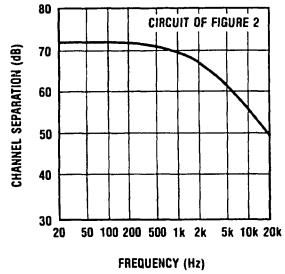
I_{CC} vs Supply Voltage



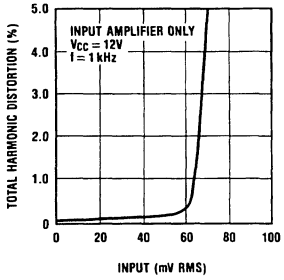
PSRR vs Frequency



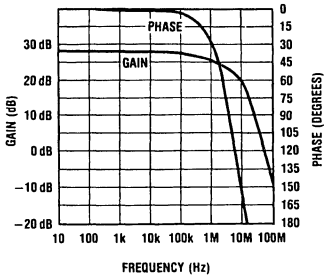
Channel Separation vs Frequency



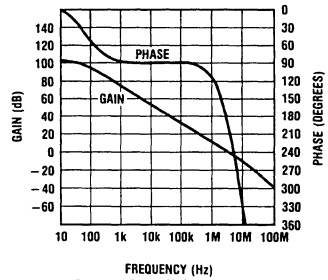
Input Amplifier THD vs Input Level



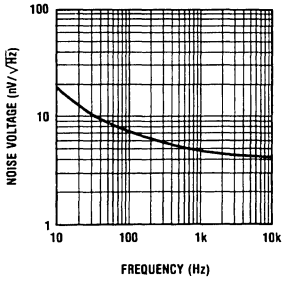
Input Amplifier Gain and Phase vs Frequency



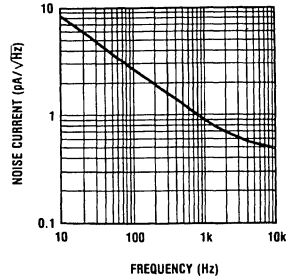
Output Amplifier Open Loop Gain and Phase vs Frequency



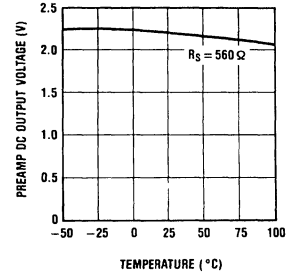
Spot Noise Voltage vs Frequency



Spot Noise Current vs Frequency



Input Amplifier DC Output Voltage vs Temperature (Pins 3, 14)



TL/H/7094–10

National Semiconductor Corporation

LM2002/LM2002A 8 Watt Audio Power Amplifier

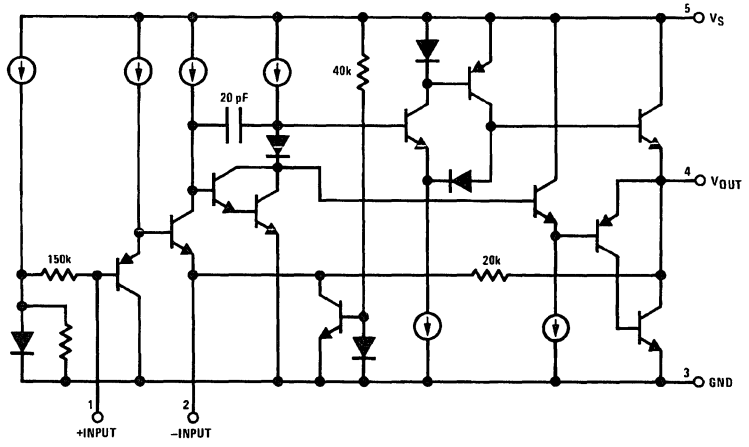
General Description

The LM2002 is a cost effective, high power amplifier suited for automotive applications. High current capability (3.5A) enables the device to drive low impedance loads with low distortion. The LM2002 is current limited and thermally protected. High voltage protection is available (LM2002A) which enables the amplifier to withstand 40V transients on its supply. The LM2002 comes in a 5-pin TO-220 package.

Features

- High peak current capability (3.5A)
- Large output voltage swing
- Externally programmable gain
- Wide supply voltage range (5V–20V)
- Few external parts required
- Low distortion
- High input impedance
- No turn-on transients
- High voltage protection available (LM2002A)
- Low noise
- AC short circuit protected
- Pin for pin compatible with TDA2002

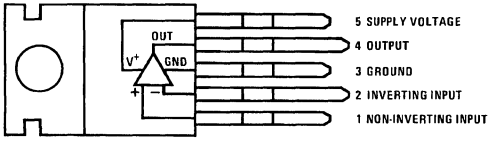
Equivalent Schematic



TL/H/7929–1

Connection Diagram

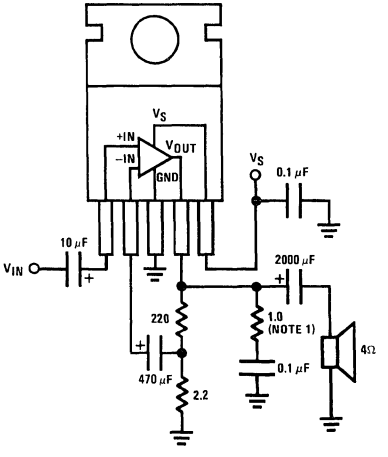
Plastic Package



TL/H/7929–2

Order Number LM2002T or LM2002AT
See NS Package Number T05A

Typical Application



TL/H/7929–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Peak Supply Voltage (50 ms)
- LM2002A (Note 2) 40V
- LM2002 25V

Operating Supply Voltage 20V

Output Current
- Repetitive 3.5A
- Non-repetitive 4.5A

Input Voltage ±0.5V

Power Dissipation (Note 3) 15W

Operating Temperature 0°C to +70°C

Storage Temperature −60°C to +150°C

Lead Temperature (Soldering, 10 sec.) 260°C

Electrical Characteristics

V_S = 14.4V, T_{TAB} = 25°C, A_V = 100 (40 dB), R_L = 4Ω, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
DC Output Level		6.4	7.2	8	V
Quiescent Supply Current	Excludes Current in Feedback Resistors		45	80	mA
Supply Voltage Range		5		20	V
Input Resistance			150		kΩ
Bandwidth	Gain = 40 dB		100		kHz
Output Power	V_S = 13.2V, f = 1 kHz				
	R_L = 4Ω, THD = 10%		4.3		W
	R_L = 2Ω, THD = 10%		6.5		W
	V_S = 13.8V, f = 1 kHz				
	R_L = 4Ω, THD = 10%		4.8		W
	R_L = 2Ω, THD = 10%		7.4		W
	V_S = 14.4V, f = 1 kHz				
	R_L = 4Ω, THD = 10%	4.8	5.2		W
	R_L = 2Ω, THD = 10%	7	8		W
	R_L = 1.6Ω, THD = 10%		9		W
	V_S = 16V, f = 1 kHz				
	R_L = 4Ω, THD = 10%		6.5		W
	R_L = 2Ω, THD = 10%		10		W
	R_L = 1.6Ω, THD = 10%		10.5		W
THD	P_O = 2W, R_L = 4Ω, f = 1 kHz		0.1		%
	P_O = 4W, R_L = 2 Ω, f = 1 kHz		0.1		%
Ripple Rejection	R_S = 50Ω, f = 100 Hz	30	40		dB
	R_S = 50Ω, f = 1 kHz		44		dB
Input Noise Voltage	R_S = 0, 15 kHz Bandwidth		2		μV
Input Noise Current	R_S = 100 kΩ, 15 kHz Bandwidth		40		pA

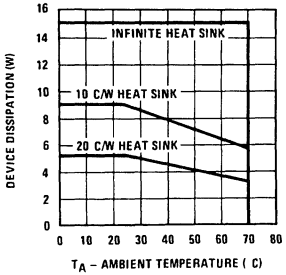
Note 1: A 1.0 resistor and 0.1 μF capacitor should be placed as close as possible to pins 3 and 4 for stability.

Note 2: The LM2002 shuts down above 25V.

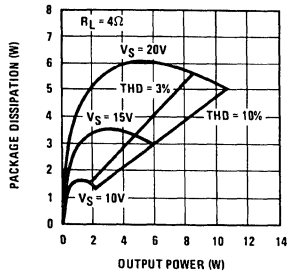
Note 3: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 4°C/W junction to case.

Typical Performance Characteristics

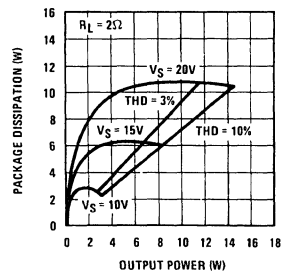
Device Dissipation vs Ambient Temperature



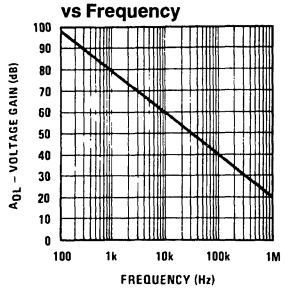
Power Dissipation vs Output Power



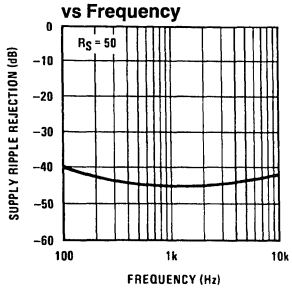
Power Dissipation vs Output Power



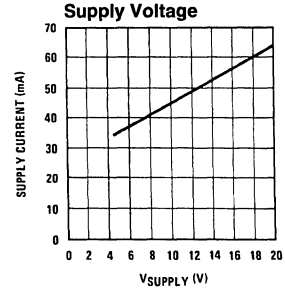
Open Loop Gain vs Frequency



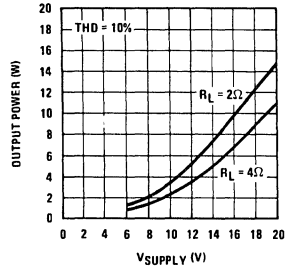
Supply Ripple Rejection vs Frequency



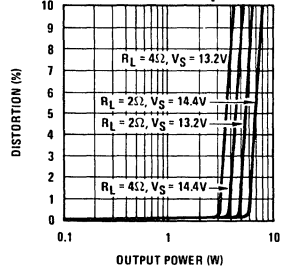
Supply Current vs Supply Voltage



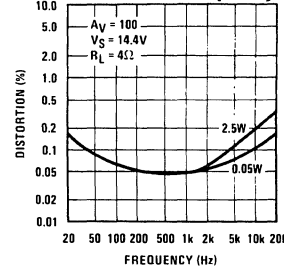
Output Power vs Supply Voltage



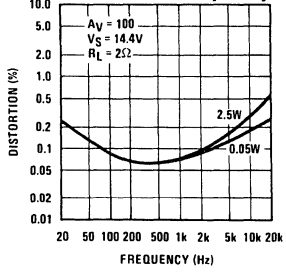
Distortion vs Output Power



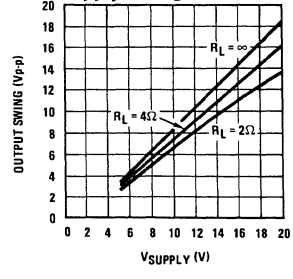
Distortion vs Frequency



Distortion vs Frequency



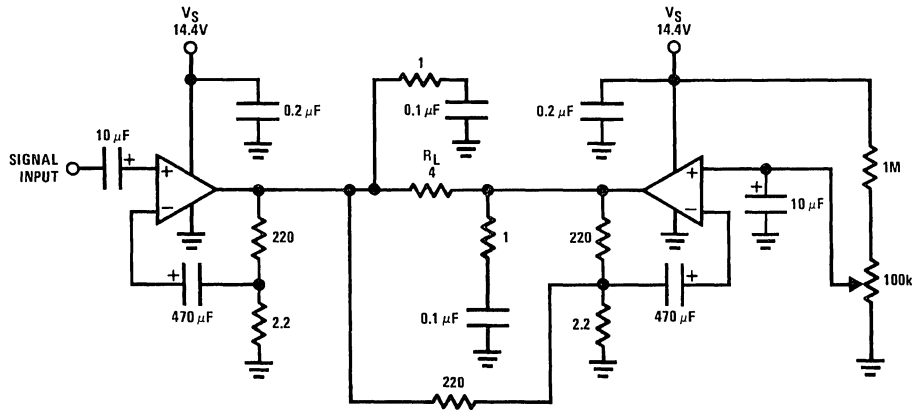
Output Swing vs Supply Voltage



TL/H/7929–4

Typical Applications (Continued)

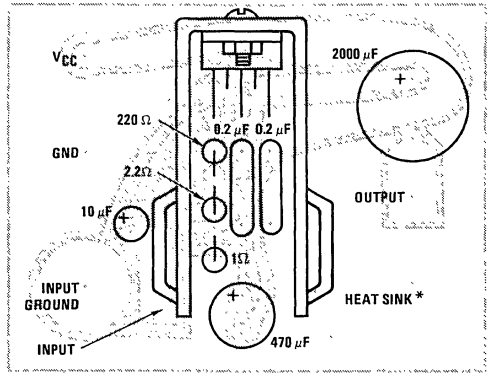
16W Bridge Amplifier



TL/H/7929–5

Component Layout

Single Amplifier
V_S = 20V
R_L = 4Ω



TL/H/7929–6

*Staver V-5 Heatsink
Staver Company
41 Saxon Ave
P.O. Drawer H
Bayshore, NY 11706
TEL: (516) 666-8000

National Semiconductor Corporation

LM2005 20-Watt Automotive Power Amplifier

General Description

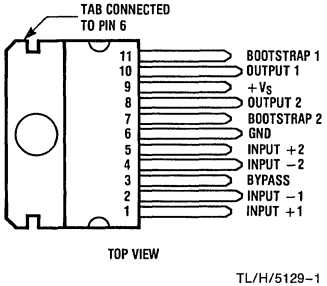
The LM2005 is a dual high power amplifier, designed to deliver optimum performance and reliability for automotive applications. High current capability (3.5A) enables the device to deliver 10W/channel into 2Ω (LM2005T-S), or 20W bridged monaural (LM2005T-M) into 4Ω, with low distortion.

Features

- Wide supply range (8V–18V)
- Externally programmable gain
- With or without bootstrap
- Low distortion
- Low noise
- High peak current capability
- P_O = 20W bridge
- High voltage protection
- AC and DC output short circuit protection to ground or across load
- Thermal protection
- Inductive load protection
- Accidental open ground protection
- Immunity to 40V power supply transients
- 3°C/W device dissipation
- Pin for pin compatible with TDA2005

Connection Diagram

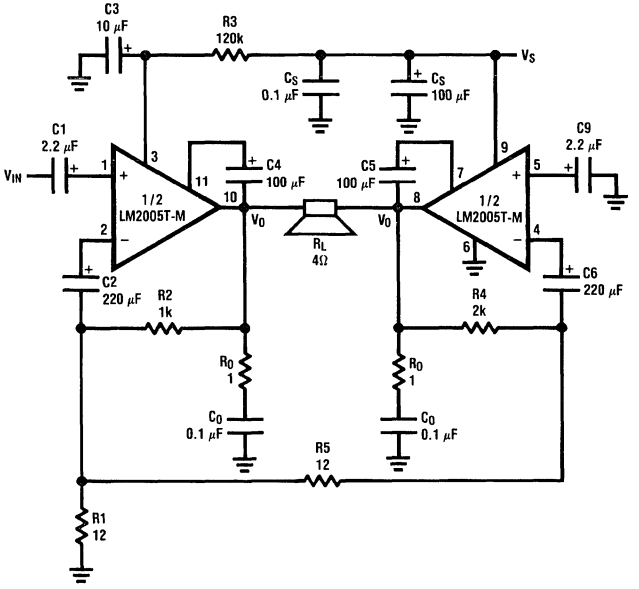
Plastic Package



TL/H/5129–1

Order Number LM2005T-S
or LM2005T-M
See NS Package Number T11A

Typical Application



TL/H/5129–2

FIGURE 1. 20W Bridge Amplifier Application and Test Circuit

LM2005T-M and LM2005T-S Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Operating Supply Voltage	18V
DC Supply Voltage (Note 1)	28V
Peak Supply Voltage (50 ms)	40V
Output Current	
Repetitive (Note 2)	3.5A
Non-Repetitive	4.5A
Power Dissipation	30W
Operating Temperature	−40°C to +85°C
Storage Temperature	−60°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

LM2005T-M

Electrical Characteristics

Refer to the **bridge** application circuit, *Figure 1*, T_{amb} = 25°C, A_V = 50 dB, $R_{th\ (heatsink)}$ = 4°C/W, unless otherwise specified

Parameter	Test Conditions	Min	Typ	Max	Units
Supply Voltage		8		18	V
Output Offset Voltage (Note 3) (between Pin 8 and 10)	V_S = 14.4V V_S = 13.2V		±20	±150 ±150	mV mV
Total Quiescent Drain Current Includes Current in Feedback Resistors	V_S = 14.4V R_L = 4Ω V_S = 13.2V R_L = 3.2Ω		75 70	150 160	mA mA
Output Power	d = 10% f = 1 kHz V_S = 14.4V R_L = 4Ω R_L = 3.2Ω V_S = 13.2V R_L = 3.2Ω	 18 20 17	 20 22 19		 W W W
THD	f = 1 kHz V_S = 14.4V R_L = 4Ω P_O = 50 mW to 15W V_S = 13.2V R_L = 3.2Ω P_O = 50 mW to 13W			 1 1	 % %
Input Sensitivity	f = 1 kHz P_O = 2W R_L = 4Ω P_O = 2W R_L = 3.2Ω		 9 8		 mV mV
Input Resistance	f = 1 kHz	70			kΩ
Low Frequency Roll Off (−3 dB)	R_L = 3.2Ω			40	Hz
High Frequency Roll Off (−3 dB)	R_L = 3.2Ω	20			kHz
Closed Loop Voltage Gain	f = 1 kHz	45	50		dB
Total Input Noise Voltage	R_g = 10 kΩ (Note 4)		3	10	μV
Supply Voltage Rejection	R_g = 10 kΩ f_{ripple} = 100 Hz C_4 = 10 μF V_{ripple} = 0.5V	45	55		dB
Efficiency	V_S = 14.4V f = 1 kHz P_O = 20W R_L = 4Ω P_O = 22W R_L = 3.2Ω V_S = 13.2V f = 1 kHz P_O = 19W R_L = 3.2Ω		 60 60 58		 % % %
Output Voltage with One Side of the Speaker Shorted to Ground	V_S = 14.4V R_L = 4Ω V_S = 13.2V R_L = 3.2V			2	V

Note 1: Internal voltage limit. Shuts down above 20V.

Note 2: Internal current limit.

Note 3: For LM2005T-M only.

Note 4: Bandwidth filter: 22 Hz to 22 kHz.

LM2005T-S

Electrical Characteristics

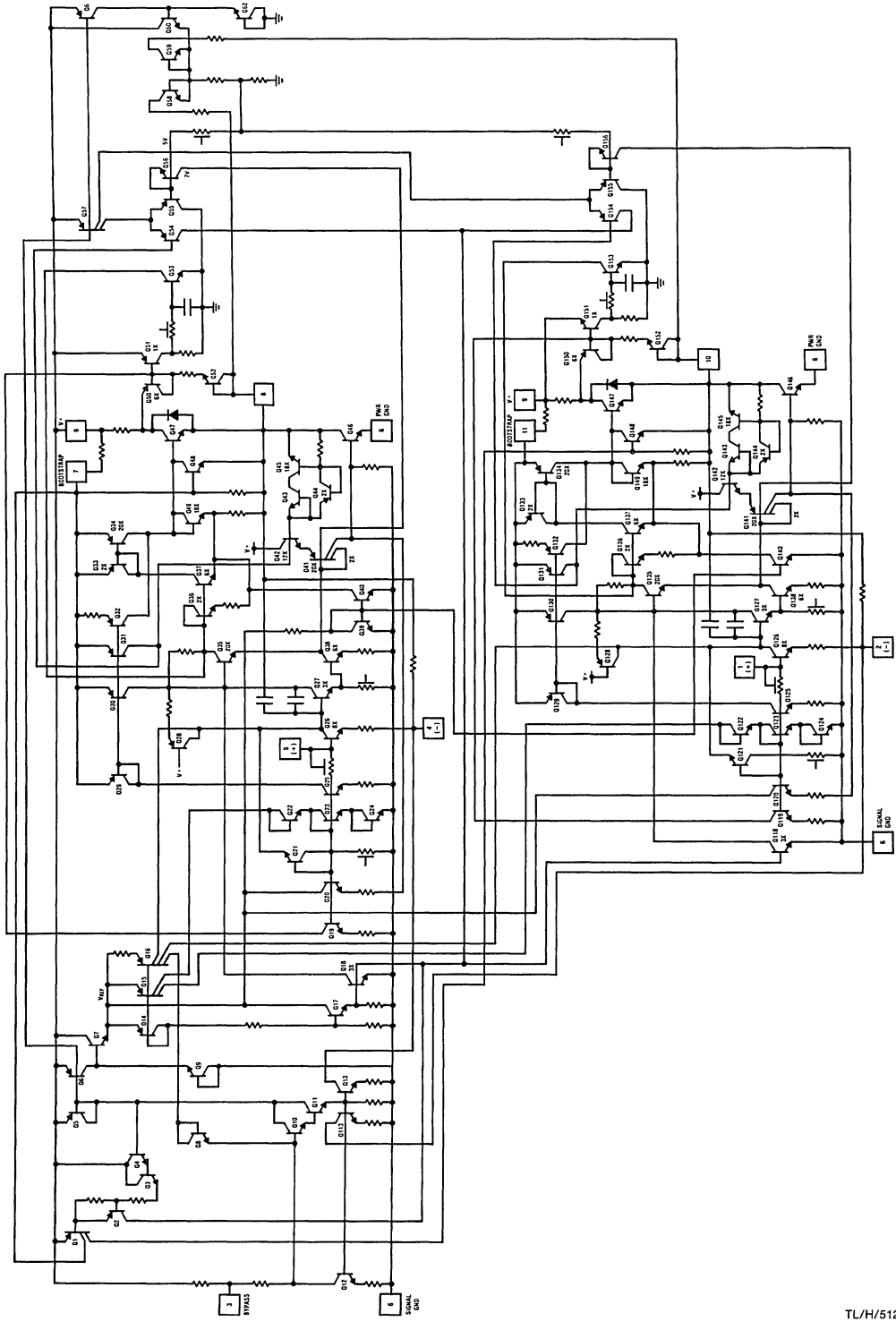
Refer to the **stereo** application circuit, *Figure 2*, T_{amb} = 25°C, G_v = 50 dB, $R_{th\ (heatsink)}$ = 4°C/W, unless otherwise specified

Parameter	Test Conditions		Min	Typ	Max	Units
Supply Voltage			8		18	V
Quiescent Output Voltage	V_S = 14.4V		6.6	7.2	7.8	V
	V_S = 13.2V		6	6.6	7.2	V
Total Quiescent Drain Current	V_S = 14.4V			65	120	mA
Includes Current in Feedback Resistors	V_S = 13.2V			62	120	mA
Output Power	f = 1 kHz	d = 10%				
(Each Channel)	V_S = 14.4V	R_L = 4Ω	6	6.5		W
		R_L = 3.2Ω	7	8		W
		R_L = 2Ω	9	10		W
		R_L = 1.6Ω	10	11		W
	V_S = 13.2V	R_L = 3.2Ω	6	6.5		W
		R_L = 1.6Ω	9	10		W
	V_S = 16V	R_L = 2Ω		12		W
THD	f = 1 kHz					
(Each Channel)	V_S = 14.4V	R_L = 4Ω				
	P_O = 50 mW to 4W			0.2	1	%
	V_S = 14.4V	R_L = 2Ω				
	P_O = 50 mW to 6W			0.3	1	%
	V_S = 13.2V	R_L = 3.2Ω				
	P_O = 50 mW to 3W			0.2	1	%
	V_S = 13.2V	R_L = 1.6Ω				
	P_O = 40 mW to 6W			0.3	1	%
Cross Talk	V_S = 14.4V					
(Note 5)	R_L = 4Ω	f = 1 kHz	40	60		dB
	V_O = 4 V_{rms}					
	R_g = 5 kΩ	f = 10 kHz		40		dB
Input Saturation Voltage			300			mV
Input Sensitivity	f = 1 kHz	P_O = 1W				
		R_L = 4Ω		6		mV
		R_L = 3.2Ω		5.5		
Input Resistance	f = 1 kHz	Non-Inverting Input	70	200		kΩ
		Inverting Input		10		kΩ
Low Frequency Roll Off (−3 dB)	R_L = 2Ω				50	Hz
High Frequency Roll Off (−3 dB)	R_L = 2Ω		15			kHz
Voltage Gain (Open Loop)	f = 1 kHz			90		dB
Voltage Gain (Closed Loop)	f = 1 kHz		48	50	51	dB
Closed Loop Gain Matching				0.5		dB
Total Input Noise Voltage	R_g = 10 kΩ (Note 6)			1.5	5	μV
Supply Voltage Rejection	R_g = 10 kΩ	f_{ripple} = 100 Hz	35	45		dB
	C_3 = 10 μF	V_{ripple} = 0.5V				
Efficiency	V_S = 14.4V	f = 1 kHz				
	R_L = 4Ω	P_O = 6.5W		70		%
	R_L = 2Ω	P_O = 10W		60		%
	V_S = 13.2V	f = 1 kHz				
	R_L = 3.2Ω	P_O = 6.5W		70		%
	R_L = 1.6Ω	P_O = 10W		60		%

Note 5: For LM2005T-S only.

Note 6: Bandwidth filter: 22 Hz to 22 kHz.

Equivalent Schematic

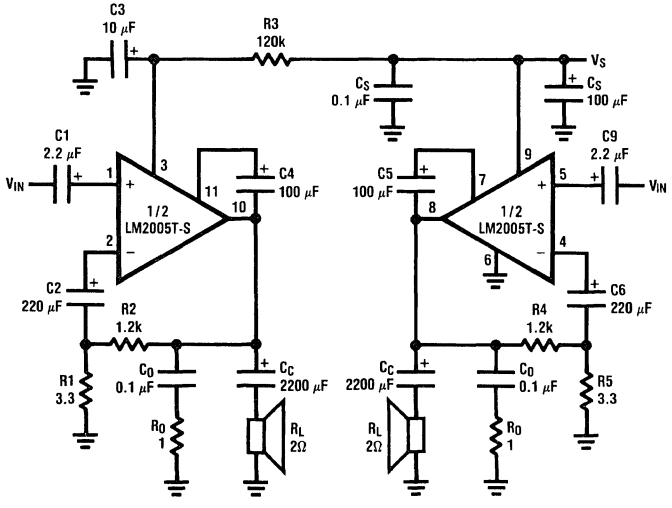


TL/H/5129–3

External Components *(Figure 2)*

Components	Comments
1. R1, R2 R5, R4	Sets voltage gain, $A_V \cong 1+\frac{R'}{R1}$ for one channel, $A_V = 1+\frac{R'}{R5}$ for the other. Where R' is the equivalent resistance of R2 in parallel with an internal 10k resistor: $R' = \frac{10k \bullet R2}{R2+10k}$. If R2 $\ll$ 10k, then $A_V \cong 1+\frac{R2}{R1}$.
2. R3	Adjusts output symmetry for maximum power output.
3. R_O, C_O	Works to stabilize internal output stage. Necessary for stability. C_O should be ceramic disc or equivalently good high frequency capacitor.
4. C1, C9	Input coupling capacitor. Low frequency pole set by $F_L1 = \frac{1}{2\pi Z\,(\text{non-inverting})\,C1}$. Decreasing capacitor value will also increase noise.
5. C4, C5	Bootstrap capacitors, used to increase drive to output stage.
6. C3	Improves power supply rejection. Increasing C3 increases turn-on delay (approximately 2 ms per μF).
7. C2, C6	Inverting input DC decouple. Low frequency pole: $F_L2 = \frac{1}{2\pi Z(\text{inverting})C2}$. Z (inverting) $\approx$ 10 kΩ.
8. C_C	Output coupling capacitor. Isolates pins 10 and 8 from load. Low frequency pole; $F_L3 = \frac{1}{2\pi R_L C_C}$.
9. C_S	Power supply filtering.

Typical Applications (Continued)

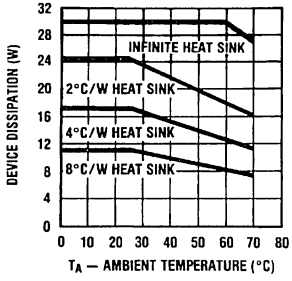


TL/H/5129–4

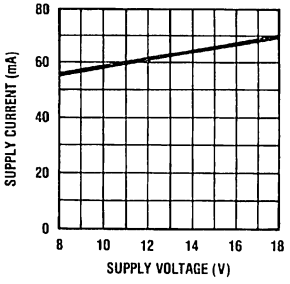
FIGURE 2. 10W/Channel Stereo Amplifier Application and Test Circuit

Typical Performance Characteristics

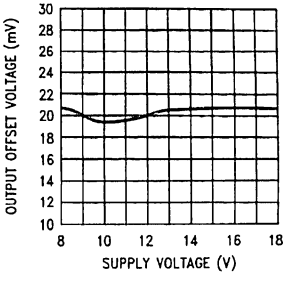
Device Dissipation vs Ambient Temperature



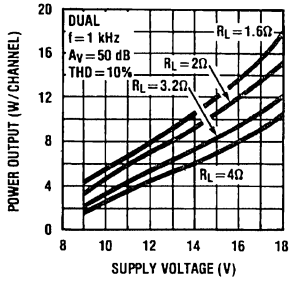
Supply Current vs Supply Voltage



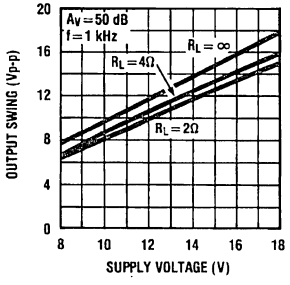
Output Offset Voltage vs Supply Voltage



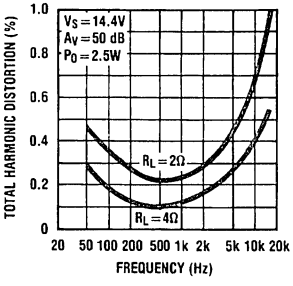
Power Output vs Supply Voltage



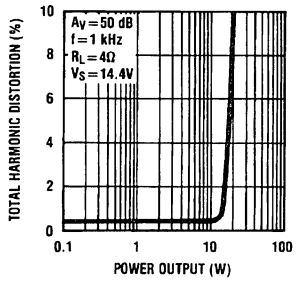
Output Swing vs Supply Voltage



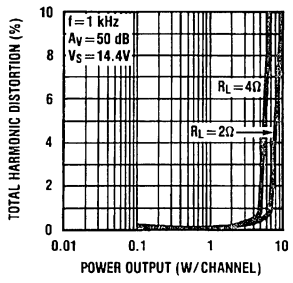
Total Harmonic Distortion vs Frequency (Dual)



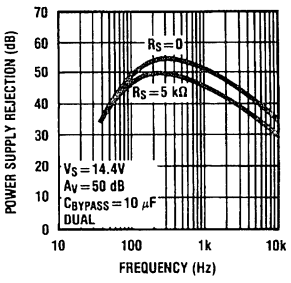
Total Harmonic Distortion vs Power Output (Bridge)



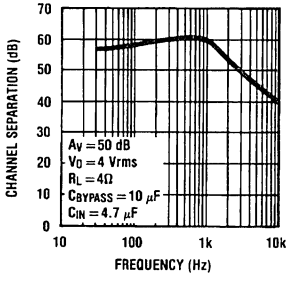
Total Harmonic Distortion vs Power Output (Dual)



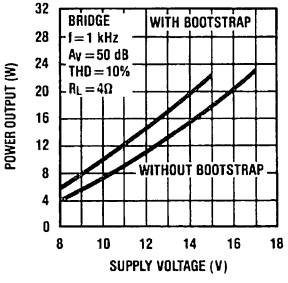
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



Channel Separation (Referred to the Output) vs Frequency



Power Output vs Supply Voltage



TL/H/5129–5

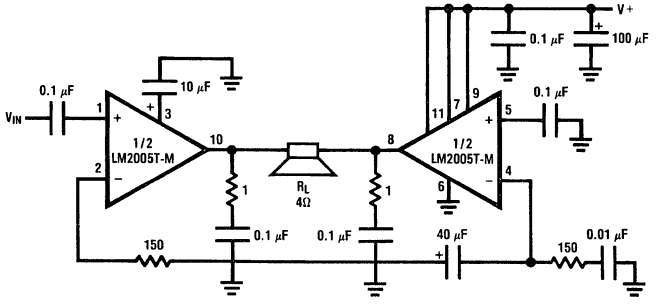
Application Hints

The high current capability of the LM2005 allows it to continuously endure either AC or DC short circuit of the output with a maximum supply voltage of 16V. This will protect the loudspeaker in a bridge mode, when a DC short of the output occurs on one side of the speaker. The device will prevent the speaker from destruction by reducing the DC across the load (bridge mode) to typically less than 2 V_{DC}(V_S = 14.4V, R_L = 4Ω), by an internal current pullback method.

The LM2005 can withstand a constant 28 V_{DC} on the supply with no damage (maximum operating voltage is 18V). The device is also protected from load dump or dangerous transients up to 40V for 50 ms (every 1000 ms) on the supply with no damage.

Protection diodes protect the device driving inductive loads, during which the load can generate voltages greater than supply or less than ground levels. The protection diodes will clamp these transients to a safe V_{BE} above and below the rails.

The bridge configuration in *Figure 3* is designed for applications requiring minimal printed circuit board area and maximum cost effectiveness. The circuit will function with the elimination of bootstrap components R3, C4 and C5 (refer to *Figure 1*). This will result in less output power by decreasing output voltage swing to the load. By using internal feedback resistors (typically 10 kΩ), feedback components R2, R3 and C2 (*Figure 1*) may be omitted where closed loop voltage gain accuracy is not critical. The net result is a stable, cost effective circuit that will satisfy many application needs.

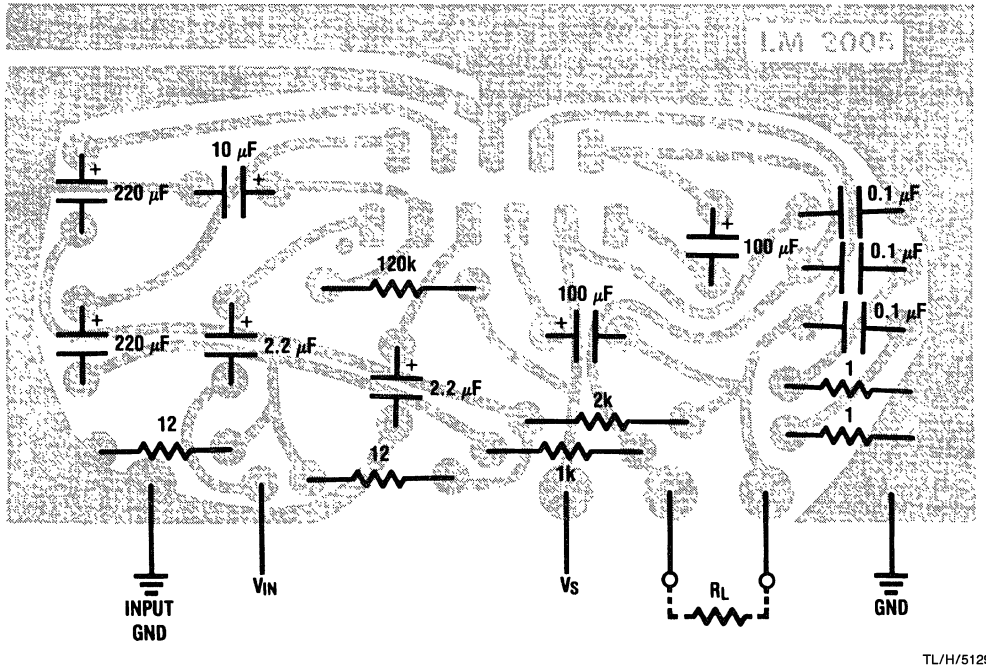


TL/H/5129–6

A_V = 41.5 dB @ 1 kHz

FIGURE 3. Minimal Component Application Circuit

Component Side (Scale 2:1)



TL/H/5129–7

FIGURE 4. Printed Circuit Board Layout for LM2005

National Semiconductor Corporation

LM2877 Dual 4-Watt Power Audio Amplifier

General Description

The LM2877 is a monolithic dual power amplifier designed to deliver 4W/channel continuous into 8Ω loads. The LM2877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection and output Q point centering. The LM2877 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package.

Features

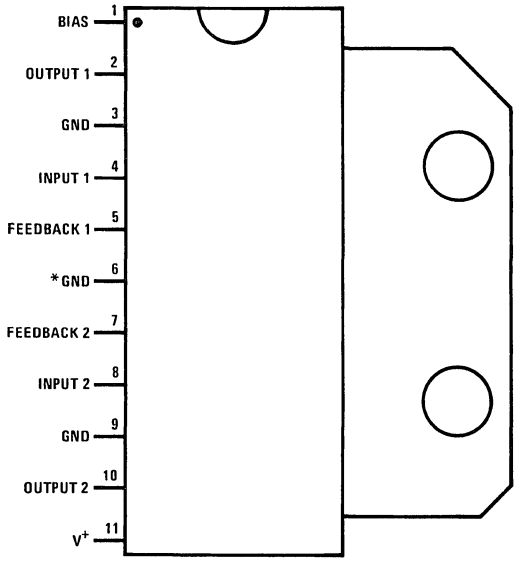
- 4W/channel
- −68 dB ripple rejection, output referred
- −70 dB channel separation, output referred
- Wide supply range, 6-24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

(Single-In-Line Package)



TL/H/7933–1

Top View

Order Number LM2877P
See NS Package Number P11A

*Pin 6 can be connected to pin 3 or pin 9, if not, pin 6 must be left with NO connection.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	26V
Input Voltage	±0.7V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec.)	260°C

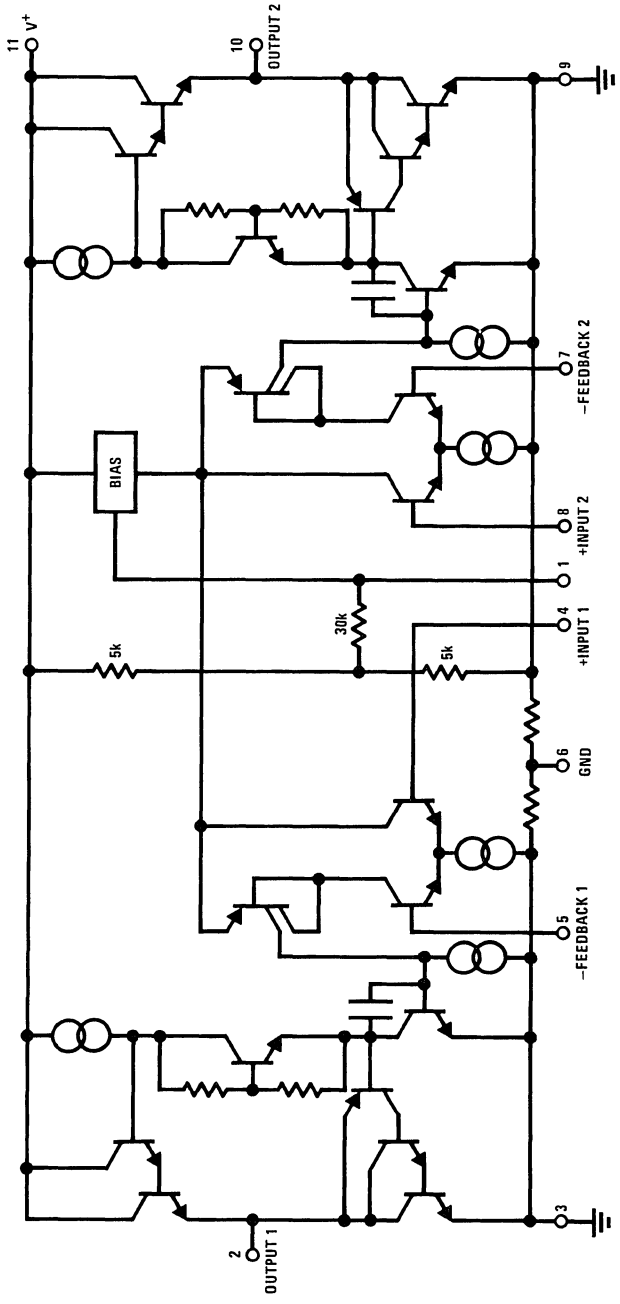
Electrical Characteristics V_S = 20V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		25	50	mA
Operating Supply Voltage		6		24	V
Output Power/Channel	f = 1 kHz, THD = 10%, T_{TAB} = 25°C				
	V_S = 20V	4.0	4.5		W
	V_S = 18V		3.6		W
	V_S = 12V, R_L = 4Ω	1.5	1.9		W
Distortion, THD	f = 1 kHz, V_S = 20V				
	P_O = 50 mW/Channel		0.1		%
	P_O = 1W/Channel		0.07	1	%
	P_O = 2W/Channel		0.07		%
	f = 1 kHz, V_S = 12V, R_L = 4Ω				
	P_O = 50 mW/Channel		0.25		%
	P_O = 500 mW/Channel		0.20		%
	P_O = 1W/Channel		0.15	1	%
Output Swing	R_L = 8Ω		V_S−4		V_{p-p}
Channel Separation	C_F = 50 μF, C_{IN} = 0.1 μF, f = 1 kHz, Output Referred				
	V_S = 20V, V_O = 4 Vrms	−50	−70		dB
	V_S = 7V, V_O = 0.5 Vrms		−60		dB
PSRR Power Supply	C_F = 50 μF, C_{IN} = 0.1 μF, f = 120 Hz				
Rejection Ratio	Output Referred				
	V_S = 20V, V_{RIPPLE} = 1 Vrms	−50	−68		dB
	V_S = 7V, V_{RIPPLE} = 0.5 Vrms		−40		dB
Noise	Equivalent Input Noise				
	R_S = 0, C_{IN} = 0.1 μF, BW = 20 Hz–20 kHz		2.5		μV
	Output Noise Wideband				
	R_S = 0, C_{IN} = 0.1 μF, A_V = 200		0.80		mV
Open Loop Gain	R_S = 0, f = 1 kHz, R_L = 8Ω		70		dB
Input Offset Voltage			15		mV
Input Bias Current			50		nA
Input Impedance	Open Loop		4		MΩ
DC Output Level	V_S = 20V	9	10	11	V
Slew Rate			2.0		V/μs
Power Bandwidth			65		kHz
Current Limit			1.0		A

Note 1: For operation at ambient temperature greater than 25°C, the LM2877 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

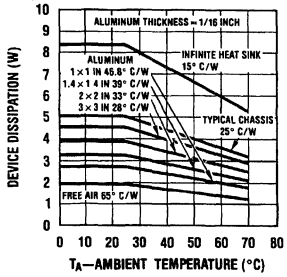
Equivalent Schematic Diagram

TL/H/7933–2

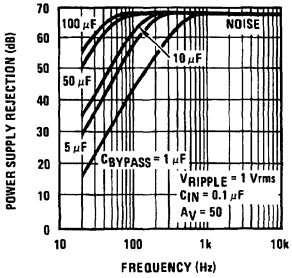


Typical Performance Characteristics

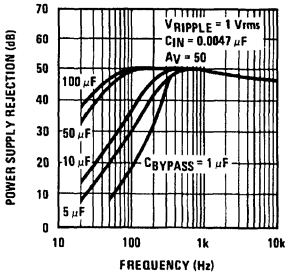
Device Dissipation vs Ambient Temperature



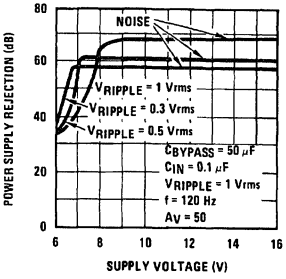
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



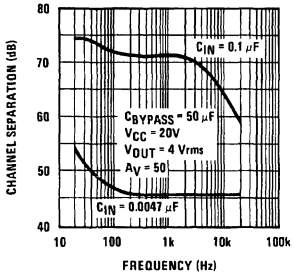
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



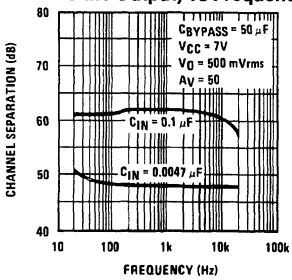
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



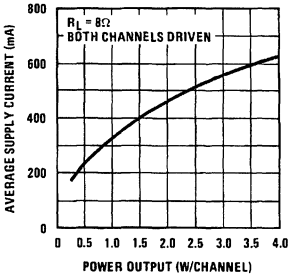
Channel Separation (Referred) to the Output) vs Frequency



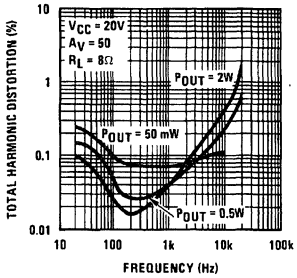
Channel Separation (Referred) to the Output) vs Frequency



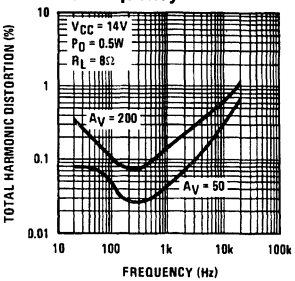
Average Supply Current vs Power Output



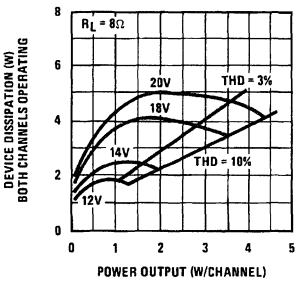
Total Harmonic Distortion vs Frequency



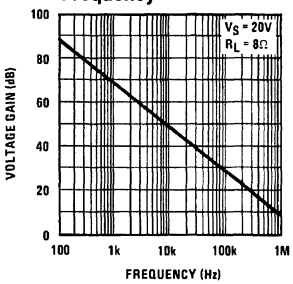
Total Harmonic Distortion vs Frequency



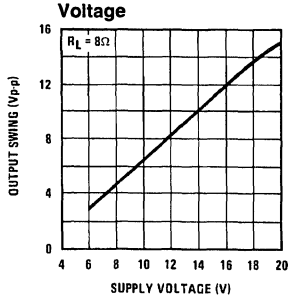
Power Dissipation vs Power Output



Open Loop Gain vs Frequency



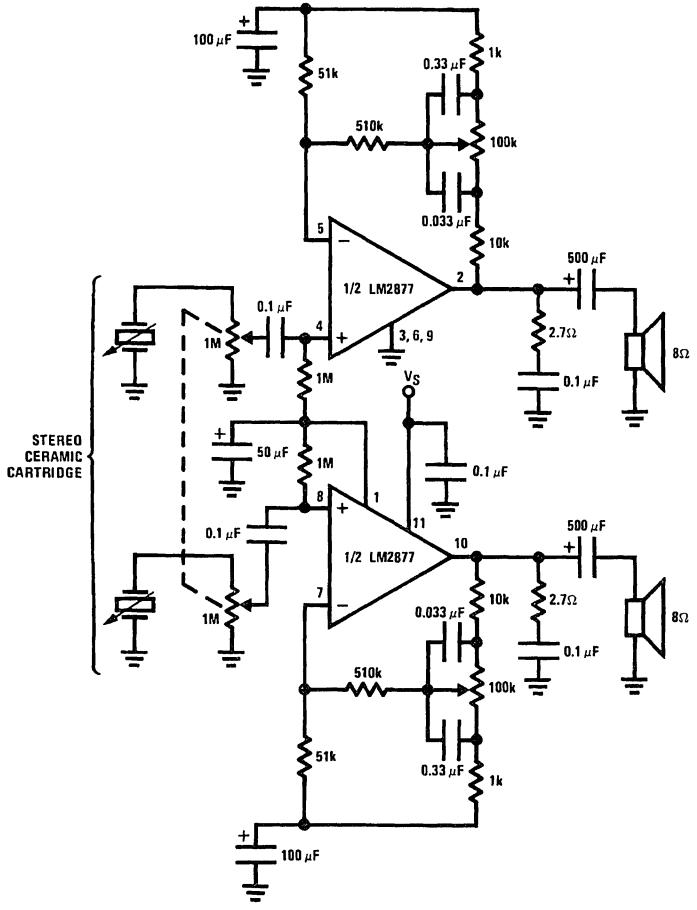
Output Swing vs Supply Voltage



TL/H/7933–3

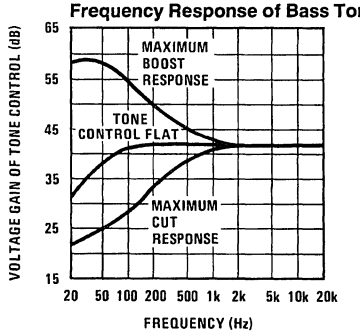
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control



TL/H/7933–4

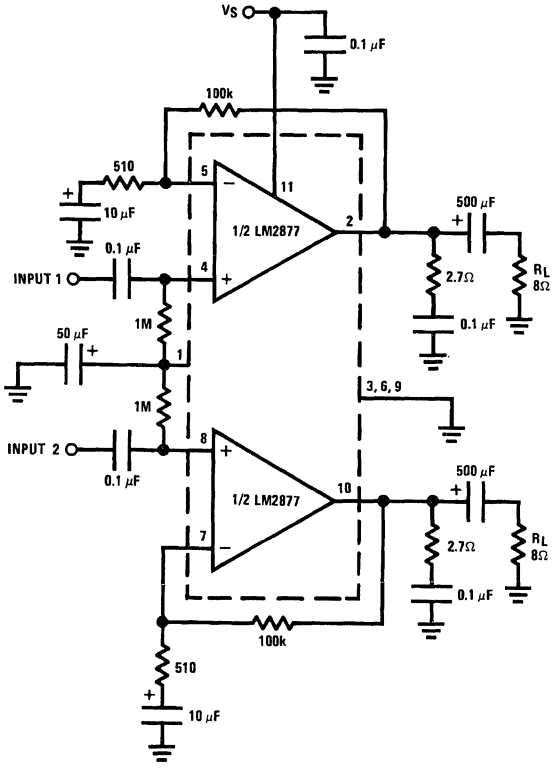
Frequency Response of Bass Tone Control



TL/H/7933–5

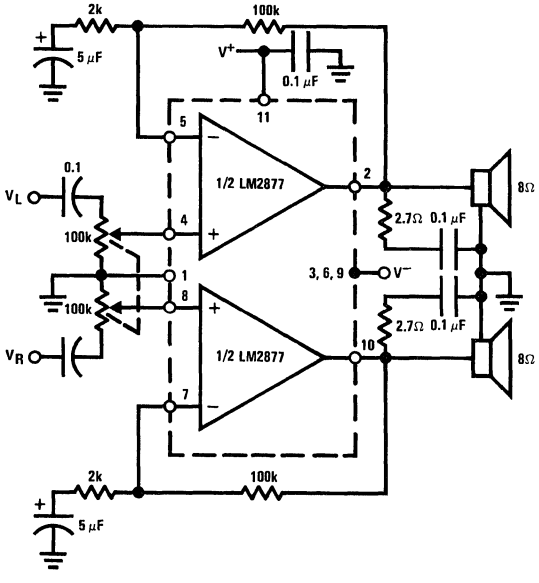
Typical Applications (Continued)

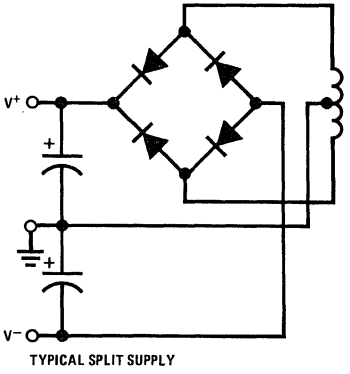
Stereo Amplifier with $A_V = 200$



TL/H/7933–6

Non-Inverting Amplifier Using Split Supply



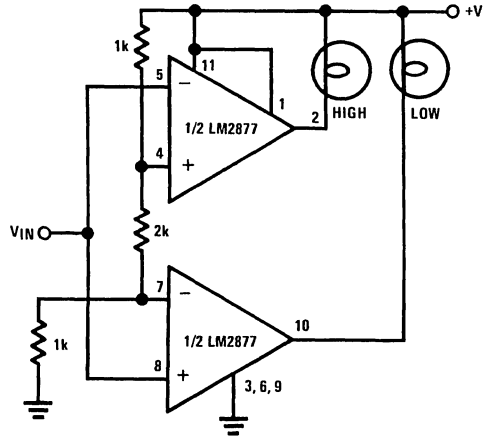


TYPICAL SPLIT SUPPLY

TL/H/7933–7

Typical Applications (Continued)

Window Comparator Driving High, Low Lamps



TL/H/7933–8

Truth Table

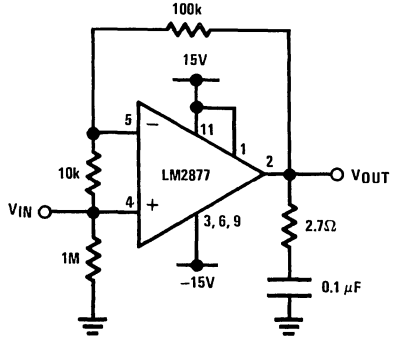
V_{IN}	High	Low
$< 1/4\ V^+$	Off	On
$1/4\ V^+$ to $3/4\ V^+$	Off	Off
$> 3/4\ V^+$	On	Off

Application Hints

The LM2877 is an improved LM377 in typical audio applications. In the LM2877, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless, the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2877 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 1 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.



TL/H/7933–9

FIGURE 1

National Semiconductor Corporation

LM2878 Dual 5 Watt Power Audio Amplifier

General Description

The LM2878 is a high voltage stereo power amplifier designed to deliver 5W/channel continuous into 8Ω loads. The amplifier is ideal for use with low regulation power supplies due to the absolute maximum rating of 35V and its superior power supply rejection. The LM2878 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders, and AM-FM stereo receivers. The flexibility of the LM2878 allows it to be used as a power operational amplifier, power comparator or servo amplifier. The LM2878 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package (SIP). The package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

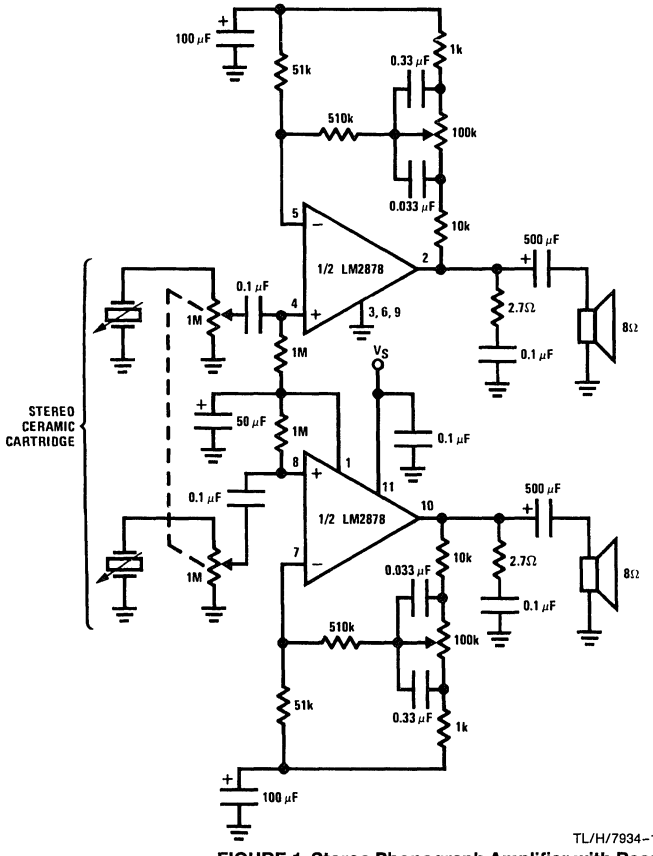
Features

- Wide operating range 6V–32V
- 5W/channel output
- 60 dB ripple rejection, output referred
- 70 dB channel separation, output referred
- Low crossover distortion
- AC short circuit protected
- Internal thermal shutdown

Applications

- Stereo phonographs
- AM-FM radio receivers
- Power op amp, power comparator
- Servo amplifiers

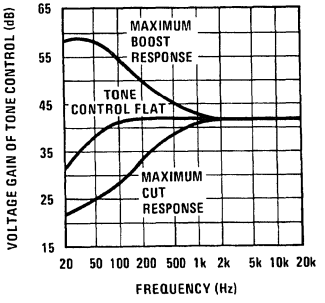
Typical Applications



TL/H/7934-1

FIGURE 1. Stereo Phonograph Amplifier with Bass Tone Control

Frequency Response of Bass Tone Control



TL/H/7934-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	+260°C

Electrical Characteristics

V_S = 22V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 50 (34 dB) unless otherwise specified.

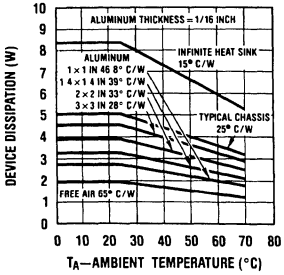
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	P_O = 0W		10	50	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, T_{TAB} = 25°C	5	5.5		W
Distortion	f = 1 kHz, R_L = 8Ω P_O = 50 mW		0.20		%
	P_O = 0.5W		0.15		%
	P_O = 2W		0.14		%
Output Swing	R_L = 8Ω		V_S − 6V		Vp-p
Channel Separation	C_{BYPASS} = 50 μF, C_{IN} = 0.1 μF f = 1 kHz, Output Referred V_O = 4 Vrms	−50	−70		dB
PSRR Power Supply Rejection Ratio	C_{BYPASS} = 50 μF, C_{IN} = 0.1 μF f = 120 Hz, Output Referred V_{ripple} = 1 Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise R_S = 0, C_{IN} = 0.1 μF BW = 20 − 20 kHz		2.5		μV
	CCIR•ARM		3.0		μV
	Output Noise Wideband R_S = 0, C_{IN} = 0.1 μF, A_V = 200		0.8		mV
Open Loop Gain	R_S = 51Ω, f = 1 kHz, R_L = 8Ω		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	V_S = 22V	10	11	12	V
Slew Rate			2		V/μS
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: ±0.7V applies to audio applications; for extended range, see Application Hints.

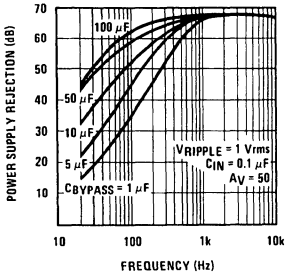
Note 2: For operation at ambient temperature greater than 25°C, the LM2878 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Typical Performance Characteristics

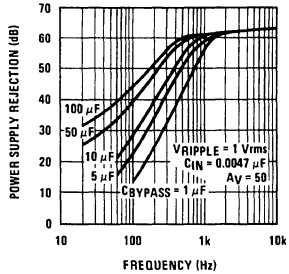
Device Dissipation vs Ambient Temperature



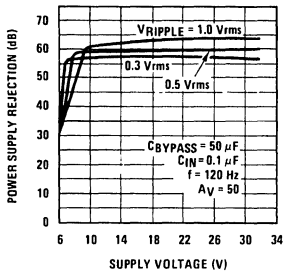
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



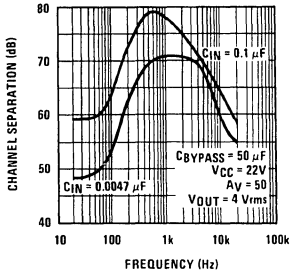
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



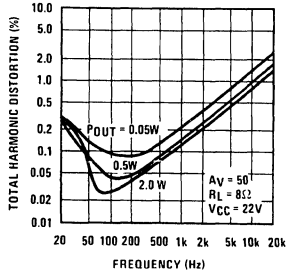
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



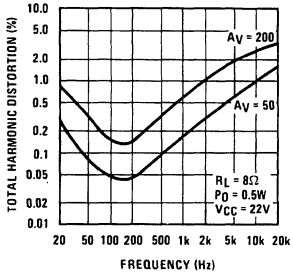
Channel Separation (Referred to the Output) vs Frequency



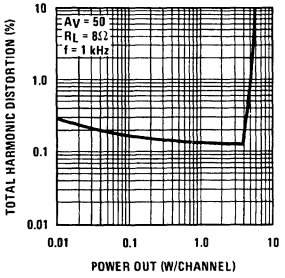
Total Harmonic Distortion vs Frequency



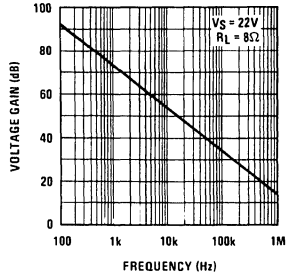
Total Harmonic Distortion vs Frequency



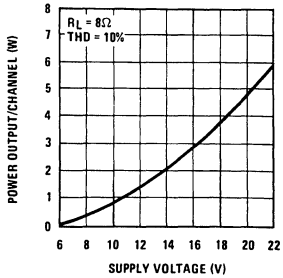
Total Harmonic Distortion vs Power Out



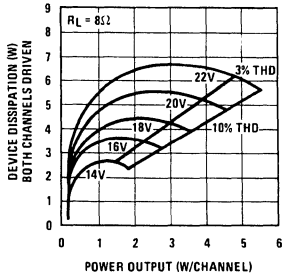
Open Loop Gain vs Frequency



Power Output/Channel vs Supply Voltage

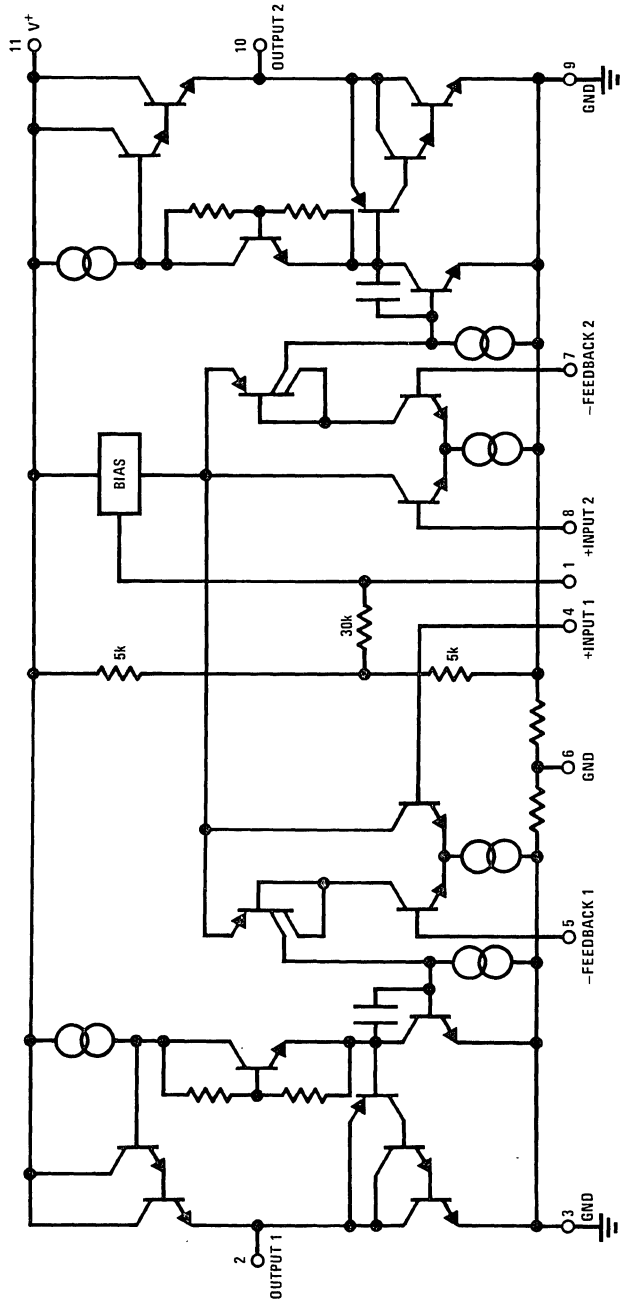


Power Dissipation vs Power Out



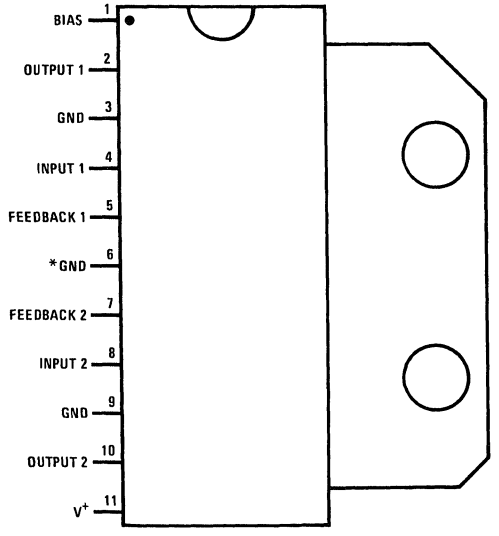
TL/H/7934–3

Equivalent Schematic Diagram



Connection Diagram

Single-In-Line Package



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Top View

*Pin 6 can be connected to pin 3 or pin 9, if not, pin 6 must be left with NO connection.

Order Number LM2878P
See NS Package Number P11A

Application Hints

The LM2878 is an improved LM378 in typical audio applications. In the LM2878, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within ±0.7V of this pin 1 voltage. Nevertheless the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2878 is to limit the maximum input differential voltage to ±7V. If this differential voltage is exceeded, the input characteristics may change.

Figure 2 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 MΩ resistor.

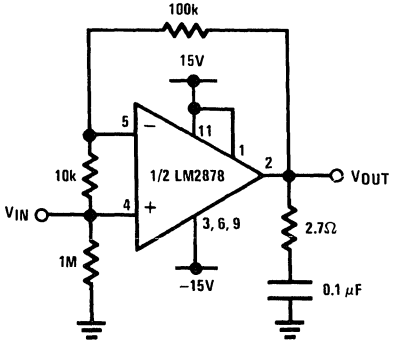

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FIGURE 2. Operational Power Amplifier, $A_V = 1$

External Components *(Figure 3)*

1. R2, R5, R7, R10 Sets voltage gain $A_V = 1 + R2/R5$ for one channel and $A_V = 1 + R10/R7$ for the other channel.
2. R4, R8 Resistors set input impedance and supply bias current for the positive input.
3. R_O Works with C_O to stabilize output stage.
4. C1 Improves power supply rejection (see Typical Performance Characteristics).
5. C11 Stabilizes amplifier, may need to be larger depending on power supply filtering.
6. C4, C8 Input coupling capacitor. Pins 4 and 8 are at a DC potential of $V_S/2$. Low frequency pole set by:

$$f_L = \frac{1}{2\pi R4C4}$$

7. C5, C7 Feedback capacitors. Ensure unity gain at DC. Also low frequency pole at:

$$f_L = \frac{1}{2\pi R5C5}$$

8. C_O Works with R_O to stabilize output stage.
9. C2, C10 Output coupling capacitor. Low frequency pole given by:

$$f_L = \frac{1}{R\pi RLC2}$$

Typical Applications (Continued)

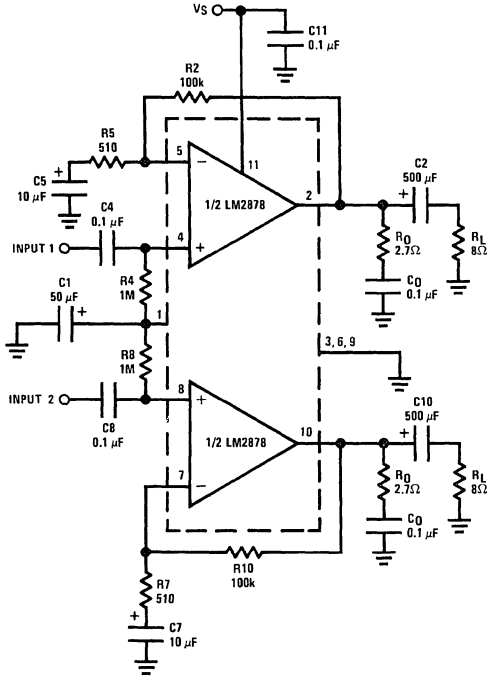

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FIGURE 3. Stereo Amplifier with $A_V = 200$

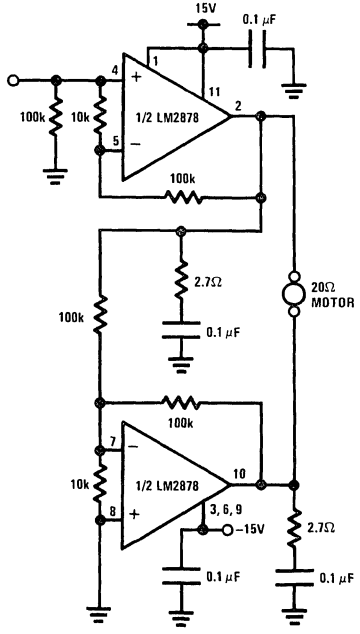

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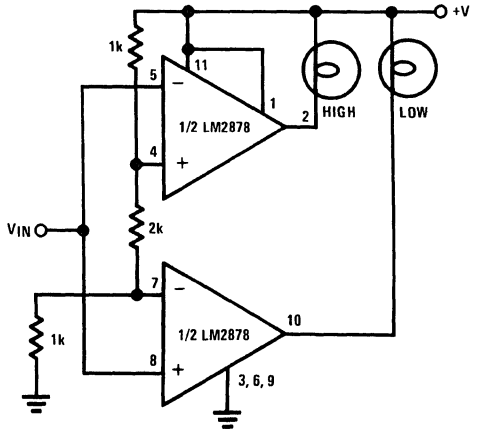
FIGURE 4. LM2878 Servo Amplifier in Bridge Configuration

Typical Applications (Continued)



Truth Table

V_{IN}	High	Low
$<1/4V^+$	Off	On
$1/4V^+$ to $3/4V^+$	Off	Off
$>3/4V^+$	On	Off

TL/H/7934–9

FIGURE 5. Window Comparator Driving High, Low Lamps

National Semiconductor Corporation

LM2879 Dual 8-Watt Audio Amplifier

General Description

The LM2879 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, AM-FM stereo receivers, etc.

The LM2879 will deliver 8W/channel to an 8Ω load. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown.

Features

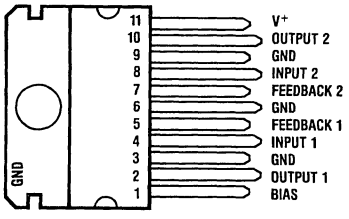
- A_{VO} typical 90 dB
- 9W per channel (typical)
- 60 dB ripple rejection
- 70 dB channel separation
- Self-centering biasing
- 4 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Applications

- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Connection Diagram and Typical Application

Plastic Package

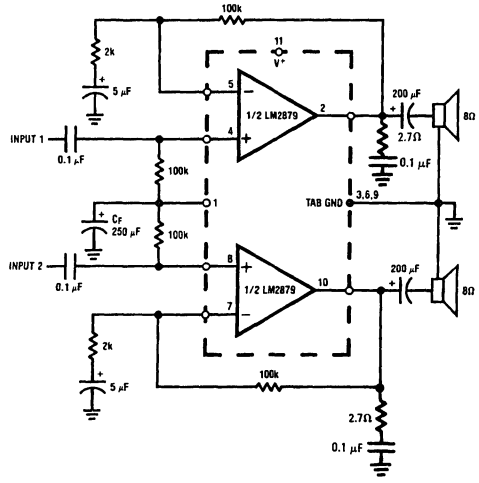


TOP VIEW

TL/H/5291–1

Order Number LM2879T
See NS Package Number T11A

Stereo Amplifier



TL/H/5291–2

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	35V
Input Voltage (Note 1)	±0.7V
Operating Temperature (Note 2)	0°C to + 70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Lead Temp. (Soldering, 10 seconds)	260°C

ESD rating to be determined.

Electrical Characteristics $V_S = 28V$, $T_{TAB} = 25°C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB), unless otherwise specified.

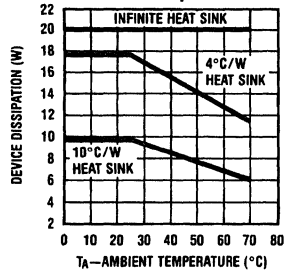
Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_O = 0W$		12	65	mA
Operating Supply Voltage		6		32	V
Output Power/Channel	f = 1 kHz, THD = 10%, $T_{TAB} = 25°C$	6	8		W
Distortion	f = 1 kHz, $R_L = 8\Omega$ P_O = 1 W/Channel		0.05	1	%
Output Swing	$R_L = 8\Omega$		$V_S - 6V$		Vp-p
Channel Separation	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 1 kHz, Output Referred V_O = 4 Vrms	−50	−70		dB
PSRR Positive Supply	$C_{BYPASS} = 50\ \mu F$, $C_{IN} = 0.1\ \mu F$ f = 120 Hz, Output Referred V_{ripple} = 1 Vrms	−50	−60		dB
PSRR Negative Supply	Measured at DC, Input Referred		−60		dB
Common-Mode Range	Split Supplies ±15V, Pin 1 Tied to Pin 11		±13.5		V
Input Offset Voltage			10		mV
Noise	Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\ \mu F$ BW = 20 −20 kHz CCIR•ARM Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\ \mu F$, $A_V = 200$		 2.5 3.0 0.8		 μV μV mV
Open Loop Gain	$R_S = 51\Omega$, f = 1 kHz, $R_L = 8\Omega$		70		dB
Input Bias Current			100		nA
Input Impedance	Open Loop		4		MΩ
DC Output Voltage	$V_S = 28V$		14		V
Slew Rate			2		V/μs
Power Bandwidth	3 dB Bandwidth at 2.5W		65		kHz
Current Limit			1.5		A

Note 1: The input voltage range is normally limited to ±0.7V with respect to pin 1. This range may be extended by shorting pin 1 to the positive supply.

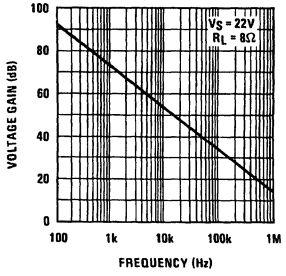
Note 2: For operation at ambient temperature greater than 25°C, the LM2879 must be derated based on a maximum 150°C junction temperature. Thermal resistance, junction to case, is 3°C/W. Thermal resistance, case to ambient, is 40°C/W.

Typical Performance Characteristics

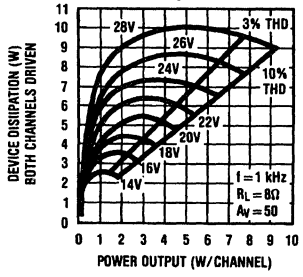
Device Dissipation vs Ambient Temperature



Open Loop Gain vs Frequency



Power Dissipation vs Power Output



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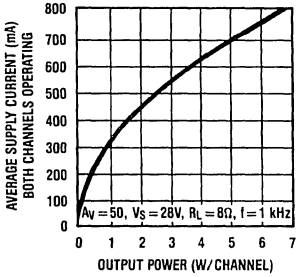
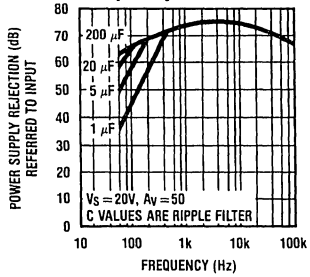
Typical Performance Characteristics (Continued)

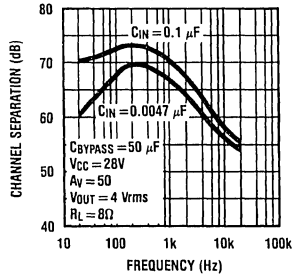
Supply Current vs Output Power



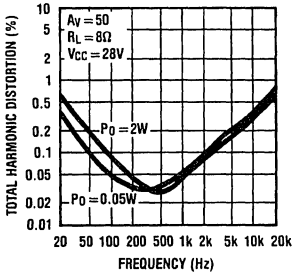
Supply Rejection vs Frequency



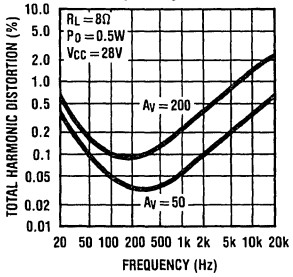
Channel Separation (Referred to the Output) Frequency



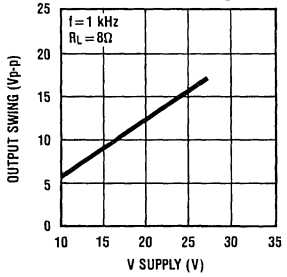
Total Harmonic Distortion vs Frequency



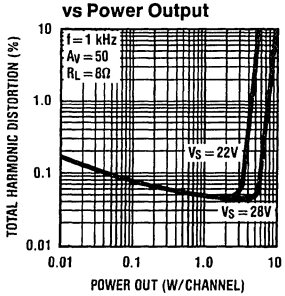
Total Harmonic Distortion vs Frequency



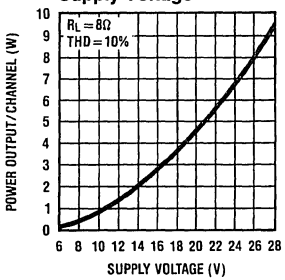
Output Swing vs V_S



Total Harmonic Distortion vs Power Output

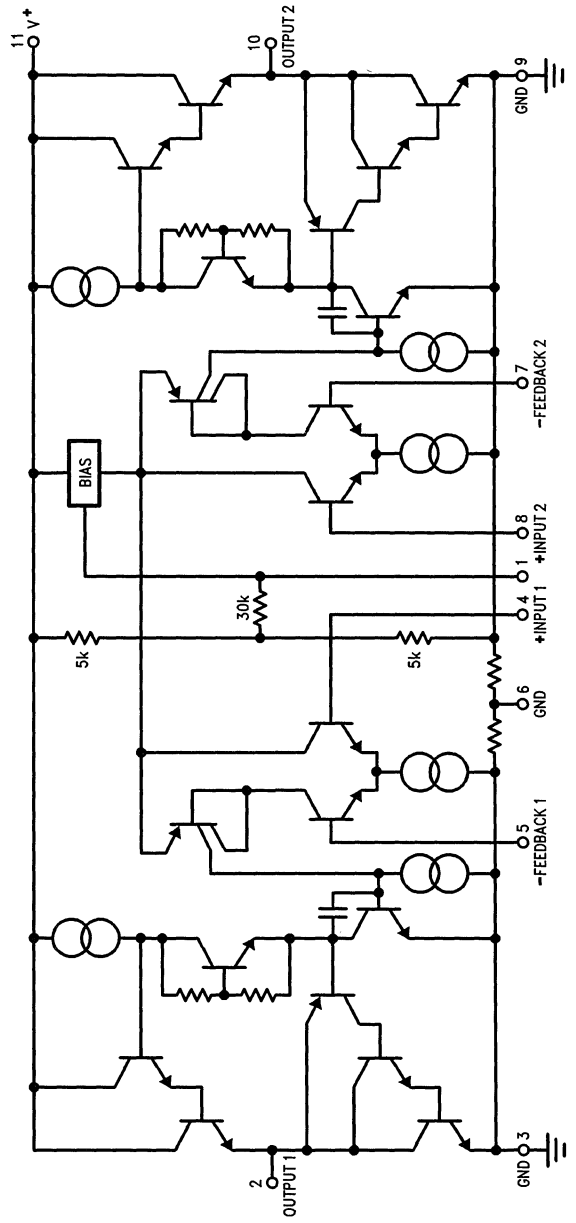


Power Output/Channel vs Supply Voltage



TL/H/5291–4

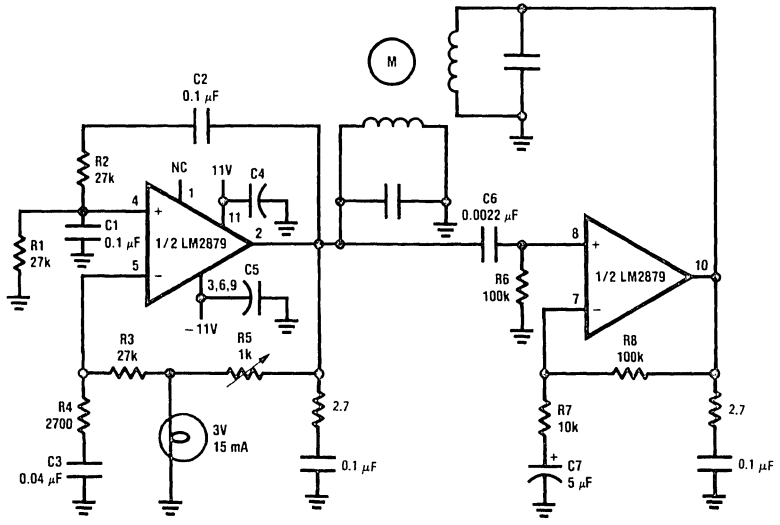
Equivalent Schematic Diagram



TL/H/5291–5

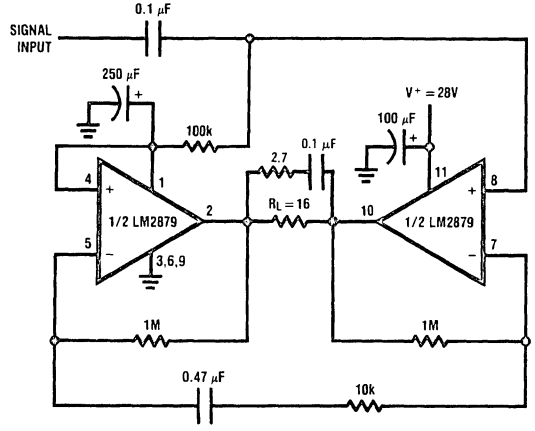
Typical Applications

Two-Phase Motor Drive



TL/H/5291–6

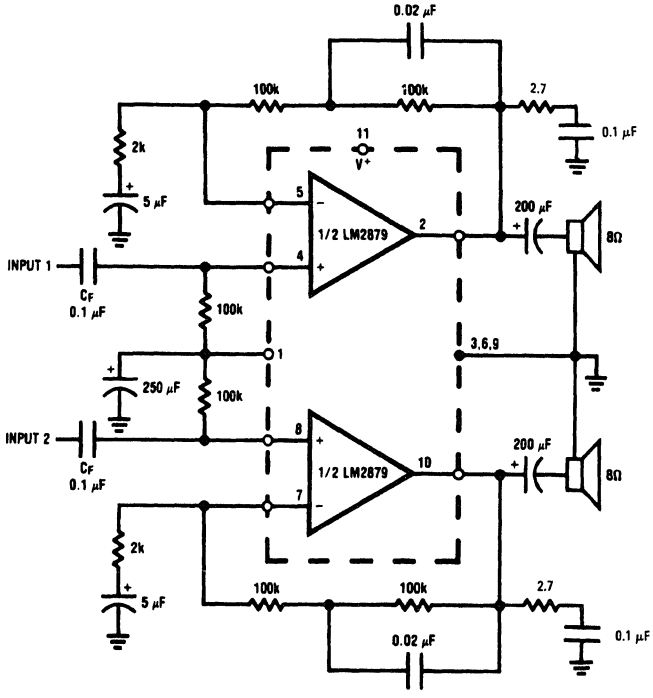
12W Bridge Amplifier



TL/H/5291–7

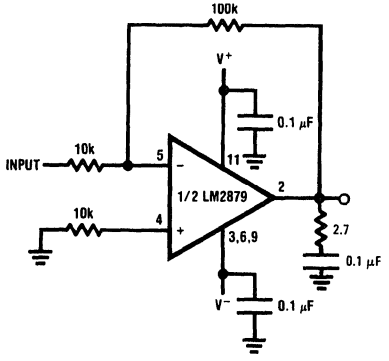
Typical Applications (Continued)

Simple Stereo Amplifier with Bass Boost



TL/H/5291–8

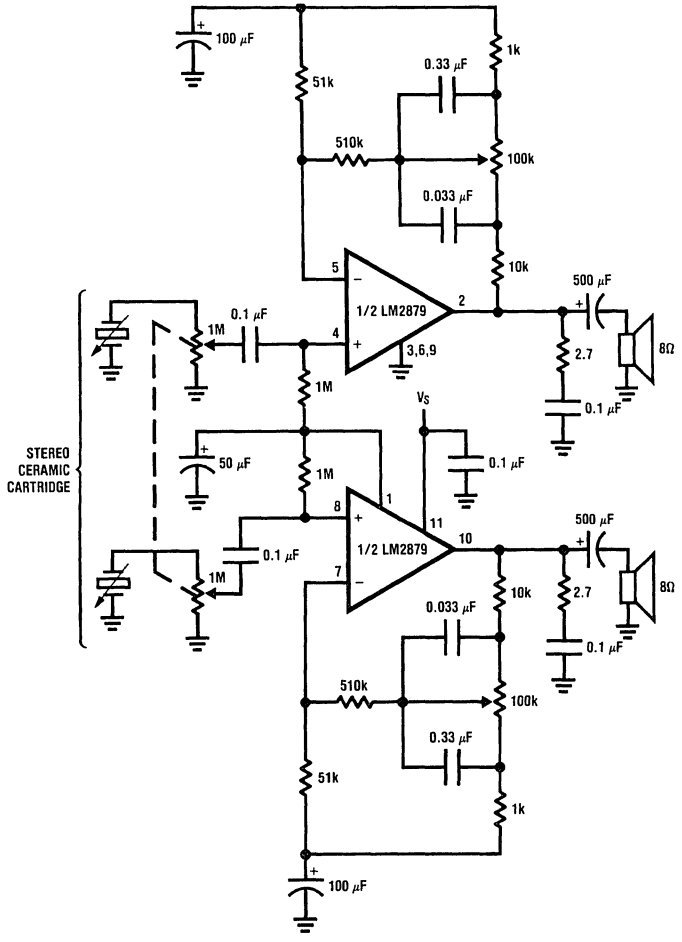
Power Op Amp (Using Split Supplies)



TL/H/5291–9

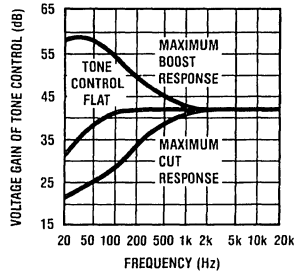
Typical Applications (Continued)

Stereo Phonograph Amplifier with Bass Tone Control



TL/H/5291–10

Frequency Response of Bass Tone Control



TL/H/5291–11

National Semiconductor Corporation

LMC835 Digital Controlled Graphic Equalizer

General Description

The LMC835 is a monolithic, digitally-controlled graphic equalizer CMOS LSI for Hi-Fi audio. The LMC835 consists of a Logic section and a Signal Path section made of analog switches and thin-film silicon-chromium resistor networks. The LMC835 is used with external resonator circuits to make a stereo equalizer with seven bands, ±12 dB or ±6 dB gain range and 25 steps each. Only three digital inputs are needed to control the equalization. The LMC835 makes it easy to build a μP-controlled equalizer.

The signal path is designed for very low noise and distortion, resulting in very high performance, compatible with PCM audio.

Features

- No volume controls required
- Three-wire interface
- 14 bands, 25 steps each
- ±12 dB or ±6 dB gain ranges
- Low noise and distortion
- TTL, CMOS logic compatible

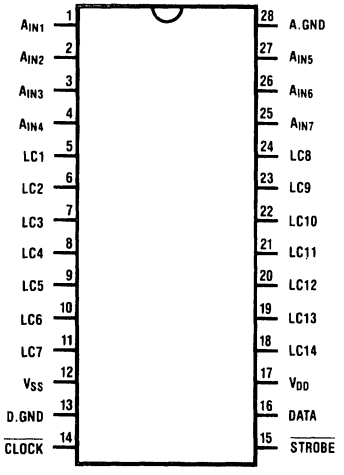
Applications

- Hi-Fi equalizer
- Receiver
- Car stereo
- Musical instrument
- Tape equalization
- Mixer
- Volume controller

Connection Diagram

Order Number LMC835N
See NS Package N28B

Dual-In-Line Package



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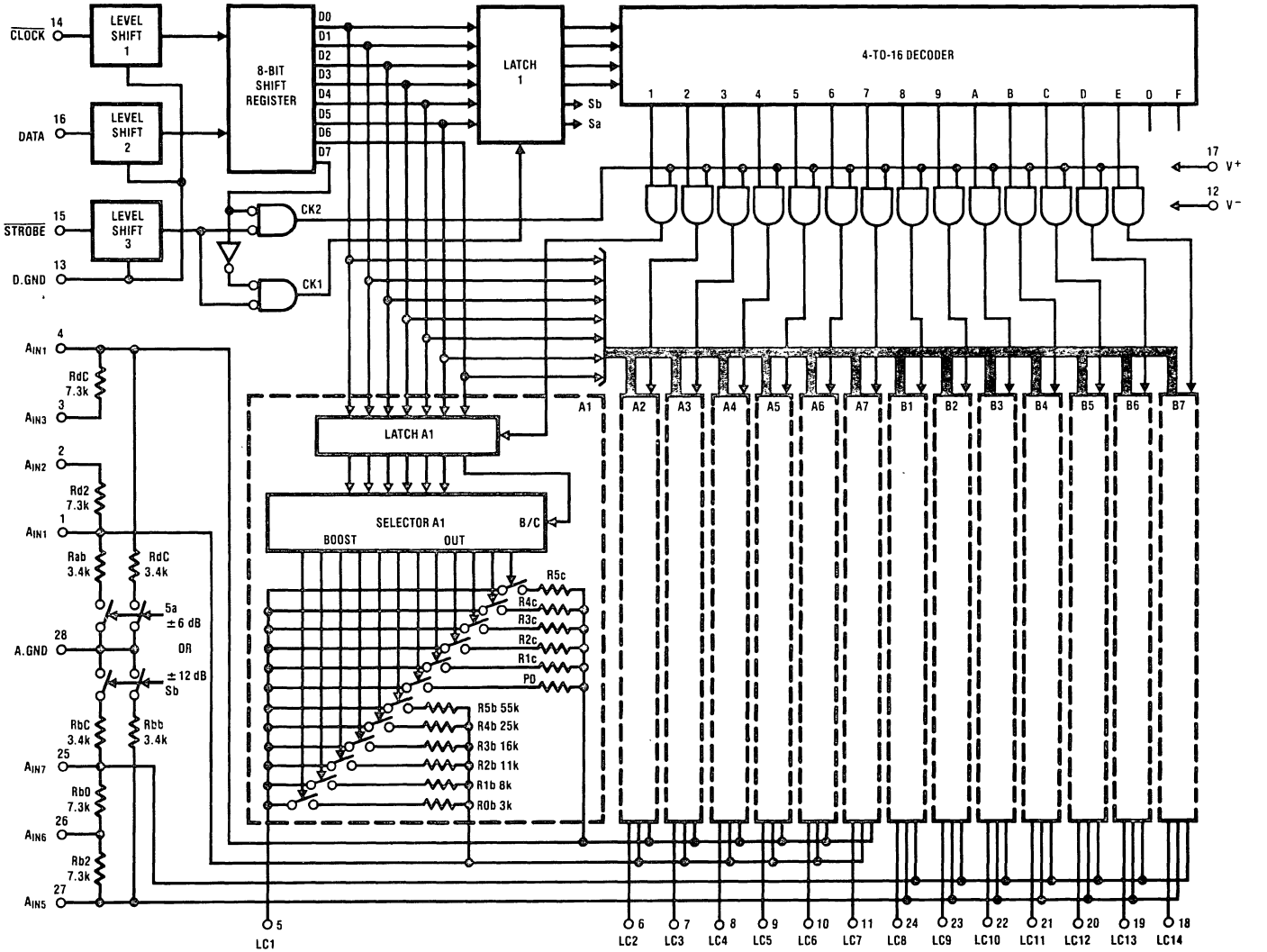
Top View


CLOCK
14
LEVEL SHIFT 1
8-BIT SHIFT REGISTER
D0
D1
D2
D3
D4
D5
D6
D7
LATCH 1
Sb
Sa
4-TO-16 DECODER
1 2 3 4 5 6 7 8 9 A B C D E O F
17
V+
12
V−
DATA
16
LEVEL SHIFT 2
STROBE
15
LEVEL SHIFT 3
CK2
CK1
D.GND
13
AIN1
4
RdC 7.3k
AIN3
3
AIN2
2
Rd2 7.3k
AIN1
1
Rab 3.4k
RdC 3.4k
5a
± 6 dB
A.GND
28
OR
± 12 dB
Sb
RbC 3.4k
Rbb 3.4k
AIN7
25
Rb0 7.3k
AIN6
26
Rb2 7.3k
AIN5
27
LATCH A1
SELECTOR A1
B/C
BOOST
OUT
R5c
R4c
R3c
R2c
R1c
P0
R5b 55k
R4b 25k
R3b 16k
R2b 11k
R1b 8k
R0b 3k
A1
A2
A3
A4
A5
A6
A7
B1
B2
B3
B4
B5
B6
B7
LC1
5
LC2
6
LC3
7
LC4
8
LC5
9
LC6
10
LC7
11
LC8
24
LC9
23
LC10
22
LC11
21
LC12
20
LC13
19
LC14
18

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, $V_{DD}-V_{SS}$	18V
Allowable Input Voltage (Note 1)	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage Temperature, T_{stg}	−60°C to +150°C
Lead Temperature (Soldering, 10 sec), T_L	+260°C

Operating Ratings

Supply Voltage, $V_{DD}-V_{SS}$	5V to 16V
Digital Ground (Pin 13)	V_{SS} to V_{DD}
Digital Input (Pins 14, 15, 16)	V_{SS} to V_{DD}
Analog Input (Pins 1, 2, 3, 4, 25, 26, 27) (Note 1)	V_{SS} to V_{DD}
Operating Temperature, T_{opr}	−40°C to +85°C

Electrical Characteristics (Note 2) $V_{DD}=7.5V$, $V_{SS}=-7.5V$, A.GND=0V

LOGIC SECTION

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
I_{DDL}	Supply Current	Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{SSL}		Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{DDH}		Pins 14, 15, 16 are 5V	1.3	5	**5**	mA (Max)
I_{SSH}		Pins 14, 15, 16 are 5V	0.9	5	**5**	mA (Max)
V_{IH}	High-Level Input Voltage	@Pins 14, 15, 16	1.8	2.3	**2.5**	V (Min)
V_{IL}	Low-Level Input Voltage	@Pins 14, 15, 16	0.9	0.6	**0.4**	V (Max)
f_o	Clock Frequency	@Pin 14	2000	500	**500**	kHz (Max)
$t_{w(\overline{STB})}$	Width of $\overline{STB}$ Input	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{setup}	Data Setup Time	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{hold}	Data Hold Time	See *Figure 1*	0.25	1	**1**	μs (Min)
t_{cs}	Delay from Rising Edge of $\overline{CLOCK}$ to $\overline{STB}$	See *Figure 1*	0.25	1	**1**	μs (Min)
I_{IN}	Input Current	@Pins 14, 15, 16 $0V<V_{IN}<5V$	±0.01	±1		μA (Max)
C_{IN}	Input Capacitance	@Pins 14, 15, 16 f=1 MHz	5			pF

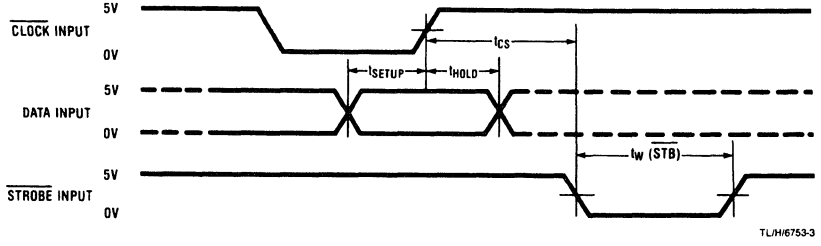
Note 1: Pins 2, 3 and 26 have a maximum input voltage range of ±22V for the typical application shown in *Figure 7*.

Note 2: Bold numbers apply at temperature extremes. All other numbers apply at $T_A=25°C$, $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND=A.GND=0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagram



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Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 1

Electrical Characteristics (Note 2) $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND=A.GND=0V

SIGNAL PATH SECTION

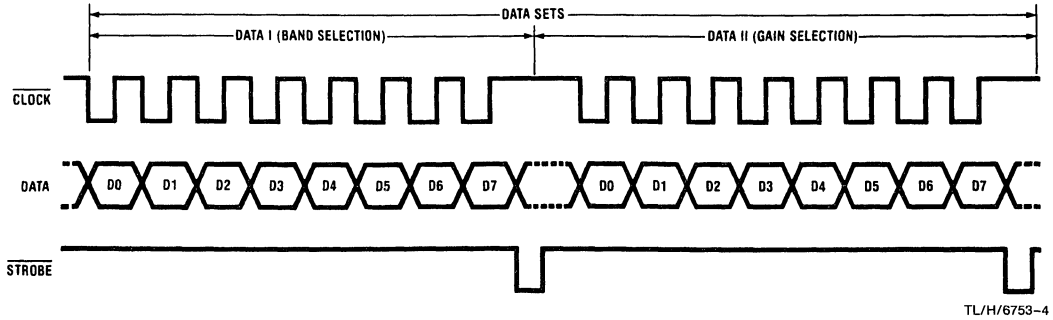
Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
E_A	Gain Error	$A_V=0$ dB @ ± 12 dB Range	0.1	0.5	**0.5**	dB (Max)
		$A_V=0$ dB @ ± 6 dB Range	0.1	1	**1**	dB (Max)
		$A_V=\pm1$ dB @ ± dB Range (R_{5b} or R_{5c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm2$ dB @ ± 12 dB Range (R_{4b} or R_{4c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm3$ dB @ ± 12 dB Range (R_{3b} or R_{3c} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm4$ dB @ ± 12 dB Range (R_{2b} or R_{2c} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V=\pm5$ dB @ ± 12 dB Range (R_{1b} or R_{1c} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V=\pm9$ dB @ ± 12 dB Range (R_{0b} or R_{0c} is ON)	0.2	1	**1.3**	dB (Max)
THD	Total Harmonic Distortion	$A_V=0$ dB @ ± 12 dB Range $V_{IN}=4V_{rms}$, f=1 kHz	0.0015			%
		$A_V=12$ dB @ ± 12 dB Range				
		$V_{IN}=1V_{rms}$, f=1 kHz	0.01	0.1		% (Max)
		$V_{IN}=1V_{rms}$, f=20 kHz	0.1	0.5		% (Max)
		$A_V=-12$ dB @ ± 12 dB Range				
		$V_{IN}=4V_{rms}$, f=1 kHz	0.01	0.1		% (Max)
		$V_{IN}=4V_{rms}$, f=20 kHz	0.1	0.5		% (Max)
$V_{O\ Max}$	Maximum Output Voltage	$A_V=0$ dB @ ± 12 dB Range THD <1%, f=1 kHz	5.5	5.1	**5**	V_{rms} (Min)
S/N	Signal to Noise Ratio	$A_V=0$ dB @ ± 12 dB Range $V_{ref}=1\ V_{rms}$	114			dB
		$A_V=12$ dB @ ± 12 dB Range $V_{ref}=1V_{rms}$	106			dB
		$A_V=-12$ dB @ ± 12 dB Range $V_{ref}=1V_{rms}$	116			dB
I_{LEAK}	Leakage Current	$A_V=0$ dB @ ± 12 dB Range (All internal switches are OFF)				
		Pin 2+3, Pin 26		500		nA (Max)
		Pin 5~Pin 11, Pin 18~Pin 24		50		nA (Max)

Note 2; Boldface numbers apply at temperature extremes. All other numbers apply at $T_A=25°C$, $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND=A.GND=0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagrams



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Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 2

Truth Tables

DATA I (Band Selection)

D7	D6	D5	D4	D3	D2	D1	D0
H	X	L	L	L	L	L	L
H	X	L	L	L	L	L	H
H	X	L	L	L	L	H	L
H	X	L	L	L	L	H	H
H	X	L	L	L	H	L	L
H	X	L	L	L	H	L	H
H	X	L	L	L	H	H	L
H	X	L	L	L	H	H	H
H	X	L	L	H	L	L	L
H	X	L	L	H	L	L	H
H	X	L	L	H	L	H	L
H	X	L	L	H	L	H	H
H	X	L	L	H	H	L	L
H	X	L	L	H	H	L	H
H	X	L	L	H	H	H	L
H	X	L	L	H	H	H	H
H	X	L	H	Valid Binary Input			
H	X	H	L	Valid Binary Input			
H	X	H	H	Valid Binary Input			
↑ ①	↑ ②	↑ ③	↑ ④	← Band Code →			

(Ch A: Band 1 ~ 7, Ch B: Band 8 ~ 14)

Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 1
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 2
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 3
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 4
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 5
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 6
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 7
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 8
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 9
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 10
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 11
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 12
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 13
Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 14
Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
Ch A ± 12 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14
Ch A ± 6 dB Range, Ch B ± 12 dB Range, Band 1 ~ 14
Ch A ± 6 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14

① DATA 1
② Don't Care
③ Ch A ±6 dB/±12 dB Range
④ Ch B ±6 dB/±12 dB Range

This is the gain if the ±12 dB range is selected by DATA I. If the ±6 dB range is selected, then the values shown must be approximately halved. See the characteristics curves for more exact data.

DATA II (Gain Selection)

	D7	D6	D5	D4	D3	D2	D1	D0
Flat	L	X	L	L	L	L	L	L
1 dB Boost	L	H	H	L	L	L	L	L
2 dB Boost	L	H	L	H	L	L	L	L
3 dB Boost	L	H	L	L	H	L	L	L
4 dB Boost	L	H	L	L	L	H	L	L
5 dB Boost	L	H	L	L	L	L	H	L
6 dB Boost	L	H	L	H	L	L	H	L
7 dB Boost	L	H	H	L	H	L	H	L
8 dB Boost	L	H	L	H	L	H	H	L
9 dB Boost	L	H	L	L	L	L	L	H
10 dB Boost	L	H	H	L	H	L	L	H
11 dB Boost	L	H	H	L	H	H	L	H
12 dB Boost	L	H	H	L	H	H	H	H
1 dB ~ 12 dB Cut	L	L	Valid Above Input					
	↑ ⑤	↑ ⑥	← Gain Code →					

⑤ DATA II
⑥ Boost/Cut

Test Circuits

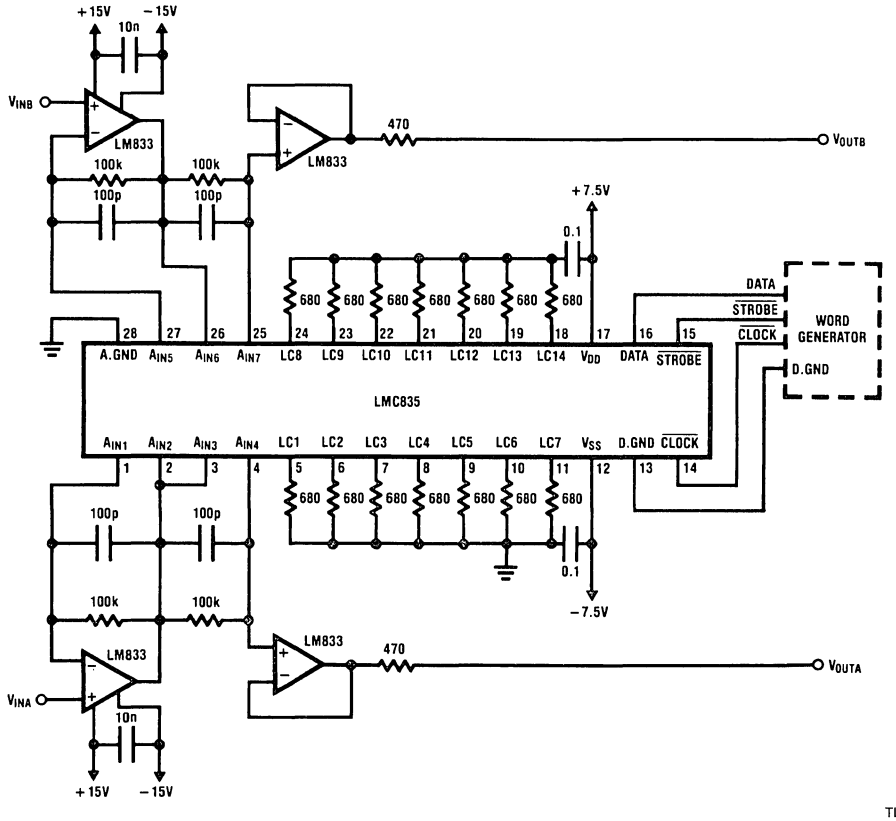

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FIGURE 3. Test Circuit for AC Measurement

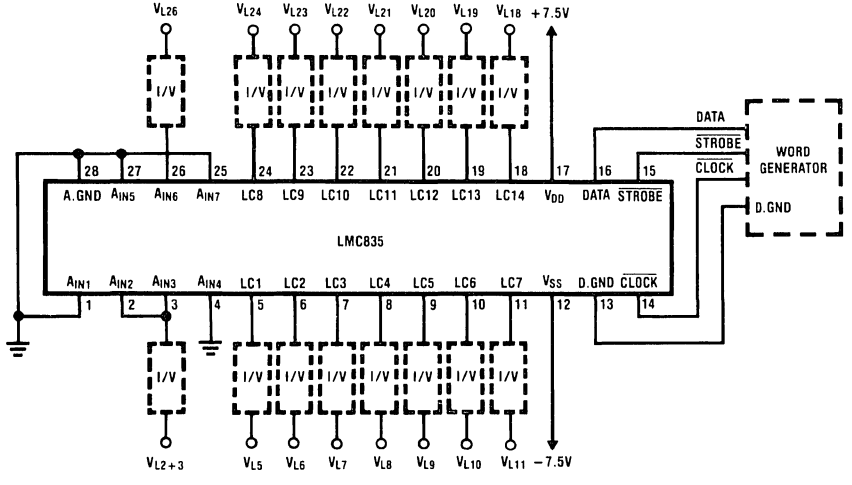

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FIGURE 4. Test Circuit for Leakage Current Measurement

Test Circuits (Continued)

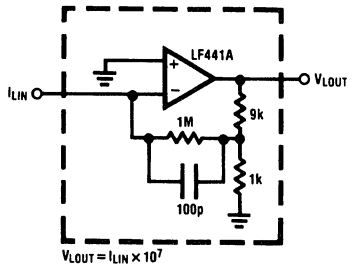

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FIGURE 5. I to V Converter

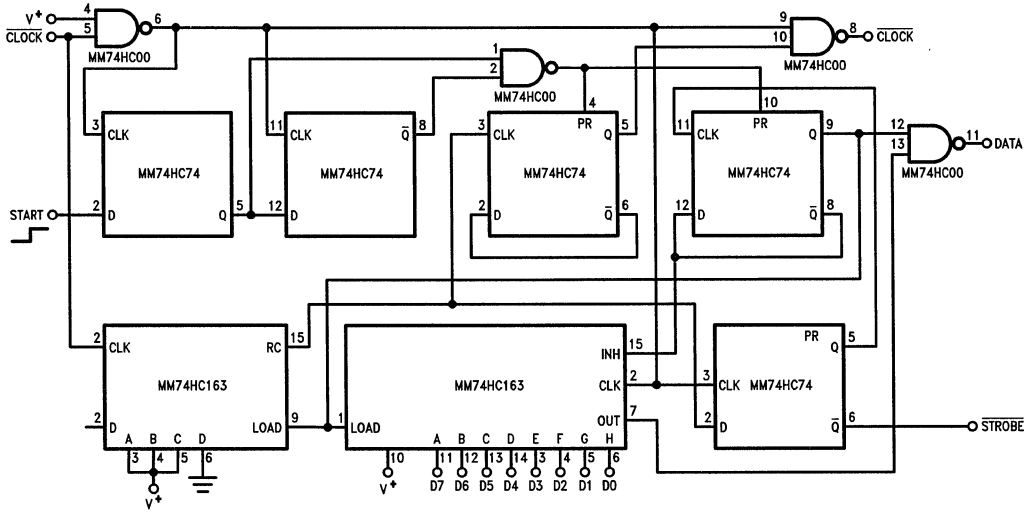

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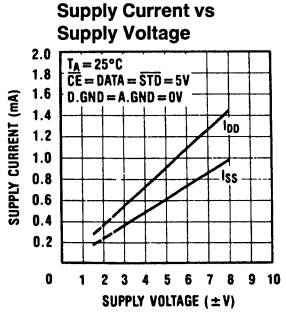
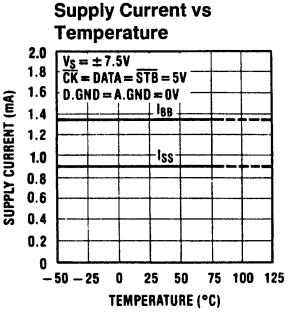
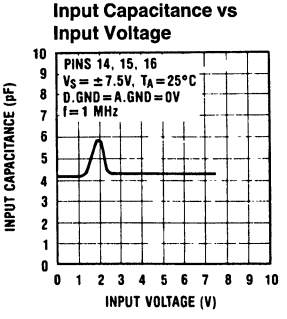
FIGURE 6. Simple Word Generator

Typical Performance Characteristics







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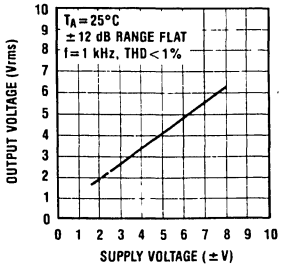
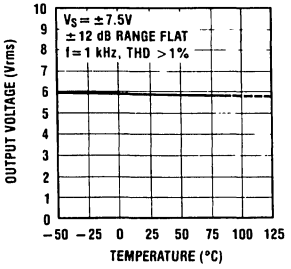
Typical Performance Characteristics (Continued)

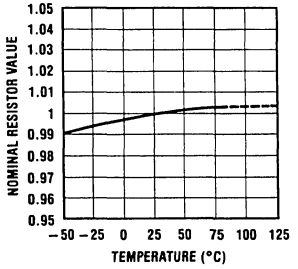
Maximum Output Voltage vs Supply Voltage



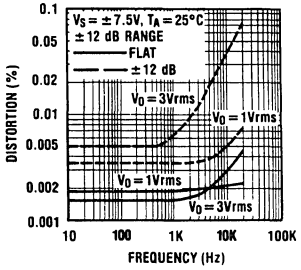
Maximum Output Voltage vs Temperature



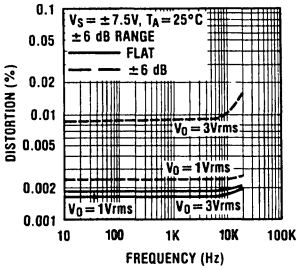
Nominal Resistor vs Temperature



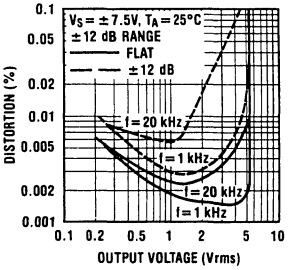
Distortion vs Frequency @ ± 12 dB Range



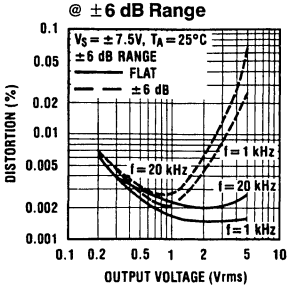
Distortion vs Frequency @ ±6 dB Range



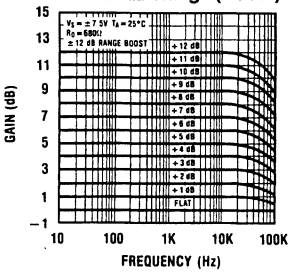
Distortion vs Output Voltage @ ± 12 dB Range



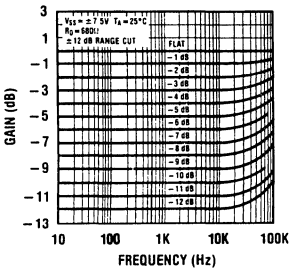
Distortion vs Output Voltage @ ±6 dB Range



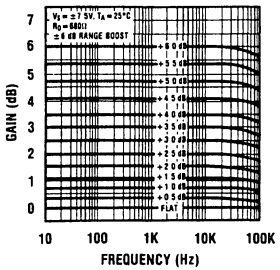
Gain vs Frequency @ ± 12 dB Range (Boost)



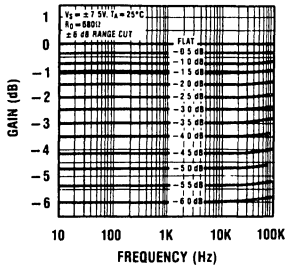
Gain vs Frequency @ ± 12 dB Range (Cut)



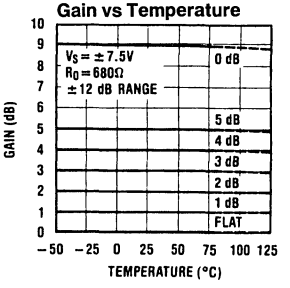
Gain vs Frequency @ ±6 dB Range (Boost)



Gain vs Frequency @ ±6 dB Range (Cut)



Gain vs Temperature



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Typical Applications

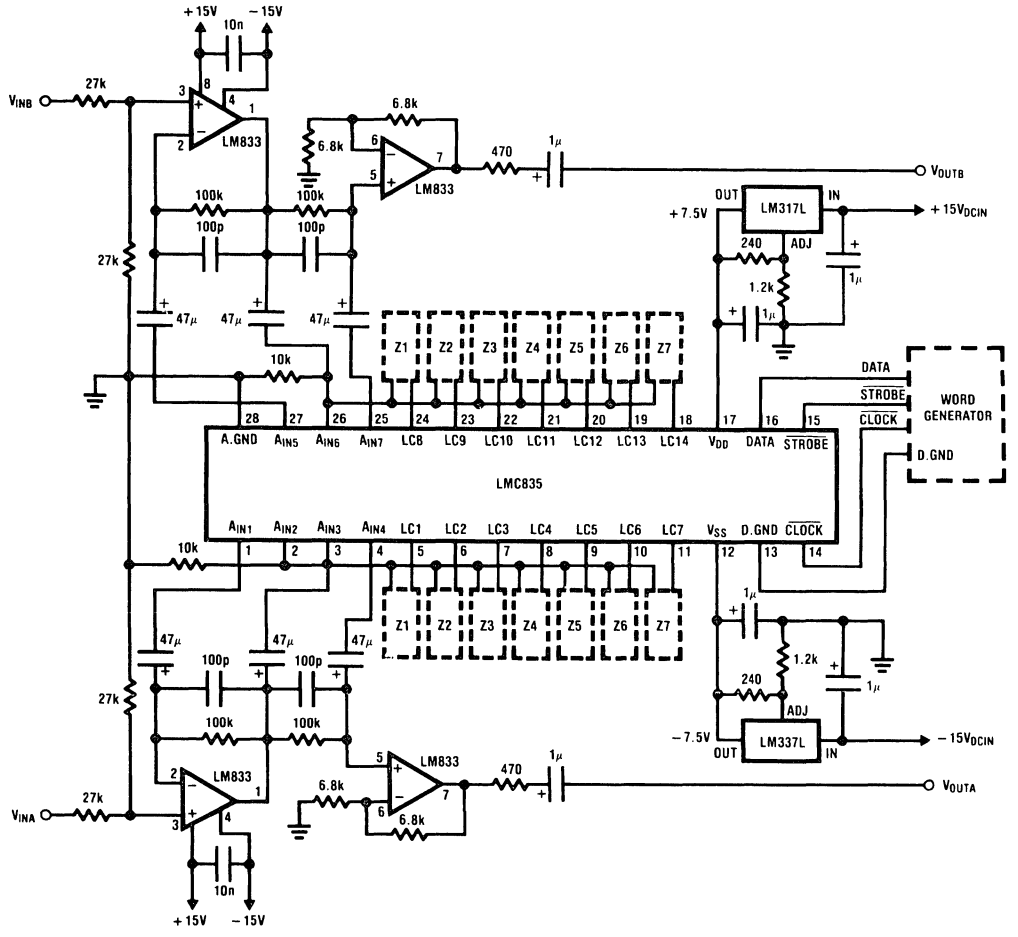

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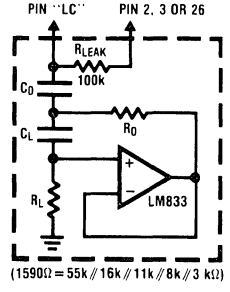
FIGURE 7. Stereo 7-Band Equalizer

TABLE I: Tuned Circuit Elements

$Q_0 = 3.5$, $Q_{12dB} = 1.05$					
Z1	**f_0 (Hz)**	**C_O (F)**	**C_L (F)**	**R_L (Ω)**	**R_O (Ω)**
Z1	63	1μ	0.1μ	100k	680
Z2	160	0.47μ	0.033μ	100k	680
Z3	400	0.15μ	0.015μ	100k	680
Z4	1k	0.068μ	0.0068μ	82k	680
Z5	2.5k	0.022μ	0.0033μ	82k	680
Z6	6.3k	0.01μ	0.0015μ	62k	680
Z7	16k	0.0047μ	680p	47k	680



$$L_O = C_L R_L R_O$$

$$f_0 = \frac{1}{2\pi\sqrt{L_O C_O}}$$

$$Q_O = \sqrt{\frac{L_O}{C_O R_O^2}}$$

$$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 1590}$$

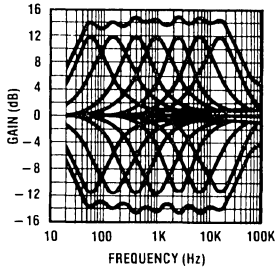
TL/H/6753–12

FIGURE 8. Tuned Circuit for Stereo 7-Band Equalizer (*Figure 7*)

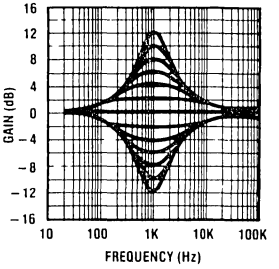
Typical Applications (Continued)

Performance Characteristics (Circuit of *Figure 7*)

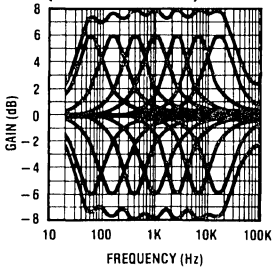
LMC835 Gain vs Frequency @ ± 12 dB Range (All Boost or Cut)



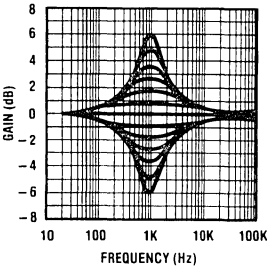
LMC835 Gain vs Frequency @ ± 12 dB Range (1 kHz Boost or Cut)



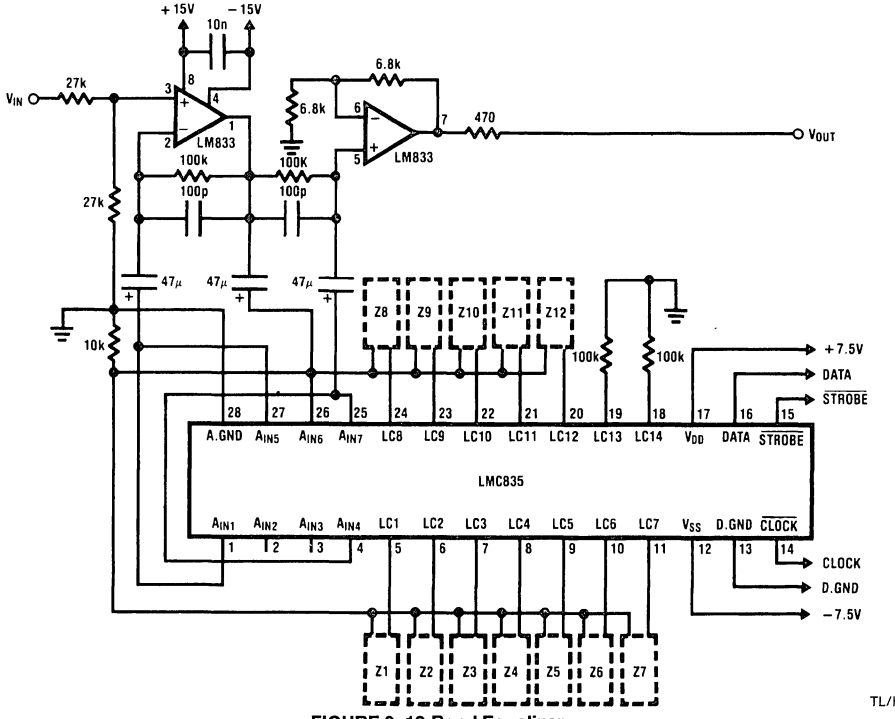
LMC835 Gain vs Frequency @ ±6 dB Range (All Boost or Cut)



LMC835 Gain vs Frequency @ ±6 dB Range (1 kHz Boost or Cut)



TL/H/6753–13



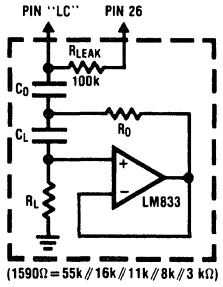
TL/H/6753–14

FIGURE 9. 12-Band Equalizer

Typical Applications (Continued)

TABLE II. Tuned Circuit Elements

$Q_0 = 4.7$, $Q_{12\,dB} = 1.4$					
	f_0 (Hz)	C_0 (F)	C_L (F)	R_L (Ω)	R_0 (Ω)
Z1	16	3.3μ	0.47μ	100k	680
Z2	31.5	15μ	0.22μ	110k	680
Z3	63	1μ	0.1μ	100k	680
Z4	125	0.39μ	0.068μ	91k	680
Z5	250	0.22μ	0.033μ	82k	680
Z6	500	0.1μ	0.015μ	100k	680
Z7	1k	0.047μ	0.01μ	82k	680
Z8	2k	0.022μ	0.0047μ	91k	680
Z9	4k	0.01μ	0.0022μ	110k	680
Z10	8k	0.0068μ	0.001μ	82k	680
Z11	16k	0.0033μ	680p	62k	680
Z12	32k	0.0015μ	470p	68k	510



$$L_0 = C_L R_L R_0$$

$$f_0 = \frac{1}{2\pi\sqrt{L_0 C_0}}$$

$$Q_0 = \sqrt{\frac{L_0}{C_0 R_0^2}}$$

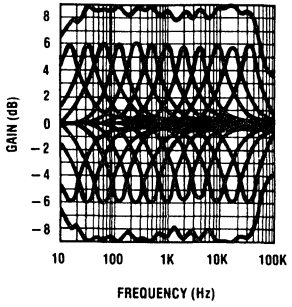
$$Q_{12\,dB} = \frac{R_0 Q_0}{R_0 + 1590}$$

TL/H/6753–15

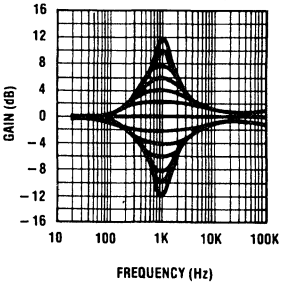
FIGURE 10. Tuned Circuit for 12-Band Equalizer (*Figure 9*)

Performance Characteristics (Circuit of Figure 9)

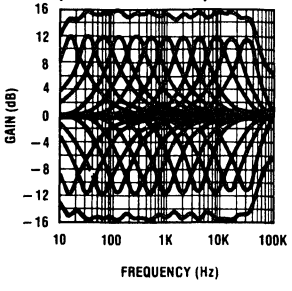
12 Band Equalizer Application
LMC835 Gain vs Frequency
@ ±6 dB Range
(All Boost or Cut)



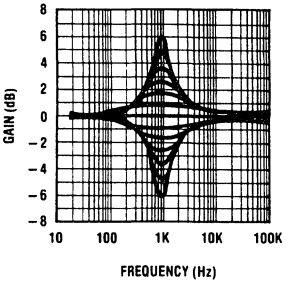
LMC835 12 Band E.Q. Application
Gain vs Frequency
@ ±12 dB Range
(1 kHz Boost or Cut)



12 Band Equalizer Application
LMC835 Gain vs Frequency
@ ± 12 dB Range
(All Boost or Cut)

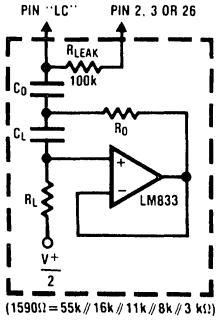


LMC835 12 Band E.Q. Application
Gain vs Frequency
@ ±6dB Range
(1 kHz Boost or Cut)



TL/H/6753–16

Typical Applications (Continued)



$L_O = C_L, R_L, R_O$

$F_O = \frac{1}{2\pi\sqrt{L_O C_O}}$

$Q_O = \sqrt{C_O R_O^2}$

$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 15°C}$

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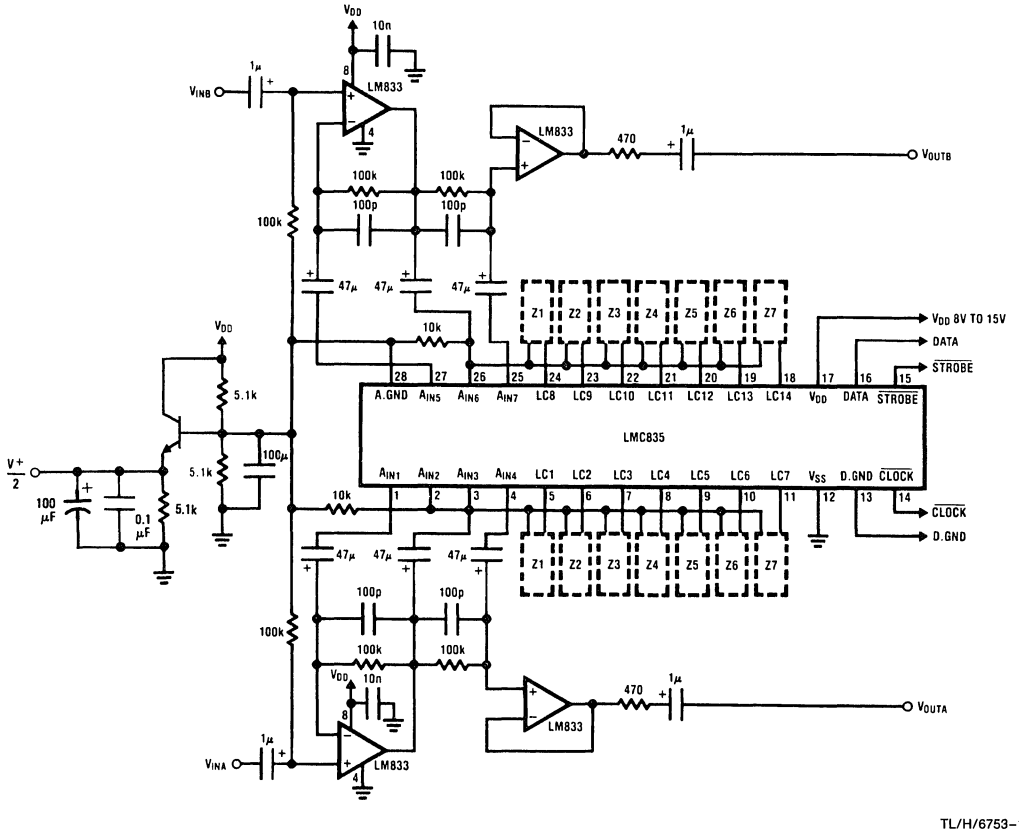


TL/H/6753–17

The $\frac{V+}{2}$ output is used to bias the gyrators

FIGURE 11. Single Supply Stereo Equalizer

Typical Applications (Continued)

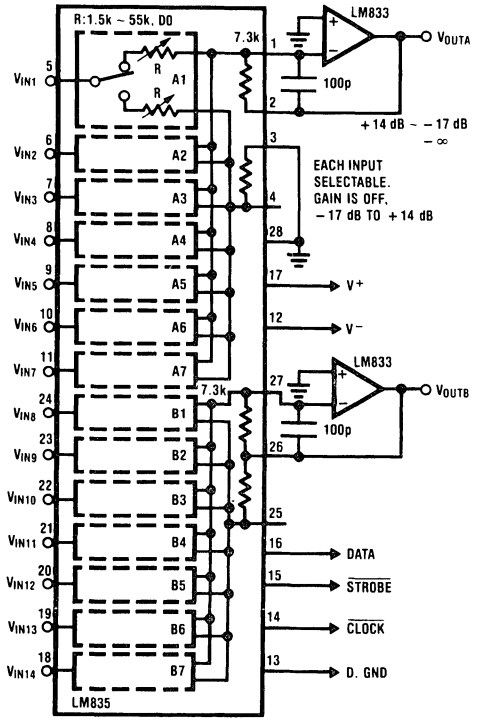


FIGURE 12. Stereo 7-Input/1-Output Mixers (THD is not as low as equalizer circuit)

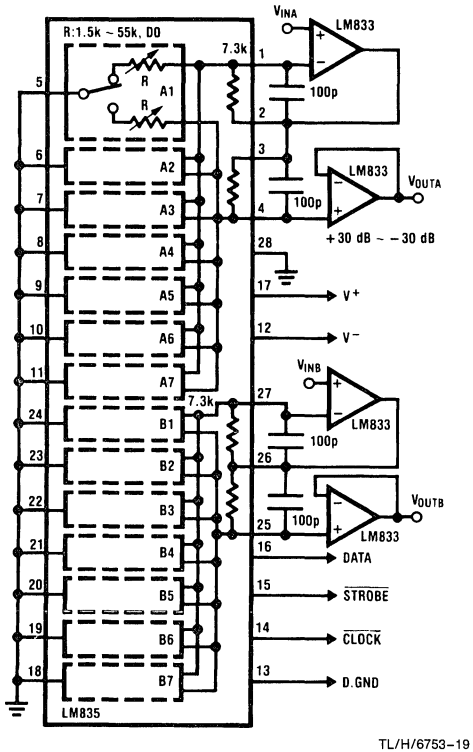


FIGURE 13. Stereo Volume Control, Very Low THD

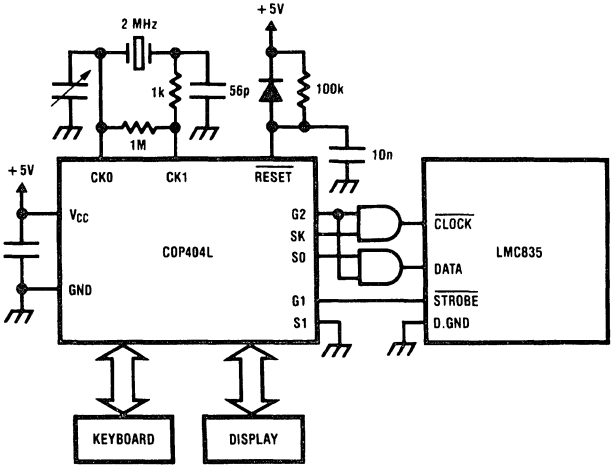


FIGURE 14. LMC835-COP404L CPU Interface

Typical Applications (Continued)

Sample Subroutine Program for *Figure 14*, LMC835-COP404L CPU Interface

```
HEX
CODE      LABEL       MNEMONICS                    COMMENTS
3F        LMC835:     LBI       3F      ;POINT TO RAMADDRESS 3F
05        SEND        LD                ;RAMDATA TO A
22                    SC                ; SET CARRY
335F                  OGI               ;SET PORT G= 1111, OPEN THE AND GATES
4F                    XAS               ;SWAP A AND SIO, CLOCK START
05                    LD                ;RAMDATA TO A, MAKE SURE A = DATA
07                    XDS               ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
05                    LD                ;RAMDATA TO A
4F                    XAS               ;SWAP A AND SIO
05                    LD                ;RAMDATA TO A, MAKE SURE A=NEWDATA
07                    XDS               ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
32                    RC                ;RESET CARRY
4F                    XAS               ;SWAP A AND SIO, CLOCK STOP
335D                  OGJ       13      ;SET PORT G=1101, MAKE STROBE LOW
335B                  OGI       11      ;SET PORT G=1011, MAKE STROBE HIGH, CLOSE THE
                                                                      GATES
4E                    CBA               ;BD TO A
43                    AISC      3       ;RAMADDRESS<3C THEN RETURN
48                    RET
80                    JP        SEND
```

```
    RAM
ADDRESS          COMMENTS
3C      DATA     ;GAIN DATA D4-D7
3D      DATA     ;GAIN DATA D0-D3
3E      DATA     ;BAND DATA D4-D7
3F      DATA     ;BAND DATA D0-D3
```

Application Hints

SWITCHING NOISE

The LMC835 uses CMOS analog switches that have small leakages (less than 50 nA). When a band is selected for flat gain, all the switches in that band are open and the resonator circuit is not connected to the LMC835 resistor network. It is only in the flat mode that the small leakage currents can cause problems. The input to the resonator circuit is usually a capacitor and the leakage currents will slowly charge up this capacitor to a large voltage if there is no resistive path to limit it. When the band is set to any value other than flat, the charge on the capacitor will be discharged by the resistor network and there will be a transient at the output. To limit the size of this transient, R_{LEAK} is necessary.

HOW TO AVOID SWITCHING NOISE DUE TO LEAKAGE CURRENT (Refer to *Figures 7* and *8*)

To avoid switching noise due to leakage currents when changing the gain, it is recommended to put R_{LEAK} = 100 kΩ between Pin 3 and Pin 5—11 each, Pin 26 and Pin 12—24 each. The resistor limits the voltage that the capacitor can charge to, with minimal effects on the equalization. The frequency response change due to R_{LEAK} are shown in *Figure 15*. The gain error is only 0.2 dB and Q error is only 5% at 12 dB boost or cut.

SIMPLE WORD GENERATOR *(Figure 6)*

Circuit operation revolves around an MM74HC165 parallel-in/serial-out shift register. Data bits D0 through D7 are applied to the parallel of the MM74HC165 from 8 toggle switches. The bits are shifted out to the DATA input of the LMC835 in sync with the clock. When all data bits have been loaded, CLOCK is inhibited and a STROBE pulse is generated: this sequence is initiated by a START pulse.

LMC835-COP404L CPU INTERFACE (Refer to *Figure 14*)

The diagram shows AND gates between the COP and the LMC835. These permit G2 to inhibit the CLOCK and DATA lines (SK and SO) during a STROBE (G1) pulse. This function may also be implemented in software. As shown in *Figure 2*, the data groups are shifted in D0 first. Data is loaded on positive clock edges.

POWER SUPPLIES

These applications show LM317/337 regulators for the ±7.5V supplies for the LMC835. Since the latter draws only 5 μA max., 1k series dropping resistors from the ±15V op amp supply and a pair of 7.5V zeners and bypass caps may also suffice.

Application Hints (Continued)

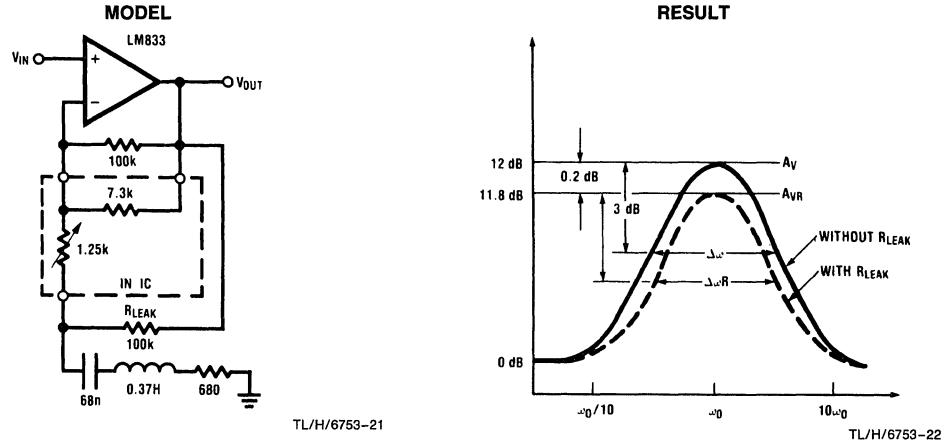


FIGURE 15. Effect of R_{LEAK}

REDUCING EXTERNAL COMPONENTS

The typical application shown in *Figure 7* is switching noise free. The DC-coupled circuit in *Figure 16* is also switching noise free, except at 12 dB/6 dB switch turn ON/OFF. This switching noise is caused by the I_{bias} and V_{offset} of the op amps. Selecting a low I_{bias} and V_{offset} op amp can minimize the switching noise due to the 12 dB/6 dB switch. The DC-coupled application can also eliminate the R_F = 100k resistors with only a 0.5 dB gain error at 12 dB boost or cut.

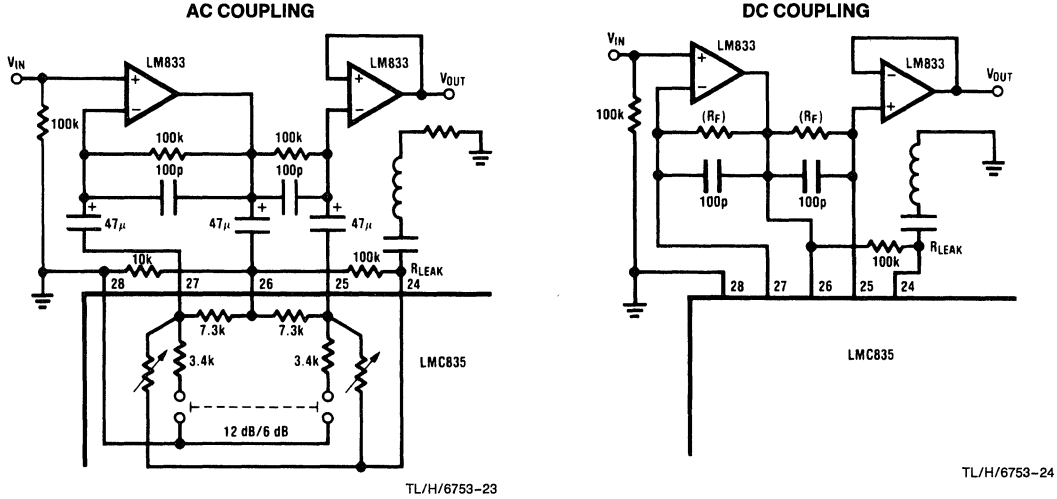


FIGURE 16. Reducing External Components

National Semiconductor Corporation

ADVANCED INFORMATION

LMC1992/LMC1993 Computer Controlled Tone and Volume Circuits

General Description

The LMC1992/3 is a tone (bass/treble), volume and fader (front/rear) circuit for stereo hi fi audio. Control is accomplished by means of a three wire microprocessor interface. Its applications include car radio, TV and remote audio systems.

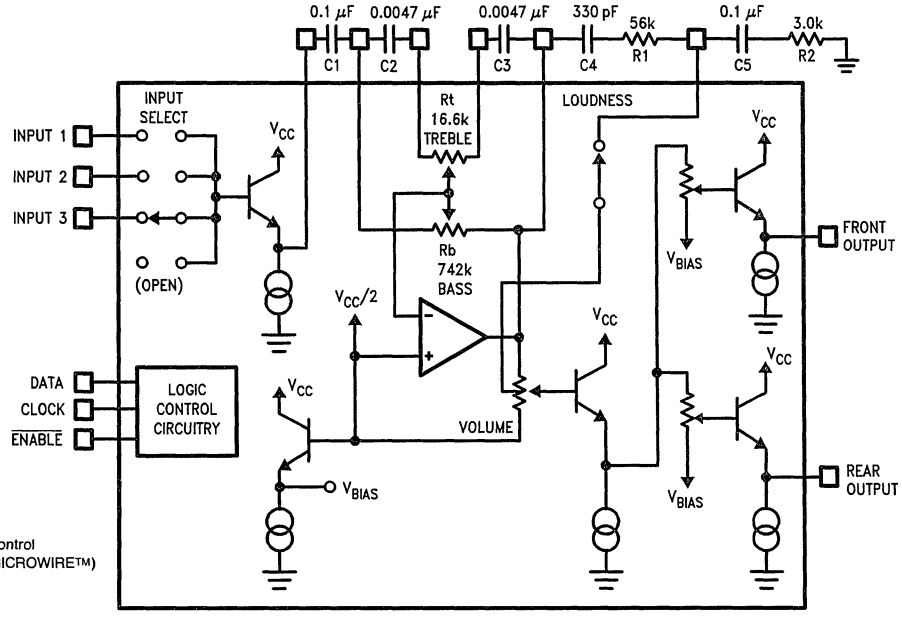
The LMC1992/3 provides stereo source selection switching, volume, fade and tone controls with very few external components. On-chip op amps enable these functions to be accomplished in a 28-pin package with minimal external components. In addition, the LMC1993 provides a loudness function with one less input source per channel.

The LMC1992/3 was designed with most capacitors less than 0.1 μF to allow use of chip capacitors. The signal path is comprised of analog switches and thin-film silicon-chromium resistor networks for very low noise and distortion. Additional tone control can be included by use of LMC843/835 digitally-controlled stereo 3/7-band graphic equalizer circuits.

Features

- 28-pin package
- Low noise and distortion
- Serial programmable: standard MICROWIRE™ interface
- Protection address (similar to DS 8906)
- TTL, CMOS logic compatible
- Inputs DC coupled
- Full boost and cut treble and bass tone control
- 40 Volume levels including mute
- Front/back fade control
- 20 Fader levels
- All attenuators 2 dB/step
- Single supply operation
- Wide supply voltage range
- Minimal external components
- Provisions for connection to DNR® and/or equalizer
- LMC1992 has 4 stereo source selection without loudness, LMC1993 has 3 with loudness
- Provisions for more stereo inputs
- Powers up with flat tone and min volume/fader

Equivalent Schematic (one channel shown) [LMC1993-loudness device]



TL/H/9048–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage $+V_S$ Referred to $-V_S$ Ground	$+18V$
Maximum Operational Supply Voltage	$+15V$
Logical Input Voltage	$+V_S$, $-V_S$
Operating Temperature Range LMC1992, LMC1993	$T_{MIN} < T_A < T_{MAX}$ $-40°C$ to $+85°C$
Storage Temperature Range	$-60°C$ to $+150°C$
Maximum Junction Temperature	125°C
Lead Temperature (Soldering, 10 sec.)	300°C

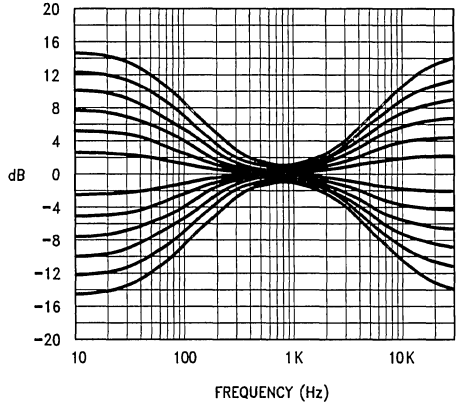
ESD rating is to be determined.

Electrical Characteristics $V^+ = 8V$, $T_A = +25°C$ unless otherwise noted

Parameter	Conditions Volume = 0 dB, Faders = 0 dB unless specified	LMC1992			Units
		Typ	Tested Limit	Design Limit	
Supply Current		15			mA
Reference Voltage	Pin 27	4.7			Vdc
Maximum Input Signal	Clipping Level (1% THD)	2.3			Vrms
Maximum Output Signal	Clipping Level (1% THD)	1.0			Vrms
THD 1 kHz	0.3 Vrms Input Volume = 0 dB	0.2			%
THD 1 kHz	0.3 Vrms Input Volume = −20 dB	0.03			%
Max Noise	CCIR, Flat Tone, Volume = 0 dB	7.0			μVrms
Min Noise	CCIR, Flat Tone, Volume = −80 dB	4.5			μVrms
Bass Range	Boost and Cut @ 50 Hz	12			±dB
Treble Range	Boost and Cut @ 15 kHz	12			±dB
Volume Range	Maximum Attenuation	80			dB
Fader Range	Maximum Attenuation	40			dB
Tracking	Attenuator Tracking	0.5			dB
Freq Response	High Frequency − 1 dB point	450			kHz
Separation	Channel Separation 1 kHz	80			dB
Isolation	Input-Input Isolation	90			dB
PSRR	100 Hz, 200 mVrms	40			dB
F_{clk}	Maximum Clock Frequency	1.0		0.50	MHz

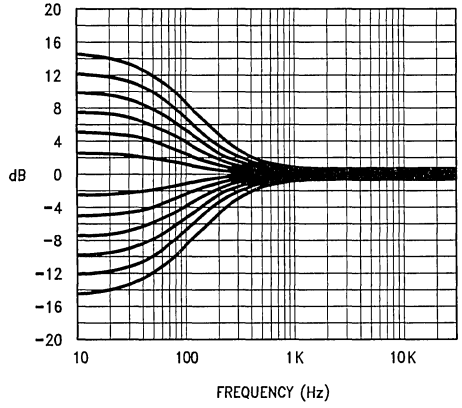
Typical Performance Characteristics

Bass Max Treble Max / Bass Min Treble Min



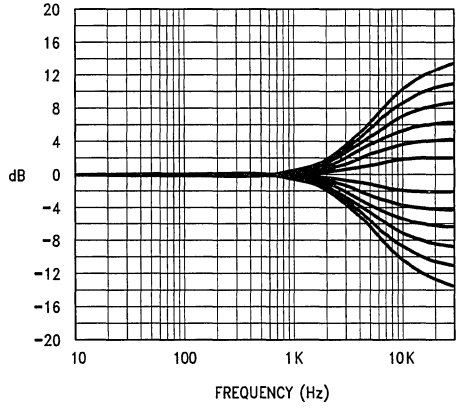
TL/H/9048–2

Bass Max Treble Flat / Bass Min Treble Flat



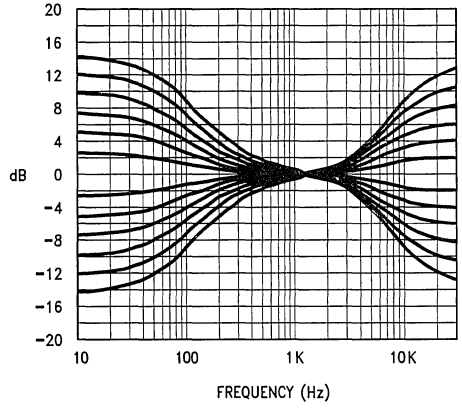
TL/H/9048–3

Bass Flat Treble Max / Bass Flat Treble Min



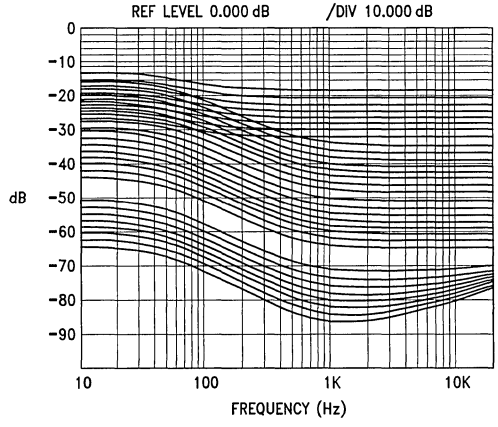
TL/H/9048–4

Bass Min Treble Max / Bass Max Treble Min



TL/H/9048–5

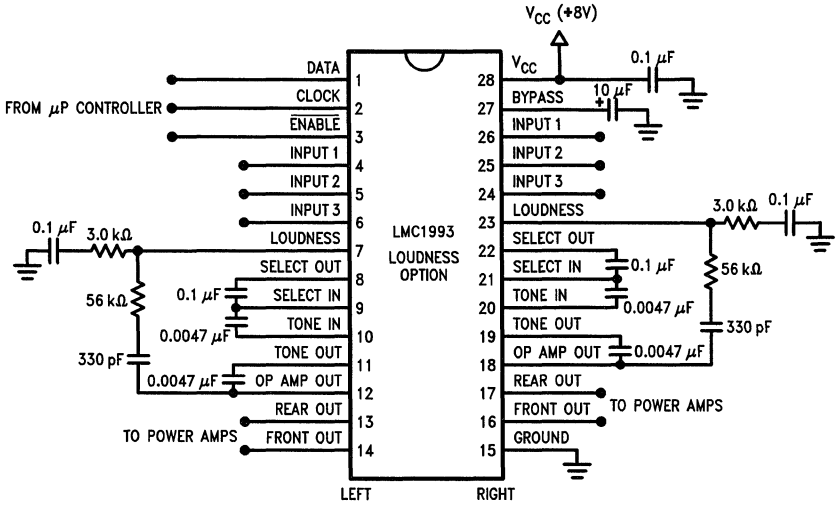
Loudness Contours LMC1993 Only



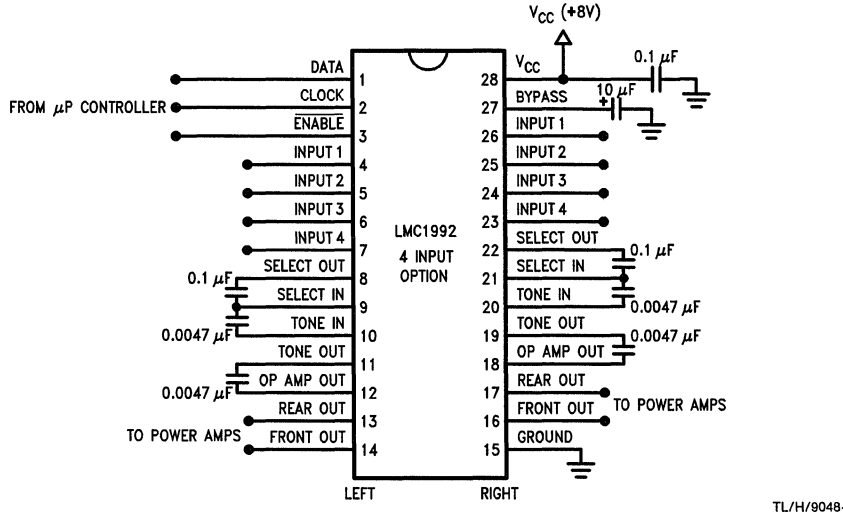
TL/H/9048–6

Note: Above graphs are tentative and thus subject to change.

Typical Applications



TL/H/9048–7



TL/H/9048–8

FIGURE 7. Connection Diagrams Options with Minimal External Components
Order Number LMC1993 (loudness device), LMC1992 (4 input device)
See NS Package Number N28B

General Information

The LMC1992/3 is a CMOS/bipolar high quality building block intended for high fidelity audio signal processing. While the LMC1992/3 is manufactured with CMOS processing, unique NPN transistors exist which are used to build low noise op amps. The combination of CMOS switches, bipolar op amps and sichrome resistors make it possible to achieve an order of magnitude quality improvement over standard bipolar circuits.

The LMC1992/3 has internal logic decoding which allows a computer (μP) to communicate directly to the audio control circuitry through a standard MICROWIRE interface. This 3 wire interface consists of DATA input line, a CLOCK input line, and an $\overline{\text{ENABLE}}$ line. When the $\overline{\text{ENABLE}}$ line is low, data can be shifted (serially) from the controller into the audio control circuit. As the $\overline{\text{ENABLE}}$ line goes through the low to high transition, data entry is disabled and data present in the internal shift register is latched and the instruction is executed.

From the controller 11 bit serial data stream, the first two bits address the device (LMC1992/3) permitting other devices (ie: PLL, equalizer) to share the same 3 wire bus. Of the remaining 9 bits, the next 3 bits are used for the function select (ie: volume, fader . . .). The remaining 6 bits are data for the function being addressed.

Serial Data Entry into the LMC1992/3

Serial information entry into the LMC1992/3 is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One bit is accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low preceding the negative transition of the $\overline{\text{ENABLE}}$ input.

The first two bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as an address. If these bits are **not** 1,0 no further information will be accepted from the DATA input, while the data latches will remain unchanged when the $\overline{\text{ENABLE}}$ line returns high.

If the first two bits are 1,0 then all succeeding bits are accepted as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Application Hints—Digital

In addition, a 12 bit data stream can be used if needed. The first two bits and last nine bits remain the same while any number of don't care bits can be inserted preceding the MSB of the three bit function select. Since these don't care bits are just shifted out internally, any number can be inserted to allow ease of programming. Thus the data stream word length becomes simply 11 + (number of extra bits).

When the $\overline{\text{ENABLE}}$ input returns high, any further serial data input is inhibited. Upon this positive transition of the $\overline{\text{ENABLE}}$, the data in the internal shift register is transferred into the data latches. Note that until this time, the states of the internal data latches have remained unchanged.

SERIAL DATA FORMAT

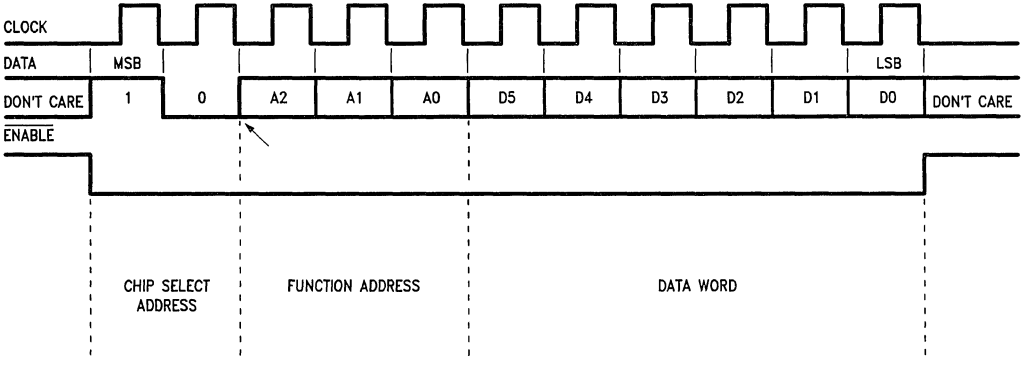
The serial data format, bit assignment and sequence is shown in Table I. Not shown in Table I are the protection address bits (1, 0) which as discussed earlier must precede the nine bit data word.

Note that not all the allotted data bits are used for all functions excluding volume. The extra bits are denoted with an "X" for don't care. Even though these extra bits have no effect on their respective controls, they still must be clocked into the LMC1992/3 for proper operation. Otherwise erroneous results will occur.

DATA COMMUNICATION

The following routines apply to operation of the LMC1992/3 with COPS™ microcontrollers. The routines arbitrarily select register 0 as the I/O register. It is assumed that chip select is high, SK (clock) is low, and SO (data) is low on entry to the routines. The routines exit with chip select high, SK low and SO low. Output port G0 is arbitrarily chosen as the chip select for the external device.

The 11 data bits intended to control the LMC1992/3 are assumed to be in the 4 bit registers 13–15 with the 4 MSB bits in register 13. This provides an extra bit (which works fine also) resulting in a data stream 12 bits long.



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Note 1: Negative transition on $\overline{\text{ENABLE}}$ clears previous address. Clock must be low during transition.

Note 2: Additional don't care states may be inserted here for ease of programming. (Optional.)

Note 3: Positive transition on $\overline{\text{ENABLE}}$ latches in new data if the LMC1992/3 has been addressed. Clock can either be high or low during transition.

FIGURE 8. Clocking Data into the Standard MICROWIRE Interface (Minimum Number of Bits in Data Stream)

Applications Hints-Digital (Continued)

DESTRUCTIVE DATA OUTPUT

This routine outputs the data under the conditions specified above. The output data is destroyed after it is transmitted. Note that this is a general purpose routine and handles all the overhead except loading the data into the registers. The routine takes a total of 17 ROM words and can be undoubtedly be reduced in specific applications.

```
OUT1:   LBI    0,13     ;point to start of data word
        SC              ;set C to enable SK clock
        OGI    14       ;select external device G0=0
        LEI    8        ;enable shift register output
SEND:   LD
        XAS             ;data transmission loop
        XIS             ;turn on clock
        JP     SEND
        RC
        XAS    15       ;deselect external device
        LEI    0        ;set S0 to 0
        RET
```

NON DESTRUCTIVE DATA OUTPUT

This routine is identical to the destructive data routine except that the transmitted data is preserved in the microcontroller. The nondestructive routine takes 21 ROM words. Four more than the destructive routine. Again this is a general purpose routine which can probably be reduced in specific applications.

```
OUT2:   LBI    0,13     ;point to start of data word
        SC
        OGI    14       ;select external device G0=0
        LEI    8        ;enable shift register output
        JP     SEND2
SEND1:XAS
SEND2:  LD              ;data output loop
        XIS
        JP     SEND 1
        XAS             ;send last data
        RC              ;wait 4 cycles-data going out
        CLRA
        NOP
        XAS             ;turn SK clock off
        OGI    15       ;deselect device
        LEI    0        ;set S0 to 0
        RET
```

Note: These routines are tentative and subject to change.

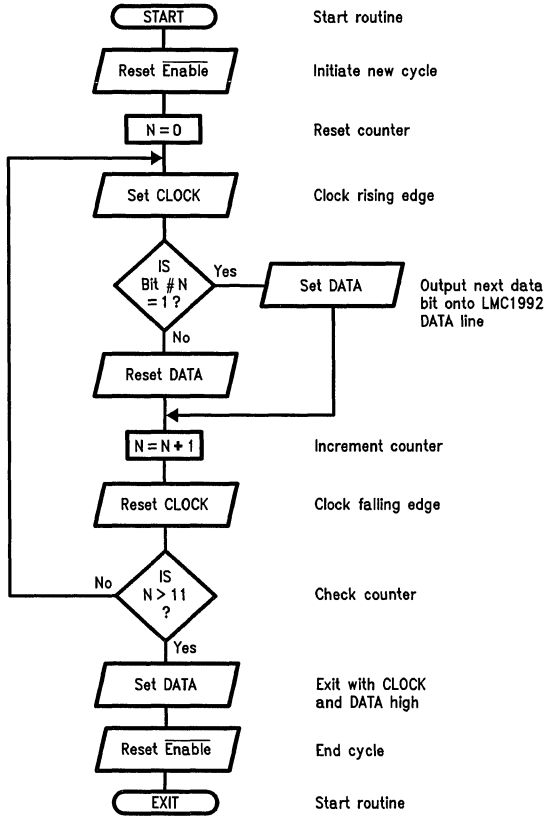

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FIGURE 9. General Flowchart for Controlling LMC1992/3 MICROWIRE Serial Inputs

Application Hints-Digital (Continued)

TABLE I. Programming Codes for LMC1992/3

Address			Function	Data						Values
A2	A1	A0		D5	D4	D3	D2	D1	D0	
1	1	1	Left Rear Fader	X	M	N	N	N	L	−40 dB = X00000 −20 dB = X01010 0 dB = X101XX
1	1	0	Right Rear Fader	X	M	N	N	N	L	−40 dB = X00000 −20 dB = X01010 0 dB = X101XX
1	0	1	Left Front Fader	X	M	N	N	N	L	−40 dB = X00000 − 20 dB = X01010 0 dB = X101XX
1	0	0	Right Front Fader	X	M	N	N	N	L	−40 dB = X00000 −20 dB = X01010 0 dB = X101XX
0	1	1	Volume	M	N	N	N	N	L	−80 dB = 000000 −40 dB = 010100 0 dB = 101XXX
0	1	0	Treble	X	X	M	N	N	L	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	1	Bass	X	X	M	N	N	L	−12 dB = XX0000 FLAT = XX0110 +12 dB = XX1100
0	0	0	Input Select & LOUDNESS	X	X	I	M	N	L	OPEN = XXI000 INPUT1 = XXI001 INPUT2 = XXI010 INPUT3 = XXI011 INPUT4 = XXI100 *(see note) LOUDNESS ON: I = 1 *(see note) LOUDNESS OFF: I = 0

***Note 1:** With LMC1993 loudness device, INPUT 4 is not available.

***Note 2:** With LMC1992 4 input device, D3 of input select must be low (0), and INPUT 4 is available.

Note 3: M & L represent most and least significant data bits.

Note 4: All attenuators 2 dB/step.

Note 5: Tone controls 2 dB/step @ 50 Hz and 15 kHz.

Application Hints—Analog

INPUT CHANNEL SELECTION

When operating from a single positive power supply, the LMC1992/3 signal inputs require a DC bias voltage for proper operation of the internal voltage followers and buffers. This usually means that the signal sources, if operated off the same single supply, can be directly coupled to the LMC1992/3 without a coupling capacitor. For example, on an 8 Vdc power supply, all signal inputs to the LMC1992/3 (pins 4–6, 24–26) should have a DC component of approximately 4 Vdc. Maximum signal levels of 2 Vrms (5.6V peak-to-peak) would then swing from 1.2V to 6.8V.

For signal sources lacking in this requirement, such as those derived from external input jacks to the system, the bias voltage needs to be provided. A simple voltage divider with filter for supply rejection as shown in *Figure 10* will suffice.

When the LMC1993 is used, input 4 is not available. That pin becomes the loudness input. Selecting input 4 when using the LMC1993, or turning on the loudness function when the LMC1992 is used can cause undesirable results, thus is not suggested.

For best results, a separate bias circuit for each channel or even one for each signal source lacking a DC component should be used to prevent crosstalk between channels and inputs. Though stereo sources can have bias circuits in common for left and right signal and still maintain reasonable separation.

Depending upon the particular input source that is selected, one of the three stereo inputs will be available at the select output pins 8 and 22 (left and right channels respectively). The DC bias voltage at those pins will be one base-emitter voltage (approximately 0.7 Vdc) below the source due to the internal emitter follower (see *Figure 1*). Thus, if the selected input has a bias of 4.0 Vdc the DC component at pins 8 and 22 will be about 3.3 Vdc.

The use of an emitter follower for input selection allows connection of additional sources to the system. For example, many radio IC's also have emitter follower outputs that allow the user to wire-or multiple outputs together and control their selection by input or supply switching. The signal output pin 8 and 22 of the LMC1992/3 are constructed similarly and may be treated in the same manner, consistent with the same requirements. If another emitter follower output is driving these nodes, the LMC1992/3 input select should be switched to either "XXX000" or "XXX11X" open input codes (see Table I).

The select output pins 8 and 22 may be directly coupled via a capacitor to the select input (pins 9 and 21) as shown in *Figure 1* or connected to external noise reduction and/or equalizer circuits as shown in *Figure 11.* Should both be utilized, it is important that noise reduction (ie: DNR® using the LM1894) be performed before equalization. Otherwise, the equalization control settings could adversely affect or even prevent the noise reduction systems from operating.

The input select switch can also be used as a mute function with volume at −80 dB, the input select can be set to "XXX000" open input to further mute the outputs to provide greater than −100 dB attenuation if desired.

TONE RESPONSE

The tone function (bass and treble) is controlled by capacitors C1 and C2 (see *Figure 1*). The exact amount of boost and cut obtained is determined by the data word as given in Table I.

The typical tone response obtained in the standard application circuit (C2 = C3 = 0.0047 μF) is shown in *Figures 2–5* for each step of boost and cut. When modifying these curves it is important to note that it is ratio of C3 to C2 that determines the mid frequency gain. For example, with C3 = 2(C3) the tone response at "flat" setting would be approximately 0 dB at 20 Hz and 20 kHz while +6 dB at 1 kHz. Thus C2 should equal C3 for a symmetric tone response.

The effect of altering the recommended values of the tone shaping capacitors C2 and C3 is to shift the tone response curve up or down in frequency. By increasing the capacitance of C2 and C3, the frequencies at which 2 dB/step is achieved will decrease from 50 Hz to 35 Hz and from 15 kHz to 10 kHz with a 0.0068 μF capacitor. Likewise with a decrease in capacitance of C2 and C3 the 2 dB/step frequencies will increase from 50 Hz to 70 Hz and from 15 kHz to 20 kHz with a 0.0033 μF capacitor.

From *Figure 1* the turnover frequencies are approximately F_{hb} = 1/sC2(13.8K) and F_{lb} = 1/sC1(116.4K) for treble and bass respectively at maximum boost. While the inflection frequencies (at which maximum boost and cut are within 3 dB of their final values) are F_h = 1/sC2(2.6K) and F_l = 1/sC1(625.6K) for treble and bass respectively at maximum boost.

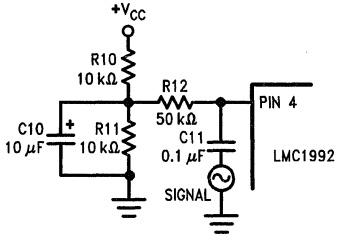

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FIGURE 10. DC Bias Input Circuit

LOUDNESS FUNCTION—LMC1993 ONLY

The loudness compensation as shown in *Figure 1* is controlled by components R1, R2, C4, C5. If selected it will introduce bass and slight treble boost (in addition to any tone shaping requested) that is dependent upon the setting of the volume control. The exact nature of the transfer function at −34 dB is given by:

$$\frac{V_o}{V_i} = \frac{1}{4.67} \frac{(s*C5*R2+1)*(s*C4*(R1+112K)+1)}{(s*C4*R1+1)*(s*C5*(R5+41.34K)+1)}$$

If only bass boost is required the external components R1 and C4 can be deleted, minimizing the external component count.

If this device is selected only three inputs will be available to input select (input 1–input 3). For systems where loudness compensation is not required the user may choose the LMC1992 or simply eliminate the components associated with the loudness pin and being careful when programming to always keep the loudness function off (see Table I).

The data bit used to enable or disable the loudness function is embedded in the input data select data word as D3. Thus care must be taken to send a complete data word (loudness on/off and input select data) in order to prevent erroneous operation.

FADER FUNCTION

Since all four fader outputs LR, LF, RR, RF are all independently adjustable, a balance control would be redundant. The balance function is accomplished via software by simultaneously changing both front and rear faders on the same channel by the desired amount of balance. Since 40 dB of attenuation is available this should satisfy most any balance requirements.

SYSTEM CONNECTION

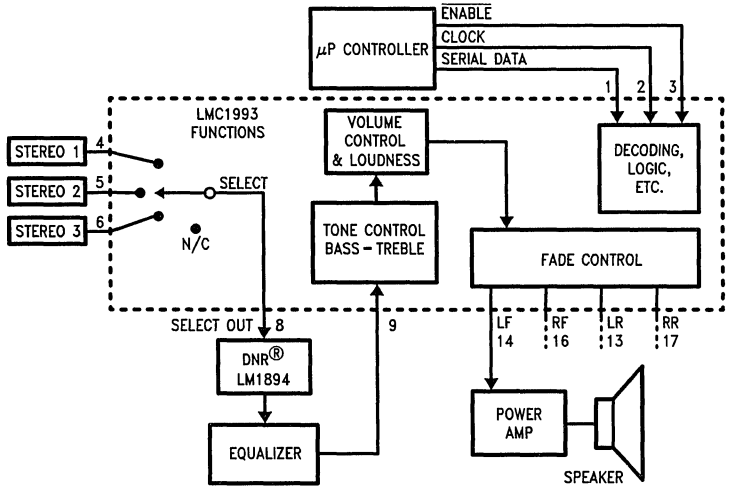

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FIGURE 11. System Block Diagram Showing Inclusion of DNR® Noise Reduction and Equalizer (LMC843, LMC835) (One Channel Only—LMC1993).

Section 2

Radio Circuits

Section 2 Contents

***Devices Not Covered In Last Publication**

National Semiconductor Corporation

Radio Circuits Definition of Terms

AGC dc Output Shift: The shift of the quiescent IC output voltage of the AGC section for a given change in AGC central voltage.

AGC Figure of Merit: The widest possible range of input signal level required to make the output signal drop by a specified amount from the specified maximum output level. Typical F.O.M. numbers are from 40 dB to 50 dB, for domestic radios and about 60 dB for automotive radios (for −10 dB output level change).

AGC Input Current: The current required to bias the central voltage input of the AGC section.

AM Rejection Ratio: The ratio of the recovered audio output produced by a desired FM signal of specified level and deviation to the recovered audio output produced by an unwanted AM signal of specified amplitude and modulating index.

Channel Separation: The level of output signal of an undriven amplifier with respect to the output level of an adjacent driven amplifier.

Detection Bandwidth: That frequency range about the free running frequency of the tone decoder/phase locked loop where a signal above a specified level will cause a detected signal condition at the output.

Detection Bandwidth Skew: The measure of how well the detection bandwidth is centered about the free running frequency. It is equal to the maximum detection bandwidth frequency plus the minimum detection bandwidth frequency minus twice the free running frequency.

Hold In Range: That range of frequencies about the free running frequency for which the phase locked loop will stay in lock if initially starting out in lock.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Input Sensitivity: The minimum level of input signal at a specified frequency required to produce a specified signal-to-noise ratio at the recovered audio output.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

−3 dB Limiting Sensitivity: In FM the input signal level which causes the recovered audio output level to drop 3 dB from the output level with a specified large signal input.

Lock In Range: That range of frequencies about the free running frequency for which the phase locked loop will come into lock if initially starting out of lock.

Maximum Sweep Rate: The maximum rate that the VCO may be made to vary its oscillating frequency over its Sweep Range.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Phase Detector Sensitivity: The change in the output voltage of the phase detector for a given change in phase between the two input signals to the phase detector.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 6 dB below the rated output. For example, an amplifier rated a 60W with $\leq$0.25% THD, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Sweep Range: That ratio of maximum oscillating frequency to minimum operating frequency produced by varying the central voltage of the VCO from its maximum value to its minimum value with fixed values of timing resistance and capacitance.

VCO Sensitivity: The change in operating frequency for a given change in VCO central voltage.

National Semiconductor Corporation

Radio Circuits Selection Guide

AM RF/IF Detector

	Portable	Home	Auto	Synthesized	Pin Count (Dip Package)	Supply Voltage	Supply Current	Input Sensitivity for 20 dB S/N Ratio	AM and FM IF	Audio Power Amplifier	Internal Detector	Meter Output
LM1863	•	•	•	•	20*	7-16	8.3 mA	30 μV			•	•
LM1866	•	•			20	3-15	15 mA	25 μV	•		•	•
LM1868	•	•			20	4.5-15	22 mA	12 μV	•	•	•	
LM3820	•	•	•		14	4.5-16	18 mA	35 μV				

*SO Surface Mount Package Only

Stereo Decoder

	Portable	Home	Auto	Pin Count Dip Package	Supply Voltage	Supply Current	THD	Separation	Blend	High Cut	Lamp Driver	Output Buffer	ARI Interference Rejection
LM1800		•		16	10-18	21 mA	0.4%	45 dB			•	•	
LM1870	•	•	•	20	7-15	26 mA	0.05%	45 dB	•	•	•	•	
LM1884*		•		16	8-16	35 mA	0.1%	—			•	•	
LM4500A	•	•	•	16	8-16	35 mA	0.1%	40 dB			•	•	•

*TV Stereo Decoder

Radio Remote Control

	Function	Pin Count (Dip Package)	Supply Voltage	Supply Current	Channels		Frequency Range
					Analog	Digital	
LM1871	Encoder/Transmitter	18	4.5-15V	14 mA	up to 6	2	up to 72 MHz
LM1872	Decoder/Receiver	18	2.5-7V	13 mA	2	2	up to 72 MHz

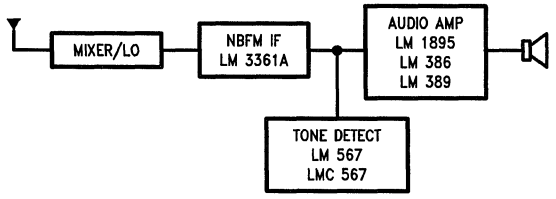
FM IF/Detector

	Portable	Home	Auto	Synthesized	Pin Count Dip	Pin Count S.O.	Supply Voltage	Supply Current	−3 dB Limiting Sensitivity	THD	Mute	AGC Outputs	AFC	Meter Output	AM/ FM IF
LM1865		•	•	•	20		7.3-16	43 mA	60 μV*	0.1%	•	Reverse	•	•	
LM1965		•	•		20		7.3-16	43 mA	60 μV*	0.1%	•	Reverse	•	•	
LM2065		•	•	•	20		7.3-16	43 mA	60 μV*	0.1%	•	Forward	•	•	
LM1866	•	•			20		3-15	17 mA	12 μV	0.5%	•	•	•	•	•
LM1868	•	•			20		4.5-15	19 mA	15 μV	1.1%					•
LM3089		•	•		16		8-16	23 mA	12 μV	0.5%	•	•	•	•	
LM3189		•	•		16		8-16	31 mA	12 μV	0.5%	•	•	•	•	
LM3361A†	•		•		16	16	2-9	2.8 mA	2 μV	-	•				

*Exclusive of 26 dB Buffer

†Narrow-Band FM-IF

Cordless Telephone Receiver



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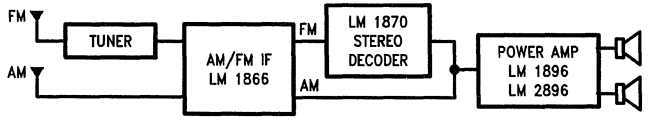
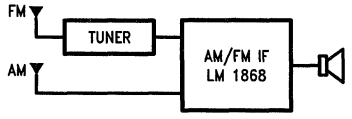
Portable Radio (Stereo)



TL/XX/0011–2

Portable Radio (Monaural)



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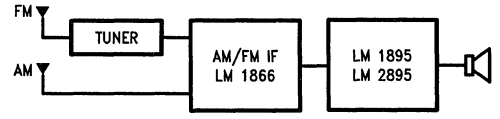
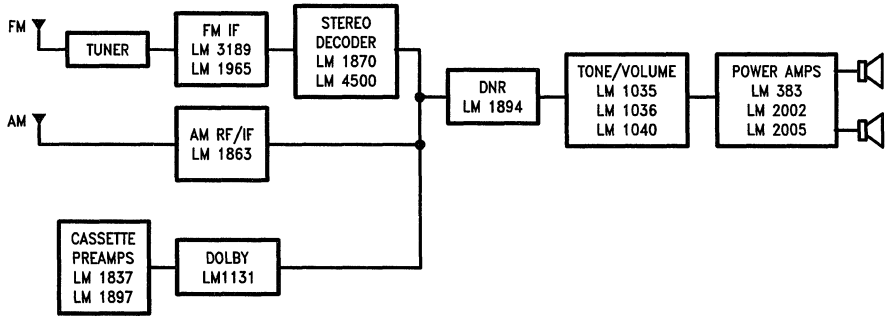
Table/Clock Radio



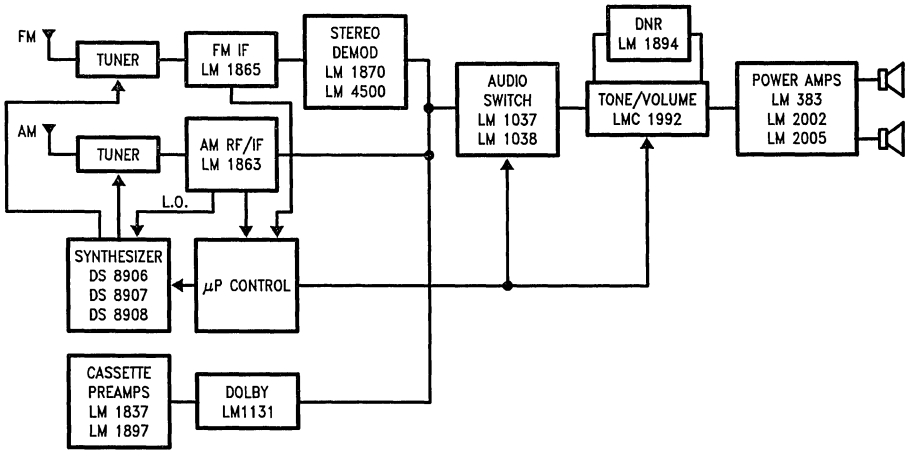
TL/XX/0011–4

Auto Radio (Manually Tuned)



TL/XX/0011–5

Automotive Radio (Electronically Tuned)



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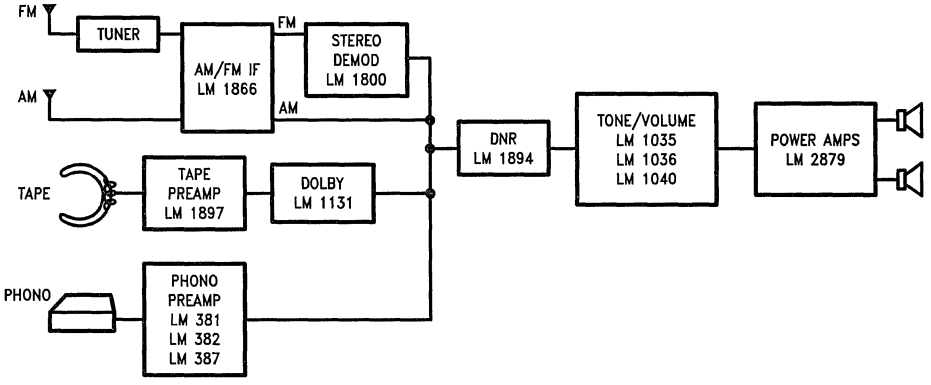
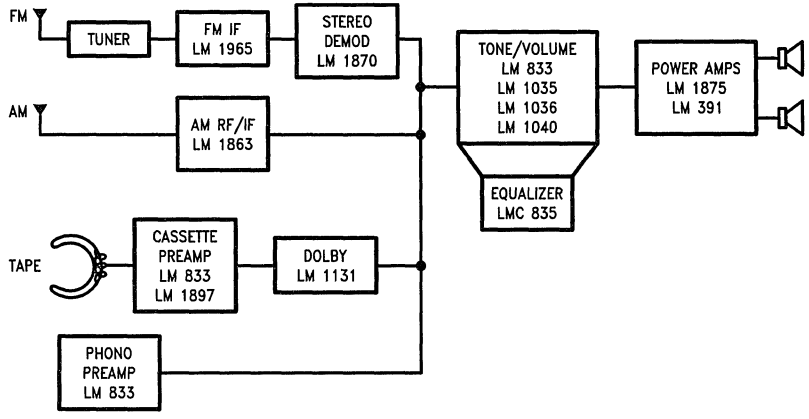
Home Stereo System (Audio Power < 10W)



TL/XX/0011–7

Home Component Stereo (Audio Power > 10W)



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National Semiconductor Corporation

LM1800 Phase-Locked Loop FM Stereo Demodulator

General Description

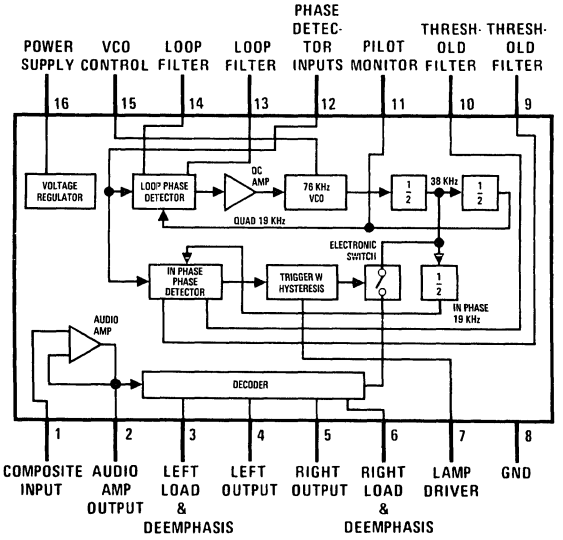
The LM1800 is a second generation integrated FM stereo demodulator using phase locked loop techniques to regenerate the 38 kHz subcarrier. The numerous features integrated on the die make possible a system delivering high fidelity sound while still meeting the cost requirements of inexpensive stereo receivers. More information available in AN-81.

Features

- Automatic stereo/monaural switching
- 45 dB power supply rejection
- No coils, all tuning performed with single potentiometer
- Wide operating supply voltage range
- Excellent channel separation
- Emitter follower output buffers

Connection Diagram

Order Number LM1800N
See NS Package Number N16A



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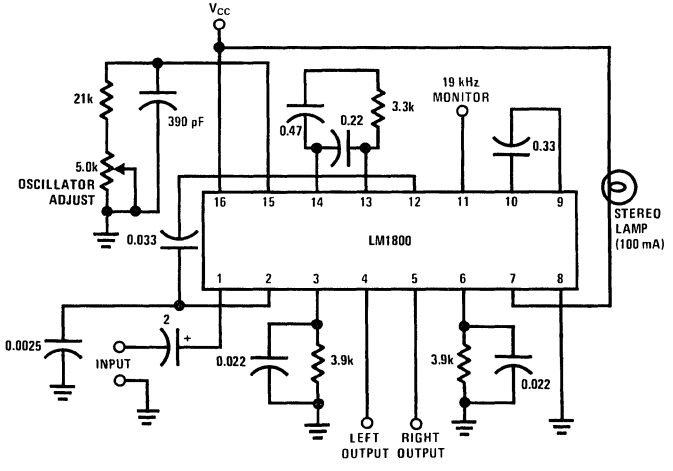
Top View

Typical Application



TL/H/7888–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	18V
Power Dissipation (Note 3)	1500 mW
Operating Temperature Range	0°C to +70°C
Operating Supply Voltage Range	+10V to +18V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	260°C

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
Supply Current	Lamp "Off"		21	30	mA
Lamp Driver Saturation	100 mA Lamp Current		1.3	1.8	V
Lamp Driver Leakage			1.0		nA
Pilot Level for Lamp "ON"	Pin 11 Adjusted to 19.00 kHz		15	20	mVrms
Pilot Level for Lamp "OFF"	Pin 11 Adjusted to 19.00 kHz	3.0	7.0		mVrms
Stereo Lamp Hysteresis		3.0	6.0		dB
Stereo Channel Separation	100 Hz (Note 2) 1000 Hz (Note 2) 10000 Hz (Note 2)	 30	40 45 45		dB dB dB
Monaural Channel Unbalance	200 mVrms, 1000 Hz Input		0.3	1.5	dB
Monaural Voltage Gain	200 mVrms, 400 Hz Input	140	200	260	mVrms
Total Harmonic Distortion	500 mVrms, 1000 Hz Input		0.4	1.0	%
Total Harmonic Distortion	500 mVrms, 1000 Hz Input, 1800A Only		0.1	0.3	%
Capture Range	25 mVrms of Pilot	±2.0		±6.0	% of f_o
Supply Ripple Rejection	200 mVrms of 200 Hz Ripple	35	45		dB
Dynamic Input Resistance		20	45		kΩ
Dynamic Output Resistance		900	1300	2000	Ω
SCA Rejection	(Note 4)		70		dB
Ultrasonic Freq. Rejection	Combined 19 and 38 kHz, Ref. to Output		33		dB

Note 1: T_A = 25°C and V^+ = 12V unless otherwise stated.

Note 2: The stereo input signal is made by summing 123 mVrms LEFT or RIGHT modulated signal with 25 mVrms of 19 kHz pilot tone, measuring all voltages with an average responding meter calibrated in rms. The resulting waveform is about 800 mVp-p.

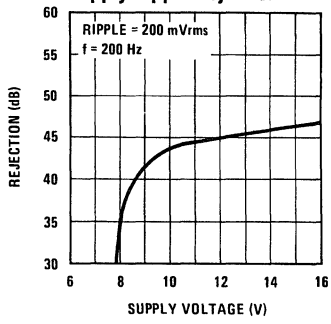
Note 3: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Note 4: Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.

Note 5: VCO "OFF" curve represents the distortion attainable using good 19 kHz and 38 kHz filters.

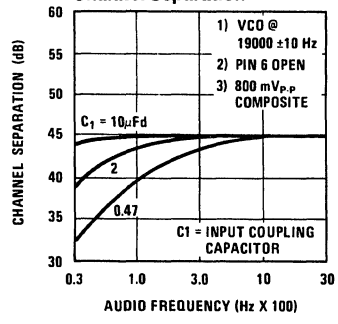
Typical Performance Characteristics

Supply Ripple Rejection



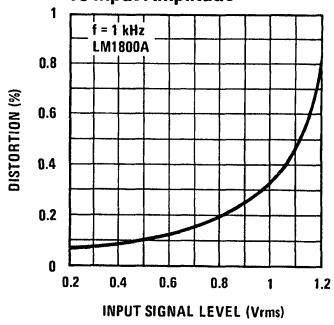
TL/H/7888–3

Channel Separation



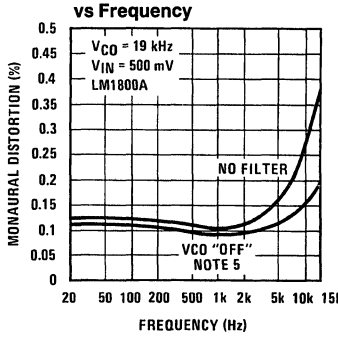
TL/H/7888–4

Monaural Distortion vs Input Amplitude



TL/H/7888–5

Monaural Distortion vs Frequency



TL/H/7888–6

National Semiconductor Corporation

LM1863 AM Radio System for Electronically Tuned Radios

General Description

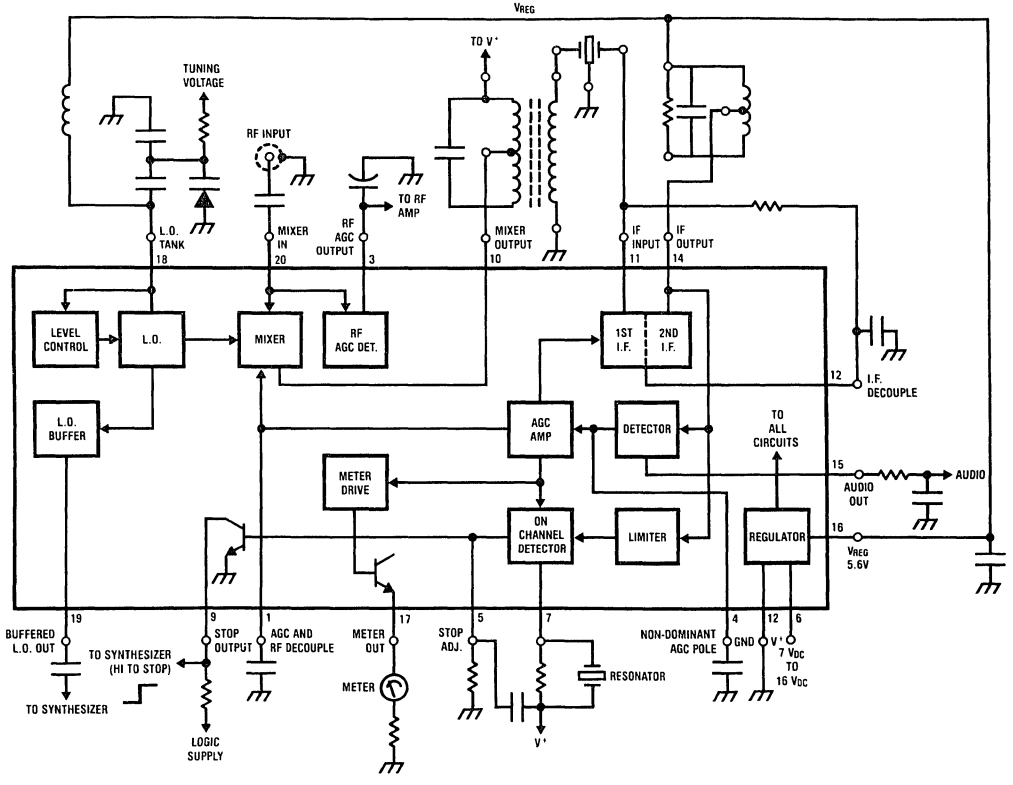
The LM1863 is a high performance AM radio system intended primarily for electronically tuned radios. Important to this application is an on-chip stop detector circuit which allows for a user adjustable signal level threshold and center frequency stop window. The IC uses a low phase noise, level-controlled local oscillator.

Low phase noise is important for AM stereo which detects phase noise as noise in the L-R channel. A buffered output for the local oscillator allows the IC to directly drive a phase locked loop synthesizer. The IC uses a RF AGC detector to gain reduce an external RF stage thereby preventing overload by strong signals. An improved noise floor and lower THD are achieved through gain reduction of the IF stage. Fast AGC settling time, which is important for accurate stop detection, and excellent THD performance are achieved with the use of a two pole AGC system. Low tweet radiation and sufficient gain are provided to allow the IC to also be used in conjunction with a loopstick antenna.

Features

- Low supply current
- Level-controlled, low phase noise local oscillator
- Buffered local oscillator output
- Stop circuitry with adjustable stop threshold and adjustable stop window
- Open collector stop output
- Excellent THD and stop time performance
- Large amount of recovered audio
- RF AGC with open collector output
- Meter output
- Compatible with AM stereo

Block Diagram



TL/H/5185–1

Order Number LM1863M
See NS Package Number M20B

Absolute Maximum Ratings

Supply Voltage	16V
Package Dissipation (Note 1)	1.7W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	0°C to +70°C
Soldering Information	
Small Outline Package	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Electrical Characteristics

(Test Circuit, T_A = 25°C, V+ = 12V, SW1 = Position 1, SW2 = Position 2, unless indicated otherwise)

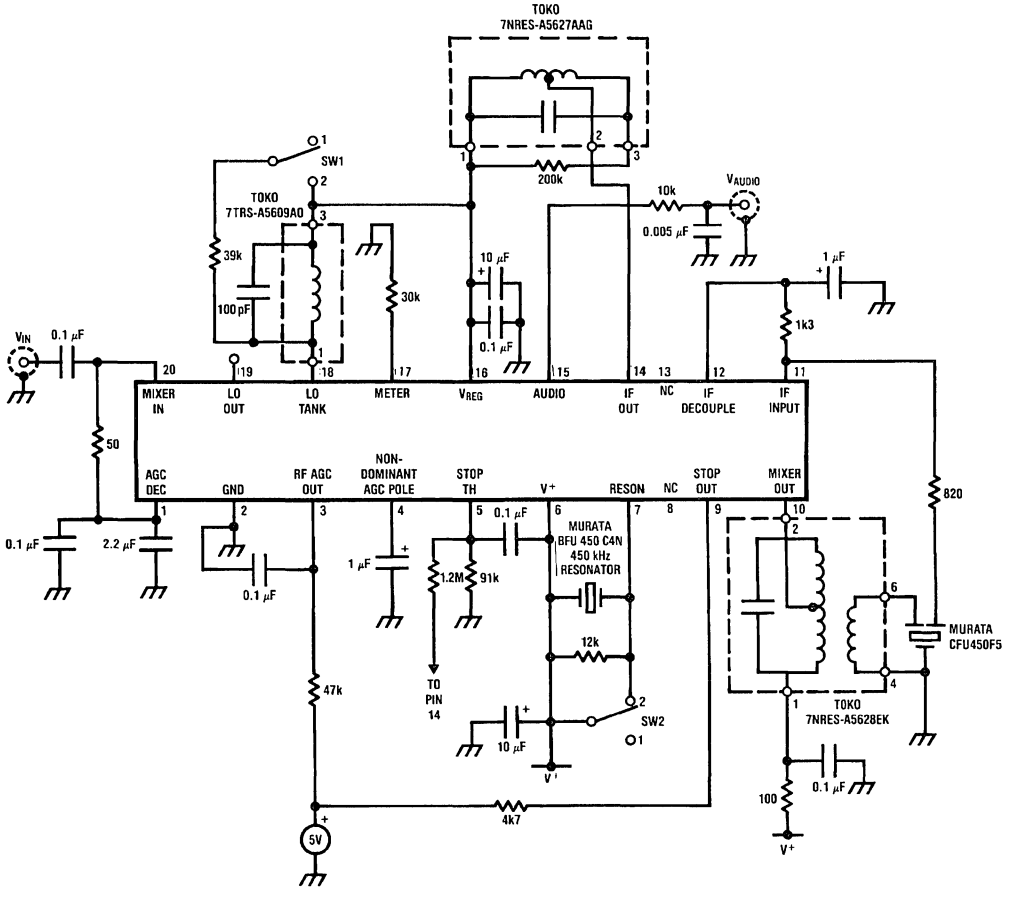
Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS					
Supply Current	V_{IN} = 0 mV		8.3	12.5	mA
Pin 16, Regulator Voltage			5.6		V
Operating Voltage Range	(See Note 2)	7		16	V
Pin 3 Leakage Current	V_{IN} = 0 mV		0.1		μA
Pin 9, Low Output Voltage	V_{IN} = 0 mV, SW2 = Position 1		.15		V
Pin 17, Output Voltage	V_{IN} = 0 mV		0		V
DYNAMIC CHARACTERISTICS: (f_{MOD} = 1 kHz, f_{IN} = 1 MHz, M = 0.3)					
Maximum Sensitivity	V_{IN} For V_{AUDIO} = 6 mVrms		7.5		μV
20 dB Quieting Sensitivity	V_{IN} for 20 dB S/N in Audio		15	30	μV
Maximum Signal to Noise Ratio	V_{IN} = 10 mV	40	54		dB
Total Harmonic Distortion	V_{IN} = 10 mV		.26		%
Total Harmonic Distortion	V_{IN} = 10 mV, M = 0.8		.63	2	%
Audio Output Level	V_{IN} = 10 mV	80	120	160	mVrms
Overload Distortion	V_{IN} = 50 mV, M = 0.8		7.5		%
Meter Output Voltage	V_{IN} = 100 μV		0.5		V
Meter Output Voltage	V_{IN} = 10 mV		4.6		V
Local Oscillator Output Level on Pin 19	(See Note 3), SW1 = Position 1	100	147		mVrms
Local Oscillator Output Level on Pin 19	(See Note 3), SW1 = Position 2		125		mVrms
Stop Detector Valid Station Frequency Window	V_{IN} = 10 mV, difference between the two frequencies at which Pin 9 < 1V, SW2 = Position 1	2.5	4	5.5	kHz
Stop Detector Valid Station Signal Level Threshold	Find V_{IN} for which Pin 9 > 1V, SW2 = Position 1	8	16	70	μVrms
RF AGC Threshold	Find V_{IN} that produces 10 μA of current into Pin 3	3	6	10	mVrms
Pin 3 Low Output Level	V_{IN} = 30 mV		0.1		V
Pin 9 Leakage Current	V_{IN} = 30 mV		0.1		μA
Pin 17 Output Resistance	V_{IN} = 10 mV		825		Ω

Note 1: Above T_A = 25°C derate based on $T_{j\,(MAX)}$ = 150°C and θ_{jA} = 85°C/W.

Note 2: All data sheet specifications are for V+ = 12V and may change slightly with supply.

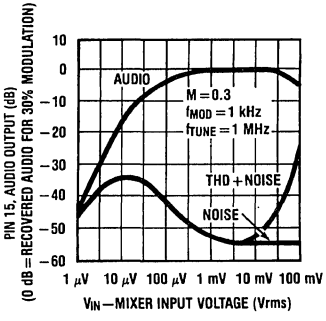
Note 3: The local oscillator level at Pin 19 is identical to the level at Pin 18 since Pin 19 is an emitter follower off of Pin 18.

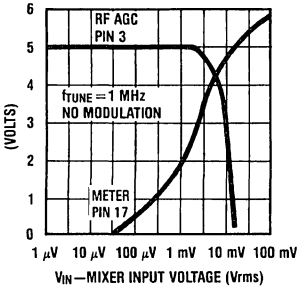
Test Circuit

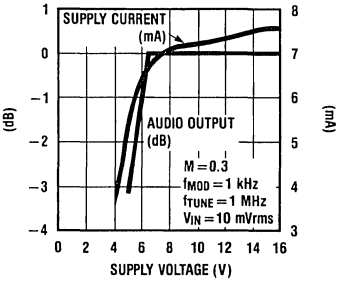


TL/H/5185–2

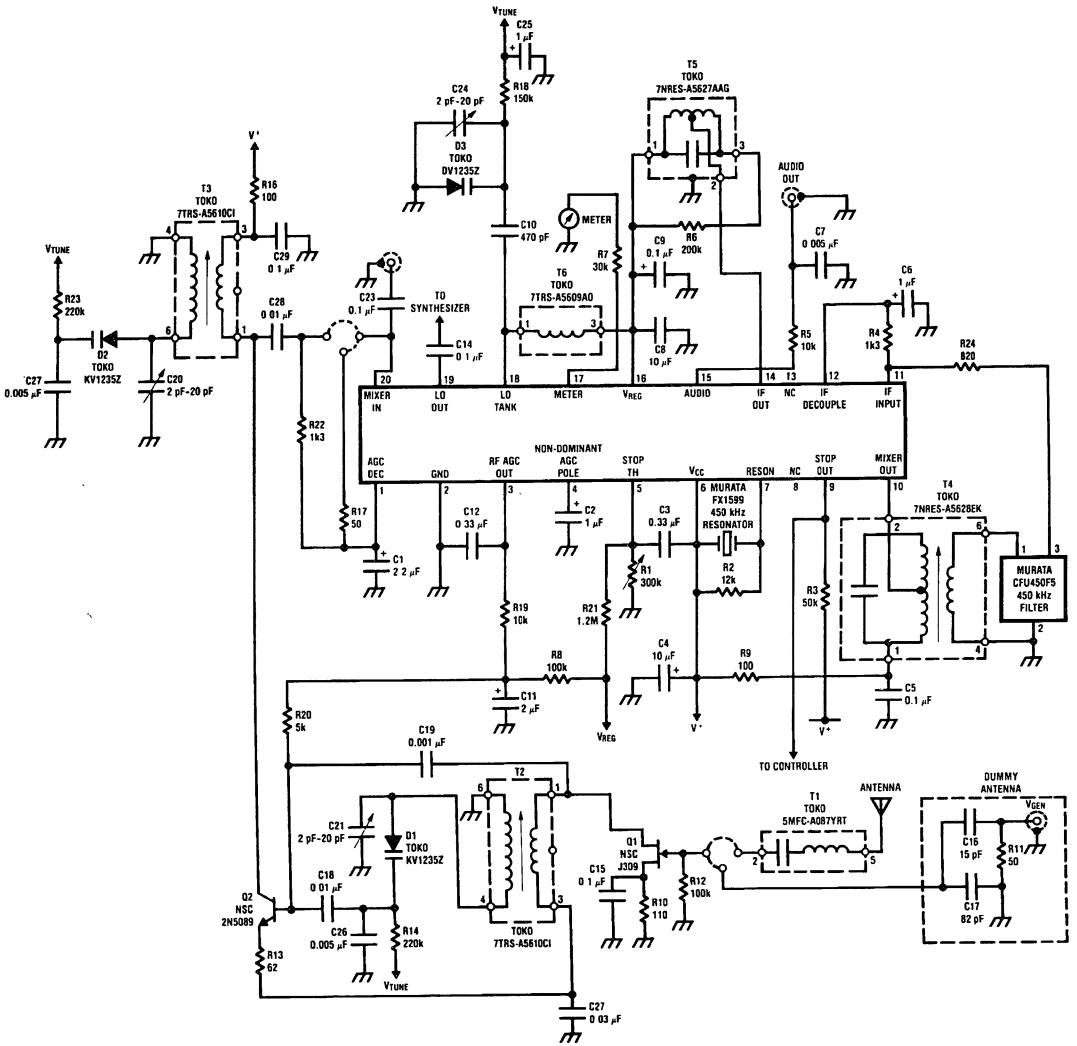
Typical Performance Characteristics (From Test Circuit)





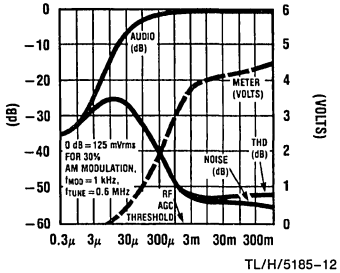


LM1863: AM ETR Radio

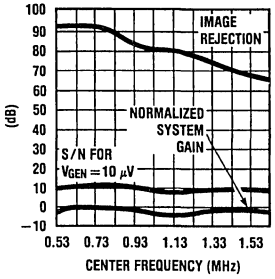


TL/H/5185–8

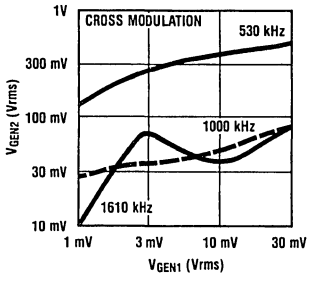
Performance Characteristics of Applications Circuit



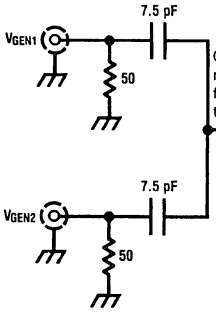
TL/H/5185–12



TL/H/5185–13



TL/H/5185–14



Cross modulation is measured using the following dummy antenna:

TL/H/5185–15

The following procedure was used to measure cross modulation:

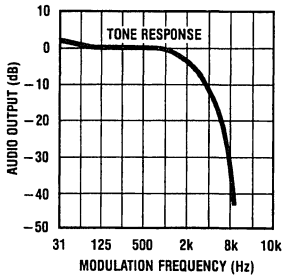
1. Tune the radio to the center frequency of interest and tune V_{GEN}, to this same frequency.

2. Set at 0 dB audio reference with V_{GEN}, = 10 mV RMS and 30% AM mod; f_{MOD} = 1 kHz.

3. Remove the modulation from V_{GEN1} and set the level of V_{GEN1}.

4. Set the modulation level of V_{GEN2} = 80% at f_{MOD} = 1 kHz and tune V_{GEN2} ± 40 kHz away from center frequency.

5. Increase the level of V_{GEN2} until −40 dB of audio is recovered. The level of V_{GEN2} is the cross modulation measurement.



TL/H/5185–16

Additional Performance Information:

* THD for 80% modulation for f_{MOD} = 1 kHZ at:
  V_{GEN} = 1V is 0.5%
  V_{GEN} = 10 mV is 0.4%
* Tweet <2% at all input levels.
* Typical time for valid stop indication < 50 ms.

Note: Tweet is an audio tone produced by the 2nd and 3rd harmonic of the IF beating against the received signal. It is measured as an equivalent modulation level: ie, 30% tweet has the same amplitude at the detector as a desired signal with 30% modulation.

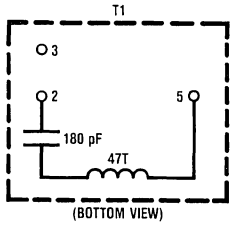
IC External Components (See Application Circuit)

Component	Typical Value	Comments
C1	2.2 μF	Sets dominant AGC pole, affects stop time and THD.
C2	1 μF	Sets non-dominant AGC pole, affects stop time and THD.
C3	0.33 μF	Stop level threshold decoupling, affects stop time and sensitivity of stop detector to large modulation peaks.
C4	10 μF	Supply decoupling, low frequency.
C5	0.1 μF	Supply decoupling, high frequency.
C6	1 μF	IF decouple, affects IF gain.
C7	0.005 μF	Audio output filter, removes IF ripple from detector.
C8	10 μF	Regulator decouple, low frequency.
C9	0.1 μF	Regulator decouple, high frequency.
C10	470 pF	Pad capacitor for varactor, affects tracking.
C11	2 μF	RF AGC decouple, affects stop time and THD.
C12	0.33 μF	RF AGC high frequency decouple.
C14	0.1 μF	Local oscillator output coupling.
C19	0.001 μF	Sets gain at high end of AM band.
C26	0.005 μF	Sets gain at low end of AM band.
C28	0.01 μF	Couples RF stage output to mixer input, keep small to insure proper stop time performance when RF AGC is active.
R1	300k Pot.	Sets level stop threshold.
R2	12k	Sets size of stop window.
R3	50k	Open collector pull up resistor.
R4	1k3	IF filter termination, and gain set.
R5	10k	Sets RC time constant on audio outputs, smaller values may cause distortion of high frequencies.
R6	200k	Sets gain of IF stage, affects noise floor and sensitivity.
R7	Meter Dependent	Sets full-scale deflection of meter.
R8	100k	Sets gain and threshold of RF AGC.
R9	100Ω	Aids mixer output decoupling.
R19	10k	Sets 2'nd pole in RF AGC, affects THD for large input signals.
R21	1.2 MΩ	Biases pin 5 to 0.4 volts which permits shorter stop time.
R24	820Ω	Sets system gain.
D1, D2, D3,	TOKO KV1235Z or Equivalent	Varactor diodes.
Resonator	450 kHz ± 1 kHz Murata*, BFU450C4N	Parallel type resonator.
IF filter	Murata* CFU450F5	Sets selectivity and tone response.

*Murata
2200 Lake Park Drive
Smyrna, GA 30080
(404) 436-1300

Performance Characteristics of Applications Circuit (Continued)

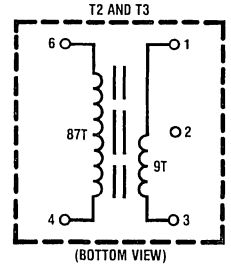
Part No. 5MFC–A087YRT
TOKO



TL/H/5185–17

Center Frequency = 2 MHz
Qu > 50 at 2 MHz

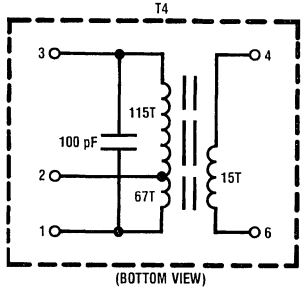
Part No. 7TRS–A5610CI
TOKO



TL/H/5185–18

Qu > 95 at 1 MHz
L_{4-6} = 200 μH

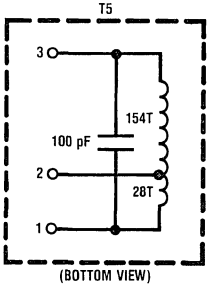
Part No. 7NRES–A5628EK
TOKO



TL/H/5185–19

Center Frequency = 450 kHz
Qu > 100 at 450 kHz

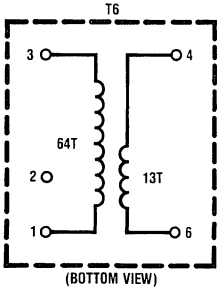
Part No. 7NRES–A5627AAG
TOKO



TL/H/5185–20

Center Frequency = 450 kHz
Qu > 100 at 450 kHz

Part No. 7TRS–A5609A0
TOKO



TL/H/5185–21

Center Frequency = 1 MHz
Qu > 95 at 1 MHz
L_{1-3} = 110 μH

*Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

Layout Considerations

Although the pinout of the LM1863 has been chosen to minimize layout problems, some care is required to insure proper performance. If the LM1863 is used with a loopstick antenna, care in the placement of C3 must be observed in order to minimize tweet radiation. Orient C3 parallel to the axis of the loopstick and as far away as possible. Keep C3 close to the IC. The ground on C6 should be located near the ground terminal of the 450 kHz ceramic filter. C11 should be located near Q2 and C12 should be located near the IC. Also, the resonator on Pin 7 and resistor R2 should be located near the IC in order to minimize tweet radiation.

The mixer output, Pin 10 and the IF input, Pin 11, traces should be as short as possible to prevent stray pick up from the resonator.

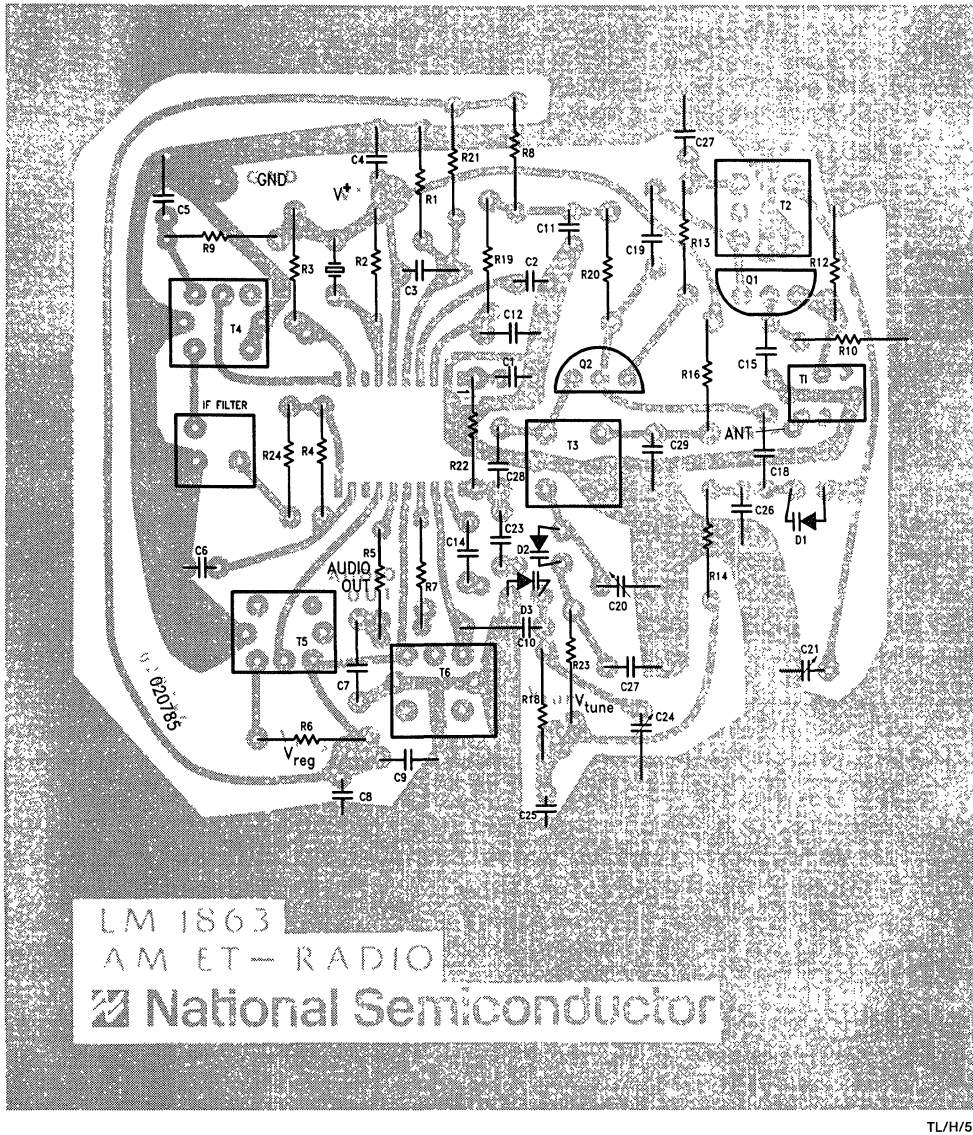
Applications Information

(See typical application and LM1863 schematic diagram.)

STOP DETECTOR

There are two criteria that determine when an electronically tuned radio is tuned to a valid station. The first criterion is that the incoming signal be of sufficient strength to be listenable. The second criterion requires that the radio be tuned

PC Layout (Component Side)



TL/H/5185–22

Applications Information (Continued)

to the center frequency of the incoming station. Both the signal strength threshold and the center tune window are externally adjustable.

The signal strength threshold is set by resistor R1. Increasing the value of this resistor will reduce the signal level threshold. There is no difficulty in setting the signal strength threshold, either above or below the AGC threshold.

Resistor R2 sets the center tune window. The incoming station is considered to be center tuned whenever the frequency of the signal at the IF output falls within the center tune window. Increasing the value of R2 will narrow the window, while decreasing R2 will widen the window. Since there is some interaction between R2 and R1, R2 should be chosen before R1. In the United States, stations within the AM band are spaced no closer than 10 kHz apart. Consequently, the controller should be set up to stop every 10 kHz within the AM band when the ETR is in scan mode. A center tune window anywhere less than ±10 kHz is therefore adequate in determining the center tune condition, though a narrower stop window is desirable in order to minimize the chance that side bands from a strong adjacent channel will fall within the stop window.

Because of asymmetry in the resonator amplitude characteristic, the center tune stop window will not be symmetric about the center frequency of the resonator. This is not a problem as long as the stop window brackets the center frequency of the IF and does not extend into the next channel. However, in order to avoid any problems in this regard it is recommended that the resonator center frequency deviate no more than ±1 kHz from the center frequency of the IF.

The stop output, Pin 9, is an open collector NPN transistor. This output must be taken to a positive voltage through a load resistor, R3. A valid stop condition is indicated by a high output level on Pin 9 (i.e., the NPN is turned off). The voltage on this pin should not exceed 16 volts.

STOP DETECTOR STOP TIME

The amount of time required for the LM1863 to output an accurate stop indication on Pin 9 is defined as the stop time. The stop time determines how quickly the ETR can scan across the AM band. There are several factors that influence the stop time. Since the signal level stop function operates in conjunction with the Automatic Gain Control (AGC), the AGC settling time is a critical factor. This settling time is dominated by the low frequency AGC pole which is set by C1 and internal IC resistances. Decreasing C1 will decrease the AGC settling time but increase total harmonic distortion, THD, of the recovered audio. A good compromise between AGC settling time and THD is very difficult to reach with a single pole AGC system. Consequently, the LM1863 has been designed with a second, higher frequency, AGC pole. This non-dominant pole is externally set by capacitor C2. As a result, C1 can be made much smaller than it otherwise could for an equivalent amount of THD. Reducing C1 will reduce the stop time. The combination of C1 and C2 as shown in the applications circuit results in a stop time of less than 50 ms for most input conditions, while at the same time the circuit achieves .9% THD at 80% modulation with 400 Hz modulation frequency at 10 mV input signal strength. Had C2 not been present the stop time would still be 50 ms but the THD for similar input conditions would be 8%. By decreasing both C1 and C2 (keeping the ratio of C1/C2 constant) the stop time can be reduced at the expense of THD, while the converse is also true.

The addition of a second pole to the AGC response does add some ringing to the AGC voltage following signal transients. The frequency, duration and amount of ringing are dependent on where both AGC poles are placed and to some extent the input signal conditions. The amount of ringing should be kept to a minimum in order to insure proper stop indications. The amount of ringing can be reduced by either reducing C2 (this will increase THD) or by increasing C1 (this will improve THD but increase stop time).

If the ratio of C1/C2 is made too small, an increase in low frequency noise may be noticed resulting from the peaking that a closed loop two pole system exhibits near the unity gain frequency. The extent of this peaking can be observed by examining the amount of recovered audio at various low frequency modulations. In general, the values shown reach a good compromise between THD, stop time, ringing and low frequency noise.

The center tuning detector on the LM1863 passes the signal at the IF output through a limiting amplifier which removes most of the modulation from the IF waveform. The output of this limiter is then applied to the resonator on Pin 7. Unfortunately, large modulation peaks are not completely removed by the limiting amplifier. Without C3, these large modulation peaks would cause glitches on the stop output when the LM1863 was tuned to a valid station. C3 acts to reduce these glitches by filtering the output of the center tune circuit. C3, however, also affects the stop time and cannot be made arbitrarily large. A time constant of about 30 ms on Pin 5 gives the best compromise. R21 biases Pin 5 to about .4 volts, which is below the stop threshold at this point. This biasing results in a shorter stop time.

Extra precaution can be taken within the software of the controller IC to further insure accurate stop detector performance over a wide variety of input signal conditions. A typical controller IC stop algorithm is as follows:

> The controller waits the first 10 ms after the LM1863 is tuned to the next channel. The controller then samples the LM1863 stop output 10 times within the next 40 ms. If no high output is sensed within that time the controller concludes there is no valid station at the frequency and moves to the next channel. If, however, at least one high output is detected within the first 50 ms the controller waits an additional 200 ms and at the end of that time re-samples the stop output in order to make its final stop determination.

RF AGC

The RF AGC detector is designed to control the gain of an external RF amplifier which is placed between the antenna and the mixer input. The RF AGC operates by detecting when the input signal to the mixer reaches 6 mVrms, the RF AGC threshold. When the mixer input signal reaches this level the RF AGC is activated and will hold the mixer input level relatively constant at the level of the RF AGC threshold. The gain of the RF AGC determines how constant the RF AGC can control the RF output. The LM1863 RF AGC is high gain and consequently the RF AGC output, Pin 3, will transition from high to low over a very narrow input range to the mixer when the LM1863 is examined in an OPEN LOOP condition. However, in a radio where the RF AGC controls the RF gain, a CLOSED LOOP negative feedback system is established. In this application the RF AGC output will transition from high to low over a large range of signal levels to the input of the RF stage.

Applications Information (Continued)

The RF AGC threshold has been carefully chosen to prevent overloading the mixer, which would cause distortion and tweet problems. However, the threshold level is sufficiently large to minimize the possibility of strong adjacent stations de-sensitizing the radio by activating the RF AGC and thereby gain reducing the RF front end.

The RF AGC output, Pin 3, is an open collector NPN transistor. This collector must be tied to a positive voltage through a load resistor, R8. Furthermore, decoupling is required (C11 and C12) in order to insure that the RF AGC does not induce significant distortion in the recovered audio. However, the tradeoff between good THD performance and fast stop time is not too severe for the RF AGC because large changes in the RF AGC level are unlikely when moving between adjacent channels. This is because the selectivity in the RF stage is not great enough to cause abrupt signal level changes at the mixer input as the radio is tuned. Thus, since the RF AGC does not have to follow abrupt signal level changes, the time constant on the AGC output can be relatively long which allows for good THD performance. C12 is required in order to insure good RF decoupling of signals at the RF AGC output, and sets the non-dominant pole.

The RF AGC 10 μA threshold is fixed at 6 mVrms at the mixer input. However, due to the gain of the RF stage and losses through the RF transformers, this level may be different when referenced to the antenna input. For the application circuit shown the RF threshold occurs at 2 mVrms at the dummy antenna input. Thus, the RF AGC threshold can effectively be adjusted by altering the gain of the RF stage. The value of R8 also has some affect on the RF AGC threshold of the application circuit. Smaller values will tend to increase the threshold while larger values will tend to reduce the threshold.

GAIN DISTRIBUTION

The purpose of this section is to clarify some of the tradeoffs involved in redistributing gain from one portion of the radio to another. An AM radio basically has three gain blocks consisting of the RF stage, the mixer, and the IF stage. The total gain of these three blocks must be sufficiently large as to insure reception of weak stations. Given then a fixed amount of required gain how does distributing this gain among the three blocks affect the radio performance?

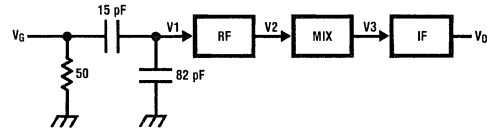
Large amounts of gain in the RF stage will have the effect of decreasing the RF AGC threshold. A decreased RF AGC threshold means that it is more likely that strong adjacent stations can activate the RF AGC and desensitize the radio. Also, a lot of RF gain implies large signals across the RF varactor diodes, which is undesirable for good tracking and can result in overloading these varactors which can cause cross modulation. On the other hand, high RF gain insures good noise performance and improved THD.

High mixer gain implies large signal swings at the mixer output, especially on AGC transients. These large signal swings could cause the mixer ouput transistors to saturate and also could overload the IF stage. On the other hand, redistributing the gain from the IF to the mixer would improve the noise performance of the radio. The gain of the mixer can be controlled moving the tap on the mixer output transformer, T4.

Since the output signal level of the IF is held constant by the AGC, increasing gain in the IF has the effect of reducing the signal level at the IF input. Noise sources at the IF input therefore become a larger percentage of the IF input signal thereby degrading the S/N floor of the radio. For this reason, the LM1863 employs 20 dB of IF AGC. The IF gain of the LM1863 is adjustable by changing the tap across the IF ouput coil, or by changing the ratio of R24 to R4.

The gain distribution for the application circuit is as follows:

Gain Distribution



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V_G = 0 dB (10 μV)
V1 = −16 dB
V2 = +10 dB (Pin 20)
V3 = +33 dB (Pin 11)
V_O = +84 dB (Pin 14)

The IF gain could also be varied by changing the value of R6 across the IF output coil. However, it is a good idea to maintain a high Q IF tank in order to achieve good adjacent channel rejection. In order to prevent distortion due to overloading the IF amplifier, it is important that the impedance Pin 14 sees looking into the IF output tank, T5, does not go below 3K ohms.

The above gain distribution is prior to any AGC action in the radio. This distribution represents a good compromise between the various tradeoffs outlined previously.

LEVEL CONTROLLED LOCAL OSCILLATOR

Tracking of the RF varactors with the local oscillator varactor is a serious consideration in order to insure adequate performance of the ETR radio. Due to non-linear capacitance versus voltage characteristic of the varactor, large signals across these varactors will tend to modulate their capacitance and cause tracking problems. This problem is compounded further if the level of the signals across the varactors change. In an AM radio, the local oscillator frequency changes a ratio of two to one. The Q of the oscillator tank remains fairly constant over this range. Thus, since $Q = R_P/\omega L$ = Constant, this implies that R_P(R_P = unloaded parallel resistance of the tank) must change two to one. The internal level-control loop prevents the two to one change in AC voltage across the tank which the change in the R_P would otherwise cause.

Phase jitter of the local oscillator is very important in regard to AM stereo, where L-R information is contained in the phase of the carrier. Local oscillator jitter has the effect of modulating the L-R channel with phase noise, thus degrading the stereo signal to noise performance. Great care has been taken in the design of the LM1863 local oscillator to insure that phase jitter is a minimum. In fact the dominant source of phase jitter is the high impedance resistor drive to the varactor. The thermal noise of the resistor modulates the varactor voltage, thus causing phase jitter.

VARACTOR TUNED RF STAGE

Electronically tuned car radios require the use of a tuned RF stage prior to the mixer. Many of the performance charac-

Applications Information (Continued)

teristics of the radio are determined by the design of this stage. Generally speaking it is very difficult to design an integrated RF stage in bipolar, as bipolar transistors do not have good overload characteristics. Thus, the RF stage is usually designed using discrete components. Because of this there is a great deal of concern with minimizing the number of discrete components without severely sacrificing performance. The applications circuit RF stage does just this.

The circuit consists of only two active devices, an N-channel JFET, Q1, which is connected in a cascode type of configuration with an NPN BJT, Q2. Both Q1 and Q2 are varactor tuned gain stages. Q2 also serves to gain reduce Q1 when Q2's base is pulled low by the RF AGC circuit on the LM1863. The gain reduction occurs because Q1 is driven into a low gain resistive region as its drain voltage is reduced. R10 and C15 set the gain of the 1'st RF stage which is kept high (about 19 dB) for good low signal, signal/noise performance. The gain of the front end to the mixer input referenced to the generator output is about +10 dB.

T2 in conjunction with D1, C21 and C26 form the 1'st tuned circuit. C26 does not completely de-couple the RF signal at the cathode of the varactor. In fact, the combination of C26 and C19 act to keep the gain of the whole RF stage constant over the entire AM band. Without special care in this regard the gain variation could be as high as 14 dB. This gain variation would result from the increase in impedance at the secondary's of T2 and T1 as the tuned frequency is increased. The increased impedance results from a constant Q=Rp/(wL) of the tanks over the AM band. With C26 and C19 the gain is held constant to within 6 dB (including the tracking error) over the entire AM band.

C27 de-couples RF signal from the top of T2's primary and allows Q2 to operate properly. C18 is a coupling capacitor which in conjunction with C19 couples the signal from the 1'st RF stage to the 2'nd RF stage. R20 acts to isolate this signal from AC ground at C11. R19 acts in conjunction with C12 to set a high frequency (ie: non-dominant) RF AGC pole which is important for low distortion when the RF AGC is active. The dominant RF AGC pole is set by R8 and C11. Q2 is a high beta transistor allowing for little voltage drop across R20 and R8 due to base current. This keeps the emitter of Q2 sufficiently high (in the absence of RF AGC) to bias Q1 in its square law region.

R13 acts to reduce the 2'nd stage gain and increase Q2's signal handling. R13 must not get too large, however, (ie: R13>100 Ω), or low level signal/noise will be degraded. T3 in conjunction with C20, C27 and D2 form the 2'nd RF tuned circuit. The output of Q2 is capacitively coupled through C28 to the mixer input. The output of Q2 is loaded not only by the reflected secondary impedance but also by R22. R22 is carefully chosen to load the 2'nd stage tuned circuit and broaden its bandwidth. The increased bandwidth of the 2'nd stage greatly improves the cross modulation performance of the front end. In the absence of this increased bandwidth, the relatively large AC signals across varactor D2 result in cross modulation. R22 also reduces the total gain of the 2'nd stage. R22 does slightly degrade (by about 6 dB) the image rejection especially at the high end of the AM band. However, the image rejection of this front end is still excellent and 6 dB is a small price to pay for the greatly increased immunity to cross modulation.

R16 and C29 decouple unwanted signals on V+ from being coupled into the RF stage. This front end also offers superior performance with respect to varactor overload by strong adjacent channels. This results because of the way that gain has been distributed between the 1'st and 2'nd stages.

In summary, this front end offers two stages of RF gain with the 2'nd stage acting to gain reduce the 1'st stage when RF AGC is active. Furthermore, a unique coupling scheme is employed from the output of the 1'st stage to the input of the 2'nd stage. This coupling scheme equalizes the gain from one end of the AM band to the other. Additional care has been taken to insure that excellent cross modulation performance, image rejection, signal to noise performance, overload performance, and low distortion are achieved. Performance characteristics for this front end in conjunction with the LM1863 are shown in the data sheet. Also, information with regard to the bandwidth of the front end versus tuned frequency are given below.

TUNED FREQUENCY	−3 dB BANDWIDTH
530 kHz	6.6 kHz
600 kHz	7.2 kHz
1200 kHz	20.6 kHz
1500 kHz	26.4 kHz
1630 kHz	36 kHz

VARACTOR ALIGNMENT PROCEDURE

The following is a procedure which will allow you to properly align the RF and local oscillator trim capacitors and coils to insure proper tracking across the AM band.

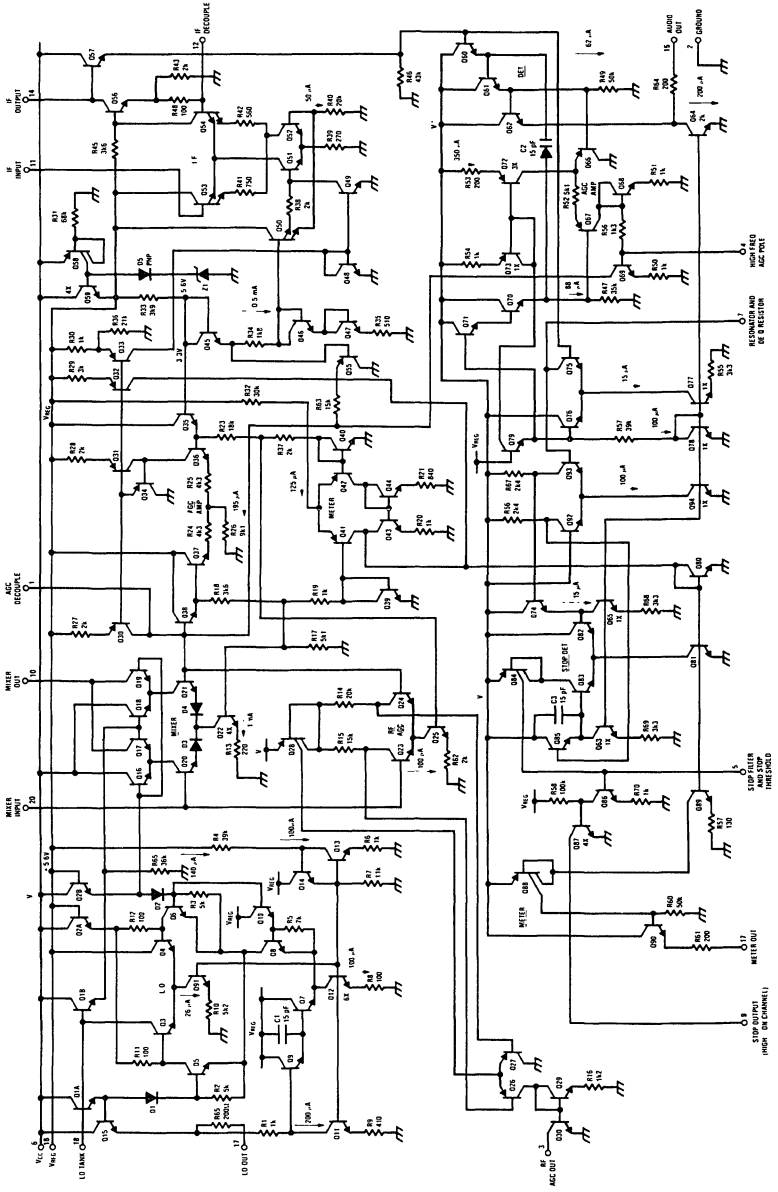
1. Set the voltage across the varactors = 1 volt.
2. Set the trimmers to 50%.
3. Adjust the oscillator coil until the local oscillator is at 980 kHz.
4. Increase the varactor voltage until the local oscillator (LO) is at 2060 kHz and check to see if this voltage is less than 9.5 volts but greater than 7.5 volts. If it is then the LO is aligned. If it is not then adjust the LO coil/trimmer until the varactor voltage falls in this range.
5. Set the RF in to 600 kHz and adjust the tuning voltage until the LO is at 1050 kHz. Peak all RF coils for maximum recovered audio at low input levels.
6. Set RF in to 1500 kHz and adjust the tuning voltage until the LO is at 1950 kHz. Peak all RF trim capacitors for maximum recovered audio at low input levels.
7. Go back to step 5 and iterate for best adjustment.
8. Check the radio gain at 530 kHz and 750 kHz to make sure that the gain is about the same at these two frequencys. If it is not, then slightly adjust the RF coils until it is.

The above procedure will insure perfect tracking at 600 kHz, 950 kHz and 1500 kHz. The amount of gain variation across the AM band using the above procedure should not exceed 6 dB.

ADDITIONAL INFORMATION

R5 and C7 act as a low pass filter to remove most of the residual 450 kHz IF signal from the audio output. Some residual 450 kHz signal is still present, however, and may need to be further removed prior to audio amplification. This need becomes more important when the LM1863 is used in conjunction with a loopstick antenna which might pick up an amplified 450 kHz signal. An additional pole can be added to the audio output after R5 and C7 prior to audio amplification if further reduction of the 450 kHz component is required.

Equivalent Schematic Diagram



TL/H/5185–24

National Semiconductor Corporation

LM1865/LM1965/LM2065 Advanced FM IF System

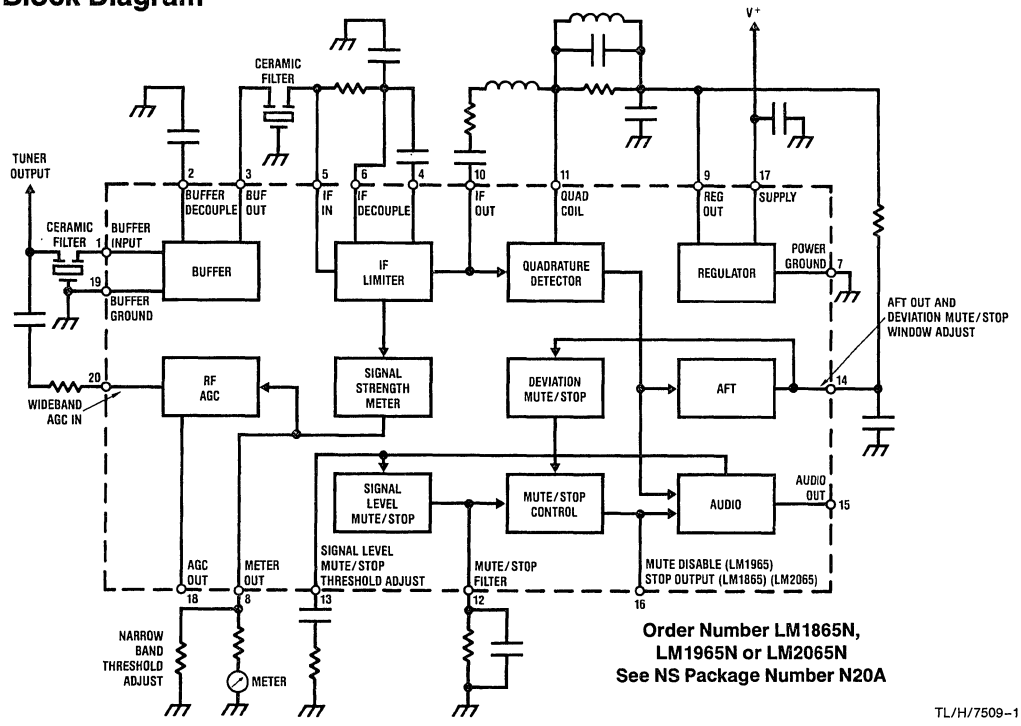
General Description

Reduced external component cost, improved performance, and additonal functions are key features to the LM1865/LM1965/LM2065 FM IF system. The LM1865 and LM2065 are designed for use in electronically tuned radio applications. These versions contain both deviation and signal level stop circuitry in addition to an open-collector stop output. The LM1865 and LM2065 differ only in the direction of the AGC output voltage they generate on pin 18. The LM1865 generates a reverse AGC voltage (ie: decreasing AGC voltage with increasing signal) and the LM2065 generates a forward AGC voltage (ie: increasing AGC voltage with increasing signal.) The LM1965 has a reverse AGC characteristic. The LM1965 is designed for use in manually tuned radios and provides a deviation and signal level mute function in addition to a pin that disables the mute function when grounded. All three versions are offered in both 20 pin D.I.P. and S.O. packages.

Features

- On-chip buffer to provide gain and terminate two ceramic filters
- Low distortion 0.1% typical with a single tuned quadrature coil for 100% modulation.
- Broad off frequency distortion characteristic
- Low THD at minimum AFT offset
- Meter output proportional to signal level
- Mute function with mute disable and soft deviation mute for LM1965
- Stop detector with open-collector output for LM1865/LM2065
- Adjustable signal level mute/stop threshold, controlled either by ultrasonic noise in the recovered audio or by the meter output
- Adjustable deviation mute/stop threshold
- Separate time constants for signal level and deviation mute/stop
- Dual threshold AGC eliminates need for local/distance switch and offers improved immunity from third order intermodulation products due to tuner overload
- User control of both AGC thresholds
- Excellent signal to noise ratio, AM rejection and system limiting sensitivity

Block Diagram



Order Number LM1865N, LM1965N or LM2065N
See NS Package Number N20A

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FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, Pin 17	16V
Package Dissipation (Note 1)	2.0W
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	−20°C to +85°C
Max Voltage on Pin 16 (Stop Output) for LM1865, LM2065	16V

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, T_A = 25°C, V^+ = 12V; S1 in position 2; S2 in position 1; and S3 in position 2 unless indicated otherwise

Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS					
Supply Current			33	45	mA
Pin 9, Regulator Voltage			5.7		V
Operating Voltage Range	(See Note 2)	7.3		16	V
Pin 18, Output Leakage Current	Pin 20 Open, V_{IF} = 0, S3 in Position 1		0.1		μA
Pin 16, Stop Low Output Voltage (LM1865 Only)	S1 in Position 1, S2 in Position 3		0.3		V
Pin 16, Stop High Output Leakage Current (LM1865 Only)	S2 in Position 2, V14 = V9		0.1		μA
Pin 15, Audio Output Resistance			4.7		kΩ
Pin 1, Buffer Input Resistance	Measured at DC		350		Ω
Pin 3, Buffer Output Resistance	Measured at DC		350		Ω
Pin 20, Wide Band Input Resistance	Measured at DC		2		Ω
Pin 8, Meter Output Resistance			1		kΩ
DYNAMIC CHARACTERISTICS f_{MOD} = 400 Hz, f_o = 10.7 MHz, Deviation = ±75 kHz					
−3 dB Limiting Sensitivity	IF Only (See Note 3)		60	120	μVrms
Buffer Voltage Gain	V_{IN} Pin 1 = 10 mVrms at 10.7 MHz	19	22	25	dB
Recovered Audio	V_{IF} = 10 mVrms, V14 = V9	275	320	470	mVrms
Signal-to-Noise	V_{IF} = 10 mVrms, V14 = V9 (See Note 4)	70	84		dB
AM Rejection	V14 = V9				
	V_{IF} = 1 mV, 30% AM Mod	50	60		dB
	V_{IF} = 10 mV, 30% AM Mod	50	60		dB
Minimum Total Harmonic Distortion	V_{IF} = 10 mV		0.1	0.35	%
THD at Frequency where V14 = V9 (Zero AFT Offset)	V_{IF} = 10 mV, Tune until V14 = V9		0.1	0.45	%
THD ± 10 kHz from Frequency where V14 = V9	V_{IF} = 10 mV		0.15		%
AFT Offset Frequency for Deviation Mute (LM1965 Only)	V_{IF} = 10 mV, Audio = −3 dB, S2 in Position 4 Offset = (Frequency for −3 dB Audio) − (Frequency where V14 = V9)		±62		kHz
AFT Offset Frequency for Low Stop Output at Pin 16 (LM1865 and LM2065 Only)	V_{IF} = 10 mV, S2 in Position 3, f_{MOD} = 0 Offset = (Frequency for Pin 16 Low) − (Frequency where V14 = V9)		±50		kHz
Ultrasonic Mute/Stop Level Threshold	V14 = V9, S1 in Position 3 (See Note 5) V_{IF} = 10 mV f_{MOD} = 100 kHz S2 in Position 4 (LM1965) S2 in Position 3 (LM1865/LM2065) Amount of Deviation where Audio Mutes (LM1965) Amount of Deviation where V16 → Low (LM1865, LM2065)		60		kHz

Electrical Characteristics

Test Circuit, T_A = 25°C, V^+ = 12V; S1 in position 2; S2 in position 1; and S3 in position 2 unless indicated otherwise (Continued)

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC CHARACTERISTICS f_{MOD} = 400 Hz, f_o = 10.7 MHz, Deviation = ±75 kHz (Continued)					
Pin 13 Mute/Stop Threshold Voltage	V14 = V9, S1 in Position 4 S2 in Position 4 (LM1965) S2 in Position 3 (LM1865, LM2065) V13 where Audio Mutes (LM1965) V13 where V16 → Low (LM1865, LM2065)		220		mV
Amount of Muting (LM1965 Only)	S2 in Position 4, S1 in Position 1, V_{IF} = 10 mV		66		dB
Amount of Muting with Pin 13 and Pin 16 Grounded	S1 in Position 1 V14, = V9, V_{IF} = 10 mV		0		dB
Narrow Band AGC Threshold	Increase IF Input until I_{AGC} = 0.1 mA Pin 20 = 30 mVrms (See Note 6)	100	210	300	μVrms
Wide Band AGC Threshold	V_{IF} = 100 mVrms Increase Signal to Pin 20 until I_{AGC} = 0.1 mA (See Note 6)	5	12	22	mVrms
Pin 18, Low Output Voltage (LM1865 and LM1965 only)	V_{IN} Pin 20 = 100 mV, V_{IF} = 100 mVrms		0.2	0.5	V
Pin 18, High Output Voltage (LM2065 only)	V_{IN} Pin 20 = 100 mV, V_{IF} = 100 mVrms, (See Note 6)		11.7		V
Pin 8, Meter Output Voltage	V_{IF} = 10 μV V_{IF} = 300 μV V_{IF} = 3 mV		0.1 1.1 2.6		V V V

Note 1: Above T_A = 25°C derate based on $T_{J(max)}$ = 150°C and θ_{JA} = 60°C/W.

Note 2: All data sheet specifications are for V^+ = 12V may change slightly with supply.

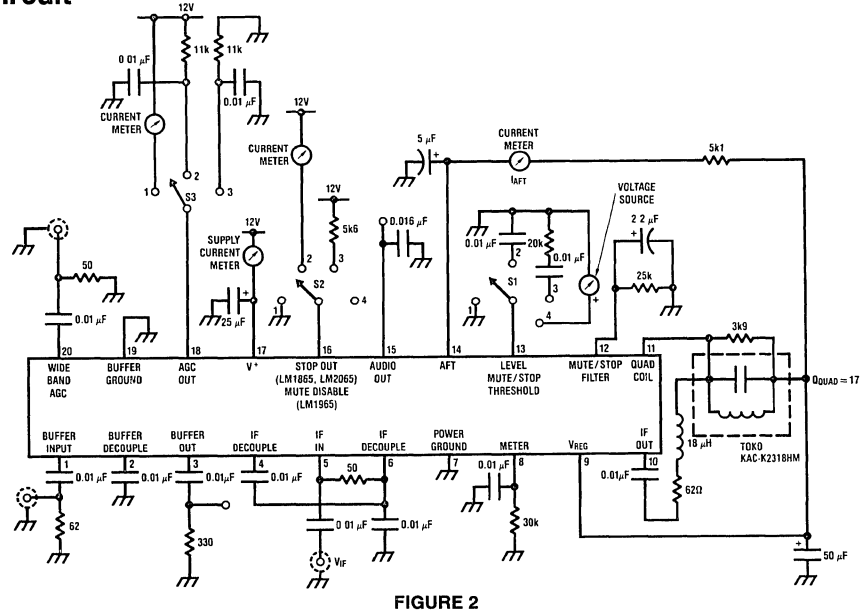
Note 3: When the IF is preceded by 22 dB gain in the buffer, excellent system sensitivity is achieved.

Note 4: Measured with a notch at 60 Hz and 20 Hz to 100 kHz bandwidth.

Note 5: FM modulate RF source with a 100 kHz audio signal and find what modulation level, expressed as kHz deviation, results in audio mute for the LM1965 or V16 → 12V for the LM1865/LM2065.

Note 6: S3 in Position 3 for LM2065.

Test Circuit

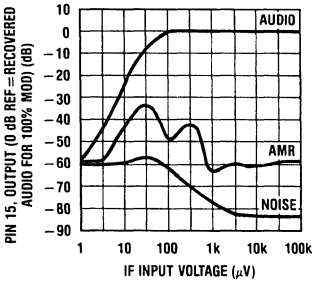


TL/H/7509–2

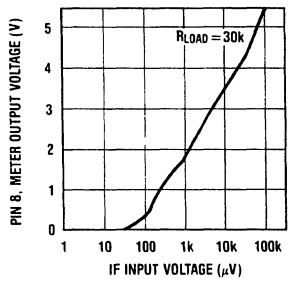
FIGURE 2

Typical Performance Characteristics (from Test Circuit)

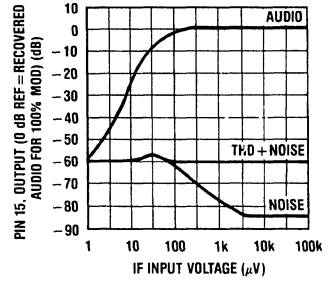
FM Limiting Characteristics and AM Rejection



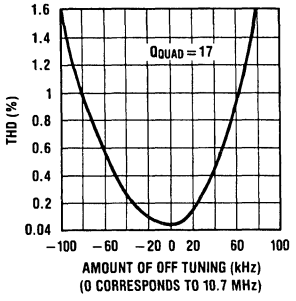
Pin 8, Meter Output Voltage vs IF Input Level



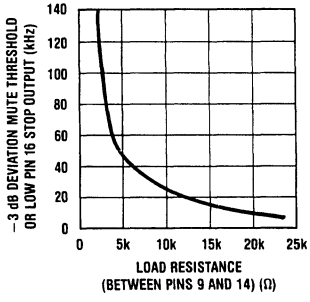
FM Limiting Characteristics + THD



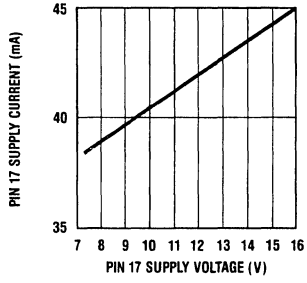
% THD vs OFF Tuning (Single Tuned Quadrature Coil)



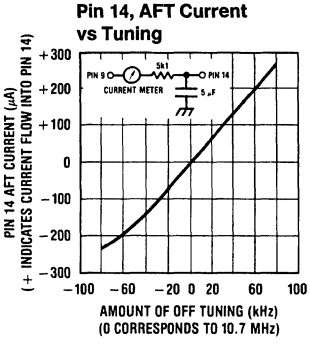
Deviation Mute/Stop Threshold as a Function of AFT Load Resistor



Supply Current vs Supply Voltage



Pin 14, AFT Current vs Tuning

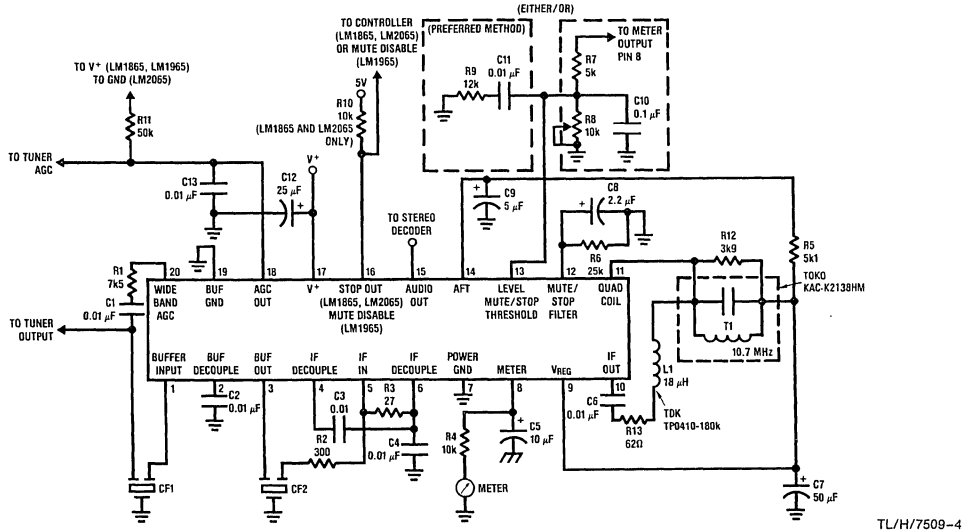


TL/H/7509–3

Coils and ceramic filters are available from:

Toko America	Murata
1250 Feehanville Drive	2200 Lake Park Drive
Mount Prospect, IL 60056	Smyrna, GA 30080
(312) 297-0070	(404) 436-1300

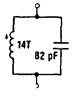
Application Circuit



TL/H/7509–4

FIGURE 3

IC External Components (See Application Circuit)

Component	Typical Value	Comments
C1	0.01 µF	AC coupling for wide band AGC input
C2	0.01 µF	Buffer and AGC supply decoupling
C3, C4	0.01 µF	IF decoupling capacitors
C5	10 µF	Meter decoupling capacitor
C6	0.01 µF	AC coupling for IF output
C7	50 µF	Regulator decoupling capacitor, affects S/N floor
C8	2.2 µF	Level mute/stop time constant
C9	5 µF	AFT decoupling, affects stop time
C10	0.1 µF	Disables noise mute/stop
C11	0.01 µF	AC coupling for noise mute/stop threshold adjust
C12	25 µF	Supply decoupling
C13	0.01 µF	AGC output decoupling capacitor
R1	Tuner Dependent	Wide band AGC threshold adjust
R2, R3	Tuner Dependent	Gain set and bias for IF; R2 + R3 = 330Ω to terminate ceramic filter
R4	Meter Dependent	Sets full-scale on meter
R5	5k1	Deviation mute/stop window adjustment
R6	25k	Mute/stop filter, affects stop time
R7	5k	Level mute/stop threshold adjustment
R8	10k Pot	Level mute/stop threshold adjustment
R9	12k	Noise mute/stop threshold adjustment, decrease resistor for lower S/N at threshold, for optimum performance over temp. and gain variation, set this resistor value so that the signal level mute/stop threshold occurs in the radio at 45dB S/N (±3 dB) in mono.
R10	10k	Load for open-collector stop output
R11	50k	AGC output load resistor for open-collector output
R12	3k9	Sets Q of quadrature coil affecting THD, S/N and recovered audio
R13	62Ω	Optimises minimum THD
L1	18 µH Q_u>50 @ 10.7 MHz TDK Electronics TPO410-180K or equivalent	Sets signal swing across quadrature coil, High Q is important to minimize effect variation of Q has on both minimum THD and AFT offset.
T1	 Q_u>70 @ 10.7 MHz, L to resonate w/82 pF @ 10.7 MHz TOKO KAC-K2318HM or equivalent	10.7 MHz quadrature coil: Q_{UL} > 70
CF1, CF2	Murata SFE10.7ML or equivalent	10.7 MHz ceramic resonators provide selectivity; good group delay characteristics important for low THD of system

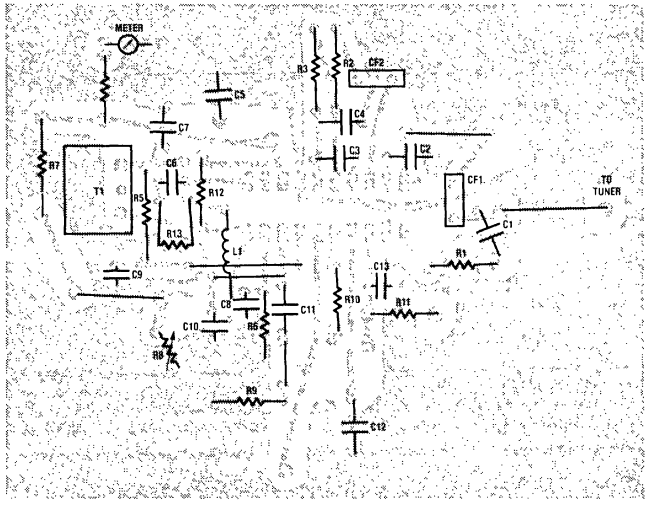
TL/H/7509–5

Typical Application

LAYOUT CONSIDERATIONS

Although the pinout of the LM1865/LM1965/LM2065 has been chosen to minimize layout problems, some care is required to insure stability. The ground terminal on CF1 should return to both the input signal ground and the buffer ground, pin 19. The ground terminal on CF2 should return to the ground side of C4. The quadrature coil T1 and inductor L1 should be separated from the input circuitry as far as possible.

PC Layout (Component Side)



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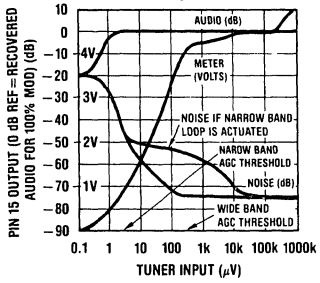
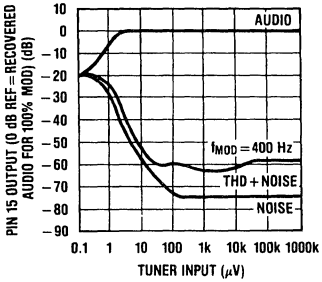
PERFORMANCE CHARACTERISTICS OF TYPICAL APPLICATION WITH TUNER

The following data was taken using the typical application circuit in conjunction with an FM tuner with 43 dB of gain, a 5.5 dB noise figure, and 30 dB of AGC range. The tuner was driven from a 50Ω source. 75 μs of de-emphasis was used on the audio output, pin 15. The 0 dB reference is for ±75 kHz deviation at 400 Hz modulation.

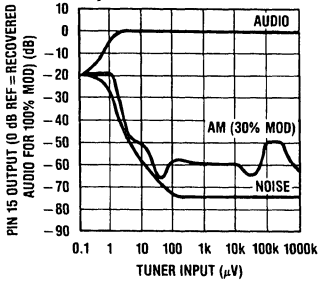
Meter Output and Signal-to-Noise vs Tuner Input



Total Harmonic Distortion vs Tuner Input



AM Rejection vs Tuner Input



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−3 dB limiting = 0.9 μV
30 dB quieting = 1.4 μV
Level stop/mute threshold = 1.4 μV
Deviation mute window (−3 dB) = ±45 kHz

Application Notes

ADJUSTABLE MUTE/STOP THRESHOLD

The threshold adjustments for the mute and stop functions are controlled by the same pins. Thus, the term mute/stop will be used to designate either function.

The adjustable mute/stop threshold in the LM1865/LM1965/LM2065 allows for user programming of the signal level at which muting or stop indication takes place. The adjustment can be made in two mutually exclusive ways. The first way is to take a voltage divider from the meter output (pin 8) to the off channel mute input (pin 13). When the voltage at pin 13 falls below 0.22V, an internal comparator is tripped causing muted or causing the stop output to go low. Adjustment of the voltage divider ratio changes the signal level at which this happens.

The second method of mute/stop detection as a function of signal level is to use the presence of ultrasonic noise in the recovered audio to trip the internal comparator. As the signal level at the antenna of the radio drops, the amount of noise in the recovered audio, both audible and ultrasonic, increases.

The recovered audio is internally coupled through a high pass filter to pin 13 which is internally biased above the comparator trip point. Large negative-going noise spikes will drive pin 13 below the comparator trip point and cause mute/stop action. A simplified circuit is shown in *Figure 4.*

Since the input to the comparator is noise, the output of the comparator is noise. Consequently, a mute/stop filter on pin 12 is required to convert output noise spikes to an average DC value. This filter is not necessary if pin 13 is driven from the meter.

Adjustment of the mute/stop threshold in the noise mode is accomplished by adjusting the pole of the high pass filter coupled to the comparator input. This is done with a series capacitor/resistor combination, R9 C11, from pin 13 to ground. As the pole is moved higher in frequency (i.e., R9 gets smaller) more ultrasonic noise is required in the recovered audio in order to initiate mute/stop action. This corresponds to a weaker signal at the antenna of the radio. In choosing the correct value for R9 it is important to make sure that recovered audio below 75 kHz is not sufficient to cause mute/stop action. This is because stereo and SCA information are contained in the audio signal up to 75 kHz. Also note that the ultrasonic mute/stop circuit will not operate properly unless a tuner is connected to the IF. This is because, at low signal levels, the noise at the tuner output dominates any noise sources in the IC. Consequently, driving the IC directly with a 50Ω generator is much less noisy than driving the IC with a tuner and therefore not realistic. The RC filter on pin 12 not only filters out noise from the comparator output but controls the "feel" when manually tuning. For example, a very long time constant will cause the mute to remain active if you rapidly tune through valid strong stations and will only release the mute if you slowly tune to a valid station. Conversely, a short time constant will allow the mute to kick in and out as one tunes rapidly through valid stations.

The advantage in using the noise mute/stop approach versus the meter driven approach is that the point at which mute/stop action occurs is directly related to the signal-to-noise ratio in the recovered audio. Furthermore, the mute/stop threshold is not subject to production and temperature variations in the meter output voltage at low signal levels, and thus might be able to be set without a production adjustment of the radio. The noise mute/stop threshold is very insensitive to temperature and gain variations. Proper operation of this circuit requires that the signal level mute/stop threshold be set at a signal level that achieves 45 dB S/N (±3 dB) in mono. in a radio. In an electronically tuned radio, the signal level stop threshold can be set to a much larger level by gain reducing the tuner (ie. pulling the AGC line) in scan mode and then releasing the AGC once the radio stops on a station. In an environment where temperature variations are minimal and manual adjustment of the signal level mute/stop threshold is desired, then the meter driven approach is the best alternative.

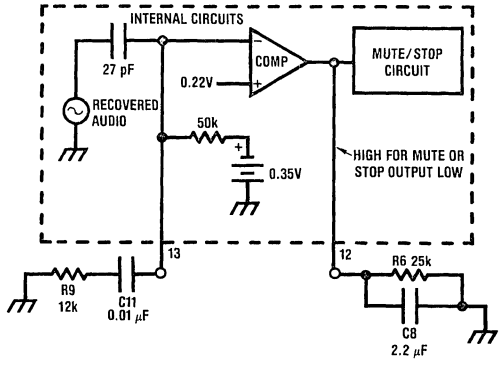

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FIGURE 4. Simplified Level Mute/Stop Circuit

Application Notes (Continued)

DEVIATION MUTE/STOP

As with the LM3189, the resistor connected between V_{REG} (pin 9) and the AFT (pin 14) sets the deviation mute/stop window (see Typical Performance Characteristics). The LM1965 was designed with a soft deviation mute. This means that the audio is gradually muted as you off tune from center frequency. Gradually muting avoids the problem of an audio pop which would otherwise occur due to the unavoidable DC voltage shift at the audio output that accompanies the muting action. Capacitor C9 on the AFT pin sets the time constant for the deviation mute/stop independent of the level mute/stop time constant. C9 should be large enough to remove the audio from the AFT. The AFT pulls high at low signal levels if the IF is driven directly from a 50Ω generator and not a tuner. This is a result of a loss of signal across the quad coil and a resulting phase shift in the quadrature detector. This phase shift offsets the AFT. With a tuner and sufficient IF gain, at low signal levels there will be enough noise across the quad coil to prevent much of this AFT shift. Thus, care should be taken when adjusting the IF gain (which is done by adjusting the ratio of R3 to R2) to minimize the AFT shift. Grounding pin 16 on the LM1965 will disable the mute function.

STOP TIME

An electronically tuned radio (ETR) pauses at fixed intervals across the FM band and awaits the stop indication from the LM1865/LM2065. If within a predetermined period of time, no stop indication is forthcoming, the controller circuit concludes that there is no valid station at that frequency and will tune to the next interval. There are several time constants that can affect the amount of time it takes the LM1865/LM2065 to output a valid stop indication on pin 16. In this section each time constant will be discussed.

Deviation Stop Time Constant

An offset voltage is generated by the AFT if the LM1865/LM2065 is tuned to either side of a station. Since deviation stop detection in the LM1865/LM2065 is detected by the voltage at pin 14, it is important that this voltage move fast enough to make the deviation stop decision within the time allowed by the controller. The speed at which the voltage at pin 14 moves is governed by the RC time constant, R5 C9. This time constant must be chosen long enough to remove recovered audio from pin 14 and short enough to allow for reasonable stop detection time.

Signal Level Stop Using Ultrasonic Noise Detection

As previously mentioned, the R6 C8 time constant on pin 12 is necessary to filter the noise spikes on the output of the internal comparator in the LM1865/LM1965/LM2065. This time constant also determines the level stop time. When the voltage at pin 12 is above a threshold voltage of about 0.6V, the stop output is low. The maximum voltage at pin 12 is about 0.8V. The level stop time is dominated by the amount of time it takes the voltage at pin 12 to fall from 0.8V to 0.6V. The voltage at pin 12 follows an exponential decay with RC time constant given by R6 C8. For example if R6 = 25k and C8 = 2.2 μF the stop time is given by

$$t = -(24k)\,(2.2\ \mu F)\ \ell n \left(\frac{0.6}{0.8}\right)$$

which yields t = 15 ms. It should be noted that the 0.6V threshold at pin 12 has a high temperature dependence and can move as much as 100 mV in either direction.

Signal Level Stop Using the Meter Output, Pin 8

As mentioned previously, R6 C8 is not necessary when the meter output is used to drive pin 13. Consequently, this time constant is not a factor in determining the stop time. However, the speed at which the meter voltage can move may become important in this regard. This speed is a function of the resistive load on pin 8 and filter capacitance, C5.

AGC Time Constant

In tuning from a strong station to a weaker station above the level stop threshold, the AGC voltage will move in order to try to maintain a constant tuner output. The AGC voltage must move sufficiently fast so that the tuner is gain increased to the point that the level stop indicates a valid station. This time constant is controlled by R11 and C13.

DISTORTION COMPENSATION CIRCUIT

The quadrature detector of the LM1865/LM1965/LM2065 has been designed with a special circuit that compensates for distortion generated by the non-linear phase characteristic of the quadrature coil. This circuit not only has the effect of reducing distortion, but also desensitizes the distortion as a function of tuning characteristic. As a result, low distortion is achieved with a single tuned quad coil without the need for a double tuned coil which is costly and difficult to adjust on a production basis. The lower distortion has been achieved without any degradation of the noise floor of the audio output. Futhermore, the compensation circuit first-order cancels the effect of quadrature coil Q on distortion.

When measuring the total harmonic distortion (THD) of the LM1865/LM1965/LM2065, it is imperative that a low distortion RF generator be used. In the past it has been possible to cancel out distortion in the generator by adjustment of the quadrature coil. This is because centering the quadrature coil at other than the point of inflection on the S-curve introduces 2nd harmonic distortion which can cancel 2nd harmonic distortion in the generator. Thus low THD numbers may have been obtained wrongly. Large AFT offsets asymmetrical off tuning characteristic, and less than minimum THD will be observed if alignment of the quadrature coil is done with a high distortion RF generator.

Care must also be taken in choosing ceramic filters for the LM1865/LM1965/LM2065. It is important to use filters with good group delay characteristics and wide enough bandwidth to pass enough FM sidebands to achieve low distortion.

Application Notes (Continued)

The LM1865/LM1965/LM2065 has been carefully designed to insure low AFT offset current at the point of minimum THD. AFT offset current will cause a non-symmetric deviation mute/stop window about the point of minimum THD. No external AFT offset adjustment should be necessary with the LM1865/LM1965/LM2065. The amount of resistance in series with the 18 μH quadrature coil drive inductor, L1, has a significant effect on the minimum THD. This series resistance is contributed not only by R13 but also by the Q of L1. The Q of L1 should be as high as possible (ie: Q>50) in order to avoid production problems with the Q variation of L1. Once R13 has been optimized for minimum THD, adjustment on a radio by radio basis should be un-necessary.

DUAL THRESHOLD AGC (AUTOMATIC LOCAL/DISTANCE SWITCH)

There is a well recognized need in the field for gain reducing (AGCing) the front end (tuner) of an FM receiver. This gain reduction is important in preventing overload of the front end which might occur for large signal inputs. Overloading the front end with two out-of-band signals, one channel spacing apart and one channel spacing from center frequency, or, two channel spacings apart and two channel spacings from center frequency, will produce a third order intermodulation product (IM_3) which falls inband. This IM_3 product can completely block out a weaker desired station. The AGC in the LM1865/LM1965/LM2065 has been specially designed to deal with the problem of IM_3.

With the LM1865/LM1965/LM2065 system, a low AGC threshold is achieved whenever there are strong out-of-band signals that might generate an interfering IM_3 product, and a high AGC threshold is achieved if there are no strong out-of-band signals. The high AGC threshold allows the receiver to obtain its best signal-to-noise performance when there is no possibility of an IM_3 product. The low AGC threshold allows for weaker desired stations to be received without gain-reducing the tuner. It should be noted that when the AGC threshold is set low, there will be a signal-to-noise compromise, but is assumed that it is more desirable to listen to a slightly noisy station than to listen to an undesired IM_3 product. The simplified circuit diagram (*Figure 5*) of the AGC system shows how the dual AGC thresholds are achieved.

V_m = 1V corresponds to a fixed in-band signal level (defined as V_{NB}) at the tuner output. V_{NB} will be referred to as the "narrow band threshold". V_{WB} also corresponds to a fixed tuner output which can either be an in-band or out-of-band signal. This fixed tuner output will be called the "wide band threshold". Always $V_{WB} > V_{NB}$. R11 and C13 define the AGC time constant. A reverse AGC system is shown. This means that V_{AGC} decreases to gain-reduce the tuner. The LM1865/LM1965 AGC output is an open-collector current source capable of sinking at least 1 mA. The LM2065 AGC output is also an open collector current source capable of sourcing at least 1 mA. The AGC voltage can move over the full range of the V^+ supply.

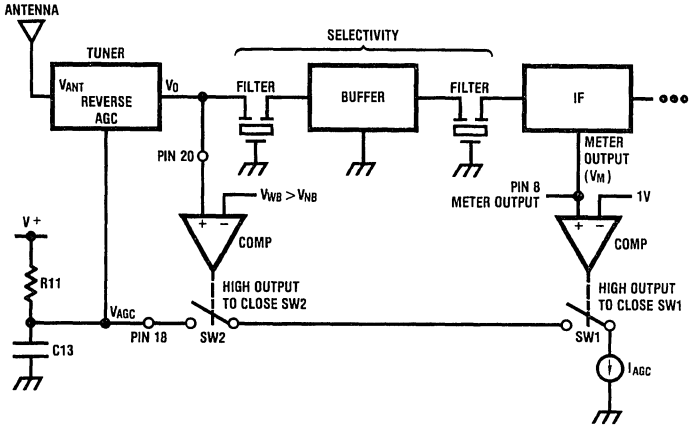

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FIGURE 5. Dual Threshold AGC

$I_1 = GM_1 V_m$ only if $V_m > 1V$
otherwise $I_1 = 0$

Gm_1, V_{WB} = constants

$I_{AGC} = Gm_2 V_o$ where $Gm_2 = I_1/26$ mV *and*
$V_o > V_{WB}$ otherwise $I_{AGC} = 0$

Application Notes (Continued)

First examine what happens with a single in-band signal as we vary the strength of this signal. *Figures 6 and 7* illustrate what happens at the tuner and AGC outputs.

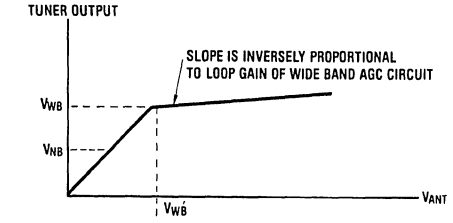

FIGURE 6

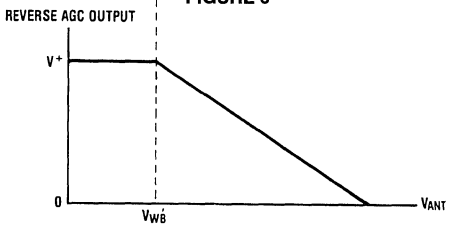

FIGURE 7

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In *Figure 7* there is no AGC output until the tuner output equals the wide band threshold. At this point both SW2 and SW1 are closed and the AGC holds the tuner output in *Figure 6* relatively constant.

Another simple case to examine is that of the single out-of-band signal. Here there is no AGC output even if the signal exceeds V_{WB}. There is no output because the ceramic filters prevent the out-of-band signal from getting to the input of the IF. With no signal at the IF input there is no meter output and SW1 is open, which means No AGC.

Figures 8 and 9 illustrate what happens at the tuner and AGC outputs when the strength of an in-band signal is varied in the presence of a strong out-of-band signal (i.e., greater than V_{WB}) which is held constant at the tuner input. For this example, the in-band signal at the tuner output will be referred to as V_D (desired signal), and the out-of-band signal as V_{UD} (undesired signal).

In *Figure 9*, we see that there is no AGC output until the tuner output exceeds the narrow band threshold, V_{NB}. At this point $V_m > 1V$ and SW1 closes. Further increase of the desired signal at the tuner input results in an AGC current that tries to hold the desired signal at the tuner output constant. This gain reduction of the tuner forces the undesired signal at the tuner output to fall. At the point that V_{UD} reaches the wide band threshold, no further gain reduction can occur as V_o would fall below V_{WB} (refer to *Figure 5*). At this point, control of the AGC shifts from the meter output (narrow band loop) to the out-of-band signal (wide band loop). Here V_{UD} is held constant along with the AGC

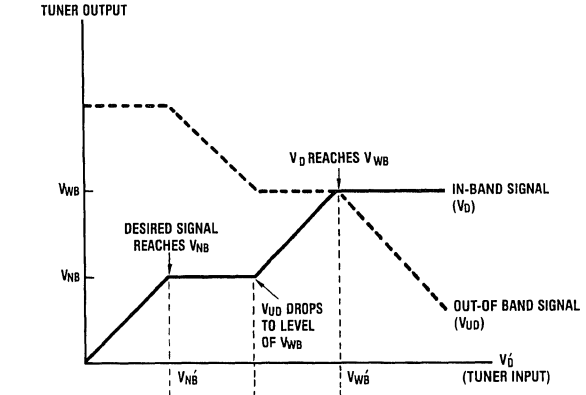
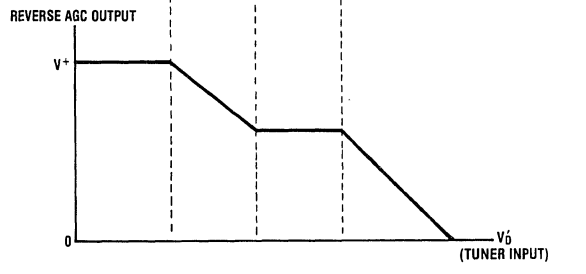


FIGURE 8



Prime indicates referenced to tuner input

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FIGURE 9

Application Notes (Continued)

voltage, while V_D is allowed to increase. V_D will increase until it reaches the level of the wide band threshold at the tuner output. When this occurs V_{UD} is no longer needed to keep $V_o > V_{WB}$ as V_D takes over the job. Thus V_{UD} will drop as the amount of AGC increases, while V_D is held constant by the AGC.

When compared to the simple case of a single in-band signal, we see that because of the presence of a strong out-of-band signal, AGC action has occurred earlier. For the simple case, AGC started when $V_D \geq V_{WB}$. For the two signal case above, AGC started when $V_D \geq V_{NB}$. Thus, the LM1865/LM1965/LM2065 achieves an early AGC when there are strong adjacent channels that might cause IM_3, and a later AGC when these signals aren't present.

For the range of signal levels that the tuner was gain-reduced and $V_D < V_{WB}$ there was loss in signal-to-noise in the recovered audio as compared to the case where there was no gain reduction in this interval. *Note, however, that the tuner is not desensitized by the AGC to weak desired stations below the narrow band threshold.*

NARROW BAND AGC THRESHOLD ADJUSTMENT

Both the narrow band and wide band AGC thresholds are user adjustable. This allows the user to optimize the AGC response to a given tuner. Referring to *Figure 5*, when the meter output exceeds 1V a comparator closes SW1. A simplified circuit diagram of this comparator is shown in *Figure 10*.

The 1K resistor in series with pin 8 allows for an upward adjustment of the narrow band threshold. This is accomplished by externally loading pin 8 with a resistor. *Figure 11* illustrates how this adjustment takes place.

From *Figure 11* it is apparent that loading the meter output not only moves the narrow band threshold, but also decreases the meter output for a given input.

In general one chooses the narrow band threshold based on what signal-to-noise compromise is considered acceptable.

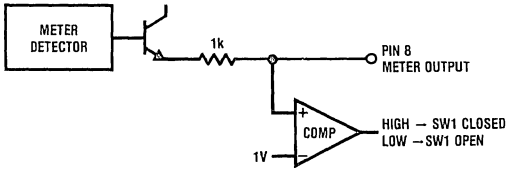

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FIGURE 10. Narrow Band Threshold Circuit

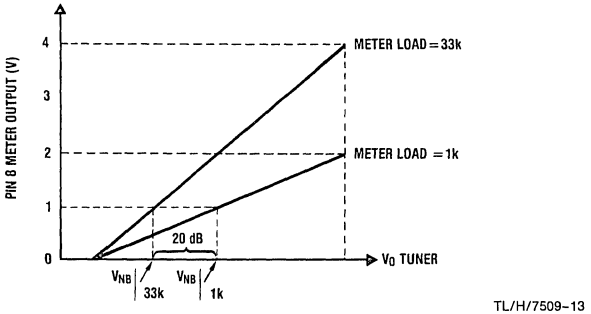

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FIGURE 11. Affect of Meter Load on Narrow Band Threshold

Application Notes (Continued)

WIDE BAND AGC THRESHOLD ADJUSTMENT

There are a number of criteria that determine where the wide band threshold should be set. If the threshold is set too high, protection against IM_3 will be lost. If the threshold is set too low, the front end, under certain input conditions, may be needlessly gain-reduced, sacrificing signal-to-noise performance. Ideally, the wide band threshold should be set to a level that will insure AGC operation whenever there are out-of-band signals strong enough to generate an IM_3 product of sufficient magnitude to exceed the narrow band threshold. Ideally, this level should be high enough to allow for a single in-band desired station to AGC the tuner, only after the maximum signal-to-noise has been achieved.

In order to insure that the wide band loop is activated whenever the IM_3 exceeds the narrow band threshold, V_{NB}, determine the minimum signal levels for two out-of-band signals necessary to produce an IM_3 equal to V_{NB}. Then, arrange for the wide band loop to be activated whenever the tuner output exceeds the rms sum of these signals. There are many combinations of two out-of-band signals that will produce an IM_3 of a given level. However, there is only one combination whose rms sum is a minimum at the tuner output. IM_3 at the tuner output is given according to the equation:

$$IM_3 = aV_{UD1}{}^2 V_{UD2} \text{ (assuming no gain reduction)} \quad (1)$$

where a = constant dependent on the tuner;

V_{UD1} = out-of-band signal 400 kHz from center frequency, applied to tuner input;

V_{UD2} = out-of-band signal 800 kHz from center frequency and 400 kHz away from V_{UD1}, applied to tuner input.

In general, due to tuned circuits within the tuner, the tuner gain is not constant with frequency. Thus, if the tuner is kept fixed at one frequency while the input frequency is changed, the output level will not remain constant. *Figure 12* illustrates this.

It can be shown that for a given IM_3, the combination of V_{UD1} and V_{UD2} that produces the smallest rms sum at the tuner output is given by the equations:

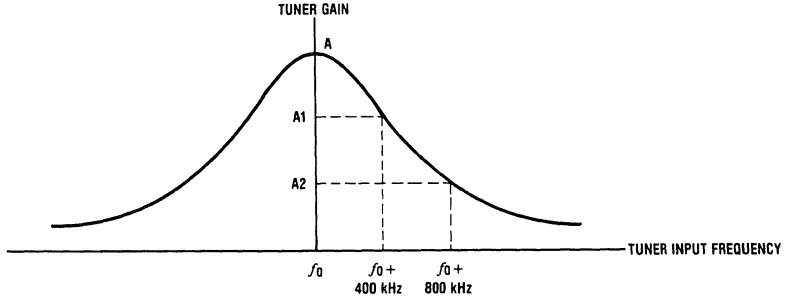
$$V_{UD1} = 1.12\left(\frac{A2}{A1}\frac{IM_3}{a}\right)^{1/3} \quad (2)$$

$$V_{UD2} = 0.794\left(\frac{A1^2}{A2^2}\frac{IM_3}{a}\right)^{1/3} \quad (3)$$

Therefore, in order to guarantee that the AGC will be keyed for an $IM_3 = V_{NB}$ we need only satisfy the condition:

$$V_{WB} \leq \sqrt{V_{NB}^2 + \left[(A1)(1.12)\left(\frac{A2}{A1}\frac{V_{NB}}{a}\right)^{1/3}\right]^2 + \left[A2\,(0.794)\left(\frac{A1^2}{A2^2}\frac{V_{NB}}{a}\right)^{1/3}\right]^2} \quad (4)$$

The right hand term of equation (4) defines an upper limit for V_{WB} called V_{WBUL}. V_{WBUL} is the rms sum of all the signals at the tuner output for two out-of-band signals, V_{UD1} and V_{UD2} [as expressed in equations (2) and (3)], applied to the tuner input.



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Define A = tuner gain at center frequency

A1 = tuner gain at f_0 + 400 kHz

A2 = tuner gain at f_0 + 800 kHz

FIGURE 12

Application Notes (Continued)

In order to make the calculation in equation (4), the constants a, A1, A2 must first be determined. This is done by the following procedure:

1. Connect together two RF generators and apply them to the tuner input. Since the generators will terminate each other, remove the 50Ω termination at the tuner input.
2. Connect a spectrum analyzer to the tuner output. Most spectrum analyzers have 50Ω input impedances. To make sure that this impedance does not load the tuner output use a FET probe connected to the spectrum analyzer. The tuner output should be terminated with a ceramic filter.
3. Disconnect the AGC line to the tuner. Make sure that the tuner is not gain-reduced.
4. Adjust the two RF generators for about 1 mV input and to frequencies 400 kHz and 800 kHz away from center frequency (*Figure 13*).
5. Note the three output levels in volts.
6. Knowing the tuner input levels for V_{UD1} and V_{UD2} and the resulting IM_3 just measured, "a" is calculated from the formula:

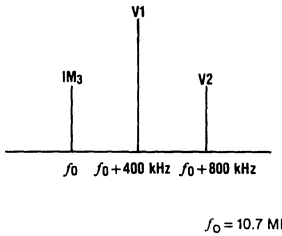
$$a = \frac{IM_3}{V_{UD1}^2 V_{UD2}} \quad (5)$$

where all levels are in volts rms. A typical value for "a" might be 2×10^6.

7. A1 and A2 are calculated according to the following formulas

$$A1 = \frac{V1}{V_{IN}\Big|_{f_0 + 400\ kHz}} \quad (6)$$

$$A2 = \frac{V2}{V_{IN}\Big|_{f_0 + 800\ kHz}} \quad (7)$$



TL/H/7509–15

FIGURE 13. Spectrum Analyzer Display of Tuner Output

If the wide band threshold was set to V_{WBUL}, then when a single in-band station reached the level V_{WBUL} at the tuner output, AGC action would start to take place. For this reason it is hoped that V_{WBUL} is above the level that will allow for maximum signal-to-noise. If, however, this is not the case, consideration might be given to improving the intermodulation performance of the tuner.

The lower limit for V_{WB} is the minimum tuner output that achieves the best possible signal-to-noise ratio in the recovered audio. In general, it is desirable to set V_{WB} closer to the upper limit rather than the lower limit. This is done to prevent AGC action within the narrow band loop except when there is a possibility of an IM_3 greater than V_{NB}.

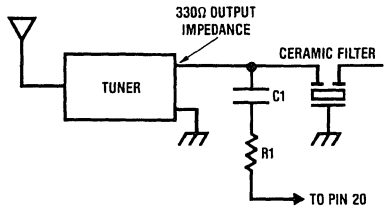
The wide band threshold at the pin 20 input to the LM1865/LM1965/LM2065 is fixed at 12 mVrms. Generally speaking, if pin 20 were driven directly from the tuner output. V_{WB} would be too low. Therefore, in general, pin 20 is not connected directly to the tuner output. Instead the tuner output is attenuated and then applied to pin 20. Increasing attenuation increases the wide band threshold, V_{WB}.

Pin 20 has an input impedance at 10.7 MHz that can be modeled as a 500Ω resistor in series with a 19 pF capacitor, giving a total impedance of 940Ω ∠−58°. Thus an easy way to attenuate the input to pin 20 is with the arrangement shown in *Figure 14*.

Notice that pin 20 must be AC coupled to the tuner output and that C1 is a bypass capacitor. R1 adjusts the amount of attenuation to pin 20. The wide band threshold will roughly increase by a factor of (R1 + 940Ω)/940Ω.

AGC CIRCUIT USED AS A CONVENTIONAL AGC

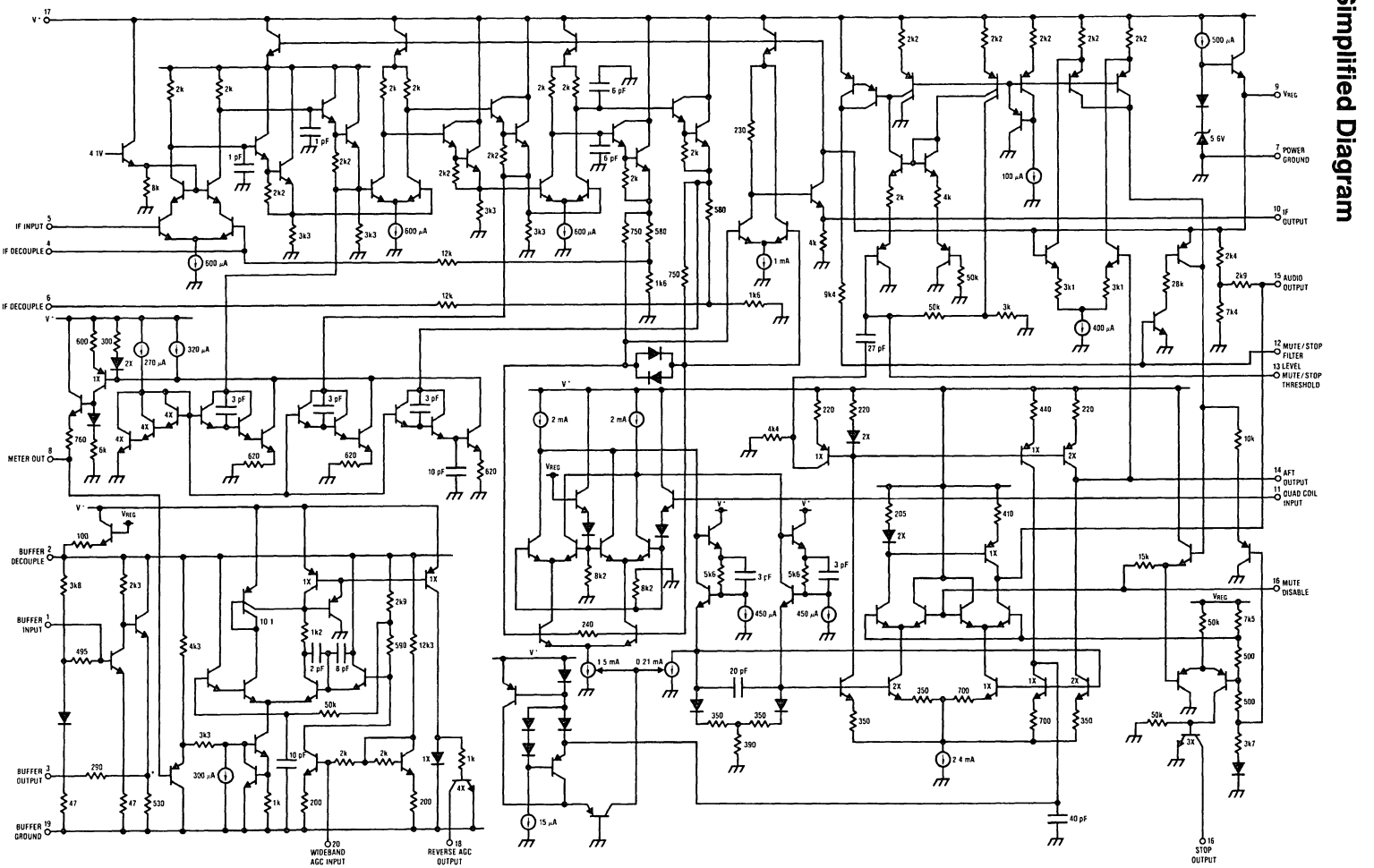
If for some reason the dual AGC thresholds are not desired, it is easy to use the LM1865/LM1965/LM2065 as a more conventional LM3189 type of AGC. This is accomplished by AC coupling the pin 20 input after the ceramic filters rather than before the filters. Thus, as with the LM3189, only in-band signals will be able to activate the AGC.



TL/H/7509–16

FIGURE 14. Wide Band Threshold Adjustment

Simplified Diagram



TL/H/7509–17

Advanced FM IF System

National Semiconductor Corporation

LM1866 Low Voltage AM/FM Receiver

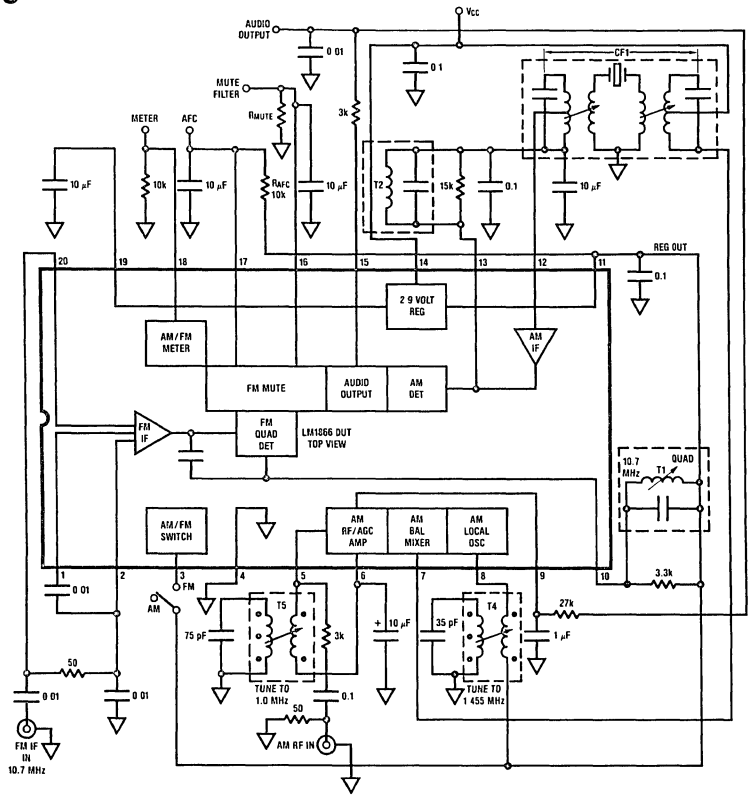
General Description

The LM1866 has been designed for high quality battery powered medium wave AM and FM receiver applications requiring operation down to 3V. The AM section contains a fully balanced, wide dynamic range, gain controlled mixer stage buffered from a single pin local oscillator. A two pin compound IF amplifier and internal detector provide a low distortion high level audio output. An AM/FM signal strength meter voltage is provided to a single output pin. The FM section contains a six stage limiting IF amplifier, quadrature detector, AFC output, deviation audio muting and noise operated audio muting. While designed for the high ripple, high battery impedance conditions found at the end of life for four "C" or "D" cells, the LM1866 will operate equally well at supply voltages up to 15V.

Features

- Operation from 3V to 5V
- Excellent power supply ripple rejection
- Fully balanced, wide dynamic range, AM mixer stage
- Internal AM detector for minimum tweet interference
- Single pole DC AM/FM mode switching
- Six stage FM IF limiting amplifier for excellent AM rejection
- "Soft" FM deviation and noise operated audio muting
- FM quadrature detector
- Single pin AM/FM meter output
- Single pin matched level AM/FM audio output

Block Diagram and Test Circuit



TL/H/7908–1

Order Number LM1866N
See NS Package Number N20A

Coil Data:
T2, Toko 159GC-A3785
CF1, Toko CFU-90D

T1, Toko KAC K2318HM
T4 = T5, Toko RBO6A5105

Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Pin 14)	15V
Package Dissipation (Note 1)	1900 mW
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Test Circuit, T_A = 25°C)

Parameter	Conditions	Min	Typ	Max	Units
STATIC DC CHARACTERISTICS: e_{IN} = 0, R_{MUTE} = 0Ω, V_{CC} = 6V					
Operating Supply Range, V14		3	6	15	V
Supply Current, I_{14}	AM Mode		15	27	mA
Supply Current, I_{14}	FM Mode		16	24	mA
Regulator Output Voltage, V11			2.9		V
Meter Output Voltage, V18	AM Mode		0	0.2	V
Meter Output Voltage, V18	FM Mode		0	0.2	V
AFC Output Voltage, V17	FM Mode		2.9		V
AM/FM Audio Output Resistance, R_O15			3		kΩ
AM DYNAMIC CHARACTERISTICS: f_{AM} = 1 MHz, f_{MOD} = 1 kHz, m = 0.3, V_{CC} = 6V					
Maximum Sensitivity	e_{AM} for e_o = 6 mV		9		μV
20 dB Quieting Sensitivity	e_{AM} for e_o = 20 dB S/N		25		μV
Signal to Noise Ratio	e_{AM} = 10 mV	40	50		dB
Total Harmonic Distortion	e_{AM} = 10 mV		0.3		%
Total Harmonic Distortion	e_{AM} = 10 mV, m = 0.8		1	2	%
Audio Output Level	e_{AM} = 10 mV	70	120		mV
Overload Distortion	e_{AM} = 50 mV, m = 0.8		2	12	%
Meter Output Voltage	e_{AM} = 1 mV		2.0	3.0	V
Meter Output Voltage	e_{AM} = 50 mV		3.0	3.5	V
FM DYNAMIC CHARACTERISTICS: f_{FM} = 10.7 MHz, f_{MOD} = 400 Hz, Δf = ±75 kHz, V_{CC} = 6V					
−3 dB Limiting Sensitivity	e_{FM} for −3 dB Limiting Sensitivity		20	35	μV
Signal to Noise Ratio	e_{FM} = 10 mV	60	76		dB
AM Rejection	e_{FM} = 10 mV, 30% AM Mod	40	55		dB
Total Harmonic Distortion	e_{FM} = 10 mV		0.5	1	%
Audio Output Level	e_{FM} = 10 mV, 30% FM Mod	60	120		mV
Meter Output Level	e_{FM} = 1 mV		1.3	2.3	V
Meter Output Level	e_{FM} = 50 mV		2.0	2.8	V
± Deviation Mute (Notes 2, 4)	e_{FM} = 10 mV, R_{AFC} = 10k		40		kHz
R_{MUTE} for Noise Mute (Notes 3, 4)	Set e_{FM} for −3 dB Limiting Sensitivity	2	5	10	kΩ
Max Audio Mute Attenuation		60	75		dB

Note 1: Above T_A = 25°C, derate based on $T_{J(max)}$ = 150°C and θ_{JA} = 65°C/W.

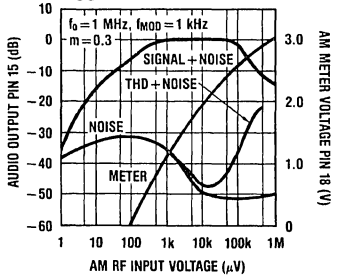
Note 2: R_{MUTE} = 2 kΩ, e_{FM} = 10 mV, adjust center frequency for V_{AFC} = V_{REG}, record f_{FM}, adjust ± f_{FM} for >50 dB audio mute attenuation.

Note 3: Adjust R_{MUTE} from 2k to 10k for >50 dB audio mute attenuation. Set e_{FM} = 10 mV and check for mute off.

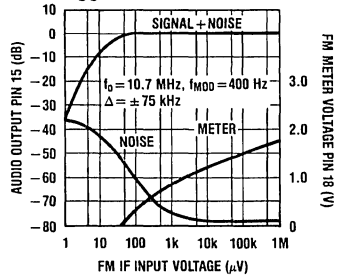
Note 4: When R_{MUTE} = 0Ω, the deviation and noise operated mute functions are disabled. When R_{MUTE} = 2 kΩ, only the noise mute function is disabled. The deviation mute bandwidth is set by the R_{AFC} resistor. The noise mute threshold is set by the R_{MUTE} resistor. Test circuit noise bandwidth characteristics prevent noise mute operation for IF input levels below the −3 dB limiting threshold. When the FM IF is used with a tuner, full noise mute capability is accessible (See Applications Information).

Typical Performance Characteristics (Test Circuit)

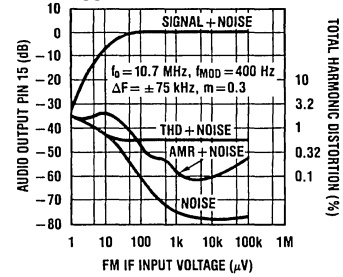
AM Characteristics
V_{CC} = 6V



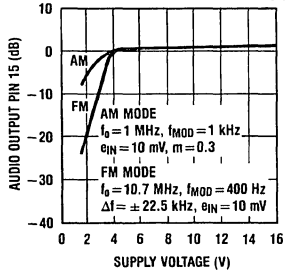
FM IF Characteristics
V_{CC} = 6V



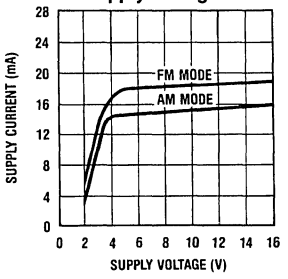
FM IF Characteristics
V_{CC} = 6V



Recovered Audio vs Supply



Quiescent Supply Current vs Supply Voltage



TL/H/7908–2

Applications Information

(See Typical Applications and LM1866 Schematic Diagram)

VOLTAGE REGULATOR SECTION

Because of the wide supply voltage range and high ripple conditions expected in battery or low cost transformer supplies, the LM1866 uses a band gap referenced active voltage regulator which is externally compensated at pin 19. This capacitor, when made large enough, improves the supply rejection and decreases the noise bandwidth to a level well below the AM reception frequencies. A 0.1 μF capacitor will compensate the regulator for low noise operation while 50 μF (max) will improve supply rejection and the maximum FM audio mute attenuation characteristics. During power turn on, the pin 19 capacitor is quick-charged to its normal operating voltage so that the AM or FM sections are in operation before the audio amplifier turn on delay has timed out. See LM1895/LM2895 and LM1896/LM2896 data sheets for additional audio amplifier information.

AM SECTION

The AM section contains a fully balanced mixer stage with the RF input applied to a differential, diode degenerated, transistor pair at pins 5 and 6. DC feedback is provided by the loopstick secondary winding. The mixer output 1st IF transformer at pin 7 should be returned to V_{CC} at pin 14 to allow maximum undistorted output swing when tuning between stations. RF and AGC decoupling at pin 6 removes noise and lowers audio distortion.

The mixer upper pairs are switched differentially by a buffer amplifier from the pin 8 local oscillator. DC feedback is provided by the oscillator coil secondary winding to the pin 11 regulator voltage.

The oscillator frequency is given by:

$$f_O = \frac{0.159}{\sqrt{LC}},$$

and the peak swing is given by: $V_P = IZ$ (I = 700 μA, Z = tank impedance at resonance). V_P should be between 0.3V and 0.5V to maintain an undistorted output at low supplies.

The two stage AM IF amplifier at pins 12 and 13 requires output to input DC feedback and external decoupling. The IF gain is given by:

$$A_V = \frac{Z_L}{12}$$

Applications Information (Continued)

where Z_L equals resonant unloaded tank impedance in parallel with R_{EXT}. In most applications Z_L = 10k and

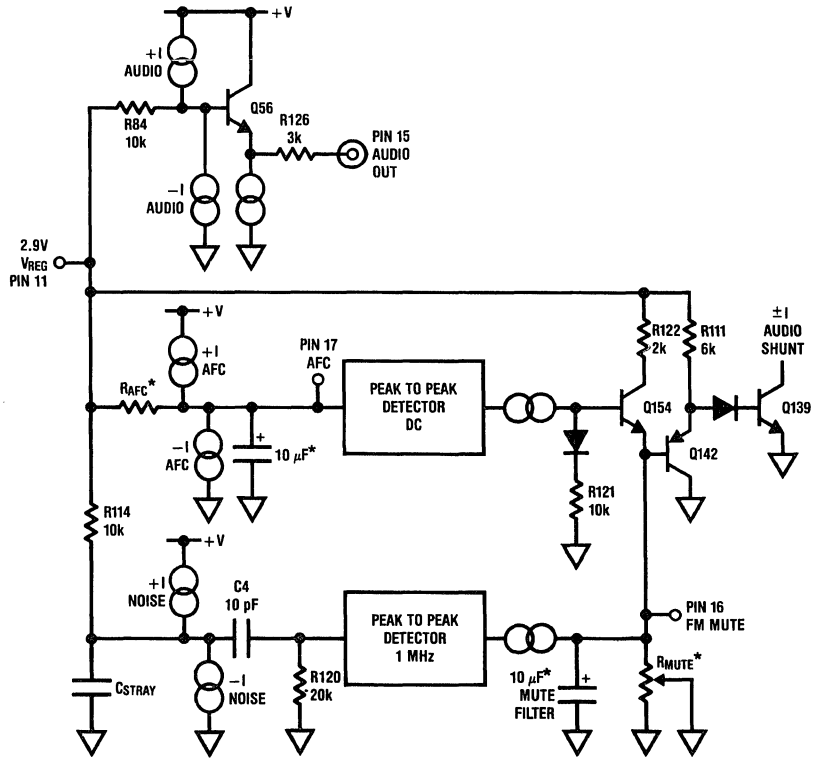
$$Q_L = \frac{Z_L}{X_C} = 5$$

where R_{EXT} = an external IF gain setting resistor and X_C = impedance of tank tuning capacitor. A rule of thumb for setting the IF gain would be to adjust R_{EXT} for 20 dB audio S/N when the audio has dropped 10 dB below the level found at the AGC threshold. (Because of the low Q_L, a non-tuned coil is acceptable.)

The output of the IF amplifier drives an internal detector which is operating at low currents. This results in very low 2nd and 3rd IF harmonic radiation for minimal tweet interference.

FM SECTION

The FM section contains a six stage limiting amplifier, quadrature detector, AFC output, deviation mute detector and a high frequency noise mute detector. (See *Figure 1* for the Simplified Mute Circuit Schematic.) The output of the quadrature detector is split into three current source pairs. The ± audio current and internal load resistor R84 provide the audio output voltage via Q56 to pin 15. The ± AFC current, external load resistor (R_{AFC}) and the 10 μF capacitor provide an audio decoupled AFC voltage to pin 17. The ± noise current and internal load resistor R114 provide a wideband detector output that is limited in frequency by C_{STRAY}. With the addition of internal C4 and R120 a band pass filter ($f_o \cong$ 1 MHz) is realized at the input of the peak to peak detector. The output current, flowing in resistor R_{MUTE} and filtered by a capacitor, provides a mute voltage at pin 16. When the mute voltage rises to approximately one V_{BE}, transistor Q139 will start to shunt the ± audio current away from R84, muting the audio output. The value of the R_{MUTE} resistor will determine the minimum audio signal to noise ratio at which one wishes to mute. The deviation mute detector will output a current only when the AFC voltage is offset above or below the V_{REG} voltage. Load resistor R121 and transistor Q154 will convert this current to a mute voltage at pin 16. This is done to prevent interaction between the two detector output currents. The external R_{AFC} resistor is used to set the deviation mute bandwidth so that the pin 16 mute voltage is one V_{BE} at the desired frequency band edge. When disabling the mute functions, pin 16 is shorted to ground, preventing Q139 from becoming active.



TL/H/7908–3

*External component

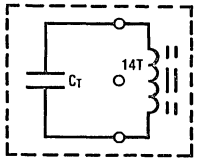
FIGURE 1. Simplified Mute Circuit Schematic

Applications Information (Continued)

TABLE I. Typical Application External Coil and Component Selection Guide

Component	Typical Value	Purpose
C1A, B, C, D	—	AM/FM tuning capacitor
R1, C2, C3	330Ω, 0.01 μF	FM IF decoupling, filter match and DC feedback
C4	1 μF–10 μF	AM/RF/AGC decoupling
R5, C5	27k, 1 μF	Sets AM AGC time constant
R6	120k–150k	Optional: decreases AM audio output but improves AM meter threshold
C6	0.1 μF	Regulator output decoupling
C7, C8	0.1 μF, 10 μF	AM IF/audio decoupling
R4 (R_{EXT})	15k	Sets AM IF gain
R7, C15, C14	10Ω, 0.1 μF, 100 μF	Supply decoupling
R3, C10	3k, 0.01 μF	Sets FM de-emphasis/AM smoothing Audio post filter pole is given by: $f = \frac{0.159}{R_T C10'}$ when $R_T = R3 + R_o15 = R3 + 3\ k\Omega$
R_{MUTE}, C11	0 to 10k, 10 μF	Sets noise mute threshold, filter. 0Ω will turn off mute function.
R_{AFC}, C12	10k, 10 μF	Sets deviation mute bandwidth, audio decoupling
C13	10 μF	Regulator decoupling and supply rejection filter

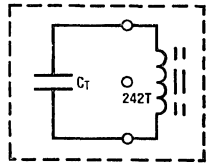
T1



TL/H/7908–4

C_T = 82 pF
Qu ≥ 70
f = 10.7 MHz
Part no. KAC K2318HM Toko

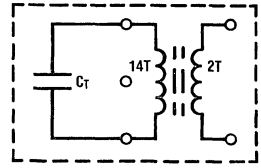
T2



TL/H/7908–5

C_T = 180 pF
Qu = 14
f = 455 MHz
Part no. 159GC-A3785 Toko

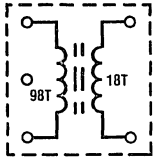
T3



TL/H/7908–6

C_T = 50 pF
Qu = 80
f = 10.7 MHz
Part no. NS-107C
Apollo Electronics Corp.

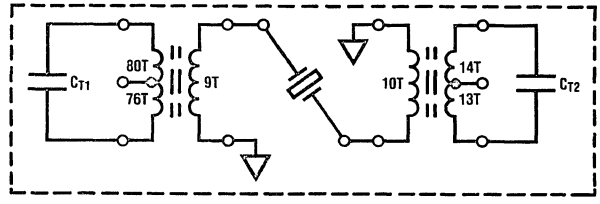
T4 and T5 MW Oscillator Coil



TL/H/7908–7

L = 360 μH
f = 796 kHz
Qu = 160
Tuning freq. = 985 kHz–2105 kHz
Part no. RBO6A5105 Toko

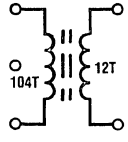
CF1



TL/H/7908–8

Toko CFU-090D or equivalent
f = 455 kHz, BW > 4.8 kHz

MW Antenna Coil

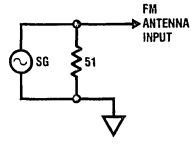


TL/H/7908–9

L = 650 μH
f = 796 kHz
Qu = 200
Tuning freq. = 530 kHz–1650 kHz

L7 SWG #20, N = 3 1/2T, ID = 5 mm
L5 SWG #20, N = 3 1/2T, ID = 5 mm
L6 L = 0.44 μH, N = 4 1/2T, Qu = 70

Dummy Antenna for FM



TL/H/7908–10

Variable Tuning Capacitor
Type: QT-22124 Toko
Capacitance: AM C1A 4 pF–142 pF, C1B 4–60 pF
FM 2.5 pF–20 pF C1C, C1D

AM Performance (525 kHz–1650 kHz)

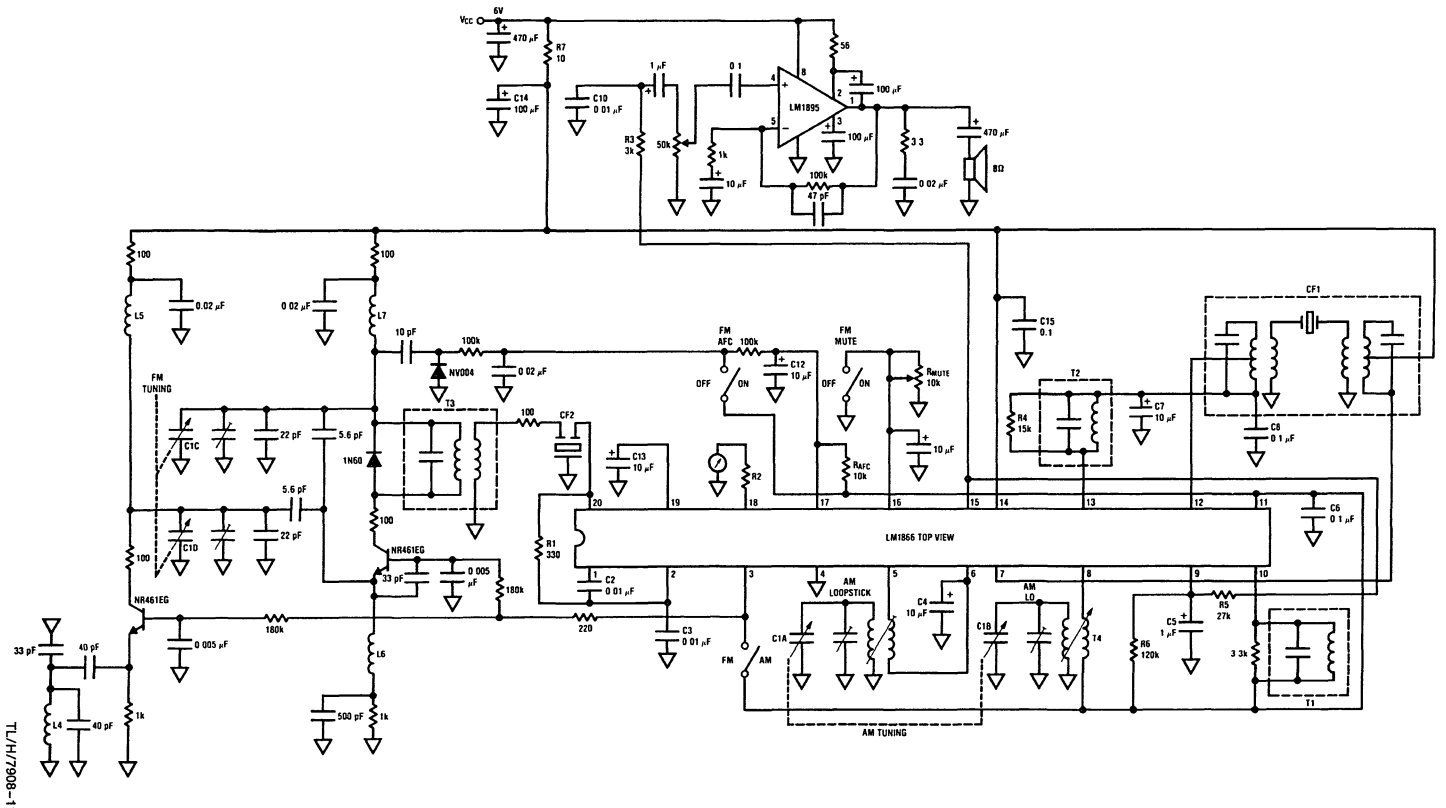
- Maximum sensitivity: 100 μV/m
- 20 dB quieting sensitivity: 250 μV/m
- Tweet* worst case: 5%
  100 mV/m: 1.5%

FM Performance (88 MHz–108 MHz)

- 30 dB quieting sensitivity: 3.5 μV
- −3 dB limiting sensitivity: 7 μV

See Table I for coil and numbered component data.

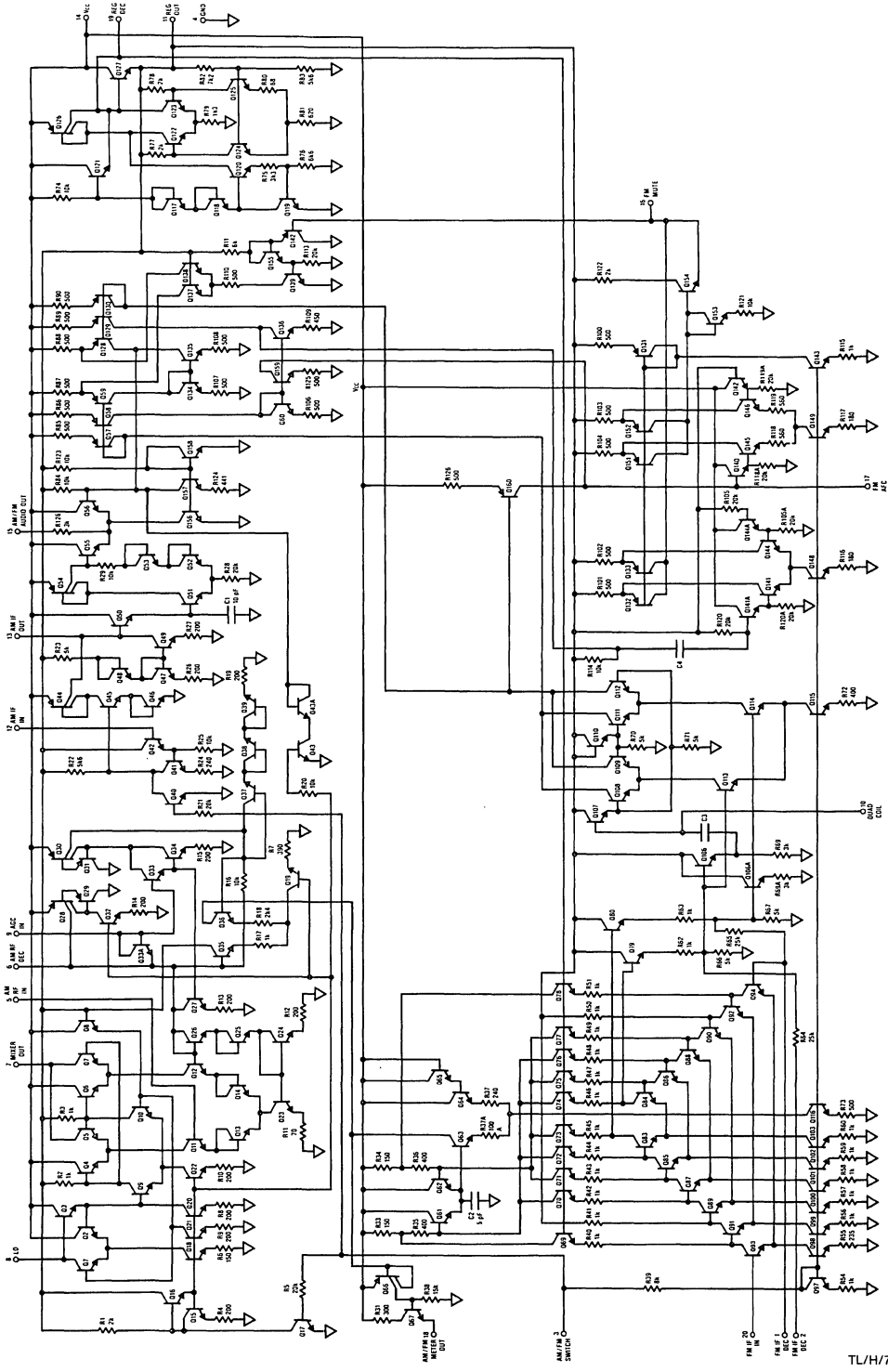
See LM1895/LM2895 data sheet for audio amp info.



*Tweet is an audio tone produced by the 2nd and 3rd harmonic of the IF beating against the received signal. It is measured as an equivalent modulation level: i.e., a 30% tweet has the same amplitude at the detector as a desired signal with 30% modulation.

FIGURE 2. Typical AM/FM Radio Application

Equivalent Schematic Diagram



TL/H/7908–12

National Semiconductor Corporation

LM1868 AM/FM Radio System

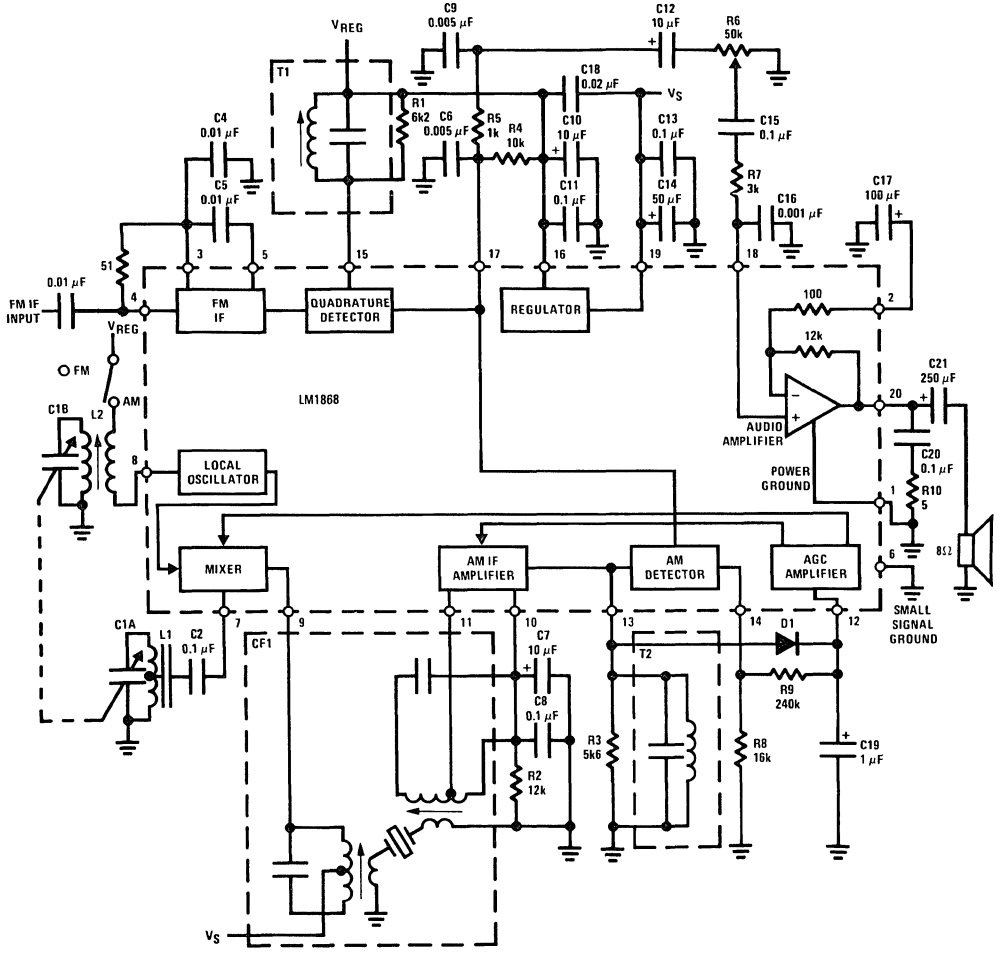
General Description

The combination of the LM1868 and an FM tuner will provide all the necessary functions for a 0.5 watt AM/FM radio. Included in the LM 1868 are the audio power amplifier, FM IF and detector, and the AM converter, IF, and detector. The device is suitable for both line operated and 9V battery applications.

Features

- DC selection of AM/FM mode
- Regulated supply
- Audio amplifier bandwidth decreased in AM mode, reducing amplifier noise in the AM band
- AM converter AGC for excellent overload characteristics
- Low current internal AM detector for low tweet radiation

Block Diagram



TL/H/7909–1

Order Number LM1868N
See NS Package Number N20A

Note: See table for coil data

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Pin 19) 15V

Package Dissipation 2.0W
Above T_A = 25°C, Derate Based on
$T_{J(MAX)}$ = 150°C and θ_{JA} = 60°C/W

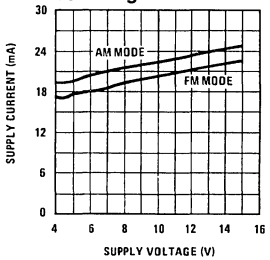
Storage Temperature Range −55°C to +150°C
Operating Temperature Range 0°C to +70°C
Lead Temperature (Soldering, 10 sec.) 260°C

Electrical Characteristics Test Circuit, T_A = 25°C, V_S = 9V, R_L = 8Ω (unless otherwise noted)

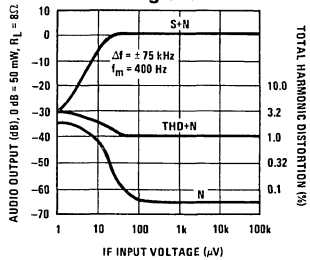
Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS e_{AM} = 0, e_{FM} = 0					
Supply Current	AM Mode, S1 in Position 1		22	30	mA
Regulator Output Voltage (Pin 16)		3.5	3.9	4.8	V
Operating Voltage Range		4.5		15	
DYNAMIC CHARACTERISTICS—AM MODE f_{AM} = 1 MHz, f_{mod} = 1 kHz, 30% Modulation, S1 in Position 1, P_O = 50 mW unless noted					
Maximum Sensitivity	Measure e_{AM} for P_O = 50 mW, Maximum Volume	8		16	μV
Signal-to-Noise	e_{AM} = 10 mV	40	50		dB
Detector Output	e_{AM} = 1 mV Measure at Top of Volume Control	40	60	85	mV
Overload Distortion	e_{AM} = 50 mV, 80% Modulation		2	10	%
Total Harmonic Distortion (THD)	e_{AM} = 10 mV		1.1	2	%
DYNAMIC CHARACTERISTICS—FM MODE f_{FM} = 10.7 MHz, f_{mod} = 400 Hz, Δf = ±75 kHz, P_O = 50 mW, S1 in Position 1					
−3 dB Limiting Sensitivity			15	45	μV
Signal-to-Noise Ratio	e_{FM} = 10 mV	50	64		dB
Detector Output	e_{FM} = 10 mV, Δf = ±22.5 kHz Measure at Top of Volume Control	40	60	85	mV
AM Rejection	e_{FM} = 10 mV, 30% AM Modulation	40	50		dB
Total Harmonic Distortion (THD)	e_{FM} = 10 mV		1.1	2	%
DYNAMIC CHARACTERISTICS—AUDIO AMPLIFIER ONLY f = 1 kHz, e_{AM} = 0, e_{FM} = 0, S1 in Position 2					
Power Output	THD = 10%, R_L 8Ω V_S = 6V V_S = 9V	 250 500	 325 700		 mW mW
Bandwidth	AM Mode, P_O = 50 mW FM Mode, P_O = 50 mW		11 22		kHz kHz
Total Harmonic Distortion (THD)	P_O = 50 mW, FM Mode		0.2		%
Voltage Gain			41		dB

Typical Performance Characteristics (Test Circuit) All curves are measured at audio output

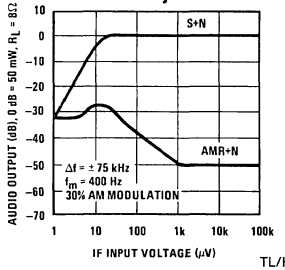
Quiescent Supply Current vs Voltage



FM Limiting Characteristics



FM IF AM Rejection

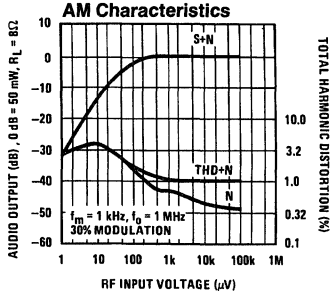


TL/H/7909–2

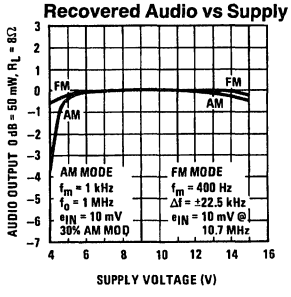
Typical Performance Characteristics (Continued)

All curves are measured at audio output (Test Circuit)

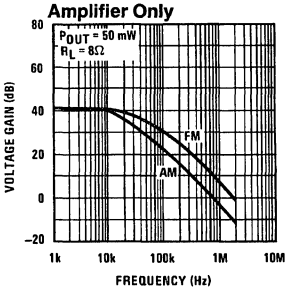
AM Characteristics



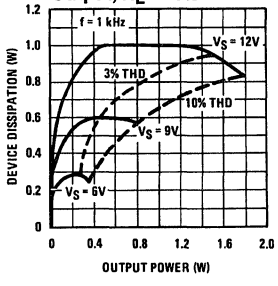
Recovered Audio vs Supply



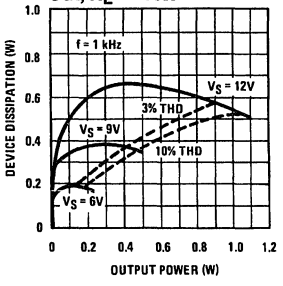
Gain vs Frequency Audio Amplifier Only



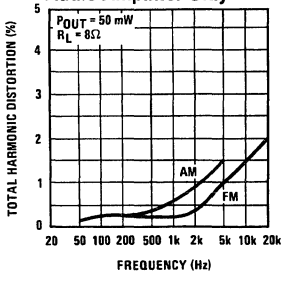
Power Dissipation vs Power Output, R_L = 8Ω



Power Dissipation vs Power Out, R_L = 16Ω

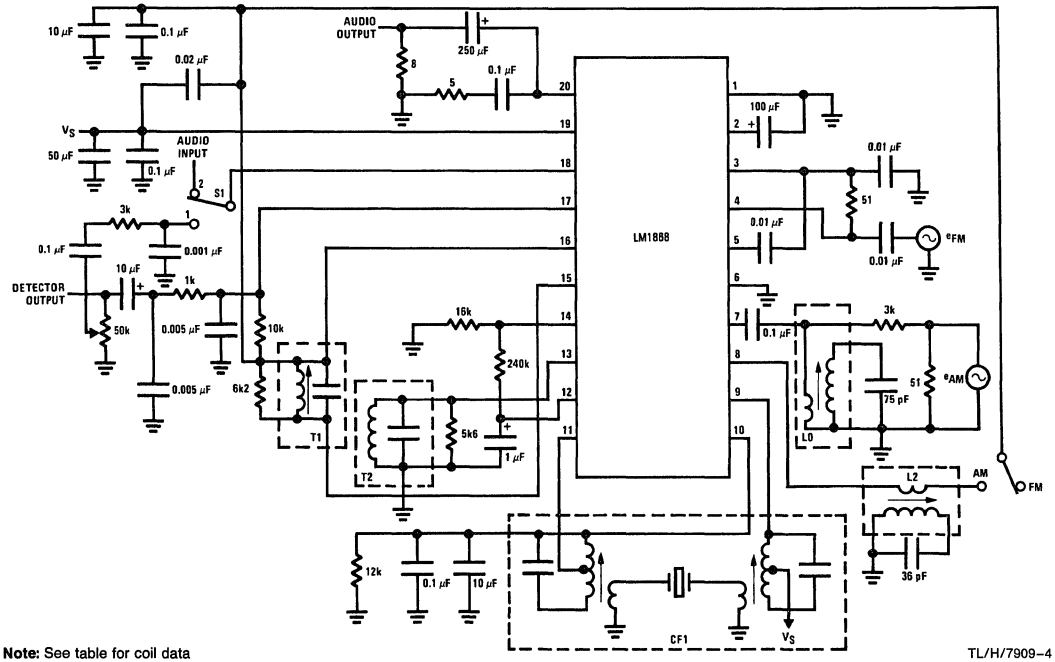


Distortion vs Frequency Audio Amplifier Only



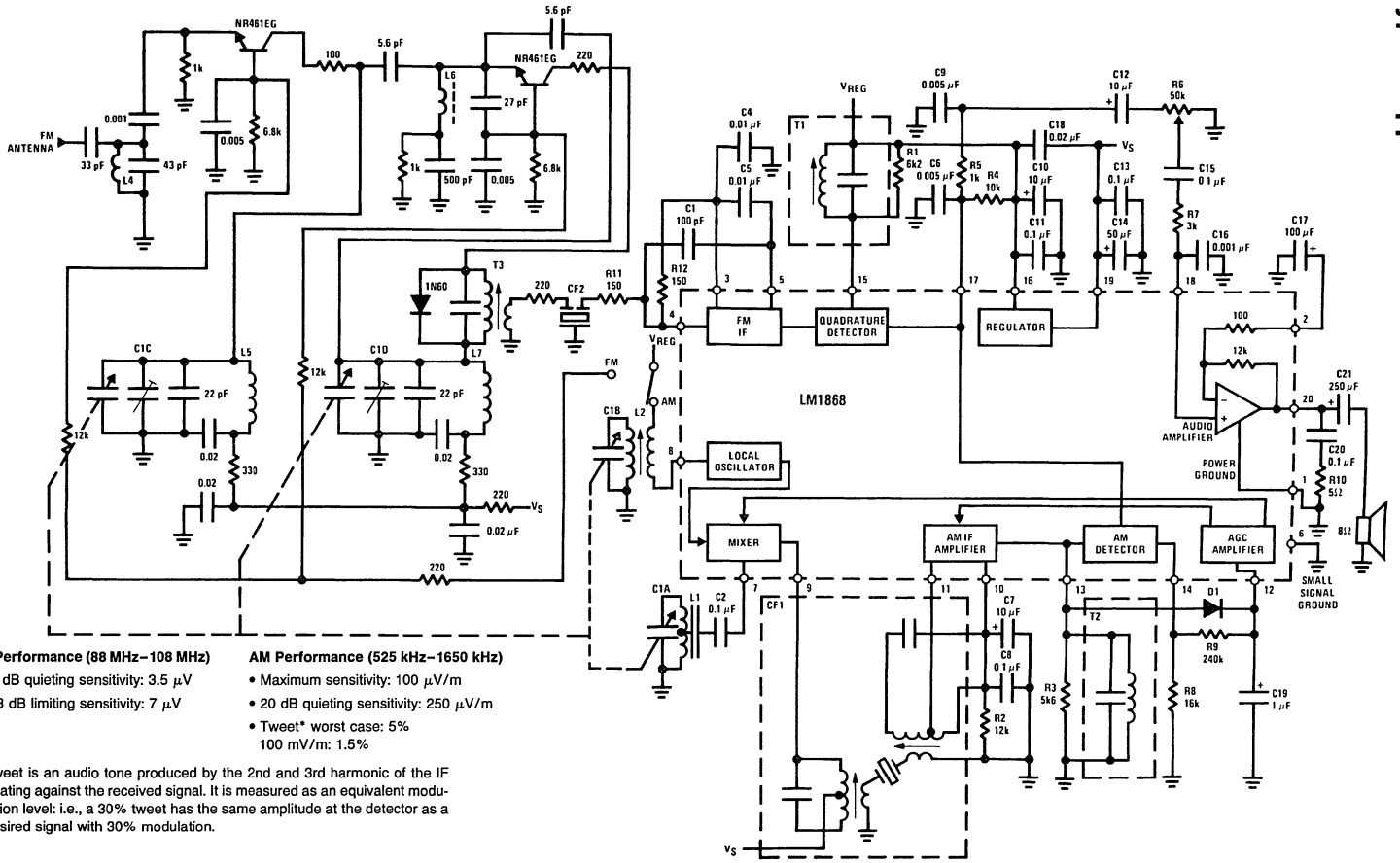
TL/H/7909–3

Test Circuit



Note: See table for coil data

TL/H/7909–4



FM Performance (88 MHz–108 MHz)

- 30 dB quieting sensitivity: 3.5 μV
- −3 dB limiting sensitivity: 7 μV

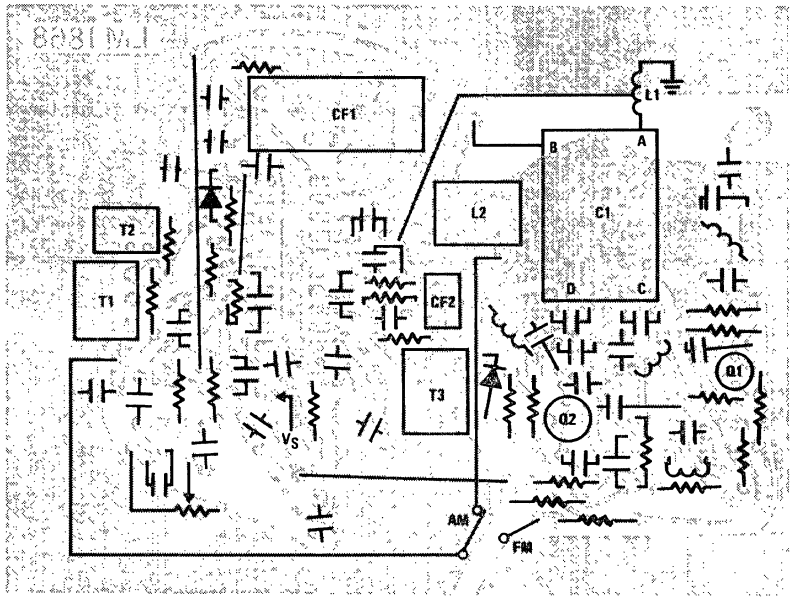
AM Performance (525 kHz–1650 kHz)

- Maximum sensitivity: 100 μV/m
- 20 dB quieting sensitivity: 250 μV/m
- Tweet* worst case: 5%
  100 mV/m: 1.5%

*Tweet is an audio tone produced by the 2nd and 3rd harmonic of the IF beating against the received signal. It is measured as an equivalent modulation level: i.e., a 30% tweet has the same amplitude at the detector as a desired signal with 30% modulation.

TL/H/7909–5

PC Board Layout

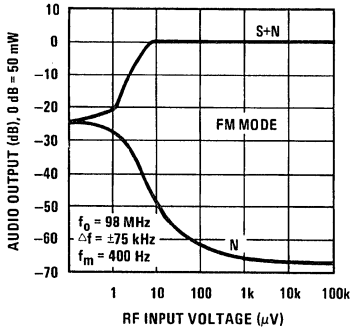


TL/H/7909–6

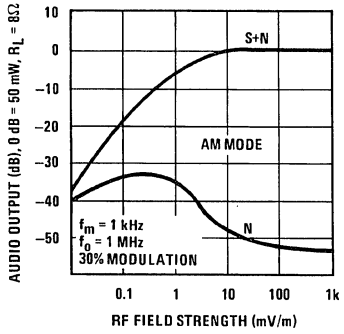
Component Side

Typical Performance Characteristics Typical Application

All curves are measured at audio output



TL/H/7909–7



TL/H/7909–8

IC External Components (Application Circuit)

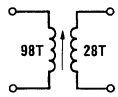
Component	Typical Value	Comments
C1	100 pF	Removes tuner LO from IF input
C2	0.1 μF	Antenna coupling capacitor
C4, C5	0.01 μF	FM IF decoupling capacitors
C6, C9	0.005 μF	AM smoothing/FM de-emphasis network, de-emphasis pole is given by. $f1 \cong \frac{1}{2\pi\,(C6 + C9)\left(\frac{R4\ \ R6}{R4 + R6}\right)}$
R5	1k	
C10	10 μF	Regulator decoupling capacitor
C11	0.1 μF	Regulator decoupling capacitor
C12	10μF	AC coupling to volume control
C13	0.1 μF	Power supply decoupling
C14	50 μF	Power supply decoupling
C15	0.1 μF	Audio amplifier input coupling
R7	3k	Roll off signals from detector in the AM band to prevent radiation
C16	0.001 μF	
C17	100 μF	Power amplifier feedback decoupling, sets low frequency supply rejection
R8	16k	AM detector bias resistor
R9	240k	Set AGC time constant
C19	1 μF	
C7	10 μF	IF coupling
C8	0.1 μF	IF coupling
C20	0.1 μF	High frequency load for audio amplifier, required to stabilize audio amplifier
R10	5Ω	
C21	250 μF	Output coupling capacitor
R1	6k2	Sets Q of quadrature coil, determining FM THD and recovered audio
R2	12k	IF amplifier bias R
R3	5k6	Sets gain of AM IF and Q of AM IF output tank
R4	10k	Detector load resistor
R6	50k	Volume control
C18	0.02 μF	Power supply decoupling
R11, R12	150Ω	Terminates the ceramic filter, biases FM IF input stage
D1	1N4148	Optional. Quickens the AGC response during turn on

Coil and Tuning Capacitor Specifications

C1 AM ANT 140 pF max 5.0 pF min
AM OSC 82 pF max 5.0 pF min
Trimmers 5 pF
FM 20 pF max 4.5 pF min
TOKO CY2-22124PT

L1 640 μH, Q_u = 200
R_P = 3k5 @ F = 796 kHz
(At secondary)
AM antenna
1 mV/meter induces approximately 100 μV open circuit at the secondary

L0, L2 360 μH, Q_U > 80 @ F= 796 kHz
TOKO RWO-6A5105 or equivalent



TL/H/7909–9

Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

L4 SWG #20, N = 3½T, inner diameter = 5 mm

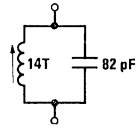
L5 SWG #20, N = 3½T, inner diameter = 5 mm

L6 L = 0.44 μH, N = 4 ½T, Qu = 70

L7 SWG #20, N = 2 ½T, inner diameter = 5 mm

CF2 10.7 MHz ceramic filter
MURATA SFE 10.7 mA or equivalent
Murata
2200 Lake Park Drive
Smyrna, GA 30080
(404) 436-1300

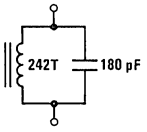
T1



TL/H/7909–10

Q_u > 70 @ 10.7 MHz, L to resonate w/82 pF @ 10.7 MHz
TOKO KAC-K2318 or equivalent

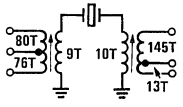
T2



TL/H/7909–11

Q_u > 14 @ 455 kHz, L to resonate w/180 pF @ 455 kHz
TOKO 159GC-A3785 or equivalent

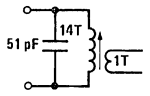
CF1



TL/H/7909–12

TOKO CFU-090D or equivalent
BW > 4.8 kHz @ 455 kHz

T3



TL/H/7909–13

Apollo Electronics NS-107C or equivalent

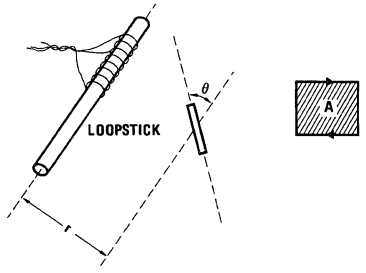
Layout Considerations

AM SECTION

Most problems in an AM radio design are associated with radiation of undesired signals to the loopstick. Depending on the source, this radiation can cause a variety of problems including tweet, poor signal-to-noise, and low frequency oscillation (motor boating). Although the level of radiation from the LM1868 is low, the overall radio performance can be degraded by improper PCB layout. Listed below are layout considerations association with common problems.

1. **Tweet:** Locate the loopstick as far as possible from detector components C6, C9, R4, and R5. Orient C6, C9, R4, and R5 parallel to the axis of the loopstick. Return R8, C6, C9, and C19 to a separate ground run (see Typical Application PCB).

2. **Poor Signal-to-Noise/Low Frequency Oscillation:** Twist speaker leads. Orient R10 and C20 parallel to the axis of the loopstick. Locate C11 away from the loopstick.



TL/H/7909–14

In general, radiation results from current flowing in a loop. In case 1 this current loop results from decoupling detector harmonics at pin 17; while in case 2, the current loop results from decoupling noise at the output of the audio amplifier and the output of the regulator. The level of radiation picked up by the loopstick is approximately proportional to: 1) $1/r^3$; where r is the distance from the center of the loopstick to the center of the current loop; 2) SIN θ, where θ is the angle between the plane of the current loop and the axis of the loopstick; 3) I, the current flowing in the loop; and 4) A, the cross-sectional area of the current loop.

Pickup is kept low by short leads (low A), proper orientation ($\theta \cong 0$ so SIN $\theta \cong 0$), maximizing distance from sources to loopstick, and keeping current levels low.

FM SECTION

The pinout of the LM1868 has been chosen to minimize layout problems, however some care in layout is required to insure stability. The input source ground should return to C4 ground. Capacitors C13 and C18 form the return path for signal currents flowing in the quadrature coil. They should connect directly to the proper pins with short PC traces (see Typical Application PCB). The quadrature coil and input circuitry should be separated from each other as far as possible.

AUDIO AMPLIFIER

The standard layout considerations for audio amplifiers apply to the LM1868, that is: positive and negative inputs should be returned to the same ground point, and leads to the high frequency load should be kept short. In the case of the LM1868 this means returning the volume control ground (R6) to the same ground point as C17, and keeping the leads to C20 and R10 short.

Circuit Description (See Equivalent Schematic)

AM SECTION

The AM section consists of a mixer stage, a separate local oscillator, an IF gain block, an envelope detector, AGC circuits for controlling the IF and mixer gains, and a switching circuit which disables the AM section in the FM mode.

Signals from the antenna are AC-coupled into pin 7, the mixer input. This stage consists of a common-emitter amplifier driving a differential amp which is switched by the local oscillator. With no mixer AGC, the current in the mixer is 330 μA; as the AGC is applied, the mixer current drops, decreasing the gain, and also the input impedance drops, reducing the signal at the input. The differential amp connected to pin 8 forms the local oscillator. Bias resistors are arranged to present a negative impedance at pin 8. The frequency of oscillation is determined by the tank circuit, the peak-to-peak amplitude is approximately 300 μA times the impedance at pin 8 in parallel with 8k2.

After passing through the ceramic filter, the IF signals are applied to the IF input. Signals at pin 11 are amplified by two AGC controlled common-emitter stages and then applied to the PNP output stage connected to pin 13. Biasing is arranged so that the current in the first two stages is set by the difference between a 250 μA current source and the Darlington device connected to pin 12.

When the AGC threshold is exceeded, the Darlington device turns ON, steering current away from the IF into ground, reducing the IF gain. Current in the IF is monitored by the mixer AGC circuit. When the current in the IF has dropped to 30 μA, corresponding to 30 dB gain reduction in the IF, the mixer AGC line begins to draw current. This causes the mixer current and input impedance to drop, as previously described.

The IF output is level shifted and then peak detected at detector cap C1. By loading C1 with only the base current of the following device, detector currents are kept low. Drive from the AGC is taken at pin 14, while the AM detector output is summed with the FM detector output at pin 17.

FM SECTION

The FM section is composed of a 6-stage limiting IF driving a quadrature detector. The IF stages are identical with the exceptions of the input stage, which is run at higher current to reduce noise, and the last stage, which is switched OFF in the AM mode. The quadrature detector collectors drive a level shift arrangement which allows the detector output load to be connected to the regulated supply.

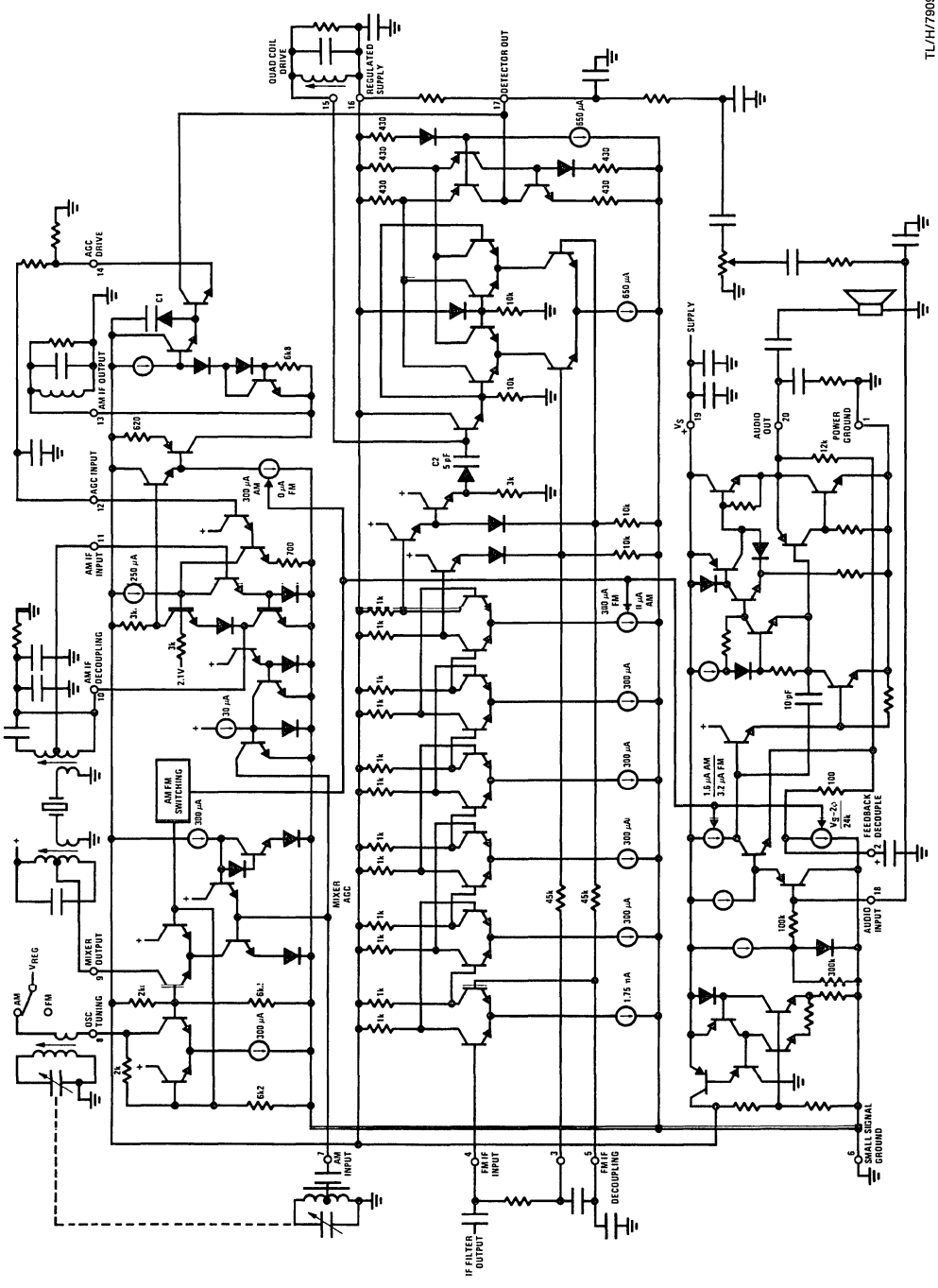
AUDIO AMPLIFIER

The audio amplifier has an internally set voltage gain of 120. The bandwidth of the audio amplifier is reduced in the AM mode so as to reduce the output noise falling in the AM band. The bandwidth reduction is accomplished by reducing the current in the input stage.

REGULATOR

A series pass regulator provides biasing for the AM and FM sections. Use of a PNP pass device allows the supply to drop to within a few hundred millivolts of the regulator output and still be in regulation.

Equivalent Schematic



TL/H/7909–15

National Semiconductor Corporation

LM1870 Stereo Demodulator with Blend

General Description

The LM1870 is a phase locked loop FM stereo demodulator with a DC control pin for reducing noise by decreasing separation during weak signal conditions.

Applications

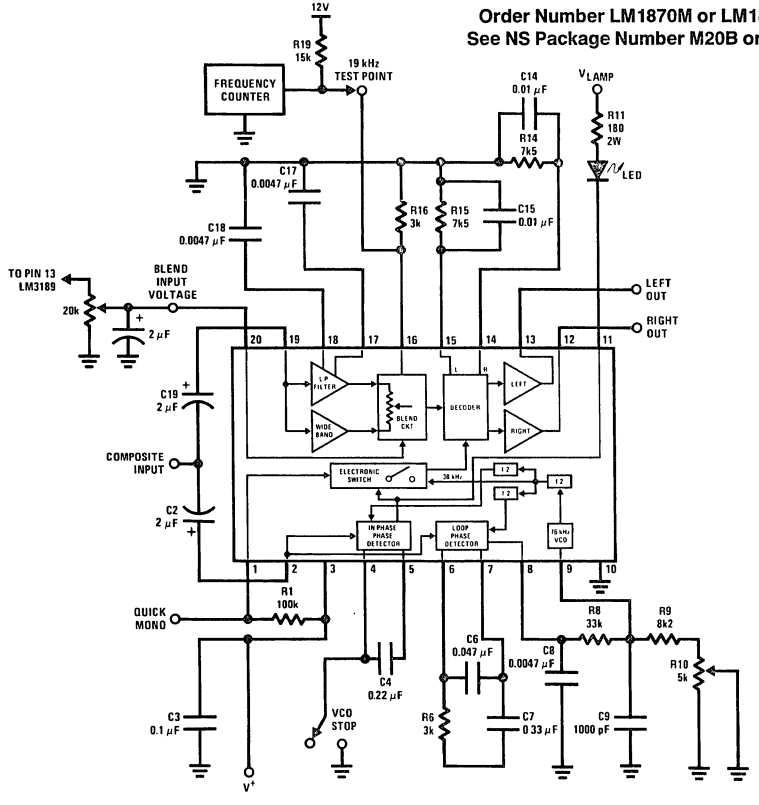
- Automobile radios
- Hi Fi receivers and tuners
- High performance portable radios

Features

- Blend control
- Large input overload
- Low beat note distortion
- Low THD diode switching outputs
- VCO stop function
- Wide supply range, 7V to 15V
- Mono override pin

Typical Application and Test Circuit

Order Number LM1870M or LM1870N
See NS Package Number M20B or N20A



TL/H/7910–1

FIGURE 1

Pin Functions

1. Quick Mono
2. PLL Input
3. V+
4. Lamp Filter and VCO Stop
5. Lamp Filter
6. Loop Filter
7. Loop Filter
8. VCO Tuning
9. VCO Tuning
10. Ground
11. Lamp Driver
12. Right Output
13. Left Output
14. Right Gain and Deemphasis
15. Left Gain and Deemphasis
16. Blend Resistor and 19 kHz Test Point
17. Blend Filter
18. Blend Filter
19. Audio Input
20. Blend Control Voltage

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, Pin 3	15V
Lamp Driver Voltage, Pin 11	18V
Output Voltage, Pin 12, 13, Supply Off	7V
Quick Mono Input (Pin 1)	V^+ (Pin 3)
Blend Input (Pin 20)	15V
Operating Temperature Range	0°C to +70°C
Power Dissipation (Note 1)	1.9W
Storage Temperature	−65°C to +125°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	260°C
Small Outline Package	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics T_A = 25°C, V^+ = 8V, *Figure 1*

Parameter	Conditions	Min	Typ	Max	Units
DC					
Operating Supply Voltage		7	8	15	V
Supply Current			26	45	mA
Input DC Voltage	Pin 19		4		V
Input DC Voltage	Pin 2		1.8		V
Supply Rejection		15	30		dB
Lamp Leakage Current	Lamp Off, Pin 11 = 16V		0.1	100	μA
Lamp Saturation Voltage	Lamp On, Pin 11 @ 75 mA		1.4	2.0	V
VCO Stop Voltage	Voltage at Pin 4 to Stop VCO	0.2	0.4		V
VCO Stop Current	Pin 4 = 0.2V		−30	−100	μA
Blend Input Bias Current	Pin 20 = 0V		−2	−20	μA
Quick Mono Switch Voltage			4		V
Quick Mono Bias Current	Pin 1 = 8V		2		μA
Output Leakage	Pin 12 or 13 = 6.5V, Pin 3 = 0V		0.1	20	μA
Audio					
Mono Gain	1 kHz	−4	−1	+2	dB
Mono THD	1 kHz @ 200 mVrms		0.05	0.25	%
Channel Balance			±0.4	±1.5	dB
Gain Shift	Mono to Stereo		±0.1	±1.0	dB
Channel Separation	Pin 20 ≥ 1.1V	30	45		dB
Output DC Shift	Mono to Stereo		±15	±100	mV
Input Resistance	Pin 19	20	40		kΩ
Output Resistance	Pin 12, 13		65	200	Ω
Ultrasonic Rejection	19 kHz + 38 kHz		30		dB
SCA Rejection	(Note 2)		70		dB
Signal to Noise	1 kHz @ 200 mVrms Mono		68		dB
PLL					
Lamp On Voltage	19 kHz on Pin 2		15	20	mV
Lamp Off Voltage	19 kHz on Pin 2	2.5	5		mV
Lamp Hysteresis			10		dB
Capture Range	25 mVrms on Pin 2	±2	±4	±6	%
Hold In Range	25 mVrms on Pin 2		±12		%
Input Resistance	Pin 2	8	14		kΩ
Blend	**Pin 20 from 1.1V to 0.2V**				
Stereo Gain Change	1 kHz L = − R Input	−25	−35		dB
Mono Gain Change	1 kHz L = R Input	−1.5	−0.5	0.5	dB
	10 kHz L = R Input	−8	−14	−20	dB
Output DC Shift			±40	±100	mV

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 65°C/W junction to ambient for the DIP and 75°C/W junction-to-ambient for the small outline package.

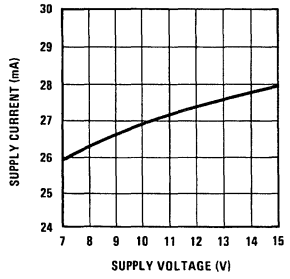
Note 2: Input is 10% SCA (74.5 kHz), 9% pilot and 1 kHz left or right. Rejection is ratio of 1 kHz output to 1.5 kHz output.

External Components

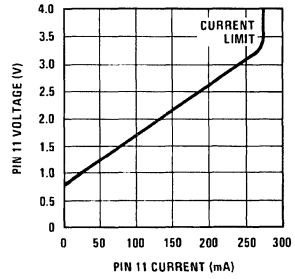
Part #	Recommended Value	Purpose	Effect		Remarks
			Smaller	Larger	
R1	100k	Pull Up for Quick Mono	OK	Errors Due to Pin 1 Bias Current	Pin 1 Can Be Shorted to Supply if Quick Mono is Not Used
C2	2 μF	PLL Input Coupling	Loading of Source Varies with Frequency		For Sources of Less Than 100Ω, Can use 0.1 μF
C3	0.1 μF	Supply Bypass			
C4	0.22 μF	Lamp Filter	Shorter Time to Switch Mono to Stereo	Longer Time to Switch Mono to Stereo	High Dielectric Resistance
R6 C6 C7	3k 0.047 μF 0.33 μF	Loop Filter	High Stereo Distortion	Narrower Capture Range	
R8	33k	Loop Filter	High Stereo Distortion	Loop Doesn't Lock	
C8	0.0047 μF			Narrower Capture Range	
C9 R9 R10	1000 pF 8.2k 5k	Sets VCO Free Running Frequency	High VCO Jitter	Narrower Capture Range	NPO 5%
			VCO Not Adjustable with C9		Metalfilm
R11	180Ω	Sets Lamp Current	Excess IC Dissipation	Dim Lamp	
R14 R15	7.5k 7.5k	Load Resistors	Low Output Voltage	Output Clips Earlier	
C14 C15	0.01 μF 0.01 μF	Deemphasis			
R16	3k	Sets Blend Characteristic	See Curves		
C17 C18	0.0047 μF 0.0047 μF	Filter for Blend	Insufficient Blend	Reduced Blend Bandwidth	
C19	2 μF	Audio Input Coupling	Poor Low Frequency Response and Separation	Turn On Delay	
R19	15k	Allows VCO Monitoring	Excess IC Dissipation	Reduces 19 kHz Output Voltage	Only Need During Set Up

Typical Performance Characteristics Blend off unless otherwise stated

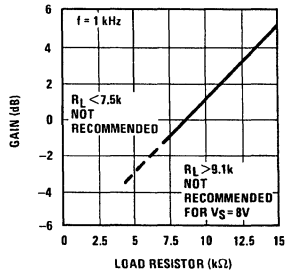
Supply Current vs Supply Voltage



Lamp Driver Voltage vs Current



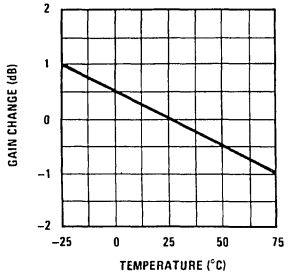
Gain vs R_L (Pin 14, 15)



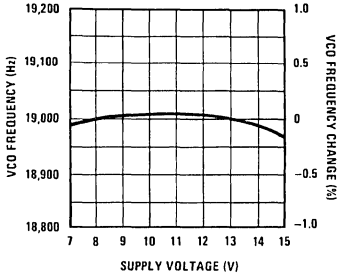
TL/H/7910–2

Typical Performance Characteristics Blend off unless otherwise stated (Continued)

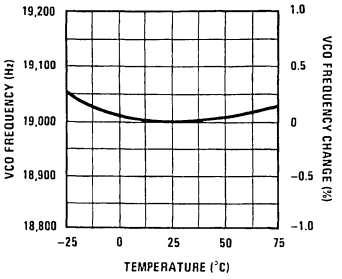
Gain Change vs Temperature



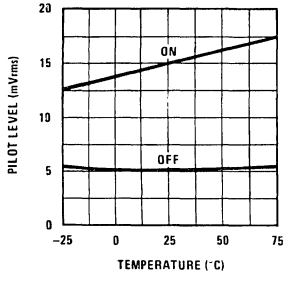
VCO Supply Sensitivity



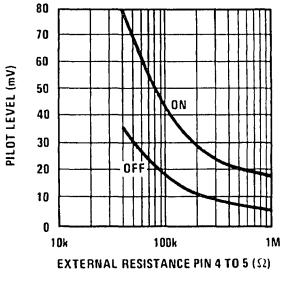
VCO Temperature Stability



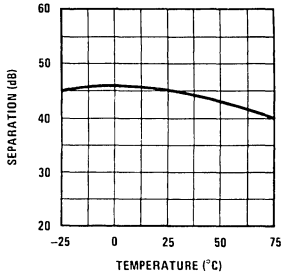
Lamp On/Off vs Temperature



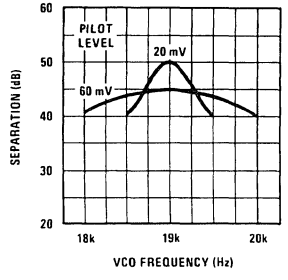
Lamp On/Off vs Resistance Pin 4 to 5



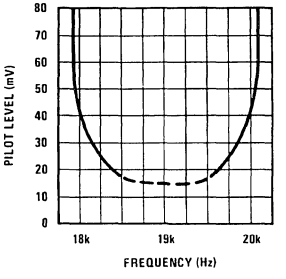
Separation vs Temperature



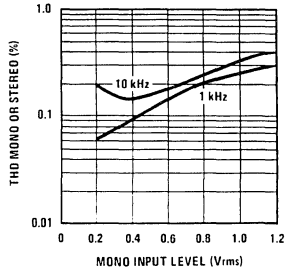
Separation vs VCO Tuning



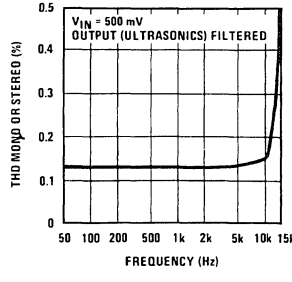
Capture Range vs Pilot Level



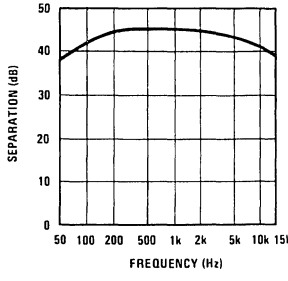
Total Harmonic Distortion vs Input Level



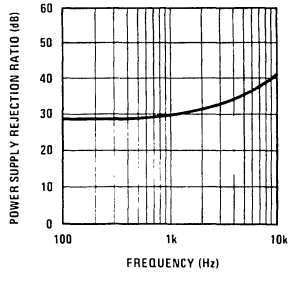
Total Harmonic Distortion vs Frequency



Separation vs Frequency



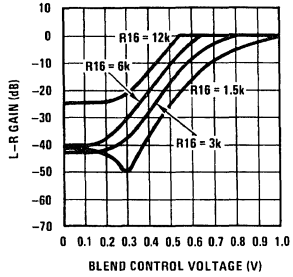
Power Supply Rejection Ratio vs Frequency



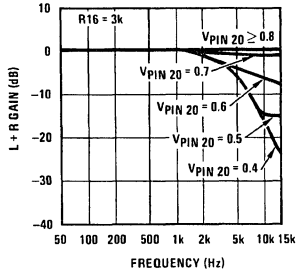
TL/H/7910–3

Typical Performance Characteristics Blend off unless otherwise stated (Continued)

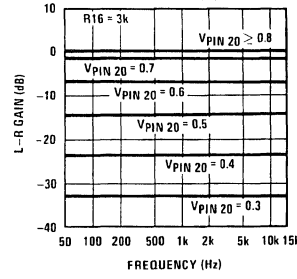
L-R Gain vs Blend Control



L + R Frequency Response with Blend Control



L-R Frequency Response with Blend Control



TL/H/7910–4

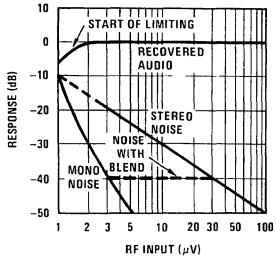
Application Hints

Blend—What & Why?

The signal to noise of a weak FM stereo signal is worse than that of an equally weak FM mono signal. For this reason FM mono radios often perform better than FM stereo radios, unless the latter is forced into mono.

The typical quieting curves of an FM stereo radio look like this:

Typical Radio Quieting Characteristic

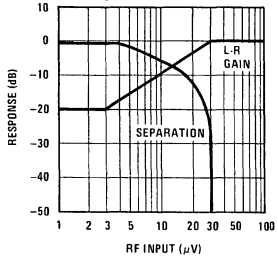


TL/H/7910–5

If an acceptable signal to noise is 40 dB, then 20 dB more signal is required in stereo compared to mono, 30 μV vs 3 μV. The degradation in noise is due to the L-R or difference channel. If the gain of the L-R is reduced, then the noise associated with it will be reduced. However, there will also be a reduction in separation.

To maintain a 40 dB signal to noise in the above example, the gain of the L-R signal should be reduced from 0 dB gain @ 30 μV downward to −20 dB at 3 μV. If this is done properly the dashed line will result. Below is a plot of L-R gain and resulting separation.

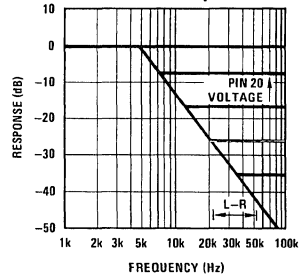
L-R Gain and Separation vs RF Input Level with Blend



TL/H/7910–6

The LM1870 reduces the gain of the L-R channel before it is demodulated. This is done by a voltage controlled shelving filter. The Bode plot of this filter is shown below:

Blend Filter Response



TL/H/7910–7

The full blend response is a two pole roll-off with each pole set by an internal 6.8k resistor and the capacitance from pins 17 and 18 to ground. The standard value for both capacitors is 4.7 nF resulting in two 5 kHz poles. The blend input (pin 20) is derived from the meter drive output of the FM IF chip (LM3089 or LM3189 pin 13). To adjust for variations in RF gain and other IC parameters, it is recommended that an adjustment be made on each radio.

Mono-Stereo Switching

The LM1870 automatically switches from mono to stereo when the level of pilot at pin 2 is about 15 mV or more. This value can be increased by putting a resistor between pins 4 and 5, as shown graphically in the Typical Performance curves.

If it is desired to switch to mono without turning off the lamp driver, pin 1 should be taken below 4V. This is a high impedance input that can be electronically switched by a transistor with a pull up resistor to the IC supply.

Outputs

The LM1870 has emitter-follower outputs resulting in a low output impedance. The output will sink or source one mA, therefore it will drive AC coupled loads greater than 2 kΩ.

In AM-FM radios the switching can be cumbersome at best. To ease the problem the outputs of the LM1870 (pins 12 and 13) are open circuit when the supply (pin 3) is open or grounded. This reduces the number of switch poles required

Application Hints (Continued)

since the outputs can remain connected at all times. This technique is commonly called diode switching but the method used in the LM1870 results in substantially lower distortion than obtained with discrete diodes.

VCO

The stereo performance of the LM1870 is very constant for small (<2%) changes in the free running frequency of the VCO. To insure that the frequency stays within 2%, low temperature coefficient components should be used for the tuning capacitor (1000 pF) and resistor (8.2k). The internal oscillator has a temperature coefficient of about 50 ppm/°C (see curve). With an NPO capacitor and a metalfilm resistor the total variation in the free running frequency will be less than 1% over the full temperature range. Tuning the VCO is done by adjusting the 5 kΩ potentiometer to get 19 kHz ±50 Hz with no input on pin 2.

The VCO frequency is monitored at pin 16 when current is supplied to the pin. During normal operation the 19 kHz square wave is not available and the resistor from pin 16 to ground programs the blend characteristics (see curves).

The VCO of the LM1870 can be stopped by taking pin 4 low. In addition to being useful for turning off the stereo indicator and forcing mono FM reception, this also allows other mono sources, such as AM, to be fed into the decoder and come out both channels. The signal will not be inadvertently decoded with the VCO off and it will have the same gain and balance characteristics as the FM. The deemphasis capacitors may need to be removed for proper frequency response. The voltage on pin 20 will also affect the freuqency response.

It should be noted that a stopped VCO cannot radiate into the rest of the radio and cause interference. Pin 4 can be taken low with a mechanical switch or an NPN transistor. If a transistor is used it must have low leakage, less than 100 nA at 3V V_{CE}, and low saturation, less than 200 mV at 100 μA collector current.

PLL

To properly demodulate the L-R signal the decoder must generate a 38 kHz signal that is locked in phase with the 19 kHz pilot signal at the input. This is done with a phase locked loop consisting of a phase detector, a loop filter (pins 6 and 7) and a VCO (pins 8 and 9).

The loop filter is similar to other standard decoders however the VCO incorporates an additional low pass filter (4.7 nF and 33 kΩ) to reduce beat note distortion an additional 20 dB.

Input Interface

There are two inputs to the LM1870, one for the PLL (pin 2) and the normal audio input (pin 19). The input impedance of the audio input is about 40 kΩ. The input coupling capacitor works with this input resistance and sets the low frequency response and separation.

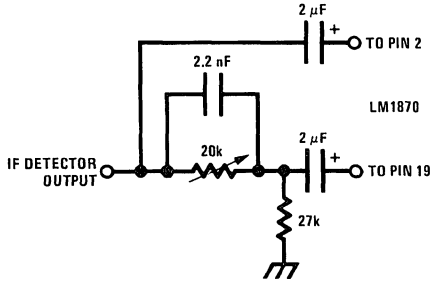
The PLL input (pin 2) locks onto the 19 kHz pilot and rejects the rest of the composite signal. For this reason it is only necessary to use a coupling capacitor large enough to insure there is no phase shift at 19 kHz. The input resistance of the PLL is 14 kΩ so a capacitor between 0.01 μF and 0.1 μF would be fine. However, the source driving this input must not be affected by this load. This is true only when the source is low impedance (less than 100Ω).

Typical FM IF circuits have detector output impedance of 5 kΩ or more. This will cause very poor low frequency response and separation unless the loading is made constant over frequency. For this reason the typical input coupling capacitor is 2 μF.

IF Correction

The separation in most radios is limited by the response of the IF. The input lead network below can often be used to improve radio separation.

IF Correction Lead Network



TL/H/7910–8

Power Supply

The LM1870 is designed to work on supplies from 7V to 15V. For automotive applications a regulator is recommended to protect against transients; the LM2930-8V is the ideal choice.

National Semiconductor Corporation

LM1871 RC Encoder/Transmitter

General Description

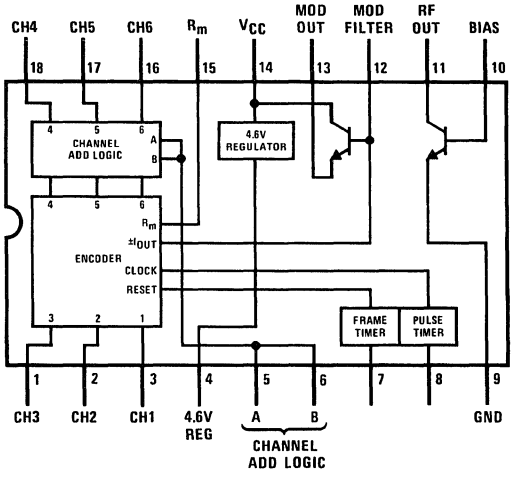
The LM1871 is a complete six-channel digital proportional encoder and RF transmitter intended for use as a low power, non-voice, unlicensed communication device at carrier frequencies of 27 MHz or 49 MHz with a field strength of 10,000 μV/meter at 3 meters. In addition to radio controlled hobby, toy and industrial applications, the encoder section can provide a serial input of six words for hard wired, infrared or fiber optic communication links. Channel add logic is provided to control the number of encoded channels from three to six, allowing increased design flexibility. When used with the LM1872 RC receiver/decoder, a low cost RF linked encoder and decoder system provides two analog and two ON/OFF decoded channels.

Features

- Low current 9V battery operation
- On-chip RF oscillator/transmitter
- One timing capacitor for six proportional channels
- Programmable number of channels
- Regulated RF output power
- External modulator bandwidth control
- On-chip 4.6V regulator
- Up to 80 MHz carrier frequency operation

Block and Connection Diagram

Dual-In-Line Package



TL/H/7911–1

Top View

Order Number LM1871N
See NS Package Number N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

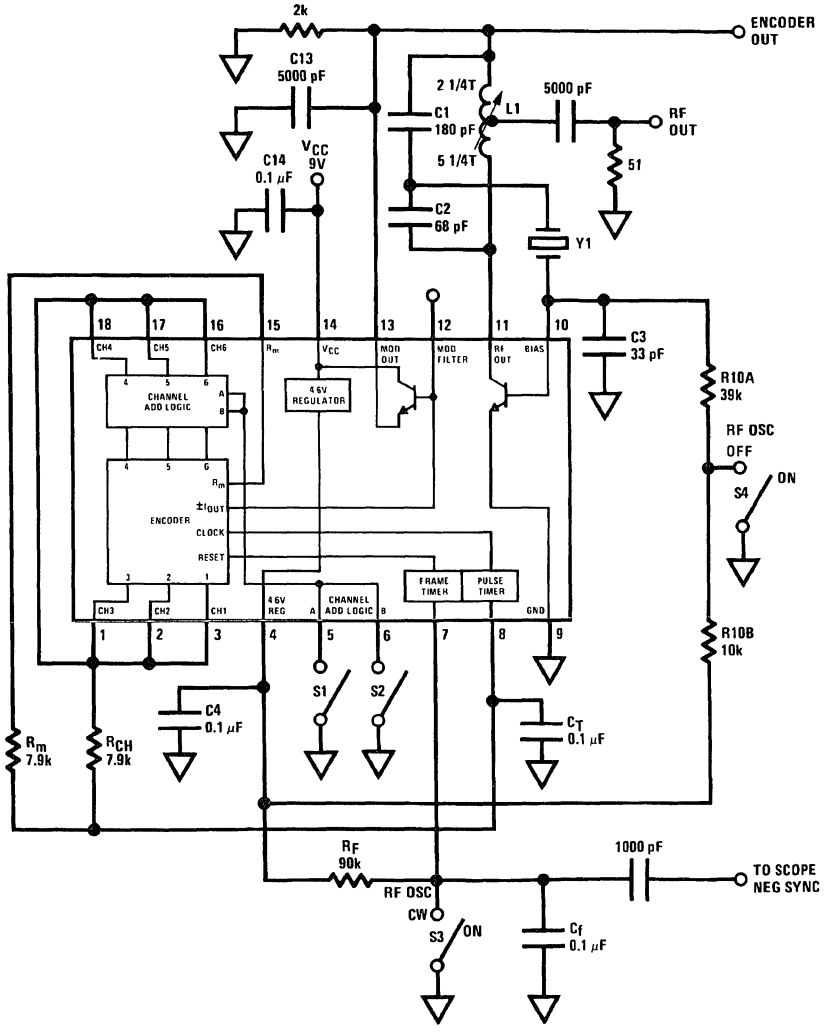
Supply Voltage	16V
DC Current Out of Pin 4	10 mA
DC Current Out of Pin 13	25 mA
Package Dissipation (Note 1)	1600 mW
Pin 4 Externally Forced	6V
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = +9V$, see Test Circuit and Waveforms

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Encoder Section, Close S1, S2, S4 Open S3						
V14	Supply Voltage		4.5	9	15	V
I_{14}	Supply Current	Encoder Only	10	14	22	mA
V4	Reference Voltage		4.1	4.8	5.4	V
t_f	Frame Time	$t_f = R_F C_F + 0.63 R_{MOD} C_T$	8	9.5	10.5	ms
t_m	Mod Time	$t_m = 0.63 R_{MOD} C_T$	0.4	0.5	0.6	ms
t_{ch}	Channel Time	$t_{ch} = 0.63 R_{CH} C_T$	0.4	0.5	0.6	ms
t_s	Sync Time, T_x Channels 1–6	Close S1, Close S2		3.5		ms
t_s	Sync Time, T_x Channels 1–5	Open S1, Close S2		4.5		ms
t_s	Sync Time, T_x Channels 1–4	Close S1, Open S2		5.5		ms
t_s	Sync Time, T_x Channels 1–3	Open S1, Open S2		6.5		ms
Δt_n	Supply Rejection, $t_m + t_{CH}$	$\Delta V_{CC} = 6V$ to 12V		0.1		%/V
ΔV13	Encoder Output Swing			3.8		V_{p-p}
ΔV12	Mod Filter Output Swing			3.8		V_{p-p}
I_{12}	Mod Filter Source/Sink Current			0.5		±mA
$R_{IN(8)}$	Pulse Timer Input Resistance			27		MΩ
$I_{TH(7)}$	Frame Timer Threshold Current			0.1		μA
$I_{LEAK(15)}$	Mod Timer Leakage Current	Pin 15 to 0V		0.01	1	μA
$V_{SAT(15)}$	Mod Timer Saturation Voltage	$I_{15} = 2$ mA, (V4–V15)		120	240	mV
$I_{LEAK(CH)}$	Channel Timer Leakage Current	Pins 1, 2, 3, 16, 17, 18 to 4.6V		0.06	1	μA
$V_{SAT(CH)}$	Channel Timer Saturation Voltage	$I_{CH} = 2$ mA		120	240	mV
RF Oscillator Section, Collector Pin 11, Base Pin 10, Emitter Pin 9 Open S4						
V_{OUT}	RF Output Level	Use RF Voltmeter Close S3		400		mV_{RMS}
I_{14}	Supply Current	Open S3, S4		30		mA
f_t	Transistor	$V_{CE} = +5V$, $I_C = 10$ mA		520		MHz
$V_{SAT(11)}$	Transistor Saturation Voltage	$f_o = 49$ MHz		800		mV
H_{FE}	Transistor BC Beta	$I_C = 10$ mA	75	150	350	
LV_{CEO}		$I_C = 10$ μA	16	20		V

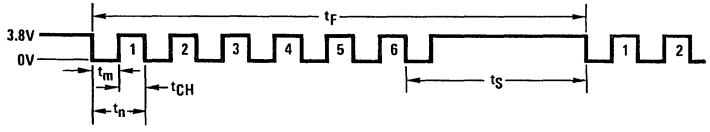
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 75°C/W junction to ambient.

Test Circuit and Switching Time Waveforms



TL/H/7911–2

Note: Test circuit has been configured for evaluation by oscilloscope. Use 1% timing components. R_M, R_{CH}, R_F, C_T



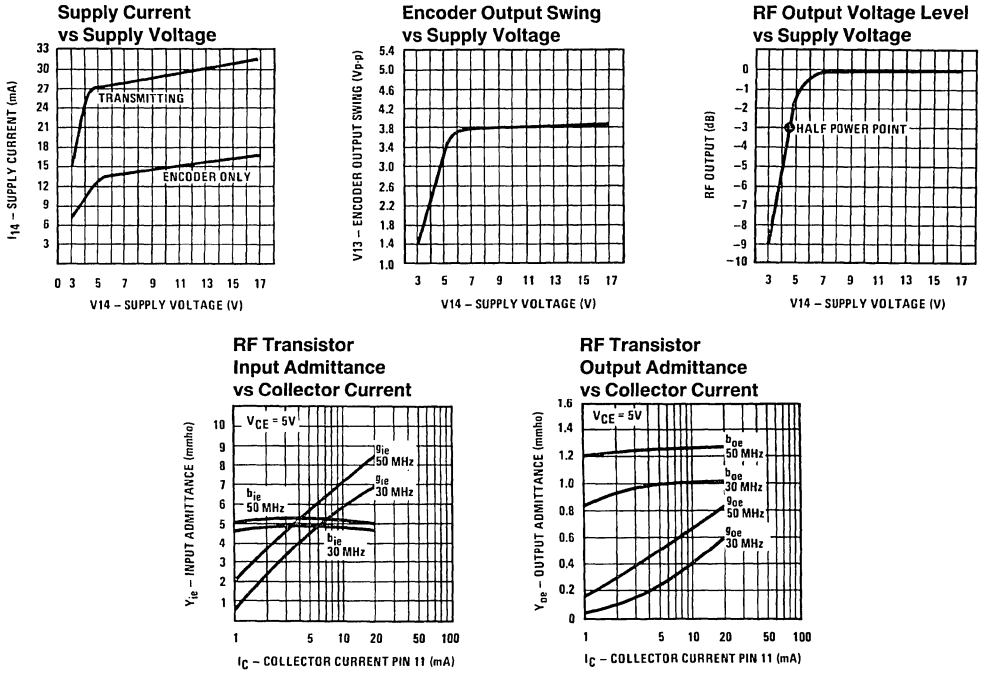
TL/H/7911–3

L1: Toko E523LN-7210019 type MC117 7½ turns with tap 2¼ turns from top

Y1: 49.86 MHz crystal 3rd overtone

Encoder output (pin 13) close S1, S2, S4, 0.5 ms/div sweep

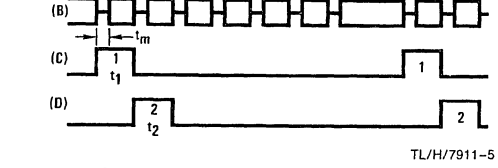
Typical Performance Characteristics



TL/H/7911–4

Applications Information

The LM1871 has been designed to encode and transmit 27 MHz or 49 MHz carriers for remote radio control (RC) of up to six independent analog functions. The encoder section converts a variable potentiometer setting to a variable pulse width. The variable pulse widths, each preceded by a fixed modulation pulse, are added together sequentially and then followed by a synchronization pulse. *Figure 1* shows the digital proportional control format and how the channel pulse widths, sync time and frame time are defined.



TL/H/7911–5

FIGURE 1. (A) Encoder Output (Pin 13)
(B) Transmitted RF Carrier Envelope
(C) Typical Receiver Channel 1 Output
(D) Typical Receiver Channel 2 Output

Figure 1 (A) shows the encoder output waveform. The modulation time (t_m) is fixed while the channel time (t_{ch}) is the variable pulse width. In *Figure 1 (C, D)* the recovered channel pulse (t_n) is the sum of t_m and t_{ch} at a rep rate set by the frame time (t_f). Because the frame time is fixed, the sync time (t_s) will vary inversely to the variable channel times.

After detection by the RC receiver, the channel pulse widths must now be converted back to the required analog functions, which might be a mechanical arm movement, motor speed control or simply an ON/OFF transistor switch. In the case of the mechanical arm movement, commercially available closed loop servo modules can be found in most hobby shops. The input requirements of these servos will determine the transmitted frame time and channel pulse width range. Usually the pulse width for arm at center will be 1.5 ms; for full left, 1.0 ms; and for full right, 2.0 ms, at a rep rate of 20 ms. A motor speed control open loop servo can be designed for the same input pulse widths: 1.0 ms for maximum forward speed, 1.5 ms with some dead band for motor OFF and 2.0 ms for maximum reverse speed. In both servo systems the input pulse width being continuously variable allows full control of arm position, motor speed and direction. The ON/OFF function could also use the same input pulse width range (1 ms ON, 2 ms OFF).

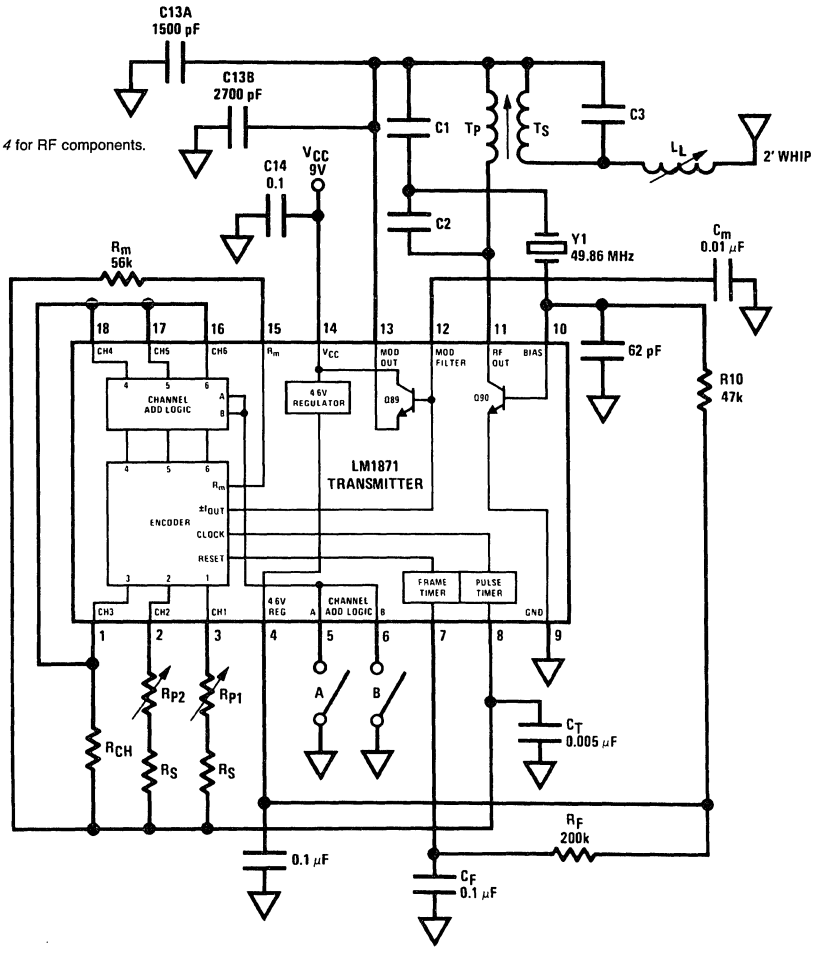
The 1.0 ms to 2.0 ms pulse width range required by most servo modules is a result of transmitted RF spectrum limitations required by the FCC. If the modulation time (t_m) and the channel time were made very short ($\cong$10 μs each)

Applications Information (Continued)

many sidebands 5 kHz apart would be generated on each side of the center frequency. The amplitude and number of sidebands are determined by the depth and duration of the modulation pulse. FCC regulations require that all sidebands greater than 10 kHz from center frequency be less than 500 μV/meter at three meters. In the example cited above, the 100% modulated carrier spectrum would not be acceptable if the field strength of the carrier was 10,000 μV/meter at three meters. If the modulation and channel times were made much longer (≅10 ms each) the transmitted spectrum would be acceptable but now the frame time would be longer than desirable for optimum servo designs. When the received channel pulse widths are between 1.0 ms and 2.0 ms at a frame rate of 20 ms the modulation time should be between 400 μs and 600 μs to insure an acceptable transmitted RF spectrum.

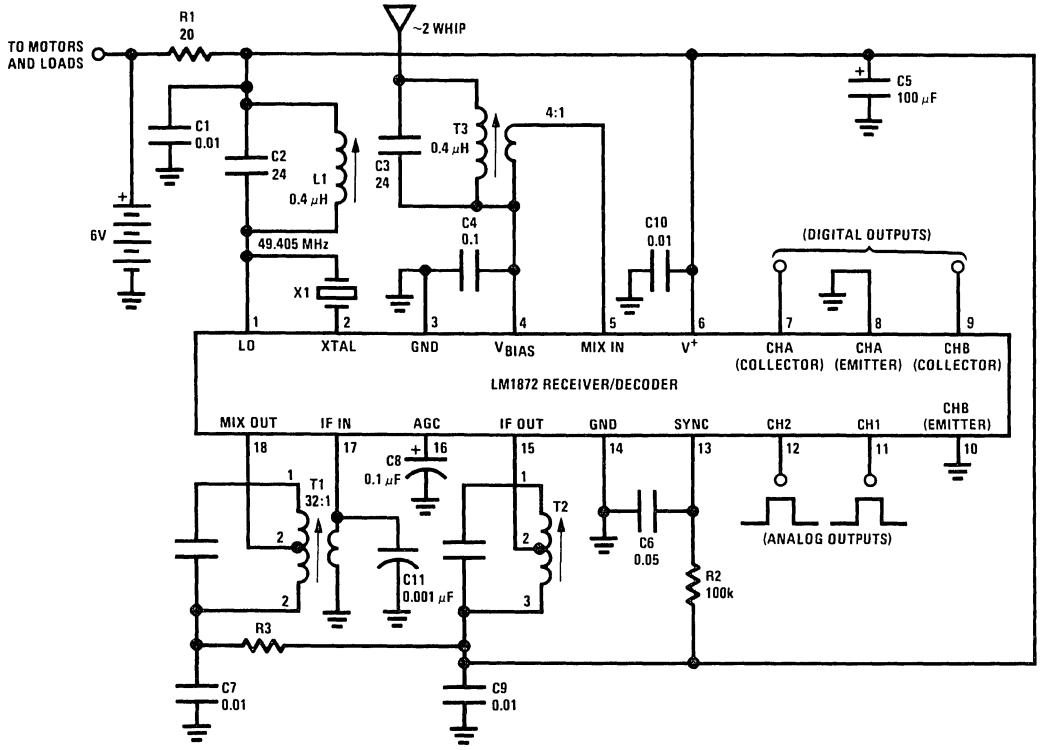
Figure 2 shows the block diagram and a typical application of the LM1871 utilizing two fully proportional (analog) channels and two uniquely encoded ON/OFF (digital) channels. The LM1872 Receiver/Decoder, a companion IC to the LM1871, has been designed to receive and decode two analog channels and two digital channels. The two digital channel output states are determined by the number of transmitted channels rather than by the width of a channel pulse. Table I shows the digital output format as a function of the number of transmitted channels.

Note: See *Figure 4* for RF components.



TL/H/7911–6

Applications Information (Continued)



TL/H/7911–7

T1 = Toko RMC 202313 } Q_O = 110
T2 = Toko RMC 402503 }
T3, L1 = Toko KEN 4028DZ

FIGURE 2. Two Channel Analog/Two Channel Digital Transmitter/Receiver Application

Applications Information (Continued)

LM1871 ENCODER TIMING

Figure 3 shows the two timing circuits and waveforms used by the LM1871. The frame timer oscillator consists of a high gain comparator and a saturating NPN transistor switch. When the NPN transistor is turned OFF the timing capacitor (C_F) will charge up to ⅔ of the V_{REG} voltage. The comparator will then turn ON the NPN transistor, discharging the capacitor back to ground ending the timing cycle. The pulse timing circuit is similar in operation except that the timing capacitor (C_T) is charged and discharged between ⅓ and ⅔ of the V_{REG} voltage. The saturating PNP transistor switch pulls up the modulation timing resistor (R_M) which charges C_T to ⅔ V_{REG} and six independently switched NPN transistors provide the discharge path through the channel timing resistors (R_{CH}). The time constant for both circuits can be found as follows:

$$\frac{-t}{RC} = \ell n \frac{V1}{V2}$$

when V1 = Voltage across timing resistor at end of timing cycle.

V2 = Voltage across timing resistor at beginning of timing cycle.

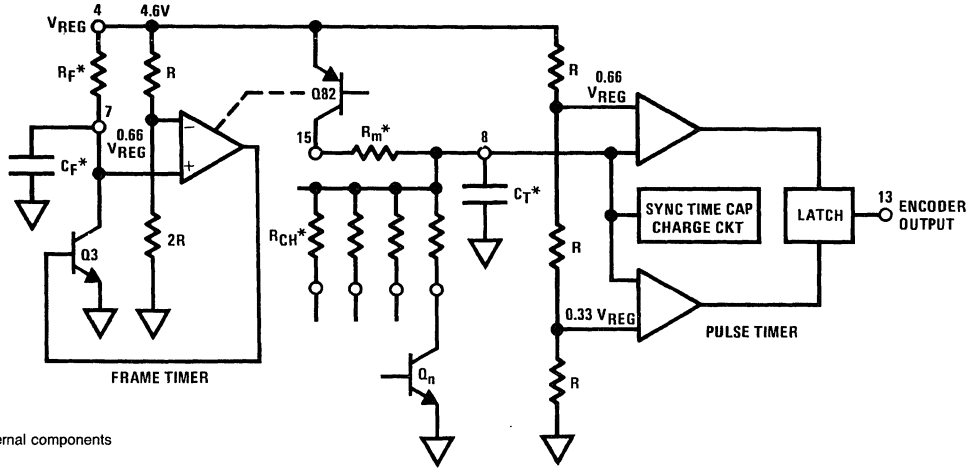
In the frame timer circuit the NPN transistor is held on for a period determined by the modulation pulse (t_m). This was done to insure that the timing capacitor was fully discharged. The frame (t_f), modulation (t_m) and channel time (t_{ch}) can be calculated as follows:

$$t_f = -\ell n \frac{1.534}{4.6V} (R_F C_F) + t_m = 1.1\, R_F C_F + t_m$$

$$t_m \text{ or } t_{ch} = -\ell n \frac{1.534}{3.06V} (R_M \text{ or } R_{CH}) C_T$$

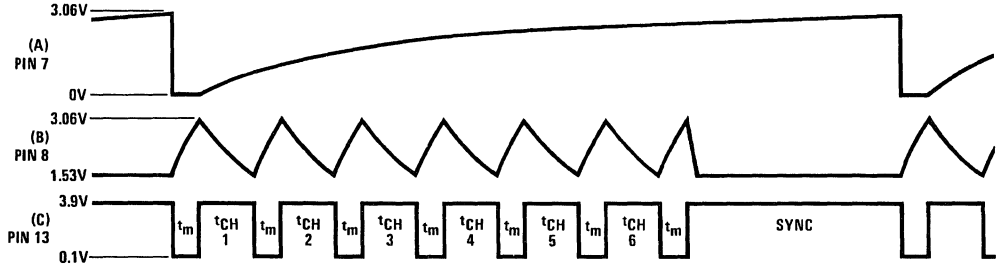
$$= 0.69\, (R_M \text{ or } R_{CH})\, C_T$$

The above calculated time constants will be modified by transistor saturation resistances and comparator switching voltages that are slightly different than the ⅓ and ⅔ V_{REG} reference. One time constant should be used for the frame time (t_f) and 0.63 time constant should be used for the modulation (t_m) and channel (t_{ch}) times. Because the switching voltages are a percentage of the V_{REG} voltage the timer accuracy will not be affected by a low battery condition (V_{CC} < 5.6V). High and low temperature (−25°C to +85°C) operation also has little effect on timer accuracy.



*External components

TL/H/7911–8



(A) Voltage on C_F

(B) Voltage on C_T

(C) Encoder pulse train output

TL/H/7911–9

FIGURE 3. Simplified Encoder Timing Circuits and Waveforms

Applications Information (Continued)

The accuracy and temperature characteristics of the external components will determine the total accuracy of the system. The capacitors should be NPO ceramics or other low-drift types.

As an example the following procedure can be used to determine the external timing components required for *Figure 2*.

Given: Frame time (t_f) = 20 ms

Modulation time (t_m) = 500 μs

Recovered pulse width (t_n) range = 1.0 ms to 2.0 ms with trim capability

Non variable channel pulse width (t_n) = 1.0 ms

1. Frame Timer Components

   Choose C_F = 0.1 μF ±10%

   $$R_F = \frac{t_f - t_m}{C_T} = \frac{20\text{ ms} - 0.50\text{ ms}}{0.1\ \mu\text{F}} = 195\ \text{k}\Omega\ (200\ \text{k}\Omega)$$

2. Modulation Time Components

   Choose C_T = 0.01 μF ±10%

   $$R_M = \frac{t_m}{0.63C_T} = \frac{500 \times 10^{-6}}{(0.63)(1 \times 10^{-8})} = 79.36\ \text{k}\Omega\ (82\ \text{k}\Omega)$$

3. Non-Variable Channel (3 through 6) Component

   $t_{ch} = t_n - t_m = 1.0\text{ ms} - 0.50\text{ ms} = 500\ \mu\text{s}$

   $$R_{CH} = \frac{t_{ch}}{0.63C_T} = \frac{500 \times 10^{-6}}{(0.63)(1 \times 10^{-8})} = 79.36\ \text{k}\Omega\ (82\text{k})$$

4. Variable Channel 1(t1) and Channel 2 (t2) Components

   When the R_P wiper arm varies across the full potentiometer range, (ΔR = 0Ω to R_P value) R_S is found for 0Ω and minimum t_n pulse width.

   $$R_S = \frac{t_n - t_m}{0.63C_T} = \frac{1\text{ ms} - 0.50\text{ ms}}{(0.63)(1 \times 10^{-8})} = 79.36\ \text{k}\Omega\ (82\text{k})$$

   $R_P(\Delta R)$ is found for maximum t_n pulse width.

   $$R_P = \frac{t_n - t_m}{0.63C_T} - R_S$$

   $$= \frac{2\text{ ms} - 0.50\text{ ms}}{(0.63)(1 \times 10^{-8})} - 82\ \text{k}\Omega$$

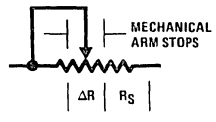
   $$= 156\ \text{k}\Omega$$

The R_P value could have been chosen first and a C_T calculated. Usually the 270° to 320° angle of potentiometer rotation is inconvenient especially if it is desired to spring return the control to center, or if lever type knobs are required. A 500 kΩ potentiometer that has 300° of end to end wiper arm rotation could be used if mechanical stops limit this range.

$$\text{Required angle of rotation} = \frac{(300°)(156\ \text{k}\Omega)}{500\ \text{k}\Omega} = 93.6°$$

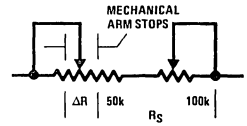
In most applications the resistor and capacitor tolerances prevent sufficient system accuracy without mechanical or electrical trimming of the analog channel pulse widths. If a 500k potentiometer is used, two trim methods can be utilized. R_S can also be included as part of the potentiometer resistance.

Potentiometer Body for Mechanical Trim



TL/H/7911–10

for Electrical Trim



TL/H/7911–11

ΔR = 156 kΩ, R_S = 82 kΩ

If t_n = 1.5 ms ±30% is required:

$$\pm R_{TRIM} = 0.3\frac{\Delta R}{2} + R_S = 48\ \text{k}\Omega$$

$$\text{Required Body Rotation} = \frac{(300°)(48\text{k})}{500\text{k}} = \pm 28.8°$$

Channel Add Logic

Table I shows the number of transmitted channels as a function of pin 5 and pin 6 conditions. The threshold voltage for both pins is ≅0.7V. When grounded, the pins are sourcing ≅300 μA from the internal pull up resistors. External voltages may be applied to these pins but should be below the V_{REG} voltage by at least one volt and not less than the pin 9 ground.

Modulator and Crystal Oscillator/Transmitter Circuit *(FIGURE 4)*

The modulator and oscillator consist of but two NPN transistors whose operation is quite straightforward. The base of the modulator transistor is driven by a bidirectional current source with the voltage range for the high condition limited by a saturating PNP collector to the pin 4 V_{REG} voltage and

TABLE I. Digital Channel Output Format as a Function of Transmitted Channels

LM1871 Channel Add Logic Pin Conditions		Number of Channels Transmitted	LM1872 Receiver Digital Outputs	
Pin 5 (A)	Pin 6 (B)		A	B
OPEN	OPEN	3	OFF	OFF
GND	OPEN	4	ON	OFF
OPEN	GND	5	OFF	ON
GND	GND	6	ON	ON

Applications Information (Continued)

low condition limited by a saturating NPN collector in series with a diode to ground. A current source of ±500 μA was chosen to provide a means for external modulator bandwidth control. When a capacitor is used at this node the transmitted RF carrier is made to slew ON and OFF at a time determined by:

Modulation slew time (t_{ms})

$$= \frac{(\Delta V12)(C_M)}{I_{12}} = \frac{(3.8V)(0.01\ \mu F)}{500\ \mu A} = 76\ \mu s$$

when ΔV12 = peak to peak voltage swing of pin 12 = 3.8V

$\pm I_{12}$ = source/sink current from pin 12 = 500 μA

C_M = capacitance at pin 12 = 0.01 μF

Figure 5 shows the advantage gained by this capacitor especially if adjacent channels are 10 kHz to 15 kHz away from the desired channel.

The crystal oscillator/transmitter is configured to oscillate in a class C mode with the conduction angle being approximately 140° to 160°. Resistor R10 provides the base bias current from the pin 4 V_{REG} voltage. This resistor value has been optimized for most RC applications. When the emitter of the modulation transistor is high (≅3.8V) the collector and tank coil are pulled up into the active range of the oscillator transistor. RF feedback to the base is via the series mode crystal which determines the oscillator frequency. Because third overtone crystals are used for 27 MHz or 49 MHz applications a tuned collector load must be used to guarantee operation at the correct frequency. Tuning the LC tank, while having little effect on oscillator frequency, will control the conduction angle and oscillator efficiency. Tuning the LC tank for minimum V_{CC} supply current while observing the carrier envelope on an oscilloscope would be the best alignment method.

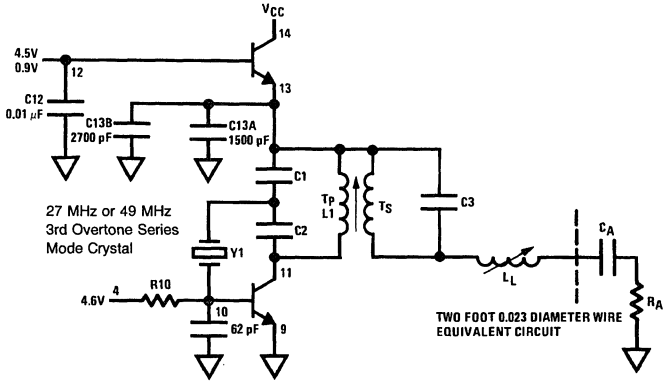
For most RC applications the carrier ON to OFF ratio must be as high as possible to ensure precise pulse width detection at the receiver. If we were to look at the base of the oscillator transistor we would see that the crystal is still oscillating during the time that the carrier is OFF (t_m). This is because of the high Q characteristic (10k to 30k) of crystals in this application. We can roughly calculate the number of cycles required for a decay or rise in amplitude for one time constant (63% of final value) by:

$$\text{Number of cycles} = \frac{4Q}{\pi}$$

At 49 MHz this will be 15k cycles or 300 μs for a crystal Q of 30k. At 27 MHz this time will be 560 μs for the same crystal Q. If long carrier OFF times were required the oscillator start up time would as a result also be quite long. The shorter carrier OFF times overcome one problem but do suggest that the crystal be isolated from the antenna circuit. During the carrier OFF time the base of the modulator transistor is held approximately 0.9V above ground such that the emitter still supplies current to the now saturated collector of the oscillator transistor. Both ends of the LC tank circuit now "see" a low impedance to ground. Further isolation is provided by the split tuning capacitor.

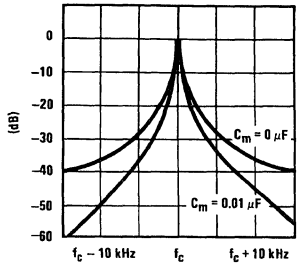
Component	27 MHz	49 MHz
T_P	2 Turns	6 Turns
T_S	3 Turns	1 Turn
L1	TOKO KXN K4636 BJF	TOKO KEN K4635 BJE
L_L	MILLER #4611	MILLER #9330-10
C_A	5.4 pF	6.2 pF
R_A	1.15Ω	3.78Ω
C1	1000 pF	220 pF
C2	680 pF	47 pF
C3	20 pF	33 pF
R10	24k	47k

Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070



TL/H/7911–12

FIGURE 4. 27 MHz and 49 MHz RF Oscillator/Transmitter



TL/H/7911–13

FIGURE 5. Envelope of Transmitted Spectrum for Circuit in *Figure 2*

Applications Information (Continued)

If the printed circuit board shown in *Figure 6* is to be reproduced, it is recommended that the layout be followed as closely as possible. The positions of pin 13 decoupling capacitors and coil components tend to be critical in regard to undesired harmonic emissions. Short lead ceramic disc capacitors and short decoupled traces are recommended. A number of boards with this configuration have successfully met all requirements of the FCC as perceived only by National Semiconductor. Final approval of any unlicensed transmitter is granted only by the FCC via certified test measurements.

Field Strength Measurements

As noted above the maximum radiated RF energy of an unlicensed transmitter operating in the 27 MHz or 49 MHz frequency band must not be greater than 10k μV per meter at a distance of 3 meters from the transmitting antenna. In addition to the carrier amplitude requirement, all sidebands greater than 10 kHz from the carrier and all other emissions (harmonic or spurious) must be less than 500 μV per meter at a distance of 3 meters.

The term used for electrical field intensity (V/meter at 3 meters) refers to the open circuit voltage induced at the ouptut of a resonant half-wave dipole antenna in a single dimensional one meter field, 3 meters distant from the transmitter under test. When making field intensity measurements, the antenna length must be adjusted for resonance at each frequency of interest and the induced voltage made proportional to the one meter reference length. The induced voltage value must not include losses caused by the insertion of a 1:1 balun transformer (−6 dB) or loading (−6 dB) and mismatch (72Ω to 50Ω, −1.7 dB) of the voltage measuring instrument. We can now relate the induced voltage (V_{IN}) to a measured voltage (V_{MEA}) by:

$$V_{MEA} = \frac{V_{IN}\,L}{\text{Losses}} \text{ or } V_{IN} = \frac{(V_{MEA})\,(\text{Losses})}{L}$$

where: V_{MEA} = Voltage measured by a spectrum analyzer or calibrated receiver.

V_{IN} = Field intensity (volts/meter).

L = Half-wave length of antenna in meters.

Losses = All mismatch, loading and insertion losses. (In this case = 13.7 dB = 4.87)

The length of a half-wave dipole antenna is found by:

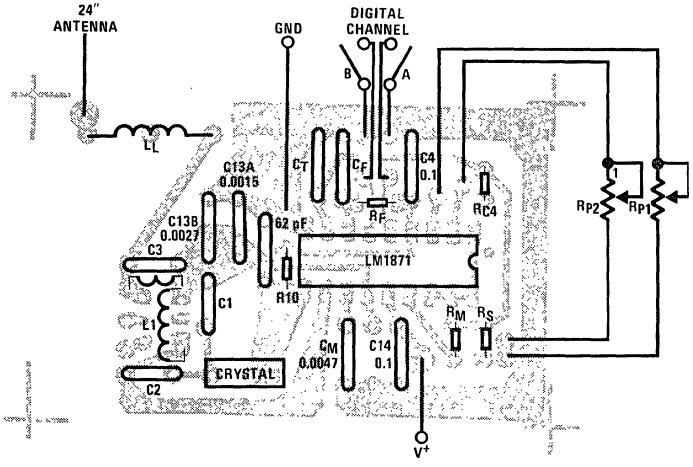
$$L = \frac{Ck}{2f} \text{ meters}$$

where: C = Speed of light in a vacuum.

k = A constant related to antenna length to width ratios, end effects and surface effects. Use k = 0.96 for practical antenna rods $5/16''$ in diameter.

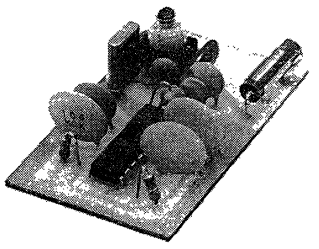
f = Frequency of interest.

Simplified: $L = \frac{144}{f\,\text{MHz}}$ meters



TL/H/7911–14

FIGURE 6



TL/H/7911–15

Applications Information (Continued)

Now that we have a way in interpreting the field strength measurements we must deal with the technique used in making these measurements. Usually all measurements are done outside on a flat area away from trees, buildings, buried pipes or whatever. The test transmitter is placed on a wooden stool or table approximately 3 feet high such that the vertical antenna is in a vertical position. The receiving dipole is adjusted for the frequency of interest and oriented to the same plane as the transmitter and placed 3 meters from the transmitter. The dipole may be mounted on a wooden pole or ladder such that the height of the antenna can easily be changed. The antenna length must always be symmetrical about the center tapped balun transformer. The operator and his test equipment must be "behind" the dipole by some 3 or more feet. If it is desired to have the operator at a much more distant location the transmission line must be characterized for additional losses. A number of measurements should be made at each frequency for different heights and orientations of both the transmitting and receiving antennas. The highest reading should be considered the correct reading. In addition to fundamental, sidebands and harmonic emissions, the frequency spectrum from 25 MHz to 1000 MHz should also be scanned for spurious emissions greater than 50 μV/meter at 3 meters.

Additional Applications

Figure 2 shows a typical application of the LM1872 Receiver/Decoder. The LM1872 consists of a crystal controlled local oscillator, IF amplifier, AGC, detector, decoder logic and digital channel output drivers. The supply voltage range of 2.5V min to 7V max was chosen to allow battery operation by four "C" or "D" cells.

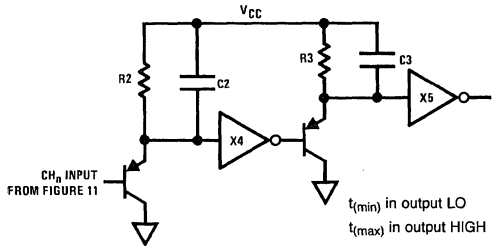
Figure 7 shows how the LM1871 encoder can be used to frequency shift a 200 kHz carrier that is transmitted over the 110V AC line in a home or office. *Figure 8* shows how ON/OFF carrier modulation is also possible. An LM1872 could be used as a receiver/decoder for the *Figure 8* transmitter circuit. When using an LM1872 the carrier frequencies should be 50 kHz or greater to insure proper detector operation.

Figure 9 shows the LM1871 configured for six analog channels with a TTL compatible output. The V_{REG} voltage at pin 4 has been shorted to V_{CC}. This allows a $V_{CC(MIN)}$ of 3V and $V_{CC(MAX)}$ of 6V. The encoder output could be used for a fiber optic transmitter/receiver link, infra-red, tone keying or transducer carrier modulation. If the encoder output is hard wired to the *Figure 10* serial input we can recover the six analog channels. From *Figure 11* we see that the data input will appear during the sync time which is always longer than any channel time (t_n). Inverter X1 will discharge C1 each time the input goes high. During the longer sync time C1 will charge up to the ½ V_{CC} threshold of X2 and via X3 provide the data input. The R and C components are calculated by:

$$t_{\text{data delay}} = 0.565\ R1\ C1$$

If large values of C1 (>0.01 μF) are required the diode D1 should be replaced by a PNP transistor with the base on X1 output, emitter to X2 input and collector to ground.

In applications requiring ON/OFF decoding of a channel pulse width the circuit shown below could be used.



TL/H/7911–16

If the recovered channel pulse width is short ($t_{(min)}$) R2 and C2 are selected such that the input to inverter X4 does not rise to the ½ V_{CC} threshold. The output of X4 will be high and the output of X5 will be low. A longer input pulse ($t_{(max)}$) will allow the output of X4 to go low pulling the input of X5 low. R3 and C3 are selected such that the input to X5 will not rise past the ½ V_{CC} threshold during the remainder of the frame time. The R and C values are found by:

Given: $t_{(min)} = 1.0$ ms, C2 = 0.01 μF

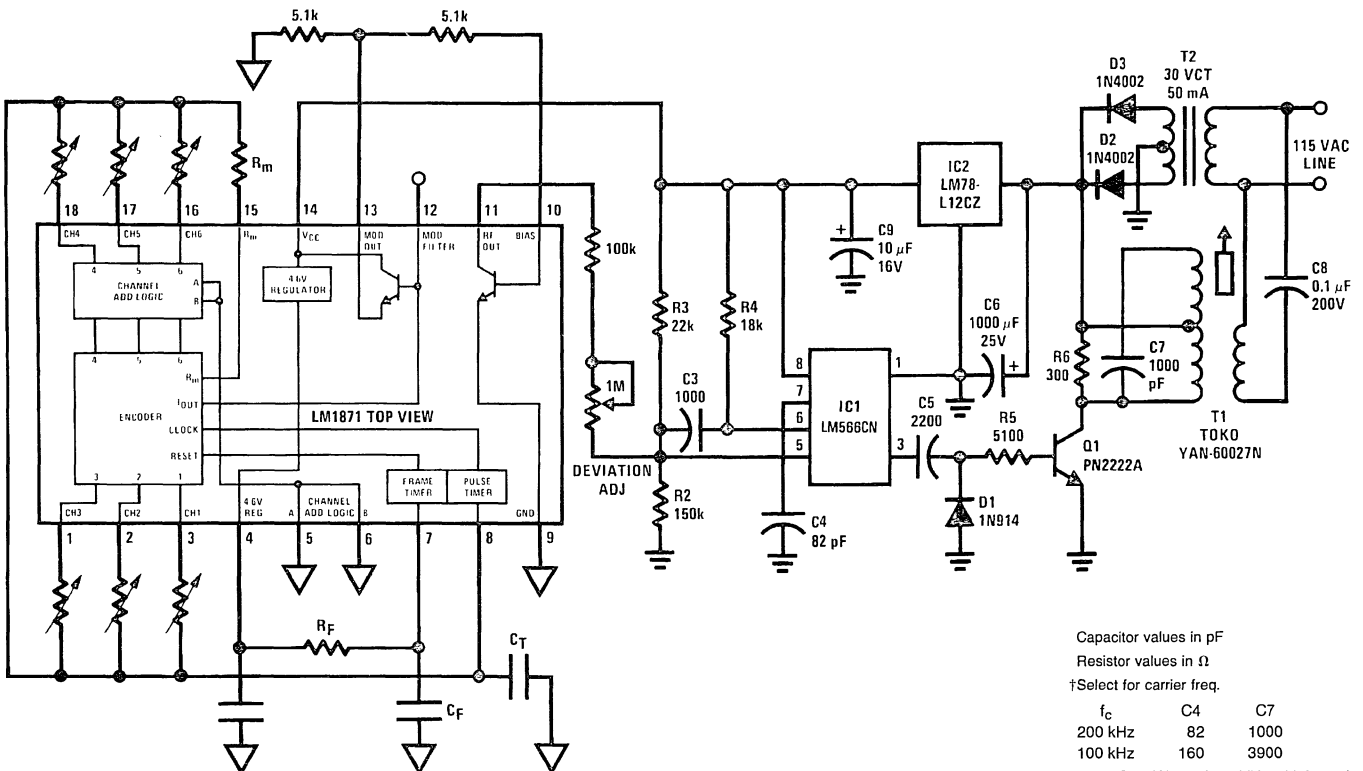
$t_{(max)} = 2.0$ ms, C3 = 0.1 μF

$t_{frame} = 20$ ms

$$0.565R2C2 = t_{(min)} + \frac{t_{(max)} - t_{(min)}}{2} = 1.5\ \text{ms}$$

$$R2 = \frac{1.5\ \text{ms}}{0.565C2} = 270\ \text{k}\Omega$$

$$R3 = \frac{t_{frame}}{0.565C3} = 360\ \text{k}\Omega$$



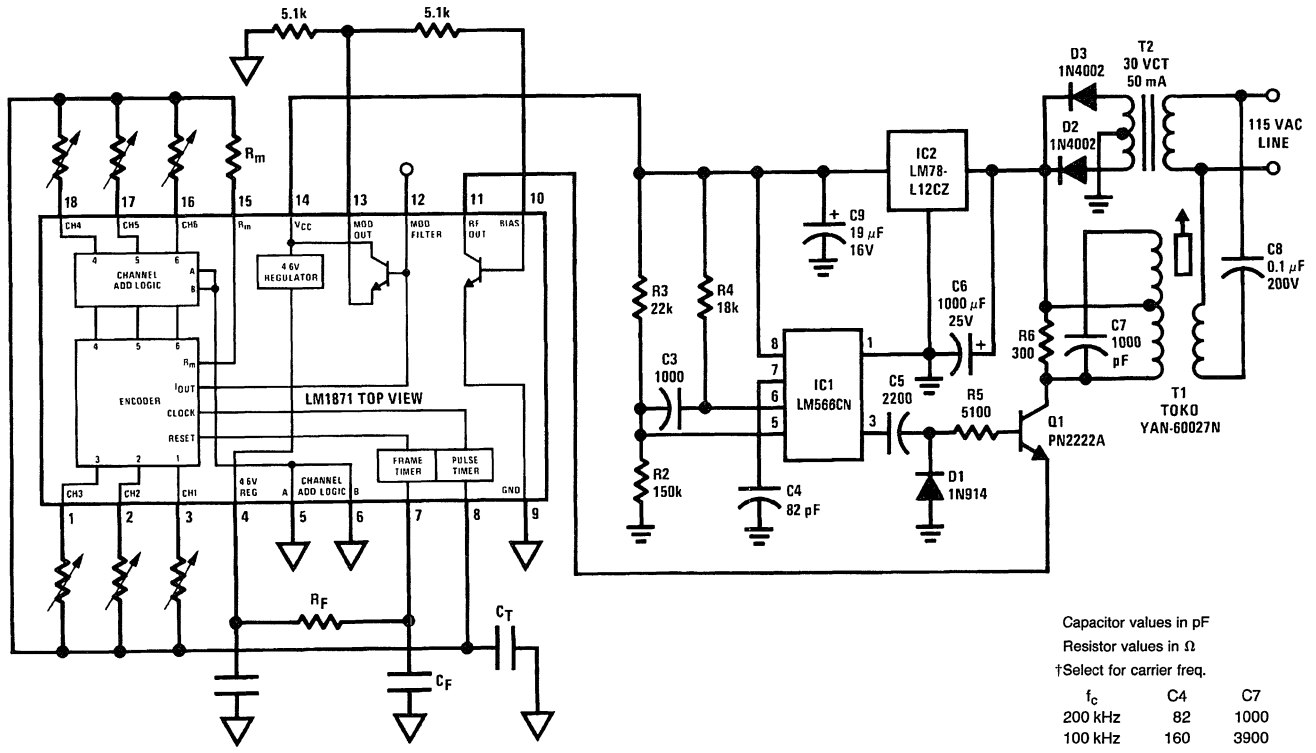
Capacitor values in pF
Resistor values in Ω
†Select for carrier freq.

f_C	C4	C7
200 kHz	82	1000
100 kHz	160	3900

Note: See AN-146 for additional information.

TL/H/7911–17

FIGURE 7. LM1871, LM566 200 kHz Line Carrier Transmitter with FSK Carrier Modulation



Capacitor values in pF
Resistor values in Ω
†Select for carrier freq.

f_c	C4	C7
200 kHz	82	1000
100 kHz	160	3900

TL/H/7911–18

FIGURE 8. LM1871, LM566 200 kHz Line Carrier Transmitter with ON/OFF Carrier Modulation

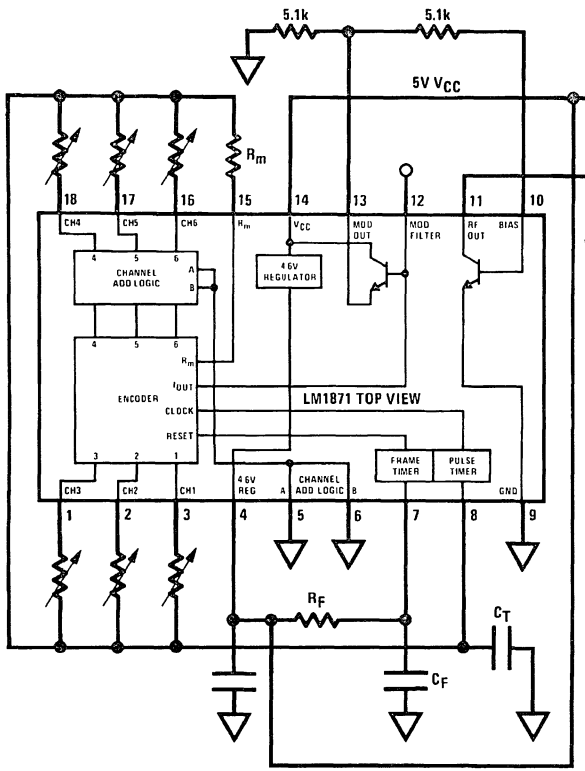
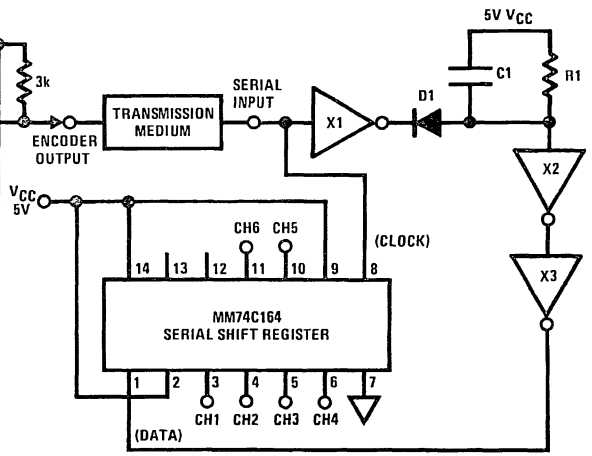


FIGURE 9. LM1871 Six Analog Channel Encoder with TTL Compatible Output



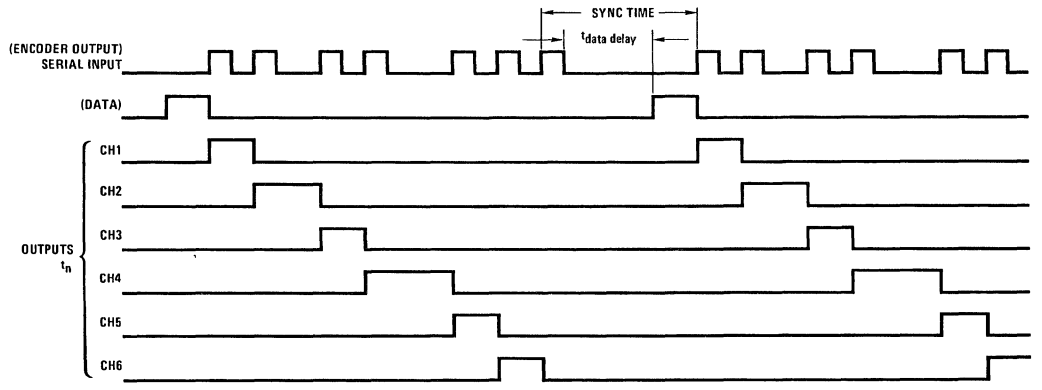
$t_{data\ delay} = 0.565\ RC$

Note: See *Figure 11* for Timing Waveforms.

TL/H/7911–19

FIGURE 10. Six Analog Channel Detector

Additional Applications (Continued)



TL/H/7911–20

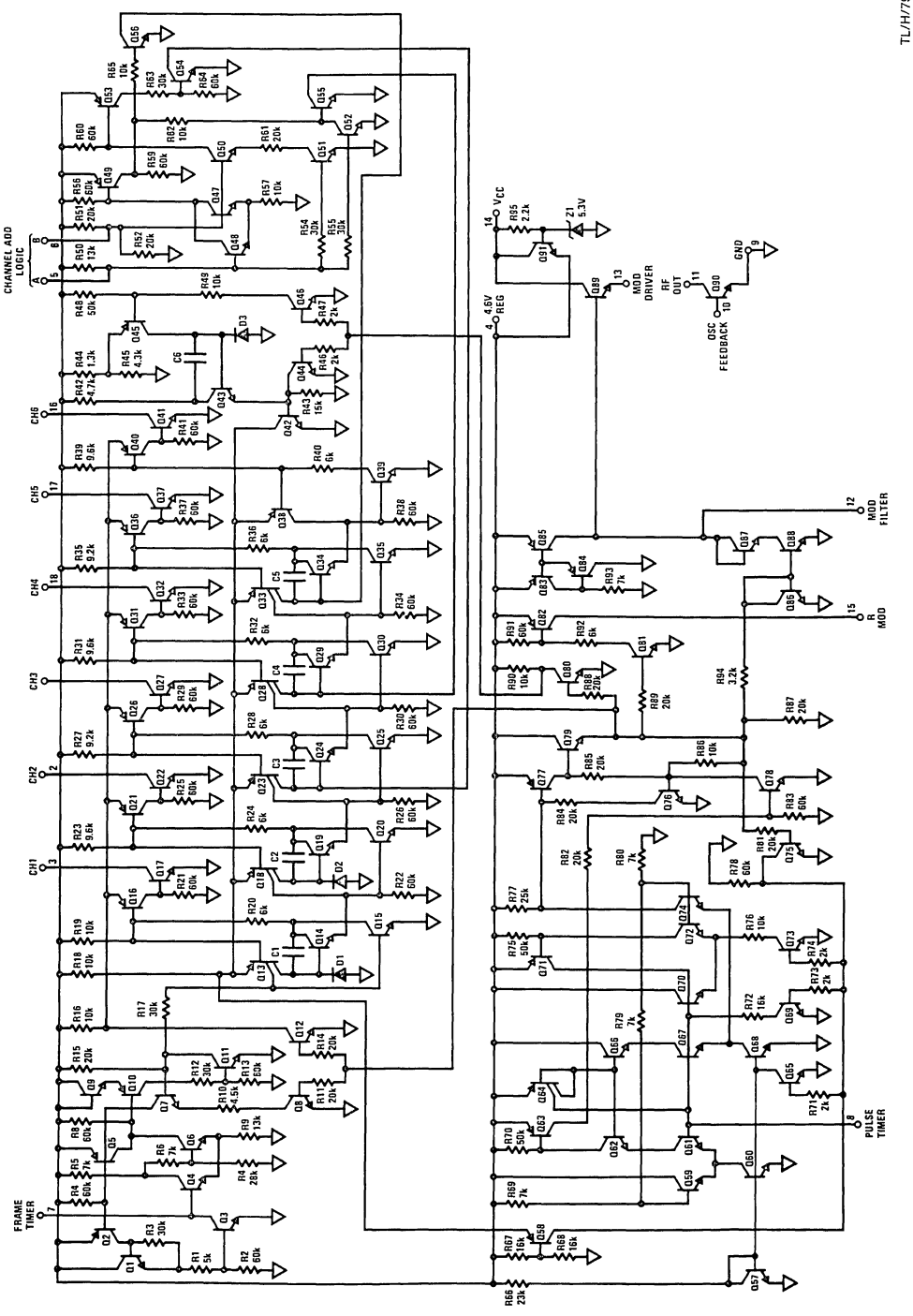
FIGURE 11. Six Analog Channel Detector Waveforms

LM1871 Component Selection Guide

Component	Min	Typ	Max	Comments
R_F	2 kΩ	180 kΩ	1M	Pin 7. Frame timer resistor used with C_F to set frame time (t_f). $t_f = R_F C_F + t_m$.
C_F	500 pF	0.1 μF	0.5 μF	Pin 7. Frame timer capacitor used with R_F.
R_M	2 kΩ	150 kΩ	1M	Pin 15. Modulation timing resistor used with C_T to set mod time (t_m). $t_m = 0.63\ R_M C_T$.
R_{CH}	2 kΩ	150 kΩ	1M	Channel pins 1, 2, 3, 16, 17, 18. Variable or fixed resistor used with C_T to set channel pulse widths (t_{ch}). $t_{ch} = 0.63\ R_{CH} C_T$.
C_T	500 pF	0.1 μF	0.5 μF	Pin 8. Pulse timer capacitor used with R_M and R_{CH}.
C_M		0.01 μF		Pin 12. Modulation slew time (t_{ms}) capacitor used to decrease modulator bandwidth. Reduces sideband emissions. $t_{ms} = \frac{(\Delta V12)(C_M)}{I_{12}} = 7600\ C_M$
C4		0.1 μF		Pin 4. 4.6V regulator decoupling capacitor.
C13A C13B		1500 pF 2700 PF		Pin 13. Modulator output RF decoupling capacitor. Improves carrier ON to OFF ratio.
C14		0.1 μF		Pin 14. V_{CC} decoupling capacitor.
R10		24 kΩ/51 kΩ		Pin 10. RF oscillator/transmitter bias resistor.

Note: See *Figure 4* for RF components. All timing capacitors should be low-drift (NPO) types.

Schematic Diagram



TL/H/7911–21

FIGURE 12

National Semiconductor Corporation

LM1872 Radio Control Receiver/Decoder

General Description

The LM1872 is a complete RF receiver/decoder for radio control applications. The device is well suited for use at either 27 MHz, 49 MHz or 72 MHz in controlling various toys or hobby craft such as cars, boats, tanks, trucks, robots, planes, and trains. The crystal controlled superhet design offers both good sensitivity and selectivity. When operated in conjunction with the companion transmitter, LM1871, it provides four independent information channels. Two of these channels are analog pulse width modulated (PWM) types, while the other two are simple ON/OFF digital channels with 100 mA drive capability. Either channel type can be converted to the other form through simple external circuitry such that up to 4 analog or up to 4 digital channels could be created. Few external parts are required to complement the self-contained device which includes local oscillator, mixer, IF detector, AGC, sync output drivers, and all decoder logic on-chip.

Features

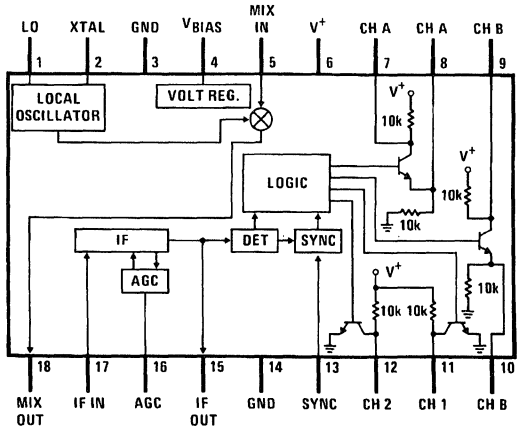
- Four independent information channels; two analog and two digital
- Completely self-contained
- Minimum of external parts
- Operation from 50 kHz to 72 MHz
- Highly selective and sensitive superhet design
- Operates from four 1.5V cells
- Excellent supply noise rejection
- 100 mA digital output drivers
- Crystal controlled
- Interfaces directly with standard hobby servos

Applications

- Toys and hobby craft
- Energy saving, remotely switched lighting systems
- Burgler alarms
- Industrial and consumer remote data links
- IR data links
- Remote slide projector control

Circuit Block and Connection Diagram

Dual-In-Line Package



TL/H/7912–1

Bottom View

Order Number LM1872N
See NS Package Number N18A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Package Dissipation (Note 2)	1600 mW
Voltage @ Pin 7, 8, 9, 10, 11 or 12	V^+
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

DC Electrical Characteristics

$V^+ = 6V$, $T_A = 25°C$, Test Circuit of *Figure 1*, $f_{LO} = 49.890$ MHz, $f_{IF} = 455$ kHz unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage	Functional for $V_{IN} = 100\ \mu V$	2.5	6	7	V
Supply Current	CH A & B Off	9	13	18	mA
	CH A & B On		27		mA
V_{BIAS}	@ Pin 4	1.85	2.1	2.35	V
Sync Timer Threshold	@ Pin 13, Going from Low to High Voltage	$V^+/2 - 0.4$	$V^+/2$	$V^+/2 + 0.3$	V
DIGITAL CHANNELS A AND B					
Saturation Voltage	@ Pins 7 & 9, $R_L = 100\Omega$		0.4	0.7	V
Saturation Resistance	@ Pins 7 & 9		7		Ω
Source Current	@ Pins 8 & 10, $V_{Pin\ 8\ \&\ Pin\ 10} \leq 1V$	100			mA
Collector Pull-Up Resistance	Pin 7 & Pin 9 to V^+	5	10	20	kΩ
Emitter Pull-Down Resistance	Pin 8 & Pin 10 to GND	5	10	20	kΩ
ANALOG CHANNELS 1 AND 2					
Saturation Voltage	@ Pins 11 & 12, $R_L = 2\ k\Omega$		0.45	0.7	V
Saturation Resistance	@ Pins 11 & 12		160		Ω
Collector Pull-Up Resistance	Pin 11 & Pin 12 to V^+	5	10	20	kΩ

AC Electrical Characteristics

Parameter	Conditions		Min	Typ	Max	Units
RF Sensitivity	For "Solid" Decoded Outputs (Note 1)			22	39	μV
RF Sensitivity	Circuit of *Figure 5* @ 49 MHz with Antenna Simulation Network of *Figure 6*			12		μV
Voltage Gain	Pin 5 to Pin 15			58		dB
PSRR of RF Sensitivity	$3V \leq V^+ \leq 6V$			−1		%Δ/V
BW	3 dB Down @ Pin 15			3.2		kHz
Noise	Referred to Input, Pin 5, $V_{IN} = 0$			0.35		μVrms
	Referred to IF, Pin 15, $V_{IN} = 0$			0.28		mVrms
AGC Threshold	Onset of AGC Relative to RF Input, V_{IN}, @ Pin 5			88		μV
	Relative to IF Output @ Pin 15		$V^+ + 0.07$	$V^+ + 0.100$	$V^+ + 0.13$	V
Mixer Conversion Transconductance	From Pin 5 to Pin 18	@ 1 MHz	2.9	4.0	6.9	mmhos
		@ 27 MHz		3.7		mmhos
		@ 49 MHz		3.5		mmhos

AC Electrical Characteristics (Continued)

Parameter	Conditions	Min	Typ	Max	Units
Mixer Input Impedance	Pin 5 to Pin 4 @ 49 MHz (See Curves)		20 kΩ + 5 pF		
Mixer Output Impedance	Pin 18 to GND		250		kΩ
IF Transconductance	Pin 17 to Pin 15 (AGC Off) @ 455 kHz	2.6	4.1	5.6	mmhos
IF Input Impedance	Pin 17 to GND		5500		Ω
IF Output Impedance	Pin 15 to GND (AGC Off)		800		kΩ
	(AGC On)		2		MΩ
IF Carrier Level	@ Pin 15, V_{IN} = 100 μV (AGC On)		70		mVrms
Detector Threshold	Relative to RF Input, V_{IN}, @ Pin 5		20		μV
	Relative to IF Output @ Pin 15	V^+ + 0.015	V^+ + 0.025	V^+ + 0.040	V
Analog Pulse Width Accuracy	Ratio of Received Pulse Width @ Pins 11 & 12 to Transmitted Pulse Width @ Pin 5 for V_{IN} = 100 μV	0.95	1.0	1.05	ms/ms

Note 1: The criteria for the outputs to be considered "solid" are as follows:

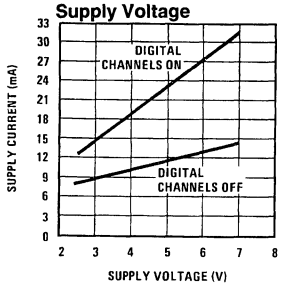
DIGITAL: In order to check the decoding section, four RF frames are inputted in sequence with the proper codes to exercise all four possible logical output combinations at pins 7 and 9. For each frame the proper output logic state must exist.

ANALOG: Each analog pulse width (measured at pins 11 & 12) in any of the above four successive frames must not vary more than ±5% from the pulse widths obtained for V_{IN} = 100 μV.

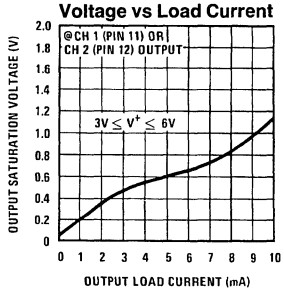
Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 75°C/W, junction to ambient.

Typical Performance Characteristics

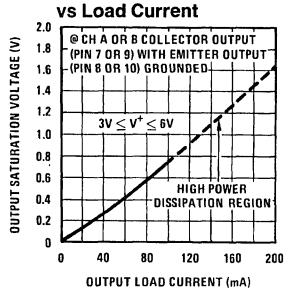
Supply Current vs Supply Voltage



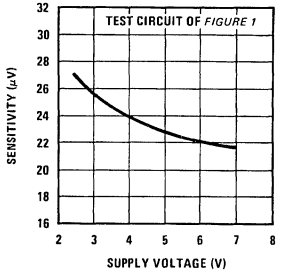
Analog Channel Output Voltage vs Load Current



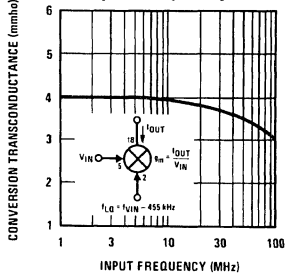
Digital Channel Collector Output Voltage vs Load Current



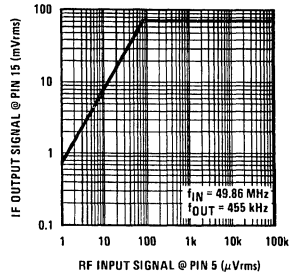
Sensitivity vs Supply Voltage



Mixer Transconductance (g_m) vs Input Frequency



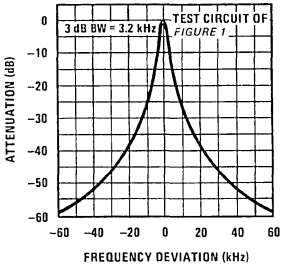
IF Output Signal Level vs RF Input Signal Level



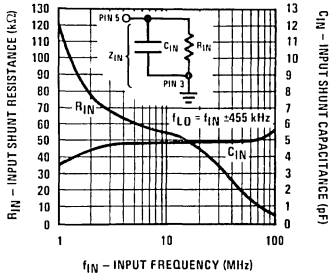
TL/H/7912–2

Typical Performance Characteristics (Continued)

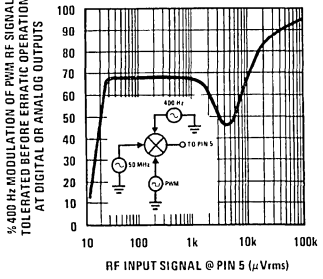
IF Bandpass Response



Equivalent Mixer Input Shunt Resistance and Capacitance vs Frequency

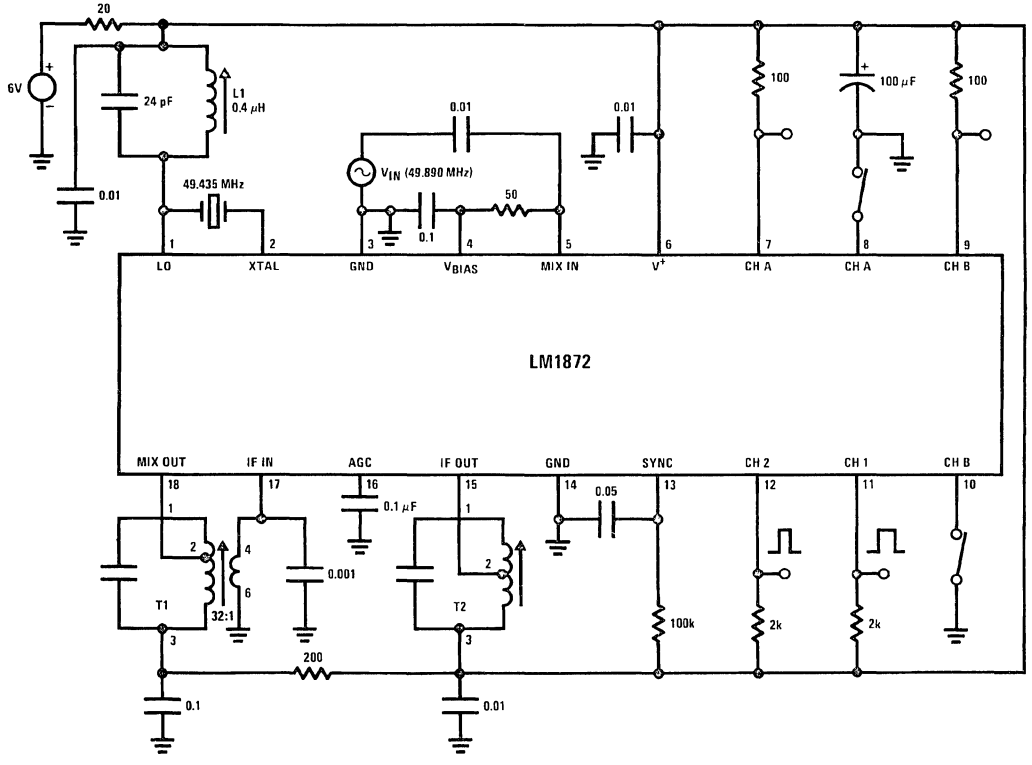


Receiver AM Rejection vs RF Input Level



TL/H/7912–3

Test Circuit



TL/H/7912–4

Bottom View

L1 = Toko* 10k type (KEN-4028 DZ); 6T
T1 = Toko* 10 EZC type (RMC 202313 NO), Qu = 110
Pin 1–2, 131T; pin 2–3, 33T
Pin 1–3, 164T; pin 4–6, 5T

T2 = Toko* 10 EZC type (RMC 402503 NO), Qu = 110
Pin 1–2, 98T; pin 2–3, 66T
Pin 1–3, 164T; pin 4–6, 8T

*Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

FIGURE 1. Test Circuit

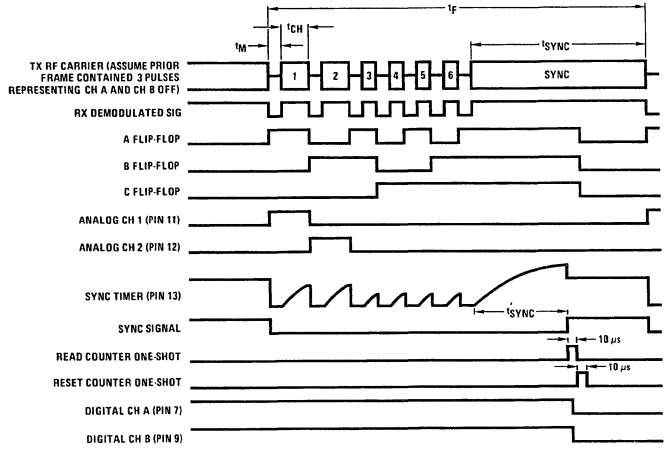
Circuit Description

The following discussion is best understood by referring to *Figures 2, 3, 4,* and *5.*

SYSTEM ENCODING AND DECODING SCHEME

For the transfer of analog information, the LM1871/LM1872 system uses conventional pulse width modulation (PWM). In applying this technique, the RF carrier is interrupted for short fixed intervals (t_M in *Figure 2*) with each interval followed by variable width pulses (t_{CH}) so as to define multiple variable time spans ($t_M + t_{CH}$) occurring in serial fashion. Synchronization is accomplished by allowing one of the transmitted variable pulse widths (t_{SYNC}) to exceed the duration (t'_{SYNC}) of a receiver-based timer, thus allowing the receiver to recognize this pulse for synchronization purposes. Taken in sequence, this collection of pulses constitutes a single frame period (t_F).

The LM1871 transmitter is equipped to transmit up to *six* channels which the companion LM1872 receiver uses to derive 2 analog and 2 digital channels. The receiver decodes the demodulated RF waveform from the transmitter by negative edge triggering a cascade of three binary dividers called the A, B, and C toggle flip-flops (*Figure 4*). By "examining" all three flip-flop outputs simultaneously, up to 6 unique channel time intervals could be identified and recovered. Only the first two channels are actually decoded however and outputted by the receiver, the rest being used for identification of two digital (ON/OFF) channels. In passing digital information, a pulse count modulation scheme is used whereby different quantities of channel pulses are transmitted by varying the number of fixed width channels following the two variable width analog channels 1 and 2 (see *Figure 3*).



TL/H/7912–5

FIGURE 2. RX Timing Waveforms

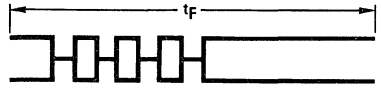
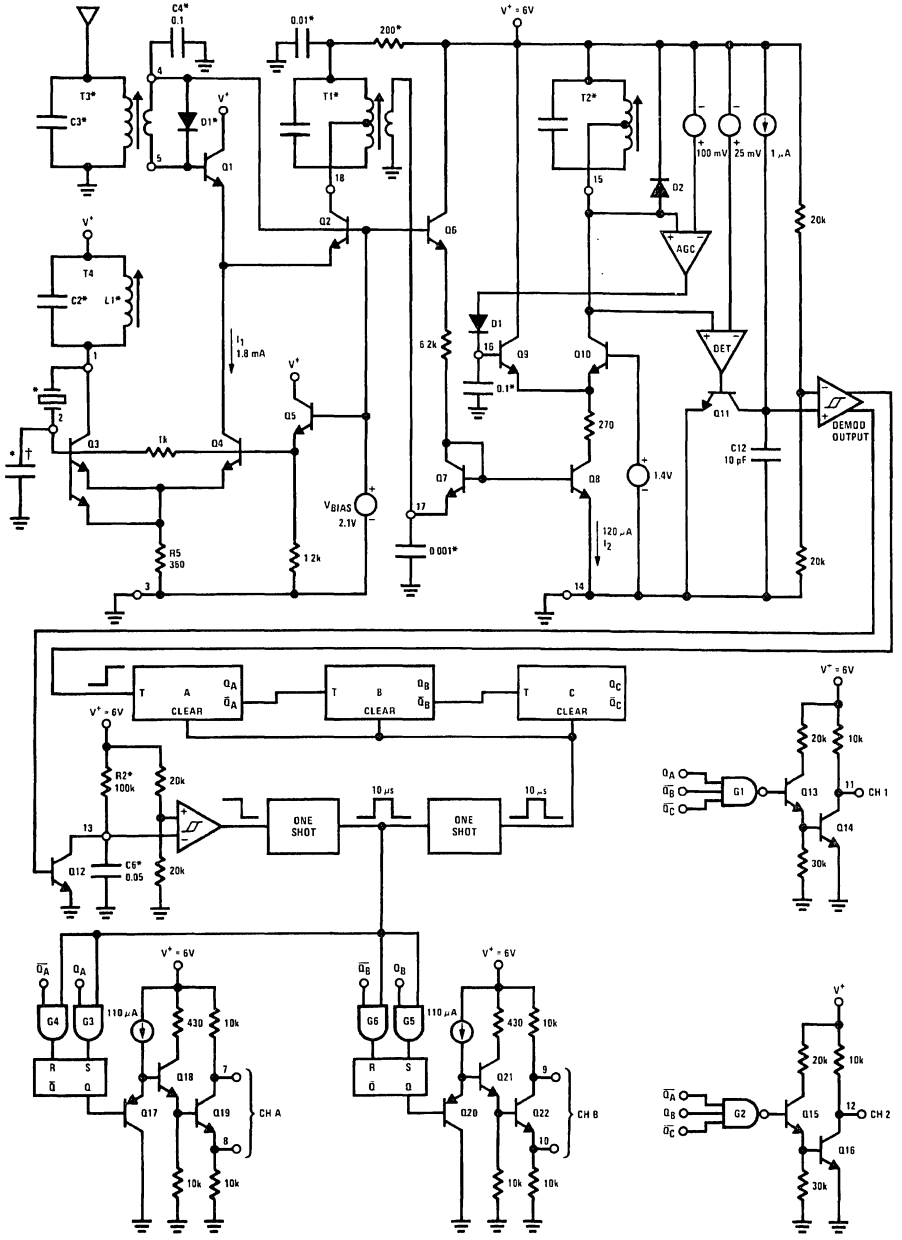
LM1871 TX			LM1872 RX		
Pin Conditions		Transmitted Waveform	Binary Pulse Count	Digital Outputs	
Pin 5 (CH A)	Pin 6 (CH B)			CH A	CH B
OPEN	OPEN	 TL/H/7912–6	100	OFF	OFF
GND	OPEN	 TL/H/7912–7	101	ON	OFF
OPEN	GND	 TL/H/7912–8	110	OFF	ON
GND	GND	 TL/H/7912–9	111	ON	ON

FIGURE 3. Digital Channel Encoding and Decoding via Pulse Count Modulation

Circuit Description (Continued)



TL/H/7912–10

*External parts

†Depending on layout, a small capacitance (10–47 pF) may be required across pins 2 and 3 to ensure oscillator start up.

FIGURE 4. Simplified Schematic Diagram

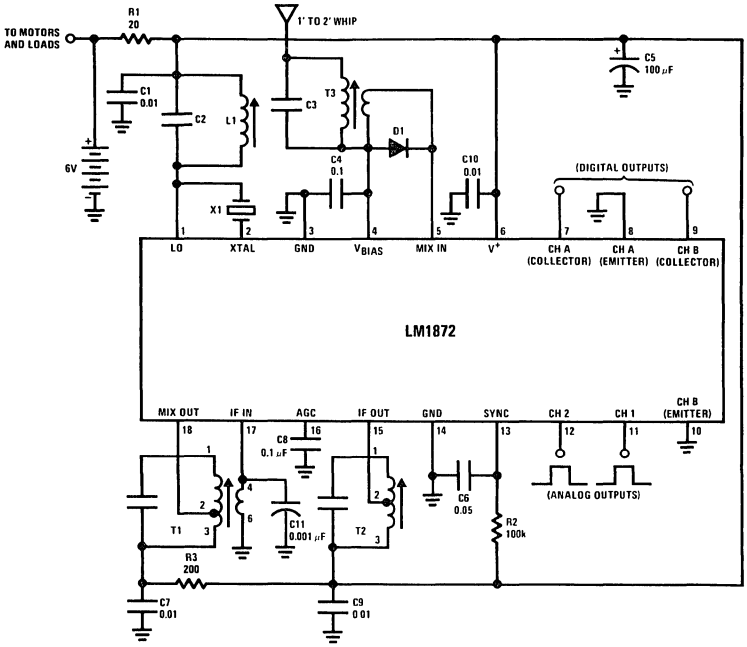
Circuit Description (Continued)

Thus either 3, 4, 5, or 6 channels are transmitted to represent the four possible codes that two digital channels represent. The receiver intrinsically counts channels with its decoder flip-flops by responding to the negative edges of the demodulated RF waveform of which there is always one more than the number of channels. The two LSBs of the binary count are read, latched, and fed to the output drivers which comprise digital channels A and B.

RECEIVER SECTION

The receiver circuit is a simple, single conversion design with AGC which mixes down to 455 kHz and provides 58 dB of gain using the suggested transformers in *Figure 5*. The active digital detector provides an additional 30 dB gain over a silicon diode resulting in an overall system gain of 88 dB. More or less gain can be obtained by using different transformers. The frequency range of operation extends from 50 kHz to 72 MHz encompassing a wide range of allocated frequency bands.

The short (1′ to 2′) vertical whip antenna that is typically used has a very low radiation resistance (0.5Ω to 4Ω) and approximately 3 pF to 5 pF of capacitance. This antenna is coupled to the mixer through a high Q tank consisting of C3



TL/H/7912–11

R1 — Motor decoupling

R2 — Sync timer; $R2 = \frac{t'_{SYNC}}{0.7\ C6'}$ R2 ≤ 470k

R3 — Mixer decoupling

C1 — LO bypass; optional

C2 — LO tank; C2 = 43 pF @ 27 MHz
= 24 pF @ 49 MHz

C3 — Ant. input tank; C3 = 39 pF @ 27 MHz
= 24 pF @ 49 MHz

C4 — V_{BIAS} bypass

C5 — Motor decoupling

C6 — Sync timer; $C6 = \frac{t'_{SYNC}}{0.7\ R2'}$ C6 ≤ 0.5 µF

C7 — Mixer decouple; 0.01 µF ≤ C7 ≤ 0.1 µF

C8 — AGC

C9 — IF bypass; optional

C10 — V^+ bypass; 0.01 µF ≤ C10 ≤ 0.1 µF

C11 — LO bypass

L1 — LO coil
Toko* 10k type (KXNA-4434 DZ) 9T; 0.8 µH @ 27 MHz
Toko* 10k type (KEN-4028 DZ) 6T; 0.4 µH @ 49 MHz
L1 could be made a fixed coil, if desired.

T1 — 455 kHz mixer transformer
Toko* 10 EZC type (RMC-202313 NO), Qu = 110
Pin 1–2, 131T; pin 2–3, 33T
Pin 1–3, 164T; pin 4–6, 5T

T2 — 455 kHz IF transformer
Toko* 10 EZC type (RMC-402503 NO), Qu = 110
Pin 1–2, 98T; pin 2–3, 66T
Pin 1–3, 164T; pin 4–6, 8T

T3 — Ant. input transformer
Toko* 10k type (KXNA-4434 DZ), 3T sec. & 9T pri. of 0.8 µH @ 27 MHz
Toko* 10k type (KEN-4028 DZ), 1½T sec. & 6T pri. of 0.4 µH @ 49 MHz

X1 — 3rd overtone parallel-mode crystal

D1 — Electrostatic discharge (ESD) protection

*Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

FIGURE 5. Typical Application Circuit for 27 MHz or 49 MHz

Circuit Description (Continued)

and T3. This tank effectively keeps strong out-of-band signals such as FM and TV broadcast from cross-modulating with the desired signal. When operating at 49 MHz or 72 MHz, CB interference is also effectively minimized. Image rejection is relatively low, however, being only 7 dB @ 49 MHz, but this does not present a problem due to the usual absence of strong interfering signals 910 kHz below the desired signal.

The antenna signal is stepped down and DC coupled to the mixer which consists of the emitter-coupled pair Q1 and Q2. Emitter-follower, Q1, feeds the common-base device, Q2, while effectively buffering the antenna from the LO energy delivered by Q4. Mixer transconductance is 4 mmhos at low frequency (1 MHz) falling to 3.3 mmhos at the upper end (72 MHz).

The local oscillator utilizes an emitter coupled pair, Q3 and Q4, for accurate control of mixer drive, I_1. Quiescently, Q3 and Q4 share I_1 set by 0.69V/R5, but healthy voltage swings at pin 2 due to oscillation of Q3 implement thorough switching of the differential pair. As a result, the full 1.8 mA of drive "tailgates" (switches) the mixer emitter coupled pair, Q1 and Q2. This current is well regulated from supply voltage changes by the V_{BIAS} circuitry. The TC of V_{BIAS} is positive by design in order to impress a positive TC on I_1 so as to compensate for the temperature dependence of bipolar transconductance in the mixer. Inasmuch as Q4 operates as an emitter-gated, common-base-connected device, excellent isolation between local oscillator and mixer is obtained. As long as pin 4 is properly bypassed, Q5 presents a low impedance to the base of Q4, resulting in low oscillator noise. The oscillator easily operates up to 72 MHz with overtone crystals operating parallel mode.

The mixer signal is stepped down from the high Q mixer tank, T1, and DC coupled to the IF via a secondary winding. The IF stage consists of Q7, Q8 and Q10 and delivers a transconductance of 4 mmhos @ 455 kHz. The quiescent current, I_2, is set at 120 μA by V_{BIAS} and a 6.2k resistor. Again, the positive TC of V_{BIAS} is used to compensate for the temperature dependence of transconductance. The impedance at the IF output, pin 15, is very high ($\geq$800k) permitting the IF transformer, T2, to operate at near unloaded Q (110). The overall 3 dB bandwidth of the receiver section is 3.2 kHz (see characteristic curves); this is narrow enough to permit adjacent channel operation without interference yet wide enough to pass the 500 μs modulation pulses (t_M in *Figure 2*).

The IF signal is DC coupled to the digital detector which consists of a high gain precision comparator, a 30 μs integrator, and a supply-referred 25 mV voltage reference. Whenever the peak IF signal exceeds 25 mV, the comparator drives Q11 to reset the digital envelope detector capacitor, C12. Since it takes 30 μs for the 1 μA current source to ramp C12 to the 3V ($V^+/2$) necessary to fire the Schmitt trigger, the presence of 455 kHz carrier (period = 2.2 μs) greater than 25 mVp will prevent C12 from ever reaching this threshold. When the carrier drops out, the Schmitt trigger will respond 30 μs later. This delay (like that associated with the burst response of the 455 kHz IF tanks) is constant over the time interval of interest. Thus, it is of no consequence to timing accuracy because the LM1872 responds only to negative edges in the decoder.

AGC is provided only to the IF; the mixer having sufficient overload recovery for the magnitude of signals available from a properly operating (i.e. good carrier ON/OFF ratio) 10,000 μV/m transmitter. The AGC differential amplifier regulates the peak carrier level to 100 mV by comparing it to an internal 100 mV supply-referred voltage reference. The resultant error signal is amplified and drives Q9 via rectifier diode, D1, to shunt current away from Q10. C8 provides compensation for the AGC loop which spans a 70 dB range. The 100 mV AGC reference is accurately ratioed to the 25 mV detector reference to permit a controlled amount of brief carrier loss before dropping below detector threshold. Once into AGC, typically 60% amplitude modulation of the PWM carrier is possible before the detector will recognize the interference (see characteristic curves). This kind of noise immunity is invaluable when the troublesome effects of other physically close toys or walkie-talkies on the same or adjacent frequencies are encountered.

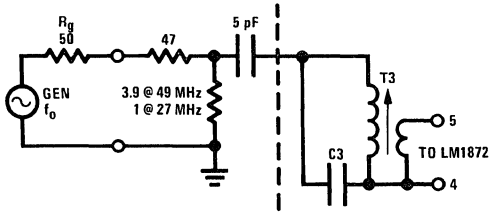
DECODER SECTION

The purpose of the decoder is to extract the time information from the carrier for the analog channels and the pulse count information for the digital channels. The core of the decoder is a three-stage binary counter chain comprising flip-flops A, B, and C. The demodulated output from the detector Schmitt-trigger drives both the counter chain and the sync timer (Q12, R2, C6, and another Schmitt trigger). When the RF carrier drops out for the first modulation pulse, t_M, the falling edge advances the counter (see *Figure 2*). During the t_M interval the sync timer capacitor is held low by Q12. When the carrier comes up again for the variable channel interval, t_{CH}, C6 begins to ramp towards threshold ($V^+/2$) but is unable to reach it in the short time that is available. At the end of the t_{CH} period the carrier drops out again, the counter advances one more, and the sequence is repeated for the second analog channel. To decode the two analog channels, 3-input NAND gates G1 and G2 examine the counter chain binary output so as to identify the time slots that represent those channels. Decoded in this manner, the output pulse width equals the sum of t_M, a fixed pulse, and t_{CH}, a variable width pulse. A Darlington output driver interfaces this repetitive pulse to standard hobby servos.

Following the transmission of the second analog channel, a variable quantity from one to four, of fixed width pulses (500 μs) are transmitted that contain the digital channel information. Up until the end of the pulse group frame period, t_F, the decoder responds as if these fixed pulses were analog channels but delivers no outputs. At the conclusion of the frame the sync pulse, t_{SYNC}, is sent. Since t_{SYNC} is always made longer than the sync timer period (t'_{SYNC} = 3.5 ms), the sync timer will output a sync signal to the first of two cascaded 10 μs one-shots. The first one-shot enables AND gates G3 $\rightarrow$ G6 to read the A and B flip-flops of the counter into a pair of RS latches. The state of flip-flop A, for example, is then stored and buffered to drive 100 mA sink or source at the channel A digital output. An identical parallel path allows the state of flip-flop B to appear at the channel B power output. Upon conclusion of the 10 μs read pulse, another 10 μs one-shot is triggered that resets the counter to be ready for the next frame.

Application Hints

A typical application circuit for either 27 MHz or 49 MHz is shown in *Figure 5*. Using the recommended antenna input networks and driving the circuit through the antenna simulation network of *Figure 6*, a solid decoded output occurs for 10 μV and 12 μV input signals at 27 MHz and 49 MHz respectively.



TL/H/7912–12

FIGURE 6. Antenna Simulation Network

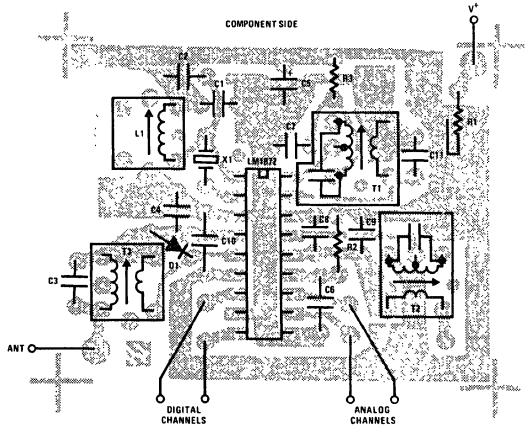
This sensitivity has been determined empirically to be optimum for toy vehicle applications. Less gain will reduce range unacceptably and more gain will increase susceptibility to noise. However, should the application require greater range (>50m for a land vehicle, for example), either the antenna could be lengthened beyond 2′ and/or receiver sensitivity could be improved. There are a number of ways to alter the sensitivity of the receiver. Decreasing the turns ratio of input transformer, T3, for example, will couple more signal into the mixer at the expense of lower tank Q due to mixer loading. Moving the primary tap on mixer transformer, T1, further from the supply side and/or decreasing the primary to secondary turns ratio will also increase gain. For example, just changing T1 from a 32:1 primary to secondary ratio to a 5:1 turns ratio (Toko #RMC202202) will double 49 MHz sensitivity (6 μV vs 12 μV). Mixer tank Q will be affected but overall 3 dB BW will remain largely unchanged.

The primary tap on the IF transformer, T2, can also be adjusted (further from the supply side) for higher gain, but it is possible to cause the AGC loop to oscillate with this method.

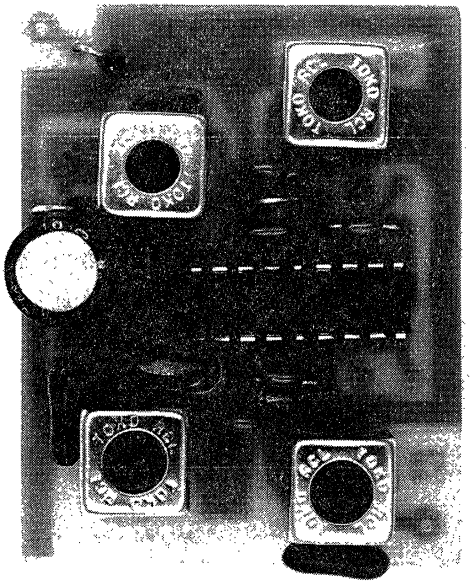
Narrow overall bandwidth is important for good receiver operation. The 3.2 kHz 3 dB bandwidth of the circuit in *Figure 5* is just wide enough to pass 500 μs carrier dropout pulses, t_M, yet narrow enough to hold down electrical noise and reject potentially interfering adjacent channels. In the 49 MHz band, the five frequencies available are only 15 kHz apart. Should only two frequencies be used simultaneously, these channels could be chosen 60 kHz apart. Should three frequencies be used, the spacing could be no more than 30 kHz. At four or five frequencies, 15 kHz spacings must be dealt with, making narrow bandwidth highly desirable. Even at 27 MHz, where allocated frequencies are 50 kHz apart, the proliferation of CB stations only 10 kHz away represents a formidable source of interference. The response of the circuit of *Figure 5* is 34 dB and 56 dB down at 15 kHz and 50 kHz away, respectively (see characteristic curves).

The sync timer should have a timeout, t'_{SYNC}, set longer than the longest channel pulse transmitted, but shorter than the shortest sync pulse, t_{SYNC}, transmitted. Using the component values in *Figure 5*, t'_{SYNC}, = 3.5 ms, which works well with a transmitted sync pulse, $t_{SYNC} \geq 5$ ms.

Numerous bypass capacitors appear in the circuit of *Figure 5*, not all of which may be necessary for good stability and performance. A low cost approach may eliminate one or more of the capacitors C1, C9, C10, and C11. The cleaner and tighter the PCB layout used, the more likely is the case that bypass capacitors can be eliminated. In the case of marginal board stability, increasing the size of capacitors C7, C9, and C10 to 0.1 μF may prove helpful. If the PCB layout and parts loading diagram shown in *Figure 7* is used, the circuit will be quite stable up to 72 MHz.



TL/H/7912–13



TL/H/7912–14

FIGURE 7. PCB Layout, Stuffing Diagram and Complete RX Module for Typical Application Circuit of *Figure 5*

Application Hints (Continued)

The digital channel output devices have significant drive capability; they can typically sink 100 mA and possess a 7Ω saturation resistance. Through their emitters they can source 100 mA up to 1V above ground for driving grounded NPNs and SCRs. Unfortunately, this kind of drive capability can cause thermally induced chip destruction unless total power dissipation is limited to less than 1000 mW. It is good practice and highly recommended to allow the digital output devices to fully saturate at all times (sinking or sourcing) and to limit the current at saturation to no more than 100 mA. For extra drive the two digital outputs can always be summed by connecting pin 7 to pin 9.

The IF frequency is not constrained to be 455 kHz. Operation is limited on the high end to about 1 MHz due to the frequency response limitations of the active detector. The low end is limited to about 50 kHz due to the envelope detector integration time *(Figure 4)*.

RECEIVER ALIGNMENT

The receiver alignment procedure is relatively straightforward because of an absence of interaction between the adjustments. First, the oscillator is tuned by adjusting L1 while monitoring the LO signal at pin 2 with a low capacity (≅10 pF) probe. During tuning the amplitude will rise, peak, and then abruptly quit. Adjust the coil away from the quitting point and just below the amplitude peak.

In order to properly tune T1, T2, and T3, the RF signal must be provided through the receiver antenna by the specific transmitter which is to be used with that specific receiver. This is because the crystals which are commonly used with these systems may have tolerances as loose as ±0.01%. At 49 MHz the resultant ±5 kHz deviation could easily put the incoming signal out of the 3.2 kHz receiver IF bandpass. The signal should be coupled through the receiving antenna to ensure proper loading of the T3 input tank.

Alignment is easier with a defeated AGC, which is accomplished by merely grounding pin 16. The amplitude of the 455 kHz signal at pin 15 is used to guide alignment. Care should be exercised that the signal swing not exceed roughly 400 mVp or diode, D2, in *Figure 4* will threshold and clamp the waveform. Also note that a standard 10 pF probe at pin 15 will shift the IF tank frequency an undesirable 2 kHz. Unless a lower capacity probe is available, it is recommended that the signal be monitored at the unused secondary of T2. Although the signal amplitude would be down by a factor of 8.25 relative to pin 15, up to 50 pF probe capacitance could be tolerated with negligible frequency shift.

The incoming signal is obtained by removing the antenna from the transmitter and then locating the transmitter at a sufficient distance from the receiver to give a convenient signal level (≤400 mVp) at pin 15. T3, T1, and T2 are then tuned for maximum signal.

Applications

OPERATION AT 72 MHz

The licensed 72 MHz band is popular among hobby enthusiasts for controlling aircraft. The higher transmitted power levels that the FCC allows yield much greater operating range and the frequency band is uncluttered relative to 27 MHz. Elevated frequencies such as 72 MHz are no problem with the LM1872. The part is stable and will provide good sensitivity and selectivity at that frequency. The application circuit in *Figure 8* will provide a set of solid decoded outputs for <2 μV of signal at the antenna input, which is designed to match the 100Ω resistive impedance of the ¼ wavelength antenna. IF bandwidth is a respectable 3.2 kHz. For good immunity to overload from a very closely (antennas touching) operating high power transmitter, the transmitter design should emphasize a high carrier ON/OFF ratio. Using the LM1871 as a low power exciter to drive one or more external class C power amplifier stages will result in a simple, acceptable, low cost transmitter at 72 MHz.

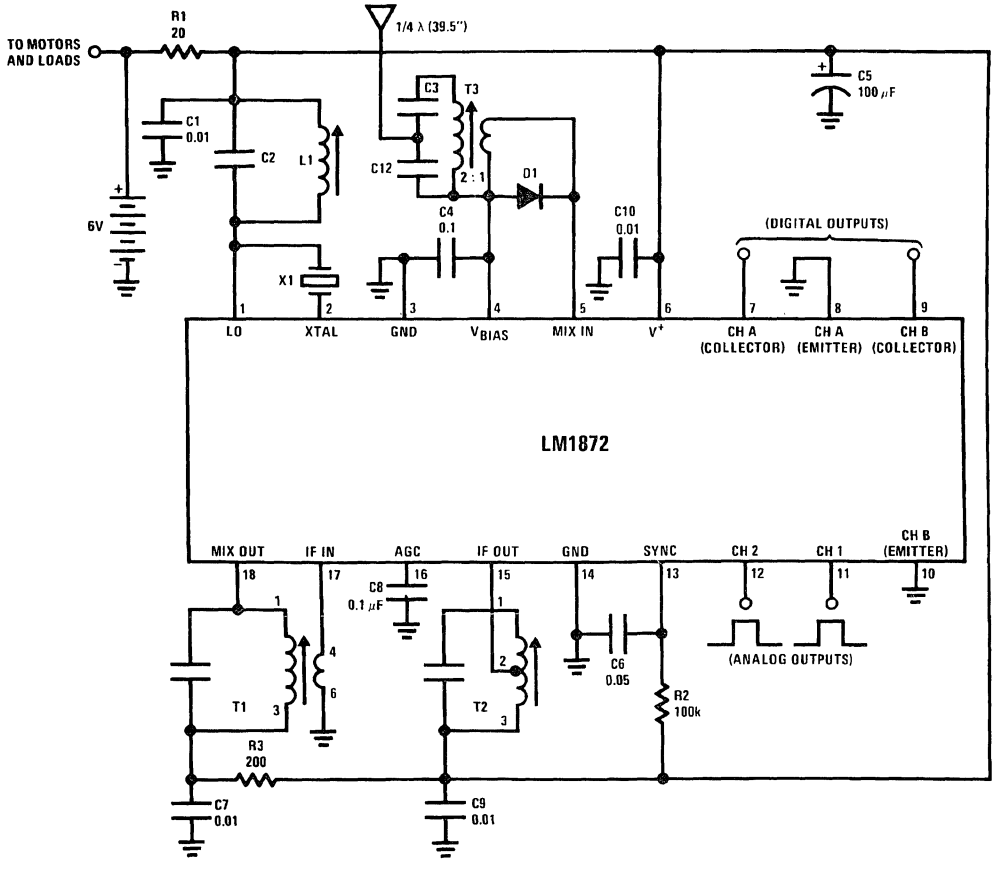
Inasmuch as many hobby applications require more analog channels than the LM1872 normally provides, particular attention should be paid to *Figures 10 and 12* which describe how to expand analog channel capacity up to 4 and 6 channels, respectively.

OPERATION WITH AN IR CARRIER

An infra-red (or visible) light data link is a useful alternative to its RF counterpart. Should the application demand that the radiation not leave the room, or that it be directional, or not involve FCC certification then a light carrier should be given consideration. The principal drawbacks to this approach include short range (≤20 ft.) and high transmitter power consumption. There is little that can be done to dramatically improve range, but short burst-type operation of the transmitter will still permit battery operation.

The information link *(Figure 9a)* consists of a light carrier amplitude modulated by a 455 kHz subcarrier. The subcarrier in turn is modulated by the normal Pulse Width/Pulse Count Scheme produced by the LM1871 encoder. A husky, focused LED is used as the transmitter running Class A 100% modulated with an average current drain of 50 mA to 500 mA depending upon range requirements. The detector consists of a large area silicon PN or PIN photodiode for good sensitivity. The LM1872 will directly interface to such a diode and give very good performance. Only a few nanoamps of photo current from D1 are required to threshold the detector. Ambient light rejection is excellect due to the very narrow bandwidth (≅3 kHz) that results from the use of three high Q 455 kHz transformers, T1, T2, and T3. Note that the LO has been defeated and the mixer runs as a conventional 455 kHz amplifier. Otherwise, circuit operation is the same as if an RF carrier were being received.

Applications (Continued)



TL/H/7912–15

R1 — Motor decoupling

R2 — Sync timer; $R2 = \frac{t'_{SYNC}}{0.7\ C6'}$ R2 ≤ 470k

R3 — Mixer decoupling

C1 — LO bypass; optional

C2 — LO tank; C2 = 22 pF @ 72 MHz

C3 — Ant. input tank; C3 = 24 pF @ 72 MHz

C4 — V_{BIAS} bypass

C5 — Motor decoupling

C6 — Sync timer; $C6 = \frac{t'_{SYNC}}{0.7\ R2'}$ C6 ≤ 0.5 μF

C7 — Mixer decouple; 0.01 μF ≤ C7 ≤ 0.1 μF

C8 — AGC

C9 — IF bypass; optional

C10 — V^+ bypass; 0.01 μF ≤ C10 ≤ 0.1 μF

C12 — Ant. input tank; C12 = 160 pF @ 72 MHz

L1 — LO Coil
Toko 10k type (KENC) 4T; 0.2 μH @ 72 MHz
L1 could be made a fixed coil, if desired

T1 — 455 kHz mixer transformer
Toko 10 EZC type (RMC-502182), Qu = 110
Pin 1–2, 82T; pin 2–3, 82T
Pin 1–3, 164T; pin 4–6, 30T

T2 — 455 kHz IF transformer
Toko 10 EZC type (RMC-502503), Qu = 110
Pin 1–2, 82T; pin 2–3, 82T
Pin 1–3, 164T; pin 4–6, 8T

T3 — Ant. input transformer
Toko 10k type (KENC), 4T sec &
2T pri. of 0.2 μH @ 72 MHz

X1 — 5th overtone crystal, parallel-mode, 72 MHz

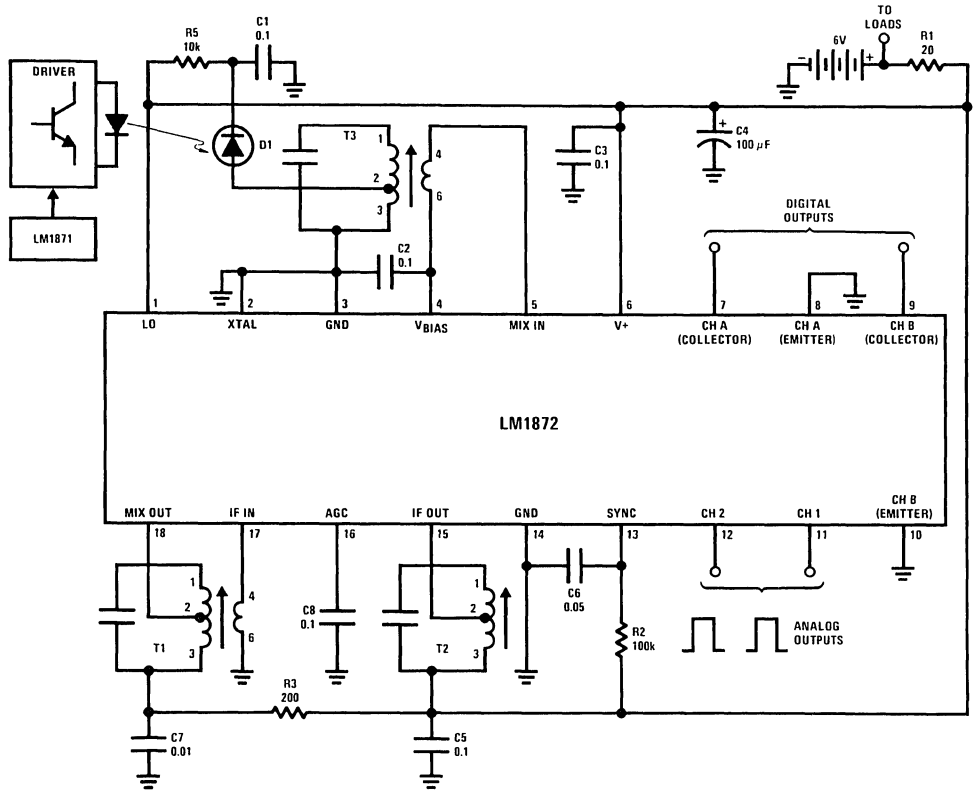
D1 — Electrostatic discharge (ESD) protection

FIGURE 8. 72 MHz Receiver Circuit

In a practical remote data link, the transmitter could be battery operated and set up to transmit for brief intervals only in order to save power. The brief transmission could be used to set or reset the digital output latches in the LM1872 and/or command new motor positions via the analog channels. After transmission, the commands would be stored electrically in the case of the digital channels and mechanically in the case of the analog channels.

As a final note, if the case of D1 is connected to the anode rather than the cathode, the circuit of *Figure 9b* should be used at the input to maintain electromagnetic shielding.

Applications (Continued)



TL/H/7912–16

Bottom View

FIGURE 9a. IR Type Data Link

R1 — Load decoupling

R2 — Sync timer; $R2 = \frac{t}{0.7\ C6}$, $R2 \leq 470k$

R3 — Preamp decoupling

R5 — Photodiode decoupling

C1 — Photodiode decoupling

C2 — V_{BIAS} bypass

C3 — V^+ bypass

C4 — Load decoupling

C5 — IF bypass; optional

C6 — Sync timer; $C6 = \frac{t_{SYNC}}{0.7\ R2}$, $C6 \leq 0.5\ \mu F$

C7 — Preamp decoupling

C8 — AGC

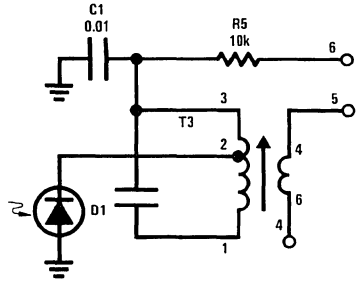
T1 — 455 kHz preamp transformer
Toko 10 EZC type (RMC-502182), Qu = 110
Pin 1–2, 82T; pin 2–3, 82T
Pin 1–3, 164T; pin 4-6, 30T

T2 — 455 kHz IF transformer
Toko 10 EZC type (RMC-402503), Qu = 110
Pin 1–2, 98T; pin 2–3, 66T
Pin 1–3, 164T; pin 4–6, 8T

T3 — 455 kHz input transformer
Toko 10 EZC type (RMC-202313), Qu = 110
Pin 1–2, 131T; pin 2–3, 33T
Pin 1–3, 164T; pin 4–6, 5T

D1 — PN or PIN Silicon Photodiode

Photodiode, D1		Active Area (cm^2)
Vactec	VTS 5088	0.18
Vactec	VTS 6089	0.52
UDT	PIN 6D or 6 DP	0.20
UDT	PIN 220 DP	2.0
Siemens	BPY 12	0.20



TL/H/7912–17

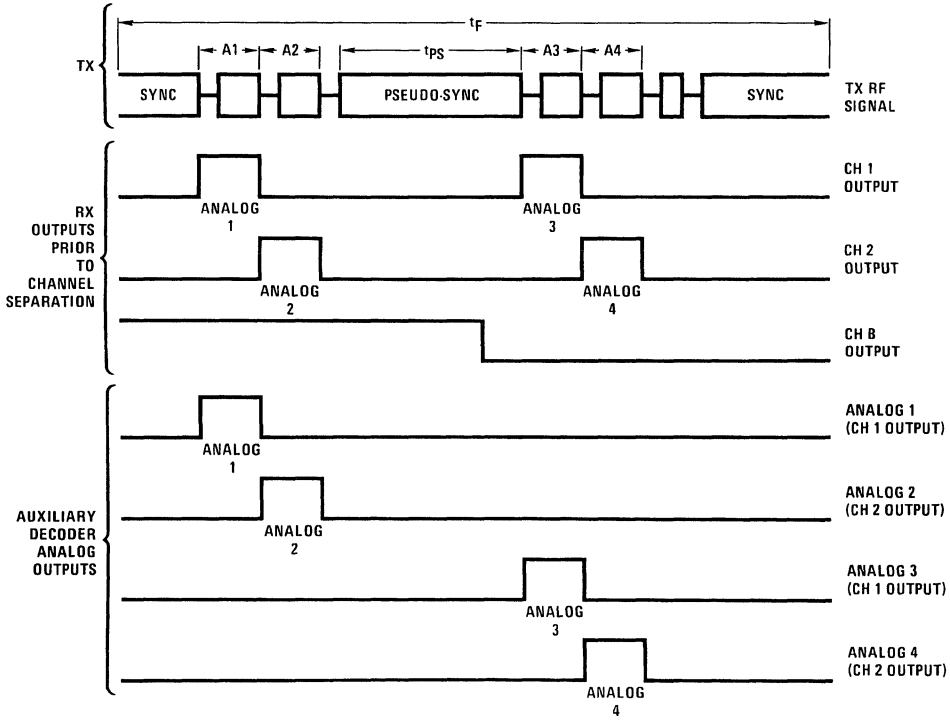
FIGURE 9b. Input Stage Where the Case of D1 is Connected to the Anode

Applications (Continued)

EXPANSION TO FOUR ANALOG CHANNELS

For those applications that require more than the two analog channels that are normally provided, the LM1872 can easily be expanded to 4 channels with appropriate external circuitry. This is accomplished by creating a pseudo-sync pulse (t_{PS}) among a six channel transmitted frame from the LM1871 *(Figure 10)*. The pseudo-sync pulse deceives the decoder in the LM1872 causing premature recognition of end-of-frame, effectively splitting a single frame into two. The idea is to transmit analog channels 1 and 2 in the first half of the normal frame period and analog channels 3 and 4 in the second half. External logic will then steer the four channels from the LM1872's only two analog output pins into four new analog outputs. Steering is accomplished with the help of one of the digital channels. Inasmuch as the digital channels respond only to the *number* of pulses received between any two sync (or pseudo-sync!) pulses, the channels are capable of toggling in step with the alternating transmission of two and three channel pulse mini-groups occurring within each half frame. *Figure 10a* reveals that both digital channels A and B are high during the dual pulse half frame and low during its triple pulse counterpart. *Figure 10b* shows just how simple the external circuitry can be. Digital channel B drives the channel select pin of a quad 2-input MUX that routes the LM1872 channels 1 and 2 outputs to the four new outputs labeled analog 1 through 4.

Although not the model of simplicity of *Figure 10b, Figure 10c* is a lower cost alternative that works just as well. The diodes with the asterisk prevent a ground step from occurring that could false trip an excessively edge sensitive servo and can be eliminated in many cases.

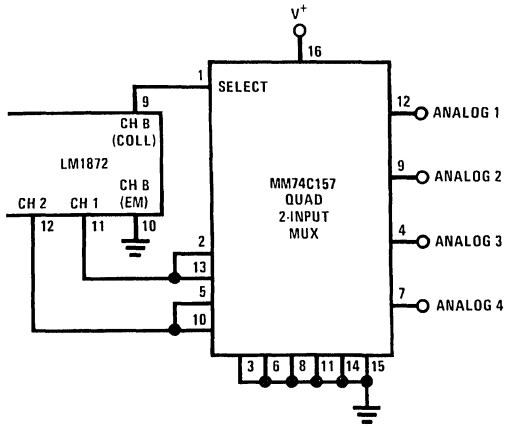


TL/H/7912–18

a) Transmitter, Receiver, and Auxiliary Decoder Timing Diagram

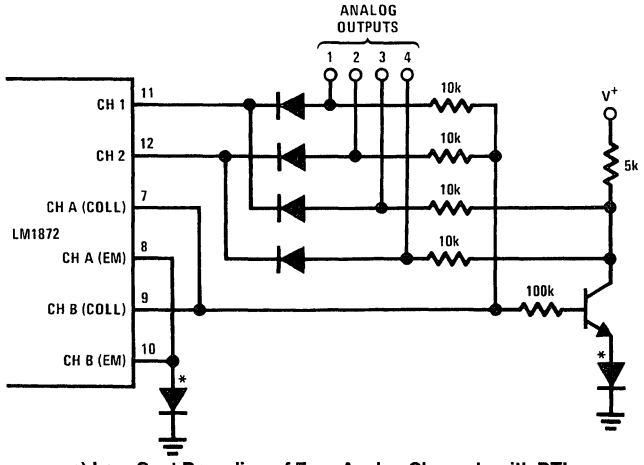
FIGURE 10. Deriving Four Analog Channels Through the Use of an Auxiliary Decoder

Applications (Continued)



TL/H/7912-19

b) Simple Decoding of Four Analog Channels with CMOS



*See Text
TL/H/7912-20

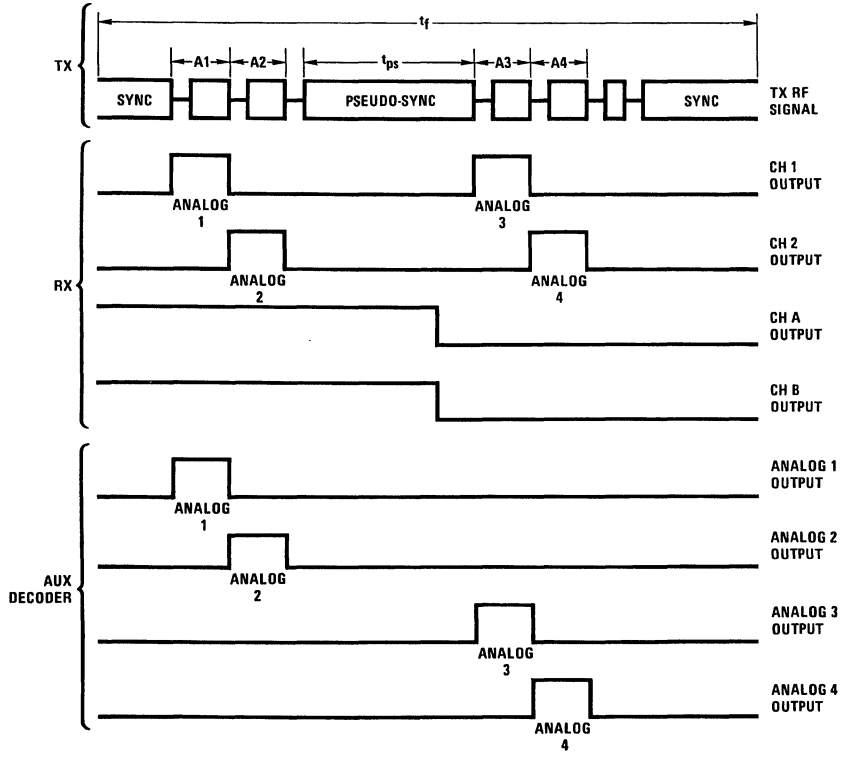
c) Low-Cost Decoding of Four Analog Channels with DTL

FIGURE 10. Deriving Four Analog Channels Through the Use of an Auxiliary Decoder (Continued)

FOUR SINGLE CHANNEL RECEIVERS DRIVEN FROM A SINGLE TRANSMITTER

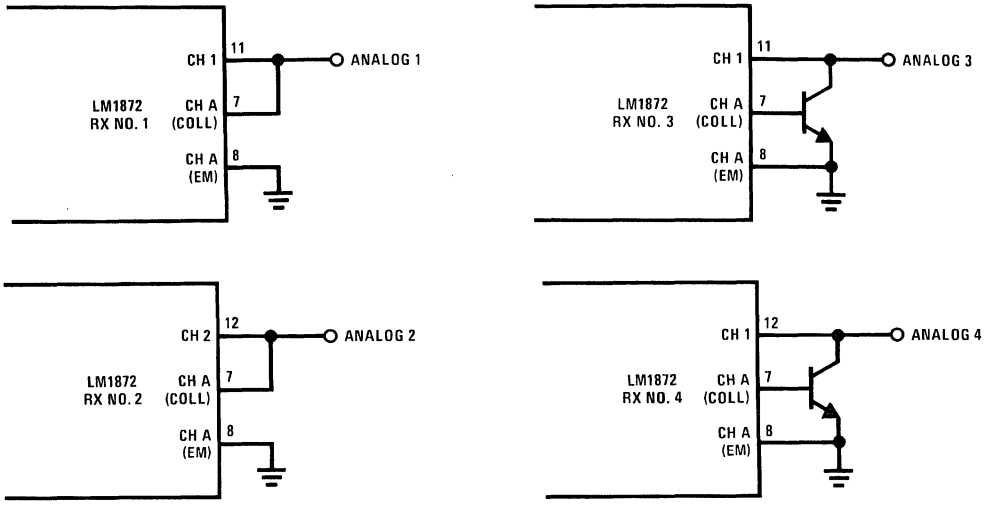
When it is desired to control more than two vehicles or remote stations with the analog information from a single transmitter, the LM1872 can be put to the task. By utilizing the frame splitting technique previously described in *Figure 10*, up to four independent single analog channel receivers can be made to operate from a single transmitter *(Figure 11)*. Toggling digital channel A, either directly or through an inversion, is used to suppress a given receiver's analog output when the undesired analog channels are transmitted. In this manner, only the desired analog channel is outputted at each receiver. The amount of external circuitry required to do this is minimal; two receivers require a single transistor apiece while the other two receivers need no extra parts at all.

Applications (Continued)



TL/H/7912–21

a) Transmitter, Receiver, and Separated Channels Timing Diagram



TL/H/7912–22

b) Simple Channel Separation with Two External Transistors

FIGURE 11. Obtaining Four Independent Single Analog Channel Receivers from a Single Common Transmitter

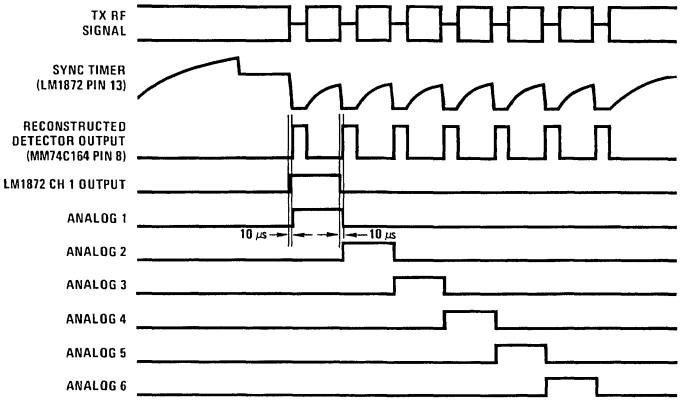
Applications (Continued)

EXPANSION TO SIX ANALOG CHANNELS

Still greater analog capacity can be obtained with an outboard auxiliary decoder. The LM1872, a simple comparator, and an 8-bit parallel-out serial shift register comprise a six analog channel receiver/decoder *(Figure 12)*. The one transistor comparator reconstructs the detector output of the LM1872 from the sync timer waveform and feeds it to the clock input of the shift register. The channel 1 output then loads a "one" into the register and the clock shifts the "one" down the line of analog channel outputs in accordance with the time information from the detector output. Note that the reconstructed detector waveform lags the channel 1 output very slightly ($\cong 10\ \mu s$) due to the finite slope of the sync capacitor discharge edge. This delay is very important as it insures that channel 1 is high when the clock strikes initially (thus loading a "1") and low for each subsequent positive clock edge (thus preventing the loading of extraneous "1's").

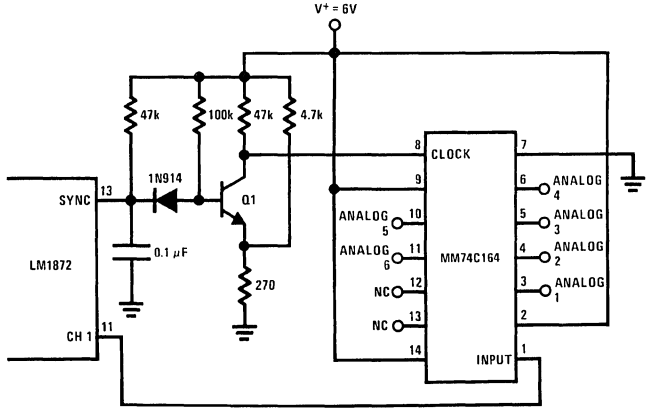
CONVERTING AN ANALOG CHANNEL TO A DIGITAL CHANNEL

Either analog channel can be converted to a digital channel with the aid of a low cost CMOS hex inverter *(Figure 13)*. The internal 10k resistor and external capacitor, C1, set a time constant (1 ms) that falls between a short (0.5 ms) and a long (2 ms) transmitted pulse option. For pulses longer than 1 ms, the first inverter will pull low momentarily once each frame. Repetitive discharges of C2 prevent it from ever reaching threshold ($V^+/2$) because the R1 C2 time constant is set longer (70 ms) than the frame period. With the inverter input below threshold, Q1 will energize the load. For analog output pulses shorter than 1 ms, the first inverter will back bias D1 allowing C2 to ramp past threshold and Q1 to go off. For extra output drive, the remaining inverters in the package can be paralleled to drive Q1. Alternatively, for light loads Q1 can be eliminated altogether.



TL/H/7912–23

a) Six Channel Timing Diagram



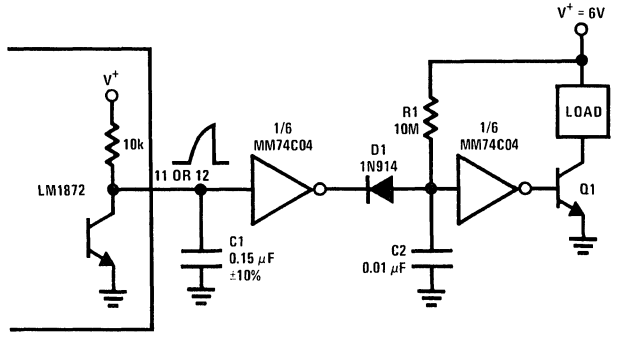
TL/H/7912–24

b) Six Channel Auxiliary Decoder

FIGURE 12. Deriving Six Analog Channels

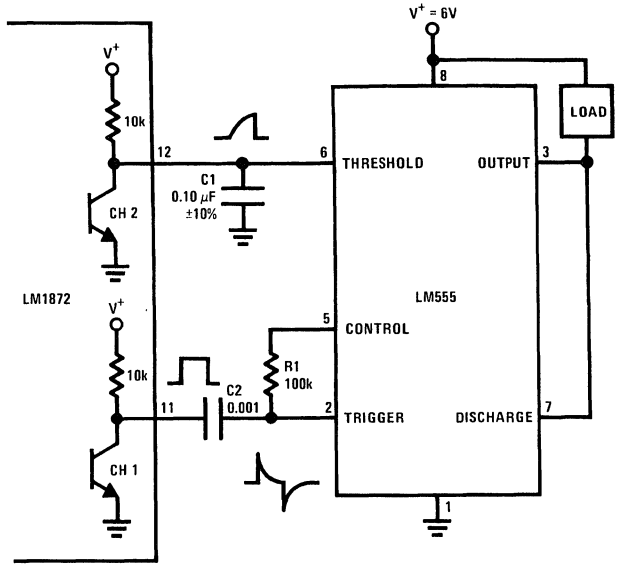
Applications (Continued)

Where only one of the two available analog channels needs conversion to a digital format, the LM555 approach offers simplicity combined with up to 150 mA of output drive *(Figure 14)*. The trailing edge of CH 1's output pulse is used to reset the timer in preparation for comparing CH 2's pulse width to the time constant (1.1 ms) set by the internal 10k resistor and C1. For CH 2 pulse widths greater than 1.1 ms C1 ramps to threshold, setting an internal latch in the LM555 and causing the load to be energized. Due to the timing of the reset pulse, however, the LM555 output will go high again for 1.1 ms during the next pulse comparison cycle thus producing an ON state duty cycle of about 95%. For most commonly encountered loads such as motors, solenoids, lamps, and horns, this is of little consequence. The OFF state duty cycle is 100%.



TL/H/7912-25

FIGURE 13. Conversion of an Analog Channel to a Digital (On/Off) Channel



TL/H/7912-26

FIGURE 14. Simple Conversion of an Analog to a Digital Channel

Applications (Continued)

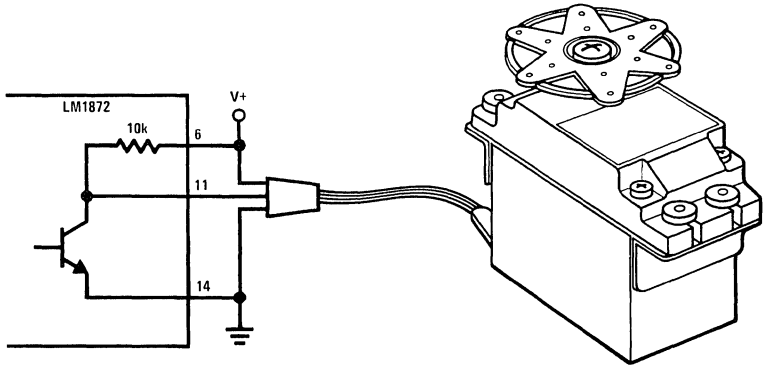
BRIDGE DRIVING A MOTOR

The two digital channels can be used to propel a car forward, off, and reverse without the need for a costly servo *(Figure 16)*. The 100 mA digital output capability is used to drive a bridge of four transistors with Q5 added as a protection device. Should an erroneous command to power both sides of the bridge occur (as may happen due to noise with the car out of range) the large motor drive transistors would fight one another resulting in the thermal destruction of one or more of those devices. But Q5 will disable the left side of the bridge whenever the right side is powered, preventing the problem from ever occurring. The motor noise suppression network shown has proven to be especially effective in reducing electrical noise and is therefore highly recommended.

NOISE INTEGRATION OF A DIGITAL CHANNEL

Commonly available inexpensive DC motors are a formidable source of electromagnetic interference. Radiation can come from the power feed leads and/or directly from the brushes. Usually proper lead dress and board orientation coupled with a good filter network (*see Figure 16*) will eliminate any problems. In particularly stubborn cases of motor interference, the digital channels may experience more objectionable interference than the analog channels. This is generally not because the digital channels are more susceptible, but rather because the type of load they typically drive (i.e. a horn) will make more of a nuisance of itself than a typical analog load (i.e. a steering servo) when subjected to interference.

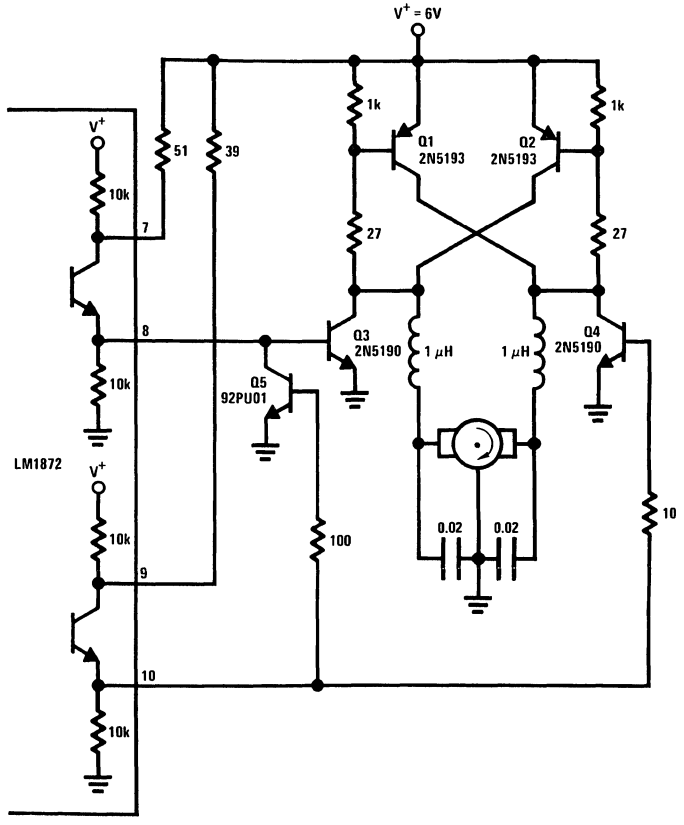
Straightforward time integration of the digital channel outputs works very well with any type or degree of motor interference. The simple circuits of *Figure 17* integrate over a period of about three frames (70 ms) and have approximately equal delay either going off or coming on.



TL/H/7912–27

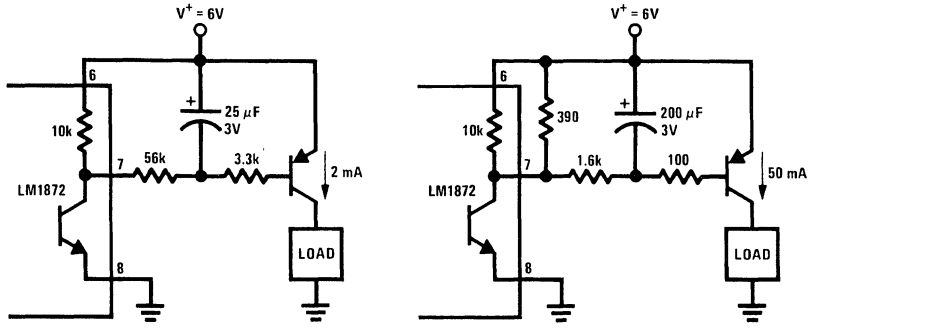
FIGURE 15. Interfacing Directly to Standard Hobby Servos

Applications (Continued)



TL/H/7912–28

FIGURE 16. Digital Bridge Motor Drive



TL/H/7912–29

a) Low Current Load **b) High Current Load**

FIGURE 17. Integrating a Digital Channel Output to Achieve Noise Immunity

National Semiconductor Corporation

LM1884 TV Stereo Decoder

General Description

The LM1884 is a decoder designed for television stereo. An L-R output is provided to drive further audio processing.

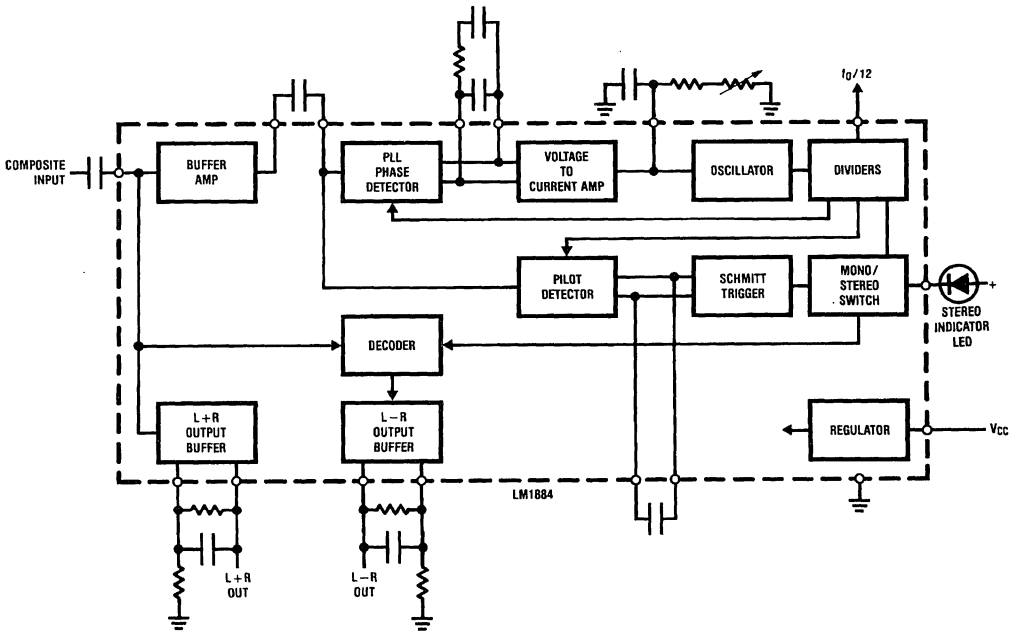
Features

- Low impedance L+R and L−R outputs
- Mono/Stereo switching and indication
- Low distortion—0.10% typical

Applications

- Stereo television sets
- Stereo adapters
- Cable television
- Auto sound

Block Diagram



TL/H/6759–1

Order Number LM1884N
See NS Package Number N16A

Absolute Maximum Ratings $T_A = +25°C$ unless otherwise noted

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

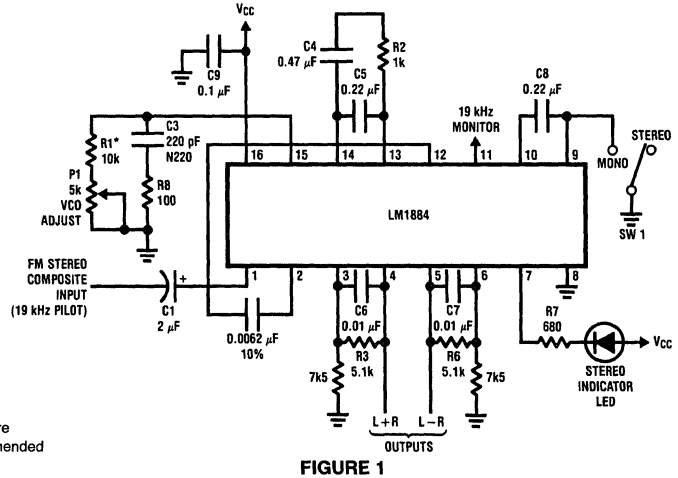
Power Supply Voltage	16V
Power Dissipation (Package Limitation)	1800 mW
Derate Above $T_A = +25°C$	15 mW/°C
Operating Temp. Range (Ambient)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lamp Drive Voltage	
Max Voltage at Pin 7 with Lamp "Off"	16V
Lamp Current	100 mA
Lead Temperature (Soldering 10 sec.)	260°C

Electrical Characteristics

Parameters Guaranteed by Electrical Testing Test Circuit, $T_A = +25°C$, $V_{CC} = 12V$ unless noted

Parameter	Conditions	Min	Typ	Max	Units
DC	$V_{IN} = 0$				
Supply Current	$V_{CC} = 16V$	15	33.5	50	mA
Output Voltage	Pin 4	1.7	3.5	5.0	V
Output Voltage	Pin 5	1.7	3.8	5.0	V
Output Impedance	Pins 4, 5		100	300	Ω
Lamp Leakage	Lamp off, pin 7 voltage = 16V			0.1	mA
Lamp Saturation Voltage	Lamp on, pin 7 current = 100 mA			2.0	V
Audio Composite signal with 38 kHz subcarrier and 10% 19 kHz pilot, fmod = 1 kHz. Adjust P1 for 19 kHz ±10 Hz.					
L+R Channel Gain	$V_{IN} = 2.5Vpp$ L = R, pilot off, pin 4	0.8	1.0	1.2	
L+R Channel THD	$V_{IN} = 2.5Vpp$ L = R, pilot off, pin 4		0.1	1.0	%
Gain Ratio, L+R Channel to L−R Channel	$V_{IN} = 2.5Vpp$, L only	−2.0	0.0	2.0	db
Supply Rejection	100 mVrms, 1 kHz on supply, $V_{IN} = 0$	30	60		db
DC Output Shift, Mono to Stereo	Pilot off to on, pins 4, 5			±20	mV
Input Impedance	Pin 1	15	50	150	kΩ
PLL					
Pilot Level for Lamp On		12		20	mV
Pilot Level for Lamp Off		3		10	mV
Capture Range	Pilot = 25 mVrms	±0.5			%

Test Circuit

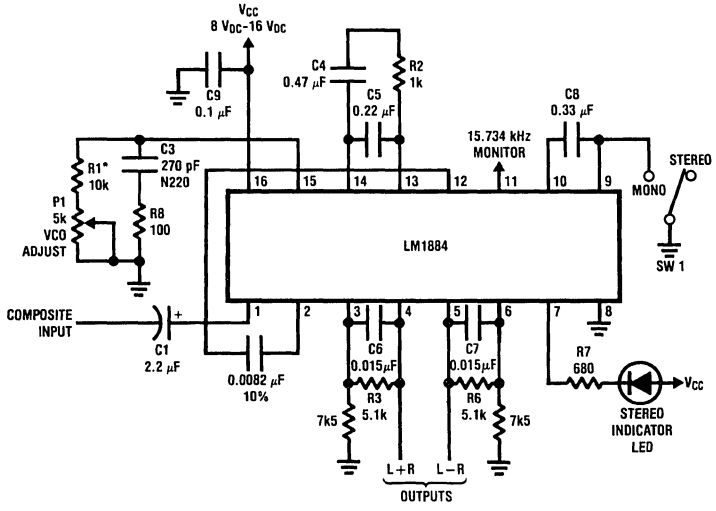


*Metal film, zero temperature coefficient resistor recommended

TL/H/6759–3

FIGURE 1

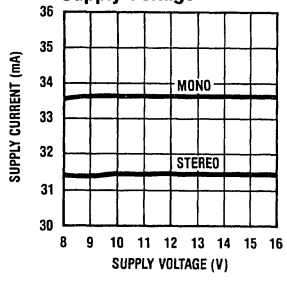
Typical Application



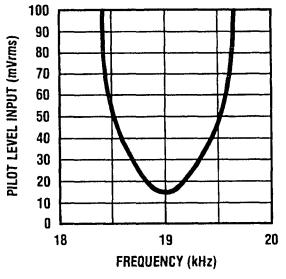
TL/H/6759–2

* Metal film, zero temperature coefficient resistor recommended

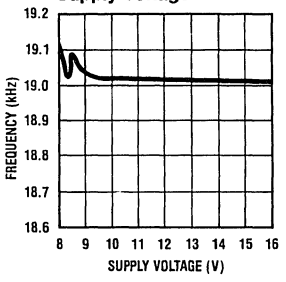
Supply Current vs Supply Voltage



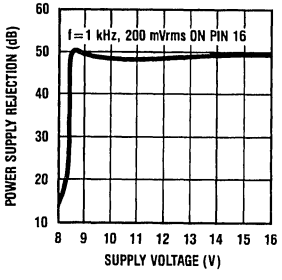
Capture Range vs Pilot Level



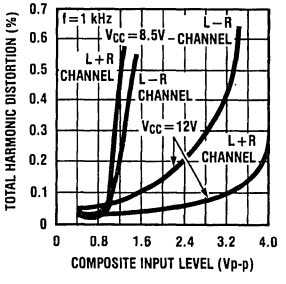
VCO Frequency vs Supply Voltage



Power Supply Rejection vs Supply Voltage



Total Harmonic Distortion vs Composite Input Level



TL/H/6759–4

National Semiconductor Corporation

LM3089 FM Receiver IF System

General Description

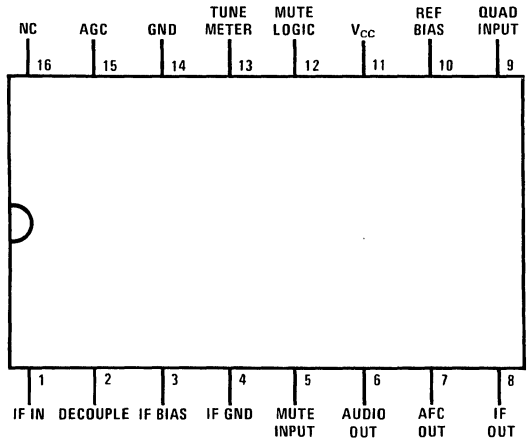
The LM3089 has been designed to provide all the major functions required for modern FM IF designs of automotive, high-fidelity and communications receivers.

Features

- Three stage IF amplifier/limiter provides 12 μV (typ) −3 dB limiting sensitivity
- Balanced product detector and audio amplifier provide 400 mV (typ) of recovered audio with distortion as low as 0.1% with proper external coil designs.
- Four internal carrier level detectors provide delayed AGC signal to tuner, IF level meter drive current and interchannel mute control
- AFC amplifier provides AFC current for tuner and/or center tuning meters
- Improved operating and temperature performance, especially when using high Q quadrature coils in narrow band FM communications receivers
- No mute circuit latchup problems
- A direct replacement for CA3089E

Connection Diagram

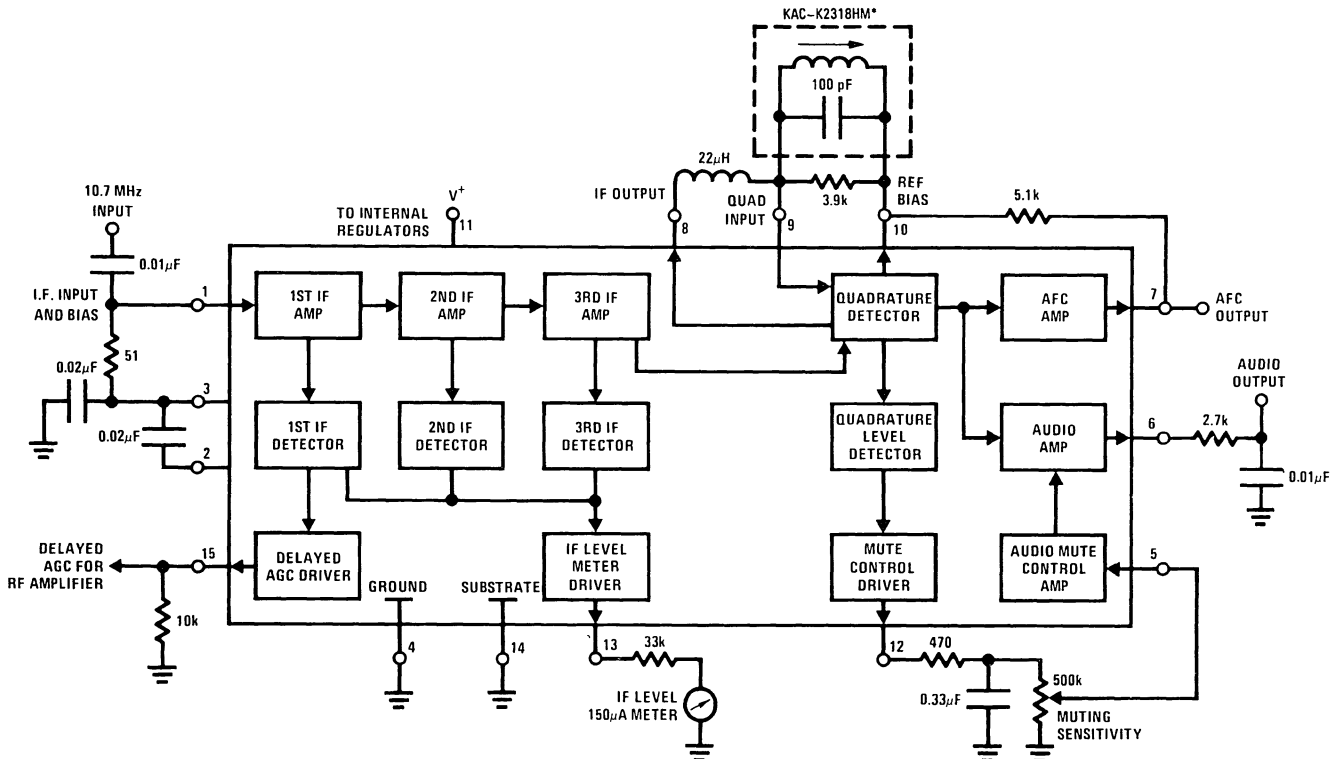
Dual-In-Line Package



TL/H/7149–2

Top View

Order Number LM3089N
See NS Package Number N16E



TL/H/7149–1

Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage Between Pin 11 and Pins 4, 14	+16V
DC Current Out of Pin 12	5 mA
DC Current Out of Pin 13	5 mA
DC Current Out of Pin 15	2 mA
Power Dissipation (Note 2)	1500 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +12V, see Test Circuit)

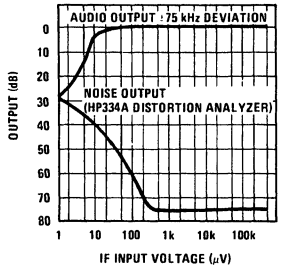
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC CHARACTERISTICS (V_{IN} = 0, NOT MUTED)						
I_{11}	Supply Current		16	23	30	mA
V1, 2, 3	IF Input and Bias		1.2	1.9	2.4	V
V6	Audio Output		5.0	5.6	6.0	V
V7	AFC Output		5.0	5.6	6.0	V
V10	Reference Bias		5.0	5.6	6.0	V
V12	Mute Control		5.0	5.4	6.0	V
V13	IF Level			0	0.5	V
V15	Delayed AGC		4.2	4.7	5.3	V
DYNAMIC CHARACTERISTICS f_o = 10.7 MHZ, Δf = ±75 kHz @ 400 Hz						
V_{IN}(LIM)	Input Limiting −3 dB			12	25	μV
AMR	AM Rejection	V_{IN} = 100 mV, AM: 30%	45	55		−dB
V_O(AF)	Recovered Audio	V_{IN} = 10 mV	300	400	500	mVrms
THD	Total Harmonic Distortion					
	Single Tuned (Note 1)	V_{IN} = 100 mV		0.5	1.0	%
	Double Tuned (Note 1)	V_{IN} = 100 mV		0.1	0.3	%
S+N/N	Signal to Noise Ratio	V_{IN} = 100 mV	60	70		dB
V12	Mute Control	V_{IN} = 100 mV		0	0.5	V
V13	IF Level	V_{IN} = 100 mV	4.0	5.0	6.0	V
V13	IF Level	V_{IN} = 500 μV	1.0	1.5	2.0	V
V15	Delayed AGC	V_{IN} = 100 mV		0.1	0.5	V
V15	Delayed AGC	V_{IN} = 30 mV		2.5		V
V_O(AF)	Audio Muted	V_{IN} = 100 mV, V5 = +2.5V		60		−dB

Note 1: Distortion is a function of quadrature coil used.

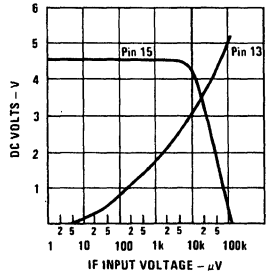
Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Typical Performance Characteristics

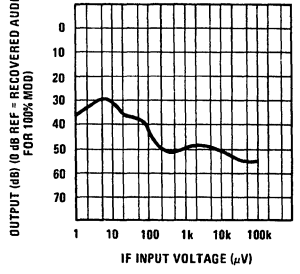
Typical S + N/N and IF Limiting Sensitivity vs IF Input Signal



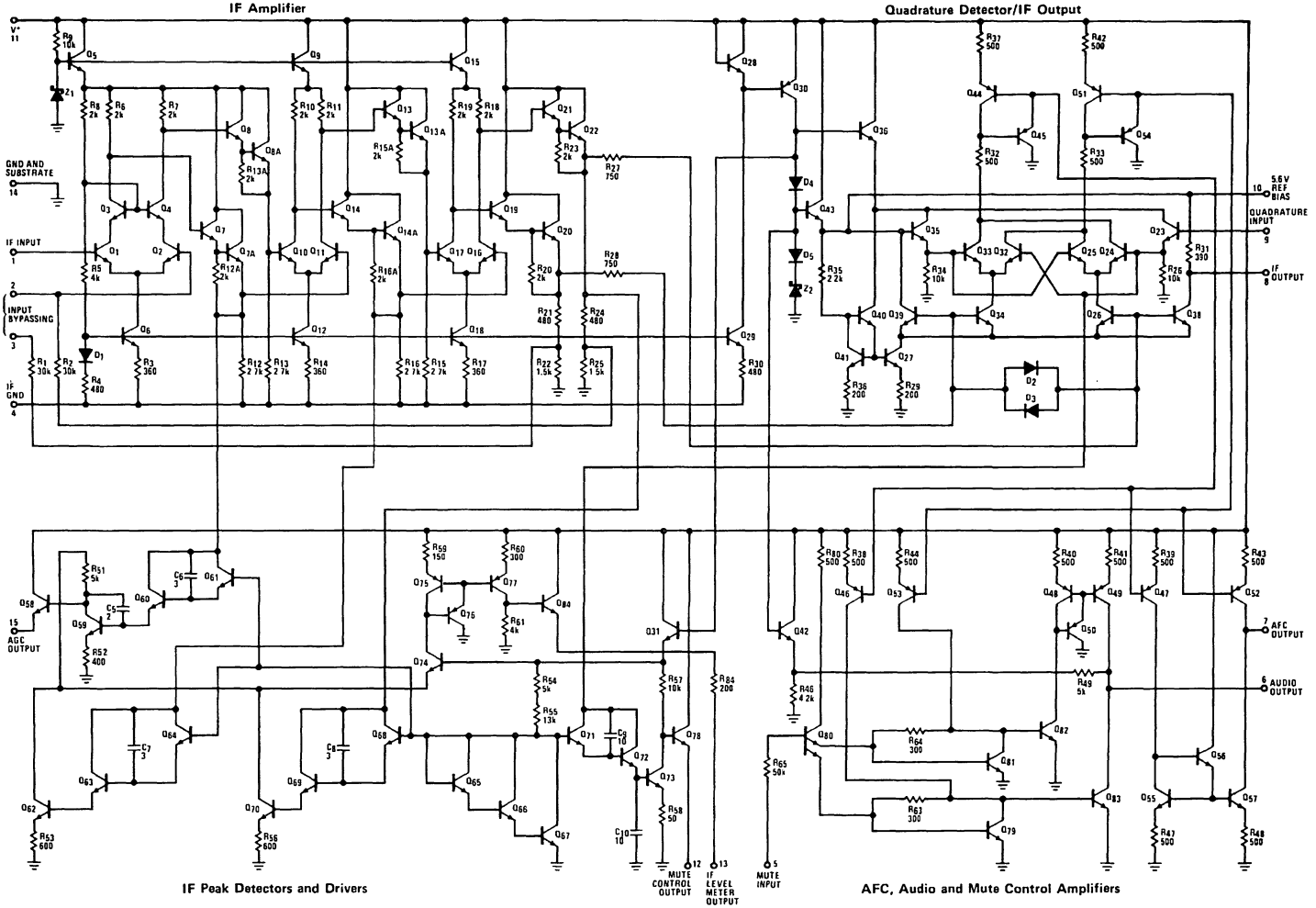
Typical AGC (Pin 15) and Meter Output (Pin 13) vs IF Input Signal



AM Rejection (30% Mod) vs IF Input Signal

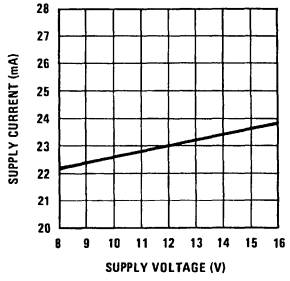


TL/H/7149–3

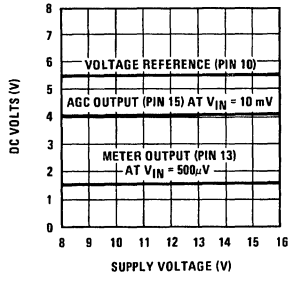

IF Amplifier
Quadrature Detector/IF Output
V+
11
GND AND SUBSTRATE
14
IF INPUT
1
2
INPUT BYPASSING
3
IF GND
4
5.6V REF BIAS
10
QUADRATURE INPUT
9
IF OUTPUT
8
AGC OUTPUT
15
AFC OUTPUT
7
AUDIO OUTPUT
6
MUTE CONTROL OUTPUT
12
IF LEVEL METER OUTPUT
13
MUTE INPUT
5
IF Peak Detectors and Drivers
AFC, Audio and Mute Control Amplifiers
TL/H/7149-4

Typical Performance Characteristics

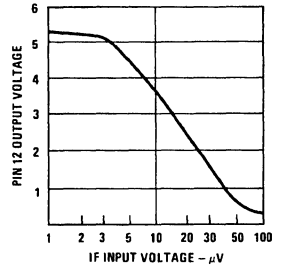
Supply Current (I_{11}) vs Supply Voltage (V11)



Reference Voltage, AGC and Meter Output vs Supply Voltage

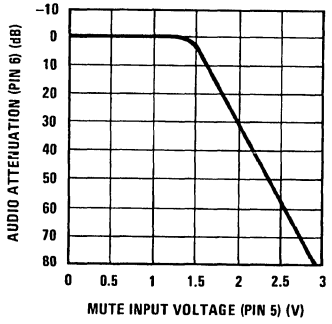


Mute Control Output (Pin 12) vs IF Input Signal



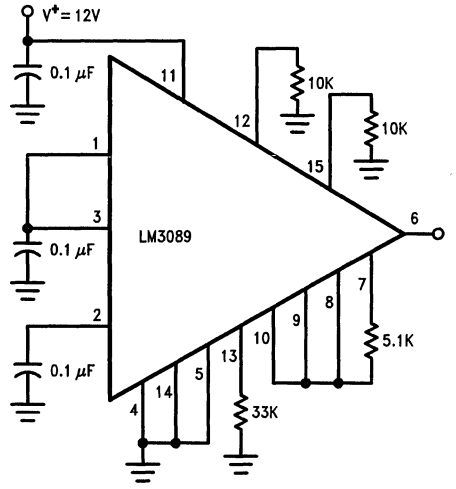
TL/H/7149–5

Typical Audio Attenuation (Pin 6) vs Mute Input Voltage (Pin 5)



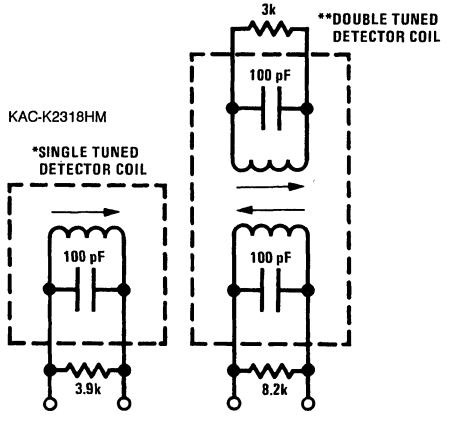
TL/H/7149–6

DC Test Circuit



TL/H/7149–7

AC Test Circuit



TL/H/7149–8

*For single tuned dectector coil:
L_O tunes with 100 pF at 10.7 MHz
Q_{UL} (unloaded) ≅ 75
Q_L (loaded) ≅ 13 for V9 ≅ 150 mVrms

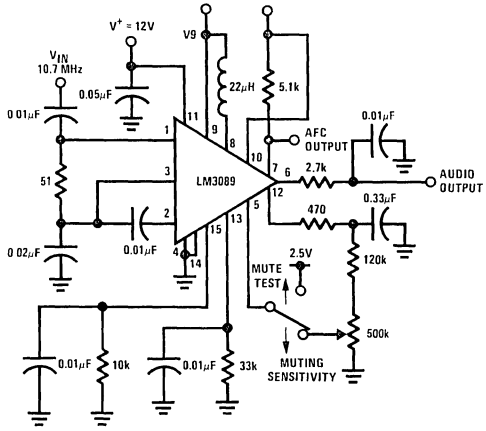
**For double tuned detector coil:
$Q_{ULPRI} = Q_{ULSEC} \cong 75$
$kQ \cong 0.7$ for V9 ≅ 150 mVrms

Note:

The recovered audio output voltage will be approximately 0.5 dB less when using the double tuned detector coil.

For proper operation of the mute circuit, the RF voltage at pin 9 should be 150 mVrms ±30 mV.

AC Test Circuit (Continued)



TL/H/7149–9

National Semiconductor Corporation

LM3189 FM IF System

General Description

The LM3189N is a monolithic integrated circuit that provides all the functions of a comprehensive FM IF system. The block diagram of the LM3189N includes a three stage FM IF amplifier/limiter configuration with level detectors for each stage, a doubly balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5V to +16V.

The LM3189N is ideal for high fidelity operation. Distortion in an LM3189N FM IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

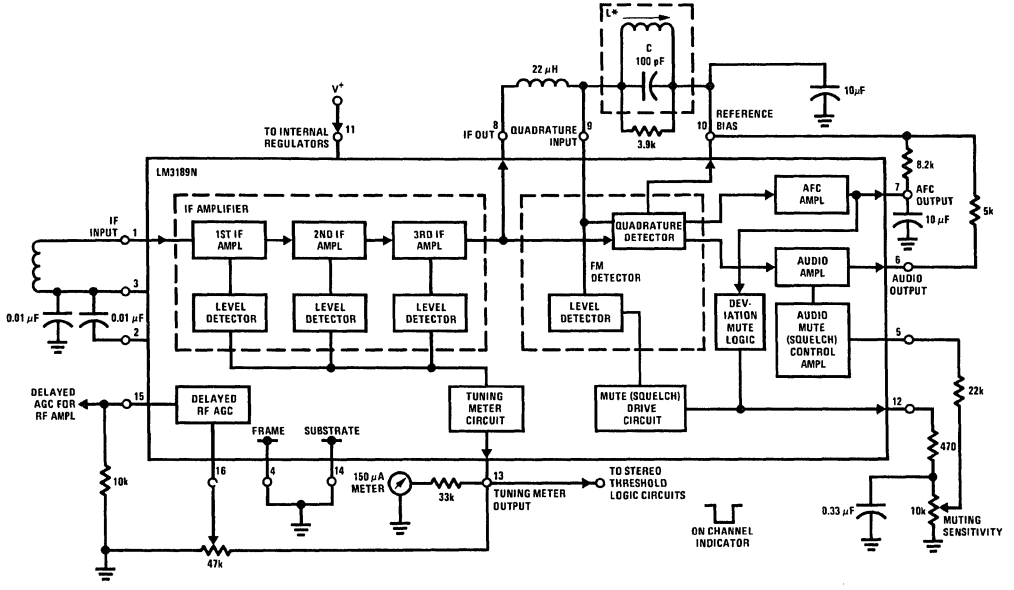
The LM3189N has all the features of the LM3089N plus additions.

The LM3189N utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of −40°C to +85°C.

Features

- Exceptional limiting sensitivity: 12 μV typ at −3 dB point
- Low distortion: 0.1% typ (with double-tuned coil)
- Single-coil tuning capability
- Improved (S + N)/N ratio
- Externally programmable recovered audio level
- Provides specific signal for control of inter-channel muting (squelch)
- Provides specific signal for direct drive of a tuning meter
- On channel step for search control
- Provides programmable AGC voltage for RF amplifier
- Provides a specific circuit for flexible audio output
- Internal supply voltage regulators
- Externally programmable ON channel step width, and deviation at which muting occurs

Block Diagram



TL/H/7960–1

All resistance values are in Ω

*L tunes with 100 pF (C) at 10.7 MHz, $Q_0 \cong 75$
(Toko No. KACS K586HM or equivalent)

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage Between Pin 11 and Pins 4, 14	16V
DC Current Out of Pin 12	5 mA
DC Current Out of Pin 13	5 mA
DC Current Out of Pin 15	2 mA
Power Dissipation (Note 2)	1500 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics $T_A = 25°C, V^+ = 12V$

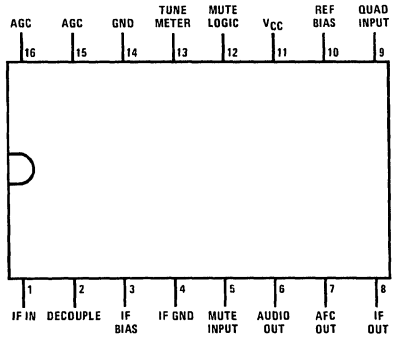
Symbol	Parameter	Conditions (See Single-Tuned Test Circuit)		Min	Typ	Max	Units
STATIC (DC) CHARACTERISTICS							
I_{11}	Quiescent Circuit Current			20	31	44	mA
	DC Voltages:						
V1	Terminal 1 (IF Input)	No Signal Input, Non Muted		1.2	2.0	2.4	V
V2	Terminal 2 (AC Return to Input)			1.2	2.0	2.4	V
V3	Terminal 3 (DC Bias to Input)			1.2	2.0	2.4	V
V15	Terminal 15 (RF AGC)			7.5	9.5	11	V
V10	Terminal 10 (DC Reference)			5	5.75	6	V
DYNAMIC CHARACTERISTICS							
V_I(lim)	Input Limiting Voltage (−3 dB Point)				12	25	μV
AMR	AM Rejection (Term. 6)	V_{IN} = 0.1V		45	55		dB
V_O(AF)	Recovered AF Voltage (Term. 6)	AM Mod. = 30%	f_O = 10.7 MHz, f_{mod} = 400 Hz, Deviation ±75 kHz	325	500	650	mV
THD	Total Harmonic Distortion (Note 1)						
	Single Tuned (Term. 6)	V_{IN} = 0.1V			0.5	1	%
	Double Tuned (Term. 6)				0.1		%
S + N/N	Signal Plus Noise to Noise Ratio (Term. 6)			65	80		dB
f_{DEV}	Deviation Mute Frequency		f_{mod} = 0		±40		kHz
V16	RF AGC Threshold				1.25		V
V12	On Channel Step	V_{IN} = 0.1V	f_{DEV} < ±40 kHz		0		V
			f_{DEV} > ±40 kHz		5.6		

Note 1: THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

Note 2: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Connection Diagram

Dual-In-Line Package



TL/H/7960–2

Top View

Order Number LM3189N
See NS Package Number N16E

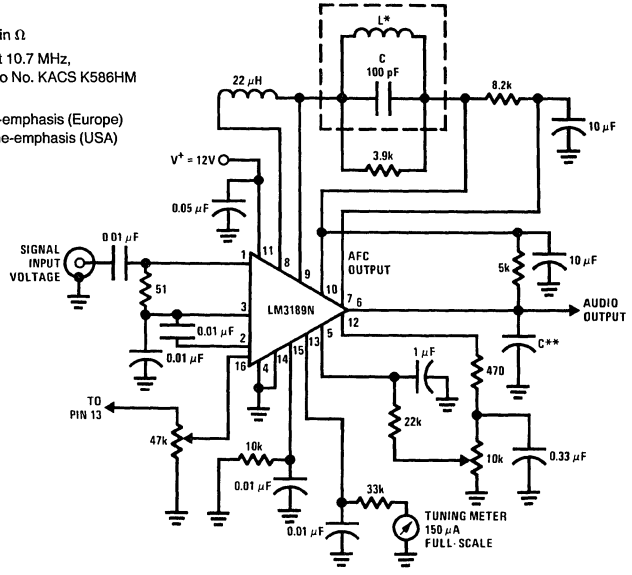
Test Circuits

Test Circuit for LM3189N Using a Single-Tuned Detector Coil

All resistance values are in Ω

*L tunes with 100 pF (C) at 10.7 MHz, Q_o(unloaded) ≅ 75 (Toko No. KACS K586HM or equivalent)

**C = 0.01 μF for 50 μs de-emphasis (Europe)
= 0.015 μF for 75 μs de-emphasis (USA)



TL/H/7960–3

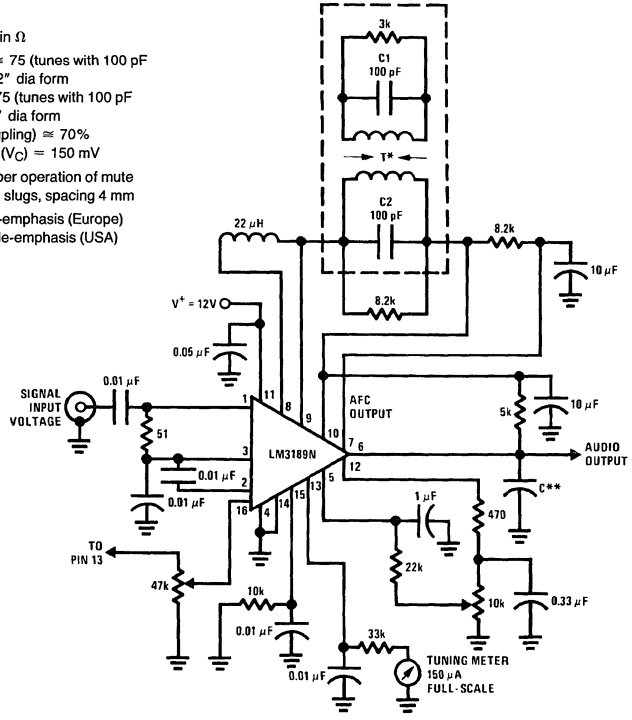
Test Circuit for LM3189N Using a Double-Tuned Detector Coil

All resistance values are in Ω

*T:PRI—Q_o(unloaded— ≅ 75 (tunes with 100 pF (C12)) 20t of 34e on 7/32" dia form
SEC—Q_o(unloaded) ≅ 75 (tunes with 100 pF (C2)) 20t of 34e on 7/32" dia form
kQ(percent of critical coupling) ≅ 70%
(adjusted for coil voltage (V_C) = 150 mV

Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4 mm

**C = 0.01 μF for 50 μs de-emphasis (Europe)
= 0.015 μF for 75 μs de-emphasis (USA)

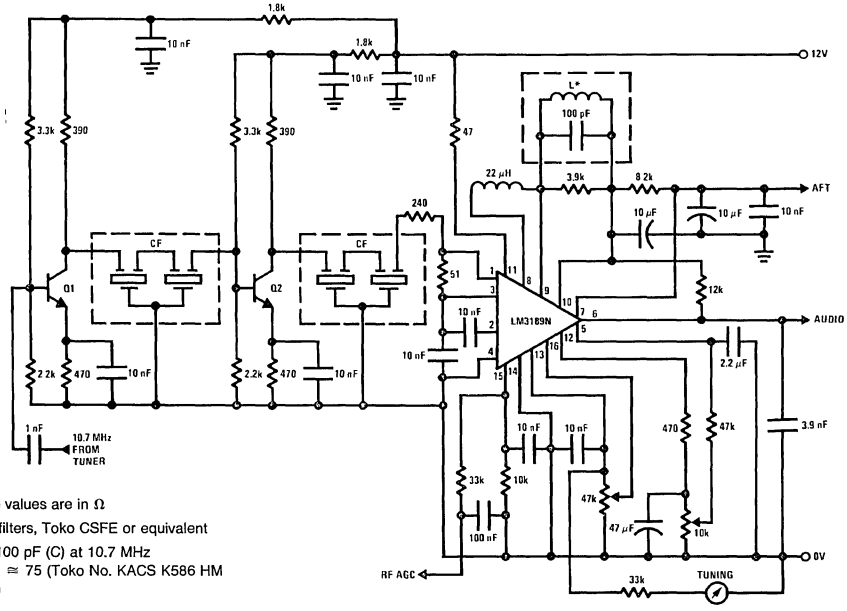


TL/H/7960–4

Complete FM IF System for High Quality Tuners

The circuit provides a complete FM IF system for a high quality receiver. Either one or two stages of amplification and bandpass filtering may be desired, depening on the receiver requirements. See graph for Typical Limiting and Noise Characteristics for each circuit configuration which can be compared to the LM3189N alone.

Complete FM IF System for High Quality Receivers



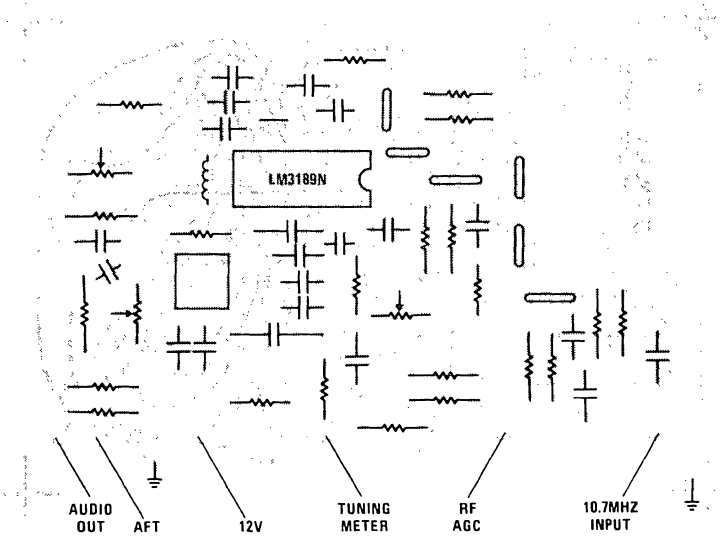
All resistance values are in Ω

CF: Ceramic filters, Toko CSFE or equivalent

*L tunes with 100 pF (C) at 10.7 MHz
Q_o(unloaded) ≅ 75 (Toko No. KACS K586 HM or equivalent)

TL/H/7960–5

Printed Circuit Board and Component Layout

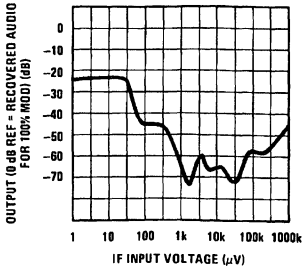


TL/H/7960–6

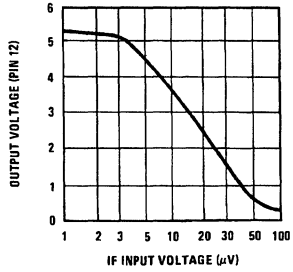
Component Side

Typical Performance Characteristics

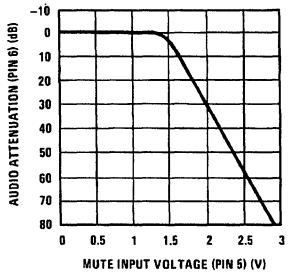
AM Rejection (30% Mod) vs IF Input Signal



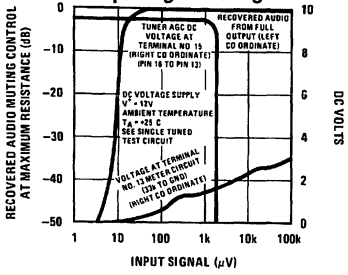
Mute Control Output (Pin 12) vs IF Input Signal



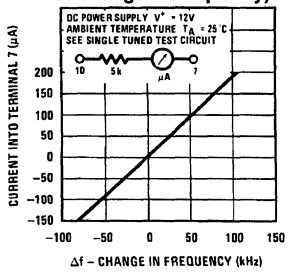
Typical Audio Attenuation (Pin 6) vs Mute Input Voltage (Pin 5)



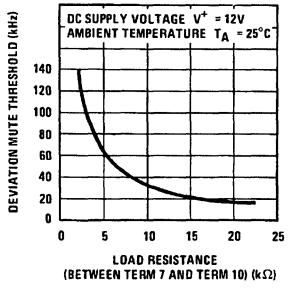
Muting Action, Tuner AGC, and Tuning Meter Output as a Function of Input Signal Voltage



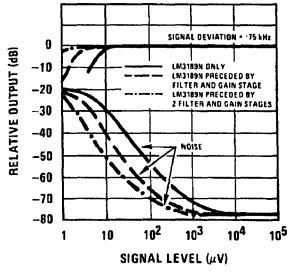
AFC Characteristics (Current at Term 7 as a Function of Change in Frequency)



Deviation Mute Threshold as a Function of Load Resistance (Between Term 7 and Term 10)

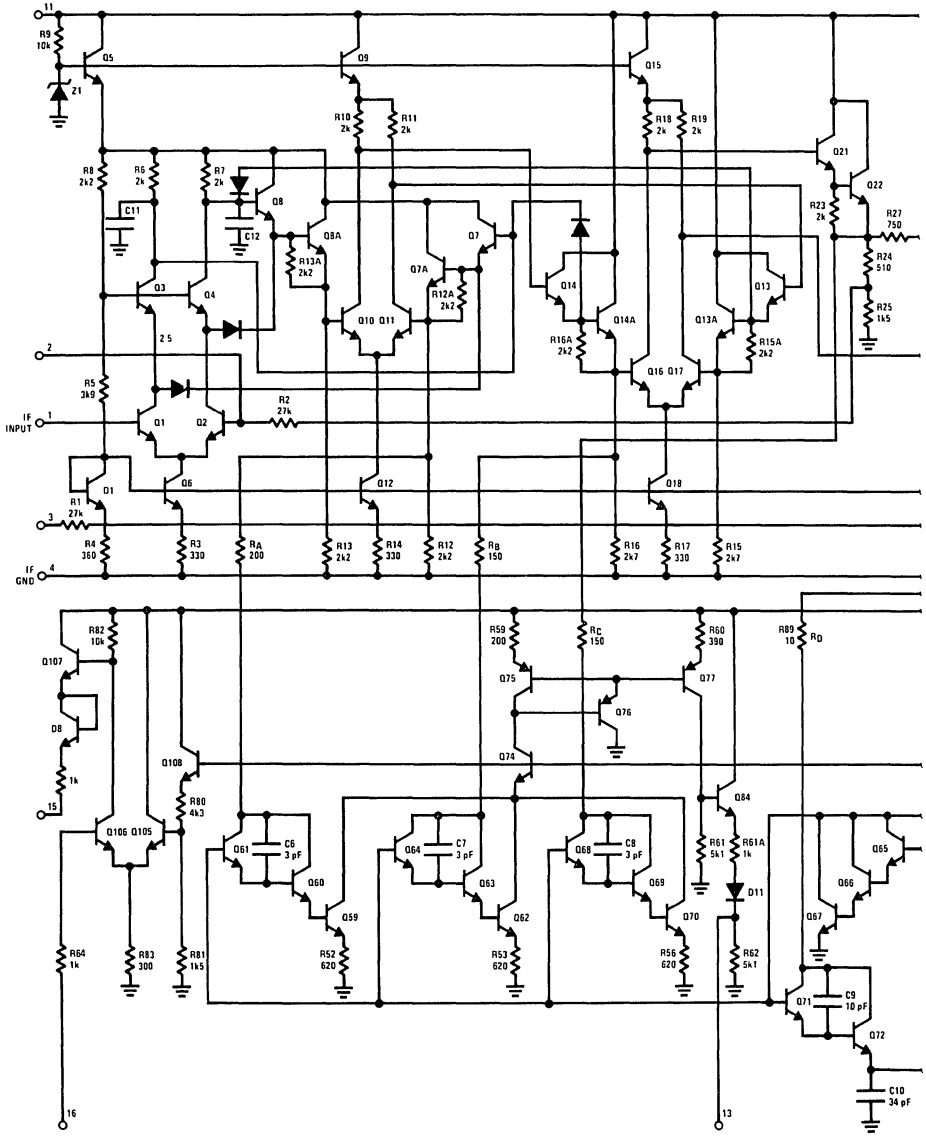


Typical Limiting and Noise Characteristics



TL/H/7960–7

Schematic Diagram



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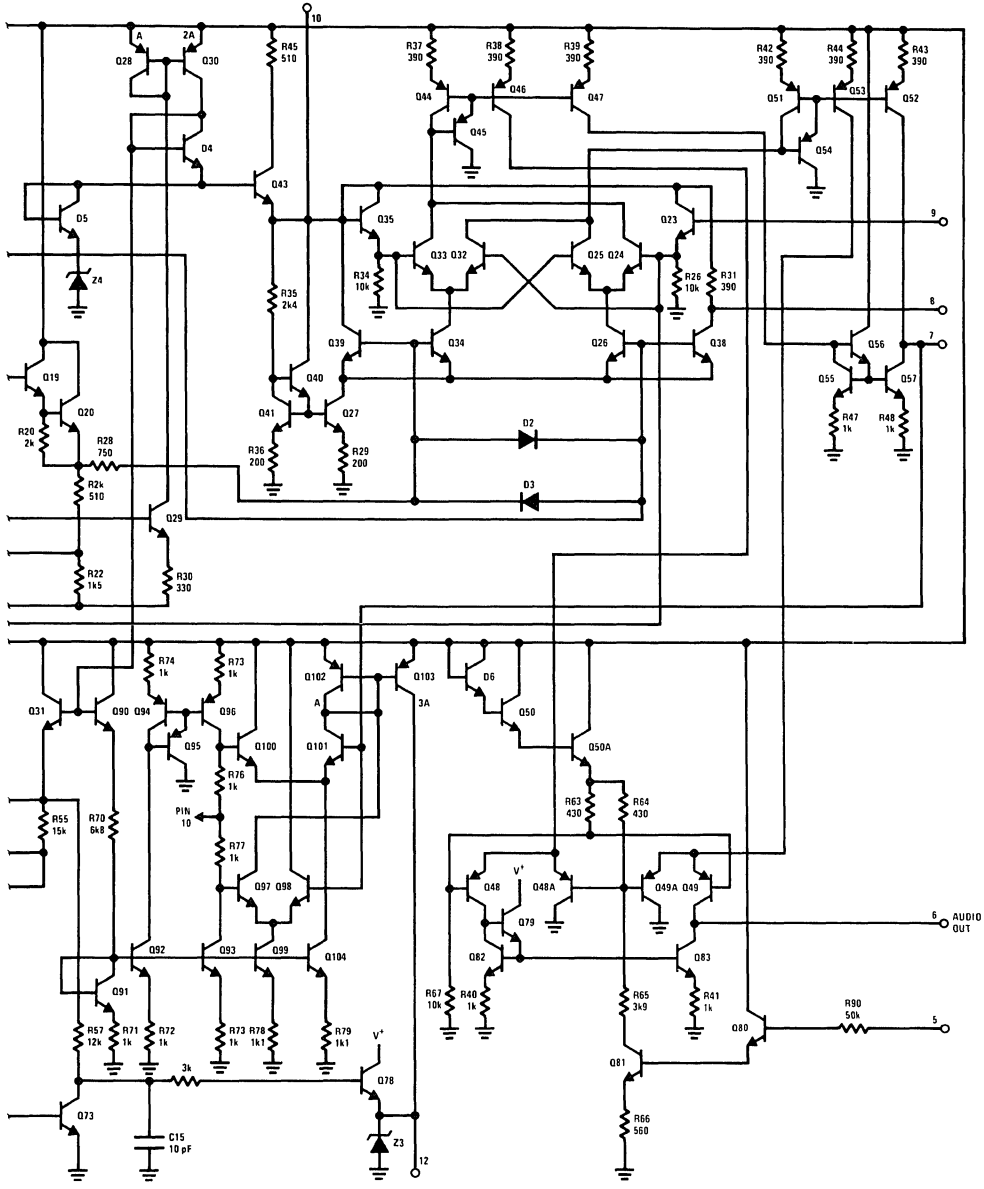
Schematic Diagram (Continued)



TL/H/7960–9

National Semiconductor Corporation

PRELIMINARY

LM3361A Low Voltage/Power Narrow Band FM IF System

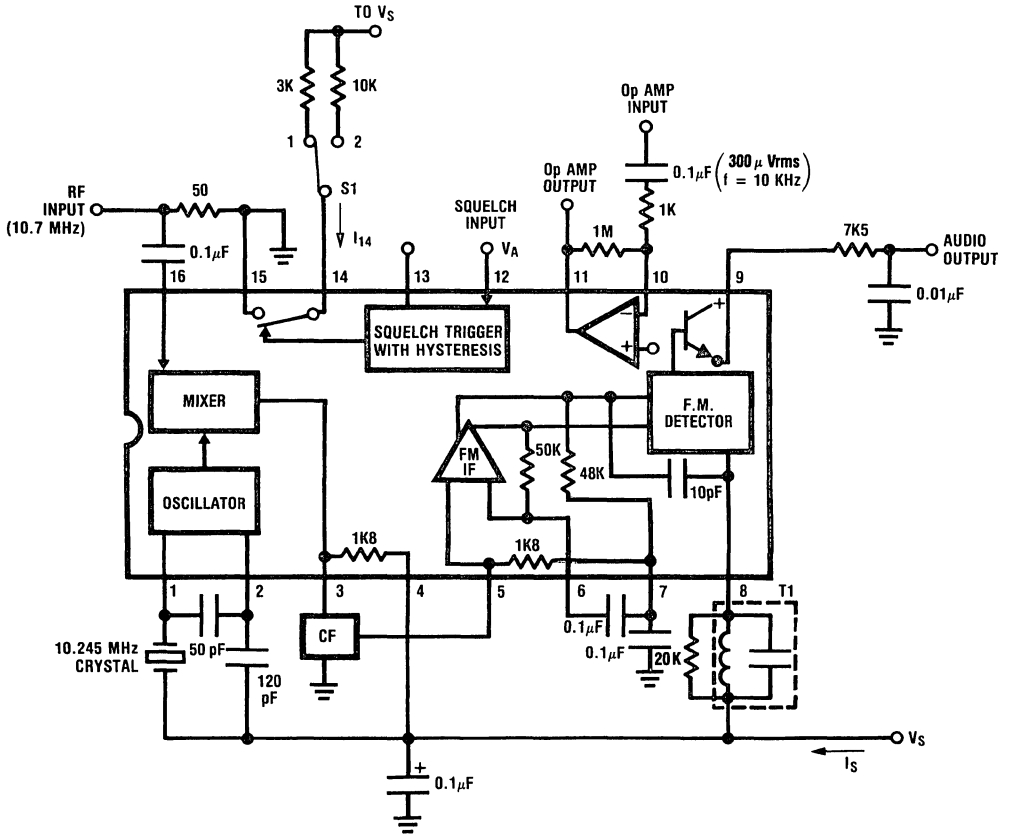
General Description

The LM3361A contains a complete narrow band FM demodulation system operable to less than 2V supply voltage. Blocks within the device include an oscillator, mixer, FM IF limiting amplifier, FM demodulator, op amp, scan control, and mute switch. The LM3361A is similar to the MC3361 with the following improvements: the LM3361A has higher voltage swing both at the op amp and audio outputs. It also has lower nominal drain current and a squelch circuit that draws significantly less current than the MC3361. Device pinout functions are identical with some slightly different operating characteristics.

Features

- Functions at low supply voltage (less than 2V)
- Highly sensitive (−3 dB limiting at 2.0 μV input typical)
- High audio output (increased 6 dB over MC3361)
- Low drain current (2.8 mA typ., V_{CC} = 3.6V)
- Minimal drain current increase when squelched
- Low external parts count

Block Diagram And Test Circuit



TL/H/5586–1

Order Number LM3661AM or LM3361AN
See NS Package Number M16A or N16E

T1-TOKO RMC-2A6597HM
CF-MURATA CFU 455E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Package Dissipation (Note 1)	1500 mW
Power Supply Voltage (V_S)	12 V
RF Input Voltage ($V_S > 3.6V$)	1 Vrms
Mute Function (pin 14)	−0.7 to 5 Vp
Operating Ambient Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Parameters Guaranteed By Electrical Testing

(Test ckt., $T_A = 25°C$, $V_S = 3.6V$, $f_O = 10.7$ MHz, $\Delta f = \pm 3$ kHz, $f_{MOD} = 1$ kHz, 50Ω source)

Parameter	Measure	Min	Typ	Max	Units
Supply Voltage Range	V_S	2.0	3.6	9.0	V
Supply Current					
Squelch Off	I_S		2.8	5.0	mA
Squelch On	I_S		3.6	6.0	mA
RF Input for −3 dB Limiting	RF Input		2.0	6.0	μV
Recovered Audio at Audio Output	Audio Output	200	350		mV_{RMS}
Audio Out DC	V_9	1.2	1.5	1.8	V_{DC}
Op Amp Gain	V_{11}/V_{IN}	40	55		dB
Op Amp Output DC	V_{10}	0.4	0.7		V_{DC}
Op Amp Input Bias Current	$(V_{10}-V_{11})/1M\Omega$		20	75	nA
Scan Voltage					
Pin 12 high (2V)	V_{13}		0	0.5	V_{DC}
Pin 12 Low (0V)	V_{13}	3.0	3.4		V_{DC}
Mute Switch Impedance, Pin 12 = 0V Switch S1 from pos.1 to pos.2	$\Delta V_{14}/\Delta I_{14}$		15	30	Ω

Design Parameters Not Tested or Guaranteed

	Typ	
Mixer Conversion Gain (Note 2)	46	V/V
Mixer Input Resistance	3.6	kΩ
Mixer Input Capacitance	2.2	pF
Detector Output Impedance	500	Ω
Trigger Hysterisis	100	mV
Mute Off Impedance (measure pin 14 with pin 12 @ 2V)	10	MΩ
Squelch Threshold	0.65	V_{DC}
Detector Center Frequency Slope	0.15	V/kHz

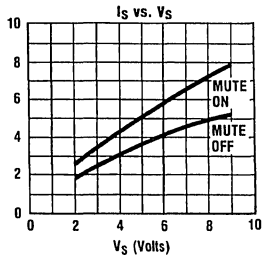
Note 1. For operation above 25°C ambient temperature, the device must be derated based on 150°C maximum junction temperature and a thermal resistance θ_{JA} of 80°C/W.

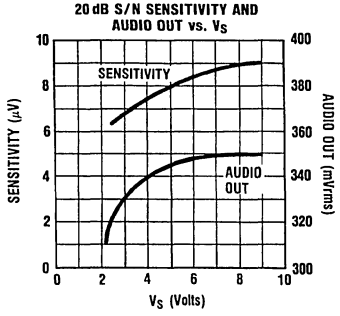
Note 2. Mixer gain is supply dependent and effects overall sensitivity accordingly (See Typical Performance Characteristics).

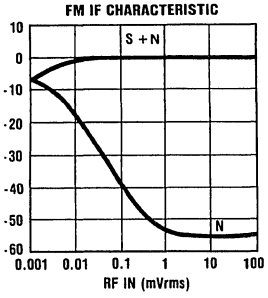
Coils:
Toko America
1250 Feehanville Drive
Mount Prospect, IL 60056
(312) 297-0070

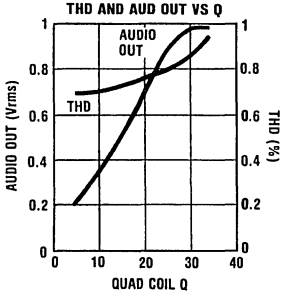
Filters:
Murata
2200 Lake Park Drive
Smyrna, GA 30080
(404) 436-1300

Typical Performance Characteristics (Test Circuits)



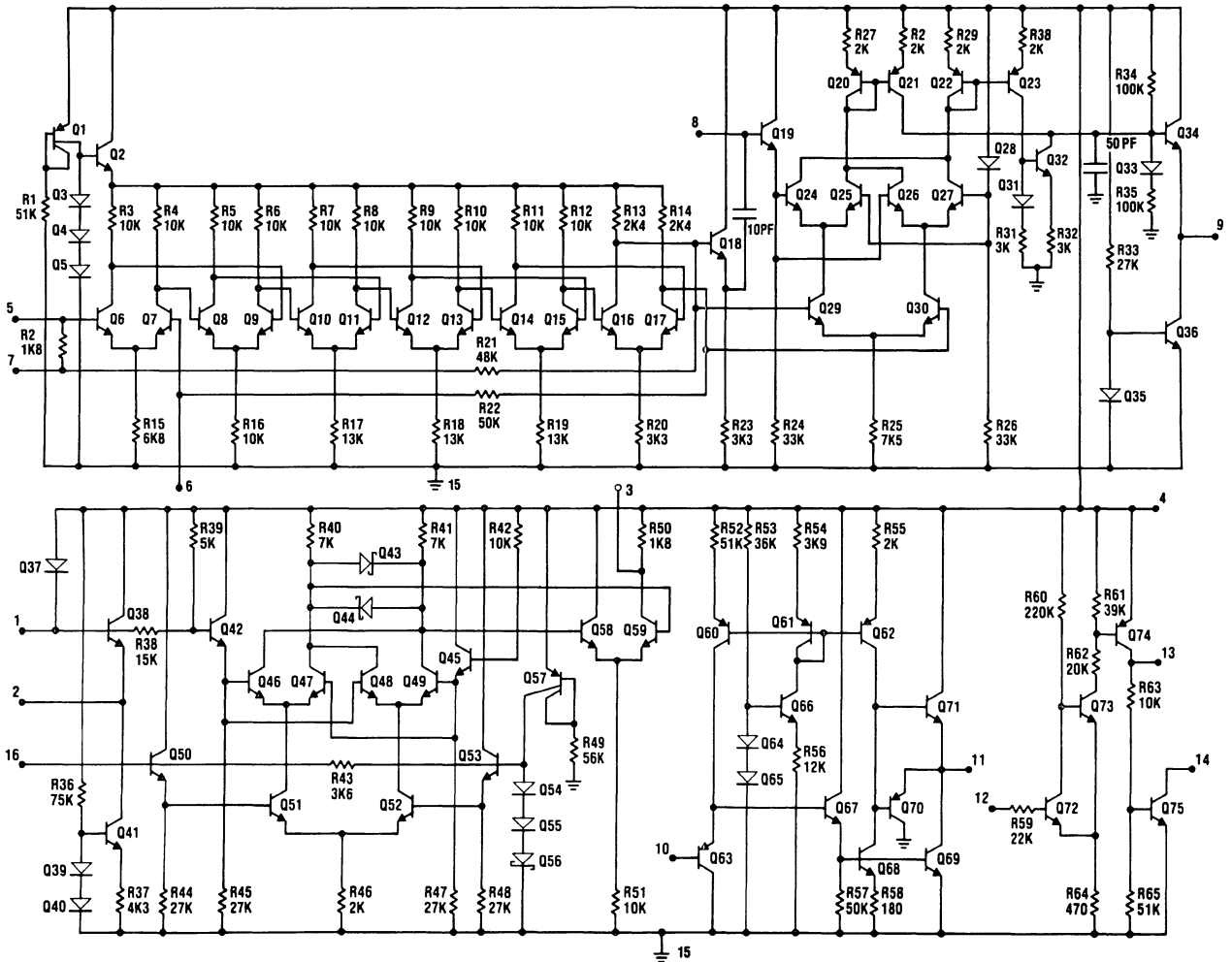






TL/H/5586–2

Internal Schematic

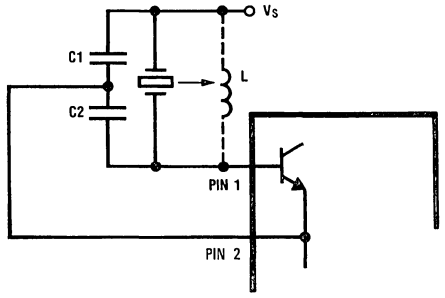


TL/H/5586-3

Applications Information (See Internal Schematic)

OSCILLATOR

The Colpitts type oscillator is internally biased with a regulated current source which assures proper operation over a wide supply range. The collector, base, and emitter terminals are at pins 4, 1, and 2 respectively. The crystal, which is used in the parallel resonant mode, may be replaced with an appropriate inductor if the application does not require the stability of a crystal oscillator. In this case, the resonant frequency will be determined by the inductor in parallel with the series combination of C1 and C2.



TL/H/5586–4

so $Ct = (C1)(C2)/(C1+C2)$

and $f_O = .159/\sqrt{L(Ct)}$

MIXER

The mixer is double balanced to reduce spurious responses. The upper pairs are switched by the oscillator while the RF input is applied to the lower pair (pin 16). R43 sets the mixer input impedance at 3.6 kΩ. The mixer output impedance of 1.8 kΩ will properly match the input impedance of a ceramic filter which is used as a bandpass filter coupling the mixer output to the IF limiting amplifier.

IF LIMITER

The IF amplifier consists of six differential gain stages, with the input impedance set by R2 at 1.8 kΩ to properly terminate the ceramic filter driving the IF. The IF alone (without mixer) has a −3 dB limiting sensitivity of approximately 50 μV. The system bandwidth is limited to about 5 MHz due to high impedances in the IF which are necessary to meet low power requirements. The IF output is connected to the external quad coil at pin 8 via an internal 10 pF capacitor.

FM DEMOD AUDIO OUT

A conventional quadrature detector is used to demodulate the FM signal. The Q of the quad coil, which is determined by the external resistor placed across it, has multiple effects on the audio output. Increasing the Q increases output level but because of nonlinearities in the tank phase characteristic, also increases distortion (see Typical Performance Characteristics). For proper operation, the voltage swing on pin 8 should be adequate to drive the upper rank of the multiplier into switching (about 100 mVrms). This voltage level is dependent on the internal 10 pF capacitor and the tank R_P voltage divider network. After detection and de-emphasis, the audio output at pin 9 is buffered by an emitter follower.

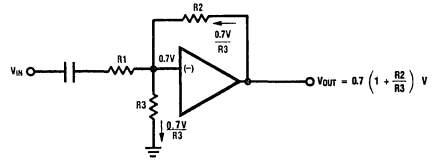
OP AMP

The op amp inverting input (pin 10) which is internally referenced to 0.7V, receives dc bias from the output at pin 11 through the external feedback network. Because of the low D.C. bias, maximum swing on the op amp output with 10% distortion is 500 mVrms. This can be increased when operating on supplies over 2.3V by adding a resistor from the op amp input to ground which raises the quiescent D.C. at the output allowing more swing (see figure below for selection of added resistor). The op amp is normally utilized as either a bandpass filter to extract a specific frequency from the audio output, such as a ring or dial tone, or as a high pass filter to detect noise due to no input at the mixer. The latter condition will generate a signal at the op amp output, which when applied to pin 12 can mute the external audio amp.

For max swing: $V_{OUT} = (V_S - V_{BE})/2$ (from internal circuit)

$$\text{so } (V_S - V_{BE})/2 = 0.7\left(1 + \frac{R2}{R3}\right)$$

$$\text{therefore } \frac{R2}{R3} = \left(\frac{V_S - V_{BE}}{1.4}\right) - 1$$



TL/H/5586–5

Increasing OP Amp Swing

SQUELCH TRIGGER CIRCUIT

The squelch trigger circuit is configured such that a low bias on the input (pin 12) will force pin 13 high (200 mV below supply), where it can support at least a 1 mA load, and pin 14 to be a low impedance, typically 15Ω to ground. Connecting pin 14 to a high impedance ground reference point in the audio path between pin 9 and the audio amp will mute the audio output. Pulling pin 12 above mute threshold (0.65V) will force pin 13 to an impedance of about 60 kΩ to ground and pin 14 will be an open circuit. There is 100 mV of hysterisis at pin 12 which effectively prevents jitter.

National Semiconductor Corporation

LM3820 AM Radio System

General Description

The LM3820 is a 3-stage AM radio IC consisting of an RF amplifier, oscillator, mixer, IF amplifier, AGC detector, and zener regulator.

The device was originally designed for use in slug-tuned auto radio applications, but is also suitable for capacitor-tuned portable radios.

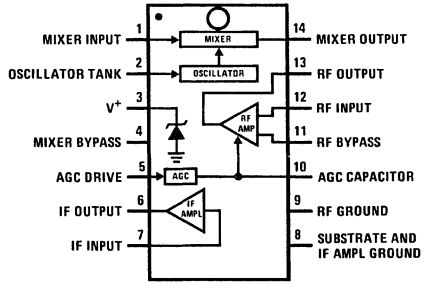
The LM3820 is an improved replacement for the LM1820.

Features

- Input protection diodes
- Good control on sensitivity
- Improved S/N and tweet
- Versatile building-block approach
- Gain-controlled RF stage
- Cascode IF amplifier
- Regulated supply
- Pin compatible with LM1820

Connection Diagram

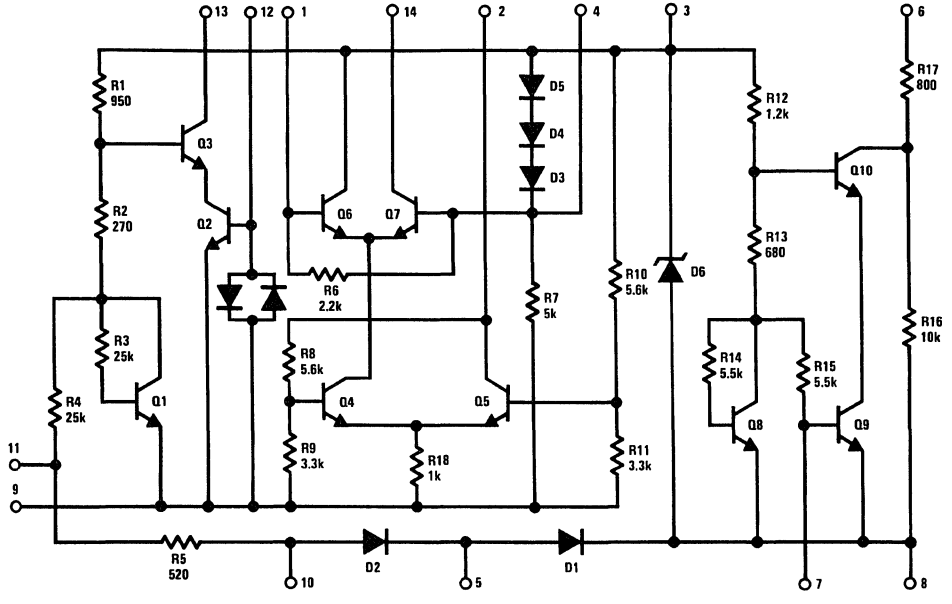
Dual-In-Line Package



TL/H/7967–1

Order Number LM3820N
See NS Package Number N14A

Circuit Schematic



TL/H/7967–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

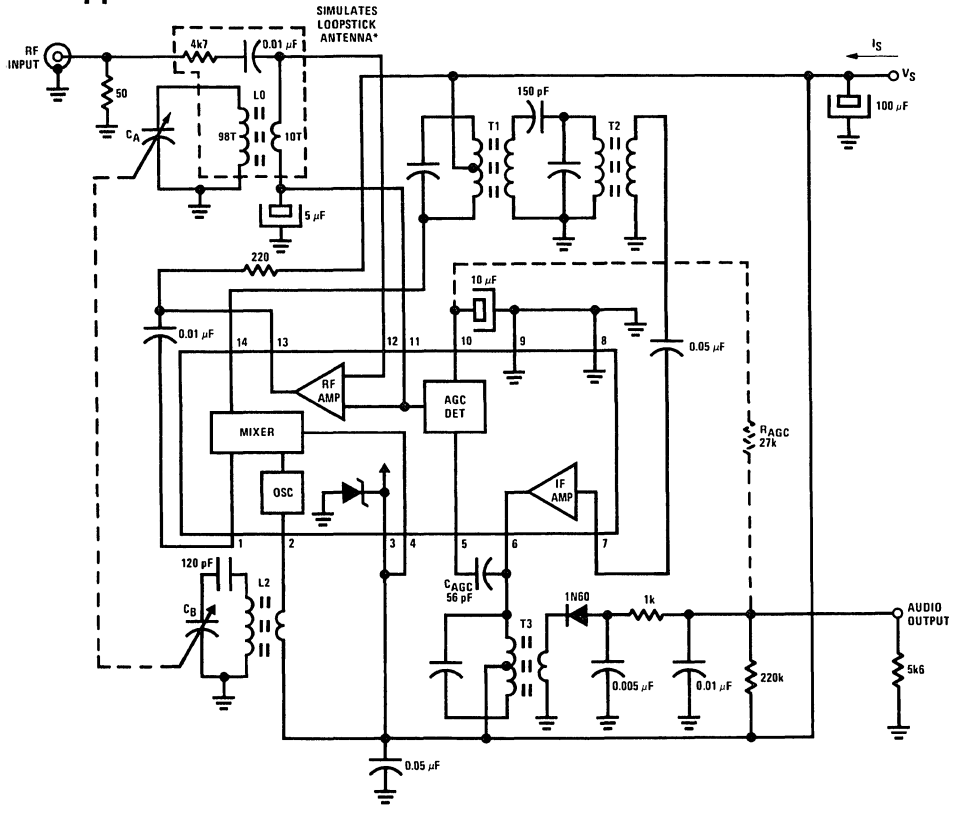
Power Dissipation (Note 1)	1200 mW
Supply Voltage	16V
Current into Supply Terminal (Pin 3)	35 mA
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (*Figure 1*, T_A = 25°C, V_S = 6V unless noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_S	Supply Current	No RF Input	12	18	24	mA
V_Z	Internal Zener Voltage		7.0	7.5	8.0	V
	Input Sensitivity	f = 1 MHz, 30% Mod 400 Hz Measure RF Input Level for 10 mV Audio Output with Tuning Peaked	15	35	70	μV
	Signal to Noise Ratio	f = 1 MHz, 30% Mod 1 kHz (S + N)/N at Audio Output with 100 μV RF Input	22	28	—	dB
	Overload Distortion	f = 1 MHz, 90% Mod 1 kHz THD at Audio Output with 30 mV RF Input	—	6	10	%

Note 1: Above T_A = 25°C, derate based on $T_{J(Max)}$ = 150°C and θ_{JA} = 100 °C/W.

Typical Applications



*100 μV RF INPUT is equivalent to approx. 1 mV/meter field strength. See Applications Information for coil specifications.

TL/H/7967–3

FIGURE 1. Capacitor-Tuned Test Fixture

Applications Information

The circuit shown in *Figure 1* is recommended as a starting point for portable radio designs. Loopstick antenna L1 is used in place of L0, and the RF amplifier is used with a resistor load to drive the mixer. A double tuned circuit at the output of the mixer provides selectivity, while the remainder of the gain is provided by the IF section, which is matched to the diode through a unity turns ratio transformer. R_{AGC} may be used in place of C_{AGC} to bypass the internal AGC detector and provide more recovered audio.

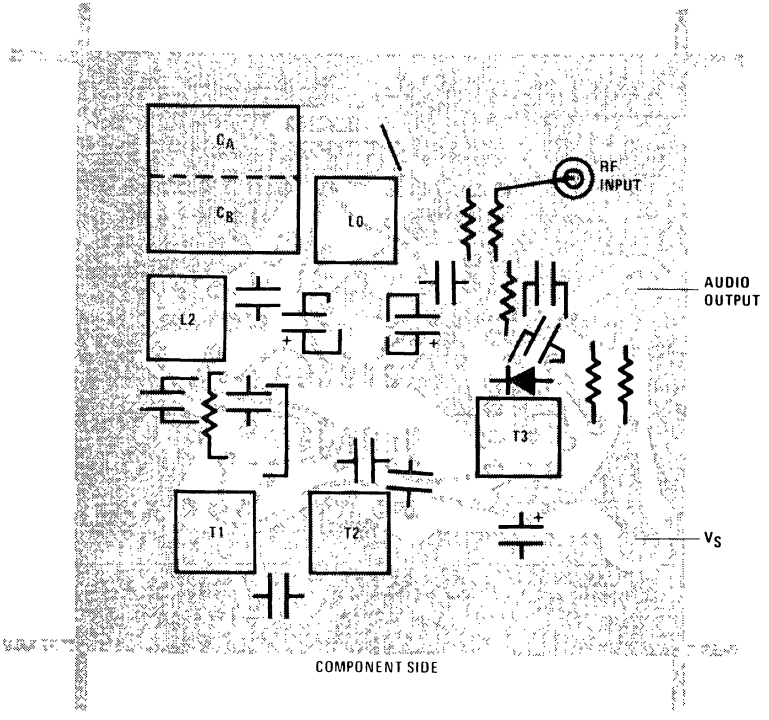
An AM automobile radio design is shown in *Figure 2*. Tuning of both the input and the output of the RF amplifier and the mixer is accomplished with variable inductors. Better selectivity is obtained through the use of double tuned interstage transformers. Input circuits are inductively tuned to prevent microphonics and provide a linear tuning motion to facilitate push-button operation.

Coil specifications for *Figure 1* are as follows:

VC	AM PVC	L1	AM ANT	L0, L2	AM OSC
			525 kHz-1650 kHz		980 kHz-2105 kHz
C_A = 140 pF C_B = 60 pF		110T, 100 x 8 mm, 5T L = 650 μH Qu = 250		98T, 10T L = 360 μH Qu = 110	
T1	**AM 1st IF**	**T2**	**AM 2nd IF**	**T3**	**AM 3rd IF**
	455 kHz		**455 kHz**		**455 kHz**
71T, 71T, 2T C = 180 pF Qu = 140		150 pF EXT, 142T, 7T C = 47 pF Qu = 120		71T, 71T, 35T C = 180 pF Qu = 140	

TL/H/7967–4

PCB Layout for *Figure 1* Circuit



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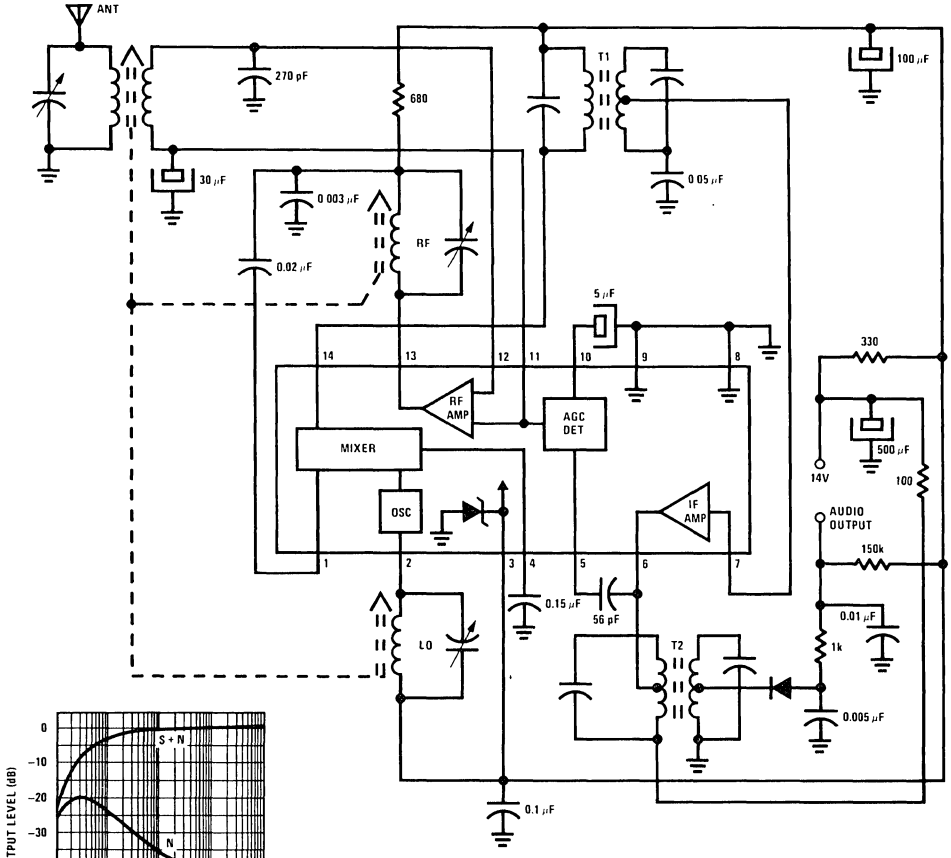
Applications Information (Continued)



TRANSFORMERS

T1: C = 130 pF primary & secondary
primary to secondary tap ratio—30:1
Q = 60
coupling—critical

T2: C = 130 pF primary & secondary
primary tap ratio—8.5:1
secondary tap ratio—8.5:1
Q = 60
coupling—critical

TL/H/7967–6

FIGURE 2. Slug-Tuned Auto Radio

National Semiconductor Corporation

LM4500A High Fidelity FM Stereo Demodulator with Blend

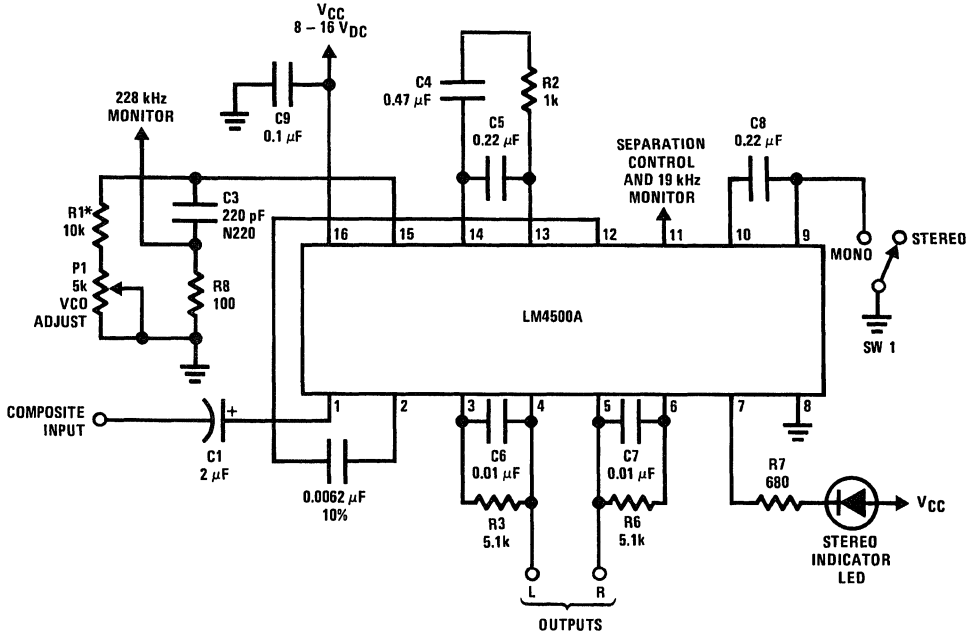
General Description

The LM4500A is an improved stereo demodulator IC offering very low audio distortion. A new demodulator technique minimizes adjacent station interference caused by subcarrier harmonics and prevents lock-up problems from pilot carrier frequency harmonics. The IC features a blend circuit which optimizes the signal-to-noise ratio under weak signal conditions by gradually combining left and right channel information.

Features

- Low distortion—0.1% typ
- High subcarrier harmonic rejection
- Large input dynamic range—2.5 Vp-p
- Voltage controlled blend
- High separation—fixed or adjustable
- Adjustable gain
- Reduced stereo-mono DC shift—5 mV typ
- 55 dB supply ripple rejection
- Low output impedance
- Requires no external inductors
- Wide supply range 8V-16V
- Excellent rejection of 57 kHz ARI subcarrier

Typical Application



*Metal film, zero temperature coefficient resistor recommended

TL/H/7973–1

FIGURE 1

Order Number LM4500AN
See NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	16V
Power Dissipation (Package Limitation)	1800 mW
Derate above $T_A = +25°C$	15 mW/°C
Operating Temperature Range (Ambient)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lamp Drive Voltage	
Max Voltage at Pin 7 with Lamp "Off"	30V
Lamp Current	100 mA
Blend Control Input Voltage (Pin 11)	10V
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

Unless otherwise noted: $V_{CC} = 12\ V_{DC}$, $T_A = 25°C$, Vp-p standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 10% pilot level, using circuit of *Figure 1*

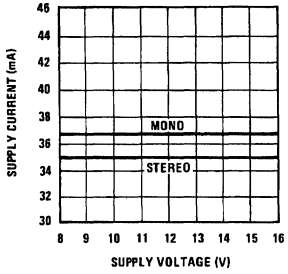
Parameter	Conditions	Min	Typ	Max	Units
Stereo Channel Separation	Unadjusted Optimized on Other Channel (Note 1)	30 40			dB dB
Measured Voltage Gain (Note 1)		0.8	1	1.2	
THD	2.5 Vp-p Composite Input Signal 1.5 Vp-p Composite Input Signal		0.15 0.08	0.3	% %
Signal-to-Noise Ratio	DIN45405 Quasi Peak Reading rms 20 Hz-15 kHz		83 88		dB dB
Ultrasonic Frequency Rejection	19 kHz 38 kHz		31 45		dB dB
Stereo Switch Level	19 kHz Input Level for Lamp "On"	12	16	20	mVrms
Hysteresis			8		dB
Output Voltage Change	With Mono/Stereo Switching (Note 2)		3	20	mV_{DC}
Stereo Blend Control Voltage (Pin 11) (See *Figure 8*)	3 dB Separation 30 dB Separation		0.7 1.7		V V
Minimum Separation	Pin 11 at 0V			1	dB
Monaural Channel Imbalance	Pilot Tone Off		0.03	0.3	dB
Sub-Carrier Harmonic Rejection	76 kHz 114 kHz 152 kHz		80 70 83		dB dB dB
Supply Ripple Rejection	f = 1 kHz		57		dB
Input Impedance			50		kΩ
Output Impedance			100		Ω
Blend Control Current (Note 1)			−100	−300	μA
Capture Range			±4		%
Operating Supply Voltage		8		16	V
Current Drain	Lamp Disconnected		35		mA

Note 1: See Applications Information and Circuit Description.

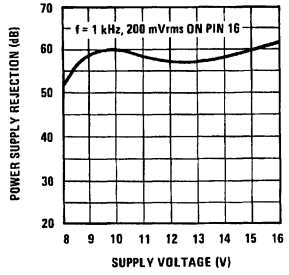
Note 2: This test is done with the stereo indicator lamp disconnected in order to remove DC shift due to thermal changes. These shifts have long time constants (100 ms) and therefore do not produce audible transients.

Typical Performance Characteristics

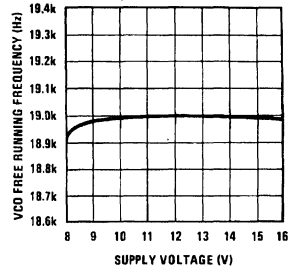
Supply Current vs Supply Voltage



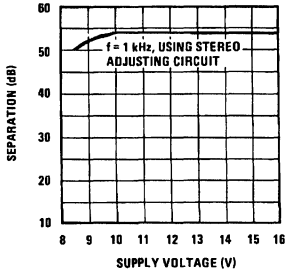
Power Supply Rejection vs Supply Voltage



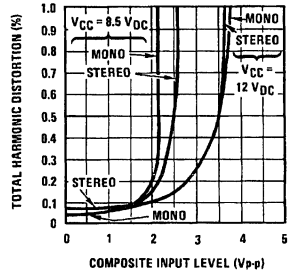
VCO Free Running Frequency vs Supply Voltage



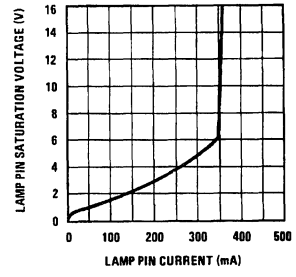
Channel Separation vs Supply Voltage



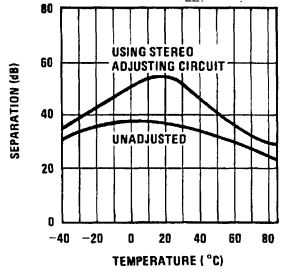
Total Harmonic Distortion vs Composite Input Level



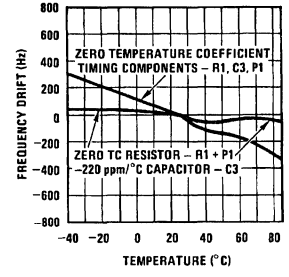
Lamp Pin Saturation Voltage vs Current



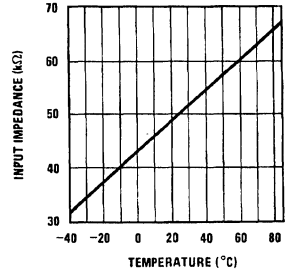
Stereo Separation vs Temperature



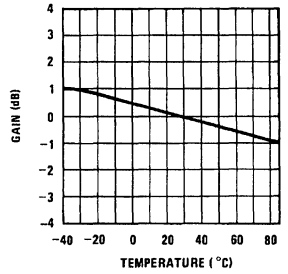
VCO Free Running Frequency Drift vs Temperature



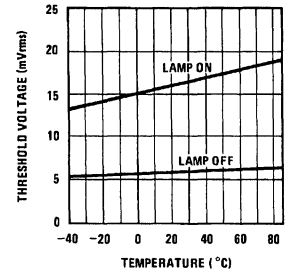
Input Impedance vs Temperature



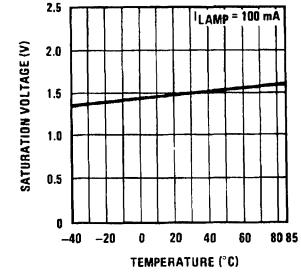
Gain vs Temperature



Stereo Switch Threshold vs Temperature



Lamp Pin Saturation Voltage vs Temperature



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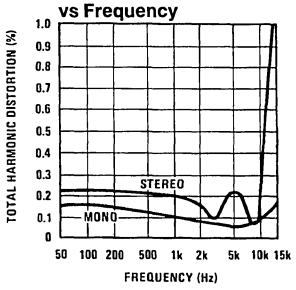
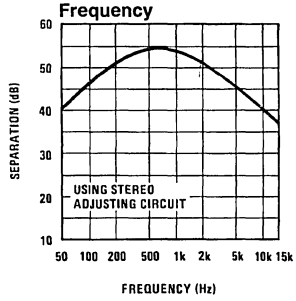
Typical Performance Characteristics (Continued)

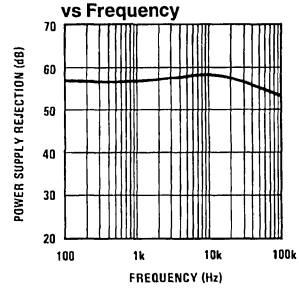
Total Harmonic Distortion vs Frequency



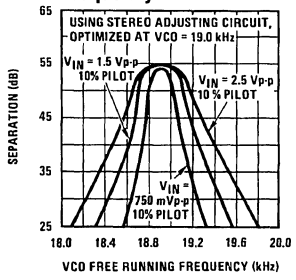
Separation vs Frequency



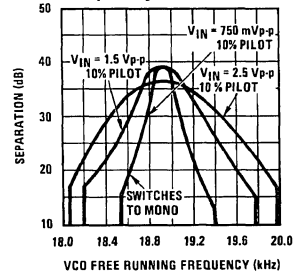
Power Supply Rejection vs Frequency



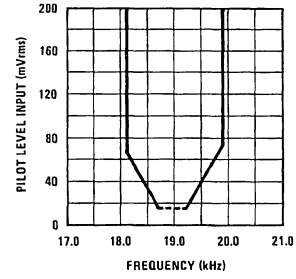
Adjusted Separation vs VCO Free Running Frequency



Unadjusted Separation vs VCO Free Running Frequency



Capture Range vs Pilot Level



TL/H/7973–3

Block Diagram

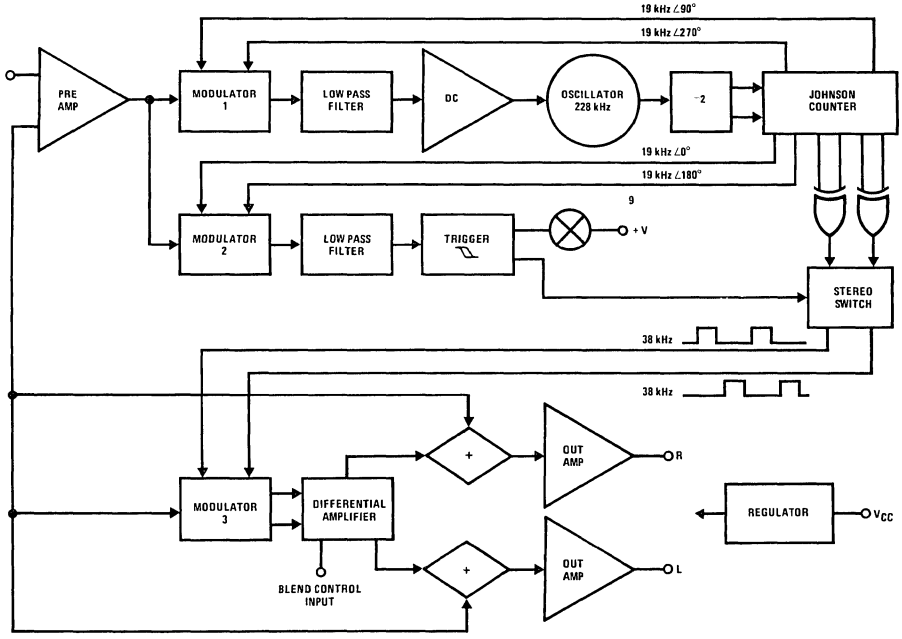


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FIGURE 2

Circuit Description

INTRODUCTION

The LM4500A is a phase-lock-loop stereo decoder which incorporates a variable separation control, and in which sensitivity to the third harmonics of both the pilot and sub-carrier frequencies has been eliminated by the use of appropriate, digitally generated, waveforms in the phase-lock-loop and decoder sections.

The variable separation control may be operated manually, or by a receiver's AGC or S meter signals, to provide smooth transitions between monaural and stereo reception. It operates only during stereo reception: the circit switches automatically to monaural if the 19 kHz pilot tone is absent.

The elimination of sensitivity to the third harmonic of the sub-carrier (114 kHz) excludes interference from the sidebands of adjacent transmitters, while the elimination of sensitivity to the third harmonic of the pilot tone (57 kHz) excludes interference from the ARI* system which employs this frequency.

CIRCUIT OPERATION

The block diagram of the circuit, shown in *Figure 2*, consists of three sections, the phase-lock-loop, including the digital waveform generator, the stereo switch, and the decoder, in which the composite stereo signal is demodulated and matrixed to separate L and R channels.

In the phase-lock-loop the internal RC oscillator, operating at 228 kHz, feeds a 3-stage Johnson counter, via a binary divider, to generate a series of 19 kHz square waves. By the use of suitably connected NAND and EXCLUSIVE OR gates, the waveforms shown in *Figure 3*, which are used to drive the various modulators in the circuit, are developed.

*Auto Radio Information - used in Europe

The use of such drive waveforms produces the modulating functions also shown in *Figure 3*. The usual square waveforms have been replaced in the PLL and decoder sections by 3-level forms which contain no third harmonic (actually no harmonics which are mutliples of 2 or 3 are present). This eliminates the frequency translation of interference from these bands into the low frequency region. Such translation may produce audible components in the decoder section from the sidebands of adjacent channel FM signals, and may produce phase jitter, and consequent intermodulation distortion, in the PLL, from the modulated 57 kHz tones of the ARI system. The LM4500A is inherently free from these effects.

The stereo switch section is of conventional form (e.g. LM1310).

The decoder section consists of a modulator (driven by the waveforms shown in *Figure 3*) whose outputs are the inverted and non-inverted channel difference signals. These signals pass to the output amplifiers via the variable blend circuit in which they are partially combined, and hence mutually attenuated, according to the control voltage applied.

Matrixing occurs at the inputs of the output amplifiers, where the unmodified composite signal is added to the blended channel difference signals. The stereo separation may be progressively reduced from maximum to zero; dependent on the blending. The control law has been made non-linear, as the major redistribution of sound energy occurs at very low separation levels. For monaural, or very weak stereo signals, the modulator in the decoder section is deactivated by the stereo switch circuit. The variable separation control is thus, also, automatically disabled.

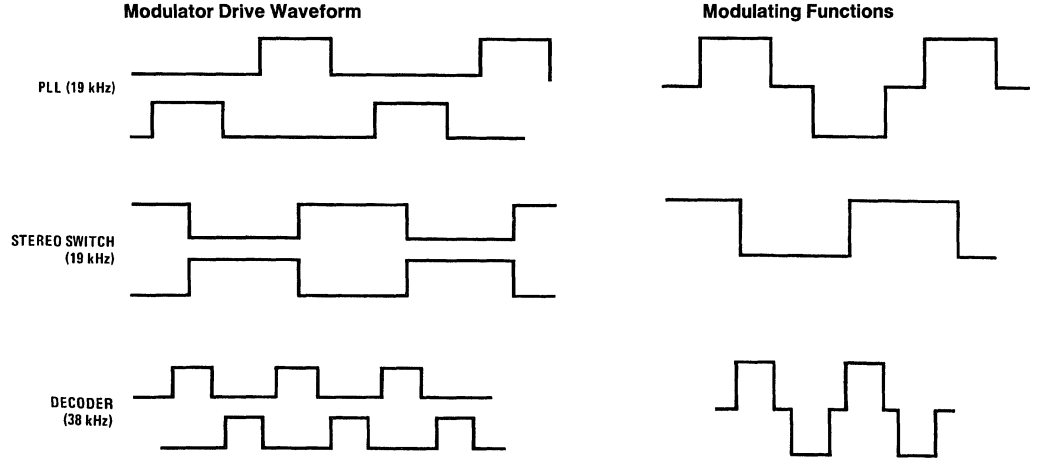

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FIGURE 3. Digital Waveforms

Applications Information

GAIN AND DE-EMPHASIS

The gain and de-emphasis characteristics of the circuit are defined by shunt feedback via the external RC networks (R3, C5, R4, C7 of *Figure 1*) around the output amplifiers. The gain is unity when resistors of 5.1 kΩ are used. Higher gains may be obtained by using networks of the form shown in *Figure 4*.

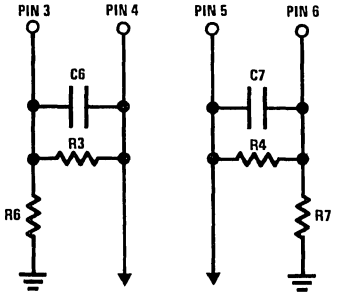

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FIGURE 4. Output Amplifier Feedback Networks

The resistors R6, R7 are added to correct the output quiescent voltage levels which are optimized for R3, R4 = 5.1 kΩ and which would, if uncorrected, become too low with higher value resistors. Suitable network values are as follows:

Gain (dB)	R3, R4	C6, C7		R6, R7
		50 μs	75 μs	
0	5.1 kΩ	10 nF	15 nF	
3	6.8 kΩ	6.8 nF	10 nF	47k ± 10%
6	10k	4.7 nF	6.8 nF	27k ± 10%

The maximum output level is 1 Vrms; consequently the max input is limited to 1.4 Vp-p if the gain is set to 6 dB.

SEPARATION ADJUSTMENT

A separation adjustment may be added, as shown in *Figure 5*, to compensate for the receiver's IF characteristics.

This network reduces the amplification of the channel sum signal in the decoder, to compensate the attenuation of the channel difference signal in the receiver's IF section. The network shown will compensate for up to 2 dB attenuation at 38 kHz. The decoder gain is, obviously, reduced by an amount equal to the compensation required. When used as described, the adjustment also corrects the inherent separation of the decoder, which may be optimized on one channel. Optimization of both channels is possible if separate potentiometers are used to feed each output amplifier.

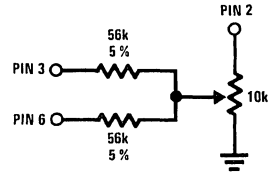

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FIGURE 5. Networking Providing Adjustable Separation

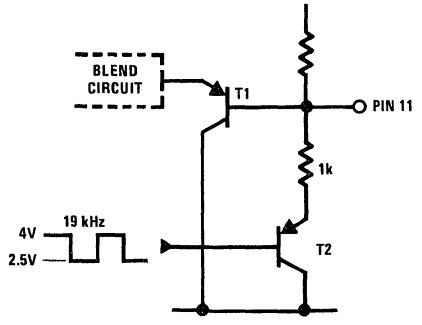
VARIABLE SEPARATION (BLEND) CONTROL AND 19 kHz OUTPUT

To retain the 16-Pin package the blend control has been combined with the 19 kHz output on Pin 11. The internal circuit providing this combination is shown in *Figure 6*.

If Pin 11 is left open-circuit the 19 kHz signal appears at a mean DC level of 4V. The blend circuit is inoperative at this level and the decoder provides full separation. The 19 kHz signal can be used to tune the internal oscillator.

To reduce the separation the voltage on Pin 11 is reduced. At 3.2V T2 ceases conduction and the 19 kHz signal disappears.

At 2.0V the blend circuit comes into operation and the separation decreases according to the curve shown in *Figure 8*.



TL/H/7973–8

FIGURE 6. Blend Control Input Circuit

Applications Information (Continued)

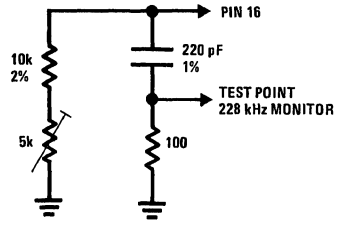


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FIGURE 7. Oscillator Network for Direct Frequency Measurement

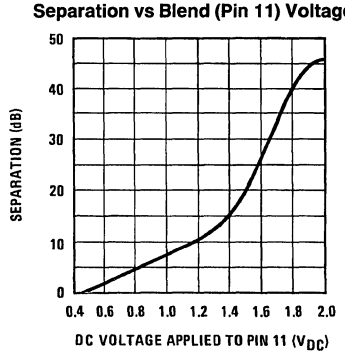

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FIGURE 8

Oscillator Tuning

If the variable separation facility is not required Pin 11 is left open-circuit and the 19 kHz signal which then appears may be used to indicate the oscillator frequency. If the variable separation is used, and the drive circuit prevents access to the 19 kHz signal, then the oscillator frequency must be measured directly. A test point should be obtained by modifying the oscillator RC network as in *Figure 7*.

The output is a pulse train of appoximately 1.5V amplitude. Connecting frequency counters of up to 300 pF input capacitance produces less than 0.3% change of the oscillator frequency, which should be set to 228 kHz.

HIGH LOOP GAIN COMPONENTS

For applications demanding operation under low pilot level (e.g. car radio) the following component changes to *Figure 1* are recommended.

R1 = 12k C3 = 150 pF
R2 = 1.5k C4 = 330 pF
R8 = 330 C5 = 150 pF
P1 = 10k

EXTERNAL MONO-STEREO SWITCHING AND OSCILLATOR KILLING

If required the LM4500A can be forced into mono mode simply by grounding Pin 9 (see *Figure 1*). The 228 kHz oscillator will be automatically stopped.

The conditions governing mono/stereo switching on Pin 9 are the following:

Quiescent voltage: +2.3 V_{DC}

Current required to ensure mono operation (with 100 mVrms pilot level): 10 μA (from Pin 9 to ground)

Hysteresis: 0.7 μA

Stereo/mono switching & oscillator killing; less than +500 mV

Maximum stray capacitance between Pin 9 and ground: 100 pF

EXTERNAL COMPONENT FUNCTIONS

P1 19 kHz frequency adjustment.

P2 Channel separation adjustment and compensation for IF roll-off.

R3, R6 Gain fixing resistors. The values shown in the schematic are for unity gain.

C6, C7 De-emphasis capacitors. Value to give: RC = 50 μs.

National Semiconductor Corporation

TBA120S IF Amplifier and Detector

General Description

The TBA120S is a monolithic integrated circuit specifically designed for audio detection in TV and FM radio receivers. It incorporates an 8-stage limiting IF amplifier and balanced detector plus a DC operated volume control.

The TBA120S is supplied in four groups depending on the resistance required between pin 5 and ground to attenuate the audio output by 30 dB. The group number as defined below is marked on the package.

Group	II	III	IV	V	
R5-GND	1.9–2.2	2.1–2.5	2.4–2.9	2.8–3.3	kΩ

Pins 3 and 4 are connected to the collector and base of a transistor which may be used as an AF-preamplifier or as a switch.

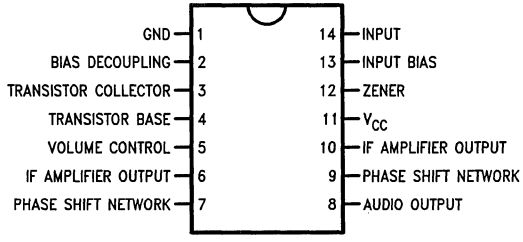
At pin 12 a zener-diode is accessible which can be used to stabilize the supply voltage of this integrated circuit or the voltage of other circuit elements in the set.

Features

- Electronic attenuator: replaces conventional AC volume control
- Volume reduction range 85 dB typ
- Sensitivity: 3 dB limiting voltage 30 μV typ
- Excellent AM rejection 68 dB typ at 10 mV
- Audio output voltage 1V typ
- Wide supply voltage range (6V–18V)
- Internal zener diode regulator
- Very low external component requirement
- Simple detector alignment: one coil

Connection Diagram

Dual-In-Line Package



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Top View

Order Number TBA120S II, TBA120S III, TBA120S IV or TBA120S V
See NS Package Number N14A

2

Absolute Maximum Ratings

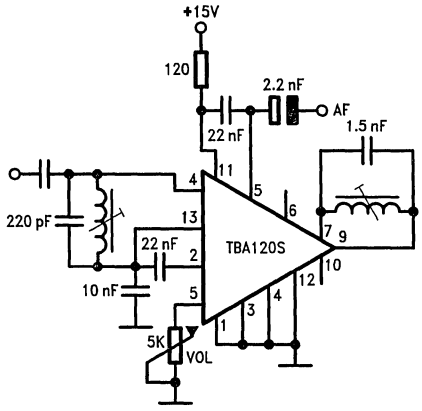
If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V11	18V
Volume Control Voltage, V5	4V
Zener Current, I_{12}	20 mA
Transistor Collector Current, I_3	5 mA
Transistor Base Current, I_4	2 mA
Bias Resistance (Max), R13-14	1 kΩ
Operating Temperature Range	−15°C to +70°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics (V_{CC} = 12V, T_A = 25°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	R5 = ∞	10	14	18	mA
		R5 = 0	11		20	
G_V	IF Voltage Gain	f = 5.5 MHz		68		dB
V_O	IF Output Voltage, Each Output at Limiting		170	250		mVp-p
V_{af}	AF Output Voltage	f = 5.5 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, V_I = 10 mV, Q = 45	0.7	1.0		V
	Distortion (5.5 MHz)	f = 5.5 MHz, Δf = 25 kHz, f_{MOD} = 1 kHz, V_I = 10 mV, Q = 45		1.5		%
	Distortion (10.7 MHz)	f = 10.7 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, V_I = 10 mV, Q = 20		0.2		
V_{LIM}	Input Voltage Before Limiting	f = 5.5 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, Q = 45		30	60	μV
Z_I	Input Impedance	f = 5.5 MHz	15/6	40/4.5		kΩ/pF
R_O	Output Resistance		1.9	2.6	3.3	kΩ
$\frac{Vaf\ max}{Vaf\ min}$	Volume Control Range		70	85		dB
V8	DC Component of the Output Signal	V_I = 0	6.2	7.3	8.4	V
a_{AM}	AM Rejection	f = 5.5 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, V_I = 500 μV m = 30%	50	60		dB
a_{AM}	AM Rejection	f = 5.5 MHz, Δf = ±50 kHz, f_{MOD} = 1 kHz, V_I = 10 mV, m = 30%		68		dB
R5	Potentiometer Resistance	1 dB Attenuation		3.7	4.7	kΩ
V5	Voltage	1 dB Attenuation		2.2	2.5	V
R5	Potentiometer Resistance	70 dB Attenuation	1.0	1.4		kΩ
V5	Voltage	70 dB Attenuation		1.2		V
	Noise Voltage at Output	V_I = 10 mV		30		μV
V12	Zener Voltage	I_{12} = 5 mA	11.2	12	13.4	V
R_Z	Zener Slope Resistance			30	50	Ω
V_{cbo}	Breakdown Voltage		45	65		V
V_{ceo}	Breakdown Voltage	I_3 = 500 μA	18	24		V
h_{fe}	Current Gain	I_3 = 1 mA	50	100	500	

Typical Application (5.5 MHz)



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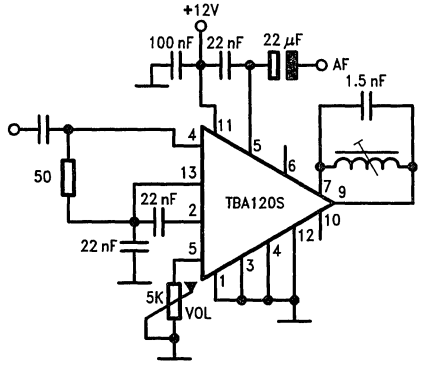
Test Circuit (5.5 MHz)



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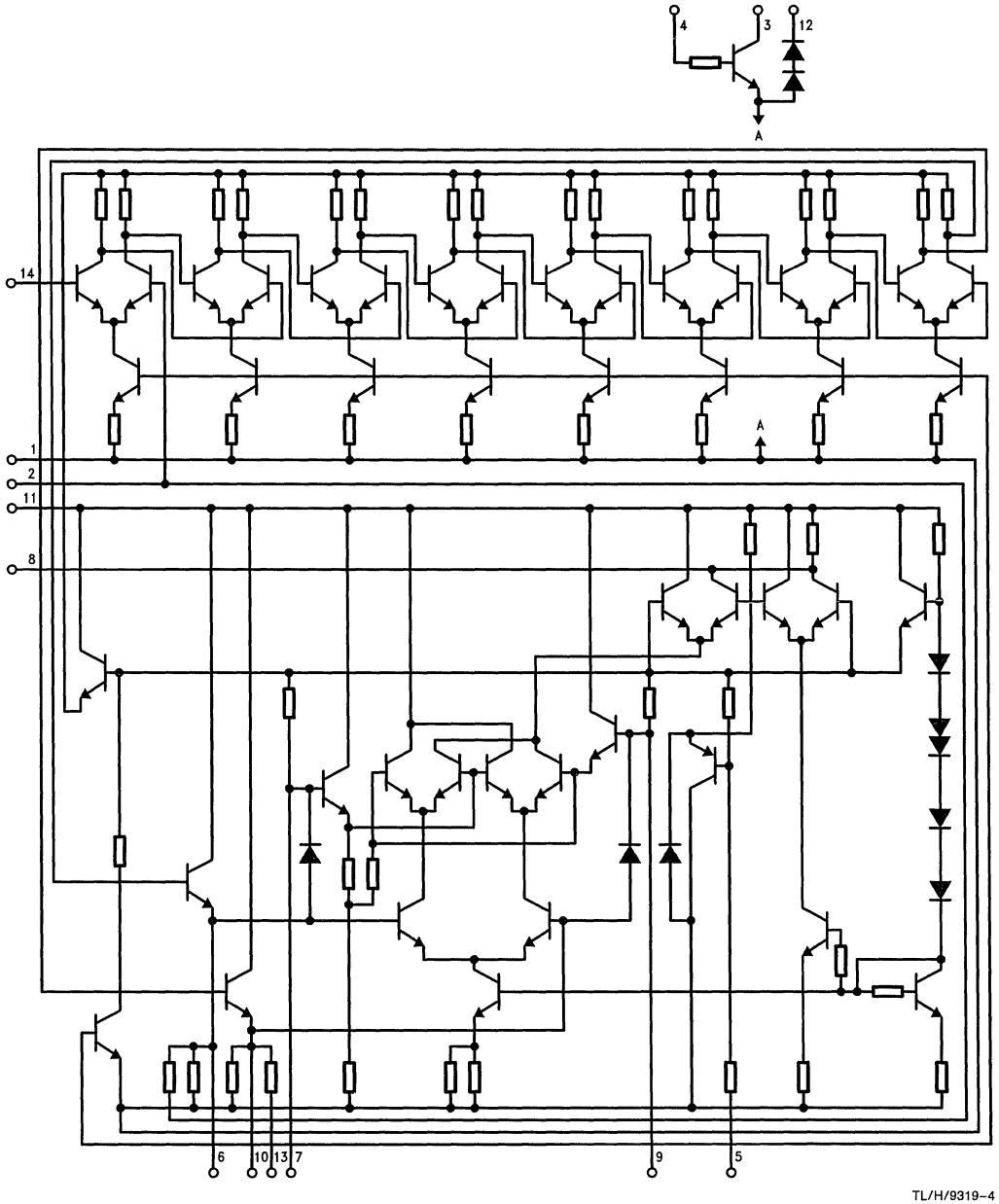
Schematic Diagram



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Section 3

Video Circuits

Section 3 Contents

***Devices Not Covered In Last Publication**

National Semiconductor Corporation

Video
Definition of Terms

Aspect Ratio: The ratio of picture width to picture height. For the NTSC system this is 4:3.

Back Porch: The section of the composite video signal between the trailing edge of the line (horizontal) sync pulse and the end of the blanking pulse period (when picture information begins). For a monochrome signal the back porch is simply at the blanking level. For a color signal, the color burst is added within this section.

Black Level: The DC voltage level in the picture signal which corresponds to beam cut-off on the display tube. It can be at the blanking level (given by the back porch) or slightly higher (7.5% to 10% of the peak white signal above the blanking level).

Blacker-than-Black: The amplitude region in the composite video signal that extends below the reference black level in the direction of the synchronizing pulses.

Blanking: A portion of the composite video signal whose instantaneous amplitude makes the vertical and horizontal scan retrace not visible on the display tube.

Blanking Level: The level of the front and back porches of the composite video signal.

Blanking Period: The period in the composite video signal where the level is reduced to the blanking level, below which the display electron beam is cut-off. This allows non-visible retrace of the beam from the right side of the display to the left side at the end of each scan line (horizontal blanking) and non-visible return of the electron beam from the bottom of the display to the top. Horizontal blanking occurs for approximately 11 μs between each scan line and vertical blanking for 1.2 ms between each field.

Blooming: Defocussing of the picture in regions where the brightness is too high.

Breezeway: The section in the signal blanking period between the end of the sync pulse and the start of the color burst.

C.C.I.R.: International Radio Consultative Committee—a worldwide standards organization.

Chrominance Signal: That part of the NTSC signal that contains the color information.

Clamping: A process that established a fixed DC voltage level for the picture signal. This is important for proper RF modulation and for maintaining the correct picture black level.

Color: An attribute of an object being scanned that distinguishes it from other objects, apart from shape, texture, and brightness. In television systems the color of an object is further subdivided into hue (tint) and saturation. The hue or tint refers to the dominant wavelength of a spectral color, i.e., light red is the same hue as deep red and dark red. Deep red has more vividness or saturation (less white), whereas dark red has less brightness. Similar terms are used to describe non-spectral colors (a mixture of hues).

Color Burst: Normally refers to approximately 9 cycles of the 3.58 MHz subcarrier superimposed on the back porch of the composite video signal. The phase of this burst establishes the reference color phase for tint or hue, and the amplitude provides a reference for the color saturation level.

Color Subcarrier: A subcarrier at 3.579545 MHz (NTSC) whose modulation sidebands are added to a monochrome video signal to convey the color information. Similar subcarriers are used for SECAM and PAL.

Composite Video Signal: The complete video signal. For monochrome, it consists of blanking and synchronizing signals, with a picture signal representing the scene brightness. For color, an additional subcarrier is added for color synchronization and picture color content.

Compression: An undesired decrease in amplitude of one portion of the composite video signal relative to another portion.

Contrast: The range of dark and light values in a picture.

Cross-talk: An undesired signal interfering with a desired signal.

Definition: See resolution.

Differential Gain: The amplitude change in the 3.58 MHz color subcarrier as the picture signal varies from blanking to peak white level. This is the result of system non-linearities and is measured in percent change.

Differential Phase: The phase change, measured in degrees, of the 3.58 MHz color subcarrier as the picture signal varies from blanking to peak white level.

Equalizing Pulses: Pulses of one half the width of the line (horizontal) sync pulses, transmitted at twice the line rate for the three line periods before and after the field (vertical) sync pulse. They are used to help the vertical sync system of the receiver accommodate the half line difference in the number of scan lines on successive fields.

Field: One half of a complete picture interval. A field will contain either all the odd numbered scanning lines or all the even numbered scanning lines in the picture.

Field Frequency: The rate at which a complete field is scanned. For NTSC color signals this is nominally 59.94 Hz.

Fly-back: See Horizontal Retrace.

Frame: A complete picture consisting of two interlocking fields.

Frame Frequency: The rate at which a complete frame is scanned. In the U.S. this is nominally 30 frames or pictures per second.

Front Porch: The section of the composite video signal between the end of the picture information on a scan line (start of blanking) and the start of the line synchronization pulse.

Horizontal Blanking: The blanking signal at the end of each scan line that prevents the retrace of the display tube electron beam from being visible.

Horizontal Retrace: The rapid return of the scanning electron beam from the right side of the raster to the left side.

Horizontal Hum Bars: Relatively broad horizontal bars drifting slowly up the screen as a result of interference from the 60 Hz main frequency.

Hue (Tint): Describes the color that is being represented on the screen, i.e., red, blue, magenta, green, orange, etc.

Interlace: A scanning process in which each adjacent line belongs to the alternate field.

I.R.E.: Institute of Radio Engineers. Now combined with the AIEE to form the IEEE.

I.R.E. Scale: An oscilloscope scale calibrated for composite video and divided vertically into 140 units. The picture signal occupies the range from 0 to 100 with syncs in the range 0 to −40.

Luminance: The monochrome or brightness part of the color signal, composed of specific proportions of the three primary colors, red, blue, and green.

N.T.S.C.: National Television System Committee, used in reference to the system adopted for color television broadcasting in the U.S. at the end of 1953.

Noise: In a television picture, 'noise' refers to random interference producing a salt and pepper pattern over the picture. Heavy noise totally obscuring the picture is called "snow".

Overshoot: An (excessive) response to a unidirectional signal change. Overshoot is often used deliberately to enhance the luminance portion of a signal.

Pairing: A partial or complete failure of interlace in which scan lines of alternate fields fall in pairs, one on top of the other.

Pedestal Level: See Blanking Level.

Percentage Sync:

Video: The ratio in percent of the amplitude of the synchronizing pulse to the peak amplitude of the picture signal between blanking and reference white level. For a properly constituted composite video signal this is 40%.

RF: The ratio is a percent of the amplitude of the synchronizing pulse to the peak amplitude of the modulated RF signal. For correct modulation this is 25%.

P.A.L.: Phase Alternation Line. A variation of the NTSC system involving phase reversal of one of the color difference signals on a line by line basis, introduced into the U.K. and Germany in 1967.

Picture Signal: That portion of the composite video signal which is above the blanking level and contains the picture information.

Pre-emphasis: An increase in the level of a band of frequency components with respect to the remainder of the signal. For U.S. television, the audio signal is increased at a 6 db/octave rate above 2.1 kHz.

Raster: The area on the face of the display tube that is scanned by the electron beam. This is not always entirely visible since commercial receivers employ overscan so that the edges of the raster are hidden by the faceplate.

Reference Signals: See V.I.T.S. and V.I.R.S.

Resolution (Horizontal): The amount of resolvable detail in the horizontal direction of the picture. This depends on the high frequency and phase response of the transmission system and the receiver.

Resolution (Vertical): The amount of resolvable detail in the vertical direction of the picture. This depends primarily on the number of scan lines that are used and secondarily on the size (shape) of the electron scanning beam.

Saturation (Color): The amplitude of the chrominance signal. Increased saturation means increased chrominance signal level. Visibly, this refers to a color increasing from pale or pastel to deep.

S.E.C.A.M.: Sequential Couleur Avec Memoire. The color broadcasting system used predominantly in France which utilizes sequential transmission of the color difference signals, which are FM modulated on two separate subcarriers (1967).

Setup: The difference in level between the blanking level and the reference black level expressed as a percent of the reference white level.

Smear: Smear describes a picture condition where objects appear extended in the horizontal direction producing an ill-defined, blurry picture. This often occurs when the receiver is tuned slightly above the proper pix carrier frequency.

Sync: Abbreviation for synchronizing or synchronization.

Sync Level: The level of the synchronizing pulse tips.

Vertical Blanking: The blanking signal at the end of each field starting three lines before the vertical sync pulse.

Vertical Retrace: The return of the electron beam from the bottom of the display to the top after a complete field has been scanned.

V.I.R.S.: Vertical Interval Reference Signal. A quality control signal added to a horizontal scan line during the vertical blanking period. It is used to provide a chrominance, luminance and black level reference.

V.I.T.S.: Vertical Interval Test Signals. A series of test signals that are added to horizontal lines during the vertical blanking for in-service testing of the transmission equipment. They can be deleted or added at various points in the transmission link, unlike the VIRS, which is added at program origination and stays with the program material.

Vestigal Sideband Transmission: A broadcast transmission technique wherein only one side band of an amplitude modulated carrier is fully transmitted with the other sideband (usually lower) truncated.

Video: The visible portion of the transmitted signal representing the picture.

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Video Selection Guide

VIDEO AMPLIFIERS

	Bandwidth	Gain	Package	Supply Voltage	Comments
LM592	120 MHz	100, 400	14 Pin DIP 14 PIN SO	±3V–±6V	Differential IN, Differential OUT
LM733	120 MHz	10, 100, 400	14 Pin DIP	±3V–±6V	Differential IN, Differential OUT
LM1201 (Advanced Information)	100 MHz	4–10	16 Pin DIP	+12V	Single Amplifier with Black Level and Contrast Control
LM1203	50 MHz	4–10	28 Pin DIP	+12V	Triple Amplifier System with Black Level and Contrast Control
LM359 (Note 1)	400 MHz GBW 30 MHz @ $A_V = 1$		14 Pin DIP	5V–22V	Dual Norton Amplifiers

VIDEO TIMING

	Function	Package	Supply Voltage	Comments
LM1391	PLL	8 Pin DIP	Internal Shunt Zener	—
LM1880	No-Holds Vert/Horiz	14 Pin DIP	Internal Shunt Zener	—
LM1881	Sync Separator	8 Pin DIP 8 Pin SO	5V–15V	Outputs Provided: Composite Sync Vertical Burst Gate Odd/Even Field

VIDEO MODULATORS/DEMODULATORS

	Function	Package	Comments
LM1496 (Note 2)	Balanced Modulator-Demodulator (Modulator—Suppressed Carrier, AM Demodulator—Synchronous, FM Phase Detection)	14 Pin DIP 10 Pin TO-5 14 Pin SO	Operating Frequency to 100 MHz Balanced Inputs and Outputs
LM1889	Modulates Color Difference, Luminance, Audio onto Low-VHF Channels	18 Pin DIP	DC Channel Switching Chroma Reference
LM2889	Modulates Composite Video, Audio onto Low-VHF Channels	14 Pin DIP	DC Channel Switching, Low Distortion FM Sound Modulator, Video Clamp

Note 1: Data sheet in Linear 1.

Note 2: Data sheet in Linear 3—Special Functions Chapter 5.

VIDEO IFs

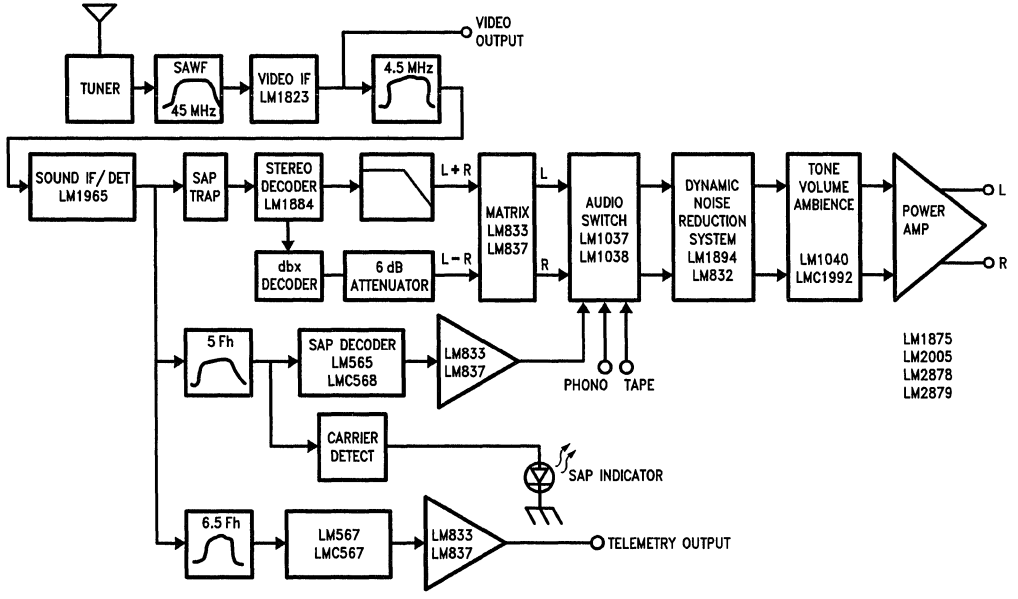
	Application	Package	Comments
LM1211 (Note 3)	Broadband Demodulator	20 Pin DIP	Operating Range 20 MHz–80 MHz Quasi-Synchronous Detector 25 MHz Output Amplifier
LM1823	Video IF	28 Pin DIP	Operating Range 20 MHz–70 MHz Synchronous Detector using PLL 9 MHz Output Amplifier

OTHER VIDEO PRODUCTS

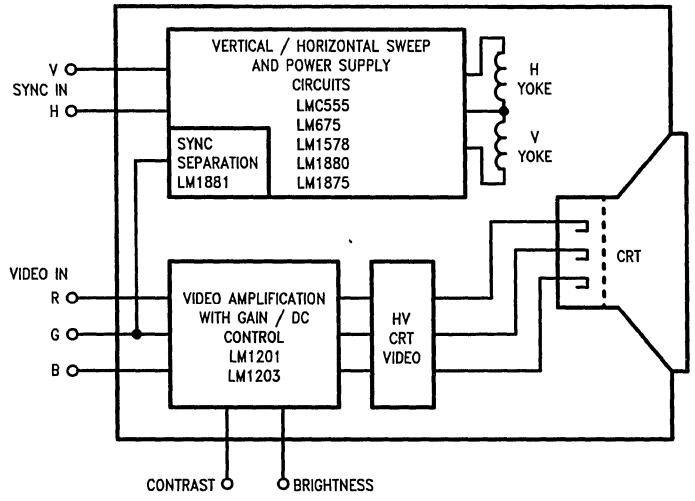
	Function	Package	Supply Voltage	Comments
LM1044	Video Switch	24 Pin DIP	8V–16V	• DC Switch between 3 Composite Video Channels or 2 RGB Channels • 60 dB Channel Separation
LM1884 (Note 4)	TV Stereo Decoder	16 Pin DIP	9V–15V	Provides L − R, L + R Outputs from Composite Input
LM1886	TV Video Matrix D to A	20 Pin DIP	+5V, +12V	Encodes Luminance and Color Difference Signals from 3-Bit RGB Inputs

Note 3: Data Sheet in Linear 3.

Note 4: Data Sheet in Linear 3.



TL/XX/0012–1



TL/XX/0012-2

FIGURE 1. Typical RGB Color Monitor Block Diagram

Application Notes* Cross Reference

Device	AN #
LM359	AN-278, AB-24
LM1823	AN-391
LM1886	AN-402
LM1889	AN-402
LM2889	AN-391, AN-402

*National Semiconductor Corporation Linear Application Notes

National Semiconductor Corporation

LM592 Differential Video Amp

General Description

The LM592 is a two stage differential input, differential output, wideband video amplifier. The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. Emitter follower outputs provide low output impedances necessary to drive capacitive loads. This device offers fixed gains of 100 and 400 with no external components plus the flexibility of adjusting the gain from 0 to 400 with the addition of a single resistor. This flexibility also allows the device to be configured as a high pass, low pass, or band pass filter.

The LM592 is ideal for use in magnetic memory systems. The device is also very useful as a video and pulse amplifier in video recorders and other communications systems.

Features

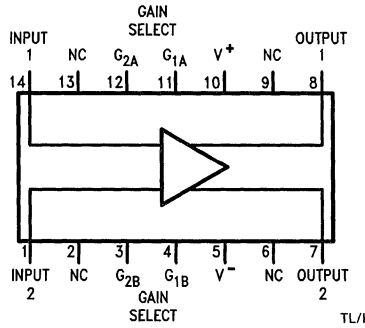
- 120 MHz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required

Applications

- Disc file memories
- Magnetic tape systems
- Thin film or plated wire memories
- Wide band video amplifiers

Connection Diagram

Dual-In-Line and Small Outline Package

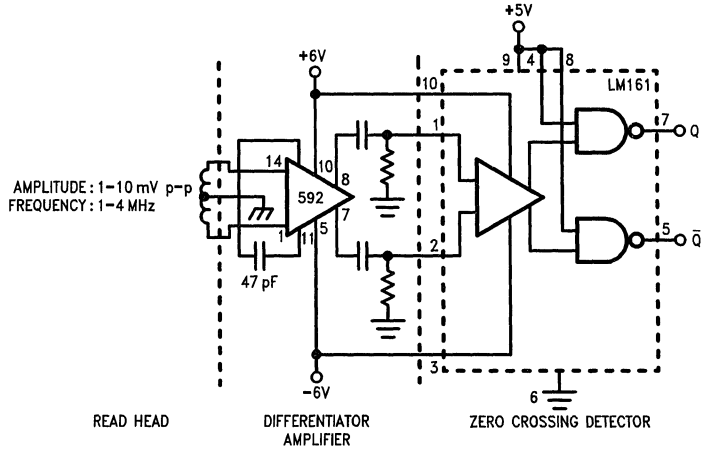


TL/H/6701–1

Top View

Order Number LM592M or LM592N
See NS Package Number M14A or N14A

Disc/Tape Phase Modulated Readback Systems



TL/H/6701–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
V_{supply}	±8V
Output Current	10 mA
Power Dissipation (Note 1)	500 mW
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics T_A = 25°C, unless otherwise specified, see test circuits, V_S = ±6.0V (Note 5)

Characteristics	Test Circuit	Test Conditions	LM592 Typ	LM592 Tested Limit (Note 6)	LM592 Design Limit (Note 7)	Units (Limit)
Differential Voltage Gain						
Gain 1 (Note 2)	1	R_L = 2 kΩ, V_{OUT} = 3 V_{PP}	400	250 600	**210** **620**	(Min) (Max)
Gain 2 (Note 3)			100	80 120	**75** **120**	(Min) (Max)
Bandwidth						
Gain 1			40			MHz
Gain 2	2		90			MHz
Rise Time						
Gain 1		V_{OUT} = 1 V_{PP}	10.5			ns
Gain 2	2		4.5		12	ns (Max)
Propagation Delay						
Gain 1		V_{OUT} = 1 V_{PP}	7.5			ns
Gain 2	2		6		10	ns (Max)
Input Resistance						
Gain 1			4			kΩ
Gain 2			23		10	kΩ (Min)
Input Capacitance		Gain 2	2			pF
Input Offset Current			0.4	5	**6**	μA (Max)
Input Bias Current			9	26	**31**	μA (Max)
Input Noise Voltage		BW = 1 kHz to 10 MHz	12			μV rms
Input Voltage Range	1			±1	**±1**	V (Min)
Common Mode Rejection Ratio						
Gain 2	1	V_{CM} = ±1V	86	60	**50**	dB (Min)
Gain 2		V_{CM} = ±1V, f = 5 mHz	60			dB
Supply Voltage Rejection Ratio						
Gain 2	1	ΔV_S = ±0.5V	70	50	**50**	dB (Min)
Output Offset Voltage						
Gain 1	1	R_L = ∞	0.35	0.75	**0.75**	V (Max)
Output Common Mode Voltage	1	R_L = ∞	2.9	2.4	**2.4**	V (Min)
(Note 4)				3.4	**3.4**	V (Max)
Output Voltage Swing	1	R_L = 2k	4	3	**3**	V (Min)
Output Sink Current			3.6	2.5	**2.3**	mA (Min)
Output Resistance			20			Ω
Power Supply Current	1	R_L = ∞	18	24	**24**	mA (Max)

Note 1: For operation at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{jA} and $T_j$max. θ_{jA} = 90°C/W in the "N" package and 135°C/W in the "M" package. $T_j$max = 150°C.

Note 2: Pins G1A and G1B connected together.

Note 3: Pins G2A and G2B connected together.

Note 4: Gain select pins open. Output Common Mode Voltage = $(V_{01} + V_{02})/2$.

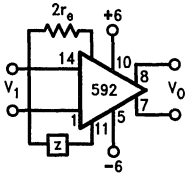
Note 5: Boldface numbers apply at temperature extremes.

Note 6: Guaranteed and 100% production tested.

Note 7: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Typical Applications

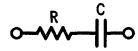
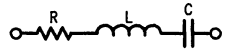
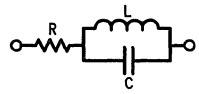
Filter Networks



TL/H/6701–3

$$\frac{V_0(S)}{V_1(S)} = \frac{1.4 \times 10^4}{Z(s) + 2r_e} = \frac{1.4 \times 10^4}{Z(s) + 32}$$

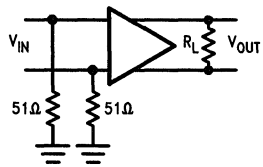
BASIC CONFIGURATION

Impedance Network	Desired Filter	$\frac{V_0(S)}{V_1(S)}$ Transfer Function
 TL/H/6701–10	Low Pass	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
 TL/H/6701–11	High Pass	$\frac{1.4 \times 10^4}{R}\left[\frac{1}{s + 1/RC}\right]$
 TL/H/6701–12	Band Pass	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/Ls + 1/LC}\right]$
 TL/H/6701–13	Band Reject	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

Note: In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω

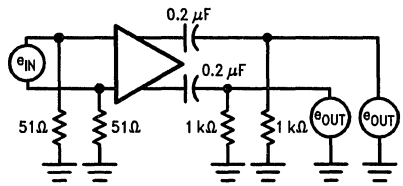
Test Circuits

Test Circuit 1



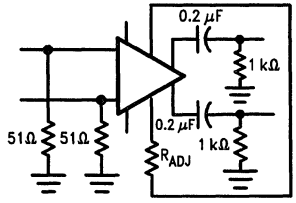
TL/H/6701–4

Test Circuit 2



TL/H/6701–5

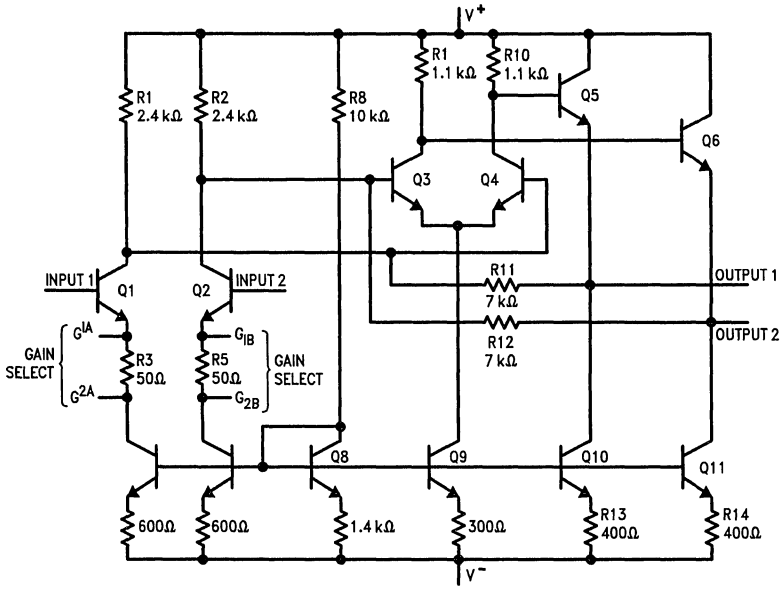
Voltage Gain Adjust Circuit



TL/H/6701–6

$V_S = \pm 6V$
$T_A = 25°C$

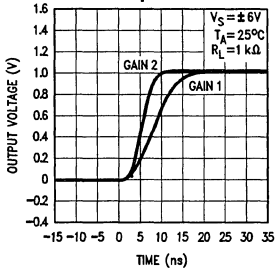
Schematic Diagram



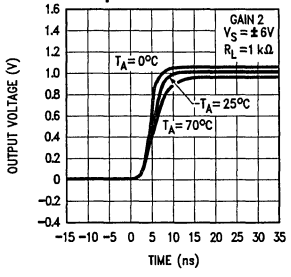
TL/H/6701–7

Typical Performance Characteristics

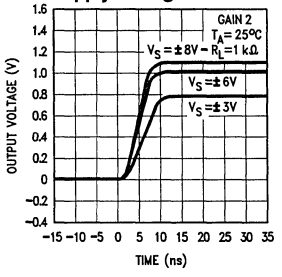
Pulse Response



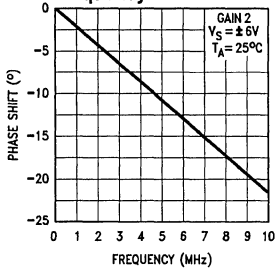
Pulse Response vs Temperature



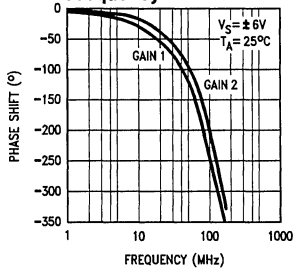
Pulse Response vs Supply Voltage



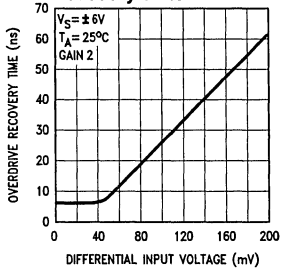
Phase Shift vs Frequency



Phase Shift vs Frequency



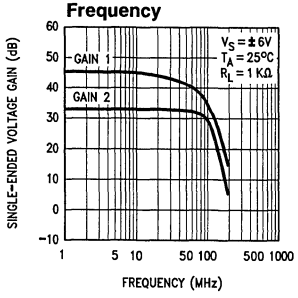
Differential Overdrive Recovery Time



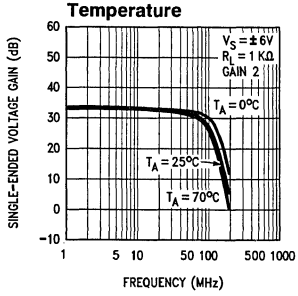
TL/H/6701–8

Typical Performance Characteristics (Continued)

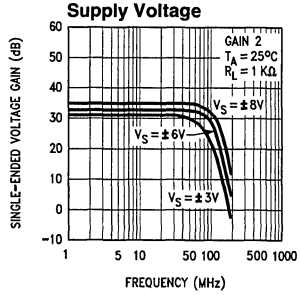
Voltage Gain vs Frequency



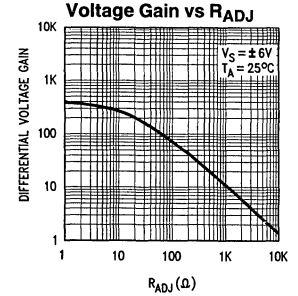
Gain vs Frequency Temperature



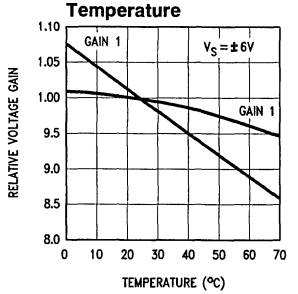
Gain vs Frequency vs Supply Voltage



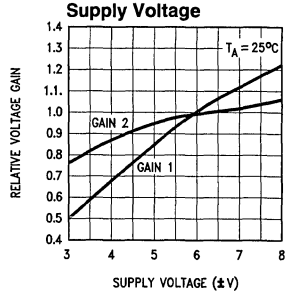
Voltage Gain vs R_{ADJ}



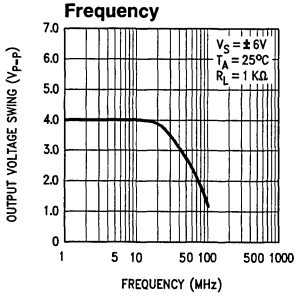
Voltage Gain vs Temperature



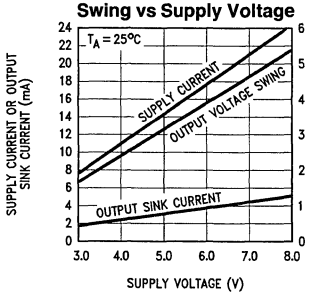
Voltage Gain vs Supply Voltage



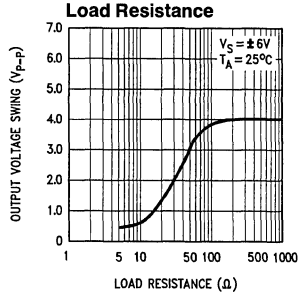
Output Voltage Swing vs Frequency



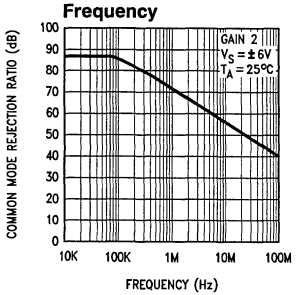
Supply Current, Output Voltage and Current Swing vs Supply Voltage



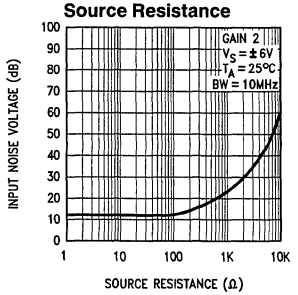
Output Voltage Swing vs Load Resistance



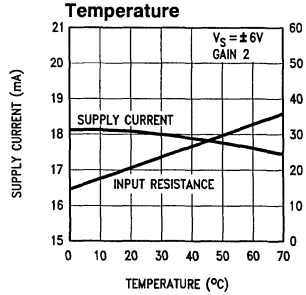
Common Mode Rejection Ratio vs Frequency



Input Noise Voltage vs Source Resistance



Supply Current and Input Resistance vs Temperature



TL/H/6701-9

National Semiconductor Corporation

LM733/LM733C Differential Amp

General Description

The LM733/LM733C is a two-stage, differential input, differential output, wide-band video amplifier. The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. Emitter-follower outputs provide a high current drive, low impedance capability. Its 120 MHz bandwidth and selectable gains of 10, 100 and 400, without need for frequency compensation, make it a very useful circuit for memory element drivers, pulse amplifiers, and wide band linear gain stages.

The LM733 is specified for operation over the −55°C to +125°C military temperature range. The LM733C is specified for operation over the 0°C to +70°C temperature range.

Features

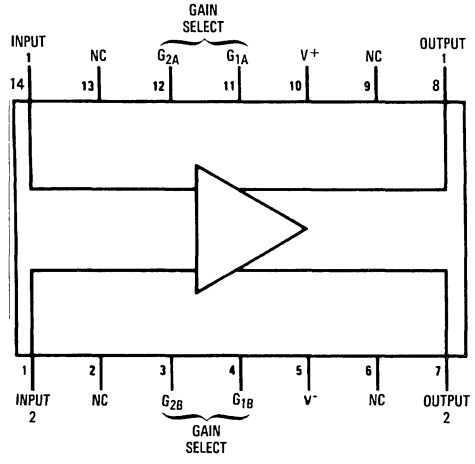
- 120 MHz bandwidth
- 250 kΩ input resistance
- Selectable gains of 10, 100, 400
- No frequency compensation
- High common mode rejection ratio at high frequencies

Applications

- Magnetic tape systems
- Disk file memories
- Thin and thick film memories
- Woven and plated wire memories
- Wide band video amplifiers

Connection Diagrams

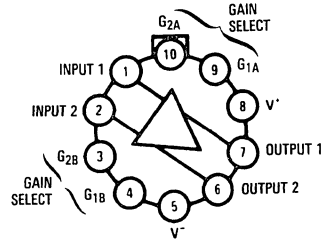
Dual-In-Line Package



TL/H/7866–1

Top View
Order Number LM733CN
See NS Package Number N14A

Metal Can Package



TL/H/7866–2

Note: Pin 5 connected to case.

Top View
Order Number LM733H or LM733CH
See NS Package Number H10D

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Diffential Input Voltage	±5V
Common Mode Input Voltage	±6V
V_{CC}	±8V
Output Current	10 mA
Power Dissipation (Note 1)	500 mW
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LM733	−55°C to +125°C
LM733C	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuits, V_S = ±6.0V)

Characteristics	Test Circuit	Test Conditions	LM733			LM733C			Units
			Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain									
Gain 1 (Note 2)			300	400	500	250	400	600	
Gain 2 (Note 3)	1		90	100	110	80	100	120	
Gain 3 (Note 4)		R_L = 2 kΩ V_{OUT} = 3 Vp-p	9.0	10	11	8.0	10	12	
Bandwidth									
Gain 1				40			40		MHz
Gain 2	2			90			90		MHz
Gain 3				120			120		MHz
Rise Time									
Gain 1		V_{OUT} = 1 Vp-p		10.5			10.5		ns
Gain 2	2			4.5	10		4.5	12	ns
Gain 3				2.5			2.5		ns
Propagation Delay		V_{OUT} = 1 Vp-p							
Gain 1				7.5			7.5		ns
Gain 2	2			6.0	10		6.0	10	ns
Gain 3				3.6			3.6		ns
Input Resistance									
Gain 1				4.0			4.0		kΩ
Gain 2			20	30		10	30		kΩ
Gain 3				250			250		kΩ
Input Capacitance		Gain 2		2.0			2.0		pF
Input Offset Current				0.4	3.0		0.4	5.0	μA
Input Bias Current				9.0	20		9.0	30	μA
Input Noise Voltage		BW = 1 kHz to 10 MHz		12			12		μVrms
Input Voltage Range	1		±1.0			±1.0			V
Common Mode Rejection Ratio									
Gain 2	1	V_{CM} = ±1V f ≤ 100 kHz	60	86		60	86		dB
Gain 2		V_{CM} = ±1V f = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio									
Gain 2	1	ΔV_S = ±0.5V	50	70		50	70		dB
Output Offset Voltage									
Gain 1	1	R_L = ∞		0.6	1.5		0.6	1.5	V
Gain 2 and 3				0.35	1.0		0.35	1.5	V
Output Common Mode Voltage	1	R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	1	R_L = 2k	3.0	4.0		3.0	4.0		
Output Sink Current			2.5	3.6		2.5	3.6		mA
Output Resistance				20			20		Ω
Power Supply Current	1	R_L = ∞		18	24		18	24	mA

Electrical Characteristics (Continued)

(The following specifications apply for $-55°C < T_A < 125°C$ for the LM733 and $0°C < T_A < 70°C$ for the LM733C, $V_S = \pm 6.0V$)

Characteristics	Test Circuit	Test Conditions	LM733			LM733C			Units
			Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain Gain 1 Gain 2 Gain 3	1	$R_L = 2\,k\Omega$, $V_{OUT} = 3$ Vp-p	 200 80 8.0		 600 120 12.0	 250 80 8.0		 600 120 12.0	
Input Resistance Gain 2			8			8			kΩ
Input Offset Current					5			6	μA
Input Bias Current					40			40	μA
Input Voltage Range	1		±1			±1			V
Common Mode Rejection Ratio Gain 2	1	$V_{CM} = \pm 1V$ f ≤ 100 kHz	50			50			dB
Supply Voltage Rejection Ratio Gain 2	1	$\Delta V_S = \pm 0.5V$	50			50			dB
Output Offset Voltage Gain 1 Gain 2 and 3	1	$R_L = \infty$			 1.5 1.2			 1.5 1.5	 V V
Output Voltage Swing	1	$R_L = 2k$	2.5			2.8			V_{pp}
Output Sink Current			2.2			2.5			mA
Power Supply Current	1	$R_L = \infty$			27			27	mA

Note 1: The maximum junction temperature of the LM733 is 150°C, while that of the LM733C is 100°C. For operation at elevated temperatures devices in the TO-100 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case. Thermal resistance of the dual-in-line package is 90°C/W.

Note 2: Pins G1A and G1B connected together.

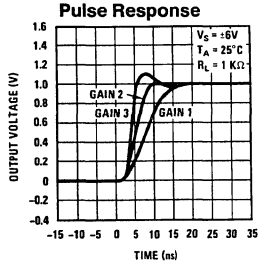
Note 3: Pins G2A and G2B connected together.

Note 4: Gain select pins open.

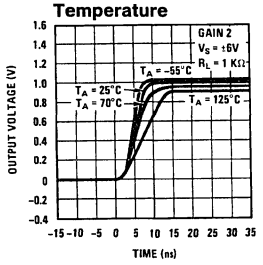
Note 5: Refer to RETS733X drawing for specifications of LM733H version.

Typical Performance Characteristics

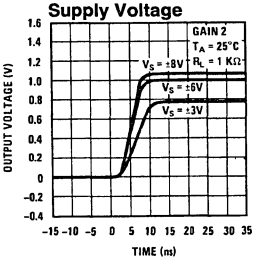
Pulse Response



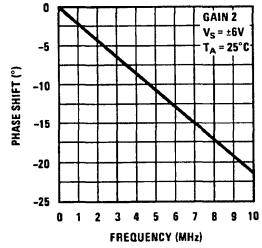
Pulse Response vs Temperature



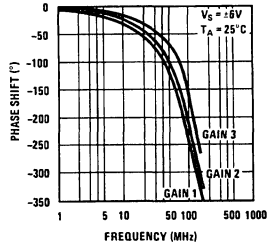
Pulse Response vs Supply Voltage



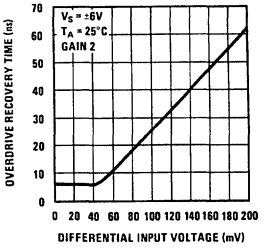
Phase Shift vs Frequency



Phase Shift vs Frequency



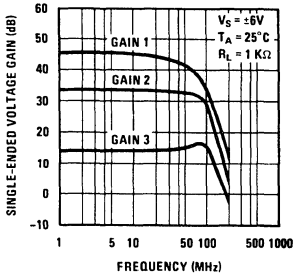
Differential Overdrive Recovery Time



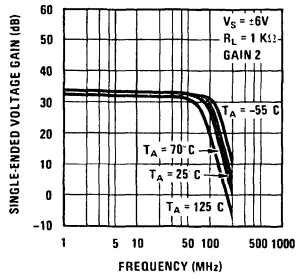
TL/H/7866–6

Typical Performance Characteristics (Continued)

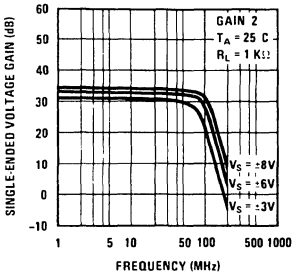
Voltage Gain vs Frequency



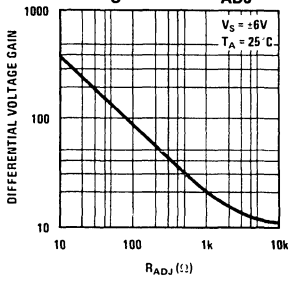
Gain vs Frequency Temperature



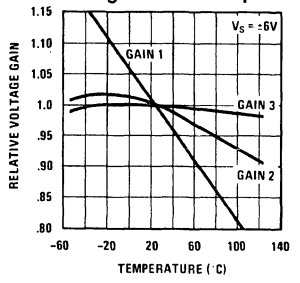
Gain vs Frequency vs Supply Voltage



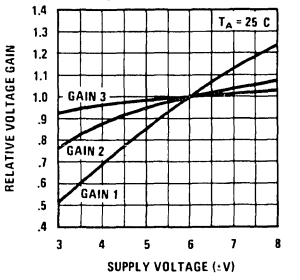
Voltage Gain vs R_{ADJ}



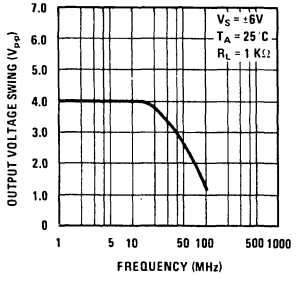
Voltage Gain vs Temperature



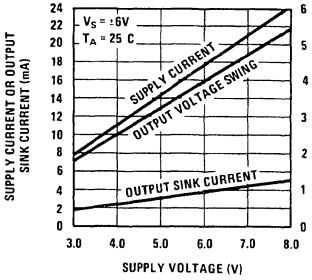
Voltage Gain vs Supply Voltage



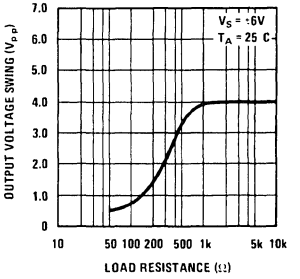
Output Voltage Swing vs Frequency



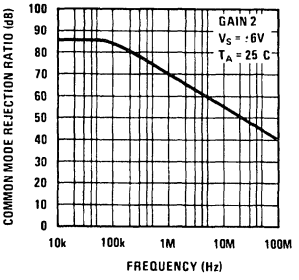
Supply Current, Output Voltage and Current Swing vs Supply Voltage



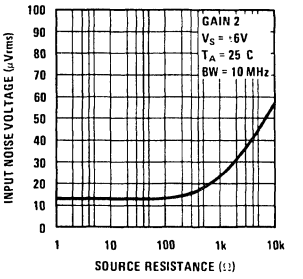
Output Voltage Swing vs Load Resistance



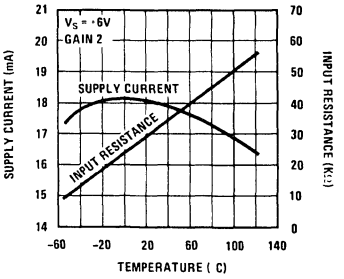
Common Mode Rejection Ratio vs Frequency



Input Noise Voltage vs Source Resistance



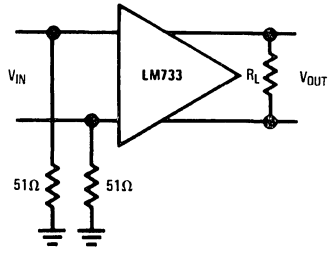
Supply Current and Input Resistance vs Temperature



TL/H/7866–7

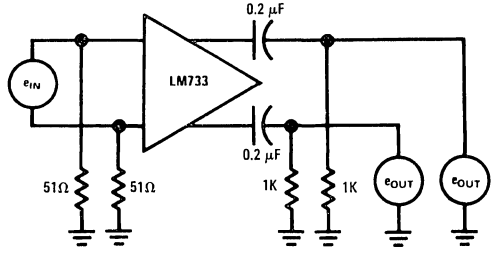
Test Circuits

Test Circuit 1



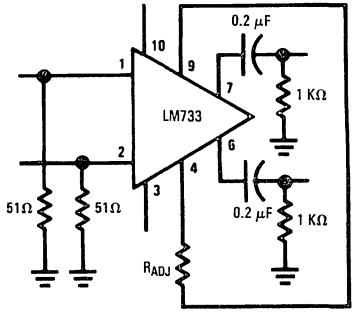
TL/H/7866–3

Test Circuit 2



TL/H/7866–4

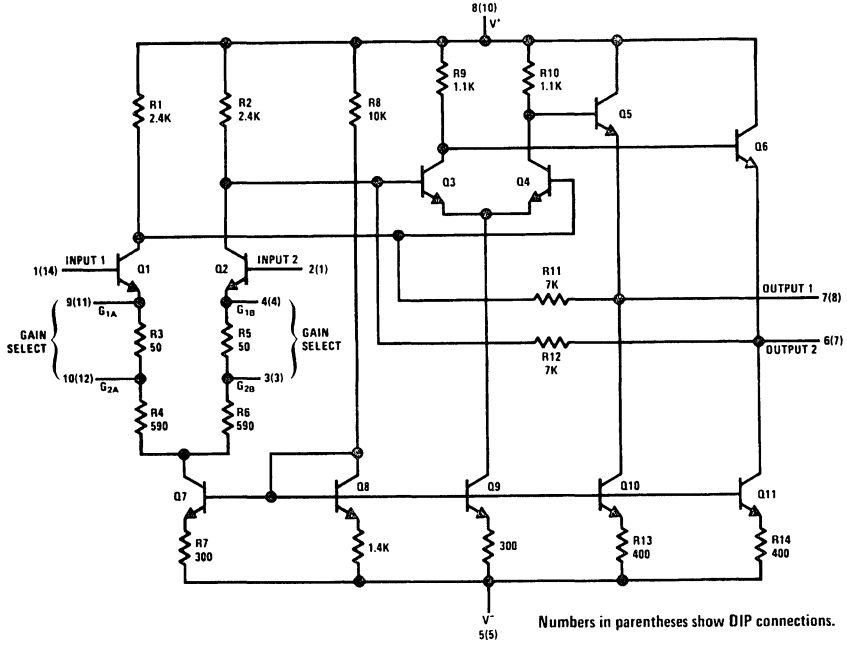
Voltage Gain Adjust Circuit



TL/H/7866–5

V_S = 6V, T_A = 25°C
(Pin numbers apply to TO-5 package)

Schematic Diagram



TL/H/7866–8

National Semiconductor Corporation

PRELIMINARY

LM1044 Analog Video Switch

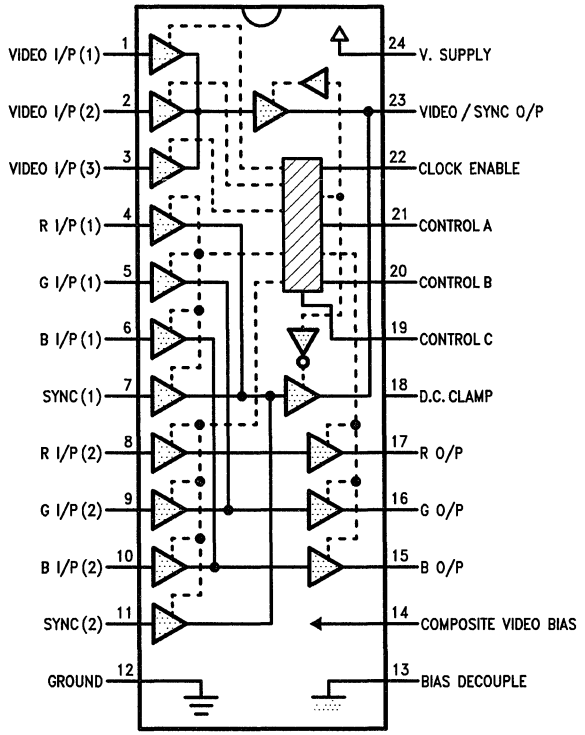
General Description

The LM1044 is a monolithic D.C. controlled analog switch, allowing the selection of any one of three composite video channels of voltage gain +6 dB or two R.G.B. channels with voltage gains of 0 dB. Channel selection is achieved by utilizing clocked, TTL compatible control logic which can interface to most micro-controllers. The device is supplied in a 24 pin dual-in-line package.

Features

- R.G.B. channels are level clamped
- Wide bandwidth, typically 10 MHz @ 2 V_{p-p}
- High signal to noise ratio, typically −60 dB
- Excellent channel isolation and crosstalk typically −60 dB and −50 dB respectively @ 5 MHz
- High RGB output currents, typically 4 mA peak
- Logically compatible with LM1038 audio select switch

Block Diagram



TL/H/9252–1

Order Number LM1044N
See NS Package Number N24A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	V_S = 17V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics V_S = 12V, T_A = 25°C unless otherwise stated

Parameter	Conditions	Test Limit		Design Limit			Units
		Min	Max	Min	Typ	Max	
Supply Voltage		8	16	8	12	16	V
Supply Current			60		42	60	mA
P.S.R.R.	Signal = 1 V_{p-p} @ 1 kHz	50			50		dB
Signal To Noise Ratio					60		dB
TTL High Level (A,B,C Enable)		2.0		2.0			V
TTL Low Level (A,B,C Enable)			0.8			0.8	V
Enable Pulse Length					5.0		μs
Channel Select Time					4.0		μs
COMPOSITE VIDEO CHANNELS							
Maximum Input Voltage Swing	R_L = 600Ω, V_S = 12V Output T.H.D. = 1%	1.5		1.5			V_{p-p}
Input Impedance					2.0		kΩ
Dynamic Output Impedance					10		Ω
Voltage Gain	Signal = 500 mV @ 1 MHz	5.5		5.5	6.0	6.5	dB
Bandwidth	−3 dB, R_L = 600Ω	6.0		6.0	10.0		MHz
Channel Isolation In Mute	Signal = 500 mV @ 5 MHz				−60		dB
Crosstalk	Signal = 500 mV @ 5 MHz				−50		dB
Load Resistance				600			Ω
R.G.B. CHANNELS							
Clamp Drive High Level Threshold				9.0			V
Clamp Drive Low Level Threshold						5.0	V
Clamp Pulse Delay					0.2		ns
Input Voltage Swing	R_L = 600Ω Output T.H.D. = 1%					3.0	V_{p-p}

Electrical Characteristics V_S = 12V, T_A = 25°C unless otherwise stated (Continued)

Parameter	Condition	Test Limit		Design Limit			Units
		Min	Max	Min	Typ	Max	
Input Impedance					2.0		kΩ
Dynamic Output Impedance					10		Ω
Voltage Gain	Signal = 500 mV @ 1 MHz	−0.5		−0.5	0	+0.5	dB
Input Bias Current	Clamp Drive Low. DC bias = 7V		50			50	μA
Bandwidth	−3 dB, R_L = 600Ω	6.0		6.0	10.0		MHz
Load Resistance				600			Ω
Channel Isolation	Signal = 500 mV @ 5 MHz			−60			dB
Crosstalk	Signal = 500 mV @ 5 MHz			−50			dB

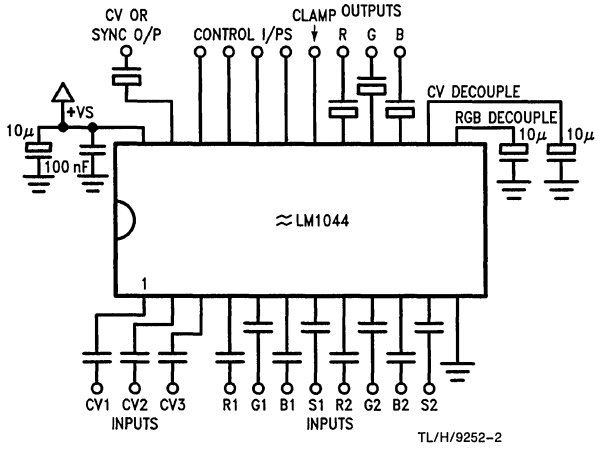
Application Notes

Signal channel selection is achieved by the application of D.C. voltages to control pins 19, 20, 21, and 22. Pin 22 is the logic enable pin and may be used to clock in logic data on pins 19, 20, and 21 by applying a pulse of > 5 μs. Alternatively pin 22 may be wired TTL HIGH and channels selected directly by applying the appropriate logic levels on pins 19, 20 and 21.

The control logic of the LM1044 is designed to be compatible with that of the LM1038N four channel stereo audio switch. The control pins of each device may be connected in parallel to give stereo audio selection on Composite Video channels 1, 2 and 3 and RGB channel 1. This is achieved by connecting pins 19, 20, 21 and 22 of the LM1044 to pins 1, 16, 3 and 18 of the LM1038N respectively.

Control Logic				Channel Selected
Pin 22	Pin 19	Pin 21	Pin 20	
1	0	0	0	Composite Video 1, RGB outputs muted
1	0	0	1	Composite Video 2, RGB outputs muted
1	0	1	0	Composite Video 3, RGB outputs muted
1	0	1	1	RGB 1 with sync.
1	1	1	1	RGB 2 with sync.
1	1	0	1	Mute
1	1	1	0	Mute
1	1	0	0	Mute
0	X	X	X	Previous selection retained

Application Circuits



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Coupling Capacitors	
RGB and Sync i/ps	100 nF
RGB and Sync o/ps	10 μF
Composite Video o/p	10 μF
Composite Video i/ps	100 nF

National Semiconductor Corporation

ADVANCED INFORMATION

LM1201 Video Amplifier System

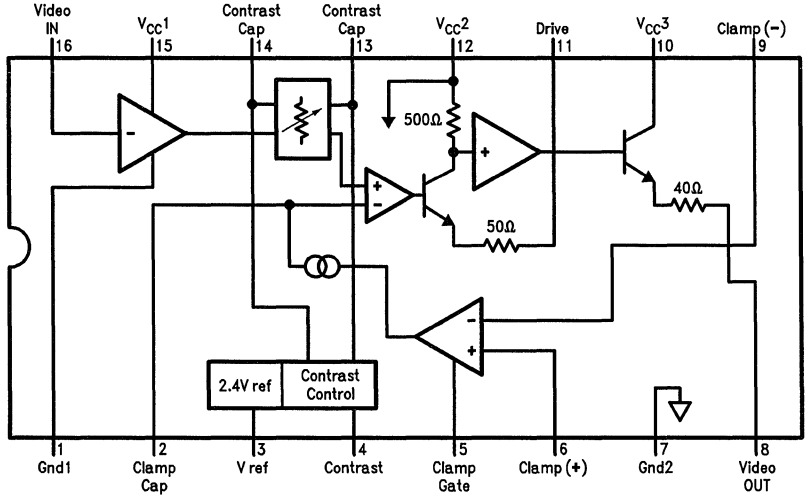
General Description

The LM1201 is a wideband video amplifier system intended for high resolution monochrome or RGB monitor applications. In addition to the wideband video amplifier the LM1201 contains a gated differential input black level clamp comparator for brightness control and an attenuator circuit for contrast control. The LM1201 also provides a "Drive" pin for setting system gain and peaking of the video amplifier. The LM1201 also contains a voltage reference for the video input. For medium resolution RGB color monitor applications also see the LM1203 Video Amplifier System data sheet.

Features

- Wideband video amplifier (100 MHz)
- Attenuator circuit for contrast control (>40 dB range)
- Externally gated comparator for brightness control
- Provisions for external gain set and peaking of video amplifier
- Video input voltage reference
- Low impedance output driver

Block and Connection Diagram



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Top View

National Semiconductor Corporation

PRELIMINARY

LM1203 RGB Video Amplifier System

General Description

The LM1203 is a wideband video amplifier system intended for high resolution RGB color monitor applications. In addition to three matched video amplifiers, the LM1203 contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain (Av = 4 to 10) as well as providing trim capability. The LM1203 also contains a voltage reference for the video inputs.

Features

- Three wideband video amplifiers (70 MHz @ −3dB)
- Inherently matched (±0.5 dB) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for independent gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Block and Connection Diagram

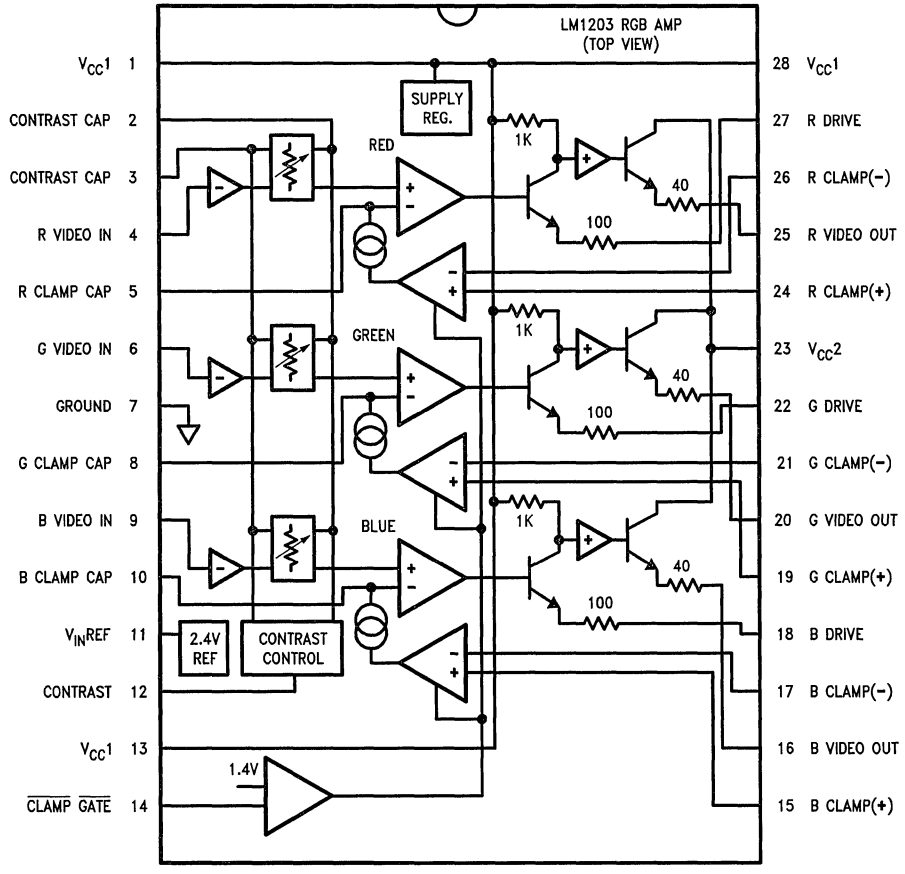

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FIGURE 1
Order Number LM1203N
See NS Package Number N28B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC} Pins 1, 13, 23, 28 (Note 1) 13.5V

Voltage at Any Input Pin, V_{IN} $V_{CC} \geq V_{IN} \geq$ GND

Video Output Current, I16, 20 or 25 28 mA

Power Dissipation, Pd 2.5W

(Above 25°C) Derate Based on θja and T_j

Thermal Resistance, θja 50°C/W

Junction Temperature, T_j 150°C

Operating Temperature Range, T_A 0°C to +70°C

Storage Temperature Range, T_{STG} −65°C to +150°C

Lead Temperature, (Soldering, 10 sec.) 265°C

ESD susceptibility 2 kV

Human body model: 100 pF discharged through a 1.5 kΩ resistor

Electrical Characteristics Test Circuit, T_A = 25°C; $V_{CC1} = V_{CC2}$ = 12V

DC Static Tests S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated

Label	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	(Limits) Units
Is	Supply Current	V_{CC} 1 only	73	90.0		mA Max
V11	Video Input Reference Voltage		2.4	2.2		V_{MIN}
				2.6		V_{MAX}
Ib	Video Input Bias Current	Any One Amplifier	5.0	20		μA Max
V14 l	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8		V_{MIN}
V14 h	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0		V_{MAX}
I14 l	Clamp Gate Low Input Current	V14 = 0V	−0.5	−5.0		μA Max
I14 h	Clamp Gate High Input Current	V14 = V_{CC}	0.005	1		μA Max
Iclamp+	Clamp Cap Charge Current	V5, 8 or 10 = 0V	850			μA
Iclamp−	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	−850			μA
Vol	Video Output Low Voltage	V5, 8 or 10 = 0V	1.2			V
Voh	Video Output High Voltage	V5, 8 or 10 = 5V	8.9			V
ΔVo(2V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 2V	±0.5	±50		mV Max
ΔVo(4V)	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 4V	±0.5	±50		mV Max

AC Dynamic Tests S17, 21, 26 Closed; V14 = 0V; V15 = 4V; f_{IN} = 10 KHz unless otherwise stated

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Av max	Video Amplifier Gain	V12 = 12V, V_{IN} = 560 mVp-p	6.6			V/V
Av mid	Video Amplifier Gain	V12 = 5V, V_{IN} = 560 mVp-p	2			V/V
V12low	V12 for Av Low	V_{IN} = 1 Vp-p (Note 4)	2			V
ΔAv max	Video Gain Match at Av max	V12 = 12V (Note 5)	±0.2			dB
ΔAv mid	Video Gain Match at Av mid	V12 = 5V (Note 5)	±0.2			dB
ΔAv low	Video Gain Match at Av low	V12 = V12 low (Notes 4, 5)	±0.3			dB
T.H.D	Video Amplifier Distortion	V12 = 3V, V_{IN} = 1 Vp-p	0.5			%
f(−3dB)	Video Amplifier Bandwidth	V12 = 12V (Notes 6, 8)	70			MHz

AC Dynamic Tests S17, 21, 26 Closed; V14 = 0V; V15 = 4V; f_{IN} = 10 kHz unless otherwise stated (Continued)

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
Vsep 10 kHz	Video Amplifier 10 kHz Isolation	V12 = 12V (Note 7)	−60			dB
Vsep 10 MHz	Video Amplifier 10 MHz Isolation	V12 = 12V (Notes 7, 8)	−40			dB

Note 1: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

Note 4: Determine V_{12} low for −40 dB attenuation of output. Reference to A_V max.

Note 5: Measure gain difference between any two amplifiers. V_{IN} = 1 Vp-p

Note 6: Adjust input frequency, fin, from 10 kHz (Av max ref level) to the −3 dB corner frequency (f − 3 dB). V_{IN} = 560 mVp-p

Note 7: V_{IN} = 560 mVp-p at f_{IN} = 10 kHz to any one amplifier. Measure output levels of the other two undriven amplifiers relative to driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for Vsep = 10 MHz.

Note 8: Special test fixture without socket required.

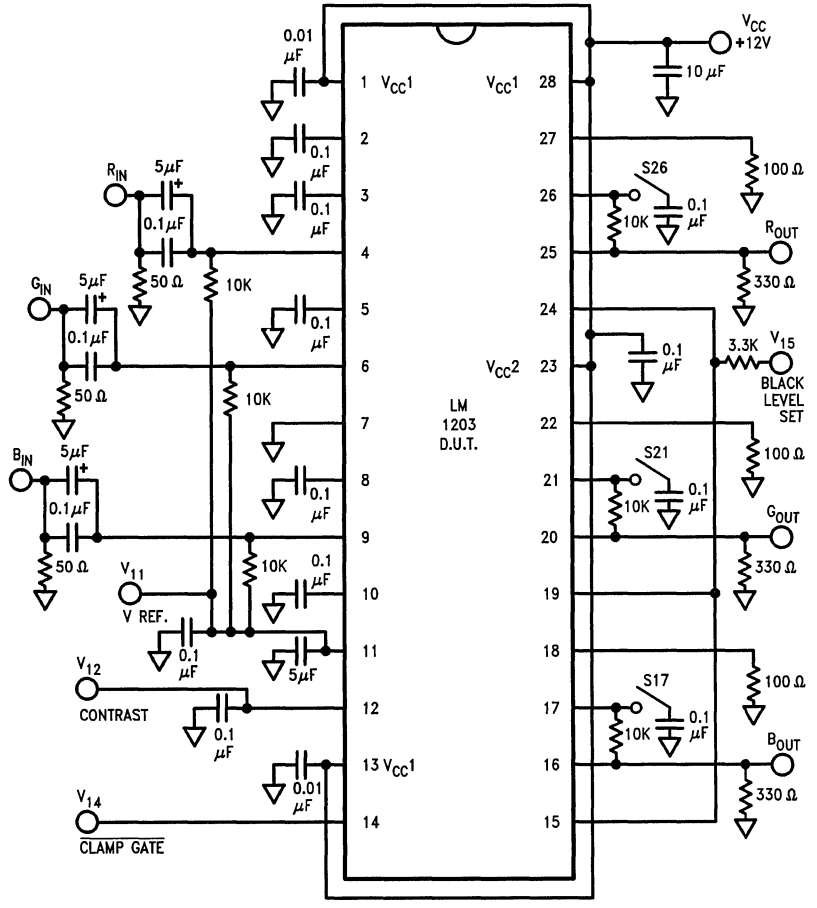

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FIGURE 2. LM1203 Test Circuit

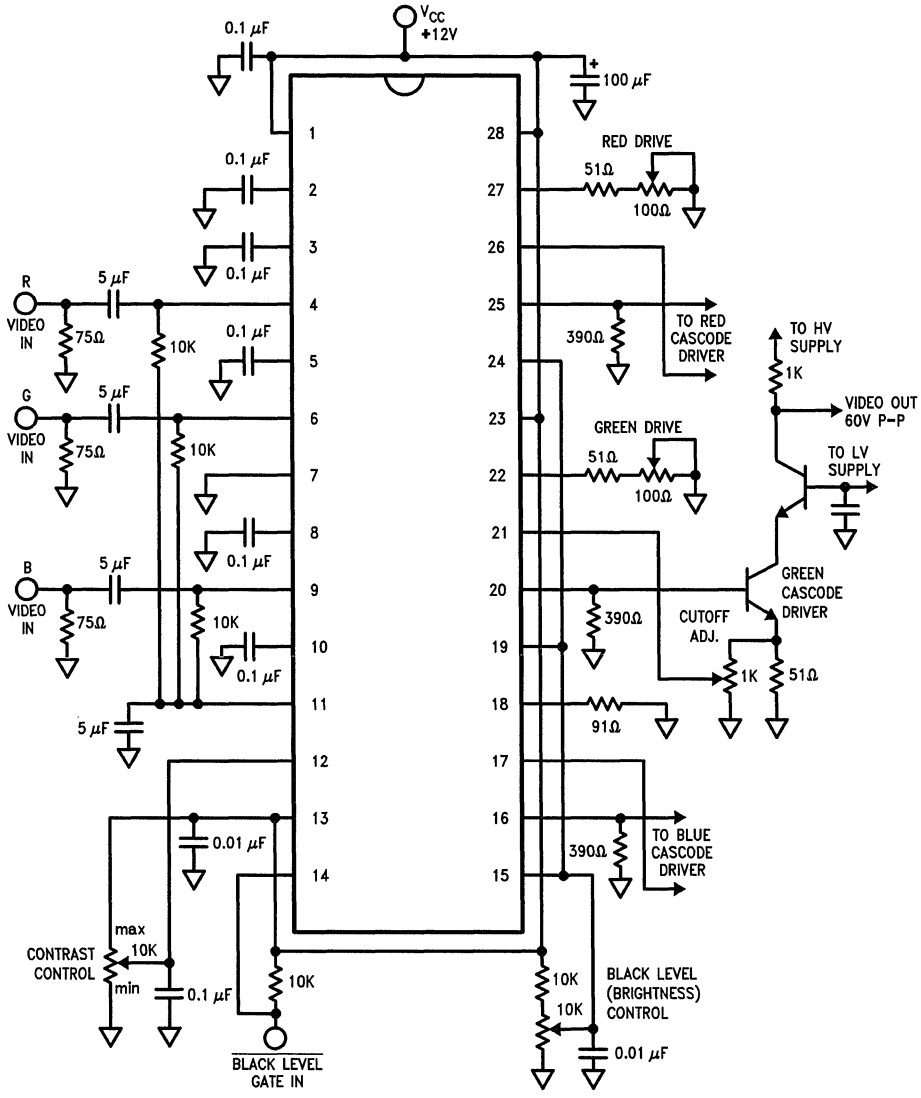

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FIGURE 3. LM1203 Typical Application

LM1203 RGB Video Amplifier Application Notes

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in *Figure 4*. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally ac coupled to the video amplifiers. These input signals are approximately 1 volt peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The *Figure 4* block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203 which contains the three matched video amplifiers, contrast control and brightness control.

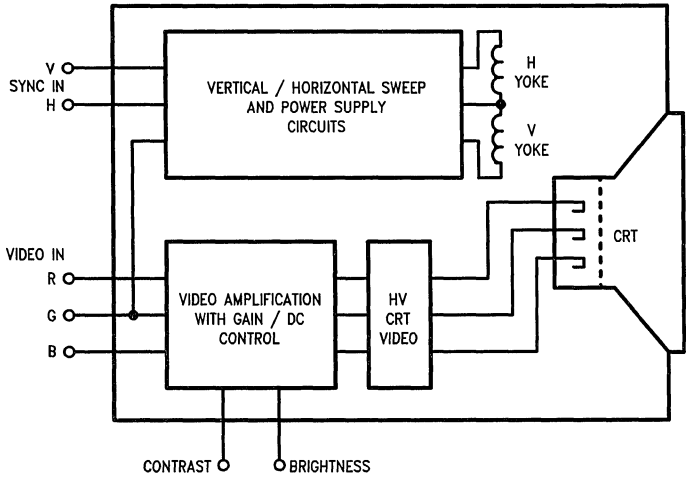

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FIGURE 4. Typical RGB Color Monitor Block Diagram

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a dc-operated attenuator which varies the ac gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the dc bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 5 via the 10 μF coupling capacitor. DC bias to the video input is through the 10 kΩ resistor which is connected to the 2.4V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC} 1 supply directly or through the 1k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. RF decoupling capacitors are required at pins 2 and 3 to insure high frequency isolation between the three video amplifiers which share these common connections. The black level dc voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.

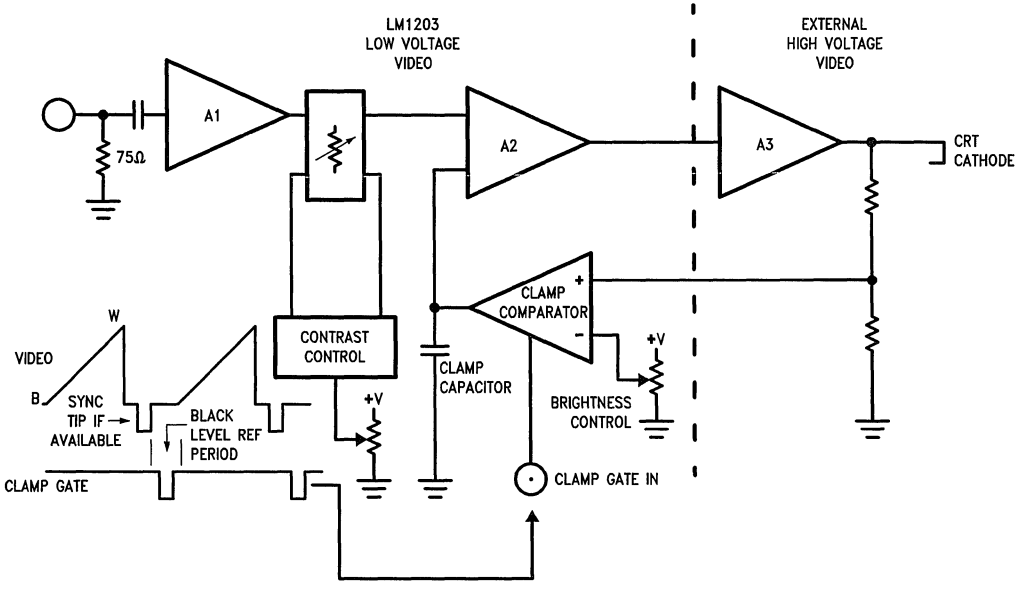

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FIGURE 5. Block Diagram of LM1203 Video Amplifier with Contrast and Black Level Control

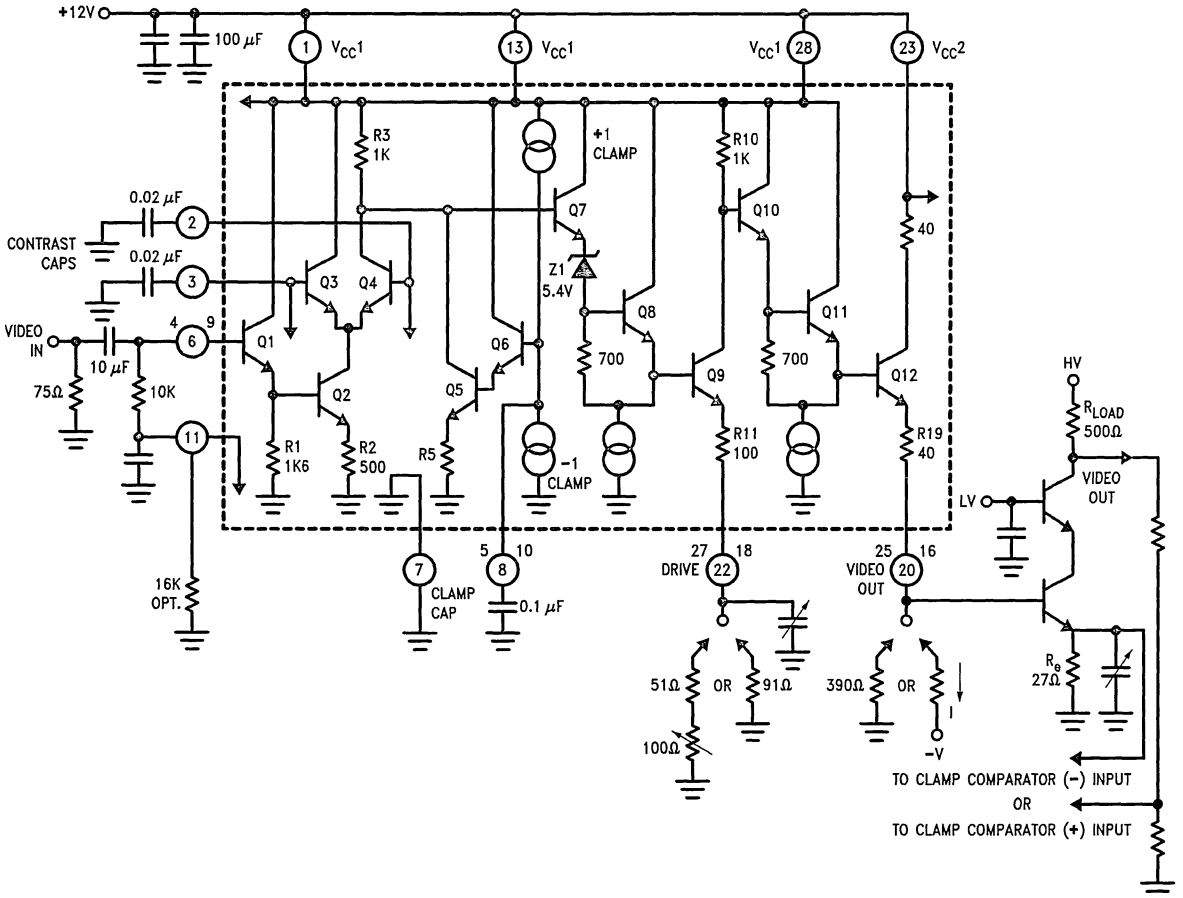

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FIGURE 6. Simplified LM1203 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to trim the Q9 gain of each amplifier to correct for differences in the CRT and high voltage cathode driver gain stages. A small capacitor (33 pF) at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. To use this capacitor and still provide variable gain adjustment, the 51Ω and series 100Ω pot should be used with the red and green drive pins. The 91Ω resistor used with the blue drive pin will set the system gain to approximately 6.5 and allow adjustment of the red and green gains to 6.5 plus or minus 25%. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 40Ω resistor which was included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 390Ω or package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (>10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is −12V and the emitter current is approximately 10 mA. The system gain will also increase slightly because less signal will be lost across the internal 40Ω resistor. Precautions must be taken to prevent the video output pin from going below ground because IC substrate currents may cause erratic operation. The collector currents from the video output transistors are returned to the power supply at V_{CC} 2 pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC} 1 supply current at 12V. The IC power dissipation contribution of VCC 2 is dependent upon the video output emitter pull down load.

In normal operation the minimum black level voltage that can be set at the video output pin is approximately 2V when at maximum contrast. In applications that require a lower black level voltage a resistor (approximately 16 kΩ) can be added from pin 11 to ground. This has the effect of raising the dc voltage at the collector of Q4 which will extend the range of the black level clamp by allowing Q5 to remain active. In applications that require video amplifier shut down because of fault conditions detected by monitor protection circuits, pin 11 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control pots and V_{CC}.

Figure 7 shows the internal construction of the pin 11 2.4V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier inputs. The value of the external DC biasing resistors should not be larger than 10 kΩ because minor differences in input bias currents to the individual video amplifiers may cause offsets in gain.

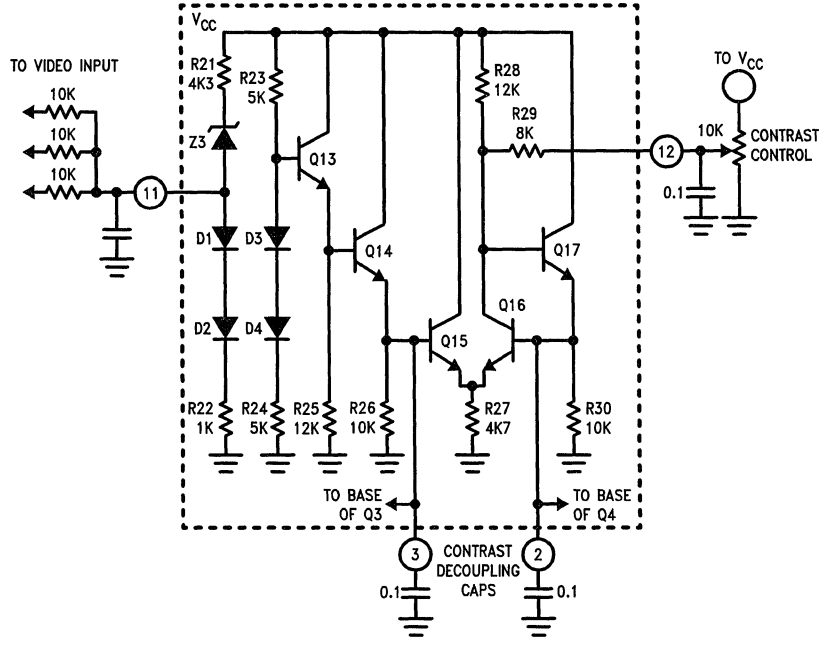

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FIGURE 7. LM1203 Video Input Voltage Reference and Contrast Control Circuits

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, 24, diodes D3, 4 and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, 16 and feedback transistor Q17 along with resistors R27, 28 establish a diferential base voltage for Q3 and Q4 in *Figure 6*. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 12. A capacitor should be added from pin 12 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator sections of the LM1203. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, 20) and an output switch (Q21). When the clamp gate input at pin 14 is high (>1.5V) the Q21 switch is on and shunts the I1 850 μA current to ground. When pin 14 is low (<1.3V) the Q21 switch is off and the I1 850 μA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 850 μA current source for the clamp comparator(s). The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitors at pins 5, 8, or 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNPs will operate with base voltages at or near ground and will usually have a greater reverse emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors a resistor (R34) with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, 25 to approximately 350 mV. The clamp comparator common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

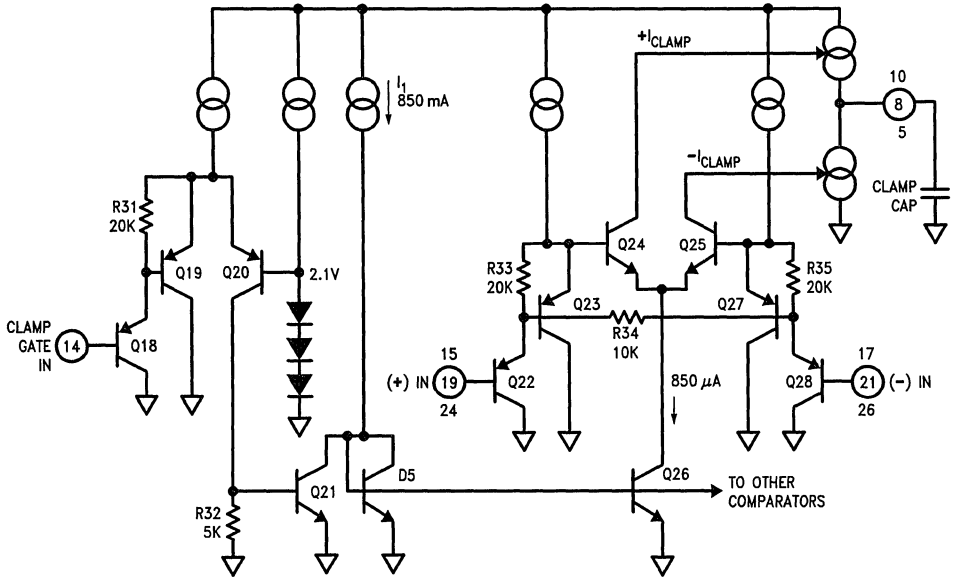

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FIGURE 8. Simplified Schematic of LM1203 Clamp Gate and Clamp Comparator Circuits

Additional Applications of the LM1203

Figure 9 shows how the LM1203 can be set up as a video buffer which could be used in low cost video switcher applications. Pin 14 is tied high to turn off the clamp comparators. The comparator input pins should be grounded as shown. Sync tip (black level if sync is not included) clamping is provided by diodes at the amplifier inputs. Note that the clamp cap pins are tied to the Pin 11 2.4V reference. This was done, along with the choice of 200Ω for the drive pin resistor, to establish an optimum DC output voltage. The contrast control (Pin 12) will provide the necessary gain or attenuation required for channel balancing. Changing the contrast control setting will cause minor DC shifts at the amplifier output which will not be objectionable as the output is AC coupled to the load. The dual NPN/PNP emitter follower will provide a low impedance output drive to the AC coupled 75Ω output impedance setting resistor. The dual 500 μF capacitors will set the low frequency response to approximately 4 Hz.

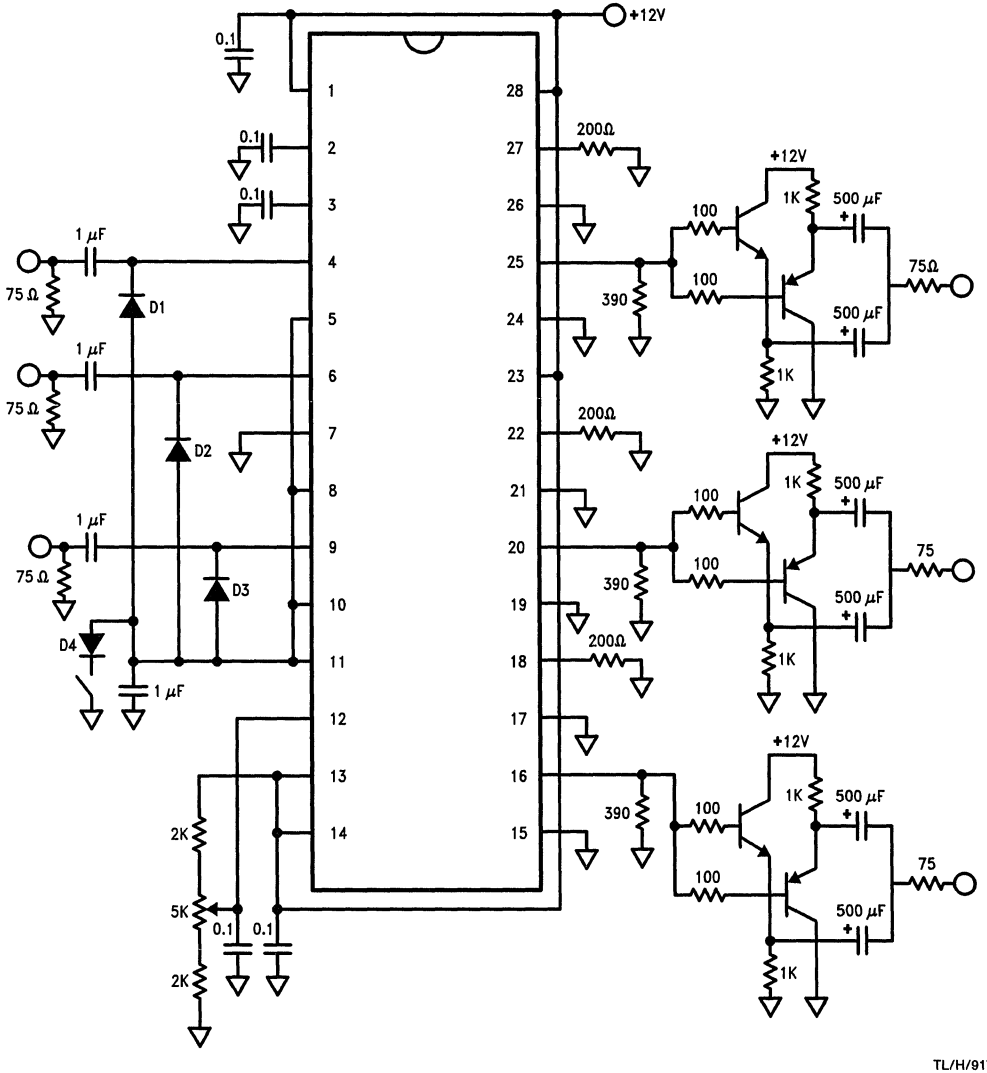

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FIGURE 9. RGB Video Buffer with Diode Sync Tip Clamps and 75Ω Cable Driver

Additional Applications of the LM1203 (Continued)

When diode D4 at Pin 11 is switched to ground the input video signals will be DC shifted down and clamped at a voltage near ground (approximately 250 mV). This will disable the video amplifiers and force the output DC level low. The DC outputs from other similarly configured LM1203s could overide this lower DC level and provide the output signals to the 75Ω cable drivers. In this case any additional LM1203s would share the same 390Ω output resistor. The maximum DC plus peak white output voltage should not be allowed to exceed 7V because the "off" amplifier output stage could suffer internal zener damage. See *Figure 3* and text for a description of the internal configuration of the video amplifier.

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0 and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.

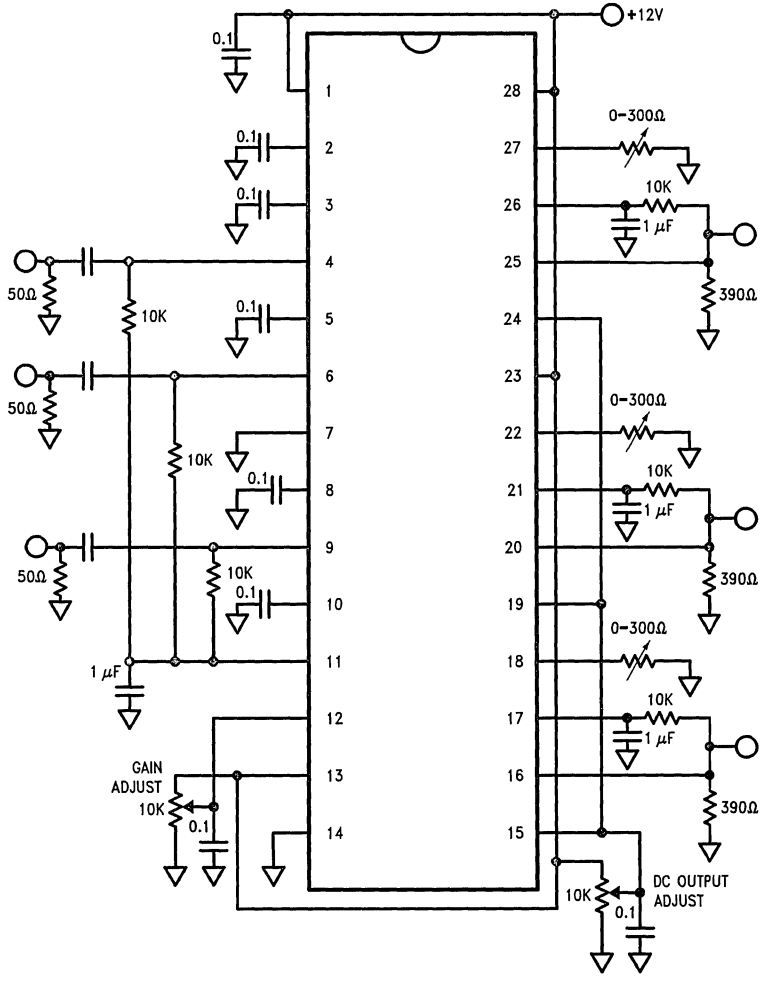

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FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Applications)

National Semiconductor Corporation

LM1391 Phase-Locked Loop

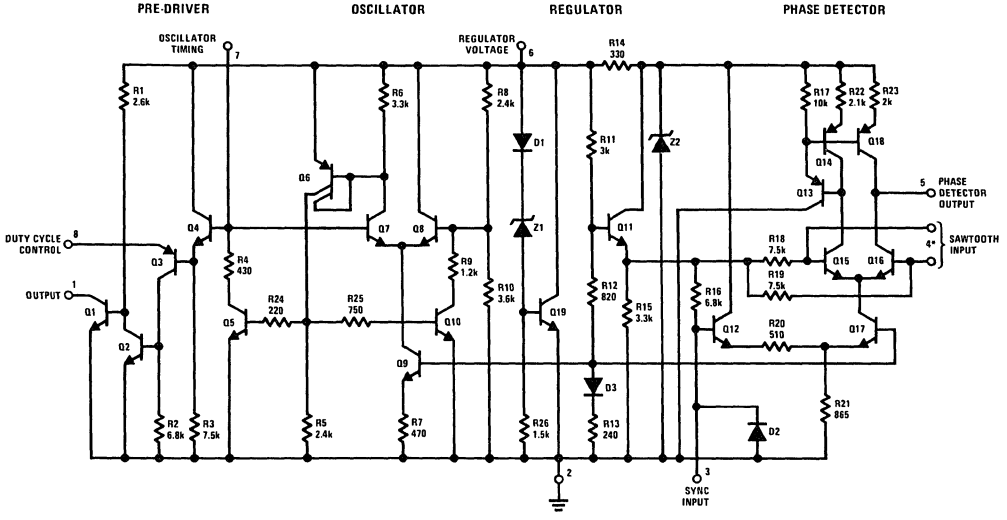
General Description

The LM1391 integrated circuit has been designed primarily for use in the horizontal section of TV receivers, but may find use in other low frequency signal processing applications. It includes a stable VCO, linear pulse phase detector, and variable duty cycle output driver.

Features

- Internal active regulator for improved supply rejection
- Uncommitted collector of output transistor
- Output transistor with low saturation and high voltage swing
- APC of the oscillator with a synchronizing signal
- DC controlled output duty cycle
- ±300 Hz typical pull-in
- Linear balanced phase detector
- Low thermal frequency drift
- Small static phase error
- Adjustable DC loop gain

Schematic Diagram



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(*) Pin 4 Base of Q16 (LM1391) for use with (+) flyback pulse

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Current	40 mA_{DC}
Output Voltage	40 V_{DC}
Output Current	30 mA_{DC}
Sync Input Voltage (Pin 3)	5.0 Vp-p
Flyback Input Voltage (Pin 4)	5.0 Vp-p
Power Dissipation (Package Limitation) Plastic Package (Note 1)	1000 mW
Operating Temperature Range (Ambient)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

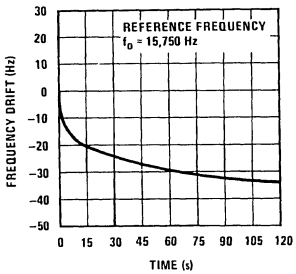
Electrical Characteristics T_A = 25°C (see test circuit, all switches in position 1)

Parameter	Conditions	Min	Typ	Max	Units
Regulated Voltage (Pin 6)	I_6 = 22 mA_{DC}	8.0	8.6	9.2	V_{DC}
Supply Current (Pin 6)			20		mA_{DC}
Collector-Emitter Saturation Voltage of Output Transistor (Pin 1)	I_{C1} = 20 mA		0.30	0.40	V_{DC}
Pin 4 Voltage			2.0		V_{DC}
Oscillator Pull-in Range	Adjust R_H		±300		Hz
Oscillator Hold-in Range	Adjust R_H		±900		Hz
Static Phase Error	Δf = 300 Hz		0.5		μs
Free-running Frequency Supply Dependance	S1 in position 2		±3.0		Hz/V_{DC}
Phase Detector Leakage (Pin 5)	All switches in position 2			±1.0	μA
Sync Input Voltage (Pin 3)		2.0		5.0	Vp-p
Sawtooth Input Voltage (Pin 4)		1.0		3.0	Vp-p
Maximum Oscillator Frequency			500		kHz

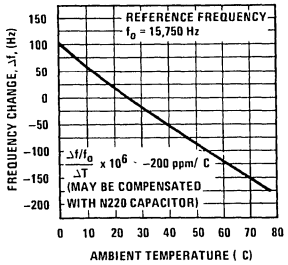
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 120°C/W junction to ambient.

Typical Performance Characteristics

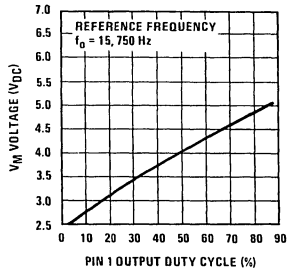
Frequency Drift vs Warm-Up Time



Frequency vs Temperature



Output Duty Cycle vs V_M Voltage



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Application Information

The following equations may be considered when using the LM1391 in a particular application.

$$R201 = R301 = \frac{V_{CC} - 8.6}{0.02}\ \Omega$$

$$f_O \cong \frac{1}{0.6\ R_O C_O}\ \text{Hz}\quad 1.5\text{k} \le R_O < 51\text{k}$$

$$R204 \cong 10\ R_O$$

$$C203 = C204 \cong \frac{1}{600\ f_O(\text{Hz})}\ \text{F}$$

DC Loop Gain $\mu\beta \cong 3.2 \times 10^{-5}\ R_O f_O$ Hz/rad

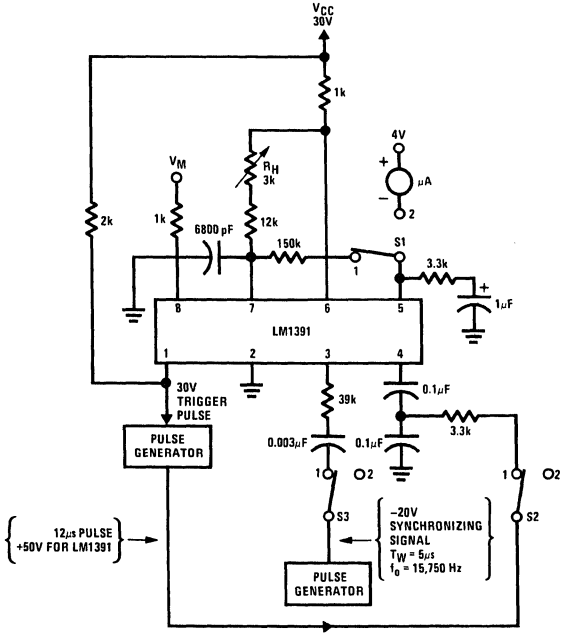
Noise Bandwidth

$$f_{nn} \cong \frac{1 + 2\pi \frac{R_X^2}{R_Y} C_C\ \mu\beta}{4 R_X C_C}\ \text{Hz}$$

Damping Factor

$$K \cong \frac{\pi}{2} \frac{R_X^2}{R_Y} C_C\ \mu\beta$$

Test Circuit



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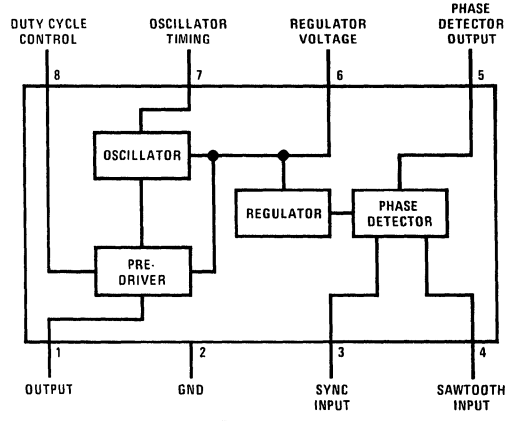
Connection Diagram

Dual-In-Line Package



TL/H/7889–2

Top View
Order Number LM1391N
See NS Package Number N08E

Typical Applications

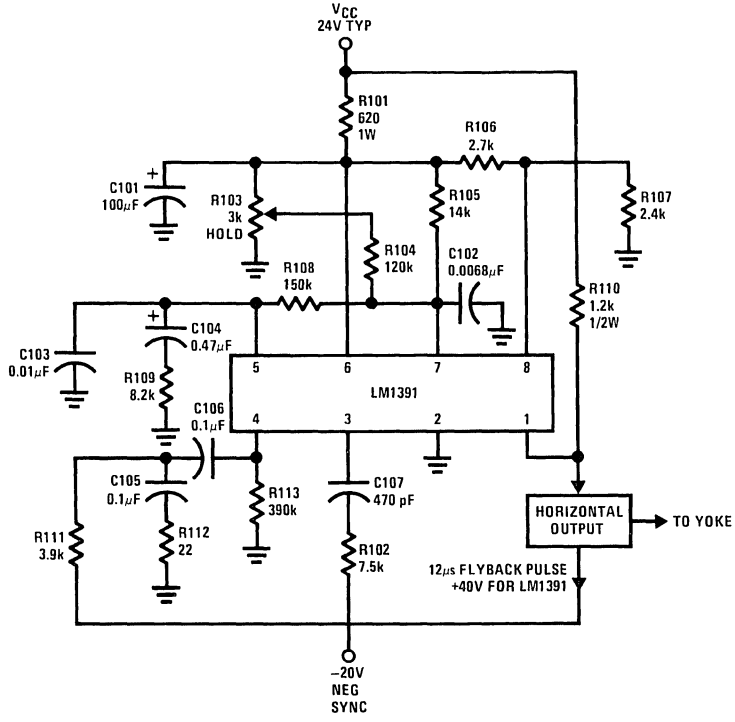


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FIGURE 1. TV Horizontal Processor

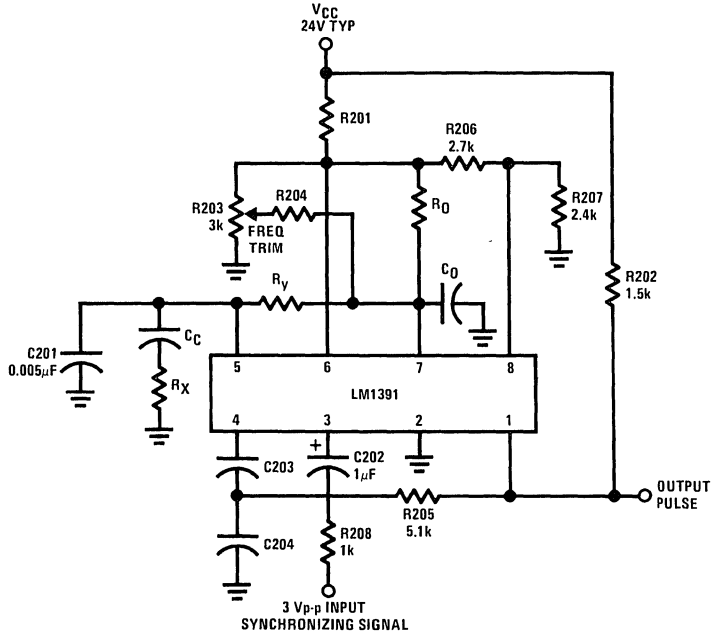

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FIGURE 2. General Purpose Phase-Lock Loop
(See Applications Information)

Typical Applications (Continued)

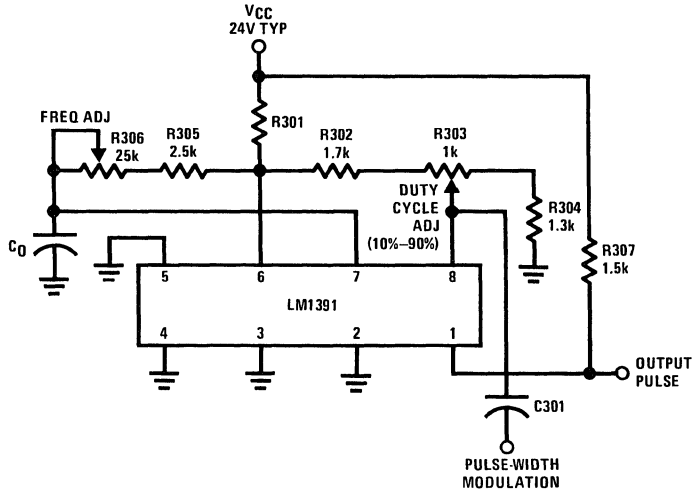

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FIGURE 3. Variable Duty Cycle Oscillator (See Applications Information)

National Semiconductor Corporation

LM1823 Video IF Amplifier/PLL Detector System

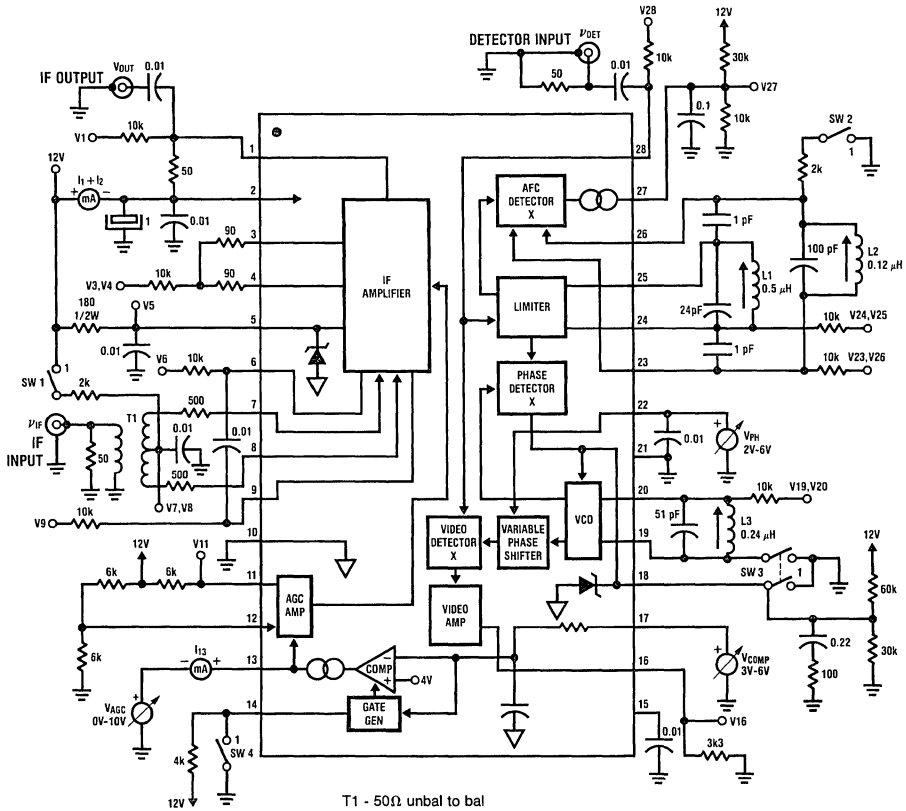
General Description

The LM1823 is a complete video IF signal processing system on a chip. It contains a 5-stage gain-controlled IF amplifier, a PLL synchronous amplitude detector, self-contained gated AGC, and a switchable AFC detector. The increased flexibility of the LM1823 makes it suitable for a wide variety of television applications where high quality video or sound carrier recovery is required. These include home receiver video IFs, cable and subscription TV decoders, and parallel sound IF/intercarrier detector systems. Typical operating frequencies are 38.9 MHz, 45.75 MHz, 58.75 MHz, and 61.25 MHz.

Features

- Low differential gain and phase
- IF and detector pin compatible with LM1822
- Common-base IF inputs for SAW filters
- True synchronous video detector using PLL
- Excellent stability at high system gains
- Noise-averaged gated AGC system
- Uncommitted AGC comparator input
- Internal AGC gate generator
- Superior small-signal detector linearity
- AFC detector with adjustable output bias
- 9 MHz video bandwidth
- Reverse tuner AGC output

Test Circuit Measure parameters at indicated test points



T1 - 50Ω unbal to bal
Mini-Circuits Lab TM01-1T

L1 - 9½T
L2 - 4½T
L3 - 6½T
#22 wire on 3/16" form with HF core, shielded

All caps in µF unless noted

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Order Number LM1823N
See NS Package N28B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage, V2	15V
IF Supply Current, I_5	60mA
AGC Gate Voltage, V14	±5V
Video Output Current, I_{16}	10 mA
PLL Filter Current, I_{18}	5 mA
Detector Input Signal, v_{DET}	1 Vrms
Power Dissipation	2W
Thermal Resistance, θ_{JA}	50° C/W
Junction Temperature	125°C
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

DC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

$T_A = 25°C$, Test Circuit, $v_{IF} = v_{DET} = 0$, $V_{PH} = 4V$, $V_{COMP} = 4V$, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
12V Supply Current, $I_1 + I_2$	$V_{AGC} = 6.7V$. $V_{COMP} = 6V$	35	60	80	mA
IF Regulator Voltage, V5	$V_{AGC} = 6.7V$, SW4 Position 1	5.8	6.4	7.0	V
IF Input Voltage, V7, V8	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	3.2	3.7	4.1	V
IF Decouple Offset, V6–V9	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1		0	±30	mV
IF Peaker Voltage (Max Gain), V3, V4	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	2.3	3.0	3.6	V
IF Output Current, I1	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1, Measure V1, $I_1 = (12 - V1)/50$	3.1	5.5	7.8	mA
IF Peaker Voltage (Min Gain), V3, V4	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1	5.5	6.2		V
Detector Input Voltage, V28	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
Limiter Tank Voltage, V24, V25	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	6.4	7.0	7.6	V
AFC Tank Voltage, V23, V26	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
VCO Tank Voltage, V19, V20	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.7	5.2	5.7	V
AGC Sync Threshold, V17	SW 1, 2 Position 1, Adjust V_{COMP} for $I_{13} = 0$	3.8	4.0	4.2	V
AGC Filter Leakage Current, I_{13}	SW 1, 2, 4 Position 1		0	±5	μA
AGC Filter Charge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 3.5V$	1.6	2.2	2.8	mA
AGC Filter Discharge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 4.5V$	−0.45	−0.70	−0.90	mA
RF AGC Leakage current, I_{11}	$V_{AGC} = 2V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$		0	20	μA
RF AGC Output Current, I_{11}	$V_{AGC} = 10V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$	1.5	1.8		mA

Detector AC Set-Up Procedure SW 1, 4 position 1, $V_{AGC}=0V$

1. Apply $v_{DET}=10$ mVrms, 45.75 MHz CW at the detector input. Tune L1 for maximum AC signal at pin 25, measured with a 10x FET probe or through a 1 pF capacitor to prevent loading of the limiter tank.
2. Increase v_{DET} to 60 mVrms. Adjust L3 until the PLL locks, as indicated by a DC voltage at the video output pin 16.
3. With the detector locked, adjust L3 for 4.0V at pin 18.
4. Adjust V_{PH} for maximum detector efficiency by monitoring pin 16 for a minimum DC voltage.
5. Adjust L2 for 3.0V at pin 27 (on sensitive slope of AFC curve).

AC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

T_A = 25°C, Test Circuit, detector set-up as above, f = 45.75 MHz, V_{AGC} = 6.7V, V_{COMP} = 4V, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
IF Amplifier Gain, v_{OUT}/v_{IF} (Note 1)	$V_{AGC}=2V$, SW 2, 3, 4 Position 1, $v_{IF}=500\ \mu Vrms$	25	35		dB
V_{AGC} for 15 dB Gain Reduction	SW 2, 3, 4 Position 1, $v_{IF}=2.8$ mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	4.2	4.6	5.0	V
V_{AGC} for 45 dB Gain Reduction	SW 2, 3, 4 Position 1, $v_{IF}=89$ mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	5.1	5.5	6.1	V
Zero Carrier Level, V16	SW 1, 2, 4 Position 1, $v_{DET}=0$	6.6	7.4	8.4	V
Detected Output Level, ΔV16	SW 1, 2, 4 Position 1, $v_{DET}=60$ m/Vrms, Measure Change in V16 from Zero Carrier Test	2	3	4.3	V
Overload Output Voltage, V16	SW 1, 2, 4 Position 1, $v_{DET}=600$ mVrms		2	3	V
AFC Output Voltage (OFF), V27	SW 1, 2, 4 Position 1, $v_{DET}=0$	2.8	3.0	3.2	V
AFC Minimum Output Voltage, V27	SW 1, 4 Position 1, $v_{DET}=60$ mVrms, 46.75 MHz		0.5	1.0	V
AFC Maximum Output Voltage, V27	SW 1, 4 Position 1, $v_{DET}=60$ mVrms, 44.75 MHz	9	10		V
PLL Pull-In Range, Δf	SW 1, 4 Position 1, $v_{DET}=60$ mVrms, Vary Frequency and Measure the Difference between Lock Points	2	3		MHz

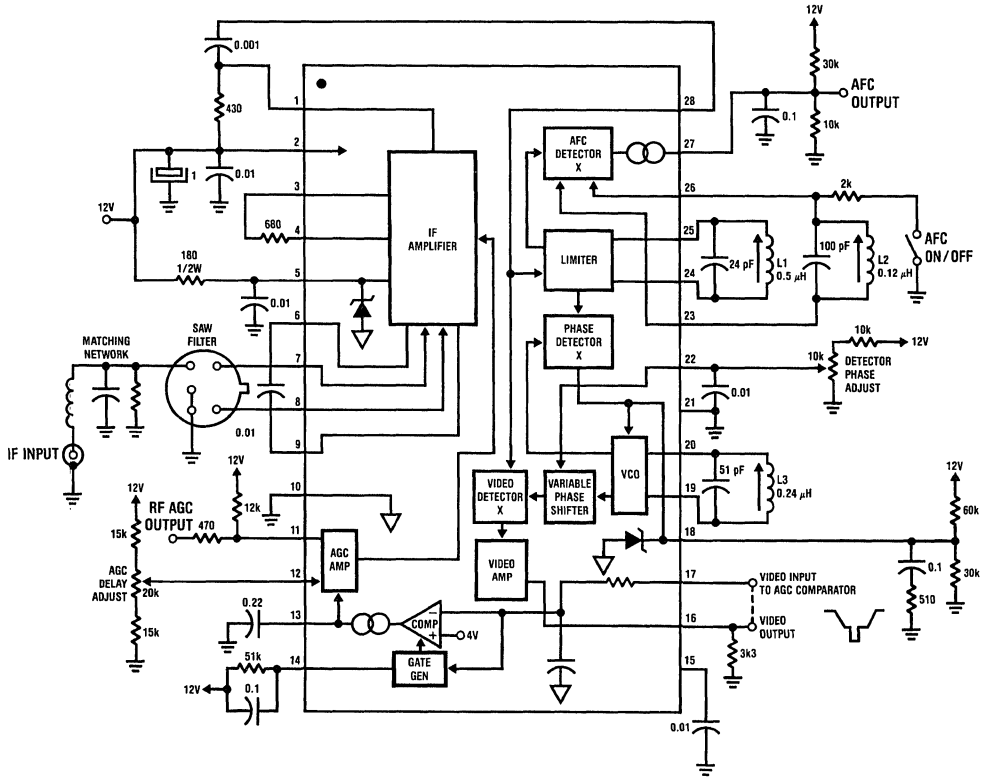
Note 1: The IF amplifier gain is specified with the IF output connected to a 50Ω measurement system which results in a 25Ω loaded impedance. The gain in an actual application will typically be 26 dB higher.

Design Parameters NOT TESTED OR GUARANTEED Typical Application Circuit

Parameter	Typ	Units
Maximum System Operating Frequency	70	MHz
IF Input Impedance (Differential Pin 7–8), 45 MHz	60	Ω
IF Output Impedance, 45 MHz	10	kΩ
IF Gain Control Range	55	dB
Detector Input Impedance, 45 MHz	2	kΩ
Detector Output Bandwidth, −3 dB	9	MHz
Detector Differential Gain (Note 2)	3	%
Detector Differential Phase (Note 2)	1	deg
Detector Output Harmonic Levels below 3 Vp-p Video	−40	dB
VCO Temperature Coefficient	−150	ppm/°C

Note: 2: Differential gain and phase measured with the limiter tank adjusted for minimum differential phase.

Typical Application 45.75 MHz (see Application Notes)



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SAW Filter - MuRata SAF45MC/MA

L1 - 9½T } #22 wire
L2 - 4½T } on 3.16" form with
L3 - 6½T } HF core, shielded

All caps in µF unless noted

Application Notes Refer to Typical Application Circuit

COMMENTS ON RF Coupling

The LM1823 is a high gain RF system which is critically dependent on the ground plane and positioning of the external components. For this reason, it is suggested that the printed circuit layout shown in *Figure 3* be strictly adhered to.

The most sensitive points in the system to unwanted RF coupling are the IF input pins 6–9. There are two different signals which can cause different problems when coupling into the IF inputs. If the IF output is coupling to the input, it can cause bandpass tilting, peaking, and in extreme cases, oscillation. The other signal which can couple to the IF inputs is the PLL detector VCO. This VCO coupling can cause AFC skewing, non-symmetrical detector pull-in, and failure of the detector to acquire lock at weak signal levels. These input coupling problems will be most acute at maximum gain and will decrease as the IF is gain reduced by AGC action.

The differential IF inputs offer a large amount of inherent rejection to unwanted RF coupling. Therefore, A FULLY BALANCED INPUT SOURCE IS MANDATORY. The input leads must be routed together and socketless operation is recommended above 50 MHz. However, residual coupling may still dictate the maximum IF amplifier gain which can be taken (see Pin Descriptions).

PIN DESCRIPTIONS

Pin 1-IF Amplifier Output: Pin 1 is connected to an open-collector NPN device. The load on pin 1 must be returned to the 12V supply as close as possible to pin 2. The IF output load may be either resistive as shown in the Typical Application, or an LC tank. The tank need only be used if a tunable bandpass characteristic is desired, or in conjunction with a sound trap.

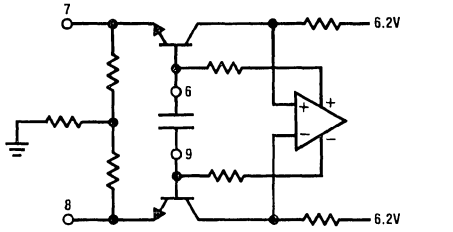
Pin 2–12V Supply: The LM1823 requires a nominal 12V supply but can accept a ±10% variation. Pin 2 must be RF decoupled to a good ground as close as possible to the IC.

Pins 3, 4-IF Gain Adjustment: Pins 3 and 4 are connected to the two emitters of the 4th IF differential amplifier such that the gain of the stage is set by the impedance between the pins. There is an internal 1360Ω resistor to set the minimum gain when the pins are left open. Adding an external resistor increases the gain by the ratio of the parallel impedance to the original 1360Ω. The pin 3 to 4 external resistor primarily affects the maximum IF gain; the relative gain increase goes away over the first 20 dB of AGC.

Pin 5-IF Supply: The IF supply employs an internal 6.4V shunt regulator which is fed by an external dropping resistor from pin 2 to pin 5. RF decoupling from pin 5 to the pin 10 ground plane is critical.

Pins 6–9-IF Input and Decouple Pins: The LM1823 uses a common-base differential input stage as shown in *Figure 1*. Pins 7 and 8 connect directly to the emitters of the input devices, while pins 6 and 9 decouple the DC feedback loop at the bases.

The gain of a common-base amplifier depends inversely on the source impedance. The LM1823 is designed to operate from differential impedances in the 500Ω to 2000Ω range, which is typical for surface acoustic wave (SAW) filters. Alternatively, the IF may be used with a transformer input configuration similar to that shown in the Test Circuit, as long as the required source impedance is maintained. In all cases a balanced source must be used.



TL/H/5222–3

FIGURE 1. IF Input Stage

Both the input network to pins 7 and 8 and decoupling capacitor between pin 6 and pin 9 must be as close to the device as is physically possible to minimize RF coupling.

Pin 10-IF Ground: Pin 10 grounds the IF and AGC circuits in the LM1823. It is separate from the detector and chip substrate grounds to prevent internal coupling.

Pin 11-RF AGC Output: Pin 11 is connected to an open-collector NPN device. It begins to conduct current when the voltage on the AGC filter capacitor at pin 13 exceeds the voltage set at the takeover pin 12 by approximately 0.6V. When connected to a resistor to 12V, this produces a falling voltage at pin 11 suitable for reverse tuner AGC inputs.

Pin 12-RF AGC Takeover Adjust: The voltage preset at pin 12 determines when the IF stops gain reducing and the tuner begins gain reducing as the pin 13 AGC filter capacitor voltage increases with signal level. A higher voltage at pin 12 delays the RF AGC takeover until more IF gain reduction has been taken (higher signal levels), while a lower voltage limits the IF gain reduction before RF takeover.

When the LM1823 is being used without a tuner, pin 12 may be connected to supply.

Pin 13-AGC Filter: Pin 13 is a push-pull current source output from the AGC comparator. The comparator compares the negative sync tips of noise-averaged pin 17 video with an internal 4V reference. Increases in signal produce a current out of pin 13 which charges the filter capacitor, while decreases discharge the capacitor. The resulting change in voltage at pin 13 controls the IF and tuner gains to maintain the pin 17 sync tip level at 4V. An optional capacitor between pin 13 and the takeover pin 12 couples the ripple produced by a rapidly varying signal into the takeover pin to enhance the AGC loop response.

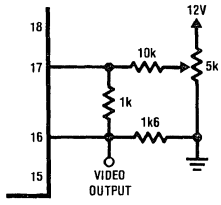
Pin 14-AGC Gate Generator Time Constant: The AGC comparator is gated on during sync time by a pulse from an internal gate generator. The gate pulse which activates the comparator is derived from the sync pulse in the same video which feeds the comparator input (see pin 17 description). An RC time constant on pin 14 determines the slice level on the leading edge of the sync pulse at which the comparator is gated on. This level is approximately $V_{SLICE} = 1/(2RC)$ in millivolts above the sync tip, and should be set at ≤25% of the sync amplitude. Note that V_{SLICE} only determines when the AGC comparator turns on, and is unrelated to the comparator reference.

In the Typical Application, $V_{SLICE} = 100$ mV, or 10% of a 1V sync pulse. Increasing V_{SLICE} improves the AGC recovery from step changes in signal level but increases the risk of video interaction. When modifying the time constant, change the capacitor value only.

Application Notes (Continued) Refer to Typical Application Circuit

Pin 15-Supply Decouple: Pin 15 is an additional connection to the 12V supply to allow RF decoupling on the detector side of the chip.

Pin 16-Video Output: Pin 16 is a Darlington NPN emitter-follower output supplying negative sync video. With no detector input signal the pin 16 voltage sits at the zero carrier level, representing peak white. As the input signal level increases, the pin 16 voltage decreases towards black. The sync pulses are normally the most negative portion of the recovered video.



TL/H/5222–4

FIGURE 2. Adjustable Recovered Video Level

Pin 17-AGC Comparator Input: External negative sync video is fed to the AGC comparator and gate generator via pin 17. An internal low pass filter removes high frequency noise and transients. The peak-to-peak video level with the AGC loop active is determined by the difference between the zero carrier level at pin 17 and the 4V sync tip level being held by the AGC comparator (see pin 13 description).

When the LM1823 is being used to recover normal video, pin 17 may simply be returned to pin 16. This results in a nominal 3 Vp-p video level, but which is subject to variations in the pin 16 zero carrier level. The network shown in *Figure 2* can be used to change the zero carrier at pin 17, thus providing an adjustable recovered video level. The pin 16 video level should be maintained at between 1 Vp-p minimum and 4 Vp-p maximum.

In suppressed sync systems, the recovered video at pin 16 may require processing to restore normal sync amplitude before being fed to pin 17. In this case, it is mandatory that a DC path be maintained for the zero carrier level through any external circuitry. Any DC level shift between pins 16 and 17 will have the effect of changing the video level as previously described.

Pin 18-PLL Filter: Pin 18 is connected to both the output of the phase detector and the control input of the VCO. The polarity of the VCO control characteristic is such that increasing the pin 18 voltage increases the VCO frequency. An external resistive divider at pin 18 serves two functions. The divider parallel impedance sets the gain of the phase detector, while the divider ratio places the quiescent voltage at the center of the VCO control characteristic. The 20 kΩ impedance, ⅓ supply divider shown in the Typical Application has been chosen to provide optimum performance. The series capacitor and resistor to ground complete the PLL filter.

An internal zener clamp to ground at pin 18 prevents the phase detector output from pulling the VCO control input over 5.6V. For this reason, external voltages should not be forced at pin 18 to avoid damaging the clamp.

Pins 19, 20-VCO Tank: A parallel LC tank between pins 19 and 20 sets the VCO center frequency. The tank Q is RpL/Xc, where RpL is the coil Rp loaded by an internal 1500Ω resistor. Increasing the Q (larger C) improves stability but reduces the VCO control range. The tank shown in the Typical Application will yield a loaded Q of around 15, providing stable operation with a control range in excess of 2 MHz.

Pin 21-Substrate Ground: Pin 21 grounds the chip substrate along with all of the AFC and PLL detector grounds.

Pin 22-Detector Phase Adjust: The video detector requires a reference signal in phase with the input signal carrier for maximum detection efficiency. However, the action of the PLL inherently sets the VCO phase in quadrature (at 90 degrees) with the limiter output. Therefore a variable phase shift network, controlled by pin 22, is used internally between the VCO and video detector to insure proper phasing. Pin 22 requires an adjustment voltage centered at ⅓ supply with ±2V of control range.

The pin 22 adjustment procedure described in the Detector AC Set-Up Procedure is an open loop approach where the voltage is adjusted for maximum detected output with a fixed detector input signal. In the Typical Application, with the detector input being fed from the IF amplifier and the AGC loop active, the pin 22 adjustment is made by maximizing the AGC filter voltage at pin 13. In all cases the detector phase adjustment must be performed after the limiter is tuned.

Pins 23, 26-AFC Tank: A parallel LC tank between pins 23 and 26 sets the center of the AFC characteristic. The internal resistance is typically 20 kΩ, so that Q will be dominated by the coil Rp. The L/C ratio shown in the Typical Application maximizes Q to provide a steep AFC output slope.

A quadrature input signal is required at the AFC tank to operate the AFC detector. This signal is derived by light capacitive coupling from the limiter tank. For applications at 45 MHz and above, the stray printed circuit capacitance from the adjacent limiter tank couples sufficient signal for proper operation. However, at lower IF frequencies, small (1 pF–5 pF) capacitors may be required between the adjacent pins as shown in the Test Circuit.

A second function of pins 23 and 26 allows turning the AFC detector OFF by grounding either side of the AFC tank. Up to 2 kΩ may be placed in series with the switch connection to prevent unbalancing the tank.

Pins 24, 25-Limiter Tank: A parallel LC tank between pins 24 and 25 forms the tuned load for a single stage limiting amplifier which strips amplitude information from the signals feeding the AFC and phase detectors. The amplifier has a small signal gain of approximately 50, with internal Schottky diodes across the tank to limit the output amplitude to 500 mVp-p.

The linearity of the detector video outputs depends directly on limiter tuning. Making the limiter adjustment based on maximum signal level at pins 24, 25 as outlined in the Detector AC Set-Up Procedure results in nearly optimum output linearity. However, to completely null the output differential phase the limiter should be adjusted while monitoring this parameter.

Pin 27-AFC Detector Output: Pin 27 is push-pull current source output from the AFC detector. The polarity is such that pin 27 sources current when the input signal is below the center frequency, and sinks current above the center frequency. An external resistive divider sets both the gain and quiescent output voltage of the AFC. Although the net-

Application Notes (Continued) Refer to Typical Application Circuit

work shown in the Typical Application sets up the output at ¼ supply, it could easily be changed to ½ supply by using equal-valued resistors. When setting up the AFC detector, the tank should always be tuned so the output is at the quiescent divider voltage with the desired center frequency applied.

Pin 28-Detector Input: Pin 28 is internally DC-biased and requires an AC-coupled input signal. The network between pins 1 and 28 should not allow over 1 Vrms at the input during signal transients to prevent overloading the detector. When a tank is being used for the IF output load, a capacitive divider may be used from pin 1 to pin 28 in which the series equivalent capacitance resonates with the coil.

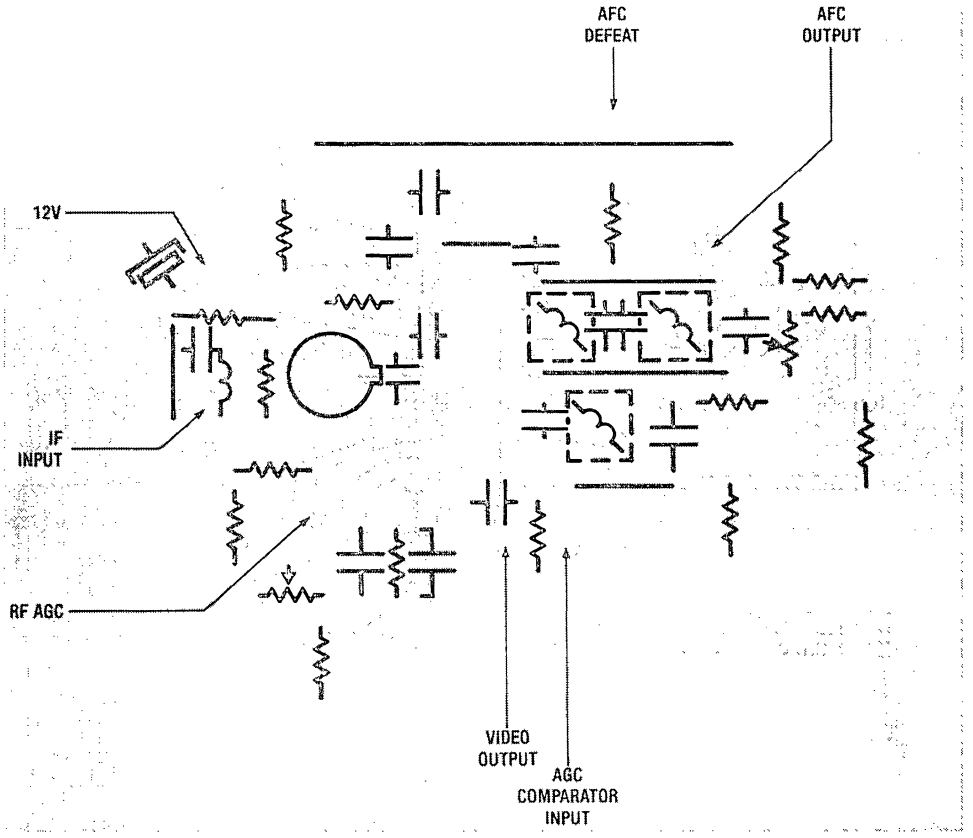


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FIGURE 3. Printed Circuit Layout (Component Side).

National Semiconductor Corporation

LM1880 No-Holds Vertical/Horizontal

General Description

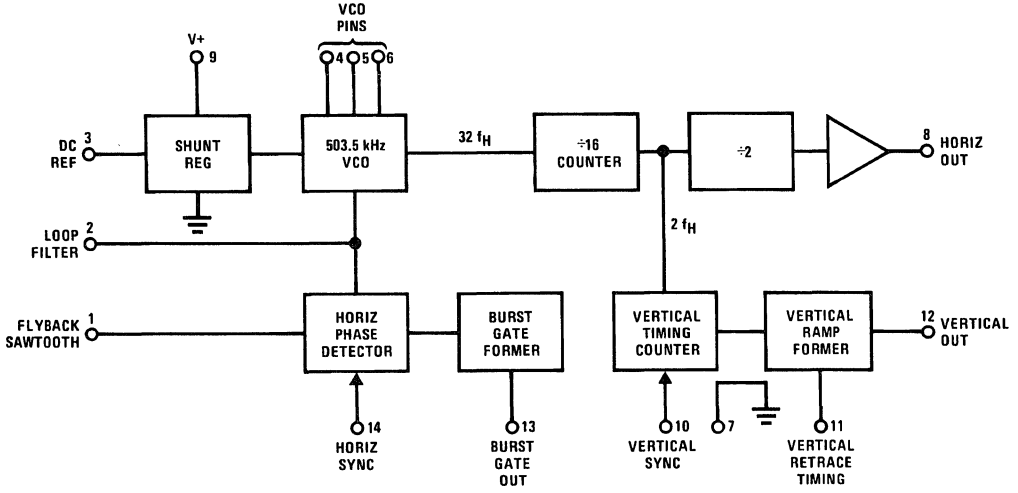
The LM1880 uses compatible Linear/I^2L technology to produce the first T.V. horizontal and vertical processing system which completely eliminates the hold controls. The heart of the system is a precision 32 times horizontal frequency VCO which is designed to use a low-cost ceramic resonator as a tuning element.

The VCO signal is divided down in the horizontal section to produce a pre-driver output which is locked to negative sync by means of an on-chip phase detector. The vertical output ramp is injection-locked by vertical sync subject to a sync window derived from the vertical countdown section. A gate pulse centered on the chroma burst is also provided.

Features

- No frequency set-up required for horizontal or vertical
- Ceramic resonator frequency reference
- Accurate horizontal pre-driver duty cycle
- Vertical sync window referenced to horizontal
- Precise interlaced vertical output
- APC loop parameters completely adjustable
- Vertical retrace time adjustable
- Chroma burst gate output
- Internal voltage regulator
- Improved vertical lock time

Block Diagram



TL/H/7915–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Current (Pin 9)	40 mA
Output Voltage (Pins 8, 12, 13)	12V
Output Current	
Pin 8	50 mA
Pin 12	15 mA
Pin 13	10 mA
Sync. Input Voltage (Pins 10, 14)	5 Vp-p
Sawtooth Input Voltage (Pin 1)	5 Vp-p
Package Dissipation, $T_A = +25°C$	1400 mW
Above $T_A = 25°C$, Derate Based on $T_{J(MAX)} = +150°C$ and $\theta_{JA} = +90°C/W$	
Storage Temperature Range	$-55°C$ to $+150°C$
Operating Temperature Range	$0°C$ to $+70°C$
Lead Temperature (Soldering, 10 sec.)	$+260°C$

Electrical Characteristics (Test Circuit, all SW normally pos. 1, $T_A = 25°C$, $V^+ = 12V$)

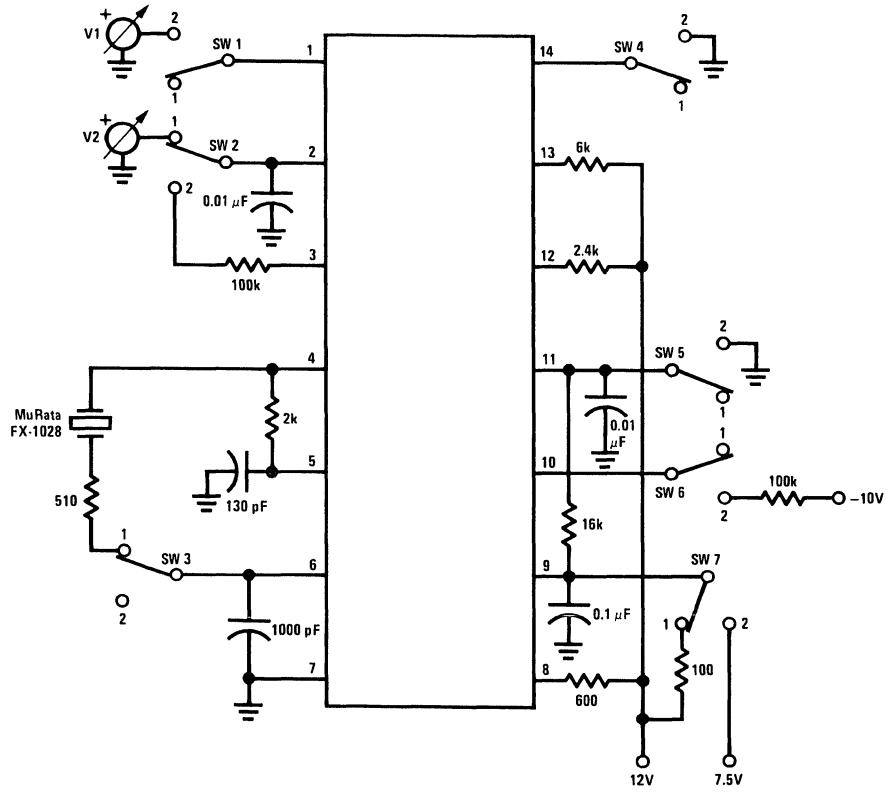
Parameter	Conditions	Min	Typ	Max	Units
Regulated Voltage (Pin 9)		8.2	8.7	9.2	V
Supply Current (Pin 9)	SW 7 Pos. 2, $V_9 = +7.5V$	12	18	24	mA
VCO Reference Voltage (Pin 3)			5.1		V
VCO Control Current (Pin 2)	V2 = 5V		0.25	1.0	μA
Horizontal Phase Detector Sink Current (Pin 2)	SW 1, SW 4 Pos. 2, V1 = 3.9V, V2 = 5V	0.3	0.5		mA
Horizontal Phase Detector Source Current (Pin 2)	SW 1, SW 4 Pos. 2, V1 = 1.9V, V2 = 5V	0.3	0.5		mA
Horizontal Output Leakage (Pin 8, OFF Condition)	Change SW 3 to Pos. 2 with Pin 8 High			150	μA
Horizontal Output Saturation Voltage (Pin 8, ON Condition)	Change SW 3 to Pos. 2 with Pin 8 Low		0.15	0.4	V
Vertical Output Saturation Voltage (Pin 12)	SW 3, SW 5 Pos. 2		0.25	0.5	V
Burst Gate Saturation Voltage (Pin 13)	SW 1, SW 4 Pos. 2, V1 = 1.9V		0.15	0.4	V
Horizontal Oscillator Free-Running Frequency (Pin 8), (Note 1)	SW 2 Pos. 2	15,550	15,750	15,950	Hz
Horizontal Oscillator Maximum Frequency (Pin 8)	V2 = 7V	16,300			Hz
Horizontal Oscillator Minimum Frequency (Pin 8)	V2 = 3V			15,150	Hz
Vertical Minimum Lock Frequency (Pin 12)	$f_H = 15,734$ Hz			55.0	Hz
Vertical Maximum Lock Frequency (Pin 12)	SW 6 Pos. 2, $f_H = 15,734$ Hz	61.7			Hz

Note 1: Assumes ceramic resonator $f_R = 503.48$ kHz.

Design Parameters (Application Circuit)

Parameter	Conditions	Min	Typ	Max	Units
Horizontal Pull-In Range			±600		Hz
Horizontal Static Phase Error (S.P.E.)	$\Delta f_H = \pm 600$ Hz		±0.5		μs
Horizontal Output Duty Cycle			50		%
Horizontal Oscillator Supply Sensitivity			−1		Hz/V
Vertical Output Retrace Time			600		μs
Burst Gate Width	Flyback Width = 12 μs		5		μs

Test Circuit

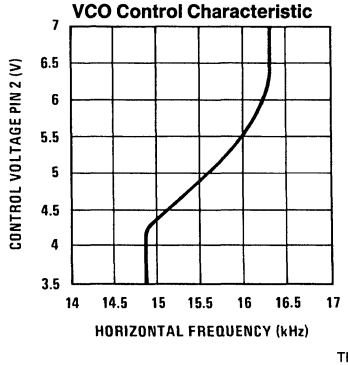


TL/H/7915–2

Order Number LM1880J
See NS Package Number J14A

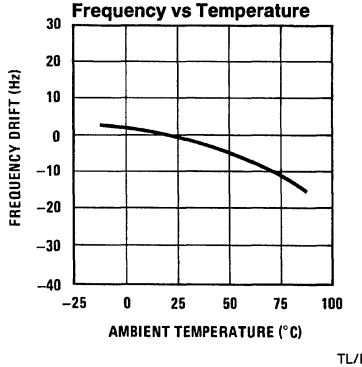
Typical Performance Characteristics

VCO Control Characteristic



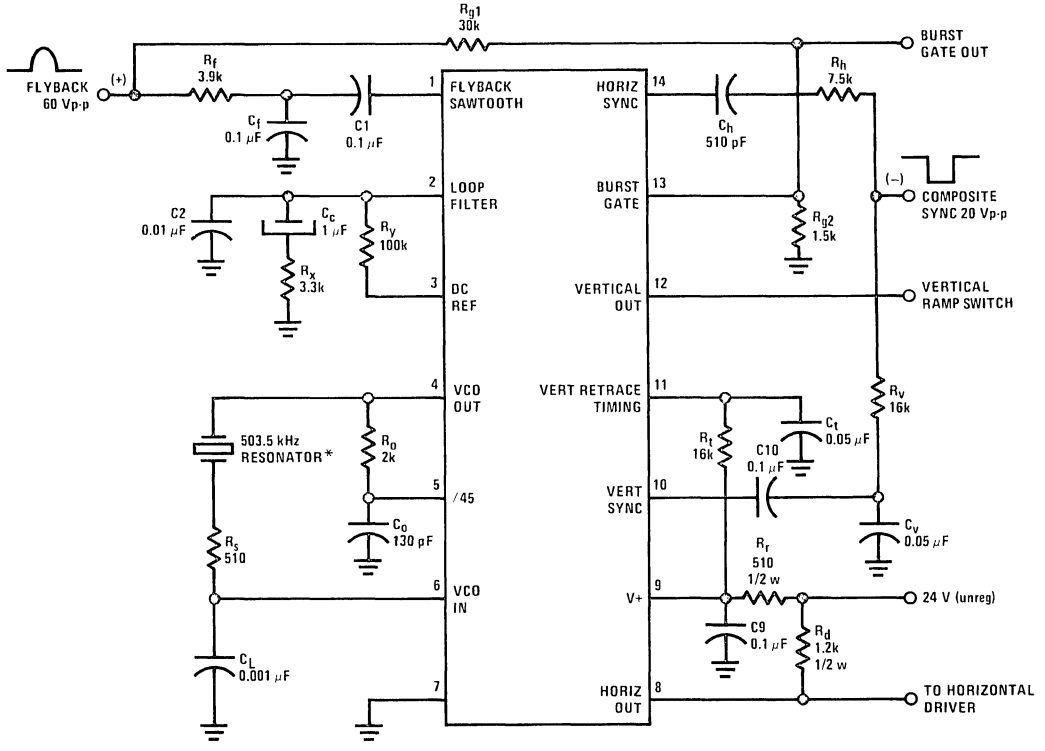
TL/H/7915–3

Horizontal Free-Running Frequency vs Temperature



TL/H/7915–4

Typical Application



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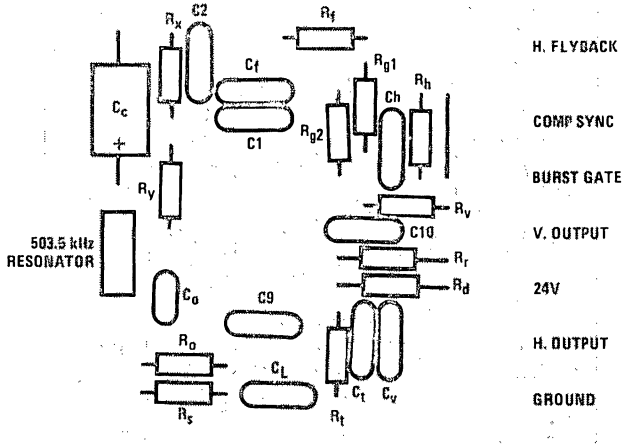
*MuRata Corporation of America, Part No. CSB503B

Printed Circuit Layout

(COMPONENT SIDE)



TL/H/7915–6

External Components (Application Circuit)

Component	Typical Value	Comments
R_{g1}	30k	Burst Gate series resistor.
R_{g2}	1.5k	Burst Gate shunt resistor, works with R_{g1} to divide flyback pulse and set Burst Gate amplitude. $V_{B.G.pk} = \frac{R_{g2}}{R_{g1} + R_{g2}} V_{FLYBACK}$
R_f	3.9k	Flyback Sawtooth integrator resistor, works with C_f to integrate flyback pulse to 1 Vp-p min sawtooth. For $C_f = 0.1\ \mu F$, $V_{SAW\ p\text{-}p} \cong \frac{85 V_{FLYBACK}}{R_f}$
C_f	0.1 μF	Flyback Sawtooth integrator capacitor.
C1	0.1 μF	Sawtooth input coupling capacitor.
R_h	7.5k	Horizontal Sync input coupling resistor. $R_h = 0.4 \times V_{SYNC\ p\text{-}p}\ k\Omega$
C_h	510 pF	Horizontal Sync input coupling capacitor, blocks vertical sync components.
R_v	16k	Vertical sync input integrator resistor.
C_v	0.05 μF	Vertical sync input integrator capacitor, works with R_v to integrate composite sync to -2 Vp-p min pulse. For N.T.S.C. sync, Vert. sync $\cong \frac{1.4 \times 10^{-4}}{R_v C_v}$ (Comp. sync) Vp-p
C10	0.1 μF	Vertical sync coupling capacitor.
R_t	16k	Vertical Retrace timing resistor.
C_t	0.05 μF	Vertical Retrace timing capacitor, works with R_t to determine ON time of vertical ramp switch at pin 12. t_V. RETRACE $\cong 0.75\ R_t C_t$ sec.
R_o	2k	Oscillator phase shift resistor.
C_o	130 pF	Works with R_o to produce 45° lag required by VCO phase shifter.
R_s	510Ω	Defines Q of ceramic resonator tuned network, which affects VCO control curve.
C_L	1000 pF	Completes VCO loop with phase lag, required to sustain oscillation and suppress resonator overtones.
R_r	510Ω	Series resistor to device supply pin 9. Must supply sufficient current to activate internal shunt regulator. $R_r = \frac{V_{(unreg)} - 9V}{0.03}\ \Omega$
C9	0.1 μF	Device supply decoupling capacitor.
R_d	1.2k	Horizontal pre-driver output resistor, supplies base current to Horizontal driver transistor when pin 8 is OFF.
C2	0.01 μF	Horizontal APC loop filter high frequency roll-off. C2 also prevents signal on loop filter from saturating phase detector output.
R_x	3.3k	R_x, R_Y and C_c form the Horizontal APC loop filter. See Applications Information to modify loop parameters.
R_y	100k	
C_c	1 μF	

Applications Information

I. VERTICAL COUNTER

The vertical counter in the LM1880 replaces the conventional vertical oscillator in a television receiver. The vertical lock-in range is governed by the width of the vertical sync window, which opens from count 510 to count 574 following a vertical reset. The vertical lock frequencies are referenced to twice horizontal frequency to insure interlaced vertical and horizontal outputs. For f_{HORIZ} = 15,734 Hz, the vertical lock frequencies are calculated as follows:

$$f_{V.HIGH} = \frac{2\,(15{,}734)}{510} = 61.7\ \text{Hz}.$$

$$f_{V.LOW} = \frac{2\,(15{,}734)}{574} = 54.8\ \text{Hz}.$$

In virtually all standard and non-standard sync signals the vertical sync is also derived from the horizontal, so that as long as the horizontal sync frequency is within the pull-in range of the LM1880 (approximately ±600 Hz), the vertical lock window will remain centered on the vertical sync. Thus, the effective vertical lock range is increased by the horizontal APC:

$$f_{V.HIGH(EFF)} = \frac{2\,(15{,}734 + 600)}{510} = 64\ \text{Hz}.$$

$$f_{V.LOW(EFF)} = \frac{2\,(15{,}734 - 600)}{574} = 52.7\ \text{Hz}.$$

The time required for the vertical to "roll-thru" and lock is a function of the difference frequency and relative phase of $f_{V.LOW}$ and the vertical sync:

$$t_{ROLL\text{-}THRU\ (AVG)} = \frac{1}{2}\,\frac{1}{60 - 55\ \text{Hz}} = 100\ \text{ms}.$$

II. HORIZONTAL APC LOOP PARAMETERS

The following information is given to provide a basis for modifying the filter to achieve the desired loop performance. Although the VCO is actually running at 503.5 kHz, for convenience all parameters are referenced to the actual horizontal output frequency at pin 8.

DC Loop Gain

The DC loop gain is the product of the phase detector conversion gain (μ) and the VCO sensitivity (β). For the typical application circuit,

$\mu = 1.6 \times 10^{-4}\ R_y\ \text{V/Rad}$

and

$\beta = 800\ \text{Hz/V}$

$\mu\beta = 0.13\ R_y\ \text{Hz/Rad}$

for $R_y = 100\ \text{k}\Omega$, $\mu\beta = 13{,}000\ \text{Hz/Rad}$

In order to determine static phase error (S.P.E.), the loop gain may be expressed in Hz/μs:

$$\mu\beta = \frac{13{,}000 \times 2\pi}{63.5\ \mu\text{s}} = 1{,}286\ \text{Hz/}\mu\text{s}$$

For comparison, this value is nearly double the loop gain of the LM1391. The increased loop gain (reduced phase error) guarantees accurate centering of the burst gate pulse on pin 13 of the LM1880.

The following equations cover AC loop parameters of interest:

Noise Bandwidth

$$f_{NN} \cong \frac{1 + 2\pi\,(R_x^2/R_y)\,C_C\,\mu\beta}{4R_xC_C}\ \text{Hz}.$$

Damping Factor

$$K \cong \frac{\pi}{2}\,\frac{R_x^2}{R_y}\,C_C\,\mu\beta$$

Pull-In Range

The pull-in and hold-in range of the LM1880 horizontal APC loop are directly determined by the VCO control range. Thus the loop would be capable of pulling the VCO further than ±600 Hz, but it has well defined frequency limits which prevent it from doing so. As a result of these built-in "stops", the loop parameters may be varied over a large range without affecting pull-in performance.

The VCO control range, and hence pull-in, can be modified to some extent by varying the Q of the ceramic resonator with resistor R_S:

Incr. R_S → Incr. Pull-in
Reduce R_S → Reduce Pull-in

However, because of the non-linearity of the resonator, R_S has a much greater effect on the negative side pull-in than the positive side.

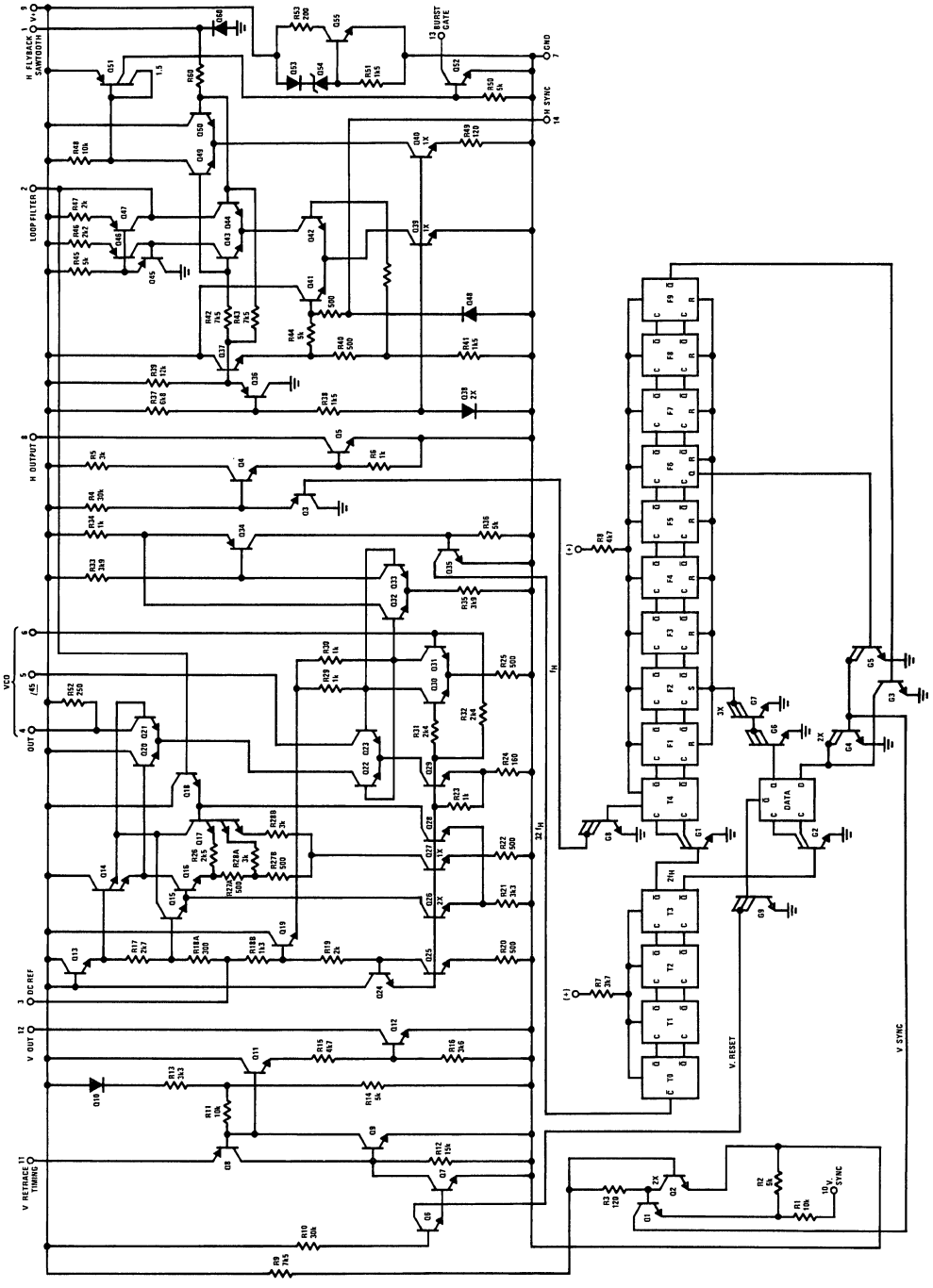
III. LAYOUT NOTES

Since the LM1880 uses a counter to derive the horizontal frequency, care must be taken to prevent extraneous signals from the horizontal driver and output stages from feeding back to the VCO where they could cause false counts and consequent severe phase jitter. The following guidelines will prevent this problem from occuring:

A. Keep the VCO feedback capacitor, C_L, as close as possible to device pins 6 and 7.

B. Limit the lead length on the horizontal output pin 8. If a long line is required to the driver base, isolate it with a small series resistor (200–300Ω) next to pin 8.

Schematic Diagram



TL/H/7915–7

Circuit Description (See Schematic Diagram)

The LM1880 uses a phase-shift type voltage-controlled oscillator (VCO). The gain for the oscillator loop is derived from differential amplifiers Q30, Q31 and Q22, Q23. The collector current in Q23 is phase-shifted 45° at pin 5 and summed with a portion of the current in Q22, controlled by differential amplifier Q20, Q21. The resulting output phase at pin 4 coupled through the ceramic resonator to pin 6 defines the oscillation frequency. Differential amplifier Q16, Q17, controlled by the pin 2 voltage, determines the current split in Q20 and Q21 and, consequently, the pin 4 phase and oscillation frequency. The multiple-emitter degeneration in Q17 compensates the resonator phase characteristic to produce a nearly linear VCO control curve.

The 503.5 kHz output of the VCO is taken from squaring amplifier Q32, Q33 through Q34 and Q35 to the $I^2L \div 16$ pre-scaler T0–T3. The $2f_H$ output is then divided again in T4 to produce the desired horizontal frequency at gate G8. The horizontal pre-driver section consists of Q3, Q4 and Q5, which produce an open-collector output square-wave at pin 8.

The $2f_H$ pre-scaler output also drives a data flip-flop which resets the vertical counter F1–F9. The data input of the reset flip-flop is controlled by the vertical sync from pin 10 subject to gates G3 and G5. After 510 $2f_H$ cycles following reset, vertical sync from Q1 and G4 is enabled by G3. A sync pulse received after this time initiates reset on the next $2f_H$ cycle. If no pulse is received after 542 cycles, G5 will initiate the reset process. A reset pulse from the counter is taken via G9 to the retrace timing section. SCR Q8, Q9 is normally ON, holding a capacitor on pin 11 near ground. During this time Q11 and Q12 are OFF, allowing the vertical ramp to form on pin 12. When the reset pulse is received, Q7 turns Q8, Q9 OFF and Q11, Q12 ON, discharging the vertical ramp for the duration of the retrace time. Retrace is completed when the pin 11 capacitor charges to the Q8 threshold, and the SCR again latches.

The remaining sections of the device are the horizontal phase detector and burst gate former. The balanced phase detector consists of comparator Q43, Q44 and current source Q39 gated by differential amplifier Q41, Q42. Negative horizontal sync pulses on pin 14 enable the comparator, and the flyback sawtooth on pin 1 switches the current from Q43 to Q44 based on the relative phase between the sync and sawtooth. Q44 takes a (−) current pulse from pin 2, while the pulse in Q43 is turned around in the current mirror Q45, Q46 and Q47 to produce a (+) current pulse at pin 2. These currents are then integrated by the external loop filter to control the VCO.

The flyback sawtooth also switches differential amplifier Q49, Q50, which activates the burst gate. During the first half of the flyback pulse Q49 will be ON, which turns Q51 and Q52 ON and clamps pin 13 near ground. The sawtooth switches Q49, Q51 and Q52 OFF at the peak of the flyback, releasing pin 13. In this manner, the second half of a flyback pulse fed to pin 13 can be used as a burst gate.

Q53, Q54 and Q55 form the active shunt regulator which holds the supply pin 9 at 8.7V typ.

National Semiconductor Corporation

PRELIMINARY

LM1881 Video Sync Separator

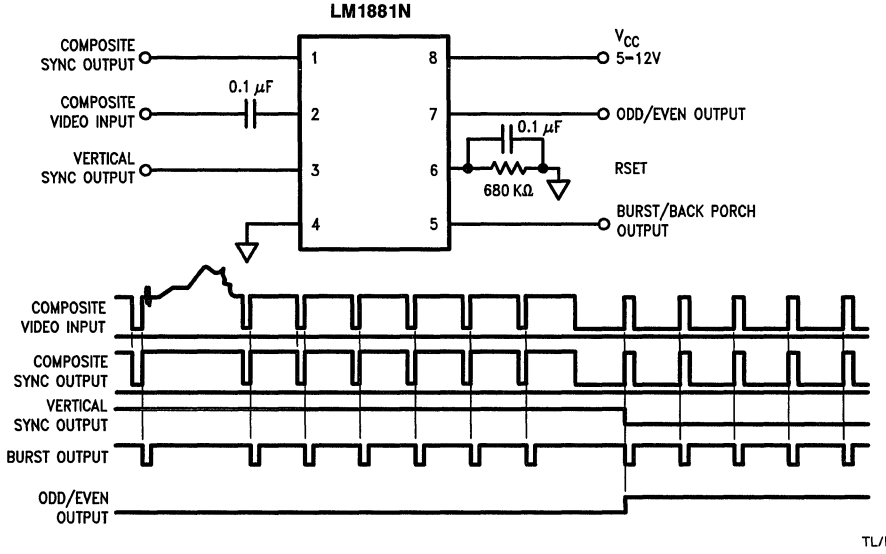
General Description

The LM1881 Video sync separator extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from a standard negative going sync NTSC video signal with amplitude from 0.5 to 2V p-p. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals by changing an external horizontal scan rate setting resistor. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the internally set delay period, such as might be the case for a non-standard video signal.

Features

- AC coupled composite input signal
- >10 kΩ input resistance
- <10 mA power supply drain current
- Composite sync and vertical outputs
- Odd/even field output
- Burst gate/back porch output
- Resistor programmable horizontal scan rate (up to 64 kHz)
- Edge triggered vertical output
- Default triggered vertical output for non-standard video signal (video games-home computers)

Connection Diagram



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Order Number LM1881M or LM1881N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	13.2V
Input Voltage	3 Vp-p
Output Sink Currents; Pins 1, 3, 5	5 mA
Output Sink Current; Pin 7	2 mA
Package Dissipation (Note 1)	1100 mW
Operating Temperature Range	0°C − 70°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility (Note 2)	2 kV
Soldering Information	
Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

V_{CC} = 5V; Rset = 680 kΩ; T_A = 25°C; Unless otherwise specified

Parameter	Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Units (Limits)
Supply Current	V_{CC} = 5V; Outputs at Logic 1	5.2	10		mAmax
	V_{CC} = 12V; Outputs at Logic 1	5.5	12		mAmax
DC Input Voltage	Pin 2	1.5	1.3 1.8		Vmin Vmax
Input Threshold Voltage	Note 5	70	55 85		mVmin mVmax
Input Discharge Current	Pin 2; V_{IN} = 2V	11	6 16		μAmin μAmax
Input Clamp Charge Current	Pin 2; V_{IN} = 1V	0.8	0.2		mAmin
R_{SET} Pin Reference Voltage	Pin 6; Note 6	1.22	1.10 1.35		Vmin Vmax
Composite Sync. & Vertical Outputs	I_{OUT} = 40 μA; Logic 1	4.5	4.0		Vmin
	I_{OUT} = 1.6 mA; Logic 1	3.6	2.4		Vmin
Burst Gate & Odd/Even Outputs	I_{OUT} = 40 μA; Logic 1	4.5	4.0		Vmin
Composite Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 1	0.2	0.8		Vmax
Vertical Sync. Output	I_{OUT} = −1.6 mA; Logic 0; Pin 3	0.2	0.8		Vmax
Burst Gate Output	I_{OUT} = −1.6 mA; Logic 0; Pin 5	0.2	0.8		Vmax
Odd/Even Output	I_{OUT} = −1.6 mA; Logic 0; Pin 7	0.2	0.8		Vmax
Vertical Sync Width		230	190 300		μsmin μsmax
Burst Gate Width	2.7 kΩ from Pin 5 to V_{CC}	4	2.5 4.7		μsmin μsmax
Vertical Default Time	Note 7	65	32 90		μsmin μsmax

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a package thermal resistance of 110° C/W, junction to ambient.

Note 2: ESD susceptibility test uses the "human body model, 100 pF discharged through a 1.5 kΩ resistor".

Note 3: These parameters are guaranteed and 100% production tested.

Note 4: Design Limits are guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

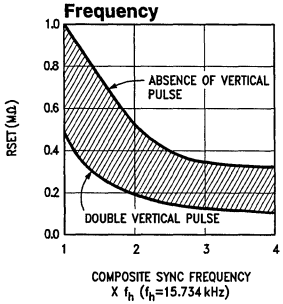
Note 5: Relative difference between the input clamp voltage and the minimum input voltage which produces a horizontal output pulse.

Note 6: Careful attention should be made to prevent parasitic capacitance coupling from any output pin (Pins 1, 3, 5, and 7) to the R_{SET} pin (Pin 6).

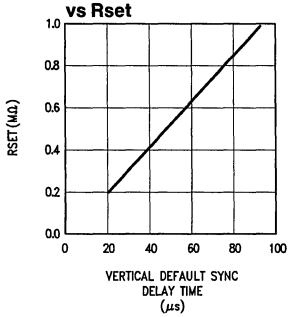
Note 7: Delay time between the start of vertical sync (at input) and the vertical output pulse.

Typical Performance Characteristics

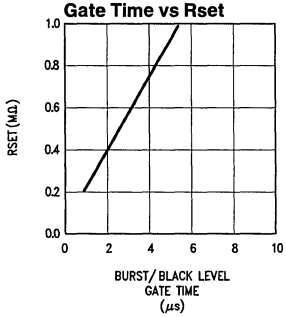
Rset Value Selection vs Composite Sync Frequency



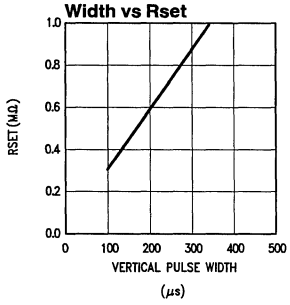
Vertical Default Sync Delay Time vs Rset



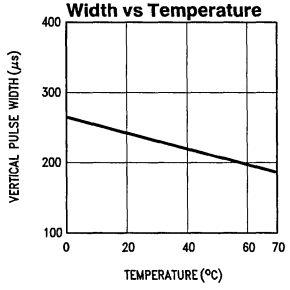
Burst/Black Level Gate Time vs Rset



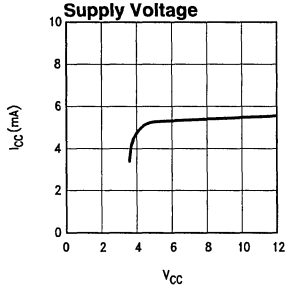
Vertical Pulse Width vs Rset



Vertical Pulse Width vs Temperature



Supply Current vs Supply Voltage



TL/H/9150–2

Application Notes

The LM1881 is designed to strip the synchronization signals from composite video sources that are in, or similar to, the N.T.S.C. format. Input signals with positive polarity video (increasing signal voltage signifies increasing scene brightness) from 0.5V (p-p) to 2V (p-p) can be accommodated. The LM1881 operates from a single supply voltage between 5V DC and 12V DC. The only required external components beside power supply and set current decoupling are the input coupling capacitor and a single resistor that sets internal current levels, allowing the LM1881 to be adjusted for source signals with line scan frequencies differing from 15.734 kHz. Four major sync signals are available from the I/C: composite sync including both horizontal and vertical scan timing information; a vertical sync pulse; a burst gate or back porch clamp pulse; and an odd/even output. The odd/even output level identifies which video field of an interlaced video source is present at the input. The outputs from the LM1881 can be used to gen-lock video camera/VTR signals with graphics sources, provide identification of video fields for memory storage, recover suppressed or contaminated sync signals, and provide timing references for the extraction of coded or uncoded data on specific video scan lines.

To better understand the LM1881 timing information and the type of signals that are used, refer to *Figure 2(a–e)* which shows a portion of the composite video signal from the end of one field through the beginning of the next field.

COMPOSITE SYNC OUTPUT

The composite sync output, *Figure 2(b)*, is simply a reproduction of the signal waveform below the composite video black level, with the video completely removed. This is obtained by clamping the video signal sync tips to 1.5V DC at Pin 2 and using a comparator threshold set just above this voltage to strip the sync signal, which is then buffered out to Pin 1. The threshold separation from the clamped sync tip is nominally 70 mV which means that for the minimum input level of 0.5V (p-p), the clipping level is close to the halfway point on the sync pulse amplitude (shown by the dashed line on *Figure 2(a)*). This threshold separation is independent of the signal amplitude, therefore, for a 2V (p-p) input the clipping level occurs at 11% of the sync pulse amplitude. The charging current for the input coupling capacitor is 0.8 mA, whereas the discharge current is only 11 μA, typically. This allows relatively small capacitor values to be used—0.1 μF is generally recommended.

Normally the signal source for the LM1881 is assumed to be clean and relatively noise-free, but some sources may have excessive video peaking, causing high frequency video and chroma components to extend below the black level reference. Some video discs keep the chroma burst pulse present throughout the vertical blanking period so that the burst actually appears on the sync tips for three line periods instead of at black level. A clean composite sync signal can be generated from these sources by filtering the input signal. When the source impedance is low, typically 75Ω, a 620Ω resistor in series with the source and a 510 pF capacitor to ground will form a low pass filter with a corner frequency of 500 kHz. This bandwidth is more than sufficient to pass the sync pulse portion of the waveform; however, any subcarrier content in the signal will be attenuated by almost 18 dB, effectively taking it below the comparator threshold. Filtering will also help if the source is contaminated with thermal noise. The output waveforms will become delayed from between 40 ns to as much as 200 ns due to this filter. This much delay will not usually be significant but it does contribute to the sync delay produced by any additional signal processing. Since the original video may also undergo processing, the need for time delay correction will depend on the total system, not just the sync stripper.

VERTICAL SYNC OUTPUT

A vertical sync output is derived by internally integrating the composite sync waveform *(Figure 3)*. Horizontal sync pulses are not able to charge the integrating capacitor sufficiently because of their short duty cycle, but when the vertical retrace interval is reached, the broad serrated pulse charges the capacitor past a fixed threshold. Once the threshold is reached, the next serration in the sync waveform triggers an R-S flipflop and starts the vertical output pulse at Pin 3. Simultaneously an internal oscillator begins clocking a counter. When a count of eight is reached the vertical output pulse is terminated and the circuit resets. Both the time required to reach the integrator threshold and the period of the oscillator are programmed by an external resistor at Pin 6. For an N.T.S.C. signal with 32 μs between serrations, a 680 kΩ resistor will ensure the vertical output pulse will start coincident with the leading edge of the first vertical serration *(Figure 2c)*. If the resistor value gets too small it becomes possible for the oscillator circuit to time out before the input vertical sync period has ended. When this is the case, the sequence will repeat and a double vertical output pulse will appear. Therefore, the resistor value for a given horizontal scan rate is chosen small enough to trigger the vertical output pulse on the first serration yet not so small as to give a double pulse, rather than attempting to choose a value that gives a specific output pulse width. If the incoming vertical sync is not serrated, the integrating capacitor is allowed to charge to a second threshold which automatically initiates the vertical output pulse sequence. In this instance, the start of the vertical pulse as well as the pulse period will be dependent on the resistor value.

ODD/EVEN FIELD PULSE

An unusual feature of LM1881 is an output level from Pin 7 that identifies the video field present at the input to the LM1881. This can be useful in frame memory storage applications or in extracting test signals that occur only in alternate fields. For a composite video signal that is interlaced, one of the two fields that make up each video frame or picture must have a half horizontal scan line period at the end of the vertical scan—i.e., at the bottom of the picture. This is called the "odd field" or "field 1". The "even field" or "field 2" has a complete horizontal scan line at the end of the field. An odd field starts on the leading edge of the first equalizing pulse, whereas the even field starts on the leading edge of the second equalizing pulse of the vertical retrace interval. *Figure 2(a)* shows the end of the even field and the start of the odd field.

To detect the odd/even fields the LM1881 again integrates the composite sync waveform *(Figure 3)*. A capacitor is charged during the period between sync pulses and discharged when the sync pulse is present. The period between normal horizontal sync pulses is enough to allow the capacitor voltage to reach a threshold level of a comparator that clears a flipflop which is also being clocked by the sync waveform. When the vertical interval is reached, the shorter integration time between equalizing pulses prevents this

Application Notes (Continued)

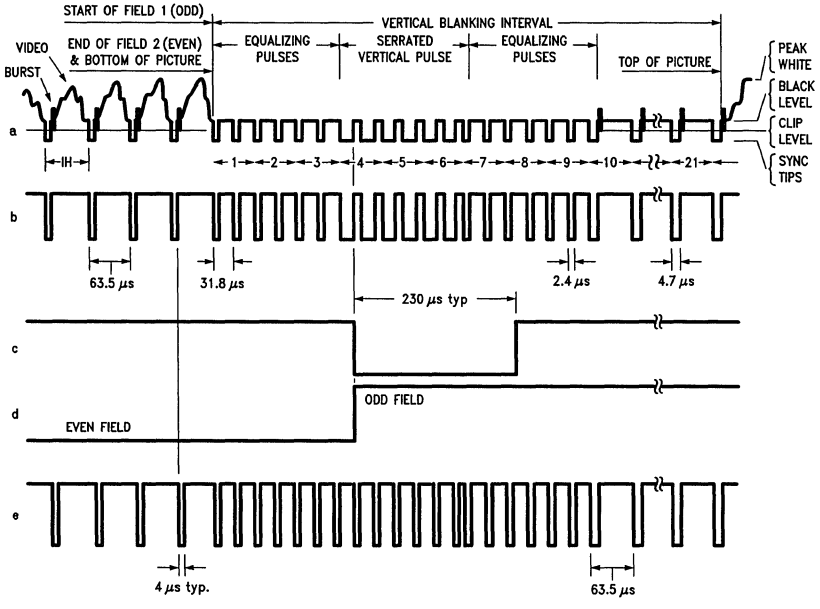


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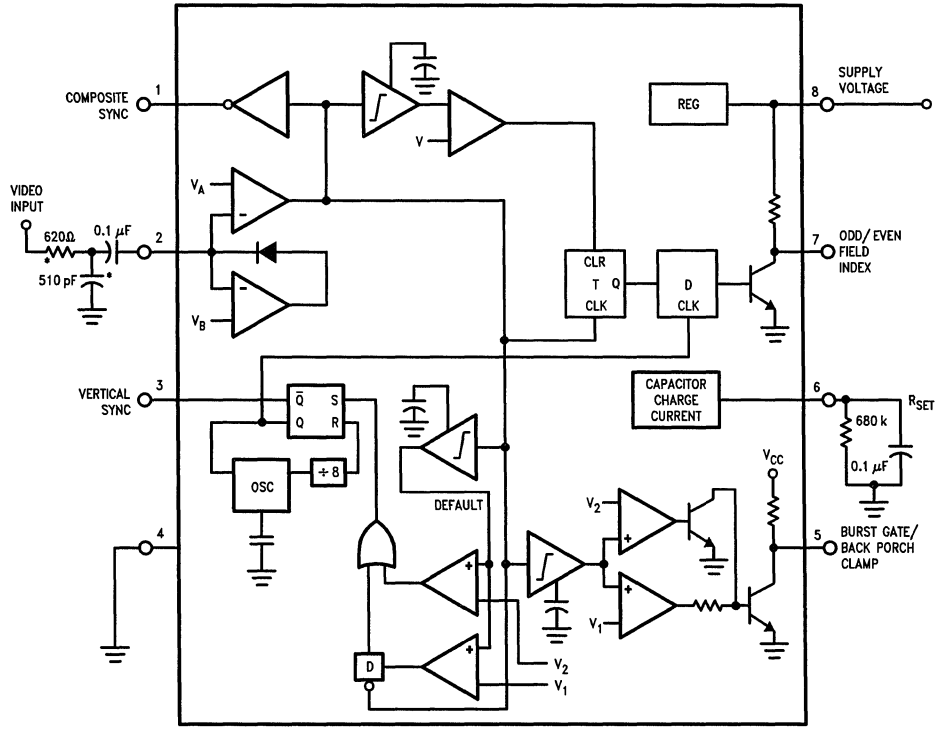
FIGURE 2. (a) Composite Video; (b) Composite Sync; (c) Vertical Output Pulse; (d) Odd/Even Field Index; (e) Burst Gate/Back Porch Clamp



*Components Optional, See Text

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FIGURE 3

Application Notes (Continued)

threshold from being reached and the Q output of the flip-flop is toggled with each equalizing pulse. Since the half line period at the end of the odd field will have the same effect as an equalizing pulse period, the Q output will have a different polarity on successive fields. Thus by comparing the Q polarity with the vertical output pulse, an odd/even field index is generated. Pin 7 remains low during the even field and high during the odd field.

BURST/BACKPORCH OUTPUT PULSE

In a composite video signal, the chroma burst is located on the backporch of the horizontal blanking period. This period, approximately 4.8 μs long, is also the black level reference for the subsequent video scan line. The LM1881 generates a pulse at Pin 5 that can be used either to retrieve the chroma burst from the composite video signal (thus providing a subcarrier synchronizing signal) or as a clamp for the DC restoration of the video waveform. This output is obtained simply by charging an internal capacitor starting on the trailing edge of the horizontal sync pulses. Simultaneously the output of Pin 5 is pulled low and held until the capacitor charge circuit times out—4 μs later. A shorter output burst gate pulse can be derived by differentiating the burst output using a series C-R network. This may be necessary in applications which require high horizontal scan rates in combination with normal (60–120 Hz) vertical scan rates.

APPLICATIONS

Apart from extracting a composite sync signal free of video information, the LM1881 outputs allow a number of interesting applications to be developed. As mentioned above, the burst gate/backporch clamp pulse allows DC restoration of the original video waveform for display or remodulation on an R.F. carrier, and retrieval of the color burst for color synchronization and decoding into R.G.B. components. For frame memory storage applications, the odd/even field level allows identification of the appropriate field ensuring the correct read or write sequence. The vertical pulse output is particularly useful since it begins at a precise time—the rising edge of the first vertical serration in the sync waveform. This means that individual lines within the vertical blanking period (or anywhere in the active scan line period) can easily be extracted by counting the required number of transitions in the composite sync waveform following the start of the vertical output pulse.

The vertical blanking interval is proving popular as a means to transmit data which will not appear on a normal T.V. receiver screen. Data can be inserted beginning with line 10 (the first horizontal scan line on which the color burst appears) through to line 21. Usually lines 10 through 13 are not used which leaves lines 14 through 21 for inserting signals, which may be different from field to field. In the U.S., line 19 is normally reserved for a vertical interval reference signal (VIRS) and line 21 is reserved for closed caption data for the hearing impaired. The remaining lines are used in a number of ways. Lines 17 and 18 are frequently used during studio processing to add and delete vertical interval test signals (VITS) while lines 14 through 18 and line 20 can be used for Videotex/Teletext data. Several institutions are proposing to transmit financial data on line 17 and cable systems use the available lines in the vertical interval to send decoding data for descrambler terminals.

Since the vertical output pulse from the LM1881 coincides with the leading edge of the first vertical serration, sixteen positive or negative transitions later will be the start of line 14 in either field. At this point simple counters can be used to select the desired line(s) for insertion or deletion of data.

VIDEO LINE SELECTOR

The circuit in *Figure 4* puts out a single video line according to the binary coded information applied to line select bits b0–b7. A line is selected by adding two to the desired line number, converting to a binary equivalent and applying the result to the line select inputs. The falling edge of the LM1881's vertical pulse is used to load the appropriate number into the counters (MM74C193N) and to set a start count latch using two NAND gates. Composite sync transitions are counted using the borrow out of the desired number of counters. The final borrow out pulse is used to turn on the analog switch (CD4066BC) during the desired line. The falling edge of this signal also resets the start count latch, thereby terminating the counting.

The circuit, as shown, will provide a single line output for each field in an interlaced video system (television) or a single line output in each frame for a non-interlaced video system (computer monitor). When a particular line in only one field of an interlaced video signal is desired, the odd/even field index output must be used instead of the vertical output pulse (invert the field index output to select the odd field). A single counter is needed for selecting lines 3 to 14; two counters are needed for selecting lines 15 to 253; and three counters will work for up to 2046 lines. An output buffer is required to drive low impedance loads.

MULTIPLE CONTIGUOUS VIDEO LINE SELECTOR WITH BLACK LEVEL RESTORATION

The circuit in *Figure 5* will select a number of adjoining lines starting with the line selected as in the previous example. Additional counters can be added as described previously for either higher starting line numbers or an increased number of contiguous output lines. The back porch pulse output of the LM1881 is used to gate the video input's black level through a low pass filter (10 kΩ, 10 μF) providing black level restoration at the video output when the output selected line(s) is not being gated through.

Typical Applications

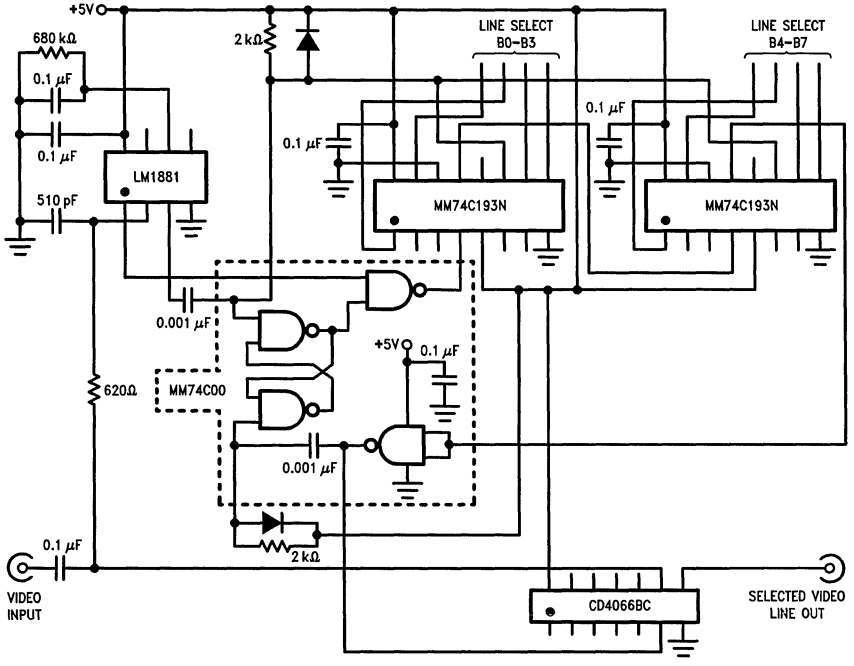

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FIGURE 4. Video Line Selector

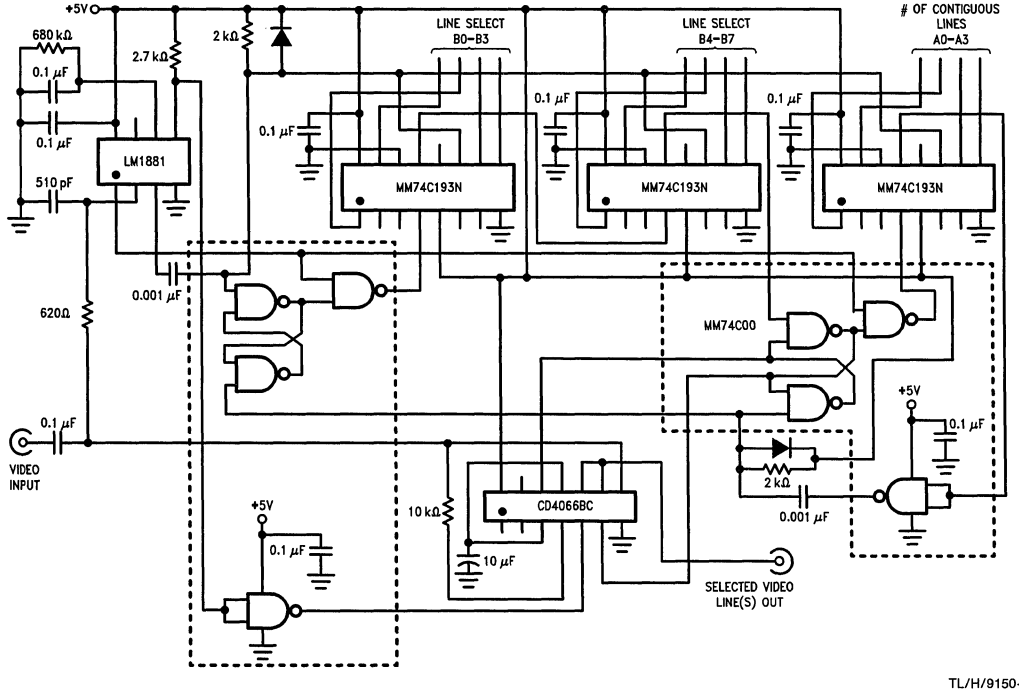

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FIGURE 5. Multiple Contiguous Video Line Selector With Black Level Restoration

National Semiconductor Corporation

LM1886 TV Video Matrix D to A

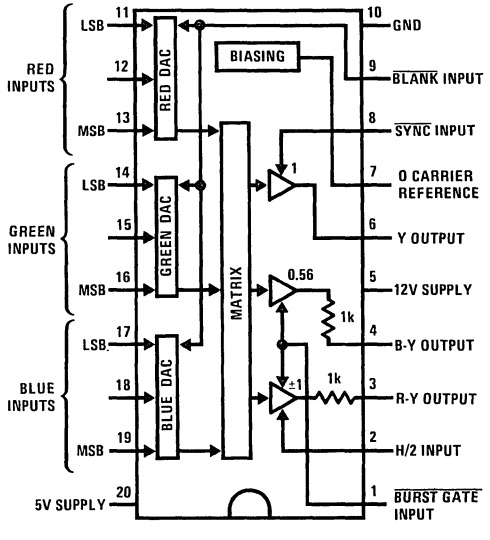
General Description

The LM1886 is a TV video matrix D to A converter which encodes luminance and color difference signals from 3-bit red, green and blue inputs. The luminance output is encoded from the NTSC equation Y = 0.3R + 0.59G + 0.11B and the R-Y and B-Y outputs are weighted to prevent overmodulation. A built-in R-Y and burst gate polarity switch allow European PAL compatible signals to be encoded. All output levels including an RF O Carrier Bias Voltage have been referenced to 5V for direct connection to the LM1889 TV video modulator. When used in combination with the LM1889 and a suitable sync generator, 3-bit, R, G and B information may be encoded to both composite video and RF channel carrier.

Features

- Complete digital to RF coding with LM1889
- 1-pin PAL/NTSC mode select
- True NTSC matrix
- 8 levels of grey scale
- Allows wide range of colorimetry
- Low power TTL inputs
- Wideband luminance output
- Weighted R-Y, B-Y outputs

Connection Diagram



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Top View

FIGURE 1

Order Number LM1886N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
Pin 5	15V
Pin 20	6V
Input Voltage (Pins 1, 8, 9, 11–19)	−0.5V, +12V
Pin 2 Voltage Relative to Pin 20	0.8V
Output Current	5 mA
Power Dissipation, T_A = 25°C (Note 1)	1900 mW
Storage Temperature Range	−55°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°

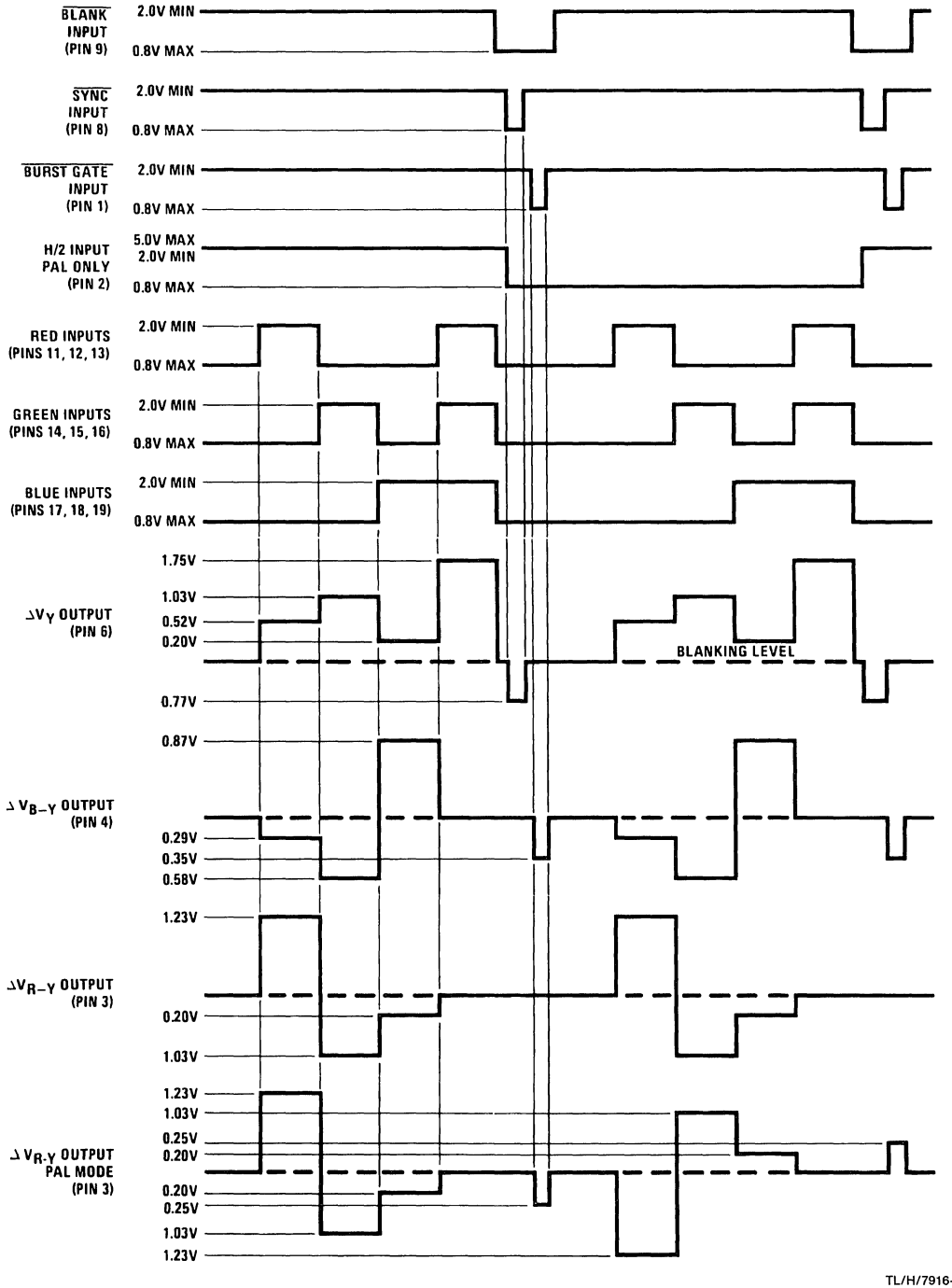
Electrical Characteristics T_A = 25°C, (*Figure 2*, Note 2)

Parameter	Conditions	Min	Typ	Max	Units
5V Supply Current (Pin 20)	$\overline{\text{BLANK}}$ = 0.8V	7	11	16	mA
12V Supply Current (Pin 5)	$\overline{\text{BLANK}}$ = 0.8V	9	13	17	mA
Logic "1" Input Current (Pins 1, 2, 8, 9, 11–19)	Input Voltage = 5.0V		0	10	μA
Logic "0" Input Current (Pins 1, 2, 8, 9, 11–19)	Input Voltage = 0.3V		−0.01	−0.18	mA
Output Offsets	R, G, B, = 0.8V				
ΔV_Y			0	±50	mV
ΔV_{R-Y}			0	±50	mV
ΔV_{B-Y}			0	±50	mV
R-Y Full Scale, $(\Delta V_{R-Y})_{FS}$	R = 2V; G, B = 0.8V	1.0	1.23	1.4	V
B-Y Full Scale, $(\Delta V_{B-Y})_{FS}$	B = 2V; R, G = 0.8V	0.7	0.87	1.0	V
Green Full Scale	G = 2V; R, B = 0.8V				
ΔV_{R-Y}		−0.85	−1.03	−1.2	V
ΔV_{B-Y}		−0.45	−0.58	−0.7	V
Y Full Scale	R, G, B = 2V				
$(\Delta V_Y)_{FS}$		1.6	1.75	1.9	V
ΔV_{R-Y}			0	±100	mV
ΔV_{B-Y}			0	±75	mV
O Carrier Reference, ΔV_O		2.0	2.2	2.5	V
Blanking Level, ΔV_Y	$\overline{\text{BLANK}}$ = 0.8V		0	±50	mV
Sync Level, ΔV_Y	$\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ = 0.8V	−0.67	−0.77	−0.87	V
NTSC Burst, ΔV_{B-Y}	$\overline{\text{BLANK}}$, $\overline{\text{BURST GATE}}$ = 0.8V	−0.26	−0.35	−0.46	V
PAL Burst	SW in PAL Position;				
ΔV_{R-Y}	$\overline{\text{BLANK}}$, $\overline{\text{BURST GATE}}$,	−0.2	−0.25	−0.32	V
ΔV_{B-Y}	H/2 = 0.8V	−0.2	−0.25	−0.32	V
PAL Inversion Ratio $(\Delta V_{R-Y})_{PAL}/(\Delta V_{R-Y})_{FS}$	R= 2V; G, B, H/2 = 0.8V SW to PAL Position	−0.9	−1.0	−1.1	
Y Linearity Error	*Figure 2b* Input Connection		±1	±6	%FS
Y Switching Times	15 kHz Square Wave Switching				
Rise Time, t_R	R, G, B in Parallel		35		ns
Fall Time, t_F			30		ns
Settling Time ±1 LSB			50		ns

Note 1: Above T_A = 25°C, derate based on $T_{J(MAX)}$ = 150°C and θ_{JA} = 65°C/W.

Note 2: Unless otherwise noted, $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$, $\overline{\text{BURST GATE}}$ = 2V and SW is in NTSC position. All outputs are referenced to the +5V supply as shown in *Figure 2a*.

Typical Input and Output Waveforms



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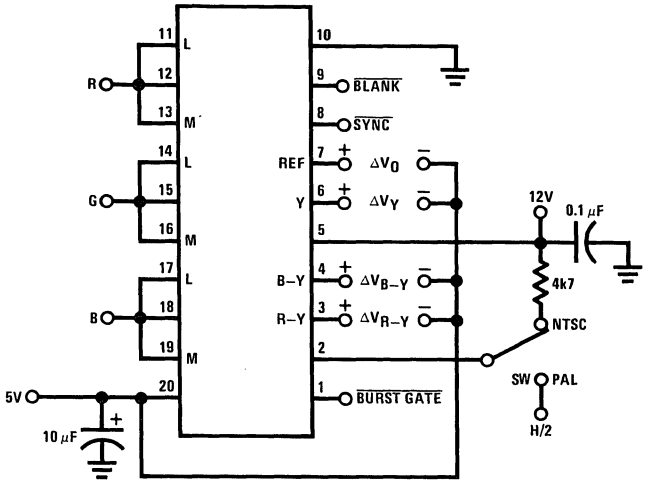
Test Circuits



TL/H/7916–2

FIGURE 2a. 6-Color Input Connection

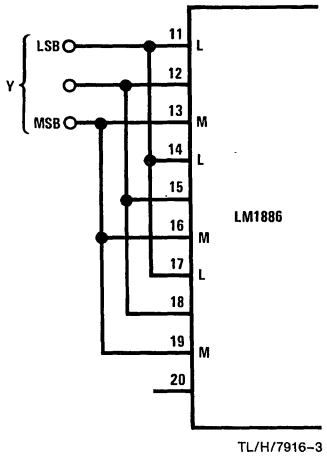


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FIGURE 2b. 8-level Grey Scale Input Connection

Application Notes (Refer to *Figure 3*)

$\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{BURST GATE}}$ may be obtained from a sync generator IC. For PAL operation, the H/2 square wave may be obtained by a ÷2 from horizontal sync.

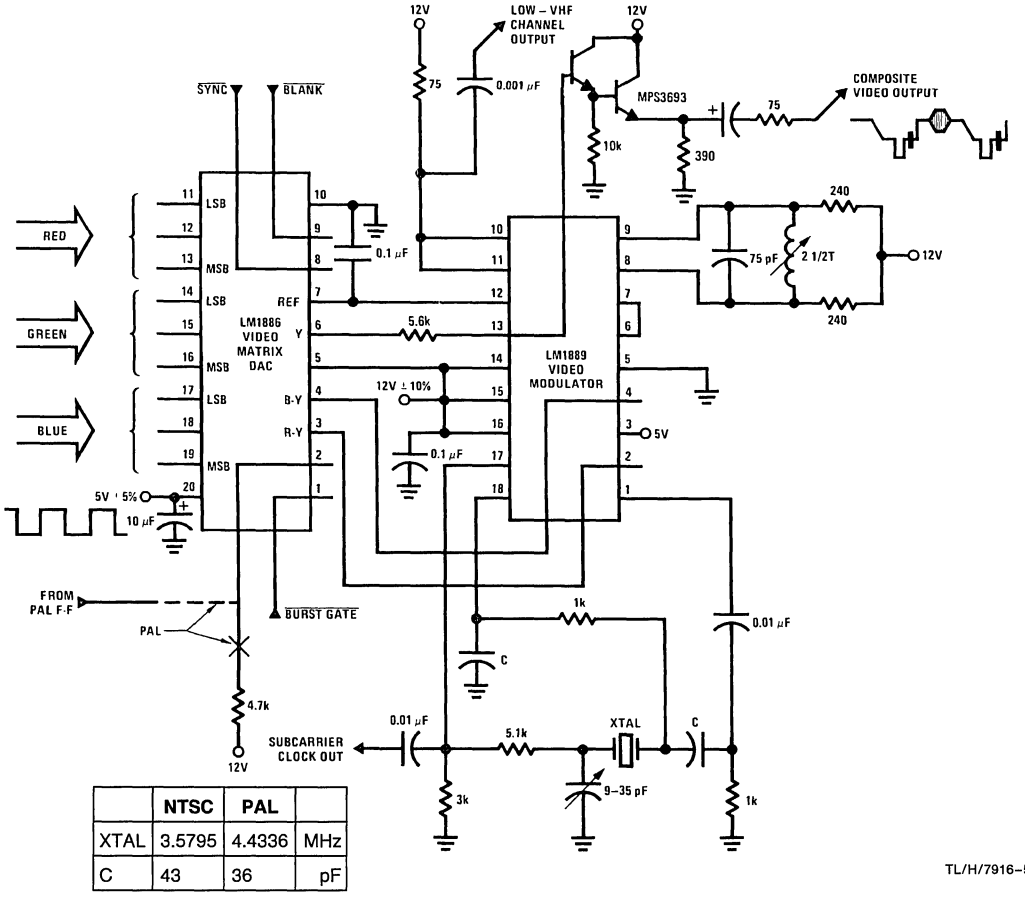
All inputs are low-power TTL compatible. Because of the very low typical input currents, the color inputs may be paralleled in various combinations. For simple color requirements, the *Figure 2a* input connection may be used to produce the 6 primary and complementary colors listed in Table I, along with black and white. To add complex colors such as those at the bottom of Table I, all 9 input bits may be required separately. When choosing input codes for other colors, always check the new color against both light and dark backgrounds.

All outputs are referenced to the +5V supply for direct connection to the LM1889. The resistor on the luminance output pin 6 is used to sum the chroma subcarrier from the LM1889 and must be wired as tightly as possible to preserve the video bandwidth. For the addition of sound or a second RF channel, refer to the LM1889 data sheet.

TABLE I. Input Code Examples for Common Colors

		Input Code								
		Red			Green			Blue		
	Color	M		L	M		L	M		L
	Black	0	0	0	0	0	0	0	0	0
	Dark Grey	0	1	0	0	1	0	0	1	0
	Light Grey	1	0	1	1	0	1	1	0	1
	White	1	1	1	1	1	1	1	1	1
Primary	Red	1	1	1	0	0	0	0	0	0
Primary	Green	0	0	0	1	1	1	0	0	0
Primary	Blue	0	0	0	0	0	0	1	1	1
Complementary	Cyan	0	0	0	1	1	1	1	1	1
Complementary	Magenta	1	1	1	0	0	0	1	1	1
Complementary	Yellow	1	1	1	1	1	1	0	0	0
	Brown	0	1	1	0	1	1	0	0	0
	Orange	1	1	1	1	0	0	0	0	0
	Flesh Tone	1	1	1	1	1	0	1	0	1
	Pink	1	1	1	1	1	0	1	1	0
	Sky Blue	1	0	1	1	0	1	1	1	1

Typical Application



	NTSC	PAL	
XTAL	3.5795	4.4336	MHz
C	43	36	pF

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FIGURE 3

Circuit Description (Refer to *Figure 4*)

The 3-bit red, green, and blue inputs go to identical 3-bit current-mode digital-to-analog converters (DACs). Each DAC consists of three binary-weighted current sources controlled by diff-amp current switches. The DAC output currents are arbitrarily given a weighting factor of 0.59, which is the green coefficient in the luminance equation. Portions of the red and blue currents are split off, so that the remaining currents combined with the green current form the luminance current $I_Y = 0.3\ I_R + 0.59\ I_G + 0.11\ I_B$. I_Y develops the luminance voltage V_Y across R_O in a summing amplifier referenced to the +5V supply. A current switch operated by pin 8 adds (−) sync pulses to the Y output at pin 6.

The portions of red and blue currents previously split off flow through resistors $R_O/0.29$ and $R_O/0.48$, which are weighted to form the red and blue voltages respectively. Since the opposite ends of the 2 resistors are connected to V_Y, the red and blue voltages across the resistors subtract from V_Y to develop the color difference voltages V_{Y-R} and V_{Y-B}. V_{Y-B} is coupled through a X.56 gain, 5V-referenced inverting amplifier to the B-Y output at pin 4. V_{Y-R} feeds parallel inverting and non-inverting unity gain amplifiers which allow either polarity to be coupled to the R-Y output pin 3. Switching between the 2 amplifiers is controlled by a current switch activated by the H/2 pin 2. A (−) burst gate pulse on pin 1 controls current switches which add the burst pulse components to the B-Y and R-Y outputs.

The requirements for PAL and NTSC encoding differ in the areas of burst gate operation and R-Y polarity, both of which are controlled via pin 2 as follows:

PAL, pin 2 fed by a half-line frequency TTL square wave—in this mode a PNP switch between pin 2 and +5V is held off continuously, which results in equal burst pulse components on the B-Y and R-Y outputs. In addition, the H/2 square wave causes the R-Y output polarity to reverse every line. (When fed to the LM1889 chroma modulator this causes the phase of the R-Y subcarrier to change 180° as required in PAL.)

NTSC, pin 2 tied through an external resistor to +12V—this turns on the PNP switch continuously, which eliminates the burst pulse on the R-Y output and increases the amplitude of the B-Y pulse. Since pin 2 is being held high, the R-Y output is locked in the positive polarity.

Blanking is activated by a low on pin 9, which de-biases the left side of the DAC diff-amps, so that $I_R = I_G = I_B = 0$ independent of the input states. When blanked, the Y, B-Y and R-Y outputs all go to +5V. An additional amplifier produces a 0 carrier reference voltage at pin 7 which is 25% above the peak white voltage on the Y output, relative to +5V.

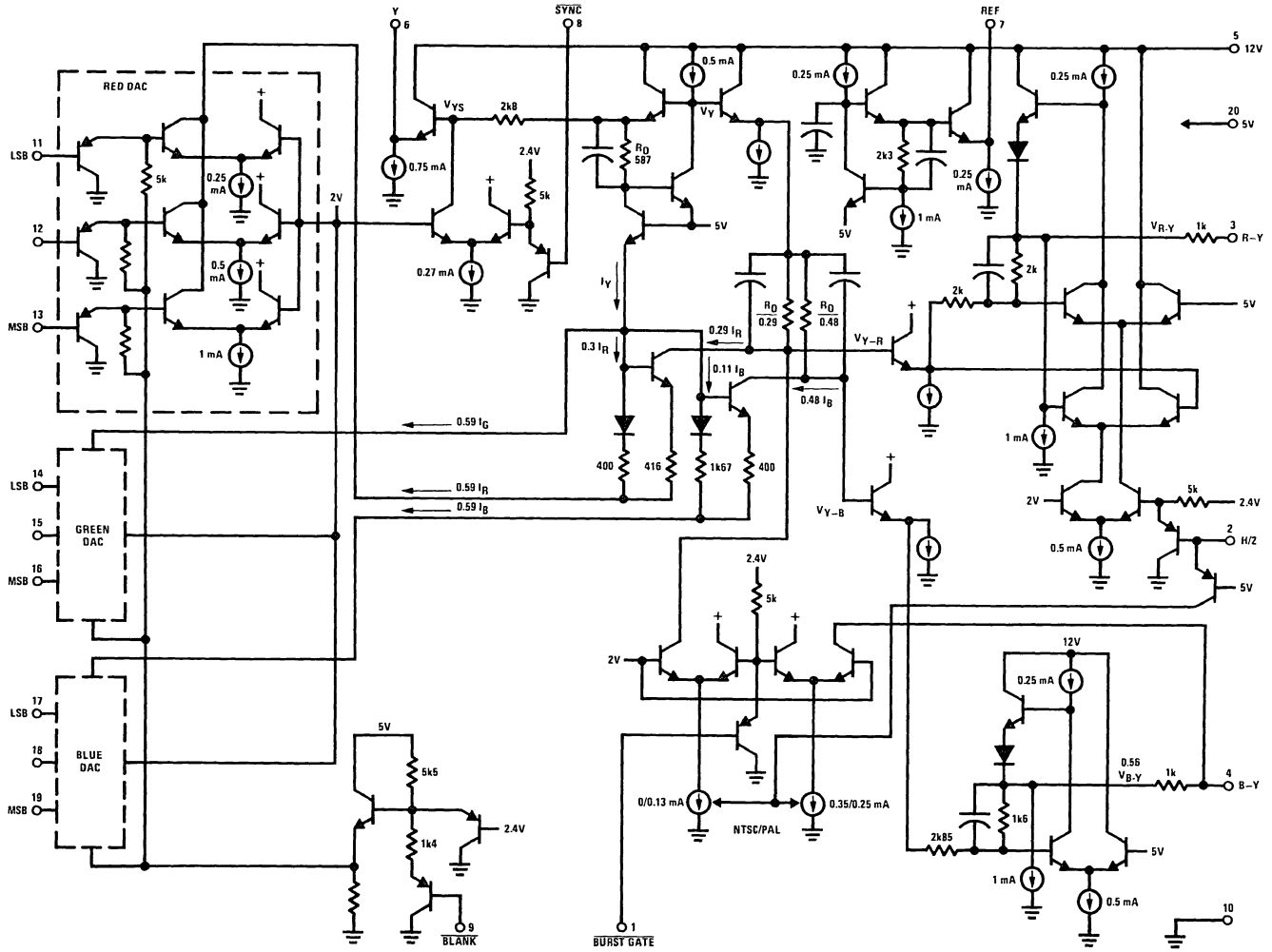

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FIGURE 4. LM1886 Equivalent Schematic

National Semiconductor Corporation

PRELIMINARY

LM1889 TV Video Modulator

General Description

The LM1889 is designed to interface audio, color difference, and luminance signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator, chroma subcarrier oscillator, quadrature chroma modulators, and RF oscillators and modulators for two low-VHF channels.

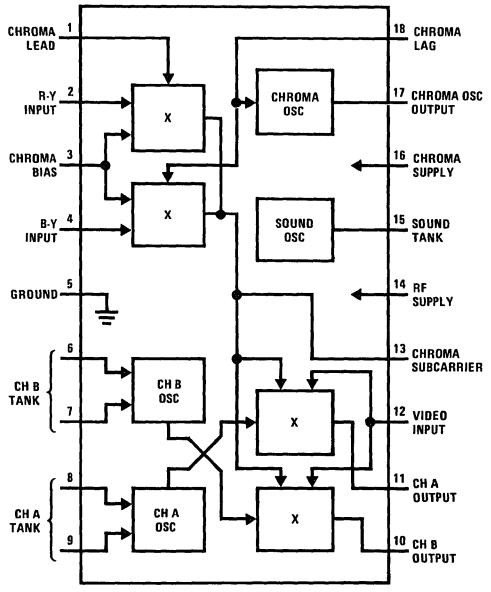
The LM1889 allows video information from VTR's, games, test equipment, or similar sources to be displayed on black and white or color TV receivers. When used with the MM57100 and MM53104, a complete TV game is formed.

Features

- dc channel switching
- 12V to 18V supply operation
- Excellent oscillator stability
- Low intermodulation products
- 5 Vp-p chroma reference signal
- May be used to encode composite video

Block Diagram

Dual-In-Line Package



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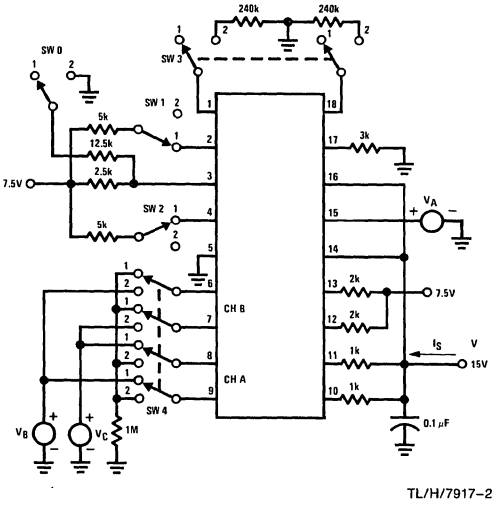
Order Number LM1889N
See NS Package Number N18A

DC Test Circuit



TL/H/7917–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V14, V16 max	19 V_{DC}
Power Dissipation Package (Note 1)	1800 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Chroma Osc Current I_{17} max	10 mA_{DC}
(V16–V15) max	±5 V_{DC}
(V14–V10) max	7V
(V14–V11) max	7V
Lead Temperature (Soldering, 10 sec.)	260°C

DC Electrical Characteristics (dc Test Circuit, All SW Normally Pos. 1, V_A = 15V, V_B = V_C = 12V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_S	Supply Current		20	35	45	mA
ΔI_{15}	Sound Oscillator, Current Change	Change V_A from 12.5 to 17.5V	0.3	0.6	0.9	mA
V17	Chroma Oscillator Balance		9.5	11.0	12.5	V
V13	Chroma Modulator Balance		7.0	7.4	7.8	V
ΔV13	R-Y Modulator Output Level	SW 3, Pos. 2, Change SW 1 from Pos. 1 to Pos. 2	0.6	0.9	1.2	V
ΔV13	B-Y Modulator Output Level	SW 3, Pos. 2, Change SW 2 from Pos. 1 to Pos. 2	0.6	0.9	1.2	V
ΔV13/ΔV3	Chroma Modulator Conversion Ratio	SW 3, Pos. 2, Change SW 0 from Pos. 1 to Pos. 2 Divide ΔV13 by ΔV3	0.45	0.70	0.95	V/V
V8, V9	Ch. A Oscillator "OFF" Voltage	SW 4, Pos. 2		1.0	3.0	V
I_9	Ch. A Oscillator Current Level	V_B = 12V, V_C = 13V	3.0	4.0	5.5	mA
V6, V7	Ch. B Oscillator "OFF" Voltage			1.0	3.0	V
I_6	Ch. B Oscillator Current Level	SW 4, Pos. 2, V_B = 12V, V_C = 13V	3.0	4.0	5.5	mA
ΔV11/(V13–V12)	Ch. A Modulator Conversion Ratio	SW 1, SW2, SW 3, Pos. 2, Measure ΔV11(V10) by Changing from V_B = 12.5V, V_C = 11.5V to V_B = 11.5V, V_C = 12.5V and Divide by V13–V12	0.35	0.55	0.75	V/V
ΔV10/(V13–V12)	Ch. B Modulator Conversion Ratio	Divide as Above	0.35	0.55	0.75	V/V

AC Electrical Characteristics (AC Test Circuit, V = 15V)

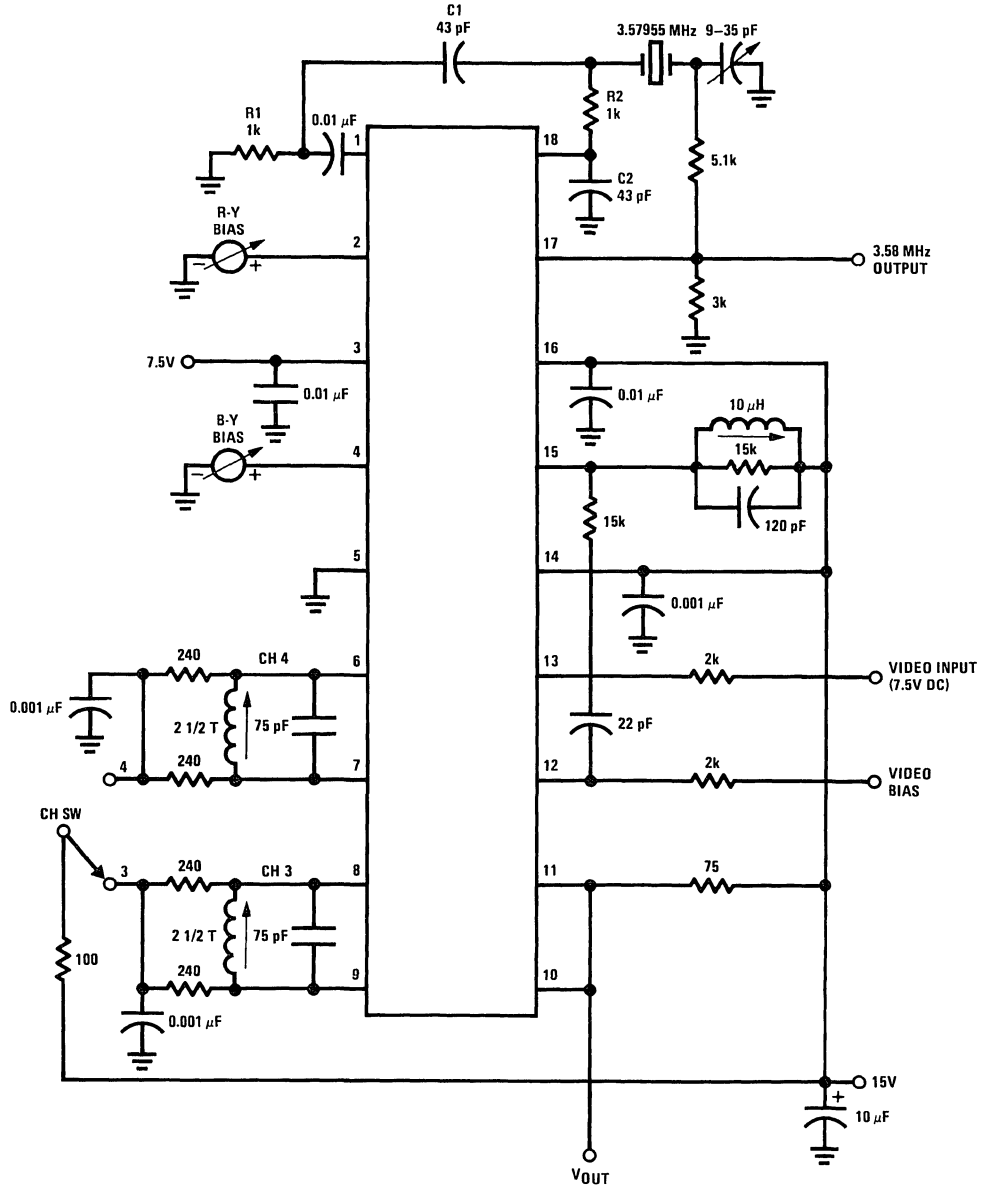
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V17	Chroma Oscillator Output Level	$C_{LOAD} \leq$ 20 pF	4	5		Vp-p
V15	Sound Carrier Oscillator Level	Loaded by RC Coupling Network	2	3	4	Vp-p
V8, V9	Ch. 3 RF Oscillator Level	Ch. SW. Pos. 3, f = 61.25 MHz, Use FET Probe	200	350		mVp-p
V6, V7	Ch. 4 RF Oscillator Level	Ch. Sw. Pos. 4, f = 67.25 MHz Use FET Probe	200	350		mVp-p

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150° maximum junction temperature and a thermal resistance of 70°C C/W junction to ambient.

Design Characteristics (AC Test Circuit, V = 15V)

Parameter	Typ	Units	Parameter	Typ	Units
Oscillator Supply Dependence			RF Modulator		
Chroma, f_o = 3.579545 MHz	3	Hz/V	Conversion Gain, f = 61.25 MHz,		
Sound Carrier, RF	See Curves		V_{OUT}/(V13−V12)	10	mVrms/V
Oscillator Temperature Dependence (IC Only)			3.58 MHz Differential Gain	5	%
Chroma	0.05	ppm/°C	Differential Phase	3	degrees
Sound Carrier	−15	ppm/°C	2.5 Vp-p Video, 87.5% mod.		
RF	−50	ppm/°C	Output Harmonics below Carrier		
Chroma Oscillator Output, Pin 17			2nd, 3rd	−12	dB
t_{RISE}, 10–90%	20	ns	4th and above	−20	dB
t_{FALL}, 90–10%	30	ns	Input Impedances		
Duty Cycle (+) Half Cycle	51	%	Chroma Modulator, Pins 2, 4	500k//2 pF	
(−) Half Cycle	49	%	RF Modulator, Pin 12	1M//2 pF	
RF Oscillator Maximum Operating Frequency	100	MHz	Pin 13	250k//3.5 pF	
(Temperature Stability Degraded)					
Chroma Modulator (f = 3.58 MHz)					
B-Y Conversion Gain V13/(V4−V3)	0.6	Vp-p/V			
R-Y Conversion Gain V13/(V2−V3)	0.6	Vp-p/V			
Gain Balance	±0.5	dB			
Bandwidth	See Curve				

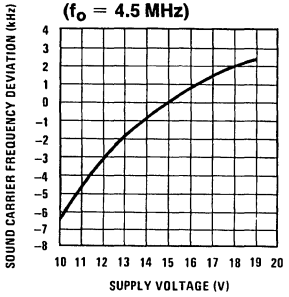
AC Test Circuit



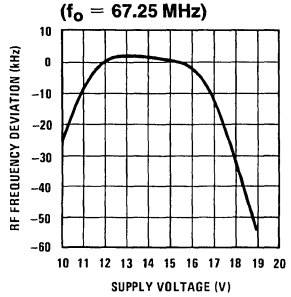
TL/H/7917–3

Typical Performance Characteristics

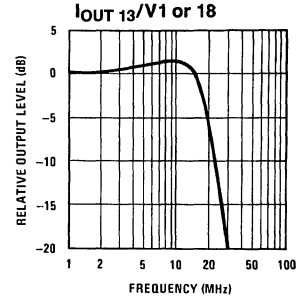
Sound Carrier Oscillator Supply Dependence (f_o = 4.5 MHz)



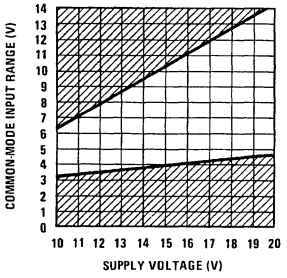
RF Oscillator Frequency Supply Dependence (f_o = 67.25 MHz)



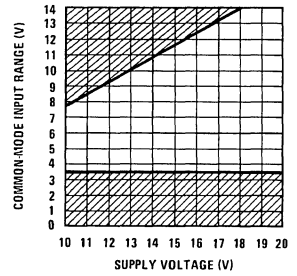
Chroma Modulator Transconductance Bandwidth $I_{OUT\ 13}/V1$ or 18



Chroma Modulator Common-Mode Input Range Pins 2, 3, 4



RF Modulator Common-Mode Input Range Pins 12, 13 (Application Circuit)



TL/H/7917–4

Circuit Description (Refer to Circuit Diagram)

The sound carrier oscillator is formed by differential amplifier Q3, Q4 operated with positive feedback from the pin 15 tank to the base of Q4.

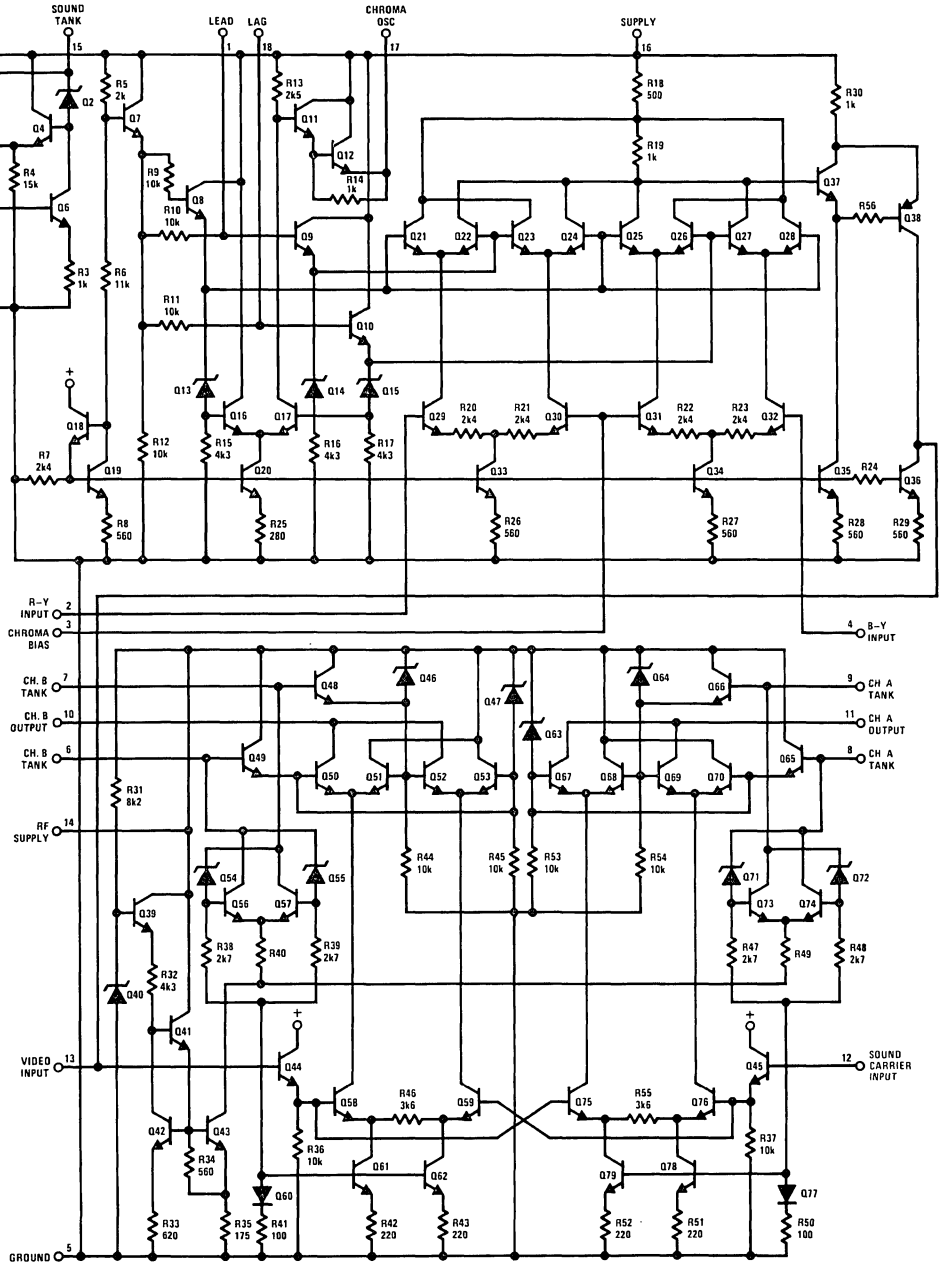
The chroma oscillator consists of the inverting amplifier Q16, Q17 and Darlington emitter follower Q11, Q12. An external RC and crystal network from pin 17 to pin 18 provides an additional 180 degrees phase lag back to the base of Q17 to produce oscillation at the crystal resonance frequency. (See AC test circuit).

The feedback signal from the crystal is split in a lead-lag network to pins 1 and 18, respectively, to generate the subcarrier reference signals for the chroma modulators. The R-Y modulator consists of multiplier devices Q29, Q30 and Q21–Q24, while the B-Y modulator consists of Q31, Q32 and Q25–Q28. The multiplier outputs are coupled through a balanced summing amplifier Q37, Q38 to the input of the RF modulators at pin 13. With 0 offset at the lower pairs of the multipliers, no chroma output is produced. However, when either pin 2 or pin 4 is offset relative to pin 3 a subcarrier output current of the appropriate phase is produced at pin 13.

The channel B oscillator consists of devices Q56 and Q57 cross-coupled through level-shift zener diodes Q54 and Q55. A current regulator consisting of devices Q39–Q43 is used to achieve good RF frequency stability over supply and temperature. The channel B modulator consists of multiplier devices Q58, Q59 and Q50–Q53. The top quad is coupled to the channel B tank through isolating devices Q48 and Q49. A dc offset between pins 12 and 13 offsets the lower pair to produce an output RF carrier at pin 10. That carrier is then modulated by both the chroma signal at pin 13 and the video and sound carrier signals at pin 12. The channel A modulator shares pin 12 and 13 buffers Q45 and Q44 with channel B and operates in an identical manner.

The current flowing through channel B oscillator diodes Q54, Q55 is turned around in Q60, Q61 and Q62 to source current for the channel B RF modulator. In the same manner, the channel A oscillator Q71–Q74 uses turn around Q77, Q78 and Q79 to source the channel A modulator. One oscillator at a time may be activated by connecting its tank to supply (see ac test circuit). The corresponding modulator is then activated by its current turn-around, and the other oscillator/modulator combination remains "OFF".

Circuit Diagram



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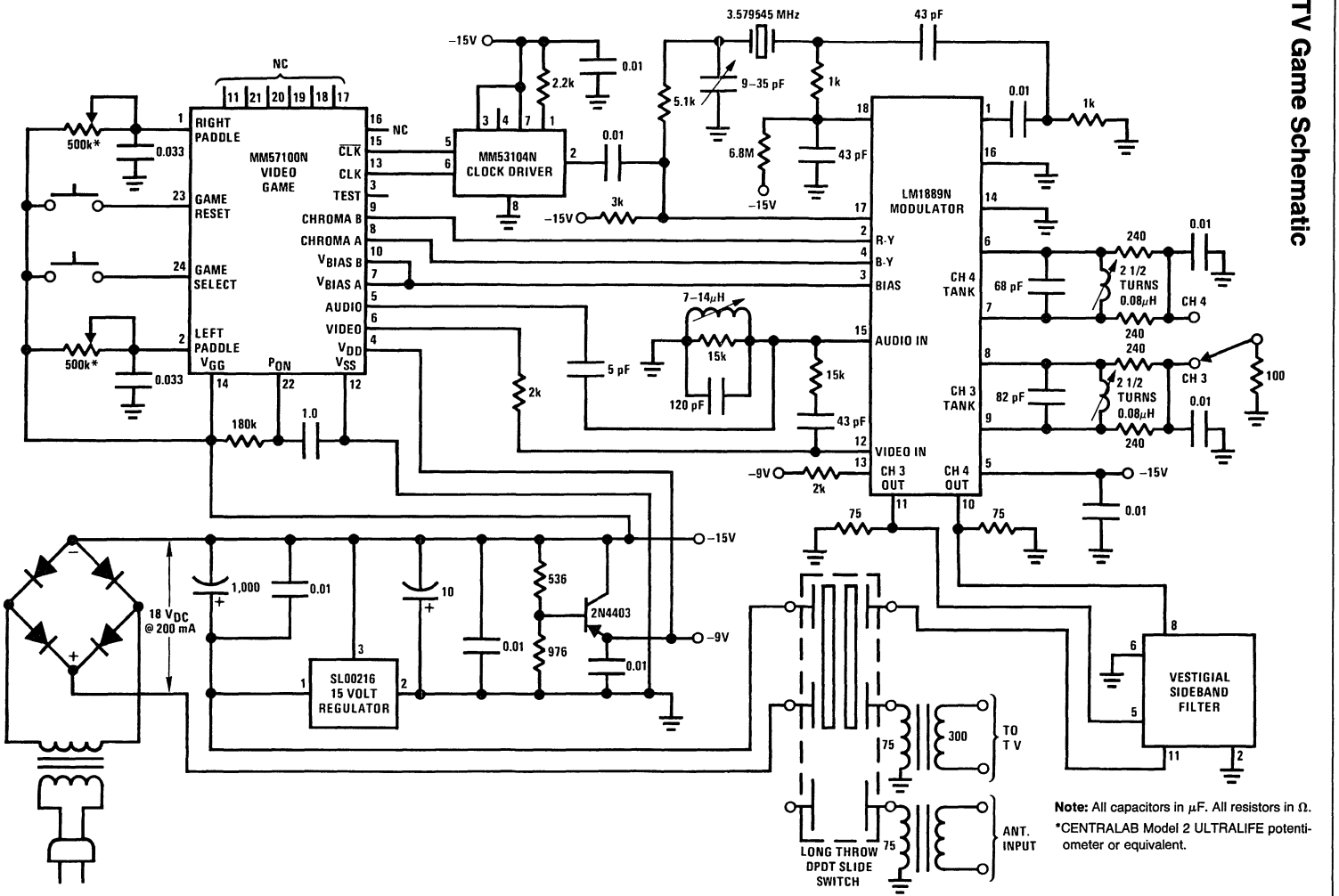
TV Game Schematic



Note: All capacitors in μF. All resistors in Ω.

*CENTRALAB Model 2 ULTRALIFE potentiometer or equivalent.

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Applications Information

Subcarrier Oscillator

The oscillator is a crystal-controlled design to ensure the accuracy and stability required of the subcarrier frequency for use with television receivers. Lag-lead networks (R2C2 and C1R1) define a quadrature phase relationship between pins 1 and 18 at the subcarrier frequency of 3.579545 MHz. Other frequencies can be used and where high stability is not a requirement, the crystal can be replaced with a parallel resonant L-C tank circuit—to provide a 2 MHz clock, for example. Note that since one of the chrominance modulators is internally connected to the feedback path of the oscillator, operation of the oscillator at other than the correct subcarrier frequency precludes chrominance modulation.

When an external subcarrier source is available or preferred, this can be used instead. For proper modulator operation, a subcarrier amplitude of 500 mVp-p is required at pins 1 and 18. If the quadrature phase shift networks shown in the application circuit are retained, about 1 Vp-p subcarrier injected at the junction of C1 and R2 is sufficient. The crystal, C4 and R3 are eliminated and pin 17 provides a 5 Vp-p signal shifted +125°C from the external reference.

Chrominance Modulation

The simplest method of chroma encoding is to define the quadrature phases provided at pins 1 and 18 as the color difference axes R-Y and B-Y. A signal at pin 2 (R-Y) will give a chrominance subcarrier output from the modulator with a relative phase of 90°C compared to the subcarrier output produced by a signal at pin 4 (B-Y). The zero signal dc level of the R-Y and B-Y inputs will determine the bias level required at pin 3. For example, a pin 2 signal that is 1V positive with respect to pin 3 will give 0.6 Vp-p subcarrier at a relative phase of 90°C. If pin 2 is 1V negative with repsect to pin 3, the output is again 0.6 Vp-p, but with a relative phase of 270°C. When a simultaneous signal exists at pin 4, the subcarrier output level and phase will be the vector sum of the quadrature components produced by pin 2 and 4 inputs. Clearly, with the modulation axes defined as above, a negative pulse on pin 4 during the burst gate period will produce the chrominance synchronizing "burst" with a phase of 180°. Both color difference signals must be dc coupled to the modulators and the zero signal dc level of both must be the same and within the common-mode range of the modulators.

The 0.6 Vp-p/V_{dc} conversion gain of the chrominance modulators is obtained with a 2 kΩ resistor connected at pin 13. Larger resistor values can be used to increase the gain, but capacitance at pin 13 will reduce the bandwidth. Notice that equi-bandwidth encoding of the color difference signals is implied as both modulator outputs are internally connected and summed into the same load resistor.

Sound Oscillator

Frequency modulation is achieved by using a 4.5 MHz tank circuit and deviating the center frequency via a capacitor or a varactor diode. Switching a 5 pF capacitor to ground at an audio frequency rate will cause a 50 kHz deviation from 4.5 MHz. A 1N5447 diode biassed −4V from pin 16 will give ±20 kHz deviation with a 1 Vp-p audio signal. The coupling network to the video modulator input and the varactor diode bias must be included when the tank circuit is tuned to center frequency.

A good level for the RF sound carrier is between 2% and 20% of the picture carrier level. For example, if the peak video signal offset of pin 12 with respect to pin 13 is 3V, this corresponds to a 30 mVrms picture RF carrier. The source impedance at pin 12 is defined by the external 2 kΩ resistor and so a series network of 15 kΩ and 24 pF will give a sound carrier level at −32 dB to the picture carrier.

RF Modulation

Two RF channels are available, with carrier frequencies up to 100 MHz being determined by L-C tank circuits at pins 6, 7, 8 and 9. The signal inputs (pins 12, 13) to both modulators are common, but removing the power supply from an RF oscillator tank circuit will also disable that modulator.

As with the chrominance modulators, it is the offset between the two signal input pins that determines the level of RF carrier output. Since one signal input (pin 13) is also internally connected to the chrominance modulators, the 2 kΩ load resistor at this point should be connected to a bias source within the common-mode input range of the video modulators. However, this bias source is independent of the chrominance modulator bias and where chrominance modulation is not used, the 2 kΩ resistor is eliminated and the bias source connected directly to pin 13.

To preserve the dc content of the video signal, amplitude modulation of the RF carrier is done in one direction only, with increasing video (toward peak white) decreasing the carrier level. This means the active composite video signal at pin 12 must be offset with respect to pin 13 and the sync pulse should produce the largest offset (i.e., the offset voltage of pin 12 with respect to pin 13 should have the same polarity as the sync pulses.

The largest video signal (peak white) should not be able to suppress the carrier completely, particularly if sound transmission is needed. For example, a signal with 1V sync amplitude and 2.5V peak white (3.5 Vp-p, negative polarity sync) and a black level at 5 V_{dc} will require a dc bias of 8V on pin 13 for correct modulation. A simple way of obtaining the required offset is to bias pin 13 at 4 x (sync amplitude) from the sync tip level at pin 12.

Applications Information (Continued)

Split Power Supplies

The LM1889 is designed to operate over a wide range of supply voltages so that much of the time it can utilize the signal source power supplies. An example of this is shown in *Figure 2* where the composite video signal from a character generator is modulated onto an RF carrier for display on a conventional home TV receiver. The LM1889 is biased between the −12V and +5V supplies and pin 13 is put at ground. A 9.1 kΩ resistor from pin 12 to −12V dc offsets the video input signal (which has sync tips at ground) to establish the proper modulation depth − R1/R2 = V_{IN}/12 x 0.875. This design is for monochrome transmission and features an extremely low external parts count.

DC Clamped Inputs

Utilizing a DC clamp will make matching the LM1889 to available signal generator outputs a simple process. *Figure 3* shows the LM1889 configured to accept the composite video patterns available from a Tektronix Type 144 generator that has black level at ground and negative polarity syncs. In this application, the chroma oscillator amplifier is used to provide a gain of two. The 100k pot adjusts the overall DC level of the amplified signal which determines the modulation depth of the RF output. Clamping the input requires a minimum of DC correction to obtain the correct DC output level. This allows the adjustment to be a high impedance that will have minimum effect on the amplifier closed loop gain.

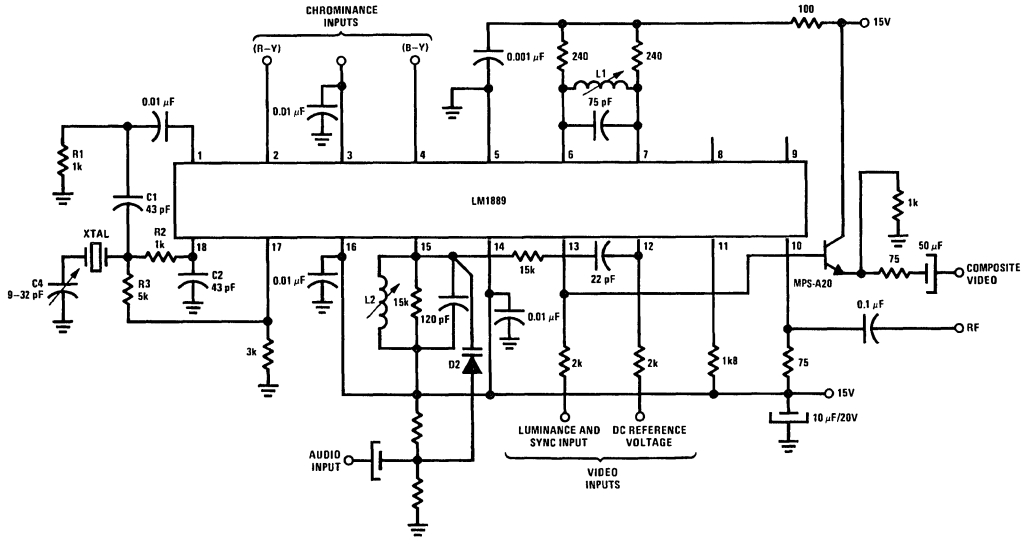

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FIGURE 1. Luminance and Chrominance Encoding Composite Video or RF Output

Applications Information (Continued)

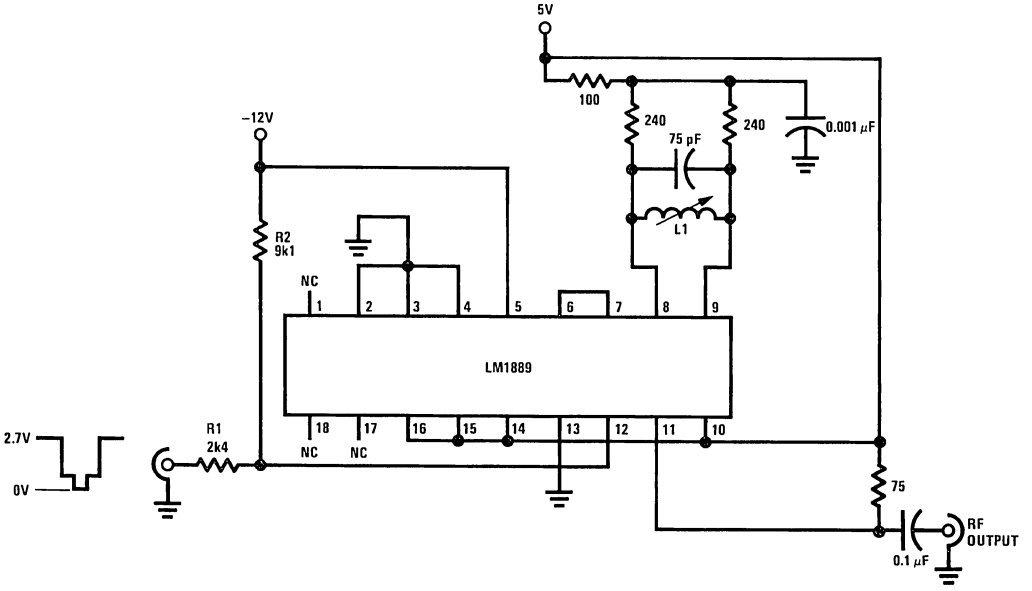

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FIGURE 2. Low-Cost Monochrome Modulator for Character Generator Display

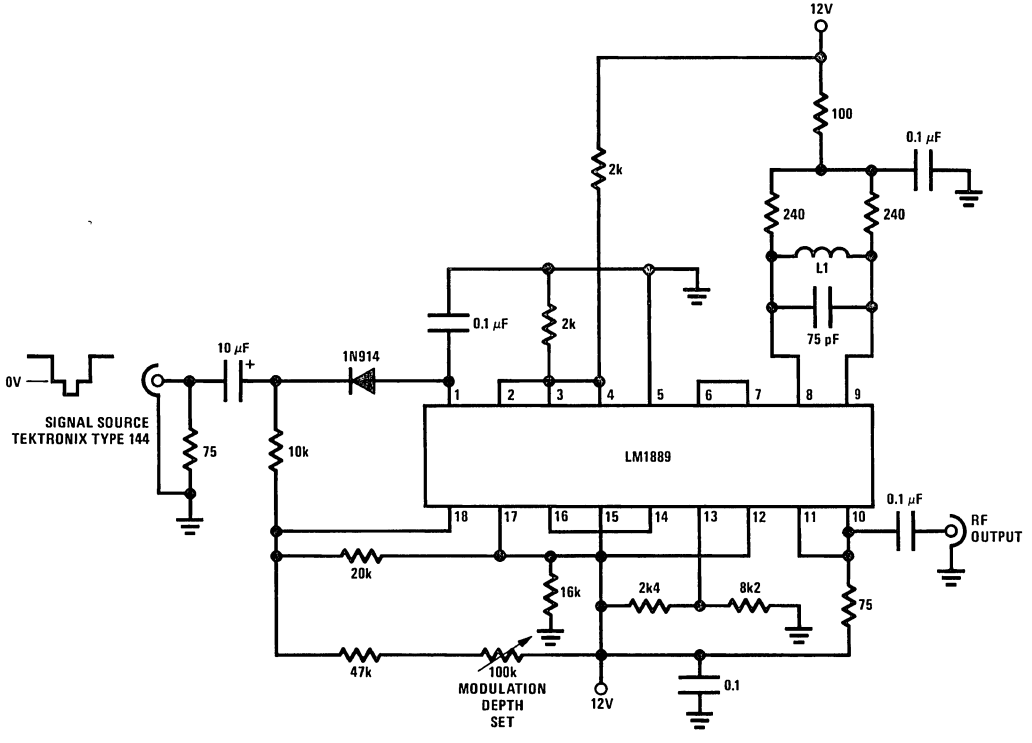

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FIGURE 3. DC Clamped Modulator for NTSC Pattern Generators

National Semiconductor Corporation

PRELIMINARY

LM2889 TV Video Modulator

General Description

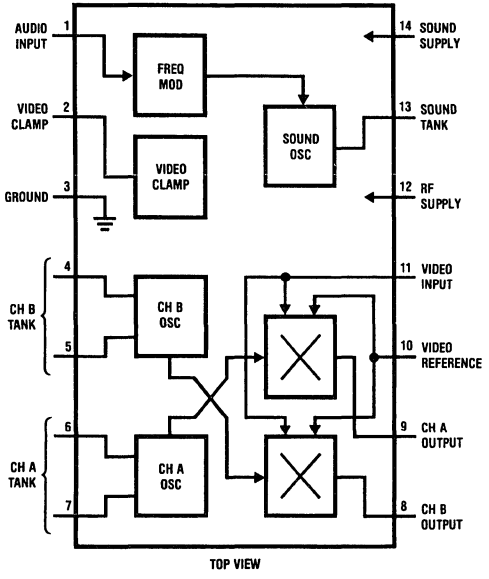
The LM2889 is designed to interface audio and video signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator and FM modulator, video clamp, and RF oscillators and modulators for two low-VHF channels.

The LM2889 allows video information from VTRs, video disk systems, games, test equipment, or similar sources to be displayed on black and white or color TV receivers.

Features

- Pin for pin compatible with LM1889 RF section
- Low distortion FM sound modulator (less than 1% THD)
- Video clamp for AC-coupled video
- Low sound oscillator harmonic levels
- 10V to 16V supply operation
- DC channel switching
- Excellent oscillator stability
- Low intermodulation products

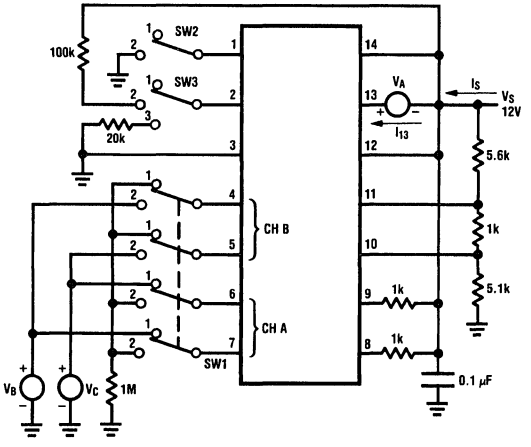
Block and Connection Diagrams (Dual-In-Line Package)



TOP VIEW

Order Number LM2889N
See NS Package Number N14A

DC Test Circuit



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	$18V_{DC}$
Power Dissipation Package (Note 1)	700 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
(V14−V13) Max	$\pm 5V_{DC}$
(V12−V8) Max	$7V_{DC}$
(V12−V9) Max	$7V_{DC}$
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics

(DC test circuit, all switches normally pos. 1, $V_S = 12V$, $V_A = 2V$, $V_B = V_C = 10V$)

Parameter	Conditions	Min	Typ	Max	Units
Supply Current I_S		10	16	25	mA
Sound Oscillator Current ΔI_{13}	Change V_A from −2V to +2V	0.2	0.35	0.6	mA
Sound Oscillator Zener Current I_{13}			0.85		mA
Sound Modulator Audio Current ΔI_{13}	Change SW2 from Pos. 1 to Pos. 2		0.9		mA
Video Clamp Voltage V2 Unloaded Loaded	 SW3 Pos. 3	5.0	 5.25 5.1	5.5	 V_{DC} V_{DC}
Video Clamp Capacitor Discharge Current $(V_S-V2)/10^5$	SW3 Pos. 2		20		μA
Ch. A Oscillator OFF Voltage, V6, V7	SW1 Pos. 2		2		mV_{DC}
Ch. A Oscillator Current Level I_7	$V_B = 10V$, $V_C = 11V$	2.5	3.5	5.0	mA
Ch. B Oscillator OFF Voltage V4, V5			2		mV_{DC}
Ch. B Oscillator Current Level I_4	SW1 Pos. 2, $V_B = 10V$, $V_C = 11V$	2.5	3.5	5.0	mA
Ch. A Modulator Conversion Ratio $\Delta V9/(V11-V10)$	Measure ΔV9 by Changing from $V_B = 10V$, $V_C = 11V$, to $V_B = 11V$, $V_C = 10V$; Divide by V11−V10	0.3	0.50	0.75	V/V
Ch. B Modulator Conversion Ratio $\Delta V8/(V11-V10)$	SW1 Pos. 2, Measure ΔV8 by Changing from $V_B = 10V$, $V_C = 11V$, to $V_B = 11V$, $V_C = 10V$; Divide by V11−V10	0.3	0.50	0.75	V/V

AC Electrical Characteristics (AC test circuit, $V_S = 12V$)

Parameter	Conditions	Min	Typ	Max	Units
Sound Carrier Oscillator Level (V13)			3.4		Vp-p
Sound Modulator Deviation	$\Delta f/\Delta V_{IN}$, SW1 Pos. 2, Change V_{IN} from 1.4V to 1.0V, Measure Δf at Pin 13, Divide as Shown		250		Hz/mV
Ch. 3 RF Oscillator Level $\nu 6$, $\nu 7$	Ch. Sw. Pos. 3, f = 61.25 MHz, Use FET Probe		550		mVp-p
Ch. 4 RF Oscillator Level, $\nu 4$, $\nu 5$,	Ch. Sw. Pos. 4, f = 67.25 MHz, Use FET Probe		550		mVp-p
RF Modulator Conversion Gain $\nu_{OUT}/(V10-V11)$	Ch. Sw. Pos. 3, f = 61.25 MHz. (Note 2)		10		mVrms/V

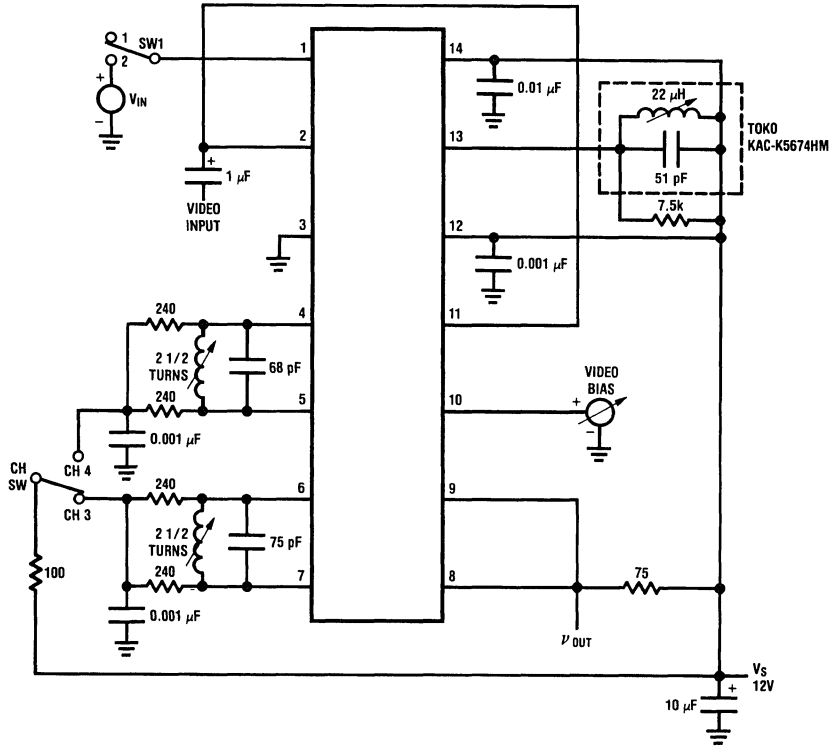
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Note 2: Conversion gain shown is measured with 75Ω input RF meter which makes the AC RF output load 37.5Ω.

Design Characteristics (AC test circuit, $V_S = 12V$)

Parameter	Typ	Units
Sound Modulator Audio THD at ±25 kHz Deviation, V_{IN} must be 1 kHz Source, Demodulate as Shown in *Figure 1*	0.8	%
Sound Modulator Input Impedance (Pin 1)	1.5	kΩ
Sound Modulator Bandwidth	100	kHz
Oscillator Supply Dependence, Sound Carrier, RF	See Curves	
Oscillator Temperature Dependence (IC Only)		
Sound Carrier	−15	ppm/°C
RF	−50	ppm/°C
RF Oscillator Maximum Operating Frequency (Temperature Stability Degraded)	100	MHz
RF Modulator		
Carrier Suppression (Adjust Video Bias for Minimum RF Carrier at ν_{OUT} and Reference to ν_{OUT} with 3V Offset at Pins 10 and 11, See Applications Information, RF Modulation Section)	30	dB
3.58 MHz Differential Gain	5	%
Differential Phase	3	degrees
2.5V Vp-p Video, 87.5% Mod		
Output Harmonics below RF Carrier		
2nd, 3rd	−12	dB
4th and Above	−20	dB
Input Impedance, Pin 10, Pin 11	1 MΩ//2 pF	

AC Test Circuit



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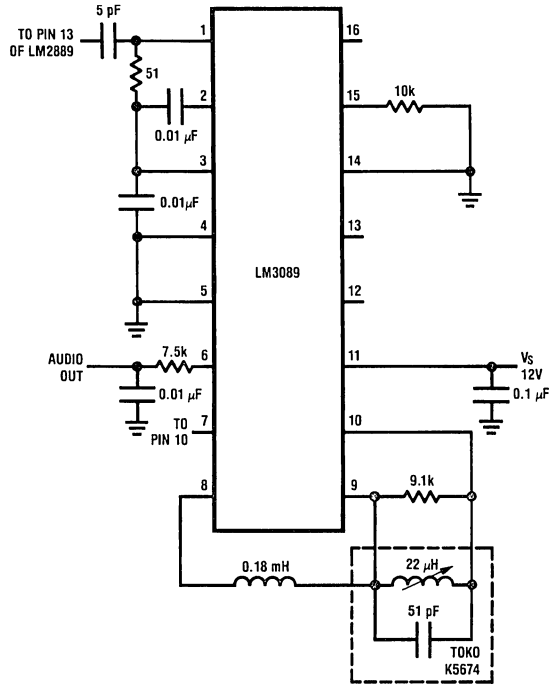
Test Circuit

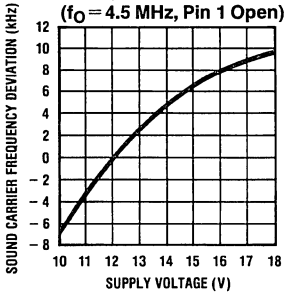


TL/H/5079–3

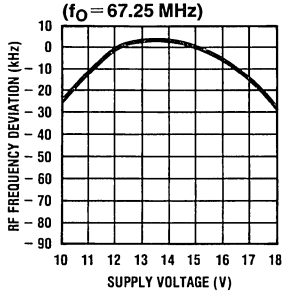
FIGURE 1. 4.5 MHz Sound FM Demodulator

Typical Performance Characteristics (Refer to AC test circuit unless noted)

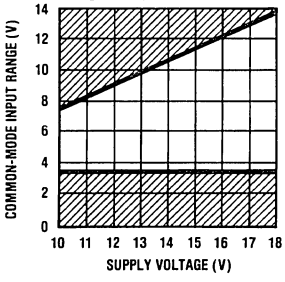
Sound Carrier Oscillator Supply Dependence (f_O = 4.5 MHz, Pin 1 Open)



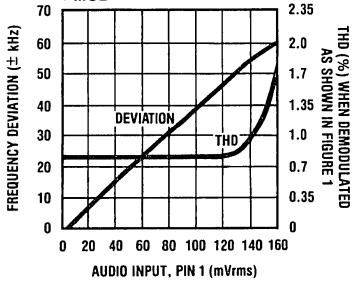
RF Oscillator Frequency Supply Dependence (f_O = 67.25 MHz)



RF Modulator Common-Mode Input Range Pins 10, 11 (Circuit Diagrams)



FM Sound Modulator Dynamic Characteristics (f_{MOD} = 1 kHz)



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Circuit Description (Refer to Circuit Diagrams)

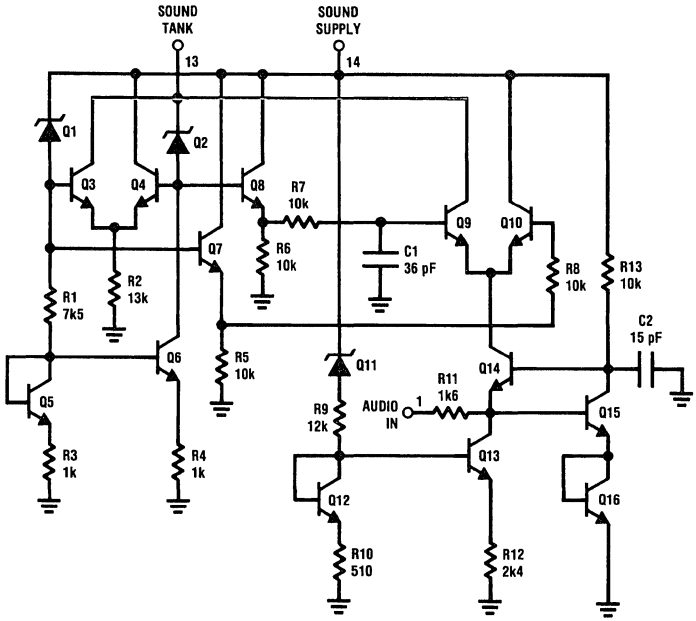
The sound carrier oscillator is formed by differential amplifier Q3, Q4 operated with positive feedback from the pin 13 tank to the base of Q4. Frequency modulation is obtained by varying the 90 degree phase shifted current of Q9. Q14's emitter is a virtual ground, so the voltage at pin 1 determines the current R11, which ultimately modulates the collector current of Q9.

The video clamp is comprised of devices Q58-Q60. The clamp voltage is set by resistors R40, R41, R49, and R50. The $\Delta V_{BE}/R42$ current sets the capacitor discharge current. Q59 and the above mentioned resistor string help maintain a temperature stable clamp voltage.

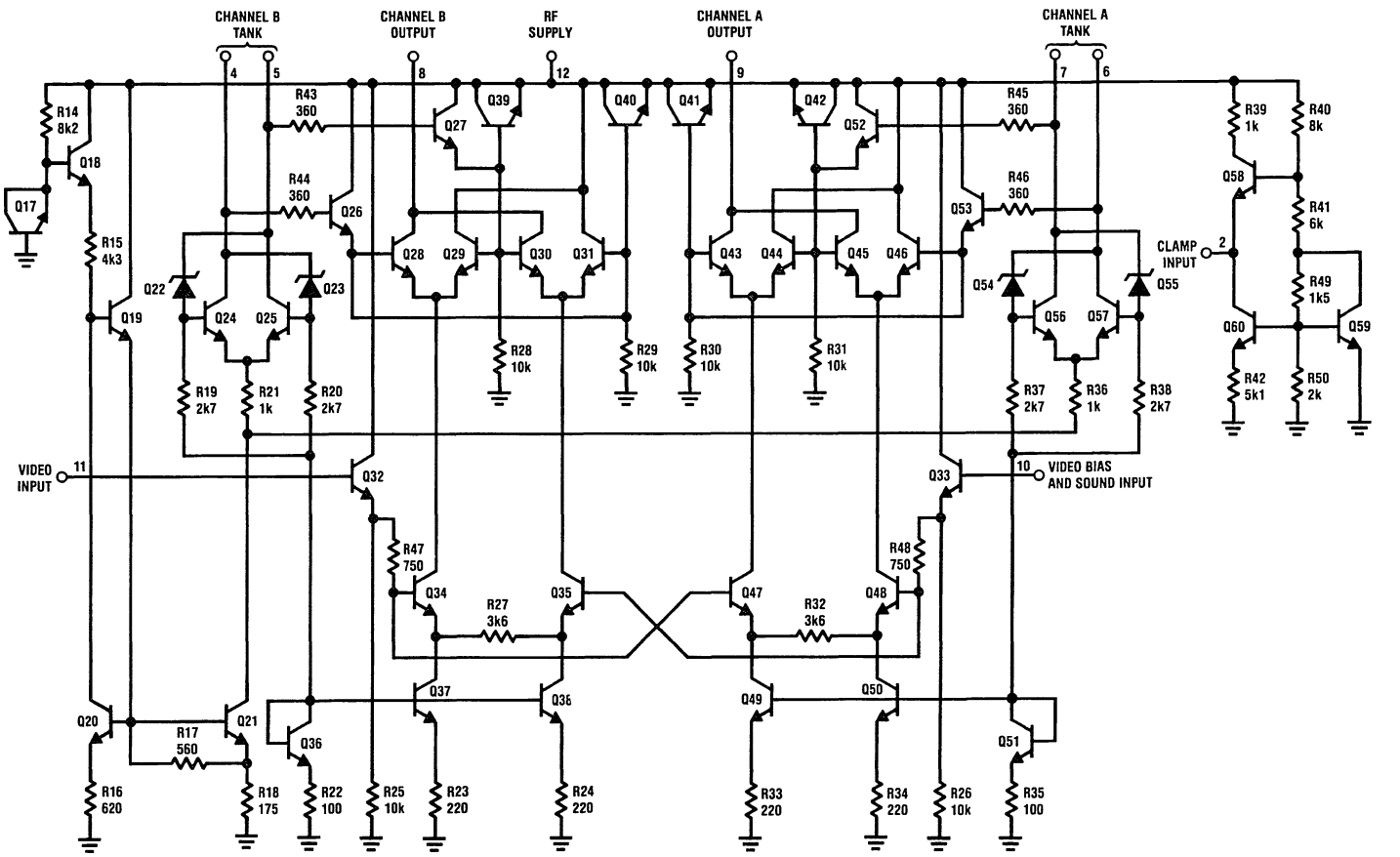
The channel B oscillator consists of devices Q24 and Q25 cross-coupled through level-shift zener diodes Q22 and Q23. A current regulator consisting of devices Q17–Q21 is used to achieve good RF stability over temperature and supply. The channel B modulator consists of multiplier devices Q28–Q31, Q34 and Q35. The top quad is coupled to the channel B tank through isolating devices Q26 and Q27. A DC potential between pins 10 and 11 offsets the lower pair to produce an output RF carrier at pin 8. That carrier is then modulated by both the sound subcarrier at pin 10 and the composite video signal at pin 11. The channel A modulator shares pin 10 and 11 buffers, Q32 and Q33, with channel B and operates in an identical manner.

The current flowing through channel B oscillator diodes Q22, Q23 is turned around in Q36–Q38 to source current for the channel B RF modulator. In the same manner, the channel A oscillator Q54–Q57 uses turn-around Q49–Q51 to source the channel A modulator. One oscillator at a time may be activated by its current turn-around, and the other oscillator/modulator combination remains off.

Circuit Diagrams



TL/H/5079–5


CHANNEL B TANK
CHANNEL B OUTPUT
RF SUPPLY
CHANNEL A OUTPUT
CHANNEL A TANK
4
5
8
12
9
7
6
R14 8k2
Q18
Q17
R15 4k3
R43 360
R44 360
Q26
Q27
Q39
Q40
Q41
Q42
Q52
R45 360
R46 360
Q53
R39 1k
R40 8k
Q58
R41 6k
CLAMP INPUT
2
R49 1k5
Q60
Q59
R42 5k1
R50 2k
Q22
Q23
Q24
Q25
Q19
Q28
Q29
Q30
Q31
Q43
Q44
Q45
Q46
Q54
Q55
Q56
Q57
R19 2k7
R21 1k
R20 2k7
R28 10k
R29 10k
R30 10k
R31 10k
R37 2k7
R36 1k
R38 2k7
VIDEO INPUT
11
Q32
Q33
10
VIDEO BIAS AND SOUND INPUT
R47 750
R48 750
Q34
Q35
Q47
Q48
R27 3k6
R32 3k6
Q37
Q36
Q49
Q50
Q20
Q21
R17 560
Q36
Q51
R16 620
R18 175
R22 100
R25 10k
R23 220
R24 220
R33 220
R34 220
R26 10k
R35 100

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Applications Information

SOUND FM MODULATOR

Frequency deviation is determined by the Q of the tank circuit at pin 13 and the current entering the audio input, pin 1. This current is set by the input voltage V_{IN}, the device input impedance (1.5 kΩ), and any impedance network connected externally. A signal of 60 mVrms at pin 1 will yield about ±25 kHz deviation when configured as shown in *Figure 2*.

VIDEO CLAMP

When video is not available at DC levels within the RF modulator common-mode range, or if the DC level of the video is not temperature stable, then it should be AC-coupled as shown in the typical applications circuit (*Figure 2*). The clamp holds the horizontal sync pulses at 5.2V for $V_S = 12V$. The clamp coupling capacitor is charged during every sync pulse and discharged when video information is present. The discharge current is approximately 20 μA. This current and the amount of acceptable tilt over a line of video determines the value of the coupling capacitor C1. For most applications 1 μF is sufficient.

RF MODULATION

Two RF channels are available, with carrier frequencies up to 100 MHz being determined by L-C tank circuits at pins 4/ 5 and 6/7. The signal inputs (pins 10 and 11) are common to both modulators, but removing the power supply from an RF oscillator will also disable that modulator.

The offset between the two signal pins determines the level of the RF carrier output. To preserve the DC content of the video signal, amplitude modulation of the RF carrier is done in one direction only, with increasing video (toward peak white) decreasing the carrier level. This means the active composite video signal at pin 11 must be offset with respect to pin 10 and the sync pulse should produce the largest offset.

The largest video signal (peak white) should not be able to suppress the carrier completely, particularly if sound transmission is needed. This requires that pin 10 be biased above the largest expected video signal. Because peak white level is often difficult to define, a good rule to follow is to bias pin 10 at a level which is four times the sync amplitude above the sync tip level at pin 11. For example, the DC bias at pin 10 with 0.5V sync clamped to 5.2V on pin 11, should be $5.2 + (4 \times 0.5) = 7.2V$.

Typical Application

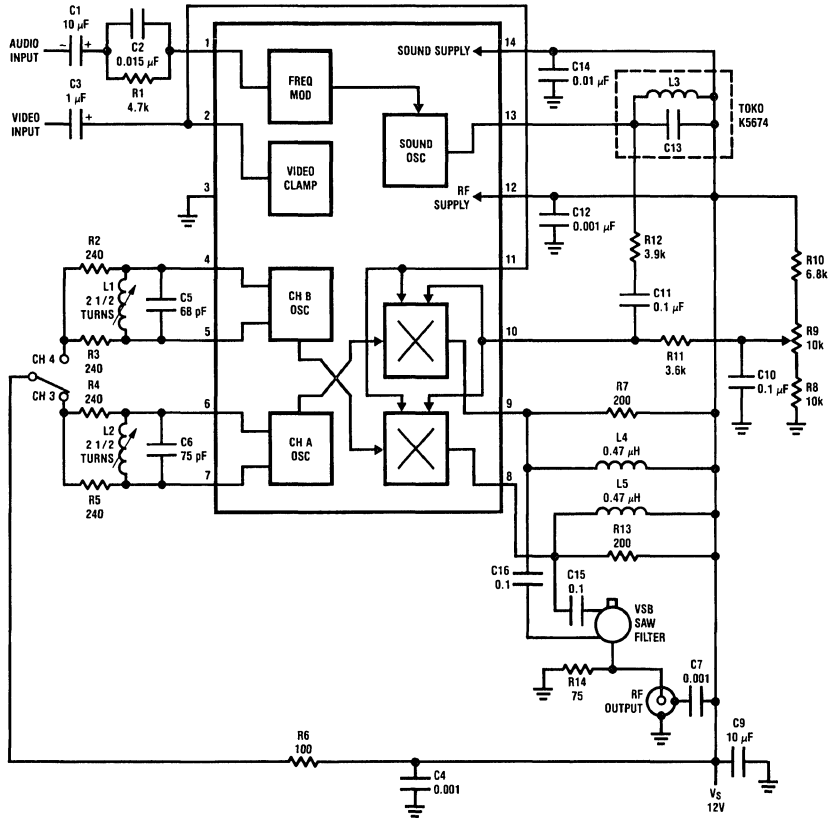

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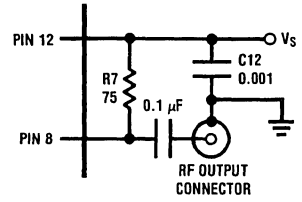
FIGURE 2. Two Channel Video Modulator with FM Sound

Applications Information (Continued)

When the signal inputs are exactly balanced, ideally there is no RF carrier at the output. Circuit board layout is critical to this measurement. For optimum performance, the output and supply decoupling circuitry should be configured as shown in *Figure 3*.



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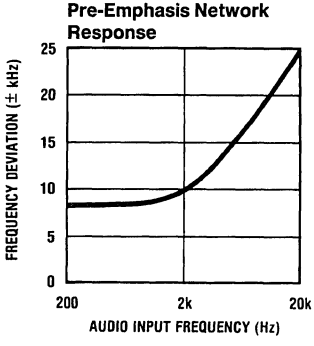
RF decouple supply directly to output ground.

FIGURE 3. Correct RF Supply Decoupling

The video clamp level is derived from a resistive divider connected to supply (V_S). To maintain good supply rejection, pin 10, which is biased externally, should also be referenced to supply (see *Figure 2*).

Pin Description (Refer to *Figure 2*)

Pin 1—Audio Input: Pin 1 is the audio input to the sound FM generator. Frequency deviation is proportional to the signal at this pin. A pre-emphasis network comprised of R1, C2, and the device input impedance yields the following response with an 80 mVrms audio input.



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Increasing R1 lowers the boost frequency, and decreases deviation below the boost frequency. Increasing C2 only lowers the boost frequency. C1 is a coupling capacitor, and must be a low impedance compared to the sum of R1 and the device input impedance (1.5 kΩ).

Pin 2—Video Clamp: The video clamp restores the DC component to AC-coupled video. The video is AC-coupled to the clamp via C3. Decreasing C3 will cause a larger tilt between vertical sync pulses in the clamped video waveform.

Pin 3—Ground: Although separate on the chip level, all ground terminate at pin 3.

Pins 4/5—Channel 4 Oscillator: Pins 4 and 5 are the collector outputs of the channel 4 oscillator. L1 and C5 set the oscillator frequency defined by $f_O = 0.159/\sqrt{L1C5}$. Increasing L1 will decrease the oscillator frequency while decreasing L1 will increase the oscillator frequency. Decreasing C5 will increase the oscillator frequency and lower the tank Q causing possible drift problems. R2 and R3 are the oscillator loads which determine the oscillator amplitude and the tank Q. Increasing these resistors increases the Q and the oscillator amplitude, possibly overdriving the RF modulator, which will increase output RF harmonics. Decreasing R2 and R3 reduces the tank Q and may cause increased drift. C4 is an RF decoupling capacitor. Increasing C4 may result in less effective decoupling at RF. Decreasing C4 may introduce RF to supply coupling.

Pins 6/7—Channel 3 Oscillator; Pins 6 and 7 are the channel 3 oscillator outputs. Every component at these pins has the same purpose and effect as those at pins 4 and 5.

Pin 8—Channel 4 RF Output: Pin 8 is the channel 4 RF output and R13 is the load resistor. The RF signal is AC coupled via C15 to the output filter which is a two channel VSB filter. L5 is parallel resonant with the filter input capacitance minimizing loss in the output network. R14 terminated the filter output.

Pin 9—Channel 3 RF Output: Pin 9 is the channel 3 RF output with all components performing the same functions as those in the pin 8 description.

Pin 10—RF Modulator Sound Subcarrier Input: Pin 10 is one of the RF modulator inputs and may be used for video or sound. It is used as a sound subcarrier input in *Figure 2*. R8, R9, and R10 set the DC bias on this pin which determines the modulation depth of the RF output (see Application Notes). R12 and C11 AC-couple the sound subcarrier from the sound modulator to the RF modulator. R12 and R11 form a resistive divider that determines the level of sound at pin 10; which in turn sets the picture carrier to sound subcarrier ratio. Increasing the ratio of R11/R12 will increase the sound subcarrier at the output. C10 forms an AC ground, preventing R8, R9, and R10 from having any effects on the circuit other than setting the DC potential at pin 10. R11 and R12 also effect the FM sound modulator (see pin 13 description).

Pin Description (Continued)

Pin 11—Video Input: Pin 11, when configured as shown, is the RF modulator video input. In this application, video is coupled directly from the video clamp. Alternatively, video could be DC-coupled directly to pin 11 if it is already within the DC common-mode input range of the RF modulator (see curves). In any case, the video sync tip at pin 11 must have a constant DC level independent of video content. Because of circuit symmetry, pins 10 and 11 may be interchanged.

Pin 12—RF Supply: Pin 12 is the RF supply, with C12 and C7 serving as RF decouple capacitors. Increasing C12 or C7 may result in less effective RF decoupling, while decreasing them may cause supply interaction. It is important that C7 be grounded at the RF output ground.

Pin 13—Sound Tank: Pin 13 is the collector output of the sound oscillator. L3 and C13 determine the oscillating frequency by the relationship $f_O = 0.159/\sqrt{L3C13}$. Increasing L3 or C13 will lower the operating frequency, while decreasing them will raise the frequency. L3 and C13 also help define the Q of the tank, on which FM modulator deviation level depends. As C13 increases, Q increases, and frequency deviation decreases. Likewise, decreasing C13 increases deviation. The other factor concerning Q is the external resistance across the tank. The series combination R11 + R12 usually dominates the tank Q. Decreasing this resistive network will decrease Q and increase deviation. It should be noted that because the level of phase modulation of the 4.5 MHz signal remains constant, variation in Q will not effect distortion of the frequency modulation process if the audio at pin 1 is left constant. The amplitude of the sound subcarrier is directly proportional to Q, so increasing the unloaded Q or either of the resistors mentioned above will increase the sound subcarrier amplitude. For proper operation of the frequency modulator, the sound subcarrier amplitude should be greater than 2 Vp-p.

Pin 14—Sound Supply: Pin 14 is the sound supply and C14 is an RF decouple capacitor. Decreasing C14 may result in increased supply interaction.

Printed Circuit Layout

Printed circuit board layout is critical in preventing RF feedthrough. The location of RF bypass capacitors on supply is very important. *Figure 4* shows an example of a properly layed out circuit board. It is recommended that this layout be used.

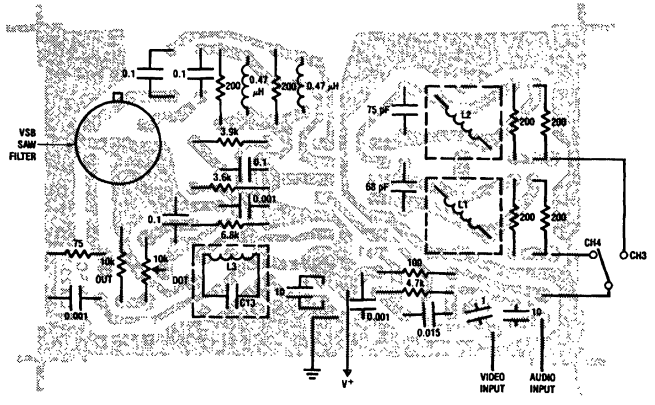

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FIGURE 4. Printed Circuit Board and Component Diagram (Component Side 1X)

Section 4

Motion Control

Section 4 Contents

***Devices Not Covered In Last Publication**

National Semiconductor Corporation

Motion Control Selection Guide

Dedicated Motor Control Functions

Part Number	Function	Features
LM621	Brushless D.C. Motor	Deadband Timer for Direction Reversal 40V Max. Operation 35 mA Outputs for Direct Drive of Bipolar Power Transistors
LM628	High Performance Position Control for D.C. and Brushless D.C. Motors	On Board 32-Bit Incremental Shaft Encoder Interface 256 μs Loop Time Automatic Trajectory Generator Velocity Programmable "On-the-Fly" Internal Programmable PID Filter Convenient 8-Bit Host Interface 8-Bit or 12-Bit Port to DAC (LM628) 8-Bit PWM Output (LM629)
LM622	P.W.M. Controller for Brushless and Brush D.C. Motors	Flexible Output Structure Drives H-Switches or Commutators Precision On-Board Reference Flexible Error Amp/Feedback Structure

H-Switches

Output Current (Amps)		Device	Supply Voltage (Max)	Full Current Saturation Voltage		Operating Temp. Range	Package	Description
Peak (Typical)	Continuous (Max)			Source (Max)	Sink (Max)			
4	2	LM18298	50	2.8	2.6	−40°C to +150°C	15-Pin TO-220	Quad ½ H Switch
1.5	1	LM18293	36	1.8	1.8	−40°C to +125°C	16-Pin DIP	Dual Full H Switch

Power Op-Amps*

Output Current Amps		Device	Supply Voltage (Max)	Input Offset Voltage (Max)	Quiescent Current	Slew Rate (Typical)	Operating Temp. Range	Package	Features
Peak (Typical)	Continous (Max)								
3	1.5	LM675	60	10 mV	50 mA	8 V/μs	0°C to +70°C	5-Pin TO-220	Thermal Parole
15	10	LM12L	60	15 mV	80 mA	9 V/μs	−55°C to +125°C	4-Pin TO-3	Fully Protected
15	10	LM12CL	60	20 mV	120 mA	9 V/μs	0°C to +70°C	4-Pin TO-3	Fully Protected
15	10	LM12	80	15 mV	80 mA	9 V/μs	−55°C to +125°C	4-Pin TO-3	Fully Protected
15	10	LM12C	80	20 mV	120 mA	9 V/μs	0°C to +70°C	4-Pin TO-3	Fully Protected
1	0.5	LM18272	28	100 mV	15 mA (Typ)	0.5 V/μs	0°C to +85°C	8-Pin DIP	Dual (Bridge)

*For more information on Power Amps, see the Amplifier section of the Linear Databook. For more High Power Amplifiers, refer to the Audio Amplifier section.

National Semiconductor Corporation

PRELIMINARY

LM621 Brushless Motor Commutator IC

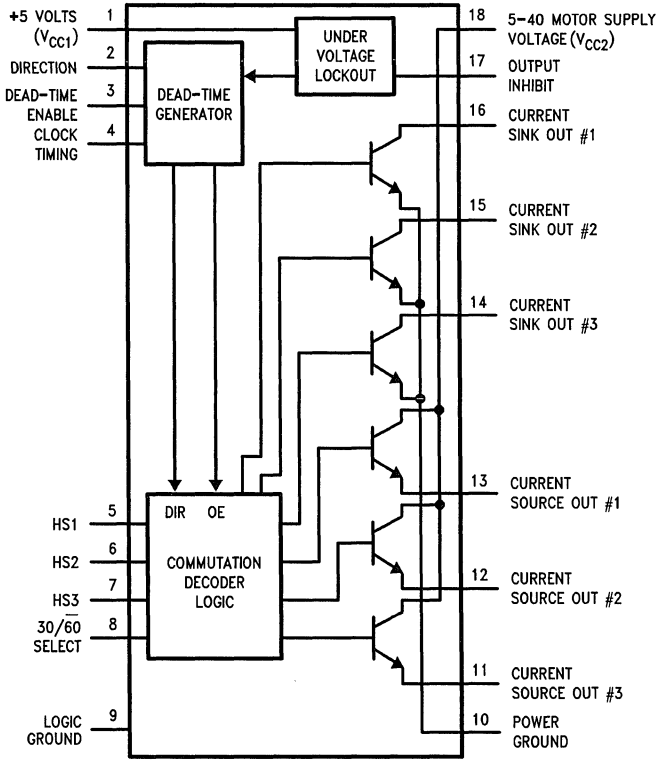
General Description

The LM621 is a bipolar IC designed for commutation of brushless DC motors. The part is compatible with both three- and four-phase motors. It can directly drive the power switching devices used to drive the motor. The LM621 provides an adjustable dead-time circuit to eliminate "shoot-through" current spiking in the power switching circuitry. Operation is from a 5V supply, but output swings of up to 40V are accommodated. The part is packaged in an 18-pin, dual-in-line package.

Features

- Adjustable dead-time feature eliminates current spiking
- On-chip clock oscillator for dead-time feature
- Outputs drive bipolar power devices (up to 35 mA base current) or MOSFET power devices
- Compatible with three- and four-phase motors . . .
  - — Bipolar drive to delta- or Y-wound motors
  - — Unipolar drive to center-tapped Y-wound motors
  - — Supports 30- and 60-degree shaft position sensor placements for three-phase motors
  - — Supports 90-degree sensor placement for four-phase motors
- Directly interfaces to pulse-width modulator output(s) via OUTPUT INHIBIT (PWM magnitude) and DIRECTION (PWM sign) inputs
- Direct interface to Hall sensors
- Outputs are current limited
- Undervoltage lockout

Connection Diagram



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Order Number LM621N
See NS Package Number N18A

Absolute Maximum Ratings (See Notes)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC1}	+7V
V_{CC2}	+45V
Logic Inputs (Note 1)	V_{CC1} +0.5V, −0.5V
Logic Input Clamp Current	20 mA
Output Voltages	+45V, −0.5V
Output Currents	Internally current limited

Operating Ambient Temperature Range LM621	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Susceptibility (Note 10)	2000V
Lead Temperature, N pkg. (Soldering, 4 sec.)	260°C

Electrical Characteristics (See Notes)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units
DECODER SECTION					
High Level Input Voltage					
HS1, HS2, HS3:			2.0	**2.0**	V min
30/$\overline{60}$ SELECT:			2.0	**2.0**	V min
High Level Input Current					
HS1, HS2, HS3:	$V_{IH} = V_{CC1}$		100	**200**	μA max
30/$\overline{60}$ SELECT:	$V_{IH} = V_{CC1}$		120	**240**	μA max
Low Level Input Voltage					
HS1, HS3 and HS2	30/$\overline{60}$ = 5V		0.6	**0.4**	V max
HS1, HS3 and HS2	30/$\overline{60}$ = 0V		0.6	**0.4**	V max
30/$\overline{60}$ Select	$H_{SI} = H_{S3}$ = 5V		0.6	**0.4**	V_{max}
Low Level Input Current					
HS1 and HS3:	V_{IL} = 0.35V		−400	**−600**	μA max
HS2:	V_{IL} = 0.4V		−100	**−200**	μA max
30/$\overline{60}$ SELECT	V_{IL} = 0.0V		−700	**−800**	μA max
Input Clamp Voltage	I_{in} = 1 mA	(V_{CC1} + 0.7)			V
(Pins 2, 3, 5, 6, 7, 8, 17)	I_{in} = −1 mA	(−0.6)			V
Output Leakage Current	Outputs Off				
Sinking Outputs	V_{CC2} = 40V, V_{OUT} = 40V	0.2		1.0	μA
Sourcing Outputs	V_{OUT} = 0V	−0.2		−1.0	μA
Short-Circuit Current	V_{CC2} = 10V,	50	35		mA min
Sinking Outputs	V_{OUT} = 10V				
Sourcing Outputs	V_{OUT} = 0V	−50	−35		mA min
V_{sat} (sinking)	I = 20 mA	0.83		1.00	V max
V_{drop} (sourcing) = ($V_{CC2} - V_{OUT}$)	I = −20 mA	1.7		2.00	V max
Output Rise Time	(sourcing) C_L < 10 pF	50			ns
Output Fall Time	(sinking) $C_L \leq$ 10 pF	50			ns
Propagation Delay (Hall Input to Output)	Dead-Time Off	200			ns

Electrical Characteristics (See Notes) (Continued)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units
DEAD-TIME SECTION					
High Level Input Voltage					
DIRECTION:	Pin 3 = 0V		2.0	**2.0**	V min
OUTPUT INHIBIT:			2.0	**2.0**	V min
DEAD-TIME ENABLE:	Pin 17 = 0V		2.0	**2.0**	V min
High Level Input Current	V_{in} = 5V				
DIRECTION:	Pin 3 = 0V		100	**150**	μA max
OUTPUT INHIBIT:			60	**100**	μA max
DEAD-TIME ENABLE:			200	**300**	μA max
Low Level Input Voltage					
DIRECTION:	Pin 3 = 0V		0.6	**0.4**	V max
OUTPUT INHIBIT:			0.6	**0.4**	V max
DEAD-TIME ENABLE:			0.3	**0.2**	V max
Low Level Input Current					
DIRECTION:	V_{in} = 0.6V		−100	**−150**	μA max
OUTPUT INHIBIT:	V_{in} = 0.6V		−60	**−100**	μA max
DEAD-TIME ENABLE:	V_{in} = 0V		−200	**−300**	μA max
Propagation Delays (Inputs to Outputs)	Dead-Time Off, (Pin 3 = 0V)				
OUTPUT INHIBIT		200			ns
DIRECTION		200			ns
Minimum Clock Period, T_{CLK} (Note 3)	R = 11 kΩ C = 200 pF	2.2			μs
Clock Accuracy f = 100 kHz	R = 30k C = 400 pF	±3			%
Minimum Dead-Time	Dead-Time Off	15			ns
Minimum Dead-Time	Dead-Time On	2			T_{CLK}
COMPLETE CIRCUIT					
Total Current Drains	Outputs Off				
I_{CC1}			10		mA min
I_{CC1}		15	22	**30**	mA max
I_{CC2}	V_{CC2} = 40V		2		mA min
I_{CC2}		3	6	**9**	mA max
Undervoltage Lockout V_{CC1}		3.6	3.0		V_{MAX}

Note 1. Unless otherwise noted ambient temperature (T_A) = 25°C.

Note 2. Unless otherwise noted: V_{CC1} = +5.0V, "recommended operating range V_{CC} = 4.5V to 5.5V" V_{CC2} = +10.0V, ambient temperature = 25°C.

Note 3. Clock oscillator period, T_{CLK} = RC, where T_{CLK} is in μs, R is in kΩ, and C is pF. Also see selection graph in Typical Characteristics for determining values of R and C. Note that the value of R should be no less than 11 kΩ and C no less than 200 pF.

Note 4. Tested limits are guaranteed and 100% production tested.

Note 5. Design limits are guaranteed (but not 100% production tested) at the indicated temperature and supply voltages. These limits are not used to calculate outgoing quality levels.

Note 6. Specifications in **boldface** apply over junction temperature range of −40°C to +85°C.

Note 7. Typical Thermal Resistances O_{JA} (see Note 8):

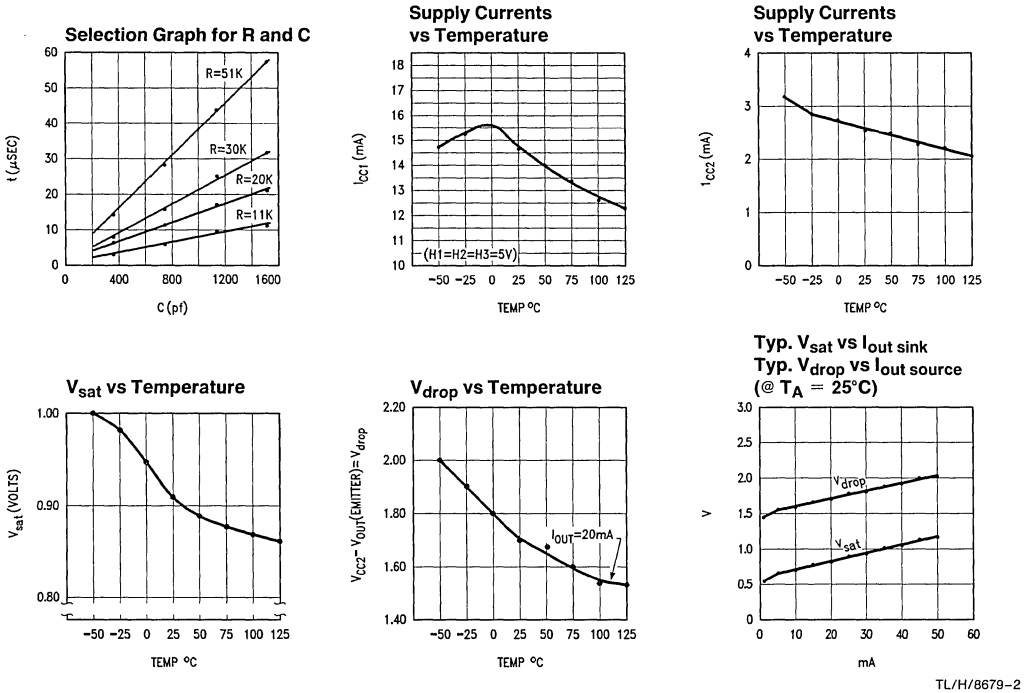
N pkg, board mounted	110°C/W
N pkg, socketed	118°C/W

Note 8. Package thermal resistance indicates the ability of the package to dissipate heat generated on the die. Given ambient temperature and power dissipation, the thermal resistance parameter can be used to determine the approximate operating junction temperature. Operating junction temperature directly effects product performance and reliability.

Note 9. This part specifically does not have thermal shutdown protection to avoid safety problems related to an unintentional restart due to thermal time constant variations. Care should be taken to prevent excessive power dissipation on the die.

Note 10: Human body model, 100 pF, discharged through a 1500Ω resistor.

Typical Performance Characteristics



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Description of Inputs and Outputs

Pin 1: V_{CC1} (+5V). The logic and clock power supply pin.

Pin 2: DIRECTION. This input determines the direction of rotation of the motor; ie., clockwise vs. counterclockwise. See truth table.

Pin 3: DEAD-TIME ENABLE. This input enables or disables the dead-time feature. Connecting +5V to pin 3 enables dead-time, and grounding pin 3 disables it. Pin 3 should not be allowed to float.

Pin 4: CLOCK TIMING. This pin provides for connecting an external resistor and capacitor to control the period of the clock oscillator, which determines the amount of dead-time. See *Figure 4* and text.

Pins 5 thru 7: HS1, HS2, and HS3 (Hall-sensor inputs). These inputs receive the rotor-position sensor inputs from the motor. Three-phase motors provide all three signals; four phase motors provide only two, one of which is connected to both HS2 and HS3.

Pin 8: 30/$\overline{60}$ SELECT. This input is used to select the required decoding for three-phase motors; ie, either "30-degree" (+5V) or "60-degree" (ground). Connect pin 8 to +5V when using a four-phase motor.

Pin 9: LOGIC GROUND. Ground for the logic power supply.

Pin 10: POWER GROUND. Ground for the output buffer supply.

Pins 11 thru 13: SOURCE OUTPUTS. The three current-sourcing outputs which drive the external power devices that drive the motor.

Pins 14 thru 16: SINK OUTPUTS. The three current-sinking outputs which drive the external power devices that drive the motor.

Pin 17: OUTPUT INHIBIT. This input disables the LM621 outputs. It is typically driven by the magnitude signal from an external sign/magnitude PWM generator. Pin 17 = +5V = outputs off.

Pin 18: V_{CC2} (+5 to +40V). This is the supply for the collectors of the three current-sourcing outputs (pins 11 thru 13). When driving MOSFET power devices, pin 18 may be connected to a voltage source of up to +40V to achieve sufficient output swing for the gate. When driving bipolar power devices, pin 18 should be connected to +5V to minimize on-chip power dissipation. Undervoltage lockout automatically shuts down all outputs if the V_{CC1} supply is too low. All outputs will be off if V_{CC1} falls below the undervoltage lockout voltage.

Functional Description

The commutation decoder receives Hall-sensor inputs HS1, HS2, and HS3 and a 30/$\overline{60}$ SELECT input. This block decodes the gray-code sequence to the required motor-drive sequence.

The dead-time generator monitors the DIRECTION input and inhibits the outputs (pins 11 thru 16) for a time sufficient to prevent current-spiking in the external power switches when the direction is reversed.

The six chip outputs drive external power switching devices which drive the motor. Three outputs source current; the remaining three sink current. The output transistors provide up to 50 mA outputs for driving devices, or up to 40V output swings for driving MOSFETs. The LM621 logic is powered from 5V.

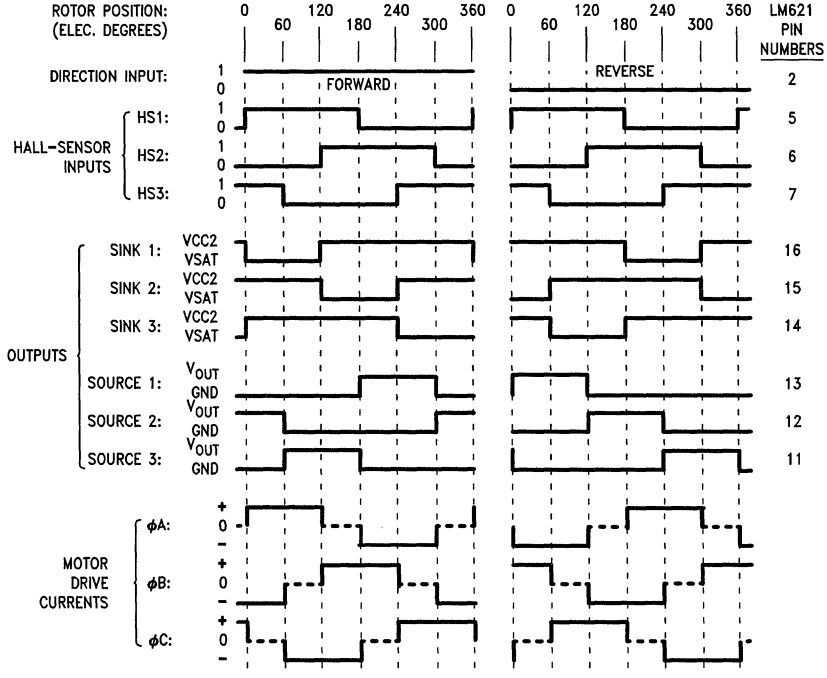
The undervoltage lockout section monitors the V_{CC} supply and if the voltage is not sufficient to permit reliable logic operation, the outputs are shutdown.

Three-Phase Motor Commutation

There are two popular conventions for establishing the relative phasing of rotor-position signals for three-phase motors. While usually referred to as 30-degree and 60-degree sensor placements, this terminology refers to mechanical degrees of sensor placement, not electrical degrees. The electrical angular resolution is the required 60 degrees in both cases. The phasing differences can be noted by comparing the sequences of HS1 through HS3 entries in Table I, LM621 Commutation Decoder Truth Table, which shows both the 30- and 60-degree phasings (and the 90-degree phasing for four-phase motors) and their required decoder logic truth tables, respectively. Table I shows the phasing (or codes) of the Hall-effect sensors for each 60-degree (electrical) position range of the rotor, and correlates these data to the commutator sink and source outputs required to drive the power switches. These phasings are common to several motor manufacturers. The 60-degree phasing is preferred to 30-degree phasing because the all-zeros and all-ones codes are not generated. The 60-degree phasing is more failsafe because the all-zeros and all-ones codes could be inadvertently generated by things like disconnected or shorted sensors.

Because the above terminology is not used consistently among all motor manufacturers, Table II, Alternative Sensor-phasing Names, will hopefully clarify some of the differences. Table II shows a different 60-degree phasing, and 120-, 240-, and 300-degree phasings. Comparison with Table I will show that these four phasings are essentially shifted and/or reversed-order versions of those used with the LM621.

Figure 1 shows the waveforms associated with the commutation decoder logic for a motor which has 60-degree rotor-position phasing, along with the generated motor-drive waveforms. As can be seen in the drawing, Hall-effect sensor signals HS1 through HS3 are separated by 60 electrical degrees, which is the required angular resolution for three-phase motors.



TL/H/8679–6

FIGURE 1. Commutation Waveforms for 60-degree Phasing

Three-Phase Motor Commutation (Continued)

TABLE I. LM621 Commutation Decoder Truth Table

Sensor Phasing	Position Range	Sensor Inputs			Sink Outputs			Source Outputs		
		HS1	HS2	HS3	1	2	3	1	2	3
30 deg	0–60	0	0	0	ON	off	off	off	ON	off
	60–120	0	0	1	ON	off	off	off	off	ON
	120–180	0	1	1	off	ON	off	off	off	ON
	180–240	1	1	1	off	ON	off	ON	off	off
	240–300	1	1	0	off	off	ON	ON	off	off
	300–360	1	0	0	off	off	ON	off	ON	off
60 deg	0–60	1	0	1	ON	off	off	off	ON	off
	60–120	1	0	0	ON	off	off	off	off	ON
	120–180	1	1	0	off	ON	off	off	off	ON
	180–240	0	1	0	off	ON	off	ON	off	off
	240–300	0	1	1	off	off	ON	ON	off	off
	300–360	0	0	1	off	off	ON	off	ON	off
90 deg	0–90	0	1	HS2	off	na	off	off	na	ON
	90–180	0	0	HS2	ON	na	off	off	na	off
	180–270	1	0	HS2	off	na	ON	off	na	off
	270–360	1	1	HS2	off	na	off	ON	na	off
Pin Numbers:		5	6	7	16	15	14	13	12	11

Note 1: The above outputs are generated when the Direction input, pin 2, is logic high. For reverse rotation (pin 2 logic low), the above sink and source output states become exchanged.

Note 2: For four-phase motors sink and source outputs number two (pins 15 and 12) are not used; hense the "na" (not applicable) in the appropriate columns above. *Figure 6* shows how the required sink and source outputs for four-phase motors are derived.

TABLE II. Alternative Sensor-Phasing Names

Alternate Phasing	Position Range	Sensor Inputs			Corresponding LM621 Position Range and/or Comments
		HS1	HS2	HS3	
"60 deg"	0–60	0	0	0	Same as 30-degree phasing, but in reverse order; i.e., only change is relative direction.
	60–120	1	0	0	
	120–180	1	1	0	
	180–240	1	1	1	
	240–300	0	1	1	
	300–360	0	0	1	
"120 deg"	0–60	0	0	1	Same as 60-degree phasing, but with shifted order of position ranges; i.e., only change is relative phasing of sensor signals.
	60–120	1	0	1	
	120–180	1	0	0	
	180–240	1	1	0	
	240–300	0	1	0	
	300–360	0	1	1	
"240 deg"	0–60	0	1	0	Same comment as above for "120 deg" phasing.
	60–120	1	1	0	
	120–180	1	0	0	
	180–240	1	0	1	
	240–300	0	0	1	
	300–360	0	1	1	
"300 deg"	0–60	0	1	1	Same as 30-degree phasing, but with shifted order of position ranges, i.e., only change is relative phasing of sensor signals.
	60–120	1	1	1	
	120–180	1	1	0	
	180–240	1	0	0	
	240–300	0	0	0	
	300–360	0	0	1	

Four-Phase Motor Commutation

Four-phase motors use a 90-degree (quadrature) rotor-position sensor phasing. This phasing scheme is also shown in Table I. LM621 Commutation Decoder Truth Table. As shown in Table I, the 90-degree phasing has only two rotor-position-sensor signals, HS1 and HS2. When using the LM621 to run a four-phase motor the HS2 signal is connected to both the HS2 and HS3 chip inputs.

Dead-Time Feature

The DEAD-TIME ENABLE input is used to enable this feature (by connecting +5V to pin 3). The reason for providing this feature is that the external power switches are usually totem-pole structures. Since these structures switch heavy currents, if either totem-pole device is not completely turned off when its complementary device turns on, heavy "shoot-through" current spiking will occur. This situation occurs when the motor DIRECTION input changes (when all output drive polarities reverse), at which time device turn-off delay can cause the undesired current spiking.

Figure 2 shows the logic of the dead-time generator. The dead-time generator includes an RC oscillator to generate a required clock. Pin 4 (CLOCK TIMING) is used to connect an external resistor and capacitor to control the frequency of this oscillator. The clock frequency should be adjusted so that two periods of oscillation just slightly exceed the worst-case turn-off time of the power switching devices. As shown by the graph in Typical Peformance Characteristics, the time of one clock period (in μs) is approximately RC (R in kΩ and C in pF); the period can be measured with an oscilloscope at pin 4. The dead-time generator function monitors the DIRECTION input for changes, synchronizes the direction changes with the internal clock, and inhibits the chip outputs for two clock periods.

Flip-flops FF1 through FF3 form a three-bit, shift-register delay line, the input of which is the DIRECTION input. The flip-flops are the only elements clocked by the internal clock generator. The shift register outputs must all have the same state in order to enable gate G1 or G2, one of which must be enabled to enable the chip outputs. As soon as a direction change input is sensed at the output of FF1, gates G1 and G2 will be disabled, thereby disabling the drive to the power switches for a time equal to two clock periods.

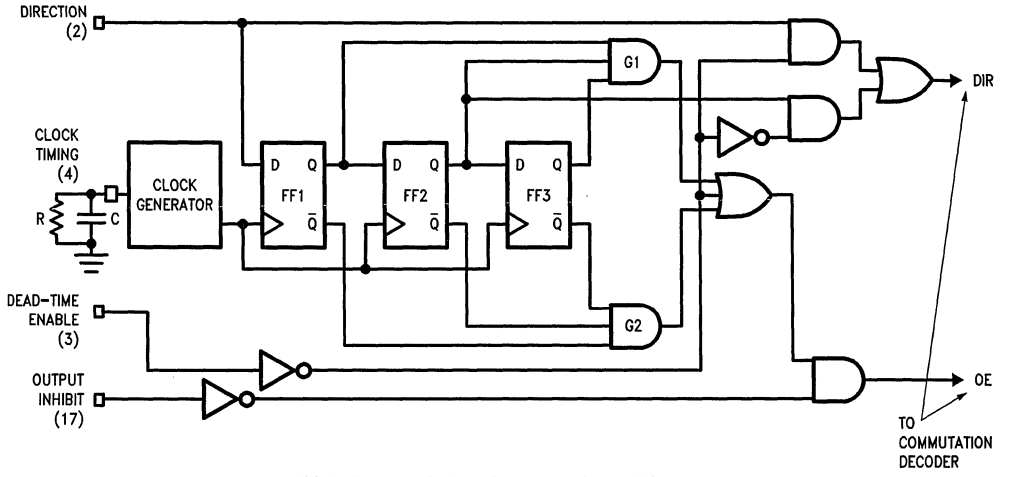


FIGURE 2. Dead-Time Generator Logic Diagram

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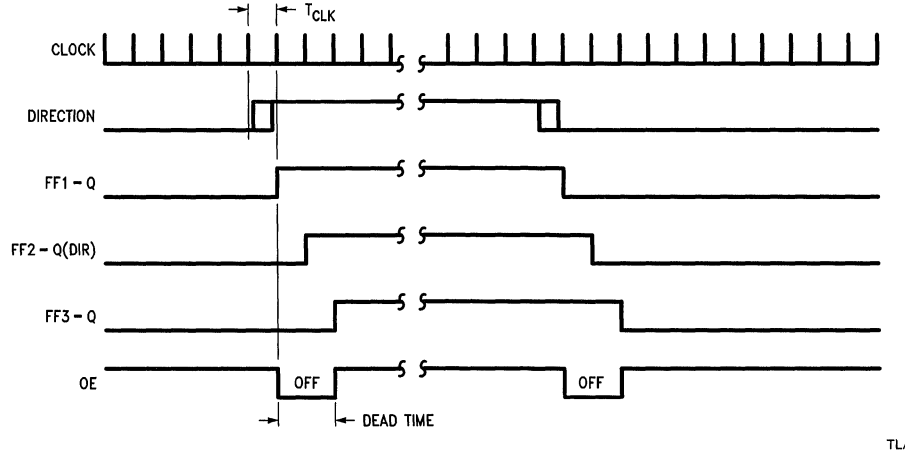

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FIGURE 3. Dead-Time Generator Waveforms

Dead-Time Feature (Continued)

Dead-time is defined as the time the outputs are blanked off (to prevent shoot-through currents) after a direction change input. See *Figure 3*. It can be seen that the dead-time is two clock periods. Since the dead-time scheme introduces delay into the system feedback control loop, which could impact system performance or stability, it is important that the dead-time be kept to a minimum. From *Figure 3* it can be seen that the time between a direction change signal and the initiation of output blanking can vary up to one clock period due to asynchronous nature of the clock and the direction signal.

Typical Applications

THREE-PHASE EXAMPLES

Figure 4 is a typical LM621 application. This circuitry is for use with a three-phase motor having 30-degree sensor phasing, as indicated by connection of the 30/$\overline{60}$ SELECT input, pin 8, to a logic "1" (+5V). The same connection of the DEAD-TIME ENABLE input, pin 3, enables this feature.

Typical power switches and a simple implementation of an overcurrent sensing circuit are also detailed in *Figure 4*. This application example assumes a device turn-off time of about 4.8 μs maximum, as evidenced by the choice or R and C. See Typical Performance Characteristics. The choice of RC should be made such that two periods are at least equal to the maximum device turn-off time.

The choice of the value for R_{limit} (the resistors which couple the LM621 outputs to the power switches) depends on the input current requirements of the power switching devices. These resistors should be chosen to provide only the amount of current needed by the device inputs, up to 50 mA (typical). The resistors minimize the dissipation incurred by the LM621. Although *Figure 4* shows the 5–40V supply (pin 18) connected to the motor supply voltage, this was done only to emphasize the ability of the part to provide up to 40V output swings. For the bipolar power switches shown, connecting pin 18 to a 5V supply would reduce on-chip power dissipation. Driving FET power switches, however, may require connecting pin 18 to a higher voltage. *Figure 5* is the three-phase application built with MOSFET power-switching components. Note that since the output V_{drop} (sourcing) is at least 1.5V, V_{CC2} can be chosen to avoid overdriving the MOSFET gates.

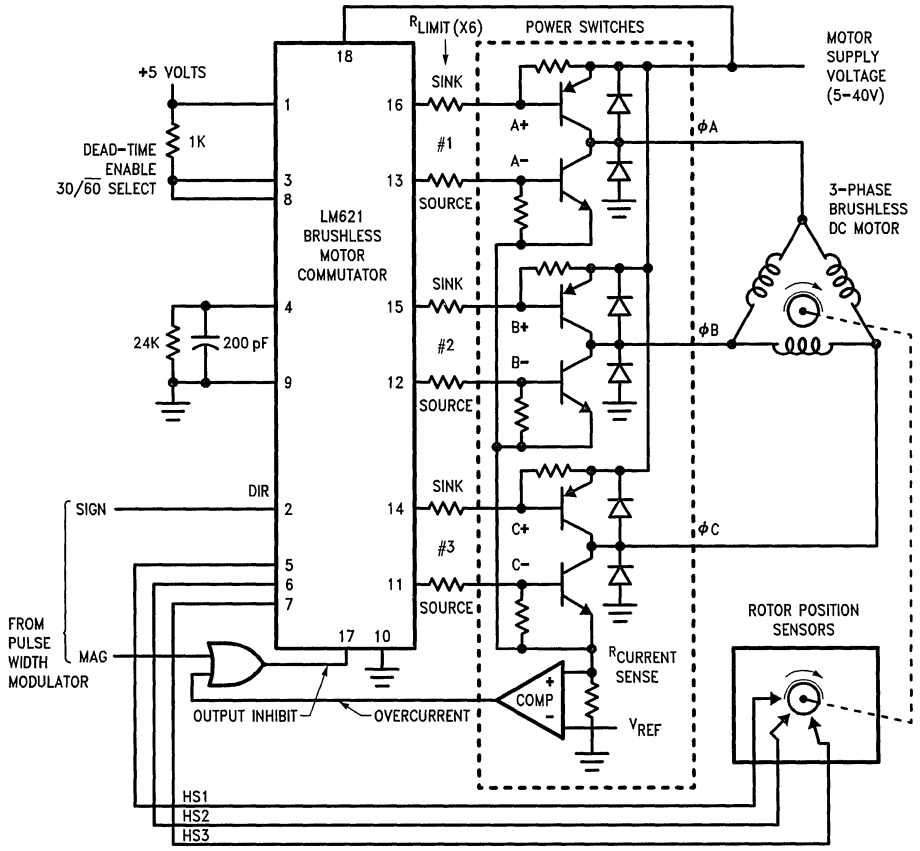

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FIGURE 4. Commutation of Three-Phase Motor (Bipolar Switches)

Typical Applications (Continued)

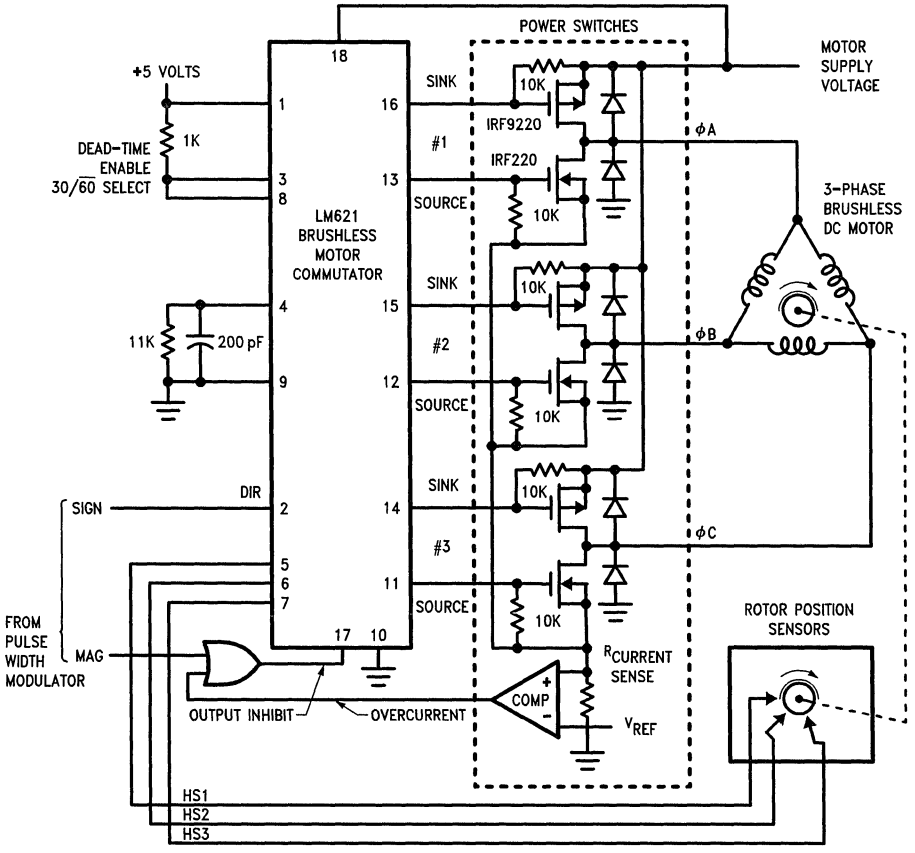

FIGURE 5. Commutation of Three-Phase Motor (MOSFET Switches)

Typical Applications (Continued)

FOUR-PHASE EXAMPLE

Figure 6 is typical of the circuitry used to commutate a four-phase motor using the LM621. This application is seen to differ from the three-phase application example in that the LM621 outputs are utilized differently. Four-phase motors require four-phase power switches, which in turn require the commutator to provide four current-sinking outputs and four current sourcing outputs. The 18-pin package of the LM621 facilitates only three sinking and three sourcing outputs. The schematic shows the 30/$\overline{60}$ SELECT input in the 30-degree select state (pin 8 high) and rotor-position sensor inputs HS2 and HS3 connected together. This connection truncates the number of possible rotor-position input states to four, which is consistent with the 90-degree quadrature rotor-position signals provided by four-phase motors. With the LM621 outputs connected as shown, this approach provides the needed power-switch drive signals for a four-phase motor. Note that only four of the six LM621 outputs (SINK #1 and #3, and SOURCE #1 and #3) are used directly, and that these are also inverted to form the remaining four. SINK #2 and SOURCE #2 outputs are not used.

HALF-WAVE DRIVE EXAMPLE

The previous applications examples involved delta-configured motor windings and full-wave operation of the motor. The application shown in *Figure 7* differs in that it features half-wave operation of a motor with the windings in a Y-configuration. This approach is suitable for automotive and other applications where only low-voltage power supplies are conveniently available. The advantage of this power-switching scheme is that there is only one switch-voltage drop in series with the motor winding, thereby conserving more of the available voltage for application to the motor winding. Half-wave operation provides only unidirectional current to the windings; in contrast to the bidirectional currents applied by the previous full-wave examples.

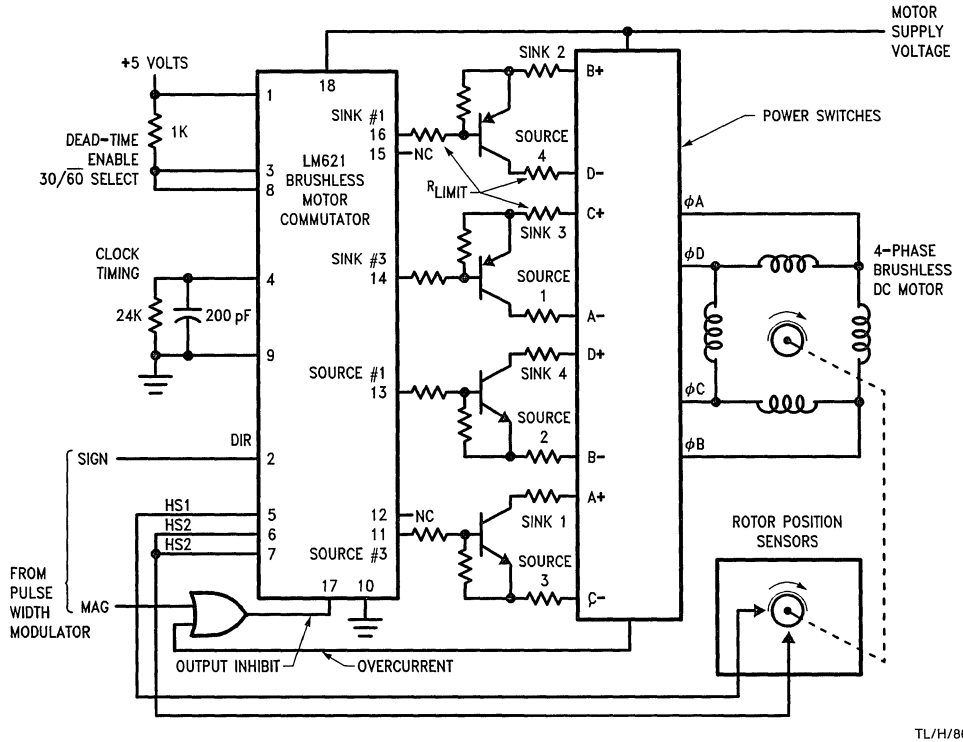

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FIGURE 6. Commutation of Four-Phase Motor

Typical Applications (Continued)

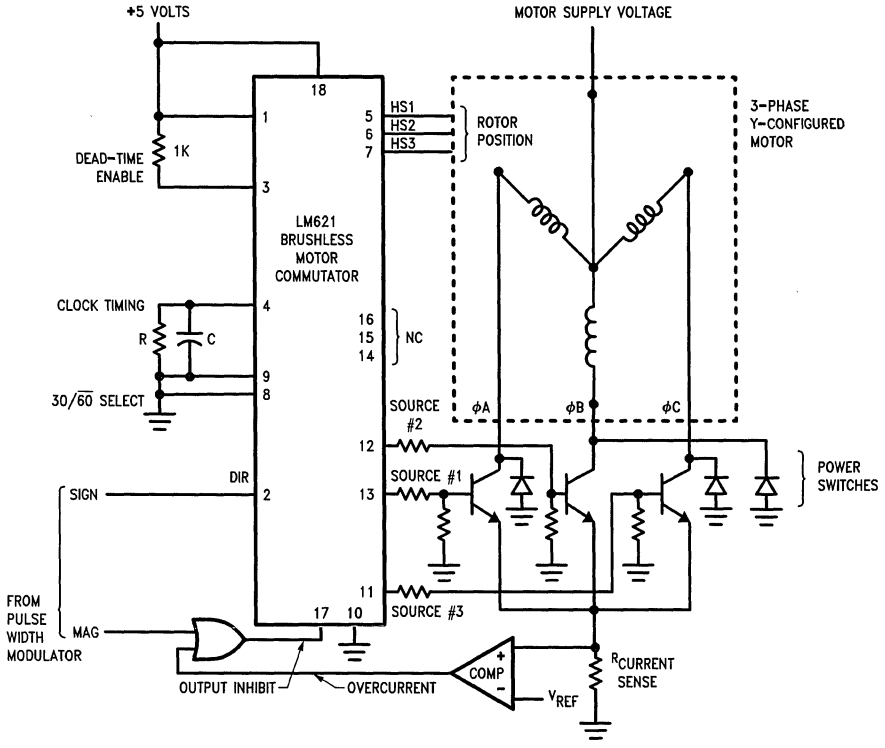

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FIGURE 7. Half-Wave Drive of Y-Configured Motor

National Semiconductor Corporation

ADVANCED INFORMATION

LM622 Pulse Width Modulator

General Description

The LM622 is a Pulse-Width-Modulator circuit designed for control of DC brush type and brushless motors. For control of brushless motors, the LM622 must be used with a commutator chip such as the LM621. It can be used for unidirectional and bidirectional drive circuits. Other applications for this flexible chip include amplifiers and switching regulators.

The chip consists of a general purpose Op Amp, three comparators followed by three latches, a triangle waveform oscillator, a ±1% precision bandgap reference and a pulse-by-pulse current limit. The protection circuitry consists of under-voltage lockout, thermal shutdown or soft-start options.

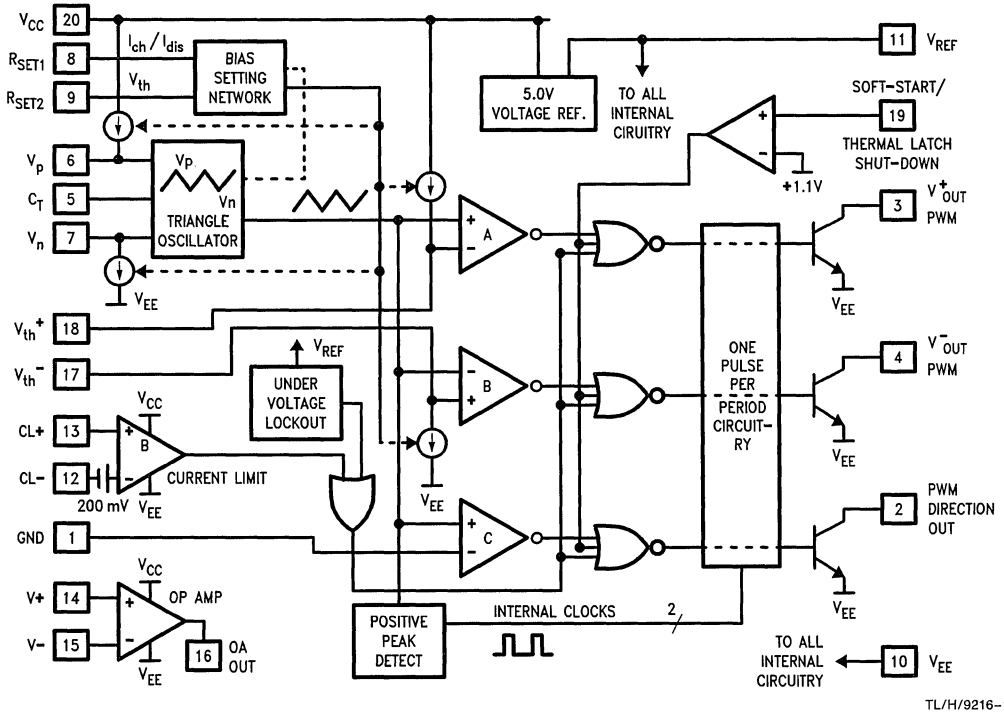
The Op Amp will generate an error voltage which will be added to the ramp voltage. The floating triangular waveform that results is compared to user programmable threshold voltages in the comparators. The signals from the comparators are gated by protection circuitry before reaching open-collector outputs. PWM signals are thus available to drive top side and bottom side switches, and to provide a direction signal.

The three comparator outputs are active low, with 20 mA current sinking capability.

Features

- Single or Dual Supply Operation
- ±4.5 to ±20V or 9.0 to 40V Input Supply Range
- Three Comparators with Open Collector Outputs
- 5.0 Volt Bandgap Reference Trimmed to ±1%
- Shutdown or Soft-Start
- Thermal Limit Latch
- Undervoltage Lockout
- 50 Hz to 350 kHz Oscillator Range
- Pulse-By-Pulse Current Limit Amplifier with Wide Common-Mode Range

LM622 Functional Block and Connection Diagram



TL/H/9216–1

National Semiconductor Corporation

ADVANCED INFORMATION

LM628 Precision Motion Controller

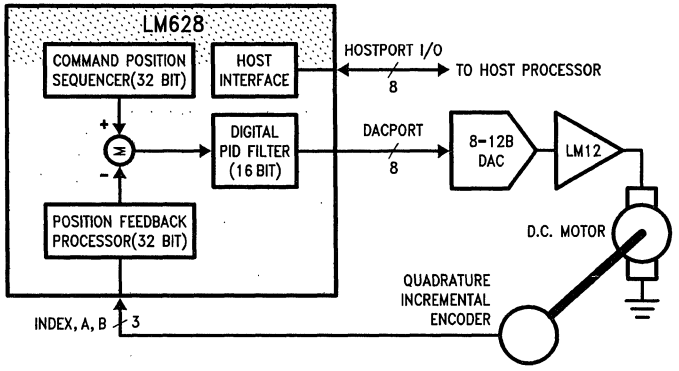
General Description

The LM628* is a dedicated processor for motion control. It can fully manage a position servo loop including quadrature feedback decoding, desired profile generation, comparison of desired position with actual position, compensation filtering of resulting error signal, and finally output of appropriate control signal to power amplifier driving the motor. Motor position is sampled and outputs generated at programmable intervals of 256 μs to 4096 μs. The LM628 has a digital programmable PID (proportional integral derivative) filter for compensating motor response. Output data is available as either 8 or 12 bits wide and is sent to a DAC via an 8-bit DAC-port. Commands and data are sent to the LM628 via an 8-bit host-port. The host can also use this port to read information from the LM628. The LM628 can be programmed to interrupt the host processor when error conditions occur and send back information about itself and the motor. All programming is done with commands that relate specifically to motion control, making the LM628 easy to use.

Features

- Programmable sample period (256 μs to 4096 μs)
- Internal trapezoidal velocity profile generator
- 12-bit or 8-bit DAC output data
- Programmable digital PID filter with 16-bit coefficients
- 32-bit position register
- 32-bit velocity register
- 32-bit acceleration register
- Quadrature incremental shaft encoder interface
- 8-bit parallel asynchronous host communication
- Operates at 8 MHz clock frequency
- TTL Compatible
- Filter coefficients can be updated during motion
- Velocity and target position can be updated during motion

Block Diagram



TL/H/9219-1

*LM628 incorporates the SDA core processor and SDA cells designed by SDA Systems

National Semiconductor Corporation

PRELIMINARY

LM18293 Four Channel Push Pull Driver

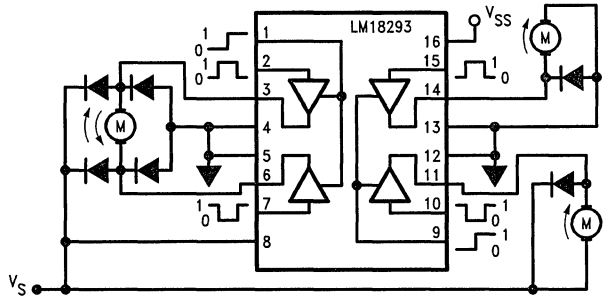
General Description

The LM18293 is designed to drive DC loads up to one amp. Typical applications include driving such inductive loads as solenoids, relays and stepper motors along with driving switching power transistors and use as a buffer for low level logic signals. The four inputs accept standard TTL and DTL levels for ease of interfacing. Two enable pins are provided that also accept the standard TTL and DTL levels. Each enable controls 2 channels and when an enable pin is disabled (tied low), the corresponding outputs are forced to the TRI-STATE® condition. If the enable pins are not connected (i.e., floating), the circuit will function as if it has been enabled. Separate pins are provided for the main power supply (pin 8), and the logic supply (pin 16). This allows a lower voltage to be used to bias up the logic resulting in reduced power dissipation. The chip is packaged in a specially designed 16 pin power DIP. The 4 center pins of this package are tied together and form the die paddle inside the package. This provides much better heat sinking capability than most other DIP packages available. The device is capable of operating at voltages up to 36 volts.

Features

- 1A output current capability per channel
- Pin for pin replacement for L293B
- Special 16 pin power DIP package
- 36 volt operation
- Internal thermal overload protection
- Logical "0" input voltage up to 1.5 volts results in high noise immunity

Typical Connection



TL/H/8706–1

FIGURE 1. Application circuit showing bidirectional and on/off control of a single DC motor using two outputs and unidirectional on/off function of two DC motors using a single output each.

Order Number LM18293N
NS Package Number N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Output Drive Supply Voltage (V_S)	36V
Logic Supply Voltage (V_{SS})	36V
Input Voltage (V_I)	7V
Enable Voltage (V_E)	7V
Peak Output Current (Non-Repetitive t = 5 ms)	2A
Junction Temperature (T_J)	+150°C
Thermal Resistance Junction to Case (θ_{JC})	14°C/W
Thermal Resistance Junction to Ambient (θ_{JA})	80°C/W
Internal Power Dissipation	Internally Limited
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Solder 10 seconds)	260°C

Electrical Characteristics

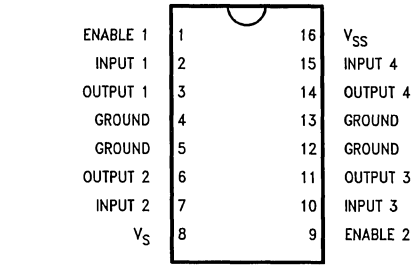
V_S = 24V, V_{SS} = 5V, T = 25°C, L = 0.4V, H = 3.5V, each channel, unless otherwise noted

Symbol	Parameter	Conditions	Typical	Tested Limit (Note 1)	Design Limit (Note 2)	Units
V_S	Main Supply (Pin 8)	Maximum Supply Voltage		36		Vmax
V_{SS}	Logic Supply (Pin 16)	Minimum Logic Supply Voltage		4.5		Vmin
		Maximum Logic Supply Voltage		36		Vmax
I_S	Total Quiescent Supply Current	V_I = L I_O = 0 V_E = H	2	6		mAmax
		V_I = H I_O = 0 V_E = H	16	24		mAmax
		V_E = L		4		mAmax
I_{SS}	Total Quiescent Logic Supply Current (pin 16)	V_I = L I_O = 0 V_E = H	44	60		mAmax
		V_I = H I_O = 0 V_E = H	16	22		mAmax
		V_E = L	16	24		mAmax
V_I	Input Voltage	Min Value of Low		−0.3		Vmin
		Max Value of Low		1.5		Vmax
		Min Value of High		2.3		Vmin
		Max Value of High ($V_{SS} \leq 7$)		V_{SS}		Vmax
		Max Value of High ($V_{SS} > 7$)		7		Vmax
I_I	Input Current	V_I = L		−10		μAmax
		V_I = H	30	100		μAmax
V_E	Enable Voltage (Pins 1, 9)	Min Value of Low		−0.3		Vmin
		Max Value of Low		1.5		Vmax
		Min Value of High		2.3		Vmin
		Max Value of High ($V_{SS} \leq 7$)		V_{SS}		Vmax
		Max Value of High ($V_{SS} > 7$)		7		Vmax
I_E	Enable Current	V_E = L	−30	−100		μAmax
		V_E = H		±10		μAmax
V_{CE} sat Top	Source Saturation Voltage	I_o = −1 amp	1.4	1.8		Vmax
V_{CE} sat Bottom	Sink Saturation Voltage	I_o = 1 amp	1.2	1.8		Vmax
t_r	Rise Time	10%–90% V_o	250			ns
t_f	Fall Time	90%–10% V_o	250			ns
t_{on}	Turn-On Delay	50% V_I to 50% V_o	450			ns
t_{off}	Turn-Off Delay	50% V_I to 50% V_o	200			ns

Note 1: Tested limits are guaranteed and 100% production tested.

Note 2: Design limits are guaranteed (but not 100% production tested) over the full supply and temperature range. These limits are not used to calculate outgoing quality levels.

Connection Diagram



Enable 1 activates outputs 1 & 2
Enable 2 activates outputs 3 & 4

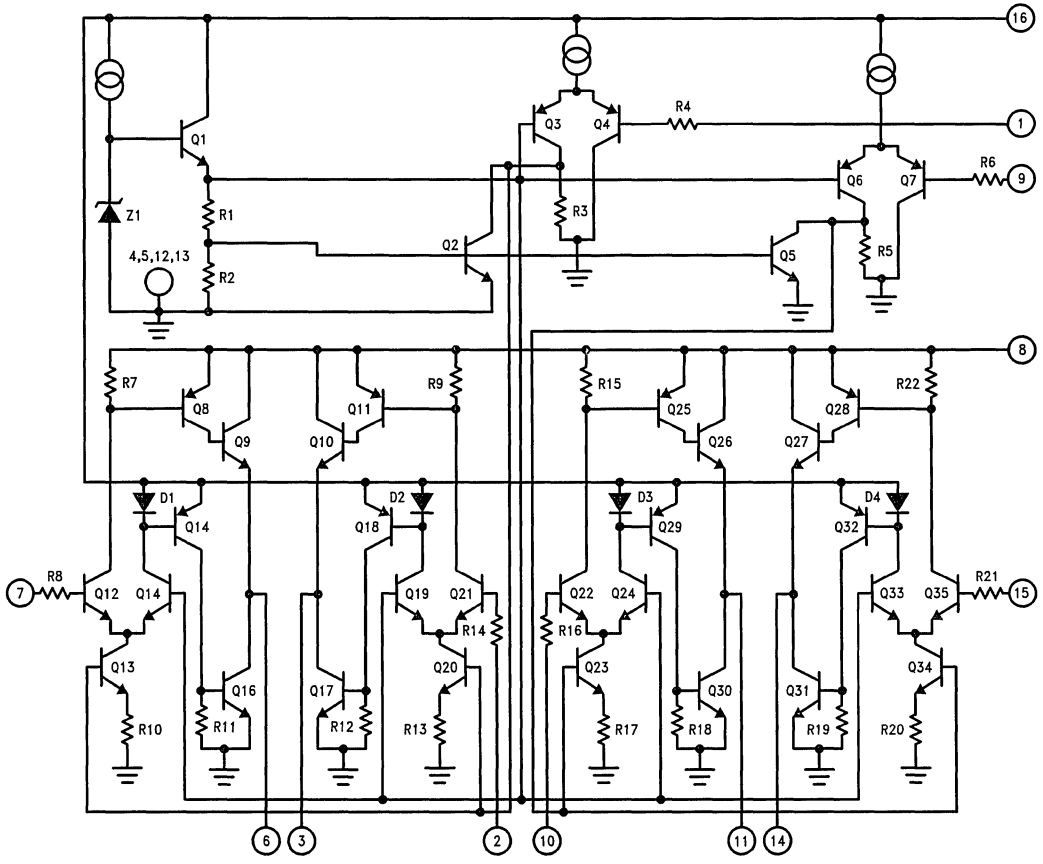
TL/H/8706–2

Input/Output Truth Table

V_E (**)	V_I (Each Channel)	V_O
H	H	H
H	L	L
L	H	X (*)
L	L	X (*)

(*) High output impedance.
(**) Relative to the pertinent channel.

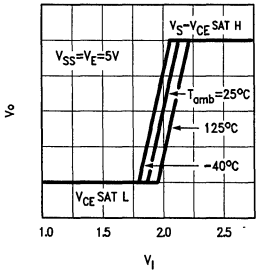
Simplified Schematic



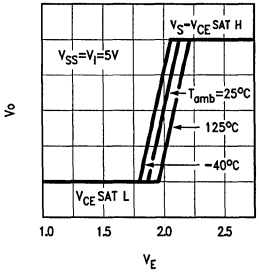
TL/H/8706–3

Typical Performance Characteristics V_S In all cases = 24V

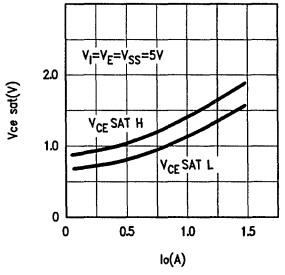
Output Voltage vs. Input Voltage



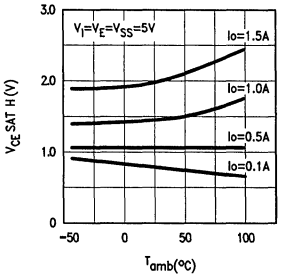
Output Voltage vs. Enable Voltage



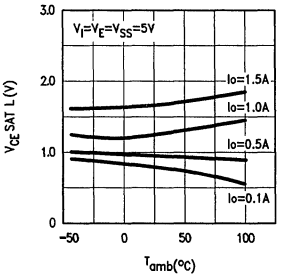
Saturation Voltage vs. Output Current



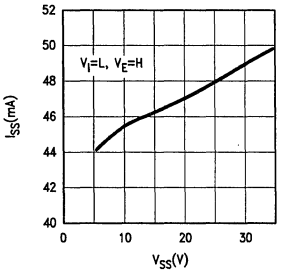
Source Saturation Voltage vs. Ambient Temperature



Sink Saturation Voltage vs. Ambient Temperature



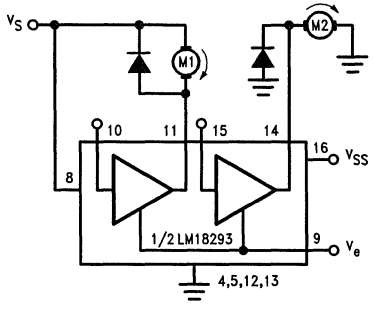
Quiescent Logic Supply Current vs. Logic Supply Voltage



TL/H/8706–4

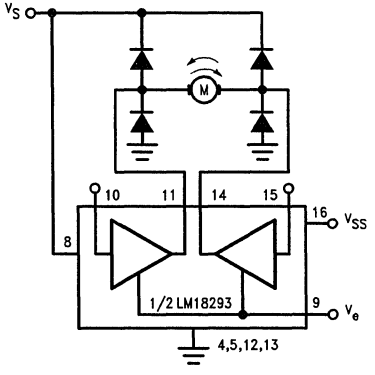
Typical Applications

DC motor controls (with connections to ground and to the supply voltages)



TL/H/8706–5

Bidirectional DC motor control



TL/H/8706–6

V_E	Pin 10	Pin 15	M1	M2
H	H	H	Fast Motor Stop	Run
H	H	L	Fast Motor Stop	Fast Motor Stop
H	L	H	Run	Run
H	L	L	Run	Fast Motor Stop
L	X	X	Free Running Motor Stop	Free Running Motor Stop

L = Low H = High X = Don't care

Inputs		Function
V_E = H	Pin 10 = H Pin 15 = L	Turn CW
	Pin 10 = L Pin 15 = H	Turn CCW
	Pin 10 = Pin 15	Fast Motor Stop
V_E = L	Pin 10 = X Pin 15 = X	Free Running Motor Stop

L = Low H = High X = Don't care

Bipolar Stepping Motor Control

Step Sequencing Tables

Full Step *

V_{IN} 1	V_{IN} 2	Step
L	L	1
L	H	2
H	H	3
H	L	4
L	L	1

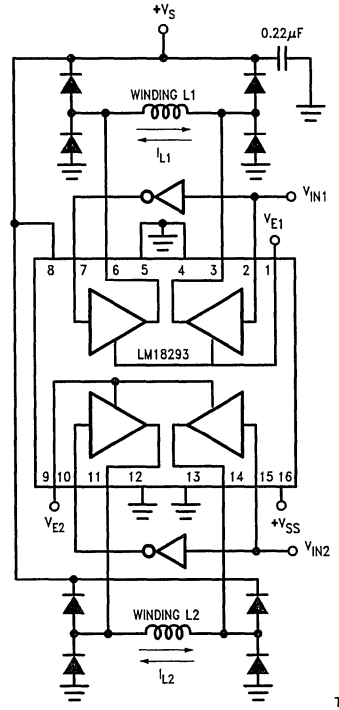
*V_E 1 and V_E 2 = H

Half Step

V_E 1	V_E 2	V_{IN} 1	V_{IN} 2	Step
H	L	L	X	1
H	H	L	L	2
L	H	X	L	3
H	H	H	L	4
H	L	H	X	5
H	H	H	H	6
L	H	X	H	7
H	H	L	H	8
H	L	L	X	1

H = High L = Low X = Don't care

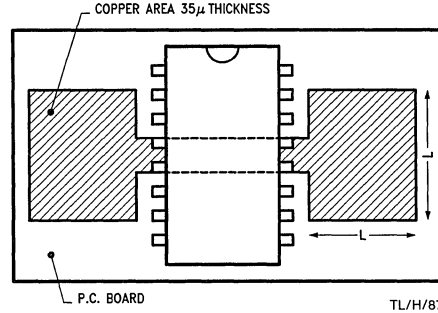
Motor Control Block Diagram



TL/H/8706-7

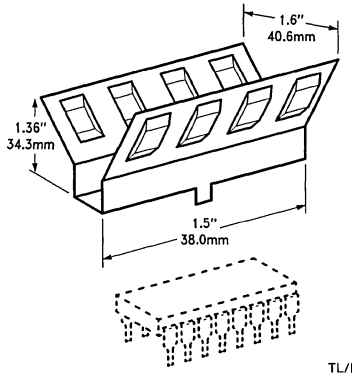
Mounting Instructions

The junction to ambient thermal resistance of the LM18293 can be reduced by soldering the ground pins to a suitable copper area of the printed circuit board or to an external heatsink. The graph below, which shows the maximum power dissipated and junction to ambient thermal resistance as a function of the side "l" of two equal square copper areas having a thickness of 35μ, illustrates this. In addition, it is possible to use an external heatsink (see illustration below). During soldering the pins temperature must not exceed 230°C and the soldering time must not be longer than 12 seconds. The external heatsink or printed circuit copper area must be connected to electrical ground.



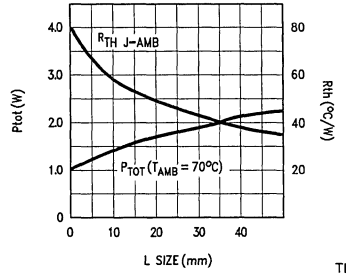
TL/H/8706-8

Staver External Heat-sink



TL/H/8706-10

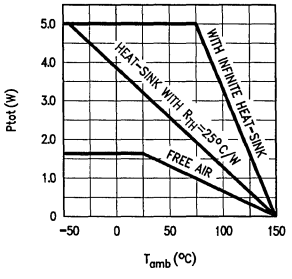
Maximum power dissipated and junction to ambient thermal resistance vs. size



TL/H/8706-9

Mounting Instructions (Continued)

Maximum allowable power dissipation vs. ambient temperature



TL/H/8706–11

National Semiconductor Corporation

ADVANCED INFORMATION

LM18298 Dual Full-Bridge Driver

General Description

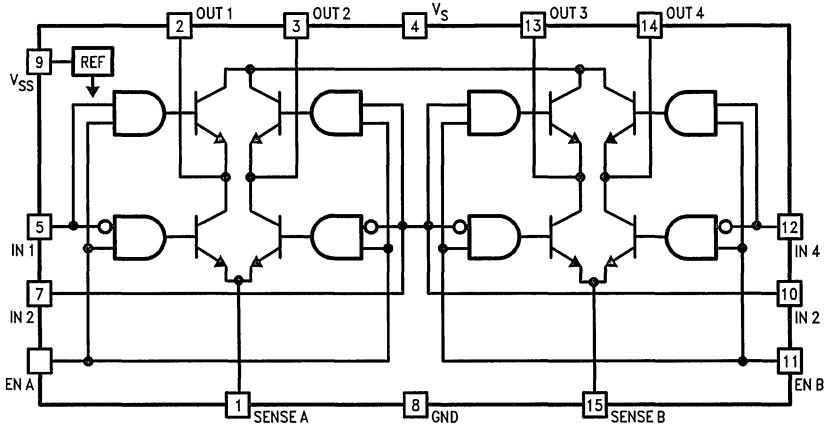
The LM18298 is a high voltage, high current dual full-bridge driver designed to accept standard TTL logic levels and drive inductive loads such as relays, solenoids, DC and stepping motors. Two inhibit inputs are provided to disable the device independently of the input signals.

The emitters of the lower transistors of each bridge are connected together and the corresponding external terminal can be used for the connection of an external sensing resistor. An additional supply input is provided so that the logic works at lower voltage.

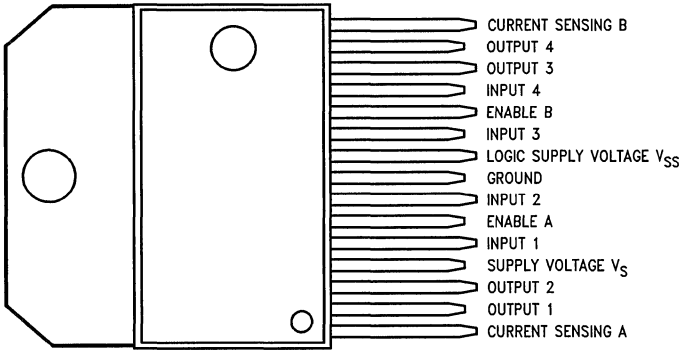
Features

- Power supply voltage up to 46V
- Total DC current up to 4A
- Low saturation voltage
- Over-temperature protection
- Logical "0" input voltage up to 1.5V (High noise immunity)

Block & Connection Diagrams



TL/H/9302–1



TL/H/9302–2

Section 5

Special Functions

Section 5 Contents

***Devices Not Covered In Last Publication**

National Semiconductor Corporation

Building Blocks

Communications-Related Building Blocks

Modulators & Demodulators Selection Guide

	LM1211	LM1496	LM1889	LM2889
Typical Application	Broadband Demodulator	Balanced Modulator-Demodulator	TV Video Modulator	TV Video Modulator
Key Features	• Configurable for AM or FM Based Signals • 0 MHz–70 MHz Operating Frequency Range • 25 MHz Detector Output Bandwidth • Linear Output Phase Response	• Wide Frequency Response to 100 MHz • Fully Balanced Inputs and Outputs • Adjustable Gain and Signal Handling	• Input Signals —Audio Modulation —Color Difference —Luminance • Channel 3 (61.25 MHz) or Channel 4 (67.25 MHz) Output • Companion Circuit to LM1886 TV Video Matrix D to A	• Input Signals —Audio —Composite Video • Channel 3 (61.25 MHz) or Channel 4 (67.25 MHz) Output • Video DC Restoration

PLL's AND TONE DECODERS

General purpose PLL's and tone decoders are available for applications that include FSK demodulation, tone decoding, SAP and SCA demodulation, and telemetry reception. Both bipolar and CMOS devices are offered. Special purpose PLL's for TV synchronization and FM stereo demodulation are also available for use in other low frequency signal processing applications.

PLL and Tone Decoder Selection Guide

	LM565	LM567	LMC567* (CMOS LM567)	LMC568	LM1391	LM1800, LM1870, LM4500A
Typical Application	PLL	Tone Decoder	Tone Decoder	PLL	TV—Horizontal PLL	FM Stereo Demodulator PLL
Center Frequency Range	15 Hz–500 kHz	0.01 Hz–500 kHz	0.01 Hz–500 kHz	0.01 Hz–500 kHz		
VCO Control Range	±30%	±7%	±7%	±30%	±300 Hz	
Supply Voltage	±5V to ±12V	4.75V–9V	2V–9V	2V–9V	8V–9.2V	Lowest: 7V Highest: 16V (See Datasheets)
Supply Current (Typ)	8 mA	12 mA	0.8 mA	1.2 mA	20 mA	Lowest: 21 mA Highest: 45 mA (See Datasheet)

*The CMOS LMC567 oscillator runs at twice the frequency of the bipolar LM567 oscillator. Refer to the datasheets for additional information.

POWER LINE CARRIER

The LM2893/LM1893 Carrier-Current Transceiver performs as a power line interface for half-duplex (bi-directional) communication of serial bit streams of virtually any coding. Applications include energy management systems, inter-office control, fire alarm systems, security systems, telemetry, and remote meter reading.

TIMERS

General purpose timers are available for generating accurate time delays or oscillation. Both bipolar and CMOS devices are offered.

Timer Selection Guide

	LM322	LM2905	LM555	LMC555* (CMOS LM555)	LM556 (Dual LM555)
Trigger Pulse Relative to Output Pulse	Can Be Longer	Can Be Longer	Must Be Shorter	Must Be Shorter	Must Be Shorter
Typical Application	Monostable	Monostable	Astable	Astable	Astable
Supply Voltage	4.5V–40V	4.5V–40V	4.5V–15V	1.2V–12V	4.5V–15V
Supply Current (Typical)	2.5 mA	2.5 mA	10 mA	0.15 mA	10 mA (Each Timer Section)

*The CMOS LMC555 can handle −10 mA to +50 mA of output current and the bipolar LM555 can handle up to ±200 mA of output current.

VCO AND FUNCTION GENERATOR

The LM566 is a general purpose voltage controlled oscillator which may be used to generate square and triangle waves. Typical applications include FM modulation, signal generation, function generation, frequency shift keying, and tone generation. The LM566 has very linear modulation characteristics.

Drive-Related Building Blocks

DISPLAY DRIVERS

LED flasher/oscillator and dot/bar display drivers are offered.

Display Driver Selection Guide

	LM3909	LM3914	LM3915	LM3916
Typical Application	Flasher/ Oscillator	Dot/Bar Display Driver	Dot/Bar Display Driver	Dot/Bar Display Driver
Display Scale	N/A	Linear	Log	VU Meter
Display Type	LED, Incandescent	LED, LCD, Vacuum Fluorescent	LED, LCD, Vacuum Fluorescent	LED, LCD, Vacuum Fluorescent

METER DRIVERS

The LM1819 Air-Core Meter Driver is a function generator/driver for air-core (moving-magnet) meter movements in tachometers and ruggedized instruments. Driver outputs are self-centering and better than 2% linearity is guaranteed over a full 305° deflection range. Signal conditioning circuitry is included on chip.

TEMPERATURE CONTROLLER

The LM3911 (Note 1) is a temperature controller containing a precision temperature sensor, op amp, and reference. It is designed for temperature sensing and closed loop temperature control applications over the −25°C to +85°C range.

Note 1: See Linear 2 for datasheet.

Precision-Related Building Blocks

CHOPPER BLOCK

The LMC669 Auto Zero Block (Note 1) is a universal commutating auto-zero block that can be used with any operational amplifier to correct offset voltage.

Note 1: See Linear 2 for datasheet.

TRANSISTOR ARRAYS

A variety of matched and power transistors are offered.

Transistor Array Selection Guide

	LM394	LM395	LM3046	LM3146
Description	NPN Transistor Pair	Power Transistor	5 NPN Transistors	5 NPN Transistors
Key Features	• Emitter-Base Voltage Matched to 50 μV • Current Gain Matched to 2%	• Collector Current: 1A • Quiescent Current: 10 mA • Switching Time: 2 μs • Current Limit • Thermal Limit • Safe Area Protection	• Emitter-Base Voltage Matched to ±5 mV • Breakdown Voltages —$V_{(BR)(CBO)}$: 20V —$V_{(BR)(CEO)}$: 15V —$V_{(BR)(CIO)}$: 20V —$V_{(BR)(EBO)}$: 5V • DC—120 MHz	• Emitter-Base Voltage Matched to ±5 mV • Breakdown Voltages —$V_{(BR)(CBO)}$: 40V —$V_{(BR)(CEO)}$: 30V —$V_{(BR)(CIO)}$: 40V —$V_{(BR)(EBO)}$: 5V • DC—120 MHz

Sensing-Related Building Blocks

LIQUID LEVEL SENSORS

A variety of liquid level sensing circuits are offered.

Liquid Level Sensor Selection Guide

	LM903	LM1042	LM1812	LM1830
Output Type	Digital HI/LO	Analog	Pulse-Echo Timing	Digital HI/LO
Operation Method	Thermoresistive Probe	Thermoresistive Probe	Acoustic Transducer	Conductive Liquid

SPECIAL AMPLIFIERS

A variety of special sensor amplifiers are offered.

Special Amplifiers Selection Guide

	LM1815	LM1964
Typical Application	Adaptive Sense Amplifier	Sensor Interface Amplifier
Sensor	Inductive Pickup	Lambda Sensor
Key Features	• Operates from 2.5V to 12V Supply • Adaptive Hysteresis • True Zero Crossing Timing Reference	• Normal Operation Guaranteed with Inputs up to 3V Below Ground on a Single Supply • Fully Protected Inputs • Input Open Circuit Detection

SPECIAL COMPARATOR

The LM1801 Battery Operated Power Comparator is an extremely low power comparator with a high current, open collector output stage. Typical applications include intrusion alarms, water leak detectors, gas leak detectors, overvoltage crowbars and battery operated monitors. The LM1801 is designed to operate in a standby mode for 1 year, powered by a 9V alkaline battery.

SPECIAL CONVERTERS

A variety of special converters for signal transformation applications are offered.

Special Converters Selection Guide

	LH0091 (Note 1)	LH0094 (Note 1)	LM331 (Note 1)	LM2907, LM2917
Converter Type	True RMS-to-DC	Multifunction	Voltage-to-Frequency	Frequency-to-Voltage
Key Features	• 0.1% Accuracy with External Trim • Uncommitted Amplifier for Filtering, Gain or High Crest Factor Configuration • True RMS Conversion	• $OUT = IN_Y\left(\frac{IN_Z}{IN_X}\right)^m$, $0.1 \leq m \leq 10$, m Continuously Adjustable • Applications —Precision Divider, Multiplier —Square Root —Square —Trigonometric Function Generator —Companding —Linearization —Control Systems —Log Amp	• 1 Hz to 100 kHz Frequency Range • Split or Single Supply Operation	• Operates Relay, Lamp or Other Load when Input Exceeds a Selected Rate • Ground Referenced Tachometer Fully Protected from Damage Due to Swings Above Supply or Below Ground

Note 1: See Linear 2 for datasheets.

ULTRASONIC TRANSCEIVER

The LM1812 Ultrasonic Transceiver is a general purpose ultrasonic transceiver designed for use in a variety of ranging, sensing, and communications applications. Typical uses include liquid level measurement, sonar, surface profiling, data links, hydro-acoustic communications, non-contact sensing and industrial process control. Depending on the acoustic transducer, typical performance capabilities include 5 feet to 100 feet in water and 4 inches to 35 feet in air.

National Semiconductor Corporation

LM122/LM322/LM2905/LM3905 Precision Timers

General Description

The LM122 series are precision timers that offer great versatility with high accuracy. They operate with unregulated supplies from 4.5V to 40V while maintaining constant timing periods from microseconds to hours. Internal logic and regulator circuits complement the basic timing function enabling the LM122 series to operate in many different applications with a minimum of external components.

The output of the timer is a floating transistor with built in current limiting. It can drive either ground referred or supply referred loads up to 40V and 50 mA. The floating nature of this output makes it ideal for interfacing, lamp or relay driving, and signal conditioning where an open collector or emitter is required. A "logic reverse" circuit can be programmed by the user to make the output transistor either "on" or "off" during the timing period.

The **trigger** input to the LM122 series has a threshold of 1.6V independent of supply voltage, but it is fully protected against inputs as high as ±40V—even when using a 5V supply. The circuitry reacts only to the rising edge of the trigger signal, and is immune to any trigger voltage during the timing periods.

An internal 3.15V regulator is included in the timer to reject supply voltage changes and to provide the user with a convenient reference for applications other than a basic timer. External loads up to 5 mA can be driven by the regulator. An internal 2V divider between the reference and ground sets the timing period to 1 RC. The timing period can be voltage controlled by driving this divider with an external source through the V_{ADJ} pin. Timing ratios of 50:1 can be easily achieved.

The comparator used in the LM122 utilizes high gain PNP input transistors to achieve 300 pA typical input bias current over a common mode range of 0V to 3V. A **boost** terminal allows the user to increase comparator operating current for timing periods less than 1 ms. This lets the timer operate over a 3 μs to multi-hour timing range with excellent repeatability.

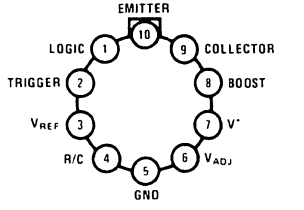
The LM122 operates over a temperature range of −55°C to +125°C. An electrically identical LM322 is specified from 0°C to +70°C. The LM2905/LM3905 are identical to the LM122 series except that the **boost** and V_{ADJ} pin options are not available, limiting minimum timing period to 1 ms.

Features

- Immune to changes in trigger voltage during timing interval
- Timing periods from microseconds to hours
- Internal logic reversal
- Immune to power supply ripple during the timing interval
- Operates from 4.5V to 40V supplies
- Input protected to ±40V
- Floating transistor output with internal current limiting
- Internal regulated reference
- Timing period can be voltage controlled
- TTL compatible input and output

Connection Diagrams

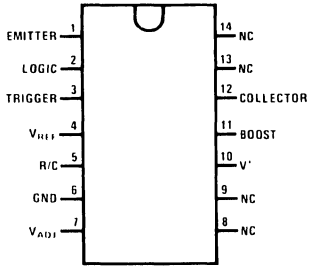
Metal Can Package



TL/H/7768–6

Top View
Order Number LM122H or LM322H
See NS Package Number H10C

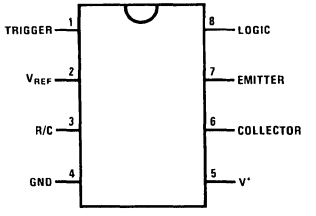
Dual-In-Line Package



TL/H/7768–7

Top View
Order Number LM322N
See NS Package Number N14A

Dual-In-Line Package



TL/H/7768–8

Top View
Order Number LM2905N or LM3905N
See NS Package Number N08B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation	500 mW
V^+ Voltage	40V
Collector Output Voltage	40V
V_{REF} Current	5 mA
Trigger Voltage	±40V
V_{ADJ} Voltage (Forced)	5V
Logic Reverse Voltage	5.5V
Output Short Circuit Duration (Note 1)	
Lead Temperature (Soldering, 10 sec.)	260°C
Operating Temperature Range	
LM122	$-55°C \le T_A \le +125°C$
LM322	$0°C \le T_A \le +70°C$
LM2905	$-40°C \le T_A \le +85°C$
LM3905	$0°C \le T_A \le +70°C$

Electrical Characteristics (Note 2)

Parameter	Conditions	LM122			LM322			LM2905/LM3905			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Timing Ratio	$T_A = 25°C$, $4.5V \le V^+ \le 40V$	0.626	0.632	0.638	0.620	0.632	0.644	0.620	0.632	0.644	
	Boost Tied to V^+, (Note 3)	0.620	0.632	0.644	0.620	0.632	0.644				
Comparator Input Current	$T_A = 25°C$, $4.5V \le V^+ \le 40V$		0.3	1.0		0.3	1.5		0.5	1.5	nA
	Boost Tied to V^+		30	100		30	100				nA
Trigger Voltage	$T_A = 25°C$, $4.5V \le V^+ \le 40V$	1.2	1.6	2	1.2	1.6	2	1.2	1.6	2	V
Trigger Current	$T_A = 25°C$, $V_{TRIG} = 2V$		25			25			25		μA
Supply Current	$T_A \ge 25°C$, $4.5V \le V^+ \le 40V$		2.5	4		2.5	4.5		2.5	4.5	mA
Timing Ratio	$4.5V \le V^+ \le 40V$	0.62		0.644	0.61		0.654	0.61		0.654	
	Boost Tied to V^+	0.62		0.644	0.61		0.654				
Comparator Input Current	$4.5V \le V^+ \le 40V$	−5		5	−2		2	−2.5		2.5	nA
	Boost Tied to V^+, (Note 4)			100			150				nA
Trigger Voltage	$4.5V \le V^+ \le 40V$	0.8		2.5	0.8		2.5	0.8		2.5	V
Trigger Current	$V_{TRIG} = 2.5V$			200			200			200	μA
Output Leakage Current	$V_{CE} = 40V$			1			5			5	μA
Capacitor Saturation Voltage	$R_t \ge 1\ M\Omega$		2.5			2.5			2.5		mV
	$R_t = 10\ k\Omega$		25			25			25		mV
Reset Resistance			150			150			150		Ω
Reference Voltage	$T_A = 25°C$	3	3.15	3.3	3	3.15	3.3	3	3.15	3.3	V
Reference Regulation	$0 \le I_{OUT} \le 3\ mA$		20	50		20	50		20	50	mV
	$4.5V \le V^+ \le 40V$		6	25		6	25		6	25	mV
Collector Saturation Voltage	$I_L = 8\ mA$		0.25	0.4		0.25	0.4		0.25	0.4	V
	$I_L = 50\ mA$		0.7	1.4		0.7	1.4		0.7	1.4	V
Emitter Saturation Voltage	$T_A = 25°C$, $I_L = 3\ mA$		1.8	2.2		1.8	2.2		1.8	2.2	V
	$T_A = 25°C$, $I_L = 50\ mA$		2.1	3		2.1	3		2.1	3	V
Average Temperature Coefficient of Timing Ratio			0.003			0.003			0.003		%/°C
Minimum Trigger Width	$V_{TRIG} = 3V$		0.25			0.25			0.25		μs

Note 1: Continuous output shorts are not allowed. Short circuit duration at ambient temperatures up to 40°C may be calculated from $t = 120/V_{CE}$ seconds, where V_{CE} is the collector to emitter voltage across the output transistor during the short.

Note 2: These specifications apply for $T_{AMIN} \le T_A \le T_{AMAX}$ unless otherwise noted.

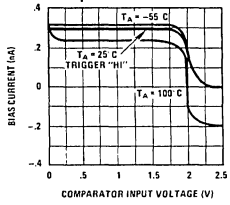
Note 3: Output pulse width can be calculated from the following equation: $t = (R_t)(C_t)[1 - 2(0.632 - r) - V_C/V_{REF})$ where r is timing ratio and V_C is capacitor saturation voltage. This reduces to $t = (R_t)(C_t)$ for all but the most critical applications.

Note 4: Sign reversal may occur at high temperatures (> 100°C) where comparator input current is predominately leakage. See typcial curves.

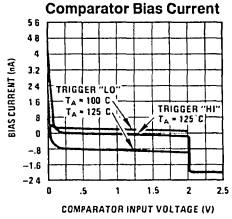
Note 5: Refer to RETS122X drawing of military LM122H version for specifications.

Typical Performance Characteristics

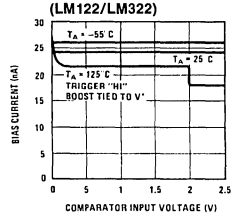
Comparator Bias Current



Comparator Bias Current



Comparator Bias Current (LM122/LM322)



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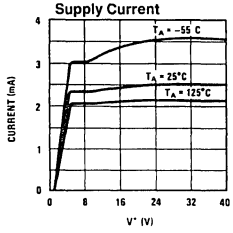
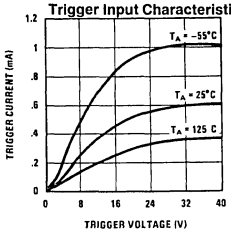
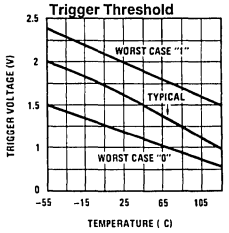
Supply Current



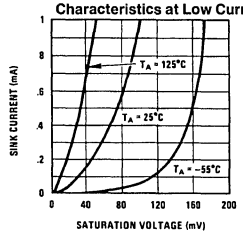
Trigger Input Characteristics



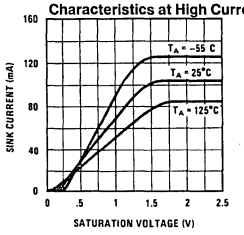
Trigger Threshold



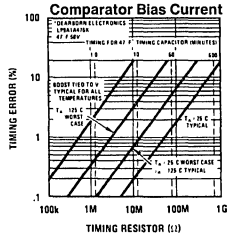
Output Transistor Saturation Characteristics at Low Currents



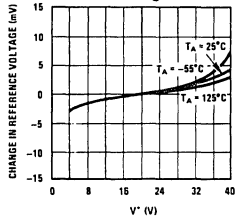
Collector Output Saturation Characteristics at High Current



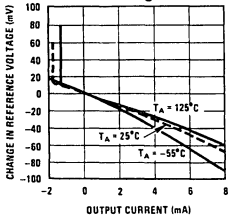
Timing Error Due to Comparator Bias Current



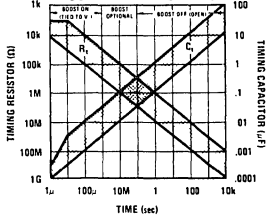
Reference Regulation



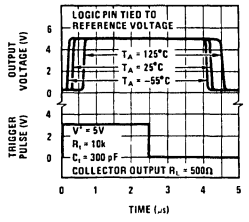
Reference Regulation



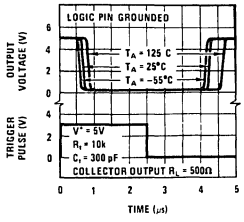
Suggested Timing Components



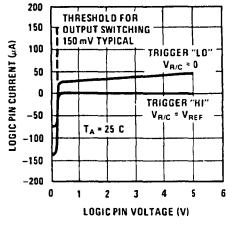
Short Output Pulse (LM122/LM322)



Short Output Pulse (LM122/LM322)



Logic Pin Characteristics



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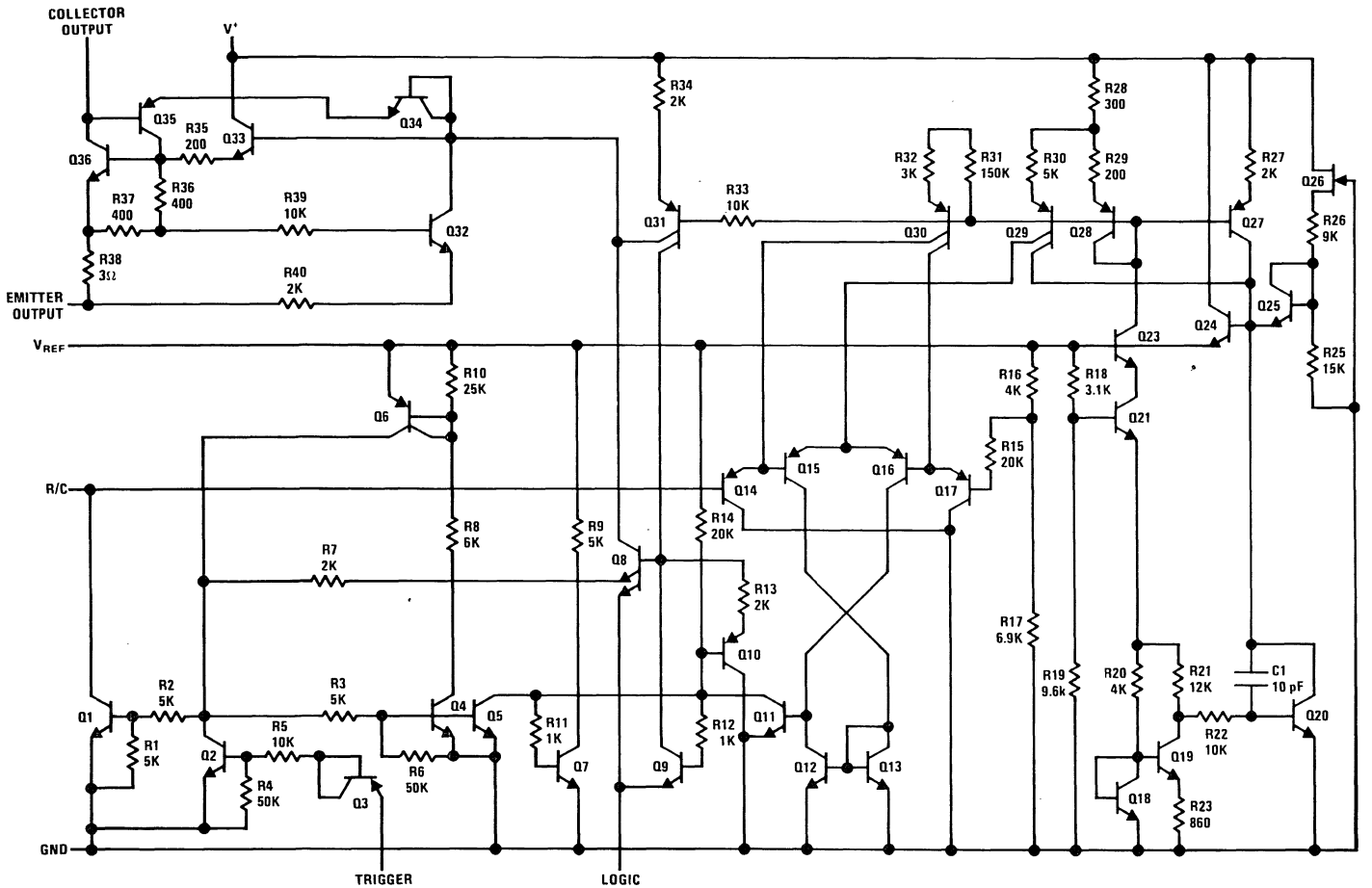
Schematic Diagram



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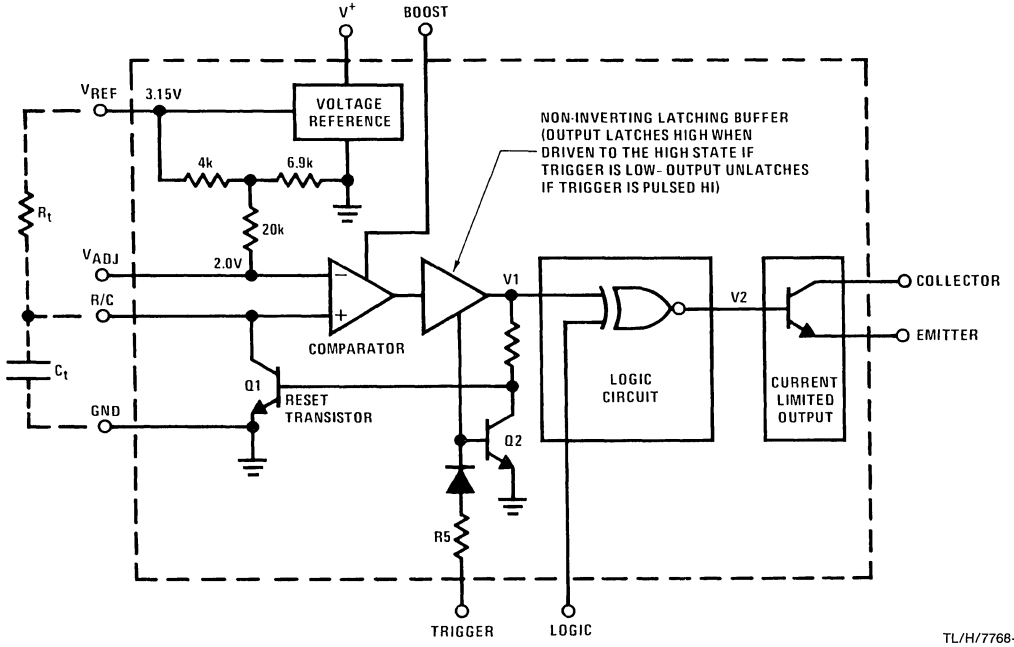
Functional Diagram



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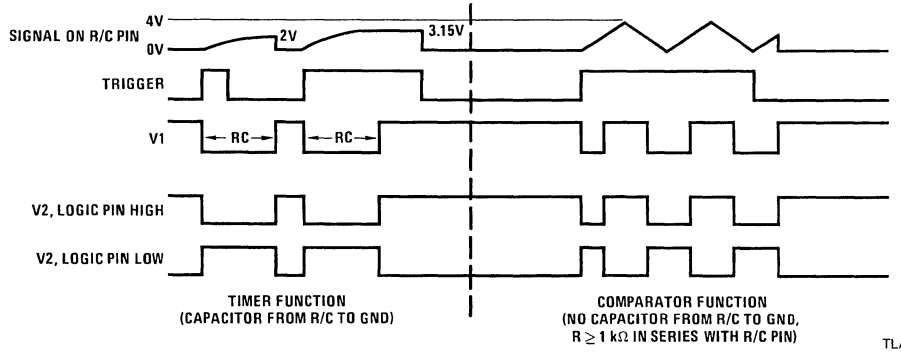
Timing Diagram



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Pin Function Description

One of the main features of the LM122 is its great versatility. Since this device is unique, a description of the functions and limitations of each pin is in order. This will make it much easier to follow the discussion of the various applications presented in this note.

V^+ is the positive supply terminal of the LM122. When using a single supply, this terminal may be driven by any voltage between 4.5V and 40V. The effect of supply variations on timing period is less than 0.005%/V, so supplies with high ripple content may be used without causing pulse width changes. Supply bypassing on V^+ is not generally needed but may be necessary when driving highly reactive loads.

Quiescent current drawn from the V^+ terminal is typically 2.5 mA, independent of the supply voltage. Of course, additional current will be drawn if the reference is externally loaded.

The V_{REF} pin is the output of a 3.15V series regulator referenced to the ground pin. Up to 5.0 mA can be drawn from this pin for driving external networks. In most applications the timing resistor is tied to V_{REF}, but it need not be in situations where a more linear charging current is required. The regulated voltage is very useful in applications where the LM122 is not used as a timer; such as switching regulators, variable reference comparators, and temperature con-

Pin Function Description (Continued)

trollers. Typical temperature drift of the reference is less than 0.01%/°C.

The **trigger** terminal is used to start a timing cycle (see functional diagram). Initially, Q1 is saturated, C_t is discharged and the latching buffer output (V1) is latched high. A trigger pulse unlatches the buffer, V1 goes low and turns Q1 off. The timing capacitor C_t connected from R/C to GND will begin to charge. When the voltage at the R/C terminal reaches the 2.0V threshold of the comparator, the comparator toggles, latching the buffer output (V1) in the high state. This turns on Q1, discharges the capacitor C_t and the cycle is ready to begin again.

If the **trigger** is held high as the timing period ends, the comparator will toggle and V1 will go high exactly as before. However, V1 will not be latched and the capacitor will not discharge until the trigger again goes low. When the trigger goes low, V1 remains high but is now latched.

Trigger threshold is typically 1.6V at 25°C and has a temperature dependence of −5.0 mV/°C. Current drawn from the **trigger** source is typically 20 μA at threshold, rising to 600 μA at 30V, then leveling off due to FET action of the series resistor, R5. For negative input trigger voltages, the only current drawn is leakage in the nA region. The **trigger** can be driven from supplies as high as ±40V, even when device supply voltage is only 5V.

The **R/C** pin is tied to the non-inverting side of the comparator and to the collector of Q1. Timing ends when the voltage on this pin reaches 2.0V (1 RC time constant referenced to the 3.15V regulator). Q1 turns on only if the trigger voltage has dropped below threshold. In comparator or regulator applications of the timer, the trigger is held permanently high and the **R/C** pin acts just like the input to an ordinary comparator. The maximum voltages which can be applied to this pin are +5.5V and −0.7V. Current from the **R/C** pin is typically 300 pA when the voltage is negative with respect to the V_{ADJ} terminal. For higher voltages, the current drops to leakage levels. In the boosted mode, input current is typically 30 nA. Gain of the comparator is very high, 200,000 or more, depending on the state of the logic reverse pin and the connection of the output transistor.

The **ground** pin of the LM122 need not necessarily be tied to system ground. It can be connected to any positive or negative voltage as long as the supply is negative with respect to the V^+ terminal. Level shifting may be necessary for the input **trigger** if the **trigger** voltage is referred to system ground. This can be done by capacitive coupling or by actual resistive or active level shifting. One point must be kept in mind; the emitter output must not be held above the **ground** terminal with a low source impedance. This could occur, for instance, if the emitter were grounded when the **ground** pin of the LM122 was tied to a negative supply.

The terminal labled V_{ADJ} is tied to one side of the comparator and to a voltage divider between V_{REF} and **ground**. The divider voltage is set at 63.2% of V_{REF} with respect to ground—exactly one RC time constant. The impedance of the divider is increased to about 30k with a series resistor to present a minimum load on external signals tied to V_{ADJ}. This resistor is a pinched type with a typical variation in nominal value of −50%, +100% and a TC of 0.7%/°C. For this reason, external signals (typically a pot between V_{REF} and **ground**) connected to V_{ADJ} should have a source resistance as low as possible. For small changes in V_{ADJ}, up to several kΩ is all right, but for large variations, 250Ω or less should be maintained. This can be accomplished with a 1k pot, since the maximum impedance from the wiper is 250Ω. If a voltage is forced on V_{ADJ} from a hard source, voltage should be limited to −0.5, and +5.0V, or current limited to ±1.0 mA. This includes capacitively coupled signals because even small values of capacitors contain enough energy to degrade the input stage if the capacitor is driven with a large, fast slewing signal. The V_{ADJ} pin may be used to abort the timing cycle. Grounding this pin during the timing period causes the timer to react just as if the capacitor voltage had reached its normal RC trigger point; the capacitor discharges and the output charges state. An exception to this occurs if the trigger pin is held high, when the V_{ADJ} pin is grounded. In this case, the output changes state, but the capacitor does not discharge.

If the trigger drops while V_{ADJ} is being held low, discharge will occur immediately and the cycle will be over. If the trigger is still high when V_{ADJ} is released, the output may or may not change state, depending on the voltage across the timing capacitor. For voltages below 2.0V across the timing capacitor, the output will change state immediately, then once more as the voltage rises past 2.0V. For voltages above 2.0V, no change will occur in the output. This pin is not available on the LM2905/LM3905.

In noisy environments or in comparator-type applications, a bypass capacitor on the V_{ADJ} terminal may be needed to eliminate spurious outputs because it is high impedance point. The size of the cap will depend on the frequency and energy content of the noise. A 0.1 μF will generally suffice for spike suppression, but several μF may be used if the timer is subjected to high level 60 Hz EMI.

The **emitter** and the **collector** outputs of the timer can be treated just as if they were an ordinary transistor with 40V minimum collector-emitter breakdown voltage. Normally, the **emitter** is tied to the **ground** pin and the signal is taken from the **collector**, or the **collector** is tied to V^+ and the signal is taken from the **emitter**. Variations on these basic connections are possible. The **collector** can be tied to any positive voltage up to 40V when the signal is taken from the **emitter**. However, the **emitter** will not be pulled higher than the supply voltage on the V^+ pin. Connecting the **collector** to a voltage less than the V^+ voltage is allowed. The **emitter** should not be connected to a low impedance load other than that to which the ground pin is tied. The transistor has built-in current limiting with a typical knee current of 120 mA. Temporary short circuits are allowed; even with **collector-emitter** voltages up to 40V. The power x time product, however, must not exceed 15 watt-seconds for power levels above the maximum rating of the package. A short to 30V,

Pin Function Description (Continued)

for instance, cannot be held for more than 4 seconds. These levels are based on 40°C maximum initial chip temperature. When driving inductive loads, always use a clamp diode to protect the transistor from inductive kick-back.

A **boost** pin is provided on the LM122 to increase the speed of the internal comparator. The comparator is normally operated at low current levels for lowest possible input current.

For timing periods less than 1 ms, where low input current is not needed, comparator operating current can be increased several orders of magnitude. Shorting the boost terminal to **V**+ increases the emitter current of the vertical PNP drivers in the differential stage from 25 nA to 5 μA. This pin is not available on the LM2905/LM3905.

With the timer in the unboosted state, timing periods are accurate down to about 1 ms. In the boosted mode, loss of accuracy due to comparator speed is only about 800 ns, so timing periods of several microseconds can be used. The 800 ns error is relatively insensitive to temperature, so temperature coefficient of pulse width is still good.

The **Logic** pin is used to reverse the signal appearing at the output transistor. An open or "high" condition on the **logic** pin programs the output transistor to be "off" during the timing period and "on" all other times. Grounding the **logic** pin reverses the sequence to make the transistor "on" during the timing period. Threshold for the **logic** pin is typically 100 mV with 150 μA flowing out of the terminal. If an active drive to the **logic** pin is desired, a saturated transistor drive is recommended, either with a discrete transistor or the open collector output of integrated logic. A maximum V_{SAT} of 25 mV at 200 μA is required. Minimum and maximum voltages that may appear on the **logic** pin are 0 and +5.0, respectively.

Typical Applications

Basic Timers

Figure 1 is a basic timer using the collector output. R_t and C_t set the time interval with R_L as the load. During the timing interval the output may be either high or low depending on the connection of the logic pin. Timing waveforms are shown in the sketch along side *Figure 1*. Note that the trigger pulse may be either shorter or longer than the output pulse width.

Figure 2 is again a basic timer, but with the output taken from the emitter of the output transistor. As with the collector output, either a high or low condition may be obtained during the timing period.

Simulating a Thermal Delay Relay

Figure 3 is an application where the LM122 is used to simulate a thermal delay relay which prevents power from being applied to other circuitry until the supply has been on for some time. The relay remains de-energized for R_t C_t seconds after V_{CC} is applied, then closes and stays energized until V_{CC} is turned off. *Figure 4* is a similar circuit except that the relay is energized as soon as V_{CC} is applied. R_t C_t seconds later, the relay is de-energized and stays off until the V_{CC} supply is recycled.

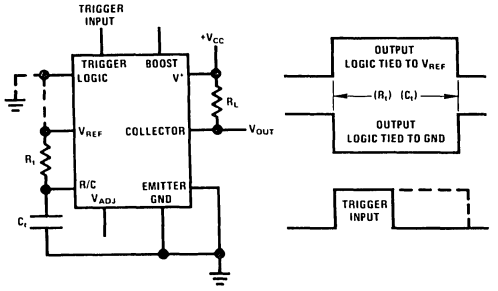

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FIGURE 1. Basic Timer-Collector Output and Timing Chart

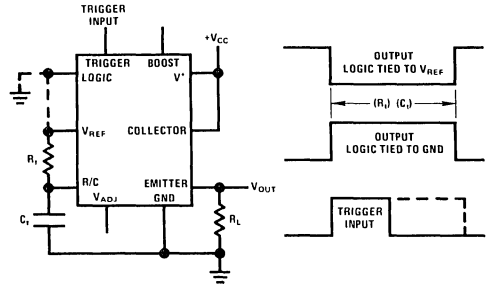

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FIGURE 2. Basic Timer-Emitter Output and Timing Chart

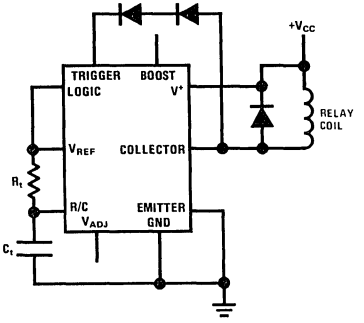

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FIGURE 3. Time Out on Power Up (Relay Energized R_t C_t Seconds after V_{CC} is Applied)

+5V Supply Driving 28V Relay

Figure 5 shows the timer interfacing 5V logic to a high voltage relay. Although the V+ terminal could be tied to the +28V supply, this may be an unnecessary waste of power in the IC or require extra wiring if the LM122 is on a logic card. In either case, the threshold for the trigger is 1.6V.

Typical Applications (Continued)

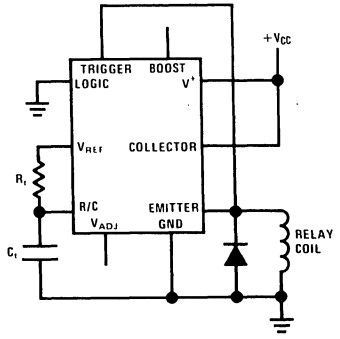

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FIGURE 4. Time Out on Power Up (Relay Energized *Until* R_t C_t Seconds After V_{CC} is Applied)

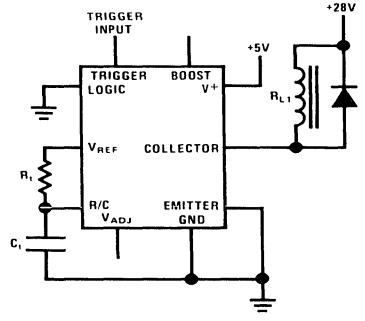

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FIGURE 5. 5V Logic Supply Driving 28V Relay

30V Supply Interfacing with 5V Logic

Figure 6 indicates the ability of the timer to interface to digital logic when operating off a high supply voltage. V_{OUT} swings between +5V and ground with a minimum fanout of 5 for medium speed TTL. If the logic is sensitive to rise/fall time of the trailing edge of the output pulse, the trigger pin should be low at that time.

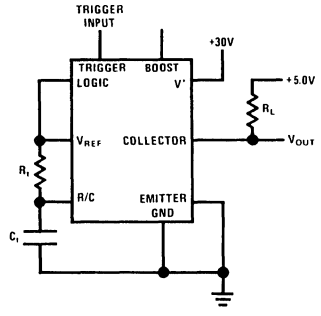

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FIGURE 6. 30V Supply Interfacing with 5V Logic

Astable Operation

The LM122 can be made into a self-starting oscillator by feeding the output back to the trigger input through a capacitor as shown in *Figure 7*. Operating frequency is $1/(R_t + R_1)(C_t)$. The output is a narrow negative pulse whose width is approximately $2R_2$ C_f. For optimum frequency stability, C_f should be as small as possible. The minimum value is determined by the time required to discharge C_t through the internal discharge transistor. A conservative value for C_f can be chosen from the graph included with *Figure 20*. For frequencies below 1 kHz, the frequency error introduced by C_f is a few tenths of one percent or less for $R_t \geq 500k$.

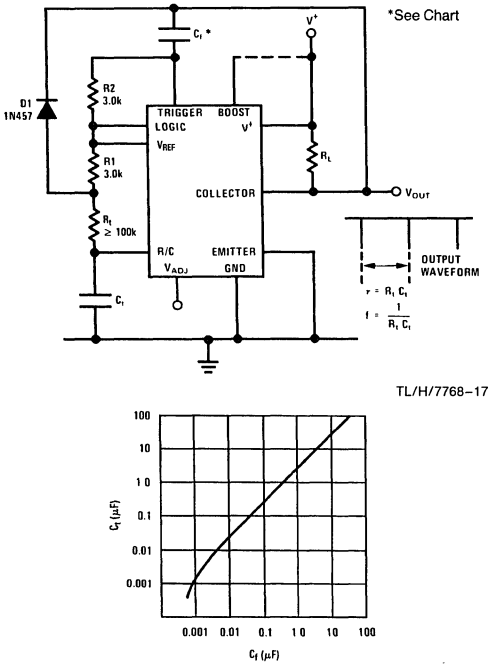

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FIGURE 7. Oscillator

One Hour Timer with Reset and Manual Cycle End

Figure 8 shows the LM122 connected as a one hour timer with manual controls for start, reset, and cycle end. S1 starts timing, but has no effect after timing has started. S2 is a center off switch which can either end the cycle prematurely with the appropriate change in output state and discharging of C_t, or cause C_t to be reset to 0V without a change in output. In the latter case, a new timing period starts as soon as S2 is released.

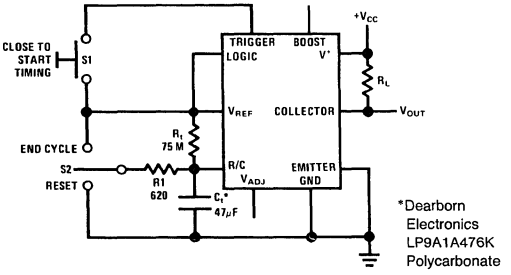

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FIGURE 8. One Hour Timer with Reset and Manual Cycle End

Typical Applications (Continued)

The average charging current through R_t is about 30 nA, so some attention must be paid to parts layout to prevent stray leakage paths. The suggested timing capacitor has a typical self time constant of 300 hours and a guaranteed minimum of 25 hours at +25°C. Other capacitor types may be used if sufficient data is available on their leakage characteristics.

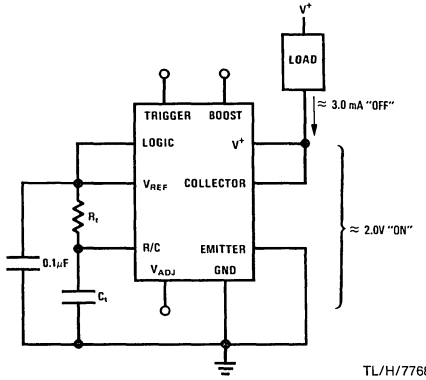
Two Terminal Time Delay Switch

The LM122 can be used as a two terminal time delay switch if an "on" voltage drop of 2V to 3V can be tolerated. In *Figure 9*, the timer is used to drive a relay "on" $R_t \bullet C_t$ seconds after application of power. "Off" current of the switch is 4 mA maximum, and "on" current can be as high as 50 mA.

Zero Power Dissipation Between Timing Intervals

In some applications it is desirable to reduce supply current drain to zero between timing cycles. In *Figure 10* this is accomplished by using an external PNP as a latch to drive the V^+ pin of the timer.

Between timing periods Q1 is off and no supply current is drawn. When a trigger pulse of 5V minimum amplitude is received, the LM122 output transistor and Q1 latch for the duration of the timing period. D1 prevents the step on the V^+ pin from coupling back into the trigger pin. If the trigger input is a short pulse, C1 and R2 may be eliminated. R_L must have a minimum value of $(V_{CC})/(2.5\ mA)$.



TL/H/7768–20

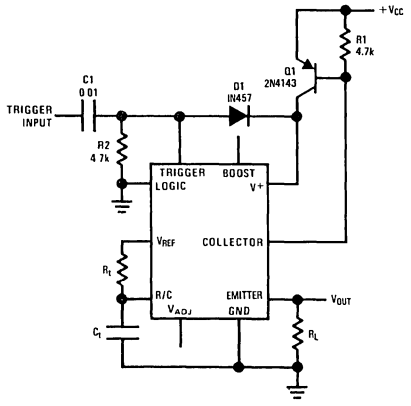
FIGURE 9. 2-Terminal Time Delay Switch

Frequency to Voltage Converter

An accurate frequency to voltage converter can be made with the LM122 by averaging output pulses with a simple one pole filter as shown in *Figure 11*. Pulse width is adjusted with R2 to provide initial calibration at 10 kHz. The collector of the output transistor is tied to V_{REF}, giving constant amplitude pulses equal to V_{REF} at the emitter output. R4 and C1 filter the pulses to give a dc output equal to, $(R_t)(C_t)(V_{REF})(f)$. Linearity is about 0.2% for a 0V to 1V output. If better linearity is desired R5 can be tied to the summing node of an op amp which has the filter in the feedback path. If a low output impedance is desired, a unity gain buffer such as the LM110 can be tied to the output. An analog meter can be driven directly by placing it in series with R5 to ground. A series RC network across the meter to provide damping will improve response at very low frequencies.

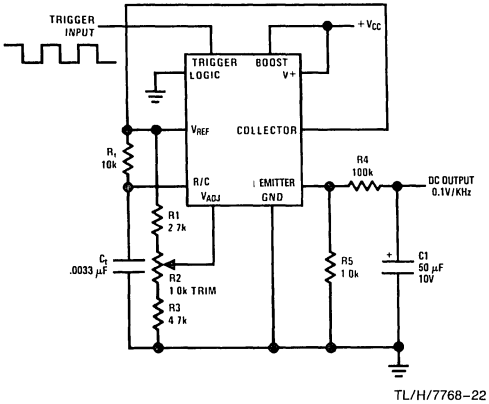
Pulse Width Detector

By driving the logic terminal of the LM122 simultaneous to the trigger input, a simple, accurate pulse width detector can be made *(Figure 12)*.



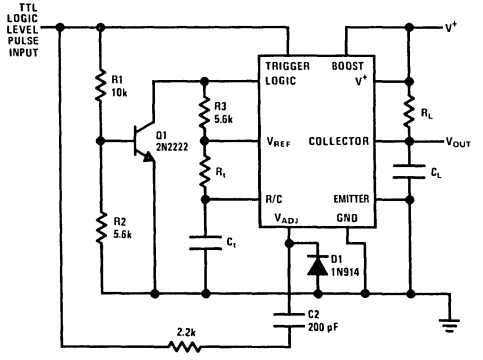
TL/H/7768–21

FIGURE 10. Zero Power Dissipation Between Timing Intervals



TL/H/7768–22

FIGURE 11. Frequency to Voltage Converter. (Tachometer) Output Independent of Supply Voltage.



TL/H/7768–23

*V_{OUT} = 0 for W R_1 C_1
Pulse Out = W − R_1 C_1 for W R_1 C_1

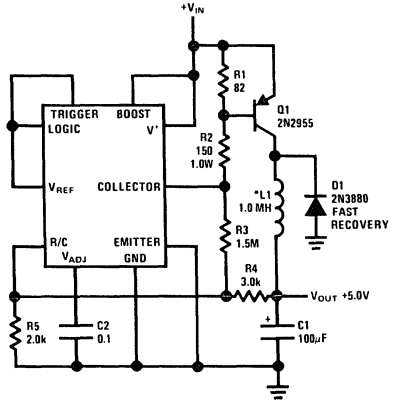
FIGURE 12. Pulse Width Detector

Typical Applications (Continued)

In this application the logic terminal is normally held high by R3. When a trigger pulse is received, Q1 is turned on, driving the logic terminal to ground. The result of triggering the timer and reversing the logic at the same time is that the output does not change from its initial low condition. The only time the output will change states is when the trigger input stays high longer than one time period set by R_t and C_t. The output pulse width is equal to the input trigger width minus $R_t \bullet C_t$. C2 insures no output pulse for short ($<RC$) trigger pulses by prematurely resetting the timing capacitor when the trigger pulse drops. C_L filters the narrow spikes which would occur at the output due to propagation delays during switching.

5V Switching Regulator

Figure 13 is an application where the LM122 does not use its timing function. A switching regulator is made using the internal reference and comparator to drive a PNP transistor switch. Features of this circuit include a 5.5V minimum input voltage at 1A output current, low part count, and good efficiency (> 75%) for input voltages to 10V. Line and load regulation are less than 0.5% and output ripple at the switching frequency is only 30 mV. Q1 is an inexpensive plastic device which does not need a heatsink for ambient temperature up to 50°C. D1 should be a fast switching diode. Output voltage can be adjusted between 1V and 30V by choosing proper values for R2, R3, R4, and R5. For outputs less than 2V, a divider with 250Ω Thevinin resistance must be connected between V_{REF} and ground with its tap point tied to V_{ADJ}.



*No. 22 Wire Wound on Molybdenum Permalloy Core TL/H/7768–24

FIGURE 13. 5V Switching Regulator with 1 Amp Output and 5.5V Minimum Input

Application Hints

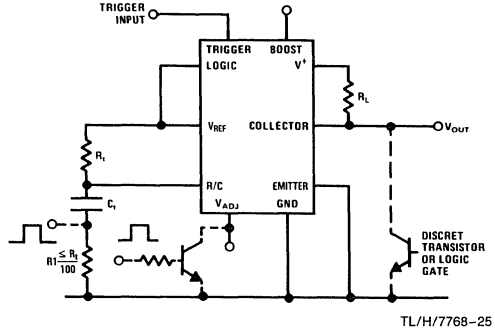
Aborting a Timing Cycle

The LM122 does not have an input specifically allocated to a stop-timing function. If such a function is desired, it may be accomplished several ways:

- Ground V_{ADJ}
- Raise R/C more positive than V_{ADJ}
- Wire "OR" the output

Grounding V_{ADJ} will end the timing cycle just as if the timing capacitor had reached its normal discharge point. A new timing cycle can be started by the trigger terminal as soon as the ground is released. A switching transistor is best for driving V_{ADJ} to as near ground as possible. Worst case sink current is about 300 μA.

A timing cycle may also be ended by a positive pulse to a resistor ($R \leq R_t/100$) in series with the timing capacitor. The pulse amplitude must be at least equal to V_{ADJ} (2.0V), but should not exceed 5.0V. When the timing capacitor discharges, a negative spike of up to 2.0V will occur across the resistor, so some caution must be used if the drive pulse is used for other circuitry.



TL/H/7768–25

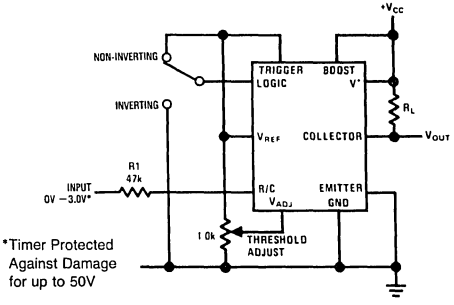
FIGURE 14. Cycle Interrupt

The output of the timer can be wire ORed with a discrete transistor or an open collector logic gate output. This allows overriding of the timer output, but does not cause the timer to be reset until its normal cycle time has elapsed.

Using the LM122 as a Comparator

A built-in reference and zero volt common mode limit make the LM122 very useful as a comparator. Threshold may be adjusted from zero to three volts by driving the V_{ADJ} terminal with a divider tied to V_{REF}. Stability of the reference voltage is typically ±1% over a temperature range of −55°C to +125°C. Offset voltage drift in the comparator is typically 25 μV/°C in the boosted mode and 50 μV/°C unboosted. A resistor can be inserted in series with the input to allow overdrives up to ±50V as shown in *Figure 15*. There is actually no limit on input voltage as long as current is limited to ±1 mA. The resistor shown contributes a worst case of 5 mV to initial offset. In the unboosted mode, the error drops to 0.25 mV maximum. The capability of operating off a single 5V supply with internal reference should make this comparator very useful.

Application Hints (Continued)



TL/H/7768–26

FIGURE 15. Comparator with 0V to 3V Threshold

Eliminating Timing Cycle Upon Initial Application of Power

The LM122 will normally start a timing cycle (with no trigger input) when V^+ is first turned on. If this characteristic is undesirable, it can be defeated by tying the timing capacitor to V_{REF} instead of ground as shown in *Figure 16*. This connection does not affect operation of the timer in any other way. If an electrolytic timing capacitor is used, be sure the negative end is tied to the R/C pin and the positive end to V_{REF}. A 1.0 kΩ resistor should be included in series with the timing capacitor to limit the surge current load on V_{REF} when the capacitor is discharged.

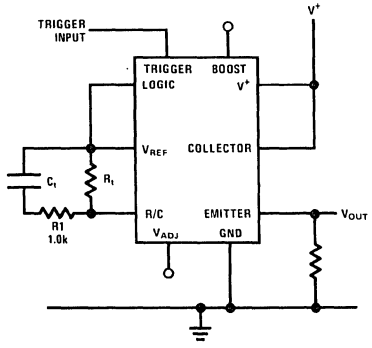


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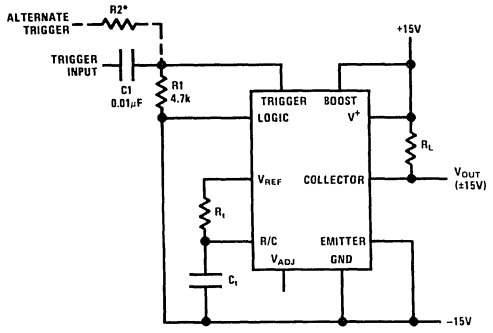
FIGURE 16. Eliminating Initial Timing Cycle

Using Dual Supplies

The LM122 can be operated off dual supplies as shown in *Figure 17*. The only limitation is that the emitter terminal cannot be tied to ground, it must either drive a load referred to V^- or be actually tied to V^- as shown. Although capacitive coupling is shown for the trigger input (to allow 5V triggering), a resistor can be substituted for C1. R2 must be chosen to give proper level shifting between the trigger signal and the trigger pin of the timer. Worst case "lo" on the trigger pin (with respect to V^-) is 0.8V, and worst case "high" is 2.5V. R2 may be calculated from the divider equation with R1 to give these levels.



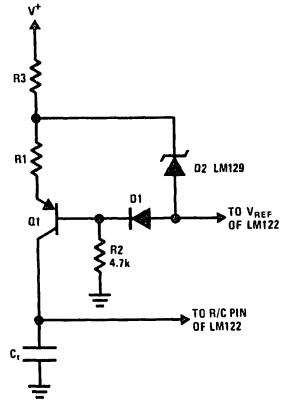
TL/H/7768–28

*Select for Proper Level Shift
Emitter Terminal or Emitter Load must be Tied to GND Pin of Timer

FIGURE 17. Operating Off Dual Supplies

Linearizing the Charging Sweep

In some applications (such as a linear pulse width modulator) it may be desirable to have the timing capacitor charge from a constant current source. A simple way to accomplish this is shown in *Figure 18*.



TL/H/7768–29

FIGURE 18. Temperature Compensated Linear Charging Sweep

Q1 converts the current through R1 to a current source independent of the voltage across C_t. R2, R3, D1, and D2 are added to make the current through R1 independent of supply variations and temperature changes. (D2 is a low TC type) D2 and R3 can be omitted if the V^+ supply is stable and D1 and R2 can be omitted also if temperature stability is not critical. With D1, D2, R2 and R3 omitted, the current through R1 will change about 0.015%/°C with a 15V supply and 0.1%/°C with a 5.0V supply.

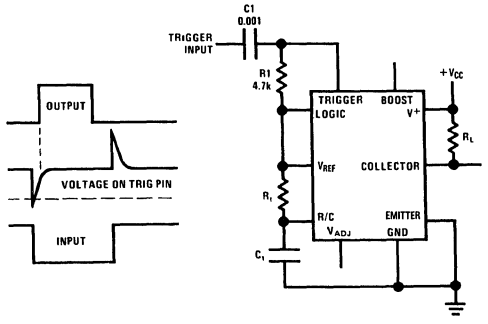
5

Application Hints (Continued)

Triggering with Negative Edge

Although the LM122 is triggered by a positive going trigger signal, a differentiator tied to a normally "high" trigger will result in negative edge triggering. In *Figure 19*, R1 serves the dual purpose of holding the trigger pin normally high and differentiating the input trigger pulse coupled through C1. The timing diagram included with *Figure 21* shows that triggering actually occurs a short time after the negative going trigger, while positive going triggers have no effect. The delay time between a negative trigger signal and actual starts of timing is approximately (0.5 to 1.5) (R1 • C1) depending on the trigger amplitude, or about 2.5 to 7.5 μs with the values shown. This time will have to be increased for C_t larger than 0.01 μF because C_t is charged to V_{REF} whenever the trigger pin is kept high and must reset itself during the short time that the trigger pin voltage is low. A conservative value for C1 is:

$$C1 \geq \frac{C_t}{10}$$

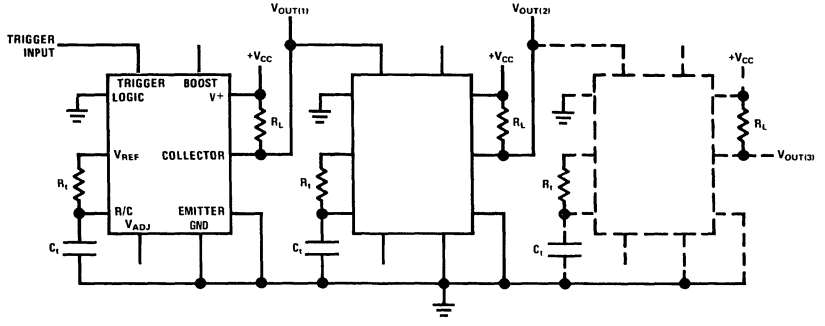


TL/H/7768–30

FIGURE 19. Timer Triggered by Negative Edge of Input Pulse

Chain of Timers

The LM122 can be connected as a chain of timers quite easily with no interface required. In *Figure 20A* and *20B*, two possible connections are shown. In both cases, the output of the timer is low during the timing period so that the positive going signal at the end of the timing period can trigger the next timer. There is no limitation on the timing period of one timer with respect to any other timer before or after it, because the trigger input to any timer can be high or low when that timer ends its timing period.



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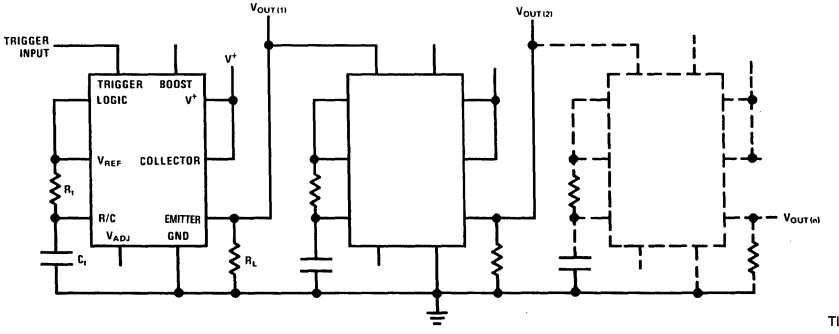
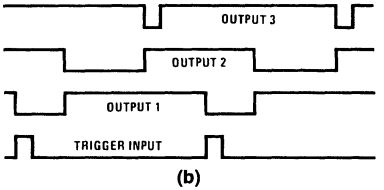
(a)



TL/H/7768–32



TL/H/7768–33

(b)

FIGURE 20. Chain of Timers

National Semiconductor Corporation

LM194/LM394 Supermatch Pair

General Description

The LM194 and LM394 are junction isolated ultra well-matched monolithic NPN transistor pairs with an order of magnitude improvement in matching over conventional transistor pairs. This was accomplished by advanced linear processing and a unique new device structure.

Electrical characteristics of these devices such as drift versus initial offset voltage, noise, and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic emitter and base resistances are much lower than presently available pairs, either monolithic or discrete, giving extremely low noise and theoretical operation over a wide current range. Most parameters are guaranteed over a current range of 1 μA to 1 mA and 0V up to 40V collector-base voltage, ensuring superior performance in nearly all applications.

To guarantee long term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current—the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

The LM194 and LM394 will provide a considerable improvement in performance in most applications requiring a closely matched transistor pair. In many cases, trimming can be eliminated entirely, improving reliability and decreasing costs. Additionally, the low noise and high gain make this device attractive even where matching is not critical.

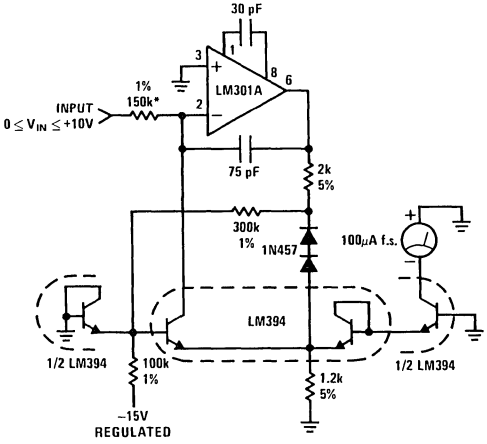
The LM194 and LM394/LM394B/LM394C are available in an isolated header 6-lead TO-5 metal can package. The LM394/LM394B/LM394C are available in an 8-pin plastic dual-in-line package. The LM394C is also available in a 8 pin plastic dual-in-line package. The LM194 is identical to the LM394 except for tighter electrical specifications and wider temperature range.

Features

- Emitter-base voltage matched to 50 μV
- Offset voltage drift less than 0.1 μV/°C
- Current gain (h_{FE}) matched to 2%
- Common-mode rejection ratio greater than 120 dB
- Parameters guaranteed over 1 μA to 1 mA collector current
- Extremely low noise
- Superior logging characteristics compared to conventional pairs
- Plug-in replacement for presently available devices

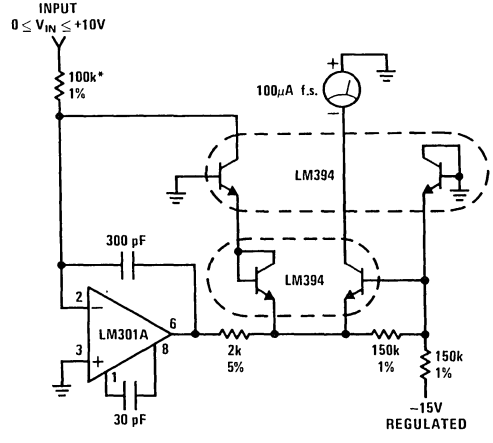
Typical Applications

Low Cost Accurate Square Root Circuit
$I_{OUT} = 10^{-5}.\sqrt{10\ V_{IN}}$



TL/H/9241–1

Low Cost Accurate Squaring Circuit
$I_{OUT} = 10^{-6}\ (V_{IN})^2$



TL/H/9241–2

*Trim for full scale accuracy

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications. (Note 4)

Collector Current	20 mA
Collector-Emitter Voltage	V_{MAX}
Collector-Emitter Voltage	40V
LM394C	20V
Collector-Base Voltage	40V
LM394C	20V
Collector-Substrate Voltage	40V
LM394C	20V
Collector-Collector Voltage	40V
LM394C	20V
Base-Emitter Current	±10 mA
Power Dissipation	500 mW
Junction Temperature	
LM194	−55°C to +125°C
LM394/LM394B/LM394C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Metal Can Package (10 sec.)	260°C
Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_J = 25°C)

Parameter	Conditions	LM194			LM394			LM394B/394C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Current Gain (h_{FE})	V_{CB} = 0V to V_{MAX} (Note 1)										
	I_C = 1 mA	500	700		300	700		225	500		
	I_C = 100 μA	400	550		250	550		200	400		
	I_C = 10 μA	300	450		200	450		150	300		
	I_C = 1 μA	200	300		150	300		100	200		
Current Gain Match, (h_{FE} Match) $= \frac{100\ [\Delta I_B]\ [h_{FE(MIN)}]}{I_C}$	V_{CB} = 0V to V_{MAX}										
	I_C = 10 μA to 1 mA		0.5	2		0.5	4		1.0	5	%
	I_C = 1 μA		1.0			1.0			2.0		%
Emitter-Base Offset Voltage	V_{CB} = 0										
	I_C = 1 μA to 1 mA		25	50		25	150		50	200	μV
Change in Emitter-Base Offset Voltage vs Collector-Base Voltage (CMRR)	(Note 1) I_C = 1 μA to 1 mA, V_{CB} = 0V to V_{MAX}		10	25		10	50		10	100	μV
Change in Emitter-Base Offset Voltage vs Collector Current	V_{CB} = 0V, I_C = 1 μA to 0.3 mA		5	25		5	50		5	50	μV
Emitter-Base Offset Voltage Temperature Drift	I_C = 10 μA to 1 mA (Note 2)		0.08	0.3		0.08	1.0		0.2	1.5	μV/°C
	$I_{C1} = I_{C2}$										
	V_{OS} Trimmed to 0 at 25°C		0.03	0.1		0.03	0.3		0.03	0.5	μV/°C
Logging Conformity	I_C = 3 nA to 300 μA, V_{CB} = 0, (Note 3)		150			150			150		μV
Collector-Base Leakage	$V_{CB} = V_{MAX}$		0.05	0.25		0.05	0.5		0.05	0.5	nA
Collector-Collector Leakage	$V_{CC} = V_{MAX}$		0.1	2.0		0.1	5.0		0.1	5.0	nA
Input Voltage Noise	I_C = 100 μA, V_{CB} = 0V, f = 100 Hz to 100 kHz		1.8			1.8			1.8		nV/$\sqrt{Hz}$
Collector to Emitter Saturation Voltage	I_C = 1 mA, I_B = 10 μA		0.2			0.2			0.2		V
	I_C = 1 mA, I_B = 100 μA		0.1			0.1			0.1		V

Note 1: Collector-base voltage is swept from 0 to V_{MAX} at a collector current of 1 μA, 10 μA, 100 μA, and 1 mA.

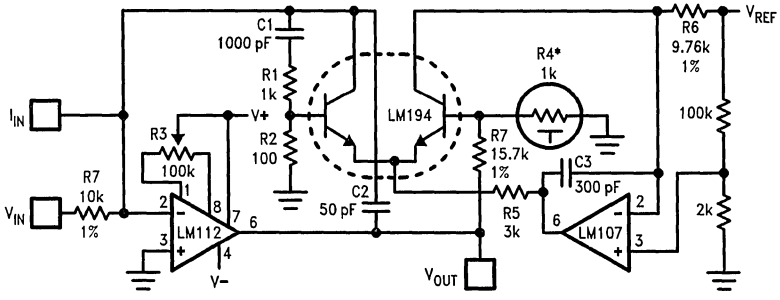
Note 2: Offset voltage drift with V_{OS} = 0 at T_A = 25°C is valid only when the ratio of I_{C1} to I_{C2} is adjusted to give the initial zero offset. This ratio must be held to within 0.003% over the entire temperature range. Measurements taken at +25°C and temperature extremes.

Note 3: Logging conformity is measured by computing the best fit to a true exponential and expressing the error as a base-emitter voltage deviation.

Note 4: Refer to RETS194X drawing of military LM194H version for specifications.

Typical Applications (Continued)

Fast, Accurate Logging Amplifier, V_{IN} = 10V to 0.1 mV or I_{IN} = 1 mA to 10 nA

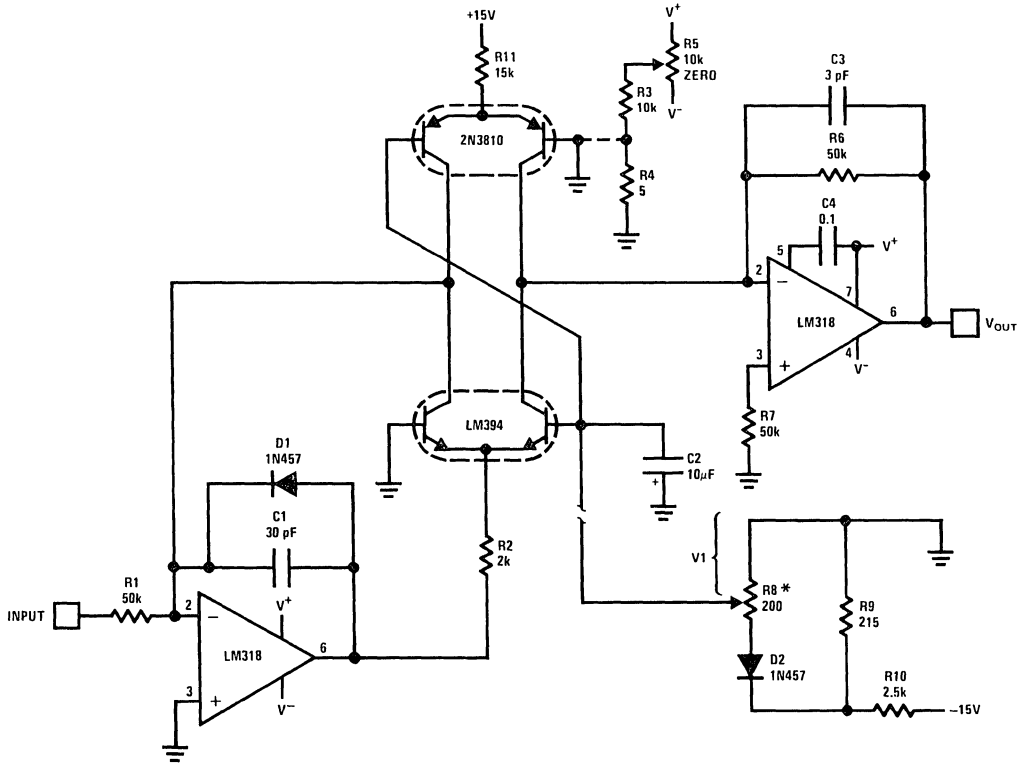


TL/H/9241-3

*Tel Labs type Q81 +0.3%/°C

$$V_{OUT} = -\log_{10}\left(\frac{V_{IN}}{V_{REF}}\right)$$

Voltage Controlled Variable Gain Amplifier



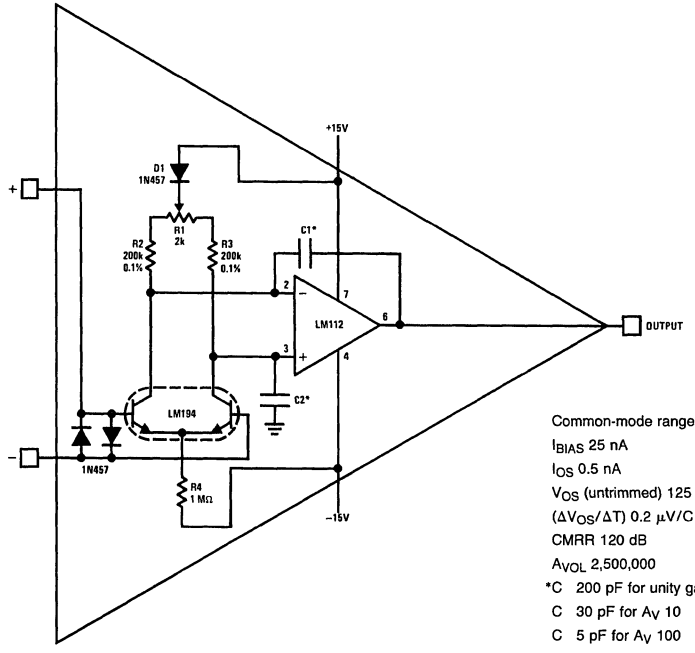
TL/H/9241-4

*R8–R10 and D2 provide a temperature independent gain control.
G = −336 V1 (dB)

Distortion < 0.1%
Bandwidth > 1 MHz
100 dB gain range

Typical Applications (Continued)

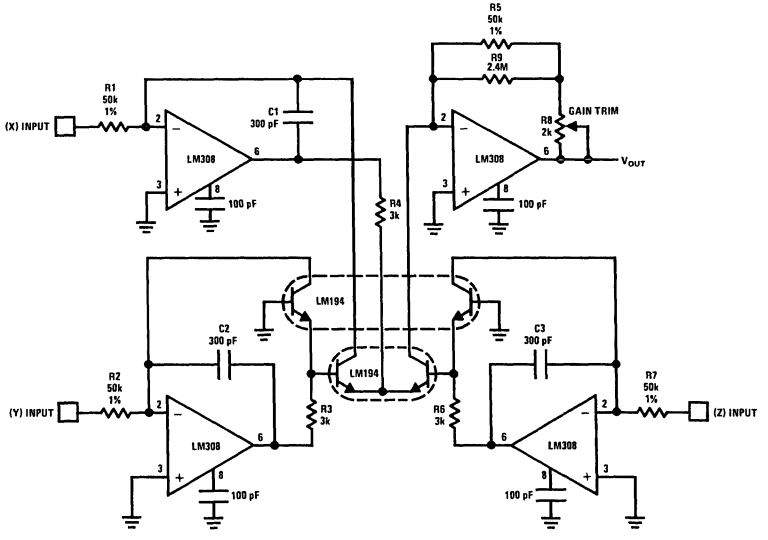
Precision Low Drift Operational Amplifier



Common-mode range 10V
I_{BIAS} 25 nA
I_{OS} 0.5 nA
V_{OS} (untrimmed) 125 μV
$(\Delta V_{OS}/\Delta T)$ 0.2 μV/C
CMRR 120 dB
A_{VOL} 2,500,000
*C 200 pF for unity gain
C 30 pF for A_V 10
C 5 pF for A_V 100
C 0 pF for A_V 1000

TL/H/9241–5

High Accuracy One Quadrant Multiplier/Divider



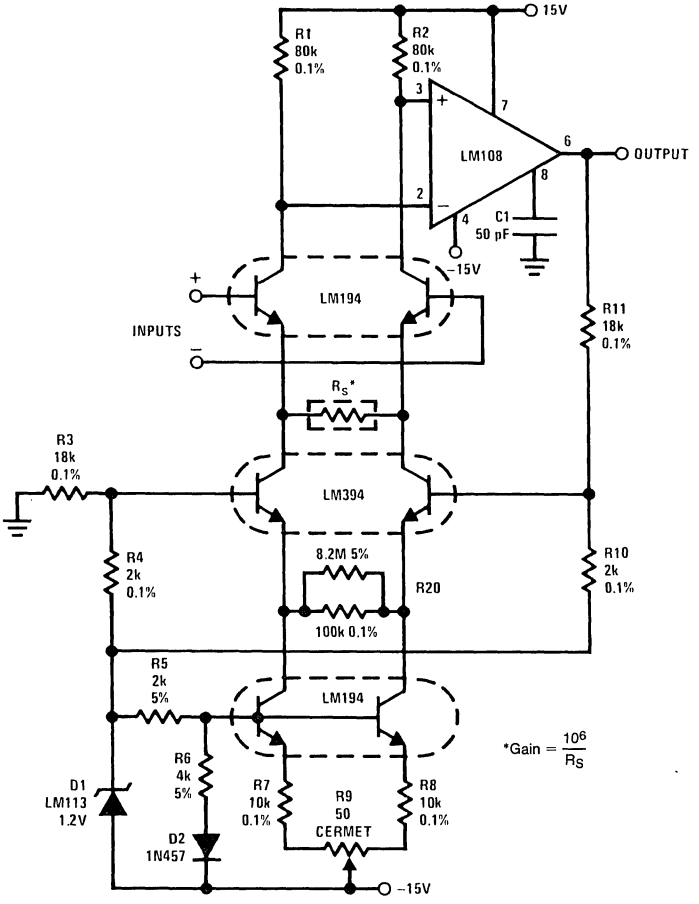
TL/H/9241–6

$V_{OUT} = \frac{(X)(Y)}{(Z)}$; positive inputs only.

*Typical linearity 0.1%

Typical Applications (Continued)

High Performance Instrumentation Amplifier



TL/H/9241–7

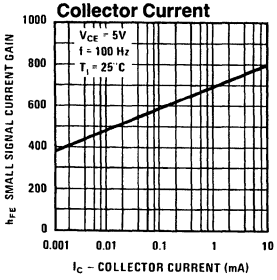
Performance Characteristics

	G = 10,000	G = 1,000	G = 100	G = 10	
Linearity of Gain (±10V Output)	≤0.01	≤0.01	≤0.02	≤0.05	%
Common-Mode Rejection Ratio (60 Hz)	≥120	≥120	≥110	≥90	dB
Common-Mode Rejection Ratio (1 kHz)	≥110	≥110	≥90	≥70	dB
Power Supply Rejection Ratio					
+Supply	>110	>110	>110	>110	dB
−Supply	>110	>110	>90	>70	dB
Bandwidth (−3 dB)	50	50	50	50	kHz
Slew Rate	0.3	0.3	0.3	0.3	V/μs
Offset Voltage Drift**	≤0.25	≤0.4	2	≤10	μV/°C
Common-Mode Input Resistance	$>10^9$	$>10^9$	$>10^9$	$>10^9$	Ω
Differential Input Resistance	$>3 \times 10^8$	$>3 \times 10^8$	$>3 \times 10^8$	$>3 \times 10^8$	Ω
Input Referred Noise (100 Hz ≤ f ≤ 10 kHz)	5	6	12	70	$\frac{nV}{\sqrt{Hz}}$
Input Bias Current	75	75	75	75	nA
Input Offset Current	1.5	1.5	1.5	1.5	nA
Common-Mode Range	±11	±11	±11	±10	V
Output Swing (R_L = 10 kΩ)	±13	±13	±13	±13	V

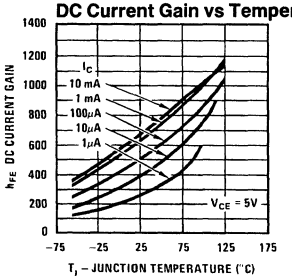
**Assumes ≤ 5 ppm/°C tracking of resistors

Typical Performance Characteristics

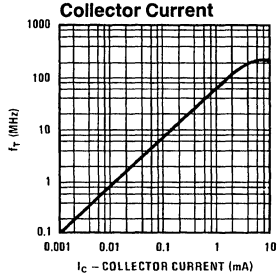
Small Signal Current Gain vs Collector Current



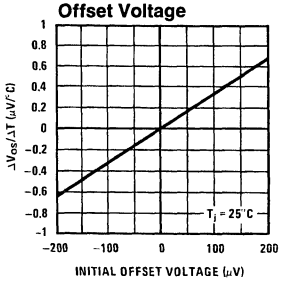
DC Current Gain vs Temperature



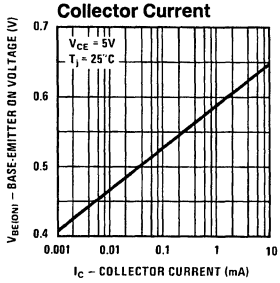
Unity Gain Frequency (f_t) vs Collector Current



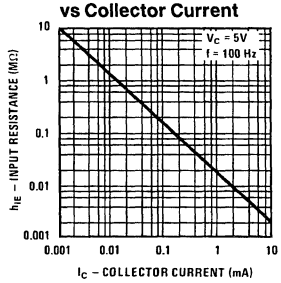
Offset Voltage Drift vs Initial Offset Voltage



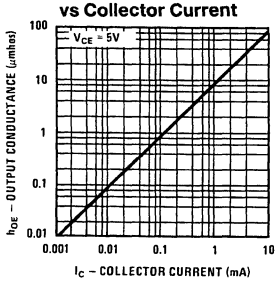
Base-Emitter On Voltage vs Collector Current



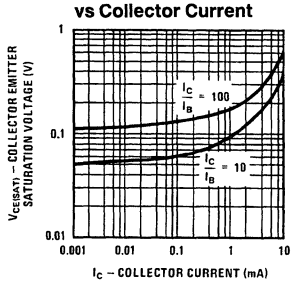
Small Signal Input Resistance (h_{ie}) vs Collector Current



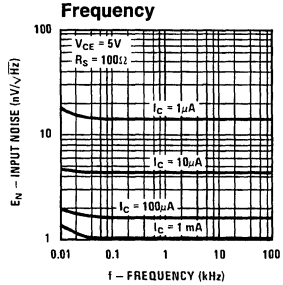
Small Signal Output Conductance vs Collector Current



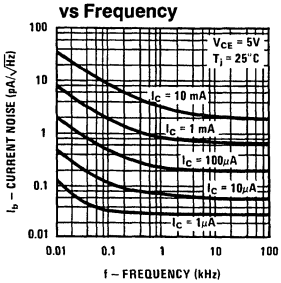
Collector-Emitter Saturation Voltage vs Collector Current



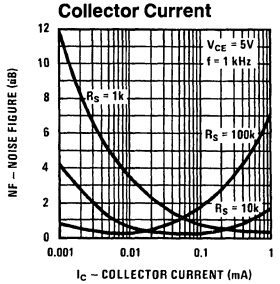
Input Voltage Noise vs Frequency



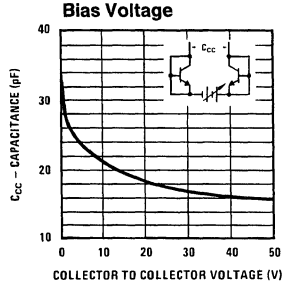
Base Current Noise vs Frequency



Noise Figure vs Collector Current



Collector to Collector Capacitance vs Reverse Bias Voltage



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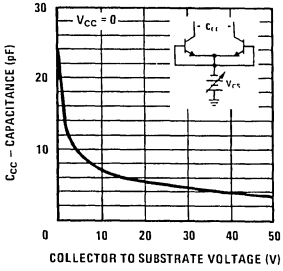
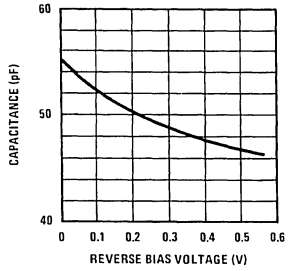
Typical Performance Characteristics (Continued)

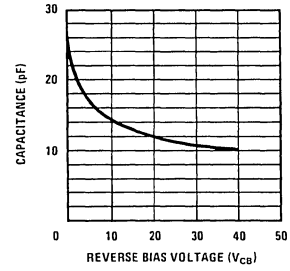
Collector to Collector Capacitance vs Collector-Substrate Voltage



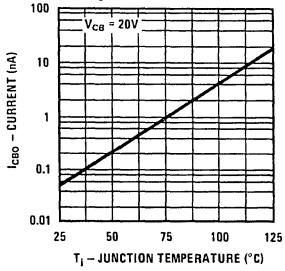
Emitter-Base Capacitance vs Reverse Bias Voltage



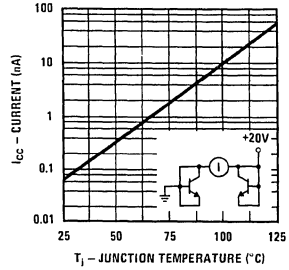
Collector-Base Capacitance vs Reverse Bias Voltage



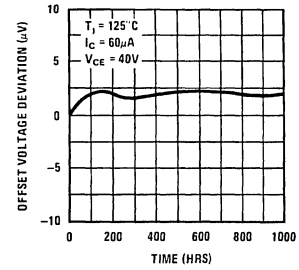
Collector-Base Leakage vs Temperature



Collector to Collector Leakage vs Temperature



Offset Voltage Long Term Stability at High Temperature



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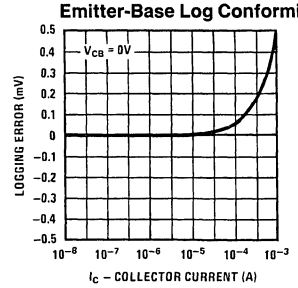
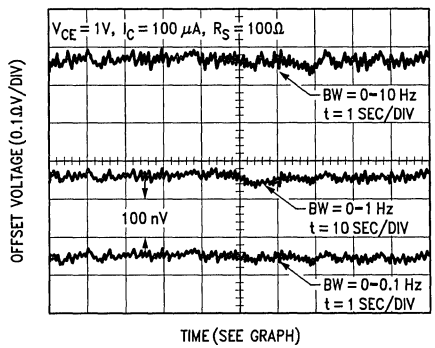
Emitter-Base Log Conformity



TL/H/9241–10

Low Frequency Noise of Differential Pair*

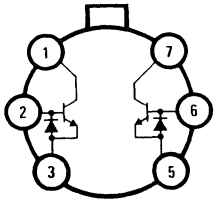


TL/H/9241–11

*Unit must be in still air environment so that differential lead temperature is held to less than 0.0003°C.

Connection Diagram

Metal Can Package

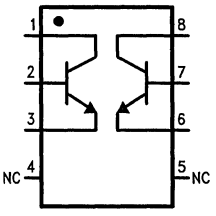


TL/H/9241–12

Top View

Order Number LM194H, LM394H, LM394BH or LM394CH
See NS Package Number H06C

Dual-In-Line and Small Outline Packages



TL/H/9241–13

Top View

Order Number LM394CM, LM394N, LM394BN or LM394CN
See NS Package Number M08A or N08E

National Semiconductor Corporation

LM195/LM295/LM395 Ultra Reliable Power Transistors

General Description

The LM195/LM295/LM395 are fast, monolithic power transistors with complete overload protection. These devices, which act as high gain power transistors, have included on the chip, current limiting, power limiting, and thermal overload protection making them virtually impossible to destroy from any type of overload. In the standard TO-3 transistor power package, the LM195 will deliver load currents in excess of 1.0A and can switch 40V in 500 ns.

The inclusion of thermal limiting, a feature not easily available in discrete designs, provides virtually absolute protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive heating.

The LM195 offers a significant increase in reliability as well as simplifying power circuitry. In some applications, where protection is unusually difficult, such as switching regulators, lamp or solenoid drivers where normal power dissipation is low, the LM195 is especially advantageous.

The LM195 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LM195 as with any power transistor. When the device is used as an emitter follower with low source impedance, it is necessary to insert a 5.0k resistor in series with the base lead to prevent possible emitter follower oscillations. Although the device is usually stable as an emitter follower, the resistor eliminates the possibility of trouble without degrading performance. Finally, since it has good high frequency response, supply bypassing is recommended.

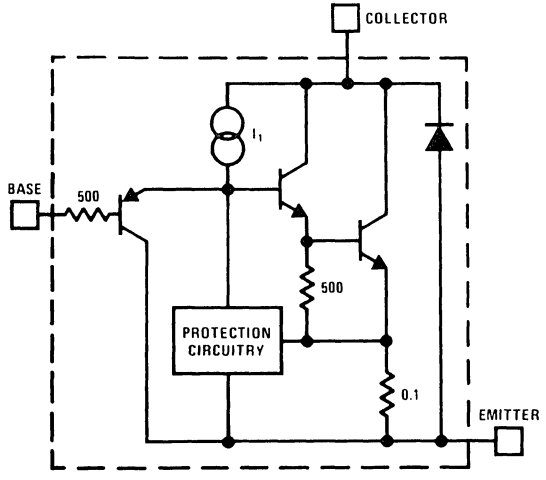
The LM195/LM295/LM395 are available in standard TO-3 power packages and solid Kovar TO-5. The LM195 is rated for operation from −55°C to +150°C, the LM295 from −25°C to +150°C and the LM395 from 0°C to +125°C.

Features

- Internal thermal limiting
- Greater than 1.0A output current
- 3.0 μA typical base current
- 500 ns switching time
- 2.0V saturation
- Base can be driven up to 40V without damage
- Directly interfaces with CMOS or TTL
- 100% electrical burn-in

Simplified Circuit

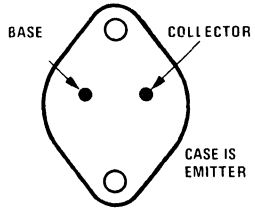
Simplified Circuit of the LM195



TL/H/6009–1

Connection Diagrams

TO-3 Metal Can Package

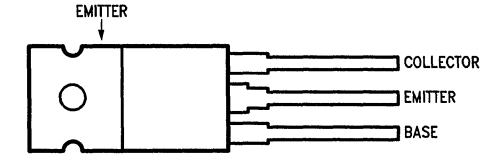


TL/H/6009-2

Bottom View

Order Number LM195K,
LM295K or LM395K
See NS Package Number K02A

TO-220 Plastic Package



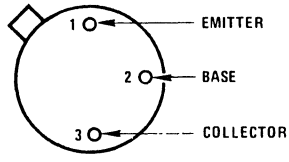
TL/H/6009-3

Case is Emitter

Top View

Order Number LM395T
See NS Package Number T03B

TO-5 Metal Can Package

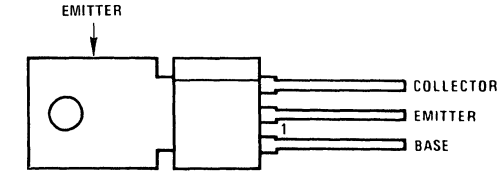


TL/H/6009-4

Bottom View

Order Number LM195H,
LM295H or LM395H
See NS Package Number H03B

TO-202 Plastic Package



TL/H/6009-5

Top View

Order Number LM395P
See NS Package Number P03A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Collector to Emitter Voltage
- LM195, LM295 — 42V
- LM395 — 36V

Collector to Base Voltage
- LM195, LM295 — 42V
- LM395 — 36V

Base to Emitter Voltage (Forward)
- LM195, LM295 — 42V
- LM395 — 36V

Base to Emitter Voltage (Reverse) — 20V

Collector Current — Internally Limited

Power Dissipation — Internally Limited

Operating Temperature Range
- LM195 — −55°C to +150°C
- LM295 — −25°C to +150°C
- LM395 — 0°C to +125°C

Storage Temperature Range — −65°C to +150°C

Lead Temperature (Soldering, 10 sec.) — 260°C

Preconditioning

100% Burn-In In Thermal Limit

Electrical Characteristics (Note 1)

Parameter	Conditions	LM195, LM295			LM395			Units
		Min	Typ	Max	Min	Typ	Max	
Collector-Emitter Operating Voltage (Note 3)	$I_Q \le I_C \le I_{MAX}$			42			36	V
Base to Emitter Breakdown Voltage	$0 \le V_{CE} \le V_{CEMAX}$	42			36	60		V
Collector Current								
TO-3, TO-220	$V_{CE} \le 15V$	1.2	2.2		1.0	2.2		A
TO-5, TO-202	$V_{CE} \le 7.0V$	1.2	1.8		1.0	1.8		A
Saturation Voltage	$I_C \le 1.0A$, $T_A = 25°C$		1.8	2.0		1.8	2.2	V
Base Current	$0 \le I_C \le I_{MAX}$ $0 \le V_{CE} \le V_{CEMAX}$		3.0	5.0		3.0	10	μA
Quiescent Current (I_Q)	$V_{be} = 0$ $0 \le V_{CE} \le V_{CEMAX}$		2.0	5.0		2.0	10	mA
Base to Emitter Voltage	$I_C = 1.0A$, $T_A = +25°C$		0.9			0.9		V
Switching Time	$V_{CE} = 36V$, $R_L = 36\Omega$, $T_A = 25°C$		500			500		ns
Thermal Resistance Junction to Case (Note 2)	TO-3 Package (K)		2.3	3.0		2.3	3.0	°C/W
	TO-5 Package (H)		12	15		12	15	°C/W
	TO-220 Package (T)					4	6	°C/W
	TO-202 Package (P)					12	15	°C/W

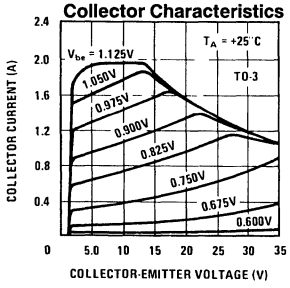
Note 1: Unless otherwise specified, these specifications apply for $-55°C \le T_j \le +150°C$ for the LM195, $-25°C \le T_j \le +150°C$ for the LM295 and $0°C \le +125°C$ for the LM395.

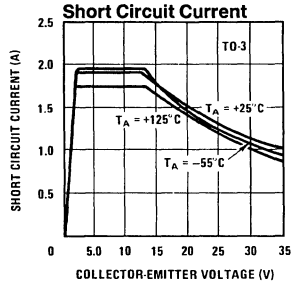
Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about +150°C/W, while that of the TO-3 package is +35°C/W.

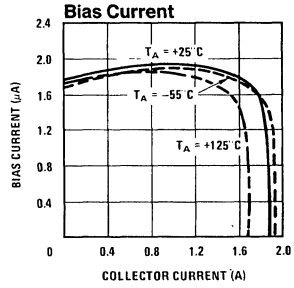
Note 3: Selected devices with higher breakdown available.

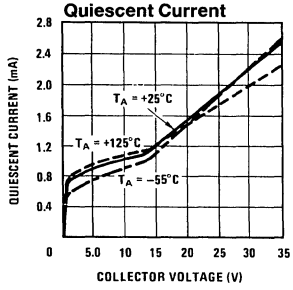
Note 4: Refer to RETS195H and RETS195K drawings of military LM195H and LM195K versions for specifications.

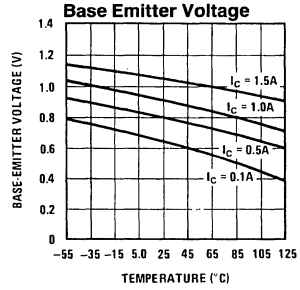
Typical Performance Characteristics (for K and T Packages)

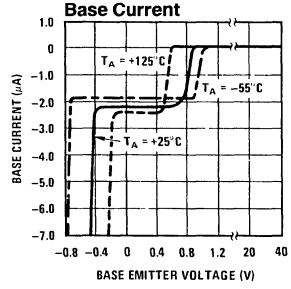


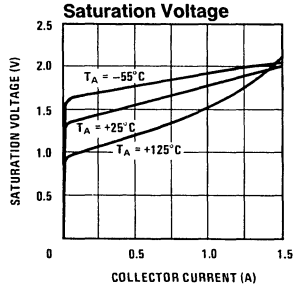


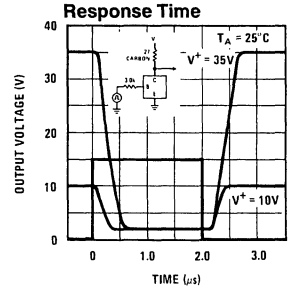


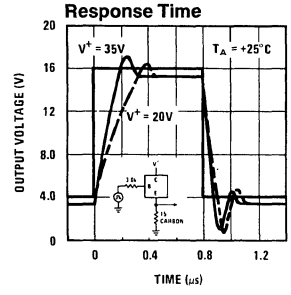








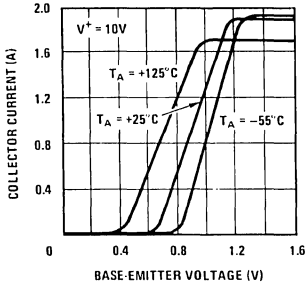




TL/H/6009–6

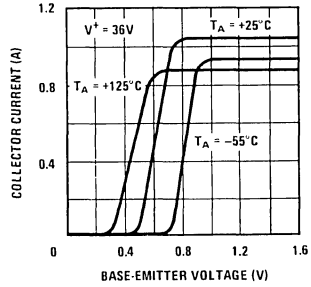
Typical Performance Characteristics (for K and T Packages) (Continued)

10V Transfer Function



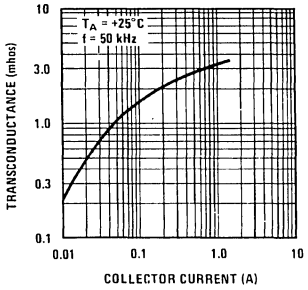
TL/H/6009–7

36V Transfer Function



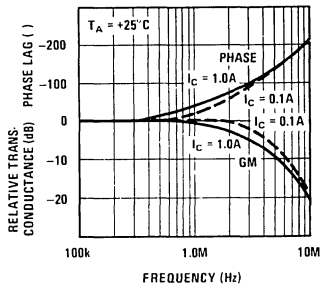
TL/H/6009–8

Transconductance



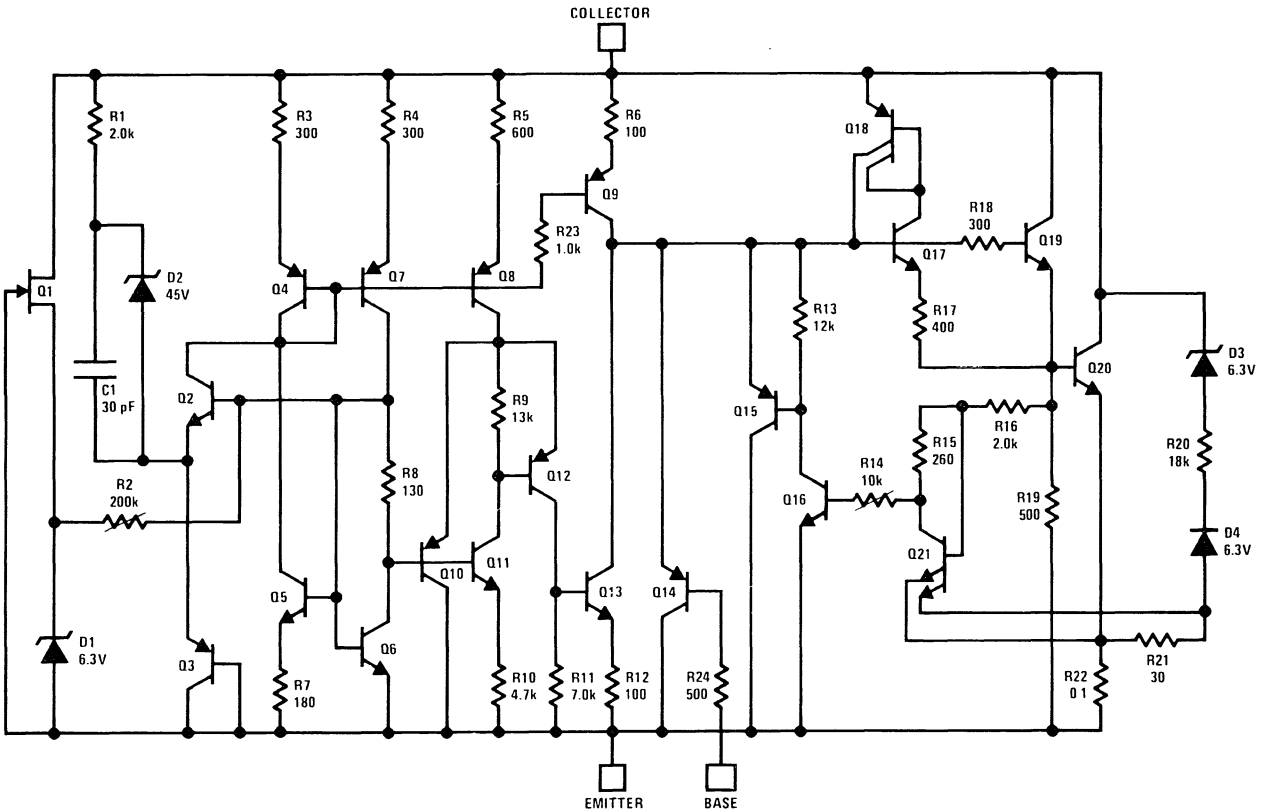
TL/H/6009–9

Small Signal Frequency Response



TL/H/6009–10

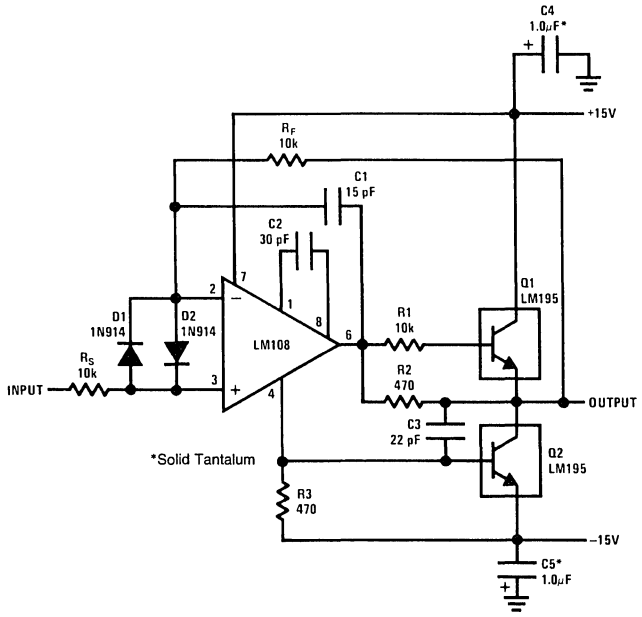
Schematic Diagram



TL/H/6009–11

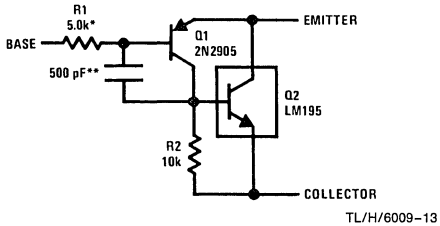
Typical Applications

1.0 Amp Voltage Follower



TL/H/6009–12

Power PNP

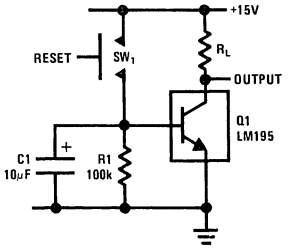


TL/H/6009–13

*Protects against excessive base drive

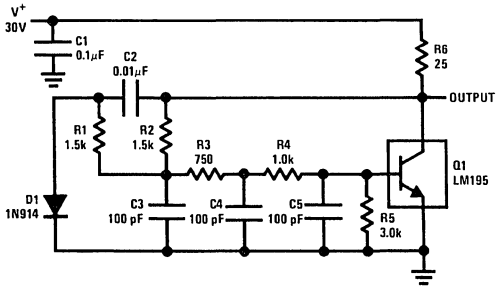
**Needed for stability

Time Delay



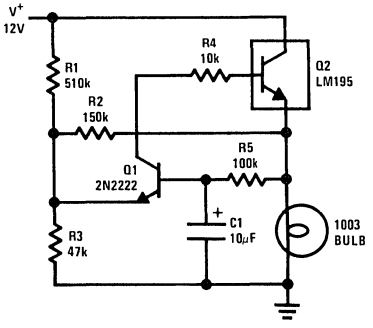
TL/H/6009–14

1.0 MHz Oscillator



TL/H/6009–15

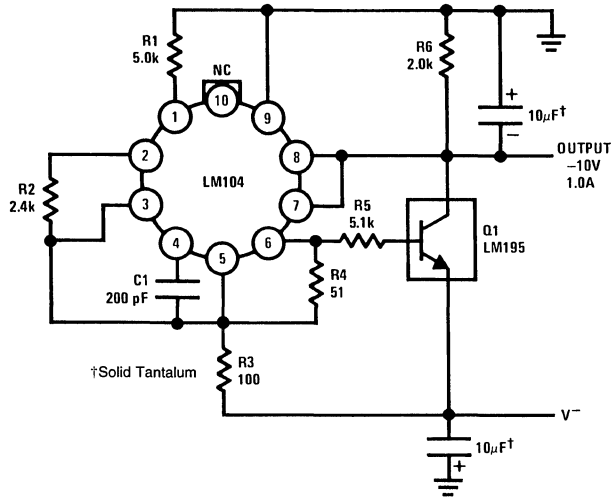
1.0 Amp Lamp Flasher



TL/H/6009–16

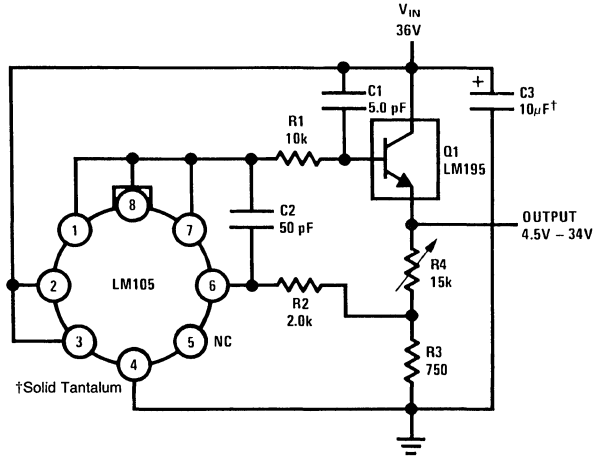
Typical Applications (Continued)

1.0 Amp Negative Regulator



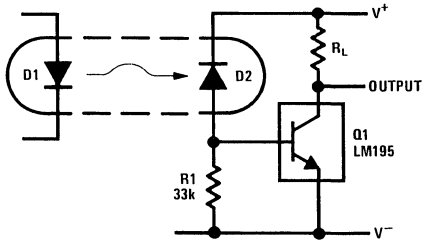
TL/H/6009–17

1.0 Amp Positive Voltage Regulator



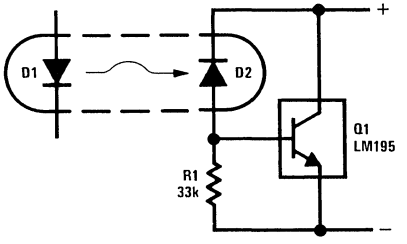
TL/H/6009–18

Fast Optically Isolated Switch



TL/H/6009–19

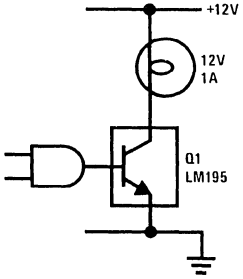
Optically Isolated Power Transistor



TL/H/6009–20

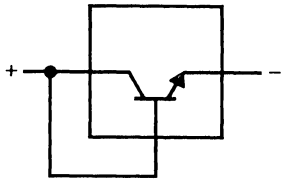
Typical Applications (Continued)

CMOS or TTL Lamp Interface



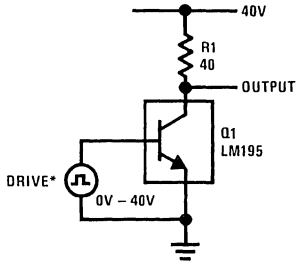
TL/H/6009–21

Two Terminal Current Limiter



TL/H/6009–22

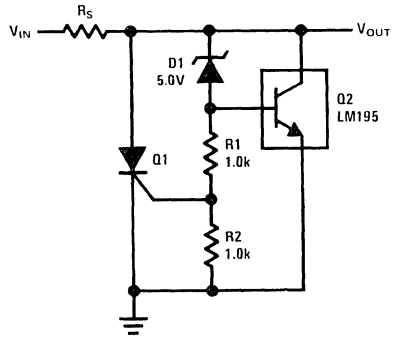
40V Switch



TL/H/6009–23

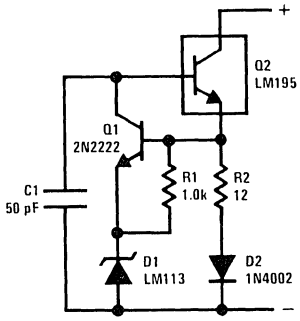
*Drive Voltage 0V to ≥ 10V ≤ 42V

6.0V Shunt Regulator with Crowbar



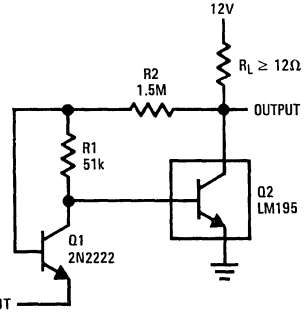
TL/H/6009–24

Two Terminal 100 mA Current Regulator



TL/H/6009–25

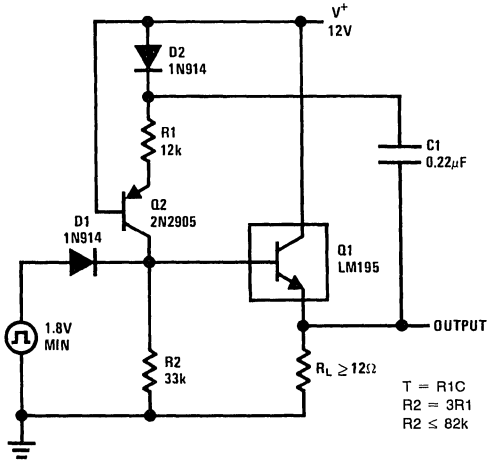
Low Level Power Switch



Turn ON = 350 mV
Turn OFF = 200 mV

TL/H/6009–26

Power One-Shot

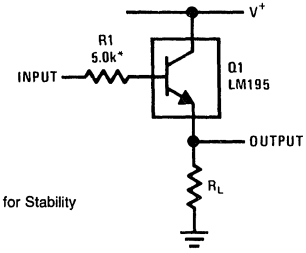


T = R1C
R2 = 3R1
R2 ≤ 82k

TL/H/6009–27

Typical Applications (Continued)

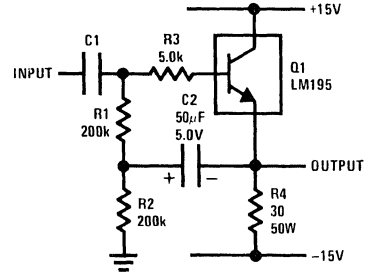
Emitter Follower



*Need for Stability

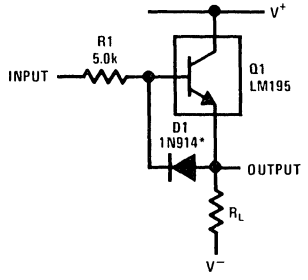
TL/H/6009–28

High Input Impedance AC Emitter Follower



TL/H/6009–29

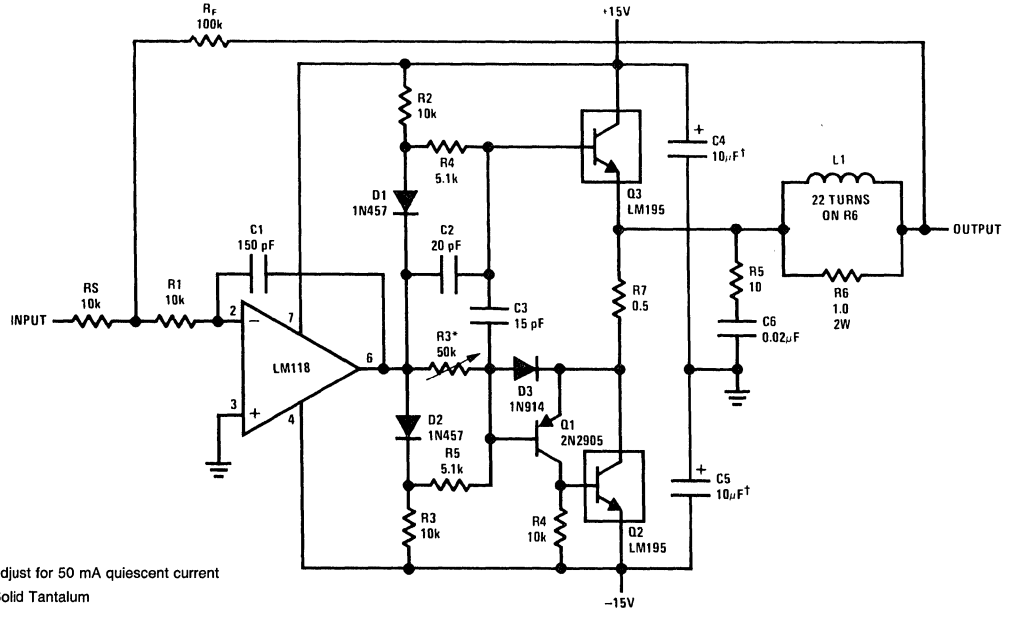
Fast Follower



TL/H/6009–30

*Prevents storage with fast fall time square wave drive

Power Op Amp



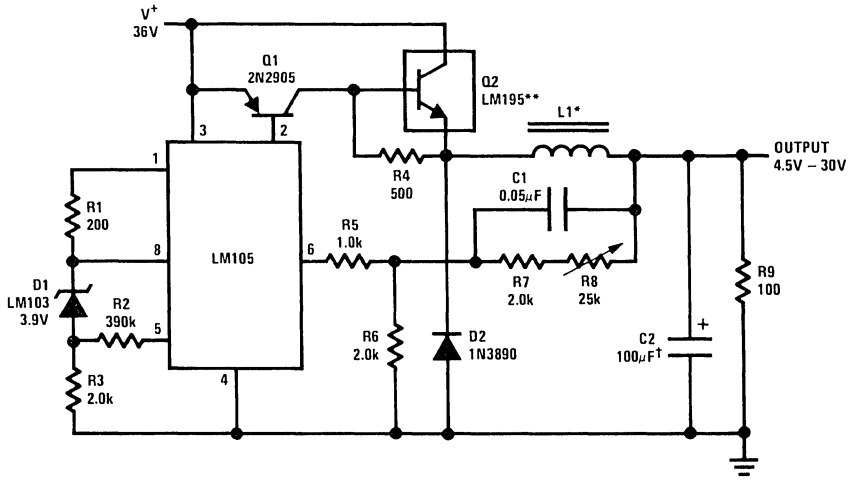
*Adjust for 50 mA quiescent current

†Solid Tantalum

TL/H/6009–31

Typical Applications (Continued)

6.0 Amp Variable Output Switching Regulator



TL/H/6009–32

*Sixty turns wound on Arnold Type A-083081-2 core.

**Four devices in parallel

†Solid tantalum

National Semiconductor Corporation

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

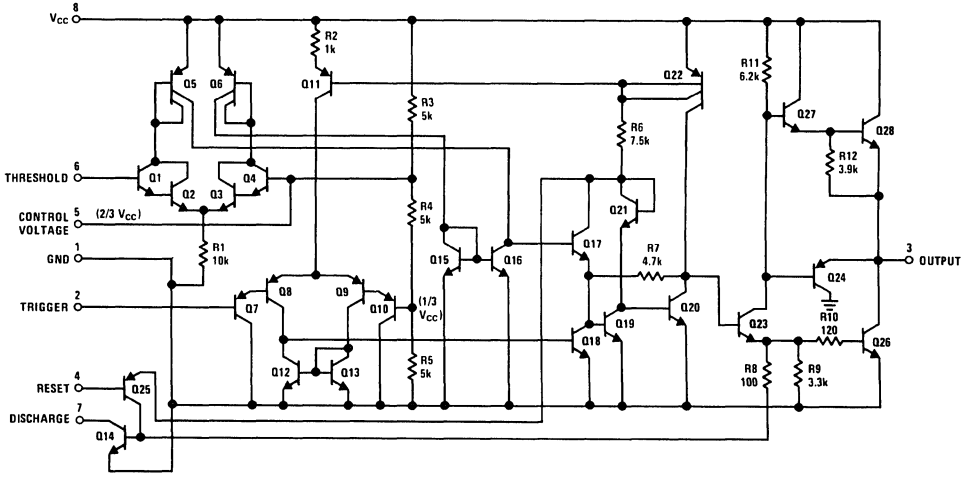
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



TL/H/7851–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage +18V

Power Dissipation (Note 1) LM555H, LM555CH 760 mW
LM555N, LM555CN 1180 mW

Operating Temperature Ranges
LM555C 0°C to +70°C
LM555 −55°C to + 125°C

Storage Temperature Range −65°C to +150°C

Soldering Information
Dual-In-Line Package
Soldering (10 Seconds) 260°C
Small Outline Package
Vapor Phase (60 Seconds) 215°C
Infrared (15 Seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞ V_{CC} = 5V, R_L = ∞ (Low State) (Note 2)		3 10	5 12		3 10	6 15	mA mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A, R_B = 1k to 100 k, C = 0.1 μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V V_{CC} = 5V	4.8 1.45	5 1.67	5.2 1.9		5 1.67		V V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V V_{CC} = 5V	9.6 2.9	10 3.33	10.4 3.8	9 2.6	10 3.33	11 4	V V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Electrical Characteristics $T_A = 25°C$, $V_{CC} = +5V$ to $+15V$, (unless othewise specified) (Continued)

Parameter	Conditions	Limits						Units
		LM555			LM555C			
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	$V_{CC} = 15V$							
	$I_{SINK} = 10$ mA		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50$ mA		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100$ mA		2	2.2		2	2.5	V
	$I_{SINK} = 200$ mA		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8$ mA		0.1	0.25				V
	$I_{SINK} = 5$ mA					0.25	0.35	V
Output Voltage Drop (High)	$I_{SOURCE} = 200$ mA, $V_{CC} = 15V$		12.5			12.5		V
	$I_{SOURCE} = 100$ mA, $V_{CC} = 15V$	13	13.3		12.75	13.3		V
	$V_{CC} = 5V$	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 164°c/w (T0-5), 106°c/w (DIP) and 170°c/w (S0-8) junction to ambient.

Note 2: Supply current when output high typically 1 mA less at $V_{CC} = 5V$.

Note 3: Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.

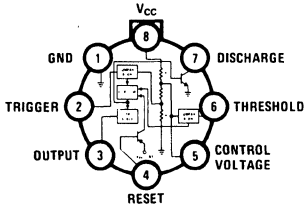
Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Note 6: Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

Connection Diagrams

Metal Can Package

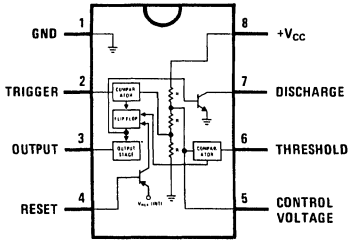


TL/H/7851–2

Top View

Order Number LM555H or LM555CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



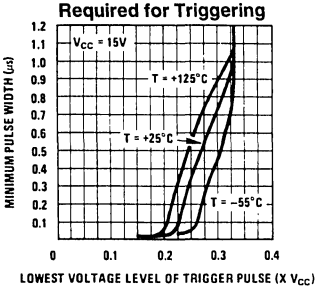
TL/H/7851–3

Top View

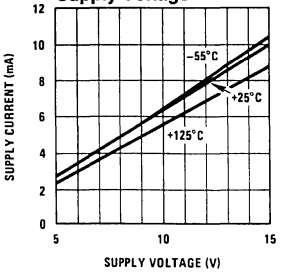
Order Number LM555J, LM555CJ, LM555CM or LM555CN
See NS Package Number J08A, M08A or N08B

Typical Performance Characteristics

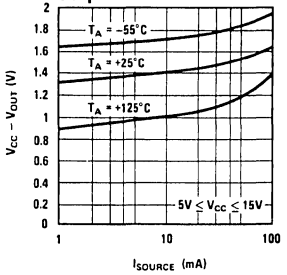
Minimuim Pulse Width Required for Triggering



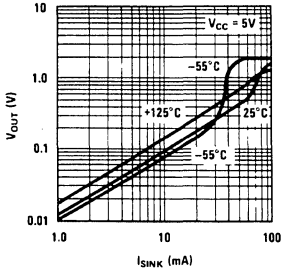
Supply Current vs Supply Voltage



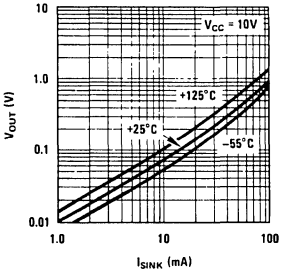
High Output Voltage vs Output Source Current



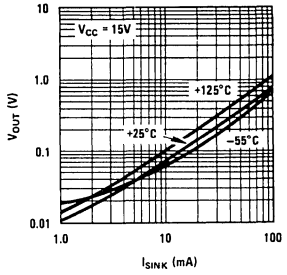
Low Output Voltage vs Output Sink Current



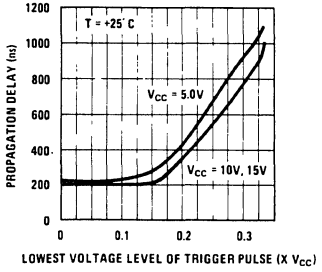
Low Output Voltage vs Output Sink Current



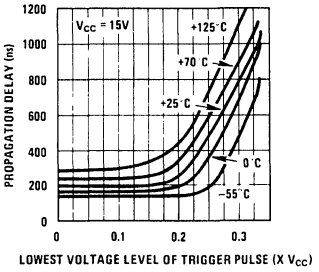
Low Output Voltage vs Output Sink Current



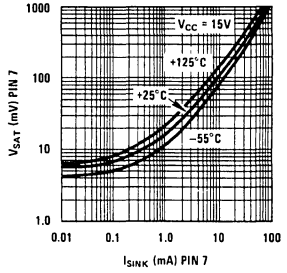
Output Propagation Delay vs Voltage Level of Trigger Pulse



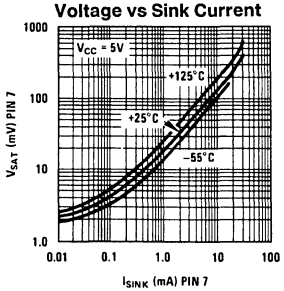
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



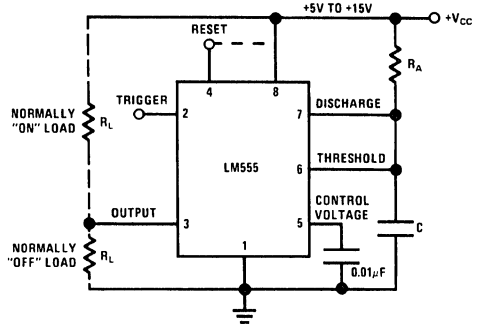
TL/H/7851–4

5

Application Information

MONOSTABLE OPERATION

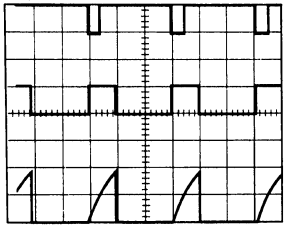
In this mode of operation, the timer functions as a one-shot *(Figure 1)*. The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.



TL/H/7851–5

FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of t = 1.1 R_A C, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.



TL/H/7851–6

V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 9.1 kΩ
C = 0.01 μF

Top Trace: Input 5V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 2V/Div.

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

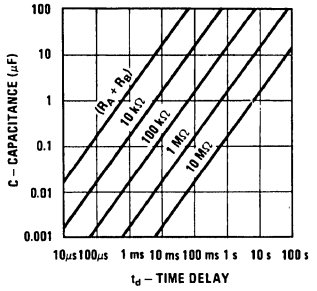
When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

ASTABLE OPERATION

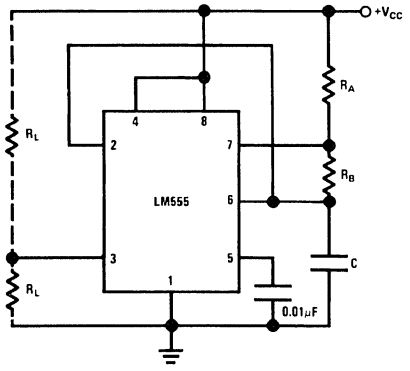
If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a



TL/H/7851–7

FIGURE 3. Time Delay

multivibrator. The external capacitor charges through R_A + R_B and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.



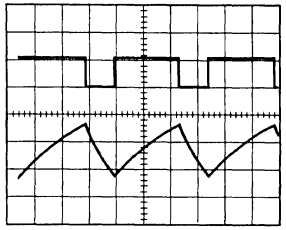
TL/H/7851–8

FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



TL/H/7851–9

V_{CC} = 5V — Top Trace: Output 5V/Div.
TIME = 20 μs/DIV. — Bottom Trace: Capacitor Voltage 1V/Div.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

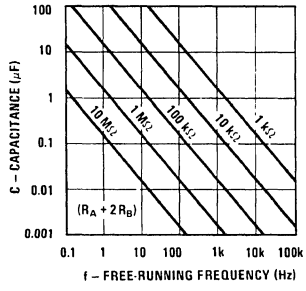
$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is: $D = \dfrac{R_B}{R_A + 2R_B}$

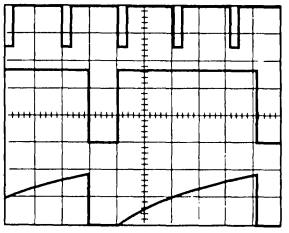


TL/H/7851–10

FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.



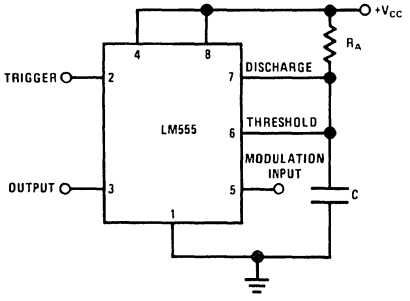
TL/H/7851–11

V_{CC} = 5V — Top Trace: Input 4V/Div.
TIME = 20 μs/DIV. — Middle Trace: Output 2V/Div.
R_A = 9.1 kΩ — Bottom Trace: Capacitor 2V/Div.
C = 0.01 μF

FIGURE 7. Frequency Divider

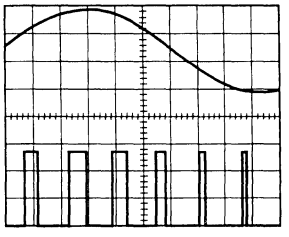
PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.



TL/H/7851–12

FIGURE 8. Pulse Width Modulator



TL/H/7851–13

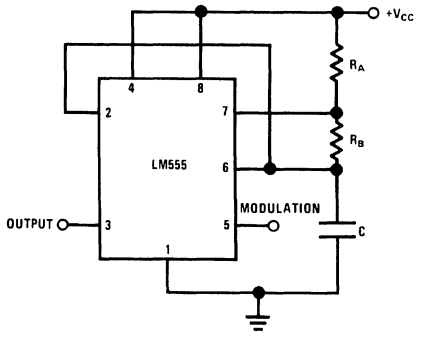
V_{CC} = 5V — Top Trace: Modulation 1V/Div.
TIME = 0.2 ms/DIV. — Bottom Trace: Capacitor Voltage 2V/Div.
R_A = 9.1 kΩ
C = 0.01 μF

FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

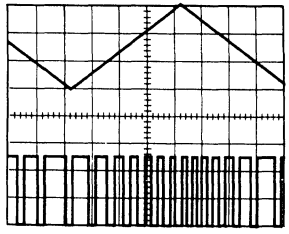
This application uses the timer connected for astable operation, as in *Figure 10,* with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

Applications Information (Continued)



TL/H/7851–14

FIGURE 10. Pulse Position Modulator



TL/H/7851–15

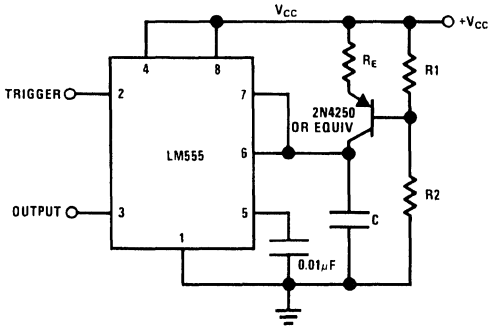
V_{CC} = 5V
TIME = 0.1 ms/DIV.
R_A = 3.9 kΩ
R_B = 3 kΩ
C = 0.01 μF

Top Trace: Modulation Input 1V/Div.
Bottom Trace: Output 2V/Div.

FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.



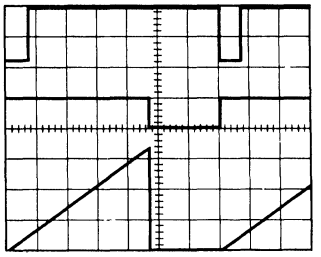
TL/H/7851–16

FIGURE 12

Figure 13 shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3\, V_{CC}\, R_E\, (R_1 + R_2)\, C}{R_1\, V_{CC} - V_{BE}\, (R_1 + R_2)}$$

$$V_{BE} \cong 0.6V$$



TL/H/7851–17

V_{CC} = 5V
TIME = 20 μs/DIV.
R_1 = 47 kΩ
R_2 = 100 kΩ
R_E = 2.7 kΩ
C = 0.01 μF

Top Trace: Input 3V/Div.
Middle Trace: Output 5V/Div.
Bottom Trace: Capacitor Voltage 1V/Div.

FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

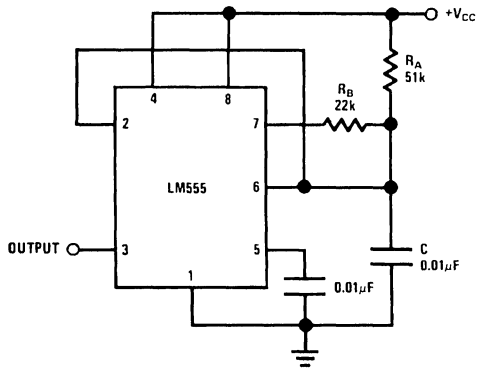
For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14.* The time period for the out-

Applications Information (Continued)

put high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$\left[(R_A\ R_B)/(R_A + R_B)\right] C \ln\left[\frac{R_A - 2R_B}{2R_A - R_B}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$



TL/H/7851–18

FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1 μF in parallel with 1 μF electrolytic.

Lower comparator storage time can be as long as 10 μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10 μs minimum.

Delay time reset to output is 0.47 μs typical. Minimum reset pulse width must be 0.3 μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

National Semiconductor Corporation

PRELIMINARY

LM556/LM556C Dual Timer

General Description

The LM556 Dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

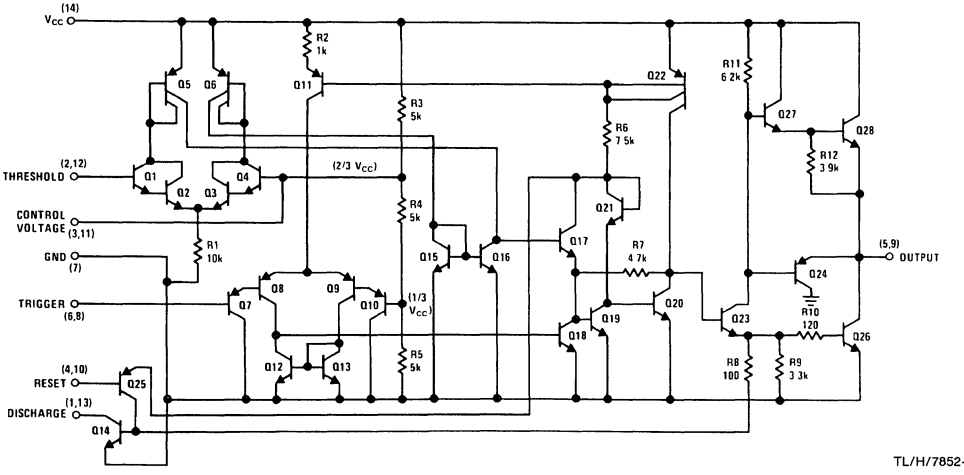
Features

- Direct replacement for SE556/NE556
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

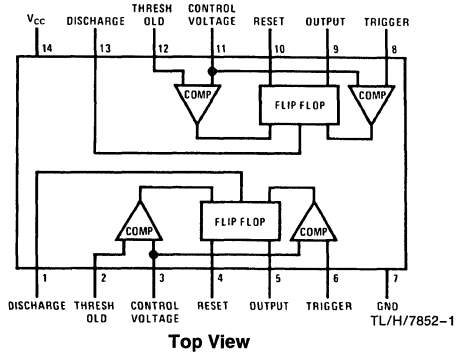
Schematic Diagram



TL/H/7852–2

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7852–1

Top View

Order Number LM556J or LM556CJ
See NS Package Number J14A

Order Number LM556CM
See NS Package Number M14A

Order Number LM556CN
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage +18V

Power Dissipation (Note 1)
- LM556J, LM556CJ 1785 mW
- LM556CN 1620 mW

Operating Temperature Ranges
- LM556C 0°C to +70°C
- LM556 −55°C to +125°C

Storage Temperature Range −65°C to +150°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

Parameter	Conditions	LM556			LM556C			Units
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
(Each Timer Section)	V_{CC} = 15V, R_L = ∞		10	11		10	14	mA
	(Low State) (Note 2)							
Timing Error, Monostable								
Initial Accuracy			0.5			0.75		%
Drift with Temperature	R_A, R_B = 1k to 100k, C = 0.1 μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2	4.5	5	5.5	V
	V_{CC} = 5V	1.45	1.67	1.9	1.25	1.67	2.0	V
Trigger Current			0.1	0.5		0.2	1.0	μA
Reset Voltage	(Note 4)	0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.6	mA
Threshold Current	V_{TH} = V-Control (Note 5)		0.03	0.1		0.03	0.1	μA
	V_{TH} = 11.2V			250			250	nA
Control Voltage Level and	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
Threshold Voltage	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 1, 13 Leakage Output High			1	100		1	100	nA
Pin 1, 13 Sat	(Note 6)							
Output Low	V_{CC} = 15V, I = 15 mA		150	240		180	300	mV
Output Low	V_{CC} = 4.5V, I = 4.5 mA		70	100		80	200	mV

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified) (Continued)

Parameter	Conditions	LM556			LM556C			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.25		2	2.75	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Matching Characteristics	(Note 7)							
Initial Timing Accuracy			0.05	0.2		0.1	2.0	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%/V

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 70°C/W (Ceramic), 77°C/W (Plastic DIP) and 110°C/W (SO-14 Narrow).

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: As reset voltage lowers, timing is inhibited and then the output goes low.

Note 5: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

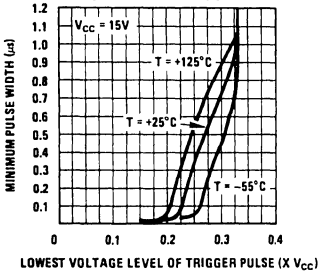
Note 6: No protection against excessive pin 1, 13 current is necessary providing the package dissipation rating will not be exceeded.

Note 7: Matching characteristics refer to the difference between performance characteristics of each timer section.

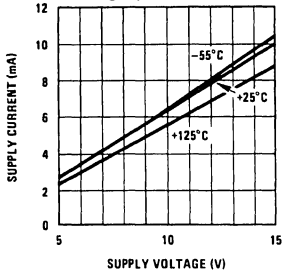
Note 8: Refer to RETS556X drawing for specifications of military LM556J version.

Typical Performance Characteristics

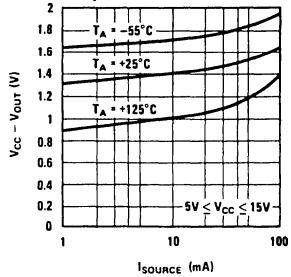
Minimum Pulse Width Required for Triggering



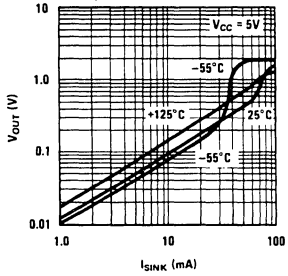
Supply Current vs Supply Voltage (Each Section)



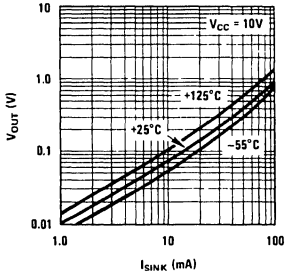
High Output Voltage vs Output Source Current



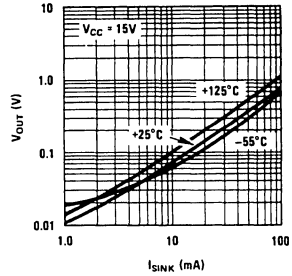
Low Output Voltage vs Output Sink Current



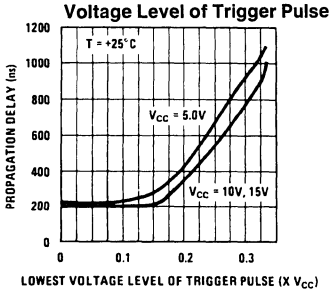
Low Output Voltage vs Output Sink Current



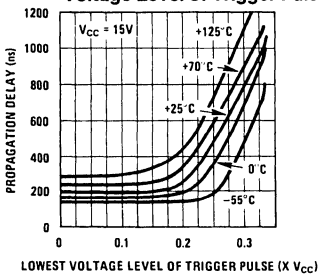
Low Output Voltage vs Output Sink Current



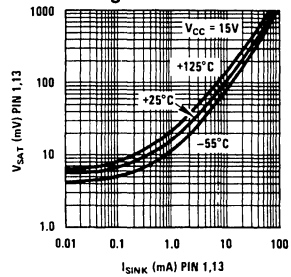
Output Propagation Delay vs Voltage Level of Trigger Pulse



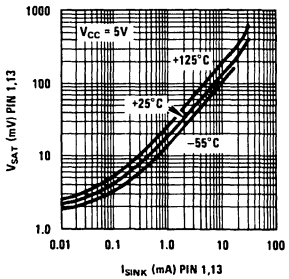
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 1, 13) Voltage vs Sink Current



Discharge Transistor (Pin 1, 13) Voltage vs Sink Current



TL/H/7852–3

National Semiconductor Corporation

LM565/LM565C Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CH and LM565CN are specified for operation over the 0°C to +70°C temperature range.

Features

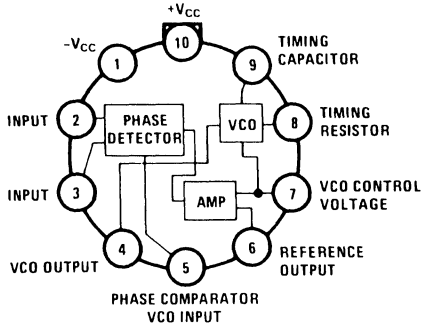
- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%

Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators

Connection Diagrams

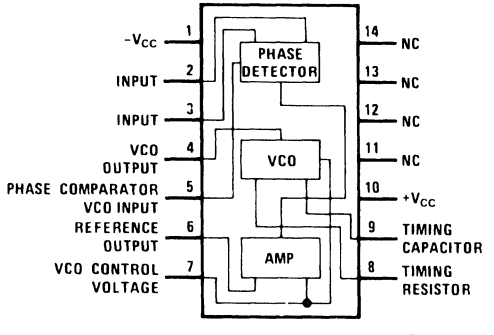
Metal Can Package



TL/H/7853-2

Order Number LM565H or LM565CH
See NS Package Number H10C

Dual-In-Line Package



TL/H/7853-3

Order Number LM565CN
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±12V
Power Dissipation (Note 1)	1400 mW
Differential Input Voltage	±1V
Operating Temperature Range	
LM565H	−55°C to +125°C
LM565CH, LM565CN	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

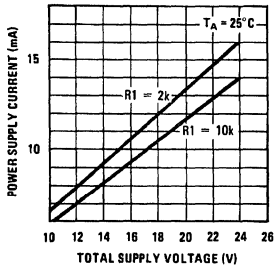
Electrical Characteristics AC Test Circuit, $T_A = 25°C$, $V_{CC} = \pm 6V$

Parameter	Conditions	LM565			LM565C			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Current			8.0	12.5		8.0	12.5	mA
Input Impedance (Pins 2, 3)	$-4V < V_2, V_3 < 0V$	7	10			5		kΩ
VCO Maximum Operating Frequency	$C_o = 2.7$ pF	300	500		250	500		kHz
VCO Free-Running Frequency	$C_o = 1.5$ nF $R_o = 20$ kΩ $f_o = 10$ kHz	−10	0	+10	−30	0	+30	%
Operating Frequency Temperature Coefficient			−100			−200		ppm/°C
Frequency Drift with Supply Voltage			0.1	1.0		0.2	1.5	%/V
Triangle Wave Output Voltage		2	2.4	3	2	2.4	3	V_{p-p}
Triangle Wave Output Linearity			0.2			0.5		%
Square Wave Output Level		4.7	5.4		4.7	5.4		V_{p-p}
Output Impedance (Pin 4)			5			5		kΩ
Square Wave Duty Cycle		45	50	55	40	50	60	%
Square Wave Rise Time			20			20		ns
Square Wave Fall Time			50			50		ns
Output Current Sink (Pin 4)		0.6	1		0.6	1		mA
VCO Sensitivity	$f_o = 10$ kHz		6600			6600		Hz/V
Demodulated Output Voltage (Pin 7)	±10% Frequency Deviation	250	300	400	200	300	450	mV_{p-p}
Total Harmonic Distortion	±10% Frequency Deviation		0.2	0.75		0.2	1.5	%
Output Impedance (Pin 7)			3.5			3.5		kΩ
DC Level (Pin 7)		4.25	4.5	4.75	4.0	4.5	5.0	V
Output Offset Voltage $\lvert V_7 - V_6 \rvert$			30	100		50	200	mV
Temperature Drift of $\lvert V_7 - V_6 \rvert$			500			500		μV/°C
AM Rejection		30	40			40		dB
Phase Detector Sensitivity K_D			.68			.68		V/radian

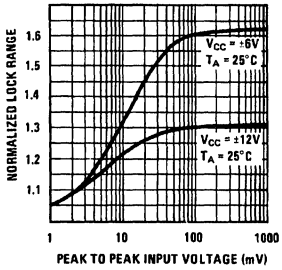
Note 1: The maximum junction temperature of the LM565 and LM565C is +150°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of +150°C/W junction to ambient or +45°C/W junction to case. Thermal resistance of the dual-in-line package is +85°C/W.

Typical Performance Characteristics

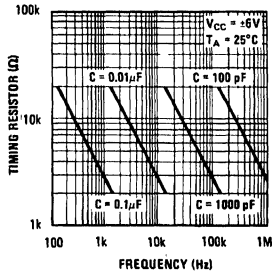
Power Supply Current as a Function of Supply Voltage



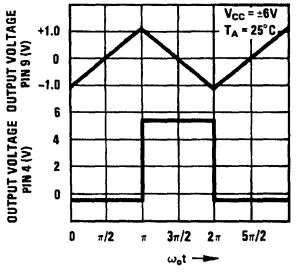
Lock Range as a Function of Input Voltage



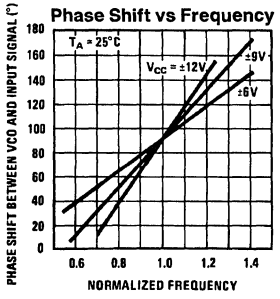
VCO Frequency



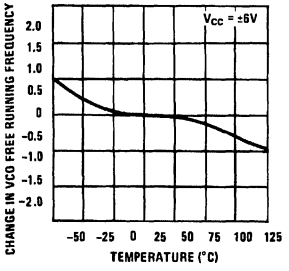
Oscillator Output Waveforms



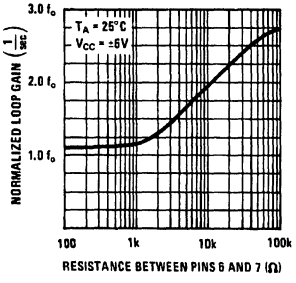
Phase Shift vs Frequency



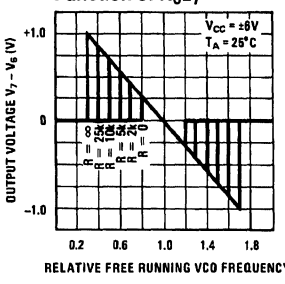
VCO Frequency as a Function of Temperature



Loop Gain vs Load Resistance

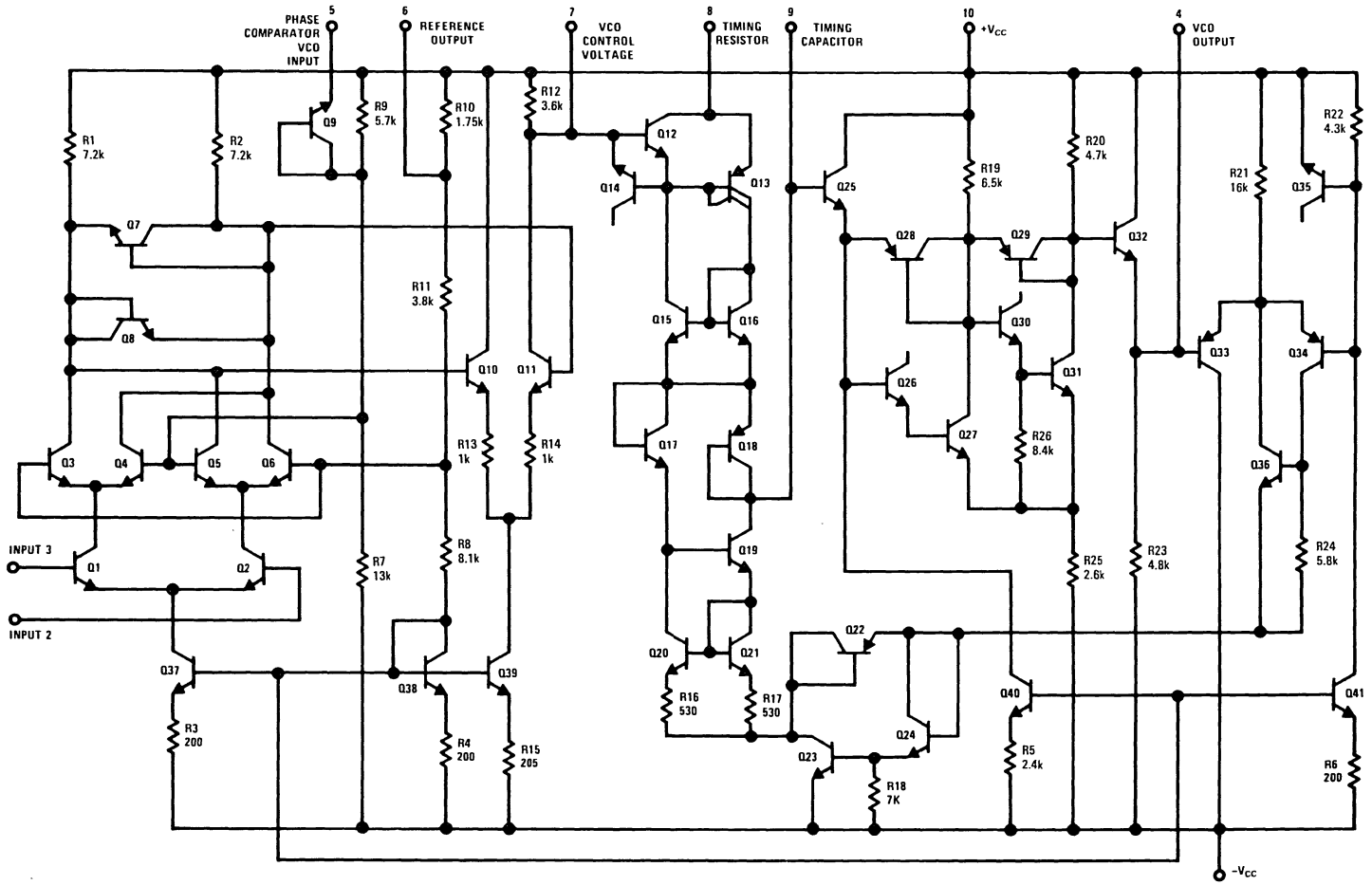


Hold in Range as a Function of R_{6-7}



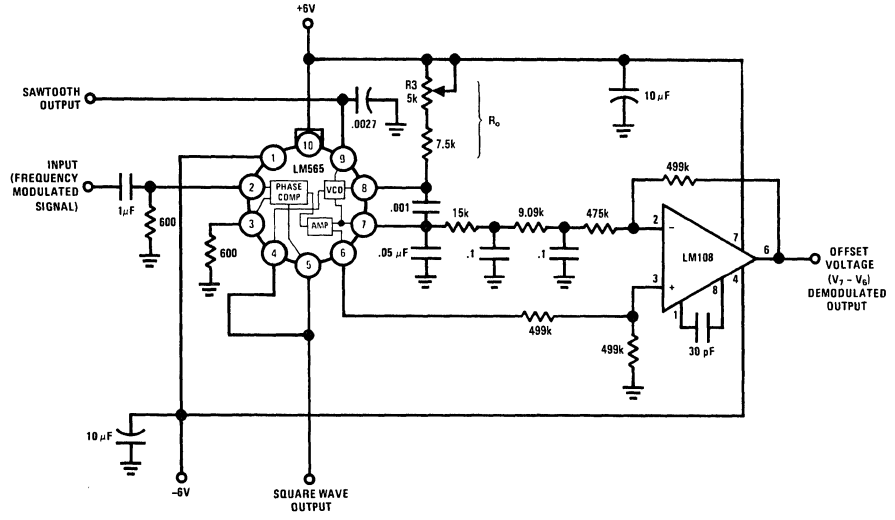
TL/H/7853–4

Schematic Diagram



TL/H/7853–1

AC Test Circuit

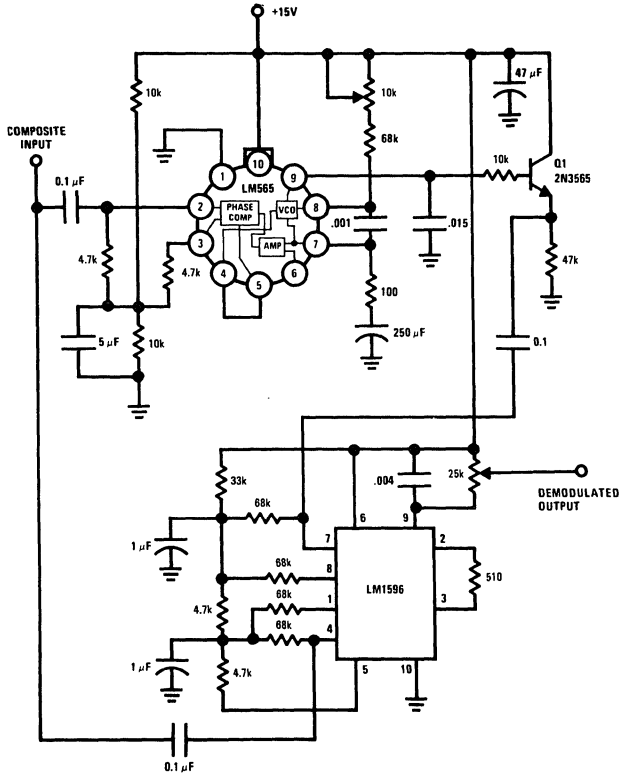


TL/H/7853–5

Note: S_1 open for output offset voltage ($V_7 - V_6$) measurement.

Typical Applications

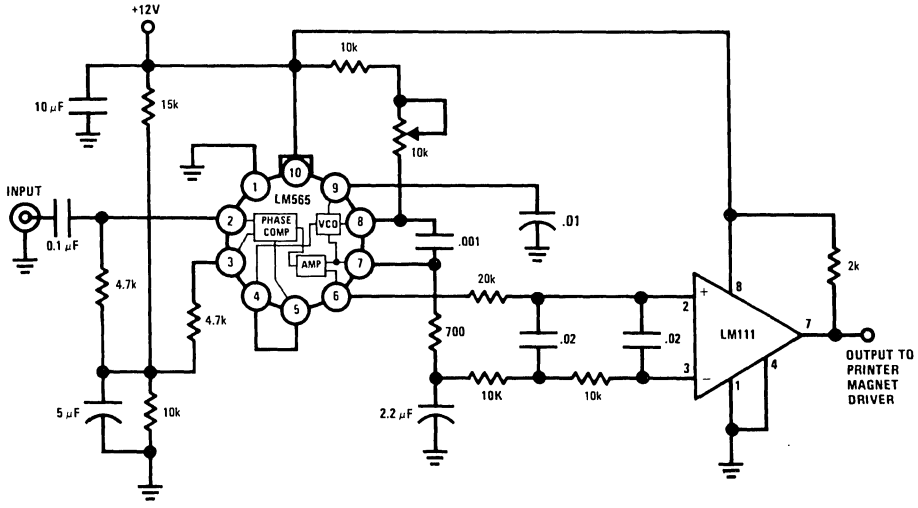
2400 Hz Synchronous AM Demodulator



TL/H/7853–6

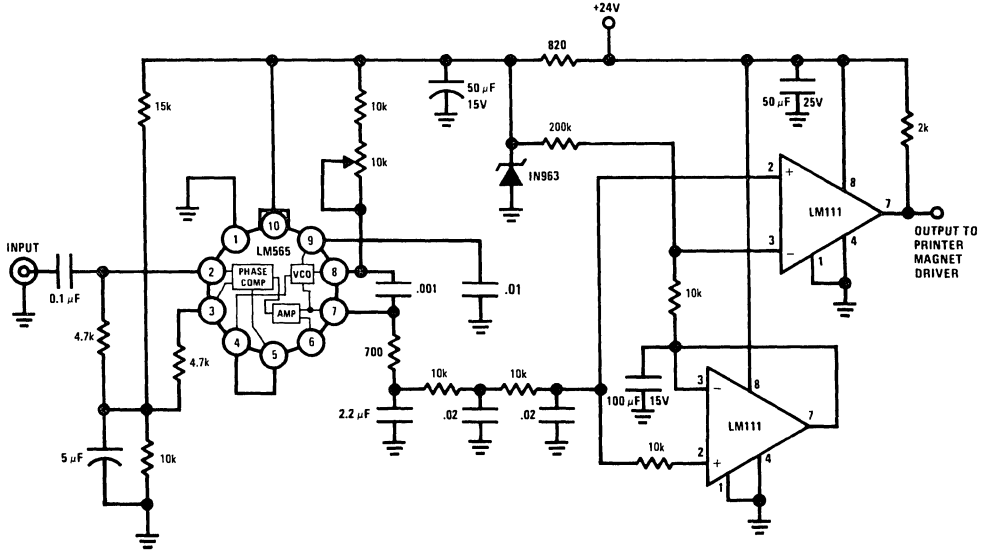
Typical Applications (Continued)

FSK Demodulator (2025–2225 cps)



TL/H/7853–7

FSK Demodulator with DC Restoration

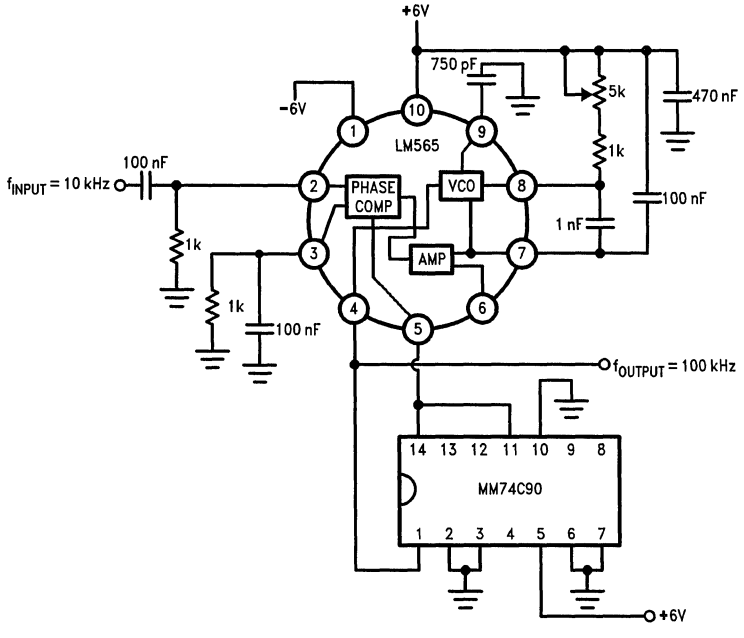


TL/H/7853–8

5

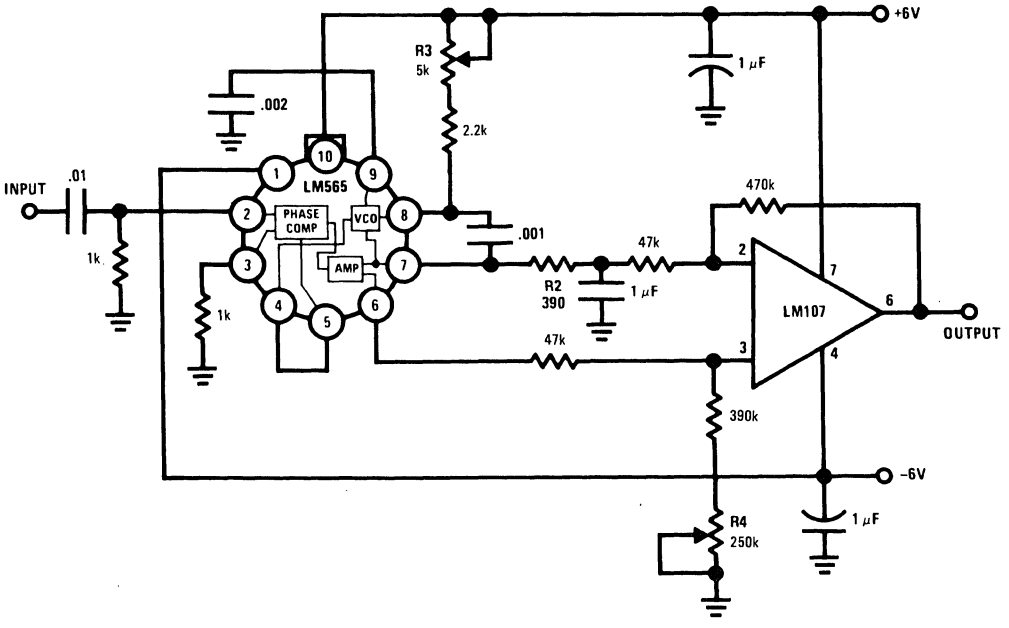
Typical Applications (Continued)

Frequency Multiplier (×10)



TL/H/7853-9

IRIG Channel 13 Demodulator



TL/H/7853-10

Applications Information

In designing with phase locked loops such as the LM565, the important parameters of interest are:

FREE RUNNING FREQUENCY

$$f_o \cong \frac{0.3}{R_o C_o}$$

LOOP GAIN: relates the amount of phase change between the input signal and the VCO signal for a shift in input signal frequency (assuming the loop remains in lock). In servo theory, this is called the "velocity error coefficient."

$$\text{Loop gain} = K_o K_D \left(\frac{1}{\text{sec}}\right)$$

$$K_o = \text{oscillator sensitivity} \left(\frac{\text{radians/sec}}{\text{volt}}\right)$$

$$K_D = \text{phase detector sensitivity} \left(\frac{\text{volts}}{\text{radian}}\right)$$

The loop gain of the LM565 is dependent on supply voltage, and may be found from:

$$K_o K_D = \frac{33.6\, f_o}{V_c}$$

f_o = VCO frequency in Hz

V_c = total supply voltage to circuit

Loop gain may be reduced by connecting a resistor between pins 6 and 7; this reduces the load impedance on the output amplifier and hence the loop gain.

HOLD IN RANGE: the range of frequencies that the loop will remain in lock after initially being locked.

$$f_H = \pm \frac{8\, f_o}{V_c}$$

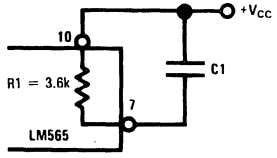
f_o = free running frequency of VCO

V_c = total supply voltage to the circuit

THE LOOP FILTER

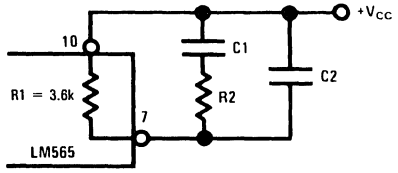
In almost all applications, it will be desirable to filter the signal at the output of the phase detector (pin 7); this filter may take one of two forms:

Simple Lag Filter



TL/H/7853–11

Lag-Lead Filter



TL/H/7853–12

A simple lag filter may be used for wide closed loop bandwidth applications such as modulation following where the frequency deviation of the carrier is fairly high (greater than 10%), or where wideband modulating signals must be followed.

The natural bandwidth of the closed loop response may be found from:

$$f_n = \frac{1}{2\pi} \sqrt{\frac{K_o K_D}{R_1 C_1}}$$

Associated with this is a damping factor:

$$\delta = \frac{1}{2} \sqrt{\frac{1}{R_1 C_1 K_o K_D}}$$

For narrow band applications where a narrow noise bandwidth is desired, such as applications involving tracking a slowly varying carrier, a lead lag filter should be used. In general, if $1/R_1C_1 < K_o K_D$, the damping factor for the loop becomes quite small resulting in large overshoot and possible instability in the transient response of the loop. In this case, the natural frequency of the loop may be found from

$$f_n = \frac{1}{2\pi} \sqrt{\frac{K_o K_D}{\tau_1 + \tau_2}}$$

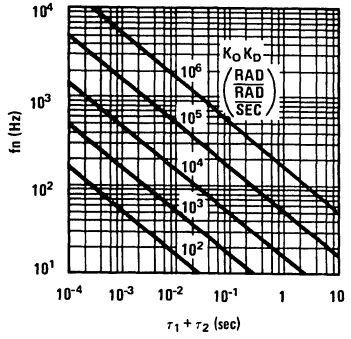
$$\tau_1 + \tau_2 = (R_1 + R_2)\, C_1$$

R_2 is selected to produce a desired damping factor δ, usually between 0.5 and 1.0. The damping factor is found from the approximation:

$$\delta \approx \pi\, \tau_2 f_n$$

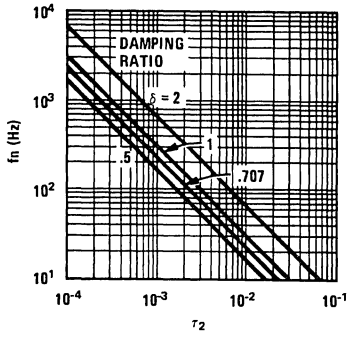
These two equations are plotted for convenience.

Filter Time Constant vs Natural Frequency



TL/H/7853–13

Damping Time Constant vs Natural Frequency



TL/H/7853–14

Capacitor C_2 should be much smaller than C_1 since its function is to provide filtering of carrier. In general $C_2 \leq 0.1\, C_1$.

5

National Semiconductor Corporation

LM566C Voltage Controlled Oscillator

General Description

The LM566CN is a general purpose voltage controlled oscillator which may be used to generate square and triangular waves, the frequency of which is a very linear function of a control voltage. The frequency is also a function of an external resistor and capacitor.

The LM566CN is specified for operation over the 0°C to +70°C temperature range.

Features

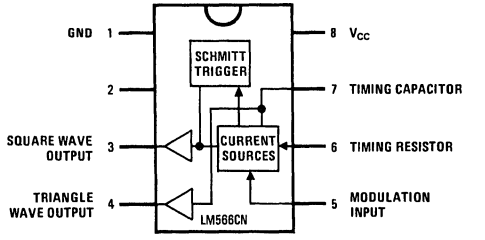
- Wide supply voltage range: 10V to 24V
- Very linear modulation characteristics
- High temperature stability
- Excellent supply voltage rejection
- 10 to 1 frequency range with fixed capacitor
- Frequency programmable by means of current, voltage, resistor or capacitor

Applications

- FM modulation
- Signal generation
- Function generation
- Frequency shift keying
- Tone generation

Connection Diagram

Dual-In-Line Package

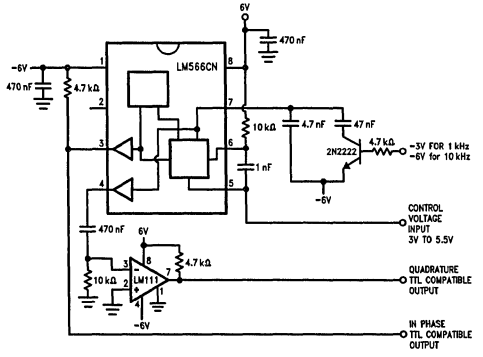


TL/H/7854–2

Order Number LM566CN
See NS Package Number N08E

Typical Application

1 kHz and 10 kHz TTL Compatible Voltage Controlled Oscillator



TL/H/7854–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	26V
Power Dissipation (Note 1)	1000 mW
Operating Temperature Range, LM566CN	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	+260°C

Electrical Characteristics V_{CC} = 12V, T_A = 25°C, AC Test Circuit

Parameter	Conditions	LM566C			Units
		Min	Typ	Max	
Maximum Operating Frequency	R0 = 2k C0 = 2.7 pF	0.5	1		MHz
VCO Free-Running Frequency	C_O = 1.5 nF R_O = 20k f_O = 10 kHz	−30	0	+30	%
Input Voltage Range Pin 5		¾ V_{CC}		V_{CC}	
Average Temperature Coefficient of Operating Frequency			200		ppm/°C
Supply Voltage Rejection	10–20V		0.1	2	%/V
Input Impedance Pin 5		0.5	1		MΩ
VCO Sensitivity	For Pin 5, From 8–10V, f_O = 10 kHz	6.0	6.6	7.2	kHz/V
FM Distortion	±10% Deviation		0.2	1.5	%
Maximum Sweep Rate			1		MHz
Sweep Range			10:1		
Output Impedance Pin 3			50		Ω
Pin 4			50		Ω
Square Wave Output Level	R_{L1} = 10k	5.0	5.4		Vp-p
Triangle Wave Output Level	R_{L2} = 10k	2.0	2.4		Vp-p
Square Wave Duty Cycle		40	50	60	%
Square Wave Rise Time			20		ns
Square Wave Fall Time			50		ns
Triangle Wave Linearity	+1V Segment at ½ V_{CC}		0.5		%

Note 1: The maximum junction temperature of the LM566CN is 150°C. For operation at elevated junction temperatures, maximum power dissipation must be derated based on a thermal resistance of 115°C/W, junction to ambient.

Applications Information

The LM566CN may be operated from either a single supply as shown in this test circuit, or from a split (±) power supply. When operating from a split supply, the square wave output (pin 3) is TTL compatible (2 mA current sink) with the addition of a 4.7 kΩ resistor from pin 3 to ground.

A 0.001 μF capacitor is connected between pins 5 and 6 to prevent parasitic oscillations that may occur during VCO switching.

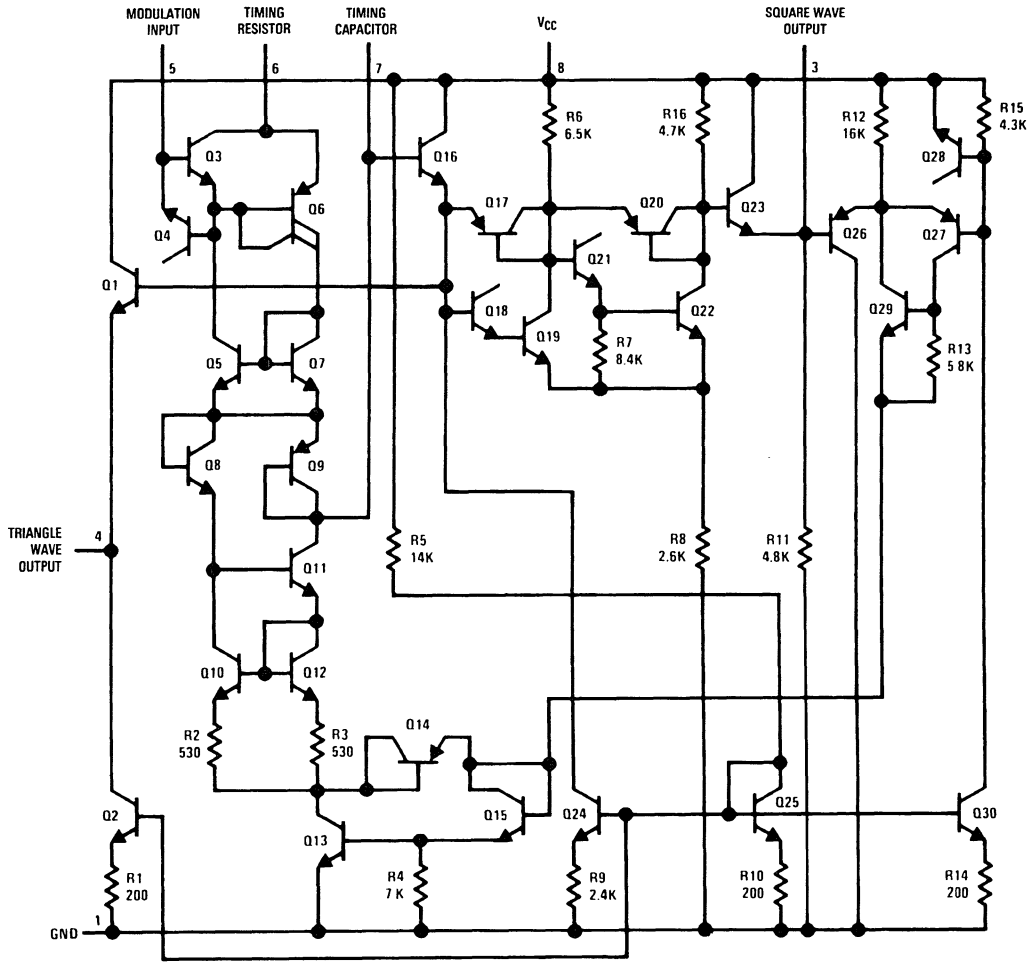
$$f_O = \frac{2.4(V^+ - V_5)}{R_O C_O V^+}$$

where

$2K < R_O < 20K$

and V_5 is voltage between pin 5 and pin 1.

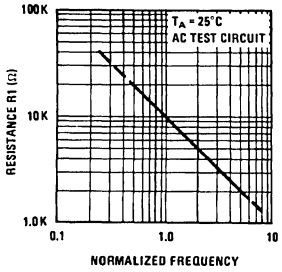
Schematic Diagram



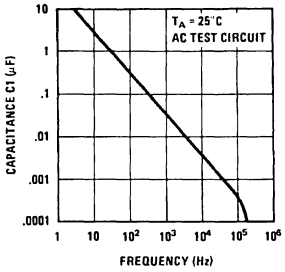
TL/H/7854–1

Typical Performance Characteristics

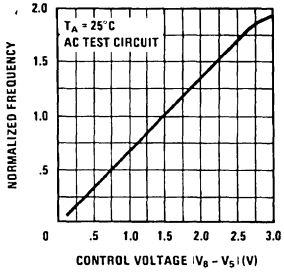
Operating Frequency as a Function of Timing Resistor



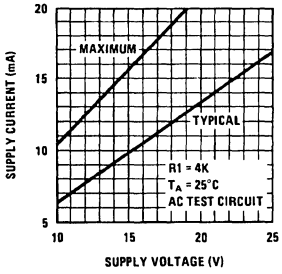
Operating Frequency as a Function of Timing Capacitor



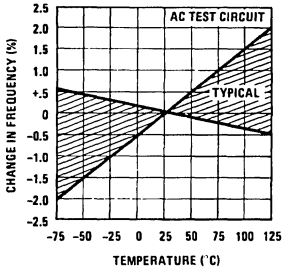
Normalized Frequency as a Function of Control Voltage



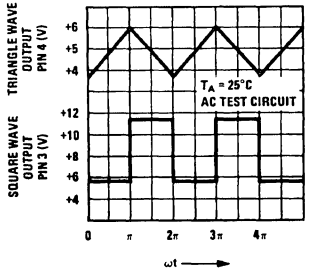
Power Supply Current



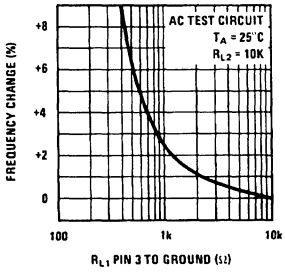
Temperature Stability



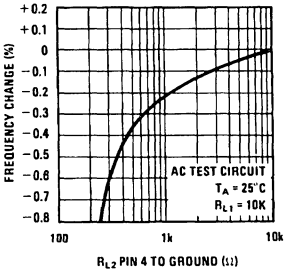
VCO Waveforms



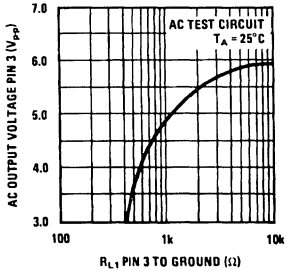
Frequency Stability vs Load Resistance (Square Wave Output)



Frequency Stability vs Load Impedance (Triangle Output)

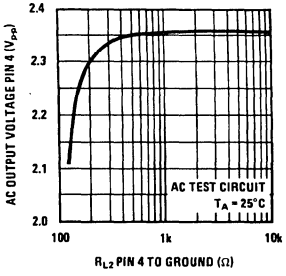


Square Wave Output Characteristics



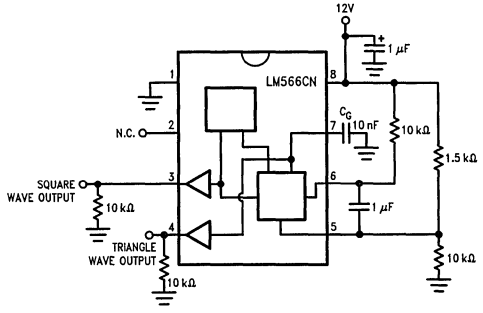
TL/H/7854-4

Triangle Wave Output Characteristics



TL/H/7854-5

AC Test Circuit



TL/H/7854-6

National Semiconductor Corporation

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

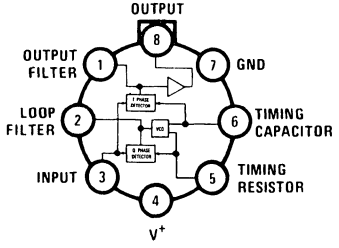
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

Connection Diagrams

Metal Can Package

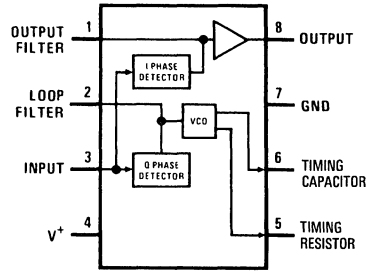


TL/H/6975–1

Top View

Order Number LM567H or LM567CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



TL/H/6975–2

Top View

Order Number LM567CM
See NS Package Number M08A

Order Number LM567CN
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage Pin	9V
Power Dissipation (Note 1)	1100 mW
V_8	15V
V_3	−10V
V_3	V_4 + 0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
LM567H	−55°C to +125°C
LM567CH, LM567CM, LM567CN	0°C to +70°C

Soldering Information

Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

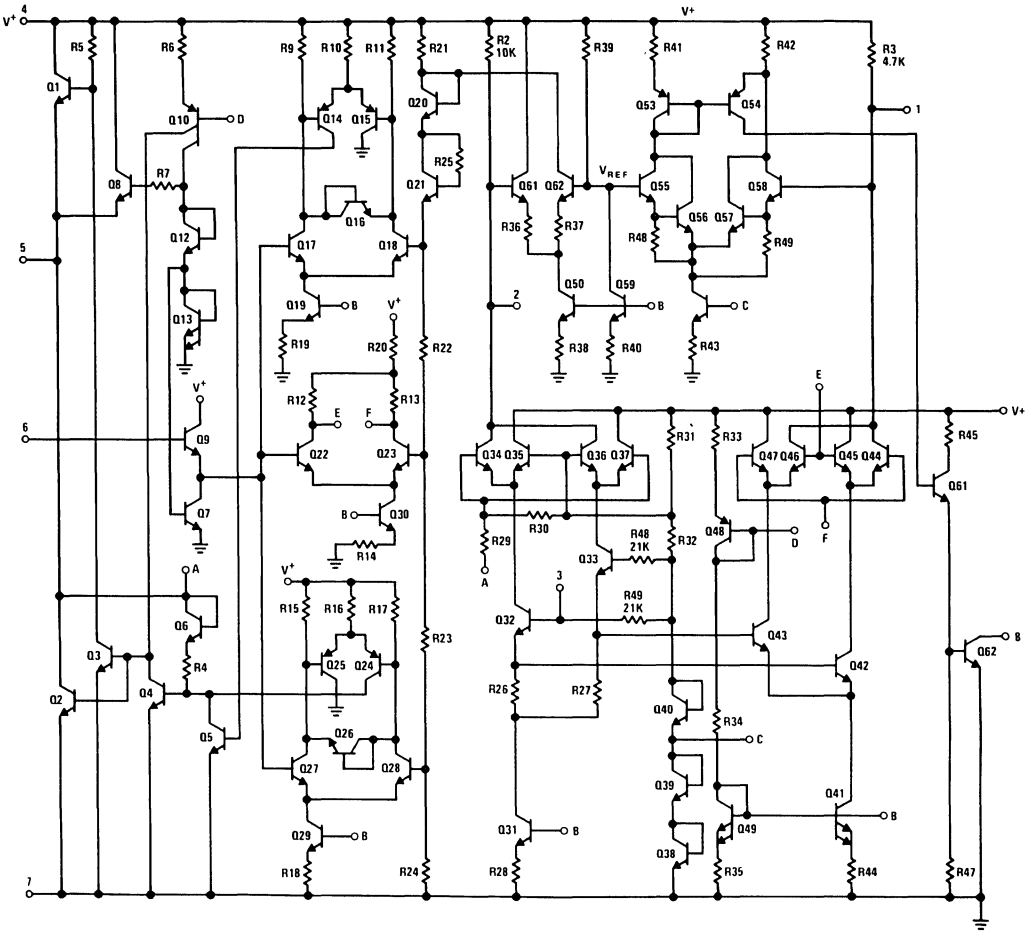
Electrical Characteristics AC Test Circuit, T_A = 25°C, V^+ = 5V

Parameters	Conditions	LM567			LM567C/LM567CM			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range		4.75	5.0	9.0	4.75	5.0	9.0	V
Power Supply Current Quiescent	R_L = 20k		6	8		7	10	mA
Power Supply Current Activated	R_L = 20k		11	13		12	15	mA
Input Resistance		18	20		15	20		kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25		20	25	mVrms
Largest No Output Input Voltage	I_C = 100 mA, $f_i = f_o$	10	15		10	15		mVrms
Largest Simultaneous Outband Signal to Inband Signal Ratio			6			6		dB
Minimum Input Signal to Wideband Noise Ratio	B_n = 140 kHz		−6			−6		dB
Largest Detection Bandwidth		12	14	16	10	14	18	% of f_o
Largest Detection Bandwidth Skew			1	2		2	3	% of f_o
Largest Detection Bandwidth Variation with Temperature			±0.1			±0.1		%/°C
Largest Detection Bandwidth Variation with Supply Voltage	4.75 − 6.75V		±1	±2		±1	±5	%V
Highest Center Frequency		100	500		100	500		kHz
Center Frequency Stability (4.75–5.75V)	$0 < T_A < 70$ $-55 < T_A < +125$		35 ± 60 35 ± 140			35 ±60 35 ± 140		ppm/°C ppm/°C
Center Frequency Shift with Supply Voltage	4.75V − 6.75V 4.75V − 9V		0.5	1.0 2.0		0.4	2.0 2.0	%/V %/V
Fastest ON-OFF Cycling Rate			f_o/20			f_o/20		
Output Leakage Current	V_8 = 15V		0.01	25		0.01	25	μA
Output Saturation Voltage	e_i = 25 mV, I_8 = 30 mA e_i = 25 mV, I_8 = 100 mA		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	V
Output Fall Time			30			30		ns
Output Rise Time			150			150		ns

Note 1: The maximum junction temperature of the LM567 and LM567C is 150°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 110°C/W, junction to ambient. For the Small Outline package, the device must be derated based on a thermal resistance of 160°C/W, junction to ambient.

Note 2: Refer to RETS567X drawing for specifications of military LM567H version.

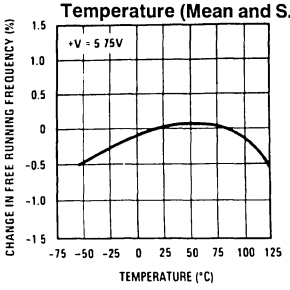
Schematic Diagram



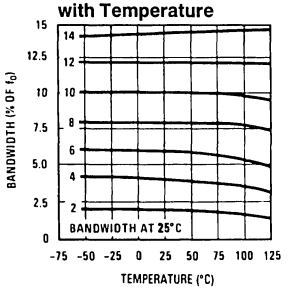
TL/H/6975–3

Typical Performance Characteristics

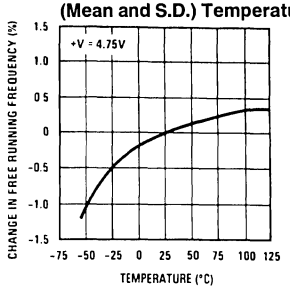
Typical Frequency Drift with Temperature (Mean and S.D.)



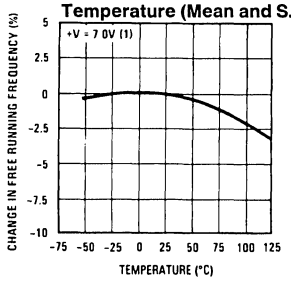
Typical Bandwidth Variation with Temperature



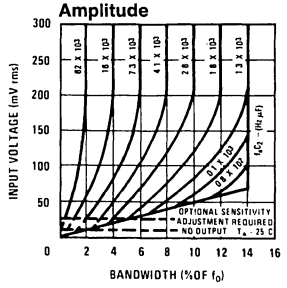
Typical Frequency Drift with (Mean and S.D.) Temperature



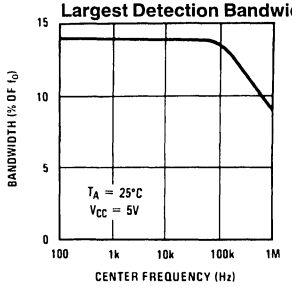
Typical Frequency Drift with Temperature (Mean and S.D.)



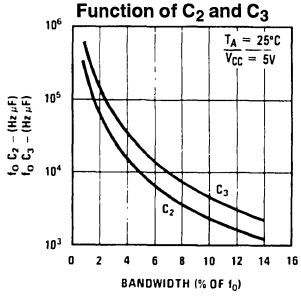
Bandwidth vs Input Signal Amplitude



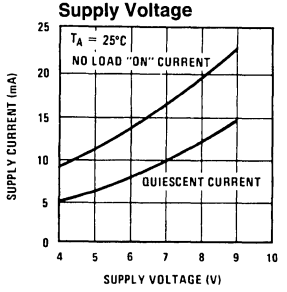
Largest Detection Bandwidth



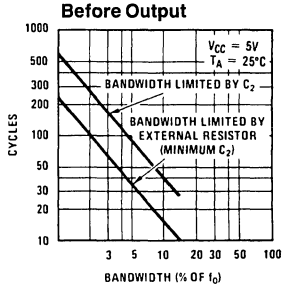
Detection Bandwidth as a Function of C_2 and C_3



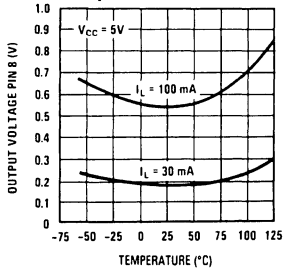
Typical Supply Current vs Supply Voltage



Greatest Number of Cycles Before Output



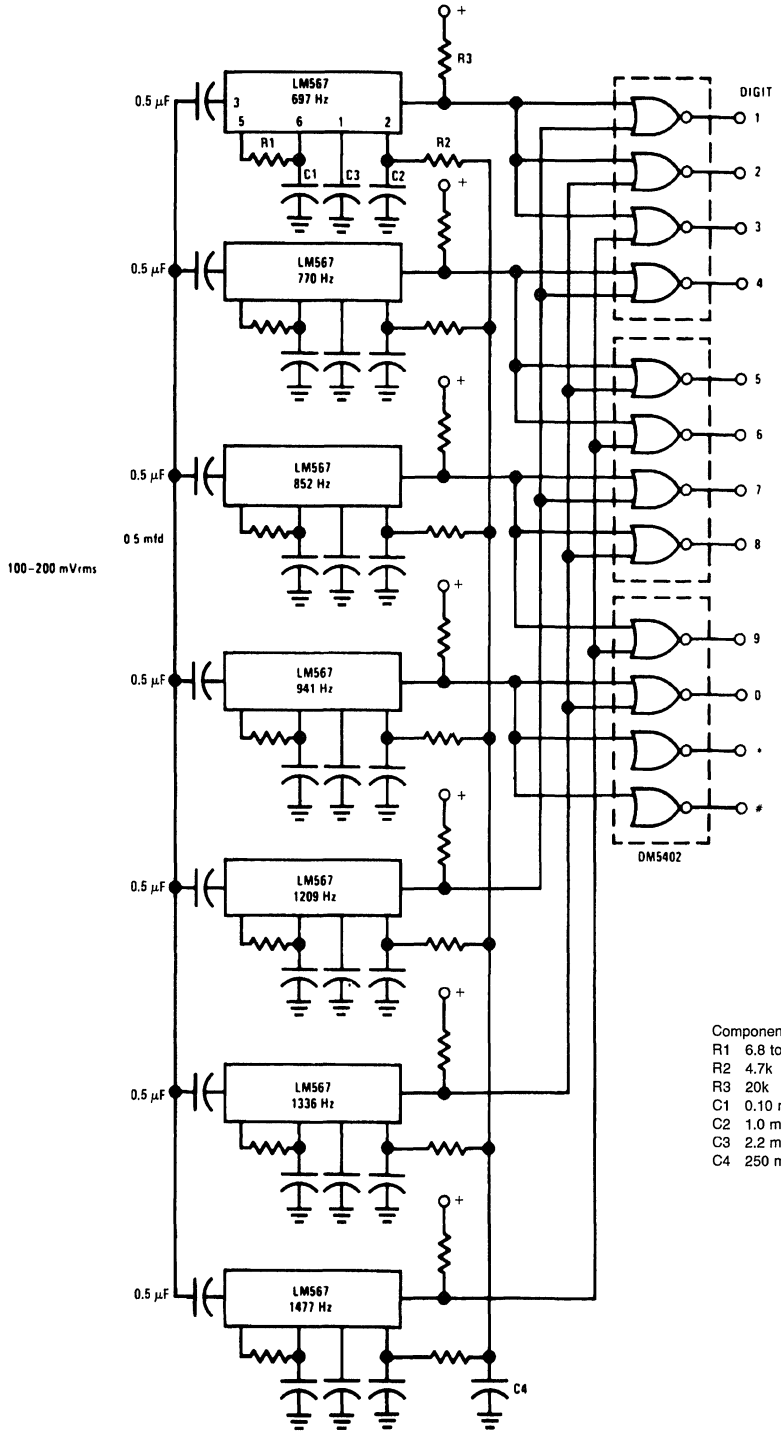
Typical Output Voltage vs Temperature



TL/H/6975–4

Typical Applications

Touch-Tone Decoder

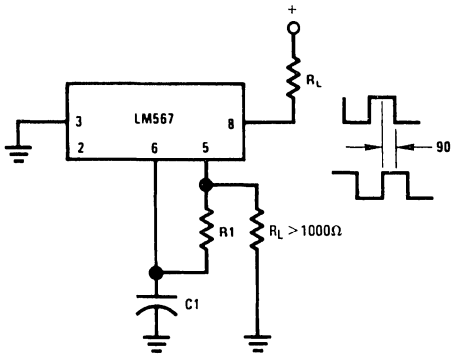


Component values (typ)
R1 6.8 to 15k
R2 4.7k
R3 20k
C1 0.10 mfd
C2 1.0 mfd 6V
C3 2.2 mfd 6V
C4 250 mfd 6V

TL/H/6975–5

Typical Applications (Continued)

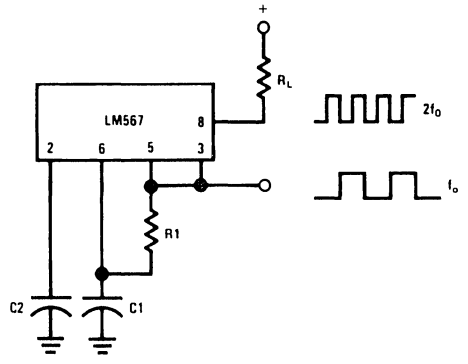
Oscillator with Quadrature Output



TL/H/6975–6

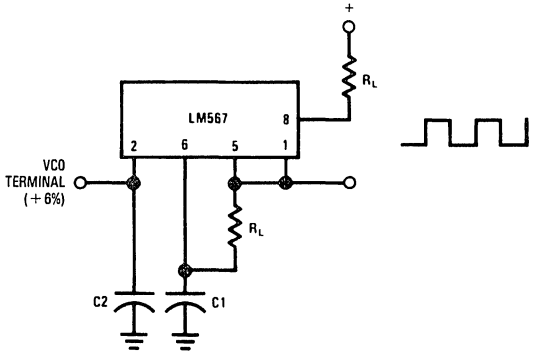
Connect Pin 3 to 2.8V to Invert Output

Oscillator with Double Frequency Output



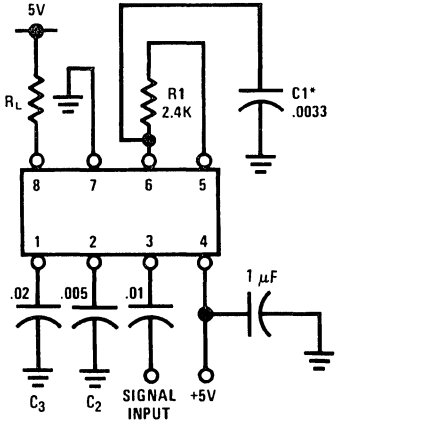
TL/H/6975–7

Precision Oscillator Drive 100 mA Loads



TL/H/6975–8

AC Test Circuit



TL/H/6975–9

f_i = 100 kHz + 5V

***Note:** Adjust for f_o = 100 kHz.

Applications Information

The center frequency of the tone decoder is equal to the free running frequency of the VCO. This is given by

$$f_o \cong \frac{1}{1.1\ R_1 C_1}$$

The bandwidth of the filter may be found from the approximation

$$BW = 1070\sqrt{\frac{V_i}{f_o C_2}} \text{ in \% of } f_o$$

Where:

V_i = Input voltage (volts rms), $V_i \leq 200$ mV

C_2 = Capacitance at Pin 2 (μF)

5

National Semiconductor Corporation

LM903 Fluid Level Detector

General Description

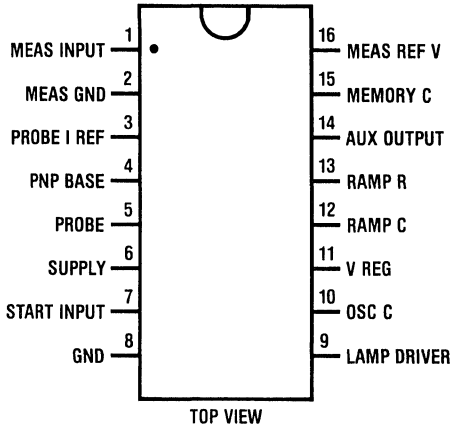
The LM903 uses the thermal-resistive probe technique to measure the level of nonflammable fluids. A low fluid level is indicated by a warning lamp operating in continuous or flashing mode. All supervisory requirements to control the thermal-resistive probe, including short and open circuit probe detection, are incorporated within the device. The circuit has possible applications in the detection of hydraulic fluid, oil level, etc., and may be used with partially conducting fluids.

Features

- Flashing or continuous warning indication
- Warning threshold externally adjustable
- Control circuitry for thermal-resistive probe
- Switch on reset and delay to avoid transients
- 600 mA flashing lamp drive capability
- Short and open circuit probe detection
- 70V transient protection on supply and control input
- 7V–18V supply range
- Internally regulated supply
- −40°C to +80°C operation

Connection Diagram

Dual-In-Line Package



TL/H/5699–1

Order Number LM903N
See NS Package Number N16E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	18V
Control Input Voltage (Pin 7)	18V
Transient Voltage (Pins, 6, 7, 9) 10 ms (Note 1)	70V
Output Current (Pin 4) I_4 (Sink)	10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature	−55°C to +150°C
Maximum Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

V_{CC} = 12V, C_T = 33 μF, R_T = 7.5 kΩ, T_A within operating range except where stated otherwise

Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		7.0	18	7.0	13	18	V
I_S	Supply Current			50			50	mA
V_{REG}	Regulated Voltage		5.5	6.2	5.3	5.8	6.3	V
	Regulation Temperature Drift	V_{CC} = 7.2V–18V		105		 500		mV μV/°C
V_6–V_3	Probe Current Reference Voltage		2.0	2.35	1.95	2.20	2.40	V
V_{REF}	Measurement Reference Voltage		790	900	780	850	910	mV
R_{REF}	Reference Input Resistor					1.2		kΩ
V_7	Start Input Logic High Level				1.6			V
V_7	Start Input Logic Low Level						1.0	V
I_7	High Input Current	Latch Off					100	nA
I_7	Latch Holding Current	Latch On				2.5		nA
R_7	Resistance Pin 7	Latch On				22		kΩ
I_{12}	Ramp Current	See Timing Diagram						
	Charging	V_{12} = 0V–1V	600	1100	590		1100	μA
		V_{12} = 1V–4V	53	93	50		96	μA
	Discharging	V_{12} = 4.1V	−700	−450	−710		−440	μA
		V_{12} = 0.5V	−650	−400	−660		−390	μA
V_{12}	Ramp Threshold	See Timing Diagram						
	Probe Current Start		570	850	550	710	870	mV
	First Measurement		910	1200	890	1055	1220	mV
	Second Measurement		910	1240	890	1080	1270	mV
V_1	Probe Input Voltage Range	V_{CC} = 7.5V–18V			1		V_{REG} − 1.0	V
V_5	Probe Open-Circuit Threshold	At Pin 5			V_{REG} − 0.85	V_{REG} − 0.6		V
V_5	Probe Short-Circuit Threshold					0.6	0.85	V
I_1	Pin 1 Input Leakage Current	Pin 1 = 300 mV	−3.5	+3.5			+5.0	nA
I_{15}	Pin 15 Leakage Current	V_{15} = 2V, V_7 = 12V	−3.5	3.5				μA
	Pin 15 Charging Current	V_{15} = 4V, V_7 = 12V	60					μA
f_9	Lamp Oscillation Frequency	C_L = 3.3 μF			0.5	1.5	2.5	Hz
I_9	Lamp Driver Current	Flashing Mode					600	mA
V_9	Lamp Driver Saturation	I_9 = 200 mA		200			250	mA

Electrical Characteristics (Continued)

V_{CC} = 12V, C_T = 33 μF, R_T = 7.5 kΩ, T_A within operating range except where stated otherwise

Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_{14}	Auxiliary Output Voltage	Lamp OFF			5.0			V
		Lamp ON					1.2	V
V_1	Alarm Level	(Difference Between First and Second Measurement)			230	280	330	mV

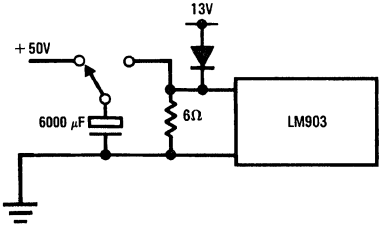
Sensitivity to Electrostatic Discharge: Pins 7, 10, 13, and 14 will withstand greater than 1500V when tested using 100 pF and 1500Ω in accordance with National Semiconductor standard ESD test procedures. All other pins will withstand in excess of 2 kV.

Note 1: Test circuit for overvoltage capability at pins 3, 6, 7.

Note 2: Guaranteed 100% production tested at 25°C. These limits are used to calculate outgoing quality levels.

Note 3: Limits guaranteed to include parametric variations. T_A = −40°C to +80°C and from V_{CC} = 7.5V–18V. These limits are not used to calculate AOQL figures.

Note 4: Variations over temperature range are not production tested.



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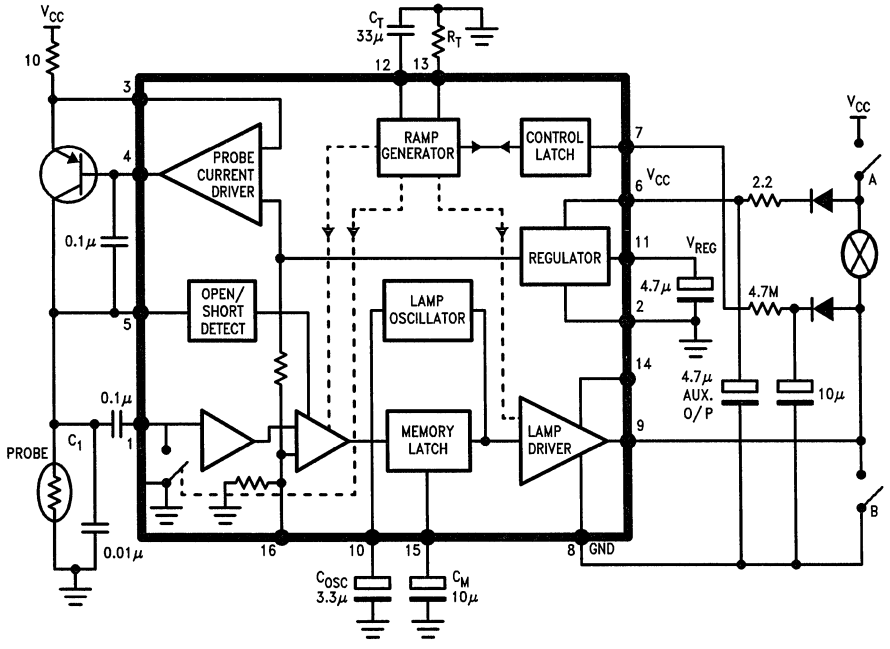
In Lamp ON condition, I_9 should be limited to 600 mA.

Block and Application Circuit



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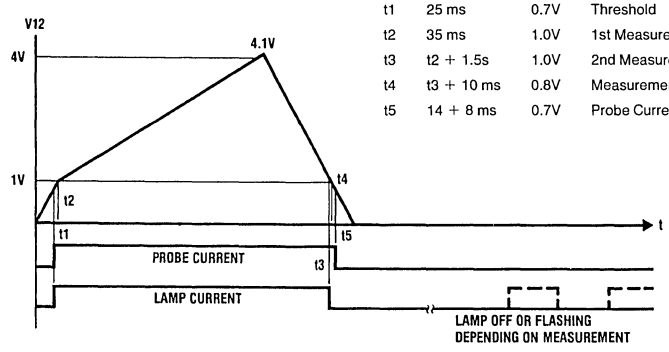
Memory capacitor on pin 15 is set

High—Lamp off

Low—Lamp on

Circuit Timing Diagram



t1	25 ms	0.7V	Threshold
t2	35 ms	1.0V	1st Measurement
t3	t2 + 1.5s	1.0V	2nd Measurement
t4	t3 + 10 ms	0.8V	Measurement Latched
t5	14 + 8 ms	0.7V	Probe Current Off

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Circuit Operation

A measurement is initiated when the supply is applied, provided the control input pin 7 is low. Once a measurement is commenced, pin 7 is latched low and the ramp capacitor on pin 12 begins to charge. After 25 ms when switch-on transients have subsided, a constant current is applied to the thermo-resistive probe. The value of probe current, which is supplied by an external PNP transistor, is set by an external resistor across an internally generated 21V reference. The lamp current is applied at the start of probe current.

35 ms after switch-on, the voltage across the probe is sampled and held on external capacitor C1 (leakage current at pin 1 less than 1 nA). After a further 1.5 seconds the difference between the present probe voltage and the initial probe voltage is measured, multiplied by 3 and compared with a reference voltage of 850 mV (externally adjustable via pin 16). If the amplified voltage difference is less than the reference voltage the lamp is switched off, otherwise the lamp commences flashing at 1 Hz to 2 Hz. 10 ms later the measurement latch operates to store the result and after a further 8 ms the probe current is switched off.

A second measurement can only be initiated by interrupting the supply. An external CR can be arranged on pin 7 to prevent a second measurement attempt for 1 minute. The measurement condition stored in the latch will control the lamp.

PROBES

The circuit effectively measures the thermal resistance of the probe. This varies depending on the surrounding medium (*Figure 1*). It is necessary to be able to heat the probe with the current applied and, for there to be sufficient change in resistance with the temperature change, to provide the voltage to be measured.

Probes require resistance wire with a high resistivity and temperature coefficient. Nickel cobalt alloy resistance wires are available with resistivity of 50 $\mu\Omega$cm and temperature coefficient of 3300 ppm which can be made into suitable probes. Wires used in probes for use in liquids must be designed to drain freely to avoid clogging. A possible arrangement is shown in *Figure 2*.

The probe voltage has to be greater than 0.7V to prevent short circuit probe detection less than 5V to avoid open circuit detection. With a 200 mA probe current this gives a probe resistance range of 4Ω to 25Ω. This low value makes it possible to use the probe in partially conducting fluids.

Using resistance wire of 50 $\mu\Omega$cm resistivity, 8 cm of 0.08 mm (40 AWG) give approximately 8Ω at 25°C. Such a probe will give about 500 mV change between first and second measurements in air, and 100 mV change with oil, hydraulic fluid, etc., in the application circuit. With an alarm threshold of 280 mV (typ) lack of fluid can readily be detected. As the probe current, measurement reference and measurement period are all externally adjustable, there is freedom to use different probes and fluids.

Another possibility is the use of high temperature coefficient resistors made for special applications and positive temperature coefficient thermistors. The encapsulation must have a sufficiently low thermal resistance so as not to mask the change due to the different surrounding mediums, and the thermal time constant must be quick enough to enable the temperature change to take place between the two measurements. The ramp timing could be adjusted to assist this. Probes in liquids must be able to drain freely.

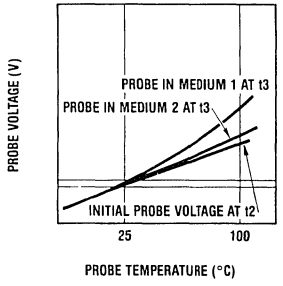

FIGURE 1. Typical Thermo-Resistive Probe

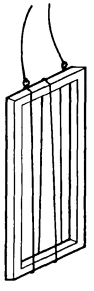

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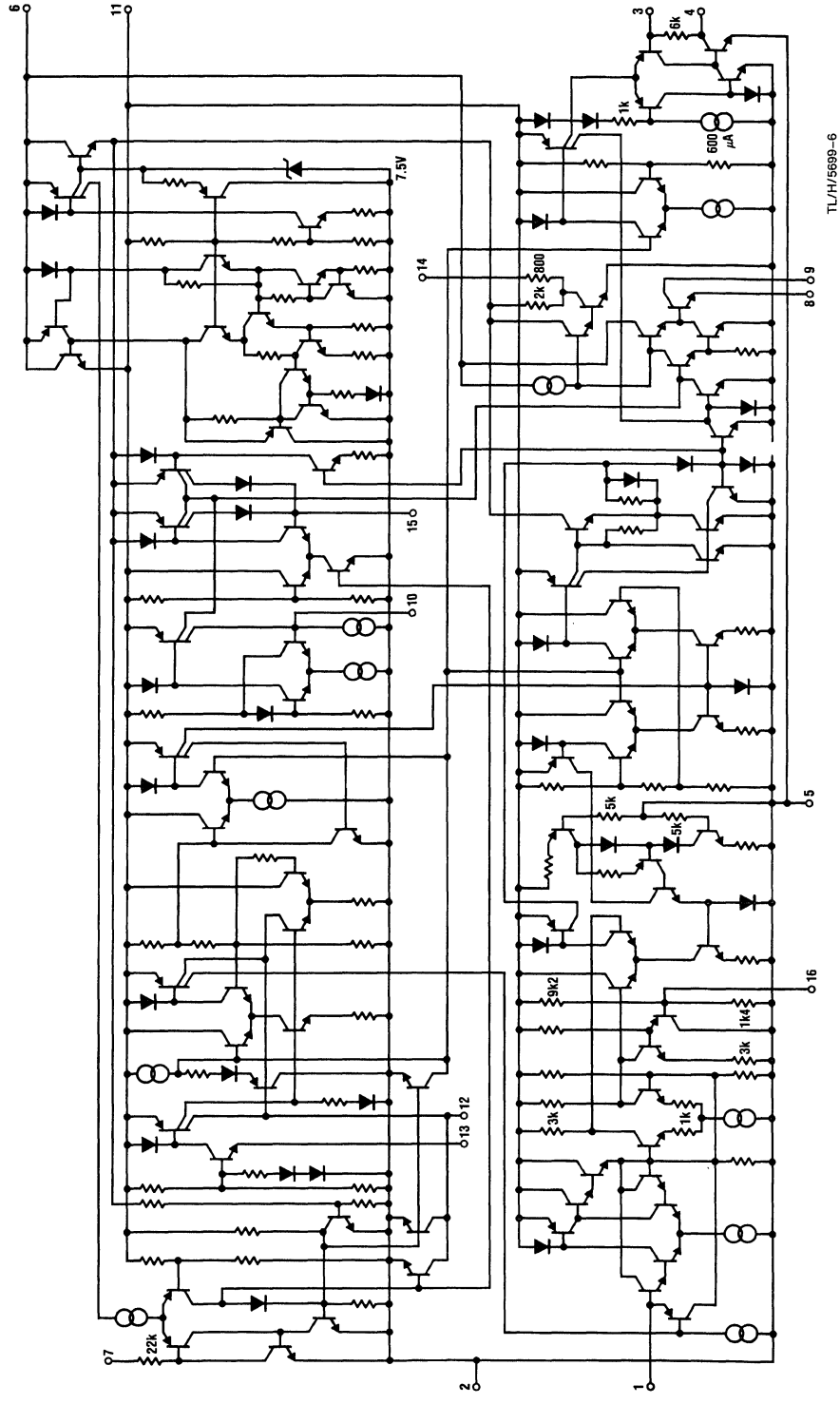
FIGURE 2

Equivalent Schematic Diagram



Application Hints

INTERNAL COMBUSTION ENGINE OIL LEVEL

The basic system provides a single shot measurement when the supply is applied and has a primary application in automotive oil, hydraulic fluid and coolant monitoring. Particularly in the case of the oil level, a valid measurement is only possible before the oil is disturbed. The application circuit shown is arranged such that the measurement is made when the ignition is switched on via switch A. Switch B is the oil pressure sensor and is closed before the engine starts, keeping pin 7 low and enabling the measurement.

STALLING AND RESTART PROTECTION

The 4M7 resistor and 10 μF capacitor connected to pin 7 provide the restart protection. When oil pressure builds up, switch B opens and the 10 μF capacitor charges through the bulb. At switch-off, the capacitor discharges slowly and is capable of preventing a low state on pin 7 for 1 minute. Unless pin 7 is low, a new measurement can not be made and the previous measurement result stored in the memory capacitor on pin 15 is used to control the output.

MEMORY

The pin 15 memory output goes high if a correct measurement is made (lamp off). If the power is removed, pin 15 leakage is less than 3 μA and the memory status is retained for some time. Provided pin 15 voltage does not fall below 3V, the memory capacitor will be refreshed on powering up again. There is no internal pull down on detecting an incorrect measurement. If it is required to use pin 15 as an output indicating the measurement result, an external pull down resistor and buffer will be required.

CONTINUOUS WARNING LAMP

The lamp can be arranged to light continuously by disabling the oscillator with a resistor of 150k or less, connected between pins 10 and 11.

REPETITIVE MEASUREMENTS

Measurements may be repeated by strobing the supply to pin 6. The probe current regulator transistor must have the same supply as pin 6, but the warning lamp can be permanently powered. The lamp will light during each measurement and will flash in between measurements when incorrect conditions are detected.

ALTERNATIVE APPLICATIONS

Gas flow detection: The cooling effect of gas flowing over a probe could be used to provide a warning signal from the LM903 in the event of gas failure.

Automatic top up: With the LM903 strobed continuously, the output may be stored, buffered, and used to drive solenoid valves to correct a fluid level as required.

National Semiconductor Corporation

PRELIMINARY

LM1042 Fluid Level Detector

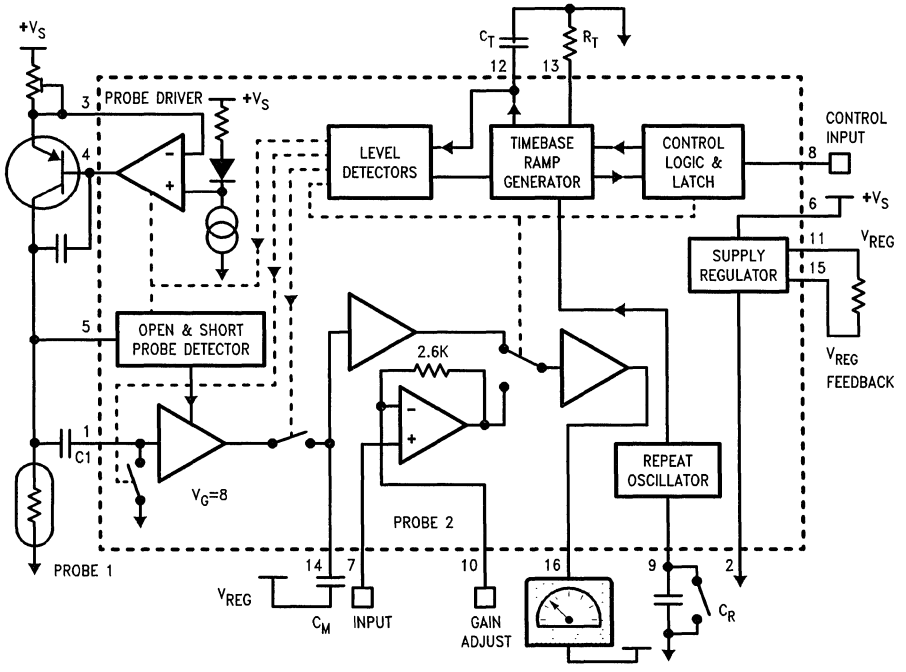
General Description

The LM1042 uses the thermal-resistive probe technique to measure the level of non-flammable fluids. An output is provided proportional to fluid level and single shot or repeating measurements may be made. All supervisory requirements to control the thermal-resistive probe, including short and open circuit probe detection, are incorporated within the device. A second linear input for alternative sensor signals may also be selected.

Features

- Selectable thermal-resistance or linear probe inputs
- Control circuitry for thermal-resistive probe
- Single-shot or repeating measurements
- Switch on reset and delay to avoid transients
- Output amplifier with 10 mA source and sink capability
- Short or open probe detection
- +50V transient protection on supply and control input
- 7.5V to 18V supply range
- Internally regulated supply
- −40°C to +80°C operation

Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V_{CC}	32V
Voltage at Pin 8	32V
Positive Peak Voltage (Pins 6, 8, 3) (Note 1) 10 ms 2A	50V
Output Current Pin 4, (I_4)(sink)	10 mA
Output Current Pin 11 (source)	25 mA
Output Current Pin 16	±10 mA
Operating Temperature Range	−40°C to +80°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering 10 sec.)	260°C
Package Power Dissipation T_A = 25°C (Note 8)	1.8W
Device Power Dissipation	0.9W

Electrical Characteristics

V_{CC} = 13V, T_A within operating range except where stated otherwise. C_T = 22 μF, R_T = 12k

Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		7.5	18	7.5	13	18	V
I_S	Supply Current			35			35	mA
V_{REG}	Regulated Voltage	Pins 15 and 11 connected	5.7	6.15	5.65	5.9	6.2	V
	Stability Over V_{CC} Range	Referred to value at V_{CC} = 13V (Note 4)		±0.5			±0.5	%
V_6-V_3	Probe Current Reference Voltage		2.15	2.35	2.10	2.25	2.40	V
	Probe Current Regulation Over V_{CC} Range	(Note 4)		±0.5			±0.8	%
T_1	Ramp Timing	See *Figure 5*	20	37	15	31	42	ms
T_2-T_1					3		16	ms
T_4-T_1	Ramp Timing		1.4	2.1	1.4	1.75	2.1	s
T_{STAB}	Ramp Timing Stability	Over V_{CC} Range		+5			±5	%
R_T	Ramp Resistor Range		3	15	3		15.0	kΩ
V_8	Start Input Logic High Level		1.7		1.7			V
V_8	Start Input Logic Low Level			0.5			0.5	V
I_8	Start Input Current	$V_8 = V_{CC}$		100			100	nA
I_8	Start Input Current	V_8 = 0V		300			300	nA
V_{16}	Maximum Output Voltage	R_L = 600Ω from Pin 16 to V_{REG}	$V_{REG}-0.3$		$V_{REG}-0.3$			V
	Minimum Output Voltage			0.5		0.2	0.6	V
	PROBE 1							
G_1	Probe 1 Gain	Pin 1 80 mV to 520 mV (Notes 6, 7)	9.9	10.4		10.15		
	Non-linearity of G_1	Pin 1 80 mV to 520 mV (Note 7)	−1	+1	−2	0	2	%
OS_1	Pin 1 Offset	(Note 7)				±5		mV
	PROBE 2							
G_2	Probe 2 Gain	Pin 7 240 mV to 1.562V (Note 7)	3.31	3.49		3.4		
	Non-linearity of G_2	Pin 7 240 mV to 1.562V (Note 7)	−1	+1	−2	0.2	2	%
OS_7	Pin 7 Offset	(Note 7)				±5		mV
R_7	Input impedance					5		MΩ

Electrical Characteristics

V_{CC} = 13V, T_A within operating range except where stated otherwise. C_T = 22 μF, R_T = 12k (Continued)

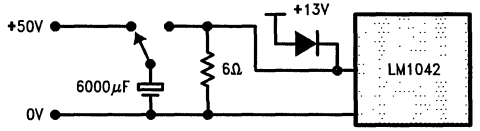
Symbol	Parameter	Conditions	Tested Limits (Note 2)		Design Limits (Note 3)			Units
			Min	Max	Min	Typ	Max	
V_1	Probe 1 Input Voltage Range	V_{CC} = 9V to 18V V_{CC} = 7.5V, I_4 < 2.5 mA (V_{REG} = 6.0V)	1	5	1 1		5 3.5	V V
V_5	Probe 1 Open Circuit Threshold	At Pin 5	$V_{REG}-0.7$	$V_{REG}-0.5$	$V_{REG}-0.85$	$V_{REG}-0.6$	$V_{REG}-0.35$	V
V_5	Probe 1 Short Circuit Threshold		0.5	0.7	0.35	0.6	0.85	V
I_{14}	Pin 14 Input Leakage Current	Pin 14 = 4V	−2.0	2.0			2.0	nA
I_1	Pin 1 Input Leakage Current	Pin 1 = 300 mV	−5.0	5.0		1.5	5.0	nA
T_R	Repeat Period	C_R = 22 μF (Note 5)	12	28	9.1	17	36	s
	C_R Discharge Time	C_R = 22 μF				70	135	ms
C_M	Memory Capacitor Value						0.47	μF
C_1	Input Capacitor Value						0.47	μF

Sensitivity fo Electrostatic Discharge—

Pins 7, 10, 13, and 14 will withstand greater than 1500V when tested using 100 pF and 1500Ω in accordance with National Semiconductor standard ESD test procedures.

All other pins will withstand in excess of 2 kV.

Note 1: Test circuit for over voltage capability at pins 3, 6, 8.



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Note 2: Guaranteed and 100% production tested at 25°C. These limits are used to calculate outgoing quality levels.

Note 3: Limits guardbanded to include parametric variations. T_A = −40°C to +80°C and from V_{CC} = 7.5V to 18V. These limits are not used to calculate AOQL figures.

Note 4: Variations over temperature range are not production tested.

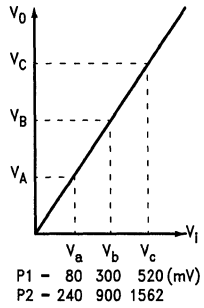
Note 5: Time for first repeat period, see *Figure 6.*

Note 6: Probe 1 amplifier tests are measured with pin 12 ramp voltage held between the T_3 and T_4 conditions (pin 12 ≈ 1.1V) having previously been held above 4.1V to simulate ramp action. See Figure 5.

Note 7: When measuring gain separate ground wire sensing is required at pin 2 to ensure sufficiently accurate results.

Linearity is defined as the difference between the predicted value of V_B (V_B*) and the measured value.

Note 8: Above T_A = 25°C derate with θ_{jA} = 70°C/W.



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For probe 1 and probe 2—Gain (G) = $\frac{V_C - V_A}{V_c - V_a}$

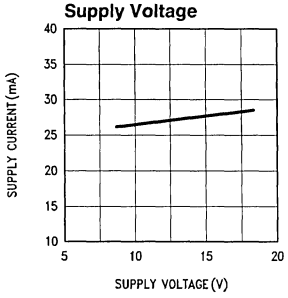
Input offset = $\left[\frac{V_C}{G} - V_c\right]$

Linearity = $\left[\frac{V_B^*}{V_B} - 1\right] \times 100\%$

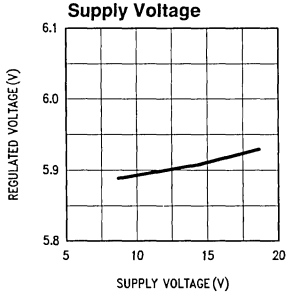
$V_B^* = V_A + G(V_b - V_a)$

Typical Performance Characteristics

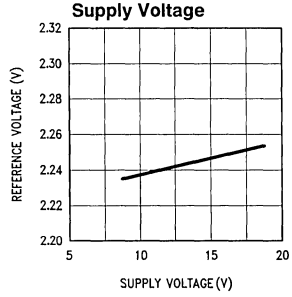
Supply Current vs Supply Voltage



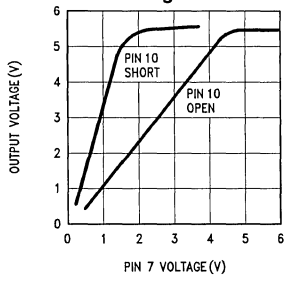
Regulated Voltage vs Supply Voltage



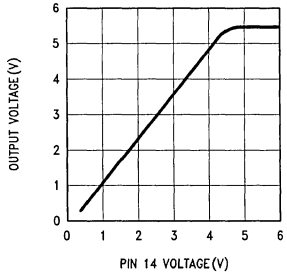
Probe Reference V vs Supply Voltage



Output Voltage vs Pin 7 Voltage



Output Voltage vs Pin 14 Voltage



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Pin Function Description

Pin 1 Input amplifier for thermo-resistive probe with 5 nA maximum leakage. Clamped to ground at the start of a probe 1 measurement.

Pin 2 Device ground — 0V.

Pin 3 This pin is connected to the emitter of an external PNP transistor to supply a 200 mA constant current to the thermo-resistive probe. An internal reference maintains this pin at $V_{SUPPLY} - 2V$.

Pin 4 Base connection for the external PNP transistor.

Pin 5 This pin is connected to the thermo-resistive probe for short and open circuit probe detection.

Pin 6 Supply pin, +7.5V to +18V, protected against +50V transients.

Pin 7 High Impedance input for second linear voltage probe with an input range from 1V to 5V. The gain may be set externally using pin 10.

Pin 8 Probe select and control input. If this pin is taken to a logic low level, probe 1 is selected and the timing cycle is initiated. The selection logic is subsequently latched low until the end of the measurement. If kept at a low level one shot or repeating probe 1 measurements will be made depending upon pin 9 conditions. A high input level selects probe 2 except during a probe 1 measurement period.

Pin 9 The repeat oscillator timing capacitor is connected from this pin to ground. A 2 μA current charges up the capacitor towards 4.3V when the probe 1 measurement cycle is restarted. If this pin is grounded the repeat oscillator is disabled and only one probe 1 measurement will be made when pin 8 goes low.

Pin 10 A resistor may be connected to ground to vary the gain of the probe 2 input amplifier. Nominal gain when open circuit is 1.2 and when shorted to ground 3.4. DC conditions may be adjusted by means of a resistor divider network to V_{REG} and ground.

Pin 11 Regulated voltage output. Requires to be connected to pin 15 to complete the supply regulator control loop.

Pin 12 The capacitor connected from this pin to ground sets the timing cycle for probe 1 measurements.

Pin 13 The resistor connected between this pin and ground defines the charging current at pin 12. Typically 12k, the value should be within the range 3k to 15k.

Pin 14 A low leakage capacitor, typical value 0.1 μF and not greater than 0.47 μF, should be connected from this pin to the regulated supply at pin 11 to act as a memory capacitor for the probe 1 measurement. The internal leakage at this pin is 2 nA max for a long memory retention time.

Pin 15 Feedback input for the internal supply regulator, normally connected to V_{REG} at pin 11. A resistor may be connected in series to adjust the regulated output voltage by an amount corresponding to the 1 mA current into pin 15.

Pin 16 Linear voltage output for probe 1 and probe 2 capable of driving up to ±10 mA. May be connected with a 600Ω meter to V_{REG}.

Application Notes

THERMO-RESISTIVE PROBES — OPERATION AND CONSTRUCTION

These probes work on the principle that when power is dissipated within the probe, the rise in probe temperature is dependent on the thermal resistance of the surrounding material and as air and other gases are much less efficient conductors of heat than liquids such as water and oil it is possible to obtain a measurement of the depth of immersion of such a probe in a liquid medium. This principle is illustrated in *Figure 1.*

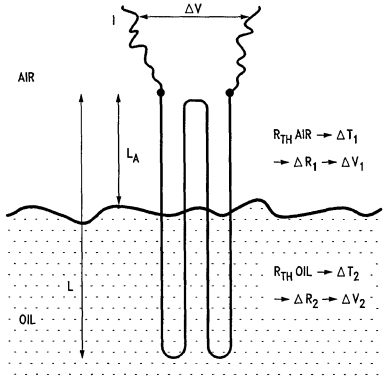

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FIGURE 1

During the measurement period a constant current drive I is applied to the probe and the voltage across the probe is sampled both at the start and just before the end of the measurement period to give ΔV. R_{TH} Air and R_{TH} Oil represent the different thermal resistances from probe to ambient in air or oil giving rise fo temperature changes ΔT_1 and ΔT_2 respectively. As a result of these temperature changes the probe resistance will change by ΔR_1 or ΔR_2 and give corresponding voltage changes ΔV_1 or ΔV_2 per unit length.

Hence

$$\Delta V = \frac{L_A}{L}\Delta V_1 + \frac{(L - L_A)}{L}\Delta V_2$$

and for $\Delta V_1 > \Delta V_2$, R_{TH} Air > R_{TH} Oil, ΔV will increase as the probe length in air increases. For best results the probe needs to have a high temperature coefficient and low thermal time constant. One way to achieve this is to make use of resistance wires held in a suitable support frame allowing free liquid access. Nickel cobalt iron alloy resistance wires are available with resistivity 50 μΩcm and 3300 ppm temperature coefficient which when made up into a probe with 4 × 2 cm 0.08 mm diameter strands between supports (10 cm total) can give the voltage vs time curve shown in *Figure 2* for 200 mA probe current. The effect of varying the probe current is shown in *Figure 3.* To avoid triggering the probe failure detection circuits the probe voltage must be between 0.7V and 5.3V (V_{REG} − 6V), hence for 200 mA the permissible probe resistance range is from 3.5Ω to 24Ω. The example given has a resistance at room temperature of 9Ω which leaves plenty of room for increase during measurements and changes in ambient temperature.

Various arrangements of probe wire are possible for any given wire gauge and probe current to suit the measurement range required, some examples are illustrated schematically in *Figure 4.* Naturally it is necessary to reduce the probe

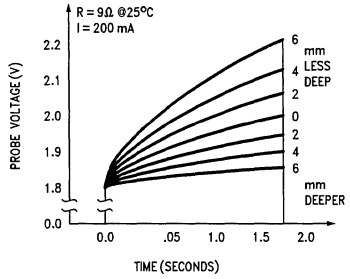

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FIGURE 2

current with very fine wires to avoid excessive heating and this current may be optimized to suit a particular type of wire. The temperature changes involved will give rise to noticeable length changes in the wire used and more sophisticated holders with tensioning devices may be devised to allow for this.

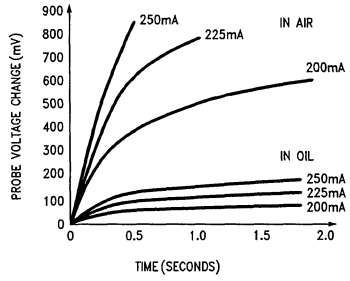

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FIGURE 3

Probes need not be limited to resistance wire types as any device with a positive temperature coefficient and sufficiently low thermal resistance to the encapsulation so as not to mask the change due to the different surrounding mediums, could be used. Positive temperature coefficient thermistors are a possibility and while their thermal time constant is likely to be longer than wire the measurement time may be increased by changing C_T to suit.

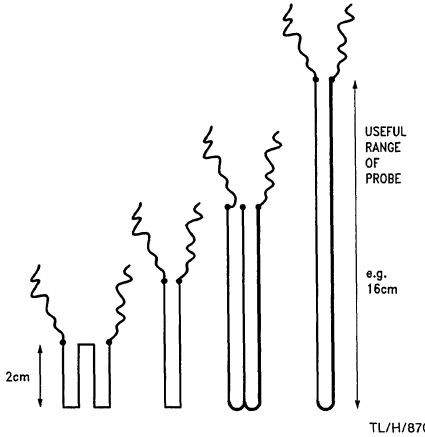

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FIGURE 4

Application Notes (Continued)

CIRCUIT OPERATION

1) Thermo-Resistive Probes

These probes require measurements to be made of their resistance before and after power has been dissipated in them. With a probe connected as probe 1 in the connection diagram the LM1042 will start a measurement when pin 8 is taken to a logic low level ($V_8 < 0.5V$) and the internal time-base ramp generator will start to generate the waveform shown in *Figure 5*. At 0.7V, T_1, the probe current drive is switched on supplying a constant 200 mA via the external PNP transistor and the probe failure circuit is enabled. At 1V pin 1 is unclamped and C_1 stores the probe voltage corresponding to this time, T_2. The ramp charge rate is now reduced as C_T charges toward 4V. As the 4.1V threshold is passed a current sink is enabled and C_T now discharges. Between 1.3V and 1.0V, T_3 and T_4, the amplified pin 1 voltage, representing the change in probe voltage since T_2 (and as the current is constant this is proportional to the resistance change) is gated onto the memory capacitor at pin 14. At 0.7V, T_5, the probe current is switched off and the measurement cycle is complete. In the event of a faulty probe being detected the memory capacitor is connected to the regulated supply during the gate period. The device leakage at pin 14 is a maximum of 2 nA to give a long memory retention time. The voltage present on pin 14 is amplifed by 1.2 to drive pin 16 with a low impedance, ±10 mA capability, between 0.5V and 4.7V. A new measurement can only be started by taking pin 8 to a low level again or by means of the repeat oscillator.

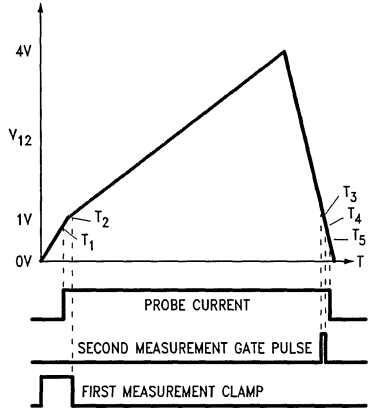

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FIGURE 5

2) Repetitive Measurement

With a capacitor connected between pin 9 and ground the repeat oscillator will run with a waveform as shown in *Figure 6* and a thermo-resistive probe measurement will be triggered each time pin 9 reaches a threshold of 4.3V, provided pin 8 is at a logic low level. The repeat oscillator runs independently of the pin 8 control logic.

As the repetition rate is increased localized heating of the probe and liquid being measured will be the main consideration in determining the minimum acceptable measurement intervals. Measurements will tend to become more dependent on the amount of fluid movement changing the rate of heat transfer away from the probe. The typical repeat time versus timing capacitor value is shown in *Figure 7*.

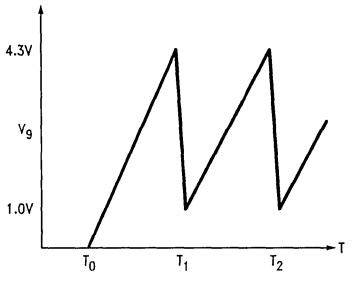

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FIGURE 6

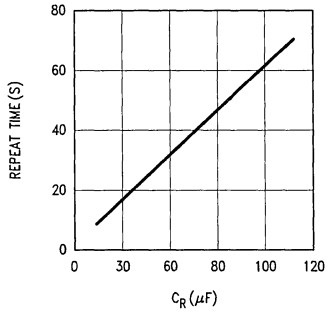

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FIGURE 7

3) Second Probe Input

A high impedance input for an alternative sensor is available at pin 7. The voltage applied to this input is amplified and output at pin 16 when the input is selected with a high level on pin 8. The gain is defined by the feedback arrangement shown in *Figure 8* with adjustment possible at pin 10. With pin 10 open the gain is set at a nominal value of 1.2, and this may be increased by connecting a resistor between pin 10 and ground up to a maximum of 3.4 with pin 10 directly grounded. A variable resistor may be used to calibrate for the variations in sensitivity of the sensor used for probe 2.

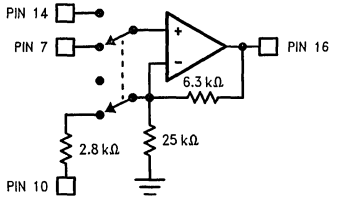

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FIGURE 8

POWER SUPPLY REGULATOR

The arrangement of the feedback for the supply regulator is shown in *Figure 9*. The circuit acts to maintain pin 15 at a constant 6V and when directly connected to pin 11 the regulated output is held at 6V. If required a resistor R may be connected between pins 15 and 11 to increase the output voltage by an amount corresponding typically to 1 mA flowing in R. In this way a variable resistor may be used to trim out the production tolerance of the regulator by adjusting for $V_{REG} \geq 6.2V$.

Application Notes (Continued)

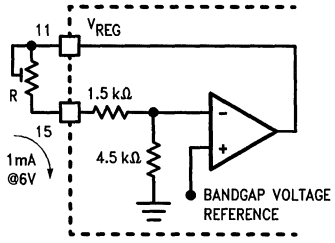

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FIGURE 9

PROBE CURRENT REFERENCE CIRCUIT

The circuit defining the probe circuit is given in *Figure 10.* A reference voltage is obtained from a bandgap regulator derived current flowing in a diode resistor chain to set up a voltage 2 volts below the supply. This is applied to an amplifier driving an external PNP transistor to maintain pin 3 at 2V below supply. The emitter resistance from pin 3 to supply defines the current which, less the base current, flows in the probe. Because of the sensitivity of the measurement to probe current evident in *Figure 3* the current should be adjusted by means of a variable resistor to the desired value. This adjustment may also be used to take out probe tolerances.

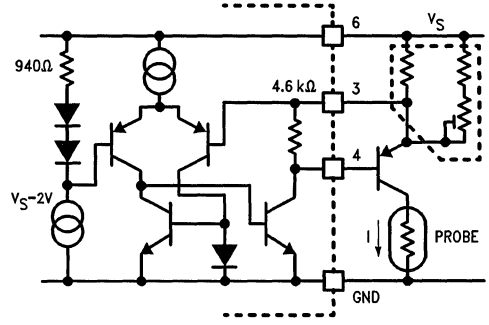

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FIGURE 10

TYPICAL APPLICATIONS CIRCUIT

A typical automotive application circuit is shown in *Figure 11* where the probe selection signal is obtained from the oil pressure switch. At power up (ignition on) the oil pressure switch is closed and pin 8 is held low by R4 causing a probe 1 (oil level) measurement to be made. Once the engine has started the oil pressure switch opens and D1 pulls pin 8 high changing over to the second auxiliary probe input. The capacitor C_5 holds pin 8 high in the event of a stalled engine so that a second probe 1 measurement can not occur in disturbed oil. Non-automotive applications may drive pin 8 directly with a logic signal.

Application Notes (Continued)

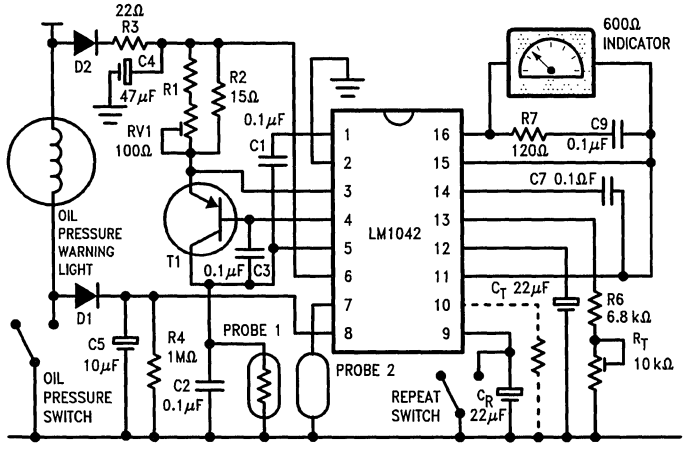

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FIGURE 11. Typical Application Circuit

Ordering Information

Order Number LM1042N

See NS Package Number N16A

National Semiconductor Corporation

LM1211 Broadband Demodulator System

General Description

The LM1211 is a high performance IF amplifier and product detection system for operation in the 20–80 MHz frequency range. It is suitable for data or video recovery from broadband local area networks and other communications systems.

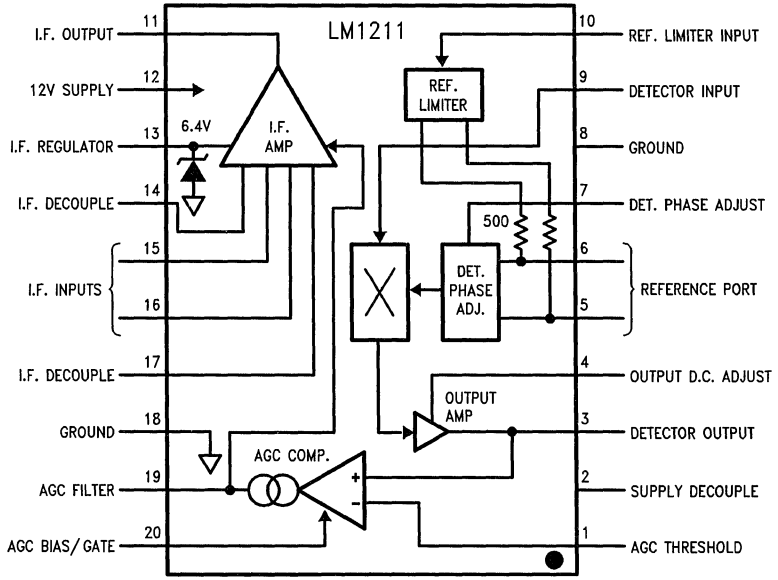
The high gain IF amplifier has a SAW filter compatible input and can be gain-controlled in excess of 40 dB. A flexible product detector is used in which the input signal is multiplied by a reference derived from limiting and phase-shifting the input. The signal input is separate from the reference path, which has a port for external connections. A DC-operated phase control is provided for detection phase adjustment.

The detector is followed by a 25 MHz bandwidth amplifier which has a symmetric output swing capability around 0V. A fast attack, peak-following AGC detector is also provided for use in AM systems.

Features

- Configurable for AM or FM based signals
- 20–80 MHz operating frequency range
- IF input SAW filter compatible
- >40 dB IF gain control range
- 25 MHz detector output bandwidth
- Linear output phase response
- Output swings ±3.5V referenced to ground
- Gateable peak-following AGC detector
- DC-adjustable detection phase
- DC-adjustable 0 carrier output level

Connection Diagram



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Order Number LM1211N
See NS Package Number N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage, V12	15V
IF Supply Current, I13	40 mA
Detector Output Current, I3	15 mA
Detector Input Signal, V9	1 Vrms
Ref. Limiter Input Signal, V10	1 Vrms
AGC Bias/Gate Current, I20	3 mA
Power Dissipation	1.67W
Thermal Resistance	60°C/W
Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
ESD Susceptibility (Note 1)	3000V

DC Electrical Characteristics

T_A = 25°C, Test Circuit, $V_{IF} = V_{Det} = 0$, $V_{AGC} = 0$, $V_{PH} = 4V$, $V_{OC} = 6V$, all switches open unless noted.

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limit)
I_S	Supply Current	SW 3 closed, $V_{AGC} = 3V$	67	80		mA (max)
V_{13}	IF Regulator Voltage	SW 3 closed, $V_{AGC} = 3V$	6.5	5.8 7.0		V (min) V (max)
$V_{15/16}$	IF Input Voltage	SW 2, 3 closed	3.9	3.4 4.4		V (min) V (max)
$V_{14}-V_{17}$	IF Decouple V_{OS}	SW 2, 3 closed, measure $V_{14}-V_{17}$	0	±50		mV (max)
I_{11}	IF Output Current	SW 2, 3 closed, $V_{AGC} = 6V$, $I_{11} = \frac{12V - V_{11}}{50}$	4.0	2.5 5.0		mA (min) mA (max)
V_{10}	Limiter Input Bias	SW 1, 2, 3 closed	5.1	4.5 5.5		V (min) V (max)
V_9	Detector Input Bias	SW 1, 2, 3 closed	5.1	4.5 5.5		V (min) V (max)
$V_{5/6}$	Reference DC Voltage	SW 1, 2, 3 closed	4.6	4.0 5.2		V (min) V (max)
V_3	O Carrier Output Voltage	SW 1, 2, 3 closed	0	±0.5		V (max)
V_{OC}	O Carrier Adjust Voltage	SW 1, 2, 3 closed, adjust V_{OC} for V_3 = OV	6.0	1.0 11.0		V (min) V (max)
$I_{19(D)}$	AGC Discharge Current	SW 1, 3 closed, $V_{AGC} = 2V$	−11	−7 −16		μA (min) μA (max)
$I_{19(C)}$	AGC Charge Current	SW 1, 4 closed, $V_{AGC} = 6V$	1.0	0.7 1.3		mA (min) mA (max)
$I_{19(L)}$	AGC Leakage Current	SW 1, 2, 4 closed, $V_{AGC} = 4V$	−25	±200		nA (max)

Note 1: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 2: Tested limits are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

Detector AC Set-up Procedure

T_A = 25°C, Test Circuit, Sw 1, 2, 3 closed, V_{AGC} = 0, V_{PH} = 4V.

1. With no input (V_{Det} = 0), adjust V_{0C} for V3 = 0V.
2. Apply V_{Det} = 100 mVrms, 60 MHz CW at the input. Tune L2 for maximum DC voltage at output Pin 3.

AC Electrical Characteristics

T_A = 25°C, Test Circuit, Follow AC set-up procedure, f = 60 MHz, V_{AGC} = 0, V_{PH} = 4V, V_{0C} as per set-up, all switches open unless noted.

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 1)	Design Limit (Note 2)	Units (Limit)
Z15/16	IF Input Impedance	Measure Differential Impedance between Pins 15 and 16.	60		40 80	Ω (min) Ω (max)
Av(IF)	Maximum IF Gain (Note 3)	SW 2 Closed, V_{IF} = 0.5 mVrms, Measure V_{out}. Av(IF) = 20 log $\left(\frac{V_{out}}{5 \times 10^{-4}}\right)$	30	20		dB (min)
V_{AGC20}	20 dB Gain Reduction	SW 2 Closed, V_{IF} = 5 mVrms, Adjust V_{AGC} for Same V_{out} as in Av(IF) Test.	2.6	2.2 3.0		V (min) V (max)
V_{AGC40}	40 dB Gain Reduction	SW 2 Closed, V_{IF} = 50 mVrms, Adjust V_{AGC} for Same V_{out} as in Av(IF) Test.	3.8	3.3 4.3		V (min) V (max)
IM	IF Intermodulation (Note 3)	SW 2 Closed, f_1 = 60 MHz, f_2 = 65 MHz, V_{IF} = 10 mVrms Ea, Adjust V_{AGC} for V_{out} = 10 mVrms Ea, Measure IM Products Relative to V_{out}.	−40		−30	dB (min)
Z9	Detector Input Impedance	Measure Impedance into Pin 9	3.0		2.0 5.0	KΩ (min) pF (max)
Z10	Reference Limiter Input Impedance	Measure Impedance into Pin 10	2.0		1.3 5.0	KΩ (min) pF (max)
Av(D)	Detector Conversion Gain	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure V_{3DC}. Av(D) = 20 log $\left(\frac{V_3}{0.1}\right)$	24	20 30		dB (min) dB (max)
LIN	Detector-6dB Linearity	SW 1, 3 Closed, V_{Det} = 50 mVrms, Measure V_3'. LIN = 20 log $\left(\frac{V_3'}{V_3}\right)$	−6	−5 −7		dB (min) dB (max)
$V_{3(Th)}$	AGC Threshold	SW 1, 3 Closed, Increase V_{Det} until I19 = 100 μA, Measure V_3.	2.8		2.6 3.0	V (min) V (max)
$V_{3(OL)}$	Detector Overload Capability	SW 1, 2, 3 Closed, V_{Det} = 1 Vrms, Measure V_3.	4.1	3.5		V (min)
PHA(+)	DC Phase Adjust (+)	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure Ratio of V_3 with V_{PH} = 6V to V_3 with V_{PH} = 4V.	0.65	0.80		V/V (max)
PHA(−)	DC Phase Adjust (−)	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure Ratio of V_3 with V_{PH} = 2V to V_3 with V_{PH} = 4V.	0.30	0.60		V/V (max)
$V_{3(-)}$	Negative Output Swing	SW 1, 2, 3 Closed, f = 70 MHz, V_{Det} = 300 mVrms, V_{PH} = 6V, Measure V_3.	−3.7	−3.0		V (min)
DBW	Detector Output Bandwidth	SW 1, 2, 3 Closed, Modulate V_{Det} with 30% AM Modulation. Increase Modulation Frequency Until Pin 3 Signal Drops 3 dB.	25		20	MHz (min)
DHL	Detector Harmonic Levels	SW 1, 2, 3 Closed, V_{Det} = 100 mVrms, Measure 60 MHz and 120 MHz Levels Relative to V_3	−35		−20	dB (min)

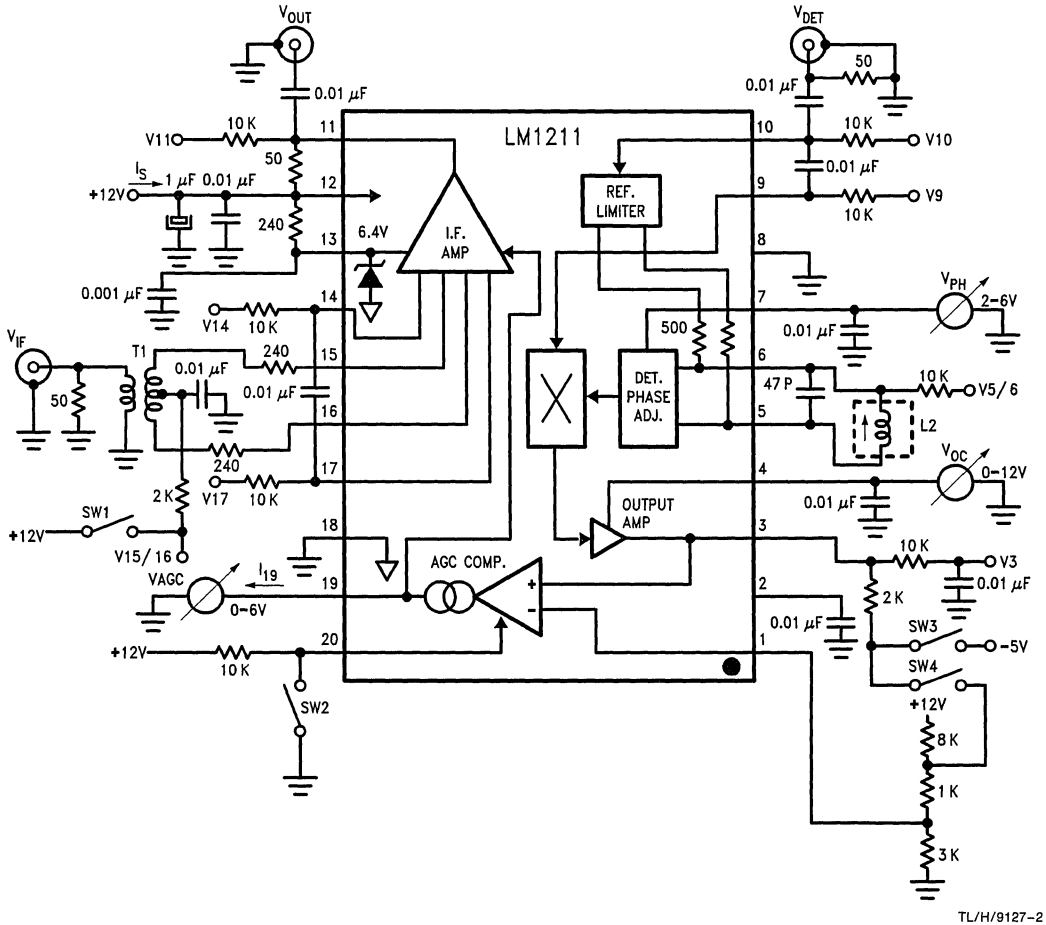
Note 1: Tested limits are guaranteed and 100% production tested.

Note 2: Design limits are guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

Note 3: The IF amplifier output is measured with the IF output connected to a 50Ω measurement system resulting in a 25Ω loaded impedance. The gain in an actual application will typically be 20 dB higher.

Test Circuit

Measure Parameters at Indicated Test Points



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T1 = 50Ω unbal. to bal. Mini-circuits Lab TM01T-1T

L2 = 4½ T #22 wire on 3/16" form with HF core, shielded

Typical Performance Characteristics

(All characteristics apply to the typical application circuit. Figure numbers are referenced in the applications information.)

FIGURE 1
IF Amplifier Gain Reduction Characteristic

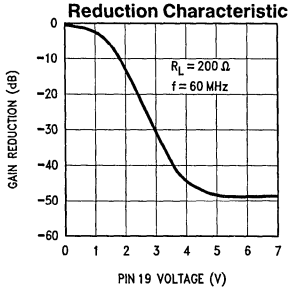


FIGURE 2
IF Amplifier Frequency Response

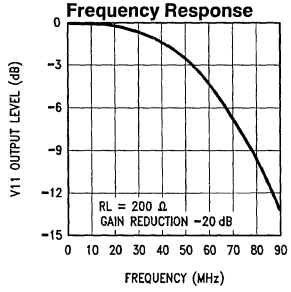


FIGURE 3
IF Amplifier Noise Figure vs. AGC

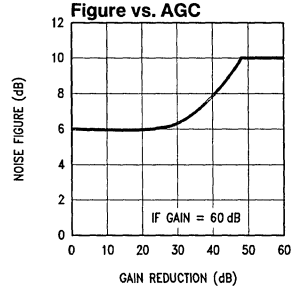


FIGURE 4
LM1211 Detection Phase

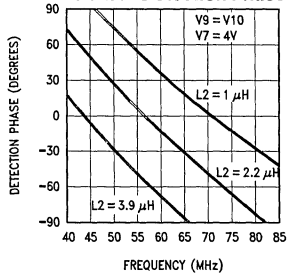


FIGURE 5
Detector Phase Adjust Characteristic

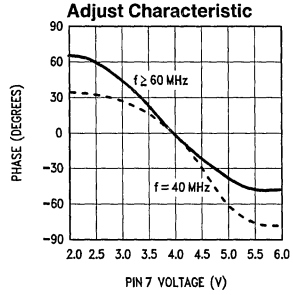
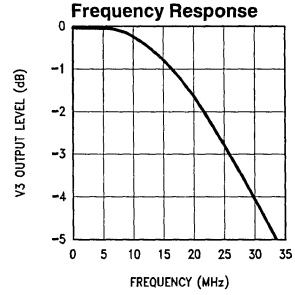


FIGURE 6
Output Amplifier Frequency Response



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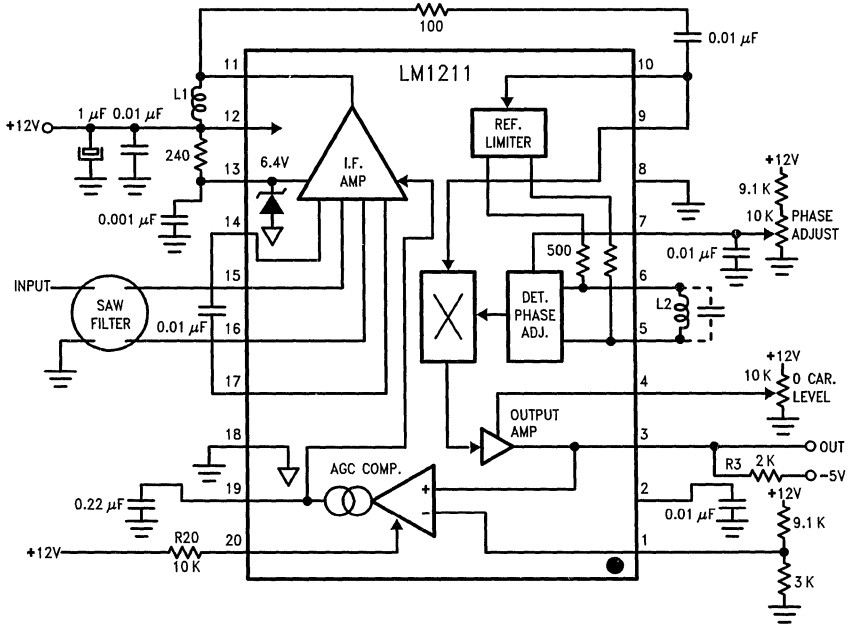
Typical Application Circuit



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Applications Information (Refer to Typical Performance Characteristics and Application Circuit.)

The LM1211 broadband demodulator system provides essentially independent IF amplifier and wideband detector blocks on the same integrated circuit. The IF amplifier consists of 5 differential stages, 3 of which have gain control capability. The detector is a highly flexible product detector with separate signal and reference input pins and a wideband output amplifier. An AGC comparator operating from the detector output is also provided. The operation of each of these blocks will now be described.

IF AMPLIFIER

The IF amplifier is powered from an internal shunt regulator between IF supply Pin 13 and IF ground Pin 18. The regulator has a nominal value of 6.5V and the IF amplifier current is delivered through a dropping resistor from the 12V rail supplying the remainder of the LM1211. The 0.001 μF ceramic RF decoupling capacitor at Pin 13 should be grounded through very short leads—preferably on the copper side of the PCB. A nominal current level into Pin 13 is 23 mA, set by a 240Ω resistor. This current should not exceed 40 mA and the minimum current is about 16 mA, below which the IF amplifier will start to lose gain as the Pin 13 voltage drops below the regulated level.

IF Amplifier Input Configuration

Circuit detail for the IF amplifier input Pins 14–17 is shown in *Figure 7.* The input stage is a common-base differential amplifier designed to give good rejection of unwanted IF output and detector reference signals that may be radiated back to the input.

The low differential input impedance of 60Ω ensures that SAW filters are terminated sufficiently to keep the triple transit echo (TTE) more than 40 dB below the signal level, even with low impedance SAW filters. Because it is a common base stage, the input stage gain is inversely proportional to the source impedance Zs presented to the input. A normal range for differential Zs is from 100Ω to 1 KΩ. As an example, a typical high impedance SAW filter has an output impedance that can be modeled as a 2 KΩ resistor in parallel with 6 pF capacitance, yielding Zs = 372Ω at 70 MHz. Alternatively, the IF may be used with a transformer input configuration similar to that shown in the Test Circuit, as long as the required source impedance is maintained.

A balanced input is extremely important since the input leads to Pins 14–17 are the most sensitive points in the system to unwanted IF coupling. For example, if the IF output or detector reference signals couple into these pins it can cause changes in the frequency response and can easily promote oscillation. A spectrum analyzer is invaluable for helping determine the system susceptibility to this phenomenon. With the input terminated by the IF filter (or an equivalent resistor), the IF amplifier output noise spectrum will show if oscillation is likely to occur at maximum gain. A good layout will have symmetrical input leads placed as close together as possible, shielded input coils (where used), and external components mounted as close to the I.C. as possible. The DC feedback decoupling capacitor connected between Pins 14 and 17 should be right against the pins.

Gain Control Stages

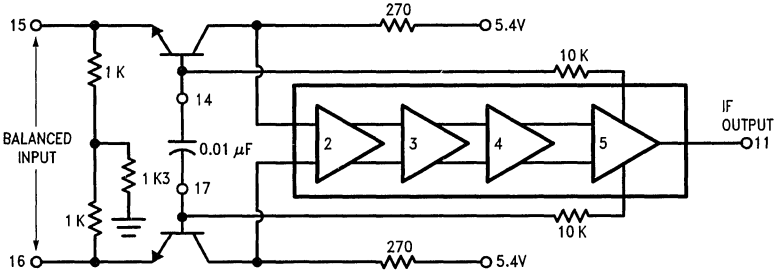
The second through fourth differential stages of the IF amplifier are gain controlled by the voltage at the AGC Filter Pin 19. 0V corresponds to maximum IF gain, while increasing the Pin 19 voltage results in the gain reduction curve shown in *Figure 1.*

In most AM applications, the Pin 19 voltage will be under control of the AGC detector (to be described later) in a closed feedback loop. If Pin 20 of the AGC detector is grounded, Pin 19 is tri-stated, allowing it to be externally controlled. In the tri-stated condition the typical input bias current at Pin 19 is only 25 nA, allowing small filter capacitors to be used in gated AGC systems. The *Figure 1* characteristics has a temperature dependence of approximately −0.1 dB/°C. While this has no bearing in a closed loop system, it precludes setting a temperature stable fixed gain via a resistive divider at Pin 19.

For FM applications, the IF amplifier may be locked at maximum gain by grounding Pin 19. Under these conditions none of the 5 stages saturate when overdriven, allowing the amplifier to function as a basic wideband limiter.

IF Amplifier Output

The fifth and final IF amplifier stage has a single-ended output, with no internal connection to the detector block. The output Pin 11 is an open collector NPN transistor which must be returned to Pin 12 via a DC path. Pin 11 is also a point at which any additional signal filtering may be applied. A resistive load connected to Pin 12 can be used, but the maximum value is limited in practice to less than 500Ω at intermediate frequencies because of stray capacitance and the loading of the detector stage input impedance.



TL/H/9127–5

FIGURE 7. Low Impedance Common Base Input Stage

Applications Information (Refer to Typical Performance Characteristics and Application Circuit.) (Continued)

The frequency response for the IF amplifier with a 200Ω load is shown in *Figure 2*. The high frequency rolloff gives rise to a potential problem called "tilt." This occurs in wide bandwidth signals when the upper frequency components are attenuated relative to the lower frequency components, which can cause amplitude distortion following demodulation. Tilt can be easily compensated at Pin 11 by using an inductive load to provide an increasing impedance with frequency. The impedance of inductive load L1, including the effects of stray capacitance, is given by:

$$|Z_L| = \frac{\omega L_1}{1 - \omega^2 L_1 C_S}$$

For example, a 0.33 μH coil with 8 pF stray capacitance at Pin 11 has an impedance of 300Ω at 70 MHz, and this impedance is on a frequency dependent slope of 0.4 dB/MHz. As the inductance is increased, the slope becomes steeper until resonance with the stray capacitance is reached. By using this technique, a flat IF response can be obtained over the frequency range of interest.

IF Amplifier Gain and Noise Figure

As described earlier, the maximum IF amplifier gain in the LM1211 is externally determined by the input source impedance, Zs, in conjunction with the output load impedance, Z_L. This gain is approximately given by:

$$A_V = \frac{(1000)|Z_L|}{|Z_S| + 60}$$

The IF amplifier noise figure (NF) as a function of gain reduction is shown in *Figure 3*. The contribution of IF NF to the overall system NF depends on the amount of gain ahead of the IF in the mixer and IF filter.

The SAW filter output mistermination, determined by the IF amplifier input impedance, is desirable from the viewpoint of keeping the TTE more than 40 dB below the signal. However, the mismatch at the input to the SAW filter is not so desirable as it simply increases the filter losses. Therefore a preferable solution is to use a low impedance SAW filter which will reduce losses, or to provide a pre-amplifier stage such as shown in *Figure 8* between the mixer and SAW filter. Since this stage can also be used to match the mixer output to the SAW filter input, the filter losses can be reduced.

To illustrate the effectiveness of this approach, a 10 dB gain pre-amp with a 4 dB NF will put the NF after the mixer stage at 23 dB, and the increase in NF with AGC action (by about 4 dB) will not contribute significantly to the system NF. A useful rule of thumb is that the total NF of the stages following the mixer should not exceed the mixer gain.

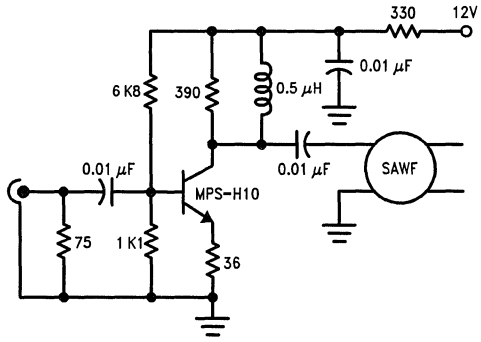


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FIGURE 8. SAW Filter Gain Stage

Detector

The detector section operates from a 12V supply between Pin 12 and ground Pin 8. The LM1211 uses a product detector comprised of a multiplier, reference limiter, detector phase adjuster, and wideband output amplifier (see block diagram). The demodulation process of multiplying the detector input by a limited version of the input is called quasi-synchronous detection. This process provides a wider reference bandwidth but reduced efficiency in carrier nulls relative to a true synchronous detector.

While the following description will apply to quasi-synchronous detection, the LM1211 can be made to function as a true synchronous detector if an external phase-locked loop (PLL) is used. In this mode, the reference limiter input Pin 10 is decoupled and the voltage-controlled oscillator (VCO) signal from the PLL is coupled into the reference port at Pins 5 and 6. Differential coupling of any external signal into the reference port is critical to minimize feedback to the IF amplifier inputs.

Multiplier

The heart of the product detector is the 6 transistor balanced multiplier shown in *Figure 9*. The detector input Vs(t) at Pin 9 is coupled to the linear differential pair, while the reference input Vr(t) switches the upper quad devices at the carrier rate.

If Vs(t) is an amplitude modulated carrier Fm(t)coswt and Vr(t) is a square wave of the same frequency w and relative phase ϕ, then the filtered output is given by:

$$V_{OUT} = \frac{2}{\pi}\frac{RL}{Re} Fm(t)\cos\phi$$

The output depends on the amplitude of Vs(t) and relative phase ϕ between Vs(t) and Vr(t). If ϕ is made 0 degrees so cosϕ is 1, then the multiplier acts as an amplitude detector and can be used to detect the amplitude modulation Fm(t) on the IF carrier. Note that around 0 degrees cos ϕ changes very little with phase. The multiplier can also be used as a

Detector (Continued)

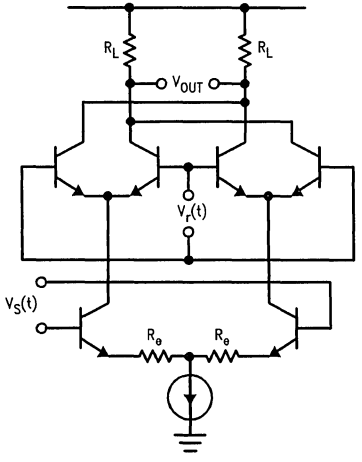

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FIGURE 9. Balanced Multiplier Circuit

phase or frequency detector if Vs(t) is limited to remove amplitude information and ϕ is centered at 90 degrees, where cosϕ produces the largest change in output for a given change in phase.

Thus a vital part of setting up the detector will be to obtain the correct relative phase for the type of demodulation desired.

Reference Limiter

The purpose of the reference limiter is to create the reference signal required for product detection by stripping AM modulation off the input signal. This should not be confused with the limiter required in an FM system, which is in the main signal path. FM limiting would be performed by locking the IF amplifier at maximum gain as previously described, in which case the reference limiter becomes redundant.

A single differential limiter stage is provided between Pin 10 and the reference port at Pins 5 and 6. Pin 10 is internally biased from a 5.1V source through a 3.3 KΩ resistor; the detector input Pin 9 is biased from the same source through 5 KΩ. By sharing a common bias point Pins 9 and 10 can be directly shorted together when fed from the same signal, thus saving a coupling capacitor. Alternatively, Pins 9 and 10 may be fed separately allowing phase and/or amplitude differences to be introduced.

The reference limiter output is a differential signal across the reference port Pins 5 and 6. Pins 5 and 6 are internally biased at 4.6V and have a 1 KΩ differential impedance. Limiting begins with 20 mVrms at Pin 10 and heavy limiting occurs above 100 mVrms input. The maximum limited output voltage is 350 mVrms.

Detector Phasing

As we have seen, the relative phase between the detector and reference inputs of the multiplier determines the LM1211 demodulation characteristic. The detector input phase is known since it connects directly to Pin 9. However, the reference phase depends on several factors: The external components at Pins 10, 5, and 6, the phase shift through the reference limiter, and lastly the setting of the detector phase adjust control at Pin 7. The general approach for phasing the detector is to first select the external components which produce the desired detection phase when the phase adjust control is in the center of its range (V7 = 4V), and then use the control to trim part-to-part and external component variations.

The curves of *Figure 4* give the multiplier detection phase versus frequency for different values of L2 with Pins 9 and 10 shorted together. These curves can be used to select the L2 value and to determine whether additional phase shift between Pins 9 and 10 is required. The detection phase versus temperature is approximately −0.25 degrees/°C.

A detection phase of ϕ = 0 degrees corresponds to maximum (+) amplitude detection efficiency, i.e. the detector output voltage increasing with Pin 9 input level. In the simplest case this can be obtained by choosing the L2 for which the *Figure 4* curve passes through 0 degrees at or near the IF frequency. When the proper phasing cannot be obtained by this means, phase lead or lag must be introduced at Pin 10 relative to Pin 9. A simple RC lead-lag network which can provide up to ±90 degrees phase shift is shown in *Figure 10.*

When XC1 = XC2 = 240Ω in the *Figure 10* circuit, approximately 90 degrees of phase difference between Pins 9 and 10 is produced with 3 dB additional attenuation. Pin 10 is shown lagging Pin 9, but the two pins could be reversed to produce phase lead. If C1 is increased or C2 is decreased, the phase difference is reduced.

A wideband FM quadrature detector is implemented in *Figure 11* by configuring the IF Amplifier for maximum gain and replacing L2 with an LC tank tuned to the IF frequency. Since the IF Amplifier performs the limiting function, the reference limiter is not used; rather, the quadrature signal is fed directly to the reference port via an RC phasing network. The DC offset at Pin 10 (13 KΩ to 12V) prevents signal leakage through the reference limiter to Pins 5 and 6.

The FM detector sensitivity depends on the phase slope of the LC tank, which is determined by the Q. For example, the tank in *Figure 11* is resonant around 70 MHz and has a Q ≅ 2 defined by the internal 1 KΩ resistance across Pins 5 and 6 in parallel with the external resistor. Deviating the input frequency produces an output characteristic given by:

$$V3 = V_{pk}[\cos(90 \pm \Delta 0)]$$

where V_{pk} is the theoretical peak output level set by the IF Pin 11 load impedance, and Δ0 is the combined phase swing produced by the tank and detector. For the *Figure 11* circuit, V_{pk} = 6V and Δ 0 ≅ 5 degrees/MHz, yielding an output swing of ±0.5 V/MHz.

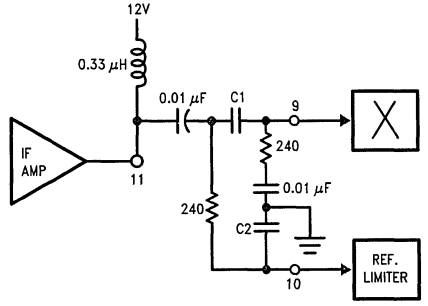

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FIGURE 10. Detector Input Phasing Network

Detector (Continued)

Phase Adjust Control

Once the external components have been selected for the correct nominal phasing, the detector phase adjust is used to perform the final set-up by monitoring the detector output either for maximum output in the case of AM detection or for 0V average level for FM detection. The phase adjust control Pin 7 is externally biased via a potentiometer and resistor from 12V and requires a 2V to 6V minimum range at Pin 7. The amount of phase lead or lag added to the reference path as a function of V_7 is given in *Figure 5*. For example, at 70 MHz a cumulative phase error of ±50 degrees could be compensated for by the phase adjust control.

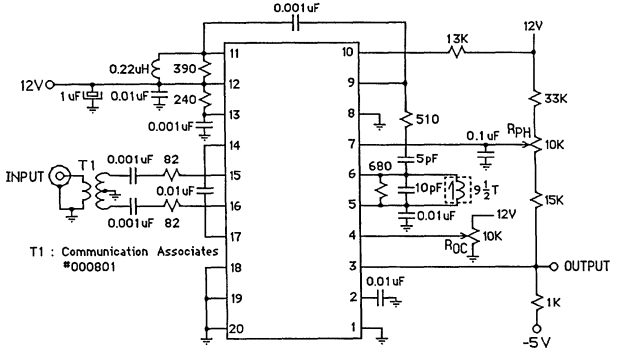
While the previously cited −0.25 degrees/°C detection phase temperature dependence is not noticeable in AM detection applications, it can cause the average DC level of the FM detector output to drift. This can be reduced by using the phase adjust control in a feedback loop as shown in *Figure 11*. Finally, it should be re-emphasized that the Pin 7 adjustment is intended as a trim rather than a substitute for correct detector phasing.

Detector Output

The LM1211 output amplifier has an NPN emitter follower driving Pin 3 through a 50Ω damping resistor as shown in *Figure 12*. The nominal 0 carrier (no input signal) output voltage is 0V, and a negative supply is required as a return point for the external load resistor R3. The output may be biased at up to 5 mA in order to maintain the (−) slew rate into capacitive loads.

The 0 carrier output voltage is adjusted by the control voltage on a potentiometer at Pin 4. The center of the Pin 4 range is ½ supply with an adjustment sensitivity of approximately 0.1 V/V. Thus on a 12V supply up to ±0.6V part-to-part output variation can be trimmed out. The Pin 3 output is capable of swinging up to ±4V; however, in certain AM detector applications the output will always remain above 0V. In these cases it may be possible to omit the negative supply and return the Pin 3 load resistor directly to ground. This will result in some degradation in linearity at low output voltages which can be minimized by pre-biasing the 0 carrier level high (V4 = 12V).

The output amplifier frequency response is shown in *Figure 6*. The output exhibits a linear phase response of approximately −5.5 degrees/MHz out to 30 MHz. The first 70 MHz carrier harmonic is approximately −46 dB and the second harmonic −40 dB referenced to a 3V peak output.



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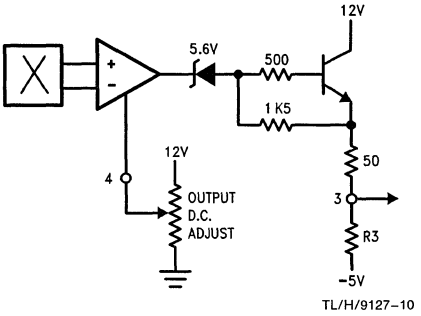


TL/H/9127-10

FIGURE 12. Detector Output Amplifier

ALIGNMENT SEQUENCE:

1. With no input, adjust R_{OC} for V3 = 0V.
2. Apply $V_{in} \geq 10$ mVrms, Fo = 70 MHz ±5 MHz Dev, Fm = 100 kHz; Tune Quadrature coil for best output linearity.
3. Adjust R_{PH} for output DC centering.

FIGURE 11. 70 MHz FM Detector Application

Detector (Continued)

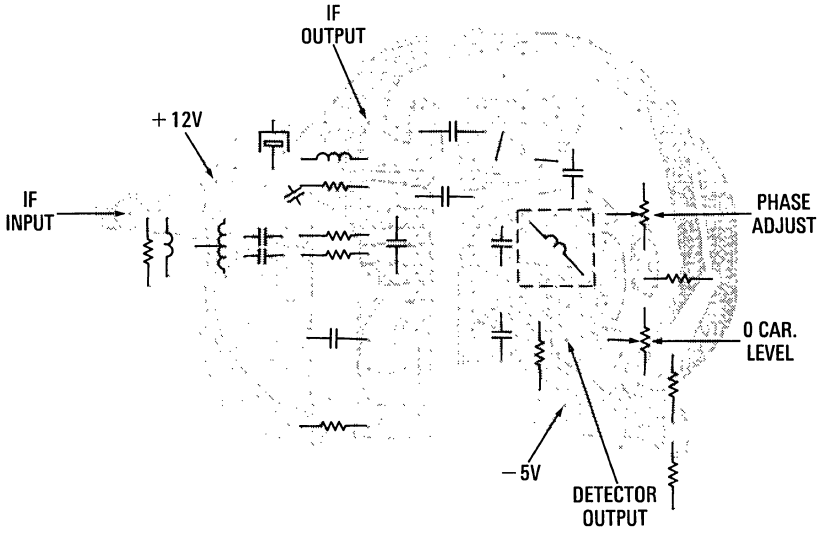
AGC Comparator

An AGC comparator is provided for use in AM systems. The (+) input is internally connected to the detector output Pin 3 while the (−) input is biased from an external resistive divider at AGC threshold Pin 1. An output current charges and discharges the AGC filter capacitor at Pin 19 to control the IF amplifier gain. The comparator is biased by a current into bias/gate Pin 20. Internally, Pin 20 has a diode in series with 1 KΩ to ground so that the current level from an external resistor R20 to 12V is given by:

$$I20 = \frac{11.3}{R20 + 1000}$$

Whenever the detector output exceeds the AGC threshold, a current equal to the Pin 20 bias current is delivered to Pin 19 to charge the AGC filter capacitor. When the detector output is below the AGC threshold, approximately 11 μA discharge current flows into Pin 19. Thus the charge to discharge current ratio at Pin 19 is given by I20/11 μA, or 90:1 for I20 = 1 mA. This large ratio creates a peak-detecting action in which the AGC loop holds the detector (+) output peaks at the AGC threshold voltage, typically 1-3V. Because of the large ratio of charge to discharge current, the LM1211 AGC has inherently faster recovery from a step increase in signal than from a decrease. The overall speed is inversely proportional to the AGC filter capacitor, with 0.05 μF being a practical lower limit for I20 = 1 mA. It is important to use a quality (low Rs) capacitor at Pin 19 to prevent AGC oscillation.

The AGC detector can be used at lower charge/discharge ratios by reducing I20 which has a direct effect on the charge current but only a second order effect on the discharge current. For I20 = 100 μA a 15:1 ratio is produced and a 0.01 μF minimum capacitor can be used. As the charge/discharge ratio is reduced, peak detection no longer occurs and gating of Pin 20 may be necessary. This requires an external gate pulse generator to turn on the Pin 20 bias current only during the time the detector output is to be sampled. In between gate pulses the Pin 19 output will be tri-stated and the filter capacitor will hold the previous voltage until the next gate pulse. Permanently grounding Pin 20 turns off the AGC comparator, allowing an external AGC signal at Pin 19 to control the IF amplifier gain.



TL/H/9127–11

Printed Circuit Layout (component side)

National Semiconductor Corporation

LM1596/LM1496 Balanced Modulator-Demodulator

General Description

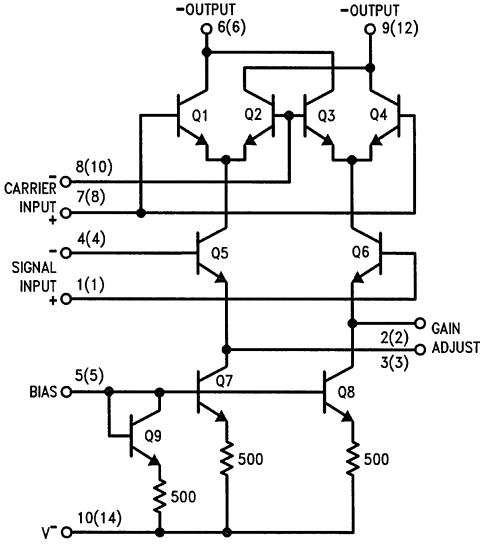
The LM1596/LM1496 are doubled balanced modulator-demodulators which produce an output voltage proportional to the product of an input (signal) voltage and a switching (carrier) signal. Typical applications include suppressed carrier modulation, amplitude modulation, synchronous detection, FM or PM detection, broadband frequency doubling and chopping.

The LM1596 is specified for operation over the −55°C to +125°C military temperature range. The LM1496 is specified for operation over the 0°C to +70°C temperature range.

Features

- Excellent carrier suppression
  - 65 dB typical at 0.5 MHz
  - 50 dB typical at 10 MHz
- Adjustable gain and signal handling
- Fully balanced inputs and outputs
- Low offset and drift
- Wide frequency response up to 100 MHz

Schematic and Connection Diagrams



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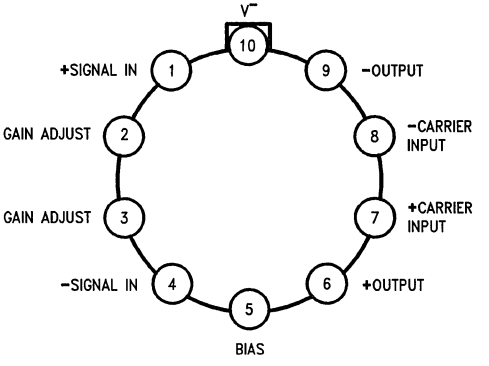
Numbers in parentheses show DIP connections.

Metal Can Package



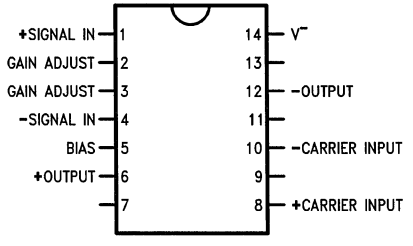
TL/H/7887–2

Top View

Note: Pin 10 is connected electrically to the case through the device substrate.

Order Number LM1496H or LM1596H
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



TL/H/7887–3

Order Number LM1496M or LM1496N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Internal Power Dissipation (Note 1)	500 mW
Applied Voltage (Note 2)	30V
Differential Input Signal ($V_7 - V_8$)	±5.0V
Differential Input Signal ($V_4 - V_1$)	$\pm(5+I_5R_0)$V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0V
Bias Current (I_5)	12 mA
Operating Temperature Range LM1596	−55°C to +125°C
LM1496	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Soldering Information

- Dual-In-Line Package
  - Soldering (10 seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 seconds) 215°C
  - Infrared (15 seconds) 220°C

See AN-450 "Surface Mounting Methods and their effects on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuit)

Parameter	Conditions	LM1596			LM1496			Units
		Min	Typ	Max	Min	Typ	Min	
Carrier Feedthrough	V_C = 60 mVrms sine wave f_C = 1.0 kHz, offset adjusted		40			40		μVrms
	V_C = 60 mVrms sine wave f_C = 10 kHz, offset adjusted		140			140		μVrms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2		0.04	0.2	mVrms
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		20	100		20	150	mVrms
Carrier Suppression	f_S = 10 kHz, 300 mVrms f_C = 500 kHz, 60 mVrms sine wave offset adjusted	50	65		50	65		dB
	f_S = 10 kHz, 300 mVrms f_C = 10 MHz, 60 mVrms sine wave offset adjusted		50			50		dB
Transadmittance Bandwidth	R_L = 50Ω Carrier Input Port, V_C = 60 mVrms sine wave f_S = 1.0 kHz, 300 mVrms sine wave		300			300		MHz
	Signal Input Port, V_S = 300 mVrms sine wave $V_7 - V_8$ = 0.5Vdc		80			80		MHz
Voltage Gain, Signal Channel	V_S = 100 mVrms, f = 1.0 kHz $V_7 - V_8$ = 0.5 Vdc	2.5	3.5		2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 Vdc		200			200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 Vdc		2.0			2.0		pF
Single Ended Output Resistance	f = 10 MHz		40			40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0			5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	25		12	30	μA
Input Bias Current	$(I_7 + I_8)/2$		12	25		12	30	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0		0.7	5.0	μA
Input Offset Current	$(I_7 - I_8)$		0.7	5.0		5.0	5.0	μA
Average Temperature Coefficient of Input Offset Current	(−55°C < T_A < +125°C) (0°C < T_A < +70°C)		2.0			2.0		nA/°C nA/°C
Output Offset Current	$(I_6 - I_9)$		14	50		14	60	μA
Average Temperature Coefficient of Output Offset Current	(−55°C < T_A < +125°C) (0°C < T_A < +70°C)		90			90		nA/°C nA/°C

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuit) (Continued)

Parameter	Conditions	LM1596			LM1496			Units
		Min	Typ	Max	Min	Typ	Min	
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0			5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 Vdc		−85			−85		dB
Common Mode Quiescent Output Voltage			8.0			8.0		Vdc
Differential Output Swing Capability			8.0			8.0		V_{p-p}
Positive Supply Current	($I_6 + I_g$)		2.0	3.0		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0		3.0	4.0	mA
Power Dissipation			33			33		mW

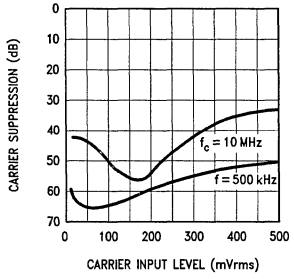
Note 1: LM1596 rating applies to case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperature above 75°C. LM1496 rating applies to case temperatures to +70°C.

Note 2: Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.

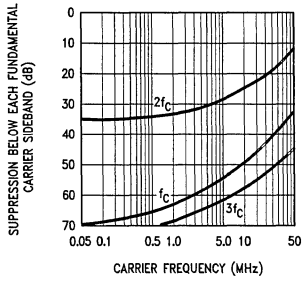
Note 3: Refer to rets1596x drawing for specifications of military LM1596H versions.

Typical Performance Characteristics

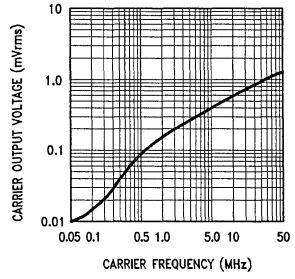
Carrier Suppression vs Carrier Input Level



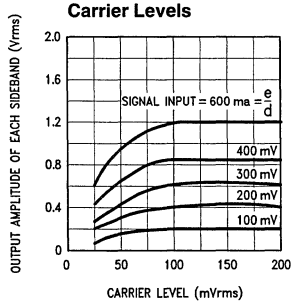
Carrier Suppression vs Frequency



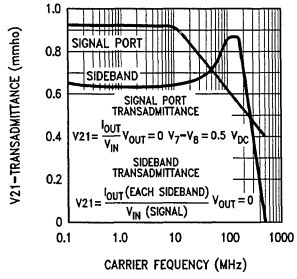
Carrier Feedthrough vs Frequency



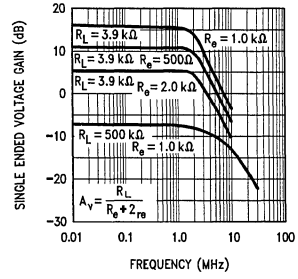
Sideband Output vs Carrier Levels



Sideband and Signal Port Transadmittances vs Frequency



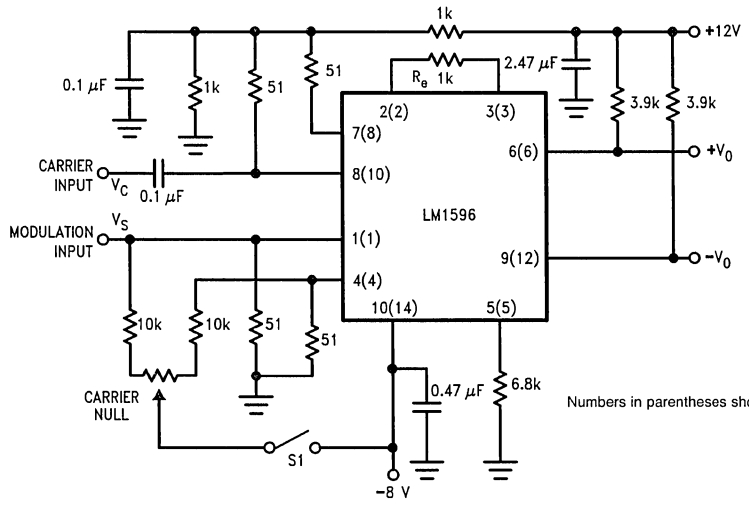
Signal-Port Frequency Response



TL/H/7887–5

Typical Application and Test Circuit

Suppressed Carrier Modulator

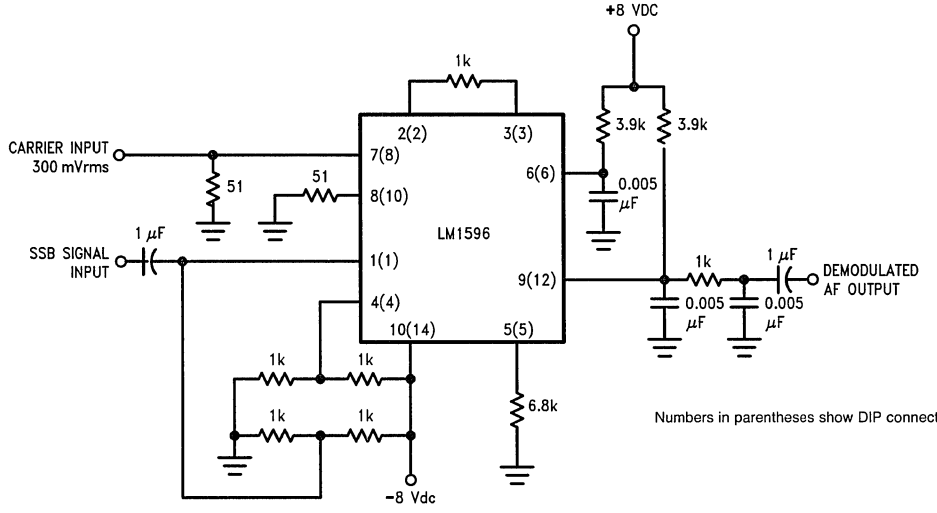


Numbers in parentheses show DIP connections.

TL/H/7887–4

Note: S_1 is closed for "adjusted" measurements.

SSB Product Detector



Numbers in parentheses show DIP connections.

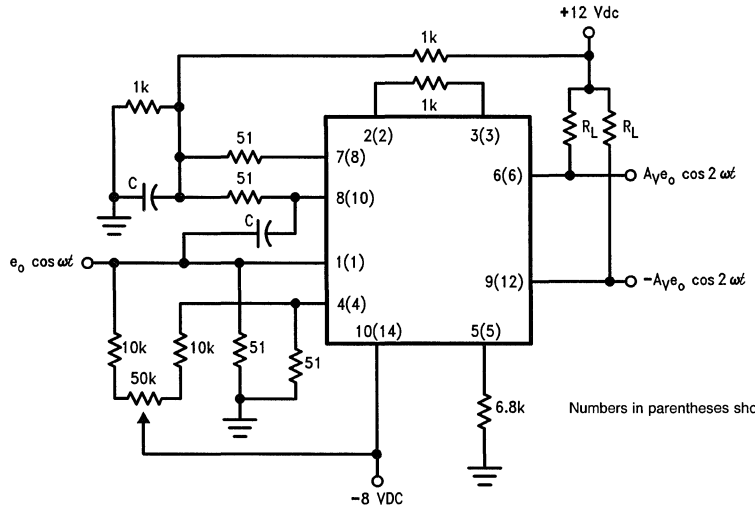
TL/H/7887–6

This figure shows the LM1596 used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mVrms is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mVrms. All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

5

Typical Applications (Continued)

Broadband Frequency Doubler



TL/H/7887–7

The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency. Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

National Semiconductor Corporation

LM1801 Battery Operated Power Comparator

General Description

The LM1801 is an extremely low power comparator with a high current, open-collector output stage. The typical supply current is only 7 μA, yet in its switched state the comparator can source or sink 0.5A. The LM1801 is designed to operate in a standby mode for 1 year, powered by a 9V alkaline battery. Provision is made for operation from supplies of up to 14V. An internal 14.5V zener clamp may be used for supply regulation in line operated applications.

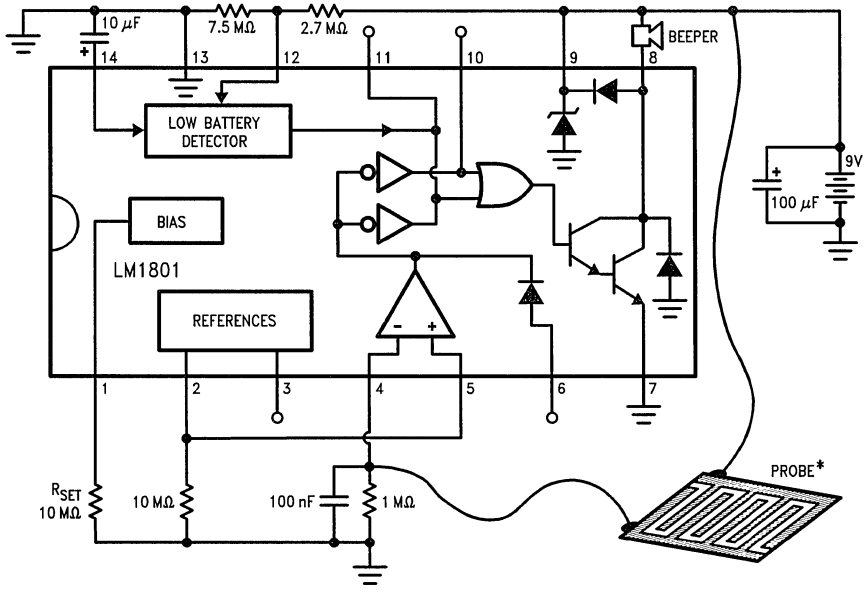
The low battery detector and stand-by current drain are externally programmed by resistors. A parallel output is provided to "OR" as many as 9 comparators, and a feedback pin allows adding hysteresis or latching functions. Two on-chip voltage sources can serve as bias points for the comparator inputs or as references for other circuit functions.

Features

- 8V to 14V operation
- Direct drive to horn
- Internal zener for supply regulation
- Parallel comparator capability
- Extremely low stand-by current drain
- 2 references on chip
- Low battery detector
- 0.5A output transistor
- Output clamp diodes on chip

Applications

- Intrusion alarms
- Water leak detectors
- Gas leak detectors
- Overvoltage crowbars
- Battery operated monitors



TL/H/9139–1

*Alarm sounds when probe conductors are bridged with water droplets. A suitable probe can be etched in copper clad board.

FIGURE 1. Water Leak Detector

Order Number LM1801N
See NS Package Number N14A

5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	14V
Input Voltage	−0.3V to 14V
Input Differential Voltage	±14V
Power Dissipation (Note 1)	1176 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 sec.)	260°C

ESD rating to be determined.

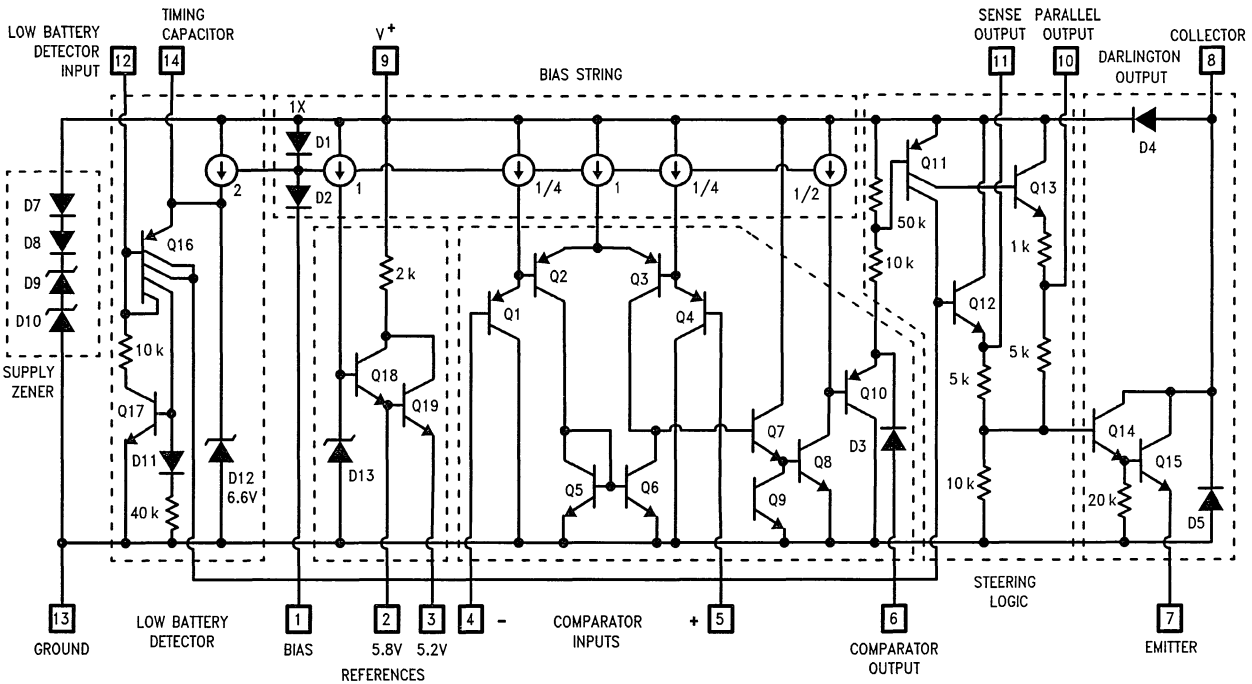
Electrical Characteristics (Note 2)

Parameter	Conditions	Min	Typ	Max	Units
Comparator					
Input Offset Voltage			5	15	mV
Input Bias Current			2	10	nA
Input Offset Current			0.5	8	nA
Pin 6 Output Low	I_{SINK} = 100 μA		1.5		V
Output Stage (Pin 8)					
Leakage Current			5	100	nA
Saturation Voltage	I_8 = 200 mA		0.7	1.3	V
Saturation Voltage	I_8 = 500 mA		1.9		V
Common Alarm Line (Pin 10)					
Drive Capabilities	V4 > V5				
Output Voltage High			6.8		V
Output Current	V10 = 0.0V		6.5		mA
Driver Requirements	V5 > V4				
Input Voltage			3.6		V
Input Current	V8 = 1.5V, I_8 = 200 mA		0.4		mA
Regulator					
Pin 2 Reference Voltage			5.8		V
Temperature Coefficient			5		mV/°C
Pin 3 Reference Voltage			5.2		V
Temperature Coefficient			7		mV/°C
Battery Check Oscillator					
Threshold Voltage (Pin 12)		5.5	6.0	6.5	V
Period	V^+ = 7.5V, C1 = 10 μF		40	50	s
Beep Pulse Width	V^+ = 7.5V, C1 = 10 μF		60		ms
Supply Current (Note 3)			6	8	μA
Zener Clamp Voltage, V9	I_9 = 1 mA		14.5		V

Note 1: For operating at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 85°C/W junction to ambient.

Note 2: R_{SET} = 10 MΩ, V^+ = 9V, T_A = 25°C, *(Figure 1)*.

Note 3: Output OFF.



TL/H/9139–2

FIGURE 2. LM1801 Internal Schematic

Applications Hints

CIRCUIT OPERATION

The LM1801 includes a bias string, comparator, steering logic, output transistor, supply clamp, low voltage detector, and reference. An internal schematic is shown in *Figure 2.*

The chip is biased by a group of current sources that are controlled externally by a fixed resistor, R_{set}. In normal, or standby operation the supply current drain is nominally 6 times the set current at pin 1. The voltage at pin 1 is two forward diode potentials (D1 + D2 = 1.2V typical) less than the positive supply voltage. Practical values of R_{set} range from 100 kΩ to 10 MΩ. Higher currents are useful where speed is important, while lower currents promote long battery life.

The total standby current drain of the LM1801 will include, in addition to the above, the current drawn by the external circuits connected at pins 2, 3, and 12. These are the resistive dividers used to set the low battery threshold and comparator threshold.

The voltage comparator consists of devices Q1 through Q10. The input features a common mode range from less than 300 mV to $V^+ - 1.2V$. If the non-inverting input is within this range, the output state remains valid for inverting inputs of 0V to V^+. If the inverting input is within the common mode range, valid comparisons hold for non-inverting inputs of 300 mV to V^+. The comparator may not switch low if the positive input is grounded.

With a set resistance of 10 MΩ, comparator input bias currents of 2 nA are typical. This allows the use of high-value resistors (10 MΩ) at the comparator inputs which help minimize total supply current. The comparator's output is available through a steering diode (D3) for latching or hysteresis functions.

The comparator output is also coupled internally to the steering logic (Q11–Q13). The comparator, low battery detector, and parallel output (pin 10) functions are OR'd in the logic circuit. In addition, the comparator output is steered to the parallel output. If the parallel outputs (pin 10) of two or more chips are wired together along with a common ground, the comparator on any one chip can cause all of the other output stages to switch, as well as its own output. Outputs are switched when the inverting comparator input is positive with respect to the non-inverting input. Low battery functions are coupled to the steering logic via Q12, and therefore do not affect the parallel output (Q13).

If the sense outputs (pin 11) of two or more chips are wired together, the comparator and low battery detector will cause all outputs to switch.

The output transistor is a 0.5A Darlington. Included in this structure are two clamp diodes. D4 clamps positive collector voltage excursions to the supply, and D5 clamps negative excursions to ground.

The output transistor is normally operated with the emitter grounded. Under these conditions the collector is guaranteed to saturate no higher than 1.3V at 200 mA. 1.9V saturation voltage is typical at 500 mA. The emitter may also be used as an output, and it can swing from ground potential up to 5V on a 9V supply. Emitter swing in the positive direction is limited in the parallel output mode.

A low battery detector with a 6V threshold is also included on chip. This circuit consists of Q16, Q17, D11, and D12. When pin 12, the battery sense input, is higher than 6V, D12 clamps the emitter of Q16 to 6.6V, and the output from the current source flows through the zener to ground. If pin 14 drops below 6V, Q16 is biased ON, and current is drawn away from the zener and into Q16. The SCR formed by Q16 and Q17 is triggered when Q16 is biased ON. The capacitor at pin 14 is discharged, part of its charge flows to the steering logic to pulse the output transistor, and the remainder holds the SCR in its ON state.

When the timing capacitor has discharged, conduction in Q16 and Q17 is commutated. Note that the output from the current source is less than the sustaining current required by the SCR. The current source slowly charges the capacitor until the voltage across it rises 0.6V above pin 12, where the cycle repeats itself. If pin 12 rises above 6V, the zener clamps the voltage at pin 14 and the low battery detector remains OFF.

Pin 12 is biased from an external resistive divider. The divider should be designed to detect at no lower than $V^+ = 7V$. The detector will continue to work at lower voltages providing pin 12 is at least 1V below the supply. For a 9V alkaline battery a threshold of 8.2V is common. A resistive divider of 2.7 MΩ and 7.5 MΩ provides the appropriate threshold.

In many applications the on-chip references can provide bias points. The references are driven from D13, and buffered by Q18 and Q19. If only one bias point is needed the first reference (pin 2) should be used, and the unused output (pin 3) may be left open. The tiny leakage currents in Q18 can cause Q19 (pin 3) to drift upward if a 10 MΩ load resistor is not included at pin 2. The combined output current from pins 2 and 3 should not exceed 1 mA. If neither reference output is used, pins 2 and 3 should be left open.

The last section of the LM1801 is the supply zener. It is built from a series combination of two diodes and two zeners. The breakdown voltage at 1 mA is 14.5V, and the series resistance is about 200Ω. In line operated applications the zener may be used for supply regulation or transient protection. The zener is designed to carry up to 10 mA.

Applications Hints (Continued)

DESIGN HINTS

If the comparator inputs are subjected to electrostatic discharges (ESD), a series resistance is recommended to provide protection. Given the low input bias currents, 100 kΩ resistors can be added without affecting circuit performance, yet they greatly enhance static protection. The LM1801 is not designed to withstand reverse battery.

With a 10 MΩ R_{set}, the LM1801 responds to an input in approximately 2.5 μs, and turns OFF in 200 μs. Higher set currents decrease the response time. With R_{set} = 1 MΩ, the output switches low in 0.5 μs, and high in 50 μs, and with R_{set} = 100 kΩ, the response times are reduced to 0.2 μs and 12 μs.

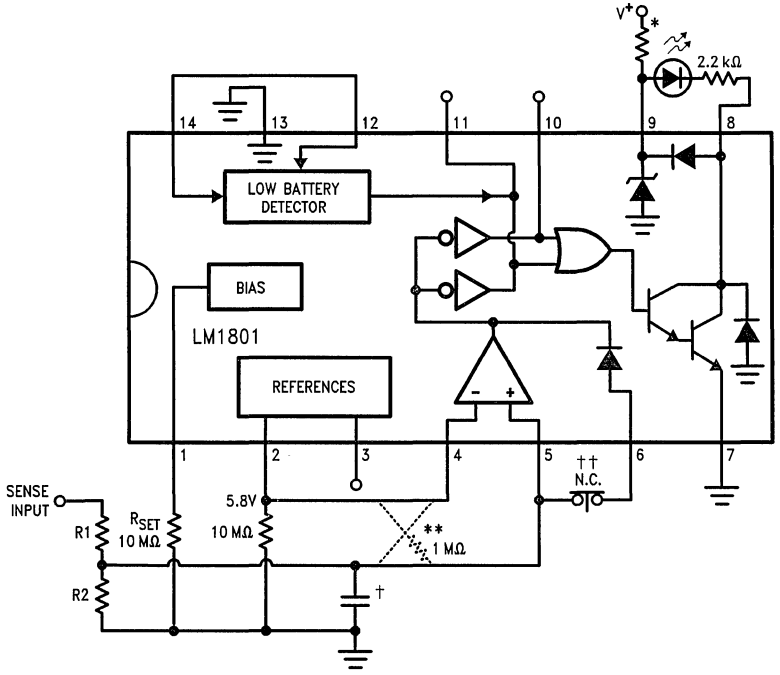
When the circuit is in the standby state (V5 > V4), the current consumption in a typical application such as *Figure 1* is less than approximately 7 μA. However, when the comparator switches LOW (V4 > V5), the supply current increases to 3 mA owing to the Darlington base current. Therefore, to realize maximum battery life, any application should be devised so that V5 > V4 in the standby or resting state.

The output stage can drive lamps, LEDs, buzzers, beepers, relays, motors, and solenoids. However, the low battery detector is not compatible with every load. Since the low battery detector generates only a short pulse (60 ms typical), it is intended for use with buzzers and beepers. Depending on the response time and resonant frequency, some buzzers may only produce a single click. Self-oscillating beepers usually start instantly and produce a recognizable "tweet" when a low battery condition is detected. Incandescent lamps, large relays and solenoids will do absolutely nothing when pulsed by the low battery detector.

Self-oscillating beepers are readily available, such as the Sonalert SNP428 and the Panasonic EAL-069A. These units are guaranteed to self-start when power is applied.

To defeat the low battery detector, short pins 12 and 14 together, and do not connect them to anything else.

Circuit board assembly procedures should include a thorough cleaning to remove flux and other residues. The input pins are often biased by very high impedance sources and even a 10 MΩ leakage path can upset circuit operation.



TL/H/9139–3

$R_1 + R_2 = 10\ M\Omega$

$$V_{TRIP} = \left(\frac{R_1 + R_2}{R_2}\right) 5.8V$$

Minimum trip voltage = 5.8V

*Use series resistor for supplies > 14V. Select for I_{ZENER} = 5 mA.

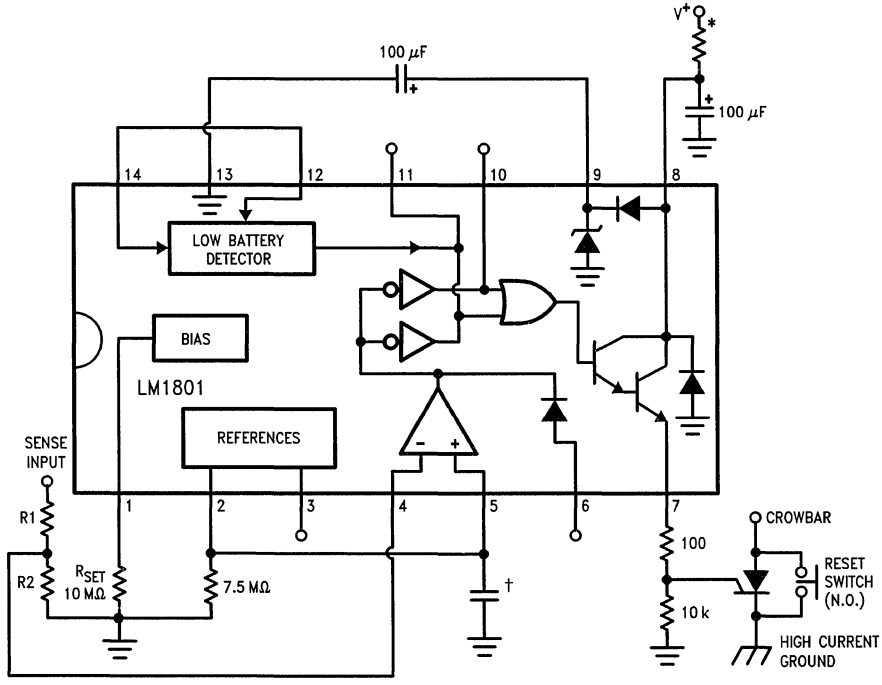
**Reverse connections and add 1 MΩ resistor for overvoltage indication.

†Optional filter capacitor, 1 nF to 100 nF.

††Push to reset. Eliminate pin 6 connection for non-latching operation.

FIGURE 3. Under (Over) Voltage Indicator

Applications Hints (Continued)



TL/H/9139–4

$R_1 + R_2 = 10\ M\Omega$

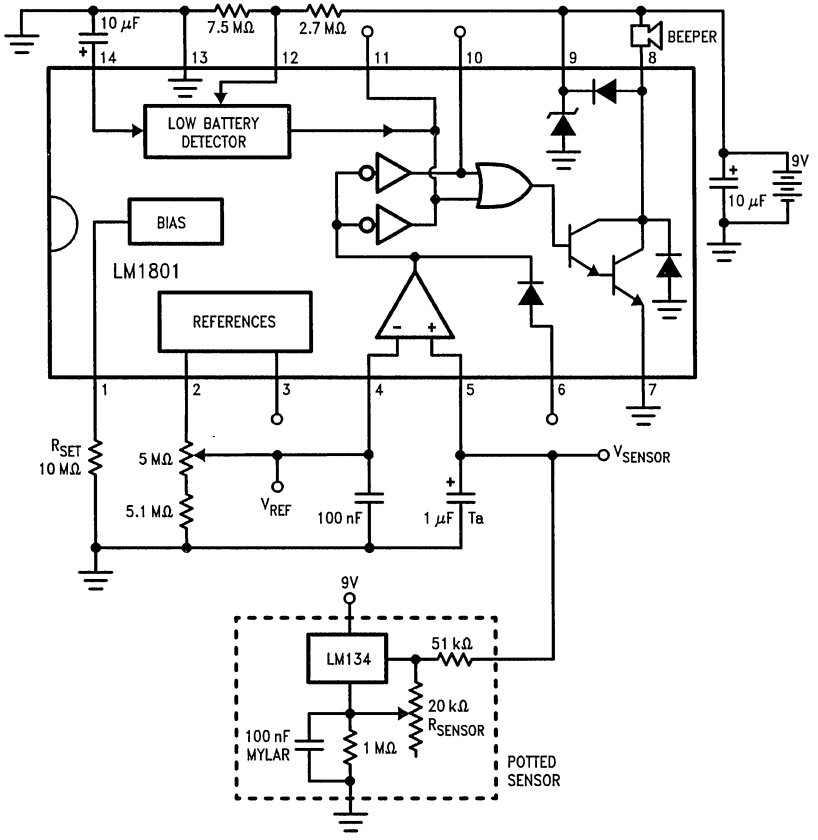
$V_{TRIP} = \left(\frac{R_1 + R_2}{R_2}\right) 5.8V$

*Use series resistor for supplies > 14V.

†Optional filter capacitor, 1 nF to 100 nF.

FIGURE 4. Overvoltage Crowbar

Applications Hints (Continued)



TL/H/9139–5

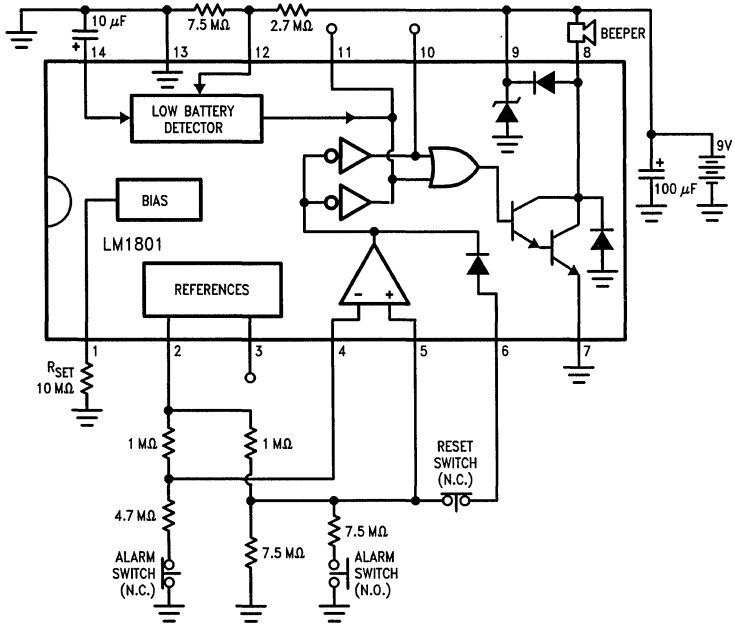
To set trip point, trim V_{REF} to 4.5V. Trim R_{SENSOR} at room temperature (23°C) for:

$$V_{SENSOR} = 4.5\left(\frac{273 + 23}{T_X + 273}\right)$$

where T_X is the desired trip point temperature in °C. As shown, the alarm is activated for over temperature conditions. Reverse the comparator connections for under temperature alarm. The 20 kΩ potentiometer allows an adjustment range of −55°C to +60°C. Add a 10k fixed resistance in series with the potentiometer for a +50°C to +125°C adjustment range. R_{SENSOR} can be replaced by a fixed resistor once the desired value is found. V_{REF} is used as a final adjustment.

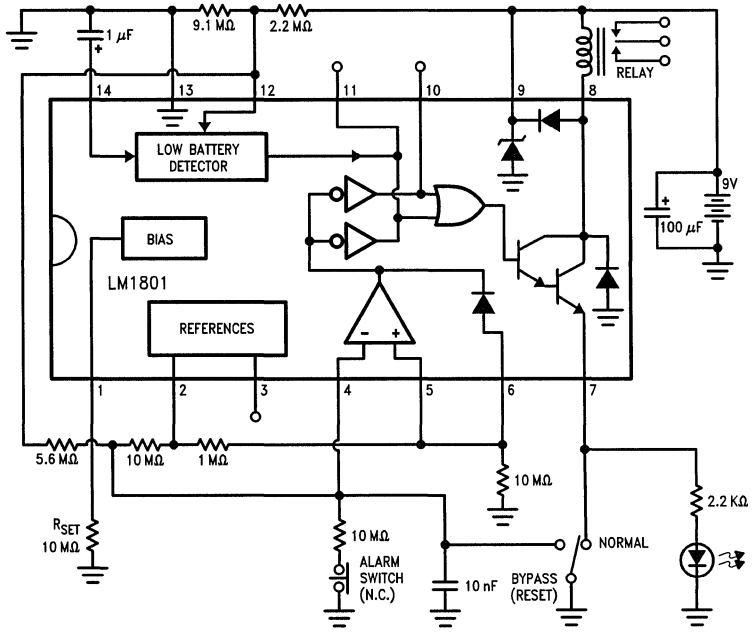
FIGURE 5. Over (Under) Temperature Alarm

Applications Hints (Continued)



TL/H/9139–6

FIGURE 6. Simple Alarm Circuit



TL/H/9139–7

FIGURE 7. Full-Featured Intrusion Alarm

National Semiconductor Corporation

LM1812 Ultrasonic Transceiver

General Description

The LM1812 is a general purpose ultrasonic transceiver designed for use in a variety of ranging, sensing, and communications applications. The chip contains a pulse-modulated class C transmitter, a high gain receiver, a pulse modulation detector, and noise rejection circuitry.

A single LC network defines the operating frequency for both the transmitter and receiver. The class C transmitter output drives up to 1A (12W) peak at frequencies up to 325 kHz. The externally programmed receiver gain provides a detection sensitivity of 200 μVp-p. Detection circuitry included on-chip is capable of rejecting impulse noise with external programming. The detector output sinks up to 1A.

Applications include sonar systems, non-contact ranging, and acoustical data links, in both liquid and gas ambients.

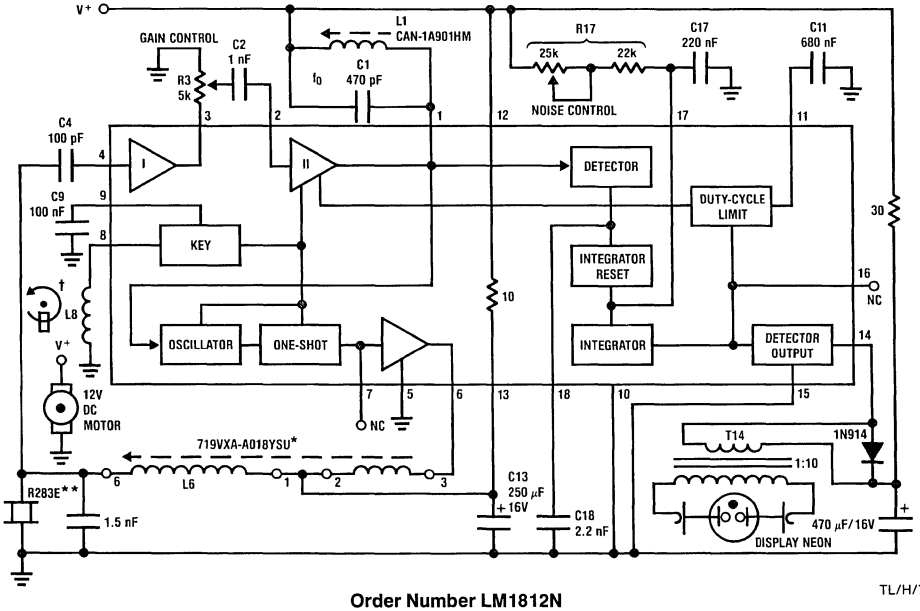
Features

- One or two-transducer operation
- Transducers interchangeable without realignment
- No external transistors
- Impulse noise rejection
- No heat sinking
- Protection circuitry included
- Detector output drives 1A peak load
- Ranges in excess of 100 feet in water, 20 feet in air
- 12W peak transmit power

Applications

- Liquid level measurement
- Sonar
- Surface profiling
- Data links
- Hydroacoustic communications
- Non-contact sensing
- Industrial process control

Typical Application



TL/H/7892–1

Order Number LM1812N
See NS Package Number N18A

†Note: Echo returns are displayed by a neon lamp on a motor driven disc. Connections to the neon are made through brushes and slip rings. Rotating with and counterbalancing the neon lamp is a permanent magnet whose field induces a pulse in a stationary coil (L8) as it passes by. This pulse keys the LM1812's transmitter.

*Available from Toko America, 1250 Feehanville Drive, Mount Prospect, Illinois 60056 Tel. (312) 297-0070

**Available from Massa Products Corporation, 280 Lincoln Street, Hingham, Massachusetts 02043 Tel. (617) 749-4800

FIGURE 1. 200 kHz Depth Sounder, 5 Feet to 100 Feet

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V^+ (Pin 12)	18V
Power Dissipation (Note 1)	1700 mW
Peak Current (Pins 6, 14)	1A
Input Current (Pins 4, 8)	50 mA
Operating Temperature	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

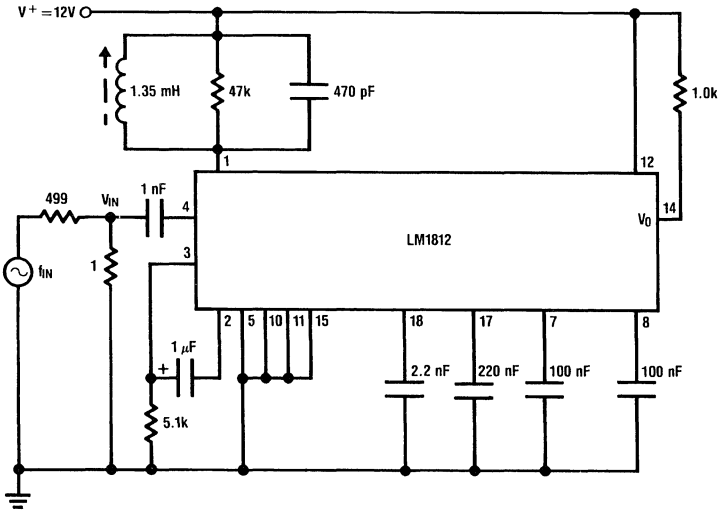
Electrical Characteristics $V^+ = 12V$, $T_A = 25°C$, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
Input Sensitivity (Note 2)	*Figure 2*		200	600	μVp-p
Input Noise			10		μVp-p
Transmitter Output, V_{SAT}	$I_6 = 1A$		1.3	3	V
Transmitter Output Leakage	V6 = 36V V8 = 0V		0.01	1	mA
Detector Output, V_{SAT}	$I_{14} = 1A$		1.5	3	V
Detector Output Leakage	V14 = 36V		0.01	1	mA
Transmitter Key Threshold	$I_8 = 1$ mA	0.55	0.7	0.9	V
Supply Current	$I_1 + I_{12}$ Receive Mode	5	8.5	20	mA
V8 for Receive Mode				0.3	V
Maximum Operating Frequency	Transmit Mode	200	325		kHz

Note 1: For operating at high temperatures, the LM1812 must be derated based upon a 125°C maximum junction temperature and a thermal resistance of 58°C C/W which applies for the device soldered in a printed circuit board and operating in a still air ambient. Due to the low duty cycle operation, only a small average power is dissipated in the package.

Note 2: A 47k resistor is added in parallel with the receiver tank at pin 1 to swamp variations in the coil's unloaded Q. The resistor reduces sensitivity (see equation 4) and is unnecessary in an actual applications circuit.

Test Circuit



TL/H/7892–2

f_{IN} = 200 kHz

Input sensitivity = minimum V_{IN} for V_O to go low

FIGURE 2. Sensitivity Test Circuit

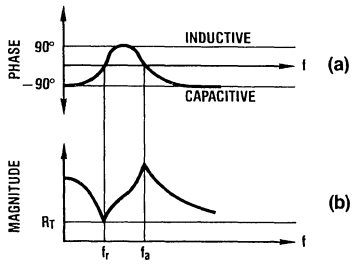
Application Hints

External Component Descriptions

Pin	Component	Typical Values	Pin Description	Component Function
1	L1, C1	500 μH–50 mH 250 pF–2.2 nF	Second gain stage output/ transmitter oscillator	Set the operating frequency (f_O) for the transmit oscillator and receiver
2	C2	500 pF–10 nF	Second gain stage input	Couples first and second gain stage
3	R3	5.1 kΩ	First gain stage output	Terminates emitter-follower output
4	C4	100 pF–10 nF	First gain stage input	Input coupling for the first gain stage
6	L6	50 μH–10 mH	Transmitter output	Matches LM1812 to the transducer
7	—	—	Transmitter driver	—
8	R8	1 kΩ–10 kΩ	Transmitter key	Current limiter for keying pulses up to 12V
9	C9	100 nF–10 μF	Receiver second stage delay	Sets the receiver turn-on delay after transmit (*Figure 10*)
11	C11	220 nF–2.2 μF	Detector output duty cycle limit	Limits the duty cycle of the detector output (short to ground to defeat)
13	C13	100 μF–1000 μF	Transmitter supply decoupling	Decouples the transmitter power supply
14	T14	$L_p \geq 50$ mH $N_S/N_P \cong 10$	Detector output	Drives neon display lamp
16	—	—	Output driver	—
17	R17, C17	22k–Open 10 nF–10 μF	Pulse integrator	Controls integration time constant (*Figure 13*)
18	C18	1 nF–100 μF	Pulse integrator reset	Controls integrator reset time constant (*Figure 14*)

TRANSDUCERS

The most common transducer used with the LM1812 is the piezo-ceramic type which is electrically similar to a quartz crystal. Piezo-ceramic transducers are resistive at only two frequencies, termed the resonant and antiresonant (f_r, f_a) frequencies. Elsewhere these transducers exhibit some reactance as shown in *Figure 3.*



TL/H/7892–3

FIGURE 3. Phase and Magnitude of Transducer Impedance

For transmitting (to maximize electrical to mechanical efficiency), the transducer should be operated at its resonant frequency. For receiving (to maximize mechanical to electrical efficiency), optimum operation is at antiresonance. In two-transducer systems the resonant frequency of the transmit transducer is matched to the antiresonant frequency of the receiver.

The LM1812 is primarily used with a single transducer performing both transmit and receive functions. In this mode, maximum echo sensitivity will occur at a frequency close to resonance.

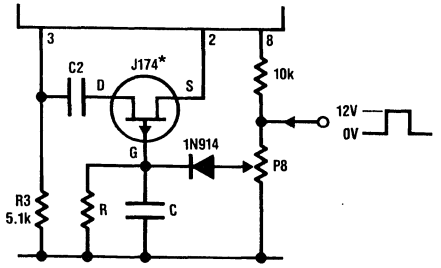
Transducer ringing is a troublesome phenomenon of single transducer systems. After a transducer has been electrically driven in the transmit mode, some time is required for the mechanical vibrations to stop. Depending on the amount of damping, this ringing may last from 10 to 1000 cycles. This mechanical ring produces an electrical signal strong enough (>200 μVp-p) to hold the detector ON, thus masking any echo signals occurring during this time.

A solution to this ring problem is to vary the receiver gain from a minimum, just after transmit, to a maximum, when the ring signal has dropped below the full-gain detection threshold. Since near-range echo signals are much stronger than ring signals, close echos will still be detected in spite of the reduced gain.

The gain is varied by attenuating the signal between pins 2 and 3 of the LM1812. *Figure 4* shows such an arrangement.

An externally generated 12V pulse (*Figure 17*) keys the transmitter and activates the attenuator. This pulse charges C to a voltage set by P8, turning the FET OFF. C slowly discharges through R, decreasing the gate voltage, which in turn decreases the attenuation of the signal passing from pin 3 to pin 2. R and C are selected so that the FET is not

Application Hints (Continued)



TL/H/7892–4

*Available from National Semiconductor Corporation

FIGURE 4. Time Variable FET Attenuator

completely turned ON until all detectable ringing has stopped. The duration of the ring is rarely specified by the transducer manufacturer and must be experimentally determined.

When designing an ultrasonic ranging system, three *transducer* parameters are very important:

1) resonant impedance (R_T in *Figure 3b*)

2) maximum peak-to-peak voltage

3) resonant frequency, f_r

This data, used in conjunction with the curves given in *Figure 6*, results in a functional output stage design.

TRANSMITTER

The transmitter (*Figure 5*) consists of an oscillator, a 1 μs one-shot, and a power amplifier.

When the transmitter is keyed ON at pin 8 the L1-C1 tank is switched to the oscillator mode. An on-chip 1 μs one-shot is triggered with each cycle of the oscillator and, in turn, drives a power amplifier. This one-shot has a reset time of 2 μs, limiting the maximum operating frequency to about 325 kHz. A transformer couples the transducer to the output stage.

The oscillator frequency is set by L1-C1 and can be calculated from

$$f_O = \frac{1}{2\pi\sqrt{L1C1}} \quad (1)$$

The L1-C1 tank must have a minimum R_p of 10 kΩ where

$$R_P = 2\pi f_O Q L1 \quad (2)$$

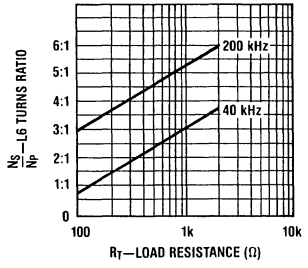
and Q = unloaded Q of L1-C1 tank.

The output transformer (L6) is designed with the aid of *Figure 6*. Curves are shown for two common frequencies: 40 kHz and 200 kHz. For a given load impedance (R_T, *Figure 3b*), a turns ratio for L6 is determined. In order not to exceed the transducer's specifications, the peak-to-peak output voltage may need to be adjusted using the equation:

$$Vp\text{-}p = 2V^+ \left(\frac{N_S}{N_P}\right) \quad (3)$$

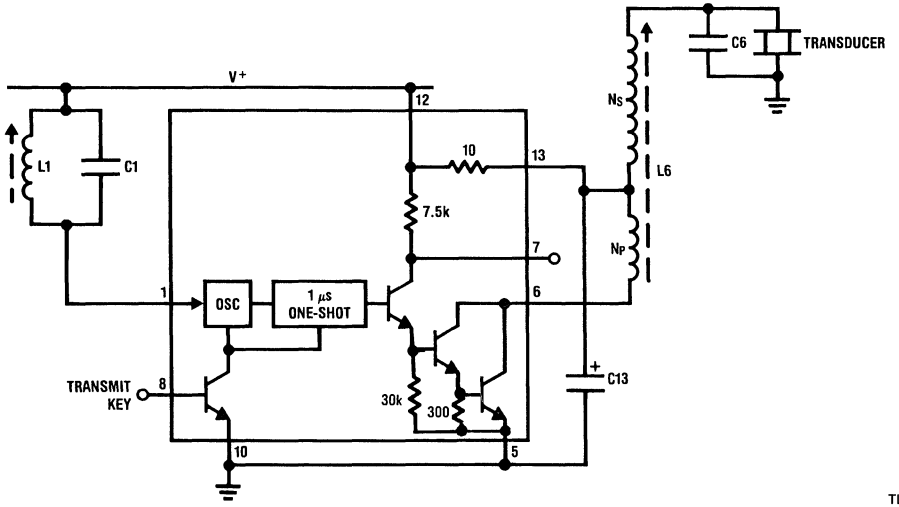
To ensure that the output stage is not overloaded, a current measurement must be made at pin 6. While the first few pulses of each transmit period may reach 2A or 3A, the steady-state current spikes must not exceed 1A. Current spikes are reduced by decreasing the turns ratio of L6.

The secondary of L6 tunes with C6 at the operating frequency, f_O.



TL/H/7892–5

FIGURE 6. L6 Turns Ratio vs Load Resistance



TL/H/7892–6

FIGURE 5. Transmitter

Application Hints (Continued)

Where additional power is desired, a pulse amplifier or a pulse stretcher can be used as shown in *Figure 7*. The pulse amplifier (*Figure 7a*) increases output current up to 5A. The pulse stretcher (*Figure 7b*) increases output current *and* pulse width. The wider pulse of *Figure 7b* is especially useful at lower frequencies where the relatively narrow 1 μs pulse creates a large peak current demand for a given power level. Pulse width as a function of R is plotted in *Figure 8*.

Pin 8 performs the function of switching the LM1812 into either the transmit or receive mode. When pin 8 is held high, the chip is in the transmit mode. When held low, it is in the receive mode. The input current at pin 8 should be designed to operate within a 1 mA–10 mA range.

RECEIVER

The receiver section (*Figure 9*) contains two separate gain stages.

In some applications large voltages are applied across the transducer during transmit. Since the receiver input is coupled to the transducer, some protection is necessary to limit the input current spikes to less than 50 mA. Where the voltage across the transducer is less than 200 Vp-p, a C4 reactance of 5 kΩ at the operating frequency is adequate protection. Above 200 Vp-p, a 5 kΩ resistor should be inserted in series with C4.

Since the L1-C1 tank circuit is shared with the oscillator, both the transmitter and receiver are always tuned to the same frequency. The second stage voltage gain is given by:

$$A_V = \frac{Q}{70}\sqrt{\frac{L1}{C1}} \qquad (4)$$

where Q = unloaded Q of L1-C1 tank.

When the LM1812 is in the transmit mode, the second gain stage is turned OFF. When switching back to the receive mode, the gain stage does not turn ON immediately, but instead turns ON after a slight delay as programmed by C9. This delay blanks the receiver (and therefore the detector) momentarily, giving the transducer time to stop ringing.

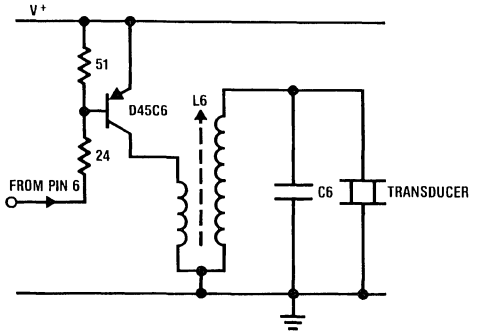


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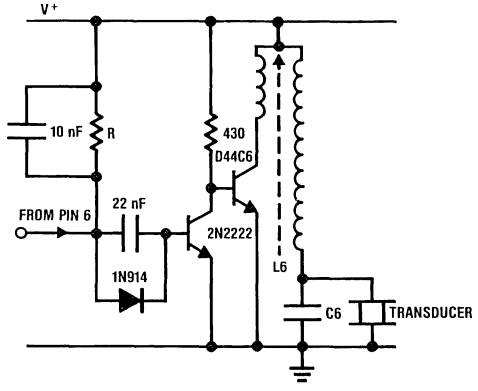
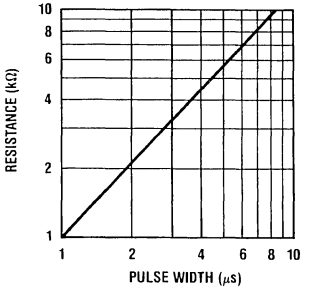
FIGURE 7a. Pulse Amplifier



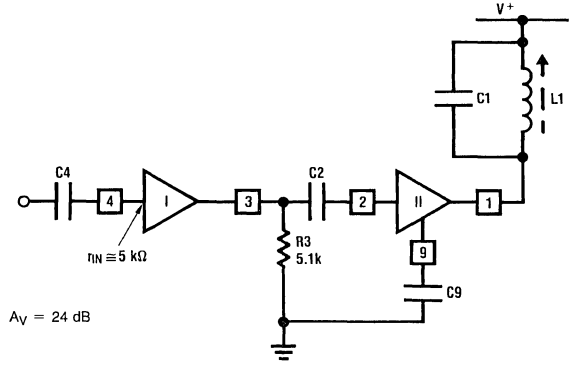
TL/H/7892–8

FIGURE 7b. Pulse Stretcher



TL/H/7892–9

FIGURE 8. Pulse Stretcher Resistance vs Pulse Width



TL/H/7892–10

FIGURE 9. Receiver Section

Application Hints (Continued)

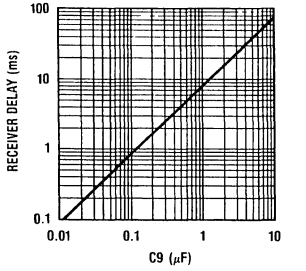
Delay as a function of C9 is plotted in *Figure 10*. The second gain stage may be shut OFF independently of pin 8 by pulling pin 9 low.

Due to the high gain of the receiver, care must be taken to avoid oscillations. Oscillation problems are reduced by keeping the components associated with pins 1 and 4 well separated (*Figure 11*). The transducer must be connected to the circuit with shielded cable. This not only helps avoid oscillation, but also reduces electrical noise pick-up. As a last resort, receiver gain can be reduced with R3 as in *Figure 1*.

PULSE DETECTOR

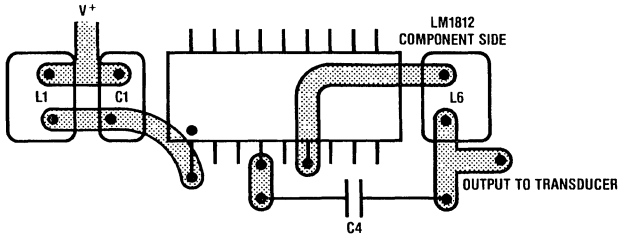
The pulse detector circuitry (*Figure 12*) consists of five distinct stages: 1) threshold detector, 2) pulse integrator reset, 3) pulse integrator, 4) output driver, 5) power output stage.

The detector (Q1, Q2) switches on all pin 1 signals that exceed 1.4 Vp-p. Since noise pulses are also detected, filtering is done by an integrator stage, C17 and R17, whose time constant is typically 10% to 50% of the transmit time. Integration starts when Q3 turns OFF, which occurs at the same moment Q1 and Q2 detect a signal. Pins 16 and 14 go low after the integration delay.



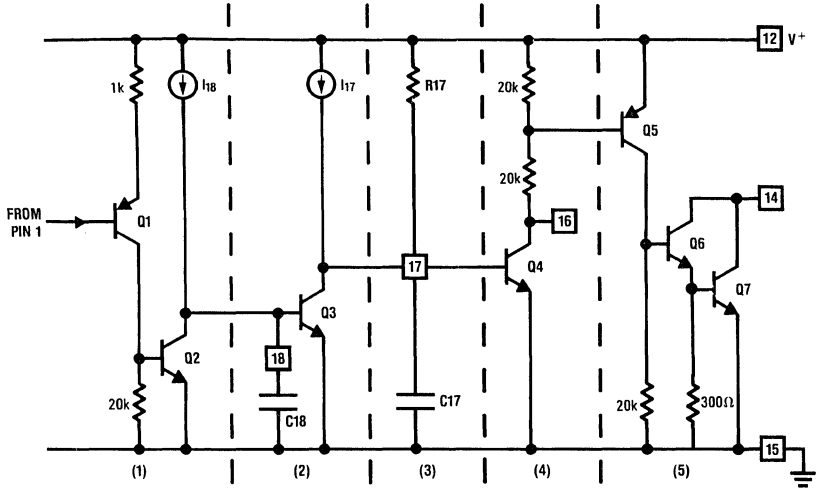
TL/H/7892–11

FIGURE 10. Receiver Delay vs C9



TL/H/7892–12

FIGURE 11. Component Side of Layout Showing Isolation of Receiver Input and Output



TL/H/7892–13

FIGURE 12. Simplified Circuit Diagram of Detector

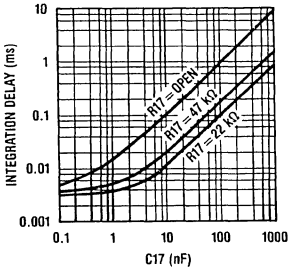
Application Hints (Continued)

When the voltage at pin 1 becomes too small to activate the detector (< 1.4 Vp-p), the integrator is reset by Q3 after a delay introduced by C18. A delay of 1 to 10 cycles of the transmitted frequency is typical. These integration and reset delays, as a function of the external component values, are shown in *Figures 13* and *14*.

Pin 16 provides a CMOS compatible logic output. For driving high-intensity displays, pin 14 will sink up to 1A. When driving a transformer such as T14 in *Figure 1*, it is possible for the primary current to integrate up to destructive levels under conditions of multiple echo reception. Pin 11 is employed to protect the power output (pin 14). C11 integrates an internal current source while pin 14 is low. When V11 reaches a 0.7V threshold, the second gain stage is turned OFF. With the receiver OFF, no signal will be applied to the detector, and pin 14 will turn OFF. After another delay C11 is discharged and the receiver is then again activated. With C11 = 680 nF and a continuous echo return, the receiver will cycle ON and OFF every 6 ms. This function can be defeated by grounding pin 11.

TYPICAL OPERATION

Figure 15 shows typical waveforms at pins 1 and 16 for 200 kHz operation, with pin 9 left open. The pin 1 oscillator signal (5 Vp-p) lasts for 200 μs. The next 900 μs show a ring signal so strong that it is clipped by the receiver. The exponential nature of the decaying ring is seen for the next 500 μs. An echo return appears at 3.9 ms. Note that the detector is held low during the transmit period and for the duration of the ring.



TL/H/7892–14

FIGURE 13. Integration Delay vs C17

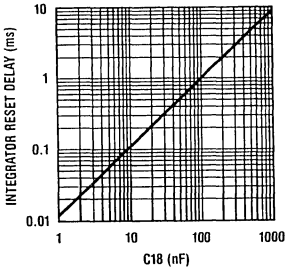


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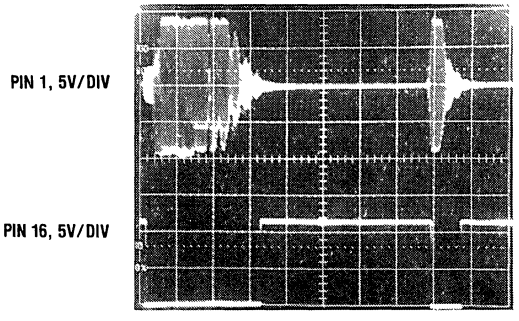
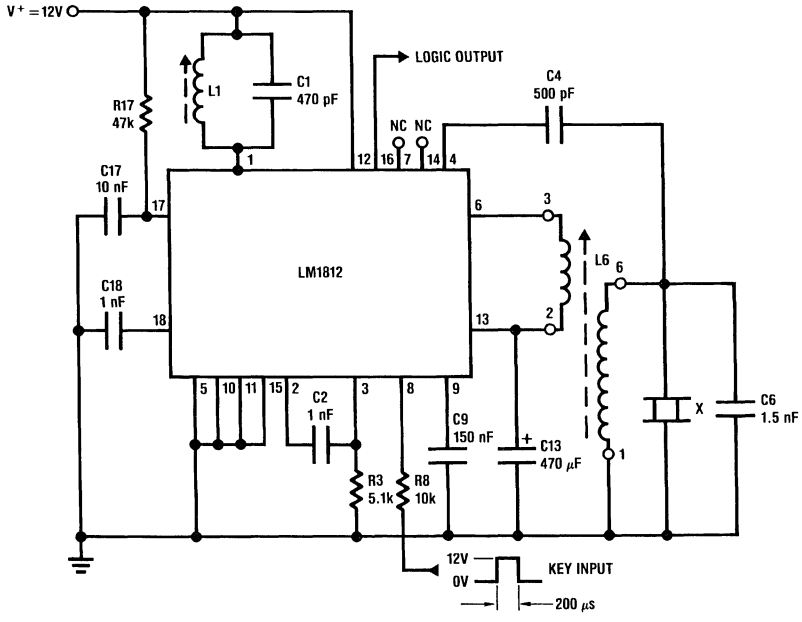
FIGURE 14. Integrator Reset Delay vs C18



TL/H/7892–16

FIGURE 15. Typical Transmit/Receive Waveforms

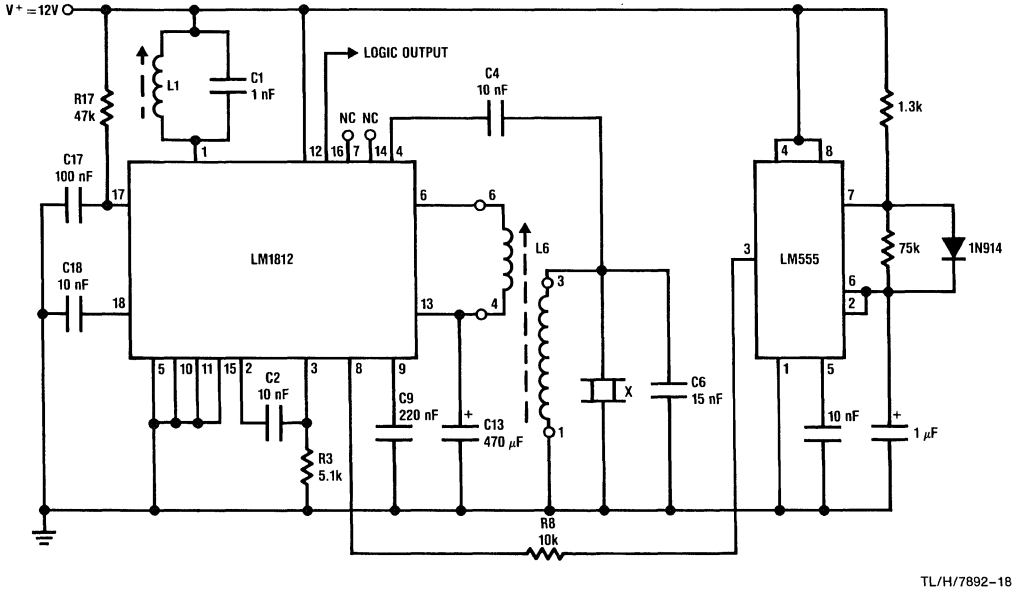
Application Hints (Continued)



TL/H/7892–17

L1 = CAN-1A901HM (Toko)
L6 = 719VXA-A018YSU (Toko)
X = R283E (Massa Products)

FIGURE 16. 200 kHz Ultrasonic Ranging System for 4 Inches to 6 Feet in Air



TL/H/7892–18

L1 = CLN-2A900HM (Toko)
L6 = 719VXA-A017AO (Toko)
X = EFR-OTB40K2 (Available from Panasonic Company, 1 Panasonic Way, Secaucus, NJ 07094, Tel. (201) 392-4511)

FIGURE 17. 40 kHz Ultrasonic Ranging System Covering a Range of 3 Feet to 20 Feet

National Semiconductor Corporation

LM1815 Adaptive Sense Amplifier

General Description

The LM1815 is an adaptive sense amplifier and default gating circuit for motor control applications. The sense amplifier provides a one-shot pulse output whose leading edge coincides with the negative-going zero crossing of a ground referenced input signal such as from a variable reluctance magnetic pick-up coil.

In normal operation, this timing reference signal is processed (delayed) externally and returned to the LM1815. A logic input is then able to select either the timing reference or the processed signal for transmission to the output driver stage.

The adaptive sense amplifier operates with a positive-going threshold which is derived by peak detecting the incoming signal and dividing this down. Thus the input hysteresis varies with input signal amplitude. This enables the circuit to sense in situations where the high speed noise is greater than the low speed signal amplitude. Minimum input signal is 100 mVp-p.

Features

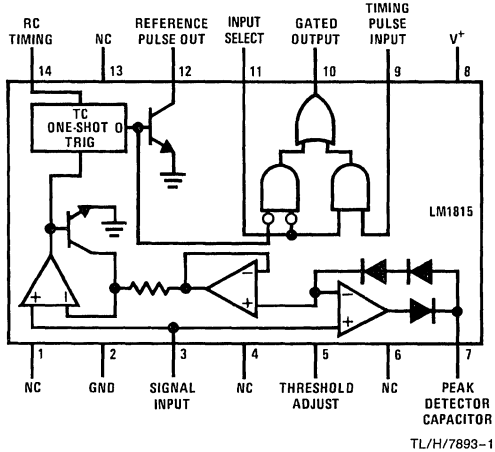
- Adaptive hysteresis
- Single supply operation
- Ground referenced input
- True zero crossing timing reference
- Operates from 2V to 12V supply voltage
- Handles inputs from 100 mV to over 120V with external resistor
- CMOS compatible logic

Applications

- Position sensing with notched wheels
- Zero crossing switch
- Motor speed control
- Tachometer
- Engine testing

Connection Diagram

Dual-In-Line Package



TL/H/7893–1

Top View

Order Number LM1815N
See NS Package Number N14A

Truth Table

Signal Input	Input Select	Timing Input	Gated Output
Pulses	L	X	Pulses
X	H	Pulses	Pulses

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	12V
Power Dissipation (Note 1)	1250 mW
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 2)	+125°C
Input Current	±30 mA
Lead Temperature (Soldering, 10 sec.)	260°C

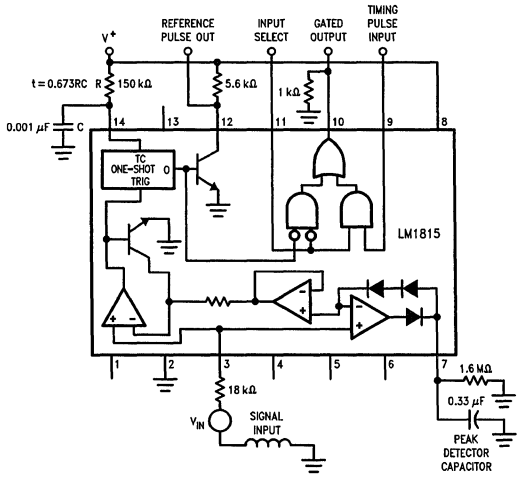
Electrical Characteristics (T_A = 25°C, V_{CC} = 10V, unless otherwise specified, see *Figure 1*)

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage		2.5	10	12	V
Supply Current	f_{IN} = 500 Hz, Pin 9 = 2V, Pin 11 = 0.8V		3.6	6	mA
Reference Pulse Width	f_{IN} = 1 Hz to 2 kHz	70	100	130	μs
Input Bias Current	V_{IN} = 2V, (Pin 9 and Pin 11)			5	μA
Input Bias Current	V_{IN} = 0V dc, (Pin 3)		200		nA
Input Impedance	V_{IN} = 5 Vrms, (Note 3)	12	20	28	kΩ
Zero Crossing Threshold	V_{IN} = 100 mVp-p, (Pin 3)			25	mV
Logic Threshold	(Pin 9 and Pin 11)	0.8	1.1	2.0	V
V_{OUT} High	R_L = 1 kΩ, (Pin 10)	7.5	8.6		V
V_{OUT} Low	I_{SINK} = 0.1 mA, (Pin 10)		0.3	0.4	V
Input Arming Threshold	Pin 5 Open, $V_{IN} \leq$ 135 mVp-p	30	45	60	mV
	Pin 5 Open, $V_{IN} \geq$ 230 mVp-p	40	80	90	% of V_3 Pk
	Pin 5 to V+	200			mV
	Pin 5 to Gnd	−25		25	mV
Output Leakage Pin 12	V_{12} = 11V		0.01	10	μA
Saturation Voltage P12	I_{12} = 2 mA		0.2	0.4	V

Note 1: For operation at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Note 2: Temporary excursions to 150°C can be tolerated.

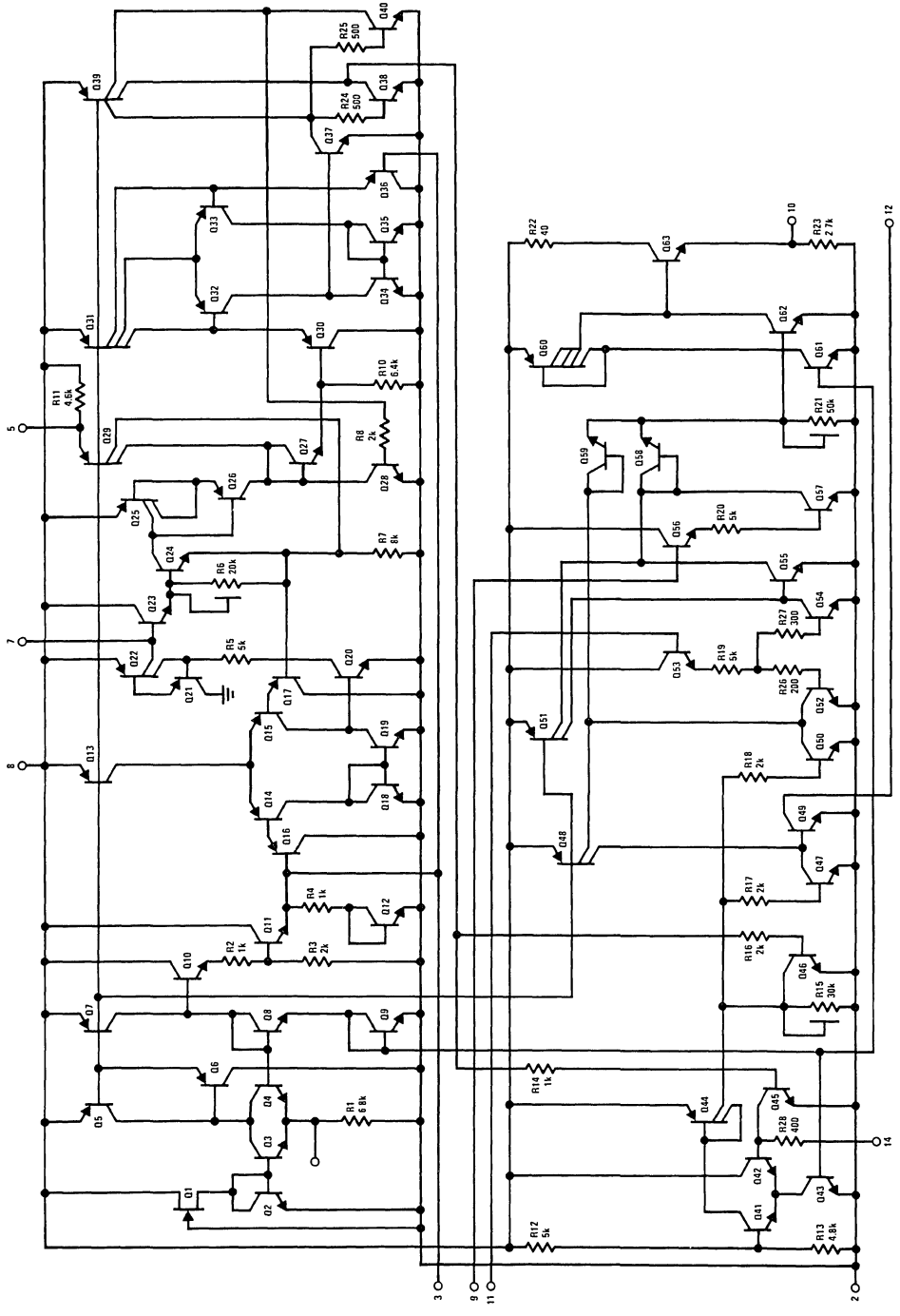
Note 3: Measured at input to external 18 kΩ resistor. IC contains 1 kΩ in series with a diode to attenuate the input signal.



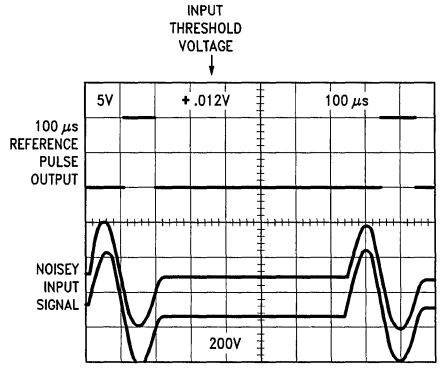
TL/H/7893–2

FIGURE 1. LM1815 Adaptive Sense Amplifier

Schematic Diagram



TL/H/7893–4



TL/H/7893–3

FIGURE 2. LM1815 Oscillograms

Application Hints

Input Clamp

The signal input at pin 3 is internally clamped. Current limit is provided by an external resistor which should be selected to allow a peak current of 3 mA in normal operation. Positive inputs are clamped by a 1 kΩ resistor and series diode, while an active clamp limits pin 3 to −350 mV for negative inputs (see R4, Q12, Q11 in internal schematic diagram).

Operation of Zero Crossing Detector

The LM1815 is designed to operate as a zero crossing detector, triggering an internal one shot on the negative-going edge of the input signal. Unlike other zero crossing detectors, the LM1815 cannot be triggered until the input signal has crossed an "arming" threshold on the positive-going portion of the waveform. The arming circuit is reset when the chip is triggered, and subsequent zero crossings are ignored until the arming threshold is exceeded again. This threshold varies depending on the connection at pin 5. Three different modes of operation are possible:

MODE 1, Pin 5 open. The adaptive mode is selected by leaving pin 5 open circuit. For input signals of less than 135 mVp-p, the input arming threshold is typically 45 mV. Under these conditions the input signal must first cross the 45 mV threshold in the positive direction to arm the zero crossing detector, and then cross zero in the negative direction to trigger it. If the signal is less than 30 mV peak (minimum rating in Electrical Characteristics), the one shot is guaranteed to not trigger.

Input signals of greater than 230 mVp-p cause the arming threshold to track at 80% of the peak input voltage. A peak detector (pin 7) stores a value relative to the positive input peaks to establish the arming threshold. Input signals must cross this threshold in the positive direction to arm the zero crossing detector, which can then be triggered by a negative-going zero crossing. The peak detector tracks rapidly as the input signal amplitude increases, and decays by virtue of the resistor connected externally at pin 7 to track decreases in the input signal.

Note that since the input is clamped, the waveform observed at pin 3 is not identical to the waveform observed at the variable reluctance sensor. Similarly, the voltage stored at pin 7 is not identical to the peak voltage appearing at pin 3.

MODE 2, Pin 5 connected to V+. The input arming threshold is fixed at 200 mV minimum when pin 5 is connected to the positive supply. The chip has no output for signals of less than 200 mV peak, and triggers on the next negative-going zero crossing when the threshold is crossed.

MODE 3, Pin 5 grounded. With pin 5 grounded, the input arming threshold is set to 0V (±25 mV maximum). Positive-going zero crossings arm the chip, and the next negative zero crossing triggers it.

The one shot timing is set by a resistor and capacitor connected to pin 14. The output pulse width is

$$\text{pulse width} = 0.673\,RC \qquad (1)$$

In some systems it is necessary to externally generate pulses, such as during stall conditions when the variable reluctance sensor has no output. External pulse inputs at pin 9 are gated through to pin 10 when the Input Select (pin 11) is pulled high. Pin 12 is a direct output for the one shot and is unaffected by the status of pin 11.

Input/output pins 9, 11, 10 and 12 are all CMOS logic compatible. In addition, pins 9, 11 and 12 are TTL compatible. Pin 10 is not guaranteed to drive a TTL load.

Pins 1, 4, 6 and 13 have no internal connections and can be grounded.

National Semiconductor Corporation

LM1819 Air-Core Meter Driver

General Description

The LM1819 is a function generator/driver for air-core (moving-magnet) meter movements. A Norton amplifier and an NPN transistor are included on chip for signal conditioning as required. Driver outputs are self-centering and develop ±4.5V swing at 20 mA. Better than 2% linearity is guaranteed over a full 305-degree operating range.

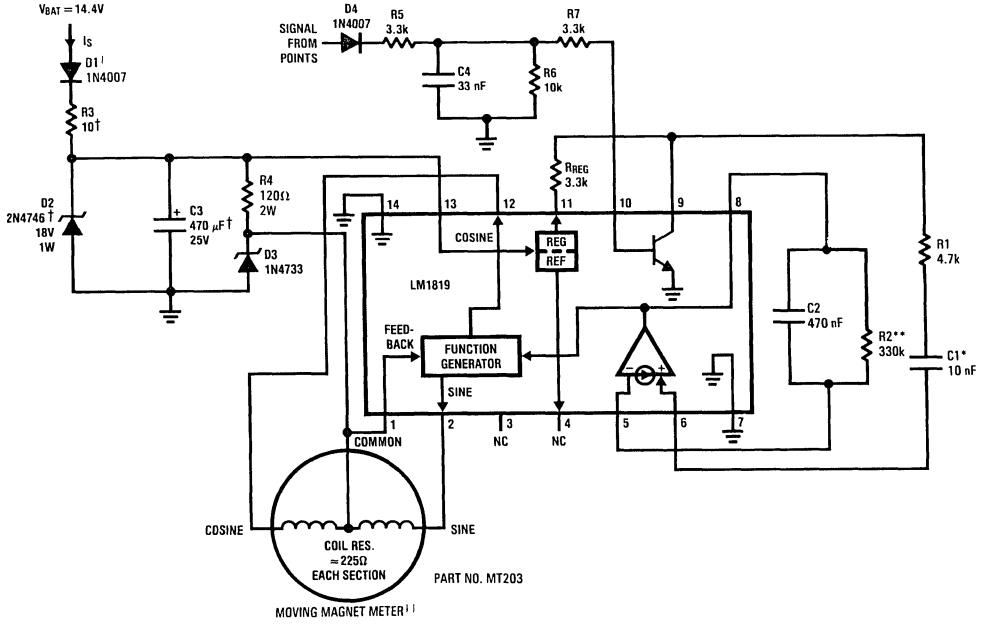
Features

- Self-centering 20 mA outputs
- 12V operation
- Norton amplifier
- Function generator

Applications

- Air-core meter driver
- Tachometers
- Ruggedized instruments

Typical Application



TL/H/5263–1

FIGURE 1. Automotive Tachometer Application. Circuit shown operates with 4 cylinder engine and deflects meter pointer (270°) at 6000 RPM.

Order Number LM1819N
See NS Package Number N14A

*TRW Type X463UW Polycarbonate Capacitor

**RNGOD Low TC Resistor (±100 ppm)

†Components Required for Automotive Load Dump Protection

††Available from FARIA Co.
P O Box 983, Uncasville, CT 06382
Tel. 203-848-9271

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V^+ (pin 13)	20V
Power Dissipation (note 1)	1300 mW
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to −150°C
Lead Temp. (Soldering, 10 seconds)	260°C
BV_{CEO}	$20V_{MIN}$

Electrical Characteristics V_S = 13.1V T_A = 25°C unless otherwise specified

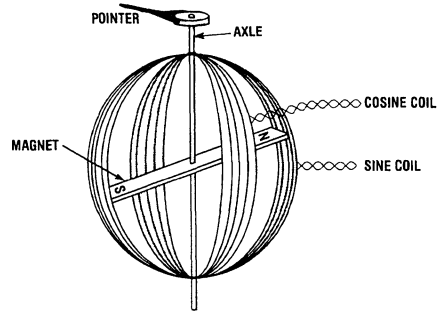
Symbol	Parameter	Pin(s)	Conditions	Min	Typ	Max	Units
I_S	Supply Current	13	Zero Input Frequency (See *Figure 1*)			65	mA
V_{REG}	Regulator Voltage	11	I_{REG} = 0 mA	8.1	8.5	8.9	V
	Regulator Output Resistance	11	I_{REG} = 0 mA to 3 mA		13.5		Ω
V_{REF}	Reference Voltage	4	I_{REF} = 0 mA	1.9	2.1	2.3	V
	Reference Output Resistance	4	I_{REF} = 0 μA to 50 μA		5.3		kΩ
	Norton Amplifier Mirror Gain	5, 6	I_{BIAS} ≅ 20 μA	0.9	1.0	1.1	
h_{FE}	NPN Transistor DC Gain	9, 10			125		
	Function Generator Feedback Bias Current	1	V_1 = 5.1V		1.0		mA
	Drive Voltage Extremes, Sine and Cosine	2, 12	I_{LOAD} = 20 mA	±4	±4.5		V
	Sine Output Voltage with Zero Input	2	$V_8 = V_{REF}$	−350	0	+350	mV
	Function Generator Linearity		FSD = 305°			±1.7	%FSD
k	Function Generator Gain		Meter Deflection/ΔV_8	50.75	53.75	56.75	°/V

Note 1: For operation above 25°C, the LM1819 must be derated based upon a 125°C maximum junction temperature and a thermal resistance of 76°C/W which applies for the device soldered in a printed circuit board and operating in a still-air ambient.

Application Hints

AIR-CORE METER MOVEMENTS

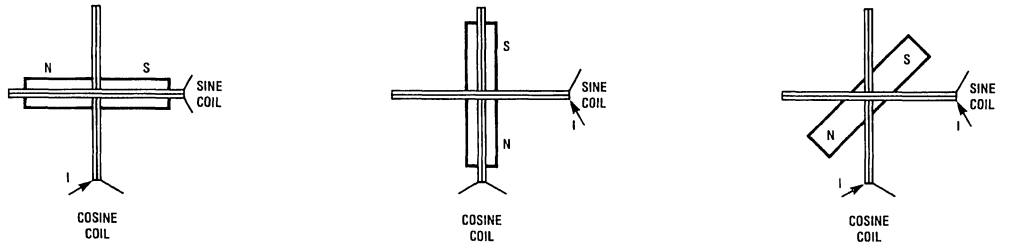
Air-core meters are often favored over other movements as a result of their mechanical ruggedness and their independence of calibration with age. A simplified diagram of an air-core meter is shown in *Figure 2.* There are three basic pieces: a magnet and pointer attached to a freely rotating axle, and two coils, each oriented at a right angle with respect to the other. The only moving part in this meter is the axle assembly. The magnet will tend to align itself with the vector sum of **H** fields of each coil, where **H** is the magnetic field strength vector. If, for instance, a current passes through the cosine coil (the reason for this nomenclature will become apparent later) as shown in *Figure 3(a)*, the magnet will align its magnetic axis with the coil's **H** field. Similarly, a current in the sine coil (*Figure 3(b)*) causes the magnet to align itself with the sine **H** field. If currents are applied simultaneously to both sine and cosine coils, the magnet will turn to the direction of the vector sum of the two **H** fields *(Figure 3(c))*. **H** is proportional to the voltage applied to a coil. Therefore, by varying both the polarity and magnitude of the coil voltages the axle assembly can be made to rotate a full 360°. The LM1819 is designed to drive the meter through a minimum of 305°.



TL/H/5263–2

FIGURE 2. Simplified Diagram of an Air Core Meter.

Application Hints (Continued)



TL/H/5263–3

(a) (b) (c)

FIGURE 3. Magnet and pointer position are controlled by the H field generated by the two drive coils.

In an air-core meter the axle assembly is supported by two nylon bushings. The torque exerted on the pointer is much greater than that found in a typical d'Arsonval movement. In contrast to a d'Arsonval movement, where calibration is a function of spring and magnet characteristics, air-core meter calibration is only affected by the mechanical alignment of the drive coils. Mechanical calibration, once set at manufacture, can not change.

Making pointer position a linear function of some input is a matter of properly ratioing the drive to each coil. The **H** field contributed by each coil is a function of the applied current, and the current is a function of the coil voltage. Our desired result is to have θ (pointer deflection, measured in degrees) proportional to an input voltage:

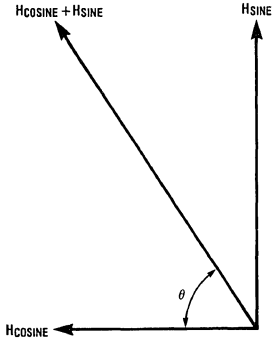
$$\theta = kV_{IN} \qquad [1]$$

where k is a constant of proportionality, with units of degrees/volt. The vector sum of each coils' **H** field must follow the deflection angle θ. We know that the axle assembly always points in the direction of the vector sum of $\mathbf{H}_{SINE}$ and $\mathbf{H}_{COSINE}$. This direction (see *Figure 4*) is found from the formula:

$$(\theta) = \arctan \{ | \mathbf{H}_{SINE} | / | \mathbf{H}_{COSINE} | \} \qquad [2]$$

Recalling some basic trigonometry,

$$(\theta) = \arctan(\sin(\theta) / \cos(\theta)) \qquad [3]$$



TL/H/5263–4

FIGURE 4. The vector sum of $\mathbf{H}_{COSINE}$ and $\mathbf{H}_{SINE}$ points in a direction θ measured in a clockwise direction from $\mathbf{H}_{COSINE}$.

Comparing [3] to [2] we see that if $\mathbf{H}_{SINE}$ varies as the sine of θ, and $\mathbf{H}_{COSINE}$ varies as the cosine of θ, we will generate a net **H** field whose direction is the same as θ. And since the axle assembly aligns itself with the net **H** field, the pointer will always point in the direction of θ.

THE LM1819

Included in the LM1819 is a function generator whose two outputs are designed to vary approximately as the sine and cosine of an input. A minimum drive of ±20 mA at ±4V is available at pins 2 (sine) and 12 (cosine). The common side of each coil is returned to a 5.1V zener diode reference and fed back to pin 1.

For the function generator, $k \cong 54°/V$ (in equation 1). The input (pin 8) is internally connected to the Norton amplifier's output. V_{IN} as considered in equation [1] is actually the difference of the voltages at pins 8 (Norton output/function generator input) and 4. Typically the reference voltage at pin 4 is 2.1V. Therefore,

$$\theta = k(V_8 - V_{REF}) = 54\ (V_8 - 2.1) \qquad [4]$$

As V_8 varies from 2.1V to 7.75V, the function generator will drive the meter through the chip's rated 305° range.

Air-core meters are mechanically zeroed during manufacture such that when only the cosine coil is driven, the pointer indicates zero degrees deflection. However, in some applications a slight trim or offset may be required. This is accomplished by sourcing or sinking a DC current of a few microamperes at pin 4.

A Norton amplifier is available for conditioning various input signals and driving the function generator. A Norton amplifier was chosen since it makes a simple frequency to voltage converter. While the non-inverting input (pin 6) bias is at one diode drop above ground, the inverting input (5) is at 2.1V, equal to the pin 4 reference. Mirror gain remains essentially flat to $I_{MIRROR} = 5$ mA. The Norton amplifier's output (8) is designed to source current into its load. To bypass the Norton amplifier simply ground the non-inverting input, tie the inverting input to the reference, and drive pin 8 (Norton output/function generator input) directly.

An NPN transistor is included on chip for buffering and squaring input signals. Its usefulness is exemplified in *Figures 1 & 6* where an ignition pulse is converted to a rectangular waveform by an RC network and the transistor. The emitter is internally connected to ground. It is important not to allow the base to drop below $-5V_{dc}$, as damage may occur. The 2.1V reference previously described is derived from an 8.5V regulator at pin 11. Pin 11 is used as a stable supply for collector loads, and currents of up to 5 mA are easily accommodated.

Application Hints (Continued)

TACHOMETER APPLICATION

A measure of the operating level of any motor or engine is the rotational velocity of its output shaft. In the case of an automotive engine the crankshaft speed is measured using the units "revolutions per minute" (RPM). It is possible to indirectly measure the speed of the crankshaft by using the signal present on the engine's ignition coil. The fundamental frequency of this signal is a function of engine speed and the number of cylinders and is calculated (for a four-stroke engine) from the formula:

$$f = n\omega/120 \quad \text{(Hz)} \quad (5)$$

where n = number of cylinders, and ω = rotational velocity of the crankshaft in RPM. From this formula the maximum frequency normally expected (for an 8 cylinder engine turning 4500RPM) is 300 Hz. In certain specialized ignition systems (motorcycles and some automobiles) where the coil waveform is operated at twice this frequency ($f = \omega/60$). These systems are identified by the fact that multiple coils are used in lieu of a single coil and distributor. Also, the coils have two outputs instead of one.

A typical automotive tachometer application is shown in *Figure 1*. The coil waveform is filtered, squared and limited by the RC network and NPN transistor. The frequency of the pulse train at pin 9 is converted to a proportional voltage by the Norton amplifier's charge pump configuration. The ignition circuit shown in *Figure 5* is typical of automotive systems. The switching element "S" is opened and closed in synchronism with engine rotation. When "S" is closed, energy is stored in Lp. When opened, the current in Lp diverts from "S" into C. The high voltage produced in Ls when "S" is opened is responsible for the arcing at the spark plug. The coil voltage (see *Figure 6*) can be used as an input to the LM1819 tachometer circuit. This waveform is essentially constant *duty cycle*. D4 rectifies this waveform thereby preventing negative voltages from reaching the chip. C4 and R5 form a low pass filter which attenuates the high frequency ringing, and R7 limits the input current to about 2.5mA. R6 acts as a base bleed to shut the transistor OFF when "S" is closed. The collector is pulled up to the internal regulator by R_{REG}. The output at pin 9 is a clean rectangular pulse.

Many ignition systems use magnetic, hall effect or optical sensors to trigger a solid state switching element at "S." These systems (see the LM1815) typically generate pulses of constant *width* and amplitude suitable for driving the charge pump directly.

The charge pump circuit in *Figure 7* can be operated in two modes: constant input pulse width (C1 acts as a coupling capacitor) and constant input duty cycle (C1 acts as a differentiating capacitor). The transfer functions for these two modes are quite diverse. However, deflection is always directly proportional to R2 and ripple is proportional to C2.

The following variables are used in the calculation of meter deflection:

symbol	description
n	number of cylinders
ω, ω_{IDLE}	engine speed at redline and idle, RPM
θ	pointer deflection at redline, degrees
δ	charge pump input pulse width, seconds
V_{IN}	peak to peak input voltages, volts
$\Delta\theta$	maximum desired ripple, degrees
k	function generator gain, degrees/volt
f, f_{IDLE}	input frequency at redline and idle, Hz

Where the NPN transistor and regulator are used to create a pulse $V_{IN} = 8.5V$. Acceptable ripple ranges from 3 to 10 degrees (a typical pointer is about 3 degrees wide) depending on meter damping and the input frequency.

The constant pulse width circuit is designed using the following equations:

(1) $100\ \mu A < \dfrac{V_{IN}}{R1} < 3\ mA$

(2) $C_1 \geq \dfrac{10\delta}{R_1}$

(3) $R_2 = \dfrac{R_1\theta}{V_{IN}\delta k f} = \dfrac{120R_1\theta}{V_{IN}n\omega\delta k}$

(4) $C_2 = \dfrac{1}{R_2\Delta\theta f_{IDLE}} = \dfrac{1}{R_2\Delta\theta n\omega_{IDLE}}$

The constant duty cycle equations are as follows:

$R_{REG} \geq 3\ k\Omega$

$R_1 \leq V_{IN} \times 10^4 - R_{REG}$

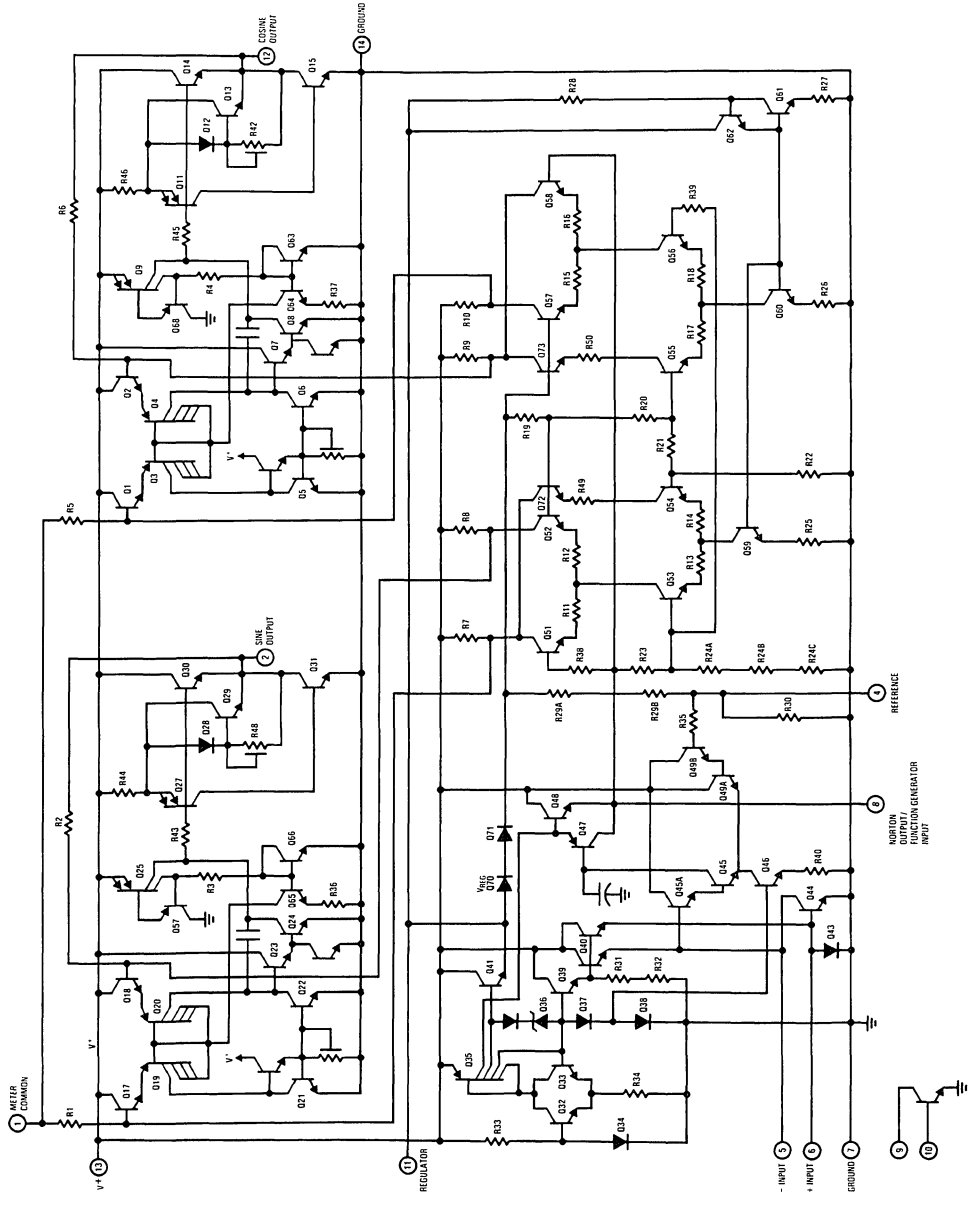
$C_1 \leq \delta/10(R_{REG} + R_1)$

$R_Z = \theta/3.54n\omega C_1 = \theta/425 f C_1$

$C_2 = 425C_1/\Delta\theta$

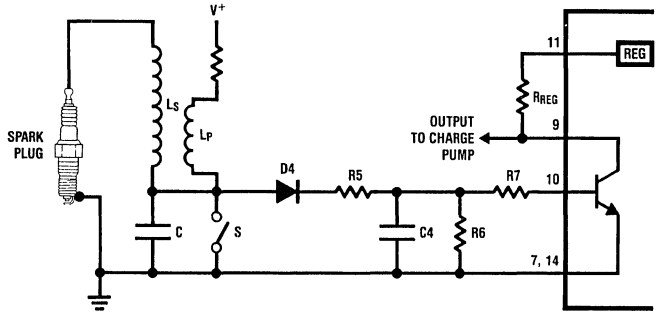
The values in *Figure 1* were calculated with n = 4, ω = 6000RPM, θ = 270 degrees, δ = 1 ms, V_{IN} is $V_{REG} - 0.7V$, and $\Delta\theta$ = 3 degrees in the constant duty cycle mode. For distributorless ignitions these same equations will apply if $\omega/60$ is substituted for f.

Equivalent Schematic



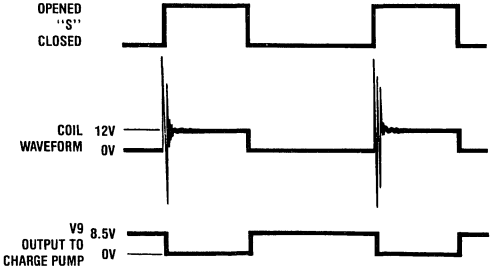
TL/H/5263–12

Typical Applications



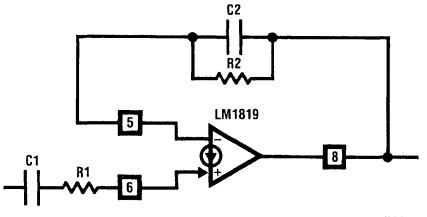
TL/H/5263–9

FIGURE 5. Typical Pulse-Squaring Circuit for Automotive Tachometers.



TL/H/5263–10

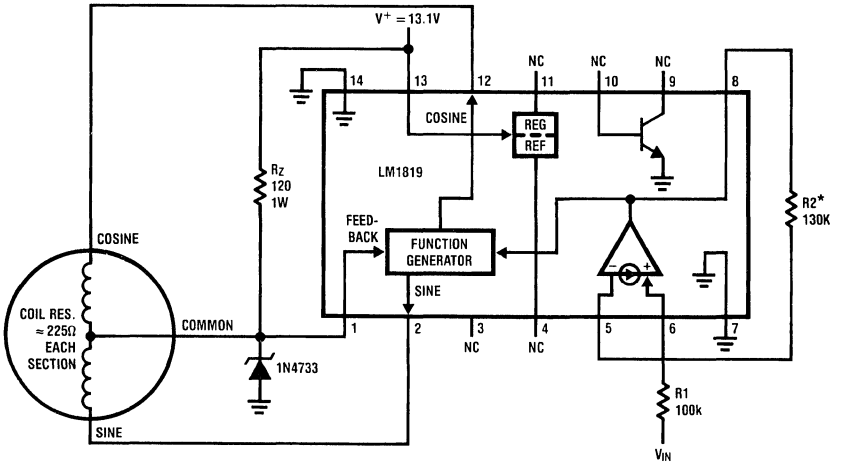
FIGURE 6. Waveforms Encountered in Automotive Tachometer Circuit.



TL/H/5263–11

FIGURE 7. Tachometer Charge Pump.

Voltage Driven Meter with Norton Amplifier Buffer



TL/H/5263–5

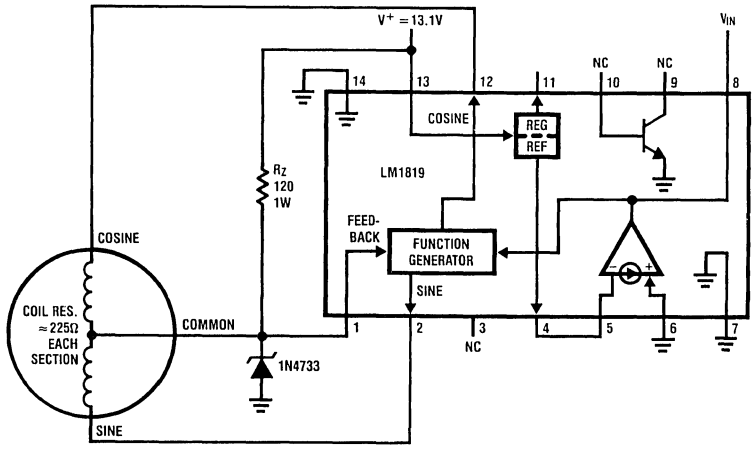
Deflection = 54 $(V_{IN} - .7)R_2/R_1$ (degrees)

0 to 305° deflection is obtained with .7 to 5V input.

*Full scale deflection is adjusted by trimming R_2.

Typical Applications (Continued)

Unbuffered Voltage Driven Meter



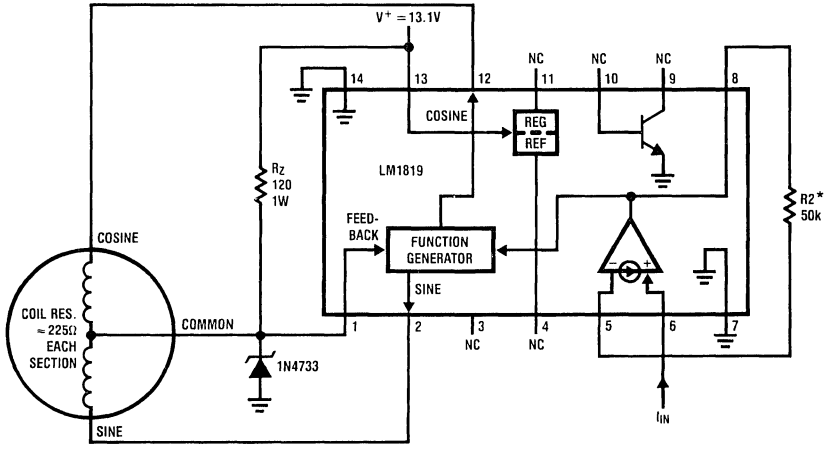
TL/H/5263–6

Deflection = $54(V_{IN} - 2.1)$ (degrees)

0 to 305° deflection is obtained for inputs of 2.1 to 7.75V.

Full scale deflection is adjusted by trimming the input voltage.

Current Driven Meter



TL/H/5263–7

Deflection = $54R_2I_{IN}$ (degrees)

Inputs of 0 to 100 μA deflect the meter 0 to 270°.

*Full scale deflection is adjusted by trimming R_2.

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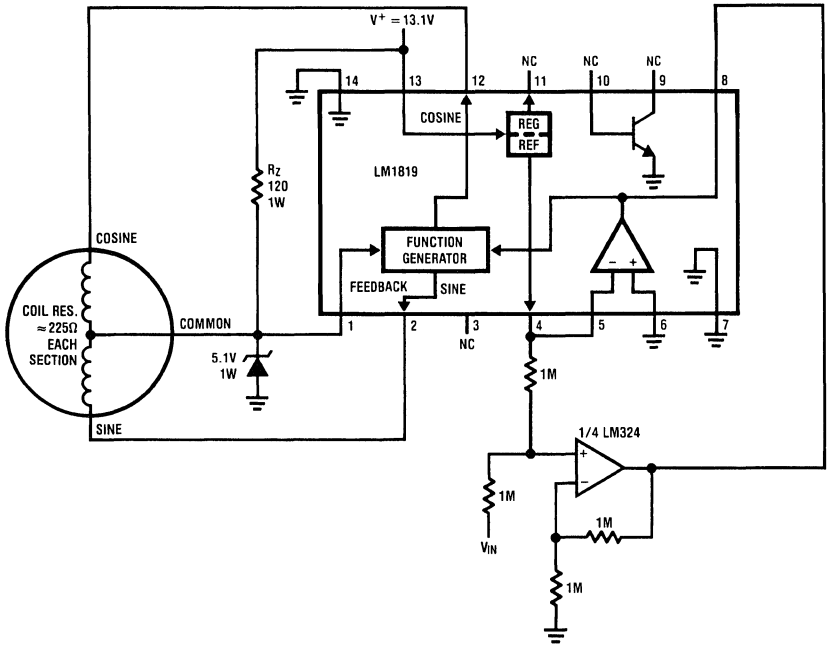
Typical Applications (Continued)

Level Shifted Voltage Driven Meter



TL/H/5263–8

Deflection = $54V_{IN}$ (degrees)

Inputs of 0 to 5.65V deflect the meter through a range of 0 to 305°.

Full scale deflection is adjusted by trimming the input voltage.

National Semiconductor Corporation

LM1830 Fluid Detector

General Description

The LM1830 is a monolithic bipolar integrated circuit designed for use in fluid detection systems. The circuit is ideal for detecting the presence, absence, or level of water, or other polar liquids. An AC signal is passed through two probes within the fluid. A detector determines the presence or absence of the fluid by comparing the resistance of the fluid between the probes with the resistance internal to the integrated circuit. An AC signal is used to overcome plating problems incurred by using a DC source. A pin is available for connecting an external resistance in cases where the fluid impedance is of a different magnitude than that of the internal resistor. When the probe resistance increases above the preset value, the oscillator signal is coupled to the base of the open-collector output transistor. In a typical application, the output could be used to drive a LED, loud speaker or a low current relay.

Features

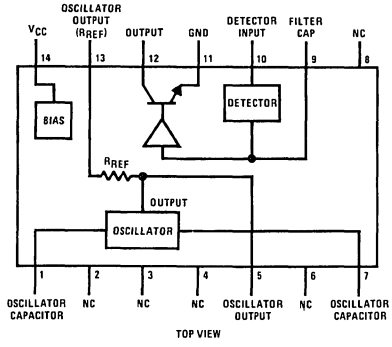
- Low external parts count
- Wide supply operating range
- One side of probe input can be grounded
- AC coupling to probe to prevent plating
- Internally regulated supply
- AC or DC output

Applications

- Beverage dispensers
- Water softeners
- Irrigation
- Sump pumps
- Aquaria
- Radiators
- Washing machines
- Reservoirs
- Boilers

Logic and Connection Diagram

Dual-In-Line Package



TL/H/5700–1

Order Number LM1830N
See NS Package Number N14A

5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

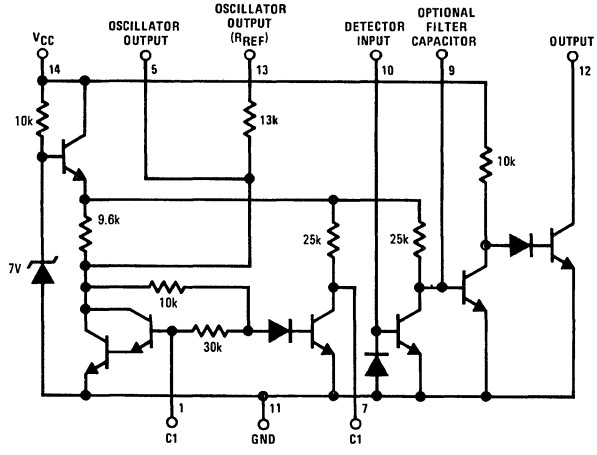
Supply Voltage	28V
Power Dissipation (Note 1)	1400 mW
Output Sink Current	20 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

Electrical Characteristics ($V^+ = 16V$, $T_A = 25°C$ unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Supply Current			5.5	10	mA
Oscillator Output Voltage					
Low			1.1		V
High			4.2		V
Internal Reference Resistor		8	13	25	kΩ
Detector Threshold Voltage			680		mV
Detector Threshold Resistance		5	10	15	kΩ
Output Saturation Voltage	$I_O = 10$ mA		0.5	2.0	V
Output Leakage	$V_{PIN\ 12} = 16V$			10	μA
Oscillator Frequency	C1 = 0.00 1μF	4	7	12	kHz

Note 1: The maximum junction temperature rating of the LM1830N is 150°C. For operation at elevated temperatures, devices in the dual-in-line plastic package must be derated based on a thermal resistance of 89°C/W.

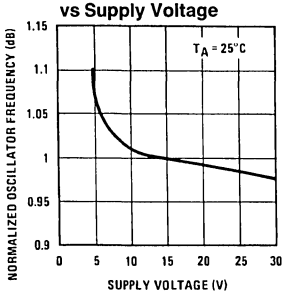
Schematic Diagram



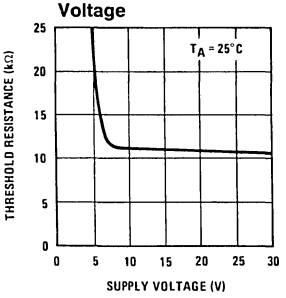
TL/H/5700–2

Typical Performance Characteristics

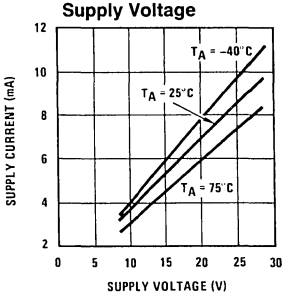
Normalized Oscillator Frequency vs Supply Voltage



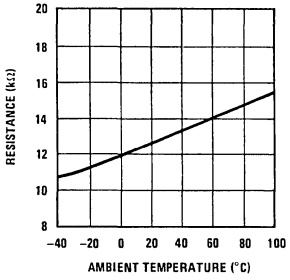
Threshold Resistance vs Supply Voltage



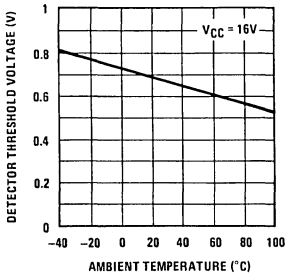
Power Supply Current vs Supply Voltage



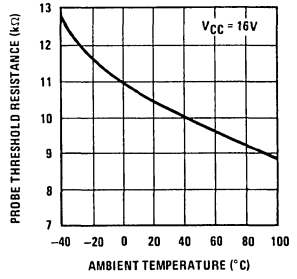
Reference Resistor vs Ambient Temperature



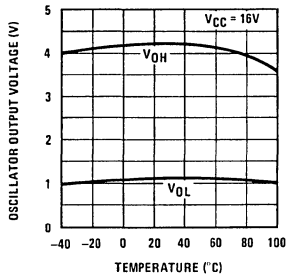
Detector Threshold Voltage vs Temperature



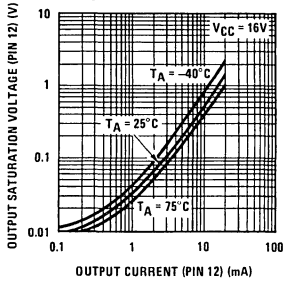
Probe Threshold Resistance vs Temperature



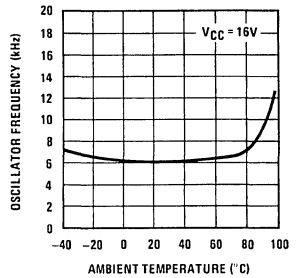
Oscillator V_{OH} and V_{OL} vs Ambient Temperature



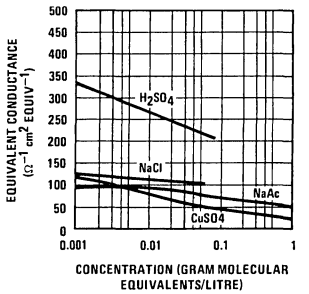
Output Saturation Voltage vs Output Current



Oscillator Frequency vs Ambient Temperature



Equivalent Resistance vs Concentration of Several Solutions



TL/H/5700–3

5

Application Hints

The LM1830 requires only an external capacitor to complete the oscillator circuit. The frequency of oscillation is inversely proportional to the external capacitor value. Using 0.001 μF capacitor, the output frequency is approximately 6 kHz. The output from the oscillator is available at pin 5. In normal applications, the output is taken from pin 13 so that the internal 13k resistor can be used to compare with the probe resistance. Pin 13 is coupled to the probe by a blocking capacitor so that there is no net dc on the probe.

Since the output amplitude from the oscillator is approximately 4 V_{BE}, the detector (which is an emitter base junction) will be turned "ON" when the probe resistance to ground is equal to the internal 13 kΩ resistor. An internal diode across the detector emitter base junction provides symmetrical limiting of the detector input signal so that the probe is excited with ± 2 V_{BE} from a 13 kΩ source. In cases where the 13 kΩ resistor is not compatible with the probe resistance range, an external resistor may be added by coupling the probe to pin 5 through the external resistor as shown in *Figure 2*. The collector of the detecting transistor is brought out to pin 9 enabling a filter capacitor to be connected so that the output will switch "ON" or "OFF" depending on the probe resistance. If this capacitor is omitted, the output will be switched at approximately 50% duty cycle when the probe resistance exceeds the reference resistance. This can be useful when an audio output is required and the output transistor can be used to directly drive a loud speaker. In addition, LED indicators do not require dc excitation. Therefore, the cost of a capacitor for filtering can be saved.

In the case of inductive loads or incandescent lamp loads, it is recommended that a filter capacitor be employed.

In a typical application where the device is employed for sensing low water level in a tank, a simple steel probe may be inserted in the top of the tank with the tank grounded. Then when the water level drops below the tip of the probe, the resistance will rise between the probe and the tank and the alarm will be operated. This is illustrated in *Figure 3*. In situations where a non-conductive container is used, the probe may be designed in a number of ways. In some cases a simple phono plug can be employed. Other probe designs include conductive parallel strips on printed circuit boards.

It is possible to calculate the resistance of any aqueous solution of an electrolyte for different concentrations, provided the dimensions of the electrodes and their spacing is known.

The resistance of a simple parallel plate probe is given by:

$$R = \frac{1000}{c.p} \bullet \frac{d}{A}\ \Omega$$

where A = area of plates (cm^2)

d = separation of plates (cm)

c = concentration (gm. mol. equivalent/litre)

p = equivalent conductance (Ω^{-1} cm^2 equiv. $^{-1}$)

(An equivalent is the number of moles of a substance that gives one mole of positive charge and one mole of negative charge. For example, one mole of NaCl gives $Na^+ + Cl^-$ so the equivalent is 1. One mole of $CaCl_2$ gives $Ca^{++} + 2Cl^-$ so the equivalent is 1/2.)

Usually the probe dimensions are not measured physically, but the ratio d/A is determined by measuring the resistance of a cell of known concentration c and equivalent conductance of 1. A graph of common solutions and their equivalent conductances is shown for reference. The data was derived from D.A. MacInnes, "The Principles of Electrochemistry," Reinhold Publishing Corp., New York., 1939.

In automotive and other applications where the power source is known to contain significant transient voltages, the internal regulator on the LM1830 allows protection to be provided by the simple means of using a series resistor in the power supply line as illustrated in *Figure 4*. If the output load is required to be returned directly to the power supply because of the high current required, it will be necessary to provide protection for the output transistor if the voltages are expected to exceed the data sheet limits.

Although the LM1830 is designed primarily for use in sensing conductive fluids, it can be used with any variable resistance device, such as light dependent resistor or thermistor or resistive position transducer.

The following table lists some common fluids which may and may not be detected by resistive probe techniques.

Conductive Fluids	Non-Conductive Fluids
City water	Pure water
Sea water	Gasoline
Copper sulphate solution	Oil
Weak acid	Brake fluid
Weak base	Alcohol
Household ammonia	Ethylene glycol
Water and glycol mixture	Paraffin
Wet soil	Dry soil
Coffee	Whiskey

Typical Applications V_{CC} = 16V

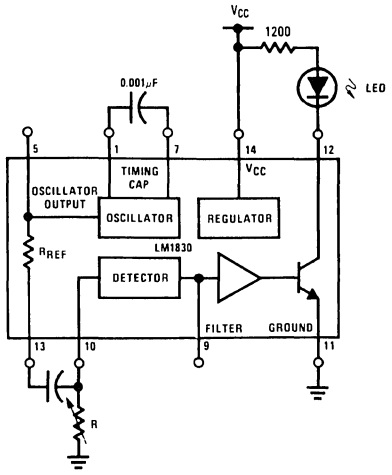


FIGURE 1. Test Circuit

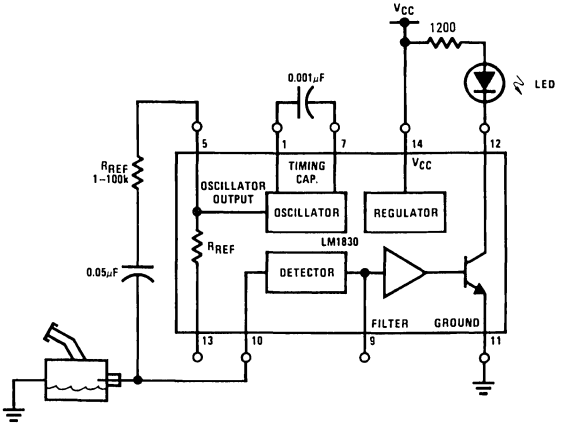


FIGURE 2. Application Using External Reference Resistor

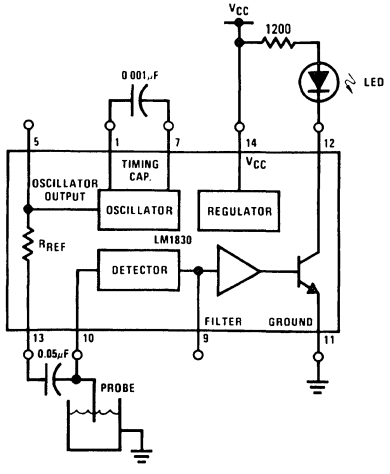
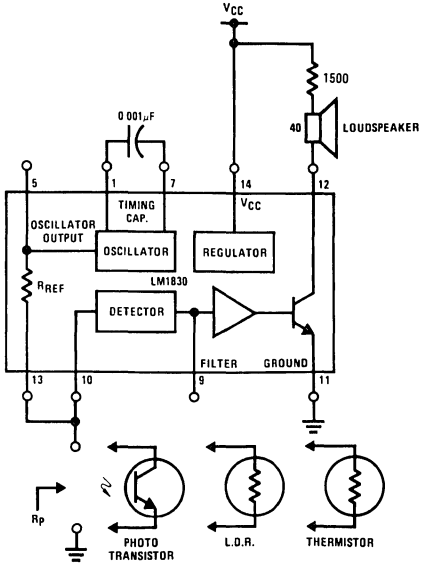


FIGURE 3. Basic Low Level Warning Device with LED Indication



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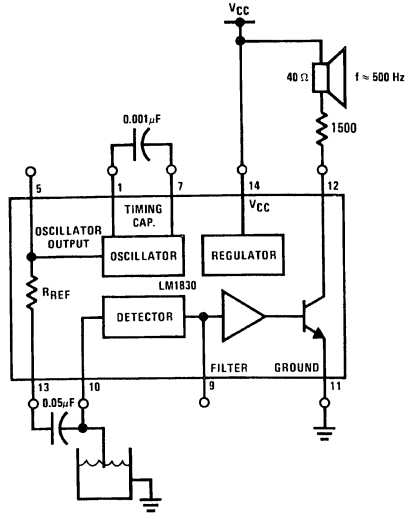
Output is activated when R_P is approximately greater than $\frac{1}{3}$ R_{REF}

FIGURE 4. Direct Coupled Applications

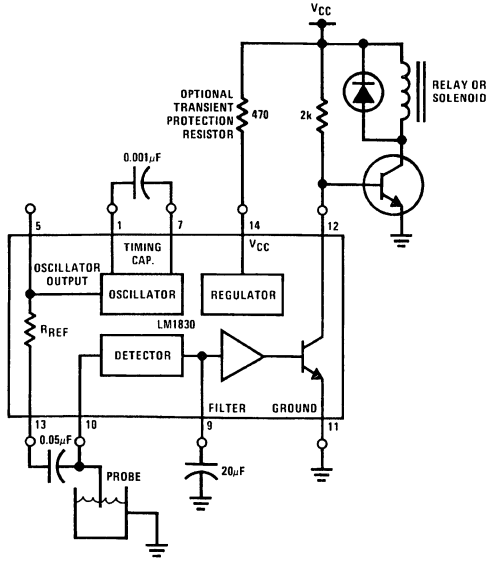
5

Typical Applications V_{CC} = 16V (Continued)

Low Level Warning with Audio Output



High Level Warning Device



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The Output is suitable for driving a sump pump or opening a drain valve, etc.

National Semiconductor Corporation

LM1851 Ground Fault Interrupter

General Description

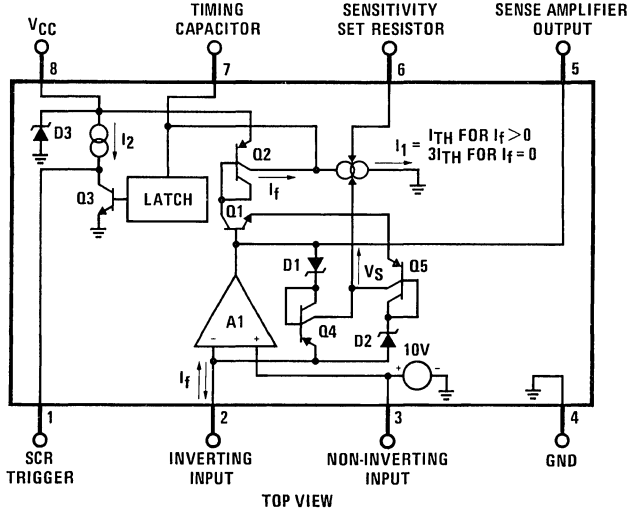
The LM1851 is designed to provide ground fault protection for AC power outlets in consumer and industrial environments. Ground fault currents greater than a presettable threshold value will trigger an external SCR-driven circuit breaker to interrupt the AC line and remove the fault condition. In addition to detection of conventional hot wire to ground faults, the neutral fault condition is also detected.

Full advantage of the U.S. UL943 timing specification is taken to insure maximum immunity to false triggering due to line noise. Special features include circuitry that rapidly resets the timing capacitor in the event that noise pulses introduce unwanted charging currents and a memory circuit that allows firing of even a sluggish breaker on either half-cycle of the line voltage when external full-wave rectification is used.

Features

- Internal power supply shunt regulator
- Externally programmable fault current threshold
- Externally programmable fault current integration time
- Direct interface to SCR
- Operates under line reversal; both load vs line and hot vs neutral
- Detects neutral line faults

Block and Connection Diagram



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Order Number LM1851M or LM1851N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Current	19 mA
Power Dissipation (Note 1)	1250 mW
Operating Temperature Range	−40°C to +70°C
Storage Temperature Range	−55°C to +150°C

Soldering Information

Dual-In-Line Package (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting and Their Effects on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1, With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1, Without Fault		100	240	mV
Output Saturation Resistance	Pin 1, Without Fault		100		Ω
Output External Current Sinking Capability	Pin 1, Without Fault, $V_{pin\ 1}$ Held to 0.3V (Note 4)	2.0	5		mA
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault and Fault Conditions	2.0	2.8	3.6	μA/μA

AC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

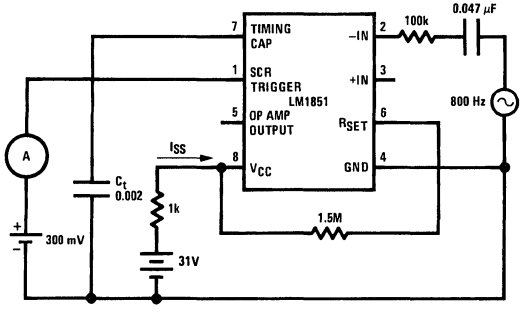
Parameter	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity	*Figure 1* (Note 3)	3	5	7	mA
Normal Fault Trip Time	500Ω Fault, *Figure 2* (Note 2)		18		ms
Normal Fault with Grounded Neutral Fault Trip Time	500Ω Normal Fault, 2Ω Neutral, *Figure 2* (Note 2)		18		ms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient for the DIP and 162°C/W for the SO Package.

Note 2: Average of 10 trials.

Note 3: Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity will be necessary.

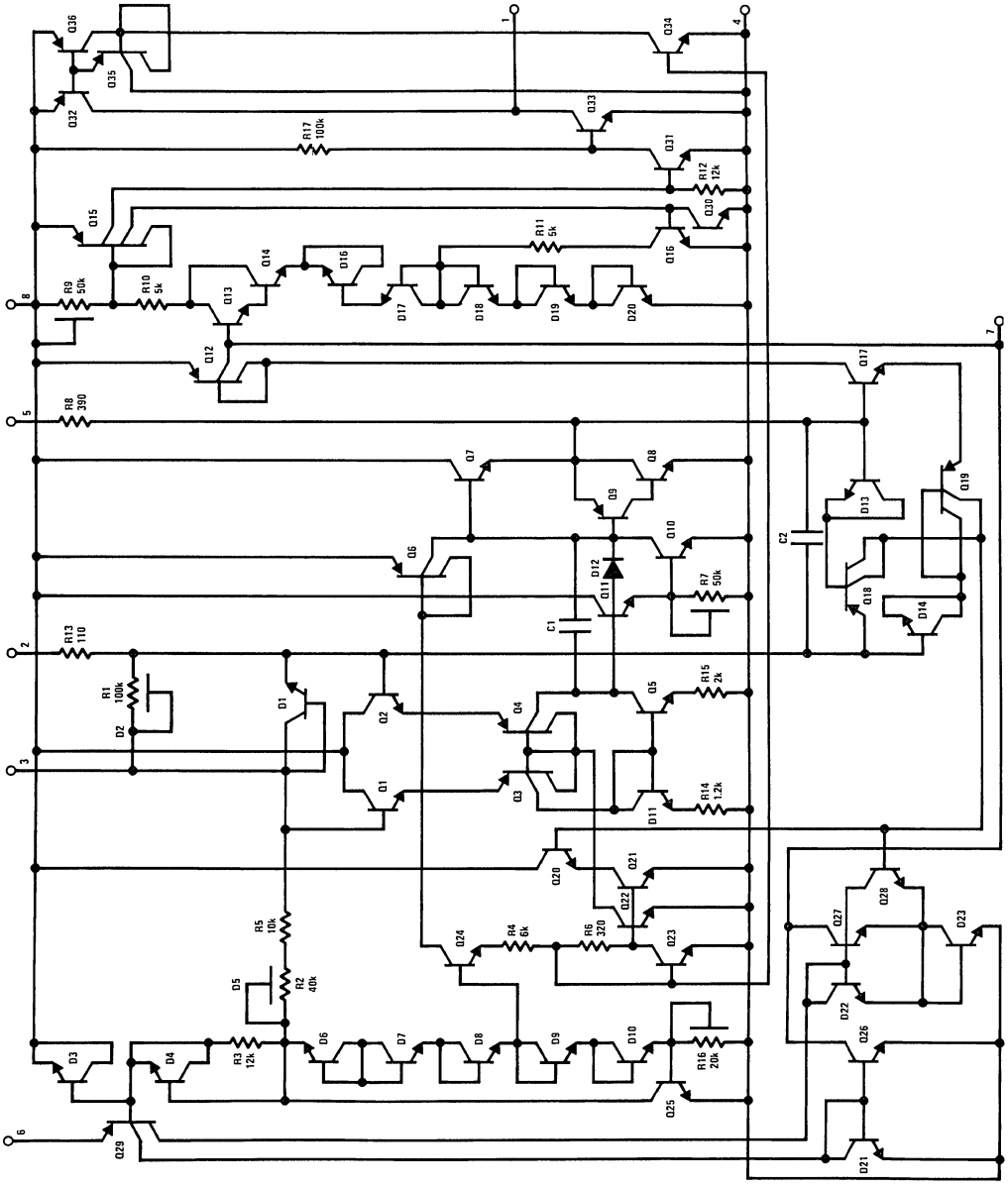
Note 4: This externally applied current is in addition to the internal "output drive current" source.



TL/H/5177–2

FIGURE 1. Normal Fault Sensitivity Test Circuit

Internal Schematic Diagram



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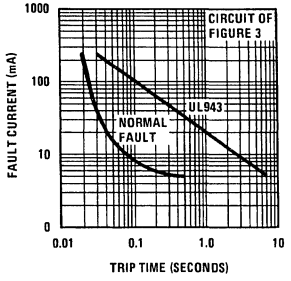
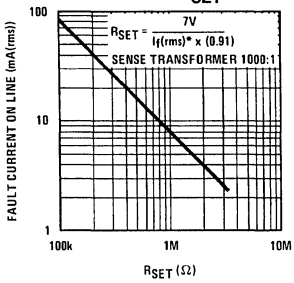
Typical Performance Characteristics

Average Trip Time vs Fault Current

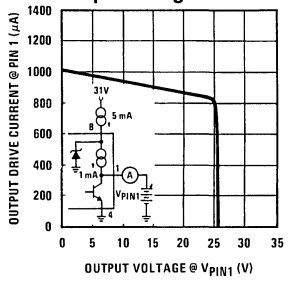


Normal Fault Current Threshold vs R_{SET}

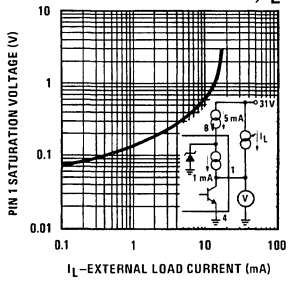


* See Block Diagram

Output Drive Current vs Output Voltage



Pin 1 Saturation Voltage vs External Load Current, I_L



TL/H/5177–4

Circuit Description

(Refer to Block and Connection Diagram)

The LM1851 operates from 26V as set by an internal shunt regulator, D3. In the absence of a fault ($I_f = 0$) the feedback path status signal (V_S) is correspondingly zero. Under these conditions the capacitor discharge current, I_1, sits quiescently at three times its threshold value, I_{TH}, so that noise induced charge on the timing capacitor will be rapidly removed. When a fault current, I_f, is induced in the secondary of the external sense transformer, the operational amplifier, A1, uses feedback to force a virtual ground at the input as it extracts I_f. The presence of I_f during either half-cycle will cause V_S to go high, which in turn changes I_1 from $3I_{TH}$ to I_{TH}. Although I_{TH} discharges the timing capacitor during both half-cycles of the line, I_f only charges the capacitor during the half-cycle in which I_f exits pin 2. Thus during one half-cycle $I_f - I_{TH}$ charges the timing capacitor, while during the other half-cycle I_{TH} discharges it. When the capacitor voltage reaches 17.5V, the latch engages and turns off Q3 permitting I_2 to drive the gate of an SCR.

Application Circuits

A typical ground fault interrupter circuit is shown in *Figure 2*. It is designed to operate on 120 V_{AC} line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the DC power required by the IC. A 1 μF capacitor at pin 8 used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load. At this time no fault current flows and the IC discharge current increases from I_{TH} to $3I_{TH}$ (see Circuit Description and Block Diagram). This quickly resets both the timing capacitor and the output latch. At this time the circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the hot and neutral lines, is stepped down by 1000 and fed into the input pins of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH}=\frac{7V}{R_{SET}}\div 2 \qquad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH}=\frac{I_{f(rms)}}{2}\times 0.91 \qquad (2)$$

where $I_{f(rms)}$ is the rms input fault current to the operational amp and the factor of 2 is due to the fact that I_f charges the timing capacitor only during one half-cycle, while I_{TH} discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have

$$R_{SET}=\frac{7V}{I_{f(rms)}\times 0.91} \qquad (3)$$

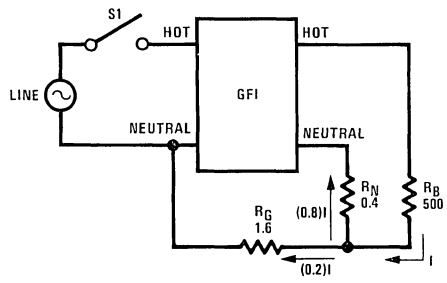
For example, to obtain 5 mA(rms) sensitivity for the circuit in *Figure 2* we have:

$$R_{SET}=\frac{7V}{\frac{5\text{ mA}\times 0.91}{1000}}=1.5\text{M }\Omega \qquad (4)$$

The correct value for R_{SET} can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of R_{SET} depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA–6 mA, provision should be made to adjust R_{SET} on a per-product basis.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_t. Due to the large number of variables involved, proper selection of C_t is best done empirically. The following design example, then should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GF1 start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagramatically below.



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UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C_t based upon charging currents due to normal fault only is as follows:

≤25 ms Specification
−3 ms GFI turn-on time (15k and 1 μF)
−8 ms Potential loss of one half-cycle due to fault current sense of half-cycles only
−4 ms Time required to open a sluggish circuit breaker
≤10 ms Maximum integration time that could be allowed
8 ms Value of integration time that accommodates component tolerances and other variables

$$C_t=\frac{I\times T}{V} \qquad (5)$$

where T = integration time
V = threshold voltage
I = average fault current into C_t

$$I=\underbrace{\left(\frac{120\ V_{AC(rms)}}{R_B}\right)}_{\substack{\text{heavy fault}\\ \text{current generated}\\ \text{(swamps } I_{TH})}}\times\underbrace{\left(\frac{R_N}{R_G+R_N}\right)}_{\substack{\text{portion of}\\ \text{fault current}\\ \text{shunted}\\ \text{around GFI}}}\times\underbrace{\left(\frac{1\text{ turn}}{1000\text{ turns}}\right)}_{\substack{\text{current}\\ \text{division of}\\ \text{input sense}\\ \text{transformer}}}\times\underbrace{\left(\frac{1}{2}\right)}_{\substack{C_t\text{ charging}\\ \text{on half-}\\ \text{cycles only}}}\times\underbrace{(0.91)}_{\substack{\text{rms to}\\ \text{average}\\ \text{conversion}}} \qquad (6)$$

therefore:

$$C_t=\frac{\left[\left(\frac{120}{500}\right)\times\left(\frac{0.4}{1.6+0.4}\right)\times\left(\frac{1}{1000}\right)\times\left(\frac{1}{2}\right)\times(0.91)\right]\times 0.0008}{17.5} \qquad (7)$$

$C_t=$ 0.01 μF

Application Circuits (Continued)

in practice, the actual value of C1 will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C1.

For UL943 requirements, 0.015 μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacitor can be used and better noise immunity obtained. The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

In *Figure 2*, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Typical Application

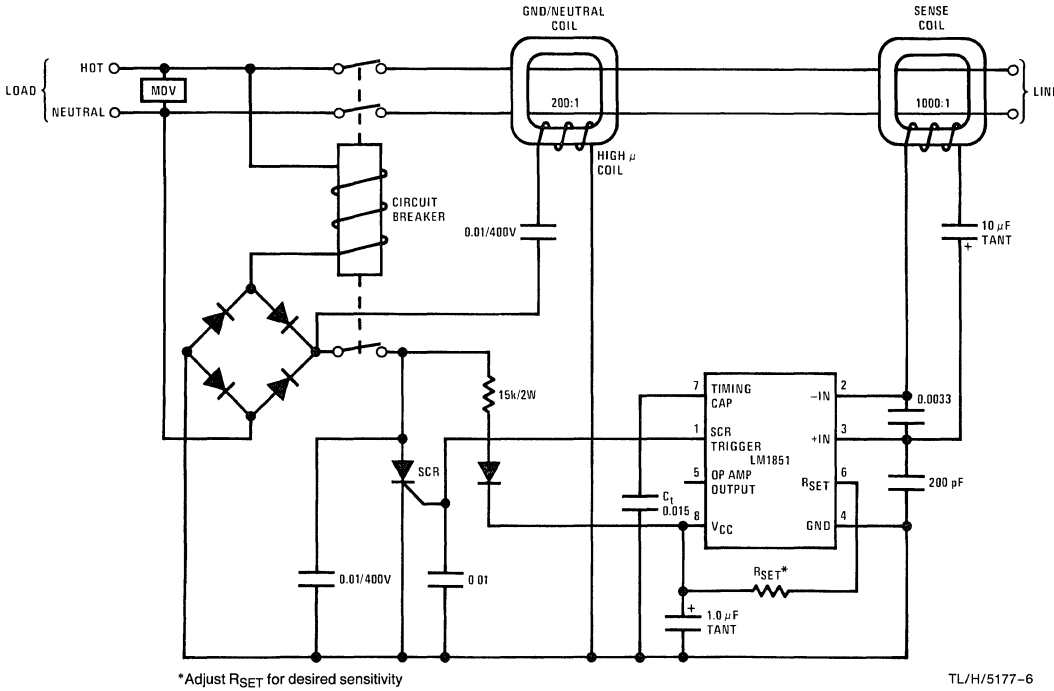
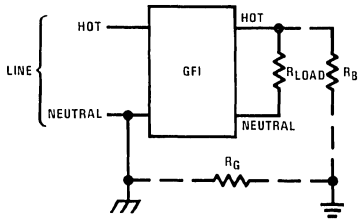


FIGURE 2. 120 Hz Neutral Transformer Approach

Definition of Terms

Normal Fault: An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines.



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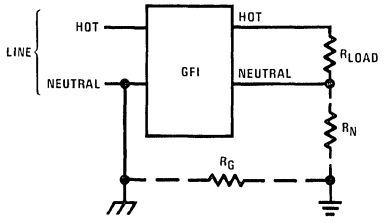
Grounded Neutral Fault: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.



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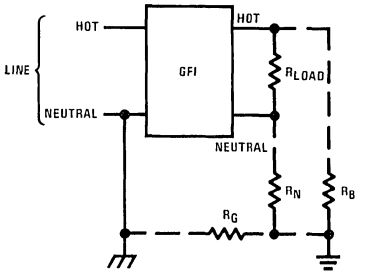
Normal Fault plus Grounded Neutral Fault: The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines.



TL/H/5177–9

National Semiconductor Corporation

BI-LINE™

LM1893/LM2893 Carrier-Current Transceiver†

General Description

Carrier-current systems use the power mains to transfer information between remote locations. This bipolar carrier-current chip performs as a power line interface for half-duplex (bi-directional) communication of serial bit streams of virtually any coding. In transmission, a sinusoidal carrier is FSK modulated and impressed on most any power line via a rugged on-chip driver. In reception, a PLL-based demodulator and impulse noise filter combine to give maximum range. A complete system may consist of the LM1893, a COPS™ controller, and discrete components.

Features

- Noise resistant FSK modulation
- User-selected impulse noise filtering
- Up to 4.8 kBaud data transmission rate
- Strings of 0's or 1's in data allowed
- Sinusoidal line drive for low RFI
- Output power easily boosted 10-fold
- 50 to 300 kHz carrier frequency choice
- TTL and MOS compatible digital levels
- Regulated voltage to power logic
- Drives all conventional power lines

Applications

- Energy management systems
- Home convenience control
- Inter-office communication
- Appliance control
- Fire alarm systems
- Security systems
- Telemetry
- Computer terminal interface

Typical Application

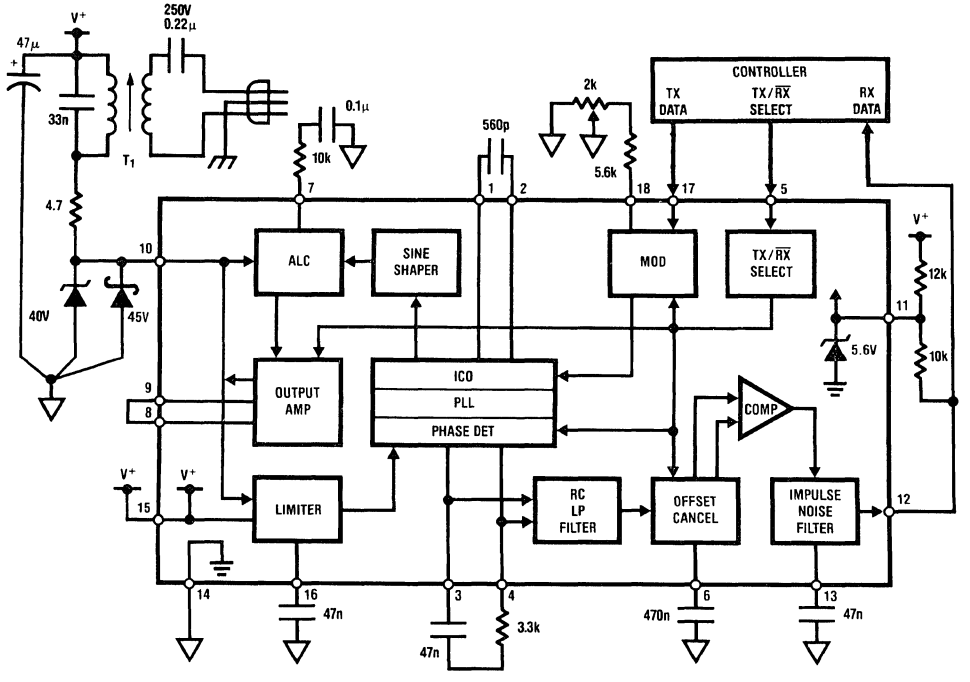


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FIGURE 1. Block diagram of carrier—current chip with a complement of discrete components making a complete $F_O = 125$ kHz, $f_{DATA} = 360$ Baud transceiver. Use caution with this circuit—dangerous line voltage is present.

†Carrier-Current Transceivers are also called Power Line Carrier (PLC) transceivers.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply voltage	30 V
Voltage on pin 12	55 V
Voltage on pin 10 (Note 1)	41 V
Voltage on pins 5 and 17	40 V
5.6 V DC zener current	100 mA
Junction temperature: transmit mode	150°C
receive mode	125°C
Electro-Static Discharge (120 pF, 1500Ω)	1KV
Maximum continuous dissipation, $T_A = 25°C$, plastic DIP N (Note 2): transmit mode	1.66 W
receive mode	1.33 W
Operating ambient temp. range	−40 to 85°C
Storage temperature range	−65 to 150°C
Lead temp., soldering, 7 seconds	260°C

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications are not ensured when operating the device above guaranteed limits but below absolute maximum limits, but there will be no device degradation.*

General Electrical Characteristics

(Note 3). The test conditions are: $V^+ = 18V$ and $F_O = 125$ kHz, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
1	5.6 V Zener voltage, V_Z	Pin 11, $I_Z = 2$ mA	5.6	5.2 5.9		V min. V max.
2	5.6 V Zener resistance, R_Z	Pin 11, $R_Z = (V_Z@10\text{ mA} - V_Z@1\text{ mA})/(10\text{ mA} - 1\text{ mA})$	5			Ω
3	Carrier I/O peak survivable transient voltage, V_{OT}	Pin 10, discharge 1 μF cap. charged to V_{OT} thru <1Ω	80	60		V max.
4	Carrier I/O clamp voltage, V_{OC}	Pin 10, $I_{OC} = 10$ mA, RX mode 2N2222 diode pin 8 to 9	44	41 50		V min. V max.
5	Carrier I/O clamp resistance, R_{10}	Pin 10, $I_{OC} = 10$ mA	20			Ω
6	TX/$\overline{RX}$ low input voltage, V_{IL}	Pin 5	1.8	0.8		V max.
7	TX/$\overline{RX}$ high input voltage, V_{IH}	Pin 5 (Note 9)	2.2	2.8		V min.
8	TX/$\overline{RX}$ low input current, I_{IL}	Pin 5 at 0.8 V	−2	−20 1		μA min. μA max.
9	TX/$\overline{RX}$ high input current, I_{IH}	Pin 5 at 40 V	10^{-4}	−1 10	**0**	μA min. μA max.
10	RX−TX switch-over time, T_{RT}	Time to develop 63% of full current drive thru pin 10	10			μs
11	TX−RX switch-over time, T_{TR}	1 bit time, $T_B = 1/(2F_{DATA})$. Time T_{TR} is user controlled with C_M, see Apps. Info.	2			bit
12	ICO initial accuracy of F_O	TX mode, $R_O = 6.65$ kΩ, $C_O = 560$ pF $F_0 = (F_1 + F_2)/2$	125	113 137		kHz min. kHz max.
13	ICO temperature coefficient of F_O	TX or RX mode, $(F_{OMAX} - F_{OMIN})/(T_{JMAX} - T_{JMIN})$	**−100**			PPM/°C
14	Temperature drift of F_O	TX or RX mode, $-40 \le T_J \le T_{JMAX}$	**±2.0**		**±5.0**	% max.

Transmitter Electrical Characteristics

(Note 3). The test conditions are: $V^+ = 18$ V and $F_O = 125$ kHz unless otherwise noted. The transmit center frequency is F_O, FSK low is F_1, and FSK high is F_2.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
15	Supply voltage, V^+, range	Meets test 17 spec. at $T_J = 25°C$ and: $\lvert(F_1[14V] - F_1[18V])/F_1[18V]\rvert < 0.01$ $\lvert(F_1[24V] - F_1[18V])/F_1[18V]\rvert < 0.01$	**13** **40**	14 24	**15** **23**	V min. V max.
16	Total supply current, I_{QT}	Pin 15. Pin 12 high. I_{QT} is I_Q through pin 15 and the average current I_{ODC} of the Carrier I/O through pin 10	52	79		mA max.
17	Carrier I/O output current, I_O	100Ω load on pin 10	70	45		mApp min.
18	Carrier I/O lower swing limit, V_{ALC}	Pin 10. Set internally be ALC. 2N2222 diode pin 8 to 9	4.7	4.0 5.7		V min. V max.
19	THD of I_O (Note 6)	Q of 10 tank driving 10Ω line 100Ω load, no tank	0.6 5.5		**5.0** 9	% max. % max.
20	FSK deviation, $F_2 - F_1$	$(F_2 - F_1)/([F_2 + F_1]/2)$	4.4	3.7 5.2		% min. % max.
21	Data In. low input voltage, V_{IL}	Pin 17	1.7	0.8		V max.
22	Data In. high input voltage, V_{IH}	Pin 17 (Note 9)	2.1	2.8		V min.
23	Data In. low input current, I_{IL}	Pin 17 at 0.8 V	−1	−10 1		μA min. μA max.
24	Data In. high input current, I_{IH}	Pin 17 at 40 V	10^{-4}	−1 10	**0**	μA min. μA max.

Receiver Electrical Characteristics (Note 3). The test conditions are: $V^+ = 18$ V, $F_O = 125$ kHz, ±2.2% deviation FSK, $F_{DATA} = 2.4$ kHz, $V_{IN} = 100$ mVpp, in the receive mode, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
25	Supply voltage, V^+, range	Functional receiver (Note 7)	**12** **37**	13 30	**13.5** **28**	V min. V max.
26	Supply current, I_{QT}	I_{QT} is pin 15 (V^+) plus pin 10 (Carrier I/O) current. 2.4 kΩ Pin 13 to GND.	11	5 14		mA min. mA max.
27	Carrier I/O input resistance, R_{10}	Pin 10	19.5	14 30		kΩ min. kΩ max.
28	Max. data rate, F_{MD}	Functional receiver (Note 7), C_F = 100 pF, R_F = 0Ω, no tank, 2.4 kHz = 4.8 kBaud	10	4.8	**2.4**	kBaud
29	PLL capture range, F_C	C_F = 100 pF, R_F = 0 Ω	±40	±15	±**10**	% min.
30	PLL lock range, F_L	C_F = 100 pF, R_F = 0 Ω	±45	±15		% min.
31	Receiver input sensitivity, S_{IN}	For a functional receiver (Note 8) Referred to chip side (pin 10) of the line-coupling XFMR: F_O = 50 kHz F_O = 300 kHz Referred to line side of XFMR: (assuming a 7.07:1 XFMR) F_O = 50 kHz F_O = 300 kHz	 1.8 2.0 1.4 0.26 0.29 0.20	10	**12**	 mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS}
32	Tolerable input dc voltage offset range, V_{INDC}	Pin 10 lower than pin 15 by V_{INDC}	2	0.1		V max.
33	Data Out. breakdown voltage	Pin 12, leakage I ≤ 20 μA	70	55		V min.
34	Data Out. low output, V_{OL}	Pin 12, sat. voltage at I_{OL} = 2 mA	0.15	0.4		V max.
35	Impulse noise filter current, I_I	Pin 13 charge and discharge current	±55	±45 ±85		μA min. μA max.
36	Offset hold cap. bias voltage, V_{CM}	Pin 6	2.0	1.3 3.5		V min. V max.
37	Offset hold capacitor max. drive current, I_{MCM}	Pin 6. V(pin 3) − V(pin 4) = ±250 mV	±55	±25 ±80		μA min. μA max.
38	Offset hold bias current, I_{OHB}	Pin 6, TX mode. Bias pin 6 as it self-biased during test 31.	−0.5	−20	−**40** **40**	nA min. nA max.
39	Phase comparator current, I_{PC}	Bias pins 3 and 4 at 8.5 V I_{PC} = I(pin 3) + I(pin 4), TX mode	100	50 200		μA min. μA max.
40	Phase detector output resistance, R_{PD}	Pins 3 and 4. R_{PD} = (V@100μA − V@50μA)/(50μA)	10	6 18		kΩ min. kΩ max.
41	Phase detector demodulated output voltage, V_{PD}	Pin 3 to 4, measured after filtering out the $2F_O$ component	100	60 180		mVpp min. mVpp max.
42	Fast offset cancel voltage "window" -to-V_{PD} ratio, V_W/V_{PD}	$V_{PIN3} - V_{PIN4} = \pm V_{WINDOW}$ + DC offset Drive for ±1 μA pin 6 current	0.95	0.70 1.20		V/V min. V/V max.
43	Power supply rejection, PSRR	C_L = 0.1 μF. PSRR = CMRR. 120 Hz	80			dB min.

Note 1: More accurately, the maximum voltage allowed on pin 10 is V_{OC}, and V_{OC} ranges from 41 to 50V. Also, transients may reach above 60V; see the transient peak voltage characteristic curve.

Note 2: The maximum power dissipation rating should be derated for device operation above 25°C to insure that the junction temperature remains below the maximum rating. Use a θ_{JA} of 75°C/W for the N package using a socket in still air (which is the worst case). Consult the Application Information section for more detail.

Note 3: The **boldface** values apply over the full junction temperature range for the specified supply voltage range. All other numbers apply at $T_A = T_J = 25°C$. Pin numbers refer to LM1893. LM2893 tested by shorting Carrier In to Carrier Out and testing it as an LM1893.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed (but not 100% production tested) over the temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Total harmonic distortion is measured using THD = [I_{RMS} (all components at or above $2F_O$)]/[I_{RMS} (fundamental)].

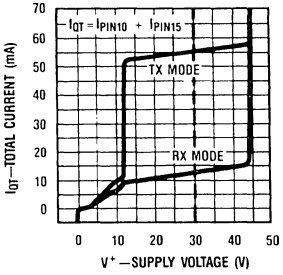
Note 7: Receiver function is defined as the error-free passage of 1 cycle of 50% duty-cycle 2.4 kHz square-wave data (2 sequential 208 μS bits), with the first bit being a "1." All of the data transitions (edges) must fall within ±10% (±20.8 μs) of their noise-free positions. RX time delay is minimized by using no impulse noise filter cap. C_I for this test.

Note 8: During the sensitivity check, note 7 requirements are followed with these exceptions: (1) data rate $F_{DATA} = 1.2$ kHz, (2) all of the data transitions must fall within ±20% (±41.6 μs) of their noise-free positions, and (3), a time-domain filter capacitor (C_I) is used. The time delay of C_I is ½ bit, or 208 μs. (C_I is approximately 6200 pF).

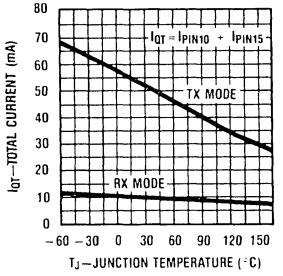
Note 9: For TTL compatibility use a pull-up resistor to increase min. V_{OH} to above 2.8 V.

Typical Performance Characteristics ($V^+ = 18V$, $F_O = 125$ kHz, circuit of *Figure 1*, pin numbers for LM1893)

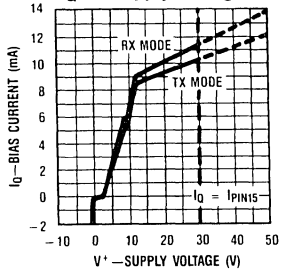
Total Current Consumption, I_{QT}, vs Supply Voltage



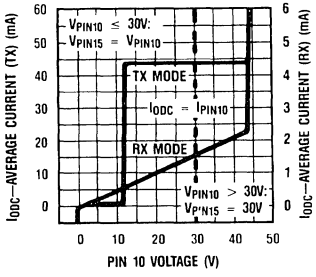
Total Current Consumption, I_{QT}, vs Junction Temperature



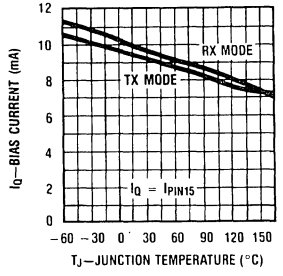
Chip Bias Current, i_Q, vs Supply Voltage



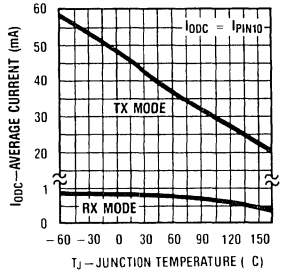
Chip Bias Current, I_Q, vs Junction Tempurature



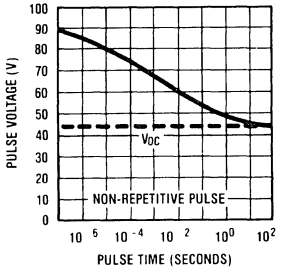
Output Stage DC Current, I_{ODC}, vs Output Voltage



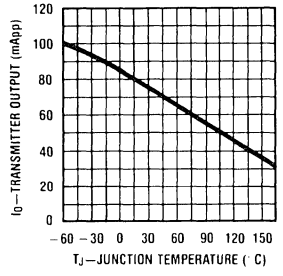
Output Stage DC Current, I_{ODC}, vs Junction Temperature



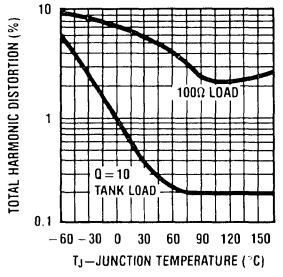
Transient Voltage Survival vs Pulse Time



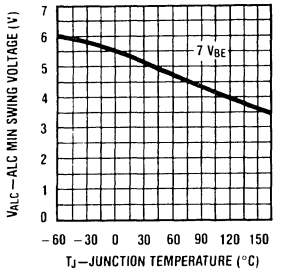
Transmitter AC Output Current vs Junction Temperature



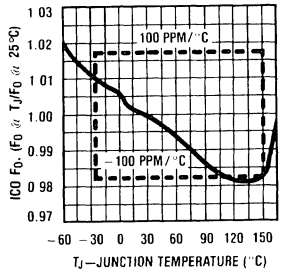
Transmitter Sinusoid THD vs Junction Temperature



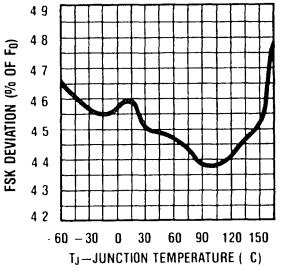
ALC Voltage vs Junction Temperature



ICO Frequency vs Junction Temperature



Transmitter FSK Deviation vs Junction Temperature



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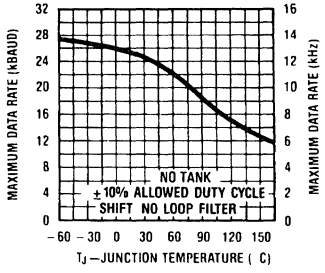
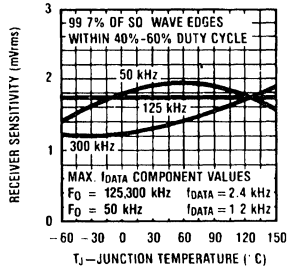
Typical Performance Characteristics (Continued)

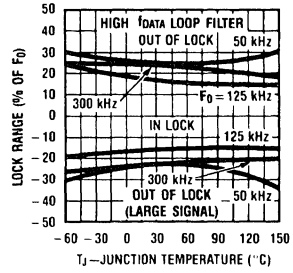
Maximum Data Rate vs Junction Temperature



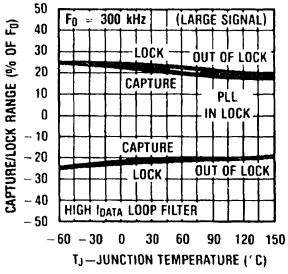
Receiver Sensitivity vs Junction Temperature



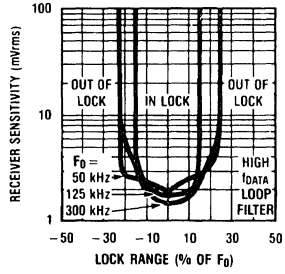
PLL Lock Range vs Junction Temperature and F_O



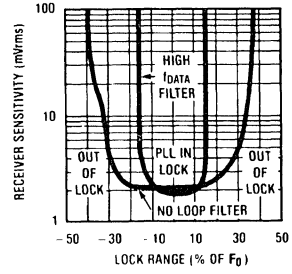
PLL Capture & Lock Range vs Junction Temperature



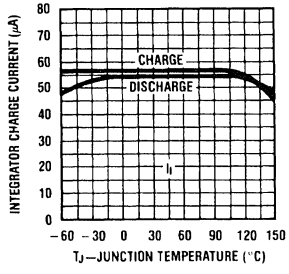
Receiver Sensitivity vs PLL Lock Range and F_O



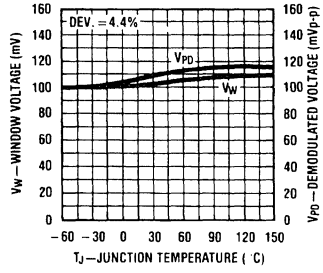
Receiver Sensitivity vs PLL Lock Range and Loop Filter



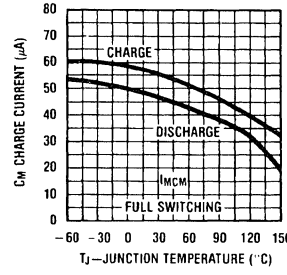
Impulse Noise Filter Current vs Junction Temperature



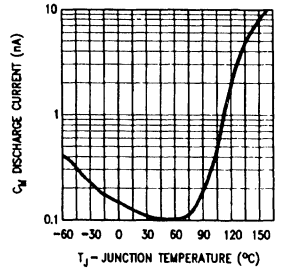
Phase Detector Output Voltage vs Junction Temperature



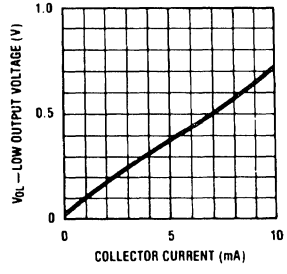
Offset Hold Cap. Charge Currents vs Junction Temperature



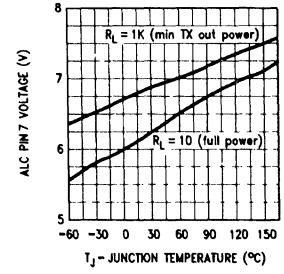
Offset Hold Cap. Bias Current vs Junction Temperature



Data Out. Low Voltage vs Pull Down Current



Pin 7 Bias Voltage vs Junction Temperature



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Application Information*

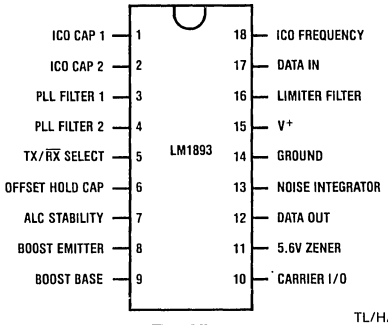
THE DATA PATH

The BI-LINE™ chip serves as a power line interface in the carrier-current transceiver (CCT) system of *Figure 3*. *Figure 4* shows the interface circuit now discussed. The controller may select either the transmit (TX) or receive (RX) mode. Serial data from the controller is used to generate a FSK-modulated 50 to 300 kHz carrier on the line in the TX mode. In the RX mode line signal passes through the coupling transformer into the PLL-based receiver. The recreated serial bit stream drives the controller.

With the IC in the TX mode (pin 5 a logic high), baseband data to 5 kHz drive the modulator's Data In pin to generate a switched 0.978I/1.022I control current to drive the low TC, triangle-wave, current-controlled oscillator to ±2.2% deviation. The tri-wave passes through a differential attenuator and sine shaper which deliver a current sinusoid through an automatic level control (ALC) circuit to the gain of 200 current output amplifier. Drive current from the Carrier I/O develops a voltage swing on T_1's (*Figure 4*) resonant tank proportional to line impedance, then passes through the step-down transformer and coupling capacitor C_C onto the line. Progressively smaller line impedances cause reduced signal swing, but never clipping-thus avoiding potential radio frequency interference. When large line impedances threaten to allow excessive output swing on pin 10, the ALC shunts current away from the output amplifier, holding the voltage swing constant and within the amp's compliance limit. The amplifier is stable with a load of any magnitude or phase angle.

In the RX mode (pin 5 a logic low), the TX sections on the chip are disabled. Carrier signal, broad-band noise, transient spikes, and power line component impinge of the receiver's input highpass filter, made up of C_C and T_1, and the tank bandpass filter. In-band carrier signal, band-limited noise, heavily attenuated line frequency component, and attenuated transient energy pass through to produce voltage swing on the tank, swinging about the positive supply to drive the Carrier I/O receiver input. The balanced Norton-input limiter amplifier removes DC offsets, attenuates line frequency, performs as a bandpass filter, and limits the signal to drive the PLL phase detector differentially. The differential demodulated output signal from the phase detector, containing AC and DC data signal, noise, system DC offsets, and a large twice-the-carrier-frequency component, passes through a 3-stage RC lowpass filter to drive the offset cancel circuit differentially. The offset cancelling circuit works by insuring that the (fixed) ±50 mV signal delivered to the data squaring ("slicing") comparator is centered around the 0 mV comparator switch point. Whenever the comparator signal plus DC offset and noise moves outside the carefully matched ±50 mV voltage "window" of the offset cancel circuit, it adjusts its DC correction voltage in series with the differential signal to force the signal back into the window. While the signal is within the ±50 mV window, the DC offset is stored on capacitor C_M. By grace of the highly non-linear offset hold capacitor charging during offset cancelling, the DC cancellation is done much more quickly than with an AC coupling capacitor normally used in place of the offset cancel circuit. Since impulse noise spikes normally ring the signal symmetrically around 0 V, the fully bilateral offset cancel topology affords excellent noise rejection. The switched current output of the comparator drives the impulse noise filter integrator capacitor that rejects all data pulses of less than the integrator charge time. Noise appears as duty-cycle jitter at the open collector serial data output.

Dual-In-Line Package



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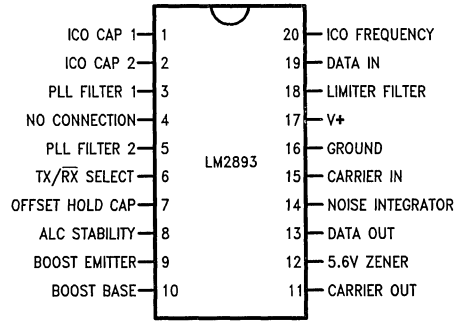
Top View

Dual-In-Line Package



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Top View

FIGURE 2. Connection Diagrams

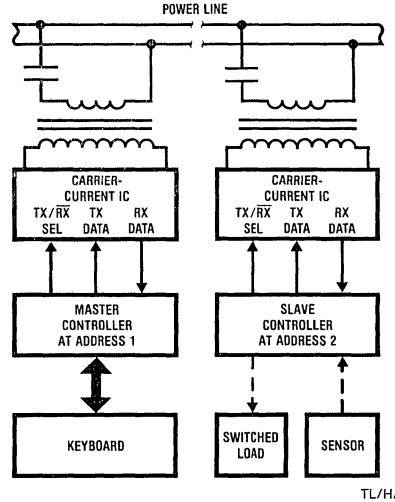

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FIGURE 3. The block diagram of a carrier-current system using the Bi-Line chip to interface digital controllers via the power line

*Unless otherwise noted, all pin references refer to LM1893, but hold true for equivalent LM2893 pin.

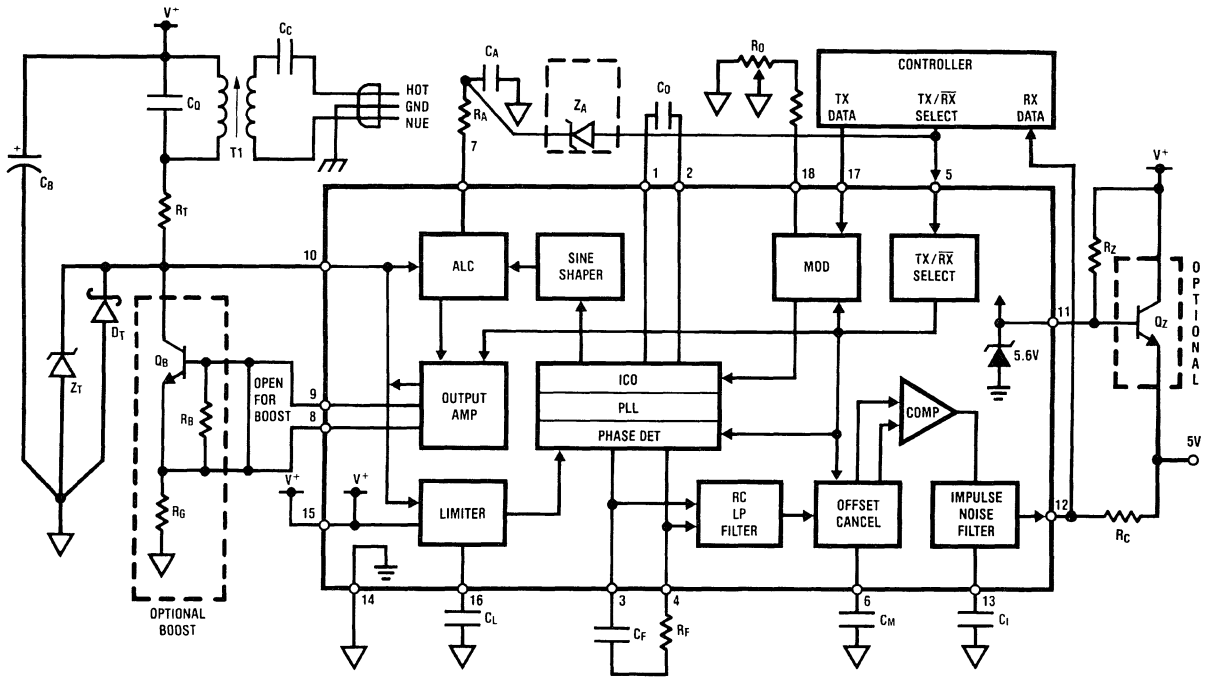

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FIGURE 4. Block diagram of a CCT system with the boost and 5V supply options shown in dashed boxes

Application Information (Continued)

#	Recommended Value	Purpose	Effect of making the component value:		Notes
			Smaller	Larger	
C_O R_O	560 pF 6.2 kΩ	Together, C_O and R_O set ICO F_O.	Increases F_O Increases F_O <5.6 k not recommended.	Decreases F_O Decreases F_O >7.6 k not recommended.	±5% NPO ceramic. Use low TC 2 k pot and 5.6 k fixed R. Poor F_O TC with <5.6 k R_O.
C_F R_F	0.047 μF 3.3 kΩ	PLL loop filter pole PLL loop filter zero	Less noise immune, higher f_{DATA}, more PLL stability. PLL less stable, allows less C_F. Less ringing.	More noise immune, lower f_{DATA}, less PLL stability. PLL more stable, allows more C_F. More ringing.	Depending on R_F value and F_O, PLL unstable with large C_F. See Apps. Info. C_F and R_F values not critical.
C_C	0.22 μF	Couples F_O to line, C_C and T_1 low-pass attenuates 60 Hz.	Low TX line amplitude. Less 60 Hz T_1 current. Less stored charge.	Drives lower line Z. More 60 Hz T_1 current. More stored charge.	≥250 V non-polar. Use $2C_C$ on hot and neutral for max. line isolation, safety.
C_Q T_1	0.033 μF Use recommended XFMR	Tank matches line Z, bandpass filters, isolates from line, and attenuates transients.	Tank F_O up or increase L of T_1 for constant F_O. Smaller L: higher F_O or increase C_C; decreased F_O line pull.	Tank F_O down or decrease L of T_1 for constant F_O. Larger L: lower F_O or decrease C_C; increased F_O line pull.	100 V nonpolar, low TC, ±10% High large-signal Q needed. Optimize for low F_O line pull with control of F_O TC and Q.
C_A R_A	0.1 μF 10 kΩ	ALC pole ALC zero	Noise spikes turn ALC off. Less stable ALC.	Slower ALC response. More stable ALC.	R_A optional. ALC stable for C_A≥100 pF.
C_L	0.047 μF	Limiter 50 kHz pole, 60 Hz rejection.	Higher pole F, more 60 Hz reject. F_O attenuation?	Lower pole F, less 60 Hz reject, more noise BW.	Any reasonably low TC cap. 300 pF guarantees stability.
C_M	0.47 μF	Holds RX path V_{OS}	Less noise immune, shorter V_{OS} hold, faster V_{OS} acquisition, shorter preamble.	More noise immune, longer V_{OS} hold, slower V_{OS} acquisition, longer preamble.	Low leakage ±20% cap. Scale with f_{DATA}.
C_I	0.047 μF	Rejects short pulses like impulse noise.	Less impulse reject, less delay, more pulse jitter.	More impulse reject, more delay, less pulse jitter.	C_I charge time ½ bit nom. Must be <1 bit worst-case.
R_C	10 kΩ	Open-col. pull-up	Less available sink I.	Less available source I.	R_C≥1.5 kΩ on 5.6 V
R_Z	12 kΩ	5.6 V Zener bias	Larger shunt current, more chip dissipation.	Smaller shunt current, less V^+ current draw.	1<I_Z<30 mA recommended. (Chip power-up needs 5.6 V)
Z_T R_T D_T	≥44 V BV <60 V peak 4.7 Ω ≥44V BV	Transient clamp Transient I limit Over-drive Clamp	Z_T failure, higher series R-excess peak V, Zener and chip damage, less ruggedness. Damage Z_T, pull up V^+. Failure on Transient	Z_T costly, lower series R gives enhanced transient clamp, more ruggedness. Excessive TX attenuation. Costly	Recommend Zener rated for ≥500 W for 1 ms. Carbon comp. recommended. IRF 11DQ05 or 1N5819
R_B Q_B R_G	180 Ω Power NPN 1.1 Ω	Base bleed Boost gain device Current setting R	Faster, lower THD I_O. Excessive T_J and V_{SAT}. More I_O, need higher h_{fe}.	Inadequate turn-off speed. More rugged, but costly. Less I_O, lower min. h_{fe}.	Boost optional. Q_B F(−3 dB) of >200 MHz. R_B > 24 Ohm. $I_O = 70[(10 + R_G)/R_G]$ mApp.
C_B	≥47 μF	Supply bypass	Transients destroy chip.	Less supply spike.	V^+ never over abs. max.
Z_A	5.1V	Stop ALC charge in RX mode	Excess ALC current flow	ALC RX charging not inhibited over T_J	Z_A optional - 5.1V ±20% low leakage type

FIGURE 5. A quick explanation of the external component function using the circuit of *Figure 4*. Values given are for V^+ = 18 V, F_O = 125 kHz, f_{DATA} = 360 Baud (180 Hz), using a 115 V 60 Hz power line

Component Selection

Assuming the circuit of *Figure 4* is used with something other than the nominal 125 kHz carrier frequency, 180 Hz data rate, 18V supply voltage, etcetera, the component values listed in *Figure 5* will need changing. This section will help direct the CCT designer in finding the required component values with emphasis placed on look-up tables and charts. It is assumed that the designer has selected values for carrier center frequency, F_O; data rate, f_{DATA}; supply voltage, V^+; power line voltage, V_L; and power line frequency, F_L. If one or more of those parameters is not defined, one may read the data sheet and make an educated guess.

Maxims to keep in mind, based on CCT electrical performance considerations only, are: 1) the higher the F_O the better, 2) the lower the maximum data rate the better, and 3) the more time and frequency filtering the better.

Use *Figure 5* as a quick reference to the external component function.

THE TRANSMITTER

C_O

Central to chip operation is the low TC of F_O emitter-coupled oscillator. With proper C_O, the F_O of the $2V_{BE}$ amplitude triangle-wave oscillator output may vary from near DC to above 300 kHz. While C_O may have any value, C_O should

Component Selection (Continued)

be made above 10 pF so that parasitic capacitance is not dominant. Excessive or unbalanced common-mode-to-ground capacitance should be avoided. A low temperature coefficient (TC) of capacitance (<100 PPM/°C), such as a monolithic NPO ceramic multilayer type, preserves low TC of F_O. *Figure 6* finds a C_O value given F_O.

R_O

Resistor R_O is used by the IC to generate a V_{BE}/R related current that is multiplied by 2 to produce the 200 μA ICO control current that sets F_O. The control current TC "bucks" the V_{BE} related tri-wave amplitude across C_O to effect a low TC of F_O. Vary R_O to trim F_O, within limits. Raising F_O more than 20% above its untrimmed value by means of decreasing R_O more than 20% is not recommended. Low R_O, and so high control current, risks ICO saturation and poor TC under worst-case conditions. Raising R_O reduces the demodulated signal amplitude from the phase detector; raising R_O by more than a factor of 2 (1 octave) is not recommended.

Since lower TC pots are relatively costly, it is recommended that R_O be made up of a 5.6 k fixed (<100 PPM/°C) resistor with a 2 kΩ (<250 PPM/°C) series pot.

C_A and R_A

Components C_A and R_A control the dynamic characteristics of the transmitter output envelope. Their values are not critical. Use the values given in *Figure 5*. C_A and R_A are functions of loaded T_1 tank Q, R_O, f_{DATA}, and line impulse noise. Any changes made in C_A and R_A should be made based on empirical measurements of a CCT on the line. Roughly, C_A acts as an ALC pole and R_A an ALC zero.

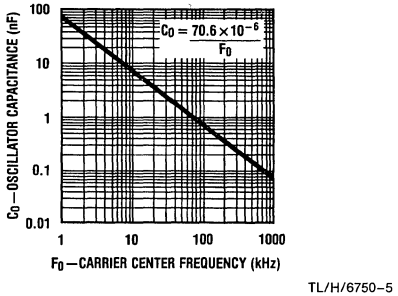
T_1

At this point, the CCT system designer may choose to use one of the recommended transformers or to design custom T_1. Consult "The Coupling Transformer" section to help with the design of T_1 if a new or boost-capable transformer is needed. The recommended 125 kHz transformer functions with an I_O of up to 600 mApp.

It is recommended that CCT systems use the recommended transformers, described in *Figure 7*, for T_1. The 3 transformers are optimized for use in the ranges of 50–100 kHz, 100–200 kHz, and 200–400 kHz with unloaded Q's (Q_U) of about 35, and loaded Q's (Q_L) of about 12. Three secondary taps are supplied with nominal 7.07, 10, and 14.1 turns ratios (N) to drive industrial and residential power line impedances of 3.5, 7, and 14Ω respectively. All are inexpensive, all have the same pin-outs for easy exchange in a PC board, and all are small - on the order of 10 mm diameter at the base.

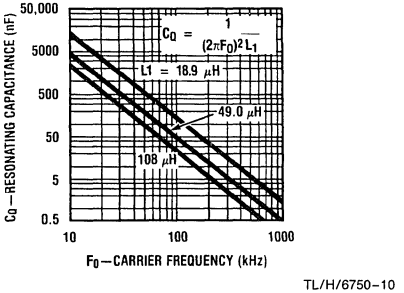
C_Q

Tank resonant frequency F_Q must be correct to allow passage of transmitter signal to the line. Use *Figure 8* to find C_Q's value. Trimming F_Q to equal F_O is done with T_1's trimming slug. The inductance of T_1 has a TC of +150 PPM/°C which may be cancelled by using a −150 PPM/°C cap such as polystyrene. Since circulating current in the tank is ¼ A_{RMS}, C_Q should have a low series resistance (a 1 Ω series resistance is too much). Polypropelene caps are excellent, "orange drop" mylars are adequate, while many other mylars are inadequate. A 100V rating is needed for transient protection.



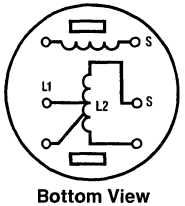
TL/H/6750–5

FIGURE 6. Find C_O's value knowing F_O



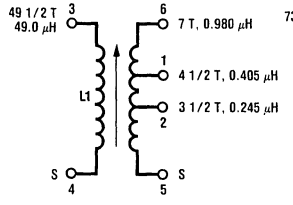
TL/H/6750–10

FIGURE 8. Find C_O's value given F_O



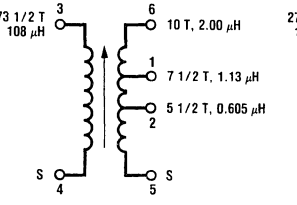
Bottom View

TL/H/6750–6



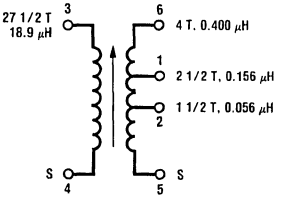
TL/H/6750–7

125 kHz
C^2 10UL-001
Toko 707VX-A042YUK



TL/H/6750–8

50 kHz
C^2 10UL-002
Toko 707VX-A043YUK



TL/H/6750–9

300 kHz
C^2 10UL-003
Toko 161XN-A207YUK

FIGURE 7. The recommended T_1 transformers, available through:
1) C^2 Electronics, 4010 Moorpark, Suite 105, San Jose, CA., 95117 (408) 248-9899
2) Toko America, 5520 W. Touhy Ave., Skokie, IL, 60077, (312) 677-3640.

Component Selection (Continued)

C_C

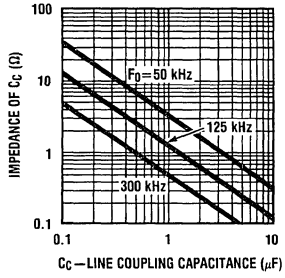
Capacitor C_C's primary function is to block the power line voltage from T_1's line-side winding. Also, C_C and T_1's line-side winding comprise a LC highpass filter. The self-inductance of T_1 is far too low to support a direct line connection. C_C must have a low enough impedance at F_O to allow T_1 to drive transmitted energy onto the line. To drive a 14Ω power line, the impedance of C_C should be below 14Ω.

Use *Figure 9* to find the reactive impedance of C_C to check that it is less than the line impedance. Then check *Figure 10* to see that the power line current is small enough to keep T_1 well out of saturation; the recommended transformers can withstand a 10 Amp-turn magnetizing force (1 Amp through the worst-case 10 turn line-side winding).

Caution is required when choosing C_C to avoid series resonance of the series combination of C_C, the transformer inductance, and the reflected tank impedance. The low resistance of the network under series resonance will load the line, possibly decreasing range. For your particular line coupling circuit, measure for series resonance using some expected line impedance load.

R_B

This base-bleed resistor turns Q_B off quickly - important since the amplifier output swing is about 200V/μs. An R_B below about 24Ω will conduct excessive current and overload the chip amplifier and is not recommended.



TL/H/6750–11

FIGURE 9. C_C's impedance should be, as a rule-of-thumb, smaller than the lowest expected line impedance

R_G

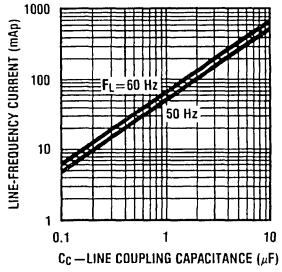
This resistor, in parallel with the internal 10Ω resistor, fixes the current gain of the output amplifier, and so the output current amplitude. *Figure 11* gives output current and minimum AC current gain h_{fe} for Q_B when R_G is used to boost output current.

Q_B

The boost gain transistor Q_B must be fast. Double-diffused devices with 50 MHz F_T's work, slower transistors (epi-base types) do not preserve a sinusoidal waveform when F_O is high or will cause the output amp. to oscillate. Q_B must have a certain minimum h_{fe} for given boost levels, as shown in *Figure 11*. *Figure 12* shows the power Q_B must dissipate continuously operating with a shorted output. BV_{CER} ($R = R_B$) must be 60V or greater and Q_B must have adequate SOA for transient survival.

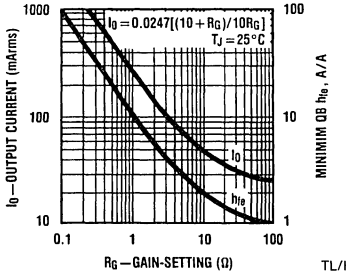
Z_T

Unfortunately, potentially damaging transient energy passes through transformer T_1 onto the Carrier I/O pin (instantaneous power of greater than 1 kW has been measured using the recommended transformers). For self protection, the Carrier I/O has an internal 44V voltage clamp with a 20Ω series resistance. A parallel low impedance 44V external transient suppression diode will then conduct the lion's share of any current when transients force the Carrier I/O to a high voltage.



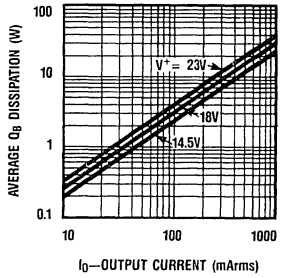
TL/H/6750–12

FIGURE 10. The AC line-induced current passed by C_C



TL/H/6750–13

FIGURE 11. Output amplifier current and required min. Q_B h_{fe} versus gain-setting resistor R_G



TL/H/6750–14

FIGURE 12. Boost transistor power dissipation versus amplifier output current

Z_T must be used unless some precaution is taken to protect the Carrier I/O pin from line transients or transients caused when stored line energy in C_C is discharged by the random phase of power line connection and disconnection. Worst case, C_C may discharge a full peak-to-peak line voltage into the tuned circuit. Another way to reduce the need for Z_T is by placing another magnetic circuit in the signal path that relies on a high, but easily saturated, permeability to couple a primary and secondary winding - a toroidal transformer for example. Toroids cost more than Z_T.

Use an avalanche diode designed specifically for transient suppression — they have orders of magnitude higher pulse

Component Selection (Continued)

power capability than standard avalanche diodes rated for equal DC dissipation. Metal oxide varistors have not proven useful because of their inferior clamping coefficient and are not recommended. Specifications for an example minimum diode are given in *Figure 13*.

Breakdown Voltage	44–49V @ 1 mA
Maximum Leakage	1 μA @ 40V
Capacitance	300 pF @ BV
Maximum Clamp Voltage	64.5V @ 7.8A
Peak Non-Repetitive Pulse Power (REA Standard Exponential Pulse)	10 kW for 1 μs
Surge Current	70A for 1/120s

FIGURE 13. Key specifications for a recommended transient suppressor Z_T available from General Semiconductor, 2001 West Tenth Place, Tempe, AZ 85281, 602–968-3101, part no. SA40A

R_T

R_T acts as a voltage divider with Z_T, absorbing transient energy that attempts to pull the Carrier Input pin above 44V. Make the resistor a carbon composition 1/4W. When experiments discharging C_C charged to the peak-to-peak 620V AC thru a 1Ω power line were carried out, film resistors blew open-circuit.

D_T

This Schottky diode is placed in parallel with the CCT chip's substrate diode to pass the majority of the current drawn from ground when the Carrier Input or Carrier Output is pulled below ground by a larger-than-twice-the supply-swing on the tank. Note that Z_T is in parallel with the substrate diode, but is ineffective due to its high forward voltage drop and high diffusion capacitance caused by its low forward speed. Tests proved that a 1N5818 kept a receive-path functional with a 20X boost transmitter with a 7:1 transformer attempted to swing the receiver's Carrier I/O to ±100V (300 mA peak ground current in the receiver). Without D_T, the receiver momentarily stops functioning at a 100 times lower ground current.

This diode is not needed if the Carrier I/O never swings below ground. If your CCT systems all run on the same regulated voltage with all matched transformers and turns ratios, it is not needed. Otherwise, it is.

THE RECEIVER

The receiver and transmitter share components C_C, T_1, C_Q, R_T, Z_T, C_O, R_O, and peripheral supply and bias components that are not in need of change for RX mode operation. Values for the balance of the components are now found.

Line-Frequency Rejection

To use the ultimate sensitivity of the device, fully 110 dB of 115 V, 60 Hz attenuation is required between the line and the limiter amplifier output. Using the circuit topology of *Figure 4*, the combined attenuation of the C_C/T_1 highpass, the tuned transformer, and the bandpass filter attenuation of the limiter amplifier give far more line rejection than the above-stated minimum. However, if some other CCT line coupling circuit is used, line rejection will become important to the system designer.

Receiver input power supply rejection (PSRR) and common-mode rejection (CMRR) are one-in-the-same using the supply-referenced signal input of *Figure 4*. Ripple swings both differential inputs of the Norton amp. equally, while the single-ended input signal swings only the positive input. Overall PSRR consists of the input CMRR (set by the input stage component matching) and the ripple-frequency attenuation of the input amplifier bandpass response that passes carrier frequency but stops low frequencies. A typical 1% resistor and 1 mV n-p-n mirror offsets give 26 dB of attenuation, the bandpass gives 54 dB 120 Hz attenuation, for an overall 80 dB PSRR to allow tens of volts of ripple before impacting ultimate sensitivity.

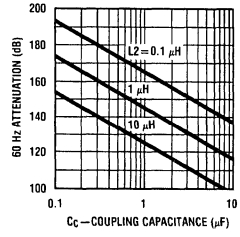
C_C

A value was chosen earlier. Knowing T_1's secondary inductance allows a check of LC line attenuation using *Figure 14*.

C_L

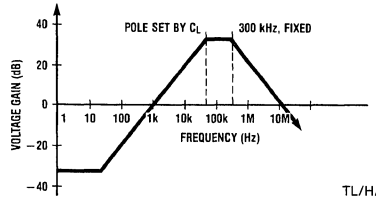
The Norton input limiter amplifier has a bandpass filter for enhanced receiver selectivity, noise immunity, and line frequency rejection. The nominal response curve for F_O = 50 kHz is shown in *Figure 15*. The 300 kHz pole is fixed. The 50 kHz pole is set by C_L's value. After C_L is found, the resulting line frequency attenuation is found for the bandpass filter.

Use *Figure 15* to find a C_L value given for F_O. The approximate line frequency attenuation of the bandpass filter may then be found in *Figure 16*. *Figure 15* returns a value for C_L 33% larger than nominal, giving a low frequency pole 33% low to allow for component tolerances.

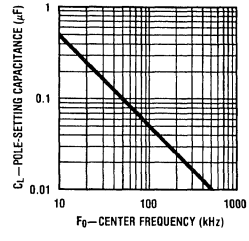


TL/H/6750–15

FIGURE 14. The 60 Hz line rejection of the highpass filter made up of C_C and T_1's line-side winding (neglecting capacitive coupling)



TL/H/6750–16



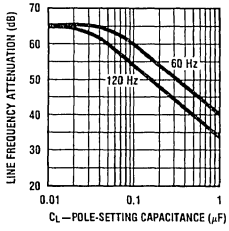
TL/H/6750–17

FIGURE 15. Given F_O, C_L is found. Also shown is the input amplifier's small signal amplitude response

Component Selection (Continued)

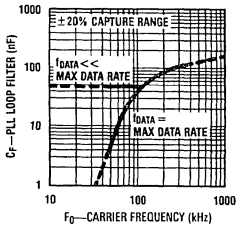
C_F and R_F

These phase-locked loop (PLL) loop filter components remove some of the noise and most of the $2F_O$ components present in the demodulated differential output voltage signal from the phase detector. They affect the PLL capture range, loop bandwidth, damping, and capture time. Because the PLL has an inherent loop pole due to the integrator action of the ICO (via C_O), the loop pole set by C_F and the zero set by R_F gives the loop filter a classical 2nd-order response.



TL/H/6750–18

FIGURE 16. The Norton-input limiter amplifier bandpass filter line-frequency signal attenuation given C_L



TL/H/6750–19

FIGURE 17. Find C_F given F_O. *Figure 19* gives the maximum data rate

No C_F and R_F give the most stable PLL with the fastest response. Large C_F's with a too-small R_F cause PLL loop instability leading to poor capture range and poor step response or oscillation.

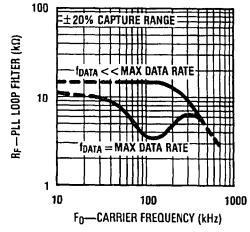
Calculation of C_F and R_F is quite difficult, involving not only the 2nd-order loop step response, but also the PLL non-dominant poles, the tuned transformer stepped-frequency response, and the RC lowpass step response (for data rates approaching 1 kHz). C_F and R_F values are best found empirically. Tolerance is not critical. Component values are selected to give the best possible impulse noise rejection while preserving a ±20% capture range and wide stability margin. *Figures 17* and *18* give C_F and R_F values versus F_O, where "f_{DATA} << MAX DATA RATE" means that f_{DATA} should be less than the maximum data rate, in kHz, from *Figure 19* divided by 10.

Note that C_F and R_F are a function of data rate only for high data rates and are not plotted against data rate - as one might expect. The reason for this is important to understand if the CCT system designer wishes to find C_F and R_F empirically. Data signal is, loosely speaking, passed through the PLL loop and is therefore potentially attenuated if the loop bandwidth is on the order of the 3rd harmonic of the data rate, or less. Overall loop bandwidth is held as low as possible for maximum noise rejection while passing the data. Loop bandwidth is roughly proportional to the geometric mean of the unfiltered loop bandwidth and the filter pole set by C_F. Therefore, C_F is related to data rate. Unfortunately, the loop capture range falls to critically low values when large enough values of C_F are used to reduce loop bandwidth down to the 100's of Hz range, for low data rates. The obvious way out is to then reduce the unfiltered loop bandwidth. That bandwidth is approximately proportional to the value of C_O. For a fixed F_O, unfiltered loop bandwidth reduction requires a larger C_O and larger control current. With this chip, changing the control current is not allowed. So one is forced to choose a C_F/R_F combination with some minimum capture range, say ±20%, that is within some guardband from the point of loop instability. Happily, impulse noise tends to last only fractions of a millisecond so that the lack of low bandwidth loop response with low data rates is not a heavy penalty. As long as there is adequate capture range, the impulse noise filter performs admirably. Note that reducing F_O will reduce the no-filter loop bandwidth, and indeed the maximum data rate falls below the limit set by the RC lowpass filter as F_O falls below 100 kHz (*Figure 19*).

The tuned transformer characteristics will affect the demodulated data waveform more than C_F and R_F at low data rates. Tank Q and off-tuning will affect overshoot during the FSK frequency steps. This is a property of tuned circuits. The maximum data rate of *Figure 19* is measured from the receiver input to the Data Out and does not include the data bandwidth reducing effects of T_I.

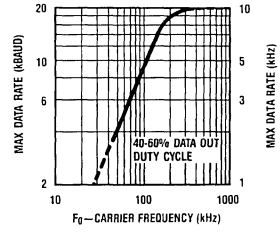
C_M

Capacitor C_M stores a voltage corresponding to a correction factor required to cancel the phase detector differential output DC offsets. The stored voltage is 5/6 of the DC offset plus some bias level of about 2.2 V. A large C_M value increases the time required to bias-up the receive path at the beginning of transmission. A large C_M does filter well and store its bias voltage long. Because of the initial random charge of C_M, the receiver must be given a data transition to charge to the proper bias voltage. Therefore, reducing C_M's value to one that may be charged in less than 2 bit-times will not save biasing time and is not recommended.



TL/H/6750–20

FIGURE 18. Find R_F given F_O with F_{DATA} a parameter

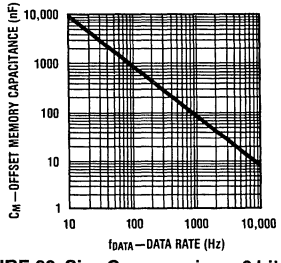


TL/H/6750–21

FIGURE 19. The maximum data rate versus F_O using loop filter components optimized for max. noise performance while retaining a min. ±20% capture range (large signal)

Use *Figure 20* to find C_M's value knowing f_{DATA}, assuming the standard 2 bit receive charge time is desired. The cap. value and TC are not critical, but the capacitor should have low leakage.

Component Selection (Continued)



TL/H/6750–22

FIGURE 20. Size C_M assuming a 2 bit-time receive bias time

C_I

The impulse noise filter integrator capacitor C_I is used to disallow the passage of any pulse shorter than the integrator charge time. That charge time, set to a nominal ½ bit time, is the time required for a ±50 μA charge current to swing C_I over a 2 V_{BE} range. Charge time under worst case conditions must never be greater than a bit time since no signal could then pass. Using a ±10% capacitor, full junction temperature range, and full specified current range, a maximum nominal charge time of ½ bit is recommended. *Figure 21* gives C_I versus data rate under those conditions.

R_C

The collector pull-up resistor is sized to supply adequate pull-up current drive and speed while preserving adequate output low current drive.

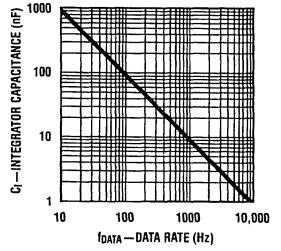


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FIGURE 21. Impulse noise filter cap. C_I versus F_{DATA} where the charge time is ½ bit time

Z_A

The 5.1V silicon zener diode Z_A is required when a short RX-to-TX switch-over time is needed at the same time that the chip is operating in the RX mode with a pin 10 input signal swing approaching or exceeding twice the supply voltage. Predominant causes of these large swings impinging on the RX input are: 1) a transmitter's supply voltage higher than the receiver's supply voltage, 2) a TX and RX pair that are electrically close, or, 3) a higher RX T_1 step-up turns ratio than the TX T_1 step-down ratio.

Normally, when in the RX mode with small incoming signal on pin 10, the ALC remains off with pin 7 at a 6V ($V_Z - 2V_{BE}$) bias voltage. C_A is then charged to 6V. TX mode may then be selected with 6V on C_A allowing 100% TX power to pump T_1's tuned circuit, and so the AC line, quickly for fast RX-to-TX switch time. As TX output swing increases so that pin 10 swings below V_{ALC} (4.7V typically), that ALC activates to charge C_A to about 6.6V to reduce TX output drive. However, if in the RX mode pin 10 ever swings below V_{ALC}, C_A will charge to above 6.6V. Now, when the TX mode is selected with C_A at 6.6V, somewhere from 0 to 100% TX output drive is available to pump T_1's tuned circuit resulting in a slower rising line signal - effectively reducing the RX-to-TX switch time.

Use a 5.1V Z_A driven by a 0 to 0.8V logic low signal to guarantee over-temp. operation. R_A must be in series with Z_A to limit current flow and should never fall below 1 kΩ. If R_A is less than 1 kΩ, then put a 2 kΩ resistor in series with Z_A. Logic high voltages above 10V will cause current flow into pin 7 that must be limited to 1 mA (with R_A or a series R).

Breadboarding Tips

During CCT system evaluation, some techniques listed below will simplify certain measurements.

— Use caution when working on this circuit - dangerous line voltages may be present.

— When evaluating PLL operation, offset cancel circuit operation, and loop filter values, use the filter of *Figure 22* to view the demodulated signal minus the $2F_O$ and noise components. This filter models the RC lowpass filter on chip.

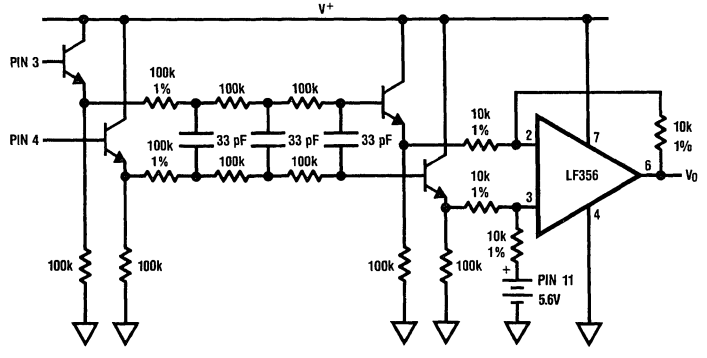

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FIGURE 22. Circuit to view the differential demodulated data signal, minus the noise and $2F_O$ components, conveniently with a single-ended gain-of-one output

Breadboarding Tips (Continued)

— When evaluating CCT system noise performance on a real power line, it is desirable to vary the signal amplitude to the receiver. This is not easy. An in-line line-proof L-pad is fine except that the line impedance is unknown and variable and so the L-pad will rarely match. Instead, the power output of a chip transmitter may be controlled using the circuit of *Figure 23*. This circuit controls the ALC.

— It is sometimes desirable to place impulse noise on the line. A simple light dimmer with a 100 W light bulb load produces representative impulse noise.

— Do not allow peak currents of over 1 A through the 5.6 V Zener. In other words, don't short charged capacitors into this low-impedance device. Take care not to momentarily short pins 10 and 11 - chip damage may result.

— *Figure 24* shows some typical signals beginning with serial data transmitted to received signal.

Tuning Procedure

This procedure applies to circuits similar to *Figure 4* LM1893 or LM2893 circuit.

First, trim F_O by putting the chip in the TX mode, setting a logical high data input, and measuring the TX high frequency, 1.022 F_O, on the Carrier I/O using these steps:

1. Take pin 17 to a logic low.
2. Take pin 5 to a logic high.
3. Place a counter on pin 10.
4. Adjust R_O on pin 18 for $F = 1.022F_O$.

Second, the line transformer is tuned. The chip is placed in the TX mode, a resistive line load is connected to disable the ALC by reducing tank voltage swing below its limit. FSK data is then passed through the tank so that the tank envelope may be adjusted for equal amplitude for high and low data frequency.

1. Take pin 5 to a logic high.
2. Place a logic-level square wave at or below the receiver's maximum data rate on pin 17.
3. Temporarily place a 330 Ω resistor across the tank.
4. Place a scope on pin 10.
5. Adjust the transformer slug for the least envelope modulation.

In lieu of the 330 Ω resistive load, T_1 may be coupled to the power line to better simulate actual load and tank pull conditions during tank tuning. Alternatively, a passive network representing an average line impedance may be connected to the line side of T_1. The circuit of *Figure 23* should then be used to defeat the leveling effect of the ALC.

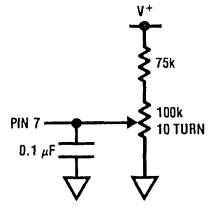

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FIGURE 23. A means of transmitter output amplitude control is shown

Thermal Considerations

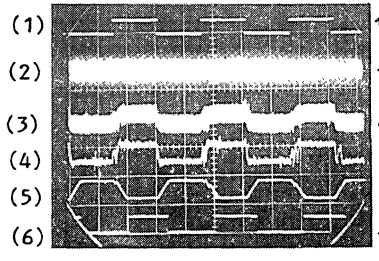
It is desirable to place the largest possible signal on the power line for maximum range, limited only by the chip power dissipation and maximum junction temperature T_J. The falling output power at elevated T_J allows a more optimal power output - high power at low T_J and lower power at high T_J for chip self-protection. However, it is still possible to exceed the maximum T_J within the specified ambient temperature limit (T_A = 85°C) under worst case conditions of 100% TX duty cyle, high supply, shorted load, poor PC board layout (with small copper foil area), and an above nominal current part. Under those conditions, a part may dissipate 2140 mW, reaching a T_J = 170°C worst-case (admittedly a rare occurrence). Proper system design includes the measurement or calculation of T_J max. to guarantee function under worst-case operation. Like all devices with failure modes modeled by the Arrhenius model, the high chip reliability is further enhanced by keeping the die temperature mercifully below the absolute maximum rating.

A direct method of measuring operating junction temperature is to measure the V_{BE} voltage on pin 18, which is always available under all operating modes. The graph of *Figure 25* may be used to find T_J, knowing V_{BE} at the operating point in question and V_{BE} at $T_A = T_J$ = 25°C. V_{BE} is found by powering up a chip (in RX mode) that has been dissipating zero power at some T_A for some time and measuring V_{BE} in less than 1 s (for better than 5°C accuracy).

Alternately, T_J may be calculated using:

$$T_J = T_A + \theta_{JA}P_D \quad (1)$$

where θ_{JA} is 75°C/W for the plastic (N) package using a socket. That θ_{JA} value is for a high confidence level; nomi-



TL/H/6750–23

FIGURE 24. Oscillogram revealing signals at several important nodes under weak signal (0.5 mV_{RMS}) conditions with SCR spikes on an otherwise quiet 115 V, 60 Hz power line. The signals are: 1) transmitted data, 2) RX carrier on the tuned transformer, 3) demodulated signal from the PLL after passing thru circuit of *Figure 22*, 4) signal after RC lowpass, 5) data at impulse noise filter integrator, and 6) received data. Horizontal scale is 10 ms per div.

Thermal Considerations (Continued)

nal θ_{JA} for an N package is 60°C/W, lower with good PC board layout. Since P_D is a relatively strong function of T_J, an iterative solution process starting with an initial guess for T_J is used. With the estimated T_J, find the total supply current found in the typical performance characteristics.

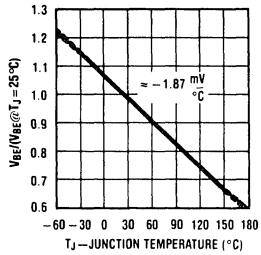


FIGURE 25. T_J may be found by using the temperature coefficient of pin 18 V_{BE} if V_{BE} is known at 25°C

Transmit-To-Receive Switch-Over Time

An important figure-of-merit for a half-duplex CCT link, affecting effective data rate, is the TX-to-RX switch time T_{TR}. Using the recommended component values gives this part a nominal 2 bit-time (1 bit time = $1/[2f_{DATA}]$) over a wide range of operating conditions, where the receiver requires 1 data transition. T_{TR} cannot be decreased significantly but does increase as noise filtering, especially via C_M, is increased. Impulse noise at switch, signals near the limiting sensitivity, poor F_O match between receiver and transmitter because of poor trim or worst-case conditions, and the statistical nature of PLL signal acquisition may all contribute to increase T_{TR} to possibly 4 bit-times.

T_{TR} is lower when a pair of LM1893's handshake rapidly. The receiver was designed to "remember" the RX-mode DC operating points on C_M and C_F while in the TX mode. Under noisy worst case conditions, C_M will discharge to the point of false operation after 35 bit-times in the TX mode (1400 bit times with no noise and a nominal part, f_{DATA} = 180 Hz). T_{TR} is about 0.8 ms (proportional to the selected F_O) plus ½ bit-time.

The major components of T_{TR} are described below for a nominal 125 kHz F_O, 180 Hz f_{DATA}, lightly-loaded tank with a Q of 20, and the circuit of *Figure 4*. The remote CCT has been operating in the TX mode with a 26.6 V_{PP} tank swing and is now selected as a receiver. An incoming signal requiring the ultimate receiver sensitivity immediately is placed on the line.

First, the tank stored energy at the transmit frequency must decay to a level below the 2.8 mV_{PP} swing caused by the 0.14 mV_{RMS} incoming line signal containing the information to be received.

$$\text{decay time} = \frac{Q}{\pi F_O} \ln\left(\frac{V_1}{V_O}\right) =$$

$$\frac{20}{\pi \times 125\,000} \ln\left(\frac{26.6}{0.0028}\right) = 0.466 \text{ ms} \qquad (2)$$

That is 0.47 ms of delay (proportional to $1/F_O$ and Q).

Second, the PLL must acquire the signal; it must lock and settle. Acquisition time is statistical and may take any length of time, but average acquisition time depends on the loop filter components C_F and R_F and the difference in center frequencies, ΔF_O, of the TX/RX pair. Using the recommended C_F and R_F (47 nF and 6.2 kΩ) with a ±4.4% ΔF_O (a ± 100 mV DC offset on C_F and R_F), lock was measured to take less than 50 cycles of F_O. That is a 0.40 ms delay (proportional to $1/F_O$).

Acquisition is incomplete until the second order PLL loop settles. For the above-mentioned C_F and R_F, the loop natural frequency F_N and damping factor are found to be 2.3 kHz and 1.0 respectively. Settling to within ±25 mV of the ±100 mV DC offset change requires 2.7 periods of F_N, or 1.2 ms (a function of C_F and R_F).

Third, the RC lowpass filter introduces a 0.12 ms delay.

Fourth, C_M must charge up to ±(5/6)100 = 83 mV depending on the polarity of F_O. Borderline data squaring with zero noise immunity is possible with only ±(5/6) 50 mV of charging. C_M charge current is an asymptotic function approximated by assuming a 50 μA charge current and the full 83 mV charge voltage. C_M charge time is then 1.7 ms (proportional to $1/f_{DATA}$).

Fifth, the impulse noise filter adds a ½ bit-time delay. Total T_{TR} is 3.9 ms plus ½ bit-time for a total of 1.9 bit-times at 360 Baud.

Receive-To-Transmit Switch-Over Time

Assume the chip has been in the RX mode and the TX mode is now selected. In less than 10 μs, full output current is exponentially building tank swing. 50% of full swing is achieved in less than 10 cycles - or under 80 μs at 125 kHz. In the same 10 μs that the output amp went on, the phase detector and loop filter are disconnected and the modulator input is enabled. FSK modulation is produced in 10 μs after switching to TX mode.

Power Line Impedance

Irrespective of how wide the limits on power line impedance Z_L are placed, there are no guarantees. However, since the CCT design requires an estimate of the lowest expected line impedance Z_{LN} encountered for the most efficient transmitter-to-line coupling, line impedance should be measured and Z_L limits fixed to a given confidence level. Reasonable values for T_1 turns ratio, loaded Q, and tank resonant frequency pull F_Q may be found to enable a CCT system design that functions with the overwhelming majority of power lines.

A limited sampling of Z_L was made, during the LM1893 design, of residential and commercial 115V 60 Hz power line. Data was also drawn from the research of Nicholson and Malack (reference 1), among others, to produce *Figures 26* and *27*. All measured impedances are contained within the shaded portions of *Figure 27*. A nominal 3.5, 7.0 and 14 Ω Z_{LN} is used throughout the application information with a nominal 45° phase angle (0° is sometimes used for simplicity).

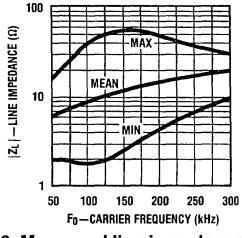


FIGURE 26. Measured line impedance range for residential and commercial 115V, 60 Hz lines

Power Line Impedance (Continued)

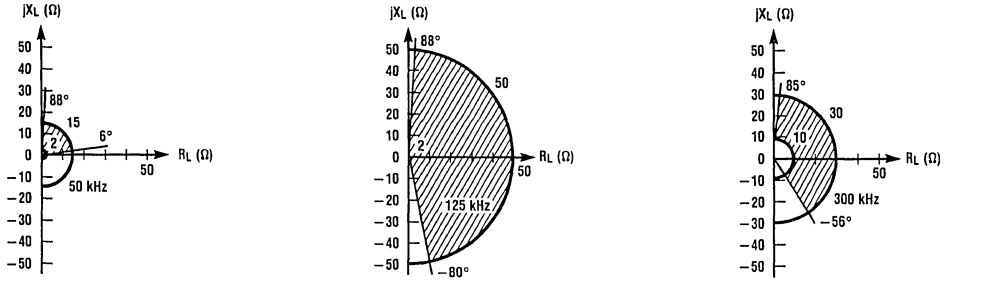


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FIGURE 27. Complex-plane plots of measured 115V, 60 Hz line impedance where $Z_L = R_L + jX_L$

Power Line Attenuation

The wiring in most US buildings is a flat 3 conductor cable called Amerflex, BX, or Romex. All referenced line impedances refer to hot-to-neutral impedances with a grounded center conductor. The cable has a 100 Ω characteristic impedance, a 125 kHz quarter-wavelength of 600 m (250 m at 300 kHz), and a measured 7 dB attenuation for a 50 m run with a 10 Ω termination. Generally, line loads may be treated as lumped impedances. Instrument line cords exhibit about 0.7 μH and 30 pF per meter.

Limited tests of CCT link range using this chip show extensive coverage while remaining on one phase of a distribution transformer (100's of m), with link failure often occuring across transformer phases or through transformers unless coupling networks are utilized. Total line attenuation allowed from full signal to limiting sensitivity is more than 70 dB. Typically, signal is coupled across transformer phases by parasitic winding capacitance, typically giving 40 dB attenuation between phased 115 V windings. Coupling capacitors may be installed for improved link operation across phases. Power factor correcting capacitor banks on industrial lines or filter capacitors across the power lines of some electronic gear short carrier signal and should be isolated with inductors. Increasing range is sometimes accomplished by electing to install the isolating inductors (*Figure 28*) and coupling capacitors, as well as by electing to use the boost option. Frequency translating or time division multiplexed repeaters will also increase range.

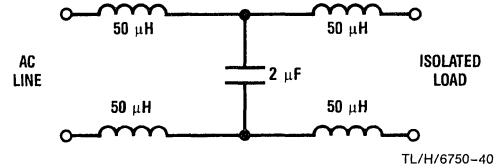

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FIGURE 28. An isolation network to prevent: 1) noise from some device from polluting the AC line, and 2) to stop some low impedance device (measured at F_O) from shorting carrier signal. Component values given as an example for $F_o = 125$ kHz on residential power lines

The Coupling Transformer

The design arrived at for T_1 is the result of an unhappy compromise - but a workable one. The goals of 1) building T_1 with a stable resonant frequency, F_Q, that is little affected by the de-tuning effect of the line impedance Z_L, and of 2) building a tightly line-coupled transformer for transmitted carrier with loose coupling for transients, are somewhat mutually exclusive. The tradeoffs are exposed in the following example for the CCT designer attempting a new boost-capable, or different core, transformer design.

The compromises are eased by separating the TX output and RX input in the LM2893. An untuned TX coupling transformer with only core coupling (not air-coupled solenoid windings) would employ a high permeability, high magnetic field, low loss, square saturating, toroidal core. The resonant RX path would be isolated from line-pull problems by a unilateral amplifier that operates at line voltages with much more than 110 dB of dynamic range, or by a capacitively coupled pulse transformer driving a unilateral amplifier and filter, for increased selectivity. See the LM2893-specific applications section.

For a LM1893-style transformer application, first, choose the turns ratio N based on an estimated lowest Z_L likely encountered, Z_{LN}. *Figure 29* shows graphically how N affects line signal. N should be as large as possible to drive Z_{LN} with full signal. If T_1 has an unloaded Q, Q_U, of well less than 35, a guess of N somewhat high should be used and later checked for accuracy. The recommended transformers have secondary taps giving a choice of N = 7.07, 10, and 14.1 (nominally) for driving Z_{LN}'s of 14, 7.0, and 3.5 Ω respectively (at T_J = 25°C, V+ = 18V, and Q_U = 35).

The resonating inductance of the tuned primary, L_1, is sought. Note that, while standard transformer design gives a transformer self-inductance with an impedance at operating frequency well above load impedance, the tuned transformer requires a low L_1 for adequate Q_U and minimum line pull. Result: relatively poor mutual coupling.

$$L_1 = \frac{R}{2\pi F_O Q} \quad (3)$$

It is known that resonant frequency $F_Q = F_O$ and some minimum bandwidth, or maximum Q, will be required to pass signal under full load conditions.

$$L_1 = \frac{R_Q \parallel |Z_{LN}|'}{2\pi F_O Q_L} \quad (4)$$

$|Z_{LN}|'$ is the reflected Z_{LN}, Q_L is the loaded Q, and parallel resistance R_Q models all transformer losses and sets Q_O. $R_Q \parallel |Z_{LN}|'$ is found knowing that it absorbs full rated power.

The Coupling Transformer (Continued)

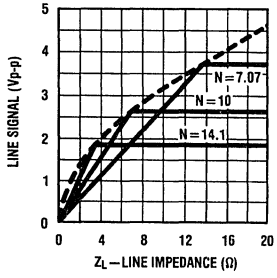

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FIGURE 29. Impressed line voltage for a given Z_L for each of the 3 taps available on the recommended transformers

$$P_O = I_O V_O = \frac{I_{OPP}}{2\sqrt{2}}\left[\frac{2(-V_{ALC}+V_+)}{2\sqrt{2}}\right] = \frac{(-4.7+V_+)I_O}{4} \quad (5)$$

where I_O is in amps peak-to-peak at an elevated T_J

$$P_O = \frac{(18 - 4.7)\,0.06}{4} = 0.200\ W \quad (6)$$

$$R_Q \| |Z_{LN}|' = \frac{V_O^2}{P_O} = \frac{(-V_{ALC} + V_+)\sqrt{2}}{I_O} = 442\ \Omega \quad (7)$$

R_Q is found using Z_{LN} and the value for N found when assuming $Q_U = 35$.

$$|Z_{LN}|' = N^2 Z_{LN} = (7.07)^2\,13.9 = 695\ \Omega \quad (8)$$

$$R_Q = \frac{1}{\frac{1}{R_Q \| |Z_{LN}|'} - \frac{1}{|Z_{LN}|'}} = \frac{1}{\frac{1}{442} - \frac{1}{695}} = 1210\ \Omega \quad (9)$$

$$R_{QS} = \frac{R_Q}{1 + Q_U^2} = \frac{1210}{1 + 35^2} = 1\ \Omega \quad (10)$$

Only Q_L remains to be found to calculate L_1. Q_L is related to the −3 dB (half-power) bandwidth by

$$Q_L = \frac{1}{BW\ (\%\ of\ F_O)} \quad (11)$$

An iterative solution is forced where line pull, ΔF_Q, must be guessed to find Q_L and L_1. L_1 is then used to check the line pull guess; a large error requires a new guess. Try a BW of 8.7% - that is 4.4% for deviation, 1% for TC of F_O, and 3.3% for ΔF_Q - giving $Q_L = 11.5$.

$$L_1 = \frac{442}{2\pi \times 125\,000 \times 11.5} = 49.0\ \mu H \quad (12)$$

Knowing the core inductance per turn, L, and L_1, the number of turns is found.

$$T_1 = \sqrt{\frac{L_1}{L}} = \sqrt{\frac{49.0\ \mu H}{20\ nH/T}} = 49\ \tfrac{1}{2}\ turns \quad (13)$$

T is normally an integer, but these transformers require so few turns that half-turns are specified, remembering that the remaining ½ turn is completed on the P.C. board and is loosely coupled. The secondary turns are calculated

$$T_2 = \frac{T_1}{N} = \frac{49.5}{7.07} = 7.00 = 7\ turns \quad (15)$$

giving an L_2 of 0.98 μH. Note that the recommended 125 kHz transformer mirrors these specifications. The resonating capacitor is

$$C_Q = \frac{1}{(2\pi F_Q)^2 L_1} = 33.1 \times 10^{-9} = 33\ nF \quad (16)$$

Line pull ΔF_Q was calculated (reference 3) for a Z_L magnitude of 14Ω and up with any phase angle from −90° to 90°. ΔF_Q was 6.4% - well above the 3.3% estimate. Referring to (11), an 11.8% bandwidth is required, forcing L_1 to be reduced to reduce Q. That fix was not implemented; some signal attenuation under worst-case drift and ΔF_Q is allowed. L_1 is already so small that the 31 gauge winding conducts a ¼ A_{RMS} circulating current.

Line Carrier Detection

While the addition of a carrier detection circuit (for a mute or squelch function) will only decrease receiver ultimate sensitivity, there is sometimes good reason to employ it to free the controller from watching for RX signal when no carrier is incoming, or to employ it to reduce the probability of line collisions (when multiple transmitters operate simultaneously to cause one or more transmissions to fail). Unless the detector is heavily filtered or uses a high carrier amplitude threshold, there will be false outputs that force the controller to have Data Out data checking capability just as is required when using no carrier detector. If false triggering is minimized, the probability of line collisions is increased due to the inability to sense low carrier amplitudes and because of sense delay. The property of the LM1893 to change output state infrequently (although the polarity is undefined) when in the RX mode, with no incoming carrier, reduces the desire to implement carrier detection and preserves the full ultimate sensitivity. Also, many impulse-noise insensitive transmission schemes, like handshaking, are easily modified to recover from line collisions.

Regarding this, it should be stated that for very complicated industrial systems with long signal runs and high line noise levels, it is probably wise to use a protocol which is inherently collision free so that no carrier detect hardware or software is needed. A token passing protocol is an example of such a system.

Figure 30 shows a low cost carrier amplitude detection circuit.

Audio Transmission

The LM1893 is designed to allow analog data transmission and reception. Base-band audio-bandwidth signals FM modulate the carrier passing through the tuned transformer (placing a limit on the usable percent modulation) onto the power line to be linearly demodulated by the receiver PLL. Because the receiver data path beyond the phase detector will pass only digital signal, external audio filtering and amplification is required. *Figure 31* shows a simple audio transmitter and receiver circuit utilizing a carrier detection mute circuit. A single LM339 quad. comparator may be used to build the carrier detect and mute. Filter bandwidth is held to a minimum to minimize noise, especially line-related correlated noise.

Communication and System Protocols

The development of communication and system protocols has historically been the single most time consuming element in design of carrier current systems. The protocols are defined as the following:

1. *Communication protocol*: a software method of encoding and decoding data that remains constant for every transmis-

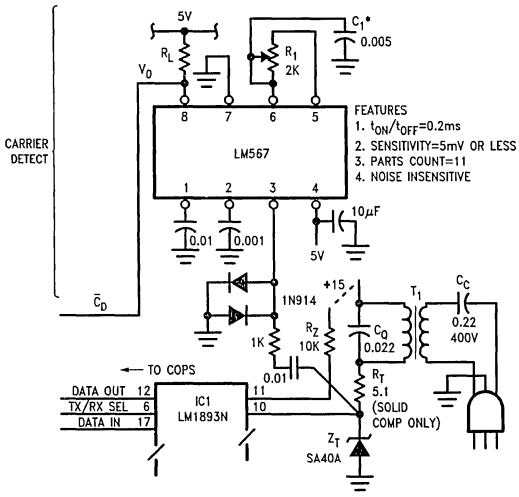

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FIGURE 30. A simple carrier amplitude detector with output low when carrier is detected

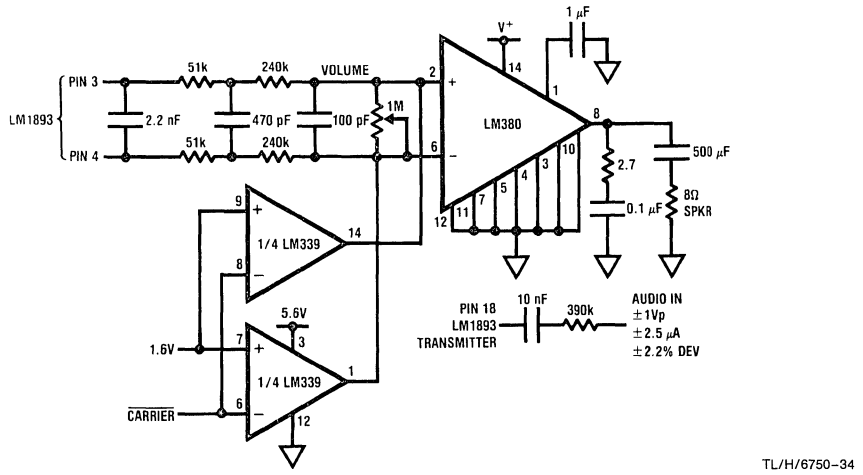

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FIGURE 31. A simple linear analog audio transmitter and receiver are shown. The carrier and 1.6V inputs are derived from the carrier detector of *Figure 30.* The remaining 2 LM339 comparators may be used to build the carrier detector circuit.

Communication and System Protocols (Continued)

sion in a system. Its first purpose is to put data in a baseband digital form that is more easily recognized as a real message at the receive end. Secondly, it incorporates encoding techniques to ensure that noise induced errors do not easily occur; and when they do, they can always be detected. Lastly, the software algorithms that are used on the receive end to decode incoming data prevent the reception of noise induced "phantom" messages, and insure the recovery of real messages from an incoming bit stream that has been altered by noise.

2. *System protocol*: the manner in which messages are coordinated between nodes in a system. Its first purpose is to ensure message retransmission to correct errors (handshake). Secondly it coordinates messages for maximum utilization and efficiency on the network. Lastly, it ensures that messages do not collide on the network. Common system protocols include master-slave, carrier detect multiple access, and token passing. Token passing and master slave have been found to be the most useful since they are inherently collision free.

Both protocols usually reside as software in a single microcontroller that is connected to the LM1893/2893 I/O. In any case, some sort of intelligence is needed to process incoming and outgoing messages. UARTs have no usefulness in

Communication and System Protocols (Continued)

carrier current applications since they do not have the intelligence needed to distinguish between real messages and noise induced phantoms.

The difficulty in designing special protocols arises out of the special nature of the AC line, an environment laden with the worst imaginable noise conditions. The relatively low data rates possible over the AC line (typically less than 9600 baud) make it even more imperative that systems utilize the most sophisticated means available to ensure network efficiency.

With these facts in mind, the designer is referred to two publications intended to aid in the development of carrier current systems. The first is literature #570075 The Bi-Line Carrier Current Networking System, a 200 pp. book that functions as the "bible" of Bi-Line system design. It has sections on LM1893 circuit optimization, protocol design, evaluation kit usage, critical component selection, and the Datachecker/DTS case study.

The second is AN-463 "A New Carrier Current Protocol Utilizing an Active Transponder for Consumer and Industrial Applications." It details the communication and system protocols developed by Datachecker/DTS for an energy management system.

Basic Data Encoding (please refer to the previously mentioned publications for advanced techniques)

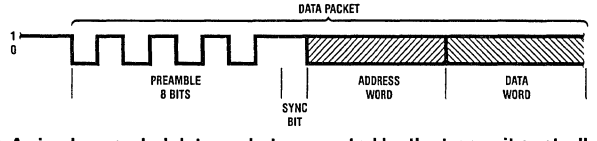
At the beginning of a received transmission, the first 0 to 2 bits may be lost while the chip's receiver settles to the DC bias point required for the given transmitter/receiver pair carrier frequency offset. With proper data encoding, dropped start bits can be tolerated and correct communication can take place. One simple data encoding scheme is now discussed.

Generally, a CCT system consists of many transceivers that normally listen to the line at all times (or during predetermined time windows), waiting for a transmission that directs one or more of the receivers to operate. If any receiver finds its address in the transmitted data packet, further action such as handshaking with the transmitter is initiated. The receiver might tell the transmitter, via retransmission, that it received this data, waiting for acknowledgement before acting on the received command. Error detecting and correcting codes may be employed throughout. The transmitter must have the capability to retransmit after a time if no response from the receiver is heard - under the assumption that the receiver didn't detect its address because of noise, or that the response was missed because of noise or a line collision. (A line collision happens when more than 1 transmitter operates at one time - causing one or more of the communications to fail). After many re-transmissions the transmitter might choose to give up. Collision recovery is achieved by waiting some variable amount of time before retransmission, using a random number of bits delay or a delay based on each transmitter's address, since each transceiver has a unique address.

An example of a simple transmission data packet is shown in *Figure 32*. The 8 bit 50% duty-cycle preamble is long enough to allow receiver biasing with enough bits left over to allow the receiver controller to detect the square-wave that signals the start of a transmission. If there had been no transmission for some time, the receiver would simply need to note that a data transition had occurred and begin its watch for a square-wave. If the receive controller detected the alternating-polarity data square-wave it would then use the sync. bit to signal that the address and data were immediately following. The address data would then be loaded, assuming the fixed format, and tested against its own. If the address was correct, the receiver would then load and store the data. If the address was not correct, either the transmission was not meant for this receiver or noise has fooled the receiver. In the former case, when the transmission was not meant for the receiver, the controller should immediately return to watching the incoming data for its address. If the later case were true, then the receive controller would continue to detect edges, tieing itself up by loading false data and being forced to handshake. The square-wave detection and address load and check routines should be fast to minimize the time spent in loops after being false-triggered by noise. If the controller detects an error (a received data bit that does not conform to the pre-defined encoding format) it should immediately resume watching the LM1893's Data Out for transmissions, the next bit would be shifted in and the process repeated.

A line-synchronous CCT system passing 3 bits per half-cycle may replace the long 8 bit preamble and sync pulse with a 2 bit start-of-transmission bias preamble. The receive controller might then assume that preamble always starts after bit 1 (the first bit after zero-crossing) so that any data transition at a zero crossing must be the start of the address bits and is tested as such. The line synchronous receiver operates with a simpler controller than an asynchronous system.

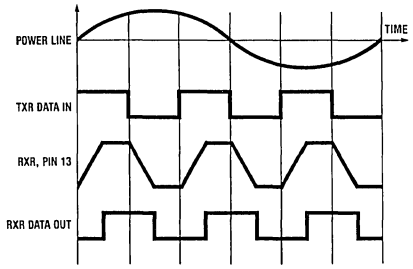
Discussion has assumed that the controller has always known when the Data Out is high or low. The controller must sample at the proper time to check the Data Out state. Since noise shows itself as pulse width jitter, symmetrically placed about the no-noise switch-points, optimum Data Out sampling is done in the center of the received data pulse. The receive data path has a time delay that, at low data rates, is dominated by the impulse noise filter integrator and is nominally ½ bit. At a 2 kHz data rate, an additional delay of approximately $1/10$ bit is added because of the cumulative delay of the remainder of the receiver. *Figure 33* shows that Data Out sampling occurs conveniently at the transmitted



TL/H/6750–35

FIGURE 32. A simple encoded data packet, generated by the transmit controller is shown. The horizontal axis is time where 1 bit time is $1/(2f_{DATA})$

Basic Data Encoding (Continued)



TL/H/6750–36

FIGURE 33. Operating waveforms of a line-synchronized transceiver pair are shown. The diagram shows how the transmitted data transitions may be used as received data sampling points

data edges for the line synchronous data transmission scheme mentioned in the previous paragraph. With the asynchronous system suggested, the receive controller must sample the Data Out pin often to determine, with several bits of accuracy, where the square-wave data transitions take place, average their positions assuming a known data rate, and calculate where the center of the data bits are and will continue to be as the address and data are read. A long preamble is helpful. Software that continuously updates the center-of-bit time estimate, as address and data are received, works even better. Alternatively, a coding scheme employing an embedded clock can be used.

LM2893 Application Hints

The LM2893 is intended for advanced applications where special circuitry is used in the transmit and receive paths. The LM2893 makes this possible by featuring separate transmit output and receive input pins.

Examples of enhancements that can be added to the basic LM1893/2893 circuit include separate transmit and receive windings on the coupling transformer, high quality ceramic or LC filters in the receive path, and simple impulse noise blanking circuits.

In many applications, the additional performance to be gained outweighs the extra cost of the additional circuitry. More than likely, high performance industrial applications such as building energy management will fit into this category, since they require the utmost in reliability.

Because of the specialized nature of individual LM2893 applications, it is not possible to give one circuit that will satisfy all requirements for performance and cost effectiveness. Therefore no specific application examples will be given. Instead the subsequent text describes in general terms the types of circuits that can be used to increase performance along with their advantages and disadvantages. It is intended to be a springboard for ideas.

LM2893 COUPLING NETWORKS

The main disadvantages of the typical LM1893 coupling network are that it functions as the bandpass filter, has loose coupling between primary and secondary, and has a single secondary. The LM1893 coupling network was designed this way mainly because of the restraint that the carrier input and output are tied together.

Because the coupling transformer is used as a filter, the LM1893 circuit is susceptible to pulling of the center frequency under conditions of changing line impedances or when several LM1893 circuits are close in proximity on the AC line. Because the tuned transformer has a high value of "Q", ringing also occurs in the presence of impulsive noise. This ringing occurs at the center frequency and increases the error rate of transmissions, especially at relatively high data rates (>2000 baud). Because it is the only tuned circuit in the system, the selectivity characteristics leave a lot to be desired.

The LM2893, having separate receive input and transmit output pins, removes the limitations on coupling transformer design, allowing the design of circuits devoid of the previous limitations.

The first enhancement that can be made with the LM2893 circuit is the use of a high permeability ferrite toroid for line coupling along with a separate filter. The transformer would be of broadband design (untuned) with two secondaries, one for coupling to the transmit output and one for coupling to the receive input. This allows impedance matching of both the transmitter and receiver, with the result of quite a bit more receive sensitivity.

Because of the increased signal and separate receive signal path, a 3 or 6 db pad can be used before the selective stages to eliminate pulling of the center frequency due to changes in line impedance.

Another advantage of the toroidal transformer is that it can be designed for use at very low line impedances due to its inherent tight coupling.

SEPARATE FILTER

Because of the separate receive path of the LM2893, a relatively high quality bandpass filter can be used for selectivity. Inexpensive ceramic filters are available that have bandpass and center frequency characteristics compatible with carrier current operation. Futhermore, the use of these filters allows multichannel operation, previously made difficult by the single tuned network of the LM1893. These filters are easily cascaded for even more off-frequency rejection. If the pad is added before the filter, there will be negligible pulling due to changes in line impedance reflected through the coupling transformer.

Alternatively, a Butterworth/Chebyshev bandpass LC filter or an active filter can be used in place of the ceramic filter.

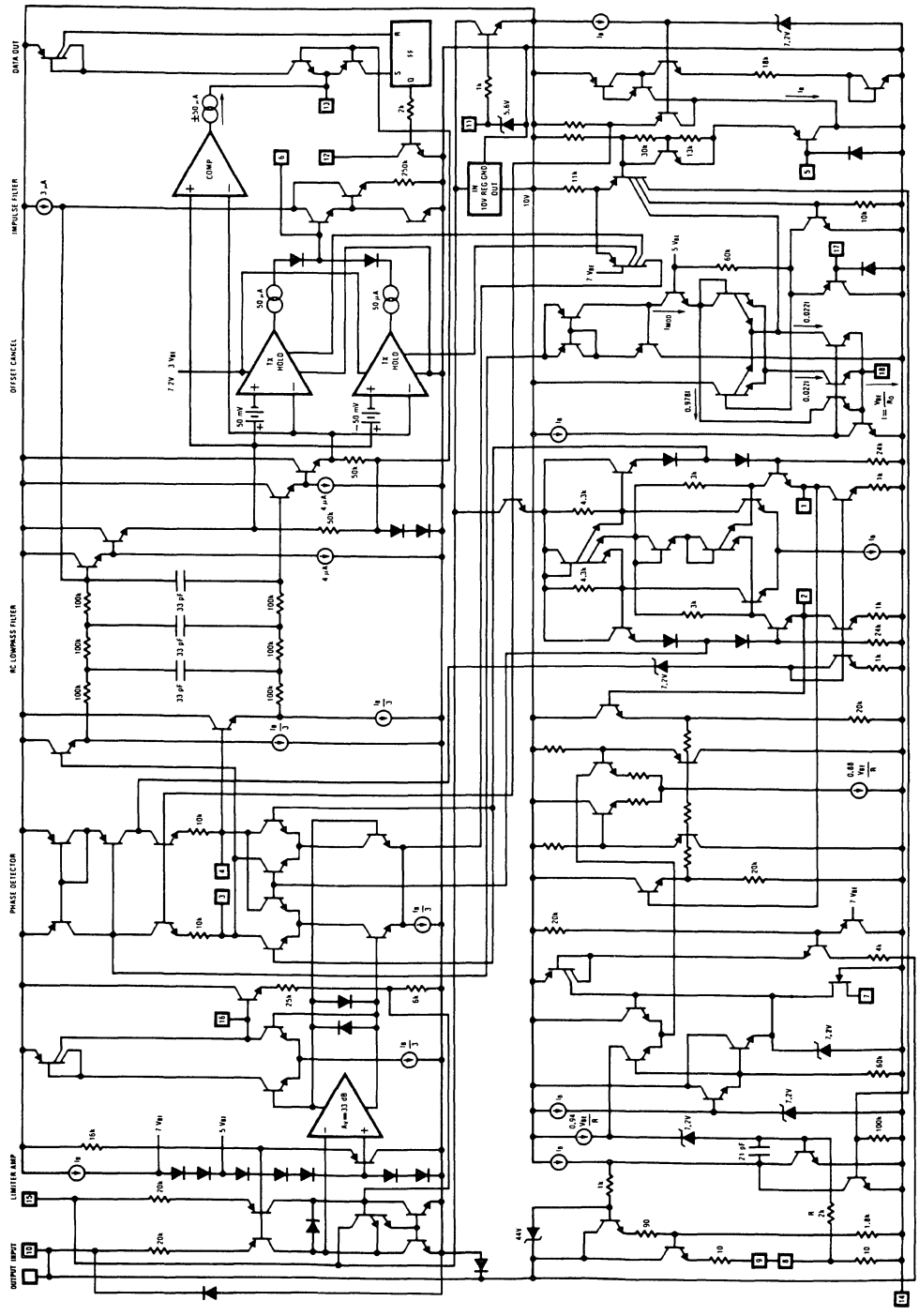
IMPULSE NOISE BLANKER

Although the LM2893 has adequate impulse noise rejection for most applications, there is reason to employ impulse blanking to improve error rates in severe AC line environments. Typically, errors occur due to pulse jitter in the LM1893/2893 data output that originates when the internal time domain filter smooths out an incoming noise pulse.

The solution involves removing the impulse completely and not simply trying to filter it. Moreover, the pulse should be removed in the receive signal path before the selective portions of the circuit to eliminate ringing. This also allows the receiver filter to smooth out the blanks that also occur in the desired incoming carrier signal.

If a carrier detect circuit is desired in conjunction with the LM2893 it can be located after the filter and impulse blanker. Because impulse noise is removed, the false triggering that plagues these circuits will be greatly reduced.

Simplified Schematic



References

1. Nicholson, J.R. and J.A. Malack; "RF Impedance of Power Lines and Line Impedance Stabilization Network in Conducted Interference Measurements;" IEEE Transactions on Electromagnetic Compatibility; May 1973; (line impedance data)
2. Southwick, R.A.; "Impedance Characteristics of Single-Phase Power Lines;" Conference Rec.; 1973 IEEE Int. Symp. on Electromagnetic Compatibility; (line impedance data)
3. Hayt, William H. Jr. and Jack E. Kemmerly; "Engineering Circuit Analysis;" McGraw-Hill Books; 1971; pp. 447–453; (linear transformer reflected impedance)
4. FCC, "Notice of Proposed Rule Making," Docket 20780, adopted Apr. 14, 1976, (Proposed regulation)
5. Monticelli, Dennis M. and Michael E. Wright; "A Carrier Current Transceiver IC for Data Transmission Over the AC Power Lines;" IEEE J. Solid-State Circuits; vol. SC-17; Dec. 1982; pp. 1158-1165; (LM1893 circuit description)
6. Lee, Mitchell; "A New Carrier Current Transceiver IC;" IEEE Trans. on Consumer Electronics; vol. CE-28; Aug. 1982; pp. 409–414; (Application of LM1893)

National Semiconductor Corporation

LM1921 1 Amp Industrial Switch

General Description

The LM1921 Relay Driver incorporates an integrated power PNP transistor as the main driving element. The advantages of this over previous integrated circuits employing NPN power elements are several. Greater output voltages are available off the same supply for driving grounded loads; typically 4.5 volts for a 500 mA load from a 5.0 volt supply. The output can swing below ground potential up to 57 volts negative with respect to the positive power supply. This can be used to facilitate rapid decay times in inductive loads. Also, the IC is immune to negative supply voltages or transients. The inherent Safe Operating Area of the lateral PNP allows use of the IC as a bulb driver or for capacitive loads.

Familiar integrated circuit features such as short circuit protection and thermal shutdown are also provided. The input voltage threshold levels are designed to be TTL, CMOS, and LSTTL compatible over the entire operating temperature range. If several drivers are used in a system, their inputs and/or outputs may be combined and wired together if their supply voltages are also common.

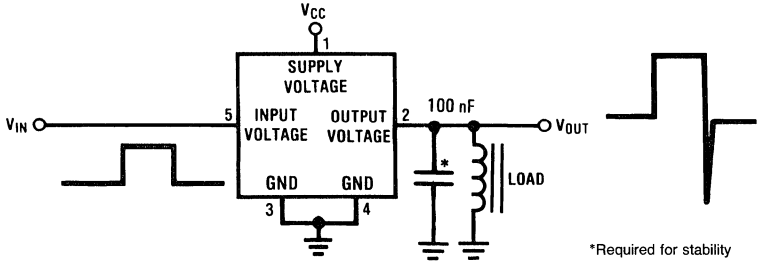
Features

- 1 Amp output drive
- Load connected to ground
- Low input-output voltage differential
- +60 volt positive transient protection
- −50 volt negative transient protection
- Automotive reverse battery protection
- Short circuit proof
- Internal thermal overload protection
- Unclamped output for fast decay times
- TTL, LSTTL, CMOS compatible input
- Plastic TO-220 package
- 100% electrical burn-in

Applications

- Relays
- Solenoids
- Valves
- Motors
- Lamps
- Heaters

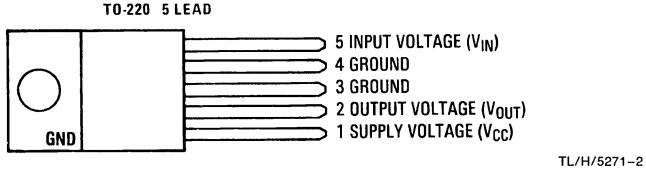
Typical Application Circuit



TL/H/5271–1

FIGURE 1. Test and Application Circuit

Connection Diagram



TL/H/5271–2

Front View
Order Number LM1921T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage	
Operating Range	26V
Overvoltage Protection (100 ms)	−50V to +60V
Internal Power Dissipation	Internally Limited
Operating Temperature Range	−40°C to +125°C
Maximum Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics (V_{CC} = 12V, I_O = 500 mA, T_J = 25°C, V_{IN} = 2V, unless otherwise specified.)

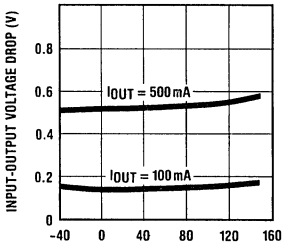
Parameter	Conditions	Typ	Tested Limits (Note 1)		Design Limits (Note 2)		Units
			Min	Max	Min	Max	
Supply Voltage							
Operational			4.75	26	6	24	V
Survival			−15	60			V_{DC}
Transient	100 ms, 1% Duty Cycle		−50				V
Supply Current							
V_{IN} = 0		0.6				1.5	mA
V_{IN} = 2V	I_o = 0 mA	6		10			mA
	I_o = 250 mA	285		350			mA
	I_o = 500 mA	575		700			mA
	I_o = 1A	1.3		1.5			A
Input to Output Voltage Drop	I_o = 500 mA	0.5		0.8			V
	I_o = 1A	1.0					V
Short Circuit Current		1.4	1.0	2.0			A
	6V ≤ V_{CC} ≤ 24V				.75	3.0	A
Output Leakage Current	V_{IN} = 0	0.1				50	μA
Input Voltage Threshhold		1.3	0.8	2.0			V
	6V ≤ V_{CC} ≤ 24V				0.8	2.0	V
Input Current		15	10	30			μA
Overvoltage Shutdown		32			26	36	V
Thermal Resistance							
junction-case	θjc	3					°C/W
case-ambient	θca	50					°C/W
Inductive Clamp Output Voltage	V_{IN} = 0, I_o = 100 mA	−60			−120	−45	V
Fault Conditions							
Output Current							
Input Floating	Pin 5 Open	0.1				50	μA
Ground Floating	Pin 3 & Pin 4 Open	0.1				50	μA
Reverse Voltage	V_{CC} = −15V	−0.01			−1		mA
Reverse Transient	V_{CC} = −50V	−100					mA
Overvoltage	V_{CC} = +60V	0.01				1	mA
Supply Current	Pin 1 & Pin 2 Short, No load	10				40	mA

Note 1: Guaranteed and 100% production tested.

Note 2: Guaranteed, not necessarily 100% production tested. Not used to calculate outgoing AQL. Limits are for the temperature range of −40°C ≤ T_j ≤ 150°C.

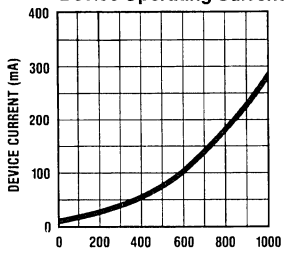
Typical Performance Characteristics

Output Voltage Drop



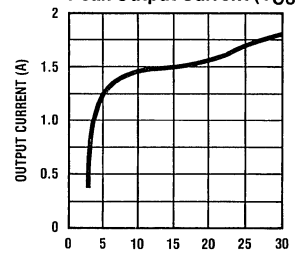
TL/H/5271–3

Device Operating Current



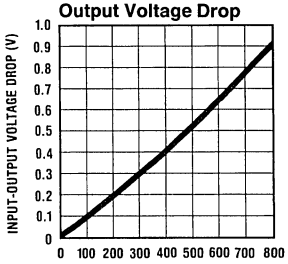
TL/H/5271–4

Peak Output Current (V_{OUT})



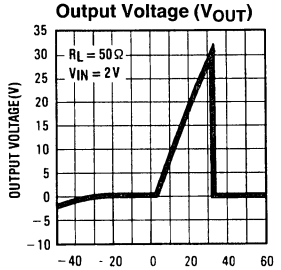
TL/H/5271–5

Output Voltage Drop



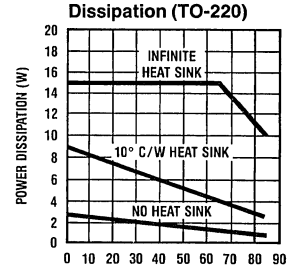
TL/H/5271–6

Output Voltage (V_{OUT})



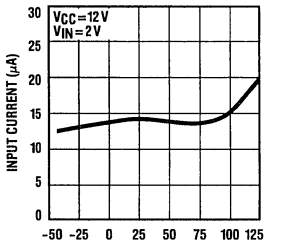
TL/H/5271–7

Maximum Power Dissipation (TO-220)



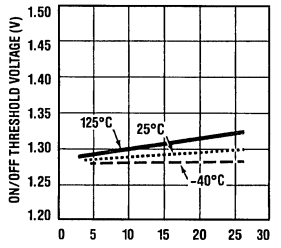
TL/H/5271–8

Input Current vs. Junction Temperature



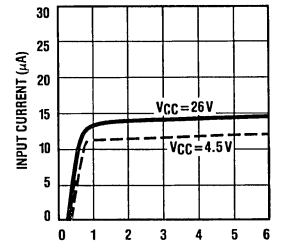
TL/H/5271–13

Threshold Voltage vs. Supply Voltage



TL/H/5271–14

Input Current vs. Input Voltage



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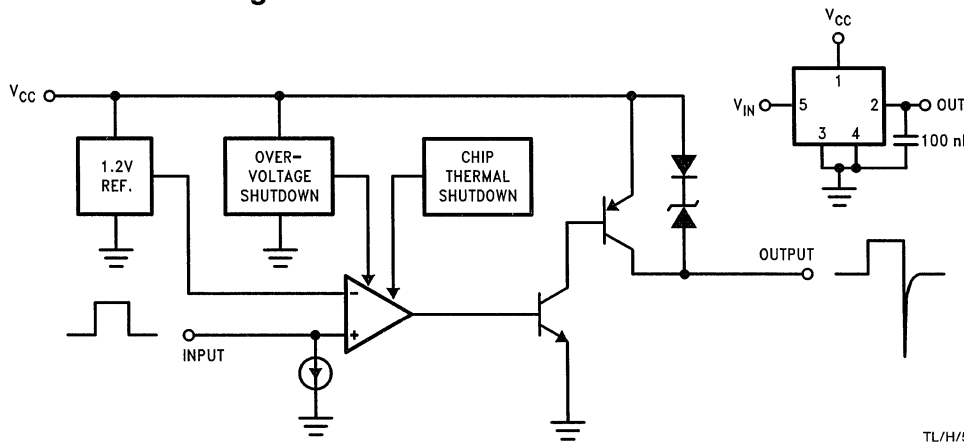
Equivalent Block Diagram



TL/H/5271–12

FIGURE 1

Circuit Schematic

TL/H/5271–9

Application Hints

HIGH CURRENT OUTPUT

The 1 Amp output is fault protected against overvoltage. If the supply voltage rises above approximately 30 volts, the output will automatically shut down. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. The 1921 will survive transients and DC voltages up to 60 volts on the supply. The output remains off during this time, independent of the state of the input logic voltage. This protects the load. The high current output is also protected against short circuits to either ground or supply voltage. Standard thermal shutdown circuits are employed to protect the 1921 from over heating.

FLYBACK RESPONSE

Since the 1921 is designed to drive inductive as well as any other type of load, inductive kickback can be expected whenever the output changes state from on to off (see waveforms on *Figure 1*). The driver output was left unclamped since it is often desirable in many systems to achieve a very rapid decay in the load current. In applications where this is not true, such as in *Figure 2*, a simple external diode clamp will suffice. In this application, the integrated current in the inductive load is controlled by varying the duty cycle of the input to the driver IC. This technique achieves response characteristics that are desirable for certain automotive transmission solenoids, for example.

For applications requiring a rapid controlled decay in the solenoid current, such as fuel injector drivers, an external zener and diode can be used as in *Figure 3*. The voltage rating of the zener should be such that it breaks down before the output of the LM1921. The minimum output breakdown voltage of the IC output is rated at −57 volts with respect to the supply voltage. Thus, on a 12 volt supply, the combined zener and diode breakdown should be less than 45 volts.

The LM1921 can be used alone as a simple relay or solenoid driver where a rapid decay of the load current is desired, but the exact rate of decay is not critical to the system. If the output is unclamped as in *Figure 1*, and the load is inductive enough, the negative flyback transient will cause the output of the IC to breakdown and behave similarly to a zener clamp. Relying upon the IC breakdown is practical, and will not damage or degrade the IC in any way. There are two considerations that must be accounted for when the driver is operated in this mode. The IC breakdown voltage is process and lot dependent. Clamp voltages ranging from −60 to −120 volts (with respect to the supply voltage) will be encountered over time on different devices. This is not at all critical in most applications. An important consideration, however, is the additional heat dissipated in the IC as a result. This must be added to normal device dissipation when considering junction temperatures and heat sinking requirements. Worst case for the additional dissipation can be approximated as:

$$\text{Additional } P_D = I^2 \times L \times f \text{ (Watts)}$$

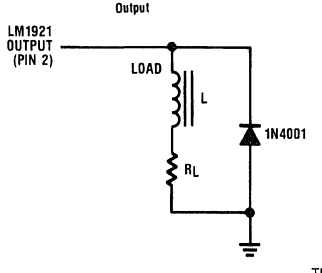
where: I = peak solenoid current (Amps)

L = solenoid inductance (Henries)

f = maximum frequency input signal (Hz)

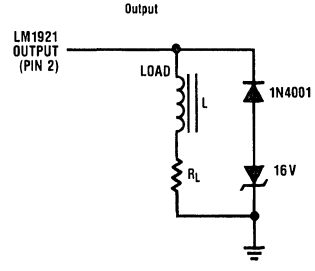
For solenoids where the inductance is less than ten millihenries, the additional power dissipation can be ignored.

Overshoot, undershoot, and ringing can occur on certain loads. The simple solution is to lower the Q of the load by the addition of a resistor in parallel or series with the load. A value that draws one tenth of the current or DC voltage of the load is usually sufficient.



TL/H/5271–10

FIGURE 2. Diode Clamp



TL/H/5271–11

FIGURE 3

Zener clamp for rapid controlled current decay

National Semiconductor Corporation

PRELIMINARY

LM1946 Over/Under Current Limit Diagnostic Circuit

General Description

The LM1946 provides the industrial or automotive system designer with over or under current limit detection superior to that of ordinary transistor or comparator-based circuits.

Applications include lamp fault detection, motor stall detection, and power supply bus monitoring.

Each of the five independent comparators can be used to monitor a separate load as either an over current or under current limit detector. Two comparators monitoring a single load can function as a current window monitor.

Current is sensed by monitoring the voltage drop across the wiring harness, pc board trace, or external sense resistor that feeds the load.

Provisions for compensating the user set limits for wiring harness resistance variations over temperature and supply voltage variations are also available.

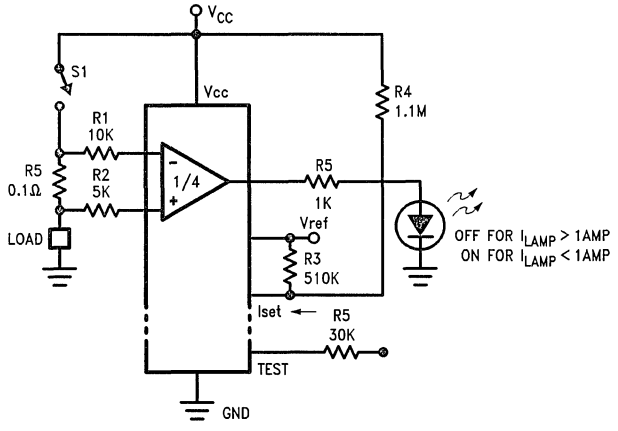
When a limit is reached in one of the comparators, it turns on its output which can drive an external LED or microprocessor.

One side of the load can be grounded (not possible with ordinary comparator designs), which is important for automotive systems.

Features

- Five independent comparators
- Capable of 30 mA per output
- Low power drain
- User set input threshold voltages
- Reverse battery protection
- 60V load dump protection on supply and all inputs
- Input common mode range exceeds V_{CC}
- Short circuit protection
- Thermal overload protection
- Prove-out test pin
- Available in plastic DIP and SO packages

Typical Application Circuit—Lamp Fault Detector (I_L > 1A)



TL/H/8707–2

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC} and Input Pins)
- Survival Voltage (T ≤ 100 ms) −50V to +60V
- Operational Voltage 26V

Internal Power Dissipation (Note 1)	Internally Limited
Output Short Circuit to Ground or V_{CC}	Continuous
Operating Temperature Range (T_A)	−40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+230°C

Electrical Characteristics

9V ≤ V_{CC} ≤ 16V, Iset = 20 μA, T_j = 25°C (unless otherwise specified)

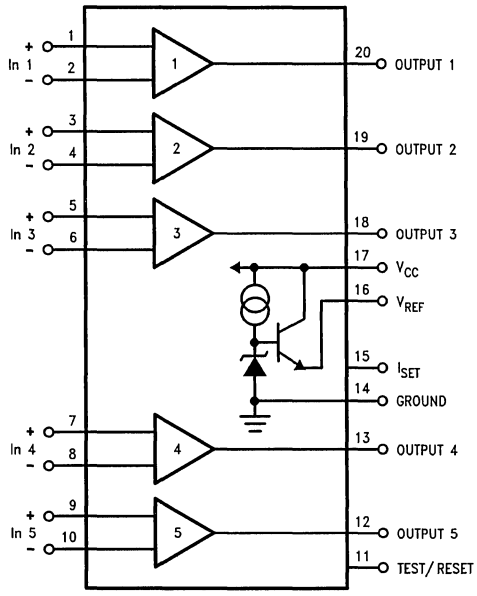
Parameter	Conditions	Min	Typ	Max	Units
Quiescent Current	All Outputs "Off"		1.40	3.00	mA_{dc}
Reference Voltage	I_{ref} = 10 μA	5.8	6.4	7.0	V_{dc}
Reference Voltage Line Regulation	9V ≤ V_{CC} ≤ 16V, I_{ref} = 10 μA		±5	±50	mV_{dc}
Iset Voltage	Iset = 20 μA	1.20	1.40	1.60	V_{dc}
Input Offset Voltage	At Output Switch Point. V_O = 2V 9V ≤ V_{CM} ≤ 16V		±1.0	±5.0	mV_{dc}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, 9V ≤ V_{CM} ≤ 16V		±0.10	±1.00	μA_{dc}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, 9V ≤ V_{CM} ≤ 16V	18.00	20.00	22.00	μA_{dc}
Input Common Mode Voltage Range		4.00		26.0	V_{dc}
Maximum Positive Input Transient	Either Input. T ≤ 100 ms	60	70		V
Maximum Negative Input Transient	Either Input. T ≤ 100 ms	−50	−60		V
Output Saturation Voltage	I_O = 2 mA, 5V ≤ V_{CC} ≤ 16V		0.80	1.00	V_{dc}
	I_O = 10 mA, 5V ≤ V_{CC} ≤ 16V		1.00	1.20	V_{dc}
Output Short Circuit Current	V_O = $0V_{dc}$, Comparator "ON"	30	45	120.0	mA_{dc}
Output Leakage Current	V_O = $0V_{dc}$. Comparator "Off"		0.01	1.00	μA_{dc}
Test Threshold Voltage	At Switch Point on Any Output V_O = 2V (Note 2)	0.80	1.25	2.00	V_{dc}
Test Threshold Current			0.2		μA_{dc}

Note 1: Thermal resistance from junction to ambient is typically 53°C/W for LM1946 (board mounting).

Note 2: The test pin is an active high input, i.e. all five will be forced high when this pin is driven high.

Connection Diagram

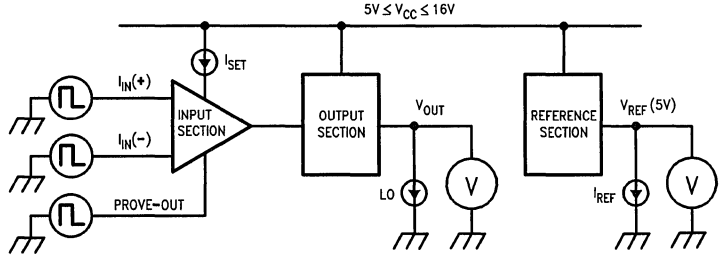
LM1946



TL/H/8707–20

Order Number LM1946N
See NS Package Number N20A

Typical Test Circuit



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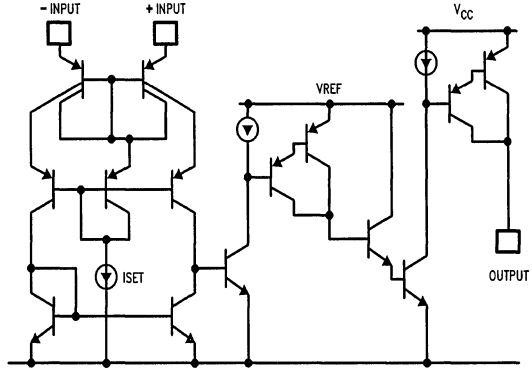
Simplified Comparator Schematic



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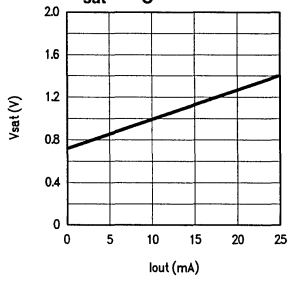
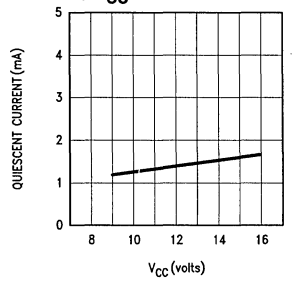
Typical Performance Characteristics (Continued)

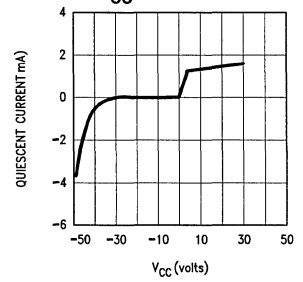
V_{sat} vs I_O



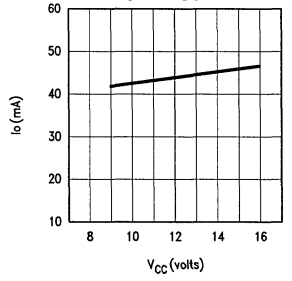
Quiescent Current vs V_{CC}



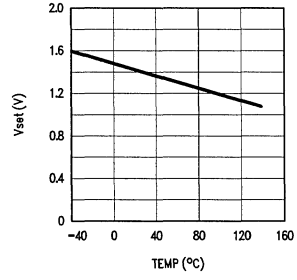
Quiescent Current vs V_{CC}



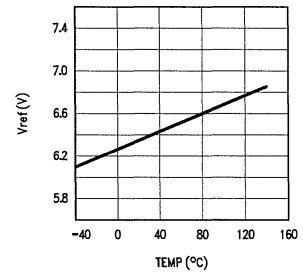
Peak I_O vs V_{CC}



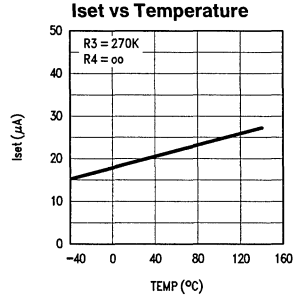
V_{set} vs Temperature



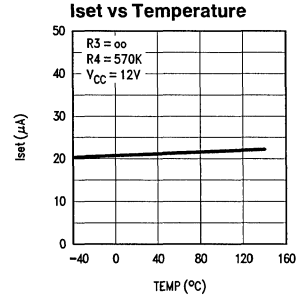
V_{ref} vs Temperature



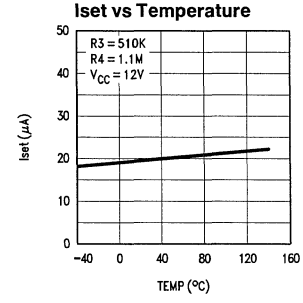
Iset vs Temperature



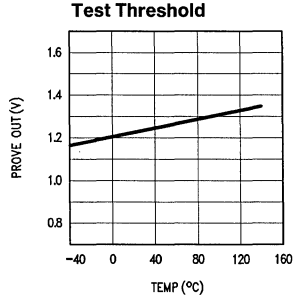
Iset vs Temperature



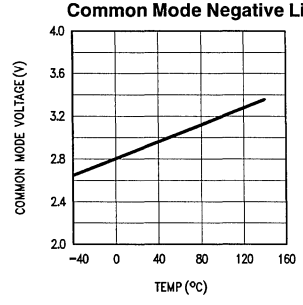
Iset vs Temperature



Test Threshold



Common Mode Negative Limit



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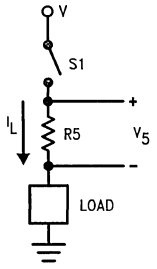
Application Hints

THEORY OF OPERATION: UNDER-CURRENT LIMIT DETECTOR



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Lamp Fault Detector

FIGURE 3. Equivalent Automotive Lamp Circuit

The diagram of *Figure 3* represents the typical lamp circuit found in most automobiles. Switch S1 represents a dashboard switch, discrete power device, relay and/or flasher circuit used for turn signals. Sense resistor R_S can be an actual circuit component (such as a 0.1Ω 1W carbon resistor) or it can represent the resistance of some or all of the wiring harness. The load, represented here as a single bulb, can just as easily be two or more bulbs in parallel, such as front and rear parking lights, or left and right highbeams, etc.

One of the easiest methods to electronically monitor proper bulb operation is to sense the voltage developed across R_S by the bulb current I_L. If a fault occurs, due to an open bulb filament, the load current and sense voltage, V_S, drop to zero (or to half their former values in the case of two bulbs wired in parallel). A comparator type circuit can then monitor this sense voltage, and alert the system or system user (e.g. power an LED) if this sense voltage drops below a predetermined level (defined as the threshold voltage).

Typical sense voltages range from tens to hundreds of millivolts. Not only does this sense voltage vary nonlinearly with the battery voltage, it may vary significantly with ambient temperature depending on the temperature coefficient (TC) of the sense resistor or wiring harness. Since these nonlinear characteristics can vary from system to system, and sometimes even within a single system, provisions must be made to accommodate them. There are two general methodologies to accomplish this.

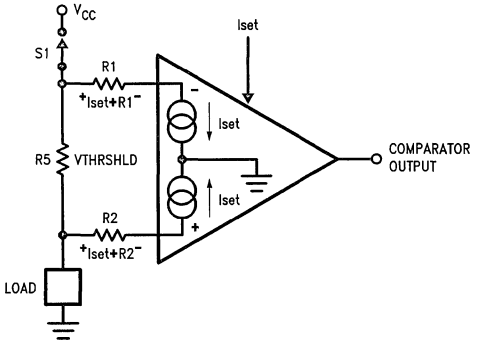
The first method uses only one bulb per monitoring circuit. A sense resistor is selected to give 50–100 mV of sense voltage in an operational circuit, and a comparator threshold detecting voltage of approximately 10 mV is set. Even if component tolerances, battery line variations, and temperature coefficients cause the sense voltage to vary 3:1 or more, circuit operation will not be affected.

The second method must be used if two or more bulbs are wired in parallel and it is necessary to detect if any single lamp fails. This is often desirable as it reduces the number of comparators and displays and system cost by at least a factor of two. In this case, the sense voltage will drop by only half (or less) of it's original value. For example, a nominal 100 mV drop across the sense resistor will drop to 50 mV if one of two bulbs fail. Therefore, a threshold detection voltage between 50 and 100 mV is required (since a 10 mV threshold would alert the system only if **both** bulbs failed). Yet a fixed threshold of 75 mV may not work if the nominal 100 mV sense voltage can vary 3:1 due to the factors mentioned earlier. What is required is a comparator with a threshold-detecting voltage that tracks the nominal sense voltage as battery line and ambient temperature change. Thus, while the sense voltage may nominally be anywhere from 50 to 150 mV, the threshold voltage will always be roughly 75% of it, or 37 mV to 112 mV, and will detect the failure of either of two bulbs.

The LM1946 integrated circuit contains five comparators especially designed for lamp monitoring requirements. Since all lamps in a system share the same battery voltage and ambient temperature, accommodations for these variations need to be made only once at the IC, and each threshold of the five comparators then tracks these variations.

SETTING THE COMPARATOR THRESHOLD VOLTAGE

The comparator threshold voltage at which the comparator output changes state is user-set in order to accommodate the many possible system designs. The input bias currents are purposely high to accomplish this, and are each equal to the user-set current into the Iset pin (more on this later). Typically around 20 μA, the effect of this across the sense resistor, R_S compared to a typical load measured in amps is negligible and can be ignored. However, when resistors R1 and R2 (*Figure 5*) are added to the circuit a shift in the threshold voltage is effected. This occurs since each input has been affected by different IR drops. The LM1946 comparator behaves like any other comparator in that the output switches when the input voltage at the IC pins is zero millivolts (ignoring offset voltage for the moment). If the output therefore has just switched states due to just the right threshold voltage across the sense resistor, then the sum of voltages around the resistor loop should equal zero:



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Vthrshld = Iset (R1 − R2)

FIGURE 4. Input Bias Current

$$\text{Vthrshld} + \text{Iset} \bullet \text{R2} - \text{Voffset} - \text{Iset} \bullet \text{R1} = 0$$

Assuming Voffset ≪ Vthrshld:

$$\text{Vthrshld} = \text{Iset} \bullet \text{R1} - \text{Iset} \bullet \text{R2}$$

$$\text{Vthrshld} = \text{Iset}\,(\text{R1} - \text{R2})$$

Application Hints (Continued)

Typical values are:

R1 = 6.2k ±5%

R2 = 1.2k ±5%

Iset = 20 μA @ 25°C

Vthrshld = 20 μA (6.2k − 1.2k) = 100 mV

For values of sense voltages greater than 100 mV, the comparator output is off (low). Sense voltages less than 100 mV turn the output on (high).

It's also important that the output of the comparator be in the "off" state when the inputs are taken to ground, i.e. S1 is opened and the light is turned "off". The input section of LM1946 has been designed to turn "off" when the inputs are grounded and therefore not deliver an erroneous bulb out indication. The comparator is only activated when the inputs are above ground by at least 3V.

R1 and R2 are necessary for another reason. These resistors protect the input terminals of the IC from the many transients in an automobile found on the battery line, some of which can exceed a thousand volts for a few microseconds. A minimum value of approximately 1 kΩ is therefore recommended.

COMPENSATING FOR BATTERY VOLTAGE

The current through a typical automotive lamp, whether a headlight or dashboard illumination lamp, will vary as battery voltage changes. The change, however, is nonlinear. Doubling the battery voltage does not double the lamp current.

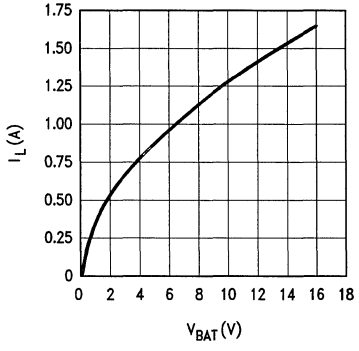

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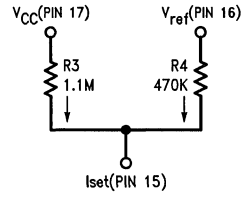
FIGURE 5

This occurs since a higher voltage will heat the filament more, increasing its resistance and allowing less current to flow than expected. *Figure 6* shows this effect. A best fit straight line over the normal battery range of 9V to 16V for this particular example can be given by:

$$I_L \text{ (Amps)} = 0.62 + 0.069 \bullet \text{Vbattery}$$



TL/H/8707–10

$$\text{Iset} = \frac{V_{CC} - 1.2}{R3} + \frac{\text{Vref} - 1.2}{R4}$$

$$\text{Iset} = \frac{V_{CC}}{R3} + \frac{\text{Vref}}{R4} - 1.2\left(\frac{1}{R3} + \frac{1}{R4}\right)$$

FIGURE 6

Thus, in actual use, the LM1946/1947 threshold voltages should track the variations in bulb current with respect to battery voltage. To accomplish this, Iset should have a component that varies with the battery. As shown in the LM1946 circuit schematic of *Figure 18*, the Iset pin is two diode drops above ground, or appoximately 1.2V. A resistor from this pin to the 6.5V reference sets the fixed component of Iset; a resistor to the battery line sets the variable component. Thus, the best fit straight line in *Figure 5* can be realized exactly with only two resistors. The result is shown in *Figure 6*, giving a nominal Iset of 20 μA that tracks the bulb current as supply varies from 9V to 16V. The graph of *Figure 7* shows the final result comparing a typical sense voltage across Rs with the comparator threshold voltage as the supply varies.

COMPENSATING FOR AMBIENT TEMPERATURE VARIATION

If the sense resistors used in a system are perfect components with no temperature coefficient, then the compensation to be subsequenty detailed here is unnecessary. However, resistors of the very small values usually required in a lamp outage system are sometimes difficult or expensive to acquire. A convenient alternative is the wiring harness, a length of wire, or even a trace on a printed circuit board. All of these are of copper material and therefore can vary by as much as 3900 ppm/°C. The LM1946 has been designed to accommodate a wide range of temperature compensation techniques. If the Iset current is designed to increase or decrease with temperature, nearly any temperature coefficient can be produced in the threshold voltage of the four input pairs.

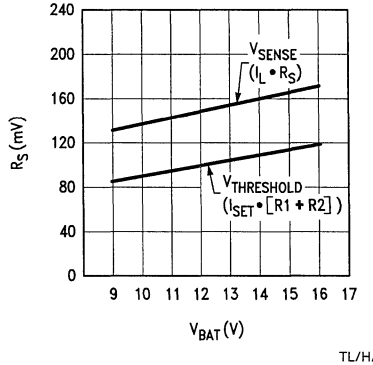


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FIGURE 7

Application Hints (Continued)

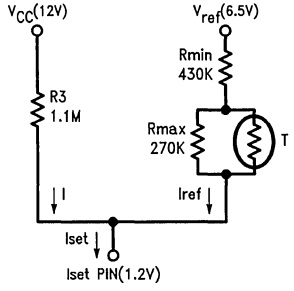
One solution is to use a low cost thermistor in conjunction with some low-TC resistors (see *Figure 8*).

There are three fixed resistors and one thermistor. This is an NTC thermistor, since it has a **negative** temperature coefficient. This is what is required in order to have Iset **increase** as the temperature rises. The data sheet with the thermistor described a number of ways to establish different final TC's. The thermistor itself has a very large TC which is somewhat difficult to describe mathematically. But, if it is used with some other fixed resistors, such as Rmin and Rmax, definite end point limits can be established and an approximate staight line TC generated. See *Figure 9* for a graphic representation of the ideal calculated values of Iset and the actual measured values generated. Notice that there is very close agreement between the two graphs. The circuit actaully creates an S-shaped curve around the ideal.

The low-cost thermistor is available from Keystone and is listed as follows: RL2008-52.3K-155-D1.

OVER-CURRENT LIMIT DETECTOR

Other applications include an over-current detector, as shown in *Figure 10*. The load represented here can be either a single component or an entire system. Resistors R3



Thermistor
Keystone:
RL2008-52.3K-155-D1
100k @ 25°C

TL/H/8707–11

FIGURE 8. Thermistor/Resistor Network

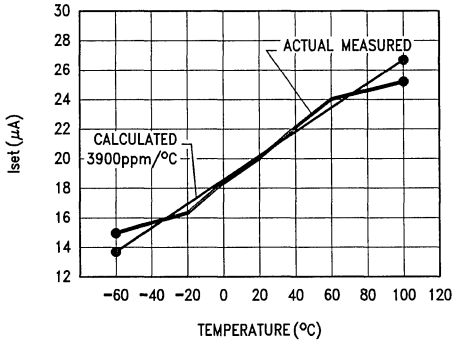


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FIGURE 9. Iset vs Temperature with *Figure 8* Circuit

Application Hints (Continued)

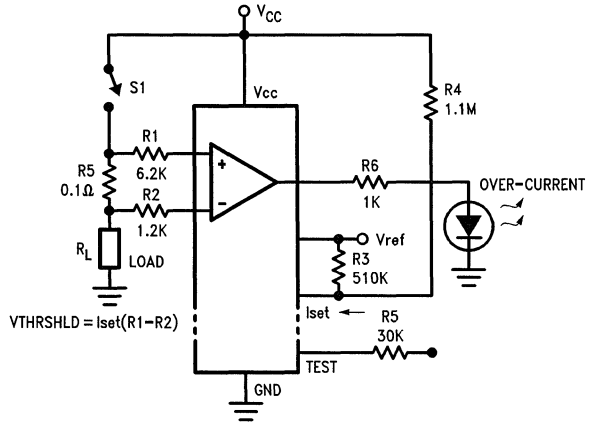

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FIGURE 10. Using the LM1946 as an Over-Current Limit Detector

and R4 again allow the system designer to tailor the threshold limit to the V/I characteristics of each particular system. The input threshold voltage is determined by, and directly proportional to, Iset into pin 20. R3, from the on-chip reference voltage, provides a current and threshold that is independent of the supply voltage, V_{CC}. R4 provides a current directly proportional to supply. These resistors allow thresholds to be either independent of, or directly proportional to supply voltage, or anything in between. For example, the values in *Figure 10* are tailored to match the V/I characteristics of the bulb filament used in earlier examples. However, if the load had purely resistive characteristics, Iset and the threshold would be set with R4 only, eliminating R3. Likewise, if the load current was independent of supply, such as in many systems powered by a voltage regulator, Iset would be better set by R3 only, eliminating R4. Further details on this and how to handle variations with ambient temperature with resistor and thermistor combinations are discussed in detail in previous sections. Compensation for temperature variations, however, is rarely necessary since short circuit or over-current values are usually much greater than the nominal value. For example, if the load in *Figure 10* represented a DC motor, the circuit could be used to detect the motor stall condition. Stall current through the sense resistor, Rs, would typically be five times the nominal running current. By setting the threshold at three times the nominal current value, enough margin exists that minor variations due to temperature can be ignored. The variation in stall current due to battery or supply voltage can be significant, however. Being approximately proportional, Iset would best be set in this case by R4 only.

WINDOW DETECTOR

The availability of more than one comparator per IC allows many other applications. One is the current sense window detector. Many times it is useful to know that a certain current is within both an upper and lower limit. Using two of the LM1946 comparators and the circuit of *Figure 11* will accomplish this. In this particular case, high and low limits are approximately 3A and 1A respectively. The outputs can be kept separate or wired-or, as shown, to a single output load as a simple out-of-bounds detector.

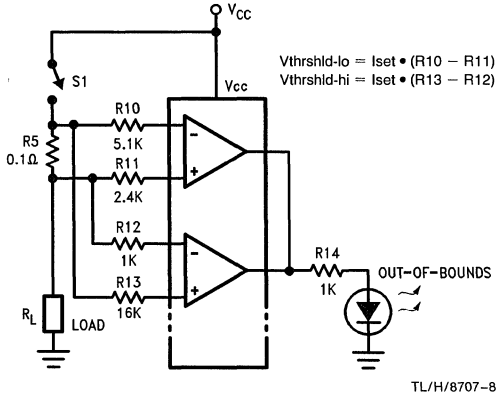

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FIGURE 11. Current Limit Window Detector

COMPARATOR INPUT STAGE

The LM1946 IC consists of five specially designed comparator input circuits to monitor the IR drop across the wiring harness or the sense resistor between the battery and the light bulb. These comparators have been designed to accommodate a wide range of input signals without damage to the IC or the load circuitry. The inputs can easily withstand a common mode voltage above the positive supply since the inputs are the emitters of two matched PNP devices (see *Figure 12*). This is vital in a system which must operate in the conditions present under the hood of an automobile. The inputs can also survive when taken well below ground. If a negative voltage is present at the inputs of the comparator, the two emitter-base PNP junctions become reverse biased and block any current flow in or out of the device.

Application Hints (Continued)

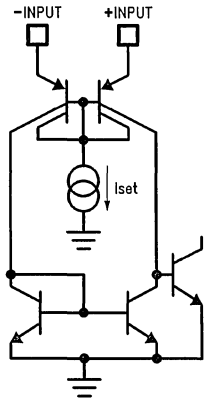

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FIGURE 12. Comparator Input Stage

THE OUTPUT SECTION

The output section of the LM1946 is different from most automotive comparators as it employs high beta proprietary PNP transistors which are very rugged and capable of higher output currents. Each of the four comparator outputs is capable of about 25 mA of drive and are internally current limited and protected against supply overvoltage. The LM1946 is therefore capable of driving LED's directly and larger bulbs via an external grounded base NPN (see *Figures 13* and *14*). The outputs can also be wired-or together without harm.

For use in systems with a microprocessor flag instead of a dashboard indicator, the LM1946 can be powered by a standard 5V logic supply. This prevents the LM1946 output from swinging above the microprocessor supply which might cause latch problems. Since the input common mode range is independent of supply, the inputs can still operate at any level up to 26V. Since the outputs can source current only, pull-down resistors as in *Figure 15* are required, their value depending on the input drive requirements of the particular microprocessor used.

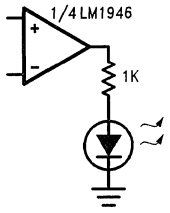

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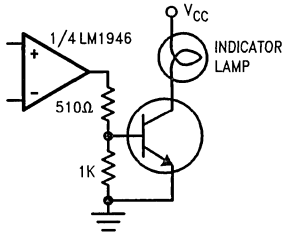
FIGURE 13



TL/H/8707–14

FIGURE 14

TEST/RESET PIN

The test pin is a high impedance logic input. Forcing this pin high ($\geq$ 2V) forces all four comparator outputs on. This is used to test the indicator LED display (or other output load). The usual application circuit connects this pin to the ignition crank line. During engine crank, therefore, the LM1946 output display will light, similar to the usual dashboard indicators. The test pin was designed to operate with the usual transient voltages found on the crank line as long as a limiting resistor (e.g. 30k) separates them *(Figure 1)*.

The test pin will also reset any comparator outputs that have been latched or delayed in the high state (see next section). This occurs on the falling edge of the test input signal. The minimum pulse width to guarantee reset is dependent on largest capacitor connected to any control pin:

Minimum pulse width (ms) $\approx$ 0.01 + 1.5 • C1 (μF)

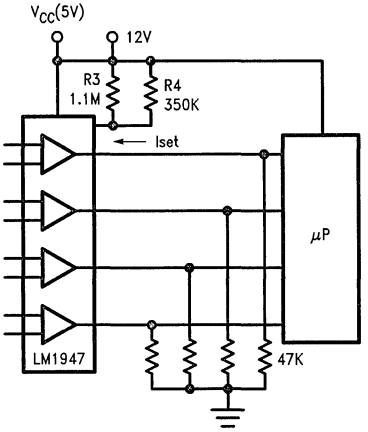


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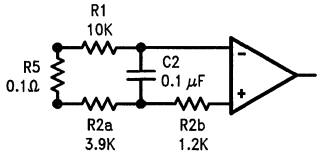
FIGURE 15

Application Hints (Continued)

MORE NOISE FILTERING

The current flowing through the sense resistor and certain loads can sometimes be very noisy, particularly when the load is a DC motor, or switching supply. Large amounts of noise on the supply line can also cause problems when threshold voltages are set to very small values. In these cases, while the average current level may remain well below the threshold trip point, noise peaks may exceed it. A LED display could then flicker or appear dimly lit, or excessive software routines and processor time may be required for a μP to disregard such noise. Noise transients can be particularly annoying in application circuits employing the output latch, as a sufficient noise spike will erroneously trip the output and require resetting the circuit. While a capacitor on the control pin can be effective for the infrequent noise transient (see "Control Pin" section) such as during power-up, it is much less effective for suppressing other types of noise. This occurs because C1 charges and discharges at different rates, typically a 50:1 ratio. A regularly occurring noise pulse would eventually "pump up" C1 to 1.2V and trigger the output. Often such noise must be filtered directly at the inputs, using the input resistors R1 and R2 and a capacitor. Care must be taken, however, that such a filter will not cause an erroneous output state upon power-up or whenever switch S1 is closed. The most effective general methodology to achieve this is to split the resistor in the positive input lead into two resistor values and connect a capacitor from here to the negative input. For example, the 1.2k resistor R2 of *Figure 1* could be replaced with 3.9k and 1.2k resistors as shown in *Figure 16a* (R1 increasing from 6.2k to 10k to compensate). The value of capacitor C2 depends upon the degree of filtering required, the amount of noise present, and the response times desired. The choice of values for the new resistors is almost arbitrary. Generally the larger value is attached to the sense resistor for better decoupling. The smaller value must be large enough so that the DC voltage across it upon power-up exceeds the maximum offset voltage expected of the comparator (i.e. Iset*R2b>5.0mV). It is this requirement that guarantees that the output will not be in an erroneous high state upon power-up or whenever S1 is closed. (Should this feature be unnecessary to a particular application circuit, the methodology described can be replaced with a simple capacitor across the comparator input pins).

For extremely severe cases, additional filter stages can be cascaded at the inputs (see *Figure 17*). Since the input bias currents of the comparator are equal at the input threshold level, the voltage drops across the 1k resistors cancel and do not affect the DC operation of the circuit (ignoring resistor match tolerance and Ios). If an application circuit is noisy enough to require such an elaborate filter, then ferrite beads, shown here as L1 and L2, will also probably help.



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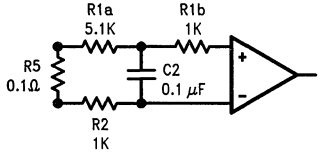
a. Open-Circuit Detector



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b. Short-Circuit Detector

FIGURE 16. Input Noise Filters for Various Application Circuits

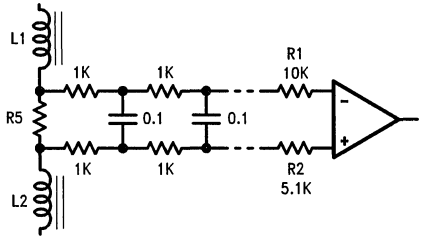

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FIGURE 17. Additional Noise Filters

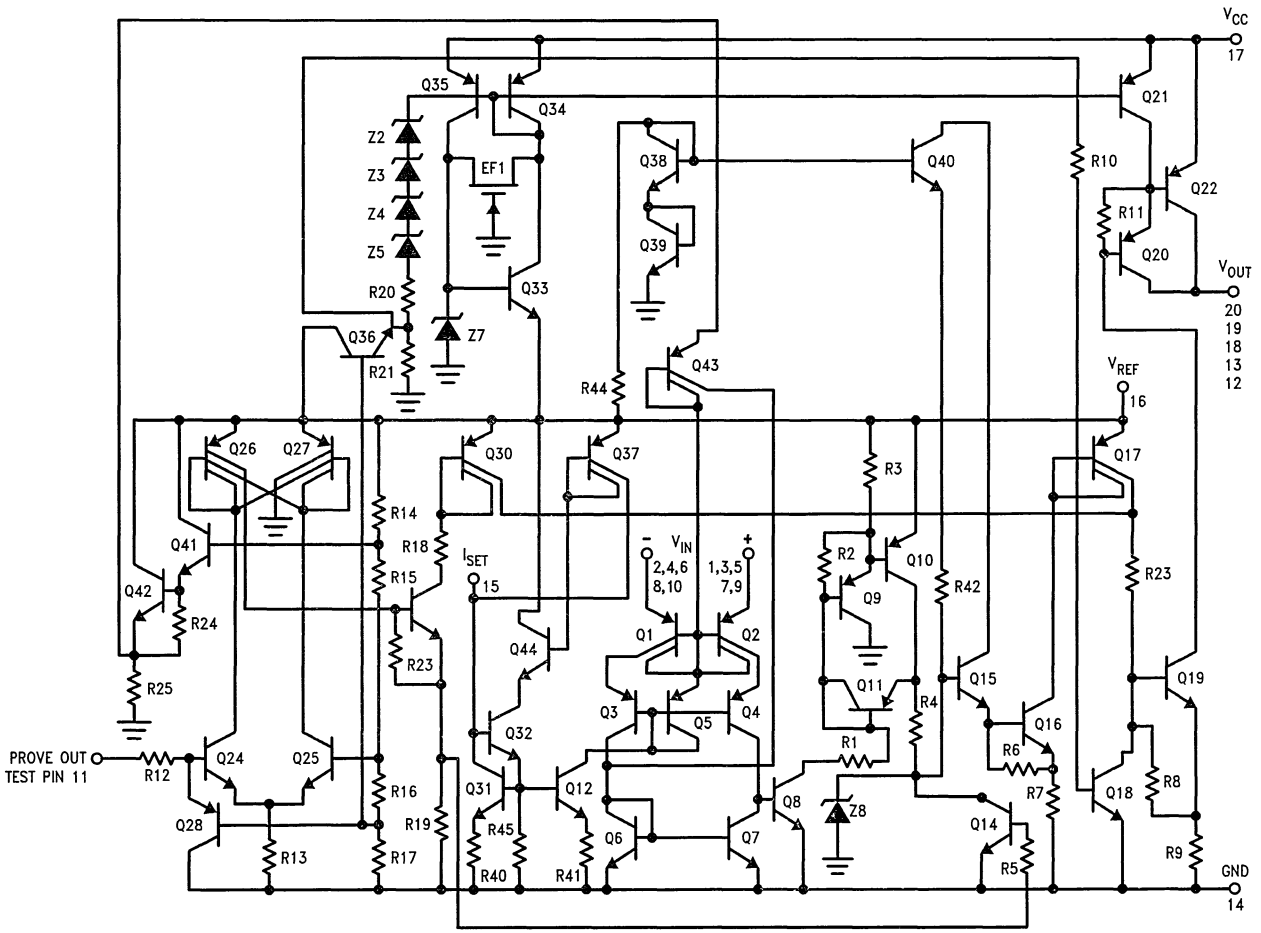

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FIGURE 18

National Semiconductor Corporation

LM1949 Injector Drive Controller

General Description

The LM1949 linear integrated circuit serves as an excellent control of fuel injector drive circuitry in modern automotive systems. The IC is designed to control an external power NPN Darlington transistor that drives the high current injector solenoid. The current required to open a solenoid is several times greater than the current necessary to merely hold it open; therefore, the LM1949, by directly sensing the actual solenoid current, initially saturates the driver until the "peak" injector current is four times that of the idle or "holding" current *(Figure 3-Figure 7)*. This guarantees opening of the injector. The current is then automatically reduced to the sufficient holding level for the duration of the input pulse. In this way, the total power consumed by the system is dramatically reduced. Also, a higher degree of correlation of fuel to the input voltage pulse (or duty cycle) is achieved, since opening and closing delays of the solenoid will be reduced.

Normally powered from a 5V ±10% supply, the IC is typically operable over the entire temperature range (−55°C to +125°C ambient) with supplies as low as 3 volts. This is particularly useful under "cold crank" conditions when the battery voltage may drop low enough to deregulate the 5-volt power supply.

The LM1949 is available in the plastic miniDIP, (contact factory for other package options).

Features

- Low voltage supply (3V-5.5V)
- 22 mA output drive current
- No RFI radiation
- Adaptable to all injector current levels
- Highly accurate operation
- TTL/CMOS compatible input logic levels
- Short circuit protection
- High impedance input
- Externally set holding current, I_H
- Internally set peak current ($4 \times I_H$)
- Externally set time-out
- Can be modified for full switching operation
- Available in plastic 8-pin miniDIP

Applications

- Fuel injection
- Throttle body injection
- Solenoid controls
- Air and fluid valves
- DC motor drives

Typical Application Circuit

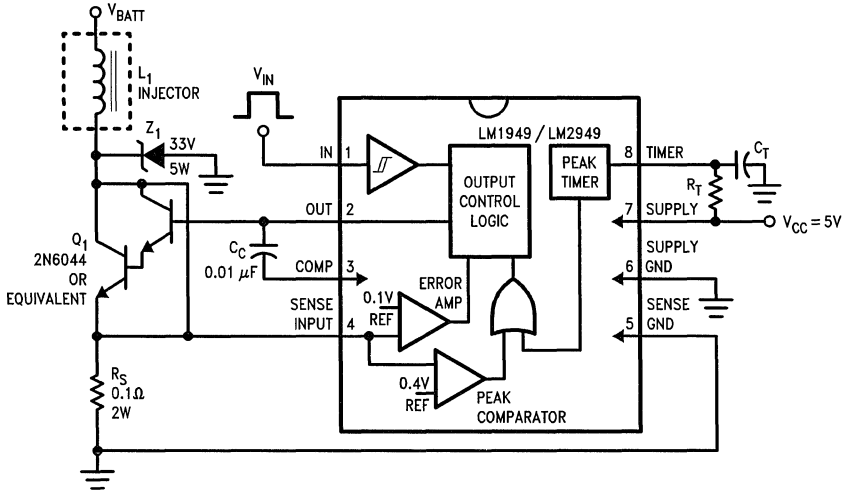

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FIGURE 1. Typical Application and Test Circuit

Order Number LM1949N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

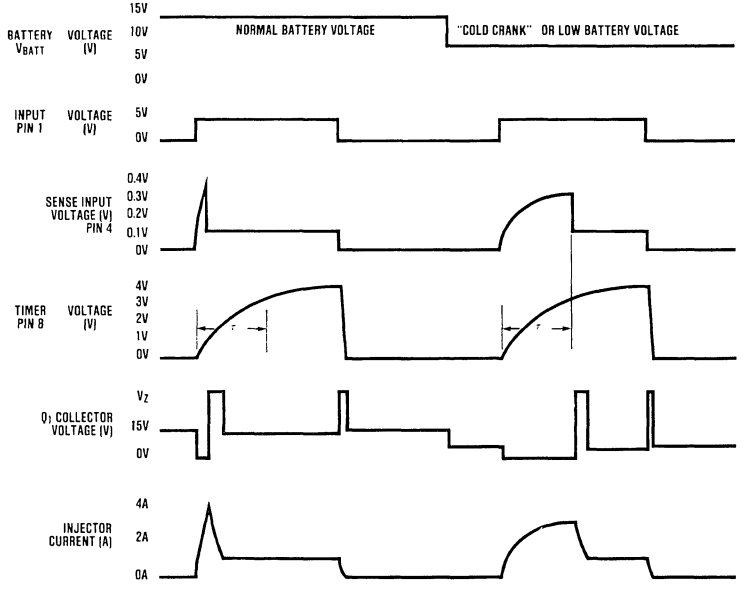
Supply Voltage	8V
Power Dissipation (Note 1)	1235 mW
Input Voltage Range	−0.3V to V_{CC}
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temp. (Soldering 10 sec.)	260°C

Electrical Characteristics (V_{CC} = 5.5V, V_{IN} = 2.4V, T_j = 25°C, *Figure 1*, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current					
	Off	V_{IN} = 0V		11	23	mA
	Peak	Pin 8 = 0V		28	54	mA
	Hold	Pin 8 Open		16	26	mA
V_{OH}	Input On Level	V_{CC} = 5.5V		1.4	2.4	V
		V_{CC} = 3.0V		1.2	1.6	V
V_{OL}	Input Off Level	V_{CC} = 5.5V	1.0	1.35		V
		V_{CC} = 3.0V	0.7	1.15		V
I_B	Input Current		−25	3	+25	μA
I_{OP}	Output Current					
	Peak	Pin 8 = 0V	−10	−22		mA
	Hold	Pin 8 Open	−1.5	−5		mA
V_S	Output Saturation Voltage	10 mA, V_{IN} = 0V		0.2	0.4	V
	Sense Input					
V_P	Peak Threshold	V_{CC} = 4.75V	350	386	415	mV
V_H	Hold Reference		88	94	102	mV
t	Time-out, t	$t \div R_T C_T$	90	100	110	%

NOTE 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 100°C/W junction to ambient.

Typical Circuit Waveforms



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Schematic Diagram

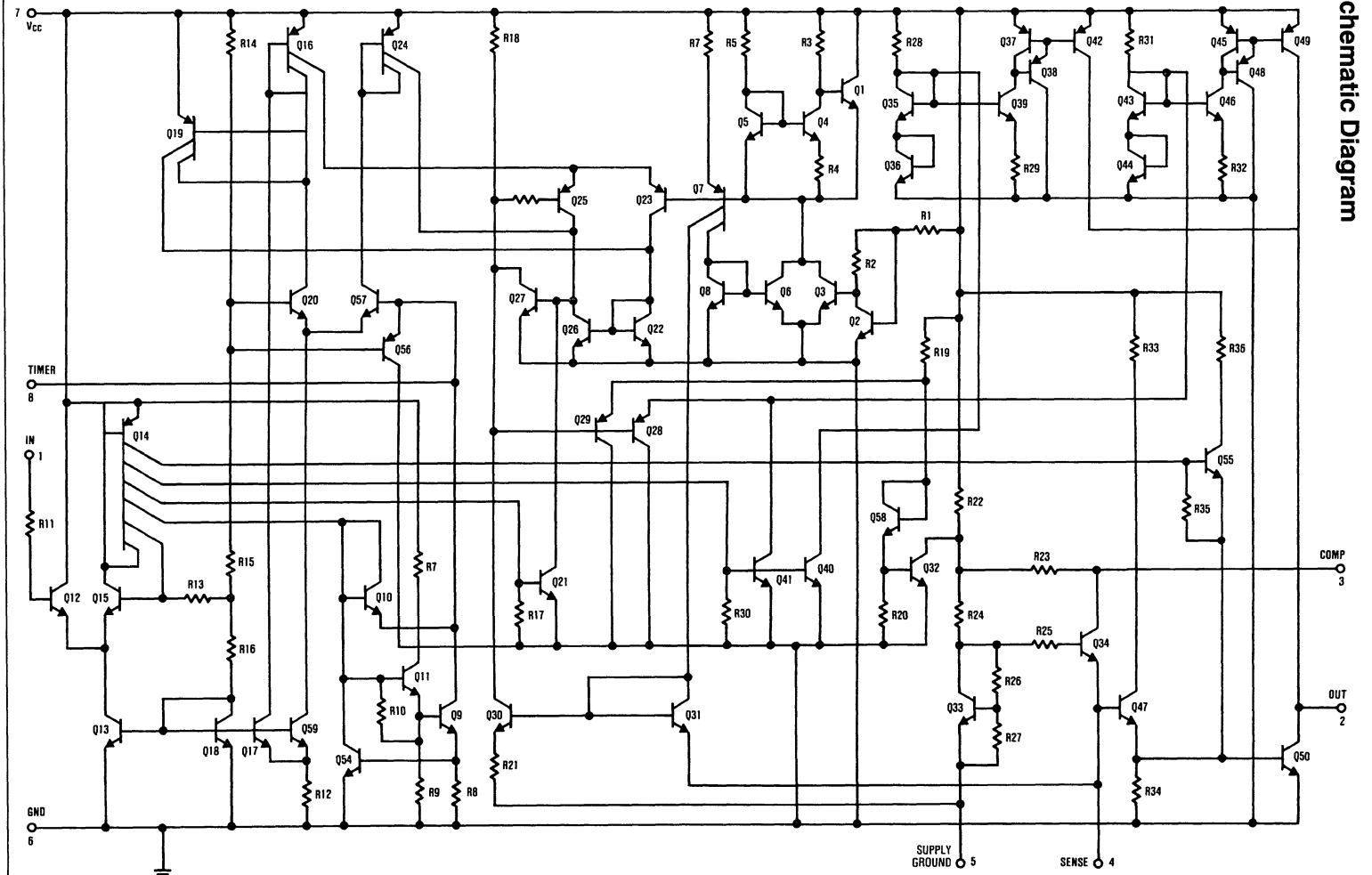

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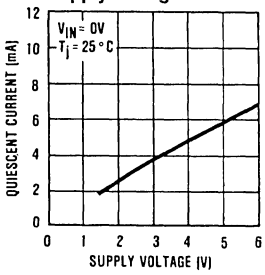
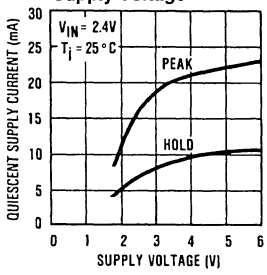
FIGURE 2. LM1949 Circuit

Typical Performance Characteristics

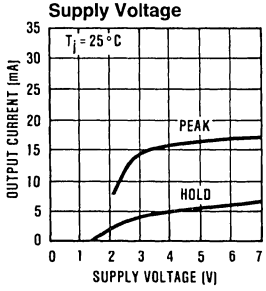
Quiescent Current vs Supply Voltage



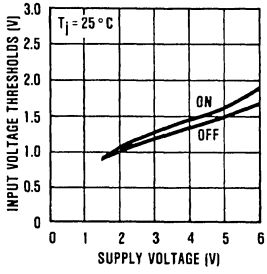
Supply Current vs Supply Voltage



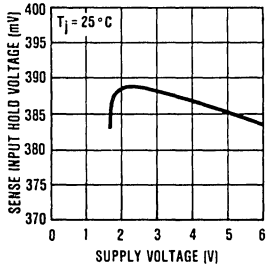
Output Current vs Supply Voltage



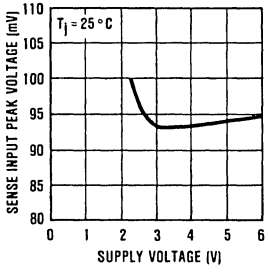
Input Voltage Thresholds vs Supply Voltage



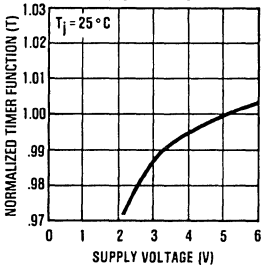
Sense Input Peak Voltage vs Supply Voltage



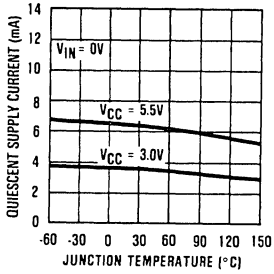
Sense Input Hold Voltage vs Supply Voltage



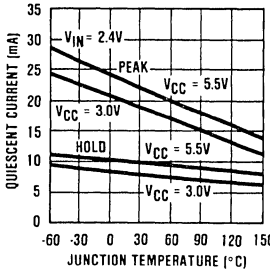
Normalized Timer Function vs Supply Voltage



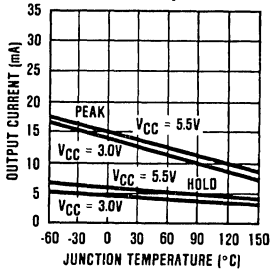
Quiescent Supply Current vs Junction Temperature



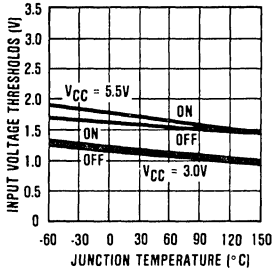
Quiescent Supply Current vs Junction Temperature



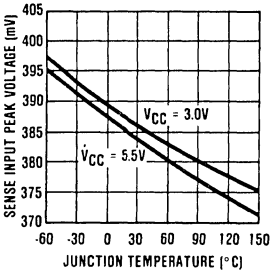
Output Current vs Junction Temperature



Input Voltage Thresholds vs Junction Temperature



Sense Input Peak Voltage vs Junction Temperature



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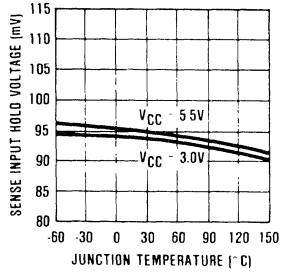
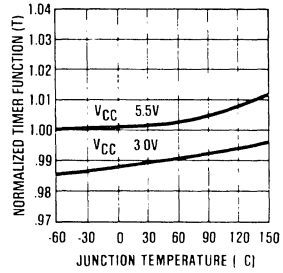
Typical Performance Characteristics (Continued)

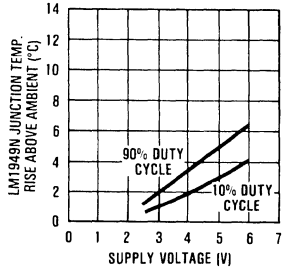
Sense Input Hold Voltage vs Junction Temperature



Normalized Timer Function vs Junction Temperature



LM1949N Junction Temperature Rise Above Ambient vs Supply Voltage



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Application Hints

The injector driver integrated circuits were designed to be used in conjunction with an external controller. The LM1949 derives its input signal from either a control oriented processor (COPS™), microprocessor, or some other system. This input signal, in the form of a square wave with a variable duty cycle and/or variable frequency, is applied to Pin 1. In a typical system, input frequency is proportional to engine RPM. Duty cycle is proportional to the engine load. The circuits discussed are suitable for use in either open or closed loop systems. In closed loop systems, the engine exhaust is monitored and the air-to-fuel mixture is varied (via the duty cycle) to maintain a perfect, or stochiometric, ratio.

INJECTORS

Injectors and solenoids are available in a vast array of sizes and characteristics. Therefore, it is necessary to be able to design a drive system to suit each type of solenoid. The purpose of this section is to enable any system designer to use and modify the LM1949 and associated circuitry to meet the system specifications.

Fuel injectors can usually be modeled by a simple RL circuit. *Figure 3* shows such a model for a typical fuel injector. In actual operation, the value of L_1 will depend upon the status of the solenoid. In other words, L_1 will change depending

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FIGURE 3. Model of a Typical Fuel Injector

upon whether the solenoid is open or closed. This effect, if pronounced enough, can be a valuable aid in determining the current necessary to open a particular type of injector. The change in inductance manifests itself as a breakpoint in the initial rise of solenoid current. The waveforms on Page 2 at the sense input show this occurring at approximately 130 mV. Thus, the current necessary to overcome the constrictive forces of that particular injector is 1.3 amperes.

PEAK AND HOLD CURRENTS

The peak and hold currents are determined by the value of the sense resistor R_S. The driver IC, when initiated by a logic 1 signal at Pin 1, initially drives Darlington transistor Q_1 into saturation. The injector current will rise exponentially from zero at a rate dependent upon L_1, R_1, the battery voltage and the saturation voltage of Q_1. The drop across the sense resistor is created by the solenoid current, and when this drop reaches the peak threshold level, typically 385 mV, the IC is tripped from the peak state into the hold state. The IC now behaves more as an op amp and drives Q_1 within a closed loop system to maintain the hold reference voltage, typically 94 mV, across R_S. Once the injector current drops from the peak level to the hold level, it remains there for the duration of the input signal at Pin 1. This mode of operation is preferable when working with solenoids, since the current required to overcome kinetic and constriction forces is often a factor of four or more times the current necessary to hold the injector open. By holding the injector current at one fourth of the peak current, power dissipation in the solenoids and Q_1 is reduced by at least the same factor.

In the circuit of *Figure 1*, it was known that the type of injector shown opens when the current exceeds 1.3 amps and closes when the current then falls below 0.3 amps. In order to guarantee injector operation over the life and temperature range of the system, a peak current of approximately 4 amps was chosen. This led to a value of R_S of 0.1Ω. Dividing the peak and hold thresholds by this factor gives peak and hold currents through the solenoid of 3.85 amps and 0.94 amps respectively.

Different types of solenoids may require different values of current. The sense resistor R_S may be changed accordingly. An 8-amp peak injector would use R_S equal to .05Ω, etc. Note that for large currents above one amp, IR drops within the component leads or printed circuit board may create substantial errors unless appropriate care is taken. The sense input and sense ground leads (Pins 4 and 5 respectively), should be Kelvin connected to R_S. High current should not be allowed to flow through any part of these traces or connections. An easy solution to this problem on double-sided PC boards (without plated-through holes) is to have the high current trace and sense trace attach to the R_S lead from opposite sides of the board.

TIMER FUNCTION

The purpose of the timer function is to limit the power dissipated by the injector or solenoid under certain conditions. Specifically, when the battery voltage is low due to engine cranking, or just undercharged, there may not be sufficient voltage available for the injector to achieve the peak current. In the *Figure 2* waveforms under the low battery condition, the injector current can be seen to be leveling out at 3

Timer Function (Continued)

amps, or 1 amp below the normal threshold. Since continuous operation at 3 amps may overheat the injectors, the timer function on the IC will force the transition into the hold state after one time constant (the time constant is equal to R_TC_T). The timer is reset at the end of each input pulse. For systems where the timer function is not needed, it can be disabled by grounding Pin 8. For systems where the initial peak state is not required, (i.e., where the solenoid current rises immediately to the hold level), the timer can be used to disable the peak function. This is done by setting the time constant equal to zero, (i.e., $C_T = 0$). Leaving R_T in place is recommended. The timer will then complete its time-out and disable the peak condition before the solenoid current has had a chance to rise above the hold level.

The actual range of the timer in injection systems will probably never vary much from the 3.9 milliseconds shown in *Figure 1*. However, the actual useful range of the timer extends from microseconds to seconds, depending on the component values chosen. The useful range of R_T is approximately 1k to 240k. The capacitor C_T is limited only by stray capacitances for low values and by leakages for large values.

The capacitor reset time at the end of each controller pulse is determined by the supply voltage and the capacitor value. The IC resets the capacitor to an initial voltage (V_{BE}) by discharging it with a current of approximately 15 mA. Thus, a 0.1 μF cap is reset in approximately 25 μs.

COMPENSATION

Compensation of the error amplifier provides stability for the circuit during the hold state. External compensation (from Pin 2 to Pin 3) allows each design to be tailored for the characteristics of the system and/or type of Darlington power device used. In the vast majority of designs, the value or type of the compensation capacitor is not critical. Values of 100 pF to 0.1 μF work well with the circuit of *Figure 1*. The value shown of .01 μF (disc) provides a close optimum in choice between economy, speed, and noise immunity. In some systems, increased phase and gain margin may be acquired by bypassing the collector of Q_1 to ground with an appropriately rated 0.1 μF capacitor. This is, however, rarely necessary.

FLYBACK ZENER

The purpose of zener Z_1 is twofold. Since the load is inductive, a voltage spike is produced at the collector of Q_1 anytime the injector current is reduced. This occurs at the peak-to-hold transition, (when the current is reduced to one fourth of its peak value), and also at the end of each input pulse, (when the current is reduced to zero). The zener provides a current path for the inductive kickback, limiting the voltage spike to the zener value and preventing Q_1 from damaging voltage levels. Thus, the rated zener voltage at the system peak current must be less than the guaranteed minimum breakdown of Q_1. Also, even while Z_1 is conducting the majority of the injector current during the peak-to-hold transition (see *Figure 4*), Q_1 is operating at the hold current level. This fact is easily overlooked and, as described in the following text, can be corrected if necessary. Since the error amplifier in the IC demands 94 mV across R_S, Q_1 will be biased to provide exactly that. Thus, the safe operating area (SOA) of Q_1 must include the hold current with a V_{CE} of Z_1 volts. For systems where this is not desired, the zener anode may be reconnected to the top of R_S as shown in *Figure 5*. Since the voltage across the sense resistor now accurately portrays the injector current at all times, the error

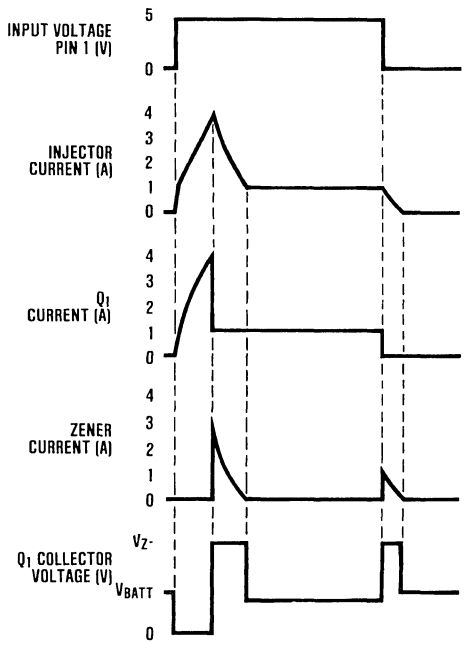

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FIGURE 4. Circuit Waveforms

amplifier keeps Q_1 off until the injector current has decayed to the proper value. The disadvantage of this particular configuration is that the ungrounded zener is more difficult to heat sink if that becomes necessary.

The second purpose of Z_1 is to provide system transient protection. Automotive systems are susceptible to a vast array of voltage transients on the battery line. Though their duration is usually only milliseconds long, Q_1 could suffer permanent damage unless buffered by the injector and Z_1. This is one reason why a zener is preferred over a clamp diode back to the battery line, the other reason being long decay times.

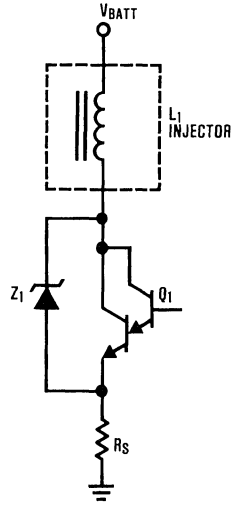

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FIGURE 5. Alternate Configuration for Zener Z_1

POWER DISSIPATION

The power dissipation of the system shown in *Figure 1* is dependent upon several external factors, including the frequency and duty cycle of the input waveform to Pin 1. Calculations are made more difficult since there are many discontinuities and breakpoints in the power waveforms of the various components, most notably at the peak-to-hold transition. Some generalizations can be made for normal operation. For example, in a typical cycle of operation, the majority of dissipation occurs during the hold state. The hold state is usually much longer than the peak state, and in the peak state nearly all power is stored as energy in the magnetic field of the injector, later to be dumped mostly through the zener. While this assumption is less accurate in the case of low battery voltage, it nevertheless gives an unexpectedly accurate set of approximations for general operation.

The following nomenclature refers to *Figure 1*. Typical values are given in parentheses:

R_S = Sense Resistor (0.1Ω)
V_H = Sense Input Hold Voltage (.094V)
V_p = Sense Input Peak Voltage (.385V)
V_Z = Z_1 Zener Breakdown Voltage (33V)
V_{BATT} = Battery Voltage (14V)
L_1 = Injector Inductance (.002H)
R_1 = Injector Resistance (1Ω)
n = Duty Cycle of Input Voltage of Pin 1 (0 to 1)
f = Frequency of Input (10Hz to 200Hz)

Q_1 Power Dissipation:

$$P_Q \approx n \bullet V_{BATT} \bullet \frac{V_H}{R_S} \text{ Watts}$$

Zener Dissipation:

$$P_Z \approx V_Z \bullet L_1 \bullet f \bullet \frac{(V_P^2 + V_H^2)}{((V_Z - V_{BATT}) \bullet R_S^2)} \text{ Watts}$$

Injector Dissipation:

$$P_I \approx n \bullet R_1 \bullet \frac{V_H^2}{R_S^2} \text{ Watts}$$

Sense Resistor:

$$P_R \approx n \frac{V_H^2}{R_S^2} \text{ Watts}$$

$$P_R \text{ (worst case)} \approx n \frac{V_P^2}{R_S^2} \text{ Watts}$$

SWITCHING INJECTOR DRIVER CIRCUIT

The power dissipation of the system, and especially of Q_1, can be reduced by employing a switching injector driver circuit. Since the injector load is mainly inductive, transistor Q_1 can be rapidly switched on and off in a manner similar to switching regulators. The solenoid inductance will naturally integrate the voltage to produce the required injector current, while the power consumed by Q_1 will be reduced. A note of caution: The large amplitude switching voltages that are present on the injector can and do generate a tremendous amount of radio frequency interference (RFI). Because of this, switching circuits are not recommended. The extra cost of shielding can easily exceed the savings of reduced power. In systems where switching circuits are mandatory, extensive field testing is required to guarantee that RFI cannot create problems with engine control or entertainment equipment within the vicinity.

The LM1949 can be easily modified to function as a switcher. Accomplished with the circuit of *Figure 7*, the only additional components required are two external resistors, R_A and R_B. Additionally, the zener needs to be reconnected, as shown, to R_S. The amount of ripple on the hold current is easily controlled by the resistor ratio of R_A to R_B. R_B is kept small so that sense input bias current (typically 0.3 mA) has negligible effect on V_H. Duty cycle and frequency of oscillation during the hold state are dependent on the injector characteristics, R_A, R_B, and the zener voltage as shown in the following equations.

$$\text{Hold Current} \approx \frac{V_H}{R_S}$$

$$\text{Minimum Hold Current} \approx \frac{\left(V_H - \frac{R_B}{R_A} \bullet V_Z\right)}{R_S}$$

$$\text{Ripple or } \Delta I \text{ Hold} \approx \frac{R_B}{R_A} \bullet V_Z \bullet \frac{1}{R_S}$$

$$f_o \approx \frac{R_S}{L_1} \bullet \frac{R_A}{R_B} \bullet \frac{V_{BATT}}{V_Z} \bullet \left(1 - \frac{V_{BATT}}{V_Z}\right)$$

f_o = Hold State Oscillation Frequency

$$\text{Duty Cycle of } f_o \approx \frac{V_{BATT}}{V_Z}$$

Component Power Dissipation

$$P_Q \approx n \bullet \left(1 - \frac{V_{BATT}}{V_Z}\right) \bullet \frac{V_{SAT}}{R_S} \bullet V_H$$

V_{SAT} = Q_1 Saturation Volt @ ~ 1 Amp (1.5V)

$$P_Z \approx n \bullet \frac{V_{BATT} \bullet V_H}{R_S}$$

$$P_{RA} \approx \frac{V_B \bullet V_Z}{R_1}$$

As shown, the power dissipation by Q_1 in this manner is substantially reduced. Measurements made with a thermocouple on the bench indicated better than a fourfold reduction in power in Q_1. However, the power dissipation of the zener (which is independent of the zener voltage chosen) is increased over the circuit of *Figure 1*.

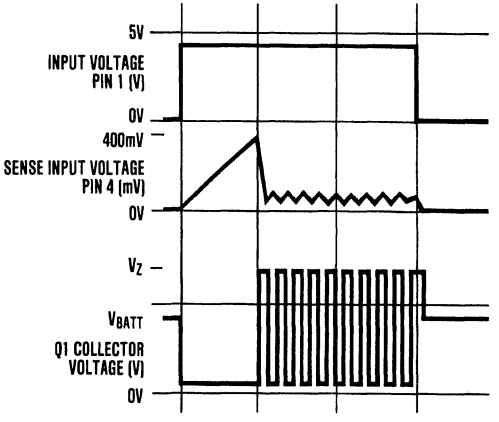

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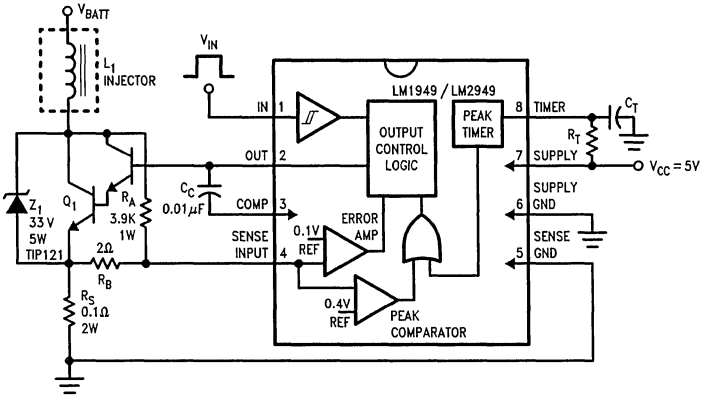
FIGURE 6. Switching Waveforms



TL/H/5062–10

FIGURE 7. Switching Application Circuit

National Semiconductor Corporation

PRELIMINARY

LM1951 Solid State 1 Amp Switch

General Description

The LM1951 is a high current, high voltage high side (PNP) switch with a built-in error detection circuit.

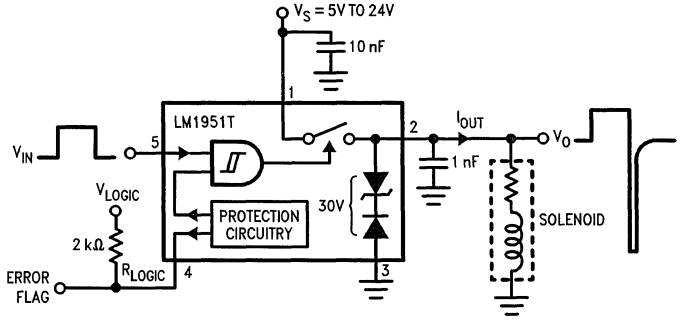
The LM1951 is guaranteed to deliver 1 Amp output current and is capable of withstanding up to ±85V transients. The built-in error detection provides an error flag output under the following fault conditions: output short to ground or supply, open load, current limit, overvoltage or thermal shutdown. The LM1951 will drive all types of resistive or inductive loads. The output has a built-in negative voltage clamp (≈ −30V) to provide a quick energy discharge path for inductive loads. The LM1951 features TTL and CMOS compatible logic input with hysteresis. Switching times, both turn on and turn off, are 2 μs (C_{load} < 0.005 μF). In addition, its quiescent current in the OFF state is typically less than 0.1 μA at room temperature and less than 10 μA over the entire operating temperature and voltage range.

The LM1951 features make it well suited for industrial and automotive applications.

Features

- 0.1 μA typical quiescent current (OFF state)
- 1.1 Amp output current
- ±85V supply voltage transients
- Reverse voltage protection
- Negative output voltage clamp
- Error flag output
- Internal overvoltage shutdown
- Internal thermal shutdown
- Short circuit proof
- High speed switching (up to 50 kHz)
- Inductive or resistive loads
- Low ON resistance (1Ω maximum)
- TTL, CMOS compatible input with hysteresis
- Plastic TO-220 5-lead package
- ESD protected
- 4.5V to 26V operation

Typical Application Circuit and Connection Diagram



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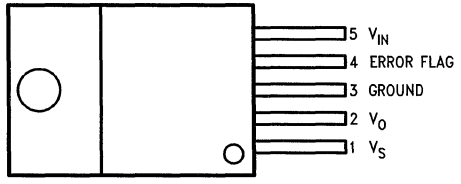
V_{IN}	Output
0	OFF
1	ON

5-Lead TO-220



TL/H/9133–2

Order Number LM1951T
See NS Package Number T05A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage
- Operational Voltage: 26 V_{DC}
- Sustained Voltage: $-40\ V_{DC} \geq V_S \leq 85\ V_{DC}$
- Transient Voltage Protection: ±85V
  (τ = 100 ms, 1% Duty Cycle, $R_S \geq 10\Omega$)
- Pins 4, 5: 26 V_{DC}

Power Dissipation (Note 1): Internally Limited

Load Inductance: 1H

Operating Temperature Range (T_A): −40°C to +125°C

Maximum Junction Temperature: 150°C

Storage Temperature Range: −65°C to +150°C

Lead Temperature (Soldering, 10 sec.): 230°C

ESD Tolerance (Note 4): 2000V
(C_{zap} = 100 pF, R_{zap} = 1500Ω)

Electrical Characteristics

V_S = 12V, I_{out} = 500 mA, C_{out} = 0.001 μF, T_A = 25°C unless otherwise specified

Parameter	Conditions		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Supply Voltage				4.5		V_{min}
Operational				26		V_{max}
Transient	τ = 100 ms, 1% Duty Cycle, $R_S \geq 10\Omega$			−85		V
				85		V
Supply Current	I_{out} = 0 mA, V_{in} = 0.8V		0.1	10	100	μA_{max}
	I_{out} = 250 mA, V_{in} = 2.0V		260	270		mA_{max}
	I_{out} = 600 mA, V_{in} = 2.0V		630	650		mA_{max}
	I_{out} = 1A, V_{in} = 2.0V		1.06	1.2		A_{max}
Voltage Drop ($V_S - V_O$)	I_{out} = 600 mA, V_{in} = 2.0V		400	600		mV_{max}
	I_{out} = 1A, V_{in} = 2.0V		0.7	1.0		V
Short Circuit Current			1.3	1.0		A_{min}
				2.5		A_{max}
Input Threshold	4.5V ≤ V_S ≤ 26V	Turn ON	1.4	2.0	2.0	V_{max}
		Turn OFF	1.2	0.8	0.8	V_{min}
Input Current	0.8V ≤ V_{in} ≤ 5.5V		25	50		μA_{max}
				10		μA_{min}
Output Clamp	I_{out} ≤ 600 mA		−30	−40		V_{min}
				−24		V_{max}
Delay Time t_d, ON	R_{load} = 20Ω, C_{load} = 0.001 μF		1	3		μs_{max}
t_d, OFF			1	3		μs_{max}
Rise Time			1	3		μs_{max}
Fall Time			1	3		μs_{max}
Error Flag Characteristics						
Output Voltage	Error Condition, Pin 5 Low, Sinking 10 mA		0.3	0.8		V_{max}
Sink Current	Error Condition, Pin 5 = 0.3V		10	3		mA_{min}
Output Leakage Current	No Error, Pin 5 = 26V		0.01	1		μA
Response Time	V_{LOGIC} = 5V, R_{LOGIC} = 2 kΩ, C_{LOGIC} = 0 μF		1			μs

Note 1: Thermal resistance without a heatsink for junction-to-case temperature is 3°C/W. Thermal resistance case-to-ambient is 50°C/W.

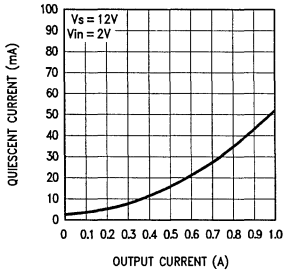
Note 2: Tested Limits are guaranteed and 100% production tested.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the operating temperature and supply voltage range. These limits are not used to calculate outgoing quality levels.

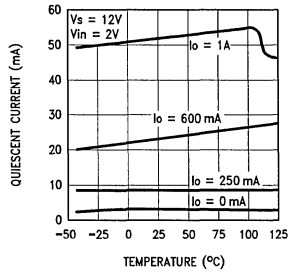
Note 4: ESD testing performed per SOP-5-028 requirements.

Typical Performance Characteristics

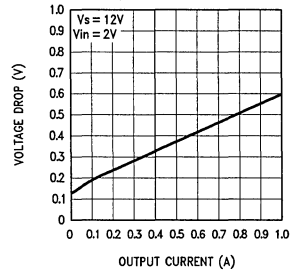
Quiescent Current



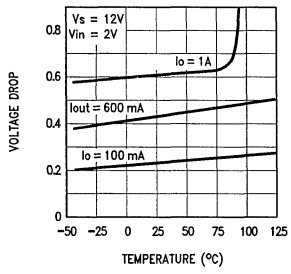
Quiescent Current



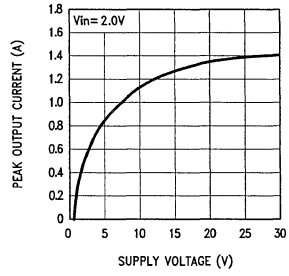
Voltage Drop



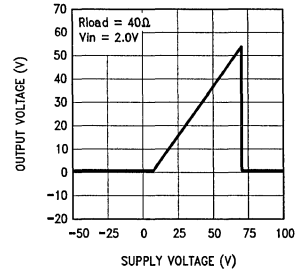
Voltage Drop



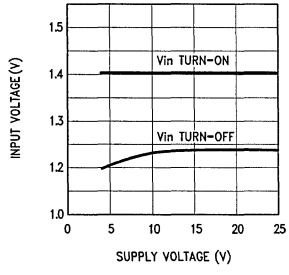
Peak Output Current



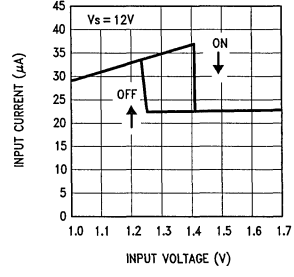
High Voltage Behavior



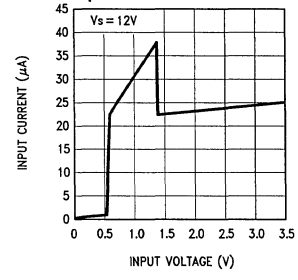
Input Threshold



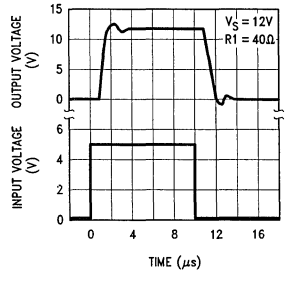
Input Current



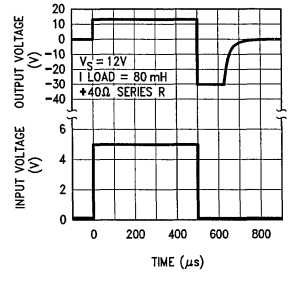
Input Current



Output Voltage
Resistive Load



Output Voltage
Inductive Load



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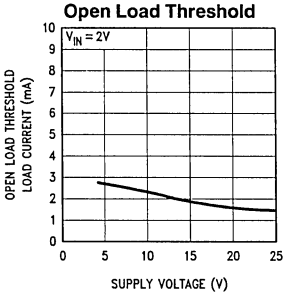
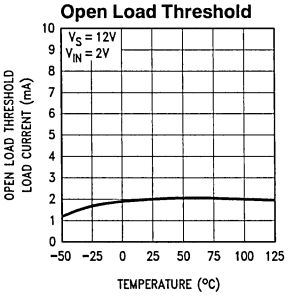
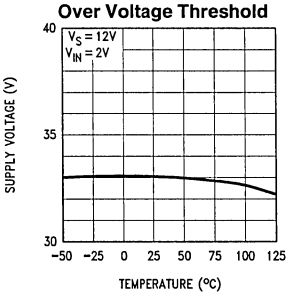
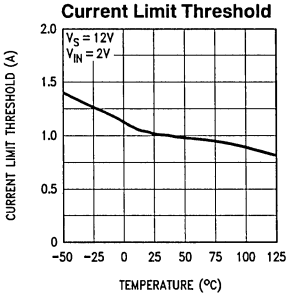
Error Flag Output Characteristics









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Truth Table

Fault Condition	V_{in}*	V_{out}	Error Flag
Normal	0	0	1
	1	1	1
Overvoltage	0	0	0
	1	0	0
Thermal Shutdown	0	0	0
	1	0	0
V_O Short to GND	0	0	1
	1	0	0
V_O Short to V_{supply}	0	1	0
	1	1	0
Open Load	0	0	1
	1	1	0
Current Limit	0	0	1
	1	1	0

* $0 \cong 0 \leq V_{in} \leq 0.8V$ $\quad 1 \cong 2V \leq V_{in} \leq 26V$

Typical Applications

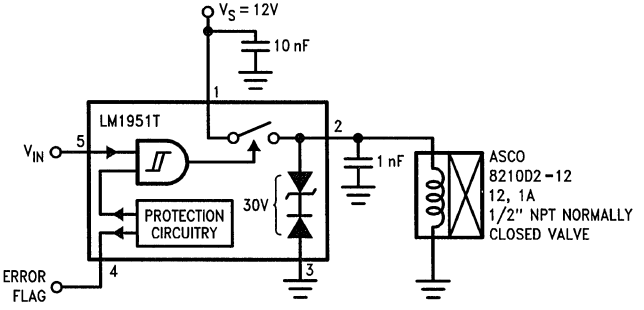

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FIGURE 1. Solenoid Actuated Valve

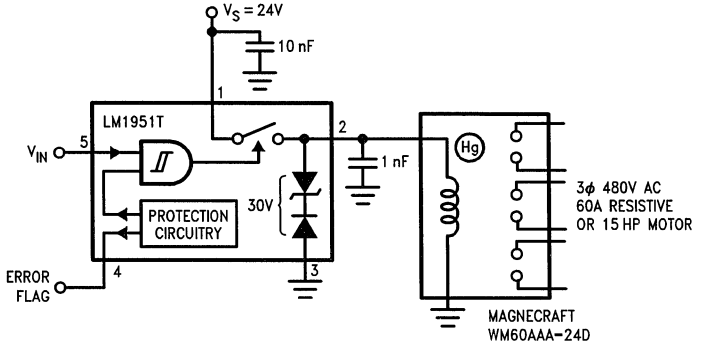

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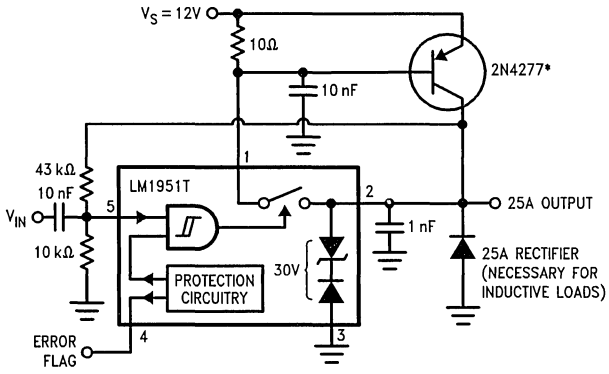
FIGURE 2. 60A 3-Phase Mercury Displacement Relay

Typical Applications (Continued)



TL/H/9133–6

*Available from Germanium Power Devices, Andover, MA, Tel. (617) 475-5982

FIGURE 3. 25A Switch with Short Circuit Foldback

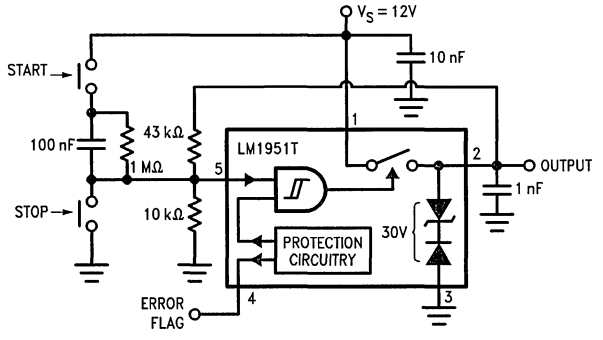


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FIGURE 4. Latching Switch

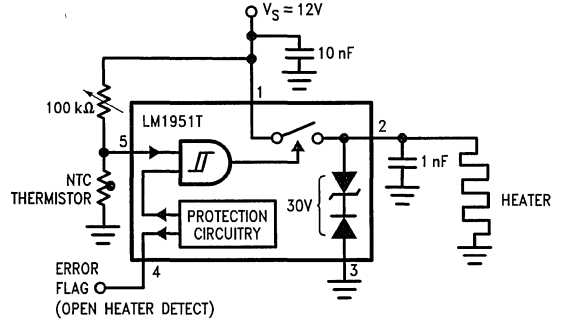

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FIGURE 5. Proportional Temperature Controller with Hysteresis

5

Typical Applications (Continued)

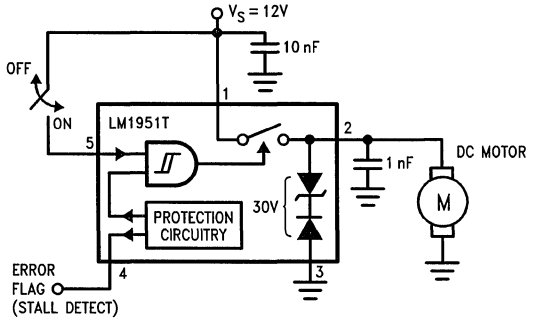

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FIGURE 6. DC Motor Driver

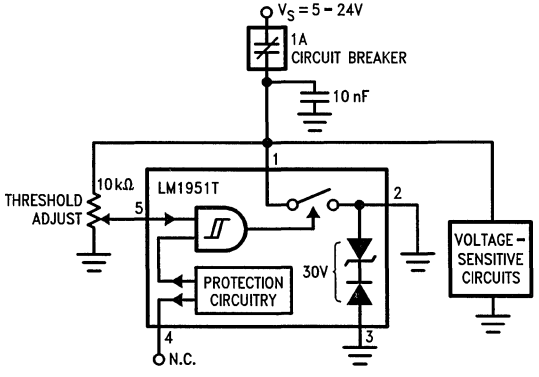

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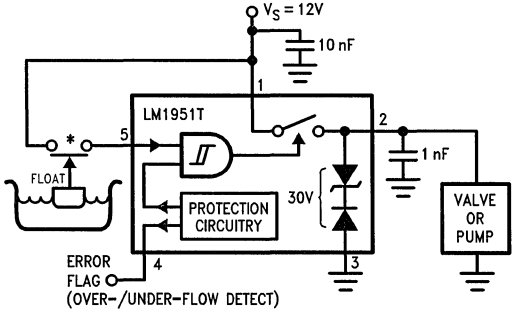
FIGURE 7. Over-Voltage Crowbar



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*

Operation	Switch Type
Empty	Normally Open
Fill	Normally Closed

FIGURE 8. Fluid Level Controller

Typical Applications (Continued)

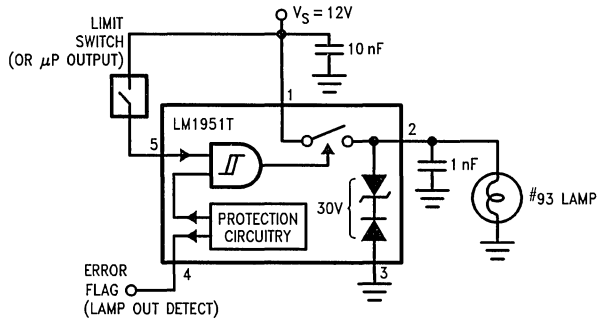


FIGURE 9. Indicator Lamp Driver

Application Hints

When inductive loads are turned OFF, they produce a negative voltage spike. The LM1951 contains a voltage clamp that limits these spikes to approximately −30V, thus an external clamp is not necessary in most applications.

Loads with an inductance of greater than 1H, driven to full output current, may damage the clamp simply by exceeding the power capabilities of the LM1951. An LM1951 can dissipate 25W continuous at 25°C ambient when mounted on a large heatsink. If the load current is limited to 800 mA, the sustained spike from an infinitely large inductance can be handled. Sustained spikes produced by higher currents and high inductances will exceed the 25W limit.

For inductances above 1H, care should be taken to see that the output current does not exceed a value that could damage the clamp. While 800 mA is acceptable for the device running at 25°C ambient on a heatsink, derate this current for smaller heatsinks or higher ambient temperatures to limit the junction temperature to 125°C. Alternatively, an external clamp or resonating capacitor can be added to handle any combination of load inductance, load current, and device temperature. This is especially important if the output current is boosted, such as the application shown in *Figure 3*. A peak power of 750W could be developed in the internal clamp if an inductive load is switched without external clamping.

Another case where the clamp's power capability may be exceeded is when driving a solenoid. The inductance of a solenoid is greatest when energized, with the plunger pulled in. As the plunger is pulled out of the solenoid, the inductance goes down. Under certain conditions of high solenoid inductance and fast mechanical time constants, the current may actually **increase** when the solenoid is turned OFF. Since the energy stored in an inductor cannot change instantaneously, the current must increase to conserve energy when the inductance decreases. This condition is traced by observing the load current with a current probe and storage oscilloscope.

Load capacitances larger than 1 nF will slow rise and fall times. Inductive loads having a capacitive component larger than 1 nF will also exhibit overshoot. Furthermore, ringing may be evident in a combination inductive/capacitive load, or in an inductive load with supply decoupling capacitors in the range of 100 nF to 1 μF. For fast rise and fall times and minimum ringing with inductive loads, a supply decoupling capacitor of 10 nF and an output capacitor of 1 nF is recommended. These should be located as close to the IC pins as possible.

The error flag is an open collector output that pulls low under certain fault conditions. These errors include overvoltage (V_S > 26V), overcurrent (I_{OUT} > 1.3A), undercurrent (I_{OUT} < 2 mA), output short circuit to ground, output short circuit to supply, and junction temperature greater than 150°C. By connecting a 2 kΩ resistor from the error flag output to a 5V supply a logic output to a microprocessor is provided.

The error flag can give seemingly false indications in a number of situations. Slewing large capacitive loads (>100 nF) can drive the LM1951 into temporary current limit, producing a momentary error indication. Incandescent lamps and DC motors require an inrush current that will also cause a temporary current limit and error indication. Large inductive loads (>50 mH) initially appear as open circuits, falsing the error flag. The error flag pulses for about 1 μs when any load is turned ON since the output is initially at ground. In microprocessor systems these false indications are easily ignored in software. In discrete logic circuits utilizing a latch at the error flag output, some filtering may be required.

An internal current sink (10 μA minimum) is connected to the input, pin 5. If this pin is left open it is guaranteed to pull low, switching the LM1951 OFF. This characteristic is important under certain fault conditions such as when the control line fails open cirucit.

Although the input threshold has hysteresis, the switch points are derived from a very stable band-gap reference. In many applications, such as *Figures 5* and *7*, the LM1951 input can replace an extenal reference and comparator.

The input (pin 5) is clamped at −0.7V and includes a series resistance of approximately 30 kΩ. This pin tolerates negative inputs of up to 1 mA without affecting the performance of the chip.

National Semiconductor Corporation

LM1964 Sensor Interface Amplifier

General Description

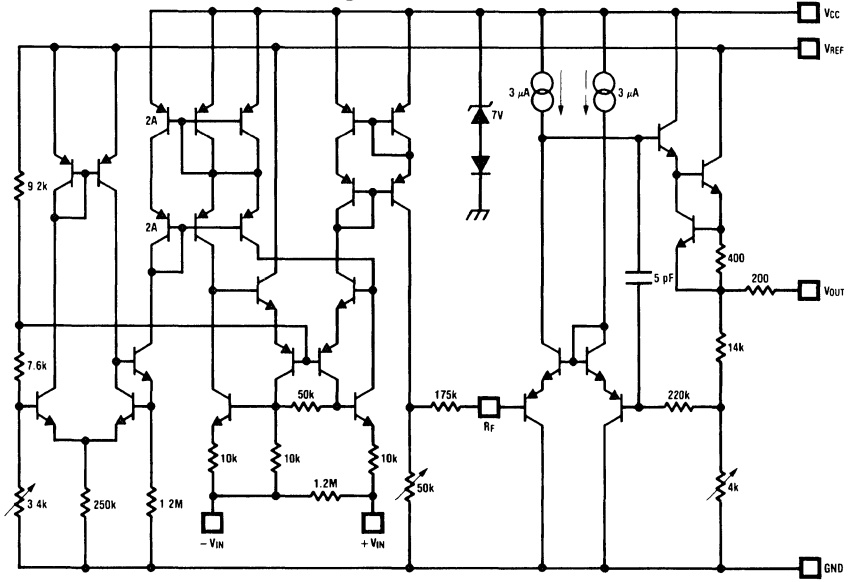
The LM1964 is a precision differential amplifier specifically designed for operation in the automotive environment. Gain accuracy is guaranteed over the entire automotive temperature range (−40°C to +125°C) and is factory trimmed prior to package assembly. The input circuitry has been specifically designed to reject common-mode signals as much as 3V below ground on a single positive power supply. This facilitates the use of sensors which are grounded at the engine block while the LM1964 itself is grounded at chassis potential. An external capacitor sets the maximum operating frequency of the amplifier, thereby filtering high frequency transients. Both inputs are protected against accidental shorting to the battery and against load dump transients. The input impedance is typically 1 MΩ.

The output op amp is capable of driving capacitive loads and is fully protected. Also, internal circuitry has been provided to detect open circuit conditions on either or both inputs and force the output to a "home" position (a ratio of the external reference voltage).

Features

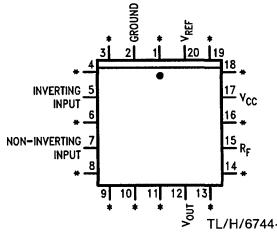
- Normal circuit operation guaranteed with inputs up to 3V below ground on a single supply
- Gain factory trimmed and guaranteed over temperature (±3% of full-scale from −40°C to +125°C)
- Low power consumption (typically 1 mA)
- Fully protected inputs
- Input open circuit detection
- Operation guaranteed over the entire automotive temperature range (−40°C to +125°C)
- Single supply operation

Schematic and Connection Diagrams



TL/H/6744-1

Plastic Chip Carrier Package



TL/H/6744-6

Top View

Order Number LM1964V
See NS Package Number V20A

*Pins 1, 3, 4, 6, 8, 9, 10, 11, 13, 14, 16, 18, 19 are trim pins and should be left floating.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} Supply Voltage (RV_{CC} = 15 kΩ)	±60V
V_{REF} Supply Voltage	−0.3V to +6V
DC Input Voltage (Either Input)	−3V to +16V
Input Transients (Note 1)	±60V
Power Dissipation (see Note 6)	1350 mW
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Plastic Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics V_{CC} = 12V, V_{REF} = 5V, T_A = 25°C unless otherwise noted

Parameter	Conditions	(Note 2)			(Note 3)			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain	V_{DIF} = 0.5V −1V ≤ V_{CM} ≤ +1V	4.41	4.50	4.59				V/V
	V_{DIF} = 0.5V, −40°C ≤ T_A ≤ 125°C −3V ≤ V_{CM} ≤ +1V				4.36	4.50	4.64	V/V
Gain Error (Note 5)	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V	−2	0	2				%/FS
	0 ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A ≤ +125°C				−3	0	3	%/FS
Differential Input Resistance	o ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V	1.00	1.20					MΩ
	0 ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A + 125°C				0.70	1.20		MΩ
Non-Inverting Input Bias Current	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V		0.3	1.0				μA
	0 ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A ≤ +125°C					0.3	1.5	μA
Inverting Input Bias Current	0 ≤ V_{DIF} ≤ 1V −1V ≤ V_{CM} ≤ +1V		45	100				μA
	0V ≤ V_{DIF} ≤ 1V −3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A ≤ +125°C					45	150	μA
V_{CC} Supply Current	V_{CC} = 12V, RV_{CC} = 15k		300	500				μA
V_{REF} Supply Current	4.75V ≤ V_{REF} ≤ 5.5V		0.5	1.0				mA
Common-Mode Voltage Range (Note 4)	−40°C ≤ T_A ≤ +125°C	−1		1	−3		1	V
DC Common-Mode Rejection Ratio	Input Referred −1V ≤ V_{CM} ≤ +1V V_{DIF} = 0.5V	50	60					dB
Open Circuit Output Voltage	One or Both Inputs Open, −1V ≤ V_{CM} ≤ +1V	0.371	0.397	0.423				XV_{REF}
	−3V ≤ V_{CM} ≤ +1V −40°C ≤ T_A ≤ +125°C				0.365	0.397	0.429	XV_{REF}
Short Circuit Output Current	Output Grounded	1.0	2.7	5.0				mA
V_{CC} Power Supply Rejection Ratio	V_{CC} = 12V, RV_{CC} = 15K V_{DIF} = 0.5V	50	65					dB
V_{REF} Power Supply Rejection Ratio	V_{REF} = 5 V_{DC} V_{DIF} = 0.5V	60	74					dB

Note 1: This test is performed with a 1000Ω source impedance.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: These parameters will be guaranteed but not 100% production tested.

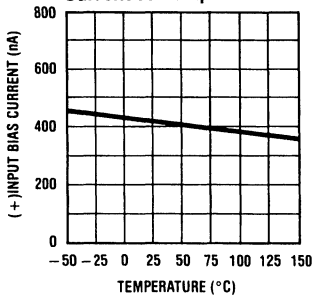
Note 4: The LM1964 has been designed to common-mode to −3V, but production testing is only performed at ±1V.

Note 5: Gain error is given as a percent of full-scale. Full-scale is defined as 1V at the input and 4.5V at the output.

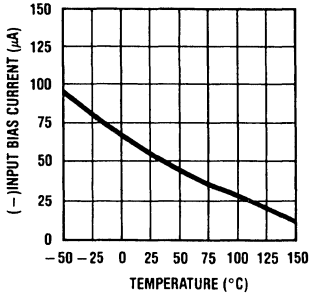
Note 6: For operation in ambient temperatures above 25°C the device must be derated based on a maximum junction temperature of 150°C and a thermal resistance of 93°C/W junction to ambient.

Typical Performance Characteristics

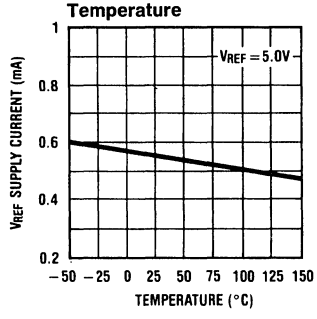
Non-Inverting Input Bias Current vs Temperature



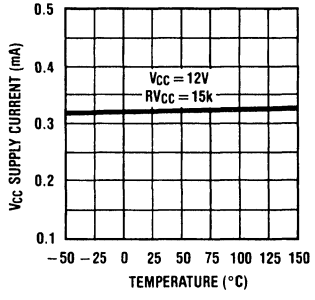
Inverting Input Bias Current vs Temperature



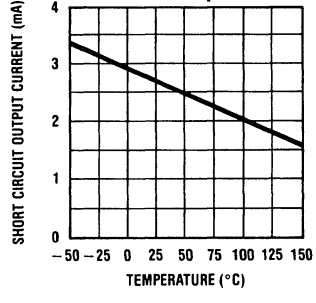
V_{REF} Supply Current vs Temperature



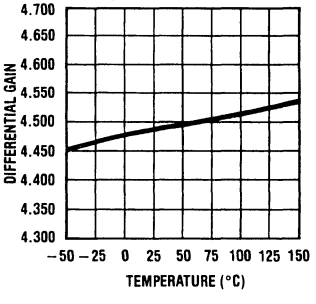
V_{CC} Supply Current vs Temperature



Short Circuit Output Current vs Temperature



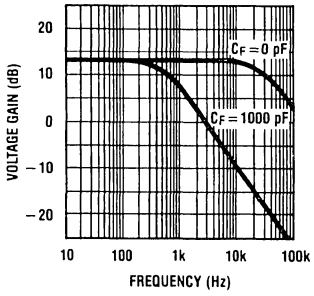
Differential Gain vs Temperature



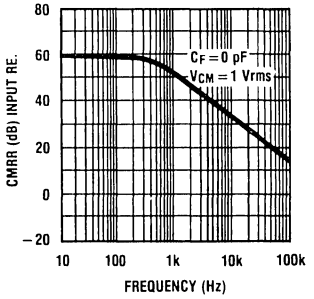
TL/H/6744–3

Typical Performance Characteristics (Continued)

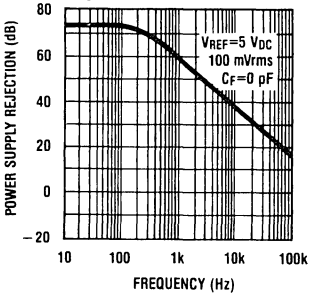
Voltage Gain vs Frequency



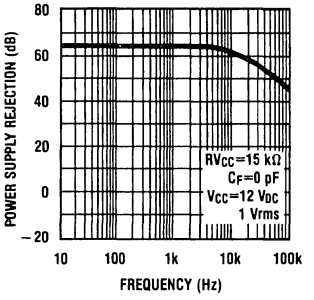
CMRR vs Frequency



V_{REF} Power Supply Rejection

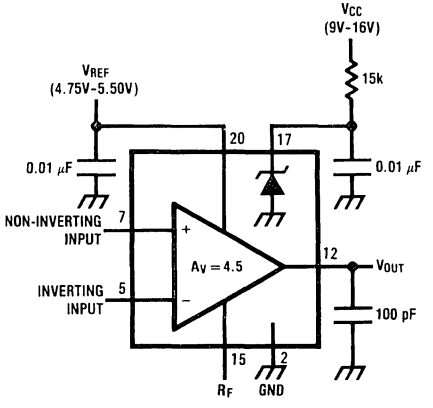


V_{CC} Power Supply Rejection



TL/H/6744–4

Test Circuit



TL/H/6744–5

National Semiconductor Corporation

LM2907/LM2917 Frequency to Voltage Converter

General Description

The LM2907, LM2917 series are monolithic frequency to voltage converters with a high gain op amp/comparator designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The tachometer uses a charge pump technique and offers frequency doubling for low ripple, full input protection in two versions (LM2907-8, LM2917-8) and its output swings to ground for a zero frequency input.

Advantages

- Output swings to ground for zero frequency input
- Easy to use; $V_{OUT} = f_{IN} \times V_{CC} \times R1 \times C1$
- Only one RC network provides frequency doubling
- Zener regulator on chip allows accurate and stable frequency to voltage or current conversion (LM2917)

Features

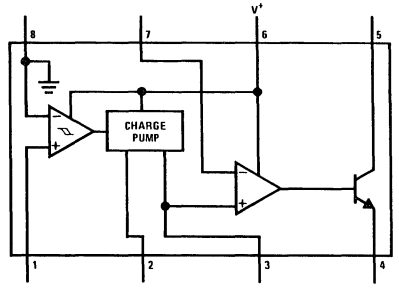
- Ground referenced tachometer input interfaces directly with variable reluctance magnetic pickups
- Op amp/comparator has floating transistor output
- 50 mA sink or source to operate relays, solenoids, meters, or LEDs
- Frequency doubling for low ripple
- Tachometer has built-in hysteresis with either differential input or ground referenced input
- Built-in zener on LM2917
- ±0.3% linearity typical
- Ground referenced tachometer is fully protected from damage due to swings above V_{CC} and below ground

Applications

- Over/under speed sensing
- Frequency to voltage conversion (tachometer)
- Speedometers
- Breaker point dwell meters
- Hand-held tachometer
- Speed governors
- Cruise control
- Automotive door lock control
- Clutch control
- Horn control
- Touch or sound switches

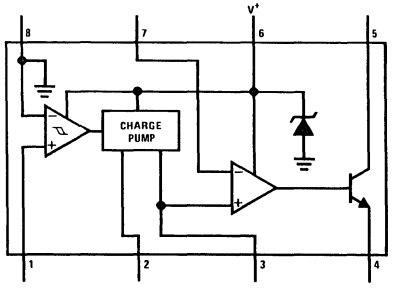
Block and Connection Diagrams

Dual-In-Line and Small Outline Packages, Top Views



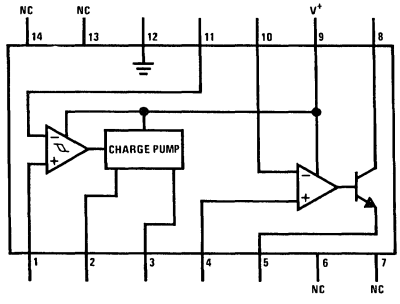
TL/H/7942–1

Order Number LM2907N-8
See NS Package Number N08E



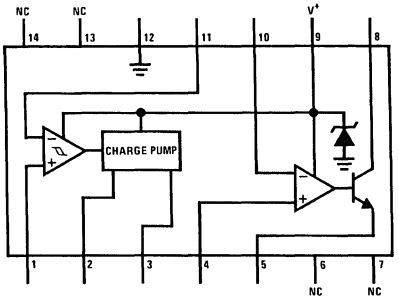
TL/H/7942–2

Order Number LM2917N-8
See NS Package Number N08E



TL/H/7942–3

Order Number LM2907N
See NS Package Number N14A



TL/H/7942–4

Order Number LM2917M or LM2917N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	28V
Supply Current (Zener Options)	25 mA
Collector Voltage	28V
Differential Input Voltage	
Tachometer	28V
Op Amp/Comparator	28V
Input Voltage Range	
Tachometer LM2907-8, LM2917-8	±28V
LM2907, LM2917	0.0V to +28V
Op Amp/Comparator	0.0V to +28V
Power Dissipation	
LM2907-8, LM2917-8	1200 mW
LM2907-14, LM2917-14 (See Note 1)	1580 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TACHOMETER						
	Input Thresholds	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)	±10	±25	±40	mV
	Hysteresis	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)		30		mV
	Offset Voltage	V_{IN} = 250 mVp-p @ 1 kHz (Note 2)				
	LM2907/LM2917			3.5	10	mV
	LM2907-8/LM2917-8			5	15	mV
	Input Bias Current	V_{IN} = ±50 mV_{DC}		0.1	1	μA
V_{OH}	Pin 2	V_{IN} = +125 mV_{DC} (Note 3)		8.3		V
V_{OL}	Pin 2	V_{IN} = −125 mV_{DC} (Note 3)		2.3		V
I_2, I_3	Output Current	V2 = V3 = 6.0V (Note 4)	140	180	240	μA
I_3	Leakage Current	I2 = 0, V3 = 0			0.1	μA
K	Gain Constant	(Note 3)	0.9	1.0	1.1	
	Linearity	f_{IN} = 1 kHz, 5 kHz, 10 kHz (Note 5)	−1.0	0.3	+1.0	%
OP/AMP COMPARATOR						
V_{OS}		V_{IN} = 6.0V		3	10	mV
I_{BIAS}		V_{IN} = 6.0V		50	500	nA
	Input Common-Mode Voltage		0		V_{CC}−1.5V	V
	Voltage Gain			200		V/mV
	Output Sink Current	V_C = 1.0	40	50		mA
	Output Source Current	V_E = V_{CC} −2.0		10		mA
	Saturation Voltage	I_{SINK} = 5 mA		0.1	0.5	V
		I_{SINK} = 20 mA			1.0	V
		I_{SINK} = 50 mA		1.0	1.5	V

Electrical Characteristics V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ZENER REGULATOR						
	Regulator Voltage	R_{DROP} = 470Ω		7.56		V
	Series Resistance			10.5	15	Ω
	Temperature Stability			+1		mV/°C
	TOTAL SUPPLY CURRENT			3.8	6	mA

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 101°C/W junction to ambient for LM2907-8 and LM2917-8, and 79°C/W junction to ambient for LM2907-14 and LM2917-14.

Note 2: Hysteresis is the sum $+V_{TH} - (-V_{TH})$, offset voltage is their difference. See test circuit.

Note 3: V_{OH} is equal to $\frac{3}{4} \times V_{CC} - 1\ V_{BE}$, V_{OL} is equal to $\frac{1}{4} \times V_{CC} - 1\ V_{BE}$ therefore $V_{OH} - V_{OL} = V_{CC}/2$. The difference, $V_{OH} - V_{OL}$, and the mirror gain, I_2/I_3, are the two factors that cause the tachometer gain constant to vary from 1.0.

Note 4: Be sure when choosing the time constant R1 × C1 that R1 is such that the maximum anticipated output voltage at pin 3 can be reached with $I_3 \times$ R1. The maximum value for R1 is limited by the output resistance of pin 3 which is greater than 10 MΩ typically.

Note 5: Nonlinearity is defined as the deviation of V_{OUT} (@ pin 3) for f_{IN} = 5 kHz from a straight line defined by the V_{OUT} @ 1 kHz and V_{OUT} @ 10 kHz. C1 = 1000 pF, R1 = 68k and C2 = 0.22 mFd.

General Description (Continued)

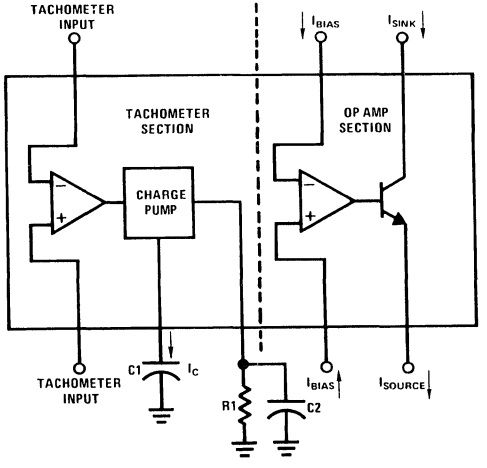
The op amp/comparator is fully compatible with the tachometer and has a floating transistor as its output. This feature allows either a ground or supply referred load of up to 50 mA. The collector may be taken above V_{CC} up to a maximum V_{CE} of 28V.

The two basic configurations offered include an 8-pin device with a *ground referenced tachometer* input and an internal connection between the tachometer output and the op amp non-inverting input. This version is well suited for single speed or frequency switching or fully buffered frequency to voltage conversion applications.

The more versatile configurations provide differential tachometer input and uncommitted op amp inputs. With this version the tachometer input may be floated and the op amp becomes suitable for active filter conditioning of the tachometer output.

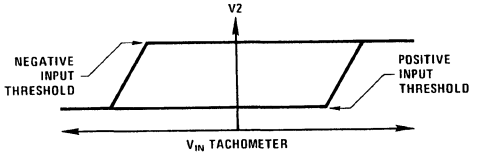
Both of these configurations are available with an active shunt regulator connected across the power leads. The regulator clamps the supply such that stable frequency to voltage and frequency to current operations are possible with any supply voltage and a suitable resistor.

Test Circuit and Waveform



TL/H/7942–6

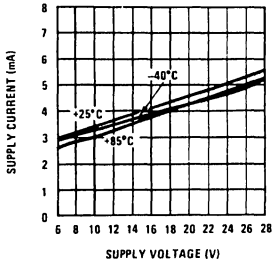
Tachometer Input Threshold Measurement



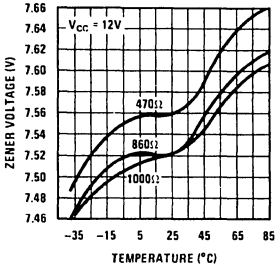
TL/H/7942–7

Typical Performance Characteristics

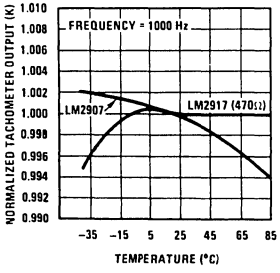
Total Supply Current



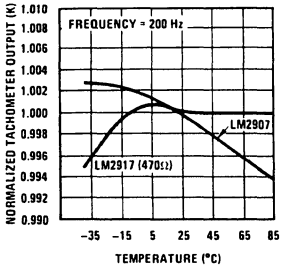
Zener Voltage vs Temperature



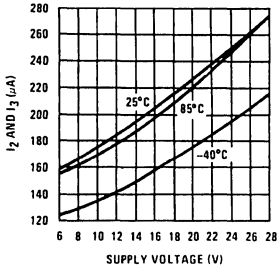
Normalized Tachometer Output vs Temperature



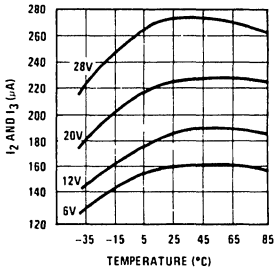
Normalized Tachometer Output vs Temperature



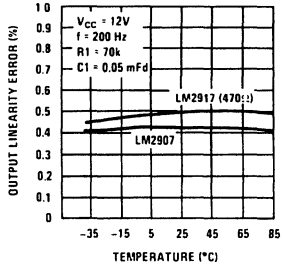
Tachometer Currents I_2 and I_3 vs Supply Voltage



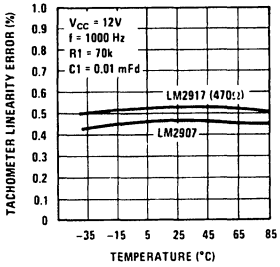
Tachometer Currents I_2 and I_3 vs Temperature



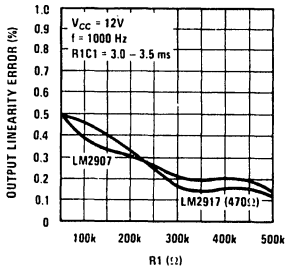
Tachometer Linearity vs Temperature



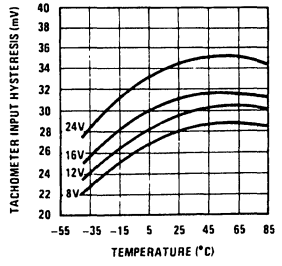
Tachometer Linearity vs Temperature



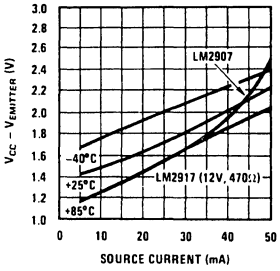
Tachometer Linearity vs R1



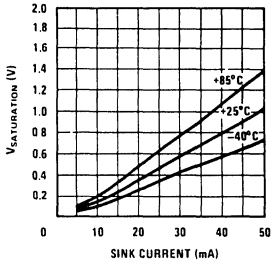
Tachometer Input Hysteresis vs Temperature



Op Amp Output Transistor Characteristics



Op Amp Output Transistor Characteristics



TL/H/7942–5

Applications Information

The LM2907 series of tachometer circuits is designed for minimum external part count applications and maximum versatility. In order to fully exploit its features and advantages let's examine its theory of operation. The first stage of operation is a differential amplifier driving a positive feedback flip-flop circuit. The input threshold voltage is the amount of differential input voltage at which the output of this stage changes state. Two options (LM2907-8, LM2917-8) have one input internally grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This is offered specifically for magnetic variable reluctance pickups which typically provide a single-ended ac output. This single input is also fully protected against voltage swings to ±28V, which are easily attained with these types of pickups.

The differential input options (LM2907, LM2917) give the user the option of setting his own input switching level and still have the hysteresis around that level for excellent noise rejection in any application. Of course in order to allow the inputs to attain common-mode voltages above ground, input protection is removed and neither input should be taken outside the limits of the supply voltage being used. It is very important that an input not go below ground without some resistance in its lead to limit the current that will then flow in the epi-substrate diode.

Following the input stage is the charge pump where the input frequency is converted to a dc voltage. To do this requires one timing capacitor, one output resistor, and an integrating or filter capacitor. When the input stage changes state (due to a suitable zero crossing or differential voltage on the input) the timing capacitor is either charged or discharged linearly between two voltages whose difference is $V_{CC}/2$. Then in one half cycle of the input frequency or a time equal to $1/2\ f_{IN}$ the change in charge on the timing capacitor is equal to $V_{CC}/2 \times C1$. The average amount of current pumped into or out of the capacitor then is:

$$\frac{\Delta Q}{T} = i_{c(AVG)} = C1 \times \frac{V_{CC}}{2} \times (2f_{IN}) = V_{CC} \times f_{IN} \times C1$$

The output circuit mirrors this current very accurately into the load resistor R1, connected to ground, such that if the pulses of current are integrated with a filter capacitor, then $V_O = i_c \times R1$, and the total conversion equation becomes:

$$V_O = V_{CC} \times f_{IN} \times C1 \times R1 \times K$$

Where K is the gain constant—typically 1.0.

The size of C2 is dependent only on the amount of ripple voltage allowable and the required response time.

CHOOSING R1 AND C1

There are some limitations on the choice of R1 and C1 which should be considered for optimum performance. The timing capacitor also provides internal compensation for the charge pump and should be kept larger than 500 pF for very accurate operation. Smaller values can cause an error current on R1, especially at low temperatures. Several considerations must be met when choosing R1. The output current at pin 3 is internally fixed and therefore $V_O/R1$ must be less than or equal to this value. If R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Also output ripple voltage must be considered and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1C2 combination is:

$$V_{RIPPLE} = \frac{V_{CC}}{2} \times \frac{C1}{C2} \times \left(1 - \frac{V_{CC} \times f_{IN} \times C1}{I_2}\right) \text{ pk-pk}$$

It appears R1 can be chosen independent of ripple, however response time, or the time it takes V_{OUT} to stabilize at a new voltage increases as the size of C2 increases, so a compromise between ripple, response time, and linearity must be chosen carefully.

As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1 and I_2:

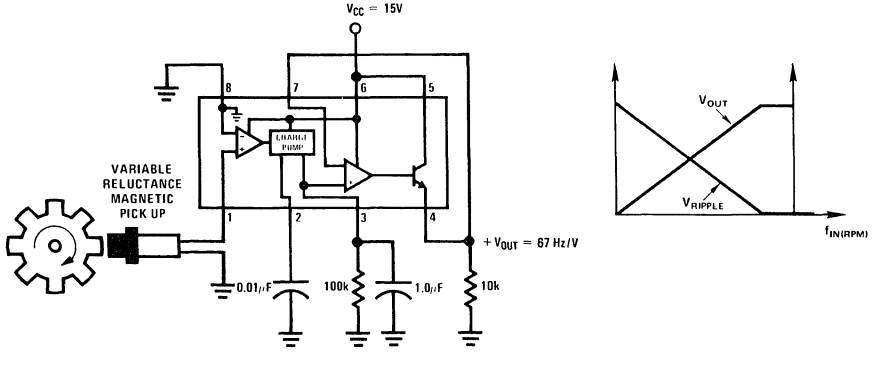
$$f_{MAX} = \frac{I_2}{C1 \times V_{CC}}$$

USING ZENER REGULATED OPTIONS (LM2917)

For those applications where an output voltage or current must be obtained independent of supply voltage variations, the LM2917 is offered. The most important consideration in choosing a dropping resistor from the unregulated supply to the device is that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the zener. At low supply voltages there must be some current flowing in the resistor above the 3 mA circuit current to operate the regulator. As an example, if the raw supply varies from 9V to 16V, a resistance of 470Ω will minimize the zener voltage variation to 160 mV. If the resistance goes under 400Ω or over 600Ω the zener variation quickly rises above 200 mV for the same input variation.

Typical Applications

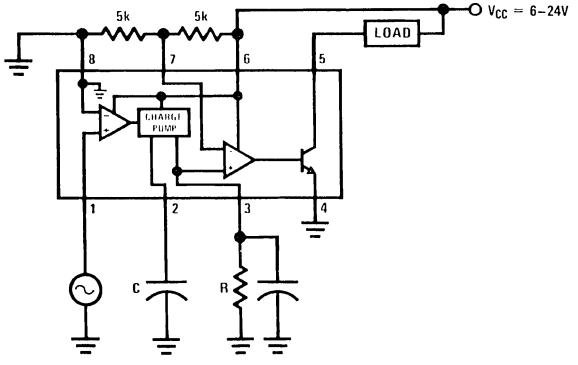
Minimum Component Tachometer



TL/H/7942–8

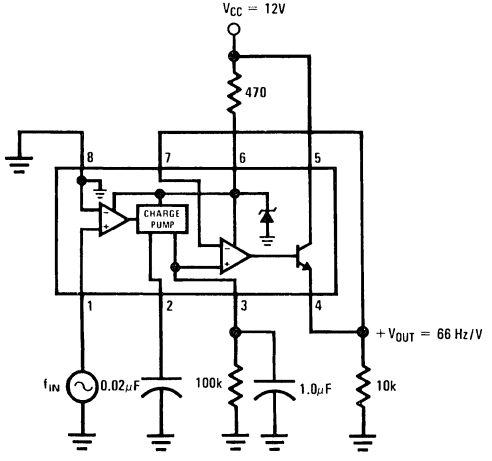
Typical Applications (Continued)

"Speed Switch" Load is Energized When $f_{IN} \geq \frac{1}{2RC}$



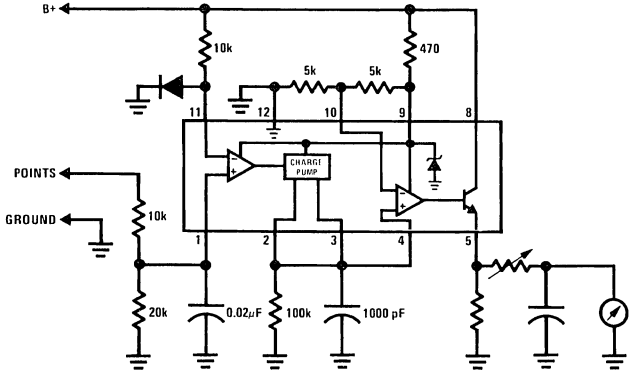
TL/H/7942–9

Zener Regulated Frequency to Voltage Converter



TL/H/7942–10

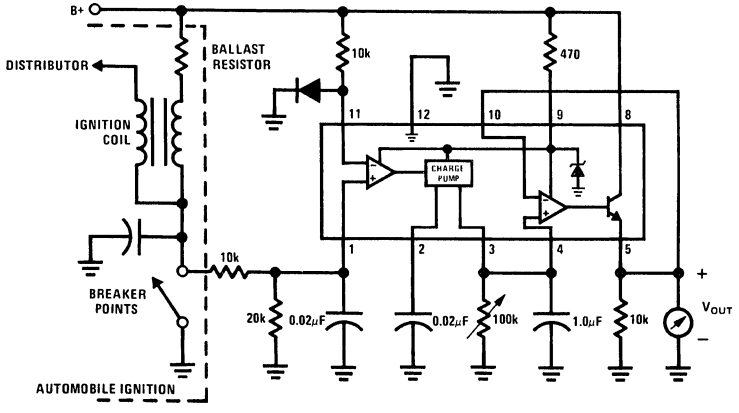
Breaker Point Dwell Meter



TL/H/7942–11

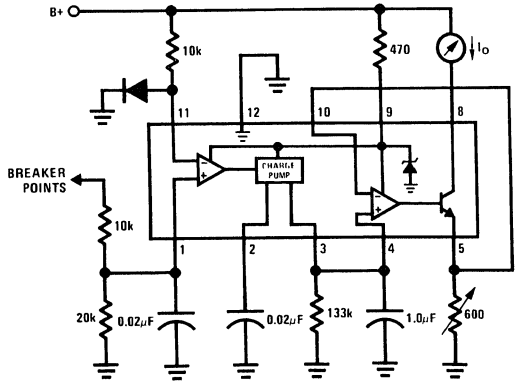
Typical Applications (Continued)

Voltage Driven Meter Indicating Engine RPM
V_O = 6V @ 400 Hz or 6000 ERPM (8 Cylinder Engine)



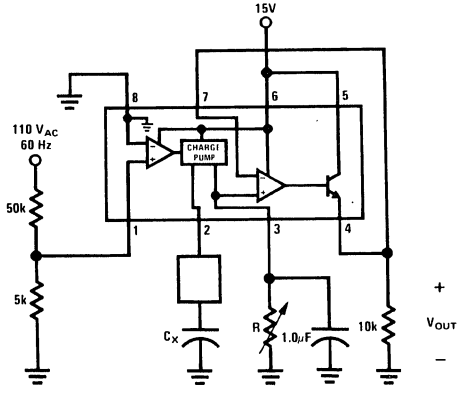
TL/H/7942–12

Current Driven Meter Indicating Engine RPM
I_O = 10 mA @ 300 Hz or 6000 ERPM (6 Cylinder Engine)



TL/H/7942–13

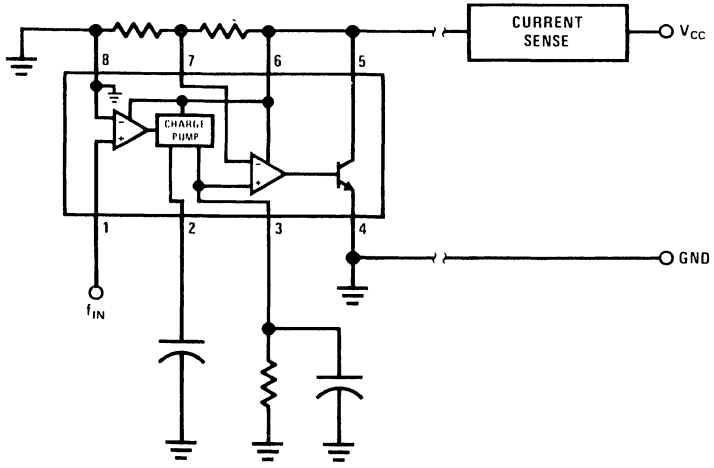
Capacitance Meter
V_{OUT} = 1V–10V for C_X = 0.01 to 0.1 mFd
(R = 111k)



TL/H/7942–14

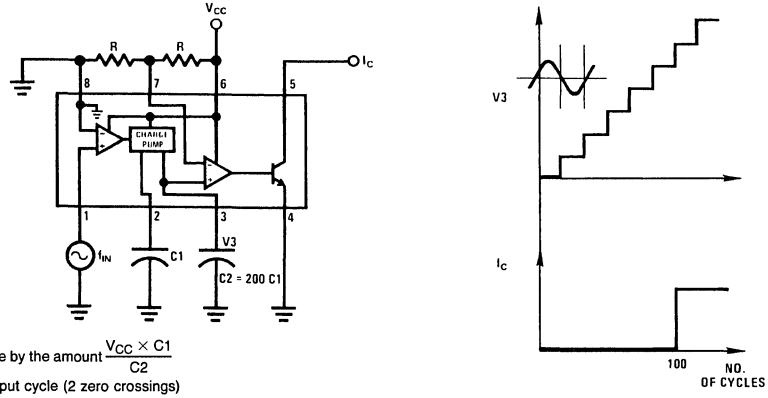
Typical Applications (Continued)

Two-Wire Remote Speed Switch



TL/H/7942–15

100 Cycle Delay Switch



TL/H/7942–16

V3 steps up in voltage by the amount $\frac{V_{CC} \times C1}{C2}$

for each complete input cycle (2 zero crossings)

Example:

If C2 = 200 C1 after 100 consecutive input cycles.

V3 = 1/2 V_{CC}

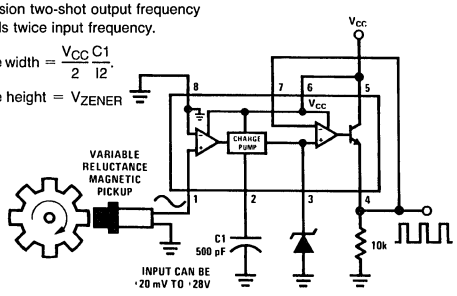
Typical Applications (Continued)

Variable Reluctance Magnetic Pickup Buffer Circuits

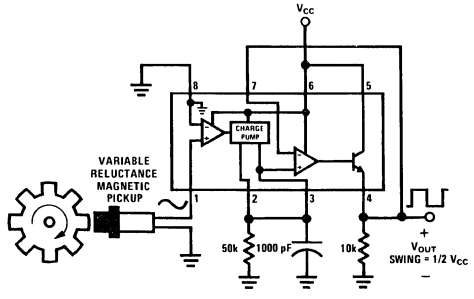
Precision two-shot output frequency equals twice input frequency.

Pulse width = $\frac{V_{CC}}{2} \frac{C1}{I2}$.

Pulse height = V_{ZENER}

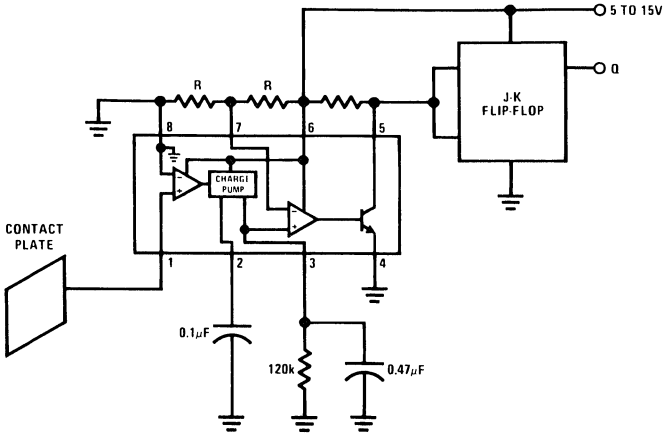


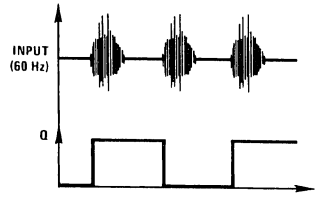
TL/H/7942–39



TL/H/7942–17

Finger Touch or Contact Switch

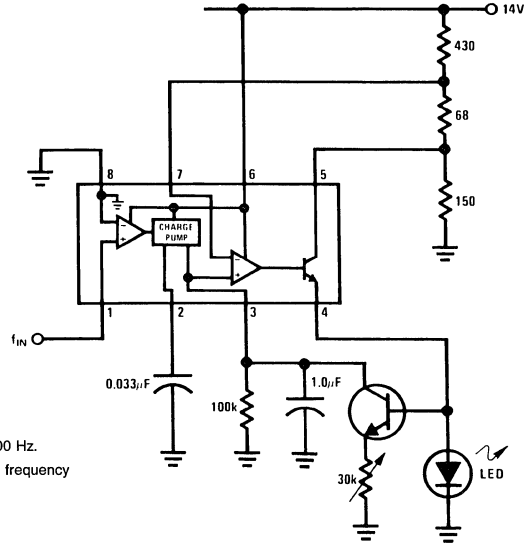




TL/H/7942–19

TL/H/7942–18

Flashing LED Indicates Overspeed



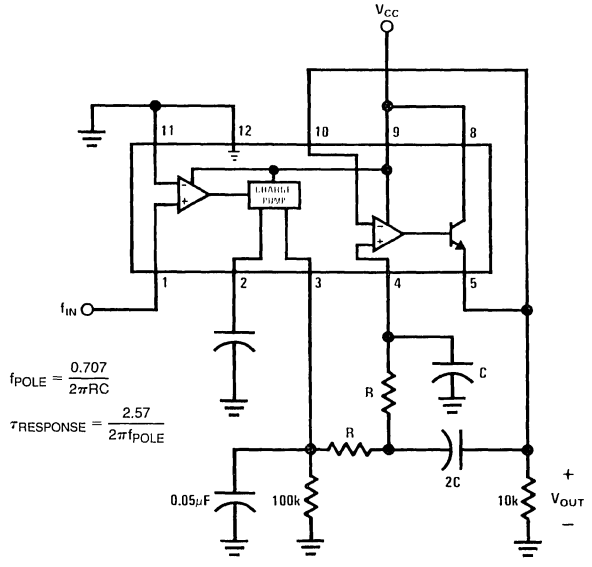
Flashing begins when $f_{IN} \geq 100$ Hz.

Flash rate increases with input frequency increase beyond trip point.

TL/H/7942–20

Typical Applications (Continued)

Frequency to Voltage Converter with 2 Pole Butterworth Filter to Reduce Ripple

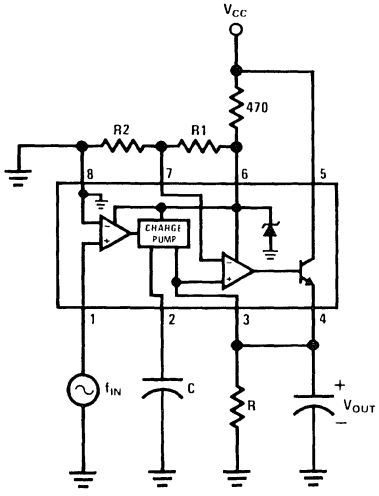


$$f_{POLE} = \frac{0.707}{2\pi RC}$$

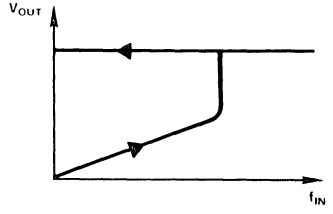
$$\tau_{RESPONSE} = \frac{2.57}{2\pi f_{POLE}}$$

TL/H/7942–21

Overspeed Latch



TL/H/7942–22



TL/H/7942–23

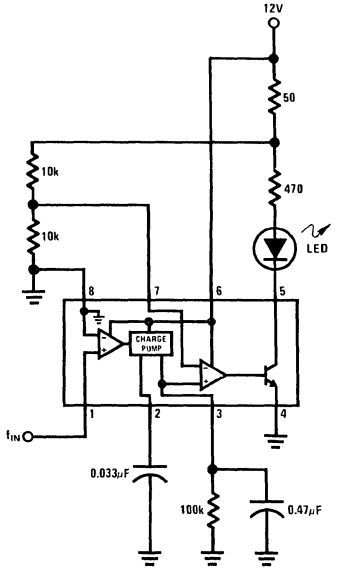
Output latches when

$$f_{IN} = \frac{R2}{R1 + R2}\frac{1}{RC}$$

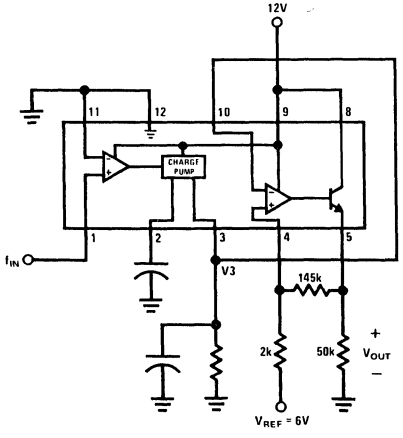
Reset by removing V_{CC}.

Typical Applications (Continued)

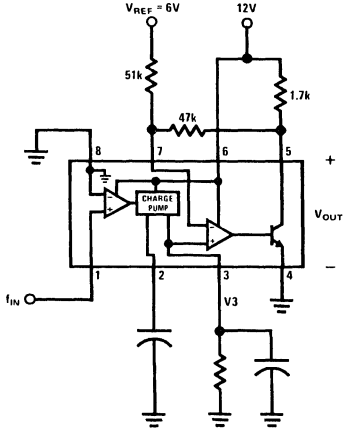
Some Frequency Switch Applications May Require Hysteresis in the Comparator Function Which can be Implemented in Several Ways:



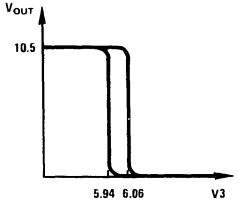
TL/H/7942–24



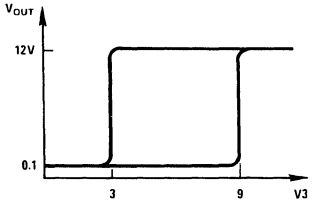
TL/H/7942–25



TL/H/7942–26



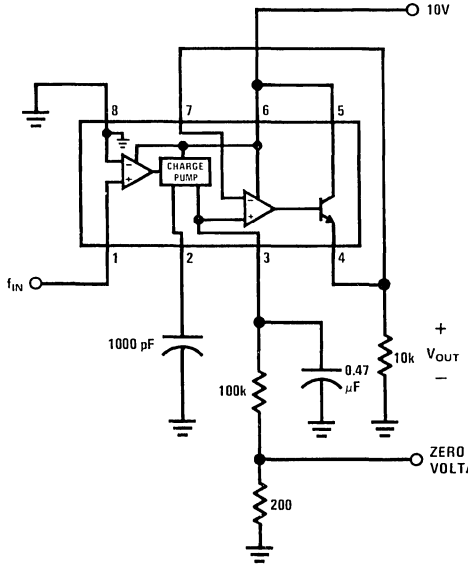
TL/H/7942–27

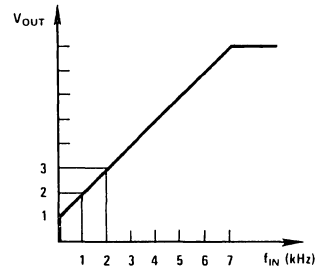


TL/H/7942–28

Typical Applications (Continued)

Changing the Output Voltage for an Input Frequency of Zero

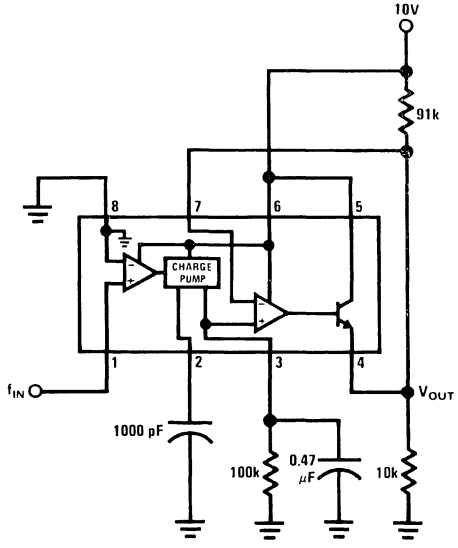


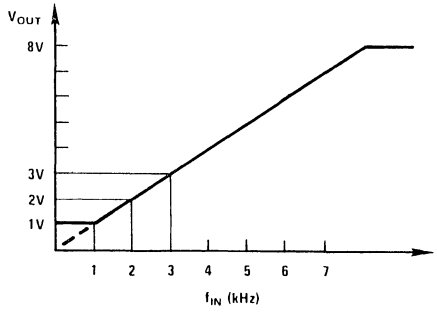


TL/H/7942–30

TL/H/7942–29

Changing Tachometer Gain Curve or Clamping the Minimum Output Voltage





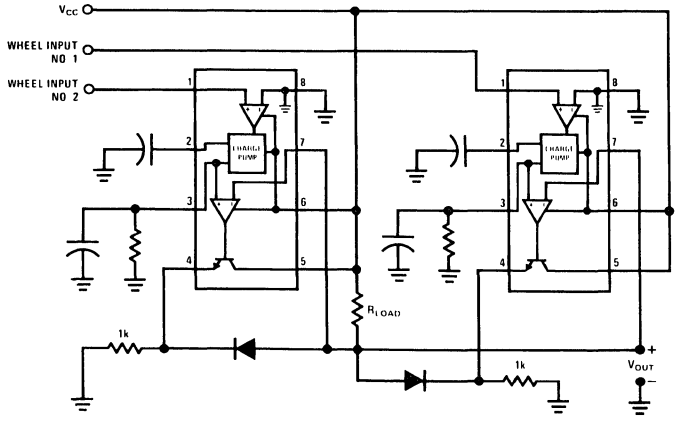
TL/H/7942–32

TL/H/7942–31

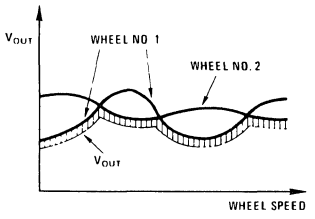
5

Anti-Skid Circuit Functions

"Select-Low" Circuit



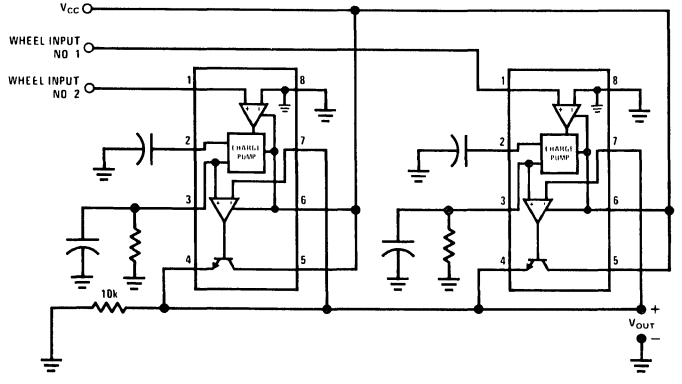
TL/H/7942–33



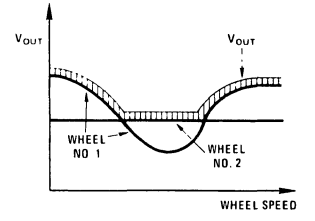
TL/H/7942–34

V_{OUT} is proportional to the lower of the two input wheel speeds.

"Select-High" Circuit



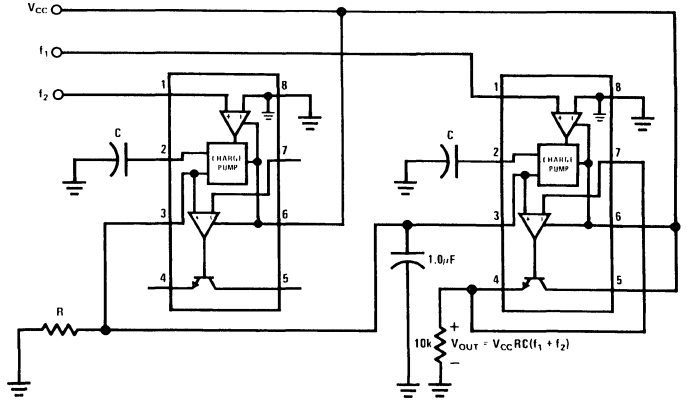
TL/H/7942–35



TL/H/7942–36

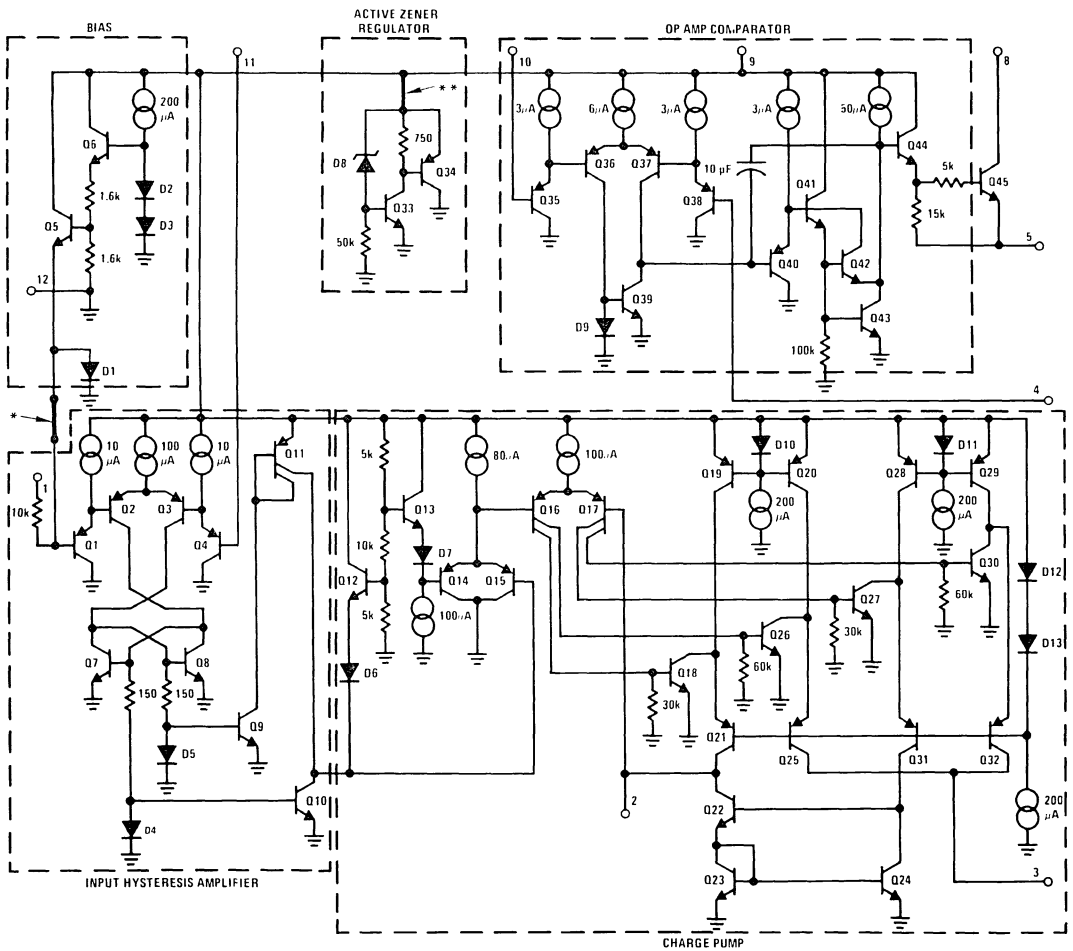
V_{OUT} is proportional to the higher of the two input wheel speeds.

"Select-Average" Circuit



TL/H/7942–37

Equivalent Schematic Diagram



TL/H/7942–38

*This connection made on LM2907-8 and LM2917-8 only.

**This connection made on LM2917 and LM2917-8 only.

National Semiconductor Corporation

LM3045/LM3046/LM3086 Transistor Arrays

General Description

The LM3045, LM3046 and LM3086 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3045 is supplied in a 14-lead cavity dual-in-line package rated for operation over the full military temperature range. The LM3046 and LM3086 are electrically identical to the LM3045 but are supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

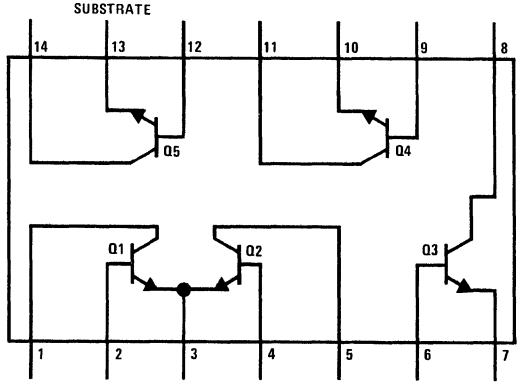
- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max at I_C = 1 mA
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz
- Full military temperature range (LM3045) −55°C to +125°C

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7950–1

Top View

Order Number LM3045J, LM3046M, LM3086M, LM3046N or LM3086N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings (T_A = 25°C)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LM3045		LM3046/LM3086		Units
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A = 25°C	300	750	300	750	mW
T_A = 25°C to 55°C			300	750	mW
T_A > 55°C			Derate at 6.67		mW/°C
T_A = 25°C to 75°C	300	750			mW
T_A > 75°C	Derate at 8				mW/°C
Collector to Emitter Voltage, V_{CEO}	15		15		V
Collector to Base Voltage, V_{CBO}	20		20		V
Collector to Substrate Voltage, V_{CIO} (Note 1)	20		20		V
Emitter to Base Voltage, V_{EBO}	5		5		V
Collector Current, I_C	50		50		mA
Operating Temperature Range	−55°C to +125°C		−40°C to +85°C		
Storage Temperature Range	−65°C to +150°C		−65°C to +85°C		
Soldering Information					
Dual-In-Line Package Soldering (10 Sec.)	260°C		260°C		
Small Outline Package					
Vapor Phase (60 Seconds)			215°C		
Infrared (15 Seconds)			220°C		

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Parameter	Conditions	Limits LM3045, LM3046			Limits LM3086			Units
		Min	Typ	Max	Min	Typ	Max	
Collector to Base Breakdown Voltage ($V_{(BR)CBO}$)	I_C = 10 μA, I_E = 0	20	60		20	60		V
Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$)	I_C = 1 mA, I_B = 0	15	24		15	24		V
Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$)	I_C = 10 μA, I_{CI} = 0	20	60		20	60		V
Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$)	I_E 10 μA, I_C = 0	5	7		5	7		V
Collector Cutoff Current (I_{CBO})	V_{CB} = 10V, I_E = 0		0.002	40		0.002	100	nA
Collector Cutoff Current (I_{CEO})	V_{CE} = 10V, I_B = 0			0.5			5	μA
Static Forward Current Transfer Ratio (Static Beta) (h_{FE})	V_{CE} = 3V, I_C = 10 mA		100			100		
	V_{CE} = 3V, I_C = 1 mA	40	100		40	100		
	V_{CE} = 3V, I_C = 10 μA		54			54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{O1} - I_{O2} \rvert$	V_{CE} = 3V, I_C = 1 mA		0.3	2				μA
Base to Emitter Voltage (V_{BE})	V_{CE} = 3V, I_E = 1 mA		0.715			0.715		V
	V_{CE} = 3V, I_E = 10 mA		0.800			0.800		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE1} - V_{BE2} \rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5				mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE3} - V_{BE4} \rvert$, $\lvert V_{BE4} - V_{BE5} \rvert$, $\lvert V_{BE5} - V_{BE3} \rvert$	V_{CE} = 3V, I_C = 1 mA		0.45	5				mV
Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		−1.9			−1.9		mV/°C
Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$)	I_B = 1 mA, I_C = 10 mA		0.23			0.23		V
Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{10}}{\Delta T}\right)$	V_{CE} = 3V, I_C = 1 mA		1.1					μV/°C

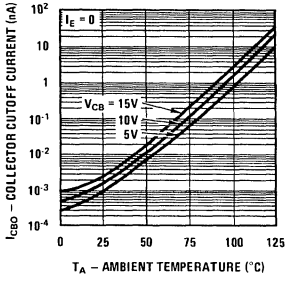
Note 1: The collector of each transistor of the LM3045, LM3046, and LM3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics (Continued)

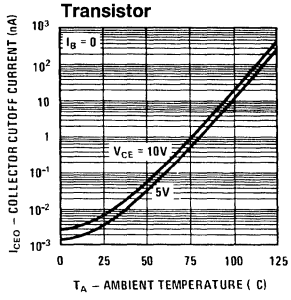
Parameter	Conditions	Min	Typ	Max	Units
Low Frequency Noise Figure (NF)	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS					
Forward Current Transfer Ratio (h_{fe})	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		110 (LM3045, LM3046) (LM3086)		
Short Circuit Input Impednace (h_{ie})			3.5		kΩ
Open Circuit Output Impedance (h_{oe})			15.6		μmho
Open Circuit Reverse Voltage Transfer Ratio (h_{re})			1.8×10^{-4}		
ADMITTANCE CHARACTERISTICS					
Forward Transfer Admittance (Y_{fe})	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		
Input Admittance (Y_{ie})			0.3 + J 0.04		
Output Admittance (Y_{oe})			0.001 + j 0.03		
Reverse Transfer Admittance (Y_{re})			See Curve		
Gain Bandwidth Product (f_T)	V_{CE} = 3V, I_C = 3 mA	300	550		
Emitter to Base Capacitance (C_{EB})	V_{EB} = 3V, I_E = 0		0.6		pF
Collector to Base Capacitance (C_{CB})	V_{CB} = 3V, I_C = 0		0.58		pF
Collector to Substrate Capacitance (C_{CI})	V_{CS} = 3V, I_C = 0		2.8		pF

Typical Performance Characteristics

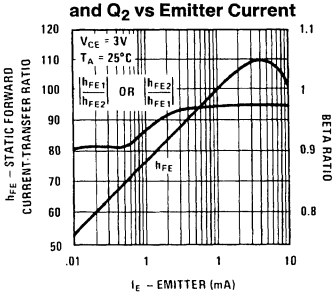
Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor



Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor

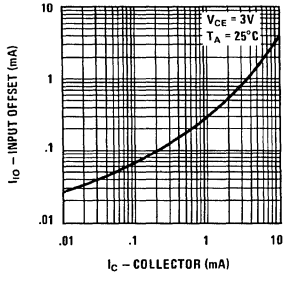


Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current

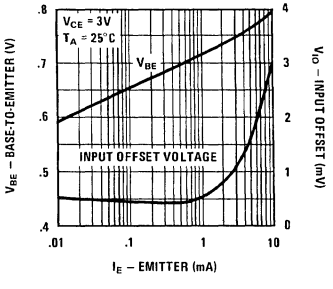


TL/H/7950–2

Typical Input Offset Current for Matched Transistor Pair Q_1 Q_2 vs Collector Current



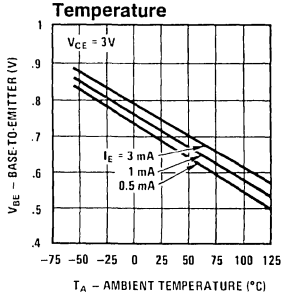
Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current



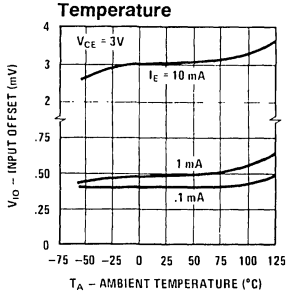
TL/H/7950–3

Typical Performance Characteristics (Continued)

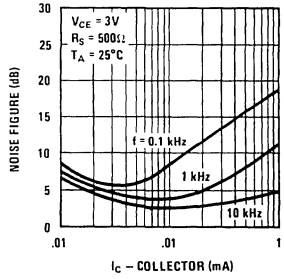
Typical Base To Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature



Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature

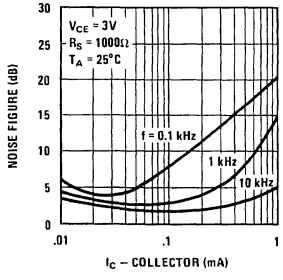


Typical Noise Figure vs Collector Current

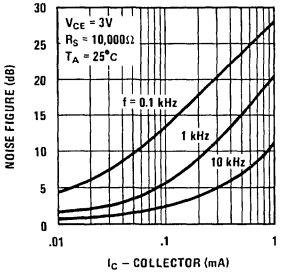


TL/H/7950–4

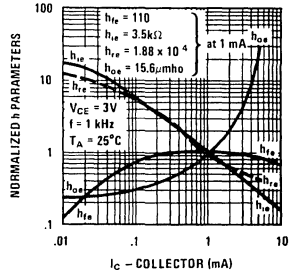
Typical Noise Figure vs Collector Current



Typical Noise Figure vs Collector Current

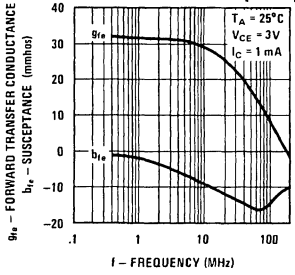


Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current

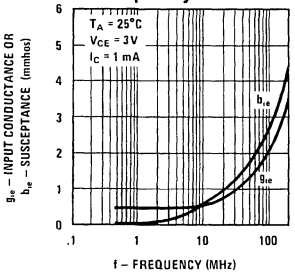


TL/H/7950–5

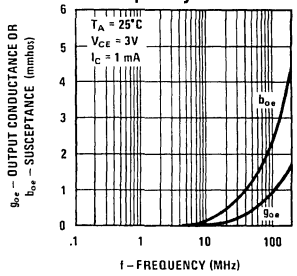
Typical Forward Transfer Admittance vs Frequency



Typical Input Admittance vs Frequency



Typical Output Admittance vs Frequency



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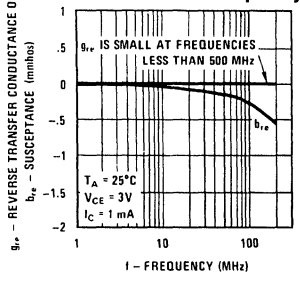
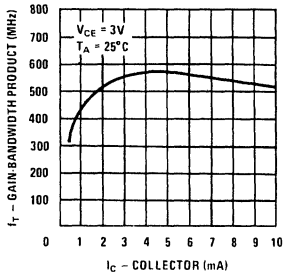
5

Typical Performance Characteristics (Continued)

Typical Reverse Transfer Admittance vs Frequency



Typical Gain-Bandwidth Product vs Collector Current



TL/H/7950–7

National Semiconductor Corporation

LM3146 High Voltage Transistor Array

General Description

The LM3146 consists of five high voltage general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the dc through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3146 is supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

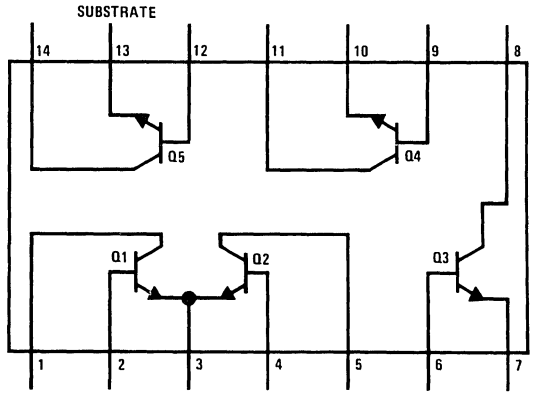
- High voltage matched pairs of transistors, V_{BE} matched ±5 mV, input offset current 2 μA max at I_C = 1 mA
- Five general purpose monolithic transistors
- Operation from dc to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from dc to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Connection Diagram

Dual-In-Line and Small Outline Packages



TL/H/7959–1

Top View

Order Number LM3146M or LM3146N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM3146	Units
Power Dissipation: Each transistor		
T_A = 25°C to 55°C	300	mW
T_A > 55°C	Derate at 6.67	mW/°C
Power Dissipation: Total Package		
T_A = 25°C	500	mW
T_A > 25°C	Derate at 6.67	mW/°C
Collector to Emitter Voltage, V_{CEO}	30	V
Collector to Base Voltage, V_{CBO}	40	V
Collector to Substrate Voltage, V_{CIO} (Note 1)	40	V
Emitter to Base Voltage, V_{EBO} (Note 2)	5	V
Collector to Current, I_C	50	mA
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +150	°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics T_A = 25°C

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
$V_{(BR)CBO}$	Collector to Base Breakdown Voltage	I_C = 10 μA, I_E = 0	40	72		V
$V_{(BR)CEO}$	Collector to Emitter Breakdown Voltage	I_C = 1 mA, I_B = 0	30	56		V
$V_{(BR)CIO}$	Collector to Substrate Breakdown Voltage	I_{CI} = 10 μA, I_B = 0, I_E = 0	40	72		V
$V_{(BR)EBO}$	Emitter to Base Breakdown Voltage (Note 2)	I_C = 0, I_E = 10 μA	5	7		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 10V, I_E = 0		0.002	100	nA
I_{CEO}	Collector Cutoff Current	V_{CE} = 10V, I_B = 0		(Note 3)	5	μA
h_{FE}	Static Forward Current Transfer Ratio (Static Beta)	I_C = 10 mA, V_{CE} = 5V I_C = 1 mA, V_{CE} = 5V I_C = 10 μA, V_{CE} = 5V	30	85 100 90		
$I_{B1}-I_{B2}$	Input Offset Current for Matched Pair Q1 and Q2	I_{C1} = 1_{C2} = 1 mA, V_{CE} = 5V		0.3	2	μA
V_{BE}	Base to Emitter Voltage	I_C = 1 mA, V_{CE} = 3V	0.63	0.73	0.83	V
$V_{BE1}-V_{BE2}$	Magnitude of Input Offset Voltage for Differential Pair	V_{CE} = 5V, I_E = 1 mA		0.48	5	mV
$\Delta V_{BE}/\Delta T$	Temperature Coefficient of Base to Emitter Voltage	V_{CE} = 5V, I_E = 1 mA		−1.9		mV/°C
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = 10 mA, I_B = 1 mA		0.33		V
$\Delta V_{10}/\Delta T$	Temperature Coefficient of Input Offset Voltage	I_C = 1 mA, V_{CE} = 5V		1.1		μV/°C

Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

Note 3: See curve.

AC Electrical Characteristics

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
NF	Low Frequency Noise Figure	f = 1 kHz, V_{CE} = 5V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
f_T	Gain Bandwidth Product	V_{CE} = 5V, I_C = 3 mA	300	500		MHz
C_{EB}	Emitter to Base Capacitance	V_{EB} = 5V, I_E = 0		0.70		pF
C_{CB}	Collector to Base Capacitance	V_{CB} = 5V, I_C = 0		0.37		pF
C_{CI}	Collector to Substrate Capacitance	V_{CI} = 5V, I_C = 0		2.2		pF
Low Frequency, Small Signal Equivalent Circuit Characteristics						
h_{fe}	Forward Current Transfer Ratio	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		100		
h_{ie}	Short Circuit Input Impedance	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		3.5		kΩ
h_{oe}	Open Circuit Output Impedance	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		15.6		μmho
h_{re}	Open Circuit Reverse Voltage Transfer Ratio	f = 1 kHz, V_{CE} = 3V, I_C = 1 mA		1.8×10^{-4}		
Admittance Characteristics						
Y_{fe}	Forward Transfer Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		31 − j 1.5		mmho
Y_{ie}	Input Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.3 + j 0.04		mmho
Y_{oe}	Output Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		0.001 + j 0.03		mmho
Y_{re}	Reverse Transfer Admittance	f = 1 MHz, V_{CE} = 3V, I_C = 1 mA		(Note 3)		mmho

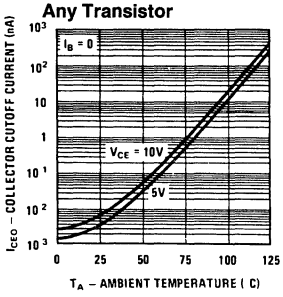
Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

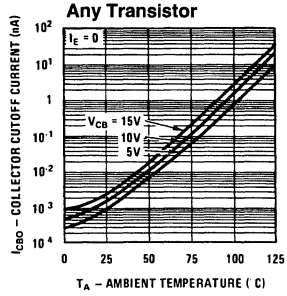
Note 3: See curve.

Typical Performance Characteristics

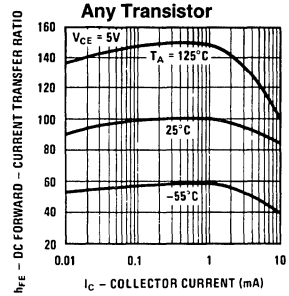
I_{CEO} vs T_A for Any Transistor



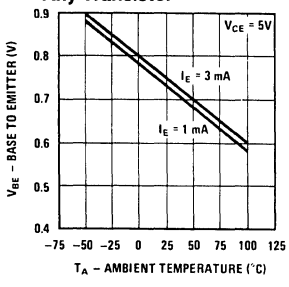
I_{CBO} vs T_A for Any Transistor



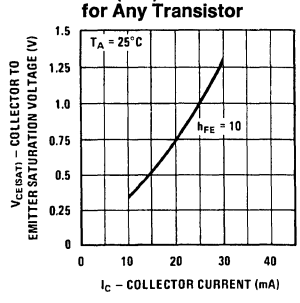
h_{FE} vs I_C for Any Transistor



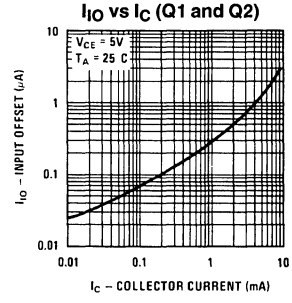
V_{BE} vs T_A for Any Transistor



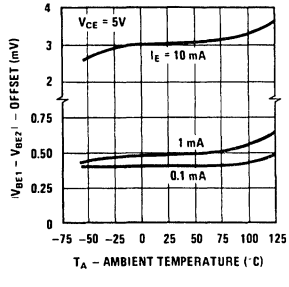
$V_{CE(SAT)}$ vs I_C for Any Transistor



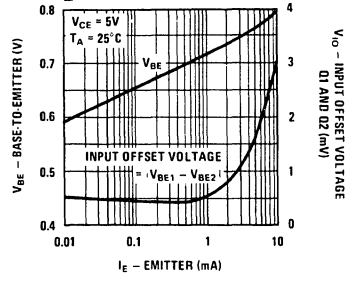
I_{IO} vs I_C (Q1 and Q2)



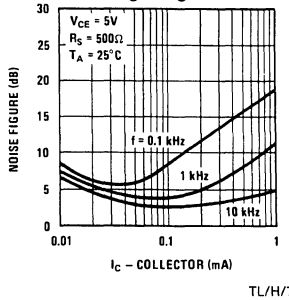
V_{IO} vs T_A for Q1 and Q2



V_{BE} and V_{IO} vs I_E for Q1 and Q2



NF vs I_C @ R_S = 500Ω



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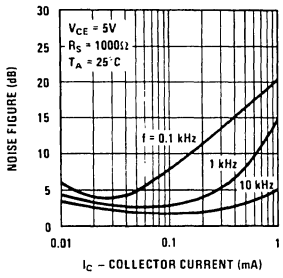
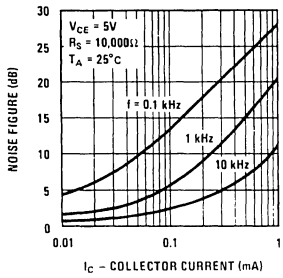
Typical Performance Characteristics (Continued)

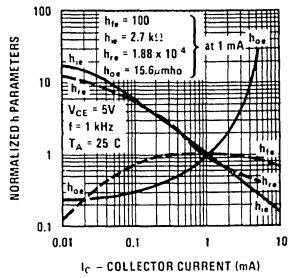
NF vs I_C @ R_S = 1 kΩ



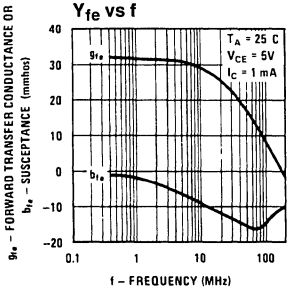
NF vs I_C = R_S = 10 kΩ



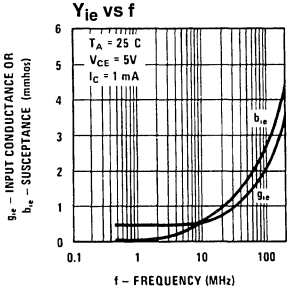
h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C



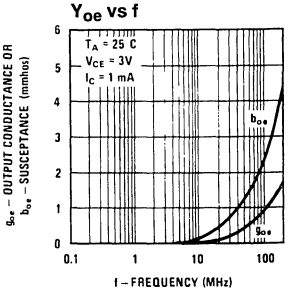
Y_{fe} vs f



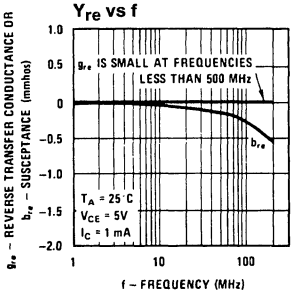
Y_{ie} vs f



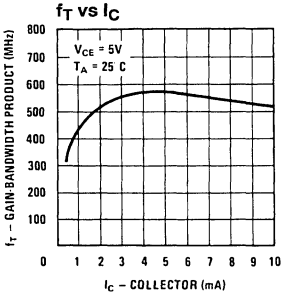
Y_{oe} vs f



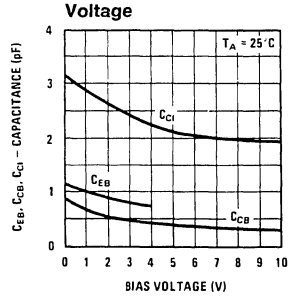
Y_{re} vs f



f_T vs I_C



C_{EB}, C_{CB}, C_{CI} vs Bias Voltage



TL/H/7959–3

5

National Semiconductor Corporation

LM3909 LED Flasher/Oscillator

General Description

The LM3909 is a monolithic oscillator specifically designed to flash Light Emitting Diodes. By using the timing capacitor for voltage boost, it delivers pulses of 2 or more volts to the LED while operating on a supply of 1.5V or less. The circuit is inherently self-starting, and requires addition of only a battery and capacitor to function as an LED flasher.

Packaged in an 8-lead plastic mini-DIP, the LM3909 will operate over the extended consumer temperature range of −25°C to +70°C. It has been optimized for low power drain and operation from weak batteries so that continuous operation life exceeds that expected from battery rating.

Application is made simple by inclusion of internal timing resistors and an internal LED current limit resistor. As shown in the first two application circuits, the timing resistors supplied are optimized for nominal flashing rates and minimum power drain at 1.5V and 3V.

Timing capacitors will generally be of the electrolytic type, and a small 3V rated part will be suitable for any LED flasher using a supply up to 6V. However, when picking flash rates, it should be remembered that some electrolytics have very broad capacitance tolerances, for example −20% to +100%.

Features

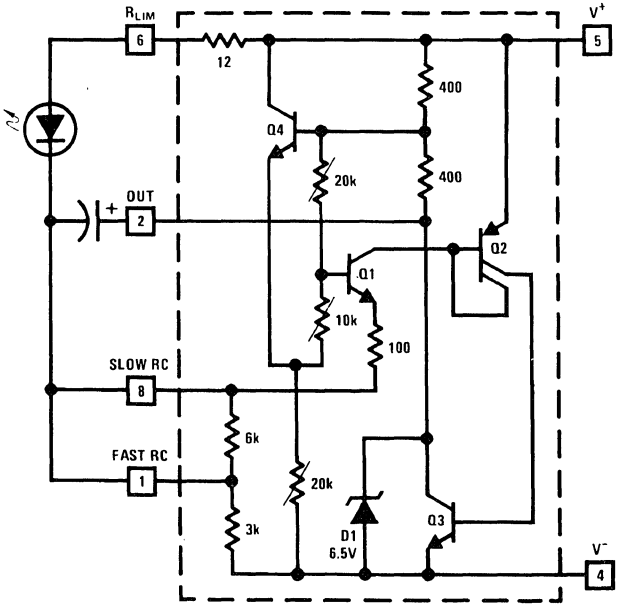
- Operation over one year from one C size flashlight cell
- Bright, high current LED pulse
- Minimum external parts
- Low cost
- Low voltage operation, from just over 1V to 5V
- Low current drain, averages under 0.5 mA during battery life
- Powerful; as an oscillator directly drives an 8Ω speaker
- Wide temperature range

Applications

- Finding flashlights in the dark, or locating boat mooring floats
- Sales and advertising gimmicks
- Emergency locators, for instance on fire extinguishers
- Toys and novelties
- Electronic applications such as trigger and sawtooth generators
- Siren for toy fire engine, (combined oscillator, speaker driver)
- Warning indicators powered by 1.4V to 200V

Schematic Diagram

Typical 1.5V Flasher



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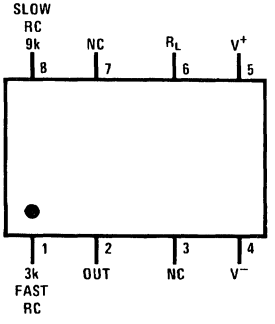
Connection Diagram

Dual-In-Line Package



TL/H/7969–2

Top View

Order Number LM3909N
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

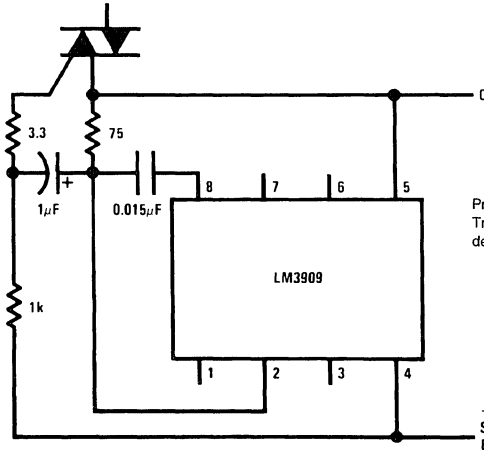
Power Dissipation	500 mW
V^+ Voltage	6.4V
Operating Temperature Range	−25°C to +70°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics

Parameter	Conditions (Applications Note 3)	Min	Typ	Max	Units
Supply Voltage	(In Oscillation)	1.15		6.0	V
Operating Current			0.55	0.75	mA
Flash Frequency	300 μF, 5% Capacitor	0.65	1.0	1.3	Hz
High Flash Frequency	0.30 μF, 5% Capacitor		1.1		kHz
Compatible LED Forward Drop	1 mA Forward Current	1.35		2.1	V
Peak LED Current	350 μF Capacitor		45		mA
Pulse Width	350 μF Capacitors at ½ Amplitude		6.0		ms

Typical Applications (See applications notes on following page)

Triac Trigger

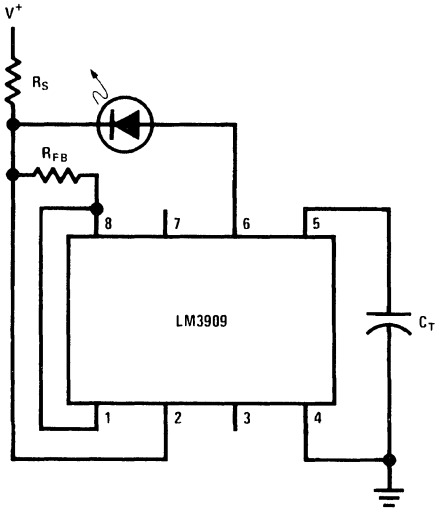


Provides 40 mA. 10 μs pulses at about 8 kHz. Triac gate may be pulse transformer isolated if desired.

TL/H/7969–3

Typical Applications (Continued)(See applications notes below)

Warning Flasher High Voltage Powered

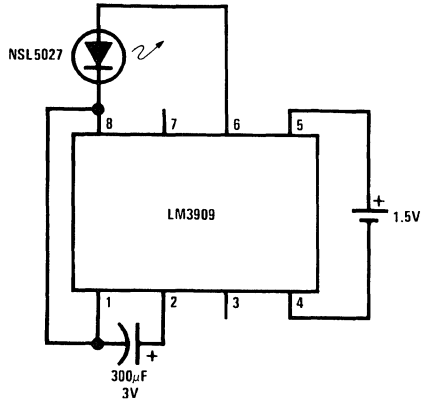


TL/H/7969–4

Typical Operating Conditions

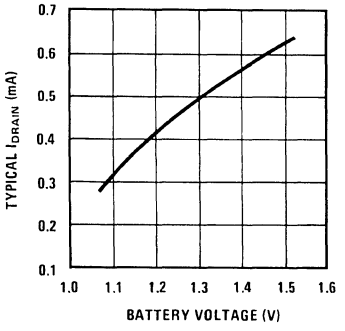
V^+	Nominal Flash Hz	C_T	R_S	R_{FB}	V^+_{RANGE}
6V	2	400 μF	1k	1.5k	5V–25V
15V	2	180 μF	3.9k	1k	13V–50V
100V	1.7	180 μF	43k 1W	1k	85V–200V

1.5V Flasher



TL/H/7969–5

Note: Nominal flash rate: 1 Hz.



TL/H/7969–6

Estimated Battery Life (Continuous 1.5V Flasher Operation)

Size Cell	Type	
	Standard	Alkaline
AA	3 months	6 months
C	7 months	15 months
D	1.3 years	2.6 years

Note: Estimates are made from our tests and manufacturers data. Conditions are fresh batteries and room temperature. Clad or "leak-proof" batteries are recommended for any application of five months or more. Nickel Cadmium cells are not recommended.

APPLICATIONS NOTES

Note 1: All capacitors shown are electrolytic unless marked otherwise.

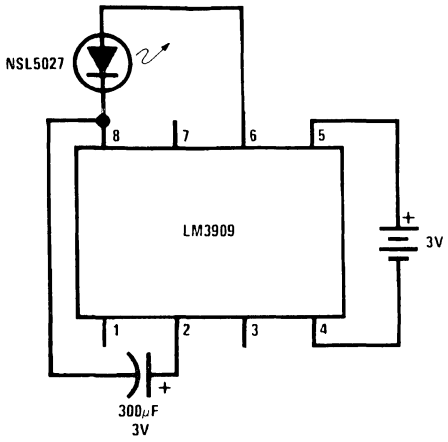
Note 2: Flash rates and frequencies assume a ±5% capacitor tolerance. Electrolytics may vary −20% to +100% of their stated value.

Note 3: Unless noted, measurements above are made with a 1.4V supply, a 25°C ambient temperature, and an LED with a forward drop of 1.5V to 1.7V at 1 mA forward current.

Note 4: Occasionally a flasher circuit will fail to oscillate due to an LED defect that may be missed because it only reduces light output 10% or so. Such LEDs can be identified by a large increase in conduction between 0.9V and 1.2V.

Typical Applications (Continued) (See applications notes on previous page)

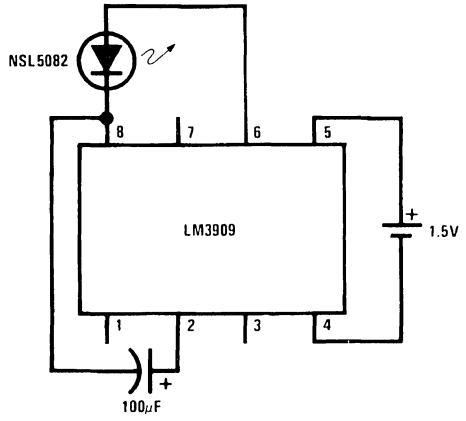
3V Flasher



TL/H/7969–7

Note: Nominal flash rate: 1 Hz. Average I_{DRAIN} = 0.77 mA.

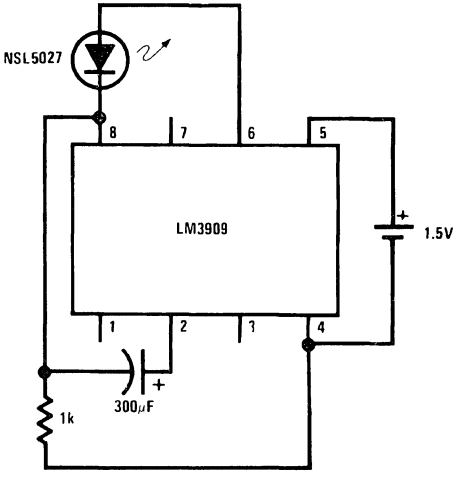
Minimum Power at 1.5V



TL/H/7969–8

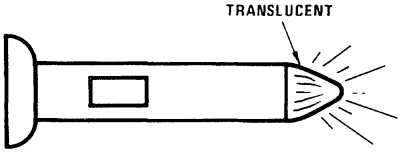
Note: Nominal flash rate: 1.1 Hz. Average I_{DRAIN} = 0.32 mA.

Fast Blinker



TL/H/7969–9

Note: Nominal flash rate: 2.6 Hz. Average I_{DRAIN} = 1.2 mA.

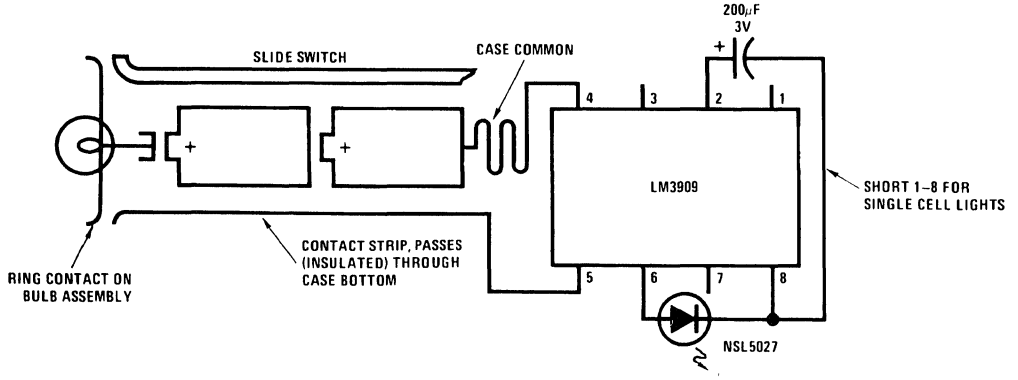


TL/H/7969–11

Note: Winking LED inside, locates light in total darkness.

Typical Applications (Continued) (See applications notes above)

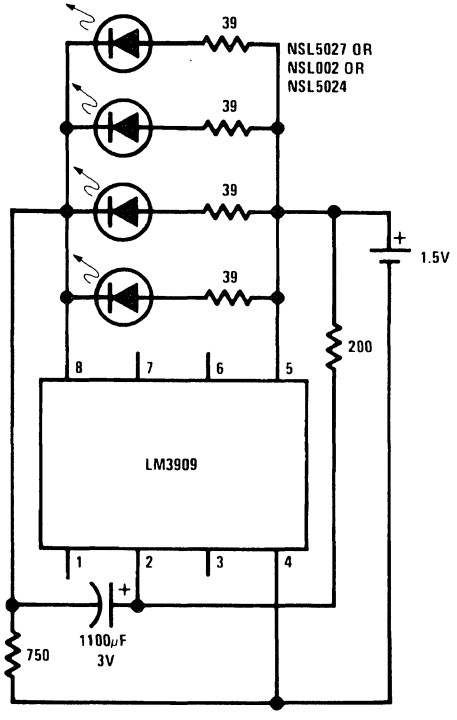
Flashlight Finder



TL/H/7969–10

Note: LM3909, capacitor, and LED are installed in a white translucent cap on the flashlight's back end. Only one contact strip (in addition to the case connection) is needed for flasher power. Drawing current through the bulb simplifies wiring and causes negligible loss since bulb resistance cold is typically less than 2Ω.

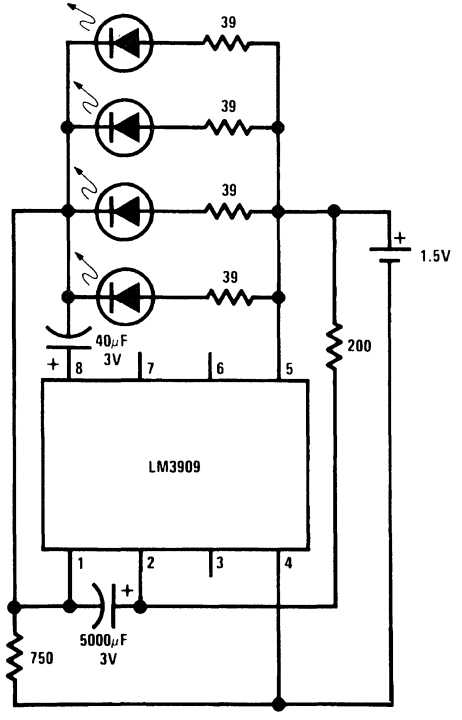
4 Parallel LEDs



TL/H/7969–12

Note: Nominal flash rate: 1.3 Hz. Average I_{DRAIN} = 2 mA.

High Efficiency Parallel Circuit

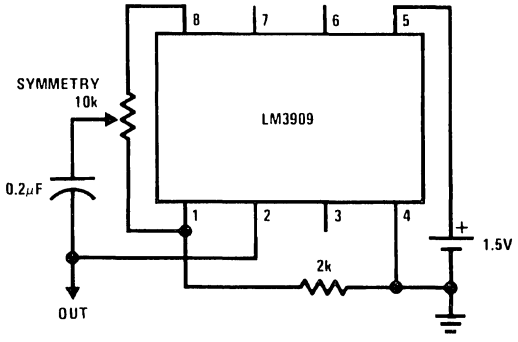


TL/H/7969–13

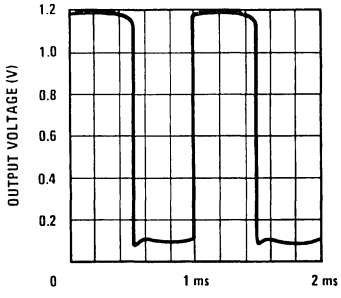
Note: Nominal flash rate: 1.5 Hz. Average I_{DRAIN} = 1.5 mA.

Typical Applications (Continued) (See applications notes above)

1 kHz Square Wave



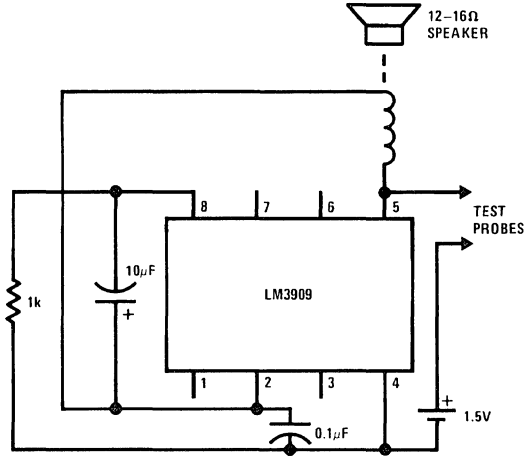
TL/H/7969–14



TL/H/7969–15

Note: Output voltage through a 10k load to ground.

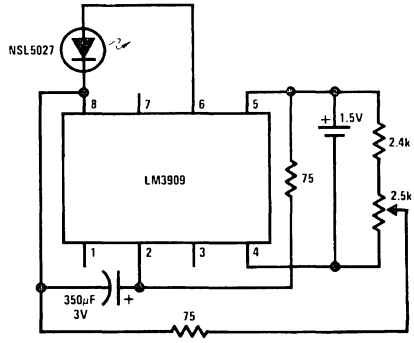
"Buzz Box" Continuity and Coil Checker



TL/H/7969–16

Note: Differences between shorts, coils, and a few ohms of resistance can be heard.

Variable Flasher

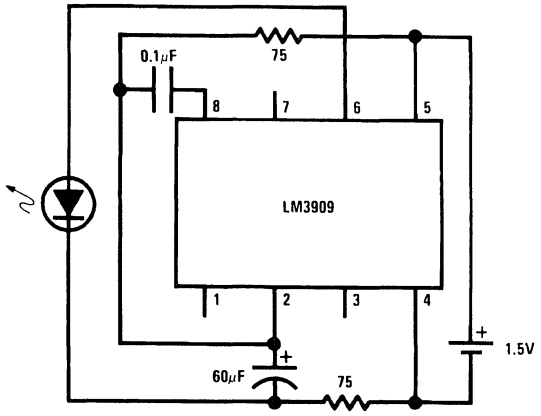


TL/H/7969–17

Note: Flash rate: 0 Hz–20 Hz.

Typical Applications (Continued) (See applications notes above)

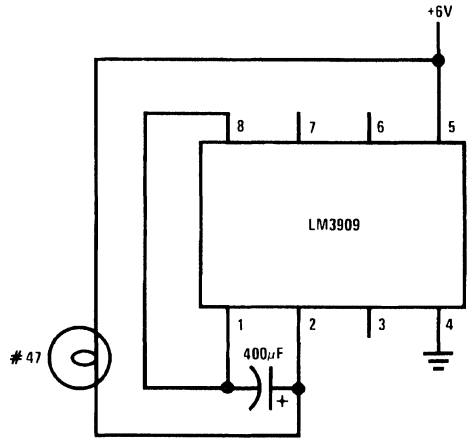
LED Booster



TL/H/7969–18

Note: High efficiency, 4 mA drain. Continuous appearing light obtained by supplying short, high current, pulses (2 kHz) to LEDs with higher than battery voltage available.

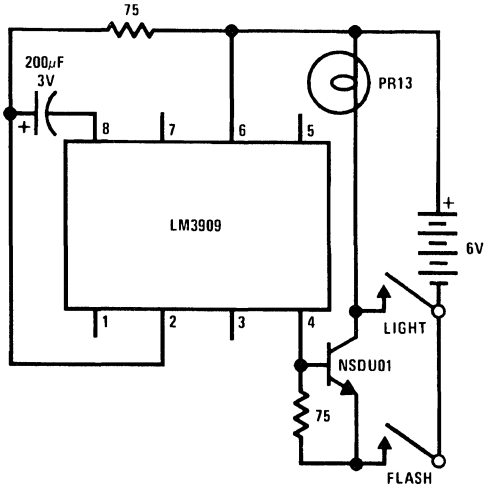
Incandescent Bulb Flasher



TL/H/7969–19

Note: Flash rate: 1.5 Hz.

Emergency Lantern/Flasher



TL/H/7969–20

Note: Nominal flash rate: 1.5 Hz.

National Semiconductor Corporation

LM3914 Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to ½%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N is available in an 18-lead molded (N) package.

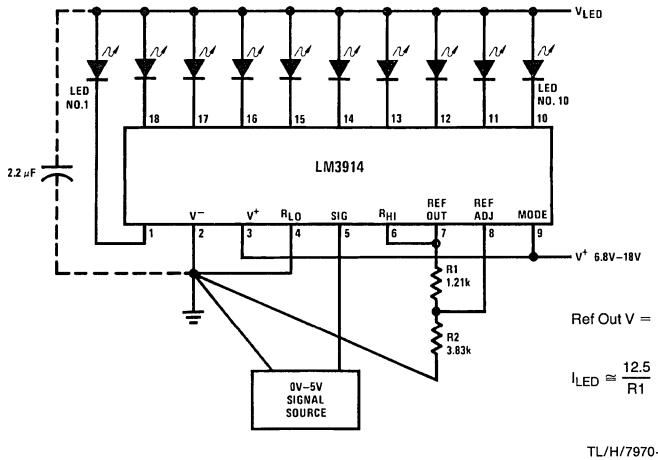
The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Features

- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 mA to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

Typical Applications

0V to 5V Bar Graph Meter



Note 1: Grounding method is typical of *all* uses. The 2.2 µF tantalum or 10 µF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} \cong \frac{12.5}{R1}$$

TL/H/7970–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation (Note 5)	
Molded DIP (N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Plastic Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 1)		Min	Typ	Max	Units
COMPARATOR						
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA			3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA			3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA		3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le V^+ - 1.5V$			25	100	nA
Input Signal Overvoltage	No Change in Display		−35		35	V
VOLTAGE-DIVIDER						
Divider Resistance	Total, Pin 6 to 4		8	12	17	kΩ
Accuracy	(Note 2)			0.5	2	%
VOLTAGE REFERENCE						
Output Voltage	$0.1\text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$		1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$			0.01	0.03	%/V
Load Regulation	$0.1\text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$			0.4	2	%
Output Voltage Change with Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = 5V$			1		%
Adjust Pin Current				75	120	μA
OUTPUT DRIVERS						
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA		7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$	$I_{LED} = 2$ mA		0.12	0.4	mA
		$I_{LED} = 20$ mA		1.2	3	
LED Current Regulation	$2V \le V_{LED} \le 17V$	$I_{LED} = 2$ mA		0.1	0.25	mA
		$I_{LED} = 20$ mA		1	3	
Dropout Voltage	$I_{LED(ON)} = 20$ mA, $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA				1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA			0.15	0.4	V
Output Leakage, Each Collector	(Bar Mode) (Note 4)			0.1	10	μA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)		Min	Typ	Max	Units
OUTPUT DRIVERS (Continued)						
Output Leakage	(Dot Mode) (Note 4)	Pins 10–18		0.1	10	μA
		Pin 1	60	150	450	μA
SUPPLY CURRENT						
Standby Supply Current (All Outputs Off)	$V^+ = 5V$, $I_{L(REF)} = 0.2$ mA			2.4	4.2	mA
	$V^+ = 20V$, $I_{L(REF)} = 1.0$ mA			6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:
$3\ V_{DC} \leq V^+ \leq 20\ V_{DC}$ V_{REF}, V_{RHI}, $V_{RLO} \leq (V^+ - 1.5V)$
$3\ V_{DC} \leq V_{LED} \leq V^+$ $0V \leq V_{IN} \leq V^+ - 1.5V$
$-0.015V \leq V_{RLO} \leq 12\ V_{DC}$ $T_A = +25°C$, $I_{L(REF)} = 0.2$ mA, $V_{LED} = 3.0V$, pin 9 connected to pin 3 (Bar Mode).
$-0.015V \leq V_{RHI} \leq 12\ V_{DC}$
For higher power dissipations, pulse testing is used.

Note 2: Accuracy is measured referred to $+10.000\ V_{DC}$ at pin 6, with $0.000\ V_{DC}$ at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+ or left open circuit. LED No. 10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

Note 5: The maximum junction temperature of the LM3914 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

Definition of Terms

Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

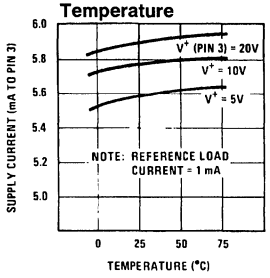
Line Regulation: The average change in reference output voltage over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage (V_{REF}) over the specified range of load current ($I_{L(REF)}$).

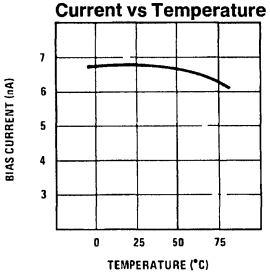
Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Typical Performance Characteristics

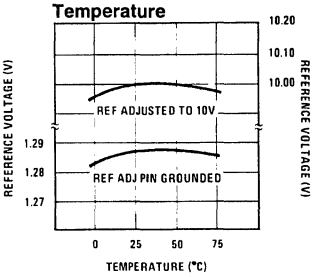
Supply Current vs Temperature



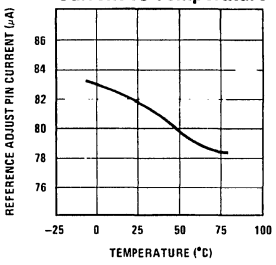
Operating Input Bias Current vs Temperature



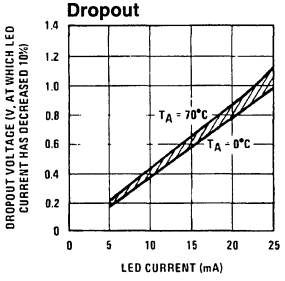
Reference Voltage vs Temperature



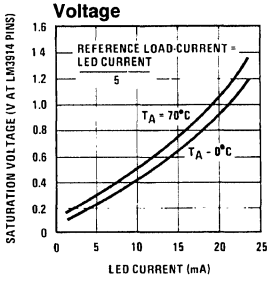
Reference Adjust Pin Current vs Temperature



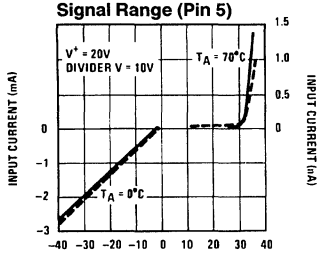
LED Current-Regulation Dropout



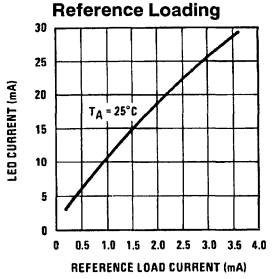
LED Driver Saturation Voltage



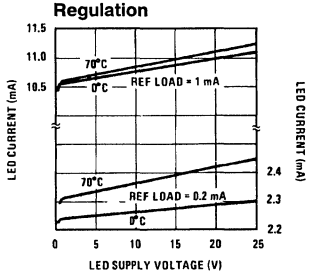
Input Current Beyond Signal Range (Pin 5)



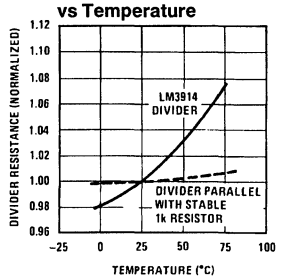
LED Current vs Reference Loading



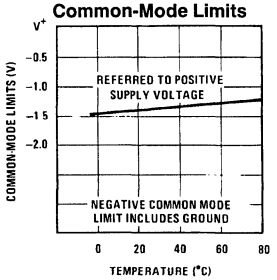
LED Driver Current Regulation



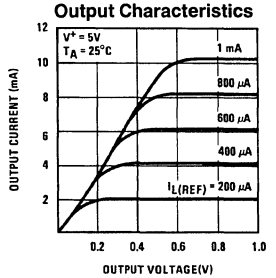
Total Divider Resistance vs Temperature



Common-Mode Limits

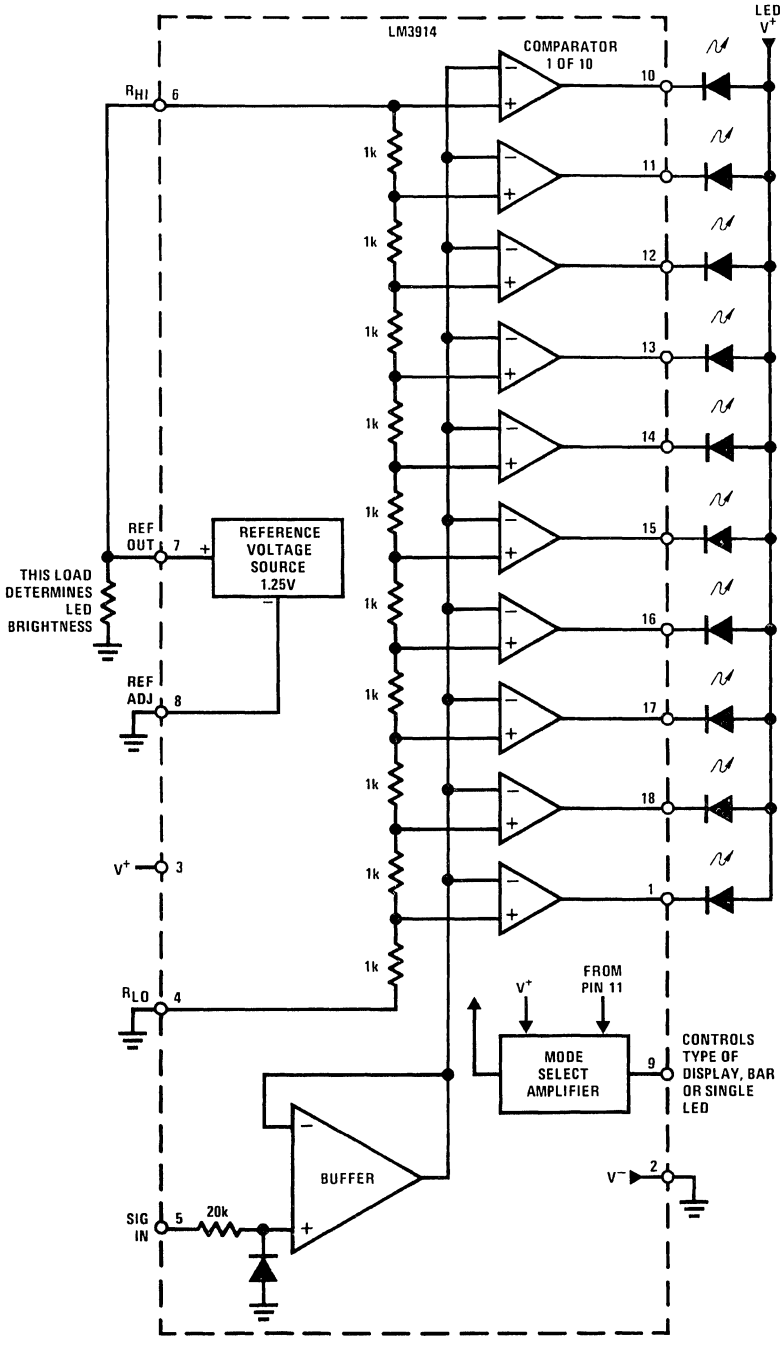


Output Characteristics



TL/H/7970–2

Block Diagram (Showing Simplest Application)



TL/H/7970–3

Functional Description

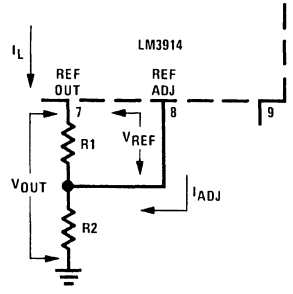
The simplifed LM3914 block diagram is to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 125 mV that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are 1.5V below V^+ and no less than V^-. If an expanded scale meter display is desired, the total divider voltage can be as little as 200 mV. Expanded-scale meter displays are more accurate and the segments light uniformly only if bar mode is used. At 50 mV or more per step, dot mode is usable.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



TL/H/7970–4

Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

MODE PIN USE

Pin 9, the Mode Select input controls chaining of multiple LM3914s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

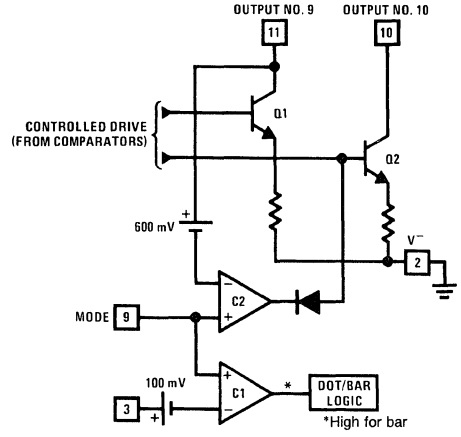
Dot Display, Single LM3914 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3914 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30, 40, or more LED displays. The last LM3914 driver in the chain will have pin 9 wired to pin 11. All previous drivers should have a 20k resistor in parallel with LED No. 9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



TL/H/7970–5

Mode Pin Functional Description (Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to ($V^+ - 100$ mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3914s are cascaded in dot mode, special circuitry has been included to shut off LED No. 10 of the first device when LED No. 1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3914, LED No. 11 is off. Pin 9 of LM3914 No. 1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED No. 11, pin 9 of LM3914 No. 1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED No. 10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED No. 9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED No. 11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3914 No. 1 is held low enough to force LED No. 10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED No. 11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED No. 10 yet small enough that LED No. 11 does not conduct significantly.

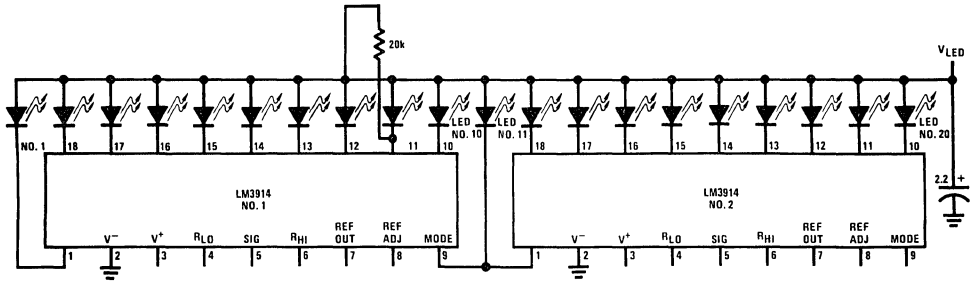
OTHER DEVICE CHARACTERISTICS

The LM3914 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA (2.5 mA max). However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3914 with a 1 mA reference pin load (1.3k), would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time between segments are all LEDs completely OFF in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range (Note 2). The change may be much more rapid between LED No. 10 of one device and LED No. 1 of a *second* device "chained" to the first.

The LM3914 features individually current regulated LED driver transistors. Further internal circuitry detects when any driver transistor goes into saturation, and prevents other circuitry from drawing excess current. This results in the ability of the LM3914 to drive and regulate LEDs powered from a pulsating DC power source, i.e., largely unfiltered. (Due to possible oscillations at low voltages a nominal bypass capacitor consisting of a 2.2 μF solid tantalum connected from the pulsating LED supply to pin 2 of the LM3914 is recommended.) This ability to operate with low or fluctuating voltages also allows the display driver to interface with logic circuitry, opto-coupled solid-state relays, and low-current incandescent lamps.

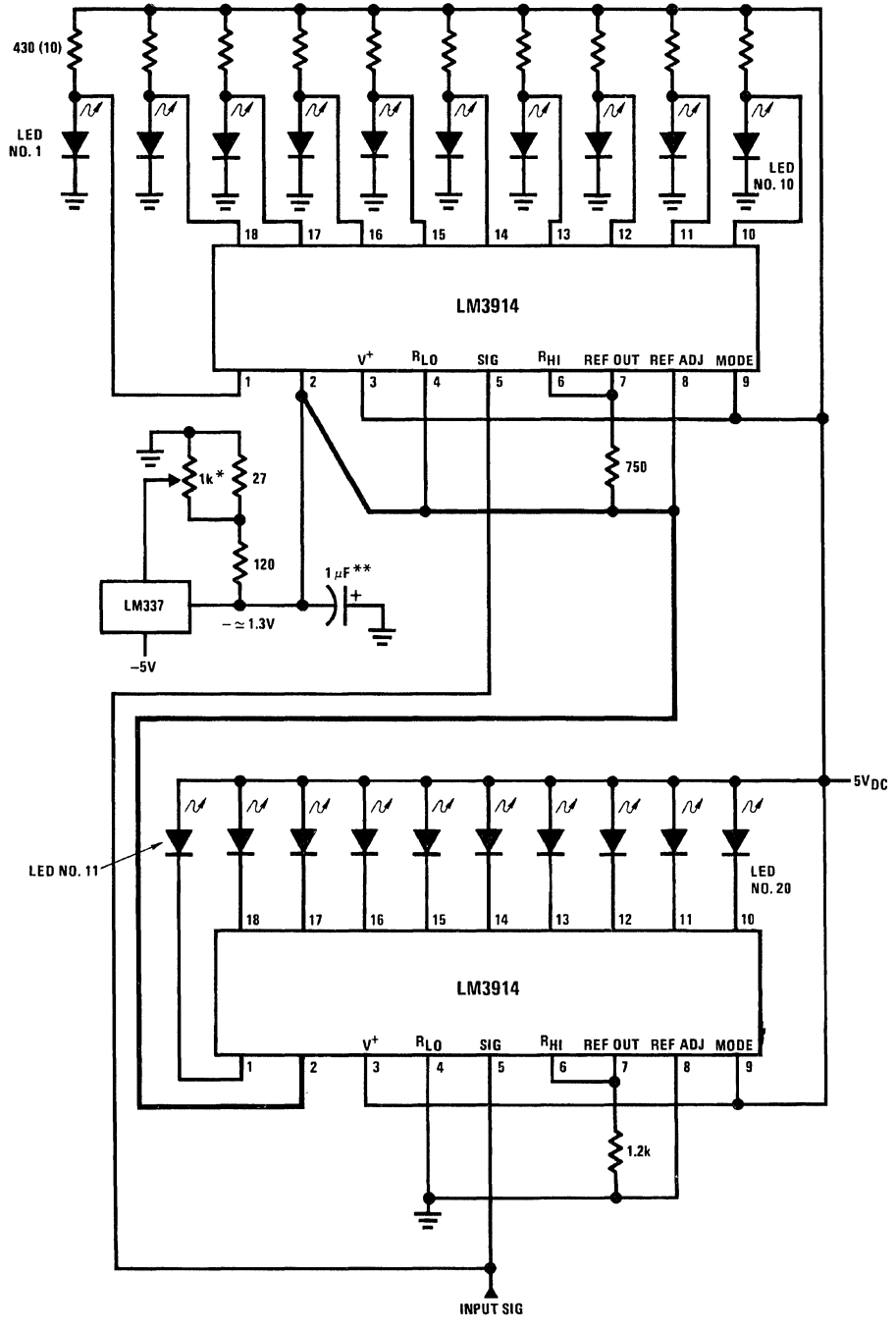
Cascading LM3914s in Dot Mode



TL/H/7970–6

Typical Applications (Continued)

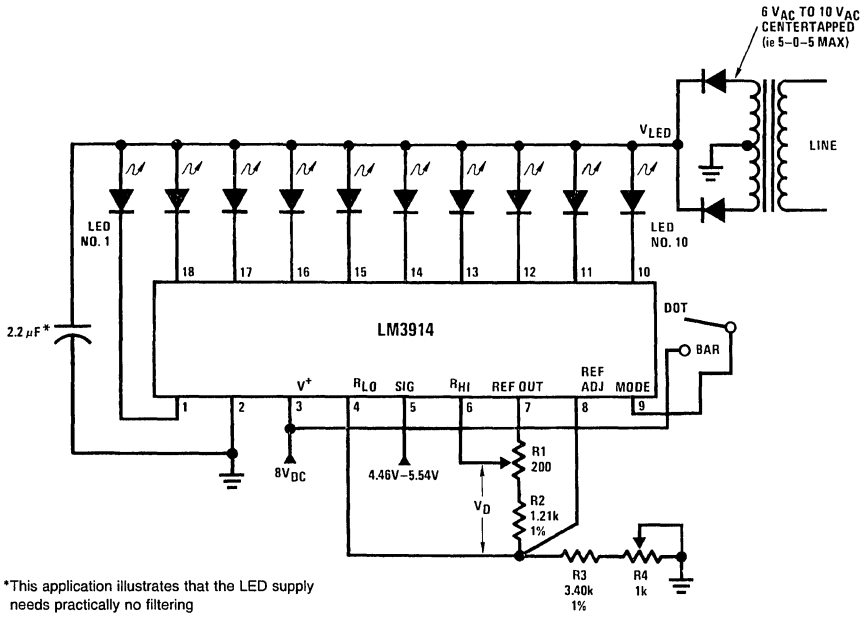
Zero-Center Meter, 20-Segment



TL/H/7970–7

Typical Applications (Continued)

Expanded Scale Meter, Dot or Bar



*This application illustrates that the LED supply needs practically no filtering

Calibration: With a precision meter between pins 4 and 6 adjust R1 for voltage V_D of 1.20V. Apply 4.94V to pin 5, and adjust R4 until LED No. 5 just lights. The adjustments are non-interacting.

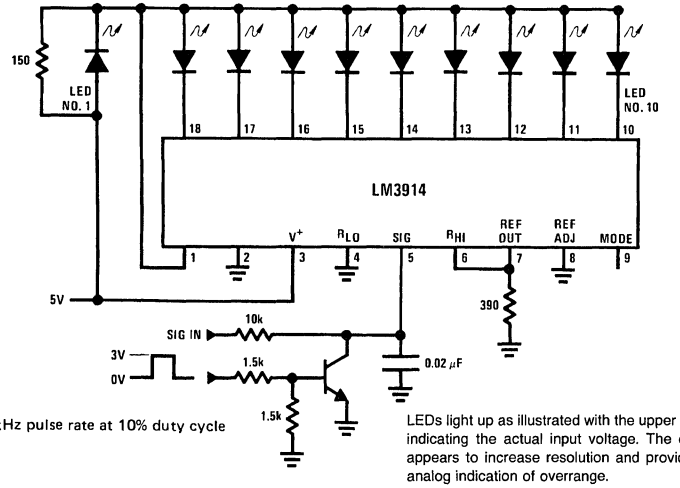
TL/H/7970–8

Application Example: Grading 5V Regulators

Highest No. LED on	Color	$V_{OUT(MIN)}$
10	Red	5.54
9	Red	5.42
8	Yellow	5.30
7	Green	5.18
6	Green	5.06
5V		
5	Green	4.94
4	Green	4.82
3	Yellow	4.7
2	Red	4.58
1	Red	4.46

Typical Applications (Continued)

"Exclamation Point" Display

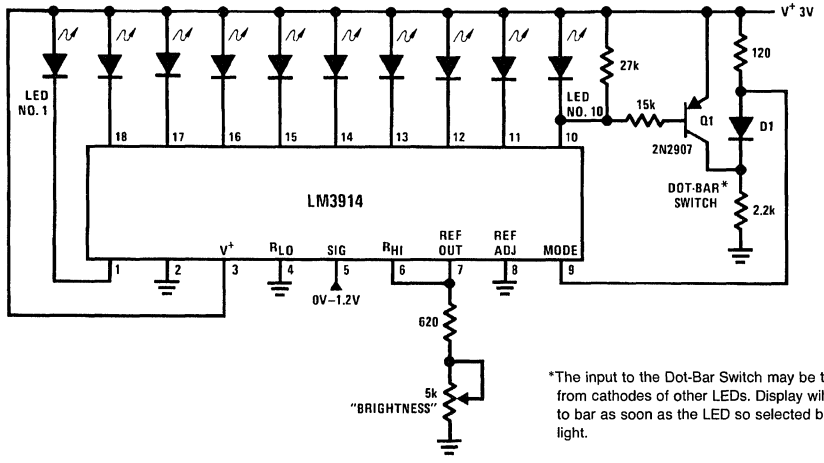


1 kHz pulse rate at 10% duty cycle

LEDs light up as illustrated with the upper lit LED indicating the actual input voltage. The display appears to increase resolution and provides an analog indication of overrange.

TL/H/7970–9

Indicator and Alarm, Full-Scale Changes Display from Dot to Bar

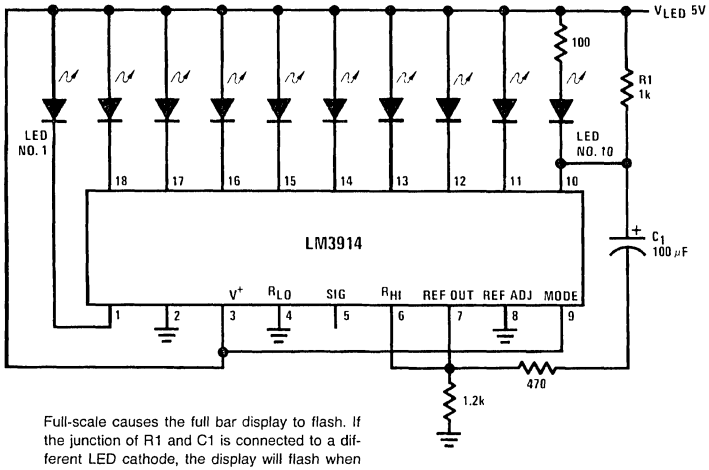


*The input to the Dot-Bar Switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

TL/H/7970–10

Typical Applications (Continued)

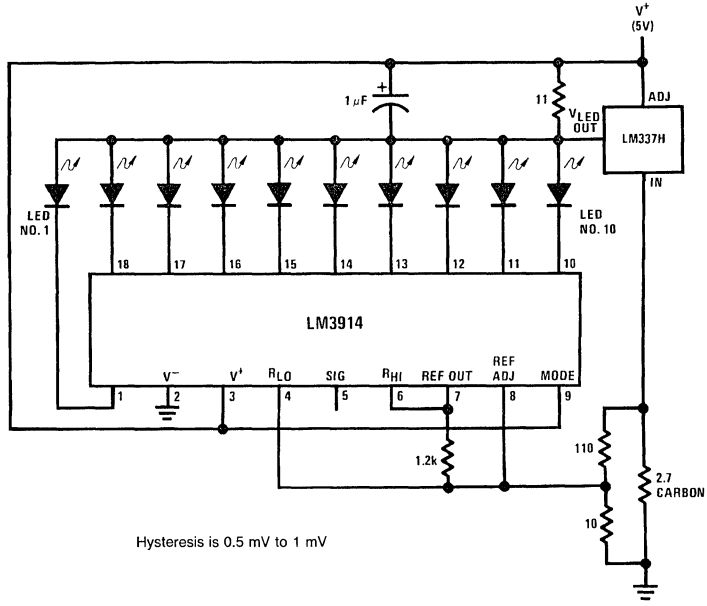
Bar Display wih Alarm Flasher



Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/7970–11

Adding Hysteresis (Single Supply, Bar Mode Only)

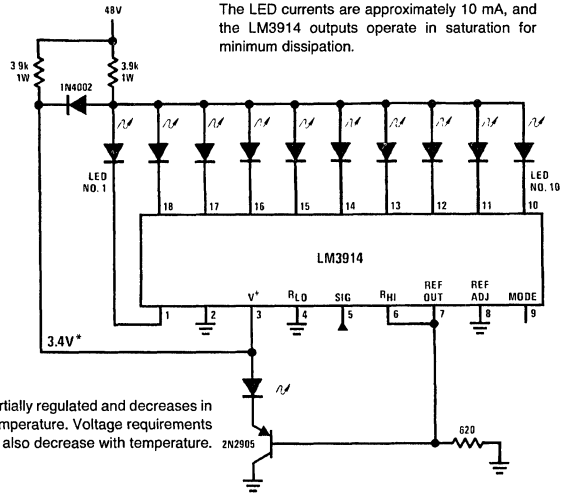


Hysteresis is 0.5 mV to 1 mV

TL/H/7970–12

Typical Application (Continued)

Operating with a High Voltage Supply (Dot Mode Only)

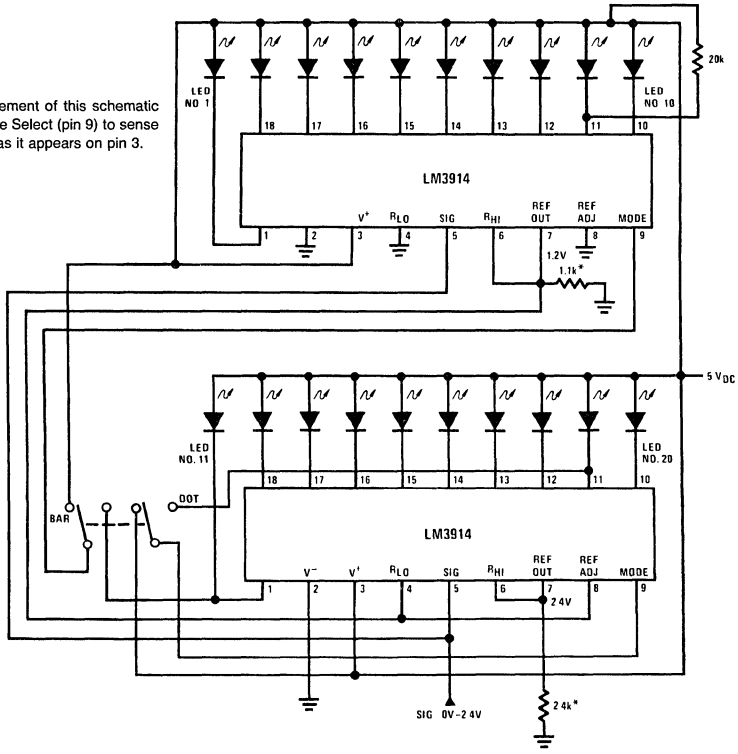


The LED currents are approximately 10 mA, and the LM3914 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3914 also decrease with temperature.

TL/H/7970–13

20-Segment Meter with Mode Switch



*The exact wiring arrangement of this schematic shows the need for Mode Select (pin 9) to sense the V+ voltage exactly as it appears on pin 3.

*Programs LEDs to 10 mA

TL/H/7970–14

Application Hints

Three of the most commonly needed precautions for using the LM3914 are shown in the first typical application drawing (see page 9-108) showing a 0V–5V bar graph meter. The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string (as illustrated) to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 μF to 2.2 μF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits (see Note 2, page 9-108). Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 μF capacitor, or up to 0.1 μF in noisy environments.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum capacitor to pin 2 of the LM3914.

Turning OFF of most of the internal current sources is accomplished by pulling positive on the reference with a current source or resistance supplying 100 μA or so. Alternately, the input signal can be gated OFF with a transistor switch.

Other special features and applications characteristics will be illustrated in the following applications schematics. Notes have been added in many cases, attempting to cover any special procedures or unusual characteristics of these applications. A special section called "Application Tips for the LM3914 Adjustable Reference" has been included with these schematics.

APPLICATION TIPS FOR THE LM3914 ADJUSTABLE REFERENCE

GREATLY EXPANDED SCALE (BAR MODE ONLY)

Placing the LM3914 internal resistor divider in parallel with a section ($\cong$230Ω) of a stable, low resistance divider greatly reduces voltage changes due to IC resistor value changes with temperature. Voltage V_1 should be trimmed to 1.1V first by use of R2. Then the voltage V_2 across the IC divider string can be adjusted to 200 mV, using R5 without affecting V_1. LED current will be approximately 10 mA.

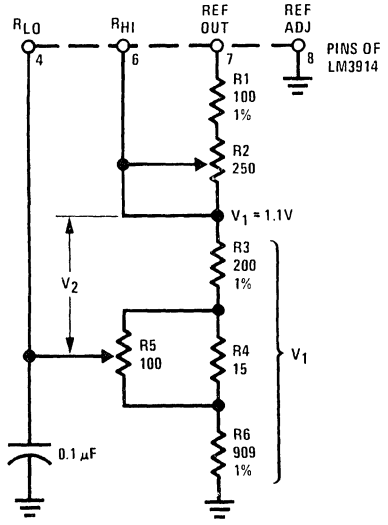
NON-INTERACTING ADJUSTMENTS FOR EXPANDED SCALE METER (4.5V to 5V, Bar *or* Dot Mode)

This arrangement allows independent adjustment of LED brightness regardless of meter span and zero adjustments.

First, V_1 is adjusted to 5V, using R2. Then the span (voltage across R4) can be adjusted to exactly 0.5V using R6 without affecting the previous adjustment.

R9 programs LED currents within a range of 2.2 mA to 20 mA after the above settings are made.

Greatly Expanded Scale (Bar Mode Only)



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ADJUSTING LINEARITY OF SEVERAL STACKED DIVIDERS

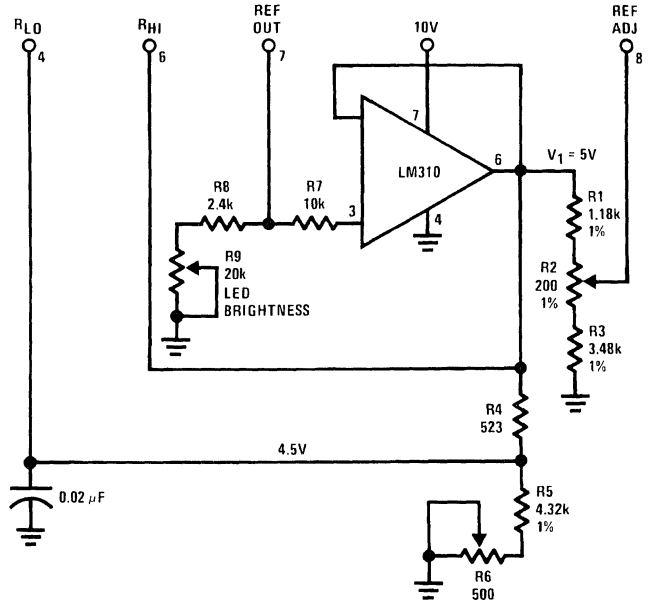
Three internal voltage dividers are shown connected in series to provide a 30-step display. If the resulting analog meter is to be accurate and linear the voltage on each divider must be adjusted, preferably without affecting any other adjustments. To do this, adjust R2 first, so that the voltage across R5 is exactly 1V. Then the voltages across R3 and R4 can be independently adjusted by shunting each with selected resistors of 6 kΩ or higher resistance. This is possible because the reference of LM3914 No. 3 is acting as a constant current source.

The references associated with LM3914s No. 1 and No. 2 should have their Ref Adj pins (pin 8) wired to ground, and their Ref Outputs loaded by a 620Ω resistor to ground. This makes available similar 20 mA current outputs to all the LEDs in the system.

If an independent LED brightness control is desired (as in the previous application), a unity gain buffer, such as the LM310, should be placed between pin 7 and R1, similar to the previous application.

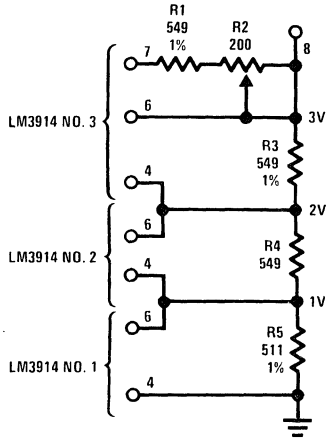
Application Hints (Continued)

Non-Interacting Adjustments for Expanded Scale Meter (4.5V to 5V, Bar *or* Dot Mode)



TL/H/7970–16

Adjusting Linearity of Several Stacked Dividers



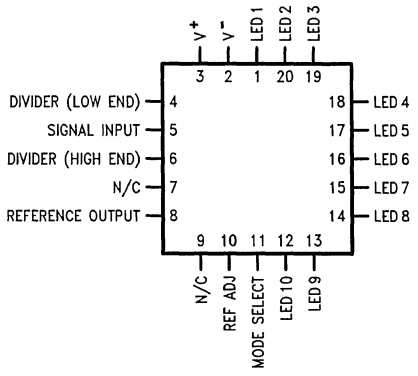
TL/H/7970–17

Other Applications

- "Slow"—fade bar or dot display (doubles resolution)
- 20-step meter with single pot brightness control
- 10-step (or multiples) programmer
- Multi-step or "staging" controller
- Combined controller and process deviation meter
- Direction and rate indicator (to add to DVMs)
- Exclamation point display for power saving
- Graduations can be added to dot displays. Dimly light every other LED using a resistor to ground
- Electronic "meter-relay"—display could be circle or semi-circle
- Moving "hole" display—indicator LED is dark, rest of bar lit
- Drives vacuum-fluorescent and LCDs using added passive parts

Connection Diagrams

Plastic Chip Carrier Package

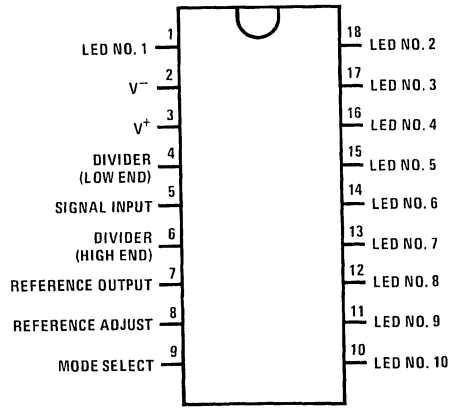


TL/H/7970–18

Top View

Order Number LM3914V
See NS Package Number V20A
(ADVANCED INFORMATION)

Dual-In-Line Package



TL/H/7970–19

Top View

Order Number LM3914N
See NS Package Number N18A

5

National Semiconductor Corporation

LM3915 Dot/Bar Display Driver

General Description

The LM3915 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing a logarithmic 3 dB/step analog display. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 1 dB.

The LM3915's 3 dB/step display is suited for signals with wide dynamic range, such as audio level, power, light intensity or vibration. Audio applications include average or peak level indicators, power meters and RF signal strength meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3915 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3915 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display with a range of 60 or 90 dB. LM3915s can also be cascaded with LM3914s for a linear/log display or with LM3916s for an extended-range VU meter.

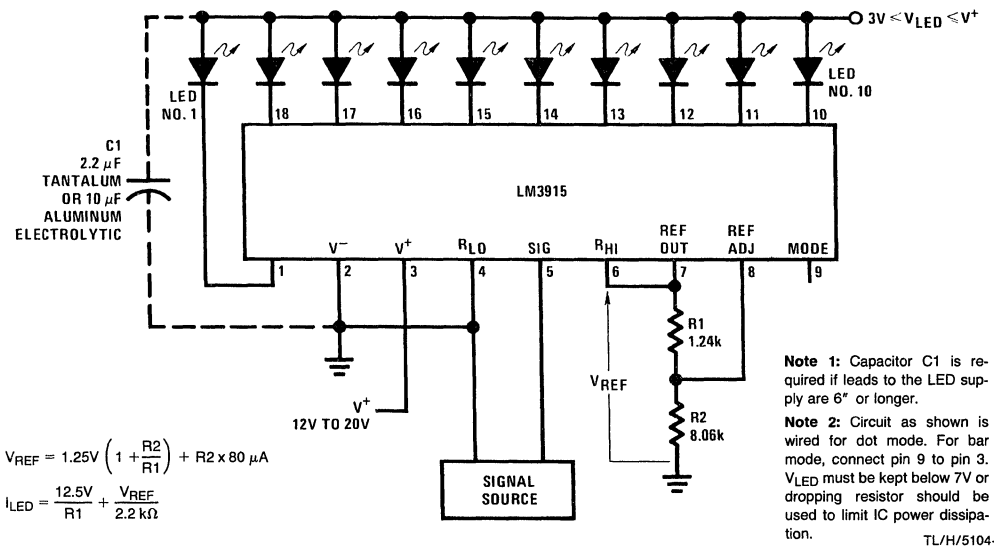
Features

- 3 dB/step, 30 dB range
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 90 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3915 is rated for operation from 0°C to +70°C. The LM3915N is available in an 18-lead molded DIP package.

Typical Applications

0V to 10V Log Display



$$V_{REF} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \times 80\,\mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\,k\Omega}$$

Note 1: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Note 2: Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation (Note 5)	
Molded DIP(N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
Comparators					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{L(REF)} = 2$ mA, $I_{LED} = 10$ mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le (V^+ - 1.5V)$		25	100	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
Voltage-Divider					
Divider Resistance	Total, Pin 6 to 4	16	28	36	kΩ
Relative Accuracy (Input Change Between Any Two Threshold Points)	(Note 2)	2.0	3.0	4.0	dB
Absolute Accuracy at Each Threshold Point	(Note 2)				
	$V_{IN} = -3, -6$ dB	−0.5		+0.5	dB
	$V_{IN} = -9$ dB	−0.5		+0.65	dB
	$V_{IN} = -12, -15, -18$ dB	−0.5		+1.0	dB
	$V_{IH} = -21, -24, -27$ dB	−0.5		+1.5	dB
Voltage Reference					
Output Voltage	$0.1 \text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$		0.01	0.03	%/V
Load Regulation	$0.1 \text{ mA} \le I_{L(REF)} \le 4$ mA, $V^+ = V_{LED} = 5V$		0.4	2	%
Output Voltage Change with Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = V_{LED}$ 5V		1		%
Adjust Pin Current			75	120	μA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
Output Drivers					
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$, $I_{LED} = 2$ mA		0.12	0.4	mA
	$V_{LED} = 5V$, I_{LED} 20 mA		1.2	3	mA
LED Current Regulation	$2V \le V_{LED} \le 17V$, $I_{LED} = 2$ mA		0.1	0.25	mA
	$I_{LED} = 20$ mA		1	3	mA
Dropout Voltage	$I_{LED(ON)} = 20$ mA @ $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA			1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA		0.15	0.4	V
Output Leakage, Each Collector	Bar Mode (Note 4)		0.1	10	μA
Output Leakage	Dot Mode (Note 4)				
Pins 10-18			0.1	10	μA
Pin 1		60	150	450	μA
Supply Current					
Standby Supply Current (All Outputs Off)	$V^+ = +5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
	$V^+ = +20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $\quad -0.015V \le V_{RLO} \le 12\ V_{DC}$ $\quad T_A = 25°C$, $I_{L(REF)} = 0.2$ mA, pin 9 connected to pin 3 (bar mode).

$3\ V_{DC} \le V_{LED} \le V^+$ $\quad V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$ For higher power dissipations, pulse testing is used.

$-0.015V \le V_{RHI} \le 12\ V_{DC}$ $\quad 0V \le V_{IN} \le V^+ - 1.5V$

Note 2: Accuracy is measured referred to 0 dB = + 10.000 V_{DC} at pin 5, with + 10.000 V_{DC} at pin 6, and 0.000 V_{DC} at pin 4. At lower full scale voltages, buffer and comparator offset voltage may add significant error. See table for threshold voltages.

Note 3: Pin 5 input current must be limited to ±3 mA. The addition of a 39k resistor in series with pin 5 allows ±100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+. LED #10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

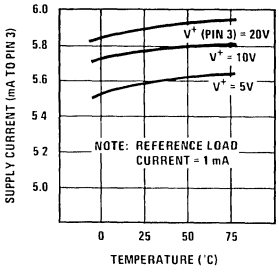
Note 5: The maximum junction temperature of the LM3915 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

THRESHOLD VOLTAGE (Note 2)

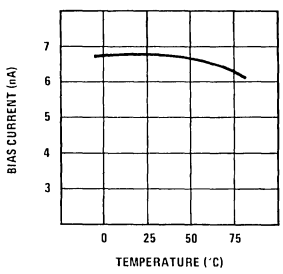
Output	dB	Min	Typ	Max	Output	dB	Min	Typ	Max
1	−27	0.422	0.447	0.531	6	−12	2.372	2.512	2.819
2	−24	0.596	0.631	0.750	7	−9	3.350	3.548	3.825
3	−21	0.841	0.891	1.059	8	−6	4.732	5.012	5.309
4	−18	1.189	1.259	1.413	9	−3	6.683	7.079	7.498
5	−15	1.679	1.778	1.995	10	0	9.985	10	10.015

Typical Performance Characteristics

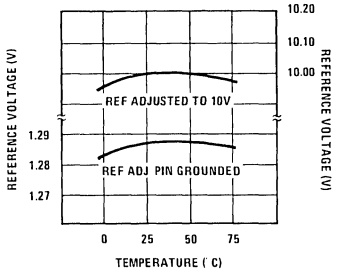
Supply Current vs Temperature



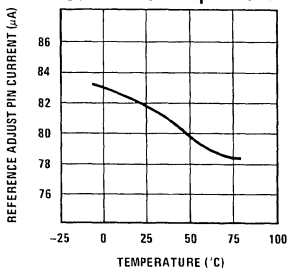
Operating Input Bias Current vs Temperature



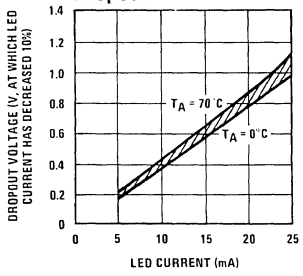
Reference Voltage vs Temperature



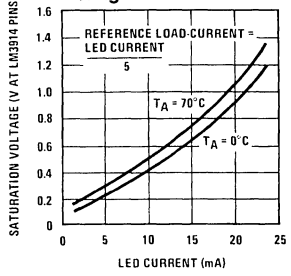
Reference Adjust Pin Current vs Temperature



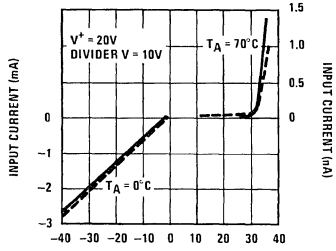
LED Current-Regulation Dropout



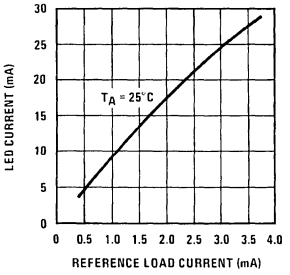
LED Driver Saturation Voltage



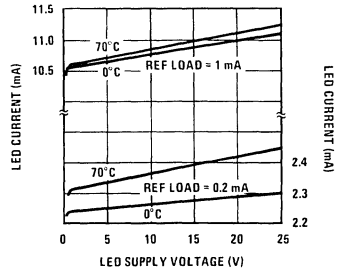
Input Current Beyond Signal Range (Pin 5)



LED Current vs Reference Loading

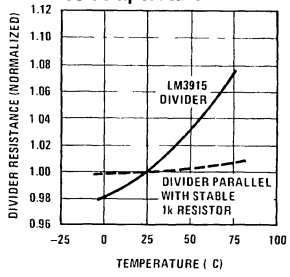


LED Driver Current Regulation

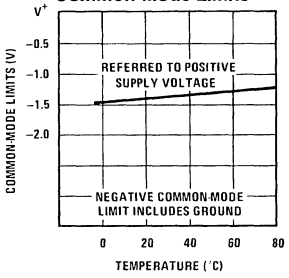


TL/H/5104–2

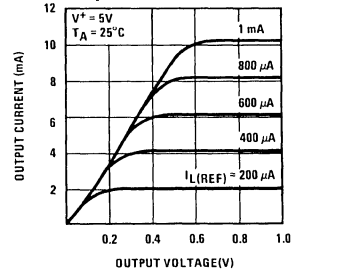
Total Divider Resistance vs Temperature



Common-Mode Limits

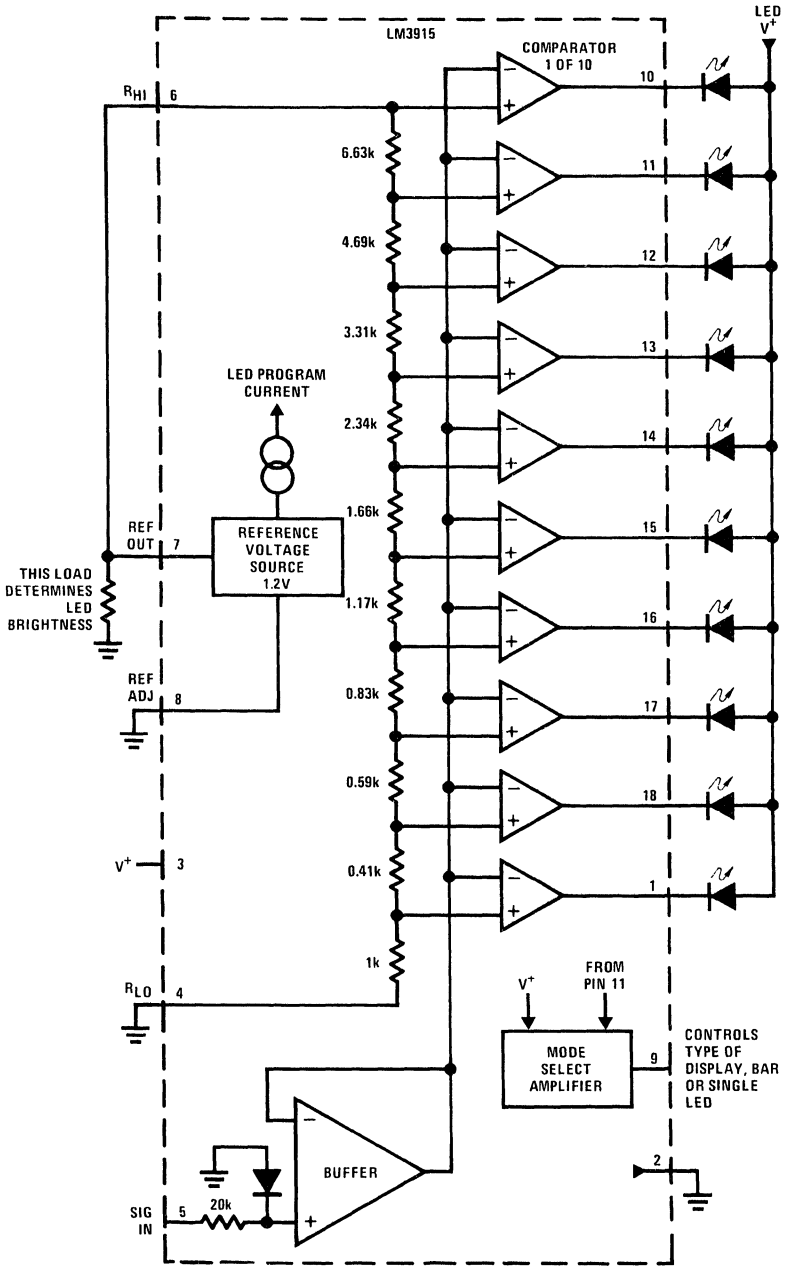


Output Characteristics



TL/H/5104–3

Block Diagram (Showing Simplest Application)



TL/H/5104–4

Functional Description

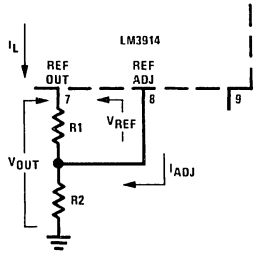
The simplified LM3915 block diagram is included to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. In this case, for each 3 dB that the input signal increases, a comparator will switch on another indicating LED. This resistor divider can be connected between any 2 voltages, providing that they are at least 1.5V below V^+ and no lower than V^-.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



TL/H/5104–5

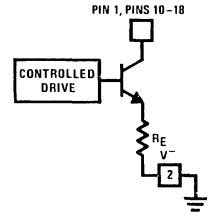
Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes. For correct operation, reference load current should be between 80 μA and 5 mA. Load capacitance should be less than 0.05 μF.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

The LM3915 outputs are current-limited NPN transistors as shown below. An internal feedback loop regulates the transistor drive. Output current is held at about 10 times the reference load current, independent of output voltage and processing variables, as long as the transistor is not saturated.

LM3915 Output Circuit



TL/H/5104–6

Outputs may be run in saturation with no adverse effects, making it possible to directly drive logic. The effective saturation resistance of the output transistors, equal to R_E plus the transistors' collector resistance, is about 50Ω. It's also possible to drive LEDs from rectified AC with no filtering. To avoid oscillations, the LED supply should be bypassed with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor.

MODE PIN USE

Pin 9, the Mode Select input, permits chaining of multiple LM3915s, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

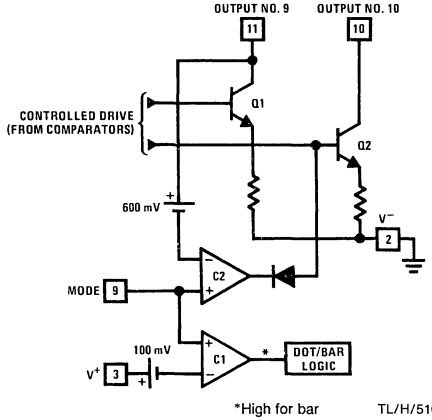
Dot Display, Single LM3915 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* driver in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3915 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30 or more LED displays. The last LM3915 driver in the chain will have pin 9 left open. All previous drivers should have a 20k resistor in parallel with LED #9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



*High for bar

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Mode Pin Functional Description
(Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to (V^+ − 100 mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for the display to make sense when multiple LM3915s are cascaded in dot mode, special circuitry has been included to shut off LED #10 of the first device when LED #1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted below.

As long as the input signal voltage is below the threshold of the second LM3915, LED #11 is off. Pin 9 of LM3915 #1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED #11, pin 9 of LM3915 #1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED #10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED #9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED #11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of LM3915 #1 is held low enough to force LED #10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED #11 with a 10k resistor. The 1V IR drop is more than the 900 mV worst case required to hold off LED #10 yet small enough that LED #11 does not conduct significantly.

OTHER DEVICE CHARACTERISTICS

The LM3916 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA. However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3916 with a 1 mA reference pin load (1.3k) would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time are all segments completely off in the dot mode. Generally 1 LED fades in while the other fades out over a mV or more of range. The change may be much more rapid between LED #10 of one device and LED #1 of a *second* device "chained" to the first.

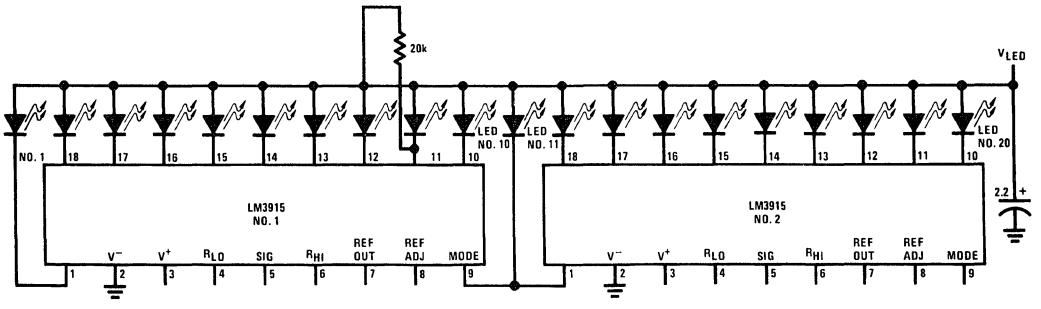
Application Hints

The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. Depending on the severity of the problem 0.05 μF to 2.2 μF decoupling capacitors from LED anode common to pin 2 will damp the circuit. If LED anode line wiring is inaccessible, often similar decoupling from pin 1 to pin 2 will be sufficient.

If LED turn ON seems slow (bar mode) or several LEDs light (dot mode), oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with at least a 0.001 μF capacitor, or up to 0.1 μF in noisy environments.

Cascading LM3915s in Dot Mode



TL/H/5104–8

Application Hints (Continued)

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum capacitor to pin 2.

TIPS ON RECTIFIER CIRCUITS

The simplest way to display an AC signal using the LM3915 is to apply it right to pin 5 unrectified. Since the LED illuminated represents the instantaneous value of the AC waveform, one can readily discern both peak and average values of audio signals in this manner. The LM3915 will respond to positive half-cycles only but will not be damaged by signals up to ±35V (or up to ±100V if a 39k resistor is in series with the input). It's recommended to use dot mode and to run the LEDs at 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an LM3915 is set up with 10V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier won't work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in *Figure 1* uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single LM3915 is used for a 30 dB display.

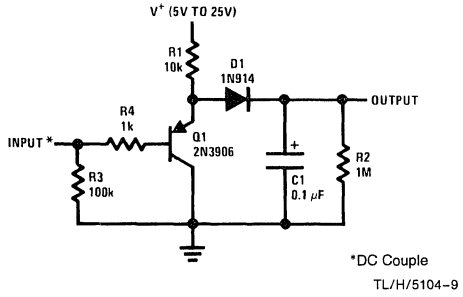
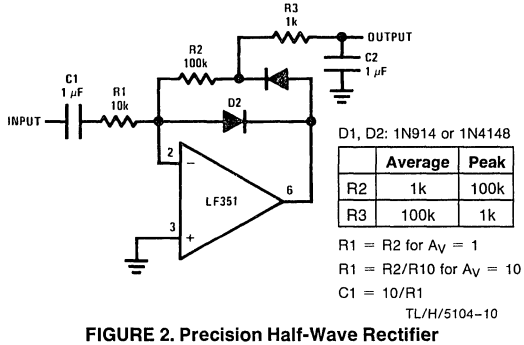


FIGURE 1. Half-Wave Peak Detector

Display circuits using two or more LM3915s for a dynamic range of 60 dB or greater require more accurate detection. In the precision half-wave rectifier of *Figure 2* the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

It's best to capacitively couple the input. Audio sources frequently have a small DC offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the LF351, LF353, or LF356, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp DC offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level AC signal (10 to 20 mV) is applied, rather than adjusting for zero output with zero input.

For precision full-wave averaging use the circuit in *Figure 3*. Using 1% resistors for R1 through R4, gain for positive and negative signal differs by only 0.5 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2 dB gain difference means that the display may have a ±1 dB error when the input is a nonsymmetrical transient). The averaging time constant is R5–C2. A simple modification results in the precision full-wave detector of *Figure 4*. Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of an LM3915.



	Average	Peak
R2	1k	100k
R3	100k	1k

FIGURE 2. Precision Half-Wave Rectifier

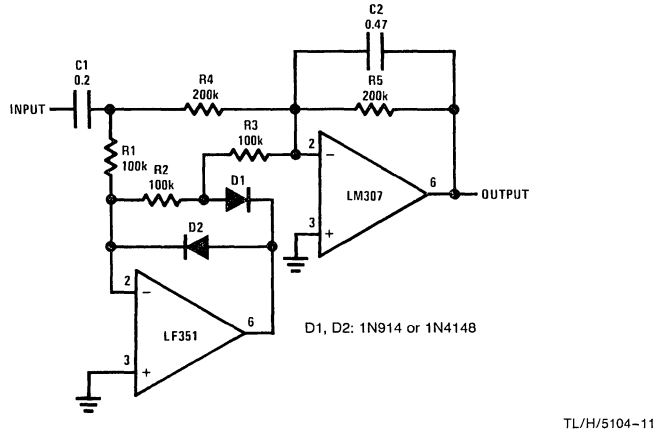


FIGURE 3. Precision Full-Wave Average Detector

Application Hints (Continued)

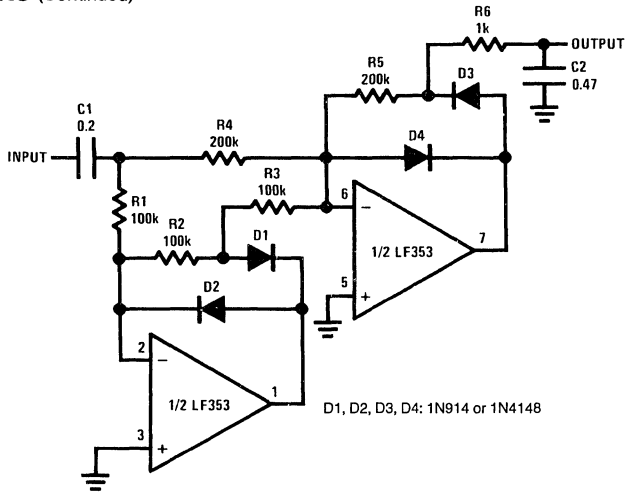


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FIGURE 4. Precision Full-Wave Peak Detector

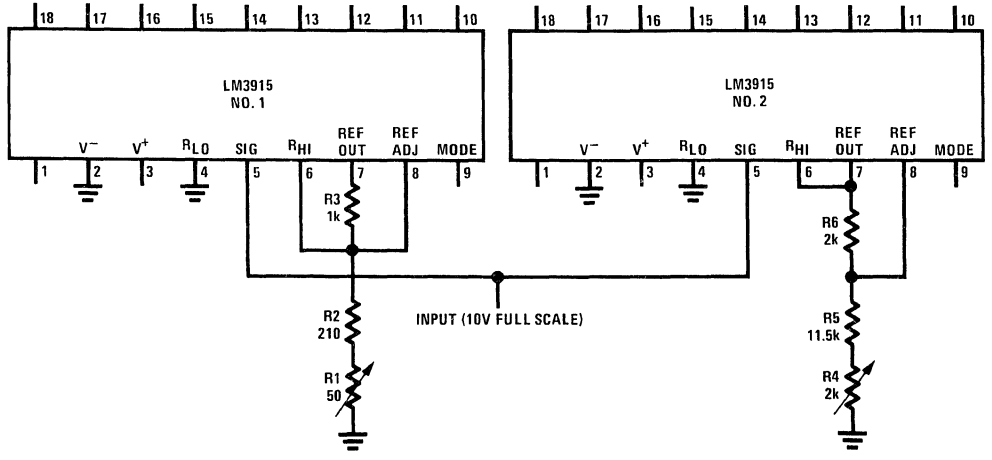
CASCADING THE LM3915

To display signals of 60 or 90 dB dynamic range, multiple LM3915s can be easily cascaded. Alternatively, it is possible to cascade an LM3915 with LM3914s for a log/linear display or with an LM3916 to get an extended range VU meter.

A simple, low cost approach to cascading two LM3915s is to set the reference voltages of the two chips 30 dB apart as in *Figure 5*. Potentiometer R1 is used to adjust the full scale voltage of LM3915 #1 to 316 mV nominally while the second IC's reference is set at 10V by R4. The drawback of this method is that the threshold of LED #1 is only 14 mV and, since the LM3915 can have an offset voltage as high as 10 mV, large errors can occur. This technique is not recommended for 60 dB displays requiring good accuracy at the first few display thresholds.

A better approach shown in *Figure 6* is to keep the reference at 10V for both LM3915s and amplify the input signal to the lower LM3915 by 30 dB. Since two 1% resistors can set the amplifier gain within ±0.2 dB, a gain trim is unnecessary. However, an op amp offset voltage of 5 mV will shift the first LED threshold as much as 4 dB, so that an offset trim may be required. Note that a single adjustment can null out offset in both the precision rectifier and the 30 dB gain stage. Alternatively, instead of amplifying, input signals of sufficient amplitude can be fed directly to the lower LM3915 and *attenuated* by 30 dB to drive the second LM3915.

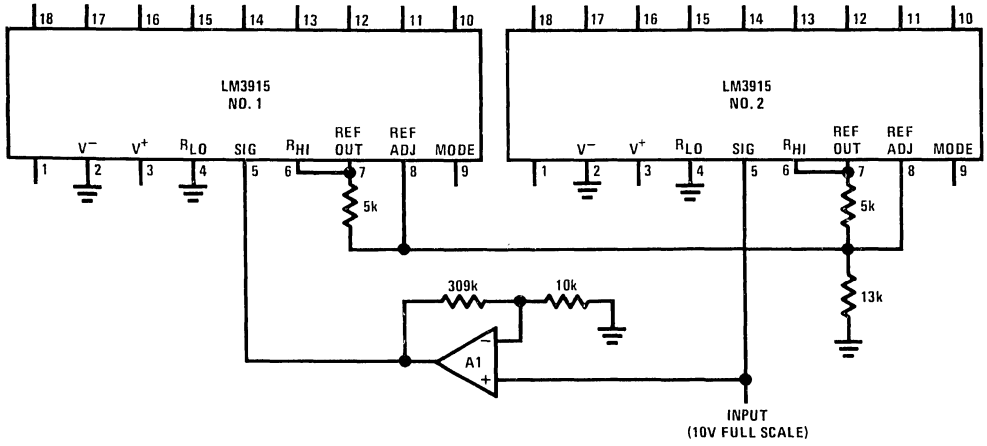
To extend this approach to get a 90 dB display, another 30 dB of amplification must be placed in the signal path ahead of the lowest LM3915. Extreme care is required as the lowest LM3915 displays input signals down to 0.5 mV! Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.



TL/H/5104–13

FIGURE 5. Low Cost Circuit for 60 dB Display

Application Hints (Continued)



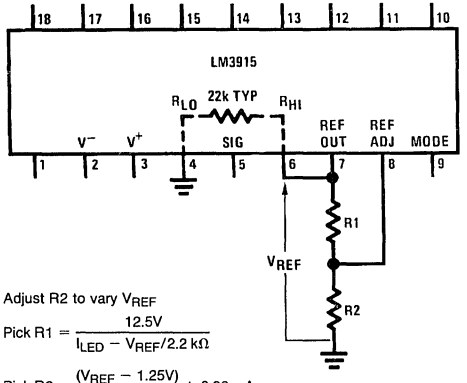
TL/H/5104–14

FIGURE 6. Improved Circuit for 60 dB Display

TIPS ON REFERENCE VOLTAGE AND LED CURRENT PROGRAMMING

SINGLE LM3915

The equations in *Figure 7* illustrate how to choose resistor values to set reference voltage for the simple case where no LED intensity adjustment is required. A LED current of 10 mA to 20 mA generally produces adequate illumination. Having 10V full-scale across the internal voltage divider gives best accuracy by keeping signal level high relative to the offset voltage of the internal comparators. However, this causes 450 μA to flow from pin 7 into the divider which means that the LED current will be at least 5 mA. R1 will typically be between 1 kΩ and 2 kΩ. To trim the reference voltage, vary R2.



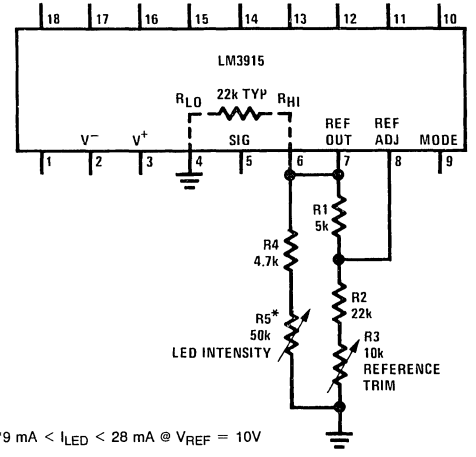
TL/H/5104–15

FIGURE 7. Design Equations for Fixed LED Intensity

The circuit in *Figure 8* shows how to add a LED intensity control which can vary LED current from 9 mA to 28 mA. The reference adjustment has some effect on LED intensity but the reverse is not true.

MULTIPLE LM3915s

Figure 9 shows how to obtain a common reference trim and intensity control for two LM3915s. The two ICs may be connected in cascade for a 60 dB display or may be handling separate channels for stereo. This technique can be extended for larger numbers of LM3915s by varying the values of R1, R2 and R3 in inverse proportion to the number of devices tied in. The ICs' internal references track within 100 mV so that worst case error from chip to chip is only 0.1 dB for V_{REF} = 10V.



TL/H/5104–16

FIGURE 8. Varying LED Intensity

Application Hints (Continued)

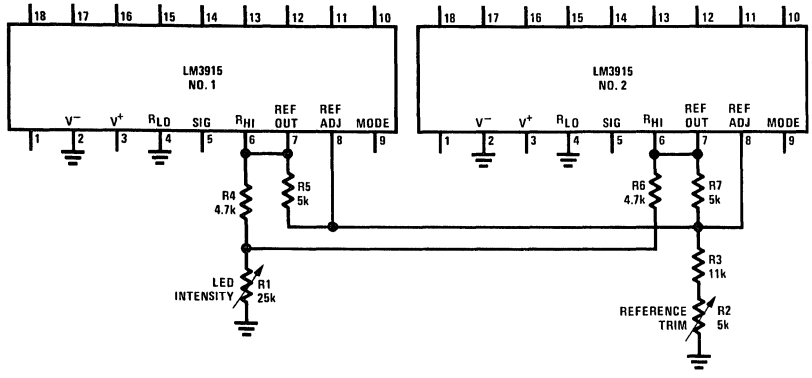


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FIGURE 9. Independent Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

The scheme in *Figure 10* is useful when the reference and LED intensity must be adjusted independently over a wide range. The R_{HI} voltage can be adjusted from 1.2V to 10V with no effect on LED current. Since the internal divider here does not load down the reference, minimum LED current is much lower. At the minimum recommended reference load of 80 μA, LED current is about 0.8 mA. The resistor values shown give a LED current range from 1.5 mA to 20 mA.

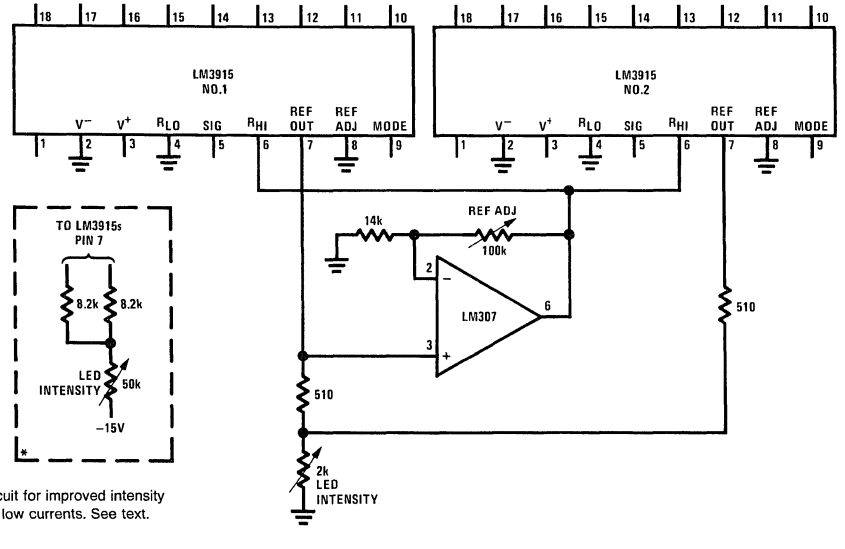
At the low end of the intensity adjustment, the voltage drop across the 510Ω current-sharing resistors is so small that chip to chip variation in reference voltage may yield a visible variation in LED intensity. The optional approach shown of connecting the bottom end of the intensity control pot to a negative supply overcomes this problem by allowing a larger voltage drop across the (larger) current-sharing resistors.

Other Applications

For increased resolution, it's possible to obtain a display with a smooth transition between LEDs. This is accomplished by varying the reference level at pin 6 by 3 dBp-p as shown in *Figure 11*. The signal can be a triangle, sawtooth or sine wave from 60 Hz to 1 kHz. The display can be run in either dot or bar mode.

When an exponentially decaying RC discharge waveform is applied to pin 5, the LM3915's outputs will switch at equal intervals. This makes a simple timer or sequencer. Each time interval is equal to RC/3. The output may be used to drive logic, opto-couplers, relays or PNP transistors, for example.

Typical Applications



*Optional circuit for improved intensity matching at low currents. See text.

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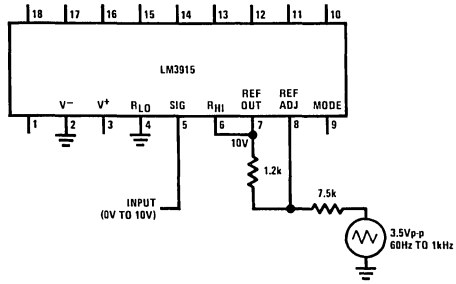
FIGURE 10. Wide-Range Adjustment of Reference Voltage and LED Intensity for Multiple LM3915s

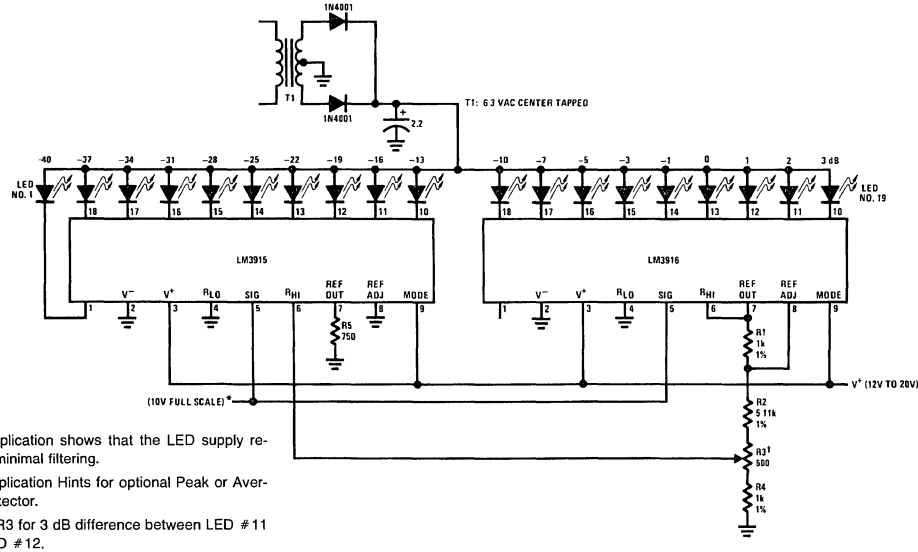
Typical Applications (Continued)



TL/H/5104–19

FIGURE 11. 0V to 10V Log Display with Smooth Transitions

Extended Range VU Meter



This application shows that the LED supply requires minimal filtering.

*See Application Hints for optional Peak or Average Detector.

†Adjust R3 for 3 dB difference between LED #11 and LED #12.

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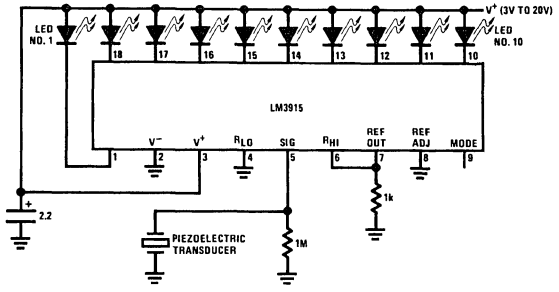
Vibration Meter



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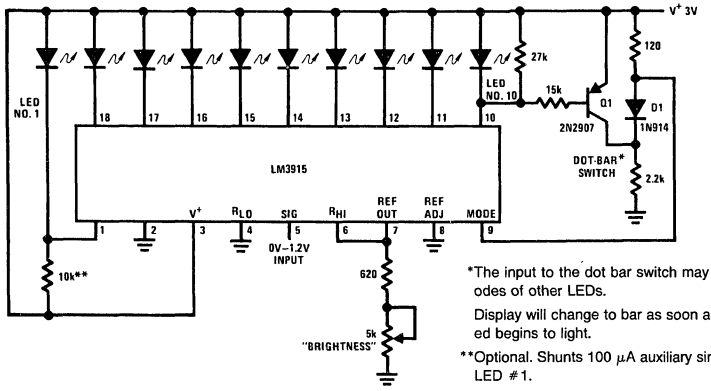
LED	Threshold
1	60 mV
2	80 mV
3	110 mV
4	160 mV
5	220 mV
6	320 mV
7	440 mV
8	630 mV
9	890 mV
10	1.25V

Typical Applications (Continued)

Indicator and Alarm, Full-Scale Changes Display From Dot to Bar



*The input to the dot bar switch may be taken from cathodes of other LEDs.

Display will change to bar as soon as the LED so selected begins to light.

**Optional. Shunts 100 μA auxiliary sink current away from LED #1.

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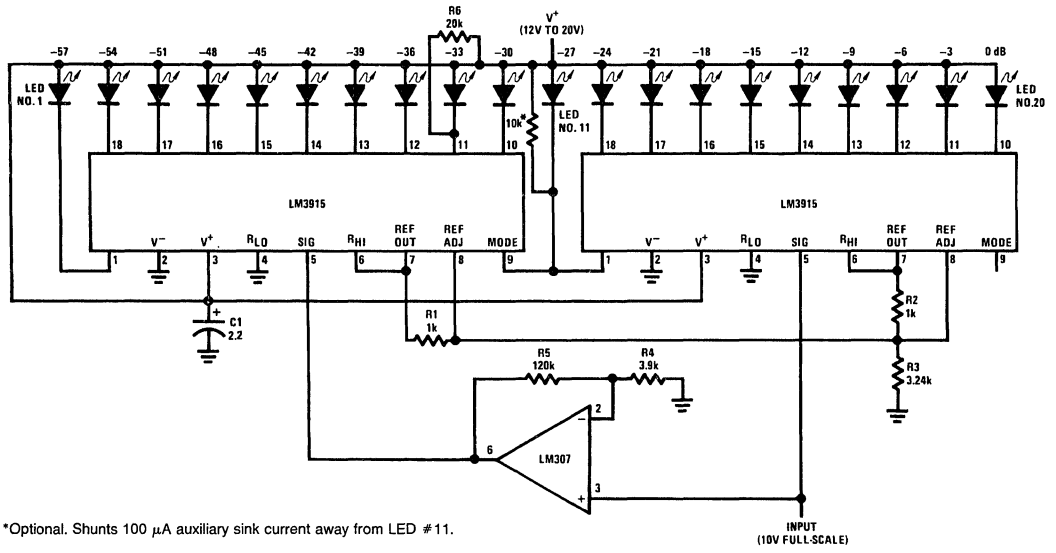
60 dB Dot Mode Display



*Optional. Shunts 100 μA auxiliary sink current away from LED #11.

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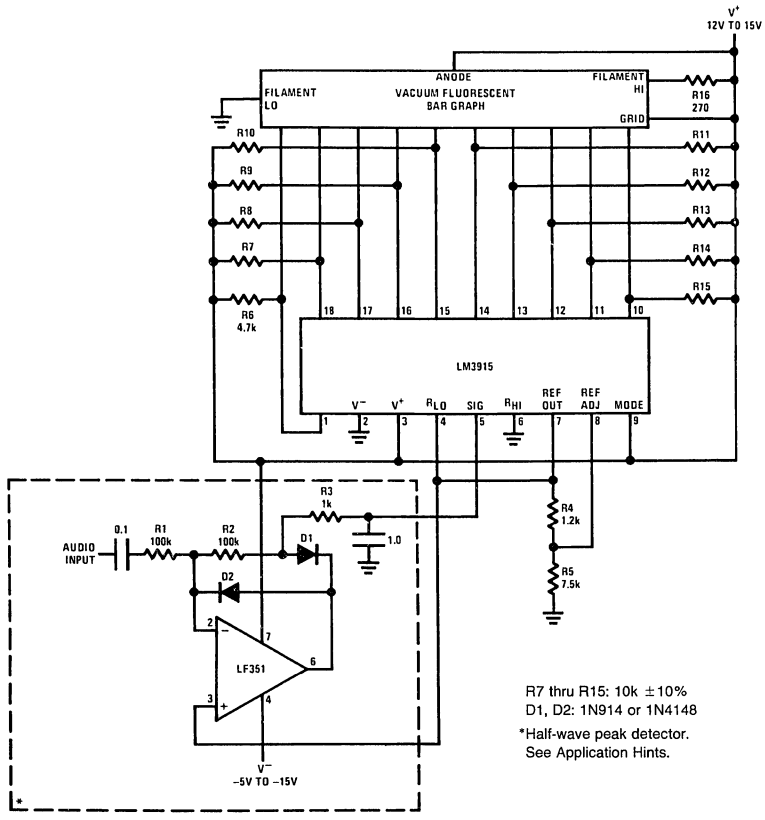
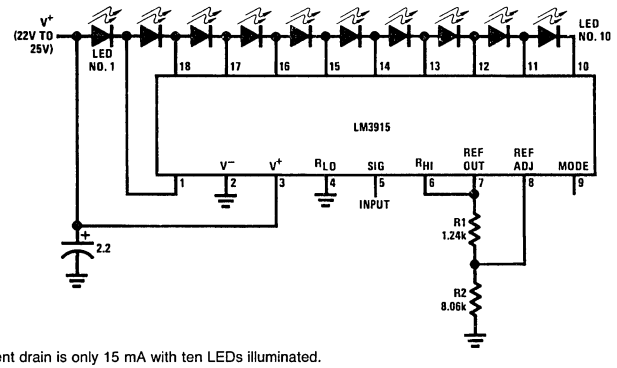
Typical Applications (Continued)

Driving Vacuum Fluorescent Display



TL/H/5104–24

Low Current Bar Mode Display

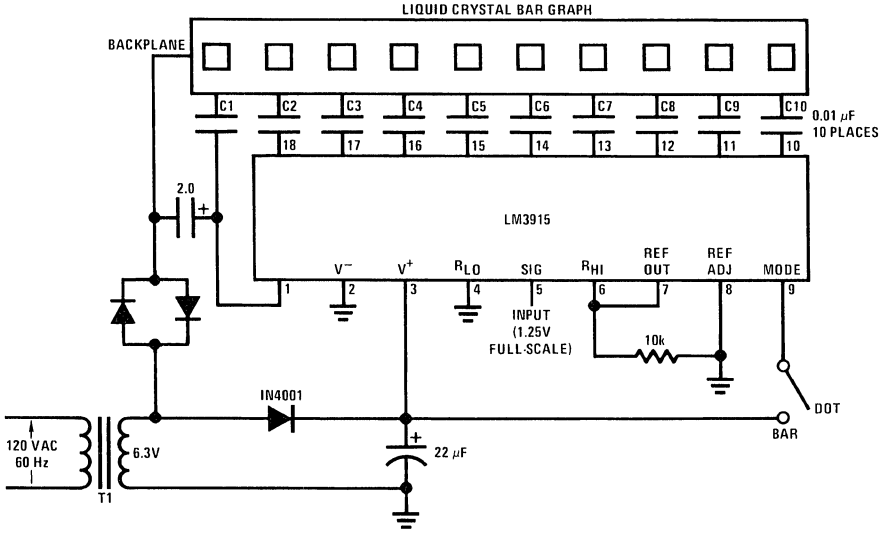


Supply current drain is only 15 mA with ten LEDs illuminated.

TL/H/5104–25

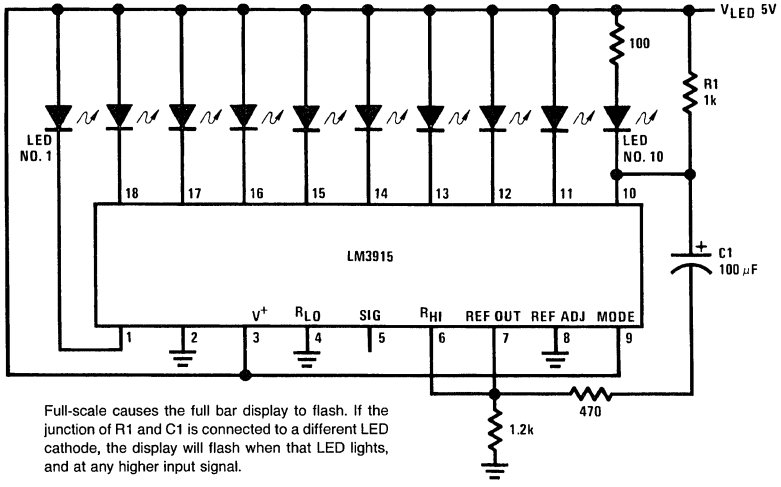
Typical Applications (Continued)

Driving Liquid Crystal Display



TL/H/5104–26

Bar Display with Alarm Flasher

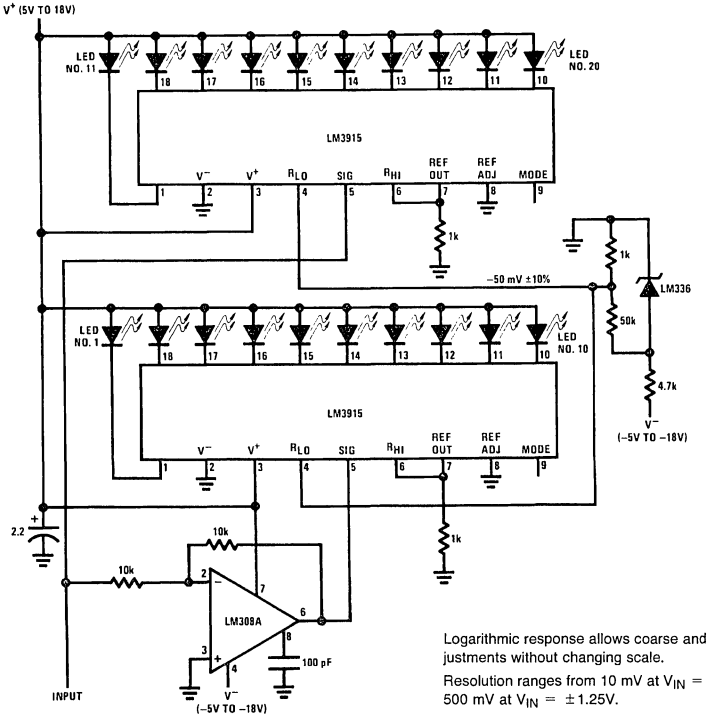


Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/5104–27

Typical Applications (Continued)

Precision Null Meter

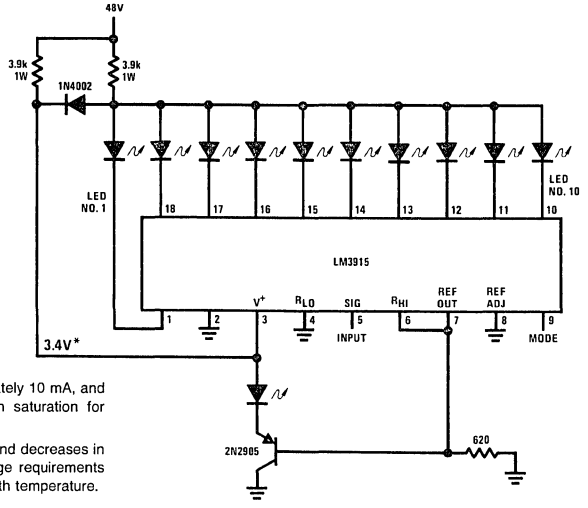


Logarithmic response allows coarse and fine adjustments without changing scale.

Resolution ranges from 10 mV at V_{IN} = 0 mV to 500 mV at V_{IN} = ±1.25V.

TL/H/5104–28

Operating with a High Voltage Supply (Dot Mode Only)



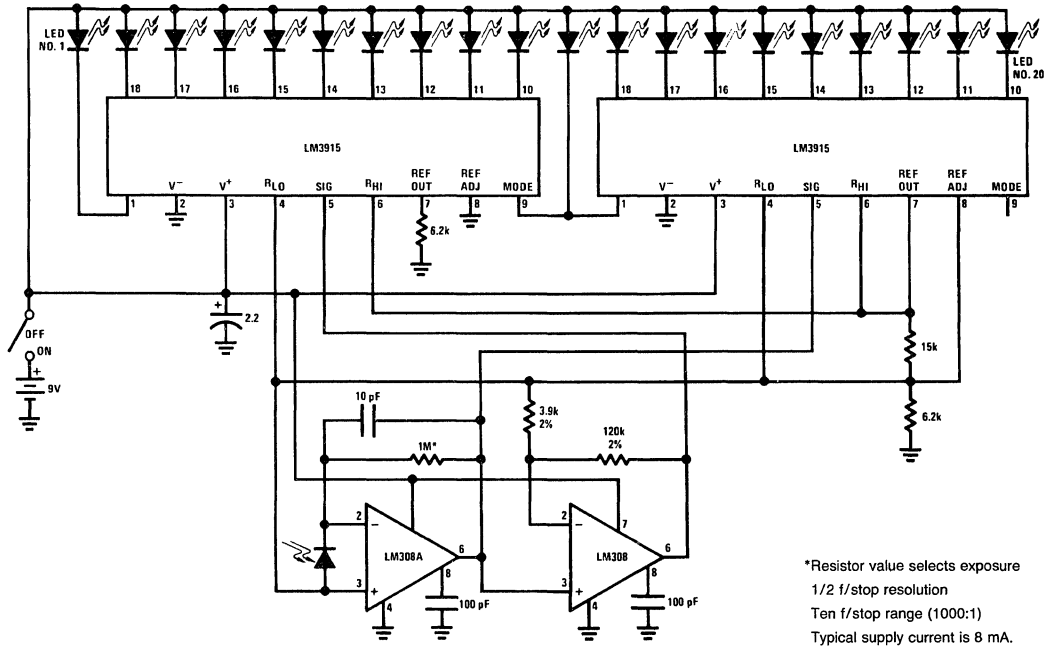
The LED currents are approximately 10 mA, and the LM3915 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3915 also decrease with temperature.

TL/H/5104–29

Typical Applications (Continued)

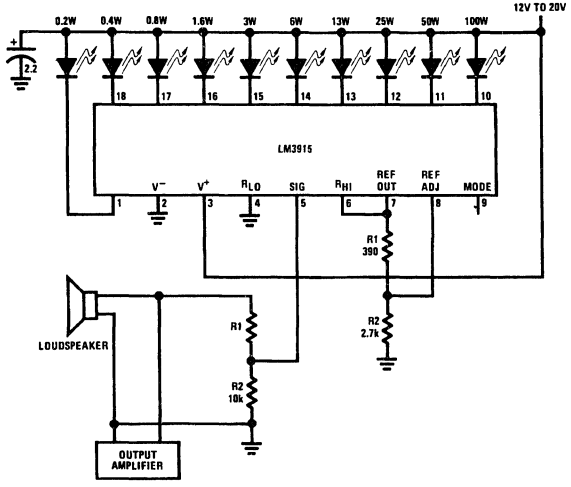
Light Meter



*Resistor value selects exposure
1/2 f/stop resolution
Ten f/stop range (1000:1)
Typical supply current is 8 mA.

TL/H/5104–30

Audio Power Meter



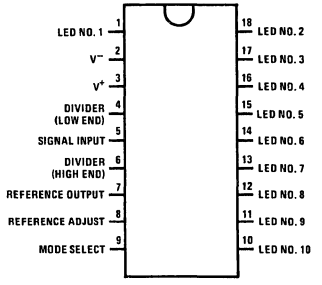
TL/H/5104–31

Load Impedance	R1
4Ω	10k
8Ω	18k
16Ω	30k

See Application Hints for optional Peak or Average Detector

Connection Diagram

Dual-In-Line Package



TL/H/5104–32

Top View

Order Number LM3915N
See NS Package Number N18A

Definition of Terms

Absolute Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference adjust pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

Line Regulation: The average change in reference output voltage (V_{REF}) over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Relative Accuracy: The difference between any two adjacent threshold points. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage

National Semiconductor Corporation

LM3916 Dot/Bar Display Driver

General Description

The LM3916 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing an electronic version of the popular VU meter. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 0.2 dB.

Audio applications include average or peak level indicators, and power meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3916 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3916 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display for increased range and/or resolution. Useful in other applications are the linear LM3914 and the logarithmic LM3915.

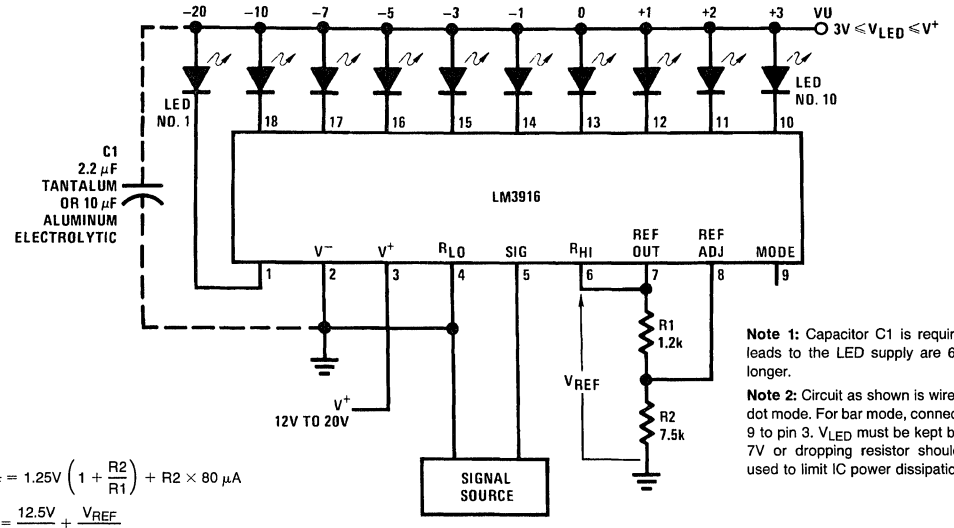
Features

- Fast responding electonic VU meter
- Drivers LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 70 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3916 is rated for operation from 0°C to +70°C. The LM3916N is available in an 18-lead molded DIP package.

Typical Applications

0V TO 10V VU Meter



$$V_{REF} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \times 80\,\mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\,k\Omega}$$

Note 1: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Note 2: Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

TL/H/7971–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation (Note 5)	
Molded DIP (N)	1365 mW
Supply Voltage	25V
Voltage on Output Drivers	25V
Input Signal Overvoltage (Note 3)	±35V
Divider Voltage	−100 mV to V^+
Reference Load Current	10 mA
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics (Note 1)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
COMPARATORS					
Offset Voltage, Buffer and First Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	10	mV
Offset Voltage, Buffer and Any Other Comparator	$0V \le V_{RLO} = V_{RHI} \le 12V$, $I_{LED} = 1$ mA		3	15	mV
Gain ($\Delta I_{LED}/\Delta V_{IN}$)	$I_{(REF)} = 2$ mA, $I_{LED} = 10$ mA	3	8		mA/mV
Input Bias Current (at Pin 5)	$0V \le V_{IN} \le (V^+ - 1.5V)$		25	100	nA
Input Signal Overvoltage	No Change in Display	−35		35	V
VOLTAGE DIVIDER					
Divider Resistance	Total, Pin 6 to 4	8	12	17	kΩ
Relative Accuracy (Input Change Between Any Two Threshold Points)	(Note 2) -1 dB $\le V_{IN} \le 3$ dB -7 dB $\le V_{IN} \le -1$ dB -10 dB $\le V_{IN} \le -7$ dB	 0.75 1.5 2.5	 1.0 2.0 3.0	 1.25 2.5 2.5	 dB dB dB
Absolute Accuracy	(Note 2) $V_{IN} = 2, 1, 0, -1$ dB $V_{IN} = -3, -5$ dB $V_{IN} = -7, -10, -20$ dB	 −0.25 −0.5 −1		 +0.25 +0.5 +1	 dB dB dB
VOLTAGE REFERENCE					
Output Voltage	$0.1\text{ mA} \le I_{L(REF)} \le 4$mA, $V^+ = V_{LED} = 5V$	1.2	1.28	1.34	V
Line Regulation	$3V \le V^+ \le 18V$		0.01	0.03	%/V
Load Regulation	$0.1\text{ mA} \le I_{L(REF)} \le 4$mA, $V^+ = V_{LED} = 5V$		0.4	2	%
Output Voltage Change with Temperature	$0°C \le T_A \le +70°C$, $I_{L(REF)} = 1$ mA, $V^+ = V_{LED} = 5V$		1		%
Adjust Pin Current			75	120	μA
OUTPUT DRIVERS					
LED Current	$V^+ = V_{LED} = 5V$, $I_{L(REF)} = 1$ mA	7	10	13	mA
LED Current Difference (Between Largest and Smallest LED Currents)	$V_{LED} = 5V$, $I_{LED} = 2$ mA $V_{LED} = 5V$, $I_{LED} = 20$ mA		0.12 1.2	0.4 3	mA mA
LED Current Regulation	$2V \le V_{LED} \le 17V$ $I_{LED} = 2$ mA $I_{LED} = 20$ mA		0.1 1	0.25 3	mA mA
Dropout Voltage	$I_{LED(ON)} = 20$ mA @ $V_{LED} = 5V$, $\Delta I_{LED} = 2$ mA			1.5	V
Saturation Voltage	$I_{LED} = 2.0$ mA, $I_{L(REF)} = 0.4$ mA		0.15	0.4	V
Output Leakage, Each Collector	Bar Mode (Note 4)		0.1	100	μA
Output Leakage	Dot Mode (Note 4)				
Pins 10–18			0.1	100	μA
Pin 1		60	150	450	μA

Electrical Characteristics (Note 1) (Continued)

Parameter	Conditions (Note 1)	Min	Typ	Max	Units
SUPPLY CURRENT					
Standby Supply Current	$V^+ = +5V$, $I_{L(REF)} = 0.2$ mA		2.4	4.2	mA
(All Outputs Off)	$V^+ = +20V$, $I_{L(REF)} = 1.0$ mA		6.1	9.2	mA

Note 1: Unless otherwise stated, all specifications apply with the following conditions:

$3\ V_{DC} \le V^+ \le 20\ V_{DC}$ $\quad -0.015V \le V_{RLO} \le 12\ V_{DC}$ $\quad T_A = 25°C$, $I_{L(REF)} = 0.2$ mA, pin 9 connected to pin 3 (bar mode).

$3\ V_{DC} \le V_{LED} \le V^+$ $\quad V_{REF}, V_{RHI}, V_{RLO} \le (V^+ - 1.5V)$ For higher power dissipations, pulse testing is used.

$-0.015V \le V_{RHI} \le 12\ V_{DC}$ $\quad 0V \le V_{IN} \le V^+ - 1.5V$

Note 2: Accuracy is measured referred to $+3$ dB $= +10.000\ V_{DC}$ at pin 5, with $+10.000\ V_{DC}$ at pin 6, and $0.000\ V_{DC}$ at pin 4. At lower full-scale voltages, buffer and comparator offset voltage may add significant error. See table for threshold voltages.

Note 3: Pin 5 input current must be limited to ± 3 mA. The addition of a 39k resistor in series with pin 5 allows ± 100V signals without damage.

Note 4: Bar mode results when pin 9 is within 20 mV of V^+. Dot mode results when pin 9 is pulled at least 200 mV below V^+. LED #10 (pin 10 output current) is disabled if pin 9 is pulled 0.9V or more below V_{LED}.

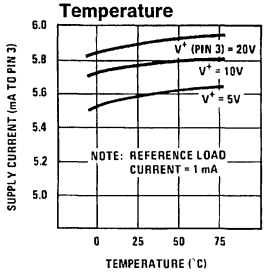
Note 5: The maximum junction temperature of the LM3916 is 100°C. Devices must be derated for operation at elevated temperatures. Junction to ambient thermal resistance is 55°C/W for the molded DIP (N package).

LM3916 Threshold Voltage (Note 2)

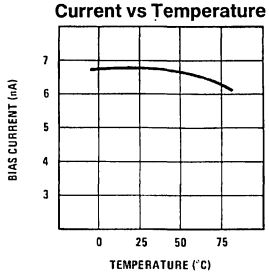
dB	Volts			dB	Volts		
	Min	Typ	Max		Min	Typ	Max
3	9.985	10.000	10.015	$-3 \pm \frac{1}{2}$	4.732	5.012	5.309
$2 \pm \frac{1}{4}$	8.660	8.913	9.173	$-5 \pm \frac{1}{2}$	3.548	3.981	4.467
$1 \pm \frac{1}{4}$	7.718	7.943	8.175	-7 ± 1	2.818	3.162	3.548
$0 \pm \frac{1}{4}$	6.879	7.079	7.286	-10 ± 1	1.995	2.239	2.512
$-1 \pm \frac{1}{2}$	5.957	6.310	6.683	-20 ± 1	0.631	0.708	0.794

Typical Performance Characteristics

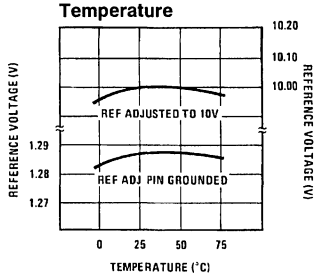
Supply Current vs Temperature



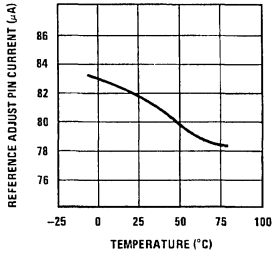
Operating Input Bias Current vs Temperature



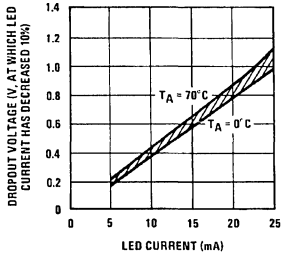
Reference Voltage vs Temperature



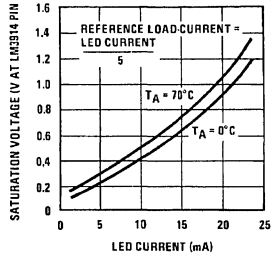
Reference Adjust Pin Current vs Temperature



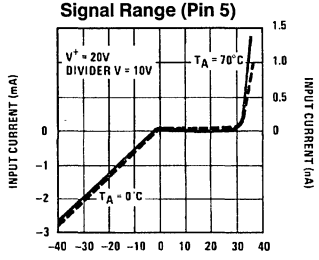
LED Current-Regulation Dropout



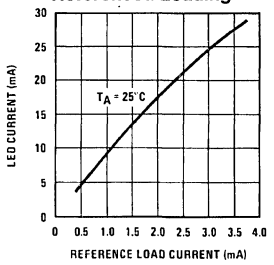
LED Driver Saturation Voltage



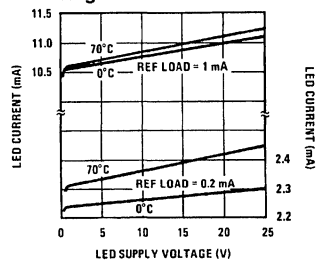
Input Current Beyond Signal Range (Pin 5)



LED Current vs Referenced Loading

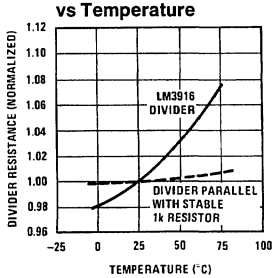


LED Driver Current Regulation

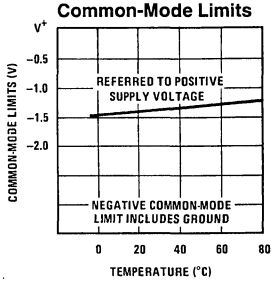


TL/H/7971–2

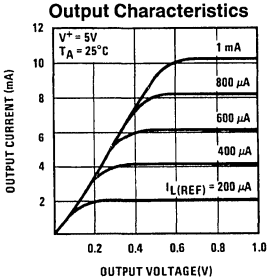
Total Divider Resistance vs Temperature



Common-Mode Limits

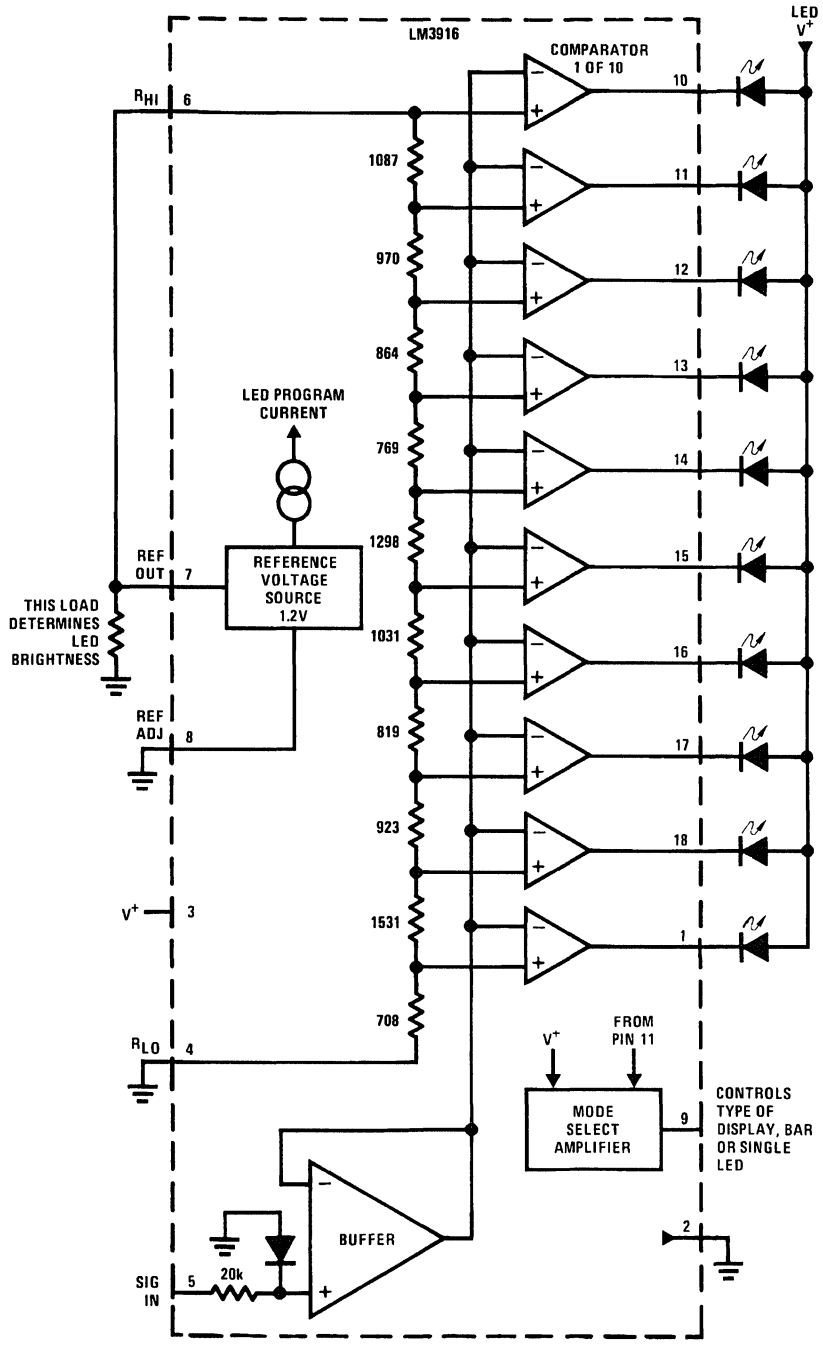


Output Characteristics



TL/H/7971–3

Block Diagram (Showing Simplest Application)



TL/H/7971–4

Functional Description

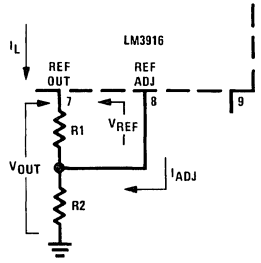
The simplified LM3916 block diagram is included to give the general idea of the circuit's operation. A high input impedance buffer operates with signals from ground to 12V, and is protected against reverse and overvoltage signals. The signal is then applied to a series of 10 comparators; each of which is biased to a different comparison level by the resistor string.

In the example illustrated, the resistor string is connected to the internal 1.25V reference voltage. As the input voltage varies from 0 to 1.25, the comparator outputs are driven low one by one, switching on the LED indicators. The resistor divider can be connected between any 2 voltages, providing that they are at least 1.5V below V^+ and no lower than V^-.

INTERNAL VOLTAGE REFERENCE

The reference is designed to be adjustable and develops a nominal 1.25V between the REF OUT (pin 7) and REF ADJ (pin 8) terminals. The reference voltage is impressed across program resistor R1 and, since the voltage is constant, a constant current I_1 then flows through the output set resistor R2 giving an output voltage of:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ}\,R2$$



TL/H/7971–5

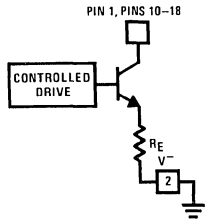
Since the 120 μA current (max) from the adjust terminal represents an error term, the reference was designed to minimize changes of this current with V^+ and load changes. For correct operation, reference load current should be between 80 μA and 5 mA. Load capacitance should be less than 0.05 μF.

CURRENT PROGRAMMING

A feature not completely illustrated by the block diagram is the LED brightness control. The current drawn out of the reference voltage pin (pin 7) determines LED current. Approximately 10 times this current will be drawn through each lighted LED, and this current will be relatively constant despite supply voltage and temperature changes. Current drawn by the internal 10-resistor divider, as well as by the external current and voltage-setting divider should be included in calculating LED drive current. The ability to modulate LED brightness with time, or in proportion to input voltage and other signals can lead to a number of novel displays or ways of indicating input overvoltages, alarms, etc.

The LM3916 outputs are current-limited NPN transistors as shown below. An internal feedback loop regulates the transistor drive. Output current is held at about 10 times the reference load current, independent of output voltage and processing variables, as long as the transistor is not saturated.

LM3916 Output Circuit



TL/H/7971–6

Outputs may be run in saturation with no adverse effects, making it possible to directly drive logic. The effective saturation resistance of the output transistors, equal to R_E plus the transistors' collector resistance, is about 50Ω. It's also possible to drive LEDs from rectified AC with no filtering. To avoid oscillations, the LED supply should be bypassed with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor.

MODE PIN USE

Pin 9, the Mode Select input, permits chaining of multiple devices, and controls bar or dot mode operation. The following tabulation shows the basic ways of using this input. Other more complex uses will be illustrated in the applications.

Bar Graph Display: Wire Mode Select (pin 9) *directly* to pin 3 (V^+ pin).

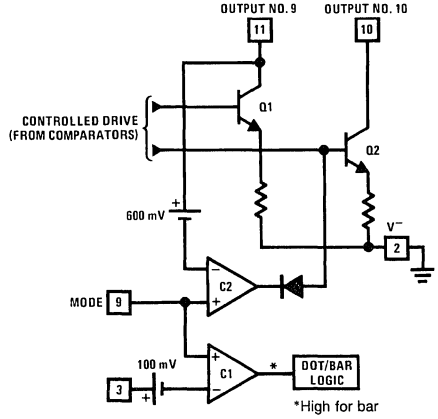
Dot Display, Single LM3916 Driver: Leave the Mode Select pin open circuit.

Dot Display, 20 or More LEDs: Connect pin 9 of the *first* drivers in the series (i.e., the one with the lowest input voltage comparison points) to pin 1 of the next higher LM3916 driver. Continue connecting pin 9 of lower input drivers to pin 1 of higher input drivers for 30 or more LED displays. The last LM3916 driver in the chain will have pin 9 left open. All previous drivers should have a 20k resistor in parallel with LED #9 (pin 11 to V_{LED}).

Mode Pin Functional Description

This pin actually performs two functions. Refer to the simplified block diagram below.

Block Diagram of Mode Pin Function



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Mode Pin Functional Description (Continued)

DOT OR BAR MODE SELECTION

The voltage at pin 9 is sensed by comparator C1, nominally referenced to ($V^+ - 100$ mV). The chip is in bar mode when pin 9 is above this level; otherwise it's in dot mode. The comparator is designed so that pin 9 can be left open circuit for dot mode.

Taking into account comparator gain and variation in the 100 mV reference level, pin 9 should be no more than 20 mV below V^+ for bar mode and more than 200 mV below V^+ (or open circuit) for dot mode. In most applications, pin 9 is either open (dot mode) or tied to V^+ (bar mode). In bar mode, pin 9 should be connected directly to pin 3. Large currents drawn from the power supply (LED current, for example) should not share this path so that large IR drops are avoided.

DOT MODE CARRY

In order for display to make sense when multiple drivers are cascaded in dot mode, special circuitry has been included to shut off LED #10 of the first device when LED #1 of the second device comes on. The connection for cascading in dot mode has already been described and is depicted in *Figure 1.*

As long as the input signal voltage is below the threshold of the second driver, LED #11 is off. Pin 9 of driver #1 thus sees effectively an open circuit so the chip is in dot mode. As soon as the input voltage reaches the threshold of LED #11, pin 9 of driver #1 is pulled an LED drop (1.5V or more) below V_{LED}. This condition is sensed by comparator C2, referenced 600 mV below V_{LED}. This forces the output of C2 low, which shuts off output transistor Q2, extinguishing LED #10.

V_{LED} is sensed via the 20k resistor connected to pin 11. The very small current (less than 100 μA) that is diverted from LED #9 does not noticeably affect its intensity.

An auxiliary current source at pin 1 keeps at least 100 μA flowing through LED #11 even if the input voltage rises high enough to extinguish the LED. This ensures that pin 9 of driver #1 is held low enough to force LED #10 off when *any* higher LED is illuminated. While 100 μA does not normally produce significant LED illumination, it may be noticeable when using high-efficiency LEDs in a dark environment. If this is bothersome, the simple cure is to shunt LED #11 (and LED #1) with a 10k resistor. The 1V 1R drop is more than the 900 mV worst case required to hold off LED #10 yet small enough that LED #11 does not conduct significantly.

In some circuits a number of outputs on the higher device are not used. Examples include the high resolution VU meter and the expanded range VU meter circuits (see Typical Applications). To provide the proper carry sense voltage in dot mode, the LEDs of the higher driver IC are tied to V_{LED} through two series-connected diodes as shown in *Figure 2.* Shunting the diodes with a 1k resistor provides a path for driver leakage current.

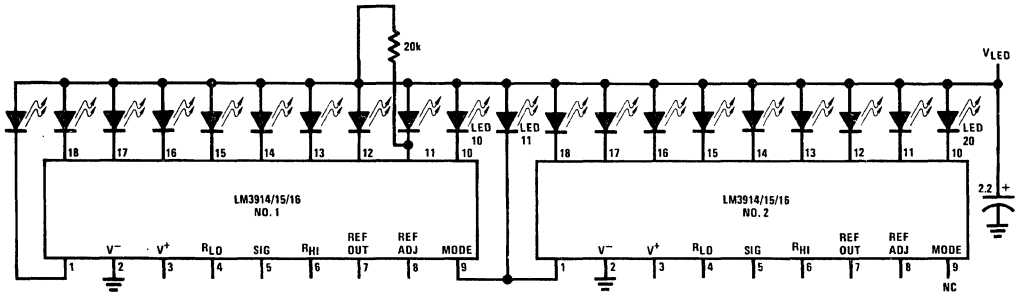

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FIGURE 1. Cascading LM3914/15/16 Series in Dot Mode

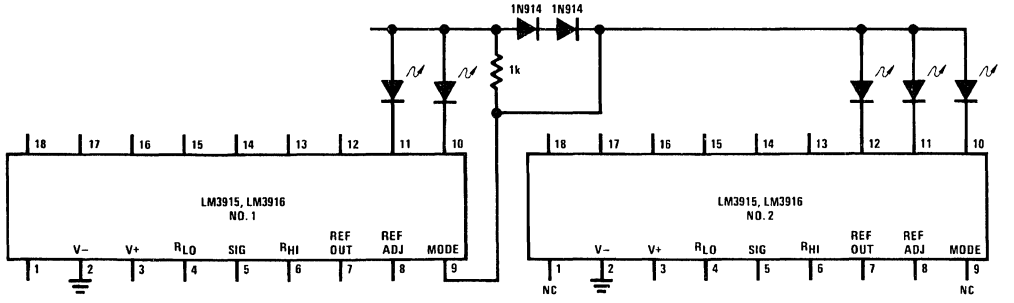

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FIGURE 2. Cascading Drivers in Dot Mode with Pin 1 of Driver #2 Unused

Mode Pin Functional Description (Continued)

OTHER DEVICE CHARACTERISTICS

The LM3915 is relatively low-powered itself, and since any number of LEDs can be powered from about 3V, it is a very efficient display driver. Typical standby supply current (all LEDs OFF) is 1.6 mA. However, any reference loading adds 4 times that current drain to the V^+ (pin 3) supply input. For example, an LM3915 with a 1 mA reference pin load (1.3k) would supply almost 10 mA to every LED while drawing only 10 mA from its V^+ pin supply. At full-scale, the IC is typically drawing less than 10% of the current supplied to the display.

The display driver does not have built-in hysteresis so that the display does not jump instantly from one LED to the next. Under rapidly changing signal conditions, this cuts down high frequency noise and often an annoying flicker. An "overlap" is built in so that at no time are all segments completely off the dot mode. Generally one LED fades in while the other fades out over a 1 mV range. The change may be much more rapid between LED #10 of one device and LED #1 of a *second* device cascaded.

Application Hints

The most difficult problem occurs when large LED currents are being drawn, especially in bar graph mode. These currents flowing out of the ground pin cause voltage drops in external wiring, and thus errors and oscillations. Bringing the return wires from signal sources, reference ground and bottom of the resistor string to a single point very near pin 2 is the best solution.

Long wires from V_{LED} to LED anode common can cause oscillations. The usual cure is bypassing the LED anodes with a 2.2 μF tantalum or 10 μF aluminum electrolytic capacitor. If the LEd anode line wiring is inaccessible, often a 0.1 μF capacitor from pin 1 to pin 2 will be sufficient.

If there is a large amount of LED overlap in the bar mode, oscillation or excessive noise is usually the problem. In cases where proper wiring and bypassing fail to stop oscillations, V^+ voltage at pin 3 is usually below suggested limits. When several LEDs are lit in dot mode, the problem is usually an AC component of the input signal which should be filtered out. Expanded scale meter applications may have one or both ends of the internal voltage divider terminated at relatively high value resistors. These high-impedance ends should be bypassed to pin 2 with 0.1 μF.

Power dissipation, especially in bar mode should be given consideration. For example, with a 5V supply and all LEDs programmed to 20 mA the driver will dissipate over 600 mW. In this case a 7.5Ω resistor in series with the LED supply will cut device heating in half. The negative end of the resistor should be bypassed with a 2.2 μF solid tantalum or 10 μF aluminum electrolytic capacitor to pin 2.

TIPS ON RECTIFIER CIRCUITS

The simplest way to display an AC signal using the LM3916 is to apply it right to pin 5 unrectified. Since the LED illuminated represents the instantaneous value of the AC waveform, one can readily discern both peak and average values of audio signals in this manner. The LM3916 will respond to positive half-cycles only but will not be damaged by signals up to ±35V (or up to ±100V if a 39k resistor is in series with the input). A smear or bar type display results even though the LM3916 is connected for dot mode. The LEDs should be run at 20 mA to 30 mA for high enough average intensity.

True average or peak detection requires rectification. If an LM3916 is set up with 10V full scale across its voltage divider, the turn-on point for the first LED is only 450 mV. A simple silicon diode rectifier won't work well at the low end due to the 600 mV diode threshold. The half-wave peak detector in *Figure 3* uses a PNP emitter-follower in front of the diode. Now, the transistor's base-emitter voltage cancels out the diode offset, within about 100 mV. This approach is usually satisfactory when a single LM3916 is used for a 23 dB display.

Display circuits such as the extended range VU meter using two or more drivers for a dynamic range of 40 dB or greater require more accurate detection. In the precision half-wave rectifier of *Figure 4* the effective diode offset is reduced by a factor equal to the open-loop gain of the op amp. Filter capacitor C2 charges through R3 and discharges through R2 and R3, so that appropriate selection of these values results in either a peak or an average detector. The circuit has a gain equal to R2/R1.

It's best to capacitively couple the input. Audio sources frequently have a small DC offset that can cause significant error at the low end of the log display. Op amps that slew quickly, such as the LF351, LF353 or LF356, are needed to faithfully respond to sudden transients. It may be necessary to trim out the op amp DC offset voltage to accurately cover a 60 dB range. Best results are obtained if the circuit is adjusted for the correct output when a low-level AC signal (10 to 20 mV) is applied, rather than adjusting for zero output with zero input.

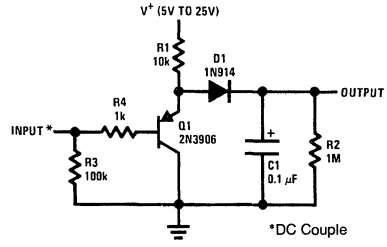

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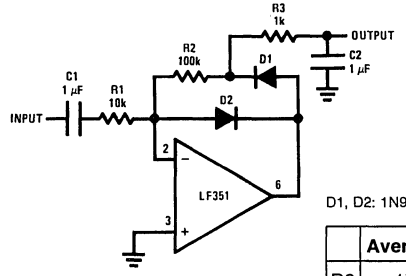
FIGURE 3. Half-Wave Peak Detector



D1, D2: 1N914 or 1N4148

	Average	Peak
R2	1k	100k
R3	100k	1k

R1 = R2 for A_V = 1
R1 = R2/10 for A_V = 10
C1 = 10/R1

TL/H/7971–11

FIGURE 4. Precision Half-Wave Rectifier

Application Hints (Continued)

For precision full-wave averaging use the circuit in *Figure 5.* Using 1% resistors for R1 through R4, gain for positive and negative signal differs by only 0.5 dB worst case. Substituting 5% resistors increases this to 2 dB worst case. (A 2 dB gain difference means that the display may have a ±1 dB error when the input is a nonsymmetrical transient). The averaging time constant is R5•C2. A simple modification results in the precision full-wave detector of *Figure 6.* Since the filter capacitor is not buffered, this circuit can drive only high impedance loads such as the input of an LM3916.

AUDIO METER STANDARDS

VU Meter

The audio level meter most frequently encountered is the VU meter. Its characteristics are defined as the ANSI specification C165. The LM3916's outputs correspond to the meter indications specified with the omission of the −2 VU indication. The VU scale divisions differ slightly from a linear scale in order to obtain whole numbers in dB.

Some of the most important specifications for an AC meter are its dynamic characteristics. These define how the meter responds to transients and how fast the reading decays. The VU meter is a relatively slow full-wave averaging type, specified to reach 99% deflection in 300 ms and overshoot by 1 to 1.5%. In engineering terms this means a slightly underdamped second order response with a resonant frequency of 2.1 Hz and a Q of 0.62. *Figure 7* depicts a simple rectifier/filter circuit that meets these criteria.

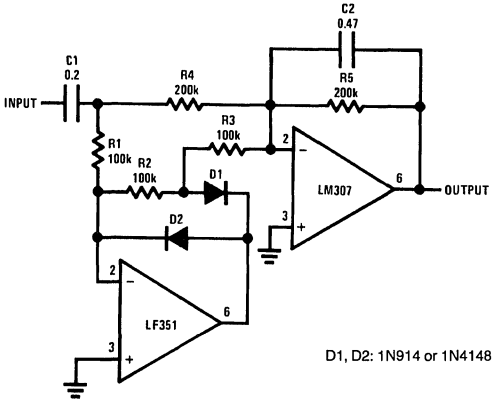


FIGURE 5. Precision Full-Wave Average Detector

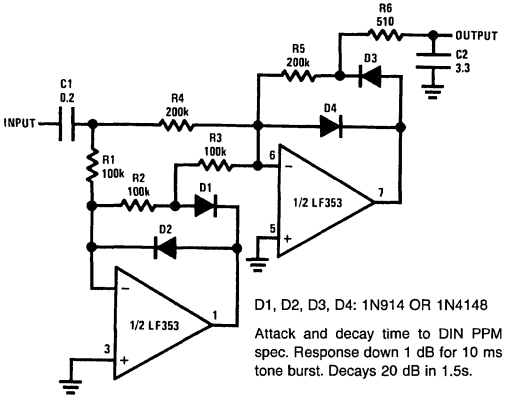
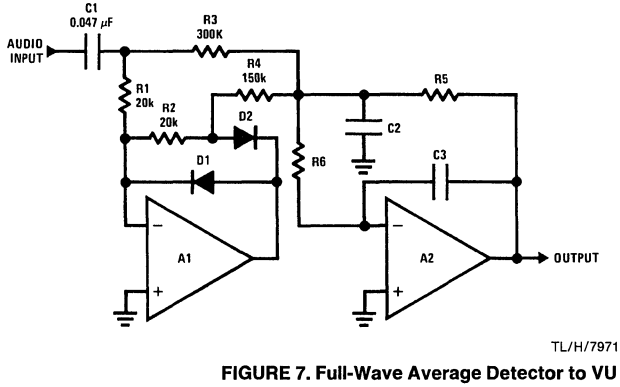


FIGURE 6. Precision Full-Wave Peak Detector



GAIN	R5	R6	C2	C3
1	100k	43k	2.0	0.56 μF
10	1M	100k	1.0	0.056 μF

Design Equations

$$\frac{1}{R5 \bullet R6 \bullet C2 \bullet C3} = \omega_0^2 = 177 \text{ sec} - 2$$

$$\frac{1}{C2}\left(\frac{1}{R3}+\frac{1}{R4}+\frac{1}{R5}+\frac{1}{R6}\right) = \frac{\omega_0}{Q} = 21.5 \text{ sec} - 1$$

$R3 = 2R4$

$R1 = R2 \ll R4$

A1, A2: ½ LF353

D1, D2: 1N914 OR 1N4148

*Reaches 99% level at 300 ms after applied tone burst and overshoots 1.2%.

FIGURE 7. Full-Wave Average Detector to VU Meter Specifications*

Application Hints (Continued)

Peak Program Meter

The VU meter, originally intended for signals sent via telephone lines, has shortcomings when used in high fidelity systems. Due to its slow response time, a VU meter will not accurately display transients that can saturate a magnetic tape or drive an amplifier into clipping. The fast-attack peak program meter (PPM) which does not have this problem is becoming increasingly popular.

While several European organizations have specifications for peak program meters, the German DIN specification 45406 is becoming a de facto standard. Rather than respond instantaneously to peak, however, PPM specifications require a finite "integration time" so that only peaks wide enough to be audible are displayed. DIN 45406 calls for a response of 1 dB down from steady-state for a 10 ms tone burst and 4 dB down for a 3 ms tone burst. These requirements are consistent with the other frequently encountered spec of 2 dB down for a 5 ms burst and are met by an attack time constant of 1.7 ms.

The specified return time of 1.5s to −20 dB requires a 650 ms decay time constant. The full-wave peak detector of *FIGURE 6* satisfies both the attack and decay time criteria.

Cascading The LM3916

The LM3916 by itself covers the 23 dB range of the conventional VU meter. To display signals of 40 dB or 70 dB dynamic range, the LM3916 may be cascaded with the 3 dB/step LM3915s. Alternatively, two LM3916s may be cascaded for increased resolution over a 28 dB range. Refer to the Extended Range VU Meter and High Resolution VU Meter in the Typical Applications section for the complete circuits for both dot and bar mode displays.

To obtain a display that makes sense when an LM3915 and an LM3916 are cascaded, the −20 dB output from the LM3916 is dropped. The full-scale display for the LM3915 is set at 3 dB below the LM3916's −10 dB output and the rest of the thresholds continue the 3 dB/step spacing. A simple, low cost approach is to set the reference voltage of the two chips 16 dB apart as in *Figure 5*. The LM3915, with pin 8 grounded, runs at 1.25V full-scale. R1 and R2 set the LM3916's reference 16 dB higher or 7.89V. Variation in the two on-chip references and resistor tolerance may cause a ± 1 dB error in the −10 dB to −13 dB transition. If this is objectionable, R2 can be trimmed.

The drawback of the aforementioned approach is that the threshold of LED #1 on the LM3915 is only 56 mV. Since comparator offset voltage may be as high as 10 mV, large errors can occur at the first few thresholds. A better approach, as shown in *Figure 9*, is to keep the reference the same for both drivers (10V in the example) and *amplify* the input signal by 16 dB ahead of the LM3915. Alternatively,

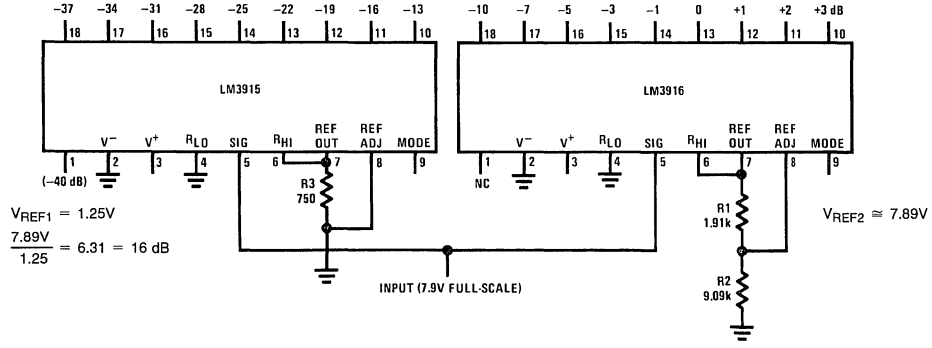


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FIGURE 8. Low Cost Circuit for 40 dB Display

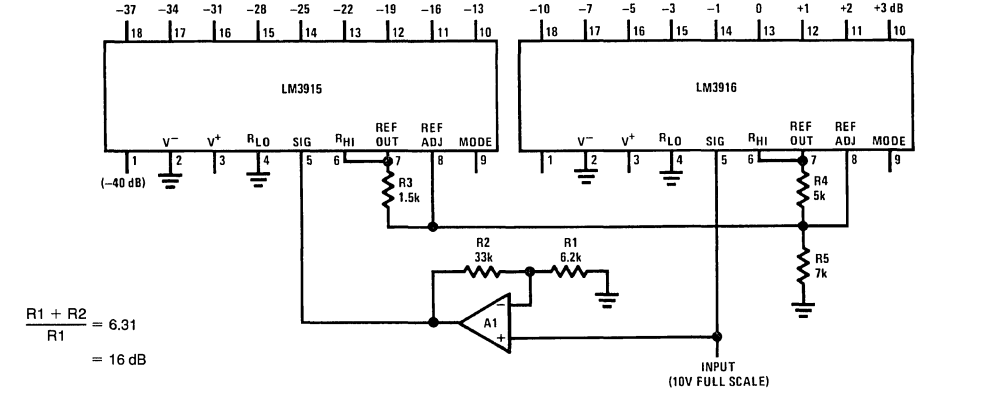

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FIGURE 9. Improved Circuit for 40 dB Display

Application Hints (Continued)

instead of amplifying, input signals of sufficient amplitude can be fed directly to the LM3916 and *attenuated* by 16 dB to drive the LM3915.

To extend this approach to get a 70 dB display, another 30 dB of amplification must be placed in the signal path ahead of the lowest LM3915. Extreme care is required as the lowest LM3915 displays input signals down to 2 mV! Several offset nulls may be required. High currents should not share the same path as the low level signal. Also power line wiring should be kept away from signal lines.

TIPS ON REFERENCE VOLTAGE AND LED CURRENT PROGRAMMING

Single Driver

The equations in *Figure 10* illustrate how to choose resistor values to set reference voltage for the simple case where no LED intensity adjustment is required. A LED current of 10 mA to 20 mA generally produces adequate illumination. Having 10V full-scale across the internal voltage divider gives best accuracy by keeping signal level high relative to the offset voltage of the internal comparators. However, this causes 1 mA to flow from pin 7 into the divider which means that the LED current will be at least 10 mA. R1 will typically be between 1 kΩ and 5 kΩ. To trim the reference voltage, vary R2.

The current in *Figure 11* shows how to add a LED intensity control which can vary LED current from 5 mA to 28 mA. Choosing V_{REF} = 5V lowers the current drawn by the ladder, increasing the intensity adjustment range. The reference adjustment has some effect on LED intensity but the reverse is not true.

Multiple Drivers

Figure 12 shows how to obtain a common reference trim and intensity control for two drivers. The two ICs may be connected in cascade or may be handling separate channels for stereo. This technique can be extended for larger numbers of drivers by varying the values of R1, R2 and R3. Because the LM3915 has a greater ladder resistance, R5 was picked less than R7 in such a way as to provide equal reference load currents. The ICs' internal references track within 100 mV so that worst case error from chip to chip is only 0.2 dB for V_{REF} = 5V.

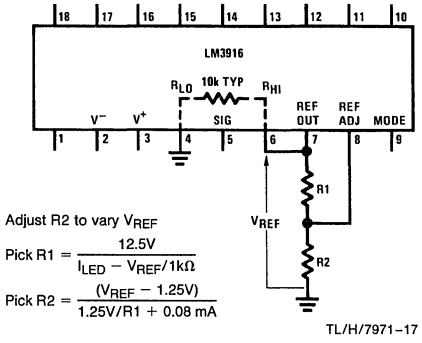


FIGURE 10. Design Equations for Fixed LED Intensity

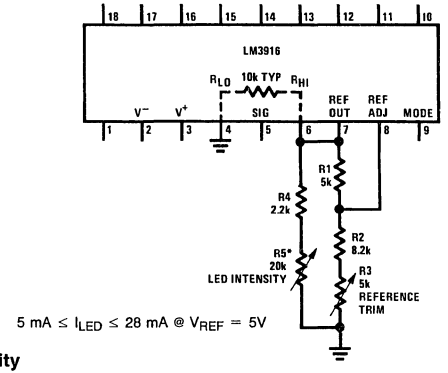


FIGURE 11. Varying LED Intensity

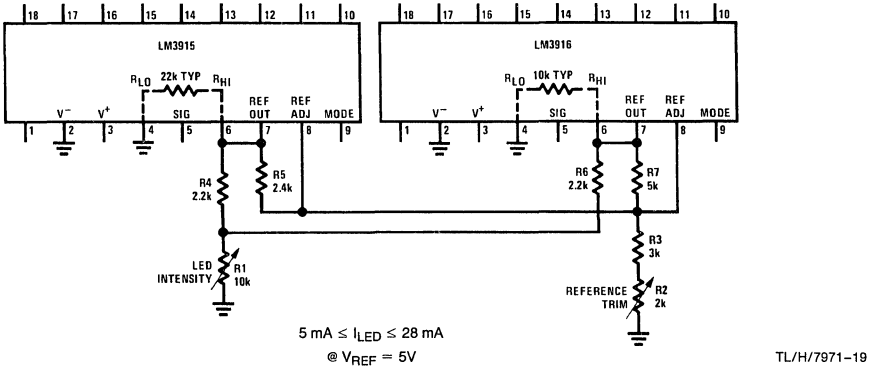


FIGURE 12. Independent Adjustment of Reference Voltage and LED Intensity for Multiple Drivers

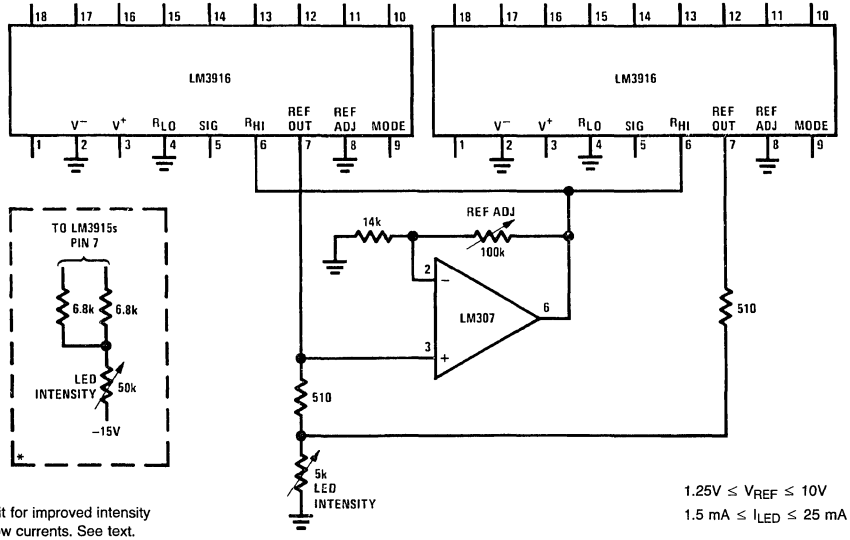
Application Hints (Continued)

The scheme in *Figure 13* is useful when the reference and LED intensity must be adjusted independently over a wide range. The R_{HI} voltage can be adjusted from 1.2V to 10V with no effect on LED current. Since the internal divider here does not load down the reference, minimum LED current is much lower. At the minimum recommended reference load of 80 μA, LED current is about 0.8 mA. The resistor values shown give a LED current range from 1.5 mA to 25 mA.

At the low end of the intensity adjustment, the voltage drop across the 510Ω current-sharing resistors is so small that chip to chip variation in reference voltage may yield a visible variation in LED intensity. The optional approach shown of connecting the bottom end of the intensity control pot to a negative supply overcomes this problem by allowing a larger voltage drop across the (larger) current-sharing resistors.

Other Applications

For increased resolution, it's possible to obtain a display with a smooth transition between LEDs. This is accomplished by superimposing an AC waveform on top of the input level as shown in *Figure 14*. The signal can be a triangle, sawtooth or sine wave from 60 Hz to 1 kHz. The display can be run in either dot or bar mode.



*Optional circuit for improved intensity matching at low currents. See text.

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FIGURE 13. Wide-Range Adjustment of Reference Voltage and LED Intensity for Multiple Drivers

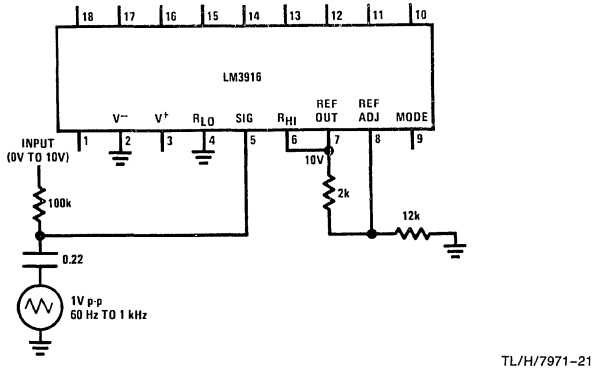

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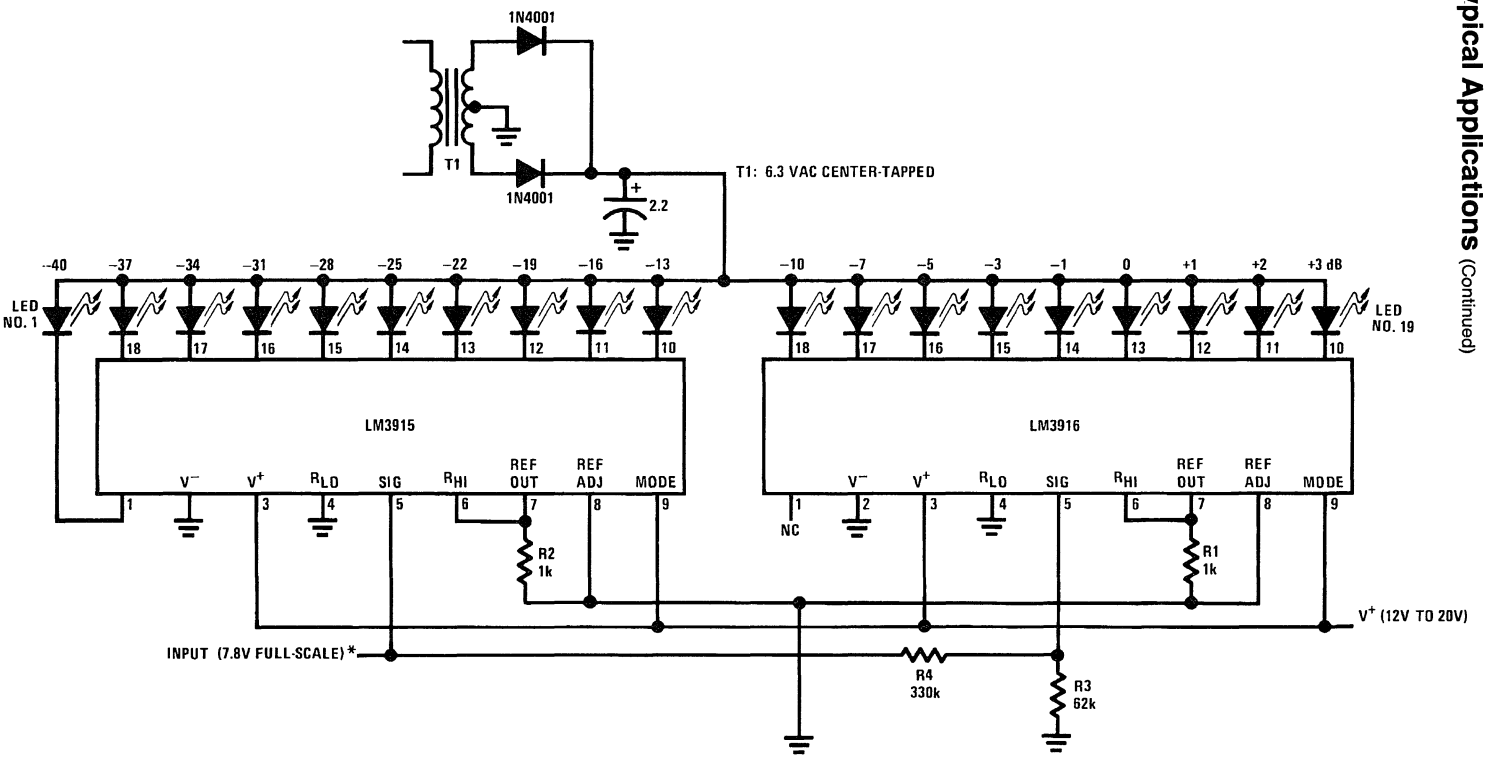
FIGURE 14. 0V to 10V VU Meter with Smooth Transitions

Extended Range VU Meter (Bar Mode)



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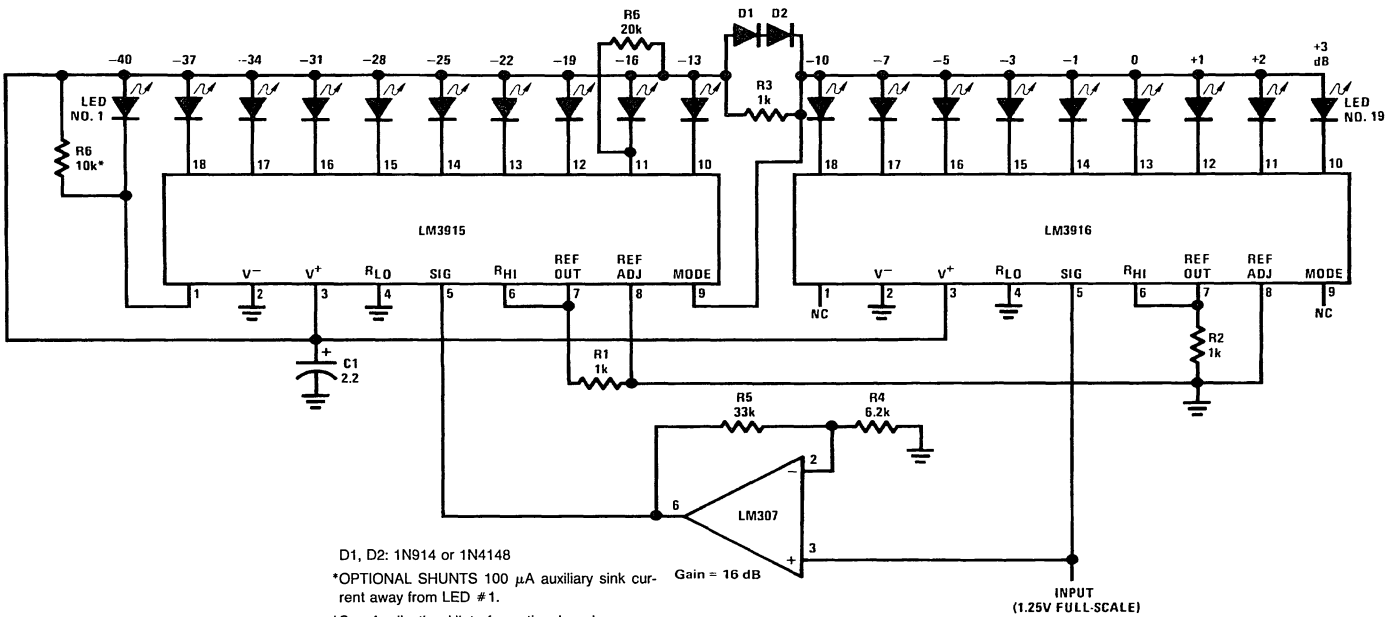
This application shows that the LED supply requires minimal filtering.

*See Application Hints for optional Peak or Average Detector.

†Adjust R3 for 3 dB difference between LED #11 and LED #12

$$\frac{R3}{R3 + R4} = 0.158 = -16\ dB$$

Extended Range VU Meter (Dot Mode)



D1, D2: 1N914 or 1N4148

*OPTIONAL SHUNTS 100 μA auxiliary sink current away from LED #1.

†See Application Hints for optional peak or average detector.

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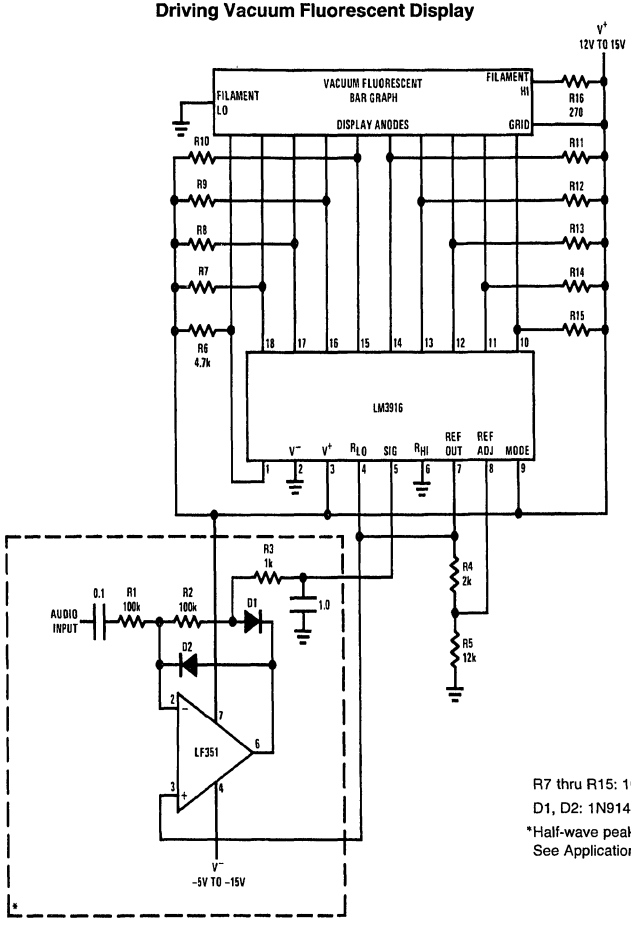
Typical Applications (Continued)

Driving Vacuum Fluorescent Display



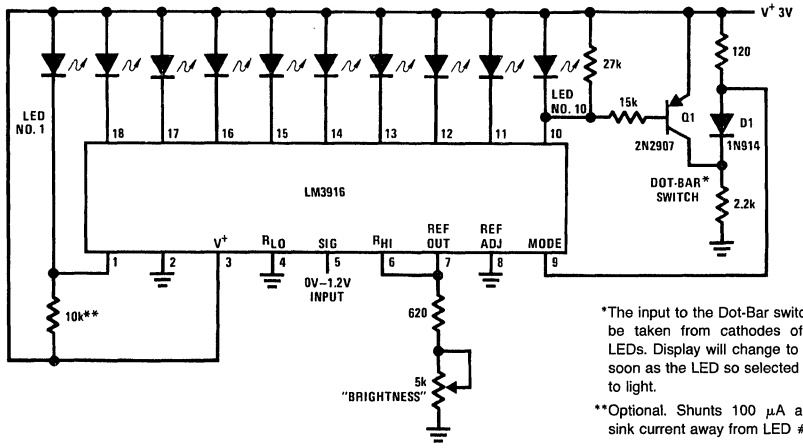
R7 thru R15: 10k ± 10%

D1, D2: 1N914 or 1N4148

*Half-wave peak detector. See Application Hints.

TL/H/7971–24

Indicator and Alarm, Full-Scale Changes Display From Dot to Bar



*The input to the Dot-Bar switch may be taken from cathodes of other LEDs. Display will change to bar as soon as the LED so selected begins to light.

**Optional. Shunts 100 μA auxiliary sink current away from LED #1.

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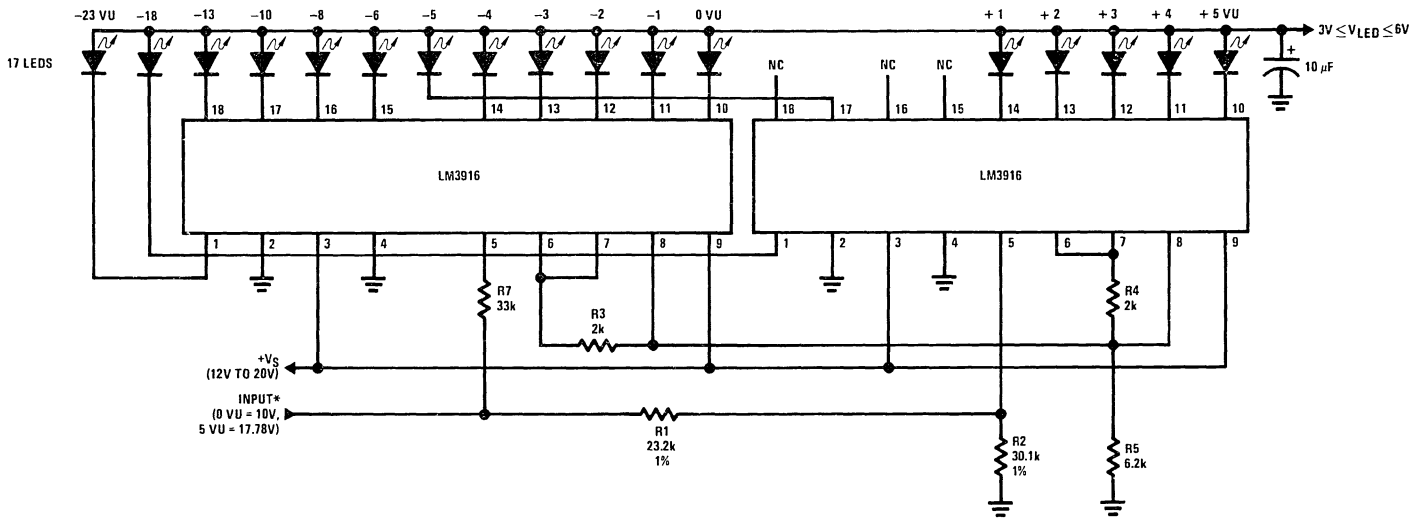
High Resolution VU Meter (Bar Mode)



TL/H/7971–26

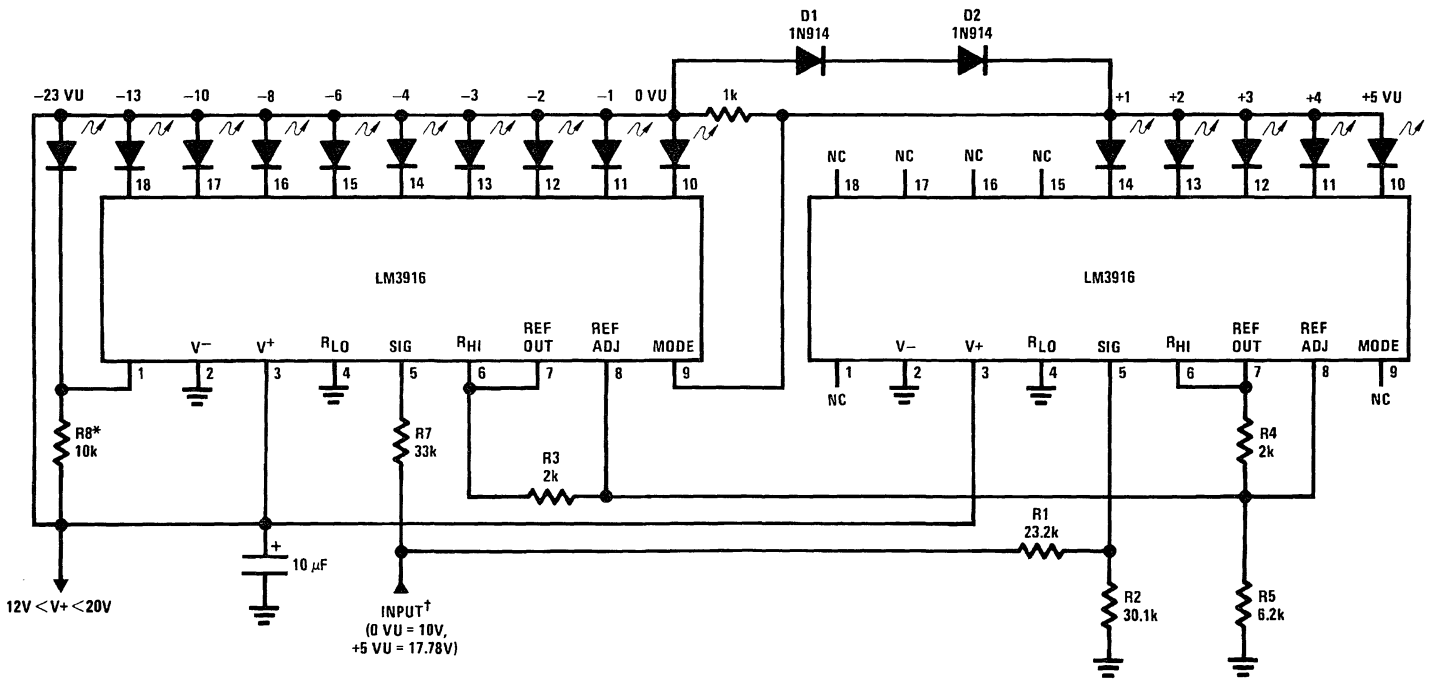
*See Application Hints for optional peak or average detector.

$$\frac{R2}{R1 + R2} \cong 0.562 = -5\ dB$$

or $R1 \cong 0.788 \bullet R2$

Typical Applications (Continued)

High Resolution VU Meter (Dot Mode)



TL/H/7971–27

*Optional shunts 100 µA auxiliary sink current away from LED #1.

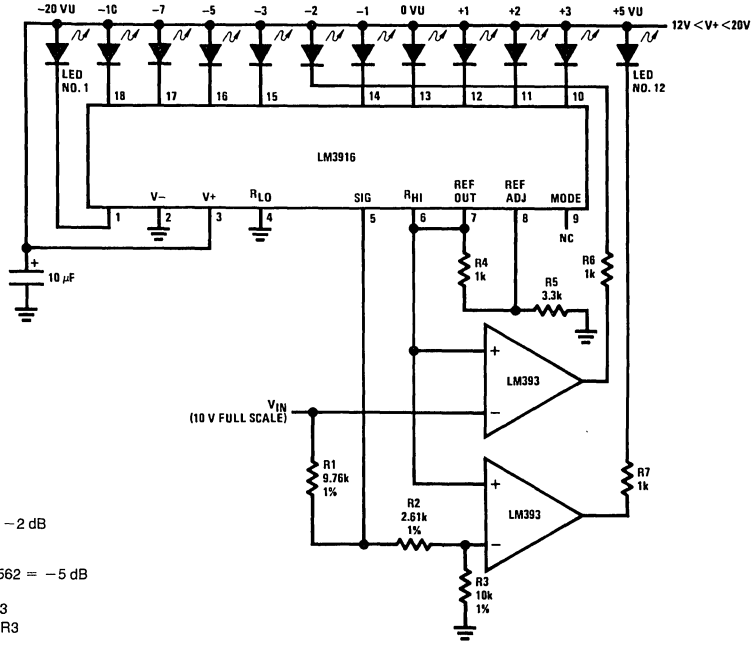
†See Application Hints for optional peak or average detector.

$$\frac{R2}{R1 + R2} \cong 0.562 = -5\ dB$$

or $R1 \cong 0.788 \bullet R2$

Typical Applications (Continued)

Displaying Additional Levels



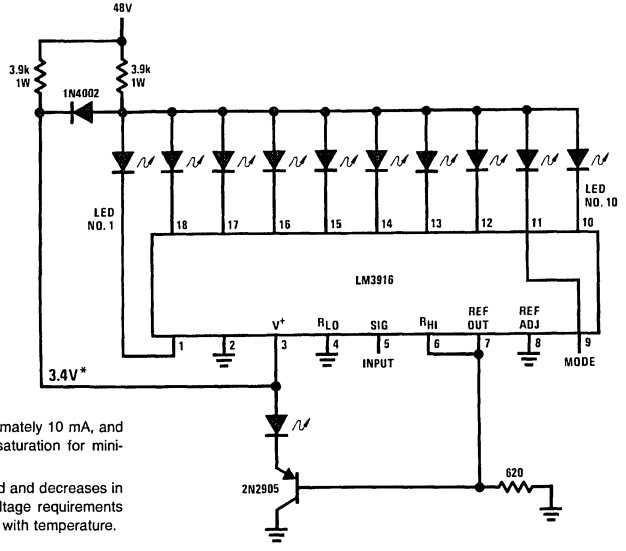
$$\frac{R3}{R2 + R3} \cong 0.794 = -2\ dB$$

$$\frac{R2 + R3}{R1 + R2 + R3} \cong 0.562 = -5\ dB$$

or R2 = 0.259 • R3
and R1 = 0.979 • R3

TL/H/7971–28

Operating with a High Voltage Supply (Dot Mode Only)



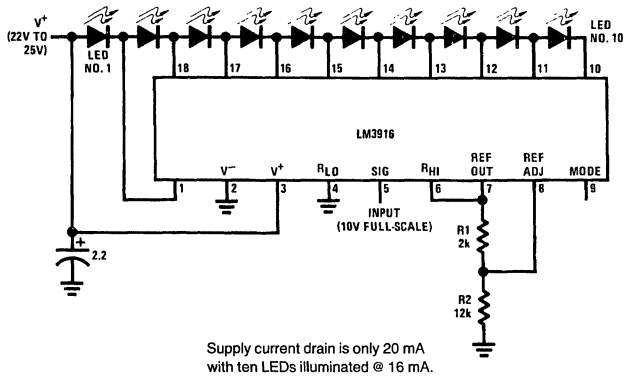
The LED currents are approximately 10 mA, and LM3916 outputs operate in saturation for minimum dissipation.

*This point is partially regulated and decreases in voltage with temperature. Voltage requirements of the LM3916 also decrease with temperature.

TL/H/7971–29

Typical Applications (Continued)

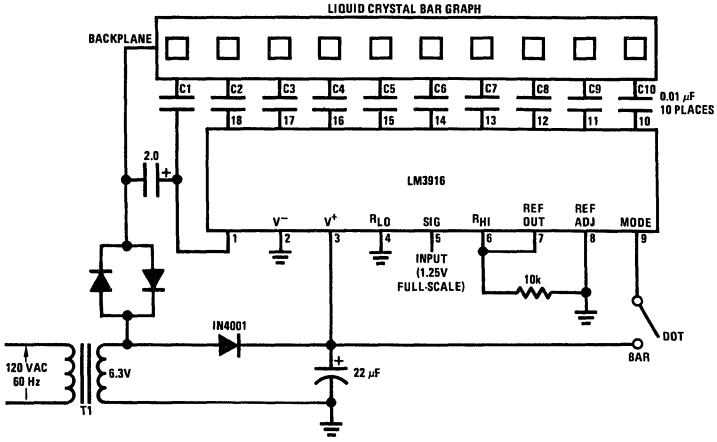
Low Current Bar Mode Display



Supply current drain is only 20 mA with ten LEDs illuminated @ 16 mA.

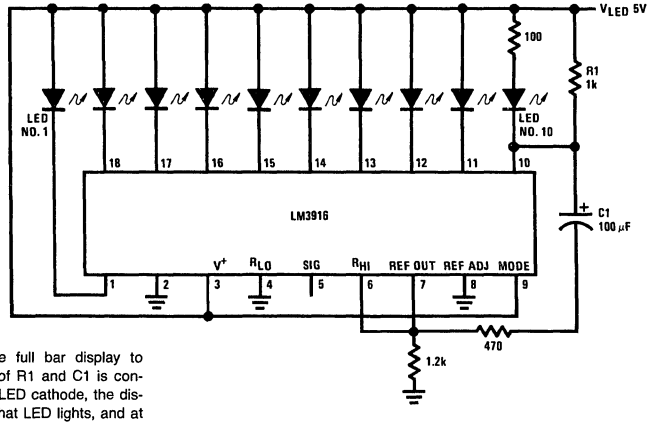
TL/H/7971–30

Driving Liquid Crystal Display



TL/H/7971–31

Bar Display with Alarm Flasher

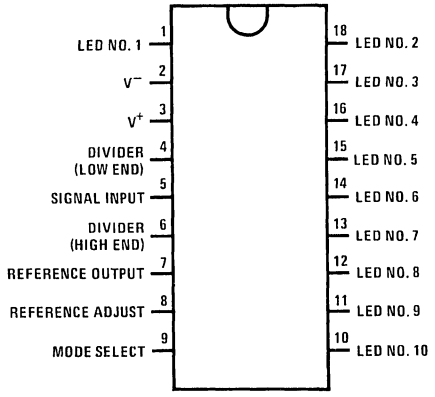


Full-scale causes the full bar display to flash. If the junction of R1 and C1 is connected to a different LED cathode, the display will flash when that LED lights, and at any higher input signal.

TL/H/7971–32

Connection Diagram

Dual-In-Line Package



TL/H/7971–33

Top View

Order Number LM3916N
See NS Package Number N18A

Definition of Terms

Absolute Accuracy: The difference between the observed threshold voltage and the ideal threshold voltage for each comparator. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

Adjust Pin Current: Current flowing out of the reference amplifier pin when the reference amplifier is in the linear region.

Comparator Gain: The ratio of the change in output current (I_{LED}) to the change in input voltage (V_{IN}) required to produce it for a comparator in the linear region.

Dropout Voltage: The voltage measured at the current source outputs required to make the output current fall by 10%.

Input Bias Current: Current flowing out of the signal input when the input buffer is in the linear region.

LED Current Regulation: The change in output current over the specified range of LED supply voltage (V_{LED}) as measured at the current source outputs. As the forward voltage of an LED does not change significantly with a small change in forward current, this is equivalent to changing the voltage at the LED anodes by the same amount.

Line Regulation: The average change in reference output voltage (V_{REF}) over the specified range of supply voltage (V^+).

Load Regulation: The change in reference output voltage over the specified range of load current ($I_{L(REF)}$).

Offset Voltage: The differential input voltage which must be applied to each comparator to bias the output in the linear region. Most significant error when the voltage across the internal voltage divider is small. Specified and tested with pin 6 voltage (V_{RHI}) equal to pin 4 voltage (V_{RLO}).

Relative Accuracy: The difference between any two adjacent threshold points. Specified and tested with 10V across the internal voltage divider so that resistor ratio matching error predominates over comparator offset voltage.

National Semiconductor Corporation

PRELIMINARY

LMC555 CMOS Timer

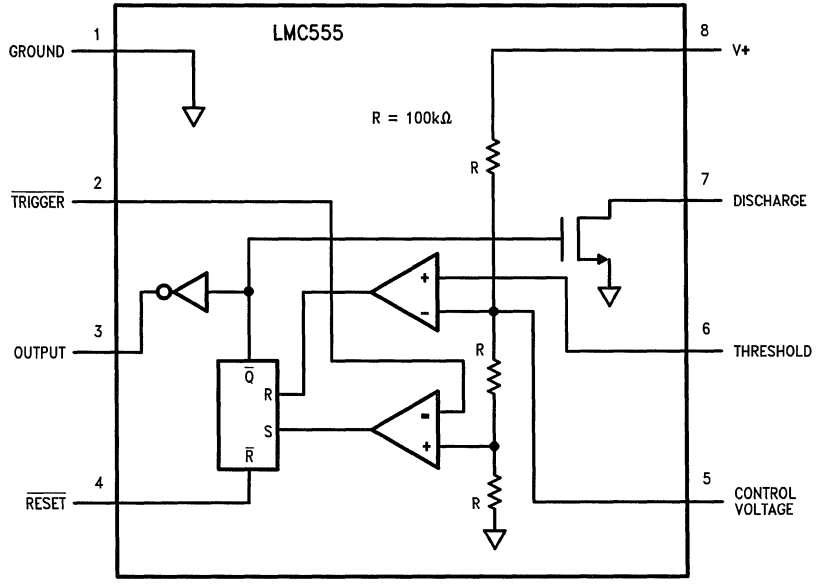
General Description

The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. It offers the same capability of generating accurate time delays and frequencies but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the astable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of National Semiconductor's LMCMOS™ process extends both the frequency range and low supply capability.

Features

- Less than 1 mW typical power dissipation at 5V supply
- 3 MHz astable frequency capability
- 1.5V supply operating voltage guaranteed
- Output fully compatible with TTL and CMOS logic at 5V supply
- Tested to −10 mA, +50 mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers

Block and Connection Diagrams



TL/H/8669–1

(Pinouts for Molded and Metal Can Packages are identical)

Order Number LMC555CH, LMC555CM or LMC555CN
See NS Package Number H08C, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V8	15V
Input Voltages, V2, V4, V5, V6	−0.3V to V_S + 0.3V
Output Voltages, V3, V7	15V
Output Current I3, I7	100 mA
Operating Temperature Range	−40°C to +85°C*
Storage Temperature Range	−65°C to +150°C

Soldering Information

Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

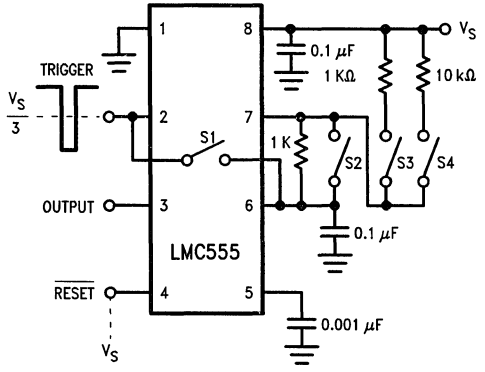
Electrical Characteristics

Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units (Limits)
I8	Supply Current	V_S = 1.5V V_S = 5V V_S = 12V		50 100 150	150 250 400	μA
V5	Control Voltage	V_S = 1.5V V_S = 5V V_S = 12V	0.8 2.9 7.4	1.0 3.3 8.0	1.2 3.8 8.6	V
V7	Discharge Saturation Voltage	V_S = 1.5V, I_7 = 1 mA V_S = 5V, I_7 = 10 mA		75 150	150 300	mV
$V3_L$	Output Voltage (Low)	V_S = 1.5V, I_3 = 1 mA V_S = 5V, I_3 = 8 mA V_S = 12V, I_3 = 50 mA		0.2 0.3 1.0	0.4 0.6 2.0	V
$V3_H$	Output Voltage (High)	V_S = 1.5V, I_3 = −0.25 mA V_S = 5V, I_3 = −2 mA V_S = 12V, I_3 = −10 mA	1.0 4.4 10.5	1.25 4.7 11.3		V
V2	Trigger Voltage	V_S = 1.5V V_S = 12V	0.4 3.7	0.5 4.0	0.6 4.3	V
I2	Trigger Current	V_S = 5V		10		pA
V4	Reset Voltage	V_S = 1.5V V_S = 12V	0.4 0.4	0.7 0.75	1.0 1.1	V
I4	Reset Current	V_S = 5V		10		pA
I6	Threshold Current	V_S = 5V		10		pA
I7	Discharge Leakage	V_S = 12V		1.0	100	nA
t	Timing Accuracy	SW 2, 4 Closed V_S = 1.5V V_S = 5V V_S = 12V	 0.9 1.0 1.0	 1.1 1.1 1.1	 1.25 1.20 1.25	ms
$\Delta t/\Delta Vs$	Timing Shift with Supply	V_S = 5V ±1V		0.3		%/V
$\Delta t/\Delta T$	Timing Shift with Temperature	V_S = 5V −40°C ≤ T ≤ +85°C		75		ppm/°C
f_A	Astable Frequency	SW 1, 3 Closed V_S = 12V	4.0	4.8	5.6	kHz
f_{MAX}	Maximum Frequency	Max. Freq. Test Circuit, V_S = 5V		3.0		MHz
t_R, t_F	Output Rise and Fall Times	Max. Freq. Test Circuit V_S = 5V, C_L = 10 pF		15		ns
t_{PD}	Trigger Propagation Delay	V_S = 5V, Measure Delay from Trigger to Output		100		ns

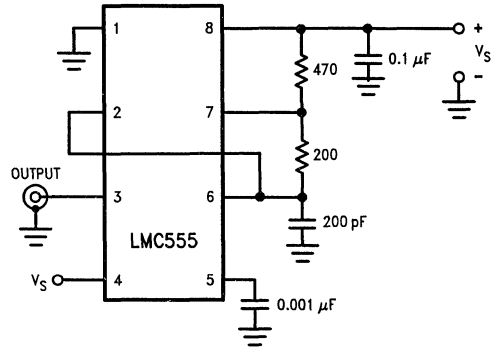
* Refer to RETSC555X drawing for specifications of military LMC555H version.

Test Circuit



TL/H/8669-2

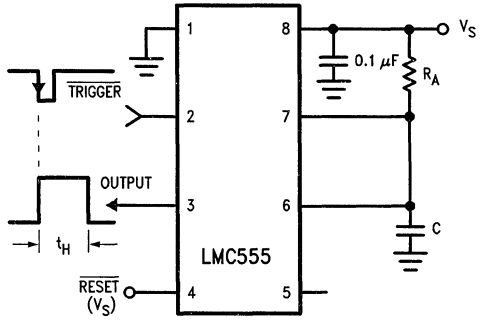
Maximum Frequency Test Circuit



TL/H/8669-3

Typical Applications

Monostable (One-Shot)



TL/H/8669-4

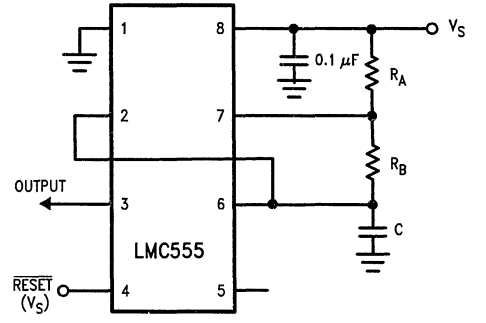
$t_H = 1.1\ R_AC$ (Gives time that output is high following trigger)

$\overline{\text{RESET}}$ overrides $\overline{\text{TRIGGER}}$, which can override THRESHOLD. Therefore, the trigger pulse must be shorter than the desired t_H.

The minimum trigger pulse width is 20 ns.

The minimum reset pulse width is 400 ns.

Variable Duty Cycle Oscillator

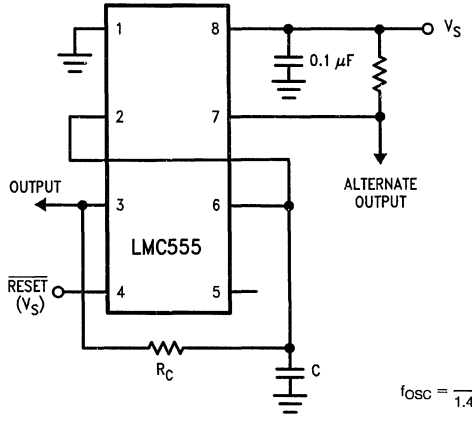


TL/H/8669-5

$$f_{OSC.} = \frac{1.44}{(R_A + 2R_B)C}$$

$$\text{Duty Cycle} = \frac{R_B}{R_A + 2R_B}$$ (Gives fraction of total period that output is low)

50% Duty Cycle Oscillator



$$f_{OSC} = \frac{1}{1.4R_CC}$$

TL/H/8669-6

National Semiconductor Corporation

PRELIMINARY

LMC567 Low Power Tone Decoder

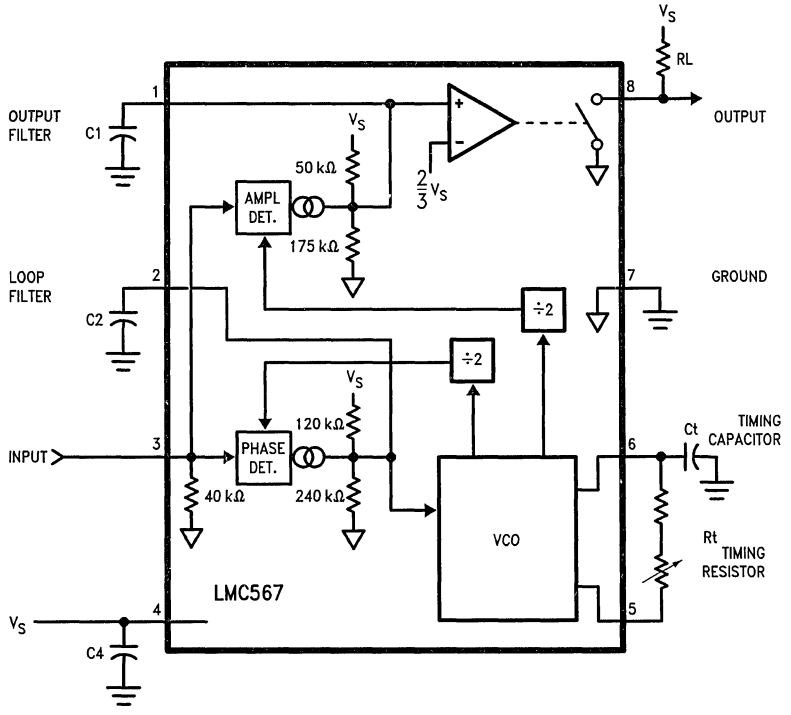
General Description

The LMC567 is a low power general purpose LMCMOS™ tone decoder which is functionally similar to the industry standard LM567. It consists of a twice frequency voltage-controlled oscillator (VCO) and quadrature dividers which establish the reference signals for phase and amplitude detectors. The phase detector and VCO form a phase-locked loop (PLL) which locks to an input signal frequency which is within the control range of the VCO. When the PLL is locked and the input signal amplitude exceeds an internally pre-set threshold, a switch to ground is activated on the output pin. External components set up the oscillator to run at twice the input frequency and determine the phase and amplitude filter time constants.

Features

- Functionally similar to LM567
- 2V to 9V supply voltage range
- Low supply current drain
- No increase in current with output activated
- Operates to 500 kHz input frequency
- High oscillator stability
- Ground-referenced input
- Hysteresis added to amplitude comparator
- Out-of-band signals and noise rejected
- 20 mA output current capability

Block Diagram (with External Components)



TL/H/8670–1

Order Number LMC567CM or LMC567CN
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage, Pin 3	2 V_{p-p}
Supply Voltage, Pin 4	10V
Output Voltage, Pin 8	13V
Voltage at All Other Pins	Vs to Gnd
Output Current, Pin 8	30 mA
Package Dissipation	500 mW
Operating Temperature Range (T_A)	−25°C to +125°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

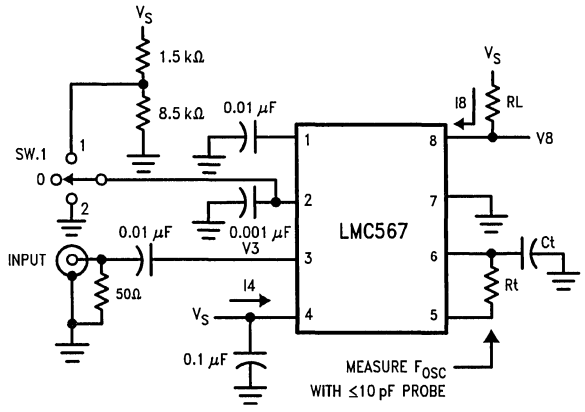
Electrical Characteristics

Test Circuit, T_A = 25°C, V_S = 5V, RtCt #2, Sw. 1 Pos. 0, and no input, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I4	Power Supply Current	RtCt #1, Quiescent or Activated	V_S = 2V		0.3		mAdc
			V_S = 5V		0.5	0.8	
			V_S = 9V		0.8	1.3	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency, $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	V_S = 2V		98		kHz
			V_S = 5V	92	103	113	
			V_S = 9V		105		
Δf_0	Center Frequency Shift with Supply	$\frac{f_0\|_{9V} - f_0\|_{2V}}{7\, f_0\|_{5V}} \times 100$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level Until Pin 8 Goes Low.	V_S = 2V	11	20	27	mVrms
			V_S = 5V	17	30	45	
			V_S = 9V		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level Until Pin 8 goes High.			1.5		mVrms
V8	Output 'Sat' Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; L.D.B.W = $\frac{F_{osc}\|_{P2} - F_{osc}\|_{P1}}{F_{osc}\|_{P0}} \times 100$	V_S = 2V	7	11	15	%
			V_S = 5V	11	14	17	
			V_S = 9V		15		
ΔBW	Bandwidth Skew	Skew = $\left(\frac{F_{osc}\|_{P2} + F_{osc}\|_{P1}}{2\, F_{osc}\|_{P0}} - 1\right) \times 100$			0	±1.0	%
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2			700		kHz
V_{in}	Input Threshold at f_{max}	Set Input Frequency Equal to f_{max} measured Above, Increase Input Level Until Pin 8 goes Low.			35		mVrms

Test Circuit

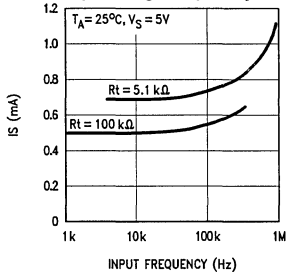
RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF



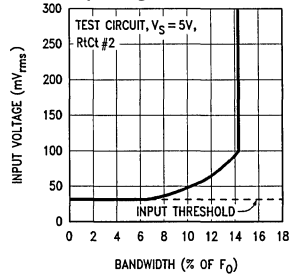
TL/H/8670–2

Typical Performance Characteristics

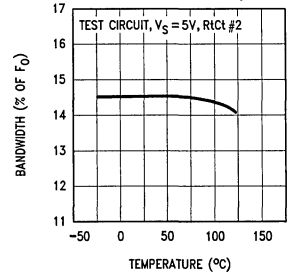
Supply Current vs. Operating Frequency



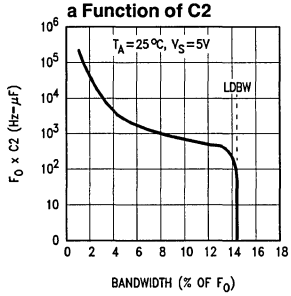
Bandwidth vs. Input Signal Level



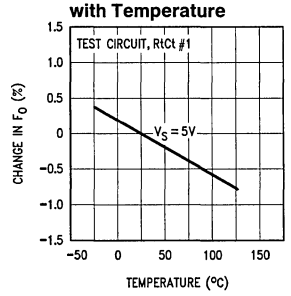
Largest Detection Bandwidth vs. Temp.



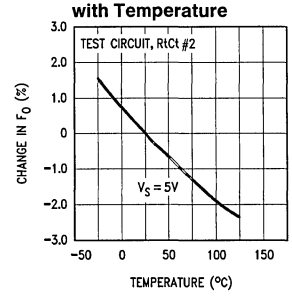
Bandwidth as a Function of C2



Frequency Drift with Temperature



Frequency Drift with Temperature



TL/H/8670–3

Applications Information (refer to Block Diagram)

GENERAL

The LMC567 low power tone decoder can be operated at supply voltages of 2V to 9V and at input frequencies ranging from 1 Hz up to 500 kHz.

The LMC567 can be directly substituted in most LM567 applications with the following provisions:

1. Oscillator timing capacitor Ct must be halved to double the oscillator frequency relative to the input frequency (See OSCILLATOR TIMING COMPONENTS).
2. Filter capacitors C1 and C2 must be reduced by a factor of 8 to maintain the same filter time constants.
3. The output current demanded of pin 8 must be limited to the specified capability of the LMC567.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC567 must be set up to run at twice the frequency of the input signal tone to be decoded. The center frequency of the VCO is set by timing resistor Rt and timing capacitor Ct connected to pins 5 and 6 of the IC. The center frequency as a function of Rt and Ct is given by:

$$F_{osc} \cong \frac{1}{1.4\ Rt\ Ct}\ Hz$$

Since this will cause an input tone of half F_{osc} to be decoded,

$$F_{input} \cong \frac{1}{2.8\ Rt\ Ct}\ Hz$$

This equation is accurate at low frequencies; however, above 50 kHz (F_{osc} = 100 kHz), internal delays cause the actual frequency to be lower than predicted.

The choice of Rt and Ct will be a tradeoff between supply current and practical capacitor values. An additional supply current component is introduced due to Rt being switched to V_S every half cycle to charge Ct:

$$I_S \text{ due to } Rt = V_S/(4Rt)$$

Thus the supply current can be minimized by keeping Rt as large as possible (see supply current vs. operating frequency curves). However, the desired frequency will dictate an RtCt product such that increasing Rt will require a smaller Ct. Below Ct = 100 pF, circuit board stray capacitances begin to play a role in determining the oscillation frequency which ultimately limits the minimum Ct.

To allow for I.C. and component value tolerances, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC567 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close as possible to pin 4.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals which are already centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via a coupling capacitor. Inputs of multiple LMC567 devices can be paralleled without individual d.c. isolation.

LOOP FILTER

Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). Capacitor C2 in conjunction with the nominal 80 kΩ pin 2 internal resistance forms the loop filter.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will begin to become narrower than the LDBW (see Bandwidth as a Function of C2 curve). However, the maximum hold-in range will always equal the LDBW.

OUTPUT FILTER

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_S. When the PLL is locked to the input, an increase in signal level causes the detector output to move negative. When pin 1 reaches 2/3 V_S the output is activated (see OUTPUT PIN).

Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Low values of C1 produce the least delay between the input and output for tone burst applications, while larger values of C1 improve noise immunity.

Pin 1 also provides a means for shifting the input threshold higher or lower by connecting an external resistor to supply or ground. However, reducing the threshold using this technique increases sensitivity to pin 1 carrier ripple and also results in more part to part threshold variation.

OUTPUT PIN

The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input tone is of sufficient amplitude to cause pin 1 to fall below 2/3 V_S. Apart from the obvious current component due to the external pin 8 load resistor, no additional supply current is required to activate the switch. The on resistance of the switch is inversely proportional to supply; thus the 'sat' voltage for a given output current will increase at lower supplies.

National Semiconductor Corporation

ADVANCED INFORMATION

LMC568 Low Power Phase-Locked Loop

General Description

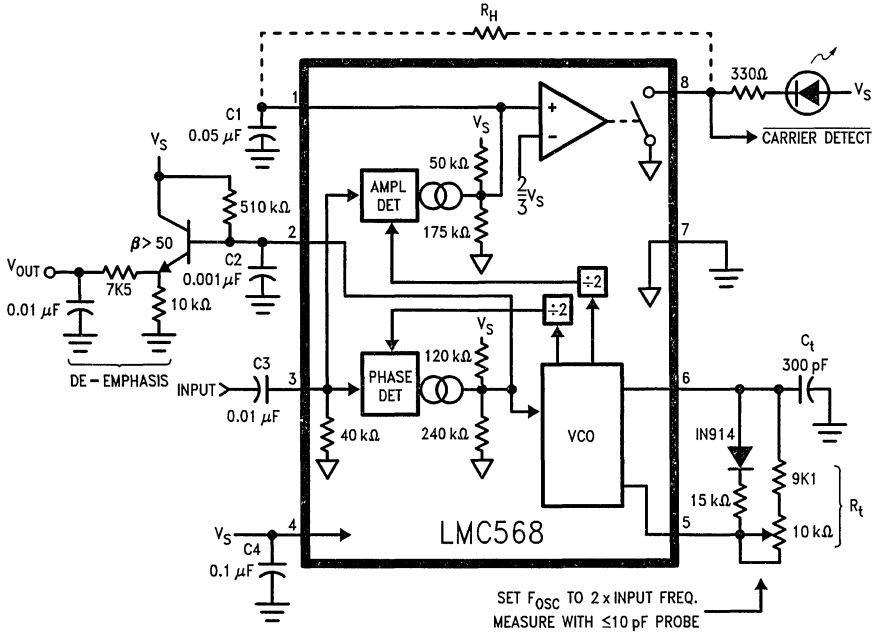
The LMC568 is an amplitude-linear phase-locked loop consisting of a linear VCO, fully balanced phase detectors, and a carrier detect output. LMCMOS™ technology is employed for high performance with low power consumption.

The VCO has a linearized control range of ±30% to allow demodulation of FM and FSK signals. Carrier detect is indicated when the PLL is locked to an input signal greater than 26 mVrms. LMC568 applications include FM SCA and TV second audio program decoders, FSK data demodulators, and voice pagers.

Features

- Demodulates ±15% deviation FM/FSK signals
- Carrier Detect Output with hysteresis
- Operation to 500 kHz input frequency
- Low THD—0.5% typ. for ±10% deviation
- 2V to 9V supply voltage range
- Low supply current drain

Typical Application (100 kHz input frequency, refer to notes pg. 3)



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Order Number LMC568CM or LMC568CN
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage, Pin 3	2 V_{p-p}
Supply Voltage, Pin 4	10V
Output Voltage, Pin 8	13V
Voltage at All Other Pins	V_S to Gnd
Output Current, Pin 8	30 mA
Package Dissipation	500 mW
Operating Temperature Range (T_A)	−25°C to +125°C
Storage Temperature Range	−55°C to +150°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

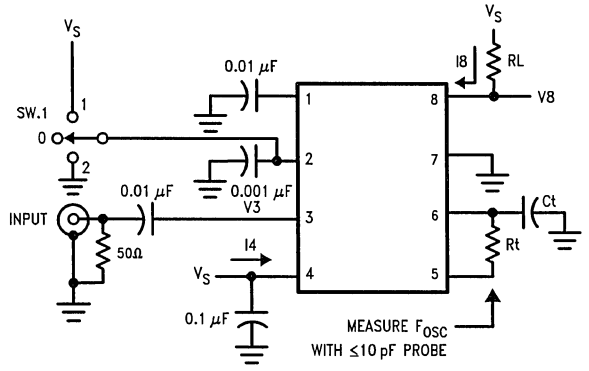
See AN-450 "Surface Mounting Methods and their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

Test Circuit, T_A = 25°C, V_S = 5V, RtCt #2, Sw. 1 Pos. 0; and no input unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I4	Power Supply Current	RtCt #1, Quiescent or Activated	V_S = 2V		0.35		mAdc
			V_S = 5V		0.75	1.5	
			V_S = 9V		1.2	2.4	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	V_S = 2V		98		kHz
			V_S = 5V	90	103	115	
			V_S = 9V		105		
Δf_0	Center Frequency Shift with Supply	$\frac{f_0\|_{9V} - f_0\|_{2V}}{7\, f_0\|_{5V}} \times 100$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level until Pin 8 Goes Low.	V_S = 2V	10	16	25	mVrms
			V_S = 5V	16	26	42	
			V_S = 9V		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level until Pin 8 Goes High.			1.5		mVrms
V8	Output 'Sat' Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; L.D.B.W. $= \frac{F_{osc}\|_{P2} - F_{osc}\|_{P1}}{F_{osc}\|_{P0}} \times 100$	V_S = 2V		30		%
			V_S = 5V	40	55		
			V_S = 9V		60		
ΔBW	Bandwidth Skew	Skew $= \left(\frac{F_{osc}\|_{P2} + F_{osc}\|_{P1}}{2\, F_{osc}\|_{P0}} - 1\right) \times 100$			1	±5	%
V_{out}	Recovered Audio	Typical Application Circuit Input = 100 mVrms, F = 100 kHz F_{mod} = 400 Hz, ±10 kHz Dev.	V_S = 2V		170		mVrms
			V_S = 5V		270		
			V_S = 9V		400		
THD	Total Harmonic Distortion	Typical Application Circuit as Above, Measure V_{out} Distortion.			0.5		%
$\frac{S+N}{N}$	Signal to Noise Ratio	Typical Application Circuit Remove Modulation, Measure V_n $(S + N)/N = 20 \log (V_{out}/V_n)$.			65		dB
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2			700		kHz

Test Circuit



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RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

Notes to Typical Application

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close to possible to pin 4. Also, due to pin voltages tracking supply, a large C4 is necessary for low frequency PSRR.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC568 must be set up to run at twice the frequency of the input signal. The components shown in the typical application are for F_{osc} = 200 kHz (100 kHz input frequency). For operation at lower frequencies, increase the capacitor value; for higher frequencies proportionally reduce the resistor values.

If low distortion is not a requirement, the series diode/resistor between pins 6 and 5 may be omitted. This will reduce VCO supply dependence and increase V_{out} by approximately 2 dB with THD = 2% typical. The center frequency as a function of Rt and Ct is given by:

$$F_{osc} \cong \frac{1}{1.4\ Rt\ Ct}\ Hz$$

To allow for I.C. and component value tolerences, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC568 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals that are centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via C3.

OUTPUT TAKEOFF

The output signal is taken off the loop filter at pin 2. Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). The nominal pin 2 source resistance is 80 kΩ, requiring the use of an external buffer transistor to drive nominal loads.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built-in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will become narrower than the LDBW. However, the maximum hold-in range will always equal the LDBW. The 2 kHz de-emphasis pole shown may be modified or omitted as required by the application.

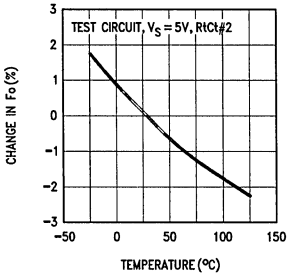
CARRIER DETECT

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_S. The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input is of sufficient amplitude to cause pin 1 to fall below 2/3 V_S. The carrier detect threshold is internally set to 26 mVrms typical on a 5V supply.

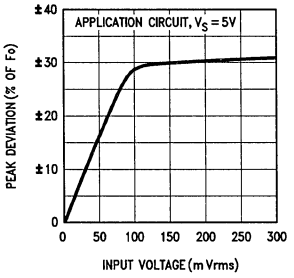
Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Optional resistor R_H increases the hysteresis in the pin 8 output for applications such as audio mute control. The minimum allowable value for R_H is 330 kΩ.

LMC568 Typical Performance Characteristics

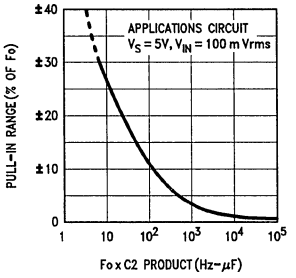
Frequency Drift with Temperature



Peak Deviation vs Input Signal Level



Pull-In Range as a Function of C2



TL/H/9135–2

Section 6

Surface Mount

Section 6 Contents

National Semiconductor Corporation

Surface Mount

Cost pressures today are forcing many electronics manufacturers to automate their production lines. Surface mount technology plays a key role in this cost-savings trend because:

1. The mounting of devices on the PC board surface eliminates the expense of drilling holes;
2. The use of pick-and-place machines to assemble the PC boards greatly reduces labor costs;
3. The lighter and more compact assembled products resulting from the smaller dimensions of surface mount packages mean lower material costs.

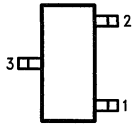
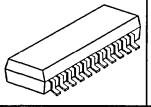
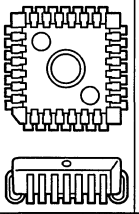
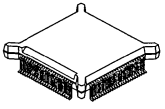
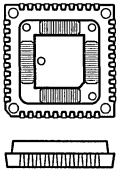
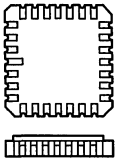
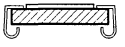
Production processes now permit both surface mount and insertion mount components to be assembled on the same PC board.

SURFACE MOUNT PACKAGING AT NATIONAL

To help our customers take advantage of this new technology, National has developed a line of surface mount packages. Ranging in lead counts from 3 to 360, the package offerings are summarized in Table I.

Lead center spacing keeps shrinking with each new generation of surface mount package. Traditional packages (e.g., DIPs) have a 100 mil lead center spacing. Surface mount packages currently in production (e.g., SOT, SOIC, PCC, LCC, LDCC) have a 50 mil lead center spacing. Surface mount packages in production release (e.g., PQFP) have a 25 mil lead center spacing. Surface mount packages in development (e.g., TAPEPAK™) will have a lead center spacing of only 12–20 mils.

TABLE I. Surface Mount Packages from National

Package Type	Small Outline Transistor (SOT)	Small Outline IC (SOIC)	Plastic Chip Carrier (PCC)	Plastic Quad Flat Pack (PQFP)	TAPEPAK™ (TP)	Leadless Chip Carrier (LCC) (LDCC)	Leaded Chip Carrier
							
Package Material	Plastic	Plastic	Plastic	Plastic	Plastic	Ceramic	Ceramic
Lead Bend	Gull Wing	Gull Wing	J-Bend	Gull Wing	Gull Wing	—	Gull Wing
Lead Center Spacing	50 Mils	50 Mils	50 Mils	25 Mils	20, 15, 12 Mils	50 Mils	50 Mils
Tape & Reel Option	Yes	Yes	Yes	tbd	tbd	No	No
Lead Counts	SOT-23 High Profile SOT-23 Low Profile	SO-8(*) SO-14(*) SO-14 Wide(*) SO-16(*) SO-16 Wide(*) SO-20(*) SO-24(*)	PCC-20(*) PCC-28(*) PCC-44(*) PCC-68 PCC-84 PCC-124	PQFP-84 PQFP-100 PQFP-132 PQFP-196(*) PQFP-244	TP-40 (*) TP-68 TP-84 TP-132 TP-172 TP-220 TP-284 TP-360	LCC-18 LCC-20(*) LCC-28 LCC-32 LCC-44 (*) LCC-48 LCC-52 LCC-68 LCC-84 LCC-124	LDCC-44 LDCC-68 LDCC-84 LDCC-124

*In production (or planned) for linear products.

LINEAR PRODUCTS IN SURFACE MOUNT

Linear functions available in surface mount include:

- Op amps
- Comparators
- Regulators
- References
- Data conversion
- Industrial
- Consumer
- Automotive

A complete list of linear part numbers in surface mount is presented in Table III. Refer to the datasheet in the appropriate chapter of this databook for a complete description of the device. In addition, National is continually expanding the list of devices offered in surface mount. If the functions you need do not appear in Table III, contact the sales office or distributor branch nearest you for additional information.

Automated manufacturers can improve their cost savings by using Tape-and-Reel for surface mount devices. Simplified handling results because hundreds-to-thousands of semiconductors are carried on a single Tape-and-Reel pack (see ordering and shipping information—printed later in this section—for a comparison of devices/reel vs. devices/rail for those surface mount package types being used for linear products). With this higher device count per reel (when compared with less than a 100 devices per rail), pick-and-place machines have to be re-loaded less frequently and lower labor costs result.

With Tape-and-Reel, manufacturers save twice—once from using surface mount technology for automated PC board assembly and again from less device handling during shipment and machine set-up.

BOARD CONVERSION

Besides new designs, many manufacturers are converting existing printed circuit board designs to surface mount. The resulting PCB will be smaller, lighter and less expensive to manufacture; but there is one caveat—be careful about the thermal dissipation capability of the surface mount package.

Because the surface mount package is smaller than the traditional dual-in-line package, the surface mount package is not capable of conducting as much heat away as the DIP (i.e., the surface mount package has a higher thermal resistance—see Table II).

The silicon for most National devices can operate up to a 150°C junction temperature (check the datasheet for the rare exception). Like the DIP, the surface mount package can actually withstand an ambient temperature of up to 125°C (although a commercial temperature range device will only be specified for a max ambient temperature of 70°C and an industrial temperature range device will only be specified for a max ambient temperature of 85°C). See AN-336, "Understanding Integrated Circuit Package Power Capabilities", (reprinted in the appendix of each linear databook volume) for more information.

TABLE II: Surface Mount Package Thermal Resistance Range*

Package	Thermal Resistance** (θ_{jA}, °C/W)
SO-8	120–175
SO-14	100–140
SO-14 Wide	70–110
SO-16	90–130
SO-16 Wide	70–100
SO-20	60–90
SO-24	55–85
PCC-20	70–100
PCC-28	60–90
PCC-44	40–60

*Actual thermal resistance for a particular device depends on die size. Refer to the datasheet for the actual θ_{jA} value.

**Test conditions: PCB mount (FR4 material), still air (room temperature), copper traces (150 × 20 × 10 mils).

Given a max junction temperature of 150°C and a maximum allowed ambient temperature, the surface mount device will be able to dissipate less power than the DIP device. This factor must be taken into account for new designs.

For board conversion, the DIP and surface mount devices would have to dissipate the same power. This means the surface mount circuit would have a lower maximum allowable ambient temperature than the DIP circuit. For DIP circuits where the maximum ambient temperature required is substantially lower than the maximum ambient temperature allowed, there may be enough margin for safe operation of the surface mount circuit with its lower maximum allowable ambient temperature. But where the maximum ambient temperature required of the DIP current is close to the maximum allowable ambient temperature, the lower maximum ambient temperature allowed for the surface mount circuit may fall below the maximum ambient temperature required. The circuit designer must be aware of this potential pitfall so that an appropriate work-around can be found to keep the surface mount package from being thermally overstressed in the application.

SURFACE MOUNT LITERATURE

National has published extensive literature on the subject of surface mount packaging. Engineers from packaging, quality, reliability, and surface mount applications have pooled their experience to provide you with practical hands-on knowledge about the construction and use of surface mount packages.

The applications note AN-450 "Surface Mounting Methods and their Effect on Product Reliability" is referenced on each SMD datasheet. In addition, "Wave Soldering of Surface Mount Components" is reprinted in this section for your information.

TABLE III. Linear Surface Mount Current Device Listing

Amplifiers and Comparators

Part Number	Part Number
LF347WM LF351M LF451CM LF353M	LM392M LM393M LM741CM LM1458M LM2901M
LF355M LF356M LF357M LF444CWM	LM2902M LM2903M LM2904M LM2924M LM3403M
LM10CWM LM10CLWM LM308M LM308AM LM310M	LM4250M LM324M LM339M LM365WM LM607CM
LM311M LM318M LM319M LM324M	LMC669BCWM LMC669CCWM
LM339M LM346M LM348M LM358M LM359M	LF441CM

Regulators and References

Part Number	Part Number
LM317LM LF3334M	LM2931M-5.0 LM3524M LM78L05ACM LM78L12ACM LM78L15ACM
LM336M-2.5 LF336BM-2.5 LM336M-5.0 LM336BM-5.0 LM337LM	LM79L05ACM LM79L12ACM LM79L15ACM LP2951ACM LP2951CM
LM385M LM385M-1.2	
LM385BM-1.2 LM385M-2.5 LM385BM-2.5 LM723CM LM2931CM	

Data Acquisition Circuits

Part Number	Part Number
ADC0802LCV ADC0802LCWM ADC0804LCV ADC0804LCWM ADC0808CCV ADC0809CCV	ADC1025BCV ADC1025CCV DAC0800LCM DAC0801LCM DAC0802LCM DAC0806LCM DAC0807LCM
ADC0811BCV ADC0811CCV ADC0819BCV ADC0819CCV ADC0820BCV ADC0820CCV	DAC0808LCM DAC0830LCWM DAC0830LCV DAC0832LCWM DAC0832LCV
ADC0838BCV ADC0838CCV ADC0841BCV ADC0841CCV ADC0848BCV ADC0848CCV ADC1005BCV ADC1005CCV	

Industrial Functions

Part Number	Part Number
AH5012CM LF13331M LF13509M LF13333M LM555CM	LM13600M LM13700M LMC555CM LM567CM MF4CWM-50
LM556CM LM567CM LM1496M LM2917M	MF4CWM-100 MF6CWM-50 MF10CCWM MF6CWM-100 MF5CWM
LM3046M LM3086M LM3146M	

Commercial and Automotive

Part Number	Part Number
LM386M-1 LM592M LM831M LM832M LM833M	LM1837M LM1851M LM1863M LM1865M LM1870M
LM837M LM838M LM1131CM	LM1894M LM1964V
	LM2893M LM3361AM LM1881M

Hybrids

Part Number	Part Number
LH0002E	LH0032E
LH4002E	LH0033E

A FINAL WORD

National is a world leader in the design and manufacture of surface mount components.

Because of design innovations such as perforated copper leadframes, our small outline package is as reliable as our DIP—the laws of physics would have meant that a straight "junior copy" of the DIP would have resulted in an "S.O." package of lower reliability. You benefit from this equivalence of reliability. In addition, our ongoing vigilance at each step of the production process assures that the reliability we designed in stays in so that only devices of the highest quality and reliability are shipped to your factory.

Our surface mount applications lab at our headquarters site in Santa Clara, California continues to research (and publish) methods to make it even easier for you to use surface mount technology. Your problems are our problems.

When you think "Surface Mount"—think "National"!

Ordering and Shipping Information

When you order a surface mount semiconductor, it will be in one of the several available surface mount package types. Specifying the Tape-and-Reel method of shipment means that you will receive your devices in the following quantities per Tape-and-Reel pack: SMD devices can also be supplied in conventional conductive rails.

Package	Package Designator	Max/Rail	Per Reel*
SO-8	M	100	2500
SO-14	M	50	2500
SO-14 Wide	WM	50	1000
SO-16	M	50	2500
SO-16 Wide	WM	50	1000
SO-20	M	40	1000
SO-24	M	30	1000
PCL-20	V	50	1000
PCL-28	V	40	1000
PCL-44	V	25	500
PQFP-196	VF	TBD	—
TP-40	TP	100	TBD
LCC-20	E	50	—
LCC-44	E	25	—

*Incremental ordering quantities. (National Semiconductor reserves the right to provide a smaller quantity of devices per Tape-and-Reel pack to preserve lot or date code integrity. See example below.)

Example: You order 5,000 LM324M ICs shipped in Tape-and-Reel.

- Case 1: All 5,000 devices have the same date code
  - You receive 2 SO-14 (Narrow) Tape-and-Reel packs, each having 2500 LM324M ICs
- Case 2: 3,000 devices have date code A and 2,000 devices have date code B
  - You receive 3 SO-14 (Narrow) Tape-and-Reel packs as follows:

    Pack #1 has 2,500 LM324M ICs with date code A

    Pack #2 has 500 LM324M ICs with date code A

    Pack #3 has 2,000 LM324M ICs with date code B

Short-Form Procurement Specification

TAPE FORMAT

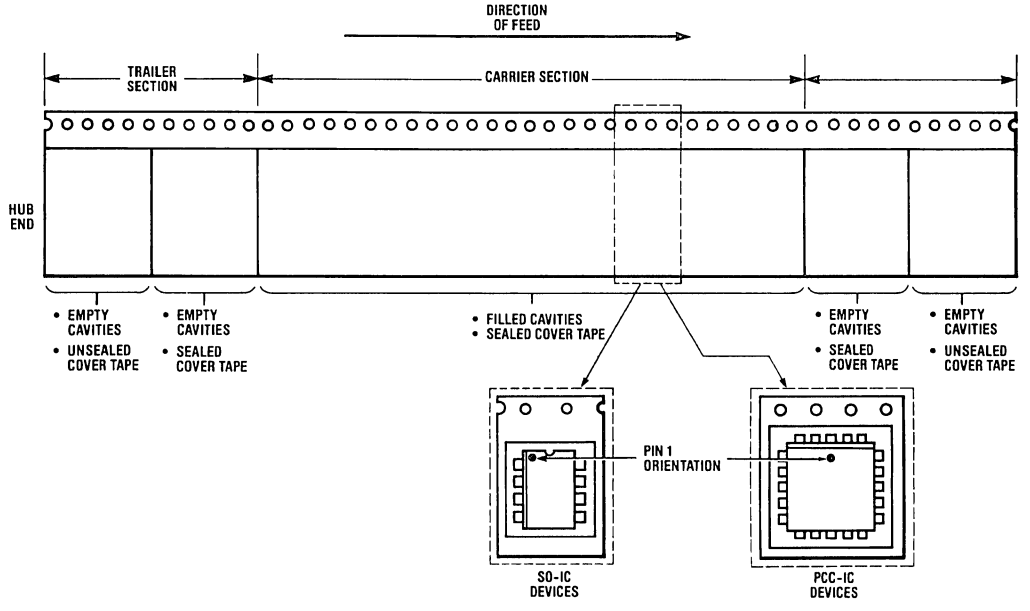
→ Direction of Feed

	Trailer (Hub End)*		Carrier*	Leader (Start End)*	
	Empty Cavities, min (Unsealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Filled Cavities (Sealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Empty Cavities, min (Unsealed Cover Tape)
Small Outline IC					
SO-8 (Narrow)	2	2	2500	5	5
SO-14 (Narrow)	2	2	2500	5	5
SO-14 (Wide)	2	2	1000	5	5
SO-16 (Narrow)	2	2	2500	5	5
SO-16 (Wide)	2	2	1000	5	5
SO-20 (Wide)	2	2	1000	5	5
SO-24 (Wide)	2	2	1000	5	5
Plastic Chip Carrier IC					
PCC-20	2	2	1000	5	5
PCC-28	2	2	750	5	5
PCC-44	2	2	500	5	5

***The following diagram identifies these sections of the tape and Pin #1 device orientation.**

Short-Form Procurement Specification (Continued)

DEVICE ORIENTATION



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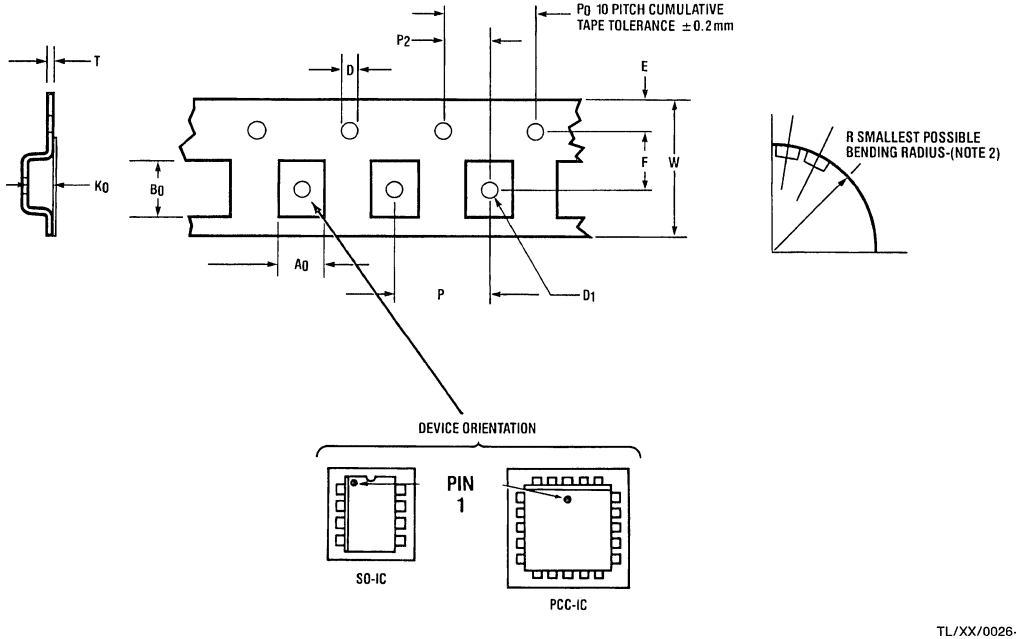
MATERIALS

- Cavity Tape: Conductive PVC (less than 10^5 Ohms/Sq)
- Cover Tape: Polyester
  - (1) Conductive cover available
- Reel:
  - (1) Solid 80 pt fibreboard (standard)
  - (2) Conductive fibreboard available
  - (3) Conductive plastic (PVC) available

TAPE DIMENSIONS (24 Millimeter Tape or Less)



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Short-Form Procurement Specification (Continued)

	W	P	F	E	P_2	P_0	D	T	A_0	B_0	K_0	D_1	R
Small Outline IC													
SO-8 (Narrow)	12±.30	8.0±.10	5.5±.05	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.4±.10	5.2±.10	2.1±.10	1.55±.05	30
SO-14 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	9.0±.10	2.1±.10	1.55±.05	40
SO-14 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	9.5±.10	3.0±.10	1.55±.05	40
SO-16 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	10.3±.10	2.1±.10	1.55±.05	40
SO-16 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	10.76±.10	3.0±.10	1.55±.05	40
SO-20 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	13.3±.10	3.0±.10	2.05±.05	50
SO-24 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	15.85±.10	3.0±.10	2.05±.05	50
Plastic Chip Carrier IC													
PCC-20	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	9.3±.10	9.3±.10	4.9±.10	1.55±.05	40
PCC-28	24±.30	16.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	13.0±.10	13.0±.10	4.9±.10	2.05±.05	50

Note 1: A_0, B_0 and K_0 dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

Note 2: Tape with components shall pass around a mandril radius R without damage.

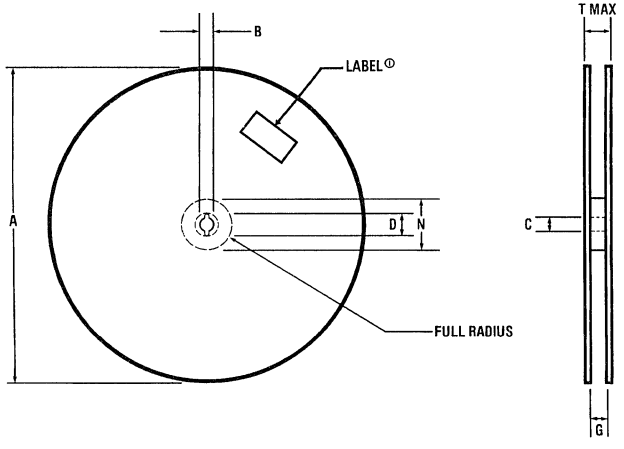
Note 3: Cavity tape material shall be PVC conductive (less than 10^5 Ohms/Sq).

Note 4: Cover tape material shall be polyester (30–65 grams peel-back force).

Note 5: D_1 Dimension is centered within cavity.

Note 6: All dimensions are in millimeters.

REEL DIMENSIONS



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STAR™* Surface Mount Tape and Reel

Short-Form Procurement Specifications (Continued)

		A (Max)	B (Min)	C	D (Min)	N (Min)	G	T (Max)
12 mm Tape	SO-8 (Narrow)	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.488^{+.078}_{-.000}$ 12.4^{+2}_{-0}	.724 18.4
16 mm Tape	SO-14 (Narrow) SO-14 (Wide) SO-16 (Narrow) SO-16 (Wide) PCC-20	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.646^{+.078}_{-.000}$ 16.4^{+2}_{-0}	.882 22.4
24 mm Tape	SO-20 (Wide) SO-24 (Wide) PCC-28	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.960^{+.078}_{-.000}$ 24.4^{+2}_{-0}	1.197 30.4
32 mm Tape	PCC-44	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$1.276^{+.078}_{-.000}$ 32.4^{+2}_{-0}	1.512 38.4

Units: Inches / Millimeters

Material: Paperboard (Non-Flaking)

LABEL

Human and Machine Readable Label is provided on reel. A variable (C.P.I) density code 39 is available. NSC STD label (7.6 C.P.I.)

FIELD

Lot Number

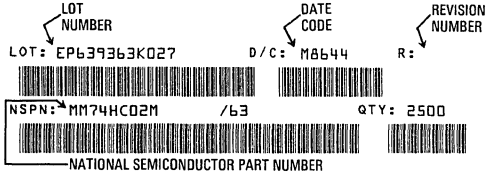
Date Code

Revision Level

National Part No. I.D.

Qty.

EXAMPLE



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Fields are separated by at least one blank space.

Future Tape-and-Reel packs will also include a smaller-size bar code label (high-density code 39) at the beginning of the tape. (This tape label is not available on current production.)

National Semiconductor will also offer additional labels containing information per your specific specification.

Wave Soldering of Surface Mount Components

ABSTRACT

In facing the upcoming surge of "surface mount technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this new process. However, as the availability of surface mount components is still limited, may have taken to mixing the lead-inserted standard dual-in-line packages (DIPs) with the surface mounted devices (SMDs). Furthermore, to take advantage of using both sides of the board, surface-mounted components are generally adhered to the bottom side of the board while the top side is reserved for the conventional lead-inserted packages. If processed through a wave solder machine, the semiconductor components are now subjected to extra thermal stresses (now that the components are totally immersed into the molten solder).

A discussion of the effect of wave soldering on the reliability of plastic semiconductor packages follows. This is intended to highlight the limitations which should be understood in the use of wave soldering of surface mounted components.

ROLE OF WAVE-SOLDERING IN APPLICATION OF SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave-soldering machine.

Wave Soldering of Surface Mount Components (Continued)

The reasons being:

1) Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.
2) Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.
3) Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW BOARD ASSEMBLY PROCEDURES

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.
b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or combination of two or more methods.

The various processes that may be employed are:

A) Wave Solder before Vapor/IR reflow solder.
   1. Components on the same side of PW Board.
      Lead insert standard DIPS onto PW Board Wave solder (conventional)
      Wash and lead trim
      Dispense solder paste on SMD pads
      Pick and place SMDs onto PW Board
      Bake
      Vapor phase/IR reflow
      Clean
   2. Components on opposite side of PW Board.
      Lead insert standard DIPs onto PW Board
      Wave Solder (conventional)
      Clean and lead trim
      Invert PW Board
      Dispense solder paste on SMD pads
      Dispense drop of adhesive on SMD sites (optional for smaller components)
      Pick and place SMDs onto board
      Bake/Cure
      Invert board to rest on raised fixture
      Vapor/IR reflow soldering
      Clean

B) Vapor/IR reflow solder then Wave Solder.
   1. Components on the same side of PW Board.
      Solder paste screened on SMD side of Printed Wire Board
      Pick and place SMDs
      Bake
      Vapor/IR reflow
      Lead insert on same side as SMDs
      Wave solder
      Clean and trim underside of PCB

C) Vapor/IR reflow only.
   1. Components on the same side of PW Board.
      Trim and form standard DIPs in "gull wing" configuration
      Solder paste screened on PW Board
      Pick and place SMDs and DIPs
      Bake
      Vapor/IR reflow
      Clean
   2. Components on opposite sides of PW Board.
      Solder paste screened on SMD-side of Printed Wire Board
      Adhesive dispensed at central location of each component
      Pick and place SMDs
      Bake
      Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads
      Lead insert DIPs
      Vapor/IR reflow
      Clean and lead trim

D) Wave Soldering Only
   1. Components on opposite sides of PW Board.
      Adhesive dispense on SMD side of PW Board
      Pick and place SMDs
      Cure adhesive
      Lead insert top side with DIPs
      Wave solder with SMDs down and into solder bath
      Clean and lead trim

All of the above assembly procedures can be divided into three categories for I.C. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a 'pallet' where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Wave Soldering of Surface Mount Components (Continued)

THERMAL CHARACTERISTICS OF MOLDED INTEGRATED CIRCUITS

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1*. Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on lead frames, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of lead frame material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal lead frame in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the expoxy-metal interface. However, if the package is subjected to temprature above its glass-transition temperature, the epoxy will begin to expand much faster than the metal and the probability of separation is greatly increased.

CONVENTIONAL WAVE-SOLDERING

Most wave-soldering operations occur at temperatures between 240–260°C. Conventional epoxies for encapsulation have glass-transition temperature between 140–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1) The PW board has a certain amount of heat-sink effect and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.
2) In conventional soldering, only the tip of each lead in a DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

EFFECT ON PACKAGE PERFORMANCE BY EPOXY-METAL SEPARATION

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metallization over time and premature failure of the device in the field.

VAPOR PHASE/IR REFLOW SOLDERING

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Operating temperatures are 215°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-lead frame interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

BIAS MOISTURE TEST

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a stream chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and

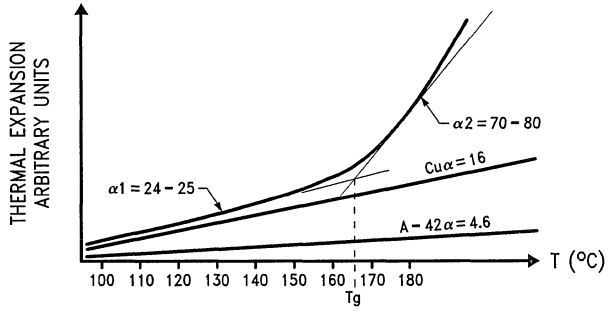

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FIGURE 1. Thermal Expansion and Glass Transition Temperature

Wave Soldering of Surface Mount Components (Continued)

85% relative humidity. Once cycle of approximately 100 hours has been shown to be equivalent to 2000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

TEST RESULTS

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave-soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec. exposure @ 215°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H., 85°C for 2000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4000 hours 85/85 test. Results were compared for packages by itself against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results (85% R.H./85°C Bias Moisture Test, 2000 hours) (# Failures/Total Tested)

	Unmounted	Mounted
Control/Vapor Phase 15 sec @ 215°C	0/114	0/84
Solder Dip 2 sec @ 260°C	2/144 (1.4%)	0/85
Solder Dip 4 sec @ 260°C	—	0/83
Solder Dip 6 sec @ 260°C	13/248 (5.2%)	1/76 (1.3%)
Solder Dip 10 sec @ 260°C	14/127 (11.0%)	3/79 (3.8%)
Package: SO-14 lead Device: LM324M		

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the package being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6000 hours in a 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturers Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Tested)

Package SO-8	Vapor Phase 30 sec	Wave Solder 2 sec	Wave Solder 4 sec	Wave Solder 6 sec	Wave Solder 10 sec
Manuf A	8/30*	1/30*	0.30	12/30*	16/30*
Manuf B	2/30*	8/30*	2/30*	22/30*	20/30*
Manuf C	0/30	0/29	0/29	0/30	0/30
Manuf D	1/30*	0/30	12/30*	14/30*	2/30*
Manuf E	1/30**	0/30	0/30	0/30	0/30
Manuf F	0/30	0/30	0/30	0/30	0/30
Manuf G	0/30	0/30	0/30	0/30	0/30

*Corrosion-failures

**No Visual Defects—Non-corrosion failures

Test: Accelerated Bias Moisture Test; 85% R.H./85°C, 6000 equivalent hours.

SUMMARY

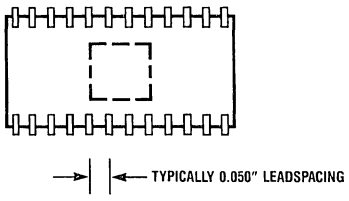
Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in a hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low Tg compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

Small Outline (SO) Package Surface Mounting Methods— Parameters and Their Effect on Product Reliability

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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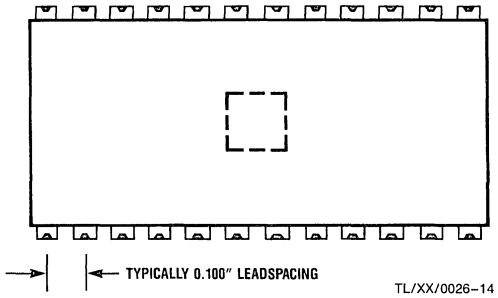
Standard DIP Package



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

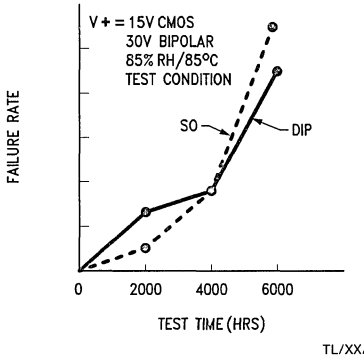

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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

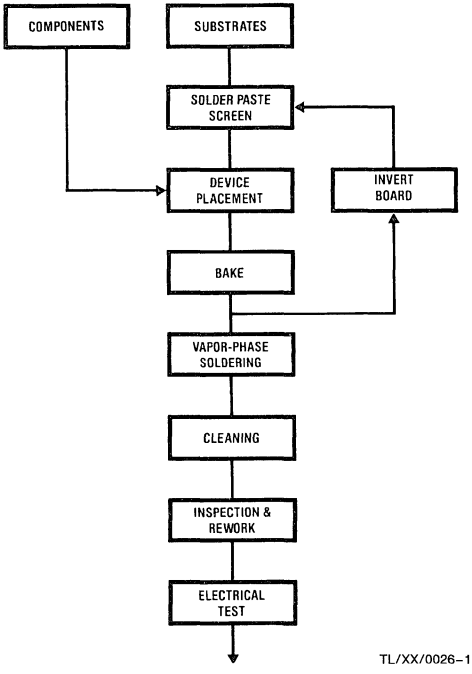
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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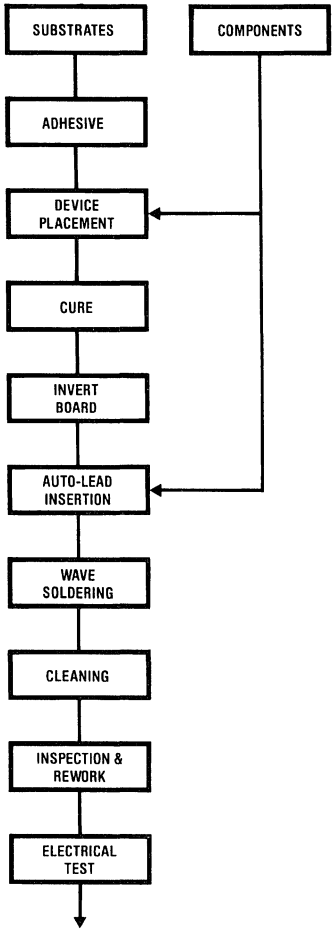
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

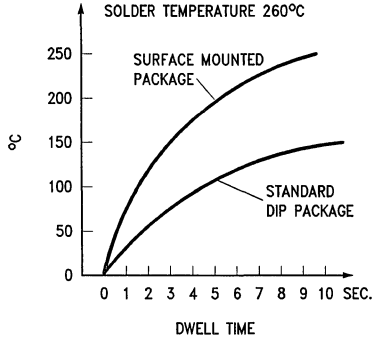

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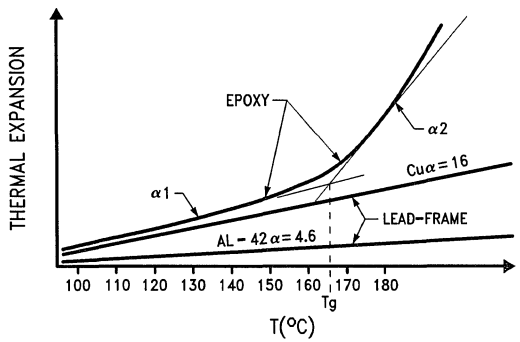
FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.



TL/XX/0026–19

FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

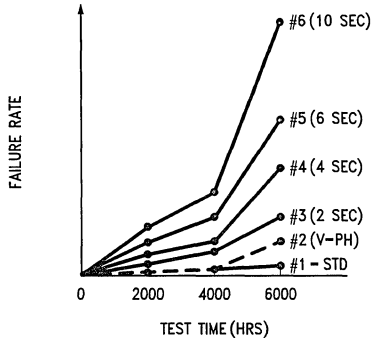


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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

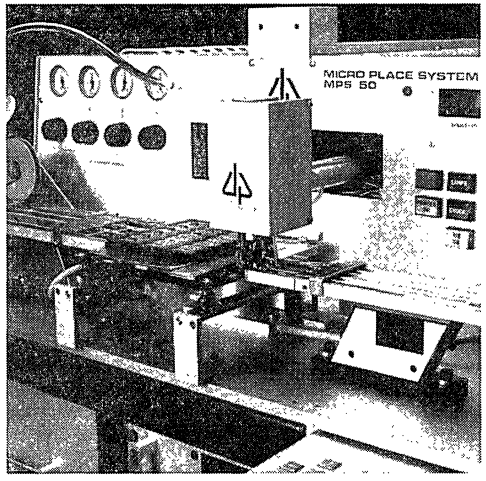
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

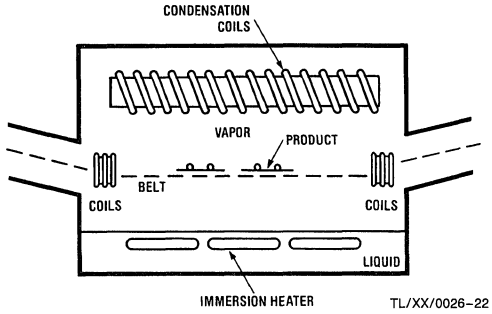
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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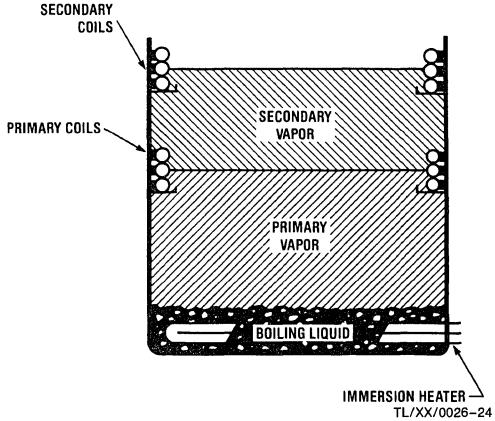
The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

TL/XX/0026–23

Batch-Fed Production Vapor-Phase Soldering Unit



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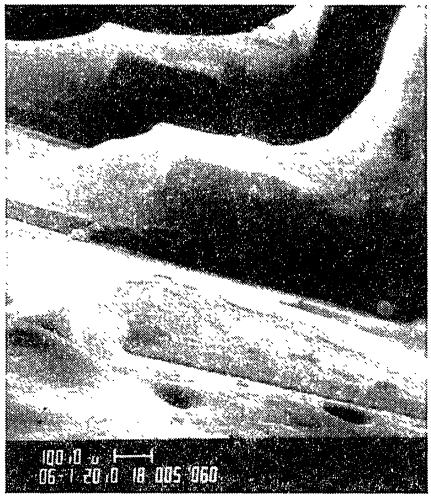
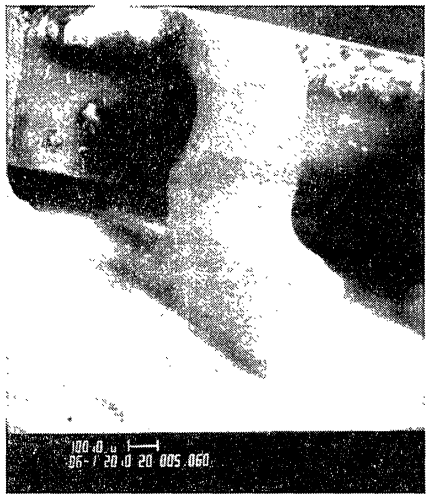
Solder Joints on a SO-14 Package on PCB



TL/XX/0026–25

Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050" lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005" usually used to achieve a solder paste thickness (wet) of about 0.008" typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed $\frac{1}{8}$", to avoid damage to screens and minimize distortion.

SOLDER PASTE

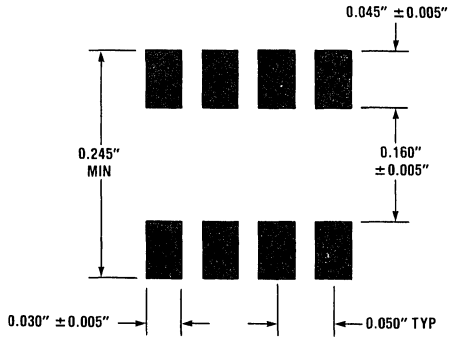
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

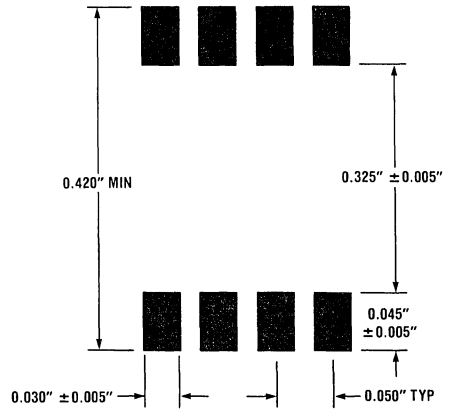
RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



TL/XX/0026-27

SO-16L, SO-20



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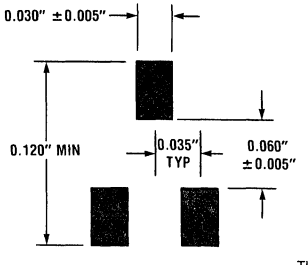
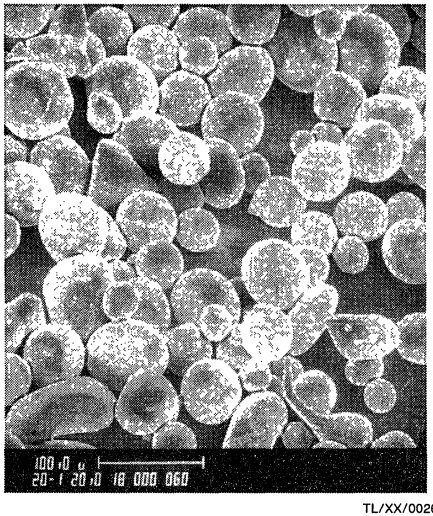
SOT-23



TL/XX/0026-29

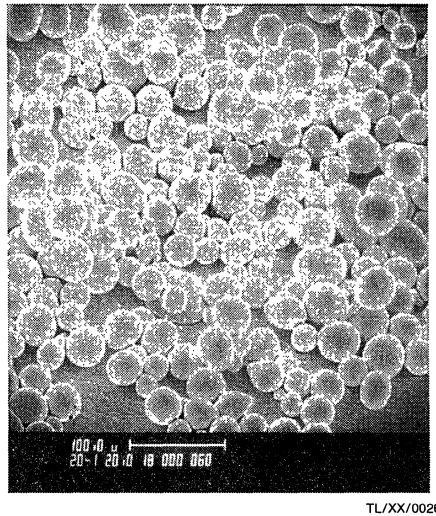
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



TL/XX/0026-30

200 × Kester (63/37)



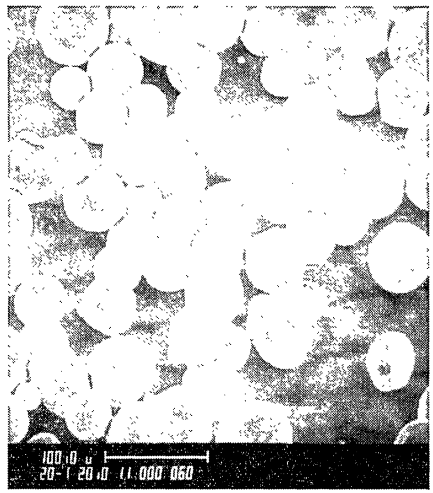
TL/XX/0026-31

Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads

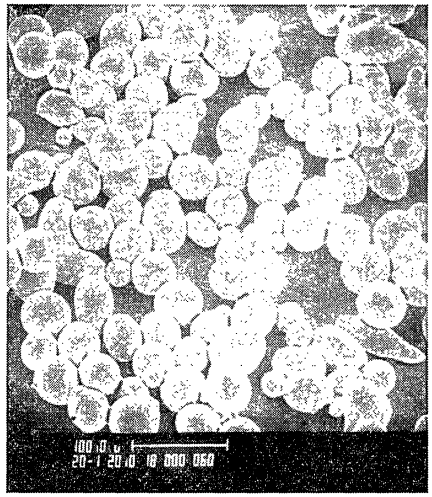
TL/XX/0026-32

200 × Fry Metal (63/37)



TL/XX/0026-33

200 ESL (63/37)



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CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

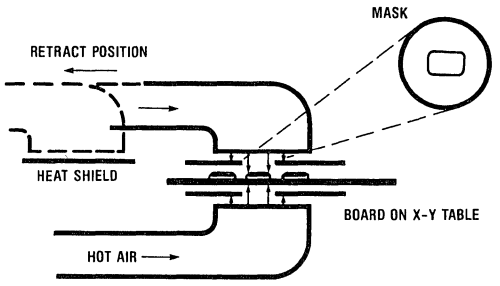
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



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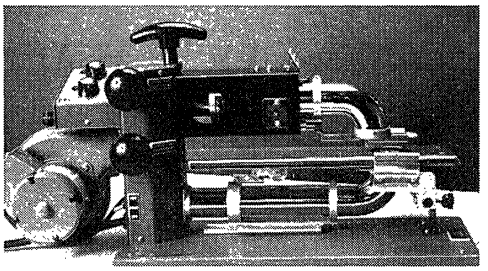
Hot-Air Rework Machine



TL/XX/0026-36

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

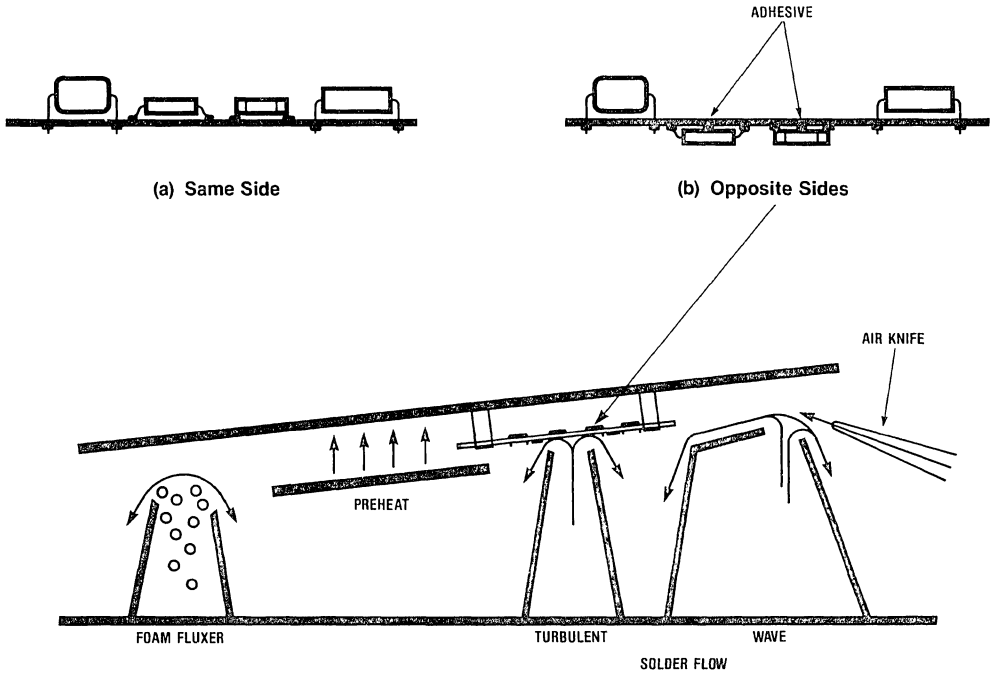
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050" vs 0.100" for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



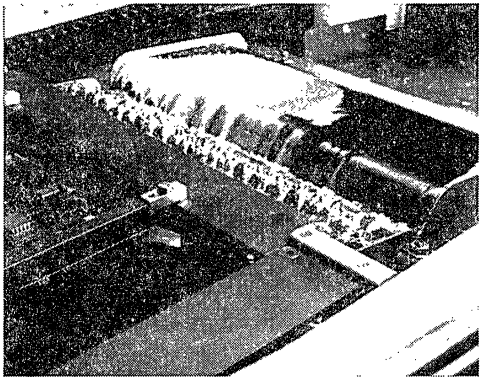
TL/XX/0026-37

A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



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CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

Section 7

Appendices/ Physical Dimensions

Section 7 Contents

National Semiconductor Corporation

Appendix A
General Product Marking & Code Explanation

LF 356 N /A+

- /A+ — RELIABILITY PROGRAM (OPTIONAL) (REFER TO PROGRAM)
- N — PACKAGE TYPE (SEE BELOW)
- 356 — DEVICE NUMBER (GENERIC TYPE) AND SUFFIX LETTER (OPTIONAL)
  - A: INPROVED ELECTRICAL SPECIFICATION
  - C: COMMERCIAL TEMPERATURE RANGE (2ND SOURCE PRODUCTS)
- LF — DEVICE FAMILY (SEE BELOW)

TL/XX/0027-1

Device Family

Integrated Circuits (IC's)

ADC	Data Conversion
AF	Active Filter
AH	Analog Switch (Hybrid)
AM	Analog Switch (Monolithic)
DAC	Data Conversion
DM	Digital (Monolithic)
HS	Hybrid
LF	Linear (Bifet)
LH	Linear (Hybrid)
LM	Linear (Monolithic)
LMC	Linear CMOS
LP	Linear (Low Power)
MF	Linear (Monolithic Filter)
SL	Special Linear
LMF	Linear Monolithic Filter

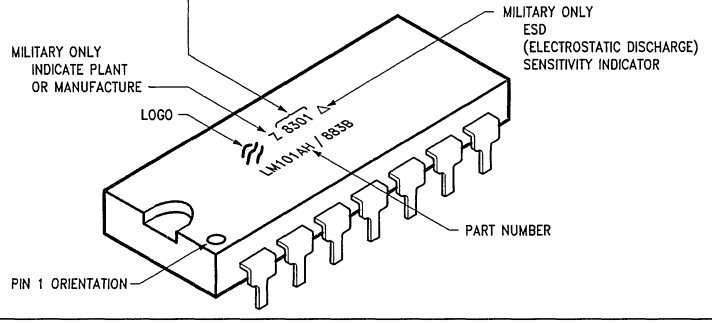
Package Type*

IC's Only

D	Glass/Metal DIP
E	Ceramic Leadless Chip Carrier (LCC)
F	Glass/Metal Flat Pak (¼" x ¼")
G	12 Lead TO-8 M/C
H	Multi-Lead M/C
H-05	4 Lead M/C (TO-5) } Shipped with
H-46	4 Lead M/C (TO-46) } Thermal Shield
J	Lo-Temp Ceramic DIP (Sometimes referred to as the "Fit-Seal" Package).
J-8	8 Lead Ceramic DIP ("MiniDIP")
J-14	14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg).
K	TO-3 M/C in Steel, except LM309K which is shipped in Aluminum
KC	TO-3 M/C (Aluminum)
K Steel	TO-3 M/C (Steel)
M	Small Outline Package
N	Molded DIP (EPOXY B)
N-01	Molded DIP (Epoxy B) with Staggered Leads
N-8	8 Lead Molded DIP (Epoxy B) ("Mini-DIP")
N-14	14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg).
P	3 Lead TO-202 PWR Pkg
Q	Cerdip with UV Window
T	3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B)
V	Multi-lead Plastic Chip Carrier (PCC)
W	Lo-Temp Ceramic Flat Pak
WM	Wide Body Small Outline Package

DATE CODE
NON-MILITARY
2ND DIGIT = CALENDAR YEAR
3RD & 4TH DIGITS = CALENDAR WORK WEEK

MILITARY = 883B & M38510
1ST & 2ND DIGITS = CALENDAR YEAR
3RD & 4TH DIGITS = CALENDAR WORK WEEK
(EXAMPLE: 8301 = 1ST WEEK OF 1983)



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Appendix B

APPLICATION NOTE REFERENCED BY PART NUMBER

National Semiconductor Linear Application notes are normally written to explain the operation and use of a particular device or family of IC's, or to present alternative technical solutions. The following PART NUMBER index references the published application notes that would offer application assistance for those specific IC's.

The 1986 Linear Applications Handbook is a complete text for all current Application Notes for both Monolithic and Hybrid products. Specific Application Notes are available upon request through National Semiconductor Sales Offices.

DEVICE NUMBER	APPLICATION NOTE
ADCXXXX	AN-156
ADC80	AN-360
ADC0801	AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53
ADC0802	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0803	AN-233, AN–274, AN-280, AN-281, LB-53
ADC0804	AN-233, AN-274, AN-276, AN-280, AN-281, LB-53
ADC0805	AN-233, AN-274, AN-280, AN-281, LB-53
ADC0808	AN-247, AN-280, AN-281
ADC0809	AN-247, AN-280
ADC0816	AN-193, AN-247, AN-258, AN-280
ADC0817	AN-247, AN-258, AN-280
ADC0820	AN-237
ADC0831	AN-280, AN-281
ADC0832	AN-280, AN-281
ADC0833	AN-280, AN-281
ADC0834	AN-280, AN-281
ADC0838	AN-280, AN-281
ADC1001	AN-276, AN-280, AN-281
ADC1005	AN-280
ADC1210	AN-245
ADC3501	AN-200, AN-202
ADC3511	AN-200
ADC3701	AN-200
ADC3711	AN-200
AH0014	AN-38
AH0019	AN-38
CD4016	AB-10
DACXXXX	AN-156
DAC0830	AN-284
DAC0831	AN-271, AN-284
DAC0832	AN-271, AN-284
DAC1000	AN-271, AN-275, AN-277, AN-284
DAC1001	AN-271, AN-275, AN-277, AN-284
DAC1002	AN-271, AN-275, AN-277, AN-284
DAC1006	AN-271, AN-275, AN-277, AN-284
DAC1007	AN-271, AN-275, AN-277, AN-284

DEVICE NUMBER	APPLICATION NOTE
DAC1008	AN-271, AN-275, AN-277, AN-284
DAC1020	AN-263, AN-269, AN-293, AN-294, AN-299
DAC1021	AN-269
DAC1022	AN-269
DAC1208	AN-271, AN-284
DAC1209	AN-271, AN-284
DAC1210	AN-271, AN-284
DAC1218	AN-293
DAC1220	AN-253, AN-269
DAC1221	AN-269
DAC1222	AN-269
DAC1230	AN-284
DAC1231	AN-271, AN-284
DAC1232	AN-271, AN-284
DAC1280	AN-261, AN-263
DH0034	AN-253
DH0035	AN-49
DS8606	AN-381, AN-382
DS8608	AN-382
DT1058	AN-287
DT1060	AN-287
DTSW250E2	AN-287
DTSW250GI	AN-287
INS8070	AN-260
LF111	LB-39
LF155	AN-263, AN-447
LF198	AN-245, AN-294
LF311	AN-301
LF347	AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447
LF351	AN-242, AN-263, AN-266, AN-271, AN-275, AN-293, AN-447, Appendix C
LF351A	AN-240
LF351B	Appendix D
LF353	AN-256, AN-258, AN-263, AN-264, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D
LF356	AN-253, AN-258, AN-260, AN-263, AN-266, AN-271, AN-272, AN-275, AN-293, AN-294, AN-295, AN-301, AN-447
LF357	AN-263, AN-447, LB-42
LF398	AN-247, AN-258, AN-266, AN-294, AN-298, LB-45
LF400	AN-428, AN-447
LF411	AN-294, AN-301, AN-344, AN-447
LF412	AN-272, AN-299, AN-301, AN-344, AN-447
LF441	AN-301, AN-447
LF13006	AN-344
LF13007	AN-344
LF13331	AN-294, AN-447
LF13508	AN-289, AN-360, AN-447
LF13509	AN-289, AN-295, AN-447
LH0002	AN-13, AN-63, AN-227, AN-244, AN-263, AN-272, AN-301
LH0022	AN-63, AN-75
LH0023	AN-245, AN-360
LH0024	AN-253
LH0032	AN-242, AN-244, AN-253
LH0033	AN-48, AN-115, AN-227, AN-253
LH0042	AN-63

DEVICE NUMBER	APPLICATION NOTE
LH0043	AN-245
LH0052	AN-63
LH0053	AN-245
LH0062	AN-75
LH0063	AN-227
LH0070	AN-301
LH0071	AN-245
LH0082	AN-244, AN-266
LH0086	AN-245, AN-360
LH0091	AN-180
LH0094	AN-301
LH0101	AN-261
LH1605	AN-343
LM10	AN-211, AN-247, AN-258, AN-271, AN-288, AN-299, AN-300
LM11	AN-241, AN-242, AN-260, AN-266, AN-271
LM12	AN-446
LM101	AN-4, AN-13, AN-20, AN-24, AN-75, LB-42, Appendix A
LM101A	AN-29, AN-30, AN-31, AN-79, AN-241, LB-1, LB-2, LB-4, LB-8, LB-14, LB-16, LB-19, LB-28
LM102	AN-4, AN-13, AN-30, LB-1, LB-5, LB-6, LB-11
LM103	AN-110, LB-41
LM104	AN-21, LB-3, LB-7, LB-10, LB-40
LM105	AN-21, AN-23, AN-110, LB-3, LB-7, LB-10
LM106	AN-41, LB-6, LB-12
LM107	AN-20, AN-31, LB-1, LB-12, LB-19, Appendix A
LM108	AN-29, AN-30, AN-31, AN-63, AN-79, AN-211, AN-241, LB-14, LB-15, LB-21
LM108A	AN-260, LB-15, LB-19
LM109	AN-42, LB-15
LM109A	LB-15
LM110	LB-11, LB-42
LM111	AN-41, AN-103, LB-12, LB-16, LB-32, LB-39
LM112	AN-63, LB-19
LM113	AN-56, AN-110, LB-21, LB-24, LB-28, LB-37
LM117	AN-178, AN-181, AN-182, LB-46, LB-47
LM117HV	LB-46, LB-47
LM118	LB-17, LB-19, LB-21, LB-23, Appendix A
LM119	AN-115, LB-23
LM120	AN-182
LM121	AN-79, AN-104, AN-184, AN-260, LB-22
LM121A	LB-32
LM122	AN-97, LB-38
LM125	AN-82
LM126	AN-82
LM129	AN-173,AN-178, AN-262, AN-266
LM131	AN-210, Appendix D
LM131A	AN-210
LM134	LB-41
LM135	AN-225, AN-262, AN-292, AN-298
LM137	LB-46
LM137HV	LB-46
LM138	LB-46
LM139	AN-74
LM143	AN-127, AN-271
LM148	AN-260

DEVICE NUMBER	APPLICATION NOTE
LM150	LB-46
LM158	AN-116
LM160	AN-87
LM161	AN-87, AN-266
LM163	AN-295
LM194	AN-222, LB-21
LM195	AN-110
LM199	AN-161, AN-260, AN-360
LM199A	AN-161
LM211	LB-39
LM216A	LB-37
LM231	AN-210
LM231A	AN-225
LM235	AN-225
LM239	AN-74
LM258	AN-116
LM260	AN-87
LM261	AN-87
LM301A	AN-178, AN-181, AN-222
LM304	LB-40
LM308	AN-88, AN-184, AN-272, LB-22, LB-28, Appendix D
LM308A	AN-225, LB-24
LM309	AN-178, AN-182
LM311	AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39
LM313	AN-263
LM316	AN-258
LM317	AN-178, LB-35, LB-46
LM317H	LB-47
LM318	AN-115, AN-299, LB-21
LM319	AN-115, AN-271, AN-293
LM320	AN-288
LM321	LB-24
LM324	AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C
LM329	AN-256, AN-263, AN-284, AN-295, AN-301
LM329B	AN-225
LM330	AN-301
LM331	AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix, C Appendix D
LM331A	AN-210, Appendix C
LM334	AN-242, AN-256, AN-284
LM335	AN-225, AN-263, AN-295
LM336	AN-202, AN-247, AN-258
LM337	LB-46
LM338	LB-49, LB-51
LM339	AN-74, AN-245, AN-274
LM340	AN-103, AN-182
LM340L	AN-256
LM342	AN-288
LM346	AN-202, LB-54
LM347	LB-44
LM348	AN-202, LB-42
LM349	LB-42
LM358	AN-116, AN-247, AN-271, AN-274, AN-284, AN-298, Appendix C
LM358A	Appendix D

DEVICE NUMBER	APPLICATION NOTE
LM3045	AN-286
LM3046	AN-146, AN-299
LM3089	AN-147
LM3524	AN-272, AN-288, AN-292, AN-293
LM3820	AN-147, LB-29
LM3900	AN-72, AN-263, AN-274, AN-278, LB-20, AB-24
LM3909	AN-154
LM3911	LB-27
LM3914	LB-48, AB-25
LM3915	AN-386
LM3999	AN161
LM4250	AN-88, LB-34
LM7800	AN-178
LM78L12	AN-146
LMC835	AN-435
LP324	AN-284
MF10	AN-307
MM1458	AN-116
MM1558	AN-116
MM1558C	AN-116
MM2716	LB-54
MM54104	AN-252, AN-287, LB-54
MM57110	AN-382
MM74C00	AN-88
MM74C02	AN-88
MM74C04	AN-88
MM74C948	AN-193
MM74LS138	LB-54
2N4339	AN-32
LH4101	AN-480
LM34/35	AN-460
LM32900	AN-478
LM3578	AB-30
LPXXXX	AN-462
LM34	AN-462
LM35	AN-462
LM385	AN-462
LMC13334	AN-462
LP2950	AN-462
LP2951	AN-462
LP311	AN-462
LP324	AN-462
LP339	AN-462
LP365	AN-462

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Appendix C
Summary of Commercial Reliability Programs

General

National Semiconductor Commercial Reliability Programs provide a broad range of off-the-shelf enhanced semiconductor products that supply an extra measure of quality and reliability needed in high-stress or difficult to service applications.

National's A+ and B+ programs allow each individual customer to:

- Minimize the need for incoming electrical inspection
- Eliminate the need and associated costs of using independent testing laboratories
- Reduction in infant mortality rate
- Reduction in reworked board costs
- Reduction in warranty and service costs

A+ Product Enhancement

The A+ Product Enhancement incorporates the benefits of the Multiple-Pass and Elevated Temperature along with "BURN-IN."

The A+ Program provides:

- 100% Temperature Cycling
- 100% Electrical Testing at Room and High Temperature
- 100% Burn-In Testing Combining Increased Temperature with Applied Voltage
- Acceptable Quality Levels Greater than Industry Norm

Typical A+ Flow is:

- SEM
- Assembly and Seal
- Four Hour 150°C Bake
- Five Temperature Cycles (0°C to +100°C)
- High Temperature Electrical Test
- Electrical Test
- Burn-In (160 hours at a minimum junction temperature of 125°C)
- DC Parametric and Function Tests
- Tightened Quality Control Inspection Plans

Note: Certain products may follow slightly different process flows dictated by specific capabilities and device characteristics, consult NSC.

P+ Product Enhancement

The P+ product enhancement program applies to regulator devices and offers an added advantage. P+ involves a dynamic self-heating burn-in that tests the thermal shutdown of the regulator. P+ is proven more effective than the standard 125°C burn-in as an early screen for infant mortality defects. It sharply reduces the cost of testing incoming components. Reliability Report L-140 further explains the P+ process. The following chart lists regulators which receive P+ prior to shipment and at no additional cost.

Device	Package Types				
	TO-3 K STEEL	TO-39 H	TO-220 T	TO-202 P	TO-92 Z
LM109/309	X	X			
LM117/317	X	X	X	X	
LM117HV/317HV	X	X			
LM120/320	X	X	X	X	
LM123/323	X				
LM137/337	X	X	X	X	
LM137HV/337HV	X	X			
LM138/338	X				
LM140/340	X	X	X	X	
LM145/345	X				
LM150/250/350	X				
LM196/396	X				
LM2930/2935/2940/2984			X		
LM2931			X		X
LM78XX			X		

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Appendix D
Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our *1987 Reliability Handbook.*

MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government-certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table III.

Tables I and II explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales offices, or DESC. DESC is located in Dayton, Ohio.

MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision C of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification Program). The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

TABLE I. The MIL-M-38510 Part Marking

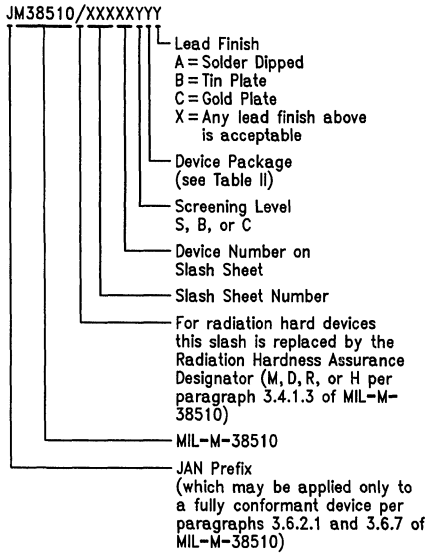

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TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-Pin 1/4" X 1/4" (metal) flat pack
B	14-Pin 3/16" X 1/4" flat pack
C	14-Pin 1/4" X 3/4" dual-in-line
D	14-Pin 1/4" X 3/8" (ceramic) flat pack
E	16-Pin 1/4" X 3/8" dual-in-line
F	16-Pin 1/4" X 3/8" (metal or ceramic) flat pack
G	8-pin TO-99 can or header
H	10-pin 1/4" x 1/4" (metal) flat pack
I	10-pin TO-100 can or header
J	24-pin 1/2" x 1-1/4" dual-in-line
K	24-pin 3/8" x 5/8" flat pack
L	24-pin 1/4" x 1-1/4" dual-in-line
M	12-pin TO-101 can or header
N	(Note 1)
P	8-pin 1/4" x 3/8" dual-in-line
Q	40-pin 3/16" x 2-1/16" dual-in-line
R	20-pin 1/4" x 1-1/16" dual-in-line
S	20-pin 1/4" x 1/2" flat pack
T	(Note 1)
U	(Note 1)
V	18-pin 3/8" x 15/16" dual-in-line
W	22-pin 3/8" x 1-1/8" dual-in-line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350" x 0.350" chip carrier
3	28-terminal 0.450" x 0.450" chip carrier

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

Screen	Class S		Class B	
	Method	Reqmt	Method	Reqmt
1. Wafer Lot Acceptance	5007	All Lots		—
2. Nondestructive Bond Pull	2023	100%		—
3. Internal Visual (Note 1)	2010, Condition A	100%	2010, Condition B	100%
4. Stabilization Bake	1008, Condition C, 24 hrs. Min.	100%	1008, Condition C, 24 hrs. Min.	100%
5. Temp. Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6. Constant Acceleration	2001, Condition E (Min.) Y_1 Orientation Only	100%	2001, Condition E, (Min.), Y_1 Orientation Only	100%
7. Visual Inspection (Note 3)		100%		100%
8. Particle Impact Noise Detection (PIND)	2020, Condition A (Note 4)	100%		—
9. Serialization	(Note 5)	100%		—
10. Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	—
11. Burn-In Test	1015 240 Hrs. @ 125°C Min. (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min.	100%
12. Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%		
13. Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min. (Cond. F Not Allowed)	100%		—
15. PDA Calculation	5% Parametric (Note 14), 3% Functional −25°C	All Lots	5% Parametric (Note 14)	All Lots
16. Final Electrical Test a) Static Tests	Per Applicable Device Specification		Per Applicable Device Specification	
1) 25°C (Subgroup 1, Table I, 5005)		100%		100%
2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005)		100%		100%
b) Dynamic Tests & Switching Tests, 25°C (Subgroups 4, 9, Table I, 5005)		100%		100%
c) Functional Test, 25°C (Subgroup 7, Table I, 5005)		100%		100%

TABLE III. 100% Screening Requirements (Continued)

Screen	Class S		Class B	
	Method	Reqmt	Method	Reqmt
17. Seal Fine, Gross	1014	100%, (Note 8)	1014	100%, (Note 9)
18. Radiographic (Note 10)	2012 Two Views	100%		—
19. Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20. External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separate or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g. flatpacks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 19.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and Record when past burn-in delta measurements are specified.

Note 14: PDA shall apply to all static, dynamic, functional, and switching measurements at either 25°C or maximum rated operating temperature.

Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

Device Type	Mil * Class B	883 Class B	Desc	JAN
AH0014D	x			
AH0015D	x			
AH0019D	x			
LF111H	x			
LF11201D		x		
LF11202D		x		
LF11331D		x		
LF11332D		x		
LF11333D		x		
LF11508D	x			
LF11509D	x			
LF147D		x		
LF155AH		x		
LF155H		x		x
LF155J-8				x
LF155W				x
LF156AH		x		
LF156H		x		x
LF156J-8				x
LF156W				x
LF157AH		x		
LF157H		x		
LF198H		x		
LF411MH		x		x
LF411W				x
LF412MH		x		x
LF441MH	x			
LF442MH		x		
LF444MD		x		
LH0002H		x	x	
LH0003H	x			
LH0004H	x			
LH0020G	x			
LH0021K	x			
LH0022D	x			
LH0022H	x			
LH0023G	x			
LH0024H	x			

Device Type	Mil * Class B	883 Class B	Desc	JAN
LH0032G	x		x	
LH0033AG	x			
LH0033G	x		x	
LH0036G	x			
LH0038D	x			
LH0041G	x			
LH0042D	x			
LH0042H	x			
LH0043G	x			
LH0044AH	x			
LH0044H	x			
LH0052H	x			
LH0053G	x			
LH0061K	x			
LH0062D	x			
LH0062H	x			
LH0063K	x			
LH0070-0H	x			
LH0070-1H	x			
LH0070-2H	x			
LH0071-0H	x			
LH0071-1H	x			
LH0071-2H	x			
LH0075G	x			
LH0076G	x			
LH0082D	x			
LH0084D	x			
LH0086D	x			
LH0091D	x			
LH0094D	x			
LH00101AK	x			
LH0101K	x			
LH2101AD		x		
LH2108AD		x		
LH2108D		x		
LH2110D		x		
LH2111D		x		
LH2111F	x			

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

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Device Type	Mil * Class B	883 Class B	Desc	JAN
LH24250F	x			
LM10H		x		
LM101AH		x		x
LM101AJ-14		x		x
LM101AJ		x		
LM101AW				x
LM102H		x		
LM103H-3.0		x	x	
LM103H-3.3		x	x	
LM103H-3.6		x	x	
LM103H-3.9		x	x	
LM104H		x		
LM105H		x		
LM106H		x		
LM107H		x		
LM107J-14		x		
LM107J		x		
LM108AH		x		x
LM108AJ-8		x		x
LM108AJ		x		
LM108AW				x
LM108H		x		
LM108J-8		x		
LM108J		x		
LM109H		x		
LM109KSTEEL		x		
LM11H		x		
LM110H		x		
LM110J-8		x		
LM110J		x		
LM111H		x		x
LM111J		x		x
LM111W				x
LM112H		x		
LM113-1H		x	x	
LM113-2H		x	x	
LM113H		x	x	
LM117H		x	x	x

Device Type	Mil * Class B	883 Class B	Desc	JAN
LM117HVH		x	x	
LM117HVKSTL		x	x	
LM117KSTEEL		x	x	x
LM118H		x		x
LM118J-8		x		x
LM118J		x		
LM118W				x
LM119H		x	x	
LM119J		x	x	
LM120H-12		x		
LM120H-15		x		
LM120H-5.0		x		
LM120K-12		x		
LM120K-15		x		
LM120K-5.0		x		
LM121AH		x		
LM121H		x		
LM122H		x		
LM123KSTEEL		x		
LM124AJ		x		
LM124J		x		x
LM125H		x		
LM126H		x		
LM129AH		x		
LM129BH		x		
LM131AH		x		
LM131H		x		
LM135H		x		
LM136AH-2.5		x	x	
LM136H-2.5		x		
LM136H-5.0		x		
LM137H		x	x	
LM137HVH		x	x	
LM137HVKSTEEL		x	x	
LM137KSTEEL		x	x	
LM138KSTEEL		x		
LM139AJ		x		
LM139J		x		x

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

Military Analog Products Available From National Semiconductor

Listed below are the military class B Analog devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

Device Type	Mil * Class B	883 Class B	Desc	JAN
LM139W				x
LM140AK-12		x		
LM140AK-15		x		
LM140AK-5.0		x		
LM140K-12		x		
LM140K-15		x		
LM140K-5.0		x		
LM140LAH-12		x		
LM140LAH-15		x		
LM140LAH-5.0		x		
LM143H		x	x	
LM144H		x	x	
LM145K-5.0		x		
LM145K-5.2		x		
LM146J		x		
LM148J		x		x
LM149J		x		
LM150KSTEEL	x			
LM1536H		x	x	
LM1558H		x		
LM1558J		x		
LM158AH		x		
LM158AJ		x		
LM158H		x		
LM158J		x		
LM1596H	x			
LM160H		x		
LM160J-14		x		
LM160J		x		
LM161F	x			
LM161H		x		
LM161J		x		
LM185BXH-1.2		x		
LM185BYH-1.2		x		

Device Type	Mil * Class B	883 Class B	Desc	JAN
LM185H-1.2		x		
LM193AH		x		
LM193H		x		x
LM193J-8				x
LM193W				x
LM194H		x		
LM195H		x		
LM195K		x		
LM199AH-20		x		
LM199AH		x		
LM199H		x		
LM4250H	x			
LM4250J	x			
LM555H		x		
LM555J		x		
LM556J	x			
LM567H		x		
LM709AH		x		
LM709H		x		
LM710H		x		
LM723H		x		
LM723J				x
LM725H		x		
LM733H	x			
LM741AJ-14		x		
LM741AJ		x		
LM741H		x		x
LM7415-14		x		
LM741J		x		x
LM741W				x
LM747H		x		x
LM747J		x		
LM748H		x		
LM748J		x		

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

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Appendix E
Understanding Integrated Circuit Package Power Capabilities

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

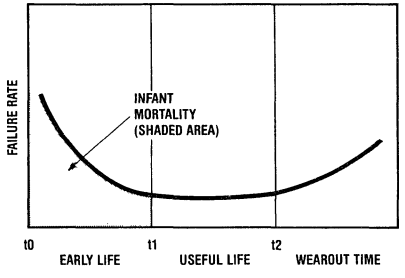

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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

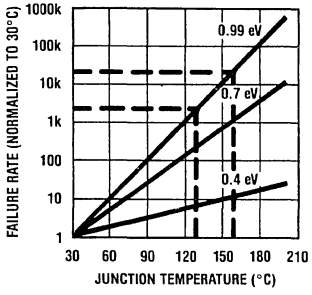

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

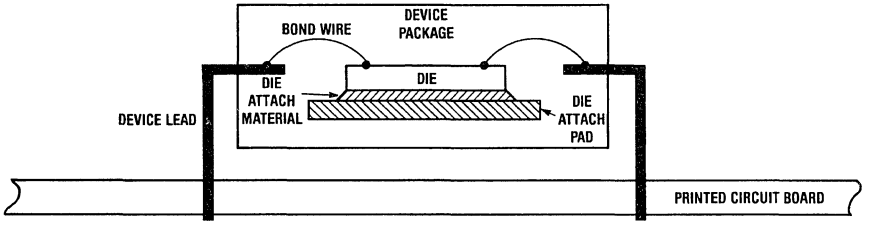

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

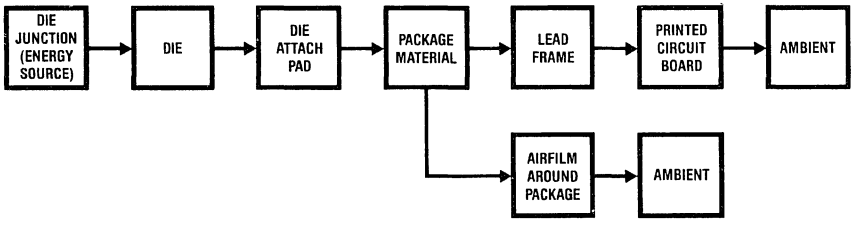

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

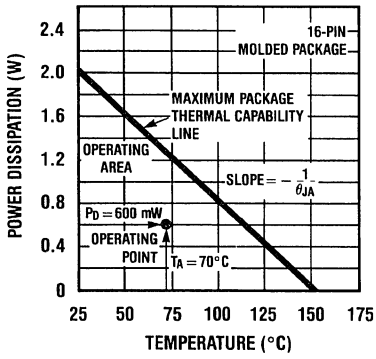

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

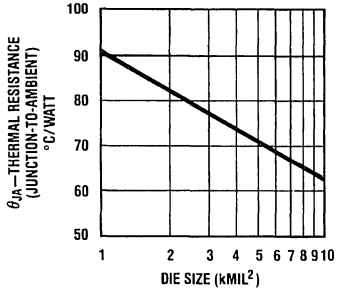

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

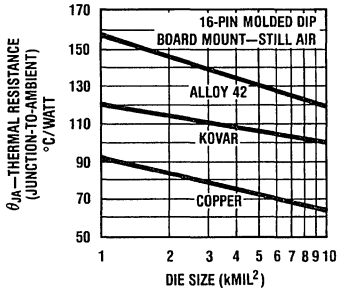

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

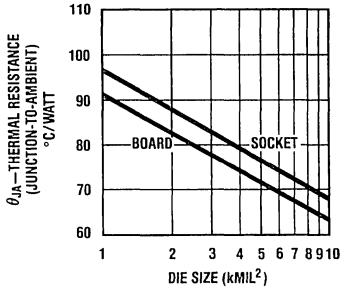

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

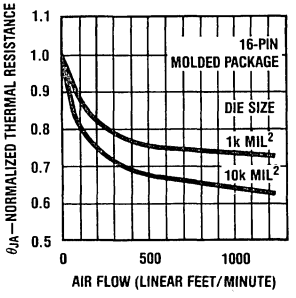

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

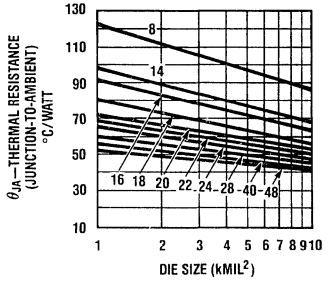
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D @ 70°C = 1476\ mW - (11.8\ mW/°C) \times (70°C - 25°C)$$
$$= 945\ mW$$

Molded (N Package) DIP*
Copper Leadframe—HTP
Die Attach Board Mount—
Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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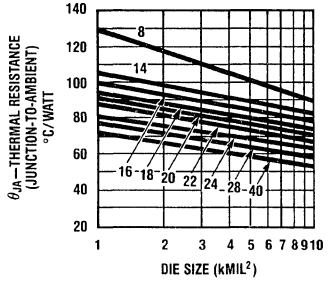
FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Cavity (J Package) DIP*
Poly Die Attach Board
Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

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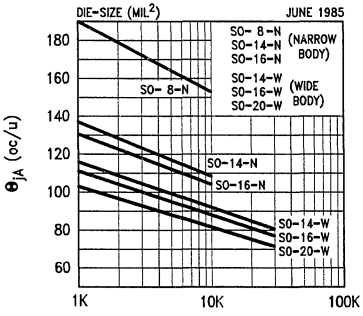
FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)



θ_{jA} – THERMAL RESISTANCE FOR "SO" PACKAGES (BOARD MOUNT)

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FIGURE 12

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APPENDIX F
How to Get the Right Information From a Data Sheet

Not All Data Sheets Are Created Alike, and False Assumptions Could Cost an Engineer Time and Money

By Robert A. Pease

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

The data sheet can show the prospective user how to apply the device, what performance specifications are guaranteed and various typical applications and characteristics. If the data-sheet writer has done a good job, the user can decide if the product will be valuable to him, exactly how well it will be of use to him and what precautions to take to avoid problems.

SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

But, if there are significant changes and improvements that nobody has seen before, then the writer must clarify what is meant by each specification. Definitions of new phrases or characteristics may even have to be added as an appendix.

For example, when fast-settling operational amplifiers were first introduced, some manufacturers defined settling time as the time after slewing before the output finally enters and stays within the error-band; but other manufacturers included the slewing time in their definition. Because both groups made their definitions clear, the user was unlikely to be confused or misled.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsmanship game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

GUARANTEES

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

For instance, in the early days of op amps (20 years ago), the differential-input impedance might have been guaranteed at 1 MΩ—but the manufacturer obviously did not measure the impedance. When a customer insisted, "I have to know how you measure this impedance," it had to be explained that the impedance was not measured, but that the base current was. The correlation between I_b and Z_{in} permitted the substitution of this simple dc test for a rather messy, noisy, hard-to-interpret test.

Every year, for the last 20 years, manufacturers have been trying to explain, with varying success, why they do not measure the Z_{in} *per se,* even though they do guarantee it.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- The tested limit represents a test that cannot be doubted, one that is actually performed directly on 100 percent of the devices, 100 percent of the time.
- The design limit covers other tests that may be indirect, implicit or simply guaranteed by the inherent design of the device, and is unlikely to cause a failure rate (on that test), even as high as one part per thousand.

Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

Some data sheets guarantee characteristics that are quite expensive and difficult to test (even harder than noise) such as long-term drift (20 ppm or 50 ppm over 1,000 hours).

The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

TYPICALS

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

It might mean that the manufacturer once actually saw one part as good as that. It could indicate that half the parts are better than that specification, and half will be worse. But it is equally likely to mean that, five years ago, half the parts were better and half worse. It could easily signify that a few parts might be slightly better, and a few parts a lot worse; after all, if the noise of an amplifier is extremely close to the theoretical limit, one cannot expect to find anything much better than that, but there will always be a few noisy ones.

If the specification of interest happens to be the bias current (I_b) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where I_b is 40 nA on one batch (where the beta is high), and a month later, many parts where the I_b is 140 nA when the beta is low.

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Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temperature,	
TO-46 Package	−76°F to +356°F
TO-92 Package	−76°F to +300°F
Lead Temp. (Soldering, 4 seconds) *	
TO-46 Package	+300°C
TO-92 Package	+260°C
Specified Operating Temp. Range (Note 2)	
	T_{MIN} to T_{MAX}
LM34, LM34A	−50°F to +300°F
LM34C, LM34CA	−40°F to +230°F
LM34D	+32°F to +212°F

DC Electrical Characteristics (Note 1, **Note 6**)

Parameter	Conditions	LM34A			LM34CA			Units (Max)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		°F
	T_A = 0°F	±0.6			±0.6		±2.0	°F
	T_A = T_{MAX}	±0.8	±2.0		±0.8	±2.0		°F
	T_A = T_{MIN}	±0.8	±2.0		±0.8		±3.0	°F
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**±0.35**		**±0.7**	**±0.30**		**±0.6**	°F
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°F, min mV/°F, max
Load Regulation (Note 3)	T_A = +77°F	±0.4	±1.0		±0.4	±1.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
	$0 \le I_L \le 1$ mA							
Line Regulation (Note 3)	T_A = +77°F	±0.01	±0.05		±0.01	±0.05		mV/V
	$5V \le V_S \le 30V$	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	V_S = +5V, +77°F	75	90		75	90		µA
	V_S = +5V	**131**		**160**	**116**		**139**	µA
	V_S = +30V, +77°F	76	92		76	92		µA
	V_S = +30V	**132**		**163**	**117**		**142**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V$, +77°F	+0.5	2.0		0.5	2.0		µA
	$5V \le V_S \le 30V$	**+1.0**		**3.0**	**1.0**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.30**		**+0.5**	**+0.30**		**+0.5**	µA/°F
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L = 0	+3.0		+5.0	+3.0		+5.0	°F
Long-Term Stability	T_j = T_{MAX} for 1000 hours	±0.16			±0.16			°F

Note 1: Unless otherwise noted, these specifications apply: $-50°F \le T_j \le +300°F$ for the LM34 and LM34A; $-40°F \le T_j \le +230°F$ for the LM34C and LM34CA; and $+32°F \le T_j \le +212°F$ for the LM34D. V_S = +5 Vdc and I_{LOAD} = 50 µA in the circuit of *Figure 2;* +6 Vdc for LM34 and LM34A for $230°F \le T_j \le 300°F$. These specifications also apply from +5°F to T_{MAX} in the circuit of *Figure 1.*

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1.*

Note 10: Contact factory for availability of LM34CAZ.

** **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family:

"Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

ORIGINS OF DATA SHEETS

Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

Even today, an attempt is made to build on the good things learned from the past and add a few improvements when necessary. But, it's important to have real improvements, not just change for the sake of change.

So, while it's not easy to get the format and everything in it exactly right to please everybody, new data sheets are continually surfacing with new features, applications ideas, specifications and aids for the user. And, if the users complain loudly enough about misleading or inadequate data sheets, they can help lead the way to change data sheets. That's how many of today's improvements came about—through customer demand.

Who writes data sheets? In some cases, a marketing person does the actual writing and engineers do the checking. In other companies, the engineer writes, while marketing people and other engineers check. Sometimes, a committee seems to be doing the writing. None of these ways is necessarily wrong.

For example, one approach might be: The original designer of the product writes the data sheet (inside his head) at the same time the product is designed. The concept here is, if one can't find the proper ingredients for a data sheet—good applications, convenient features for the user and nicely tested specifications as the part is being designed—then maybe it's not a very good product until all those ingredients are completed. Thus, the collection of raw materials for a good data sheet is an integral part of the design of a product. The actual assembly of these materials is an art which can take place later.

WHEN TO WRITE DATA SHEETS

A new product becomes available. The applications engineers start evaluating their application circuits and the test engineers examine their production test equipment.

But how can the users evaluate the new device? They have to have a data sheet—which is still in the process of being written. Every week, as the data sheet writer tries to polish and refine the incipient data sheet, other engineers are reporting, "These spec limits and conditions have to be revised," and, "Those application circuits don't work like we thought they would; we'll have one running in a couple of days." The marketing people insist that the data sheet must be finalized and frozen right away so that they can start printing copies to go out with evaluation samples.

These trying conditions may explain why data sheets always seem to have been thrown together under panic conditions and why they have so many rough spots. Users should be aware of the conflicting requirements: Getting a data sheet "as completely as possible" and "as accurately as possible" is compromised if one wants to get the data sheet "as quickly as possible."

The reader should always question the manufacturer. What are the alternatives? By not asking the right question, a misunderstanding could arise; getting angry with the manufacturer is not to anyone's advantage.

Robert Pease has been staff scientist at National Semiconductor Corp., Santa Clara, Calif., for eleven years. He has designed numerous op amps, data converters, voltage regulators and analog-circuit functions.

National Semiconductor Corporation

Appendix G
Obsolete Product Replacement Guide

Some device types, individual temperature grades and package options have been discontinued. This guide is provided to help design engineers select and specify an appropriate alternative.

NSC Part Number	Replacement	Note
ADB1200	ADC3711	2
DAC1200/1201	DAC1265	2
LF352	LM3631	2
LF13300	ADC3711	2
LH0001	LM4250	2
LH0005/LH0005A	LH0003	2
LH0037	LH0036	3
LH0132	LH0032	2
LH2011	LM11	2
LH2108	LM108	2
LH2201A	LM201A	2
LH2208	LM208	2
LH2208A	LM208A	2
LH2308	LM308	2
LH24250	LM11	2
LM170/270/370	LM13600N	2
LM171/271/371	no replacement	
LM172/272/372	no replacement	
LM173/273/373	no replacement	
LM174/274/374	no replacement	
LM175/275/375	no replacement	
LM216/316	LM11	2
LM388N-2/N-3	LM388N-1	2
LM377N	LM2877P	3
LM378N	LM2878P	3
LM379	LM2879T	3
LM1014	no replacement	
LM1017	no replacement	
LM1019	no replacement	

NSC Part Number	Replacement	Note
LM1821S	LM1823	2
LM1822	LM1823	3
LM1828	no replacement	
LM1848	no replacement	
LM1877N-1/N-2/N-3	LM1877N-9	2
LM2003	no replacement	
LM2808	no replacement	
LM2831	LM1851	2
LM3011	no replacement	
LM3064	no replacement	
LM3075	no replacement	
TBA120V	no replacement	
TBA440C	LM1823	2
TBA510	no replacement	
TBA530	no replacement	
TBA540	no replacement	
TBA560C	no replacement	
TBA920	no replacement	
TBA950-2	no replacement	
TBA970	no replacement	
TBA990	no replacement	
TDA440	no replacement	
TDA2522/23	no replacement	
TDA2530	no replacement	
TDA2530/31	no replacement	
TDA2540/41	no replacement	
TDA2560	no replacement	
TDA2590	no replacement	
TDA3500	no replacement	

Note 1: IMPROVED REPLACEMENT: Pin for Pin replacement with superior electrical specifications.

Note 2: FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

Note 3: SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

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Appendix H
Products Not Recommended for New Designs

The popular National Semiconductor Corporation monolithic IC's may have been designed into your systems. We believe that there are more cost-effective circuits manufactured by National Semiconductor Corporation that should be considered in your new designs. These recommendations are listed in this section. To eliminate the necessity to redesign proven equipment, we are continuing to make these products for use in existing designs for which they were uniquely suitable.

NSC Part Number	Recommended Replacement	Note
AF100	LMF100	3
AF150	LMF100	3
AF151	LMF100	3
AH0014	LMC13421/LMC13422	3
AH0015	LMC13421/LMC13422	3
AH0019	LMC13421/LMC13422	3
LH0023	LF198/LF298	2
LH2101A	LM101A	2
LH2108A	LM108A	2
LH2110	LM110	2
LH2111	LM111	2
LH2210	LM210	2
LH2211	LM211	2
LH2301A	LM301A	2
LH2308A	LM308A	2
LH2310	LM310	2
LH2311	LM311	2
LM103	LM185	3
LM113	LM1851-2	1
LM313	LM3851-2	1
LM377N	LM1877N-9	2
LM377N	LM2877P	3
LM378N	LM2878P	3
LM391N-60	LM391N-100	1
LM391N-80	LM391N-100	1
LM709	LF441	3
LM710	LM106	2
LM725	LM607	3
LM748	LF441	3

Notes:

Note 1: IMPROVED REPLACEMENT: Pin for Pin replacement with superior electrical specifications.

Note 2: FUNCTIONAL REPLACEMENT: Consult datasheet to determine suitability of the replacement for specific application.

Note 3: SIMILAR DEVICE with superior performance: Consult datasheet to determine suitability of the replacement for specific application.

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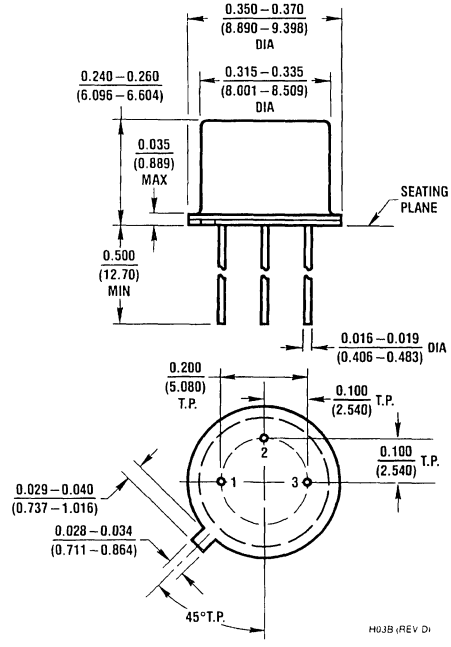
All dimensions are in inches (millimeters)



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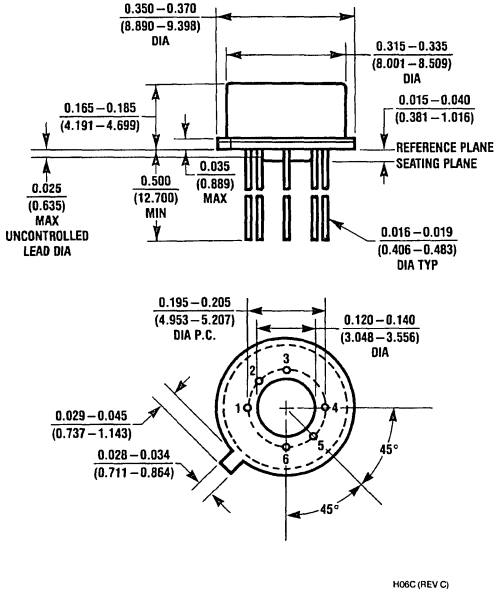

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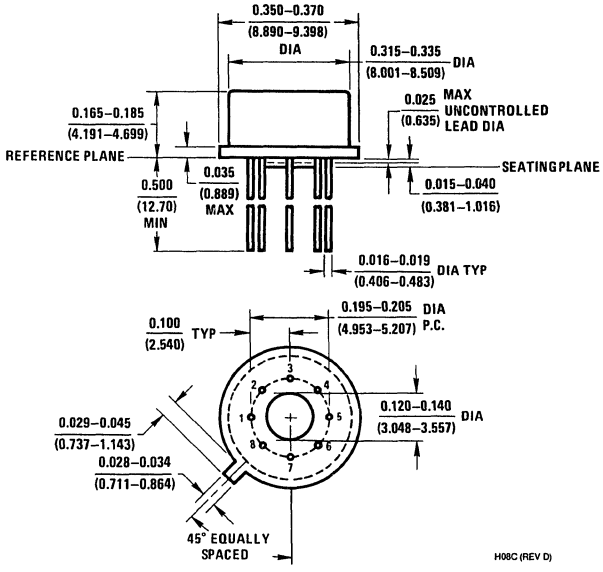

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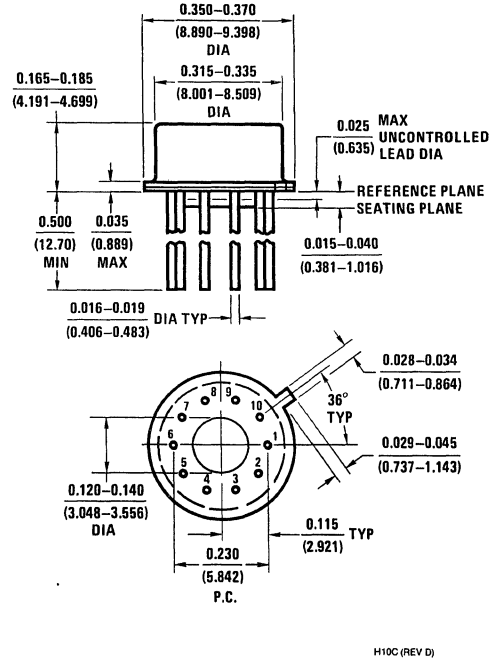

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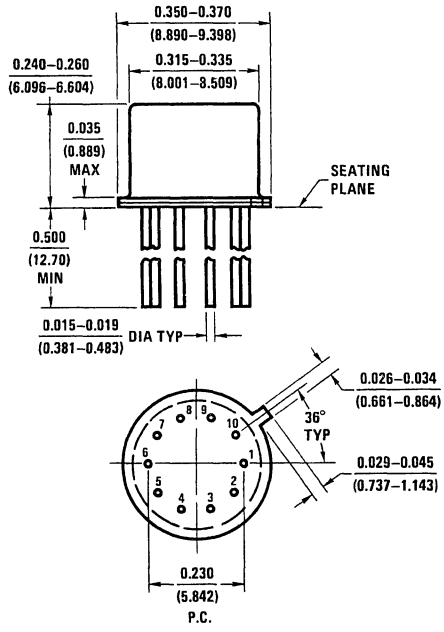

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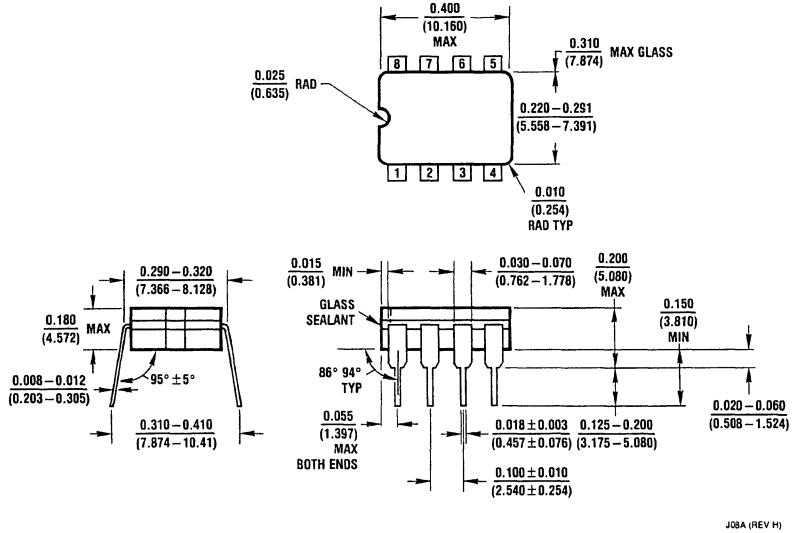

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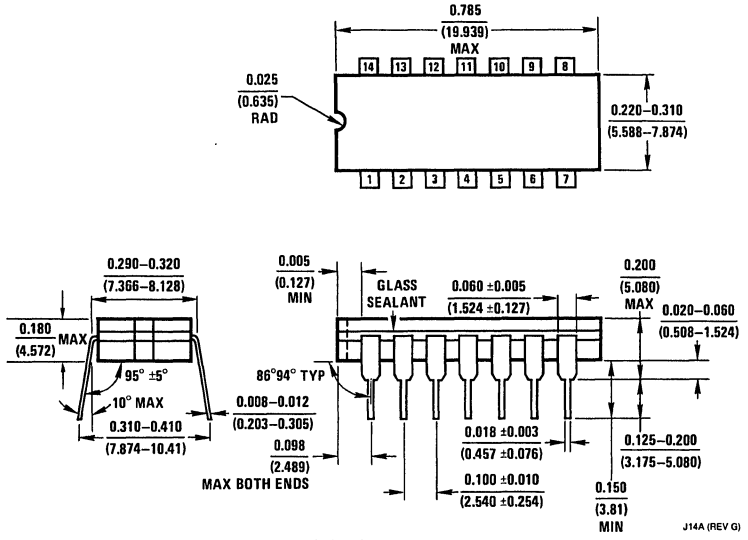

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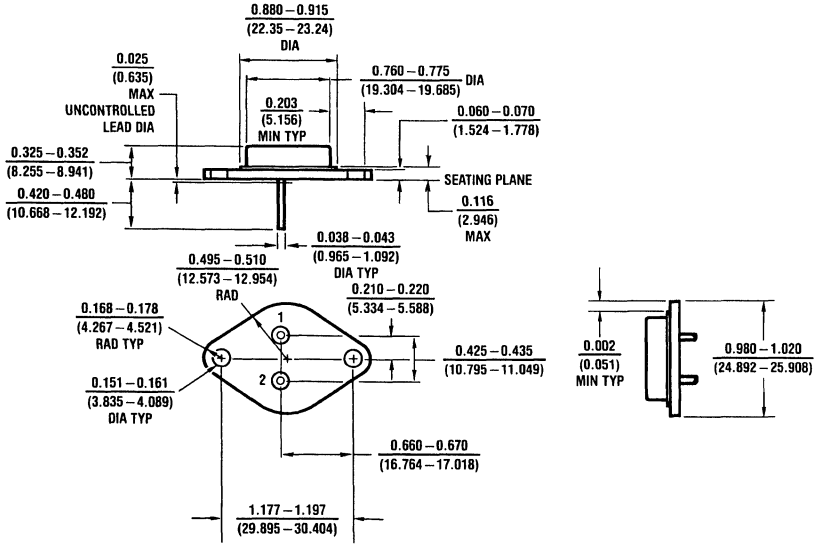

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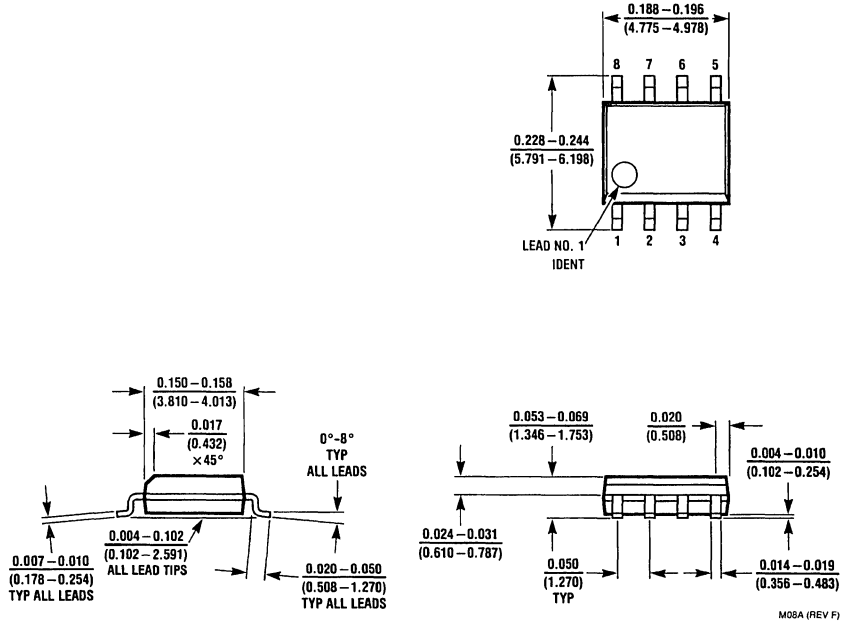

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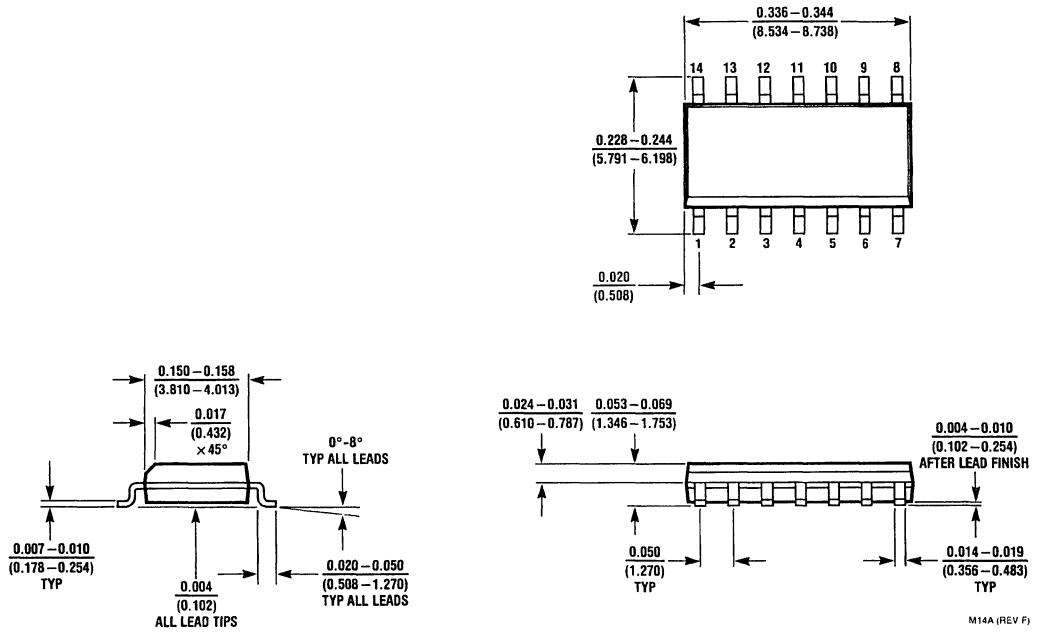

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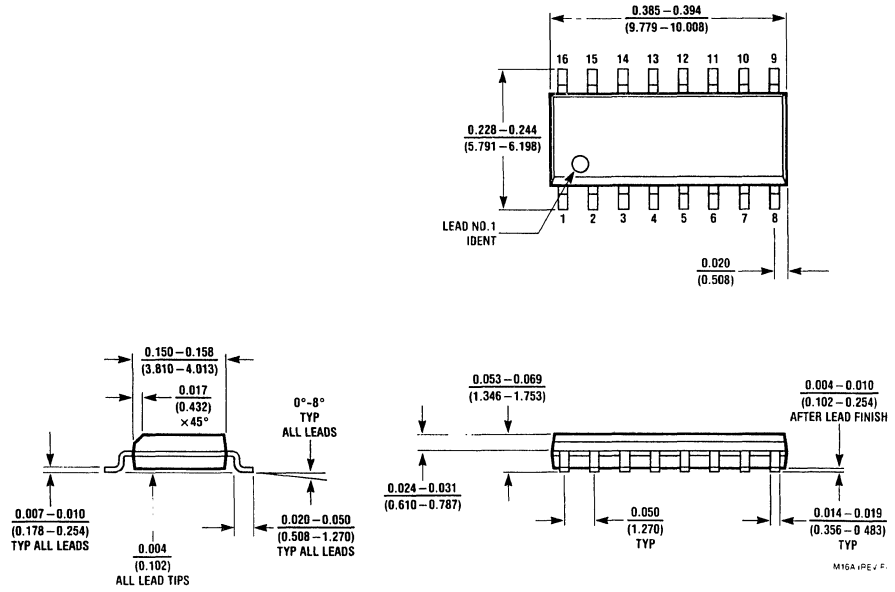

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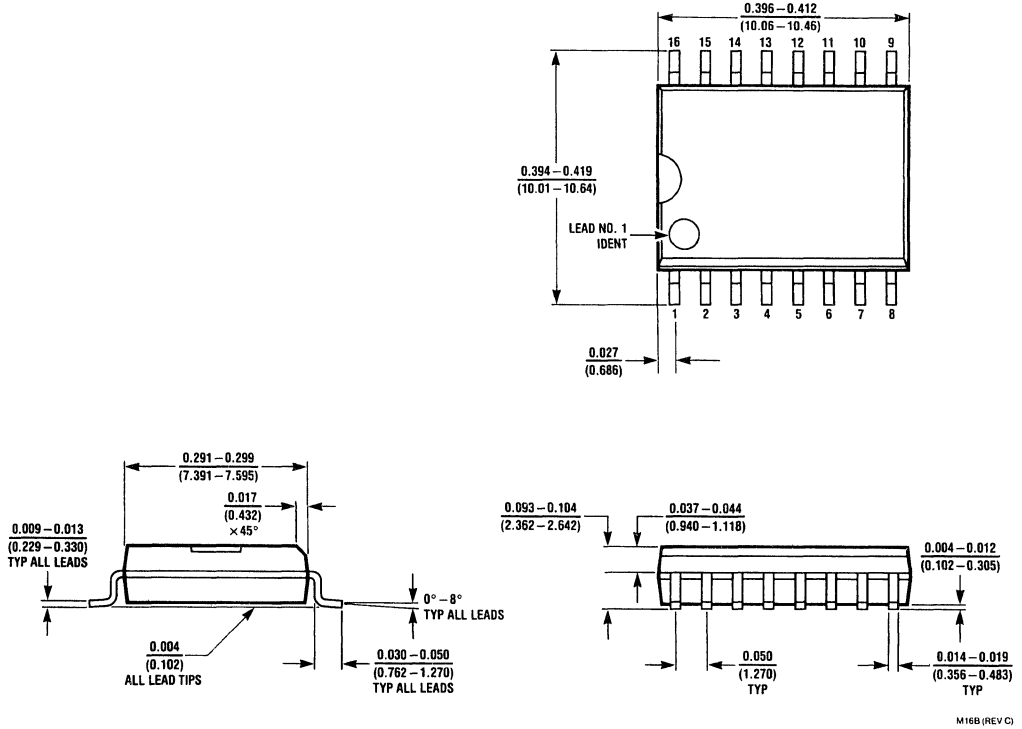

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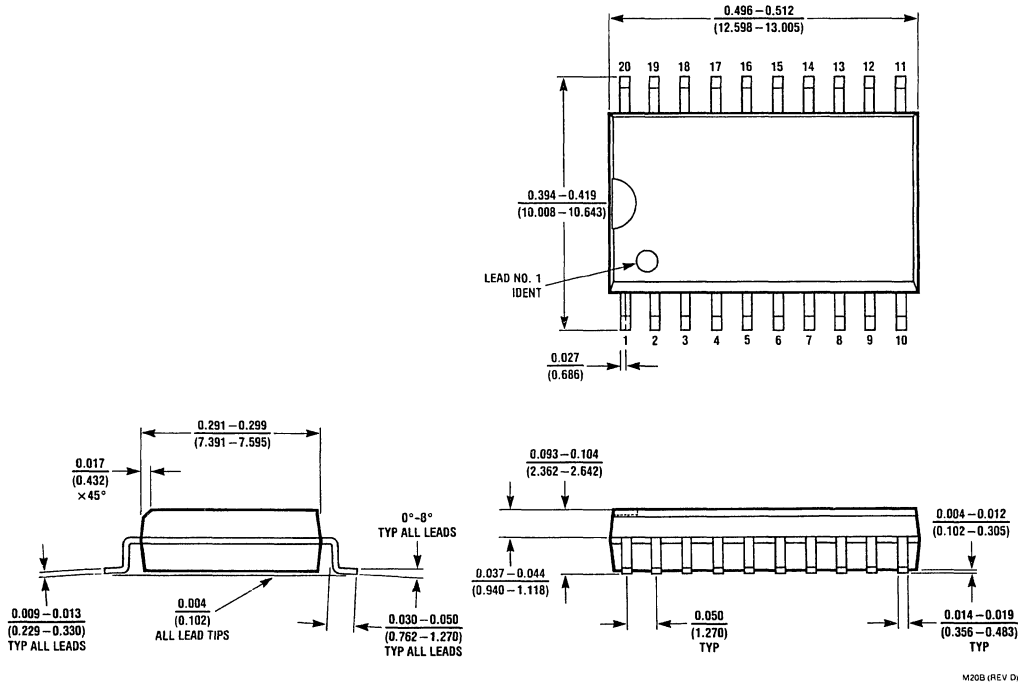

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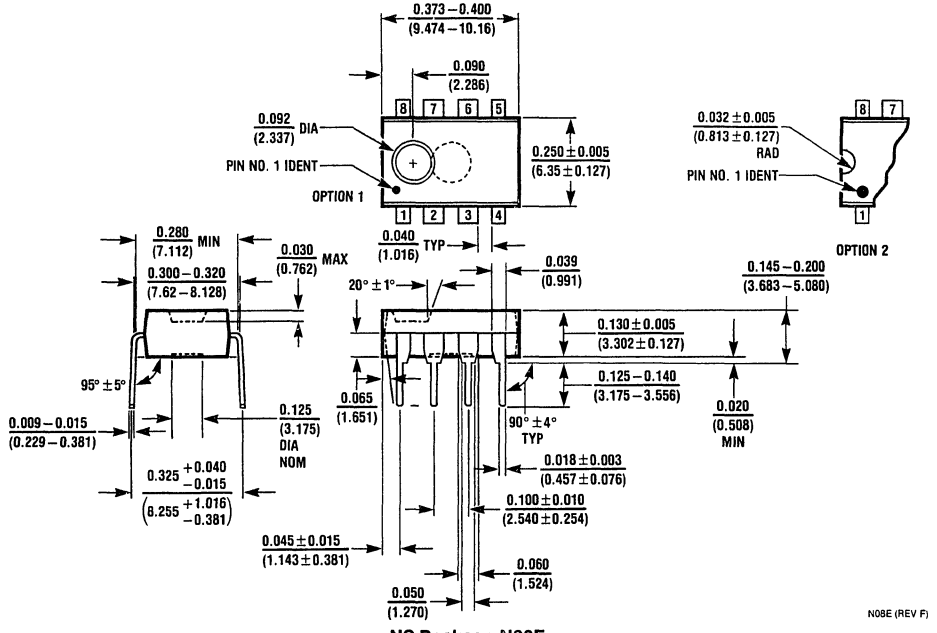

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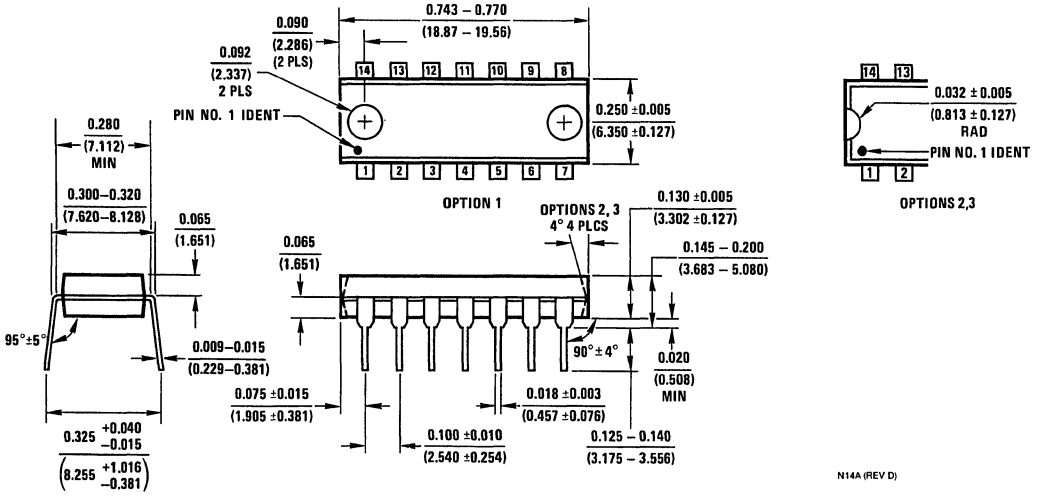

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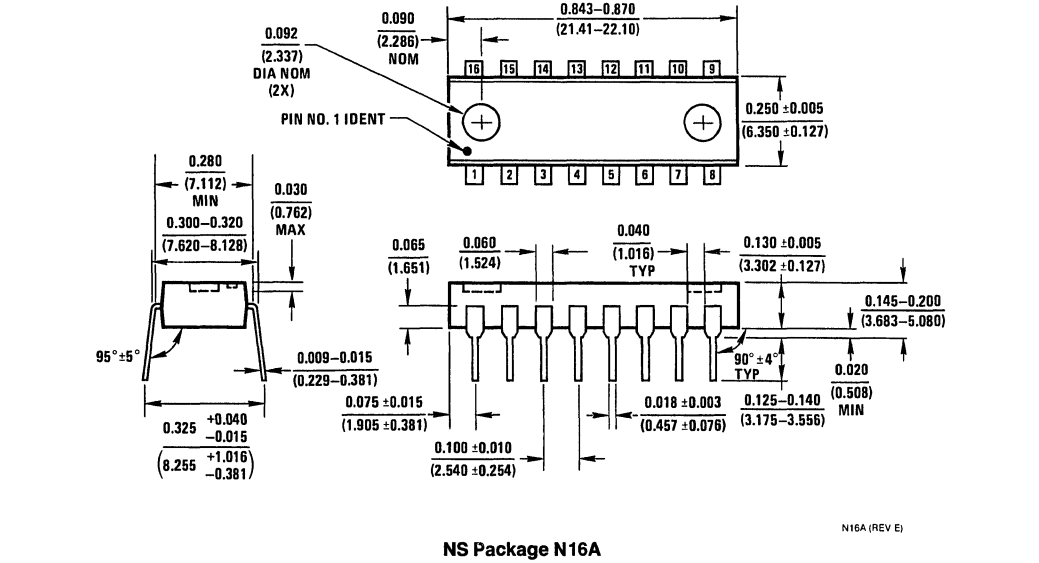

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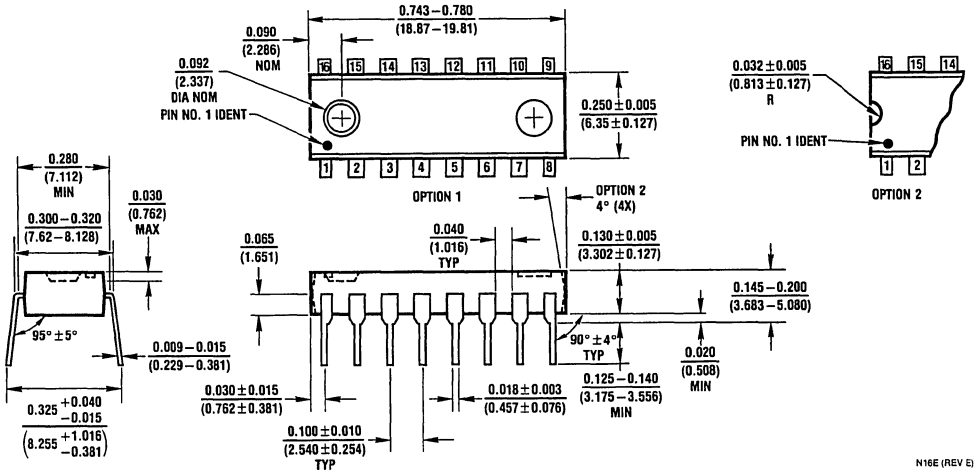

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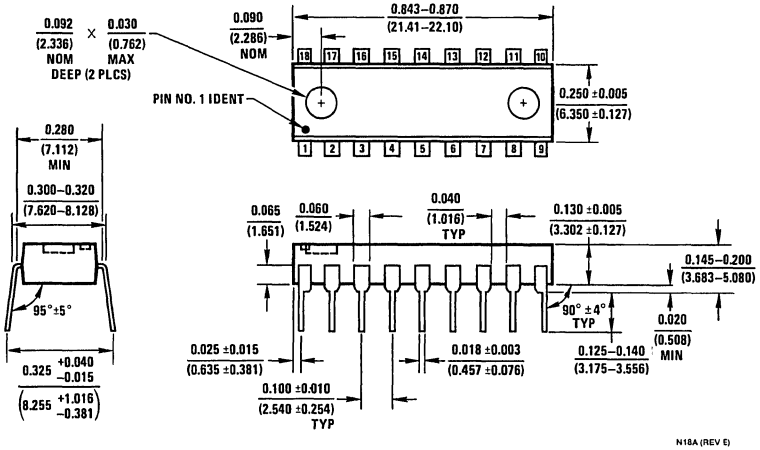

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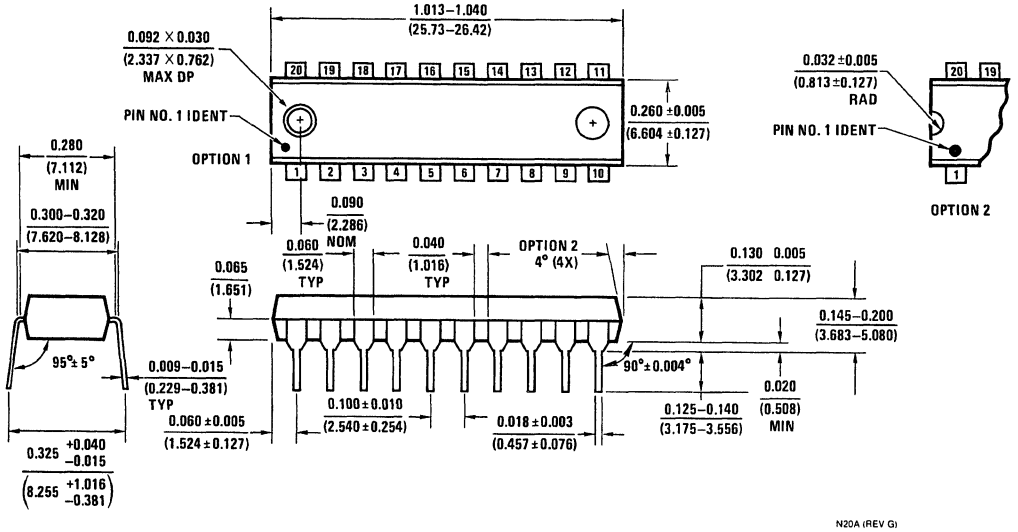

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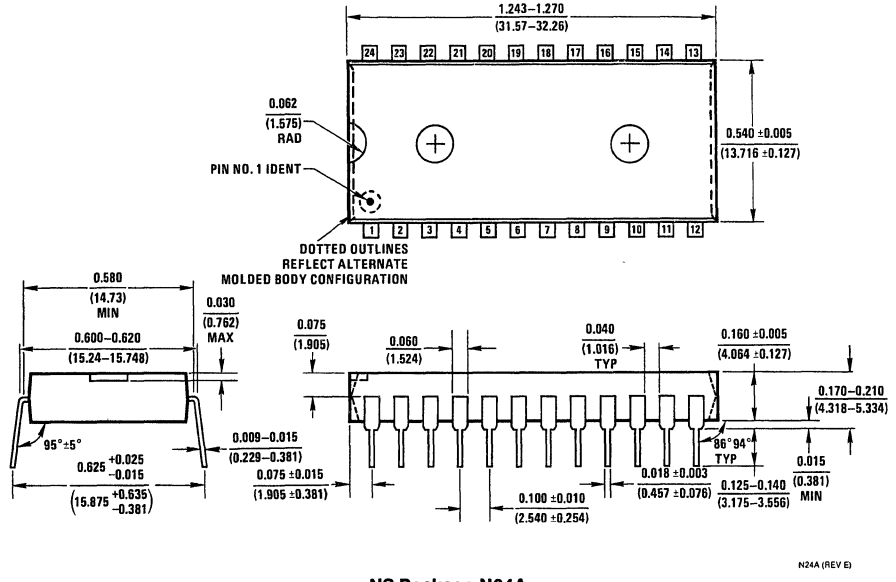

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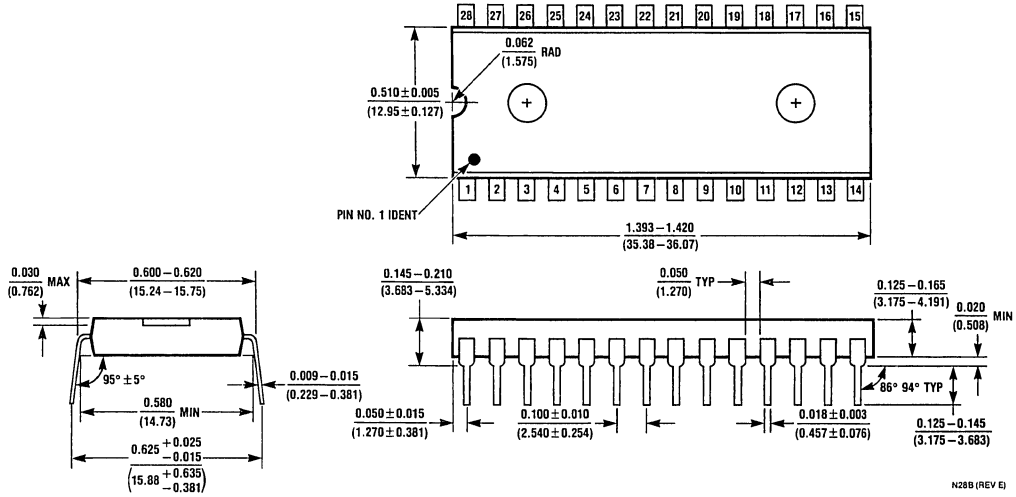

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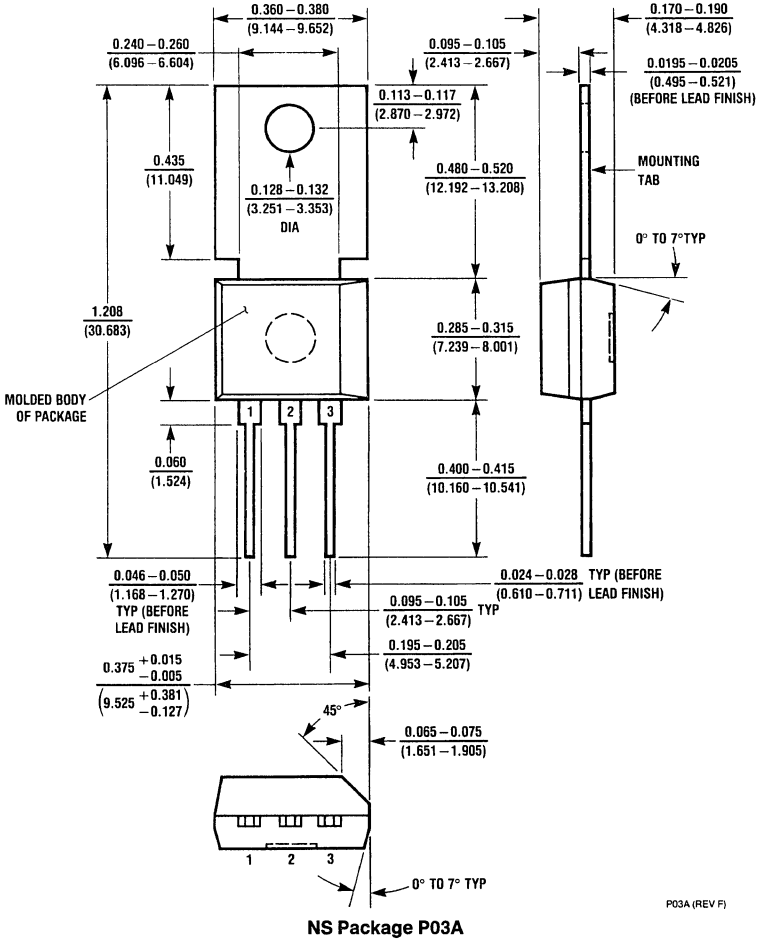

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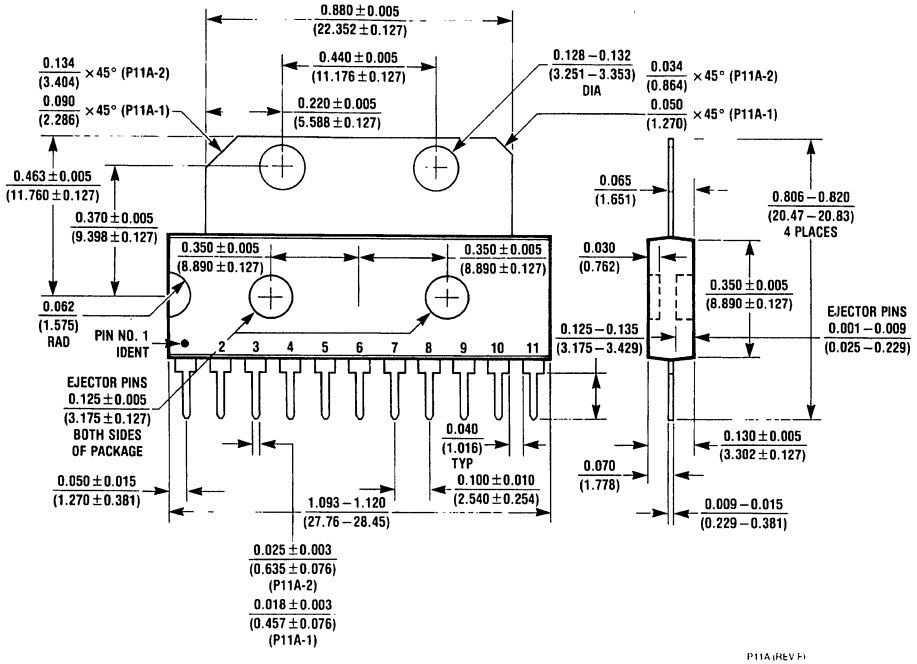

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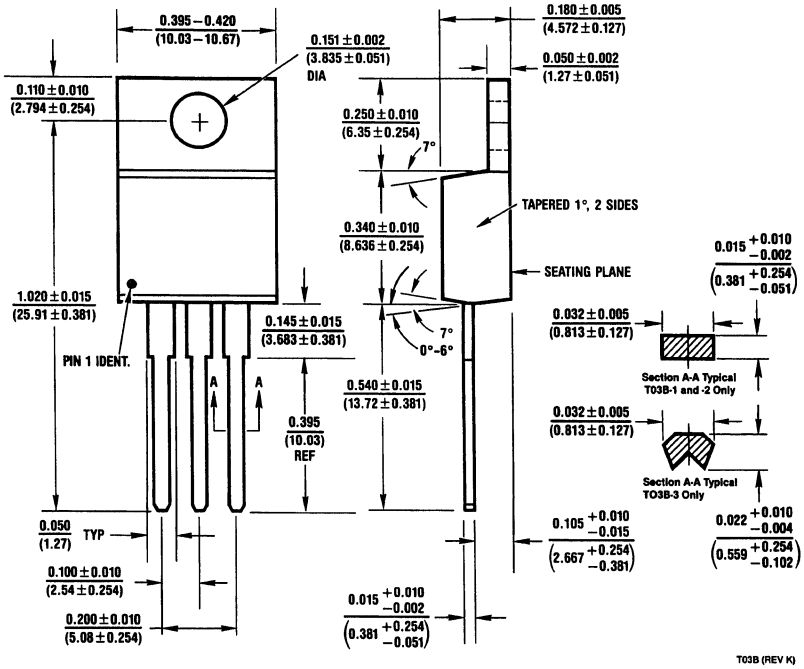

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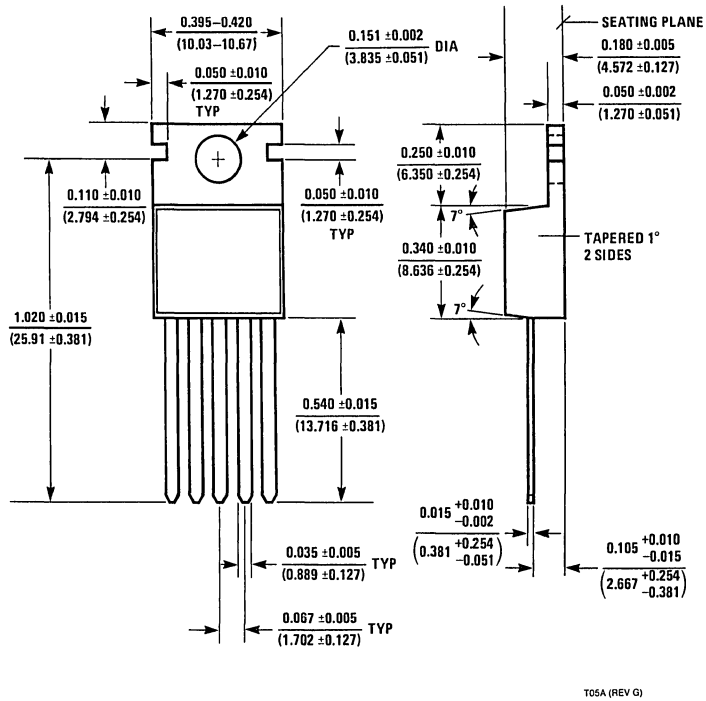

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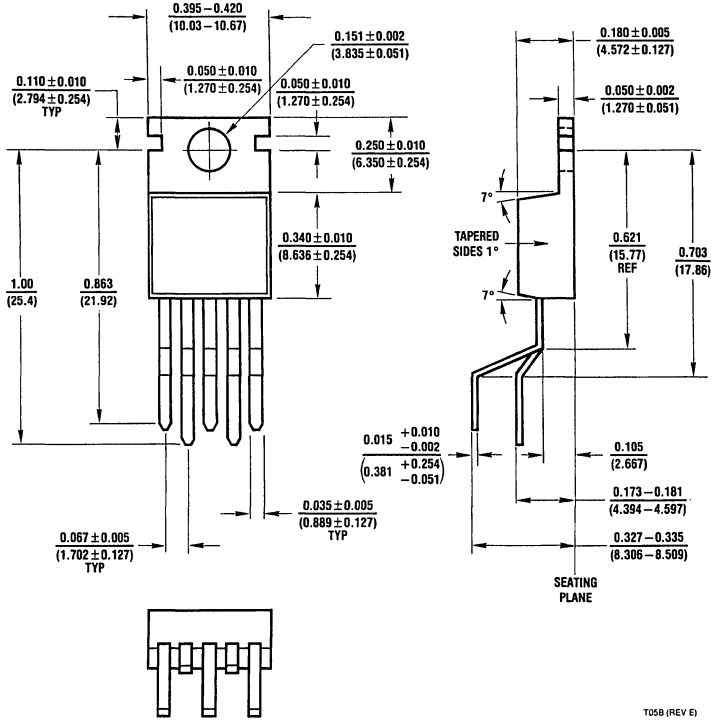

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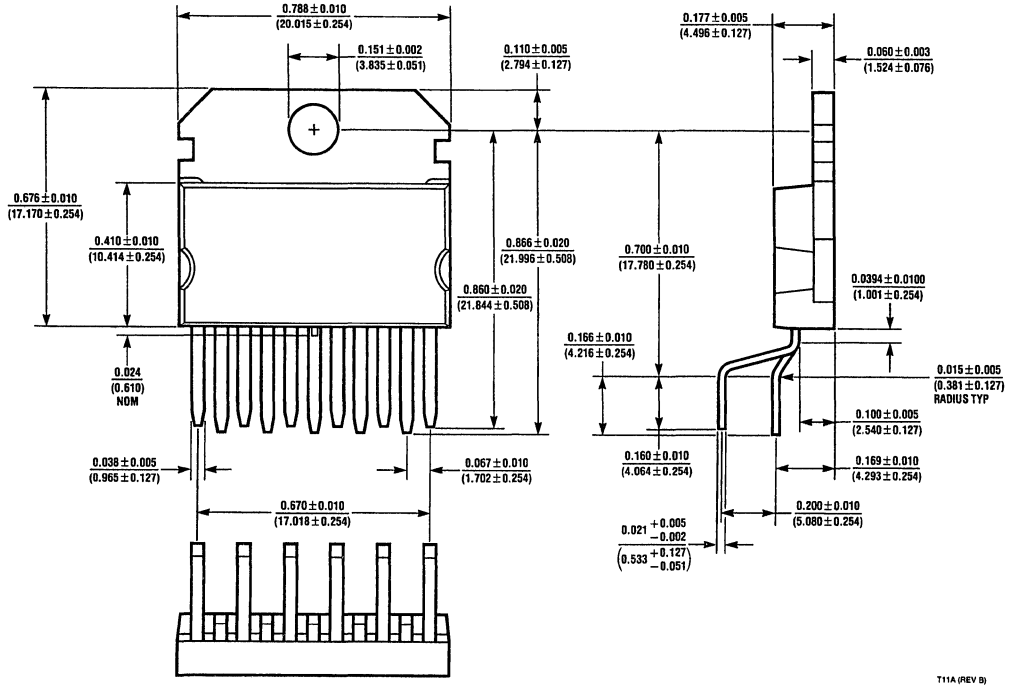

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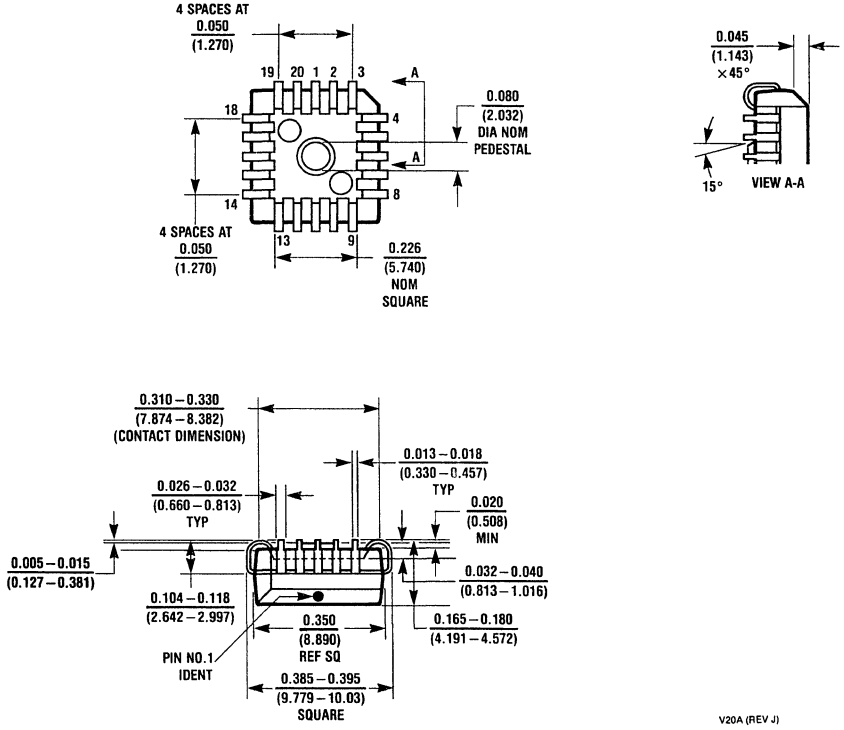

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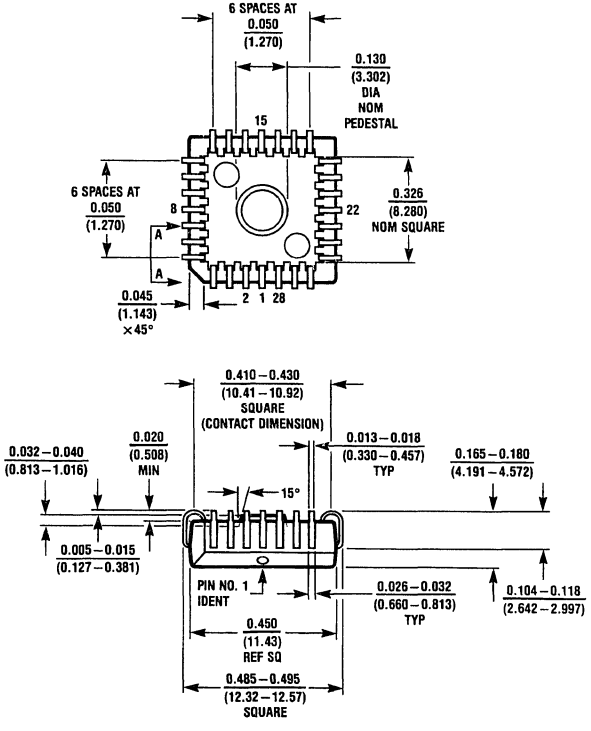

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