570025 Rev. 1

National Semiconductor Corporation

Telecommunications Databook

- *Line Card Components*
- *ISDN*
- *Modems*
- *Analog Telephone*

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TELECOMMUNICATIONS
DATABOOK

1987 Edition

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Introduction

To coincide with the advent of the Integrated Services Digital Network (ISDN), this new 1987 Telecommunications Data Book clearly portrays the continuing evolution of the Telecommunications Network and the Integrated Circuit technology required to support it. Previous editions focused heavily on analog telephones and analog line card components for digital switching. This catalog shows components supporting the emerging of a fully digital network, which upon implementation will give all of us greater world wide communications capability and flexibility than ever imagined.

The Integrated Circuits required for modern day telecommunications technology and presented within this data book are no longer simple functions but are complete systems in themselves. Their functionality and parametric performance is at levels never before achieved, and they utilize the most advanced silicon process technology available today. In response to the system designer's tasks and dilemma, this data book contains a complete product listing and data sheets for all "dedicated" telecommunications components, both present and future.

Shipping over 5 million subscriber or trunk lines per year, National Semiconductor is an industry leader in the field of telecommunications specific Integrated Circuit functions. Starting in 1977 with the introduction of the world's first commercially available integrated Codec, the TP3000, then evolving it into the worlds' first industry standard single chip codec/filter COMBO™ TP3054/57. In 1986 the announcement of the TP3070 COMBO II™ proved Nationals' ability to continue to provide high performance and cost effective state of the art solutions. Other Line Card component developments such as the parallel COMBO, Magnetic Compensation SLIC MC, Time Slot Assigner Circuit (TSAC), and now ISDN are clear signs of Nationals' dedication and long term committment to the market.

National Semiconductor will continue to monitor the evolving applications requirements in the telecommunications industry and will drive new IC designs which provide additional features and further improve cost effectiveness. Systems designers utilizing telecommunications Integrated Circuits from National Semiconductor should be confident they can design both now and in the future with the most advanced technology available, and have further assurances of success by designing in products supplied by the company which has the highest quality and reliability standards in the world.

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*Devices not covered in last publication.

Section 1

Line Card Components

Section 1 Contents

*Devices not covered in last publication

National Semiconductor Corporation

PRELIMINARY

TP3200/TP3202/TP3204 SLIC-MC Magnetic Compensation SLICs

General Description

The TP3200, TP3202 and TP3204 are monolithic Bipolar integrated circuits intended for use on subscriber and trunk interface cards of digital PABX and central office equipment. Each device contains a magnetic compensation circuit, a supervision circuit and three relay drivers with latched inputs.

The magnetic compensation circuit allows the use of a small, low cost line transformer by measuring the loop current, and producing an output current proportional to the d.c. value of the loop current. This output current is passed through a winding of the line transformer in such a way as to cancel the d.c. component of the magnetic flux. Thus the transformer may be wound on a small ferrite core without an air gap.

The supervision output is used to detect off-hook, replicate dial pulses and terminate ringing on detection of ring-trip.

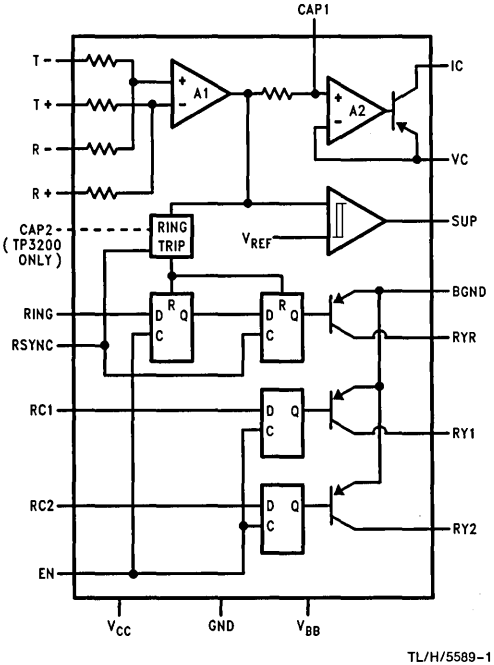
One of the three relay drivers is dedicated to the ring function, the other two are general purpose. TP3200 and TP3202 have PNP relay drivers, while TP3204 has NPN relay drivers.

Features

- Magnetic Compensation Circuit allows the use of low cost ferrite core transformers
- Supervision Circuitry provides hook-switch detect, ring-trip detect and dial pulse replication
- Ring relay driver synchronized to zero-crossings
- Automatic ring-trip circuit—TP3200, TP3204
- Three Latched relay drivers
- −48 Volt relay drivers—TP 3200, TP3202
- +5 Volt relay drivers—TP 3204
- Requires only ±5V supplies
- Thermal shutdown protection
- Power-Up reset on relay driver latches

Simplified Block Diagrams

TP3200 and TP3202



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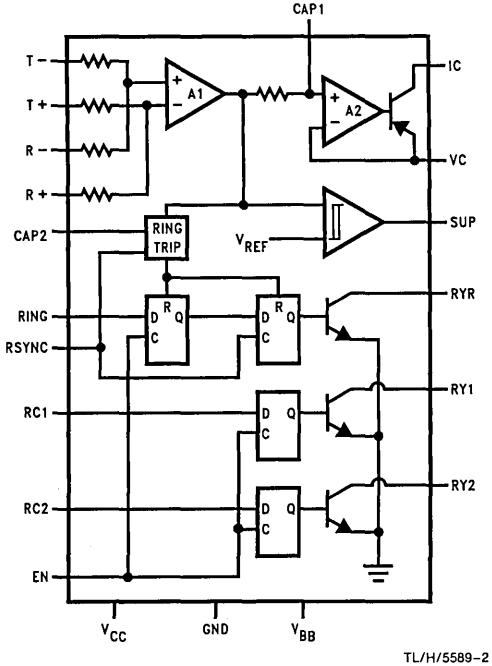
TP3204



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
V_{CC} w.r.t. GND	7V
V_{BB} w.r.t. GND	−7V
V_{CC} w.r.t. V_{BB}	14V
V_{IC} w.r.t. GND	−70V
V_{RY} w.r.t. GND (TP3200, TP3202)	−70V
V_{RY} w.r.t. GND (TP3204)	20V
Voltage at Sensing Inputs T+, T−, R+, R−, w.r.t. GND	300 V_{peak} (continuous)
I_{RY} (TP3200, TP3202)	−50 mA
I_{RY} (TP3204)	120 mA
Power Dissipation (Note 1)	1.5W

Electrical Characteristics

Unless otherwise specified, Limits printed in bold characters are guaranteed for V_{CC} = +5.0V, V_{BB} = −5.0V ±5% and T_A = 0°C to 70°C by correlation with 100% production testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at V_{CC} = +5.0V, V_{BB} = −5.0V, and T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
COMPENSATION CIRCUIT						
R_{IN}	Input Resistance	T+, T−, R+, R−		200		KΩ
V_{OS}	Offset Voltage at V_C	I_{LOOP} = 0 mA, R_S = 100Ω V_{BAT} = −48V, VC Open.	**−30**		**+30**	mV
A_V	Differential Voltage Gain	R_L = 150Ω, R_S = 100, Measure from T+, T−, R+ and R− to VC, I_{LOOP} = 10–100 mA	**0.147**		**0.153**	V/V
I_C	Maximum Compensation Current	The Output Current is Nominally Given by V_C/R_L, Where R_L is Connected from VC to GND.			25	mA
R_O	Output Resistance	Measure at CAP1	**80**	100	**120**	KΩ
VIC_{Sat}	Saturation Voltage at IC	I_C = 20 mA. Measure from VC to IC.		−0.3	**−1.5**	V
R_{IC}	IC Output Impedance	R_L = 150Ω, f = 1 kHz, I_C = 10 mA I_C = 20 mA		2 300		MΩ KΩ
N	Idle Noise	IC = 20 mA, R_L = 150Ω Connect 1500Ω from IC to V_{BAT}, Measure at IC.		0	**10**	dBrnC
SUPERVISION CIRCUITRY						
I_O	Ring-Trip Current Source	At CAP2		10		μA
I_R	Ring-Trip Threshhold	CAP2 = 0.1 μF, f = 20 Hz, R_S = 100Ω		12		mA
I+	Off-hook Positive Threshold	R_S = 100. Increase Loop Current until SUP Switches low.	**11**	13	**15**	mA
H	Off-hook Hysteresis	R_S = 100. Decrease Loop Current from I+ until SUP Switches High.		2		mA
RELAY DRIVERS						
VRY_{sat}	Relay Driver Saturation Voltage	TP3200, TP3202, IRY = 30 mA TP3204, IRY = 80 mA			**−2.2** **1**	V V
DIGITAL INTERFACE (SUP, EN, RC1, RC2, RING, RSYNC)						
V_{OL}	Output Low Level	I_{OL} = 1.6 mA			**0.4**	V
V_{OH}	Output High Level	I_{OH} = 0.1 mA	**4**			V
V_{IL}	Input Low Level				**0.7**	V
V_{IH}	Input High Level		**2**			V
I_I	Input Current	0.7 < V_{IN} < 2.0	0.1		0.1	mA
POWER DISSIPATION						
$I_{CC}0$	V_{CC} Supply I_{DLE} Current	R_L = 150Ω, R_S = 100Ω I_{LOOP} = 0 mA, All Relays Off		3	**4.5**	mA
$I_{BB}0$	V_{BB} Supply I_{DLE} Current	R_L = 150Ω, R_S = 100Ω, I_{LOOP} = 0 mA All Relays Off.		2.5	**4**	mA
$I_{CC}1$	V_{CC} Supply Active Current	R_L = 150Ω, R_S = 100Ω I_{LOOP} = 40 mA, I_{RY} = 10 mA		3	**4.7**	mA
$I_{BB}1$	V_{BB} Supply Active Current	R_L = 150Ω, R_S = 100Ω I_{LOOP} = 40 mA, I_{RY} = 10 mA		2.5	**4.2**	mA
PSRR+	Power Supply Rejection Ratio	$\Delta V_C/\Delta V_{CC}$, f = 1 kHz	**−60**	−80		dB
PSRR−		$\Delta V_C/\Delta V_{BB}$, f = 1 kHz	**−38**	−50		dB

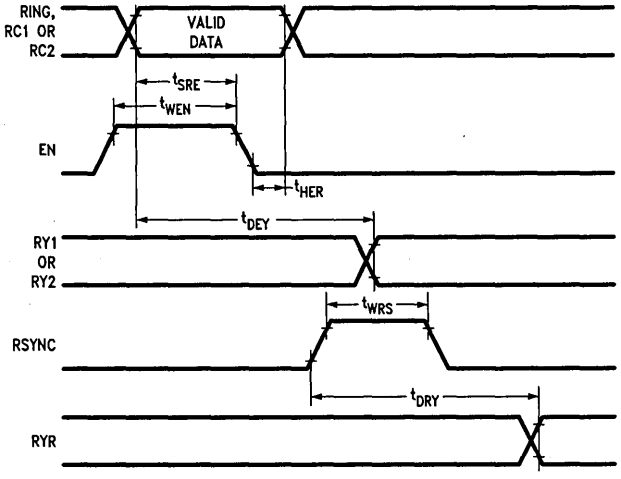
Electrical Characteristics

Unless otherwise specified, Limits printed in bold characters are guaranteed for $V_{CC} = +5.0V$, $V_{BB} = -5.0V \pm 5\%$ and $T_A = 0°C$ to $70°C$ by correlation with 100% production testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, and $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TIMING (SEE DEFINITIONS AND TIMING CONVENTIONS FOR TEST METHOD INFORMATION)						
t_{SRE}	Set-up Time	Measure from RING, or RC1, RC2 Valid to EN Falling Edge.	**1**			μs
t_{HER}	Hold Time	Measure from EN Falling Edge to RING, RC1, or RC2 Invalid.	**1**			μs
t_{WEN} t_{WRS}	Input Pulse Width EN RSYNC	Active High	**2** **3**			μs μs
t_{DEY}	RY1, RY2 Drivers Delay Time	Measure from En Active and RC1, RC2, Valid to RY1, RY2 On or Off. $I_{RY\ (on)} = 10$ mA, $I_{RY\ (off)} = 0.1$ mA			20	μs
t_{DRY}	RYR Driver Delay Time	Measure from RSYNC Rising Edge to RYR On or Off. $I_{RYR\ (on)} = 10$ mA, $I_{RYR\ (off)} = 0.1$ mA			20	μs
t_{HS}	Off-Hook Detection Time	Measure from $I_{LOOP} = 20$ mA to SUP Transition from High to Low.		2.5		μs
t_R	Ring-Trip Detection Time	Measure from $I_{LOOP} = 20$ mA to, RYR Off, CAP2 = 0.1 μF, f = 20 Hz, $I_{RYR\ (on)} = 10$ mA, $I_{RYR\ (off)} = 0.1$ mA			150	ms

Note 1: Derate based on 150°C maximum junction temperature and thermal resistance of 80°C/W, junction to ambient.

Timing Diagram



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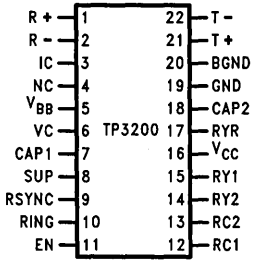
Connection Diagrams

Dual-In-Line



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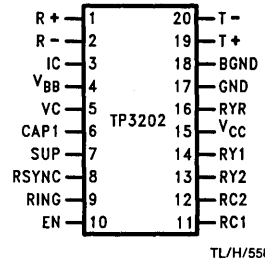
Top View

Dual-In-Line



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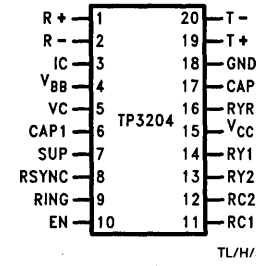
Top View

Dual-In-Line



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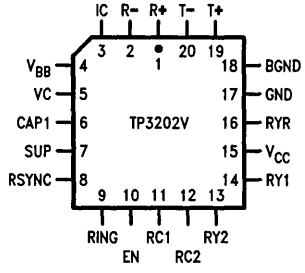
Top View

Plastic Chip Carrier



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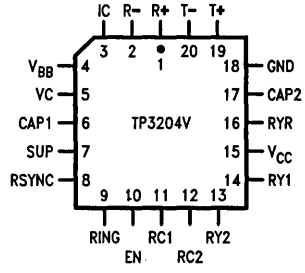
Top View

Plastic Chip Carrier



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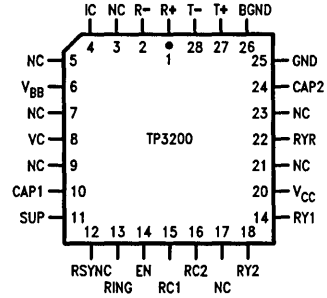
Top View

Plastic Chip Carrier



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Top View

Description of Pin Functions

Name	Function
T+	Tip positive voltage sense input connected to the positive (GND) side of the Tip current sense resistor.
T−	Tip negative voltage sense input connected to the negative (line) side of the Tip current sense resistor.
BGND	Battery ground return for the relay drivers. This ground should be connected in such a way as to minimize noise due to relay switching and also to avoid large voltage transients in the presence of lightning. Preferably it should be connected to GND on the backplane.
R−	Ring negative voltage sense input connected to the negative (V_{BAT}) side of the Ring current sense resistor.
R+	Ring positive voltage sense input connected to the positive (line) side of the Ring current sense resistor.
V_{BB}	−5 volts ±5%
IC	Compensation current output. The current sourced by this output is proportional to the d.c. loop current flowing through the line transformer. By passing this current through an auxiliary winding of appropriate winding ratio, the average magnetic flux in the transformer core can be cancelled.
CAP1	External capacitor input required to filter voice frequency components from the loop current.
CAP2	External capacitor input required to perform charging and discharging by I_O for one cycle of ring frequency in order to perform the ring-trip function.
VC	Compensation voltage output. The output voltage at this pin is proportional to the d.c. loop current flowing through the line transformer. An external resistor R_L connected from VC to GND causes a current to flow from IC which is in turn proportional to the d.c. loop current.
GND	Analog ground.
V_{CC}	+5 volts ±5%
SUP	Supervision output indicating off-hook, Dial Pulse and Ring Trip status.
EN	Enable input. The RING, RC1 and RC2 inputs are gated in during the high state of EN and latched on the falling edge.
RC1	General purpose relay control input 1, used to turn on or off relay driver 1 (RY1) when enabled by EN.
RC2	General purpose relay control input 2 used to turn on or off relay driver 2 (RY2) when enabled by EN.
RING	Ring command input used to turn on or off the ring relay driver when enabled by EN.

Description of Pin Functions (Continued)

Name	Function
RSYNC	Ring Synchronization input used to synchronize the opening and closing of the ring relay with zero crossings of the ring signal, i.e., the minimum voltage across the relay contacts. RSYNC should nominally be a square wave generated by a zero crossing detector from the ringing signal, and should have the same frequency as the ringing signal.
RYR	Ring relay driver output.
RY1	General purpose relay driver output 1.
RY2	General purpose relay driver output 2.

Functional Description

MAGNETIC COMPENSATION CIRCUIT *(Figure 1)*

The magnetic compensation circuit measures the loop current by sensing the voltage across two matched battery feed resistors, R_S, using a high impedance thin film resistor bridge, and produces a voltage proportional to the instantaneous loop current at the output of the OpAmp, A1. This voltage is filtered by the external capacitor CAP1. The output voltage follower A2 and output transistor Q1 then reproduce this voltage at the VC output. Capacitor CAP1 is selected such that the voice frequency components of the loop current are attenuated enough to prevent the compensation current from affecting the subscriber circuit output impedance. A resistor R_L connected from VC to GND causes a current V_C/R_L to flow from the IC output. This output is connected to an auxiliary winding on the line transformer. By proper selection of resistor ratios and transformer winding ratios, the current I_C can exactly cancel the flux produced by the d.c. component of the loop current. The equation relating these parameters is:

$$NP/NC = A_V R_S/R_L$$

SUPERVISION CIRCUIT *(Figure 2)*

The supervision circuit consists of a loop current comparator with built-in hysteresis. The input of the supervision circuit is taken from the output of the Op Amp A1. The voltage at this point represents the instantaneous loop current. The output is the SUP output. During on-hook operation SUP is high. When the loop current increases beyond approximately 13 mA the SUP output goes low, indicating off-hook. When the loop current falls below approximately 11 mA SUP will go high indicating on-hook. In the presence of dial pulses, SUP will produce a square-wave replication of the dial pulses. During ringing, the comparator will detect the instantaneous ringing current through the loop, causing SUP to produce a square-wave with a mark-to-space ratio larger than 50% during the on-hook condition. When the telephone goes off-hook, the resultant dc loop current causes the mark-to-space ratio to decrease until the threshhold is reached when the duty cycle of SUP output is exactly 50%. This change in duty cycle can easily be detected digitally and the ringing terminated. This is the most flexible form of ring trip since it is frequency independent and is compatible with multi-frequency ringing. A second method of ring trip is described in the next section.

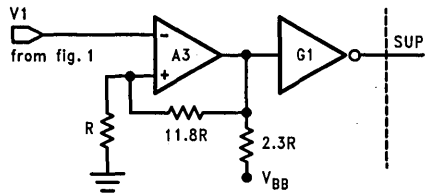

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FIGURE 2. Supervision Circuit

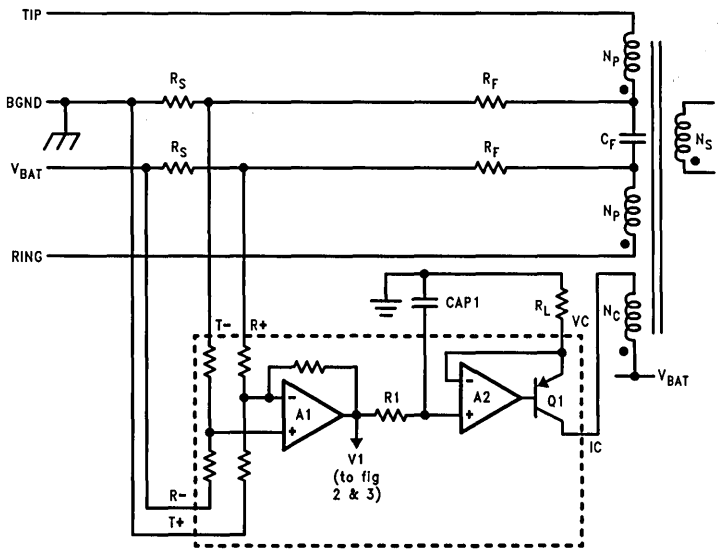

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FIGURE 1. Magnetic Compensation Circuit—Simplified Diagram

Functional Description (Continued)

RING TRIP CIRCUIT *(Figure 3)*

The ring trip circuit takes its input from the output of A1, which represents the combination of instantaneous ringing current and DC off-hook loop current, if any. A1 output voltage is compared against a reference voltage at A4. Depending on the polarity of the comparator's output, current source I_O either sources or sinks 10 μA into CAP2. This results in the charging and discharging of CAP2. Each positive transition of RSYNC enables comparator A5 for approximately 20 μs through the one-shot circuit, after which CAP2 is discharged via Q2. Thus, the resulting voltage on CAP2 after one ring cycle indicates the average DC component of the loop current. When the threshold of approximately 12 mA is reached, comparator A5 generates a pulse output at RT which is used to reset the ring driver flip-flop at approximately the zero crossing of the ringing signal.

If multiple ring frequencies must be used on the same line, then a compromise capacitor value for CAP2 must be used. A 0.1 μF value is recommended for ringing frequencies of 16 Hz to 40 Hz, and 0.033 μF for 30 Hz to 70 Hz. Alternately, if SUP output is used to perform ring trip detect externally, CAP2 input should be grounded.

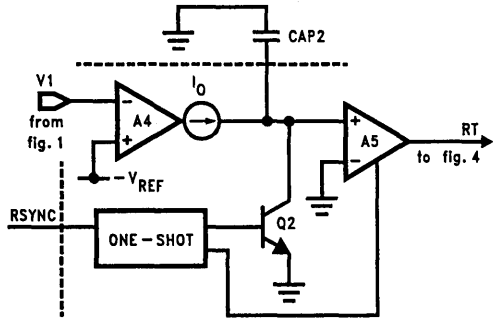

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FIGURE 3. Ring Trip Circuit

RING RELAY DRIVER *(Figure 4)*

The ring relay driver consists of the ring trip latch, a ring relay flip-flop and a relay driver output transistor. Based on the state of the ring input, the ring-trip latch is set or cleared when EN is active high, and latched on the falling edge of EN. It is also cleared by the ring trip circuit. Based on the output of the ring-trip latch, the ring relay flip-flop is set or cleared on the positive transition of RSYNC, insuring that the ring relay is turned on or off near the zero crossing of the ring signal to minimize relay contact wear. After the ring relay driver is turned on, the RING and/or EN inputs should be kept at logic low in order to prevent relay chattering.

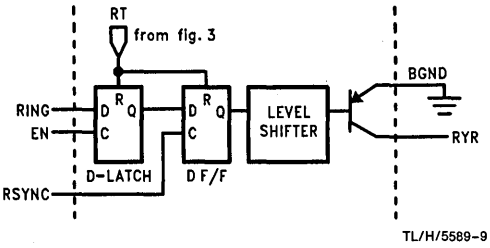

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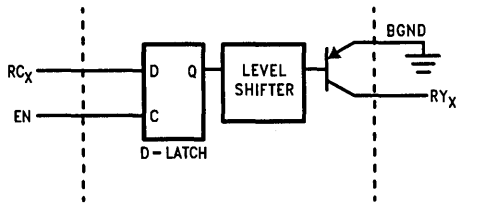
FIGURE 4. Ring Trip Relay Driver (PNP-type)

GENERAL PURPOSE RELAY DRIVERS *(Figure 5)*

The general purpose relay drivers consist of a relay driver latch and relay driver output transistor. Depending on the state of the appropriate input RC1 or RC2, the relay driver latches are set or cleared when EN is active high, and latched on the falling edge of EN. On the TP3200 and TP3202 the relay driver pnp transistors operate between BGND and a negative supply as high as −70 volts, with relay currents as high as 30 mA. On the TP3204, the relay driver npn transistors operate with a positive supply voltage up to 20 volts.



TL/H/5589–10

FIGURE 5. Relay Drivers RY1 and RY2, (PNP-type)

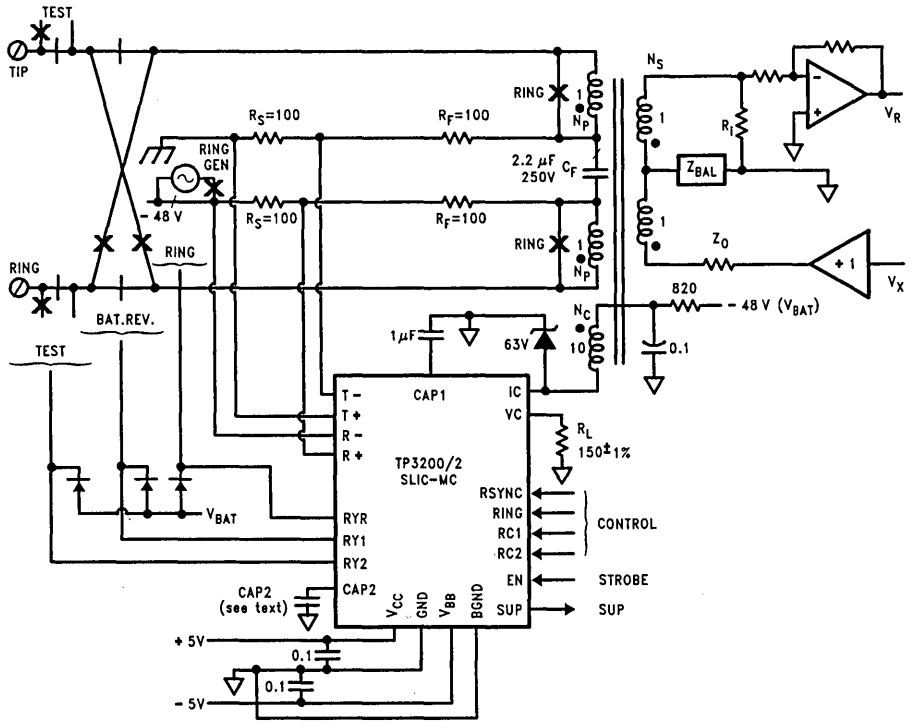


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FIGURE 6. Typical Applications Schematic

Note 1: Resistors R_S, R_F are matched to within ±0.1% to achieve 60 dB longitudinal balance.

Note 2: Transformer specifications for 600Ω Line Impedance, 5:1 cancellation ratio, $Z_o = R_i = 300\Omega$.

primary windings	N_P	210T	AWG 36
secondary windings	N_S	2x220T	AWG 38
compensation winding	N_C	210T	AWG 42

Siemens Type RM 8-T35 core (A_L = 8400 nH/T²)

Applications Information

Figure 6 illustrates the use of the TP3200/02/04 in one of many possible configurations. In this application, 200 ohm feed resistors ($R_S + R_F$) are used with a fixed −48 volt battery feed. 100 ohm current sense resistors in series with additional 100 ohm resistors insure that the T and R sense inputs of the device never see more than one half of any line transient voltages. The two general purpose relay drivers are used to operate a line test relay and a battery reversal relay. The a.c. line termination impedance is set by resistors R_i and Z_o (which should be equal to properly balance the hybrid), and the square of the turns ratio of the transformer, $(2N_p/N_S)^2$. The two amplifiers on the secondary side of the transformer are normally part of the PCM filter such as the TP3040, or the TP3050, TP3060, or TP3070 series of COMBO™ Codec/Filters. Z_{bal} represents the line circuit balance network. It is recommended that the IC pin be connected to the finish of the compensation winding in order to reduce the effective loading of the line impedance as well as Z_{bal} due to the reflected capacitance from the compensation winding at IC.

Ring voltage insertion is accomplished by breaking the battery feed path and superimposing the a.c. voltage upon the battery voltage. To prevent the feed decoupling capacitor from shunting ring current, a break contact is placed in series with C_F. To prevent the line transformer primary windings from attenuating the ring voltage or introducing distortion, make contacts are connected in shunt with the transformer primary.

Each relay driver output must be protected by a diode connected close to the relay coil. The IC pin must also be protected against line transients coupled through the transformer. Standard secondary transient suppression must also be connected from Tip to GND and Ring to GND.

In order to minimize errors in flux cancellation, the ratio of resistors R_S and R_L must be carefully controlled. Normally, all would reside on a common hybrid circuit. The two resistors, R_S, must be very accurately matched as must the two resistors, R_F, although R_F need not match R_S.

Application Information (Continued)

The a.c. loop voltage will appear at IC, amplified by the ratio $N_C/(2N_p)$. A d.c. bias voltage must be provided which is sufficiently negative to prevent the compensation transistor from saturating without producing excessive power dissipation in the integrated circuit. This bias voltage can be an intermediate supply voltage or may be generated by the compensation current flowing through a resistance. The resistance may be made up of the transformer winding resistance and discrete resistances such as the filter resistor shown in *Figure 6.* If the bias voltage is generated by an IR drop, a higher supply voltage or lower compensation current ratio will be required to allow for large variations in loop current, resulting in higher circuit power dissipation.

Design Example

Assuming a 0 TLP on the line of 0 dBm into 600Ω, a 3 dB overload corresponds to a peak signal level of 1.55 volts. The peak a.c. voltage at IC is therefore 1.55N, where $N = N_C/(2N_P)$. At minimum loop current, the d.c. bias at IC must be sufficiently positive of the zener voltage to allow negative swings without clipping. Allowing for the winding resistance and reactance, a safe limit is:

$$R_C \bullet I_{LOOP}\,(\text{min})/N > 1.55N - V_{Z\,min} + |V_{BAT}|_{max} \quad (1)$$

where V_Z is the zener voltage, R_C is the total resistance from IC to V_{BAT}.

At the opposite extreme, the compensation transistor must not saturate with maximum loop current and positive peak swings. This corresponds to a voltage at IC of not less than

$$-VIC_{sat} + VC = 1.5 + I_{LOOP}\,(\text{max}) \bullet 2R_S \bullet A_V.$$

Thus we require:

$$|V_{BAT}|\,(\text{min}) > R_C \bullet I_{LOOP}\,(\text{max})/N + 1.55N - VIC_{SAT} + I_{LOOP}(\text{max}) \bullet 2R_S \bullet A_V \quad (2)$$

Substituting for R_C,

$$|V_{BAT}|(\text{min}) > (1.55N - V_{Zmin} + |V_{BAT}|_{max}) \bullet I_{LOOP}(\text{max})/I_{LOOP}(\text{min}) + 1.55N + 1.5 + 30I_{LOOP}(\text{max})$$

Thus for a minimum loop current of 20 mA and a maximum of 100 mA, with a minimum zener voltage of 58 volts, and battery voltage from −42V to −54V, the maximum compensation current ratio is 6.18:1.

If N = 5 is chosen, i.e. N_C = 10 Np, the allowable range for R_C can then be calculated. From 1), $R_C > 938\Omega$, and from 2), $R_C < 1487\Omega$. Since the resistance of the compensation winding may typically be 600Ω, an additional 820Ω can safely be added in series to form a high frequency filter on the battery supply.

Finally, from $Np/Nc = A_V \bullet R_S/R_L$, $R_L = 150\Omega$.

Further Information

For additional information on design of suitable transformers see National Semiconductor Application Note AN-439.

For information on the design of matched attenuators suitable for setting Receive TLP levels, see the data sheet "TP3052 Family of COMBO™ Devices".

National Semiconductor Corporation

PRELIMINARY

microCMOS

TP3070/TP3071 COMBO II™ Programmable PCM CODEC/Filter

General Description

The TP3070 series are second-generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber and trunk line cards. Using advanced switched capacitor techniques, COMBO II combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

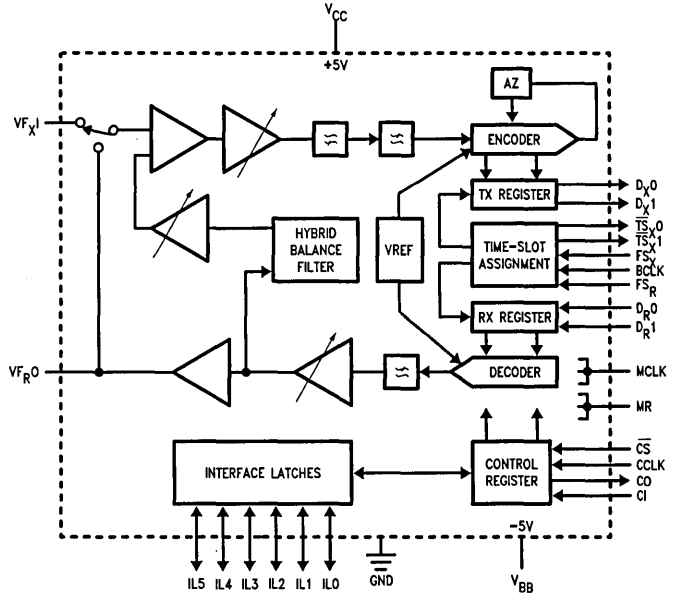
Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions. Both transformer and active SLIC interface circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

To enable COMBO II to interface to the SLIC control leads, a number of programmable latches are included; each may be configured as either an input or an output. The TP3070 provides 6 latches and the TP3071 5 latches.

Features

- Complete CODEC and FILTER system including:
  - — Transmit and receive PCM channel filters
  - — μ-law or A-law companding coder and decoder
  - — Receive power amplifier drives 300Ω
  - — 4.096 MHz serial PCM data (max)
- Programmable Functions:
  - — Transmit gain: 25.4 dB range, 0.1 dB steps
  - — Receive gain: 25.4 dB range, 0.1 dB steps
  - — Hybrid balance cancellation filter
  - — Time-slot assignment; up to 64 slots/frame
  - — 2 port assignment (TP3070)
  - — 6 interface latches (TP3070)
  - — A or μ-law
  - — Analog loopback
  - — Digital loopback
- Direct interface to solid-state SLICs
- Simplifies transformer SLIC; single winding secondary
- Standard serial control interface
- 70 mW operating power (typ)
- 5 mW standby power (typ)
- Meets or exceeds all CCITT and LSSGR specifications
- TTL and CMOS compatible digital interfaces

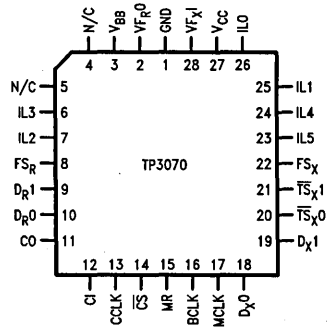
Block Diagram



TL/H/8635–1

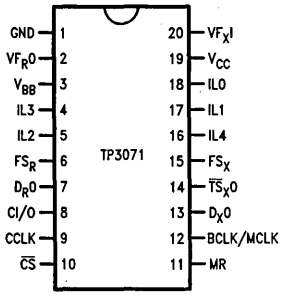
FIGURE 1

Connection Diagrams



TL/H/8635-4

Order Number TP3070V
See NS Package Number V28A



TL/H/8635-2

Order Number TP3071N
See NS Package Number N20A

Pin Descriptions

Pin	Description
V_{CC}	+5V ±5% power supply.
V_{BB}	−5V ±5% power supply.
GND	Ground. All analog and digital signals are referenced to this pin.
FS_X	Transmit Frame Sync input. Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the transmit time slot assigned to this device (non-delayed frame mode), or the start of the transmit frame (delayed frame mode using the internal time-slot assignment counter).
FS_R	Receive Frame Sync input. Normally a pulse or squarewave waveform with an 8 kHz repetition rate is applied to this input to define the start of the receive time slot assigned to this device (non-delayed frame mode), or the start of the receive frame (delayed frame mode using the internal time-slot assignment counter).
BCLK	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1.536/1.544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK.
VF_XI	The Transmit analog high-impedance input. Voice frequency signals present on this input are encoded as an A-law or μ-law PCM bit stream and shifted out on the selected D_X pin.
VF_RO	The Receive analog power amplifier output, capable of driving load impedances as low as 300Ω (depending on the peak overload level required). PCM data received on the assigned D_R pin is decoded and appears at this output as voice frequency signals.

Pin	Description
D_X0 D_X1	D_X1 is available on the TP3070 only; D_X0 is available on all devices. These Transmit Data TRI-STATE® outputs remain in the high impedance state except during the assigned transmit time slot on the assigned port, during which the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS}_X0$ $\overline{TS}_X1$	$\overline{TS}_X1$ is available on the TP3070 only; $\overline{TS}_X0$ is available on all devices. Normally these open-drain outputs are floating in a high impedance state except when a time-slot is active on one of the D_X outputs, when the appropriate $\overline{TS}_X$ output pulls low to enable a backplane line-driver.
D_R0 D_R1	D_R1 is available on the TP3070 only; D_R0 is available on all devices. These receive data input(s) are inactive except during the assigned receive time slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.
CCLK	Control Clock input. This clock shifts serial control information into or out from CI/O when the $\overline{CS}$ input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI/O	This is the Control Data I/O pin which is provided on the TP3071. Serial control information is shifted into or out from COMBO II on this pin when $\overline{CS}$ is low. The direction of the data is determined by the current instruction as defined in Table I.
CI	This is a separate Control Input, available only on the TP3070. It can be connected to CO if required.
CO	This is a separate Control Output, available only on the TP3070. It can be connected to CI if required.
$\overline{CS}$	Chip Select input. When this pin is low, control information can be written into or out from COMBO II via the CI/O pin (or CI and CO).
IL5–IL0	IL5 through IL0 are available on the TP3070. IL4 through IL0 are available on the TP3071. Each Interface Latch I/O pin may be individually

Pin Descriptions (Continued)

Pin	Description
	programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to COMBO II, while $\overline{CS}$ is low, and the information is shifted out on the CO (or CI/O) pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
MR	This logic input must be pulled low for normal operation of COMBO II. When pulled momentarily high (at least 1 μsec.), all programmable registers in the device are reset to the states specified under "Power-On Initialization".

Functional Description

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes the COMBO II and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for minimum gain, the hybrid balance circuit is turned off, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CI/O pin is set as an input ready for the first control byte of the initialization sequence. Other initial states in the Control Register are indicated in Section 2.0.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high. This may be done either when powered-up or down. For normal operation this pin must be pulled low.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing a Power-Down instruction into the serial control port as indicated in Table I. The power down instruction may be included within any other instruction code. It is recommended that the chip be powered down before executing any instructions. In the power-down state, all non-essential circuitry is de-activated and the D_X0 (and D_X1) outputs are in the high impedance TRI-STATE condition.

The coefficients stored in the Hybrid Balance circuit and the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains active. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control the SLIC.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI, is a high impedance summing input which is used as the differencing point for the internal hybrid balance cancellation signal. No external components are necessary to set the gain. Following this circuit is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active pre-filter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or μ255 coding laws, which must be selected by a control instruction during initialization (see Tables I and II). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is canceled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Transmit Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_X0 or D_X1 during the selected time slot on eight rising edges of BCLK.

DECODER AND RECEIVE FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R0 or D_R1 pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or μ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Post-Filter/Power Amplifier capable of driving a 300Ω load to ±3.5V, a 600Ω load to ±3.8V or a 15 kΩ load to ±4.0V at peak overload.

A decode cycle begins immediately after each receive time-slot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (½ frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK HIGH to one MCLK period LOW. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see Table II). Non-delayed data mode is similar to long-frame timing on the TP3050/60 series of devices; (COMBO I™) time-slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode, which is similar to short-frame sync timing on COMBO I, in which each FS input must be high at least a half-cycle of BCLK earlier than the time-slot. The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing.

When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters.

Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles. During each assigned Transmit time-slot, the selected $D_X0/1$ output shifts data out from the PCM register on the rising edges of BCLK. $\overline{TS}_X0$ (or $\overline{TS}_X1$ as appropriate) also pulls low for the first 7½ bit times of the time-slot to control the TRI-STATE Enable of a backplane line-driver. Serial PCM data is shifted into the selected $D_R0/1$ input during each assigned Receive time-slot on the falling edges of BCLK. D_X0 or D_X1 and D_R0 or D_R1 are selectable on the TP3070 only, see Section 6.

TABLE I. Programmable Register Instructions

Function	Byte 1 (Note 1) 7	6	5	4	3	2	1	0	Byte 2 (Note 1) 7	6	5	4	3	2	1	0
Single Byte Power-Up/Down	P	X	X	X	X	X	0	X	None							
Write Control Register	P	0	0	0	0	0	1	X	See Table II							
Read-Back Control Register	P	0	0	0	0	1	1	X	See Table II							
Write to Interface Latch Register	P	0	0	0	1	0	1	X	See Table V							
Read Interface Latch Register	P	0	0	0	1	1	1	X	See Table V							
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table IV							
Read Latch Direction Register	P	0	0	1	0	1	1	X	See Table IV							
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table VIII							
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table VIII							
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table VII							
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table VII							
Write Receive Time-Slot/Port	P	1	0	0	1	0	1	X	See Table VI							
Read-Back Receive Time-Slot/Port	P	1	0	0	1	1	1	X	See Table VI							
Write Transmit Time-Slot/Port	P	1	0	1	0	0	1	X	See Table VI							
Read-Back Transmit Time-Slot/Port	P	1	0	1	0	1	1	X	See Table VI							

Note 1: Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI, CO or CI/O pin. X = don't care.

Note 2: "P" is the power-up/down control bit, see "Power-up" section. ("0" = Power Up, "1" = Power Down)

Note 3: 3 additional registers are provided for the Hybrid Balance Filter, see Section 9.0.

Functional Decription (Continued)

SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO II via the serial control port consisting of the control clock CCLK; the serial data input/output, CI/O, (or separate input, CI, and output, CO, on the TP3070 only); and the Chip Select input, $\overline{CS}$. All control instructions require 2 bytes, as listed in Table I, with the exception of a single byte power-up/down command.

To shift control data into COMBO II, CCLK must be pulsed high 8 times while $\overline{CS}$ is low. Data on the CI/O (or CI) input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first contiguously, i.e. it is not mandatory for $\overline{CS}$ to return high in between the first and second control bytes. At the end of CCLK8 in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However, $\overline{CS}$ should be set high when no data transfers are in progress.

To readback Interface Latch data or status information from COMBO II, the first byte of the appropriate instruction is strobed in during the first $\overline{CS}$ pulse, as defined in Table I. $\overline{CS}$ must then be taken low for a further 8 CCLK cycles, during which the data is shifted onto the CO or CI/O pin on the rising edges of CCLK. When $\overline{CS}$ is high the CO or CI/O pin is in the high-impedance TRI-STATE, enabling the CI/O pins of many devices to be multiplexed together.

Programmable Functions

1.0 POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in Table I into COMBO II with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down by setting the "P" bit as indicated. When the power up or down control is entered as a single byte instruction, Bit one (1) must be reset to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), D_X0 (and D_X1), will remain in the high impedance state until the second FS_X pulse after power-up.

2.0 CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in Table I. The second byte has the following bit functions:

TABLE II. Control Register Byte 2 Functions

Bit Number and Name 7	6	5	4	3	2	1	0	Function
F_1	F_0	MA	IA	DN	DL	AL	PP	
0	0							MCLK = 512 kHz
0	1							MCLK = 1.536 or 1.544 MHz
1	0							MCLK = 2.048 MHz*
1	1							MCLK = 4.096 MHz
		0	X					Select μ-255 law*
		1	0					A-law, Including Even Bit Inversion
		1	1					A-law, No Even Bit Inversion
				0				Delayed Data Timing
				1				Non-Delayed Data Timing*
					0	0		Normal Operation*
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN*

* = State at power-on initialization.

Programmable Functions (Continued)

TABLE III. Coding Law Conventions

	μ255 law	True A-law with even bit inversion	A-law without even bit inversion
	MSB LSB	MSB LSB	MSB LSB
V_{IN} = +Full Scale	10000000	10101010	11111111
V_{IN} = 0V	11111111 01111111	11010101 01010101	10000000 00000000
V_{IN} = −Full Scale	00000000	00101010	01111111

Note 1: The MSB is always the first PCM bit shifted in or out of COMBO II.

2.1 Master Clock Frequency Selection

A Master clock must be provided to COMBO II for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F_1 and F_0 (see Table II) must be set during initialization to select the correct internal divider.

2.2 Coding Law Selection

Bits "MA" and "IA" in Table II permit the selection of μ255 coding or A-law coding, with or without even bit inversion.

2.3 Analog Loopback

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop.

2.4 Digital Loopback

Digital Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at $D_X0/1$. No PCM decoding or encoding takes place in this mode, VF_RO maintains a low impedance idle output.

3.0 INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see Tables I and IV.

Bits L_5–L_0 must be set by writing the specified instruction to the LDR with the L bits in the second byte set as follows:

TABLE IV. Byte 2 Functions of Latch Direction Register

Byte 2 Bit Number							
7	6	5	4	3	2	1	0
L_0	L_1	L_2	L_3	L_4	L_5	X	X

L_n Bit	IL Direction
0	Input
1	Output

X = don't care

4.0 INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Interface Latch Register (ILR) as shown in Tables I and V. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR.

It is recommended that, during initialization, the state of IL pins to be configured as outputs should first be programmed, followed immediately by the Latch Direction Register.

TABLE V. Interface Latch Data Bit Order

Bit Number							
7	6	5	4	3	2	1	0
D_0	D_1	D_2	D_3	D_4	D_5	X	X

5.0 TIME-SLOT ASSIGNMENT

COMBO II can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_r. Time-Slot Assignment may only be used with Delayed Data timing; see *Figure 5*. FS_X and FS_r may have any phase relationship with each other in BCLK period movements.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in Tables I and VI. The last 6 bits of the second byte indicate the selected time-slot from 0–63 using straight binary notation. A new assignment becomes active on the second frame following the end of the Chip-Select for the second control byte. The "EN" bit allows the PCM inputs, $D_R0/1$, or outputs, $D_X0/1$, as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the FS_X and FS_R pulses must conform to the delayed data timing format shown in *Figure 6*.

TABLE VI. Time-Slot and Port Assignment Instruction

Bit Number and Name								Function
7 EN	6 PS (Note 1)	5 T_5 (Note 2)	4 T_4	3 T_3	2 T_2	1 T_1	0 T_0	
0	0	X	X	X	X	X	X	Disable D_X0 Output (Transmit Instruction) Disable D_R0 Input (Receive Instruction)
0	1	X	X	X	X	X	X	Disable D_X1 Output (Transmit Instruction) Disable D_R1 Input (Receive Instruction)
1	0	Assign One Binary Coded Time-Slot from 0–63 Assign One Binary Coded Time-Slot from 0–63						Enable D_X0 Output (Transmit Instruction) Enable D_R0 Input (Receive Instruction)
1	1	Assign One Binary Coded Time-Slot from 0–63 Assign One Binary Coded Time-Slot from 0–63						Enable D_X1 Output (Transmit Instruction) Enable D_R1 Input (Receive Instruction)

Note 1: The "PS" bit MUST always be set to 0 for the TP3071.

Note 2: T5 is the MSB of the Time-slot assignment.

Programmable Functions (Continued)

6.0 PORT SELECTION

On the TP3070 only, an additional capability is available; 2 Transmit serial PCM ports, D_X0 and D_X1, and 2 Receive serial PCM ports, D_R0 and D_R1, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instruction using the "PS" bit in the second byte. Port Selection may only be used in Delayed Data timing mode.

On the TP3071, only ports D_X0 and D_R0 are available, therefore the "PS" bit MUST always be set to 0 for these devices.

Table VI shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

7.0 TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in Tables I and VII. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.619 Vrms and 0.087 Vrms (equivalent to +6.4 dBm to −19.0 dBm in 600Ω).

To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.08595)$$

and convert to the binary equivalent. Some examples are given in Table VII.

8.0 RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in Tables I and VIII. Note the following restrictions on output drive capability:

a) 0 dBm0 levels ≤ 1.96 Vrms at VF_RO may be driven into a load of ≥ 15 kΩ to GND;

b) 0 dBm0 levels ≤ 1.90 Vrms at VF_RO may be driven into a load of ≥ 600Ω to GND;

c) 0 dBm0 levels ≤ 1.70 Vrms at VF_RO may be driven into a load of ≥ 300Ω to GND.

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.1046)$$

and convert to the binary equivalent. Some examples are given in Table VIII.

TABLE VII. Byte 2 of Transmit Gain Instructions

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_XI
0 0 0 0 0 0 0 0	No Output
0 0 0 0 0 0 0 1	0.087
0 0 0 0 0 0 1 0	0.088
—	—
1 1 1 1 1 1 1 0	1.600
1 1 1 1 1 1 1 1	1.619

TABLE VIII. Byte 2 of Receive Gain Instruction

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_RO
0 0 0 0 0 0 0 0	No Output (Low Z to GND)
0 0 0 0 0 0 0 1	0.106
0 0 0 0 0 0 1 0	0.107
—	—
1 1 1 1 1 1 1 0	1.95
1 1 1 1 1 1 1 1	1.96

Programmable Functions (Continued)

9.0 HYBRID BALANCE FILTER

The Hybrid Balance Filter on COMBO II is a programmable filter consisting of a second-order Bi-Quad section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180 degree inverting stage is included to compensate for interface circuits which also invert the transmit input relative to the receive output signal. The Bi-quad is intended mainly to balance low frequency signals across a transformer SLIC, and the first order section to balance midrange to higher audio frequency signals.

As a Bi-Quad, Hybal1 has a pair of low frequency zeroes and a pair of complex conjugate poles. When configuring the Bi-Quad, matching the phase of the hybrid at low to midband frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancellation signal can be corrected by the programmable attenuator.

The Bi-Quad mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 Henries or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low frequency pole and 0 Hz zero. In this mode, the pole frequency may be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 section only, in which case the Hybal2 filter should be de-selected to bypass it.

Hybal2, the higher frequency first-order section, is provided for balancing an electronic SLIC, and is also helpful with a transformer SLIC in providing additional phase correction for mid and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less, such as the loaded and non-loaded loop test networks in the United States. Independent placement of the pole and zero location is provided.

Figure 2 shows a simplified diagram of the local echo path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at VF_XI, are a function of the termination impedance Z_T, the line transformer and the impedance of the 2W loop, Z_L. If the impedance reflected back into the transformer primary is expressed as Z_L' then the echo path transfer function from VF_RO to VF_XI is:

$$H(w) = Z_L'/(Z_T + Z_L') \quad (1)$$

9.1 PROGRAMMING THE FILTER

On initial power-up the Hybrid Balance filter is disabled. Before the hybrid balance filter can be programmed it is necessary to design the transformer and termination impedance in order to meet system 2W input return loss specifications, which are normally measured against a fixed test impedance (600 or 900Ω in most countries). Only then can the echo path be modeled and the hybrid balance filter programmed. Hybrid balancing is also measured against a fixed test impedance, specified by each national Telecom administration to provide adequate control of talker and listener echo over the majority of their network connections. This test impedance is Z_L in *Figure 2*. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input, D_RO, to the PCM digital output, D_XO, either by digital test signal analysis or by conversion back to analog by a PCM CODEC/Filter.

Three registers must be programmed in COMBO II to fully configure the Hybrid Balance Filter as follows:

Register 1: select/de-select Hybrid Balance Filter;
invert/non-invert cancellation signal;
select/de-select Hybal2 filter section;
attenuator setting.

Register 2: select/de-select Hybal1 filter;
set Hybal1 to Bi-quad or 1st order;
pole and zero frequency selection.

Register 3: program pole frequency in Hybal2 filter;
program zero frequency in Hybal2 filter.

Standard filter design techniques may be used to model the echo path (see Equation 1) and design a matching hybrid balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid balance filter designed to replicate it.

A Hybrid Balance filter design guide and software optimization program are available under license from National Semiconductor Corporation; order TP3077SW.

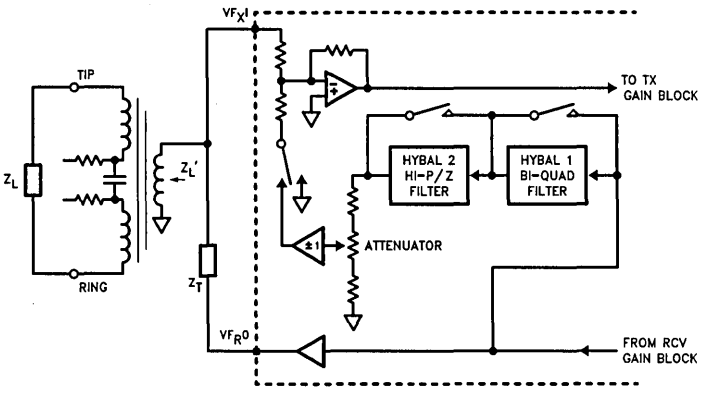


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FIGURE 2. Simplified Diagram of Hybrid Balance Circuit

Applications Information

Figure 3 shows a typical application of the TP3071 together with a transformer-based SLIC using the TP3204 Magnetic Compensation device. Four of the IL latches are configured as outputs to control the relay drivers on the SLIC, while IL4 is an input for the Supervision signal. *Figure 4* shows a similar arrangement with a monolithic SLIC.

POWER SUPPLIES

While the pins of the TP3070 COMBO II devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 μF should be connected from this common point to V_{CC} and V_{BB} as close to the device pins as possible.

Further guidelines on PCB layout techniques are provided in Application Note AN-370.

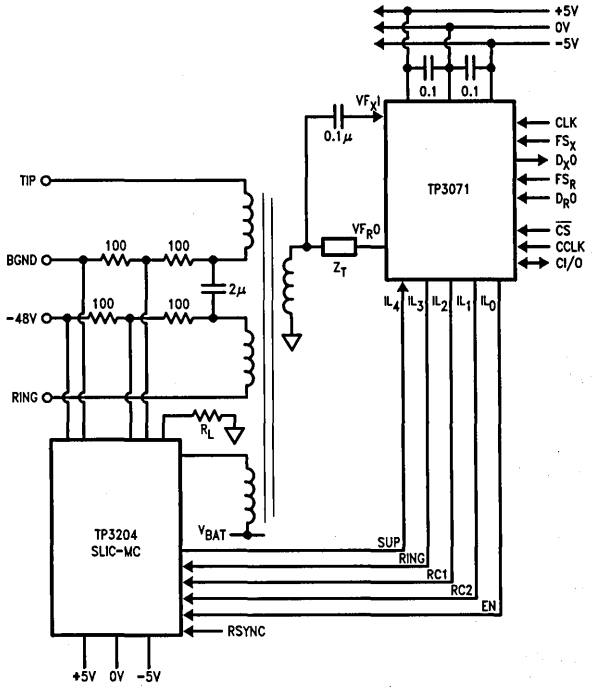

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FIGURE 3. Typical Application with Transformer SLIC

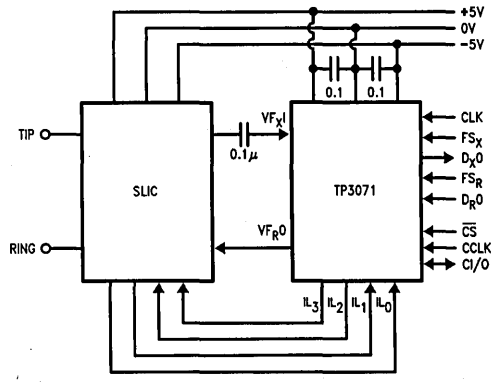

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FIGURE 4. Typical Application with Monolithic SLIC

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at VF_XI	V_{CC} + 1V to V_{BB} − 1V
Voltage at any Digital Input	V_{CC} + 1V to GND − 1V
Storage Temperature Range	−65°C to + 150°C
V_{BB} to GND	−7V
Current at VF_r0	±100 mA
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating is to be determined (TBD).

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs (DC Meas.)*			**0.7**	V
V_{IH}	Input High Voltage	All Digital Inputs (DC Meas.)*	**2.0**			V
V_{OL}	Output Low Voltage	D_X0, D_X1 and CO, I_L = 3.2 mA, All Other Digital Outputs, I_L = 1 mA			**0.4**	V
V_{OH}	Output High Voltage	D_X0, D_X1 and CO, I_L = −3.2 mA, All Other Digital Outputs (except $\overline{TS}_X$), I_L = −1 mA All Digital Outputs, I_L = −100 μA	**2.4** V_{CC} − 0.5			V V
I_{IL}	Input Low Current	Any Digital Input, GND < V_{IN} < V_{IL}	**−10**		**10**	μA
I_{IH}	Input High Current	Any Digital Input, V_{IH} < V_{IN} < V_{CC}	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X0, D_X1, CO and CI/O (as an Output) IL5–IL0 When Selected as Inputs GND < V_{OUT} < V_{CC}	**−10**		**10**	μA
ANALOG INTERFACES						
I_{VFXI}	Input Current, VF_XI	−3.3V < VF_XI < 3.3V	**−10.0**		**10.0**	μA
R_{VFXI}	Input Resistance	−3.3V < VF_XI < 3.3V	**390**			kΩ
VOS_X	Input Offset Voltage at VF_XI				20	mV
RL_{VFRO}	Load Resistance	−3.5V < VF_RO < 3.5V	**300**			Ω
CL_{VFRO}	Load Capacitance	RL_{VFRO} ≥ 300Ω CL_{VFRO} from VF_RO to GND			**200**	pF
RO_{VFRO}	Output Resistance	Steady Zero PCM Code Applied to D_R0 or D_R1		1.0	3.0	Ω
VOS_R	Output Offset Voltage at V_{FRO}	Alternating ± Zero PCM Code Applied to D_R0 or D_R1, Maximum Receive Gain	**−200**		**200**	mV
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	CCLK, CI/O, CI, CO, = 0.4V, $\overline{CS}$ = 2.4V Interface Latches Set as Outputs with No Load, All Other Inputs Active, Power Amp Disabled			**1.5**	mA
$I_{BB}0$	Power Down Current	As Above			**−0.3**	mA
$I_{CC}1$	Power Up Current	CCLK, CI/O, CI, CO = 0.4V, $\overline{CS}$ = 2.4V No Load on Power Amp Interface Latches Set as Outputs with No Load		7.0	**10.0**	mA
$I_{BB}1$	Power Up Current	As Above		−7.0	**−10.0**	mA

Note *: See definitions and timing conventions section.

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%; V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER CLOCK TIMING						
f_{MCLK}	Frequency of MCLK	Selection of Frequency is Programmable (See Table III)		512 1536 1544 2048 **4096**		kHz kHz kHz kHz kHz
t_{WMH}	Period of MCLK High	Measured from V_{IH} to V_{IH} (See Note)	**80**			ns
t_{WML}	Period of MCLK Low	Measured from V_{IL} to V_{IL} (See Note)	**80**			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBM}	HOLD Time, BCLK LOW to MCLK HIGH	TP3070 Only	**50**			ns
PCM INTERFACE TIMING						
f_{BCLK}	Frequency of BCLK	May Vary from 64 kHz to 4096 kHz in 8 kHz Increments	**64**		**4096**	kHz
t_{WBH}	Period of BCLK High	Measured from V_{IH} to V_{IH}	**80**			ns
t_{WBL}	Period of BCLK Low	Measured from V_{IL} to V_{IL}	**80**			ns
t_{RB}	Rise Time of BCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FB}	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low		**0**			ns
t_{SFB}	Setup Time, $FS_{X/R}$ High to BCLK Low		**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads			**80**	ns
t_{DBZ}	Delay Time, BCLK Low or FS_X Low to $D_X0/1$ Disabled	Applies to the Later Edge In Non-Delayed Data Mode Only	**15**		**80**	ns
t_{DBT}	Delay Time, BCLK High to $\overline{TS}_X$ Low if FS_X High, or FS_X High to $\overline{TS}_X$ Low if BCLK High	Load = 100 pF Plus 2 LSTTL Loads			60	ns
t_{ZBT}	TRI-STATE Time, BCLK Low to $\overline{TS}_X$ High if FS_X Low, or BCLK High to $\overline{TS}_X$ High if FS_X High		15		60	ns
t_{DFD}	Delay Time, $FS_{X/R}$ High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads, Applies if $FS_{X/R}$ Rises Later than BCLK Rising Edge in Non-Delayed Data Mode Only			**80**	ns
t_{SDB}	Setup Time, $D_R0/1$ Valid to BCLK Low		**30**			ns
t_{HBD}	Hold Time, BCLK Low to $D_R0/1$ Invalid		**10**			ns

Note: Applies only to MCLK Frequencies ≥ 1.536 MHz. At 512 kHz a 50:50 ±2% Duty Cycle must be used.

Timing Specifications (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL CONTROL PORT TIMING						
f_{CCLK}	Frequency of CCLK				**2048**	kHz
t_{WCH}	Period of CCLK High	Measured from V_{IH} to V_{IH}	**160**			ns
t_{WCL}	Period of CCLK Low	Measured from V_{IL} to V_{IL}	**160**			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low	CCLK1	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High	CCLK 8	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low		**50**			ns
t_{SDC}	Setup Time, CI (OI/O) Data In to CCLK Low		**50**			ns
t_{HCD}	Hold Time, CCLK Low to CI/O Invalid		50			ns
t_{DCD}	Delay Time, CCLK High to CI/O Data Out Valid	Load = 100 pF plus 2 LSTTL Loads			**50**	ns
t_{DSD}	Delay Time, $\overline{CS}$ Low to CO (CI/O) Valid	Applies Only if Separate $\overline{CS}$ used for Byte 2			**50**	ns
t_{DDZ}	Delay Time, $\overline{CS}$ High to CO (CI/O) High Impedance	Applies when $\overline{CS}$ High Occurs before 9th CCLK High	15		80	ns
INTERFACE LATCH TIMING						
t_{SLC}	Setup Time, IL to CCLK 8 of Byte 1	Interface Latch Inputs Only	**100**			ns
t_{HCL}	Hold Time, IL Valid from 8th CCLK Low (Byte 1)		50			ns
t_{DCL}	Delay Time CCLK 8 of Byte 2 to IL	Interface Latch Outputs Only C_L = 50 pF			200	ns
MASTER RESET PIN						
t_{WMR}	Duration of Master Reset High		1			μs

Timing Diagrams

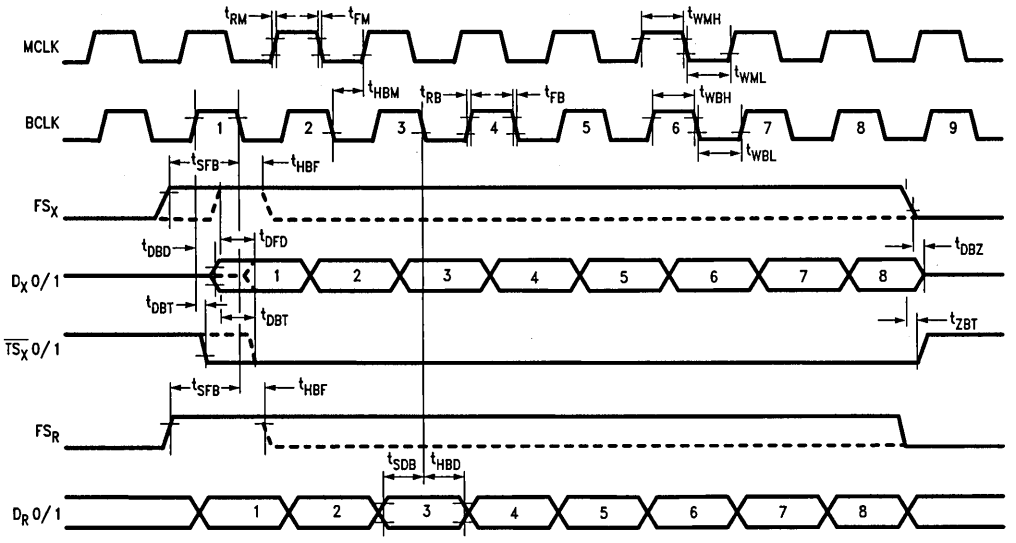

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FIGURE 5. Non Delayed Data Timing Mode

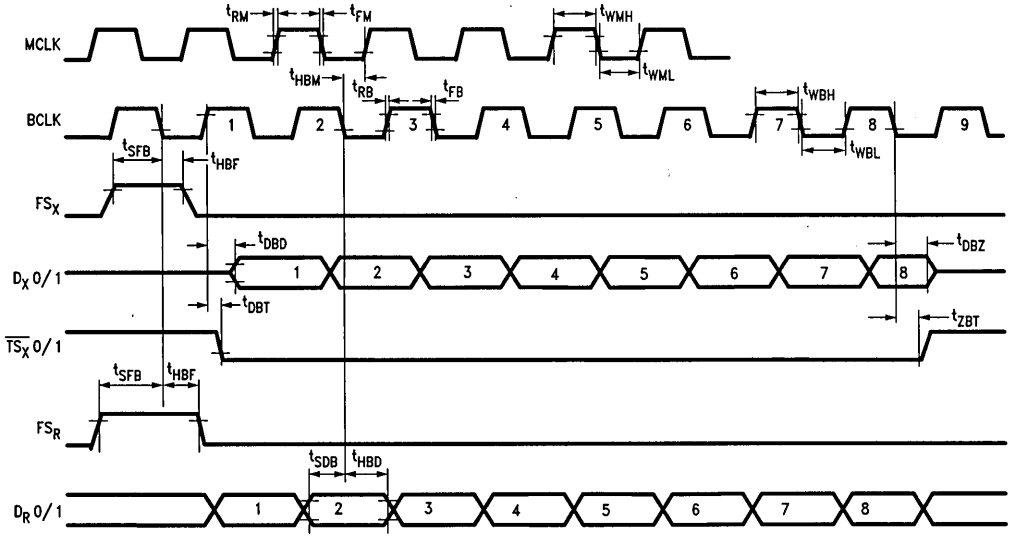

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FIGURE 6. Delayed Data Timing Mode

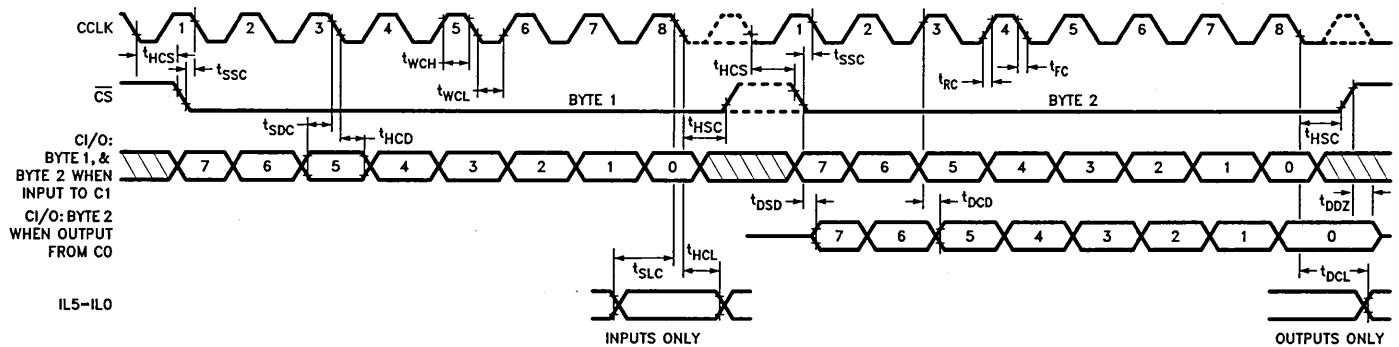

FIGURE 7. Control Port Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels, hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	The Maximum 0 dBm0 Levels are:				
		VF_XI		1.619		Vrms
		VF_RO (15 kΩ Load)		1.963		Vrms
		The Minimum 0 dBm0 Levels are:				
		VF_XI		87.0		mVrms
		VF_RO (Any Load > 300Ω)		106.0		mVrms
T_{max}	Maximum Overload	The Nominal Overload Levels are:				
		VF_XI—A-law		2.32		Vrms
		μ-law		2.33		Vrms
		VF_RO—A-law (600Ω Load)		2.73		Vrms
		μ-law (600Ω Load)		2.74		Vrms
		The Maximum Overload Levels are:				
		VF_XI—A-law		2.32		Vrms
		μ-law		2.33		Vrms
		VF_RO—A-law (15 kΩ Load)		2.82		Vrms
		μ-law (15 kΩ Load)		2.83		Vrms
		The Minimum Overload Levels are:				
		VF_XI—A-law		124.9		mVrms
		μ-law		125.3		mVrms
		VF_RO—A-law (Any Load > 300Ω)		152.2		mVrms
		μ-law (Any Load >300Ω)		152.7		mVrms
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for Maximum 0 dBm0 Test Level. Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at $D_X0/1$. T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V.	**−0.15**		**0.15**	dB
G_{XAG}	Transmit Gain Variation with Programmed Gain	Measure Transmit Gain Over the Range from Maximum to Minimum. Calculate the Deviation from the Programmed Gain Relative to G_{XA}, i.e., $G_{XAG} = G_{actual} - G_{prog} - G_{XA}$. T_A = 25°C, V_{CC} = 5V, V_{BB} = 5V	**−0.1**		**0.1**	dB
G_{XAF}	Transmit Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4) Minimum Gain < G_X < Maximum Gain D_R0 (or D_R1) = 0 dBm0 Code,				
		f = 60 Hz			−26	dB
		f = 200 Hz	−1.8		−0.1	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 4000 Hz			−14	dB
		f ≥ 4600 Hz. Measure Response at Alias Frequency from 0 kHz to 4 kHz.			−32	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels, hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE (Continued)						
G_{XAF} (Continued)		G_X = 0 dB, VF_XI = 1.619 Vrms D_R0 or D_R1 = 0 dBm0 Code (Note 4)				
		f = 62.5 Hz			**−24.9**	dB
		f = 203.125 Hz	**−1.7**		**−0.1**	dB
		f = 296.875 Hz	**−0.15**		**0.15**	dB
		f = 515.625 Hz	**−0.15**		**0.15**	dB
		f = 2796.875 Hz	**−0.15**		**0.15**	dB
		f = 3015.625 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.7**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
		f = 4593.750 Hz, Measure 3406.25 Hz			**−32**	dB
		f = 5015.625 Hz, Measure 2984.375 Hz			**−32**	dB
		f = 10015.625 Hz, Measure 2015.625 Hz			**−32**	dB
G_{XAT}	Transmit Gain Variation with Temperature	Measured Relative to G_{XA}, V_{CC} = 5V, V_{BB} = −5V, Minimum gain < G_X < Maximum Gain	−0.1		0.1	dB
G_{XAV}	Transmit Gain Variation with Supply	Measured Relative to G_{XA} V_{CC} = +5V ±5%, V_{BB} = −5V ±5% T_A = 25°C, G_X = Maximum Gain	**−0.05**		**0.05**	dB
G_{XAL}	Transmit Gain Variation with Signal Level	Sinusoidal Test Method. Reference Level = 0 dBm0.				
		VF_XI = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		VF_XI = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		VF_XI = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
G_{RA}	Receive Gain Absolute Accuracy	Receive Gain Programmed for Maximum 0 dBm0 Test Level. Apply 0 dBm0 PCM Code to D_R0 or D_R1. Measure VF_RO. T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V.	**−0.15**		**0.15**	dB
G_{RAG}	Receive Gain Variation with Programmed Gain	Measure Receive Gain Over the Range from Maximum to Minimum Setting. Calculate the Deviation from the Programmed Gain Relative to G_{RA}, i.e. $G_{RAG} = G_{actual} - G_{prog} - G_{RA}$. T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V	**−0.1**		**0.1**	dB
G_{RAT}	Receive Gain Variation with Temperature	Measured Relative to G_{RA}. V_{CC} = 5V, V_{BB} = −5V. Minimum Gain < G_R < Maximum Gain	−0.1		0.1	dB
G_{RAV}	Receive Gain Variation with Supply	Measured Relative to G_{RA}. V_{CC} = +5V ±5%, V_{BB} = −5V ±5% T_A = 25°C, G_R = Maximum Gain	**−0.05**		**0.05**	dB dB
G_{RAF}	Receive Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4) D_R0 or D_R1 = 0 dBm0 code. Minimum Gain < G_R < Maximum Gain				
		f = 200 Hz	−0.25		0.15	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 4000 Hz			−14	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels, hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE (Continued)						
G_{RAF} (Continued)		G_R = 4 dB, D_r0 = 0 dBm0 Code, G_X = 0 dBm0, VF_XI = 0 dBm. (Note 4)				
		f = 203.125 Hz	**−0.25**		**0.15**	dB
		f = 296.875 Hz	**−0.15**		**0.15**	dB
		f = 515.625 Hz	**−0.15**		**0.15**	dB
		f = 2796.875 Hz	**−0.15**		**0.15**	dB
		f = 3015.625 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.7**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
G_{RAL}	Receive Gain Variation with Signal Level	Sinusoidal Test Method. Reference Level = 0 dBm0.				
		D_r0 = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		D_r0 = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		D_r0 = −55 dBm0 to − 50 dBm0	**−1.2**		**1.2**	dB
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Tx Delay, Absolute	f = 1600 Hz			315	μs
D_{XR}	Tx Delay, Relative	f = 500–600 Hz			220	μs
		f = 600–800 Hz			145	μs
		f = 800–1000 Hz			75	μs
		f = 1000–1600 Hz			40	μs
		f = 1600–2600 Hz			75	μs
		f = 2600–2800 Hz			105	μs
		f = 2800–3000 Hz			155	μs
D_{RA}	Rx Delay, Absolute	f = 1600 Hz			200	μs
D_{RR}	Rx Delay, Relative	f = 500–1000 Hz	−40			μs
		f = 1000–1600 Hz	−30			μs
		f = 1600–2600 Hz			90	μs
		f = 2600–2800 Hz			125	μs
		f = 2800–3000 Hz			175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted, μ-law Selected	(Note 1) All '1's in Gain Register		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted, A-law Selected	(Note 1) All '1's in Gain Register		−74	**−67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted, μ-law Selected	PCM Code is Alternating Positive		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted, A-law Selected	PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 2)	**30**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 2)	**30**			dBC

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C, f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels, hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
NOISE (Continued)						
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz–4000 Hz	**30**			dBC
		f = 4 kHz–25 khz	**40**			dB
		f = 25 kHz–50 kHz	**36**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB} = −5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz–4000 Hz	**30**			dBC
		f = 4 kHz–25kHz	**40**			dB
		f = 25 kHz–50 kHz	**36**			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R0 (or D_R1)				
		4600 Hz–7600 Hz			**−30**	dB
		7600 Hz–8400 Hz			**−40**	dB
		8400 Hz–50,000 Hz			**−30**	dB
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel, μ-law Selected	Sinusoidal Test Method Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to − 30 dBm0	**36**			dBC
		= −40 dBm0 XMT	**29**			dBC
		RCV	**30**			dBC
		= −45 dBm0	**25**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Transmit or Receive Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Steady PCM Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz (Note 2)		−90	**−70**	dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0.

Note 2: $PPSR_x$, $NPSR_x$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_xI.

Note 3: A signal is Valid if it is above V_{IH} or below V_{IL} and Invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification the following conditions apply:

a) All input signals are defined as: V_{IL} = 0.4V, V_{IH} = 2.7V, t_R < 10 ns, t_F < 10 ns.

b) t_R is measured from V_{IL} to V_{IH}. t_F is measured from V_{IH} to V_{IL}.

c) Delay Times are measured from the input signal Valid to the output signal Valid.

d) Setup Times are measured from the data input Valid to the clock input Invalid.

e) Hold Times are measured from the clock signal Valid to the data input Invalid.

f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}.

Note 4: A multi-tone test technique is used.

National Semiconductor Corporation

microCMOS

TP3051/TP3056 Parallel Interface CODEC/Filter COMBO™

General Description

The TP3051, TP3056 family consists of a μ-law and A-law monolithic PCM CODEC/filter set utilizing the A/D and D/A conversion architecture shown in *Figure 1* and a parallel I/O data bus interface. The devices are fabricated on National's advanced microCMOS process.

The transmit section consists of an input gain adjust amplifier, an active RC pre-filter, and a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. A compressing coder samples the filtered signal and encodes it in the μ-255 law or A-law PCM format. Auto-zero circuitry is included on-chip. The receive section consists of an expanding decoder which reconstructs the analog signal from the compressed μ-law or A-law code, and a low pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The receive output is a single-ended power amplifier capable of driving low impedance loads. The TP3051 μ-law and TP3056 A-law devices are pin compatible parallel interface COMBOs for bus-oriented systems. They are ideally suited for use with the TP3100 family of digital line interface controllers (DLIC) in switching system applications. The DLIC communicates with the main switch controller via integrated data, signaling and control channels, and provides local time-slot and space switching capability for up to 32 TP3051 or TP3056 COMBOs.

Features

- Complete CODEC and filtering system including:
  - — Transmit high pass and low pass filtering
  - — Receive low pass filter with sin x/x correction
  - — Receive power amplifier
  - — Active RC noise filters
  - — μ-255 law COder and DECoder—TP3051
  - — A-law COder and DECoder—TP3056
  - — Internal precision voltage reference
  - — Internal auto-zero circuitry
- Meets or exceeds all LSSGR and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- High speed TRI-STATE® data bus
- 2 loopback test modes

Block Diagram

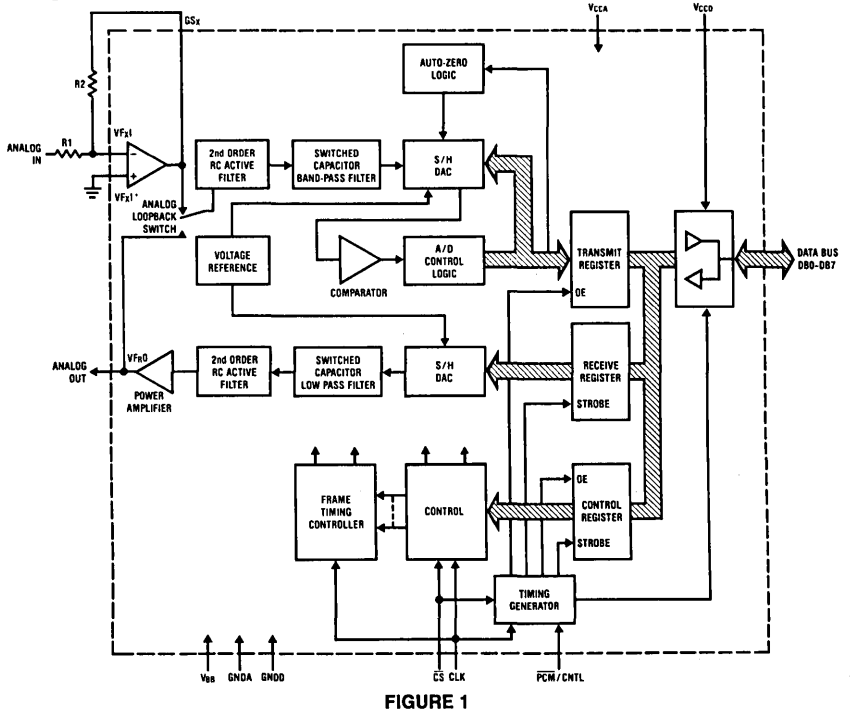

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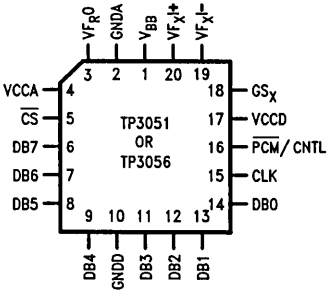
FIGURE 1

Connection Diagrams

Plastic Chip Carrier

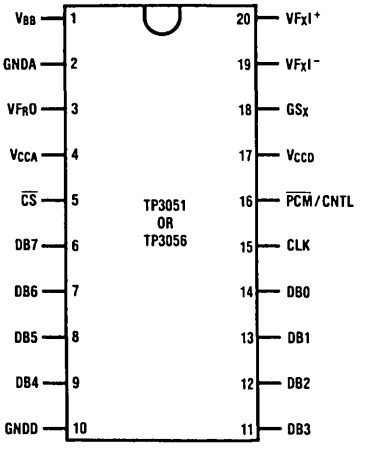


TL/H/8834-2

Top View

Order Number TP3051V or TP3056V
See NS Package Number V20P

Dual-In-Line Package



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Top View

Order Number TP3051J or TP3056J
See NS Package Number JH20

Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
GNDA	Analog ground. All analog signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier. This output can drive a 600Ω load to ±2.5V.
V_{CCA}	Positive power supply voltage pin for the analog circuitry. $V_{CCA} = 5V \pm 5\%$. Must be connected to V_{CCD}.
$\overline{CS}$	Device chip select input which controls READ, WRITE and TRI-STATE operations on the data bus. $\overline{CS}$ does not control the state of any analog functions.
DB7	Bit 7 I/O on the data bus. The PCM LSB.
DB6	Bit 6 I/O on the data bus.
DB5	Bit 5 I/O on the data bus.
DB4	Bit 4 I/O on the data bus.
GNDD	Digital ground. All digital signals are referenced to this pin.
DB3	Bit 3 I/O on the data bus.
DB2	Bit 2 I/O on the data bus.
DB1	Bit 1 I/O on the data bus.
DB0	Bit 0 I/O on the data bus. This is the PCM sign bit.
CLK	The clock input for the switched-capacitor filters and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the system clock input.
$\overline{PCM}$/CNTL	This control input determines whether the information on the data bus is PCM data or control data.
V_{CCD}	Positive power supply pin for the bus drivers. $V_{CCD} = 5V \pm 5\%$. Must be connected to V_{CCA}.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

CLOCK AND DATA BUS CONTROL

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table I and must be correctly selected by control bits C0 and C1.

CLK also functions as a READ/$\overline{WRITE}$ control signal, with the device reading the data bus on a positive half-clock cycle and writing the bus on a negative half-clock cycle, as shown in *Figures 4a* and *4b*.

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0–DB7, and receive power amplifier output, VF_RO, are in high impedance states.

The TP3051, TP3056 is powered-up via a command to the control register (see Control Register Functions). This sets

Functional Description (Continued)

the device in the standby mode with all circuitry activated, but encoding and decoding do not begin until PCM READ and PCM WRITE chip selects occur.

TABLE I. Control Bit Functions

Control Bits	Function
C0, C1	Select Clock Frequency **C0** **C1** **Frequency** 0 X 1.024 MHz 1 0 0.768 MHz or 0.772 MHz 1 1 1.28 MHz
C2, C3	Digital and Analog Loopback **C2** **C3** **Mode** 1 X digital loopback 0 1 analog loopback 0 0 normal
C4	Power-Down/Power-Up (Note 1) 1 = power-down 0 = power-up
C5	TP3051—Don't care (Note 1) TP3056 1 = A-law without even bit inversion 0 = A-law with even bit inversion
C6–C7	Don't Care (Note 1)

Note 1: These bits are always set to logical "1" when reading back the control register.

DATA BUS NOMENCLATURE

The normal order for serial PCM transmission is sign bit first, whereas the normal order for serial data is LSB first. For compatibility with the TP3110/TP3120 DLIC, the parallel data bus is defined as follows:

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

READING THE BUS

If CLK is low when $\overline{CS}$ goes low, bus data is gated in during the next positive half-clock cycle of CLK and latched on the negative-going transition. If $\overline{PCM}$/CNTL is low during the falling $\overline{CS}$ transition, then the bus data is defined as PCM voice data, which is latched into the receive register. This also functions as an internal receive frame synchronization pulse to start a decode cycle and must occur once per receive frame, i.e., at an 8 kHz rate.

If $\overline{PCM}$/CNTL is high during the falling $\overline{CS}$ transition, the bus data is latched into the control register. This does not affect frame synchronization.

WRITING THE BUS

If CLK is high when $\overline{CS}$ goes low, at the next falling transition of CLK, the bus drivers are enabled and either the PCM transmit data or the contents of the control register are gated onto the bus, depending on the level of $\overline{PCM}$/CNTL at the $\overline{CS}$ transition. If $\overline{PCM}$/CNTL is low during the $\overline{CS}$ falling transition, the transmit register data is written to the bus.

An internal transmit frame synchronization pulse is also generated to start an encode cycle, and this must occur once per transmit frame; i.e., at an 8 kHz rate.

If $\overline{PCM}$/CNTL is high during the $\overline{CS}$ falling transition, the control register data is written to the bus. This does not affect frame synchronization.

The receive register contents may also be written back to the bus, as described in the Digital Loopback section.

Except during a WRITE cycle, the bus drivers are in TRI-STATE mode.

CONTROL REGISTER FUNCTIONS

Writing to the control register allows the user to set the various operating states of the TP3051 and TP3056. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. CLK Select

   Since one of three distinct clock frequencies may be used, the actual frequency must be known by the device for proper operation of the switched-capacitor filters. This is achieved by writing control register bits C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

2. Digital Loopback

   In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in the TP3051 or TP3056 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back onto the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination at VF_RO.

3. Analog Loopback

   In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is entered by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.

4. Power-Down/Power-Up

   The TP3051 or TP3056 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, setting bit C4 to 0 powers-up the device.

TRANSMIT FILTER AND ENCODE SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 2*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2nd order RC active pre-filter, followed by an 8th order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-255 law (TP3051) or A-law (TP3056) coding schemes. A precision voltage reference is trimmed in manufacturing

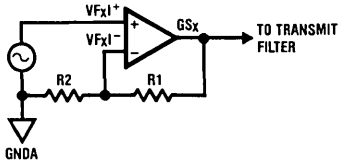
Functional Description (Continued)

to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

The total encoding delay referenced to a PCM WRITE chip select will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs.

DECODER AND RECEIVE FILTER SECTION

The receive section consists of an expanding DAC which drives a 5th order switched-capacitor low pass filter clocked at 256 kHz. The decoder is of A-law (TP3056) or μ-law (TP3051) coding law and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter. The power amplifier output stage is capable of driving a 600Ω load to a level of 7.2 dBm. See *Figure 3*. The receive section has unity-gain. Following a PCM READ chip select, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.



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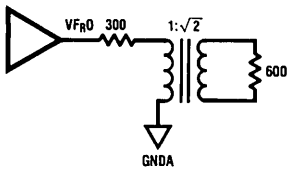
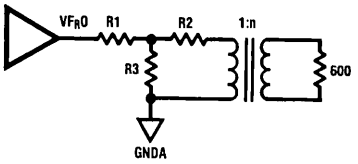
Non-inverting transmit gain = $20 \log_{10} \left(\frac{R1 + R2}{R2} \right)$

Set gain to provide peak overload level = t_{MAX} at GS_X (see Transmission Characteristics)

FIGURE 2. Transmit Gain Adjustment



Maximum output power = 7.2 dBm total, 4.2 dBm to the load.



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See Applications information for attenuator design guide.

FIGURE 3. Receive Gain Adjustment

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

GNDD to GNDA	±0.3V
V_{CCA} or V_{CCD} to GNDD or GNDA	7V
V_{BB} to GNDD or GNDA	−7V
Voltage at Any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at Any Digital Input or Output	V_{CC} + 0.3V to GNDD − 0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Electrical Characteristics

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, T_A = 0°C to 70°C; typical characteristics specified at nominal supply voltages, T_A = 25°C; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; T_A = 0°C to 70°C by correlation with 100% Electrical testing at T_A = 25°C. All other limits are assured by correlation with other production test and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	DB0–DB7, I_L = 2.5 mA			**0.4**	V
V_{OH}	Output High Voltage	DB0–DB7, I_H = −2.5 mA	**2.4**			V
I_{IL}	Input Low Current	GNDD ≤ V_{IN} ≤ V_{IL}	**−3**		**3**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−3**		**3**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	DB0–DB7, GNDD ≤ V_O ≤ V_{CC}	**−3**		**3**	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER						
I_IXA	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance, GS_X	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance, GS_X		10			kΩ
C_LXA	Load Capacitance, GS_X				50	pF
V_OXA	Output Dynamic Range, GS_X	R_L = 10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	**−2.5**		**2.5**	V
CMRRXA	Common-Mode Rejection Ratio	D.C. Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	D.C. Test	**60**			dB
RECEIVE POWER AMPLIFIER						
R_ORF	Output Resistance, VF_RO			1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	**600**			Ω
C_LRF	Load Capacitance				50	pF
VOS_RO	Output DC Offset Voltage		**−200**		**200**	mV
POWER DISSIPATION						
I_{CC0}	Power-Down Current	No Load		0.5	**1.5**	mA
I_{BB0}	Power-Down Current	No Load		0.05	**0.3**	mA
I_{CC1}	Active Current	No Load		6.0	**9.0**	mA
I_{BB1}	Active Current	No Load		6.0	**9.0**	mA

Timing Specifications

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, $T_A = 0°C$ to 70°C; typical characteristics specified at nominal supply voltages, $T_A = 25°C$; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to 70°C by correlation with 100% Electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production test and/or product design and characteristics. All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$. See Definitions and Timing Conventions section for test method information.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock		760		ns
t_{WCH}	Width of Clock High		**330**		ns
t_{WCL}	Width of Clock Low		330		ns
t_{RC}	Rise Time of Clock			50	ns
t_{FC}	Fall Time of Clock			50	ns
t_{HCCS}	Hold Time from CLK to $\overline{CS}$ Low		**100**		ns
t_{SCLC}	Set-Up Time of $\overline{CS}$ Low to CLK		**100**		ns
t_{SCHC}	Set-Up Time from $\overline{CS}$ High to Second CLK Edge		**0**		ns
t_{WCS}	Width of Chip Select		**100**		ns
t_{SPCM}	Set-Up Time of $\overline{PCM}$/CNTL to $\overline{CS}$		**0**		ns
t_{HPCM}	Hold Time from $\overline{CS}$ to $\overline{PCM}$/CNTL		**100**		ns
t_{SDC}	Set-Up Time of Data In to CLK		**50**		ns
t_{HCD}	Hold Time from CLK to Data In		20		ns
t_{DDO}	Delay Time to Data Out Valid	$C_L = 0$ pF to 200 pF	**90**	**260**	ns
t_{DDZ}	Delay Time to Data Output Disabled	$C_L = 0$ pF to 200 pF	20	80	ns

Switching Time Waveforms

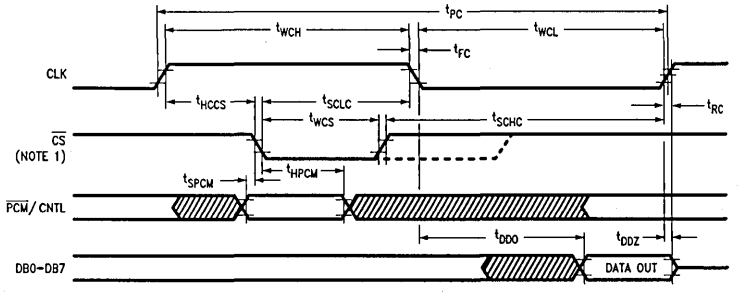

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FIGURE 4a. Timing Waveforms for COMBO Writing to the Bus

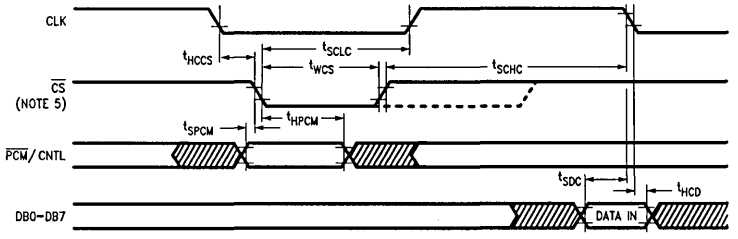

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FIGURE 4b. Timing Waveforms for COMBO Reading from the Bus

Note 5: READ and WRITE $\overline{CS}$ pulses must each occur at an 8 kHz rate, and may occur on consecutive half-cycles of CLK if required, although this is not a restriction.

Transmission Characteristics

Unless otherwise specified: T_A = 0°C to +70°C, V_{CCA} = V_{CCD} = 5V ±5%, V_{BB} = −5V ±5%, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for V_{CCA} = V_{CCD} = 5.0V ±5% and V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω)				
	0 dBm0	TP3051 TP3056		1.2276 1.2276		Vrms Vrms
t_{MAX}	Maximum Overload Level	TP3051 (+3.17 dBm0) TP3056 (+3.14 dBm0)		2.501 2.492		V_{DC} V_{DC}
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, V_{CCA} = V_{CCD} = 5.0V, V_{BB} = −5.0V Input at GS_X = 0 dBm0 at 1020 Hz	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz–3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−1.8** **−0.15** **−0.35** **−0.7** 	 	−40 −30 **−26** **−0.1** **0.15** **0.1** **0** **−14** **−32**	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variation with Level	Sinusoidal Method Reference Level = −10 dBm0 VF_XI^+ = −40 dBm0 to +3 dBm0 VF_XI^+ = −50 dBm0 to −40 dBm0 VF_XI^+ = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**	 	 **0.2** **0.4** **1.2**	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A = 25°C, V_{CCA} = V_{CCD} = 5V, V_{BB} = −5V Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	**−0.15**		**0.15**	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	**−0.15** **−0.35** **−0.7** 	 	**0.15** **0.05** **0** **−14**	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variation with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded −10 dBm0 Signal PCM Level = −40 dBm0 to +3 dBm0 PCM Level = −50 dBm0 to −40 dBm0 PCM Level = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**	 	 **0.2** **0.4** **1.2**	 dB dB dB
V_{RO}	Receive Output Drive Level	R_L = 600Ω	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise specified: T_A = 0°C to +70°C, V_{CCA} = V_{CCD} = 5V ±5%, V_{BB} = −5V ±5%, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for V_{CCA} = V_{CCD} = 5.0V ±5% and V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	μs
		f = 600 Hz–800 Hz		120	145	μs
		f = 800 Hz–1000 Hz		50	75	μs
		f = 1000 Hz–1600 Hz		20	40	μs
		f = 1600 Hz–2600 Hz		55	75	μs
		f = 2600 Hz–2800 Hz		80	105	μs
		f = 2800 Hz–3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		μs
		f = 1000 Hz–1600 Hz	−30	−20		μs
		f = 1600 Hz–2600 Hz		70	90	μs
		f = 2600 Hz–2800 Hz		100	125	μs
		f = 2800 Hz–3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3051, (Note 2)		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3056, VF_XI^+ = 0V (Note 2)		−74	**−69**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3051, PCM Code Equals Alternating Positive and Negative Zero		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3056, PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0V			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI^+ = 0V, V_{CCA} = V_{CCD} = 5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 3)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI^+ = 0 Vrms, V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 3)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3051 and TP3056 V_{CC} = 5.0 V_{DC} + 100 mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dBC
		f = 25 kHz–50 kHz	**36**			dBC
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3051 and TP3056 V_{BB} = −5.0 V_{DC} + 100 mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dBC
		f = 25 kHz–50 kHz	**36**			dBC
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz–3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO				
		4600 Hz–7600 Hz			**−32**	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			**−32**	dB

Transmission Characteristics (Continued)

Unless otherwise specified: T_A = 0°C to +70°C, V_{CCA} = V_{CCD} = 5V ±5%, V_{BB} = −5V ±5%, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for V_{CCA} = V_{CCD} = 5.0V ±5% and V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 4) Level = 3.0 dBm0 = 0 dBm0 to −30 dBm0 = −40 dBm0 XMT RCV = −55 dBm0 XMT RCV	 **33** **36** **29** **30** **14** **15**			 dB dB dB dB dB dB
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz at 0 dBm0 Transmit Level Steady PCM Receive Code		−90	**−70**	dB
CT_{R-X}	Receive to Transmit Crosstalk 0 dBm0 Receive Level	f = 300 Hz–3400 Hz at 0 dBm0 (Note 3)		−90	**−70**	dB

Note 2: Measured by extrapolation from the distortion test result.

Note 3: CT_{R-X}, $PPSR_X$, and $NPSR_X$ are measured with a −50 dBm0 activation signal applied at VF_XI^+.

Note 4: Using C message weighted filter.

Encoding Format at Data Bus Output

	TP3051 μ-Law								TP3056 True A-Law, C5 = 0 (Includes Even Bit Inversion)							
	MSB							LSB	MSB							LSB
V_{IN} = + Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
V_{IN} = − Full-Scale	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0
	Not Applicable (C5 is Don't Care)								**Sign + Magnitude A-Law, C5 = 1 (Before Even Bit Inversion)**							
V_{IN} = + Full-Scale									1	1	1	1	1	1	1	1
V_{IN} = 0V									1	0	0	0	0	0	0	0
									0	0	0	0	0	0	0	0
V_{IN} = − Full-Scale									0	1	1	1	1	1	1	1

Applications Information

POWER SUPPLIES

While the pins of the TP3051/6 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used. GNDA and GNDD MUST be connected together adjacent to each COMBO not on the connector or backplane wiring.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CCA} and V_{BB}.

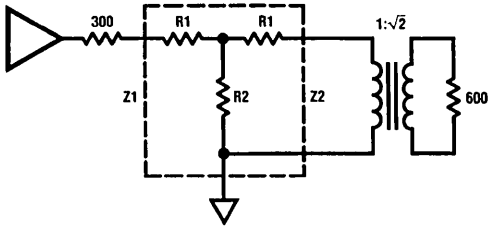
For best performance, the ground point of each COMBO on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

The positive power supply to the bus drivers, V_{CCD}, is provided on a separate pin from the positive supply for the CODEC and filter circuits to minimize noise injection when driving the bus. V_{CCA} and V_{CCD} MUST be connected together close to the CODEC/filter at the point where the 0.1 μF decoupling capacitor is connected.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family COMBO receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. (See *Figure 5.*) Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closer practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



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$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

Where: $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

and

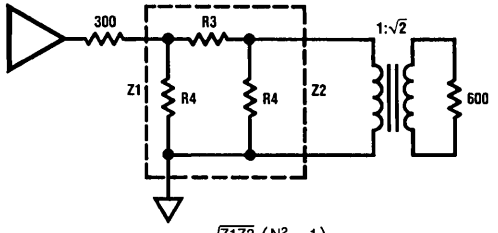
$$S = \sqrt{\frac{Z1}{Z2}}$$

Also: $Z = \sqrt{Z_{SC}\,Z_{OC}}$

Where Z_{SC} = Impedance with short circuit termination

and Z_{OC} = Impedance with open circuit termination

π-Pad Attenuator



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$$R3 = \sqrt{\frac{Z1Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R4 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

FIGURE 5. T-Pad and π-Pad Attenuator Models

TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Note: See Application Note 370 for further details.

Typical Applications

The benefits of a COMBO with a parallel data bus, rather than the usual serial port, are illustrated in *Figure 6*. This shows a 16-channel line card in which the TP3051 or TP3056 share the data bus interface to a TP3110 family Digital Line Interface Controller. The DLIC can access up to 128 channels on the serial backplane, providing fully non-blocking time and space switching capability with optional redundancy. In conjunction with a local microprocessor, typically from the INS8048 family, a standard HDLC control channel can be assigned, providing secure message capability between the line card and the system control processor. The local microprocessor can also collect and process line status and signaling information, off-loading these tasks from the main processor. A prioritized vectored interrupt scheme is used for data transfers between the microprocessor and DLIC.

System flexibility can be further enhanced by adding 2 additional bits per frame to the PCM data, operating the DLIC with 80k b/s channels rather than 64k b/s channels.

Another application of the TP3051 or TP3056 is in the all-digital telephone. The analog and digital loopback test modes are particularly useful, enabling the switching system to verify the integrity of virtually the complete channel. The transmit op amp can be set for gains in excess of 20 dB, enabling a simple AC connection to an electret microphone (with integral FET buffer) to be made. A receive transducer with an impedance no less than 600Ω can be driven directly by the receive amplifier, with a resistive network providing gain adjustment and sidetone. Low impedance transducers require an audio matching transformer.

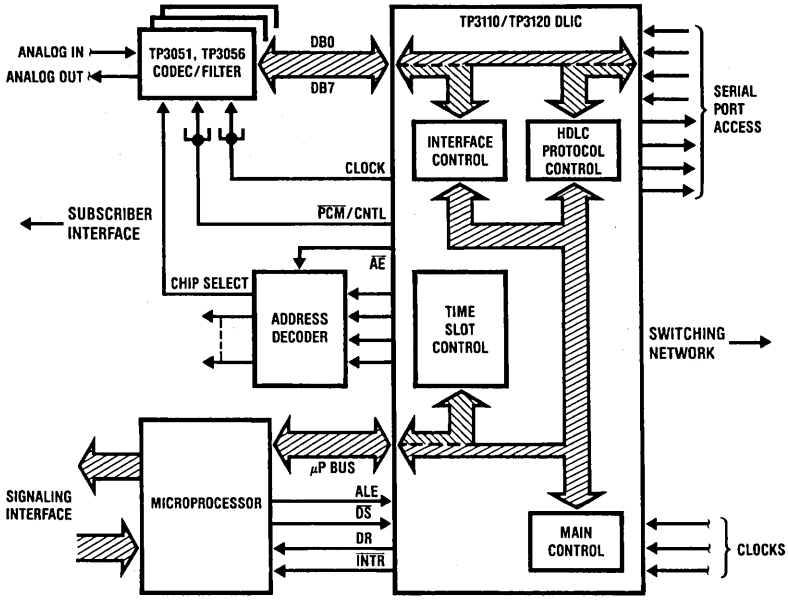

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FIGURE 6. Typical 16-Channel Line Card using TP3110/TP3120 Digital Line Interface Controller (DLIC)

National Semiconductor Corporation

PRELIMINARY

microCMOS

TP3058/TP3059 Microprocessor Compatible COMBO™

General Description

The TP3058, TP3059 family consists of a μ-law and A-law monolithic PCM COMBO set utilizing the A/D and D/A conversion architecture shown in *Figure 1* and a parallel I/O microprocessor bus interface. The devices are fabricated on National's advanced microCMOS process.

The transmit section consists of an input gain adjust amplifier, an active RC pre-filter, and a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. A compressing coder samples the filtered signal and encodes it in the μ-225 law or A-law PCM format. Auto-zero circuitry is included on-chip. The receive section consists of an expanding decoder which reconstructs the analog signal from the compressed μ-law or A-law code, and a low pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The receive output is a single-ended power amplifier capable of driving low impedance loads.

The TP3058 μ-law and TP3059 A-law devices are pin compatible parallel interface CODEC/filters for microprocessor and digital signal processor systems.

Features

- Complete CODEC and filtering system including:
  - — Transmit high pass and low pass filtering
  - — Receive low pass filter with sin x/x correction
  - — Receive power amplifier
  - — Active RC noise filters
  - — μ-255 law COder and DECoder—TP3058
  - — A-law COder and DECoder—TP3059
  - — Internal precision voltage reference
  - — Internal auto-zero circuitry
- Meets or exceeds all LSSGR and CCITT specifications
- Microprocessor interface independant of frame sync
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- 2 loopback test modes

Block Diagram

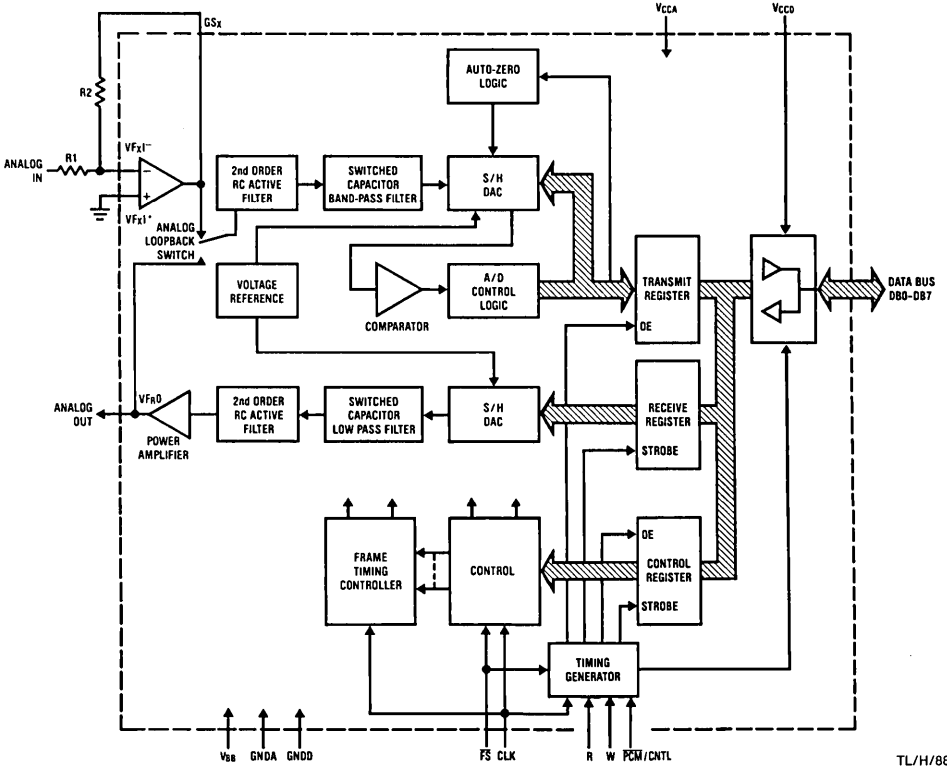

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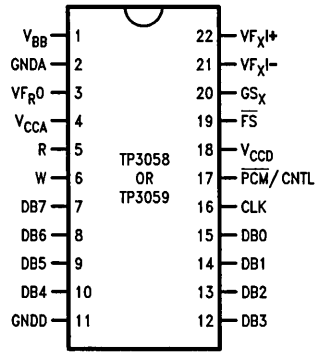
FIGURE 1

Connection Diagram

Dual-In-Line Package



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Top View

Order Number TP3058J or TP3059J
See NS Package Number J22A

Pin Descriptions

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$
GNDA	Analog ground. All analog signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier. This output can drive a 600Ω load to ±2.5V.
V_{CCA}	Positive power supply voltage pin for the analog circuitry. $V_{CCA} = 5V \pm 5\%$. Must be connected to V_{CCD}.
DB7	Bit 7 I/O on the data bus. The PCM LSB.
DB6	Bit 6 I/O on the data bus.
DB5	Bit 5 I/O on the data bus
DB4	Bit 4 I/O on the data bus.
GNDD	Digital ground. All digital signals are referenced to this pin.
DB3	Bit 3 I/O on the data bus.
DB2	Bit 2 I/O on the data bus.
DB1	Bit 1 I/O on the data bus.
DB0	Bit 0 I/O on the data bus. This is the PCM sign bit.

Symbol	Function
CLK	The clock input for the switched-capacitor filters and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the system clock input.
$\overline{FS}$	Frame sync input, which starts a new Encode and Decode cycle. Must occur at an 8 kHz rate to meet CCITT and LSSGR specifications.
R	Input from the Microprocessor READ signal, which enables the COMBO bus drivers. May be asynchronous with $\overline{FS}$.
W	Input from the Microprocessor WRITE signal, which enables the COMBO bus receivers. May be asynchronous with $\overline{FS}$.
$\overline{PCM}$/ CNTL	This control input determines whether the information on the data bus is PCM data or control data.
V_{CCD}	Positive power supply pin for the bus drivers. $V_{CCD} = 5V \pm 5\%$. Must be connected to V_{CCA}.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0–DB7, and receive power amplifier output, VF_RO, are in high impedance states.

The TP3058 and TP3059 are powered-up via a command to the control register (see Control Register Functions). This sets the device in the standby mode with all circuitry activated, but encoding and decoding do not begin until PCM READ and PCM WRITE chip selects occur.

TABLE I. Control Bit Functions

Control Bits	Function
C0, C1	Select Clock Frequency **C0 C1 Frequency** 0 X 1.024 MHz 1 0 0.768 MHz or 0.772 MHz 1 1 1.28 MHz
C2, C3	Digital and Analog Loopback **C2 C3 Mode** 1 X digital loopback 0 1 analog loopback 0 0 normal
C4	Power-Down/Power-Up 1 = power-down 0 = power-up
C5	TP3058—Don't care (Note 1) TP3059 1 = A-law without even bit inversion 0 = A-law with even bit inversion
C6–C7	Don't Care (Note 1)

Note 1: These bits are always set to "1" when reading back the control register.

DATA BUS NOMENCLATURE

The order of the data bus is as follows:

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

MICROPROCESSOR WRITING THE BUS

The microprocessor may write to either the Control Register or PCM Receive Register by first setting up the $\overline{PCM}$/CNTL address bit during a WRITE cycle. A CNTL WRITE may take place at any time without restriction, during either the powered-up or powered-down state.

A PCM WRITE cycle normally occurs once per frame, and may occur any time in the frame except during the $\overline{FS}$ falling edge. PCM data is held in a register and will not update the DAC until the next $\overline{FS}$ pulse starts a new decoding cycle.

MICROPROCESSOR READING THE BUS

The microprocessor may read either the Control Register, to verify the status of the device, or the PCM Transmit Register. Selection is again by means of the $\overline{PCM}$/CNTL address input. A CNTL READ may take place at any time without restriction, during either the powered-up or powered-down state. A PCM READ cycle normally occurs once per frame, and may occur any time in the frame except during the $\overline{FS}$ falling edge.

COMBO TIMING

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table I and must be correctly selected by control bits C0 and C1. $\overline{FS}$ is a sync input which starts both the Encode and Decode cycles. It must be an integer sub-multiple of CLK, and must occur at an 8 kHz rate to meet CCITT and LSSGR transmission specifications. Timing functions in the COMBO are not synchronized to timing on the data bus, however.

CONTROL REGISTER FUNCTIONS

Writing to the control register (see Table I) allows the user to set the various operating states of the TP3058 and TP3059. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. CLK Select

   Since one of three distinct clock frequencies may be used, the actual frequency must be known by the device for proper operation of the switched-capacitor filters. This is achieved by writing control register bits C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

2. Digital Lookback

   In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in the TP3058 and TP3059 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back onto the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination at VF_RO.

3. Analog Loopback

   In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is entered by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.

4. Power-Down/Power-Up

   The TP3058, TP3059 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, settng bit C4 to 0 powers-up the device.

Functional Description (Continued)

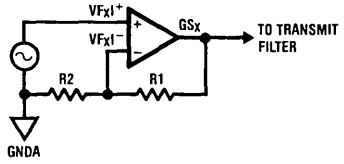
TRANSMIT FILTER AND ENCODE SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 2*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2nd order RC active pre-filter, followed by an 8th order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-255 law (TP3058) or A-law (TP3059) coding schemes. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

The total encoding delay referenced to a frame sync input select will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs.

TRANSMIT GAIN ADJUSTMENT

Figure 2 shows the connections for setting the Transmit input amplifier in non-inverting mode. Gains in excess of 20 dB can be obtained with this amplifier without significantly impairing the transmission performance of the device.



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$$\text{Non-inverting transmit gain} = 20 \log_{10}\left(\frac{R1 + R2}{R2}\right)$$

Set gain to provide peak overload level = t_{MAX} at GS_X (see Transmission Characteristics)

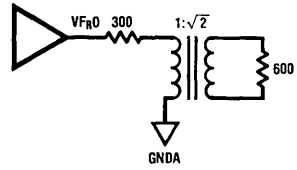
FIGURE 2. Transmit Gain Adjustment

DECODER AND RECEIVE FILTER SECTION

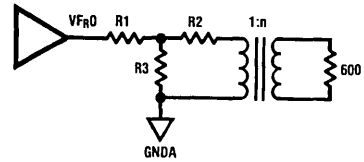
The receive section consists of an expanding DAC which drives a 5th order switched-capacitor low pass filter clocked at 256 kHz. The decoder is of A-law (TP3059) or μ-law (TP3058) coding law and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter. The power amplifier output stage is capable of driving a 600Ω load to a level of 7.2 dBm. The receive section has unity-gain. Each decoding cycle begins just prior to a $\overline{FS}$ pulse. The total decoder delay is 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 170 μs, relative to the $\overline{FS}$ pulse following the microprocessor PCM WRITE cycle.

RECEIVE GAIN ADJUSTMENT

Receive gain adjustments with a high impedance load can be implemented with a simple 2-resistor potentiometer. Gain adjustments requiring matching to a transformer should use the equations given in the Applications section.



Maximum output power = 7.2 dBm total, 4.2 dBm to the load.



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See Applications information for attenuator design guide.

FIGURE 3. Receive Gain Adjustment

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

GNDD to GNDA	±0.3V
V_{CCA} or V_{CCD} to GNDD or GNDA	7V
V_{BB} to GNDD or GNDA	−7V
Voltage at Any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at Any Digital Input or Output	V_{CC} + 0.3V to GNDD − 0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Electrical Characteristics

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, T_A = 0°C to 70°C; typical characteristics specified at nominal supply voltages, T_A = 25°C; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design characterizations.

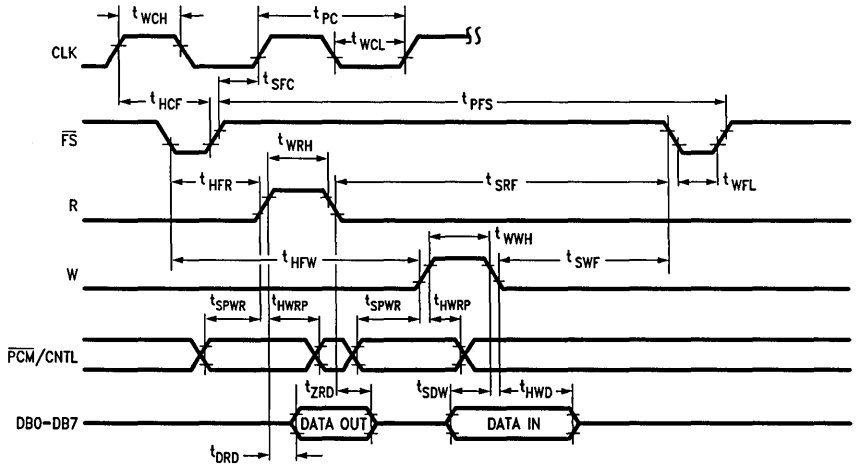
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	DB0–DB7, I_L = 2.5 mA			**0.4**	V
V_{OH}	Output High Voltage	DB0–DB7, I_H = 2.5 mA	**2.4**			V
I_{IL}	Input Low Current	GNDD ≤ V_{IN} ≤ V_{IL}	**−3**		**3**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−3**		**3**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE®)	DB0–DB7, GNDD ≤ V_O ≤ V_{CC}	**−3**		**3**	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER						
I_IXA	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance, GS_X	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance, GS_X		10			kΩ
C_LXA	Load Capacitance, GS_X				50	pF
V_OXA	Output Dynamic Range, GS_X	R_L = 10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	**−2.5**		**2.5**	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	**60**			dB
RECEIVE POWER AMPLIFIER						
R_ORF	Output Resistance, VF_RO			1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	**600**			Ω
C_LRF	Load Capacitance				50	pF
VOS_RO	Output DC Offset Voltage		**−200**		**200**	mV
POWER DISSIPATION						
I_{CC0}	Power-Down Current	No Load		0.5	**1.5**	mA
I_{BB0}	Power-Down Current	No Load		0.05	**0.3**	mA
I_{CC1}	Active Current	No Load		6.0	**9.0**	mA
I_{BB1}	Active Current	No Load		6.0	**9.0**	mA

Timing Specifications

Unless otherwise noted, $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, GNDA = 0V, $T_A = 0°C$ to $70°C$; typical characteristics specified at $V_{CCA} = V_{CCD} = 5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$; all signals are referenced to GNDA. Timing specifications are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design characterizations. See Definitions and Timing Conventions for test methods information.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock		760		ns
t_{WCH}	Width of Clock High		**330**		ns
t_{WCL}	Width of Clock Low		330		ns
t_{RC}	Rise Time of Clock			50	ns
t_{FC}	Fall Time of Clock			50	ns
t_{WFL}	Width of $\overline{FS}$ Low		200	 100	ns μs
t_{HFR}	Hold Time, $\overline{FS}$ Low to R	PCM READ Only	100		ns
t_{SRF}	Set-Up Time, R Low to $\overline{FS}$	PCM READ Only	100		ns
t_{HFW}	Hold Time, $\overline{FS}$ Low to W	PCM WRITE Only	100		ns
t_{SWF}	Set-Up Time, W Low to $\overline{FS}$	PCM WRITE Only	100		ns
t_{WRH}	Width of R High		75		ns
t_{WWH}	Width of W High		125		ns
t_{DRD}	Delay Time, R to Data Valid	$C_L = 100$ pF		65	ns
t_{ZRD}	Float Delay, R Low to DB High-Z		0	80	ns
t_{SDW}	Set-Up Time, DB to W Low		75		ns
t_{HWD}	Hold Time, W Low to DB		25		ns
t_{SPWR}	Set-Up Time, $\overline{PCM}$/CNTL to R or W		**20**		ns
t_{HWRP}	Hold-Time, W or R to $\overline{PCM}$/CNTL		100		ns
t_{HCF}	Hold-Time, $\overline{FS}$ Low after CLK High		100		ns
t_{SFC}	Set-Up Time, $\overline{FS}$ High to CLK High		100		ns
t_{PFS}	Period of $\overline{FS}$ (Note 5)	CLK = 1.024 MHz	70		μs

Timing Diagram



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Transmission Characteristics

Unless otherwise specified: $T_A = 0°C$ to 70°C, $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to 70°C by correlation with 100% testing at $T_A = 25°C$. All other limits are assured by correlation with production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω)				
	0 dBm0	TP3058		1.2276		Vrms
		TP3059		1.2276		Vrms
t_{MAX}	Maximum Overload Level	TP3058 (+3.17 dBm0)		2.501		V_{DC}
		TP3059 (+3.14 dBm0)		2.492		V_{DC}
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V_{CCA} = V_{CCD} = 5.0V$, $V_{BB} = -5.0V$ Input at GS_X = 0 dBm0 at 1020 Hz	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz			−40	dB
		f = 50 Hz			−30	dB
		f = 60 Hz			**−26**	dB
		f = 200 Hz	**−1.8**		**−0.1**	dB
		f = 300 Hz–3000 Hz	**−0.15**		**0.15**	dB
		f = 3300 Hz	**−0.35**		**0.1**	dB
		f = 3400 Hz	**−0.7**		**0**	dB
		f = 4000 Hz			**−14**	dB
		f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz			**−32**	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variation with Level	Sinusoidal Test Method				
		Reference Level = −10 dBm0				
		VF_XI^+ = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		VF_XI^+ = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		VF_XI^+ = −55 dBm0 to −50 dBm0	**1.2**		**1.2**	dB
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V_{CCA} = V_{CCD} = 5V$, $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	**−0.15**		**0.15**	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz	**−0.15**		**0.15**	dB
		f = 3300 Hz	**−0.35**		**0.05**	dB
		f = 3400 Hz	**−0.7**		**0**	dB
		f = 4000 Hz			**−14**	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variation with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded				
		PCM Level = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		= −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		= −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
V_{RO}	Receive Output Drive Level	R_L = 600Ω	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise specified: $T_A = 0°C$ to 70°C, $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; T_A = 0°C to 70°C by correlation with 100% testing at T_A = 25°C. All other limits are assured by correlation with production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	μs
		f = 600 Hz–800 Hz		120	145	μs
		f = 800 Hz–1000 Hz		50	75	μs
		f = 1000 Hz–1600 Hz		20	40	μs
		f = 1600 Hz–2600 Hz		55	75	μs
		f = 2600 Hz–2800 Hz		80	105	μs
		f = 2800 Hz–3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		μs
		f = 1000 Hz–1600 Hz	−30	−20		μs
		f = 1600 Hz–2600 Hz		70	90	μs
		f = 2600 Hz–2800 Hz		100	125	μs
		f = 2800 Hz–3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3058, (Note 2)		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3059, (Note 2)		−74	**−69**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3058, PCM Code Equals Alternating Positive and Negative Zero		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3059, PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0V$			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$V_{CCA} = V_{CCD} = 5.0\ V_{DC} + 100$ mVrms f = 0 kHz–50 kHz (Note 3)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	$V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 kHz–50 kHz (Note 3)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3058 and TP3059 $V_{CC} = 5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dBC
		f = 25 kHz–50 kHz	**36**			dBC
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3058 and TP3059 $V_{BB} = -5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dBC
		f = 25 kHz–50 kHz	**36**			dBC
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz–3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO				
		4600 Hz–7600 Hz			**−32**	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			**−32**	dB

Transmission Characteristics (Continued)

(All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for $V_{CC} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% testing at $T_A = 25°C$. All other limits are assured by correlation with production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 4) Level = 3.0 dBm0 = 0 dBm0 to −30 dBm0 = −40 dBm0 XMT RCV = −55 dBm0 XMT RCV	 **33** **36** **29** **30** **14** **15**			 dB dB dB dB dB dB
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk 0 dBm0 Transmit Level	f = 300 Hz–3000 Hz at 0 dBm0 Transmission Level Steady PCM Receive Code		−90	**−70**	dB
CT_{R-X}	Receive to Transmit Crosstalk 0 dBm0 Receive Level	f = 300 Hz–3000 Hz at 0dBm0 Transmit Level (Note 3)		−90	**−70**	dB

Note 2: Measured by extrapolation from the distortion test result.

Note 3: CT_{R-X}, $PPSR_X$, and $NPSR_X$ are measured with a −50 dBm0 activation signal applied at VF_XI^+.

Note 4: Using C message weighted filter.

Note 5: Must be 125 μs to meet CCITT and LSSGR specifications.

Encoding Format At Data Bus Output

	TP3058 μ-Law								TP3059 True A-Law, C5 = 0 (Includes Even Bit Inversion)							
	MSB							LSB	MSB							LSB
V_{IN} = + Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = − Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0
	Not Applicable (C5 is Don't Care)								Sign + Magnitude A-Law, C5 = 1 (Before Even Bit Inversion)							
V_{IN} = + Full-Scale									1	1	1	1	1	1	1	1
V_{IN} = 0V									1	0	0	0	0	0	0	0
									0	0	0	0	0	0	0	0
V_{IN} = − Full-Scale									0	1	1	1	1	1	1	1

Applications Information

POWER SUPPLIES

While the pins of the TP3058/9 family are well protected against electrical misuse, however, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used. GNDA and GNDD MUST be connected together adjacent to each COMBO, not on the connector or backplane wiring.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CCA} and V_{BB}.

For best performance, the ground point of each COMBO on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

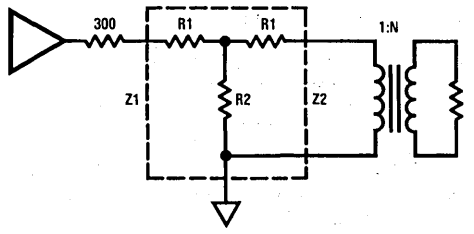
The positive power supply to the bus drivers, V_{CCD}, is provided on a separate pin from the positive supply for the COMBO circuits to minimize noise injection when driving the bus. V_{CCA} and V_{CCD} MUST be connected together close to the COMBO at the point where the 0.1 μF decoupling capacitor is connected.

Application Note AN370 provides further guidance on board layout techniques.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output as shown in *Figure 4*. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



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$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

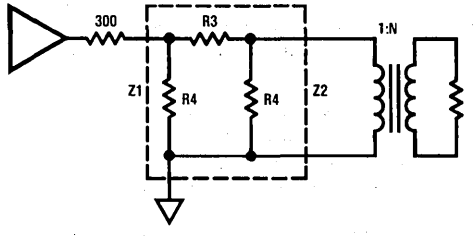
$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{SC}\,Z_{OC}}$$

Where Z_{SC} = Impedance with short circuit termination

and Z_{OC} = Impedance with open circuit termination

π-Pad Attenuator



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$$R3 = \sqrt{\frac{Z1Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R4 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

FIGURE 4. Receive Gain Adjustment for Matched Loads

Applications Information (Continued)

TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900

TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω (All Values in Ω) (Continued)

dB	R1	R2	R3	R4
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Application

Figure 5 shows a typical application of the TP3058/9 with a microprocessor having non-multiplexed address and data ports. The COMBO clocks, CLK and $\overline{FS}$, are derived from a crystal-controlled counter chain. The 8 kHz $\overline{FS}$ signal is also used as an Interrupt to the processor, prompting it to generate a PCM READ and PCM WRITE cycle sometime during the next frame period.

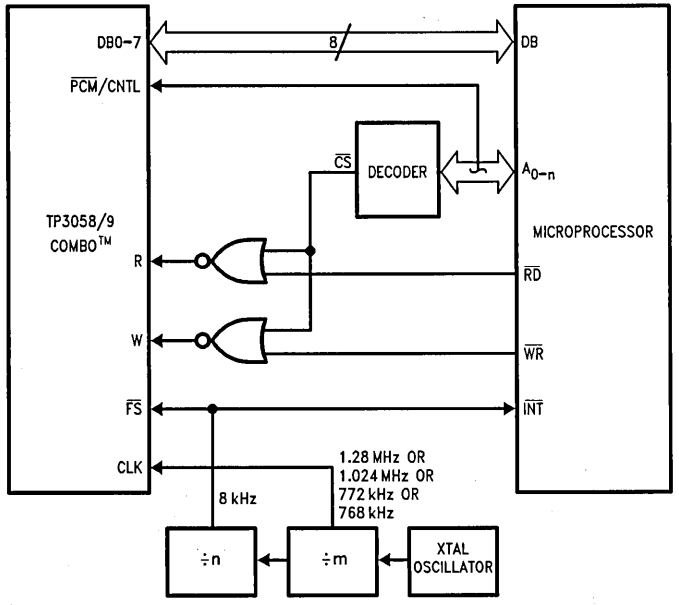

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FIGURE 5. Typical Application

National Semiconductor Corporation

microCMOS

TP3052/TP3052-1/TP3053/TP3053-1 TP3054/TP3054-1/TP3057/TP3057-1 Serial Interface CODEC/FILTER COMBO™ Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

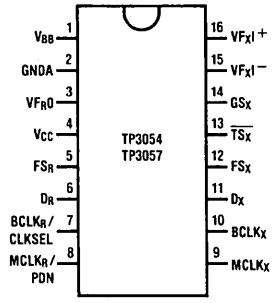
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- Complete CODEC and filtering system (COMBO) including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
- μ-law with signaling, TP3020 or TP5116A timing—TP3052
- μ-law with signaling, TP5116A family timing—TP3053
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density
- Dual-In-Line on PCC surface mount packages

Connection Diagrams (Continued on Page 15)

Dual-In-Line Package



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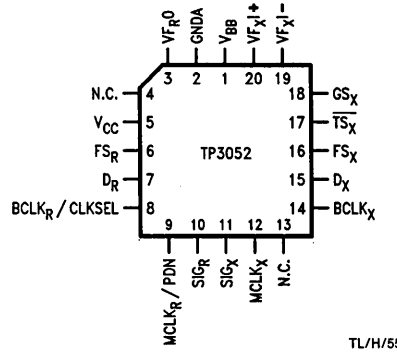
Top View

Order Number TP3054J, TP3054J-1, TP3057J or TP3057J-1
See NS Package Number J16A

Plastic Chip Carriers



TL/H/5510–10

Top View

Order Number TP3052V or TP3052V-1
See NS Package Number V20A

Block Diagram

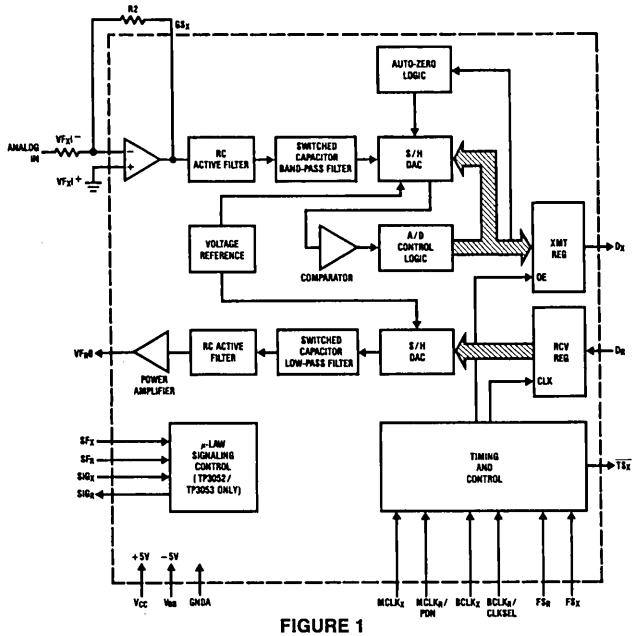


FIGURE 1 TL/H/5510–2

Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
GNDA	Analog ground. All signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1).
$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
SF_R	When high during FS_R, this input indicates a receive signal frame.
SIG_R	The eighth bit of the PCM data appears at this output after each receive signalling frame.
SIG_X	Signal data input. Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
SF_X	When high during FS_X, this input indicates a transmit signaling frame.
$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into a power-down state. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3057	TP3052 TP3053 TP3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3052, 53, 54, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the TP5116A/56A long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

SIGNALING

The TP3052 and TP3053 μ-law COMBOs contain circuitry to insert and extract signaling information in the PCM data stream. The TP3052 is intended for short frame sync applications, and the TP3053 for long frame sync applications, although the TP3053 may also be used in short frame sync applications. The TP3054 and TP3057 have no provision for signaling.

Functional Description (Continued)

Signaling for the TP3052 is accomplished by applying a frame sync pulse two bit clock periods long, as shown in *Figure 2*. With FS_X two bit clock periods long, the data present at SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With FS_R two bit clock periods long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as "½" to minimize noise and distortion. This short frame signaling may also be implemented using the TP3053, providing SF_R and SF_X are left open circuit or tied low. The TP3052 is not capable of inserting or extracting signaling information in the long frame mode.

Signaling for the TP3053 may be accomplished in either short or long frame sync mode. The short mode signaling is the same as the TP3052. For long frame signaling, two additional frame sync pulses are required, SF_X and SF_R, which indicate transmit and receive signaling frames, respectively. With an SF_X signaling frame sync, the data present at the SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With an SF_R signaling frame sync, the LSB of the PCM data at D_R will be latched and appear on the SIG_R output pin until the next signaling frame. The decoder will also do the "½" step interpretation to compensate for the loss of the LSB.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3052, TP3053, TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ-law (TP3052, TP3053, TP3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifer capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at any Digital Input or Output	V_{CC} + 0.3V to GNDA − 0.3V
Operating Temperature Range	−25°C to + 125°C
Storage Temperature Range	−65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

ESD rating is to be determined.

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA SIG_R, I_L = 1.0 mA $\overline{TS}_X$, I_L = 3.2 mA, Open Drain			**0.4** **0.4** **0.4**	V V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA SIG_R, I_H = −1.0 mA	**2.4** **2.4**			V V
I_{IL}	Input Low Current	GNDA ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	**−10**		**10**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA ≤ V_O ≤ V_{CC}	**−10**		**10**	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, R_L ≥ 10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		−200		200	mV
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current	No Load		0.5	**1.5**	mA
$I_{BB}0$	Power-Down Current	No Load		0.05	**0.3**	mA
$I_{CC}1$	Power-Up Active Current	No Load		6.0	**9.0**	mA
$I_{BB}1$	Power-Up Active Current	No Load		6.0	**9.0**	mA

Timing Specifications Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V. See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	**100**			ns
t_{WBH}	Width of Bit Clock High	V_{IH} = 2.2V	**160**			ns
t_{WBL}	Width of Bit Clock Low	V_{IL} = 0.6V	**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	**80**			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			**140**	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	C_L = 0 pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C_L = 0 pF to 150 pF	**20**		**165**	ns
t_{SSFF}	Set-Up Time from $SF_{X/R}$ High to $FS_{X/R}$	TP3053 Only	**60**			ns
t_{SSFB}	Set-Up Time from Signal Frame Sync High to $BCLK_{X/R}$ Clock	TP3053 Only	**60**			ns
t_{SSGB}	Set-Up Time from SIG_X to $BCLK_X$	TP3052 and TP3053	**100**			ns
t_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	TP3052 and TP3053	**50**			ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		**50**			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		**50**			ns
t_{HBSF}	Hold Time from $BCLK_{X/R}$ Low to Signaling Frame Sync	TP3053 Only	**100**			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	**160**			ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock		485	488	15725	ns

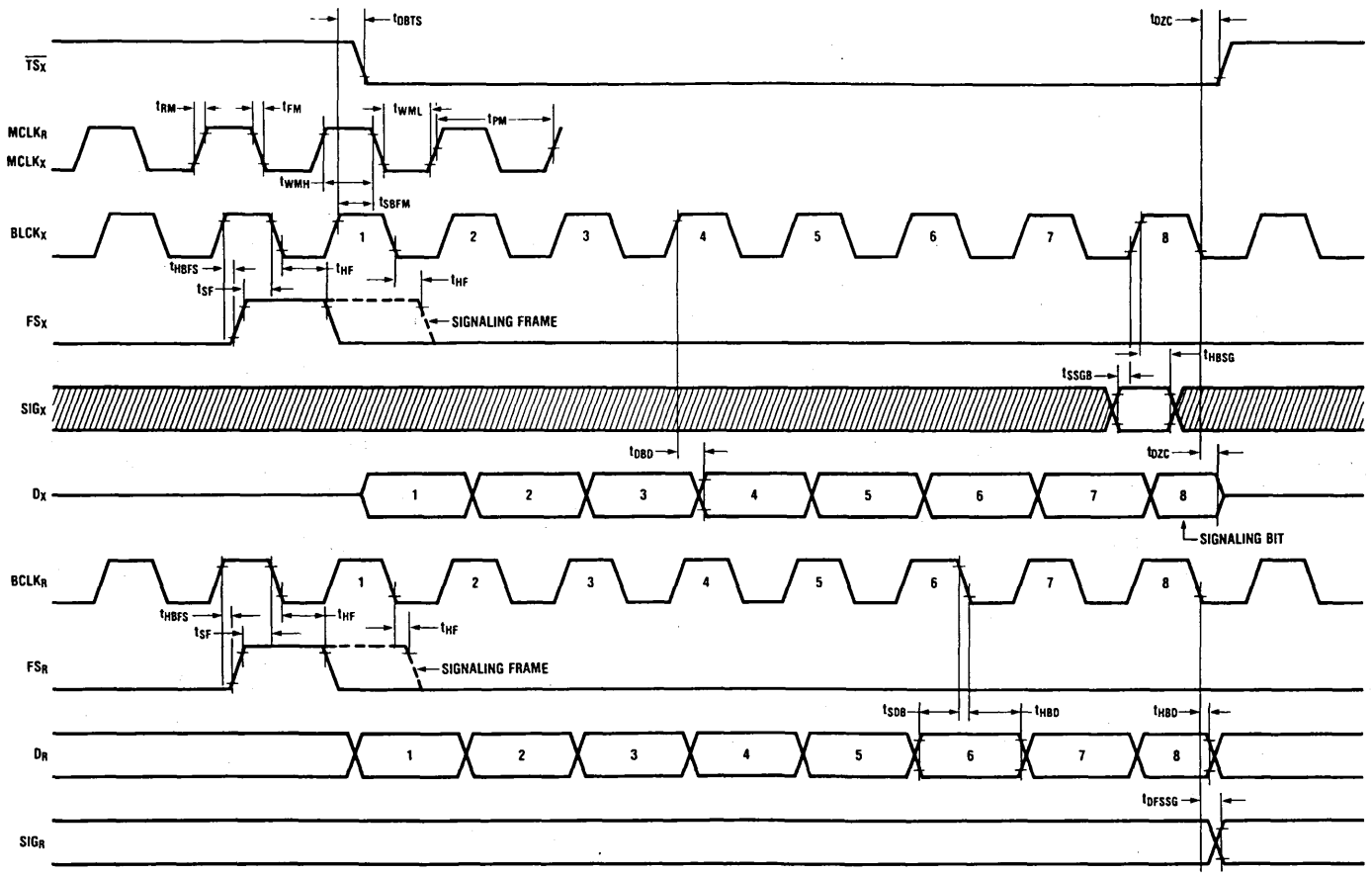


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FIGURE 2. Short Frame Sync Timing

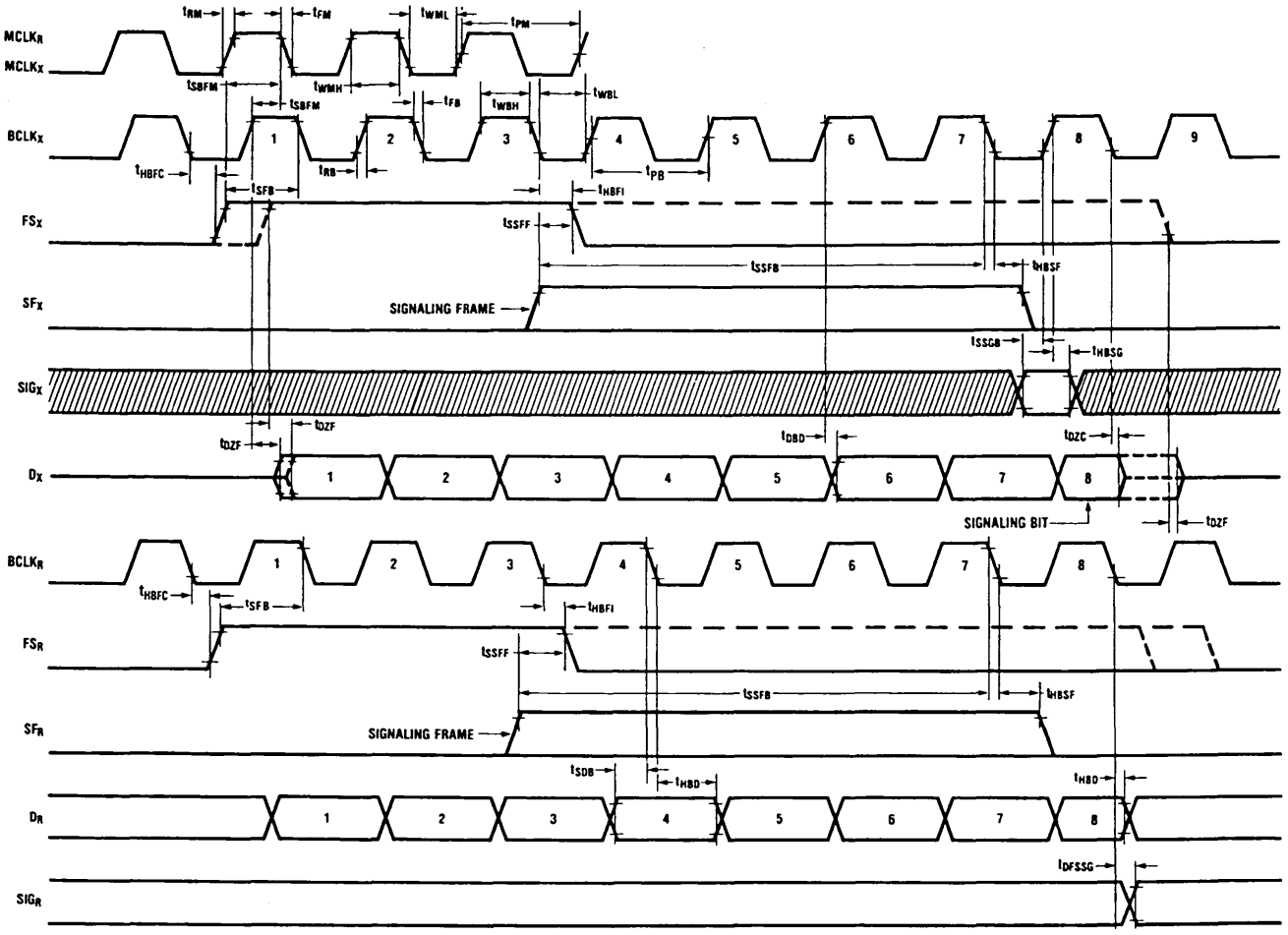

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FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		 1.2276		 Vrms
t_{MAX}		Max Overload Level TP3052, TP3053, TP3054 (3.17 dBm0) TP3057 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input at GS_X=0 dBm0 at 1020 Hz TP3052/53/54/57 TP3052/53/54/57-1	 **−0.15** **−0.20**		 **0.15** **0.20**	 dB dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16 Hz f=50 Hz f=60 Hz (TP3052/53/54/57-1) f=60 Hz (TP3052/53/54/57) f=200 Hz f=300 Hz−3000 Hz f=3300 Hz f=3400 Hz (TP3052/53/54/57) f=3400 Hz (TP3052/53/54/57-1) f=4000 Hz f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−1.8** **−0.15** **−0.35** **−0.7** **−0.95**		**−40** **−30** **−22** **−26** **−0.1** **0.15** **0.05** **0** **0.05** **−14** **−32**	dB dB dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0 VF_{XI}^+ = −40 dBm0 to +3 dBm0 VF_{XI}^+ = −50 dBm0 to −40 dBm0 VF_{XI}^+ = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz TP3052/53/54/57 TP3052/53/54/57-1	 **−0.15** **−0.20**		 **0.15** **0.20**	 dB dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0 Hz to 3000 Hz f=3300 Hz f=3400 Hz f=4000 Hz	**−0.15** **−0.35** **−0.7**		**0.15** **0.05** **0** **−14**	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level = −40 dBm0 to +3 dBm0 = −40 dBm0 to +3 dBm0 (TP3052/53/54/57-1 only) = −50 dBm0 to −40 dBm0 = −55 dBm0 to −50 dBm0	 **−0.2** **−0.25** **−0.4** **−1.2**		 **0.2** **0.25** **0.4** **1.2**	 dB dB dB dB
V_{RO}	Receive Output Drive Level	R_L=600Ω	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	μs
		f = 600 Hz–800 Hz		120	145	μs
		f = 800 Hz–1000 Hz		50	75	μs
		f = 1000 Hz–1600 Hz		20	40	μs
		f = 1600 Hz–2600 Hz		55	75	μs
		f = 2600 Hz–2800 Hz		80	105	μs
		f = 2800 Hz–3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		μs
		f = 1000 Hz–1600 Hz	−30	−20		μs
		f = 1600 Hz–2600 Hz		70	90	μs
		f = 2600 Hz–2800 Hz		100	125	μs
		f = 2800 Hz–3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3052, TP3053, TP3054		12	**15**	dBrnC0
		TP3052/53/54-1 (Note 1)			**16**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3057		−74	**−67**	dBm0p
		TP3057-1 (Note 1)			**−66**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	PCM Code is Alternating Positive and Negative Zero —				
		TP3052/53/54		8	**11**	dBrnC0
		TP3052/53/54-1			**13**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3057 PCM Code Equals Positive Zero —		−82	**−79**	dBm0p
		TP3057-1			**−77**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI^+ = −50 dBm0 V_{CC} = 5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 2)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI^+ = −50 dBm0 V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 2)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_R0				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dB
		f = 25 kHz–50 kHz	**36**			dB
		f = 0–4 kHz (TP3052/53/54/57-1)	**38**			dBC
		f = 4–50 kHz (TP3052/53/54/57-1)	**35**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB} = −5.0 V_{DC} + 100 mVrms Measure VF_R0				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dB
		f = 25 kHz–50 kHz	**36**			dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R.			−30	dB
		4600 Hz–7600 Hz			−30	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			−30	dB
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3) Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to −30 dBm0	**36**			dBC
		= −40 dBm0 XMT	**29**			dBC
		RCV	**30**			dBC
		= −55 dBm0 XMT	**14**			dBC
		RCV	**15**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_X^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Quiet PCM Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz, VF_XI = Multitone (Note 2)		−90	**−70** (Note 2)	dB

ENCODING FORMAT AT D_X OUTPUT

	TP3052, TP3053, TP3054 μ-Law								TP3057 A-Law (Includes Even Bit Inversion)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI^+.

Note 3: All devices are measured using C message weighted filter.

Applications Information

POWER SUPPLIES

While the pins of the TP3050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to the device as possible.

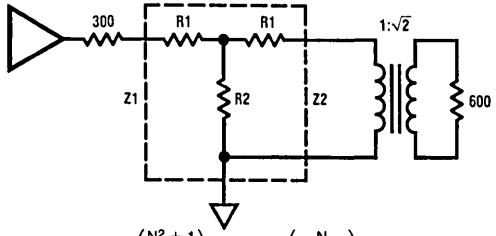
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1.Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

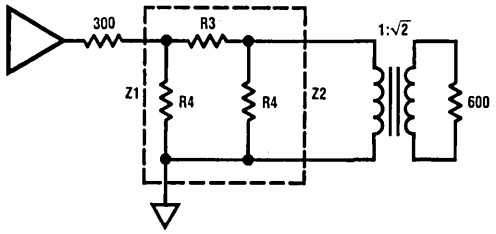
$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{SC} \bullet Z_{OC}}$$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination

π-Pad Attenuator



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$$R3 = \sqrt{\frac{Z1.Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

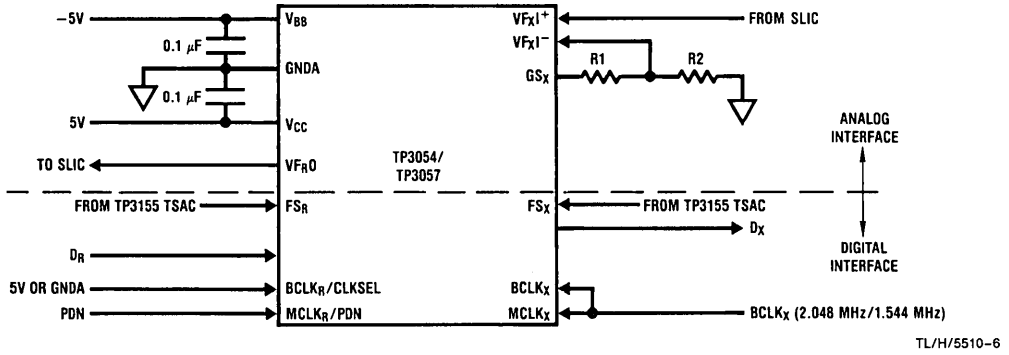
Note: See Application Note 370 for further details.

Applications Information (Continued)

TABLE II. Attentuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6l	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



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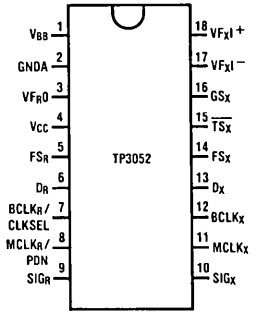
Note 1: XMIT gain = $20 \times \log \left(\frac{R1+R2}{R2} \right)$ where (R1 + R2) > 10 KΩ.

FIGURE 4

Connection Diagrams (Continued)

Dual-In-Line Package



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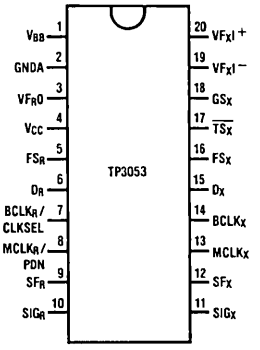
Top View
Order Number TP3052J
or TP3052J-1
See NS Package Number J18A

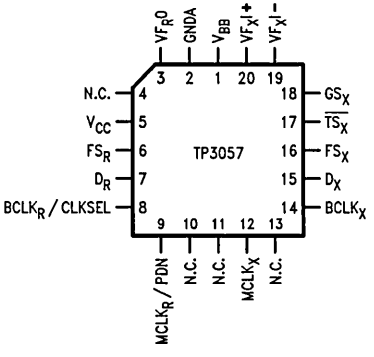
Dual-In-Line Package



TL/H/5510–9

Top View
Order Number TP3053J
or TP3053J-1
See NS Package Number J20A

Plastic Chip Carrier



TL/H/5510–7

Top View
Order Number TP3057V
or TP3057V-1
See NS Package Number V20A

1

National Semiconductor Corporation

microCMOS

TP3052-X/TP3053-X/TP3054-X TP3057-X Extended Temperature Monolithic Serial Interface CMOS CODEC/FILTER COMBO™ Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

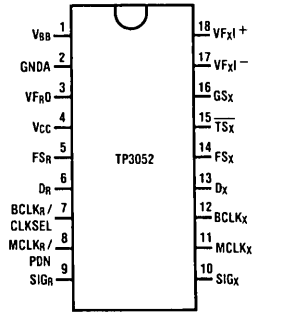
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz, and a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- −40°C to +85°C operation
- Complete CODEC and filtering system (COMBO) including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
- μ-law with signaling, TP3020 or TP5116A timing—TP3052
- μ-law with signaling, TP5116A family timing—TP3053
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

Connection Diagrams

Dual-In-Line Package

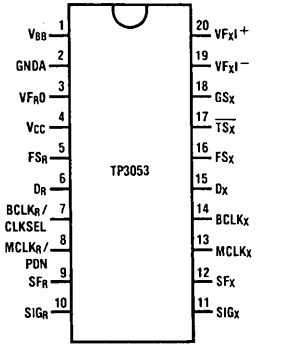


TL/H/8674-7

Top View

Order Number TP3052J-X
NS Package Number J18A

Dual-In-Line Package

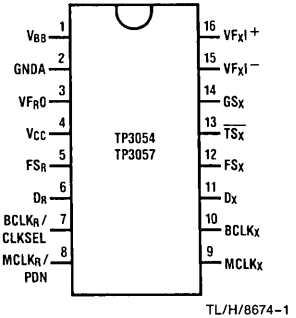


TL/H/8674-8

Top View

Order Number TP3053J-X
NS Package Number J20A

Dual-In-Line Package



TL/H/8674-1

Top View

Order Number TP3054J-X, or TP3057J-X
NS Package Number J16A

Block Diagram

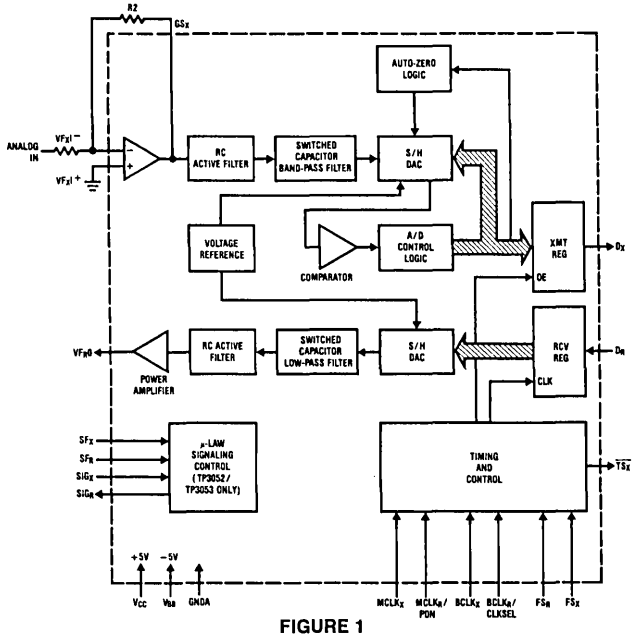


FIGURE 1 TL/H/8674-2

Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
GNDA	Analog ground. All signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1).
$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.

Symbol	Function
SF_R	When high during FS_R, this input indicates a receive signal frame.
SIG_R	The eighth bit of the PCM data appears at this output after each receive signalling frame.
SIG_X	Signal data input. Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
SF_X	When high during FS_X, this input indicates a transmit signaling frame.
$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$, but should be synchronous for best performance.
FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into a power-down state. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table I indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3057	TP3052 TP3053 TP3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3052, 53, 54, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table I are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A/56A CODECs) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

SIGNALING

The TP3052 and TP3053 μ-law COMBOs contain circuitry to insert and extract signaling information in the PCM data stream. The TP3052 is intended for short frame sync applications, and the TP3053 for long frame sync applications, although the TP3053 may also be used in short frame sync applications. The TP3054 and TP3057 have no provision for signaling.

Functional Description (Continued)

Signaling for the TP3052 Package is accomplished by applying a frame sync pulse two bit clock periods long, as shown in *Figure 2*. With FS_X two bit clock periods long, the data present at SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With FS_R two bit clock periods long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as "½" to minimize noise and distortion. This short frame signaling may also be implemented using the TP3053, providing SF_R and SF_X are left open circuit or tied low. The TP3052 is not capable of inserting or extracting signaling information in the long frame mode.

Signaling for the TP3053 may be accomplished in either short or long frame sync mode. The short mode signaling is the same as the TP3052. For long frame signaling, two additional frame sync pulses are required, SF_X and SF_R, which indicate transmit and receive signaling frames, respectively. With an SF_X signaling frame sync, the data present at the SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With an SF_R signaling frame sync, the LSB of the PCM data at D_R will be latched and appear on the SIG_R output pin until the next signaling frame. The decoder will also do the "½" step interpretation to compensate for the loss of the LSB.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3052, TP3053, TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ-law (TP3052, TP3053, TP3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifer capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at any Digital Input or Output	V_{CC} + 0.3V to GNDA − 0.3V
Operating Temperature Range	−55°C to + 125°C
Storage Temperature Range	−65°C to + 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA SIG_R, I_L = 1.0 mA $\overline{TS}_X$, I_L = 3.2 mA, Open Drain			**0.4** **0.4** **0.4**	V V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA SIG_R, I_H = −1.0 mA	**2.4** **2.4**			V V
I_{IL}	Input Low Current	GNDA ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	**−10**		**10**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA ≤ V_O ≤ V_{CC}	**−10**		**10**	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, R_L ≥ 10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		−200		200	mV
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current	No Load		0.65	**2.0**	mA
$I_{BB}0$	Power-Down Current	No Load		0.01	**0.33**	mA
$I_{CC}1$	Power-Up (Active) Current	No Load		7.0	**11.0**	mA
$I_{BB}1$	Power-Up (Active) Current	No Load		7.0	**11.0**	mA

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = 5.0V, T_A = 25°C.

All timing parameters are assured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X — Short Frame	**100**			ns
		Long Frame	**125**			
t_{WBH}	Width of Bit Clock High	V_{IH} = 2.2V	**160**			ns
t_{WBL}	Width of Bit Clock Low	V_{IL} = 0.6V	**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	**95**			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			**140**	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	C_L = 0 pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C_L = 0 pF to 150 pF	**20**		**165**	ns
t_{SSFF}	Set-Up Time from $SF_{X/R}$ High to $FS_{X/R}$	TP3053 Only	**60**			ns
t_{SSFB}	Set-Up Time from Signal Frame Sync High to $BCLK_{X/R}$ Clock	TP3053 Only	**60**			ns
t_{SSGB}	Set-Up Time from SIG_X to $BCLK_X$	TP3052 and TP3053	**100**			ns
t_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	TP3052 and TP3053	**50**			ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		**50**			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		**50**			ns
t_{HBSF}	Hold Time from $BCLK_{X/R}$ Low to Signaling Frame Sync	TP3053 Only	**100**			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	**160**			ns

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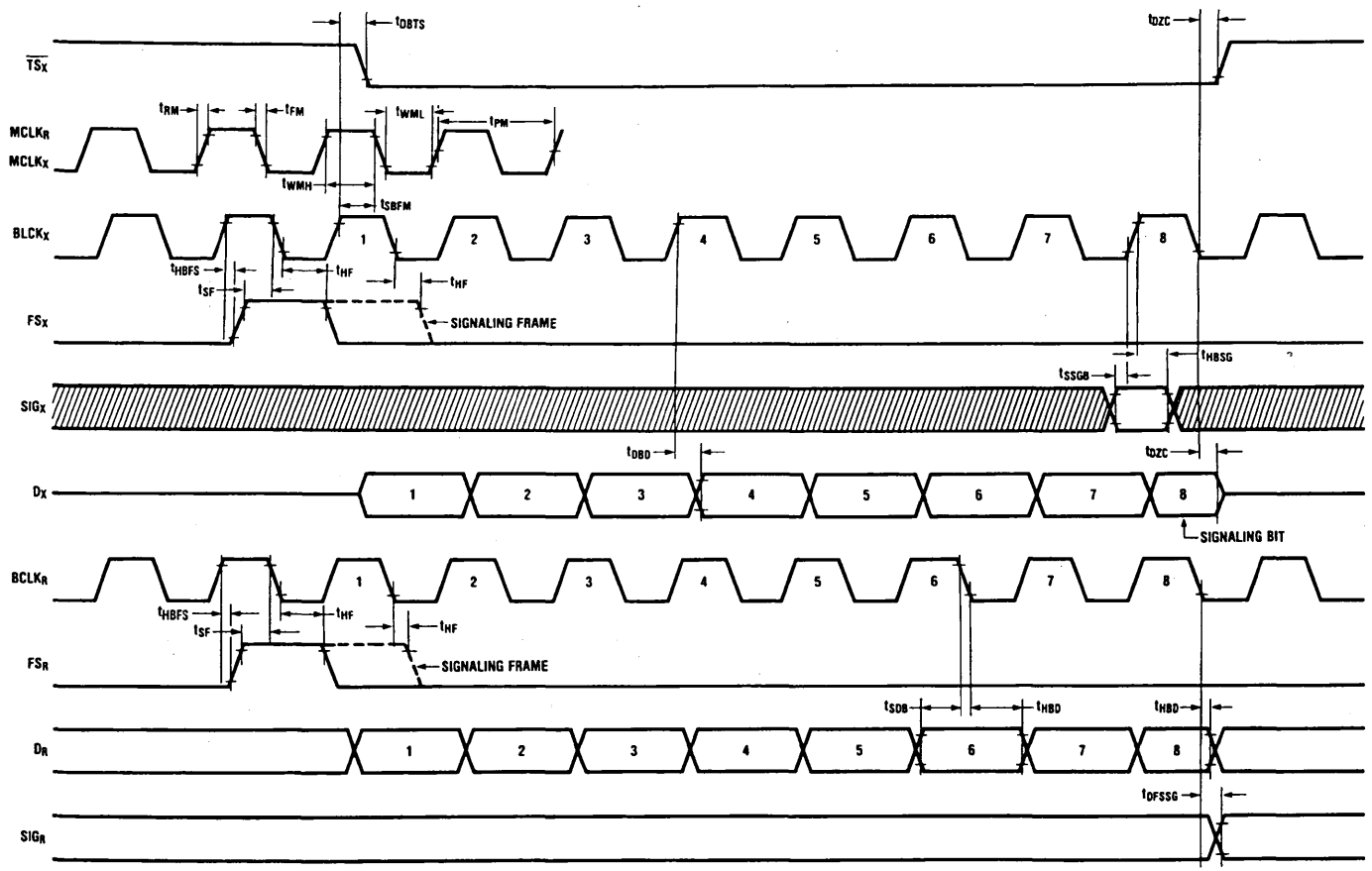
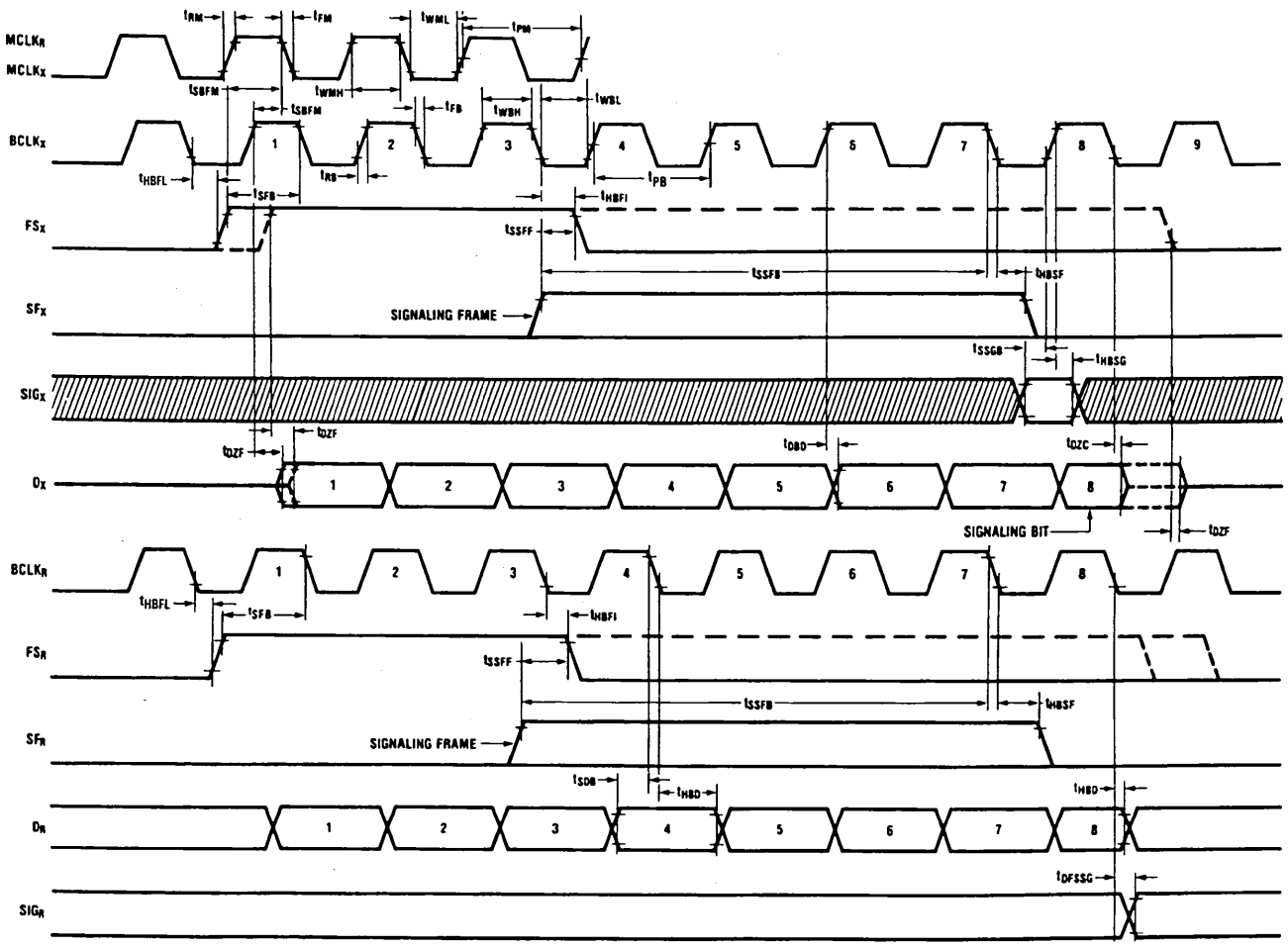


TL/H/8674-3

FIGURE 2. Short Frame Sync Timing



TL/H/8674–4

FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		 1.2276		 Vrms
t_{MAX}		Max Overload Level TP3052, TP3053, TP3054 (3.17 dBm0) TP3057 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V Input at GS_X = 0 dBm0 at 1020 Hz	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz−3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−1.8** **−0.15** **−0.35** **−0.7**		**−40** **−30** **−26** **−0.1** **0.15** **0.1** **0** **−14** **−32**	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.15		0.15	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0 VF_XI^+ = −40 dBm0 to +3 dBm0 VF_XI^+ = −50 dBm0 to −40 dBm0 VF_XI^+ = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	 **−0.15**		 **0.15**	 dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	**−0.15** **−0.35** **−0.7**		**0.15** **0.1** **0** **−14**	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.15		0.15	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Reletive to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level = −40 dBm0 to +3 dBm0 PCM Level = −50 dBm0 to −40 dBm0 PCM Level = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
V_{RO}	Receive Output Drive Level	R_L = 600Ω	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	μs
		f = 600 Hz–800 Hz		120	145	μs
		f = 800 Hz–1000 Hz		50	75	μs
		f = 1000 Hz–1600 Hz		20	40	μs
		f = 1600 Hz–2600 Hz		55	75	μs
		f = 2600 Hz–2800 Hz		80	105	μs
		f = 2800 Hz–3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		μs
		f = 1000 Hz–1600 Hz	−30	−20		μs
		f = 1600 Hz–2600 Hz		70	90	μs
		f = 2600 Hz–2800 Hz		100	125	μs
		f = 2800 Hz–3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3052, TP3053, TP3054 (Note 1)		12	**16**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3057 (Note 1)		−74	**−67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	PCM Code is Alternating Positive and Negative Zero — TP3052/53/54		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3057 PCM Code Equals Positive Zero —		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI+ = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 2)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 2)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_R0				
		f = 0 Hz–4000 Hz	**38**			dBC
		f = 4 kHz–25 kHz	**38**			dB
		f = 25 kHz–50 kHz	**35**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB} = −5.0 V_{DC} + 100 mVrms Measure VF_R0				
		f = 0 Hz–4000 Hz	**38**			dBC
		f = 4 kHz–25 kHz	**38**			dB
		f = 25 kHz–50 kHz	**35**			dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R.			−30	dB
		4600 Hz–7600 Hz			−30	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			−30	dB
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3)				
		Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to −30 dBm0	**36**			dBC
		= −40 dBm0 XMT	**28**			dBC
		RCV	**29**			dBC
		= −55 dBm0 XMT	**13**			dBC
		RCV	**14**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−43**	dB
SFD_R	Single Frequency Distortion, Receive				**−43**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_X^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz, D_R = Quiet PCM Code (Note 4)		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz, VF_XI = Multitone (Note 2)		−90	**−70** (Note 2)	dB

ENCODING FORMAT AT D_X OUTPUT

	TP3052, TP3053, TP3054 μ-Law								TP3057 A-Law (Includes Even Bit Inversion)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI^+.

Note 3: TP3052/53/54/57 are measured using C message weighted filter.

Note 4: CT_{X-R} @ 1.544 MHz $MCLK_X$ freq. is −70 dB max. 50% ±5% $BCLK_X$ duty cycle.

Applications Information

POWER SUPPLIES

While the pins of the TP3050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB} as close to device pins as possible.

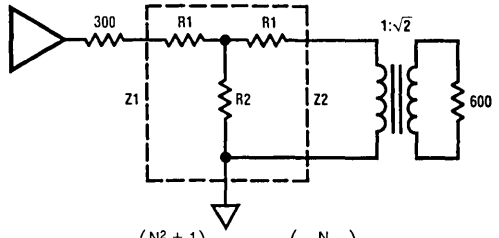
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

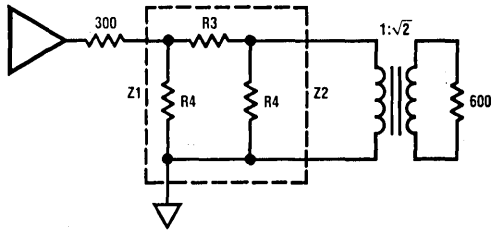
$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{SC} \cdot Z_{OC}}$$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination

π-Pad Attenuator



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$$R3 = \sqrt{\frac{Z1 \cdot Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

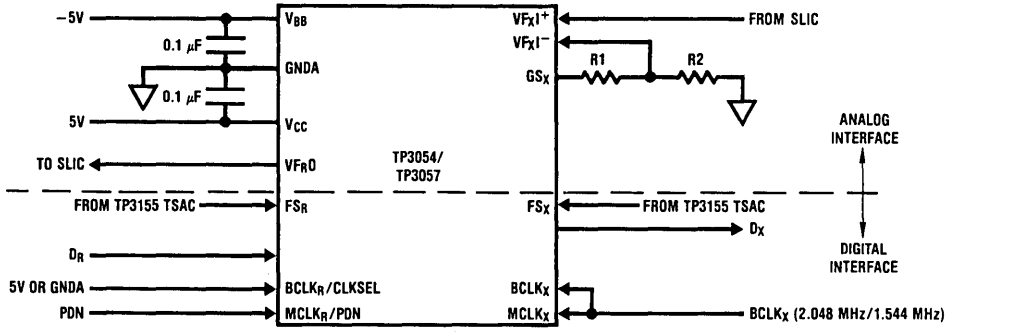
Note: See Application Note 370 for further details.

Applications Information (Continued)

TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6l	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



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Note 1: XMIT gain $= 20 \times \log\left(\frac{R1+R2}{R2}\right)$, $(R1+R2) > 10\ K\Omega$.

FIGURE 4

National Semiconductor Corporation

microCMOS

TP3064/TP3067 Monolithic Serial Interface CMOS CODEC/FILTER COMBO™

General Description

The TP3064 (μ-law) and TP3067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

Similar to the TP3050 family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ±6.6V across a balanced 600Ω load.

Also included is an Analog Loopback switch and a $\overline{TS_X}$ output.

Features

- Complete CODEC and filtering system including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
  - — Receive push-pull power amplifiers
- μ-law—TP3064
- A-law—TP3067
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 70 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

Block Diagram

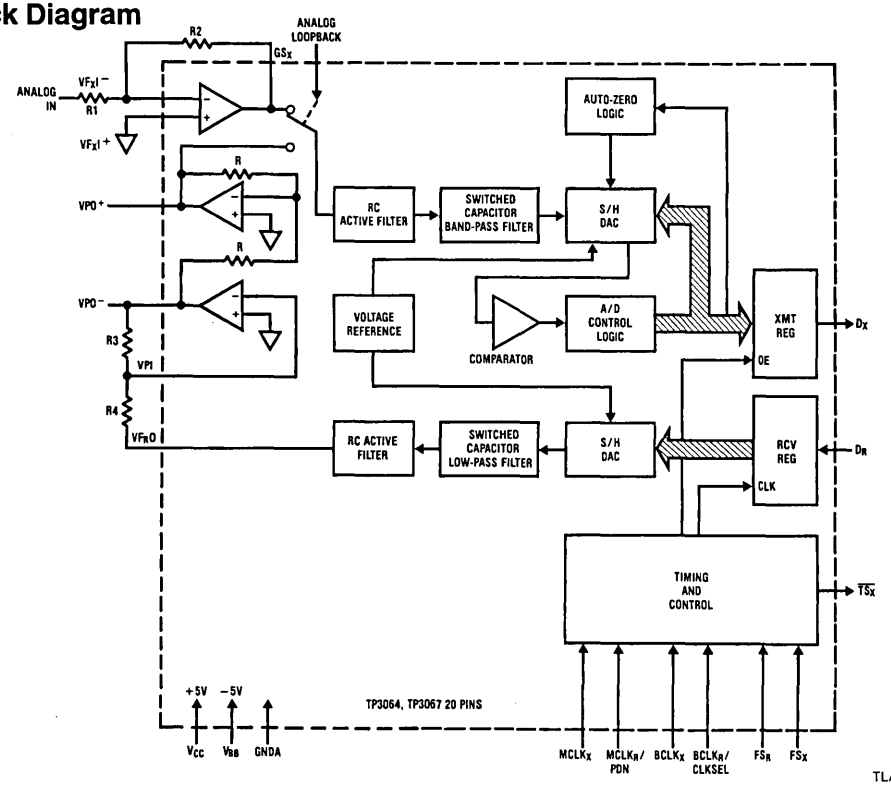

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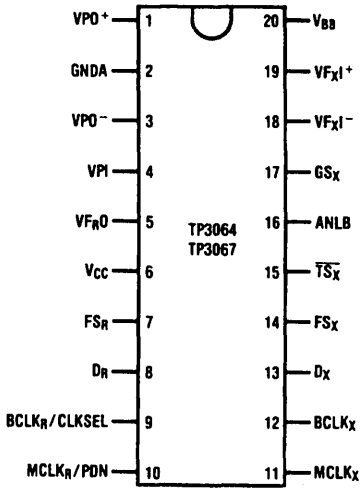
FIGURE 1

Connection Diagrams

Dual-In-Line Package



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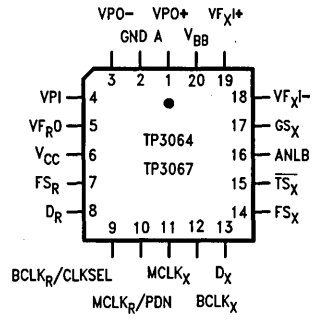
Top View

Plastic Chip Carrier



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Top View

Order Number TP3064V, TP3064V-1 or TP3067V or TP3067V-1
See NS Package V20A

Order Number TP3064J, TP3067J
See NS Package J20A

Pin Description

Symbol	Function
VPO^+	The non-inverted output of the receive power amplifier.
GNDA	Analog ground. All signals are referenced to this pin.
VPO^-	The inverted output of the receive power amplifier.
VPI	Inverting input to the receive power amplifier.
VF_RO	Analog output of the receive filter.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table I).
$MCLK_R$/ PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
ANLB	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO^+ output of the receive power amplifier.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO™ and places it into a power-down state. All non-essential circuits are deactivated and the D_X, VF_RO, VPO^- and VPO^+ outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BLCK_X$ will be selected as the bit clock for both the transmit and receive directions. Table I indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3067	TP3064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3067, or 1.536 MHZ, 1.544 MHz for the TP3064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table I are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A/56 CODECs) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$($BCLK_X$ in synchronous mode). All devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3064) or A-law (TP3067) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see

Functional Description (Continued)

table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3067) or μ-law (TP3064) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at VF_RO. The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5V peak output signal from the receive filter up to ±3.3V peak into an unbalanced 300Ω load, or ±4.0V into an unbalanced 15 kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$:1 turns ratio, as shown in *Figure 4*. A total peak power of 15.6 dBm can be delivered to the load plus termination.

ENCODING FORMAT AT D_X OUTPUT

	TP3064 μ-Law								TP3067 A-Law (Includes Even Bit Inversion)							
V_{IN} = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	$V_{CC}+0.3V$ to $V_{BB}-0.3V$
Voltage at any Digital Input or Output	$V_{CC}+0.3V$ to GNDA−0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current			0.5	**1.5**	mA
$I_{BB}0$	Power-Down Current			0.05	**0.3**	mA
$I_{CC}1$	Active Current	VPI = 0V; VF_RO, VPO+ and VPO− unloaded		7.0	**10.0**	mA
$I_{BB}1$	Active Current	VPI = 0V; VF_RO, VPO+ and VPO− unloaded		7.0	**10.0**	mA
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA $\overline{TS_X}$, I_L = 3.2 mA, Open Drain			**0.4** **0.4**	V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA	**2.4**			V
I_{IL}	Input Low Current	GNDA ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	**−10**		**10**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA ≤ V_O ≤ V_{CC}	**−10**		**10**	μA

1

Electrical Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V±5%, V_{BB} = −5.0V±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L \ge 10$ kΩ	**−2.8**		**+2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	**−2.5**		**2.5**	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	**60**			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	$VF_RO = \pm 2.5V$	10			kΩ
C_LRF	Load Capacitance	Connect from VF_RO to GNDA			25	pF
VOS_RO	Output DC Offset Voltage	Measure from VF_RO to GNDA	**−200**		**200**	mV
ANALOG INTERFACE WITH POWER AMPLIFIERS (ALL DEVICES)						
IPI	Input Leakage Current	$-1.0V \le VPI \le 1.0V$	**−100**		**100**	nA
RIPI	Input Resistance	$-1.0V \le VPI \le 1.0V$	10			MΩ
VIOS	Input Offset Voltage		**−25**		**25**	mV
ROP	Output Resistance	Inverting Unity-Gain at VPO^+ or VPO^-		1		Ω
F_C	Unity-Gain Bandwidth	Open Loop (VPO^-)		400		kHz
C_LP	Load Capacitance				100	pF
GA_P^+	Gain from VPO^- to VPO^+	$R_L = 600\Omega$ VPO^+ to VPO^- Level at $VPO^- = 1.77$ Vrms		−1		V/V
$PSRR_P$	Power Supply Rejection of V_{CC} or V_{BB}	VPO^- Connected to VPI 0 kHz−4 kHz 4 kHz−50 kHz	 60 36			 dB dB
R_LP	Load Resistance	Connect from VPO^+ to VPO^-	600			Ω

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%, T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals are referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	 $MCLK_X$ and $MCLK_R$		1.536 **1.544** **2.048**		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	**100**			ns
t_{WBH}	Width of Bit Clock High		**160**			ns
t_{WBL}	Width of Bit Clock Low		**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time for Frame Sync to Bit Clock Low	Long Frame Only	**80**			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	**0**		**180**	ns
t_{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			**140**	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled		**50**		**165**	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C_L = 0 pF to 150 pF	**20**		**165**	ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		**50**			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		**50**			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	**160**			ns

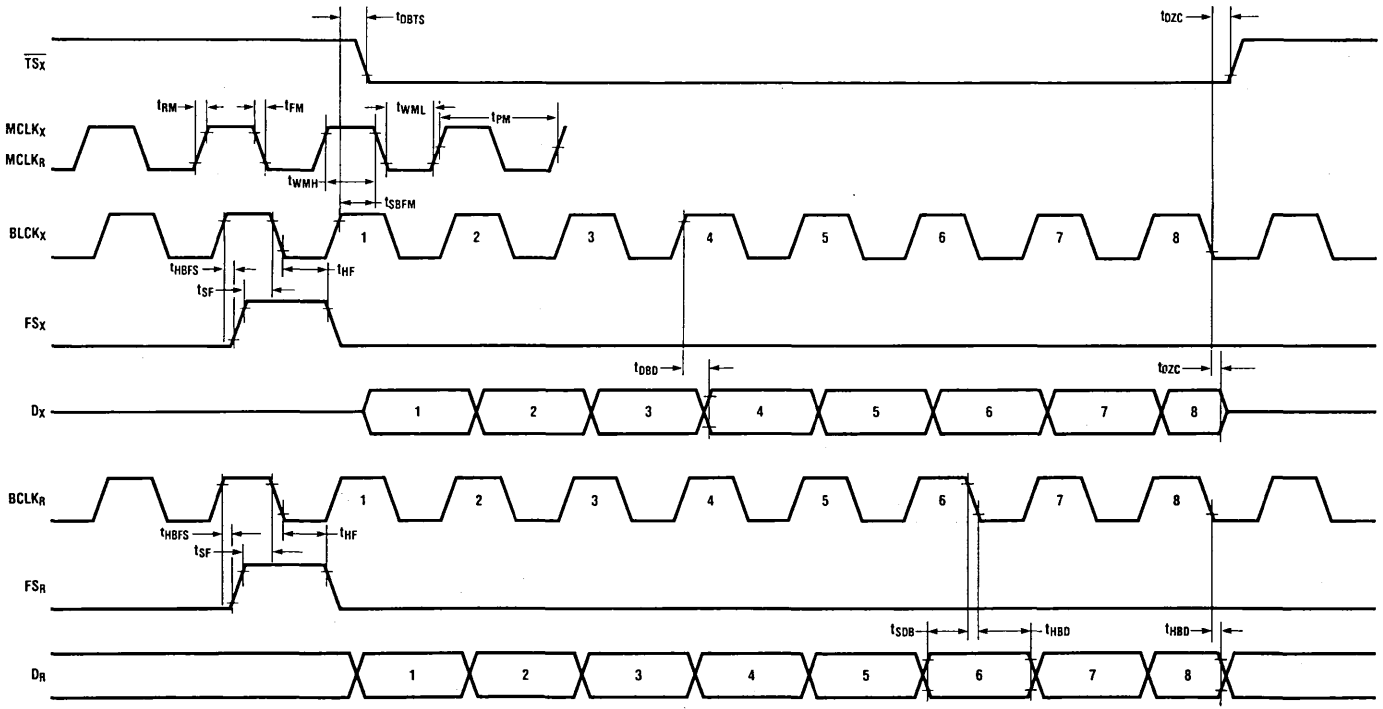

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FIGURE 2. Short Frame Sync Timing

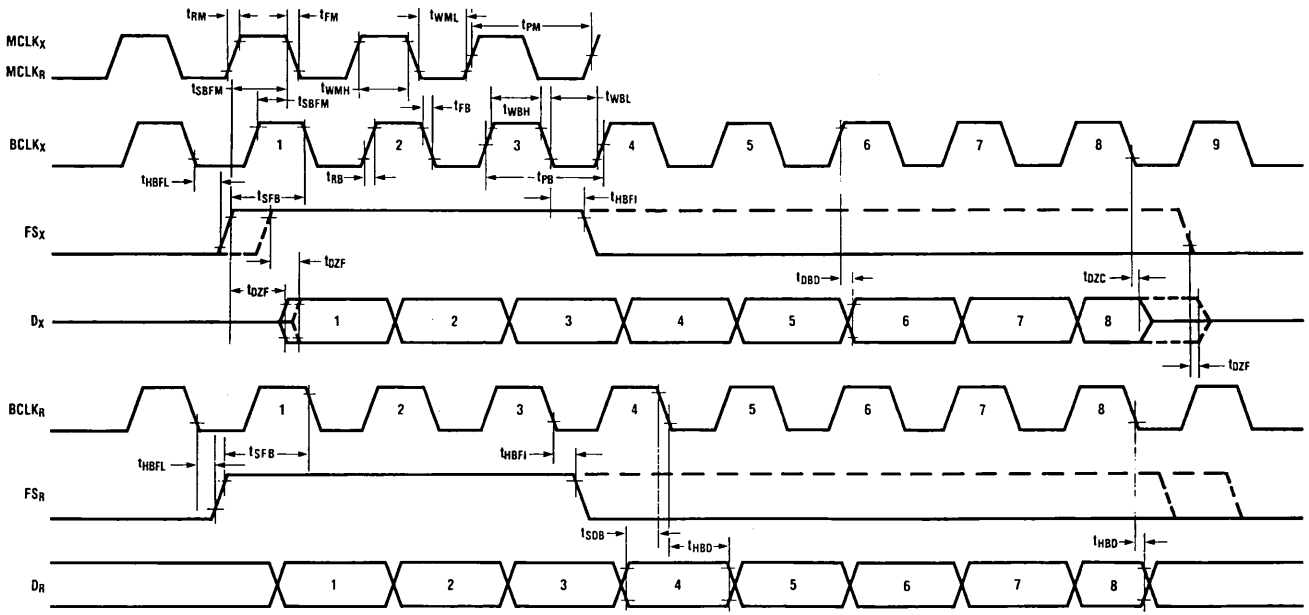

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FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of nominal gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		1.2276		Vrms
t_{MAX}		Max Transmit Overload Level TP3064 (3.17 dBm0) TP3067 (3.14 dBm0)		2.501 2.492		V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V TP3064, TP3067	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16 Hz			−40	dB
		f=50 Hz			−30	dB
		f=60 Hz, TP3064, TP3067			**−26**	dB
		f=200 Hz	**−1.8**		**−0.1**	dB
		f=300 Hz-3000 Hz	**−0.15**		**0.15**	dB
		f=3300 Hz	**−0.35**		**0.05**	dB
		f=3400 Hz, TP3064, TP3067	**−0.7**		**0**	dB
		f=4000 Hz			**−14**	dB
		f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz			**−32**	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0				
		VF_XI^+ = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		VF_XI^+ = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		VF_XI^+ = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
G_{RA}	Receive Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal TP3064, TP3067	**−0.15**		**0.15**	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0 Hz to 3000 Hz	**−0.15**		**0.15**	dB
		f=3300 Hz	**−0.35**		**0.05**	dB
		f=3400 Hz	**−0.7**		**0**	dB
		f=4000 Hz			**−14**	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded − 10 dBm0 Signal				
		PCM Level = −40 dBm0 to +3 dBm0 TP3064, TP3067	**−0.2**		**0.2**	dB
		PCM Level = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		PCM Level = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
V_{RO}	Receive Filter Output at VF_RO	RL=10 kΩ	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz−600 Hz		195	220	μs
		f = 600 Hz−800 Hz		120	145	μs
		f = 800 Hz−1000 Hz		50	75	μs
		f = 1000 Hz−1600 Hz		20	40	μs
		f = 1600 Hz−2600 Hz		55	75	μs
		f = 2600 Hz−2800 Hz		80	105	μs
		f = 2800 Hz−3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz−1000 Hz	−40	−25		μs
		f = 1000 Hz−1600 Hz	−30	−20		μs
		f = 1600 Hz−2600 Hz		70	90	μs
		f = 2600 Hz−2800 Hz		100	125	μs
		f = 2800 Hz−3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3064 (Note 1)		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3067 (Note 1)		−74	**−67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	PCM Code Equals Alternating Positive and Negative Zero TP3064		8	**11**	dBrnCO
N_{RP}	Receive Noise, P Message Weighted	PCM Code Equals Positive Zero TP3067		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 100 mVrms f = 0 kHz−50 kHz (Note 2)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz−50 kHz (Note 2)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz−4000 Hz	**38**			dBC
		f = 4 kHz−50 kHz	**25**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB} = −5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz−4000 Hz	**40**			dBC
		f = 4 kHz−25 kHz	**40**			dB
		f = 25 kHz−50 kHz	**36**			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz−3400 Hz Input PCM Code Applied at DR Measure Individual Image Signals at VF_RO				
		4600 Hz−7600 Hz			**−32**	dB
		7600 Hz−8400 Hz			−40	dB
		8400 Hz−100,000 Hz			**−32**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X, STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3)				
		Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to −30 dBm0	**36**			dBC
		= −40 dBm0 XMT	**29**			dBC
		RCV	**30**			dBC
		= −55 dBm0 XMT	**14**			dBC
		RCV	**15**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz−3400 Hz			−41	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk	f = 300 Hz−3000 Hz, D_R = Quiet PCM Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk	f = 300 Hz−3000 Hz, VF_XI = 0V (Note 2)		−90	**−70**	dB
POWER AMPLIFIERS						
V_OPA	Maximum 0 dBm0 Level (Better than ±0.1 dB Linearity over the Range −10 dBm0 to +3 dBm0)	Balanced Load, R_L Connected Between VPO^+ and VPO^-.				
		R_L = 600Ω	**3.3**			Vrms
		R_L = 1200Ω	3.5			Vrms
		R_L = 30 kΩ	4.0			Vrms
S/D_P	Signal/Distortion	R_L = 600Ω	50			dB

Note 1: Measured by extrapolation from the distortion test result.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI^+.

Note 3: TP3064 is measured using C message weighted filter. TP3067 is measured using P message weighted filter.

Applications Information

POWER SUPPLIES

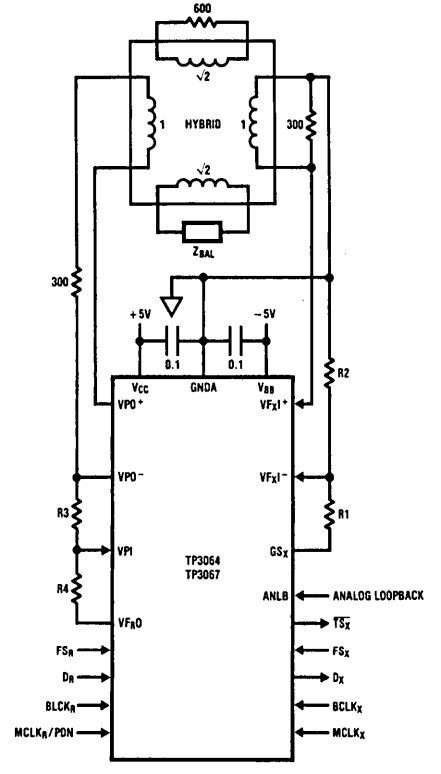
While the pins of the TP3060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in "STAR" formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

Note: See Application Note 370 for further details

Typical Asynchronous Application



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Note 1: Transmit gain $= 20 \times \log\left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10\ k\Omega$

Note 2: Receive gain $= 20 \times \log\left(\frac{2 \times R3}{R4}\right)$, $R4 \geq 10\ k\Omega$

FIGURE 4

National Semiconductor Corporation

microCMOS

TP3150 Time Slot Assignment Circuit

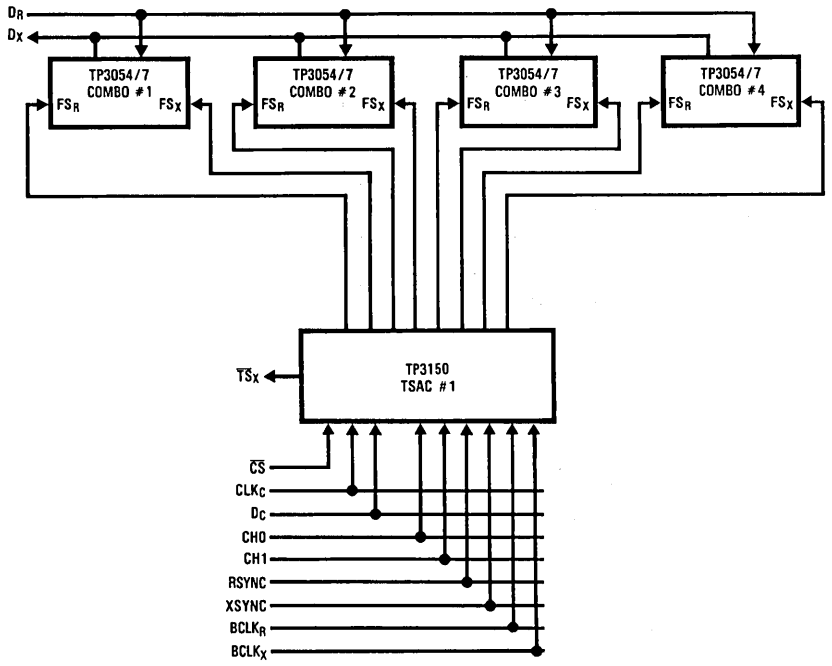
General Description

The TP3150 is a monolithic CMOS logic circuit designed to generate transmit and receive frame synchronization pulses for up to 4 COMBO™ CODEC/Filters. Each frame sync pulse may be independently assigned to a time slot in a frame of up to 32 time slots. Assignments are controlled by loading in an 8-bit word via a simple serial interface port. This control interface is compatible with that used on the TP3020/TP3021 and 2910/2911 CODECs, enabling an easy upgrade to COMBO CODEC/Filters to be made.

Features

- Controls up to 4 COMBO CODEC/Filters
- Independent transmit and receive time slot assignments
- Asynchronous transmit and receive clocks
- Up to 32 time slots per frame
- Serial control interface compatible with TP3020/TP3021 CODECs
- LS TTL and CMOS compatible inputs
- 5 mW, 5V operation

Typical Application



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} Relative to GND	7V
Voltage at Any Input or Output	V_{CC} + 0.3V to GND −0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 seconds)	300°C

ESD rating to be determined

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V to ±5%, T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/ or product design and characterization. Typicals specified at V_{CC} = +5.0V, T_A = 25°C.

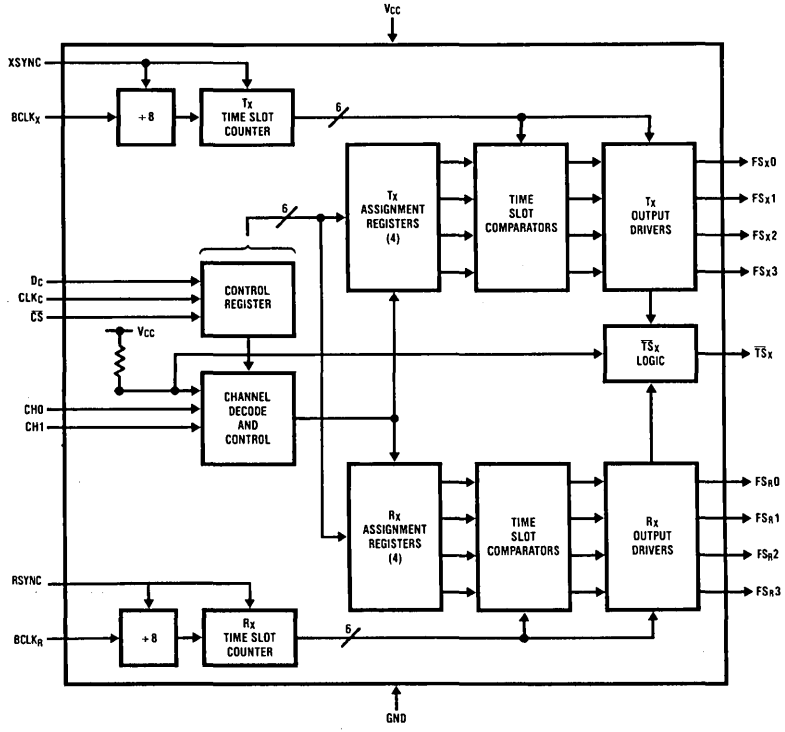
Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Levels					
V_{IH}, Logic High		**2.0**			V
V_{IL}, Logic Low				**0.7**	V
Input Currents					
All Inputs Except MODE	$V_{IL} < V_{IN} < V_{IH}$	**−1**		**1**	μA
MODE	V_{IN} = 0V	**−100**			μA
Output Voltage Levels					
V_{OH}, Logic High	FS_X and FS_R Outputs, I_{OH} = 3 mA	2.4			V
V_{OL}, Logic Low	FS_X and FS_R Outputs, I_{OL} = 5 mA			0.4	V
	$\overline{TS_X}$ Output, I_{OL} = 5 mA			**0.4**	V
Power Dissipation Operating Current	BCLK = 2.048 MHz, All Outputs Open-Circuit		1	**1.5**	mA

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V to ±5%, T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/ or product design and characterization. Typicals specified at V_{CC} = +5.0V, T_A = 25°C.
All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.
See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock	$BCLK_X$, $BCLK_R$, CLK_C	**480**		ns
t_{WCH}	Width of Clock High	$BCLK_X$, $BCLK_R$, CLK_C	**160**		ns
t_{WCL}	Width of Clock Low	$BCLK_X$, $BCLK_R$, CLK_C	**160**		ns
t_{SDC}	Set-Up Time from D_C to CLK_C		**50**		ns
t_{HCD}	Hold Time from CLK_C to D_C		**50**		ns
t_{SCC}	Set-Up Time from $\overline{CS}$ to CLK_C		**30**		ns
t_{HCC}	Hold Time from CLK_C to $\overline{CS}$		**100**		ns
t_{SCHC}	Set-Up Time from Channel Select to CLK_C		**50**		ns
t_{HCHC}	Hold Time from CLK_C to Channel Select		**50**		ns
t_{DBF}	Delay Time from $BCLK_X$ or $BCLK_R$ Low to $FS_{X/R}$ 0–3 High or Low	C_L = 50 pF		**100**	ns
t_{HSYNC}	Hold Time from $BCLK_X$, $BCLK_R$ to Frame Sync		**50**		ns
t_{SSYNC}	Set-Up Time from Frame Sync to $BCLK_X$, $BCLK_R$		**100**		ns
t_{DTL}	Delay from $BCLK_X$ or $BCLK_R$ High to $\overline{TS_X}$ Low	C_L = 50 pF		**140**	ns
t_{DTH}	Delay from $BCLK_X$ or $BCLK_R$ Low to $\overline{TS_X}$ High	R_L = 1k to V_{CC}	**30**	**140**	ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	$BCLK_X$, $BCLK_R$, CLK_C		50	ns

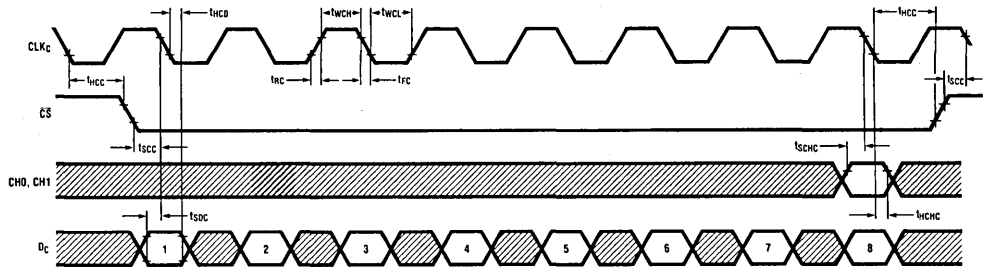
Block Diagram



TL/H/8804–2

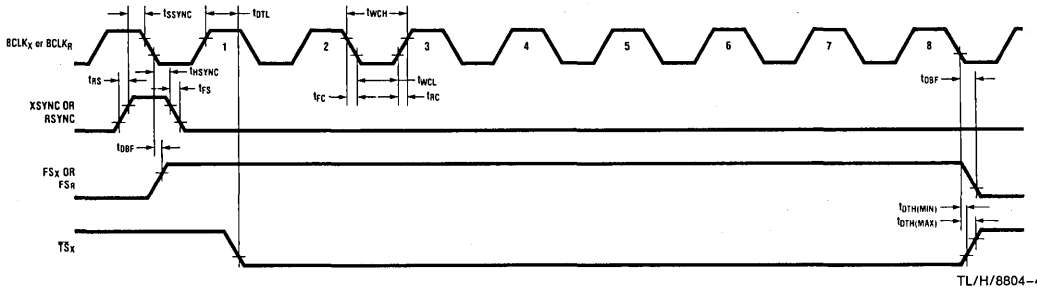
Timing Diagrams

Control Interface



TL/H/8804–3

Output



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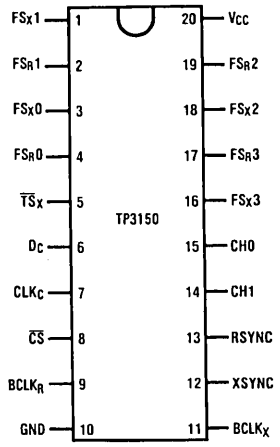
Connection Diagram

Dual-In-Line Package



TL/H/8804–5

Top View

Order Number TP3150J or TP3150N
See NS Package Number J20A or N20A

Pin Descriptions

Symbol	Description
FS_X1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.
FS_R1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.
FS_X0	A transmit frame sync output similar to pin 1.
FS_R0	A receive frame sync output similar to pin 2.
$\overline{TS}_X$	An open-drain N-channel output which is normally high impedance but pulls low during any active transmit time slot.
D_C	The input for an 8-bit serial control word. $\overline{X}$ is the first bit clocked in.
CLK_C	The clock input for the control interface.
$\overline{CS}$	The active-low chip select for the control interface.
$BCLK_R$	The receive bit clock input, which should run at the same rate as that for the CODEC/Filter COMBO, and controls four FS_R outputs.
GND	The 0V ground connection to the device.
$BCLK_X$	The transmit bit clock input, which should run at the same rate as that for the CODEC/Filter COMBO, and controls four FS_X outputs.
XSYNC	The transmit TS0 sync pulse input. Must be synchronous with $BCLK_X$.
RSYNC	The receive TS0 sync pulse input. Must be synchronous with $BCLK_R$.
CH1	The input for the next significant bit of the channel select word.
CH0	The input for the LSB of the channel select word, which defines the frame sync output affected by the following control word.
FS_X3	A transmit frame sync output similar to pin 1.
FS_R3	A receive frame sync output similar to pin 2.
FS_X2	A transmit frame sync output similar to pin 1.
FS_R2	A receive frame sync output similar to pin 2.
V_{CC}	The positive supply to the device. 5V ±5%.

Functional Description

OPERATING MODES

The TP3150 control interface requires an 8-bit serial control word which is compatible with the TP3020/TP3021 and 2910/2911 CODECs. Two bits, $\overline{X}$ and $\overline{R}$, define which of the two groups of frame sync outputs, FS_X0 to FS_X3 or FS_R0 to FS_R3, is affected by the control word, and a 6-bit assignment field specifies the selected time slot, from 0 to 31. A frame sync output is active-high for one time slot, which is always 8 cycles of $BCLK_X$ or $BCLK_R$. A frame may consist of any number of time slots up to 32. If a timeslot is assigned which is beyond the number of time slots in a frame, the FS_X or FS_R output to which it was assigned will remain inactive. Pin 13 is the RSYNC input which defines the start of each receive frame, and the four outputs, FS_R0–FS_R3, are assigned with respect to RSYNC. Pin 12 is the XSYNC input defines the start of each transmit frame and outputs FS_X0–FS_X3 are assigned with respect to XSYNC. XSYNC may have any phase relationship with RSYNC. Inputs CH0 and CH1 select the channel, from 0 to 3 (see Table Ia).

For asynchronous systems the TP3150 provides independent clocking and synchronization for the transmit and receive time slot counters. $BCLK_X$ and XSYNC control four outputs and $BCLK_R$ and RSYNC control four FS_R outputs.

POWER-UP INITIALIZATION

During power-up, all frame sync outputs, FS_X0–FS_X3 and FS_R0–FS_R3, are inhibited and held low. No outputs will go active until a valid time slot assignment is made.

LOADING CONTROL DATA

During the loading of control data, the binary code for the selected channel must be set on inputs CH0 and CH1 (see Table I).

Control data is clocked into the D_C input on the falling edges of CLK_C while $\overline{CS}$ is low.

A new time slot assignment is transferred to the selected assignment register on the high going transition of $\overline{CS}$. The new assignment is re-synchronized to the system clock such that the new FS output pulses will start at the next complete valid time slot after the rising edge of $\overline{CS}$.

TIME SLOT COUNTER OPERATION

At the start of TS0 of each transmit frame, defined by the first falling edge of $BCLK_X$ after XSYNC goes high, the transmit time slot counter is reset to 000000 and begins to increment once every 8 cycles of $BCLK_R$. Each count is compared with the 4 transmit assignment registers and, on finding a match, a frame sync pulse is generated at that FS_X output.

Similarly, the first falling edge of $BCLK_R$ after RSYNC goes high defines the start of receive TS0, and outputs FS_R0–FS_R3 are generated with respect to TS0 when the receive time slot counter matches the appropriate receive assignment register.

$\overline{TS_X}$ OUTPUT

This output pulls low whenever any FS_X output pulse is being generated. At all other times it is open-circuit, allowing the $\overline{TS_X}$ outputs of a number of TSACS to be wire-ANDed together with a common pull-up resistor. This signal can be used to control the TRI-STATE® enable input of a line driver to buffer the transmit PCM bus from the CODEC/Filters to the backplane.

TABLE I. Control Codes (TP3020/TP3021 Compatible)

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

$\overline{X}$ is the first bit clocked into the D_C input.

Control Data Format

T5	T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						:
0	1	1	1	1	0	30
0	1	1	1	1	1	31
1	X	X	X	X	X	(Note 1)

CH1	CH0	Channel Selected
0	0	Assign to FS_x0 and/or FS_R0
0	1	Assign to FS_x1 and/or FS_R1
1	0	Assign to FS_x2 and/or FS_R2
1	1	Assign to FS_x3 and/or FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to both selected FS_X and FS_R
0	1	Assign time slot to selected FS_X only
1	0	Assign time slot to selected FS_R only
1	1	Disable both selected FS_X and FS_R

Note 1: When T5 = 1 then the appropriate FS_X or FS_R output is inactive.

Applications Information

A combination of the TP3150 TSAC and any CODEC/Filter COMBO from the TP3052/3/4/7 or TP3064/7 series will result in data timing as shown in *Figure 1*. Although the FS_X output pulse goes high before $BCLK_X$ goes high, the D_X output of the combo remains in the TRI-STATE mode until both are high. The eight bit period is shortened to prevent a bus clash, just as it is on the TP3020/1 CODECs.

Alternatively, eight full-length bits can be obtained by inverting the BCLK to the combo devices, thereby aligning rising edges of BCLK and $FS_{X/R}$.

Figure 2 shows typical timing for the control data interface.

Figure 3 shows the digital interconnections of a typical line card application.

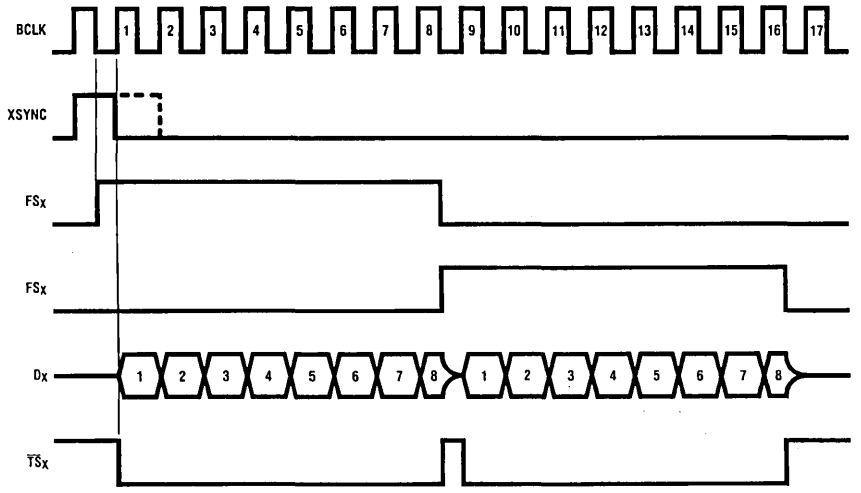


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FIGURE 1. Transmit Data Timing

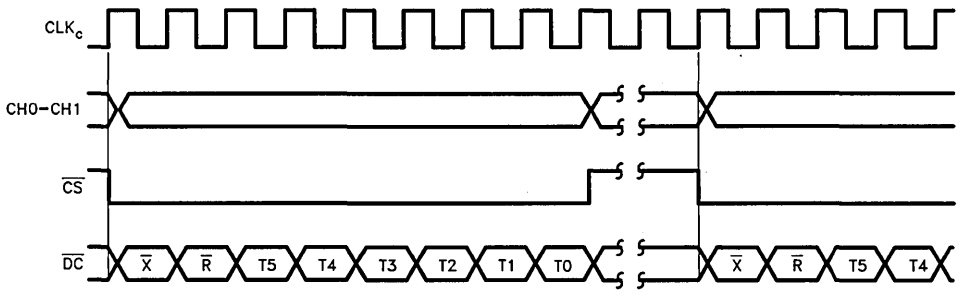

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FIGURE 2. Control Data Timing

Application Information (Continued)

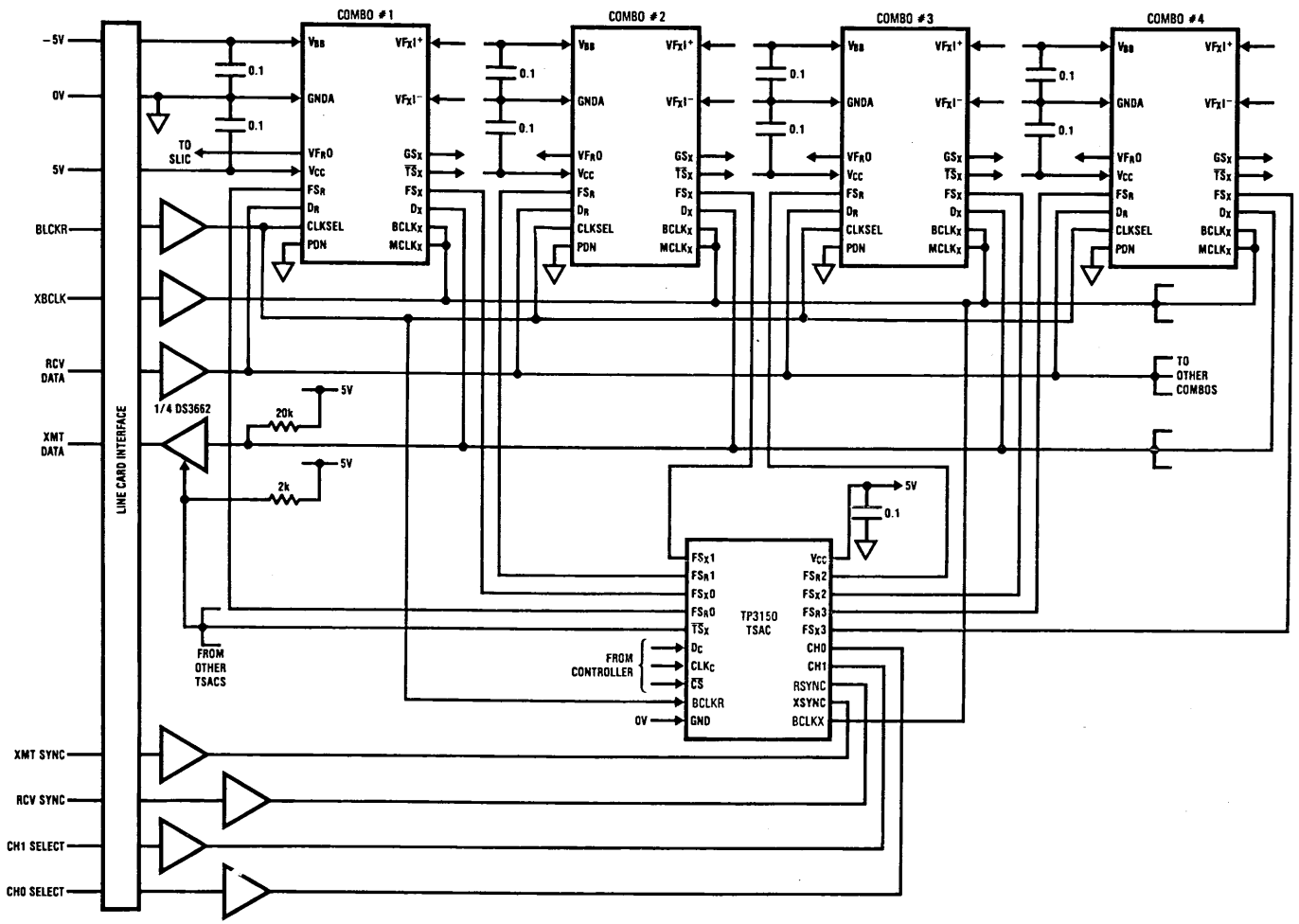

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FIGURE 3. Digital Interconnections on a Typical Synchronous Line Card

National Semiconductor Corporation

microCMOS

TP3155 Time Slot Assignment Circuit

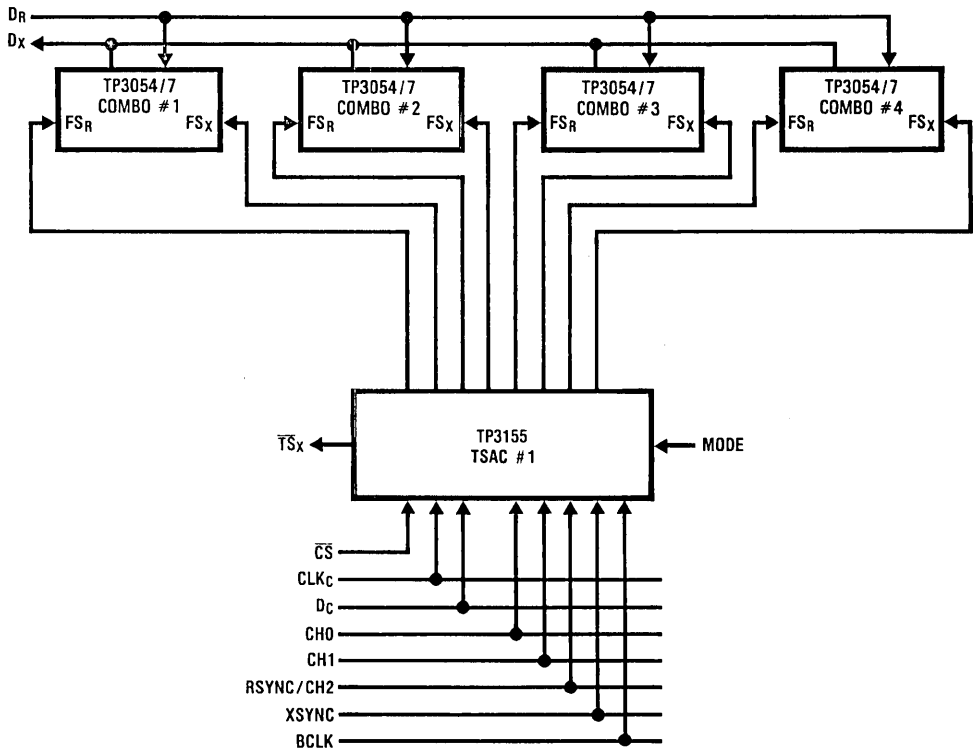
General Description

The TP3155 is a monolithic CMOS logic circuit designed to generate transmit and receive frame synchronization pulses for up to 8 COMBO™ CODEC/Filters. Each frame sync pulse may be independently assigned to a time slot in a frame of up to 32 time slots. Assignments are controlled by loading in an 8-bit word via a simple serial interface port. This control interface is compatible with that used on the TP3020/TP3021 and 2910/2911 CODECs, enabling an easy upgrade to COMBO CODEC/Filters to be made.

Features

- Controls up to 8 COMBO CODEC/Filters
- Independent transmit and receive time slot assignments
- 8-channel unidirectional mode
- Up to 32 time slots per frame
- Serial control interface compatible with TP3020/TP3021 CODECs
- LS TTL and CMOS compatible inputs
- 5 mW, 5V operation

Typical Application



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} Relative to GND 7V

Voltage at Any Input or Output V_{CC} + 0.3V to GND −0.3V

Operating Temperature Range (Ambient) −25°C to +125°C

Storage Temperature Range (Ambient) −65°C to +150°C

Maximum Lead Temperature (Soldering, 10 seconds) 300°C

ESD rating to be determined.

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/ or product design and characterization. Typicals specified at V_{CC} = 5.0V, T_A = 25°C.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Levels					
V_{IH}, Logic High		**2.0**			V
V_{IL}, Logic Low				**0.7**	V
Input Currents					
All Inputs Except MODE	$V_{IL} < V_{IN} < V_{IH}$	**−1**		**1**	μA
MODE	V_{IN} = 0V	**−100**			μA
Output Voltage Levels					
V_{OH}, Logic High	FS_X and FS_R Outputs, I_{OH} = 3 mA	2.4			V
V_{OL}, Logic Low	FS_X and FS_R Outputs, I_{OL} = 5 mA			0.4	V
	TS_X Output, I_{OL} = 5 mA			**0.4**	V
Power Dissipation Operating Current	BCLK = 2.048 MHz, All Outputs Open-Circuit		1	**1.5**	mA

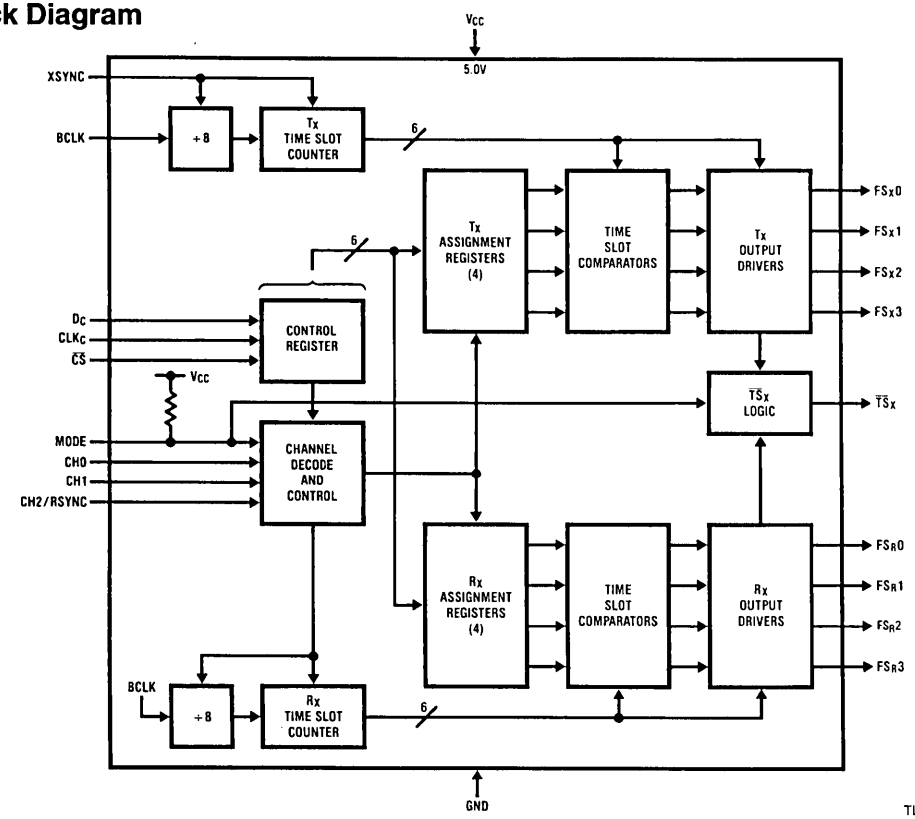
Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/ or product design and characterization. Typicals specified at V_{CC} = 5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock	BCLK, CLK_C	**480**		ns
t_{WCH}	Width of Clock High	BCLK, CLK_C	**160**		ns
t_{WCL}	Width of Clock Low	BCLK, CLK_C	**160**		ns
t_{SDC}	Set-Up Time from D_C to CLK_C		**50**		ns
t_{HCD}	Hold Time from CLK_C to D_C		**50**		ns
t_{SCC}	Set-Up Time from $\overline{CS}$ to CLK_C		**30**		ns
t_{HCC}	Hold Time from CLK_C to $\overline{CS}$		**100**		ns
t_{SCHC}	Set-Up Time from Channel Select to CLK_C		**50**		ns
t_{HCHC}	Hold Time from Channel Select to CLK_C		**50**		ns
t_{DBF}	Delay Time from BCLK Low to $FS_{X/R}$ 0–3 High or Low	C_L = 50 pF		**100**	ns
t_{HSYNC}	Hold Time from BCLK to Frame Sync		**50**		ns
t_{SSYNC}	Set-Up Time from Frame Sync to BCLK		**100**		ns
t_{DTL}	Delay to $\overline{TS_X}$ Low	C_L = 50 pF		**140**	ns
t_{DTH}	Delay to $\overline{TS_X}$ High	R_L = 1k to V_{CC}	**30**	**140**	ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	BCLK, CLK_C		50	ns

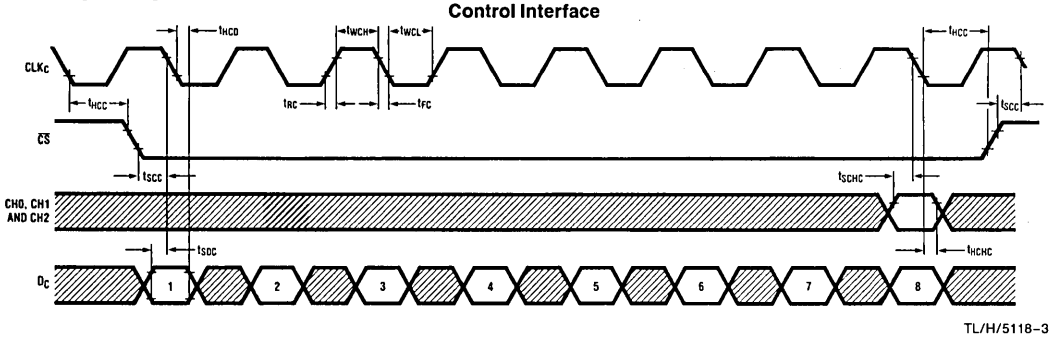
Block Diagram



TL/H/5118–2

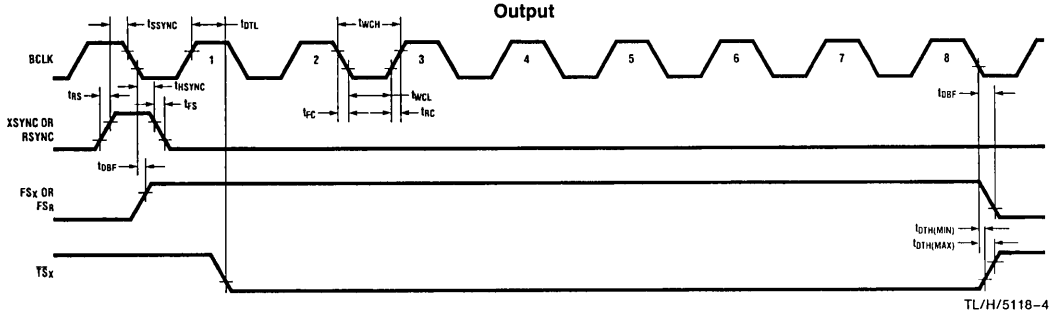
Timing Diagrams

Control Interface



TL/H/5118–3

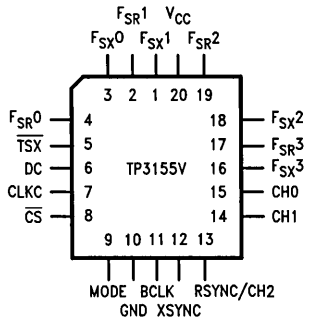
Output



TL/H/5118–4

Connection Diagrams

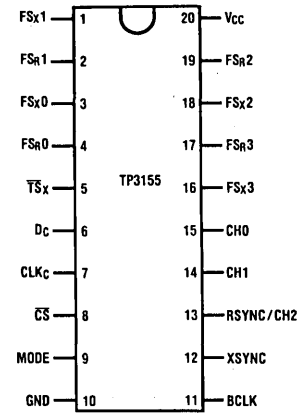
Plastic Chip Carrier (PCC) Package



TL/H/5118-5

Order Number TP3155V
See NS Package Number V20A

Dual-In-Line Package



TL/H/5118-6

Top View

Order Number TP3155J or TP3155N
See NS Package Numbers J20A, N20A

Pin Descriptions

Symbol	Description
FS_X1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.
FS_R1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.
FS_X0	A transmit frame sync output similar to pin 1.
FS_R0	A receive frame sync output similar to pin 2.
$\overline{TS}_X$	An open-drain N-channel output which is normally high impedance but pulls low during any active transmit time slot.
D_C	The input for an 8-bit serial control word. $\overline{X}$ is the first bit clocked in.
CLK_C	The clock input for the control interface.
$\overline{CS}$	The active-low chip select for the control interface.
MODE	The mode select input. When left open-circuit or connected to V_{CC}, mode 1 is selected, and when connected to GND, mode 2 is selected.
GND	The 0V ground connection to the device.
BCLK	The bit clock input, which should run at the same rate as that for the COMBO CODEC/Filter COMBO.
XSYNC	The transmit TS0 sync pulse input. Must be synchronous with BCLK.
RSYNC/CH2	The function of this input is determined by the MODE input (pin 9). In mode 1 this is the receive TS0 sync pulse, RSYNC, which must be synchronous with BCLK. In mode 2 this is the CH2 input for the MSB of the channel select word.
CH1	The input for the next significant bit of the channel select word.
CH0	The input for the LSB of the channel select word, which defines the frame sync output affected by the following control word.
FS_X3	A transmit frame sync output similar to pin 1.
FS_R3	A receive frame sync output similar to pin 2.
FS_X2	A transmit frame sync output similar to pin 1.
FS_R2	A receive frame sync output similar to pin 2.
V_{CC}	The positive supply to the device. 5V ±5%.

Functional Description

OPERATING MODES

The TP3155 control interface requires an 8-bit serial control word which is compatible with the TP3020/TP3021 and 2910/2911 CODECs. Two bits, $\overline{X}$ and $\overline{R}$, define which of the two groups of frame sync outputs, FS_X0 to FS_X3 or FS_R0 to FS_R3, is affected by the control word, and a 6-bit assignment field specifies the selected time slot, from 0 to 31. A frame sync output is active-high for one time slot, which is always 8 cycles of BCLK. A frame may consist of any number of time slots up to 32. If a timeslot is assigned which is beyond the number of time slots in a frame, the FS_X or FS_R output to which it was assigned will remain inactive.

Two modes of operation are available. Mode 1 is for systems requiring different time slot assignments for the transmit and receive direction of each channel. Mode 1 is selected by leaving pin 9 (MODE) open-circuit or connecting it to V_{CC}. In this case, Pin 13 is the RSYNC input which defines the start of each receive frame, and the four outputs, FS_R0–FS_R3, are assigned with respect to RSYNC. The XSYNC input defines the start of each transmit frame and outputs FS_X0–FS_X3 are assigned with respect to XSYNC. XSYNC may have any phase relationship with RSYNC. Inputs CH0 and CH1 select the channel, from 0 to 3 (see Table Ia).

Mode 2 provides the option of assigning all 8 frame sync outputs with respect to the XSYNC input. Mode 2 is selected by connecting pin 9 (MODE) to GND. This makes the TP3155 TSAC useful for either an 8-channel undirectional controller or for systems in which the transmit and receive directions of each channel are always assigned to the same time slot as the other, i.e., the FS_X and FS_R inputs on the COMBO CODEC/Filter are hard-wired together. In this case, logical selection of the channel to be assigned is made via inputs CH0, CH1 and CH2 (see Table Ib).

POWER-UP INITIALIZATION

During power-up, all frame sync outputs, FS_X0–FS_X3 and FS_R0–FS_R3, are inhibited and held low. No outputs will go active until a valid time slot assignment is made.

LOADING CONTROL DATA

During the loading of control data, the binary code for the selected channel must be set on inputs CH0 and CH1 (and CH2 in mode 2), see Tables Ia and Ib.

Control data is clocked into the D_C input on the falling edges of CLK_C while $\overline{CS}$ is low.

A new time slot assignment is transferred to the selected assignment register on the high going transition of $\overline{CS}$. The new assignment is re-synchronized to the system clock such that the new FS output pulses will start at the next complete valid time slot after the rising edge of $\overline{CS}$.

TIME SLOT COUNTER OPERATION

At the start of TS0 of each transmit frame, defined by the first falling edge of BCLK after XSYNC goes high, the transmit time slot counter is reset to 000000 and begins to increment once every 8 cycles of BCLK. Each count is compared with the 4 transmit assignment registers and, on finding a match, a frame sync pulse is generated at that FS_X output.

Similarly, the first falling edge of BCLK after RSYNC goes high defines the start of receive TS0, and outputs FS_R0–FS_R3 are generated with respect to TS0 when the receive time slot counter matches the appropriate receive assignment register.

$\overline{TS_X}$ OUTPUT

In mode 1 (separate transmit and receive assignments), this output pulls low whenever any FS_X output pulse is being generated. In mode 2, this output pulls low whenever any FS_X or FS_R output is being generated. At all other times it is open-circuit, allowing the $\overline{TS_X}$ outputs of a number of TSACS to be wire-ANDed together with a common pull-up resistor. This signal can be used to control the TRI-STATE® enable input of a line driver to buffer the transmit PCM bus from the CODEC/Filters to the backplane.

TABLE Ia. Control Mode 1 (TP3020/TP3021 Compatible)

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

$\overline{X}$ is the first bit clocked into the D_C input.

Control Data Format

T5	T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						:
0	1	1	1	1	0	30
0	1	1	1	1	1	31
1	X	X	X	X	X	(Note 1)

CH1	CH0	Channel Selected
0	0	Assign to FS_x0 and/or FS_R0
0	1	Assign to FS_x1 and/or FS_R1
1	0	Assign to FS_x2 and/or FS_R2
1	1	Assign to FS_x3 and/or FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to both selected FS_X and FS_R
0	1	Assign time slot to selected FS_X only
1	0	Assign time slot to selected FS_R only
1	1	Disable both selected FS_X and FS_R

TABLE Ib. Control Mode 2

CH2	CH1	CH0	Channel Selected
0	0	0	Assign to FS_X0
0	0	1	Assign to FS_X1
0	1	0	Assign to FS_X2
0	1	1	Assign to FS_X3
1	0	0	Assign to FS_R0
1	0	1	Assign to FS_R1
1	1	0	Assign to FS_R2
1	1	1	Assign to FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to selected output
0	1	
1	0	
1	1	Disable selected output

Note 1: When T5 = 1, then the appropriate FS_X or FS_R output is inactive.

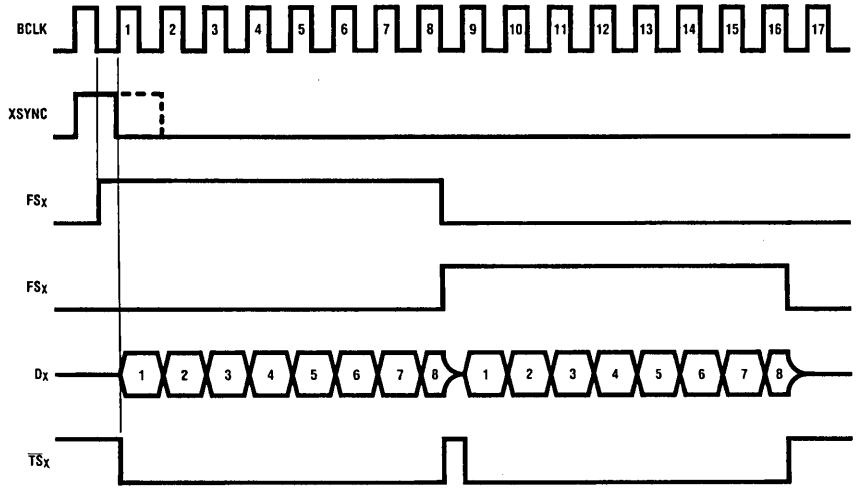
Applications Information

A combination of the TP3155 TSAC and any CODEC/Filter COMBO from the TP3052/3/4/7 or TP3064/7 series will result in data timing as shown in *Figure 1*. Although the FS_X output pulse goes high before BCLK goes high, the D_X output of the combo remains in the TRI-STATE mode until both are high. The eight bit period is shortened to prevent a bus clash, just as it is on the TP3020/1 CODECs.

Alternatively, eight full-length bits can be obtained by inverting the BCLK to the combo devices, thereby aligning rising edges of BCLK and $FS_{X/R}$.

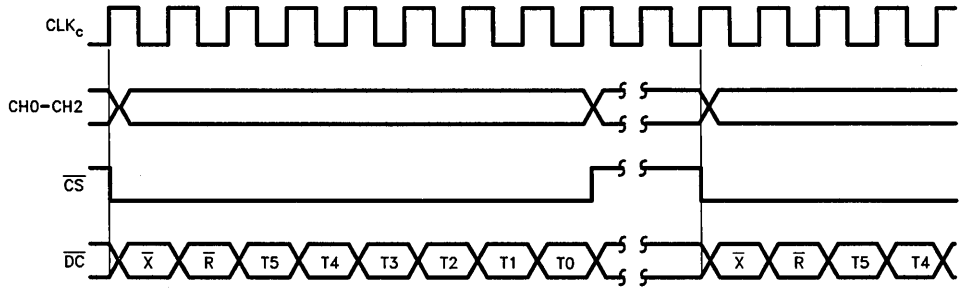
Figure 2 shows typical timing for the control data interface.

Figure 3 shows the digital interconnections of a typical line card application.



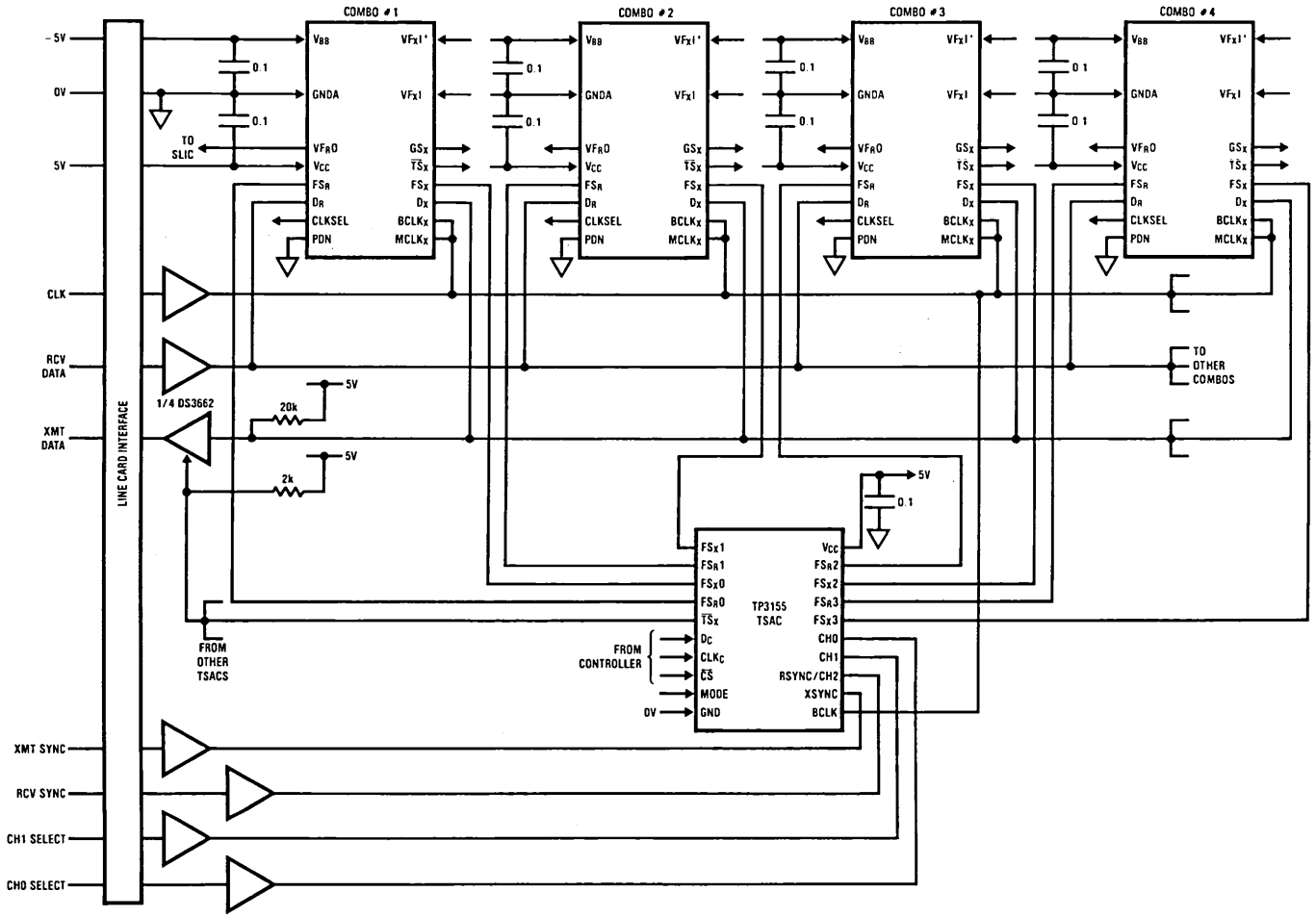
TL/H/5118–7

FIGURE 1. Transmit Data Timing



TL/H/5118–8

FIGURE 2. Control Data Timing



TL/H/5118-9

FIGURE 3. Digital Interconnections on a Typical Synchronous Line Card

National Semiconductor Corporation

microCMOS

TP3020/TP3020-1/TP3021/TP3021-1 Monolithic CODECs

General Description

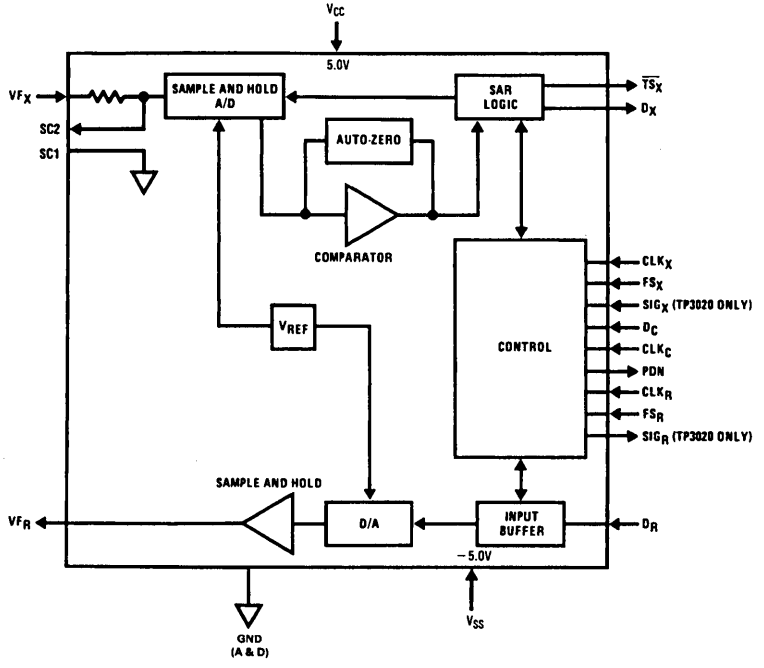
The TP3020 and TP3021 are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP3020 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The TP3021 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the TP3020/TP3021 may be operated in a fixed time slot mode. Both devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- Low operation power—45 mW typical
- Low standby power—1 mW typical
- ±5V operation
- TTL compatible digital interface
- Time slot assignment or alternate fixed time slot modes
- Internal precision reference
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP3020—μ-law coding with signaling capabilities
- TP3021—A-law coding
- Synchronous or asynchronous operation

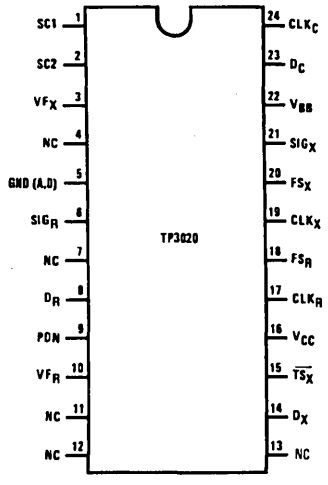
Simplified Block Diagram



TL/H/5538–1

Connection Diagrams

Dual-In-Line Package

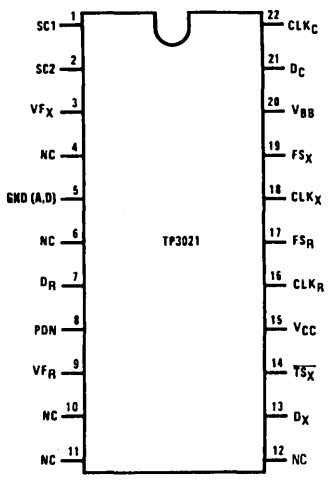


TL/H/5538-3

Top View

Order Number TP3020J or TP3020J-1
See NS Package Number J24A

Dual-In-Line Package



TL/H/5538-4

Top View

Order Number TP3021J or TP3021J-1
See NS Package Number J22A

Description of Pin Functions

Symbol	Function
SC1	Internally connected to GNDA.
SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatibility.
VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
GND	Analog and digital ground. All analog and digital signals are referenced to this pin.
SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output—SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel.
VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μS after the end of the decode time slot.

Symbol	Function
NC	Unused
D_X	Serial PCM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
V_{CC}	5V (±5%) Power Supply.
CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MH_z, 1.544 MH_z or 2048 MHz. May be asynchronous with CLK_X or CLK_C.
FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.

Description of Pin Functions (Continued)

Symbol	Function
SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
V_{BB}	−5V (±5%) input.
D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3020/TP3021 into the fixed time slot mode.

Absolute Maximum Ratings

Operating Temperature	−25°C to + 125°C
Storage Temperature	−65°C to + 150°C
V_{CC} with Respect to GND	7V
V_{BB} with Respect to GND	−7V
ESD rating is to be determined.	
Voltage at Any Analog Input or Output	V_{BB} −0.3V to V_{CC} + 0.3V
Voltage at Any Digital Input or Output	GND −0.3V to V_{CC} + 0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V and T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0 < V_{IN} < V_{CC}$	**−10**		**10**	μA
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_{OL} = 4.0 mA			**0.4**	V
		SIG_R, I_{OL} = 0.5 mA			**0.4**	V
		$\overline{TS}_X$, I_{OL} = 3.2 mA, Open Drain			**0.4**	V
		PDN, I_{OL} = 1.6 mA			**0.4**	V
V_{OH}	Output High Voltage	D_X, I_{OH} = 6 mA	**2.4**			V
		SIG_R, I_{OH} = 0.6 mA	**2.4**			V
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2.0			kΩ
Z_O	Output Impedance at VF_R	$-3.1V < VF_R < 3.1V$		10	20	Ω
V_{OS}	Output Offset Voltage at VF_R	D_R = PCM Zero Code (TP3020) or Alternating ± 1 Code (TP3021)	**−25**		**25**	mV
I_{IN}	Analog Input Bias Current	V_{IN} = 0V	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				160	kΩ
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}			0.1	**0.4**	mA
I_{BB0}	Standby Current, V_{BB}			0.03	**0.1**	mA
I_{CC1}	Operating Current, V_{CC}			4.5	**8.0**	mA
I_{BB1}	Operating Current, V_{BB}			4.5	**8.0**	mA

AC Electrical Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected. Limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP3020 and TP3021 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the TP3020/TP3021 are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute TP3020, TP3021 TP3020-1, TP3021-1	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	 **−0.125** **−0.175**		 **0.125** **0.175**	 dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%	**−0.07**		**0.07**	dB
G_{XA}	Transmit Gain, Absolute TP3020, TP3021 TP3020-1, TP3021-1	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	 **−0.325** **−0.375**		 **−0.075** **−0.025**	 dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%	**−0.07**		**0.07**	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−1.0**		 **0.3** **0.2** **0.4** **1.0**	 dB dB dB dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−1.0**		 **0.3** **0.2** **0.4** **1.0**	 dB dB dB dB
S/D_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBc dBc dBc
S/D_x	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBc dBc dBc
N_R	Receive Idle Channel Noise	D_R = Steady State PCM Code			**6**	dBrnc0
N_x	Transmit Idle Channel Noise	TP3020, (No Signaling) TP3021 (Note 1)			**13** **−66***	dBrnc0 dBn0p
HD_R	Receive Harmonic Distortion	2nd or 3rd Harmonic			**−47**	dB
HD_x	Transmit Harmonic Distortion	2nd or 3rd Harmonic			**−47**	dB
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, V_{CC} = 5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**50**			dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0 level.

AC Electrical Characteristics (Continued)

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected. Limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{CC} = 5.0 V_{DC} + 300 mVrms, F = 1.02 kHz	**40**			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**50**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = = 1.02 kHz	**45**			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			**−75**	dB
CT_{RX}	Receive to Transmit Crosstalk	Transmit Input Level = 0V TP3020 TP3021			 **−70** **−65** (Note 2)	 dB dB

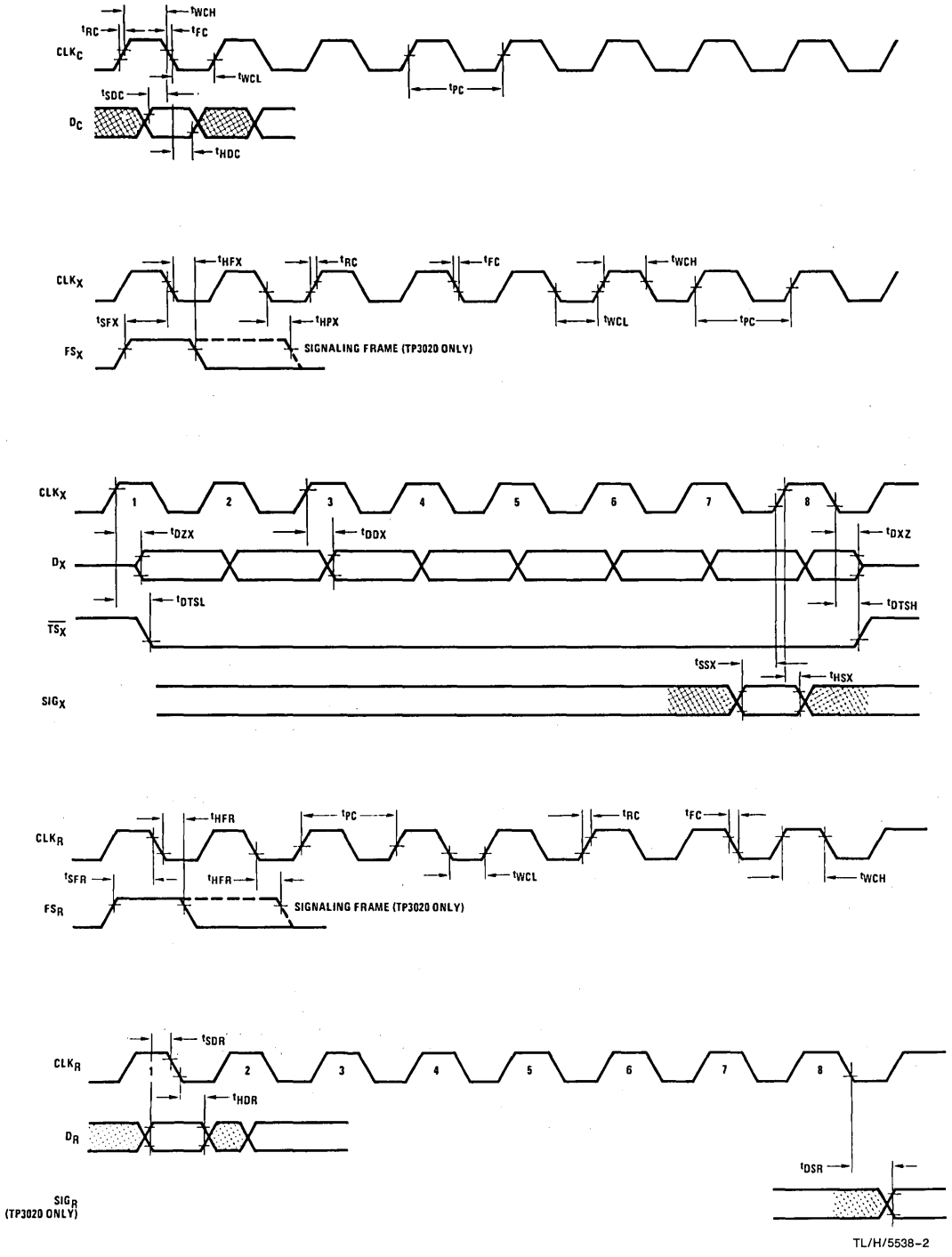
Note 2: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Timing Specification

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All digital signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PC}	Period of Clock	CLK_C, CLK_R, CLK_X	**485**			ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	CLK_C, CLK_R, CLK_X			30	ns
t_{WCH}	Width of Clock High	CLK_C, CLK_R, CLK_X	**165**			ns
t_{WCL}	Width of Clock Low	CLK_C, CLK_R, CLK_X	**165**			ns
$t_{A/D}$	A/D Conversion Time	From End of Encoder Time Slot to Completion of Conversion			**16**	Time Slots
$t_{D/A}$	D/A Conversion Time	From End of Decoder Time Slot to Transition of VF_R			**2**	Time Slots
t_{SDC}	Set-Up Time, D_C to CLK_C		**100**			ns
t_{HDC}	Hold Time, CLK_C to DC		**100**			ns
t_{SFX}	Set-Up Time, FS_X to CLK_X		**100**			ns
t_{HFX}	Hold Time, CLK_X to FS_X		**100**			ns
t_{DZX}	Delay Time to Enable D_X on TS Entry	C_L = 150 pF	25		125	ns
t_{DDX}	Delay Time, CLK_X to D_X	C_L = 150 pF			**125**	ns
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	C_L = 0 pF	50		165	ns
t_{DTSL}	Delay to $\overline{TS}_X$ Low	0 ≤ C_L ≤ 150 pF	30		185	ns
t_{DTSH}	Delay to $\overline{TS}_X$ Off	C_L = 0 pF	30		185	ns
t_{SSX}	Set-Up Time, SIG_X to CLK_X		**100**			ns
t_{HSX}	Hold Time, CLK_X to SIG_X		**100**			ns
t_{SFR}	Set-Up Time, FS_R to CLK_R		**100**			ns
t_{HFR}	Hold Time, CLK_R to FS_R		**100**			ns
t_{SDR}	Set-Up Time, D_R to CLK_R		**40**			ns
t_{HDR}	Hold Time, CLK_R to D_R		**30**			ns
t_{DSR}	Delay Time, CLK_R to SIG_R	C_L = 100 pF			300	ns

Timing Waveforms



TL/H/5538–2

Functional Description

POWER-UP

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or −5V is required. In the power-down mode, all non-essential circuits are deactivated, the TRI-STATE PCM data output D_X is placed in the high impedance state and the receive signaling output of the TP3020, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the TP3020/TP3021 depends on the chosen mode of operation, time slot assignment or fixed time slot.

TIME SLOT ASSIGNMENT MODE

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μS or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequent control bits B3−B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputted during the previously assigned time slot which may now be assigned to another CODEC.

FIXED TIME SLOT MODE

There are several ways in which the TP3020/TP3021 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

SERIAL CONTROL PORT

When the TP3020/TP3021 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	Action
0	0	Assign time slot to encoder and decoder
0	1	Assign time slot to encoder
1	0	Assign time slot to decoder
1	1	Power-down CODEC

B3	B4	B5	B6	B7	B8	Time Slot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

SIGNALING

The TP3020 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "½" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

Functional Description (Continued)

ENCODING DELAY

The encoding process begins at the start of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μS later, resulting in an encoding delay of 125 μS. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz clock, the FS rate could be increased to 15 kHz reducing the delay from 125 μS to 67 μS.

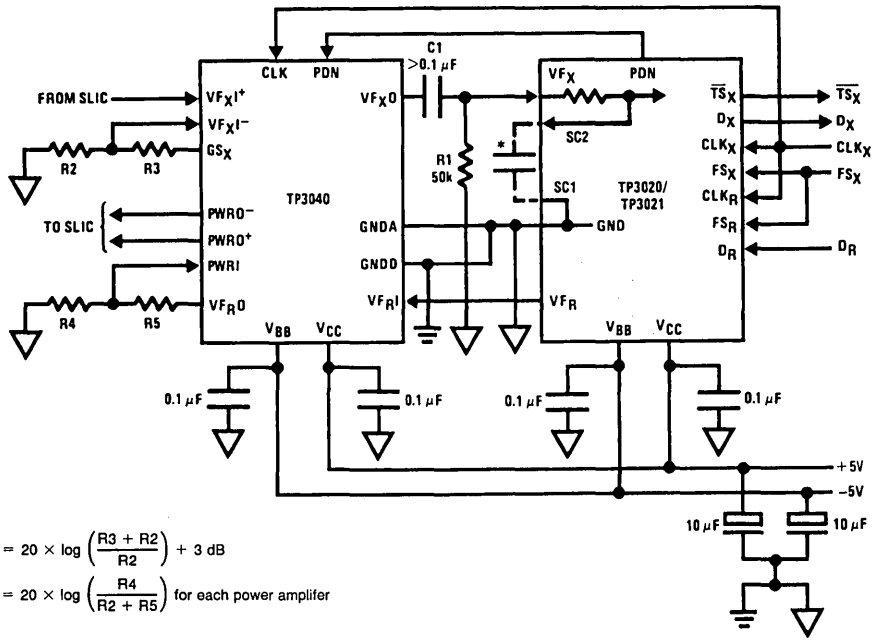
DECODING DELAY

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81 μS for a 1.544 MHz system with an 8 kHz frame rate or 76 μS for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

TYPICAL APPLICATION

A typical application of the TP3020/TP3021 used in conjunction with the TP3040 PCM filter is shown. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should not exceed 160 kΩ, and the product R1 × C1 should exceed 4 rms. 0.1 μf power supply bypass capacitors should be used and placed as close to the device as possible.

Typical Application



XMT gain = $20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3$ dB

RCV gain = $20 \times \log\left(\frac{R4}{R2 + R5}\right)$ for each power amplifer

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The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of the TP3020/TP3021/TP3040, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

*The external sample/hold capacitor required for use with pin-compatible NMOS CODECs introduces attenuation due to the capacitive divider formed with C1. The SC pin connects VF_X to this sample/hold capacitor (via a 300Ω resistor) to ensure gain compatibility. The TP3020/TP3021 itself does not require an external sample/hold capacitor.

National Semiconductor Corporation

microCMOS

TP5116A/TP5116A-1/TP5156A/TP5156A-1 Monolithic CODECs

General Description

The TP5116A and TP5156A are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP5116A is intended for μ-law applications and the TP5156A is for A-law applications.

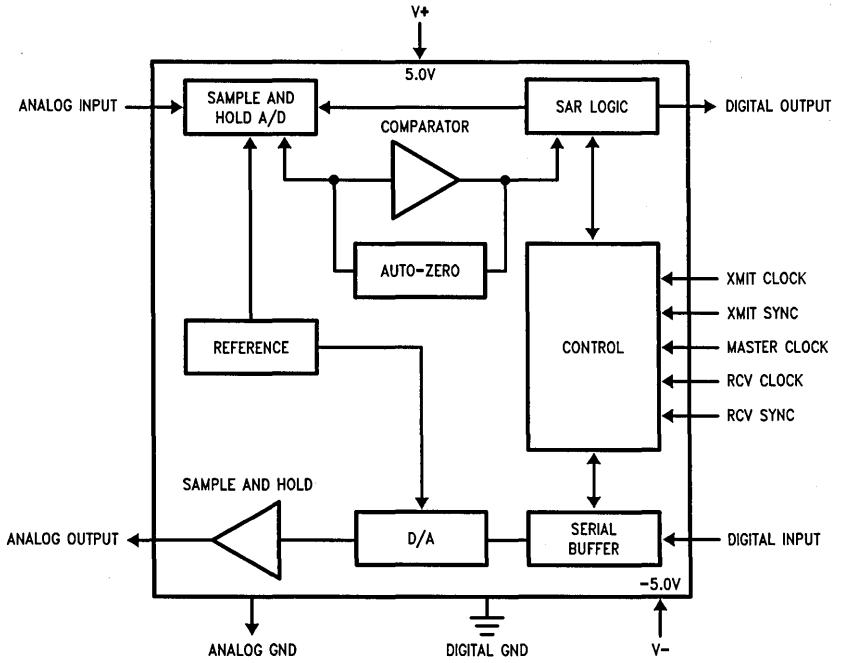
Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, and internal auto-zero circuits. Each device also contains a precision internal voltage reference, eliminating the need for an external reference. There are no internal connections to pins 15 or 16, making them directly interchangeable with CODECs using external reference components.

All devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder, smooths the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- TP5116A—μ-law coding (sign plus magnitude format)
- TP5156A—A-law coding
- Synchronous or asynchronous operation
- Precision voltage reference on-chip
- Internal sample-and-hold capacitors
- Internal auto-zero circuit
- Low operation power—40 mW typical
- ±5V operation
- TTL compatible digital interface

Simplified Block Diagram



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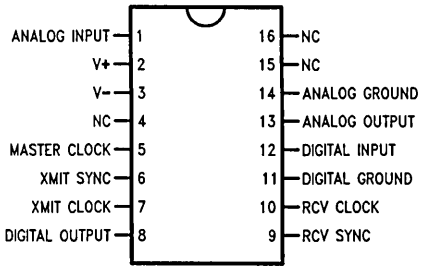
Connection Diagram

Dual-In-Line Package



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Top View

Order Number TP5116AJ or TP5156AJ
See NS Package Number J16A

Description of Pin Functions

Symbol	Function
ANALOG INPUT	ANALOG INPUT to the encoder. This signal will be sampled at the beginning of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
V^+	5V(±5%) Power Supply.
V^-	−5V(±5%) Power Supply.
NC	Unused.
MASTER CLOCK	MASTER CLOCK input used to operate the internal encode and decode sequencers. Should be 1.536 MHz, 1.544 MHz or 2.048 MHz.
XMIT SYNC	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight XMIT CLOCK cycles wide.
XMIT CLOCK	Transmit bit clock input used to shift out the PCM data on DIGITAL OUTPUT. May operate from 64 kHz to 2.048 MHz. May be asynchronous with RCV CLOCK.
DIGITAL OUTPUT	Serial PCM TRI-STATE output from encoder. During the encoder time slot, the PCM code for the previous sample of ANALOG INPUT is shifted out, most significant bit first, on the rising edge of XMIT CLOCK.
RCV SYNC	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight RCV CLOCK cycles wide.
RCV CLOCK	Receive bit clock input used to shift in the PCM data on DIGITAL INPUT. May operate from 64 kHz to 2.048 MHz. May be asynchronous with XMIT CLOCK.
DIGITAL GROUND	All digital levels referenced to the DIGITAL GROUND pin.
DIGITAL INPUT	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into DIGITAL INPUT, most significant bit first, on the rising edge of RCV CLOCK.
ANALOG OUTPUT	ANALOG OUTPUT from the decoder. The decoder sample and hold amplifier is updated approximately 15 μs after the end of the decode time slot.
ANALOG GROUND	All analog signals are referenced to the ANALOG GROUND pin.

ENCODING FORMAT AT DIGITAL OUTPUT

	TP5116A Sign + Magnitude								TP5156A A-Law (Includes Even Bit Inversion)							
V_{IN} = +Full-Scale	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1
	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
V_{IN} = −Full-Scale	0	1	1	1	1	1	1	1	0	0	1	0	1	0	1	0

Functional Description

Approximately 4 μs after the rising edge of the XMIT SYNC pulse, the voltage present on the ANALOG INPUT is sampled and the process of encoding that sample into a PCM code is begun. Simultaneously, the 8-bit PCM code corresponding to the previous sample is shifted out of the DIGITAL OUTPUT, MSB first, on the rising edge of the next eight cycles of the XMIT CLOCK. When XMIT SYNC (which is normally eight XMIT CLOCK cycles long) goes low, the TRI-STATE DIGITAL OUTPUT is returned to the high impedance state. On the TP5116A, the PCM code is in a μ-law sign plus magnitude format. The TP5156A uses the standard A-law coding.

An 8-bit PCM code is shifted into DIGITAL INPUT on the rising edge of the first eight RCV CLOCK pulses after RCV SYNC goes high. RCV SYNC is nominally eight RCV CLOCK cycles wide. Approximately 15 μs after RCV SYNC goes low, the ANALOG OUTPUT is updated to the voltage corresponding to the PCM input code.

All encoding and decoding operations are run from the MASTER CLOCK. MASTER CLOCK should be in the range of 1.536 MHz to 2.048 MHz and must be synchronous with XMIT CLOCK. The XMIT and RCV CLOCK may vary from 64 kHz to 2.048 MHz.

ENCODING DELAY

The encoding process begins immediately at the beginning of the encode time slot and is concluded no later than 18 time slots later. In normal applications, the PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125 μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz MASTER CLOCK, the FS rate could be increased to 15 kHz, reducing the delay from 125 μs to 67 μs.

DECODING DELAY

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 MASTER CLOCK cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or, 81 μs for a 1.544 MHz system with an 8 kHz frame rate or, 76 μs for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

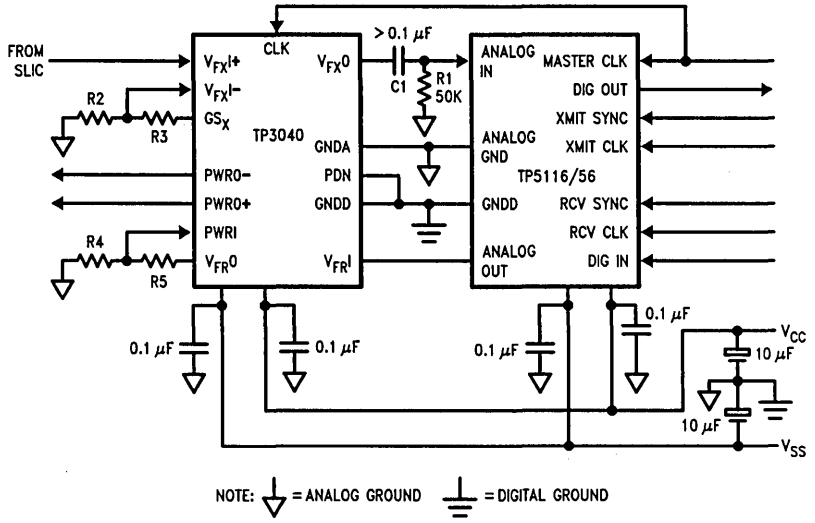
Typical Application

A typical application of these CODECs used in conjunction with the TP3040 PCM filter is shown below. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should be less than 50 kΩ, and the product R1×C1 should exceed 4 ms.

$$\text{XMIT GAIN} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\ \text{dB}$$

$$\text{RCV GAIN} = 20 \times \log\left(\frac{R4}{R4 + R5}\right)$$

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of these CODECs, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines. For card insertion into a hot connector, care should be taken to insure that GNDA and GNDD are contacted prior to V_{CC} and V_{BB}.



TL/H/6663–5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Operating Temperature	−25°C to +125°C
Storage Temperature	−65°C to +150°C
V^+ with Respect to DIGITAL GROUND	7V
V^- with Respect to DIGITAL GROUND	−7V
Voltage at Any Analog Input or Output	V^- −0.3V to V^+ +0.3V
Voltage at Any Digital Input or Output	GNDD −0.3V to V^+ + 0.3V
Lead Temperature (Solderdip 10 sec.)	300°C

ESD rating to be determined.

DC Electrical Characteristics

Unless otherwise noted T_A = 0°C to 70°C, V^+ = 5.0V ±5%, V^- = −5.0V ±5%. Typical characteristics are specified at V^+ = 5.0V,V^- = −5.0V and T_A = 25°C. All digital signals are referenced to DIGITAL GROUND. All analog signals are referenced to ANALOG GROUND. Limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0V<V_{IN}<V^+$	**−10**		**10**	μA
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 6 mA	2.4			V
ANALOG INTERFACE						
Z_I	Analog Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2			kΩ
Z_O	Output Impedance at Analog Output			10	20	Ω
I_{IN}	Analog Input Bias Current	V_{IN} = 0V	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				50	kΩ
POWER DISSIPATION						
I_{CC1}	Operating Current, V_{CC}			3.5	**8.0**	mA
I_{BB1}	Operating Current, V_{BB}			3.5	**8.0**	mA

AC Electrical Characteristics

Unless otherwise noted, T_A = 25°C, V^+ = 5.0V,V^- = −5.0V. The analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL INPUT is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected, limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP5116A is 1.227 Vrms and 1.231 Vrms for the TP5156A. The resulting nominal overload level is 2.5V peak for all devices. All gain measurements for the encode and decode portions of the devices are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute	T_A = 25°C, V^+ = 5V, V^- = −5V TP5116A, TP5156A TP5116A-1, TP5156A-1	 **−0.125** **−0.175**		 **0.125** **0.175**	 dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T_A = 0°C to 70°C	−0.05		0.05	dB

AC Electrical Characteristics (Continued)

Unless otherwise noted, T_A = 25°C, V^+ = 5.0V, V^- = −5.0V. The analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL INPUT is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected. Limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V^+ = 5V ±5%, V^- = −5V±5%	−0.07		0.07	dB
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, V^+ = 5V, V^- = −5V TP5116A, TP5156A TP5116A-1, TP5156A-1	**−0.125** **0.175**		**0.125** **0.175**	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T_A = 0°C to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V^+ = 5V ±5%, V^- = −5V ±5%	−0.07		0.07	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−1.0**		 **0.3** **0.2** **0.4** **1.0**	 dB dB dB dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 TP5116A, TP5156A TP5116A-1, TP5156A-1 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−0.475** **−1.0**		 **0.3** **0.2** **0.4** **0.475** **1.0**	 dB dB dB dB dB
STD_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBC dBC dBC
STD_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBC dBC dBC
N_R	Receive Idle Channel Noise	D_R = Idle Code			**8**	dBrnC0
N_X	Transmit Idle Channel Noise	TP5116A, VF_X = 0V TP5156A, VF_x = 0V			**13** **−66**	dBrnC0 dBm0p
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, V_{CC} = 5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**50**			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Idle Code V_{CC} = 5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**40**			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**50**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**45**			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			**−75**	dB
CT_{RX}	Receive to Transmit Crosswalk	Transmit Input Level = 0V TP5116A TP5156A			**−70** **−65** (Note 2)	dB dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0 level.

Note 2: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Timing Specifications

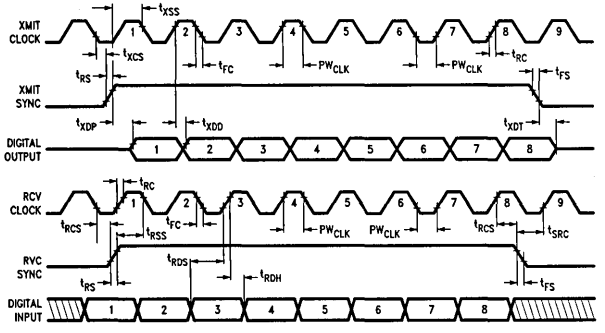
Unless otherwise noted, T_A = 0°C to 70°C, V^+ = +5V±5%, V^- = −5V ± 5%. All digital signals are referenced to DIGITAL GROUND and are measured at V_{IH} and V_{IL} as indicated in the Timing Waveforms. Limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All timing specifications measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_M	MASTER CLOCK Frequency		1.5	2.048	2.1	MHz
F_X, F_R	XMIT, RCV CLOCK Frequency		0.064	2.048	2.1	MHz
PW_{CLK}	Clock Pulse Width	MASTER, XMIT, RCV CLOCKS	150			ns
t_{RC}, t_{FC}	Clock Rise and Fall Time	MASTER, XMIT, RCV CLOCKS			50	ns
t_{RS}, t_{FS}	Sync Pulse Rise and Fall Time	RCV, XMIT, SYNC			50	ns
t_{RCS}, t_{XCS}	Clock to Sync Delay	RCV, XMIT	0			ns
t_{XSS}	XMIT SYNC Set-Up Time		150			ns
t_{XDD}	XMIT Data Delay	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDP}	XMIT Data Present	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDT}	XMIT Data TRI-STATE®				150	ns
t_{SRC}	RCV CLOCK to RCV SYNC Delay		0			ns
t_{RDS}	RCV Data Set-Up Time		0			ns
t_{RSS}	RCV SYNC Set-Up Time		150			ns
t_{RDH}	RCV Data Hold Time		100			ns
t_{XSL}	XMIT SYNC Low Time	64 kHz Operation	300			ns
t_{RSL}	RCV SYNC Low Time	64 kHz Operation	17			(Note 3)

Note 3: RCV SYNC must remain low for at least 17 cycles of MASTER CLOCK, each frame.

Timing Waveforms

72 kHz or Greater Operation



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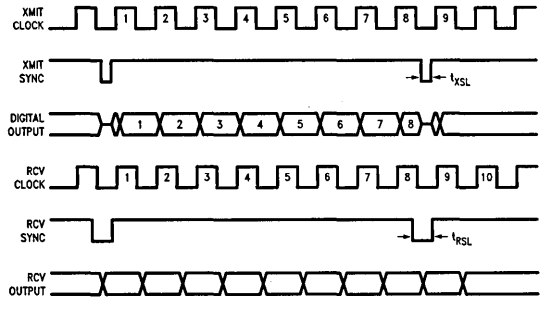
64 kHz Operation



TL/H/6663-4

National Semiconductor Corporation

microCMOS

TP3040/TP3040-1/TP3040A/TP3040A-1 PCM Monolithic Filter

General Description

The TP3040/TP3040-1/TP3040A/TP3040A-1 filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using microCMOS technology and switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

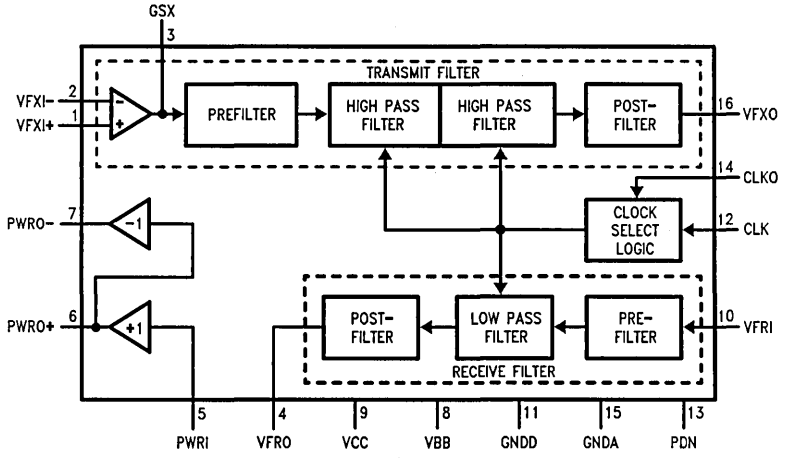
RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Features

- Exceeds all D3/D4 and CCITT specifications
- +5V, −5V power supplies
- Low power consumption:
  45 mW (0 dBm0 into 600Ω)
  30 mW (power amps disabled)
- Power down mode: 0.5 mW
- 20 dB gain adjust range
- No external anti-aliasing components
- Sin x/x correction in receive filter
- 50/60 Hz rejection in transmit filter
- TTL and CMOS compatible logic
- All inputs protected against static discharge due to handling

Block Diagram



TL/H/6660–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltages	±7V
Power Dissipation	1 W/Package
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	−25°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating to be determined	

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C. Clock frequency is 2.048 MHz. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	V_{CC} = 5.25V, V_{BB} = −5.25V, CLK0 (Pin 14) = −5.25V All other pins at GND (0V)				
		TP3040, TP3040A		50	**100**	µA
		TP3040-1, TP3040A-1			**400**	µA
I_{BB0}	V_{BB} Standby Current	V_{CC} = 5.25V, V_{BB} = −5.25V, CLK0 (Pin 14) = −5.25V All other pins at GND (0V)				
		TP3040, TP3040A		50	**100**	µA
		TP3040-1, TP3040A-1			**400**	µA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	**4.0**	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	**4.0**	mA
I_{CC2}	V_{CC} Operating Current	(Note 1)		4.6	**6.4**	mA
I_{BB2}	V_{BB} Operating Current	(Note 1)		4.6	**6.4**	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \le V_{IN} \le V_{CC}$	**−10**		**10**	µA
I_{INP}	Input Current, PDN	$V_{BB} \le V_{IN} \le V_{CC}$	**−100**			µA
I_{IN0}	Input Current, CLK0	$V_{BB} \le V_{IN} \le V_{CC}$ − 0.5V	**−10**		**−0.1**	µA
V_{IL}	Input Low Voltage, CLK, PDN		0		**0.8**	V
V_{IH}	Input High Voltage, CLK, PDN		**2.2**		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB}+0.5	V
V_{II0}	Input Intermediate Voltage, CLK0		−0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC}−0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
IB_xI	Input Leakage Current, VF_xI	−3.2V ≤ V_{IN} ≤ +3.2V	**−100**		**100**	nA
RI_xI	Input Resistance, VF_xI	$V_{BB} \le VF_xI \le V_{CC}$	10			MΩ
VOS_xI	Input Offset Voltage, VF_xI	−2.5V ≤ V_{IN} ≤ +2.5V	**−20**		**20**	mV
V_{CM}	Common-Mode Range, VF_xI		**−2.5**		**2.5**	V
CMRR	Common-Mode Rejection Ratio	−2.5V ≤ V_{IN} ≤ 2.5V	**60**			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		**60**			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				100	pF
VO_xI	Output Voltage Swing, GS_x	$R_L \ge$ 10k	**±2.5**			V
A_{VOL}	Open Loop Voltage Gain, GS_x	$R_L \ge$ 10k	**5,000**			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

AC Electrical Characteristics

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. Limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with $VF_xI = 1.09$ Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO	$-2.5V < V_{OUT} < 2.5V$ $-3.2V < V_{OUT} < 3.2V$	3 10			kΩ kΩ
CL_x	Load Capacitance, VF_xO				100	pF
RO_x	Output Resistance, VF_xO			1	**3**	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, $VF_xI+ = 0$ Vrms	**30**			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	**35**			dB
GA_x	Absolute Gain	f = 1 kHz (TP3040A, TP3040A-1) f = 1 kHz (TP3040, TP3040-1)	**2.9** **2.875**	3.0 3.0	**3.1** **3.125**	dB dB
GR_x	Gain Relative to GA_x	Below 50 Hz 50 Hz 60 Hz 200 Hz (TP3040A, TP3040A-1) 200 Hz (TP3040, TP3040-1) 300 Hz to 3 kHz (TP3040A, TP3040A-1) 300 Hz to 3 kHz (TP3040, TP3040-1) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 **−1.5** **−1.5** **−0.125** **−0.15** **−0.35** **−0.70** 	 −41 −35 −15 	−35 **−35** **−30** **0** **0.05** **0.125** **0.15** **0.03** **−0.1** **−14** **−32**	dB dB dB dB dB dB dB dB dB dB dB
DA_x	Absolute Delay at 1 kHz				230	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				**−48**	dB
DP_x2	Distortion at Maximum Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, $R_L = 10k$			−45	dB
NC_x1	Total C Message Noise at VF_xO	TP3040, TP3040A TP3040-1, TP3040A-1		2	**5** **6**	dBrnc0 dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting (Note 3) $T_A = 0°C$ to $70°C$ TP3040, TP3040A TP3040-1, TP3040A-1		 3 	 **6** **7**	 dBrnc0 dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	$V_{CC} = 5.0V \pm 5\%$ $V_{BB} = -5.0V \pm 5\%$		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms $VF_xI+ = 0$ Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			**−70**	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0	**−0.1** **−0.05** **−0.1**		**0.1** **0.05** **0.1**	dB dB dB

AC Electrical Characteristics (Continued)

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. Limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \le V_{IN} \le 3.2V$	**−100**		**100**	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	**3**	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	**35**			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	**−200**		**200**	mV
GA_R	Absolute Gain	f = 1 kHz (TP3040A, TP3040A-1) f = 1 kHz (TP3040, TP3040-1)	**−0.1** **−0.125**	0 0	**0.1** **0.125**	dB dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz 300 Hz to 3.0 kHz (TP3040A, TP3040A-1) 300 Hz to 3.0 kHz (TP3040, TP3040-1) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 **−0.125** **−0.15** **−0.35** **−0.7**		**0.125** **0.125** **0.15** **0.03** **−0.1** **−14** **−32**	dB dB dB dB dB dB dB
DA_R	Absolute Delay at 1 kHz				100	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			**−48**	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, $R_L = 10k$			−45	dB
NC_R	Total C-Message Noise at VF_RO	TP3040, TP3040A TP3040-1, TP3040A-1		3	**5** **6**	dBrnc0 dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2 Vrms $VF_RI = 0$ Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			**−70**	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 (Note 5)	**−0.1** **−0.05** **−0.1**		**0.1** **0.05** **0.1**	dB dB dB

AC Electrical Characteristics (Continued)

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. Limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-3.2V \le V_{IN} \le 3.2V$	**0.1**		**3**	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO+, PWRO−	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO+, PWRO−				500	pF
GA_p+ GA_p−	Gain, PWRI to PWRO+ Gain, PWRI to PWRO−	R_L = 600Ω Connected Between PWRO+ and PWRO−, Input Level = 0 dBm0 (Note 4)		1 −1		V/V V/V
GR_pL	Gaintracking Relative to 0 dBm0 Output Level, Including Receive Filter	V = 2.05 Vrms, R_L = 600Ω (Notes 4, 5) V = 1.75 Vrms, R_L = 300Ω	**−0.1** −0.1		**0.1** 0.1	dB dB
S/D_p	Signal/Distortion	V = 2.05 Vrms, R_L = 600Ω (Notes 4, 5) V = 1.75 Vrms, R_L = 300Ω			**−45** −45	dB dB
VOSP	Output DC Offset, PWRO+, PWRO−	PWRI Connected to GNDA	**−50**		**50**	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	**45**			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. This specification listed assumes 0 dBm is delivered to 600Ω connected from PWRO+ to PWRO−.

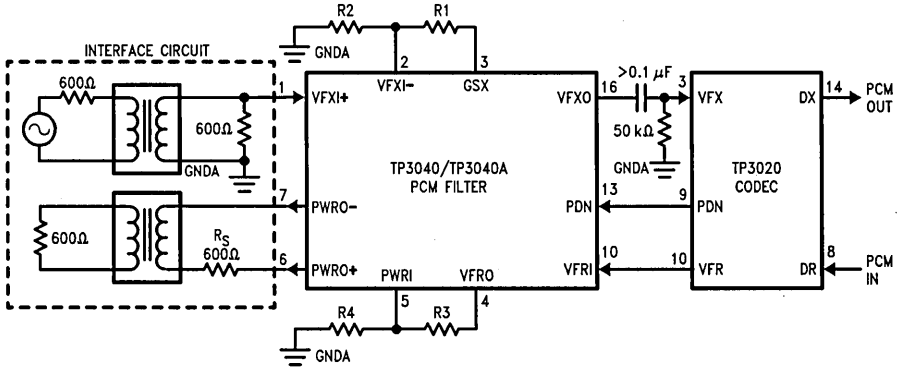
Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.

Note 3: The 0 dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.

Note 4: The 0 dBm0 level for the power amplifiers is load dependent. For R_L = 600Ω to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For R_L = 300Ω the 0 dBm0 level is 1.22 Vrms.

Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

Typical Application



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Note 1: Transmit voltage gain $= \frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3 dB gain), (R1 + R2 ≥ 10k)

Note 2: Receive gain $= \frac{R4}{R3 + R4}$

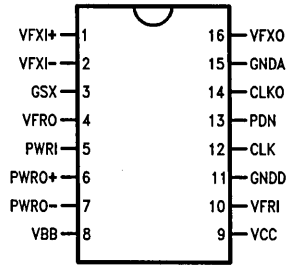
(R3 + R4 ≥ 10k)

Note: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a maximum signal level of 8.5 dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1 dBm across a 600Ω termination impedance.

FIGURE 2

Connection Diagram

Dual-In-Line Package



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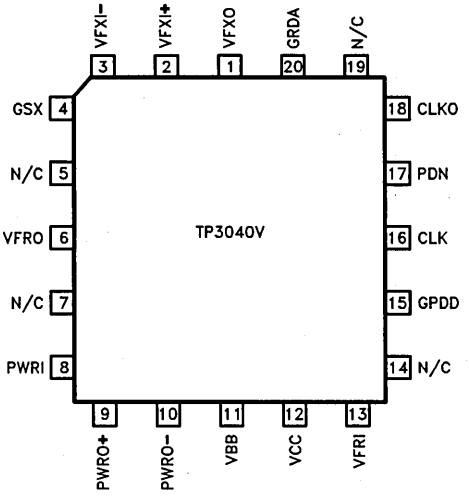
Top View

Order Number TP3040J or TP3040AJ or TP3040J-1 or TP3040AJ-1
See NS Package J16A

Plastic Lead Chip Carrier



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Order Number TP3040V or TP3040AV or TP3040V-1 or TP3040AV-1
See NS Package V20A

Description of Pin Functions

Symbol	Function
VF_XI+	The non-inverting input to the transmit filter stage.
VF_XI-	The inverting input to the transmit filter stage.
GS_X	The output used for gain adjustments of the transmit filter.
VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	The input to the receive filter differential power amplifier.
PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
PWRO−	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
V_{BB}	The negative power supply pin. Recommended input is −5V.
V_{CC}	The positive power supply pin. The recommended input is 5V.
VF_RI	The input pin for the receive filter stage.

Symbol	Function
GNDD	Digital ground input pin. All digital signals are referenced to this pin.
CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	The input pin used to power down the TP3040/TP3040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency:

CLK	Connect CLK0 to:
2048 kHz	V_{CC}
1544 kHz	GNDD
1536 kHz	V_{BB}

An internal pull-up is provided.

GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
VF_XO	The output of the transmit filter stage.

Functional Description

The TP3040/TP3040A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (*Figure 1*). A brief description of the circuit operation for each section is provided below.

TRANSMIT FILTER

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10 MΩ, a voltage gain of greater than 5,000, low power consumption (less than 3 mW), high power supply rejection, and is capable of driving a 10 kΩ load in parallel with up to 25 pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20 dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200 Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40 dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10 kΩ load in parallel with up to 25 pF.

RECEIVE FILTER

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

RECEIVE FILTER POWER AMPLIFIERS

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (*Figure 2*). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10 mW–20 mW depending on output signal amplitude.

POWER DOWN CONTROL

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1 mW. Connect PDN to GNDD for normal operation.

FREQUENCY DIVIDER AND SELECT LOGIC CIRCUIT

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1.544 MHz or 1.536 MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048 MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

Applications Information

GAIN ADJUST

Figure 2 shows the signal path interconnections between the TP3040/TP3040A and the TP3020 signal-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained from the TP3040/TP3040A filter when operated with system peak overload voltages of ±2.5V to ±3.2V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

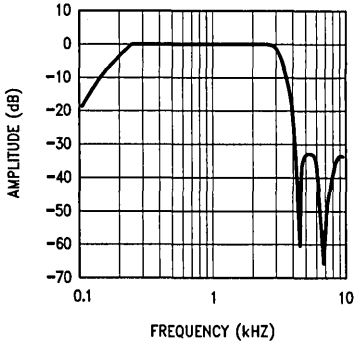
For example, the TP3040/TP3040A filter can be used with the TP3020/21 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

BOARD LAYOUT

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

Typical Performance Characteristics

Transmit Filter Stage



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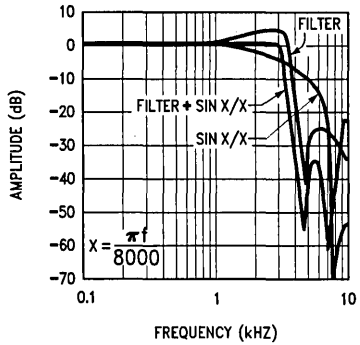
Receive Filter Stage



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Definitions and Timing Conventions

DEFINITIONS

V_{IH} — V_{IH} is the d.c. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum set-up and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.

V_{IL} — V_{IL} is the d.c. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device.

V_{OH} — V_{OH} is the minimum d.c. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.

V_{OL} — V_{OL} is the maximum d.c. output level to which and output placed in a logical zero state will converge when loaded at the maximum specified load current.

Threshold Region — The threshold region is the range of input voltages between V_{IL} and V_{IH}.

Valid Signal — A signal is Valid if it is in one of the valid logic states, (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.

Invalid Signal — A signal is Invalid if it is not in a valid logic state, i.e. when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purposes of this timing specification the following conventions apply:

Input Signals — All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ ns.

Period — The period of clock signal is designated as t_{Pxx} where $_{xx}$ represents the mnemonic of the clock signal being specified.

Rise Time — Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}.

Fall Time — Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}.

Pulse Width High — The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.

Pulse Width Low — The low pulse width is designated as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.

Set-up Time — Set-up times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose set-up time is being specified relative to a clock or strobe input represented by mnemonic xx. Set-up times are measured from the ww Valid to xx Invalid.

Hold Time — Hold times are designated as t_{Hxxww}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by the mnemonic xx. Hold times are measured from xx Valid to ww Invalid.

Delay Time — Delay times are designated as $t_{Dxxyy[H/L]}$, where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this datasheet.

Section 2

ISDN Components

Section 2 Contents

*Devices not covered in last publication

Introduction To National Semiconductor Basic Access I. C. Set

In developing the architecture of this ISDN chip set, National's major objective has been to create a flexible set of building blocks which provide elegant and cost-effective solutions for a wide range of applications. With just a few highly integrated devices, a broad spectrum of ISDN equipment can be designed, ranging from Central Office and PBX line cards to X.25 and ISDN Terminals and telephones, PC and Terminal Adapters, packet-mode statistical multiplexers, NT-1's and other ISDN equipment.

One of the keys to this flexibility is the concept that device functions in the chip set should be specifically aligned with the first 3 layers of the ISO 7 layer Protocol Reference Model. Thus, National's chip set has a distinct partitioning of functions into several transceivers which provide the bit-level transport for Layer 1, (the Physical Layer), while the functions of Layer 2, (the Data Link Layer), and Layer 3, (the Network Layer), are supported entirely by a single microprocessor. All devices in the chip set, together with other standard components such as COMBOs, can be interconnected via a common serial interface without the need for any "glue" components. The result is a very elegant architecture offering many advantages including the following:

- A high degree of modularity with minimal component count
- The same transceiver at both ends of a loop
- No interrupts for D-Channel flow control
- Powerful Packet buffer management

Other chip set architectures, which divide a layer into some functions in one device and the rest in other devices, are unable to offer all these advantages.

ISDN Chip Set Partitioning

<table>
<tr><th>ISO Layer</th><th>National</th><th colspan="2">Others</th></tr>
<tr><td>4–7</td><td>NS32322</td><td></td><td></td></tr>
<tr><td>3</td><td rowspan="2">HPC16400</td><td>Chip C</td><td rowspan="2">Chip B</td></tr>
<tr><td>2</td><td>Chip B</td></tr>
<tr><td>1</td><td>TP3401 DASL
or TP3410 EC or
TP3420 SID</td><td>Chip A</td><td>Chip A</td></tr>
</table>

NSC Solutions for Layer 1

National's solution for Layer 1 consists of 3 CMOS transceivers, which cover a wide variety of twisted-pair applications for ISDN Basic Access. Each transceiver is capable of transmitting and receiving 2 'B' channels plus 1 'D' channel, and has mode selections to enable it to operate at either end of the loop.

Transceiver Number 1

The TP3400 Digital Adapter for Subscriber Loops (DASL) is a low-cost burst-mode transceiver for 2 wire PBX and private network loops up to 6 kft in range. Scrambled Alternate Mark Inversion coding is used, together with adaptive equalization and timing-recovery, to ensure low bit error rates on a wide variety of cable types. All activation and loop timing control circuitry is also included.

Transceiver Number 2

The TP3410 Echo-canceller Family is a set of 2-wire transceivers designed to meet the rigorous requirements of the 'U' interface. Derived from a common basic architecture, these devices will be compatible with the line-code and framing structure specifications of various PTT administrations and with the U.S. standard.

Transceiver Number 3

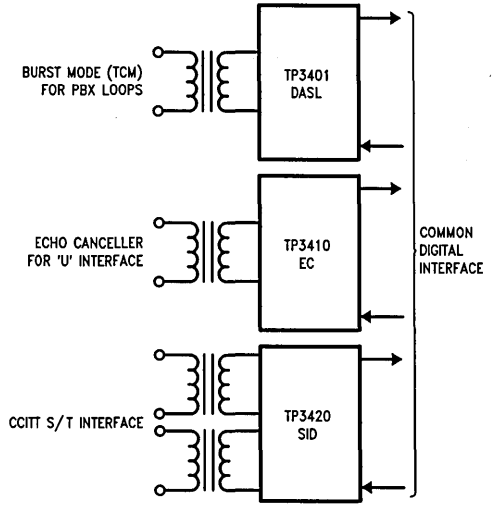
The TP3420 'S' Interface Device (SID), is a 4-wire transceiver which includes all the Layer 1 functions specified in CCITT Recommendation I.430. In addition, the TP3420 includes noise filtering and adaptive equalization, as well as a high resolution digital phase-locked loop, to provide transmission performance far in excess of that specified in I.430. All Activation and 'D' channel access sequences are handled automatically without the need to invoke any action from a microprocessor.

Digital Chip to Chip Interfaces

To retain the flexibility of interfacing components from this chip set with a variety of other products, two digital interfaces are provided on each device. One is for the synchronous transfer of 'B' and 'D' channel information in any of several popular multiplexed serial formats. This means that National's chip to chip interface is all encompassing of proprietary frame structures such as the IOM, IDL, ST-BUS and more.

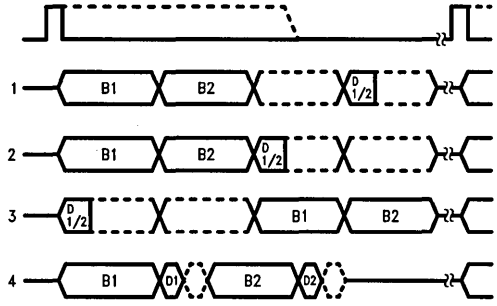
A second interface, for device mode control, e.g. power up/down, setting loopbacks etc., uses the popular MICROWIRE/PLUS™. MICROWIRE/PLUS is a synchronous serial data transfer between a microcontroller and one or more peripheral devices. National's HPC and COPS™ microcontroller families, together with a broad range of peripheral devices, support this interface, which is also easy to emulate with any microprocessor.

NSC ISDN Transceiver Chip Set



TL/X/0008-1

Popular Frame Structures Addressed by NSC ISDN Devices



TL/X/0008-2

NSC Solutions for Layers 2 and 3

National has developed an extremely powerful solution for implementing various protocols for both Layer 2 (Data Link Layer) and Layer 3 (Network Layer), including X.25 LAPB and LAPD (Q.921 and Q.931), together with the capability of several packet-mode Terminal Adaption schemes*. A single device incorporates all the processing for these functions: the HPC16400. One of National's growing family of 16-bit single chip CMOS microcontrollers, the HPC16400 is based on a high-speed (17 MHz) 16-bit CPU "core". To this core has been added 2 full HDLC formatters supported by DMA to external memory, and a UART.

This set of features makes the HPC16400 an ideal processor for running all the functions of an ISDN Terminal Adapter, TE or telephone, or the communications port of a high-end terminal. In a typical application, one of the HDLC channels may be dedicated to running the LAPD protocol in the 'D' channel, while the other provides packet-mode access to one of the 'B' channels. The UART would serve as an RS232 interface running at any of the standard synchronous or asynchronous rates up to 128 kbaud. A serial interface decoder allows either or both HDLC controllers to be directly interfaced to any of the 3 Layer 1 transceivers or to a variety of backplanes, line-card controllers and other devices using time-division multiplexed serial interfaces.

Because of the large ROM and RAM requirements for Layer 3 and the Control Field procedures of Layer 2 in LAPB and LAPD protocols, the HPC16400 has 256 bytes of RAM and no internal ROM for storage of user variables. Packet storage RAM and all user ROM is off-chip, this is by far the most cost-effective and flexible combination. A multiplexed bus to external memory provides direct addressing for up to 64 kbytes of memory, and on-chip I/O allows for expanded addressing for up to 544 kbytes of memory.

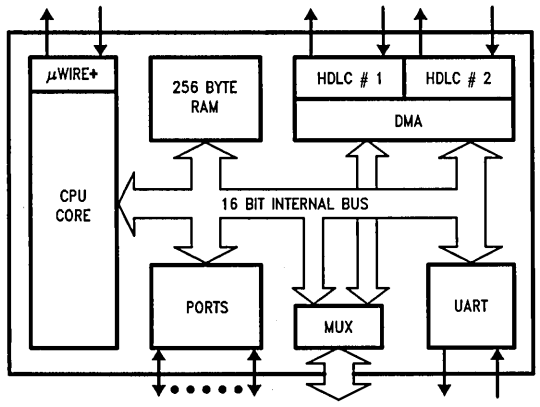
The HDLC controllers on the HPC16400 allow continuous HDLC data rates up to 4.1 Mb/s to be used. In addition to handling all Layer 2 framing, the HDLC circuitry includes automatic multiple address recognition to support, for example, multiple TEI's in LAPD. Furthermore, the DMA controller provides several register sets for packet RAM management with minimal CPU intervention, including "chaining" of successive packets. This integrated design achieves a high throughput of packet data without the need for costly FIFO's and external interrupts, thereby minimizing the impact of packet handling on CPU time.

In many applications a number of other peripheral functions must also be provided, such as sensing switches or scanning a small keyboard, interfacing to a display controller etc. A number of extra I/O ports and a MICROWIRE/PLUS serial data expansion interface are available on the HPC16400 to service these functions. In addition, 4 user configurable 16 bit timer-counters simplify the many time-outs required to manage such a system, including the default timers specified in the various protocol specifications.

Terminal adaption consistent with the CCITT V.110 method, which is based on a synchronous 80 bit frame, is readily implemented with another member of the HPC family, the HPC16040. Around the standard core CPU, the 16040 has on board I/O and 4 additional PWM timers, a UART, 4k of ROM and 256 bytes of RAM.

*For example, as per DMI Modes 2 and 3.

HPC16400 Simplified Block Diagram

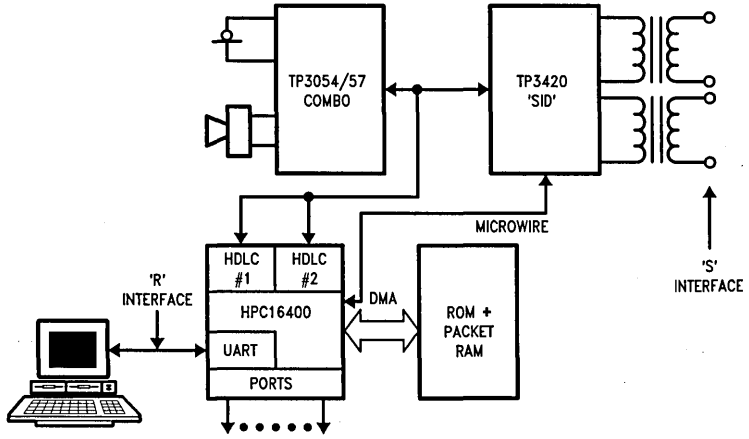


TL/X/0008-3

NSC Solutions: Systems Level

Building an ISDN TE or TA

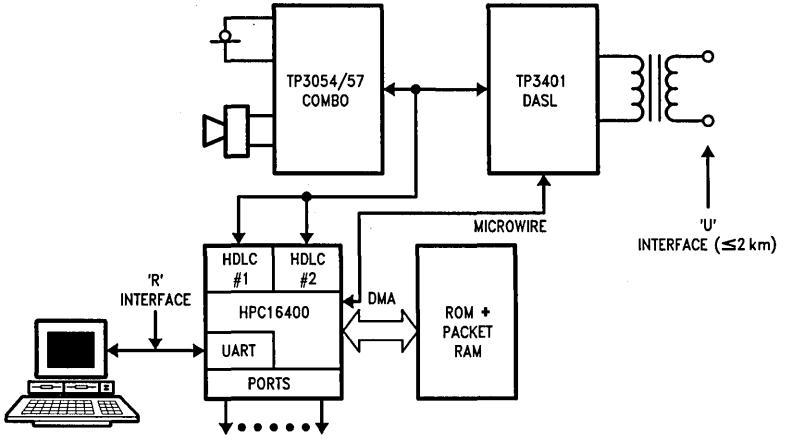
Shown below is a typical application of the chip set in a Basic Access TE, which offers one voice channel and an RS232 interface to support an external terminal. The TP3420 'S' Interface Device ensures that the system is compatible with any 'S' or 'T' standard jack socket and provides the multiplexing for the other devices operating in the 'B' and 'D' channels. All timing for the TE is derived by the TP3420 from the received line signal. In a typical application, LAPD signalling in the 'D' channel is provided via HDLC #1 on the HPC16400. HDLC #2 is working in conjunction with the UART to provide an X.25 or LAPD packet-mode in a 'B' channel at 64 kb/s. Terminal Adaption of both the data and the terminal handshaking signals is performed by the HPC16400 via the UART and HDLC controller #2, which can use either of the 'B' channels. DMI modes 2 and 3 (for a single channel) can be supported using this method, with the necessary data buffers set up in internal RAM. The other 'B' channel is occupied by the TP3054/7 PCM COMBO providing the digitized voice channel.



TL/X/0008–4

PBX 2 Wire Terminals

The following example shows how simple it is to convert an 'S' Interface terminal, which requires 2 twisted pairs, to a terminal using only a single pair by replacing the TP3420 SID with a TP3401 DASL. The clean partitioning of device functions makes this possible with no other changes to the design.

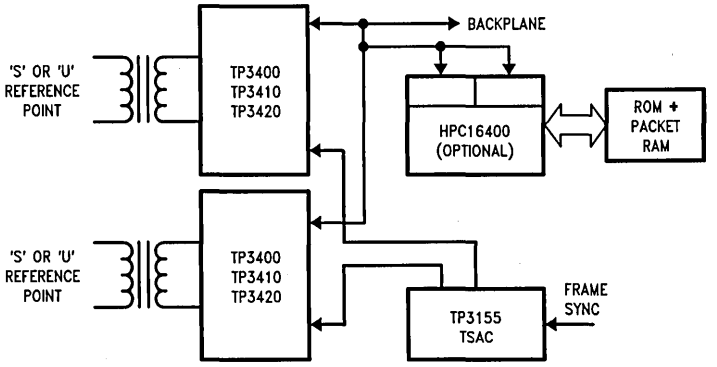


TL/X/0008–5

Basic Access Line Cards

For operation on a line card in a C.O., PABX or NT-2, each of the 3 transceiver devices can be set to operate as the timing master for the loop, being synchronized to the system clock and controlling all loop frame timing. If programmable time-slot assignment is required, the TP3155 TSAC provides 8 individually programmable frame sync pulse outputs locked to a common frame marker. 'B' channels can be interfaced to standard backplane interfaces, while 'D' channels can be either multiplexed on and off the card for processing or can undergo Layer 2 processing on the card itself.

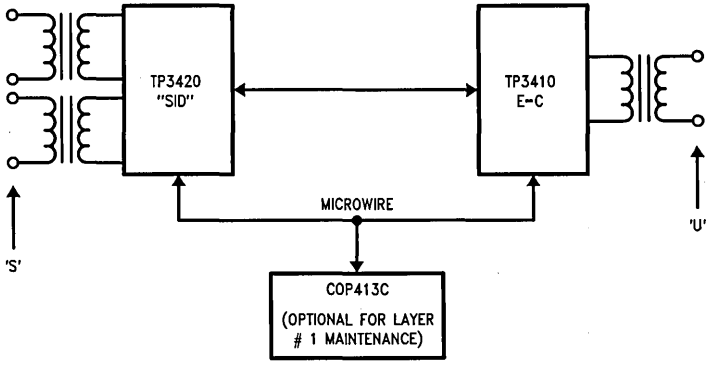
For the latter method, one HPC16400 handles Layer 2 framing for 2 basic access lines. In this manner, packets are first identified as data or signalling type by analysis of the SAPI field, with data packets being routed separately to a packet switch access node. If required, signalling packets can undergo protocol conversion in the HPC to an existing internal switch control protocol.



TL/X/0008–6

Building an NT-1

An NT-1 Network Termination is defined as a Layer 1 device only, which converts the 2-wire long-haul 'U' interface to the limited distance 4-wire 'S' interface. It has no capability for intercepting higher layers of the 'D' channel protocol. As such, it is built simply by connecting a TP3420 SID, configured in NT (or Master) mode, to a TP3410 Echo-canceller operating in Slave mode. Sharing a common 15.36 MHz crystal, these devices pass 'B' and 'D' channel information across the standard 4-wire interface. Layer 1 maintenance protocols across both the 'U' and the 'S/T' interfaces, which are as of yet not definitively specified by most adminstrations, may be handled by a low cost 4-Bit COPS™ Microcontroller via its Microwire Interface.



TL/X/0008–7

National Semiconductor Corporation

PRELIMINARY

microCMOS

TP3401 DASL Digital Adapter for Subscriber Loops

General Description

The TP3401 is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on National's advanced double poly microCMOS process, and requires only a single +5 Volt supply. Alternate Mark Inversion (AMI) line coding, in which binary '1's are alternately transmitted as a positive pulse then a negative pulse, is used to ensure low error rates in the presence of noise with lower emi radiation than other codes such as Bi-phase (Manchester).

Full-duplex transmission at 144 kb/s is achieved on a single twisted wire pair using a burst-mode technique (Time Compression Multiplexed). Thus the device operates as an ISDN 'U' Interface for short loop applications, typically in a PBX environment, providing transmission for 2 B channels and 1 D channel. On #26 cable, the range is at least 1.8 km (6k ft).

System timing is based on a Master/Slave configuration, with the line card end being the Master which controls loop timing and synchronisation. All timing sequences necessary for loop activation and de-activation are generated on-chip. A 2.048 MHz clock, which may be synchronized to the system clock, controls all transmission-related timing functions.

The system is designed to operate on any of the standard types of cable pairs commonly found in premise wiring installations, including mixed gauges from #26AWG to #19AWG. Within certain constraints the system can operate with good margins even when Bridge Taps are present.

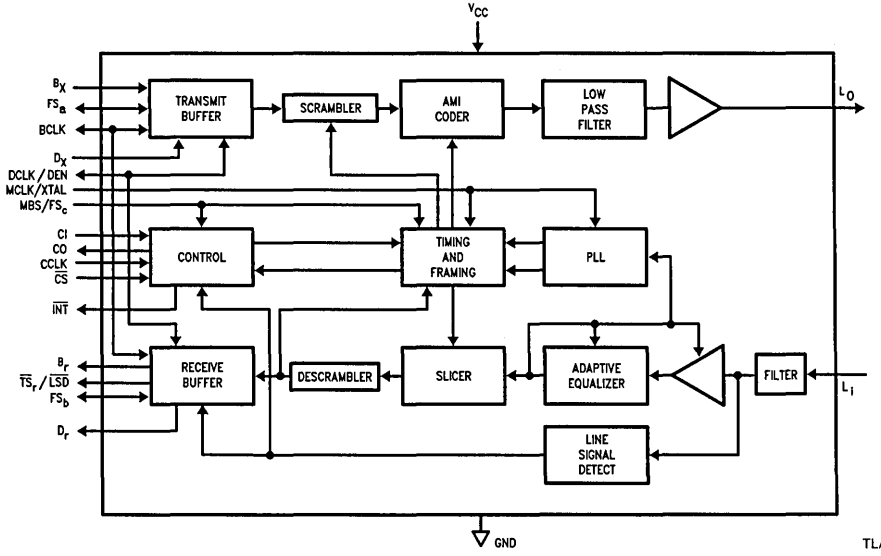
Three serial digital interfaces are provided on the TP3401; one for the transfer of B1 and B2 channel information, one for the transfer of D channel information and a third serial MICROWIRE™ compatible interface for control and status information.

Features

Complete ISDN PBX 2-Wire Data Transceiver including:

- 2 B plus D channel interface for PBX U Interface
- 144 kb/s full-duplex on 1 twisted pair using Burst Mode
- Loop range up to 6 kft (#26AWG)
- Alternate Mark Inversion coding with transmit filter and scrambler for low emi radiation
- Adaptive line equalizer
- On-chip timing recovery, no external components
- System interface with D channel Separate from B
- 2.048 MHz clock
- Driver for line transformer
- 2 loop-back test modes
- +5V only, 80 mW Active Power
- 5 mW idle mode

Block Diagram



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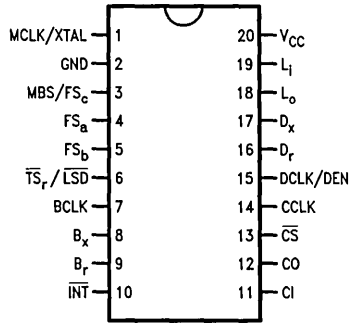
Connection Diagram

TP3401 DASL



TL/H/9264-2

Top View

Order Number TP3401
See NS Package Number J20A

Pin Descriptions

Name	Description
GND	Negative power supply pin, normally 0V. All analog and digital signals are referred to this pin.
V_{CC}	Positive power supply input, which must be $+5V \pm 5\%$.
MCLK/XTAL	The 2.048 MHz Master Clock input, which requires either a crystal* to be tied between this pin and GND, or a logic level clock input from a stable source. When using a crystal, no other external loading components are necessary.
MBS/FS_C	In Master Mode, this pin is the Master Burst Sync input, which may be clocked at 4 kHz to synchronize Transmit bursts from a number of devices at the Master end only. The 4 kHz should be nominally a square wave signal. In Slave mode, this pin is a short Frame Sync output, suitable for driving another DASL in Master Mode to provide a repeater (i.e. range-extender) capability.
BCLK	Bit Clock logic signal which determines the data shift rate for B channel data on the digital interface side of the device. In Master mode this pin is an input which may be any multiple of 8 kHz from 256 kHz to 4.1 MHz, but must be synchronous with MCLK. In Slave mode this pin is an output at 2.048 MHz.
FS_a	In Master mode only, this pin is the Transmit Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time for transmit B channel data into B_x. In Slave mode only, this pin is a digital output pulse which indicates the 8-bit periods of the B1 channel data transfer at both B_x and B_r.
FS_b	In Master mode only, this pin is the Receive Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time of the device for receive B channel data out from B_r. In Slave mode only, this pin is a digital output pulse which indicates the 8-bit periods of the B2 channel data transfer at both B_x and B_r.
B_x	Digital input for B1 and B2 channel data to be transmitted to the line; must be synchronous with BCLK.
B_r	Digital output for B1 and B2 channel data received from the line; must be synchronous with BCLK.
$\overline{TS_r}/\overline{LSD}$	In master mode only, this pin is an open-drain output which is normally high impedance but pulls low during both B channel active receive time slots. In Slave mode only, this pin is an output which is normally high impedance and pulls low when a valid line signal is received.
D_x	Digital input for D channel data to be transmitted to the line; must be synchronous with DCLK.
D_r	Digital output for D channel data received from the line; must be synchronous with DCLK.
DCLK/DEN	In Master mode this pin is an input for the 16 kHz serial shift clock for D channel data on D_x and D_r, which should be synchronous with BCLK. It may also be re-configured via the Control Register to act as an enable input for clocking the D channel interface synchronized to BCLK. In Slave mode this is a 16 kHz clock output for D channel data.

*Crystal specifications: 2.048 MHz parallel resonant, $R_S \leq 100\Omega$.

Pin Descriptions (Continued)

Name	Description
CI	MICROWIRE control channel serial data input.
CO	MICROWIRE control channel serial data output.
CCLK	Clock input for the MICROWIRE control channel.
$\overline{CS}$	Chip Select input which enables the MICROWIRE control channel data to be shifted in and out when pulled low. When high, this pin inhibits the MICROWIRE interface.
$\overline{INT}$	Interrupt output, a latched output signal which is normally high-impedance and goes low to indicate a change of status of the loop transmission system. This latch is cleared when the Status Register is read by the microprocessor.
L_o	Transmit AMI signal output to the line transformer. This pin is capable of driving a load impedance $\geq 60\Omega$.
L_i	Receive AMI signal input from the line transformer. This is a high impedance input which requires an external line termination impedance.

Functional Description

POWER-UP/POWER-DOWN CONTROL

Following the initial application of power, the TP3401 DASL enters the power-down (de-activated) state, in which all the internal circuits are inactive and in a low power state except for the line-signal detect circuit; the line output L_o is in a high impedance state and all digital outputs are inactive. All bits in the Control Register power-up initially set to '0', so that the device always initializes as the Master end. Thus, at the Slave end, a control word must be written through the MICROWIRE port to select Slave mode. While powered-down, the Line-Signal Detect circuits in both Master and Slave devices continually monitor the line, to enable loop transmission to be initiated from either end.

To power-up the device and initiate activation, bit C6 in the Control Register must be set high. Setting C6 low de-activates the loop and power-down the device, see Table I.

TABLE I. Power-Up/Power-Down Control

MBS/FS_c Pin I/P at Master	C6 State	Action
4 kHz or 1	0	Powered-down, Line-Signal Detect active
1	1	Powered-up, sending frames synchronized to FS_a at Master, or received burst at Slave
4 kHz	1	Powered-up, sending frames synchronized to MBS at Master, or received burst at Slave

LINE TRANSMIT SECTION

Alternate Mark Inversion (AMI) line coding is used on the TP3401 because of its spectral efficiency and null dc energy content. All transmitted bits, excluding the start bit in burst mode, are scrambled by a 9-bit scrambler to provide good spectral spreading with a strong timing content. The scrambler feedback polynomial is:

$$x^9 + x^5 + 1.$$

Pulse shaping is obtained by means of a transmit filter, in order to limit rf energy and crosstalk while minimizing intersymbol interference (isi). *Figure 3* shows the pulse shape at the L_o output, while a template for the typical power spectrum transmitted to the line with random data is shown in *Figure 4*.

The line-driver output, L_o, is designed to drive a transformer through a capacitor and termination resistor. A 1:1 transformer, terminated in 100Ω, results in a signal amplitude of typically 1.3V pk-pk on the line. Over-voltage protection must be included in the interface circuit.

LINE RECEIVE SECTION

The front-end of the receive section consists of a continuous anti-alias filter followed by a switched-capacitor low-pass filter designed to limit the noise bandwidth with minimum isi. To correct pulse attenuation and distortion caused by the transmission line an AGC circuit and first-order equalizer adapt to the received pulse shape, thus restoring a "flat" channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

From the equalized output a DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 2.048 MHz. At the Master end of the loop this reference is the network clock, which controls all transmit functions the DPLL clock being used only for received data sampling. At the Slave end, however, a 2.048 MHz crystal is required to generate a stable local oscillator which is used as a reference by the DPLL to run both the receive and transmit sides of the DASL device.

Following detection of the recovered symbols, the received data is de-scrambled by the same x^9+x^5+1 polynomial and presented to the digital system interface circuit.

When the device is de-activated, a Line-Signal Detect circuit remains powered-up to detect the presence of incoming bursts if the far-end starts to activate the loop. From a "cold" start, acquisition of bit timing and equalizer convergence with random scrambled data takes approximately 25 ms at each end of the loop. Full loop burst synchronization is achieved approximately 50 ms after the "activate" command at the originating end.

BURST MODE OPERATION

For full-duplex operation over a single twisted-pair, burst mode timing is used, with the line-card (exchange) end of the link acting as the timing Master.

Functional Description (Continued)

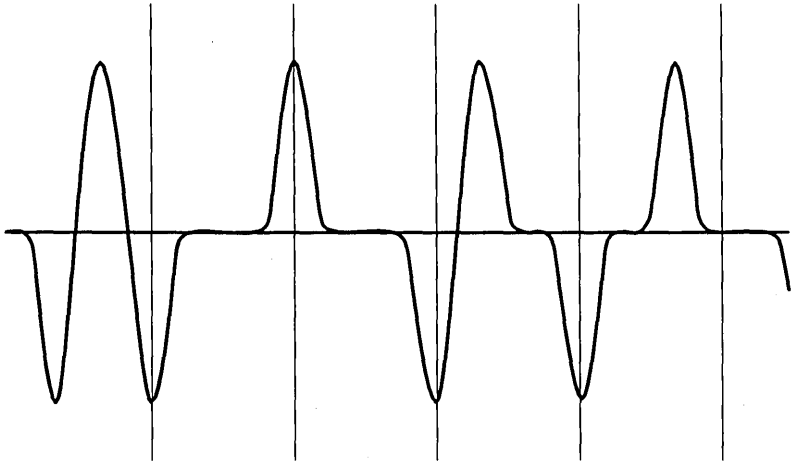


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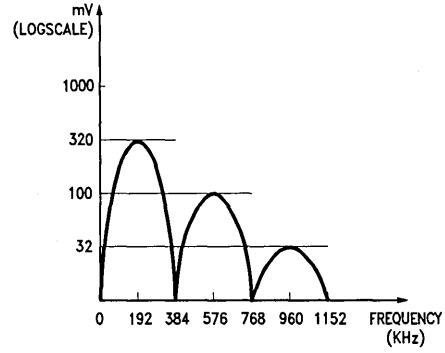
FIGURE 3. Typical AMI Waveform at L_o



TL/H/9264-4

FIGURE 4. Typical Line Transmit Spectrum

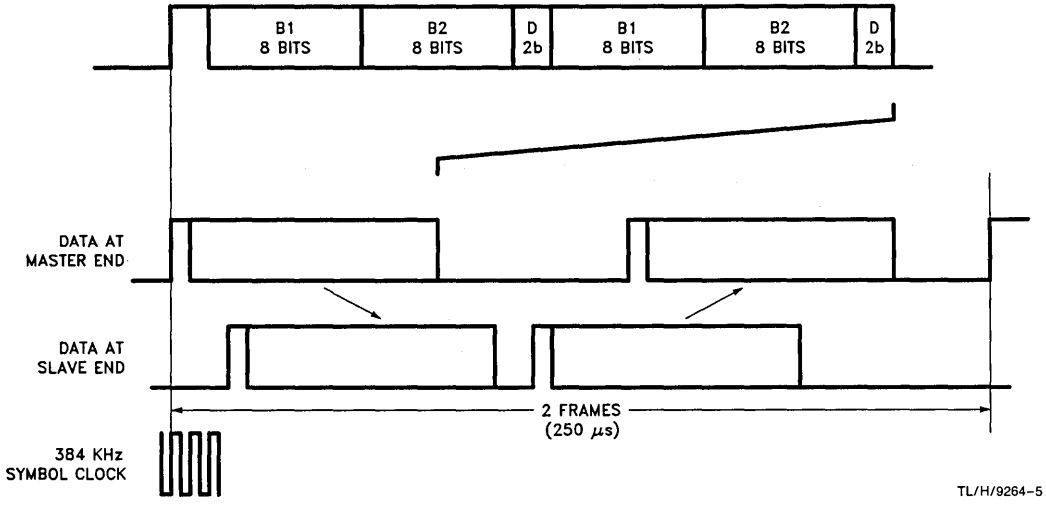


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FIGURE 5. Burst Mode Timing on the Line

Functional Description (Continued)

Each burst from the Master consists of the B1, B2 and D channel data from 2 consecutive frames combined in the format shown in *Figure 5*. During transmit bursts the Master's receiver input is inhibited to avoid disturbing the adaptive circuits. The Slave's receiver is enabled at this time and it synchronizes to the start bit of the burst, which is always an unscrambled '1' (of the opposite polarity to the last '1' sent in the previous burst). When the Slave detects that 36 bits following the start bit have been received, it disables the receiver input, waits 5 line symbol periods to match the other end settling guard time, and then begins to transmit its burst back towards the Master, which by this time has enabled its receiver input. The burst repetition rate is thus 4 kHz, which can either free-run or be locked to a synchronizing signal at the Master end by means of the MBS input, (See *Figure 10*). In the latter case, with all Master-end transmitters in a system synchronized together, near-end crosstalk between pairs in the same cable binder may be eliminated, with a consequent increase in signal-to-noise ratio (SNR).

ACTIVATION/DE-ACTIVATION

Activation (i.e. power-up and loop synchronization) may be initiated from either end of the loop. If the Master is activating the loop, it sends normal bursts of scrambled '1's, which are detected by the Slave's line-signal detect circuit, causing it to power-up. The Slave then replies with bursts of scrambled '1's synchronized to received bursts, and the flywheel circuit at each end searches for 4 consecutive correctly formatted receive bursts to acquire full loop synchronization. Each receiver indicates when it is correctly in sync with received bursts by setting the C1 bit in the Status Register high and pulling $\overline{INT}$ low.

To activate the loop from the Slave end, bit C6 in the Control Register must be set high, which will power-up the device and begin transmission of alternate bursts i.e., the burst repetition rate is 2 kHz, not 4 kHz. At this point the Slave is running from its local oscillator and is not receiving any sync information from the Master. When the Master's line-signal detect circuit recognizes this "wake-up" signal, the Master powers up and begins to transmit bursts, synchronized, as normal, to the MBS or FS_a input with a 4 kHz repetition rate. This enables the Slave's receiver to correctly identify burst timing from the Master and to re-synchronize its own burst transmissions to those it receives. The flywheel circuits then acquire full loop sync as described earlier.

Loop synchronization is considered to be lost if the flywheel finds 4 consecutive receive burst "windows" (i.e. where a receive burst should have arrived based on timing from previous bursts) do not contain valid bursts. At this point bit C1 in the Status Register is set low, the $\overline{INT}$ output is set low and the receiver searches to re-acquire loop sync.

DIGITAL SYSTEM INTERFACE

The digital system interface on the TP3401 separates B and D channel information onto different pins to provide maximum flexibility. On the B channel interface, phase skew between transmit and receive directions may be accommodated at the Master end since separate frame sync inputs, Fs_a and Fs_b, are provided. Each of these synchronizes a counter which gates the transfer of B1 and B2 channels in consecutive time-slots across the digital interface; since the counters are edge-synchronized the duration of the F_s input signals may vary from a single-bit pulse to a square-wave. The serial shift rate is determined by the BCLK input, and may be any frequency from 128 kHz to 2.048 MHz, as shown in *Figure 6*.

At the Slave end, both Fs_a and Fs_b are outputs. Fs_a goes high for 8 cycles of BCLK coincident with the 8 bits of the B1 channel in both Transmit and Receive directions. Fs_b goes high for the next 8 cycles of BCLK, which are coincident with the 8 bits of the B2 channel in both Transmit and Receive directions. BCLK is also an output at 2.048 MHz, the serial data shift rate, as shown in *Figure 7*. Data may be exchanged between the B1 and B2 channels as it passes through the device, by selling Control bit C0 = 1. An additional Frame Sync output, FS_c, is provided to enable a repeater to be built by connecting a DAS Lin Slave Mode to a DASL in Master Mode. The FS_c output from the Slave directly drives the FS_a and FS_b inputs on the Master.

D channel information, being packet-mode, requires no synchronizing input. This interface consists of the transmit data input, D_x, receive data output, D_r, and 16 kHz serial shift clock DCLK, which is an input at the Master end and an output at the Slave end. Data shifts in to D_x on falling edges of DCLK and out from D_r on rising edges, as shown in *Figure 11*. DCLK should be Synchronous with BCLK.

An alternative function of the DCLK/DEN pin allows D_x and D_r to be clocked at the same rate as BCLK at the Master end only. By setting bit C1 in the Control Register to a 1, DCLK/DEN becomes an input for an enabling pulse to gate 2 cycles of BCLK for shifting the 2 D bits per frame. Thus, at the Master end, the D channel bits can be interfaced to a TDM bus and assigned to a time-slot (the same time-slot for both transmit and receive), as shown in *Figure 12*.

CONTROL INTERFACE

A serial interface, which can be clocked independently from the B and D channel system interfaces, is provided for microprocessor control of various functions on the DASL device. All data transfers consist of a single byte shifted into the Control Register via CI simultaneous with a single byte shifted out from the Status Register via CO, see *Figure 13*. Data shifts in to CI on rising edges of CCLK and out from CO on falling edges when $\overline{CS}$ is pulled low for 8 cycles of CCLK. An Interrupt output, $\overline{INT}$ goes low to alert the microprocessor whenever a change in one of the status bits, C1 and/or C0 has occurred. This latched output is cleared high following the first CCLK pulse when $\overline{CS}$ is low. No interrupt is generated when status bit C2 goes high, however. This bit is set whenever 1 or more violations of the AMI coding rule is received, and cleared everytime the $\overline{CS}$ is pulsed. Statistics on the line bit error rate can be accumulated by regularly polling this bit.

Functional Description (Continued)

During the reading of the Status Register, the contents of the Control Register are protected, and data on the CI input is ignored.

Figure 13 shows the timing for this interface, and Table II lists the control functions and status indicators.

TABLE II. Control and Status Register Functions

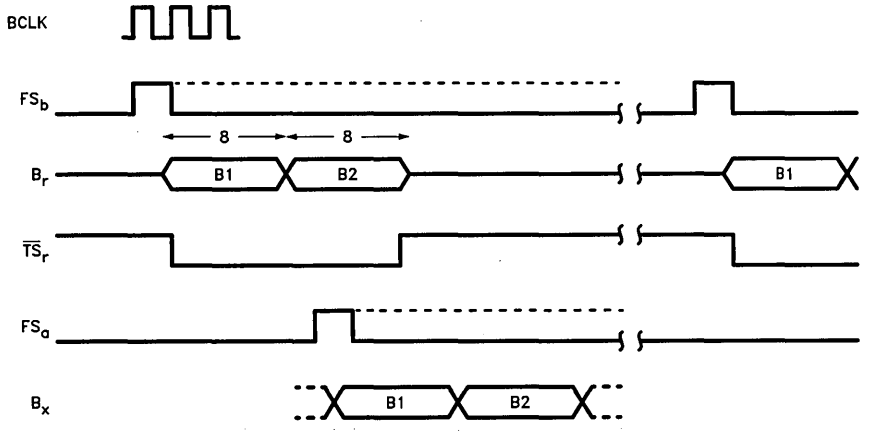
Bit	State	Control Register Function	Status Register Function
C7	0	Master Mode	Read Back C7 from Control Register
	1	Slave Mode	Read Back C7 from Control Register
C6	0	De-Activate and Power Down	Read Back C6 from Control Register
	1	Activate	Read Back C6 from Control Register
C5	0	Normal Through Connection	Read Back C5 from Control Register
	1	Loopback to Digital Interface	Read Back C5 from Control Register
C4	0	Normal Through Connection	Read Back C4 from Control Register
	1	Loopback B1 + B2 + D to Line (Note 1)	Read Back C4 from Control Register
C3	0	Normal Through Connection	Read Back C3 from Control Register
	1	Loopback B1 Only to Line (Note 1)	Read Back C3 from Control Register
C2	0	Normal Through Connection	No Error
	1	Loopback B2 Only to Line (Note 1)	Bipolar Violation Since Last READ (Note 2)
C1	0	DCLK/DEN pin = 16 kHz Clock	Out-Of-Sync
	1	DCLK/DEN pin = D Channel Enable (Note 3)	Loop In-Sync and Activation Complete
C0	0	B1/B2 Channels Direct	No Line Signal at Receiver Input
	1	B1/B2 Channels Exchanged	Line Signal Present at Receiver Input

Note 1: Receive data active.

Note 2: After the device is in sync.

Note 3: In Master mode only.

Timing Diagrams



TL/H/9264–6

FIGURE 6. B Channel Interface Timing: Master Mode

Timing Diagrams (Continued)

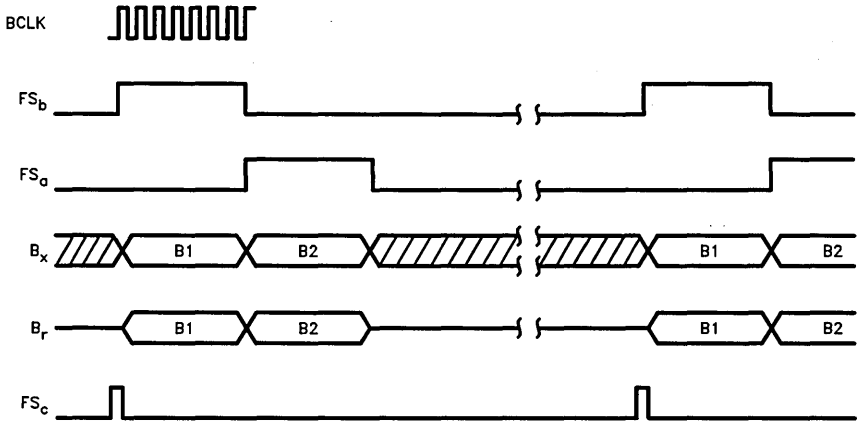


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FIGURE 7. B Channel Interface Timing: Slave Mode

Typical Applications

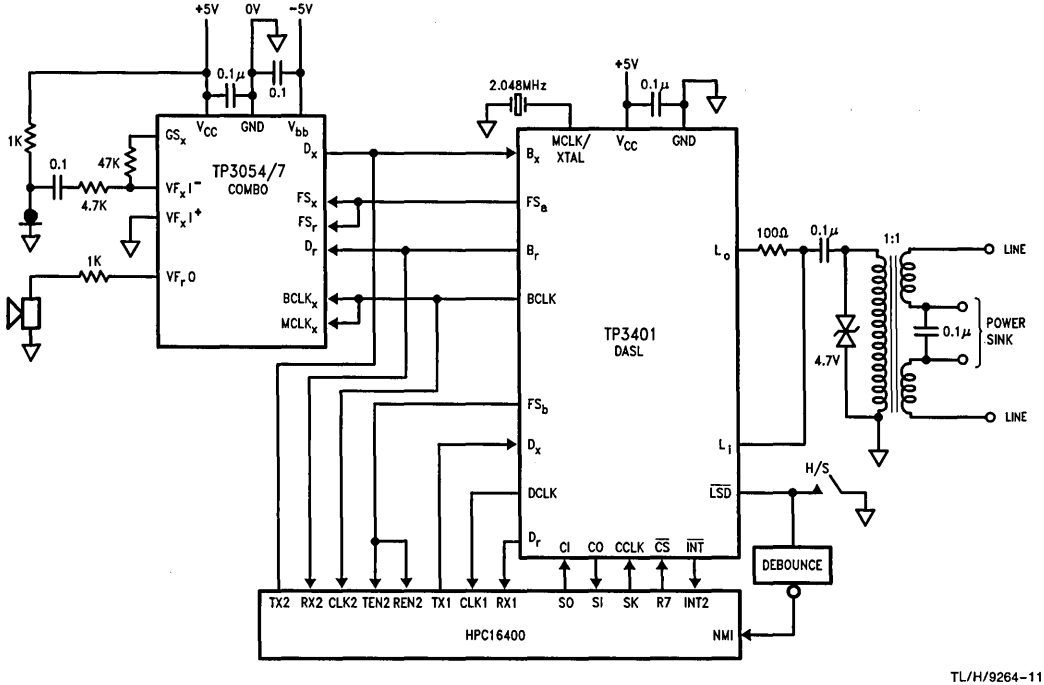

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FIGURE 8. Typical Application for Slave End

Typical Applications (Continued)

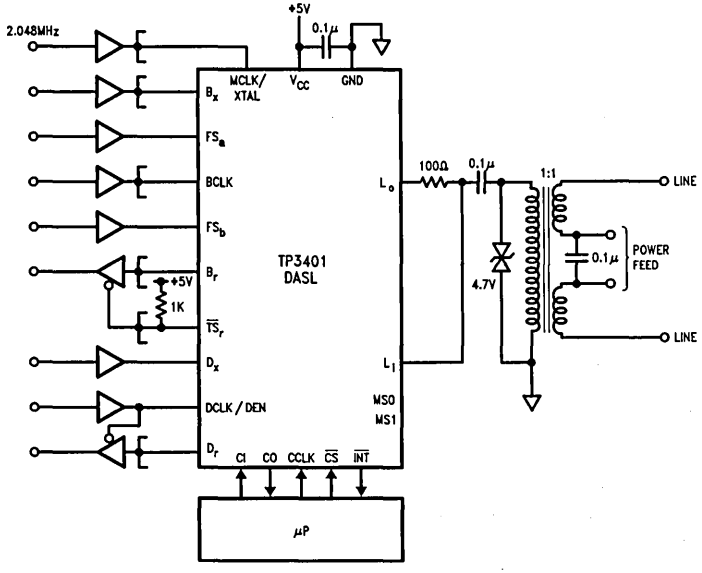

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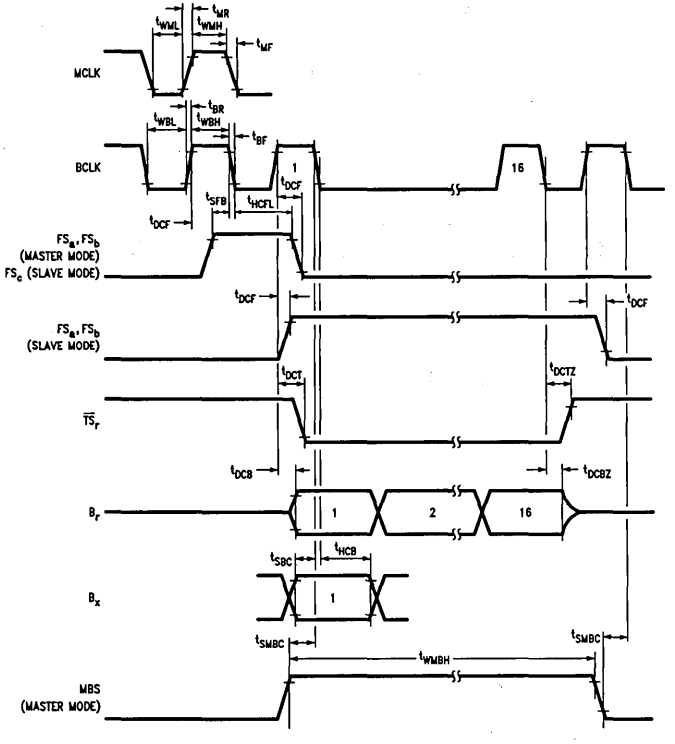
FIGURE 9. Typical Application for Master End

Timing Diagrams (Continued)



TL/H/9264-7

FIGURE 10. Timing Details

Timing Diagrams (Continued)

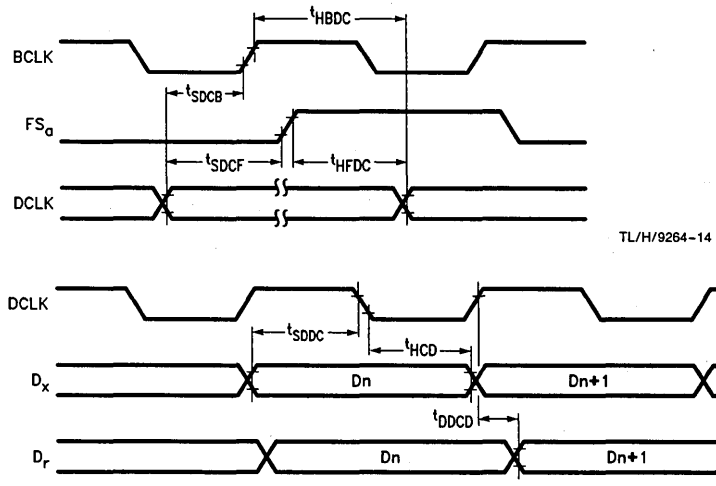


FIGURE 11. D Channel Interface Timing (Master and Slave Modes, C1 = 0)

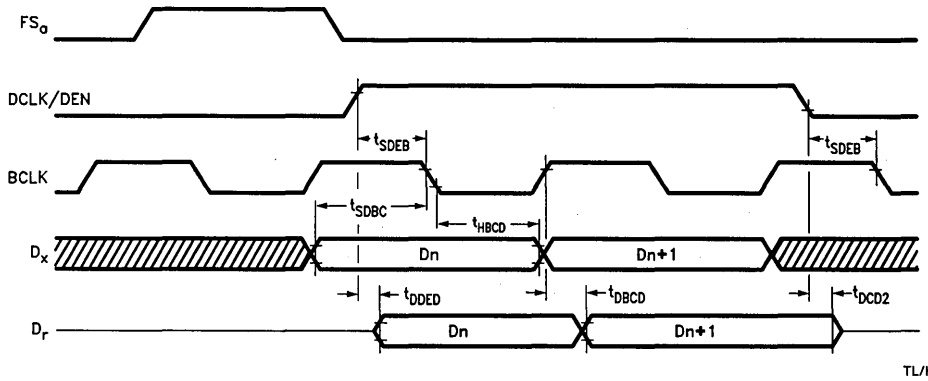


FIGURE 12. D Channel Interface Timing (Master Mode only, C1 = 1)

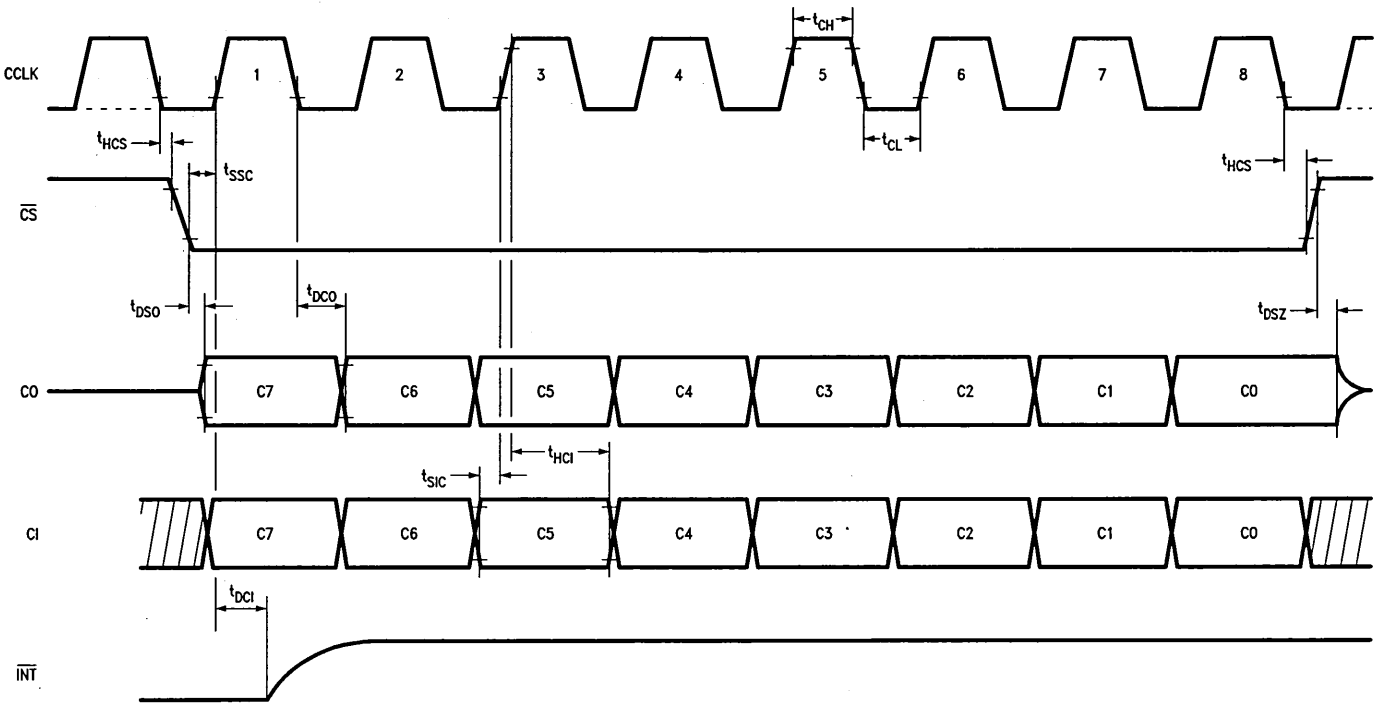


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FIGURE 13. Control Interface Timing

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at L_i, L_o	$V_{CC}+1V$ to $V_{SS}-1V$
Voltage at any Digital Input	$V_{CC}+1V$ to $V_{SS}-1V$
Storage Temperature Range	−65°C to +150°C
Current at L_o	±100 mA
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5.0V. T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2.0			V
V_{OL}	Output Low Voltage	B_r = 3.2 mA All Other Digital Outputs, I_L = 1 mA			0.4	V
V_{OH}	Output High Voltage	B_r = −3.2 mA All Other Digital Outputs, I_L = −1 mA	2.4			V
I_I	Input Current	Any Digital Input, GND < V_{IN} < V_{CC}	−10			μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE®)	B_r, GND < V_{OUT} < V_{CC}	−10		10	μA
LINE INTERFACES						
I_{Li}	Input Leakage	0V < L_i < 5.0V	−1.0		1.0	μA
R_{Li}	Input Resistance	0V < L_i < 5.0V	200			kΩ
RL_{Lo}	Load Resistance	L_o to GND	60			Ω
CL_{Lo}	Load Capacitance	100Ω in Series with 100Ω & 1 μF in Parallel from L_o to GND. CL_{Lo} from L_o to GND.			100	pF
RO	Output Resistance at L_o				3.0	Ω
V_{DC}	Mean d.c. Voltage at L_o			1.85		V
POWER DISSIPATION						
$I_{CC}0$	(De-activated)			1		mA
$I_{CC}1$	Power Up Current	RL_{LO} = 200Ω		16.0		mA
TRANSMISSION PERFORMANCE						
	Transmit Pulse Amplitude at L_o	R_L = 100Ω in Series with 0.1 μF to GND	±1.1	±1.3	±1.5	Vpk
	Input Pulse Amplitude at L_i		±60			mVpk
	Input Clock Jitter	2.048 MHz Input, 18 kHz < f < 200 kHz			200	ns pk-pk
	Timing Recovery Jitter	BCLK at Slave Relative to MCLK at Master SNR ≥ 20 dB		50	100	ns pk-pk
	Wake-up Time	Complete Loop from Cold Start		50	60	ms

Timing Characteristics

Unless otherwise noted: V_{CC} = +5V ±5%, T_A = 0°C to 70°C. Typical characteristics are specified at V_{CC} = 5V, T_A = 25°C. All signals are referenced to GND.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{MCK}	Master Clock Frequency			2.048		MHz
	Master Clock Tolerance		−50		+50	ppm
t_{WMH}, t_{WML}	Clock Pulse Width Hi & Low for MCLK	V_{IH} = 2.0V V_{IL} = 0.7V	160			ns
DIGITAL INTERFACE ***(Figure 10)***						
F_{BCK}	Bit Clock Frequency	Master Mode Only			2.1	MHz
t_{WBH}, t_{WBL}	Clock Pulse Width Hi & Low for BCLK	V_{IH} = 2.0V V_{IL} = 0.7V	100			ns
t_{MR}, t_{MF}	Rise and Fall Time of MCLK				15	ns
t_{BR}, t_{BF}	Rise and Fall Time of BCLK				15	ns
t_{SFB}	Set-Up Time, FS_a FS_b to BCLK Low	Master Mode Only	20			ns
t_{HCFL}	Hold Time, BCLK Low to FS_a and FS_b Low	Master Mode Only	100			ns
t_{DCF}	Delay Time, BCLK High to FS_a, FS_b Transition	Slave Mode Only			60	ns
t_{SBC}	Set Up Time, B_X Valid to BCLK Low		30			ns
t_{HCB}	Hold Time, BCLK Low to B_X Invalid		50			ns
t_{DCB}	Delay Time, BCLK High to B_r Valid	Load = 2 LSTTL Inputs Plus 100 pF			160	ns
t_{DCBZ}	Delay Time, BCLK Low to B_r High-Impedance		60		220	ns
t_{DCT}	Delay Time, BCLK High to $\overline{TS}_r$ Low	Load = 2 LSTTL Inputs Plus 100 pF			140	ns
t_{DCTZ}	Delay Time, BCLK Low to $\overline{TS}_r$ High-Impedance		60		185	ns
t_{SMBC}	Set-Up Time, MSB to BCLK Low (Note 1)	Master Mode Only	60			ns
t_{WMBH}	Width of MSB High	Master Mode Only		125		μs

Note 1: MSB transitions may occur anywhere in the Frame, and require no specific relationship to FS_a or FS_b.

Timing Characteristics (Continued)

Unless otherwise noted: V_{CC} = +5V ±5%, T_A = 0°C to 70°C. Typical characteristics are specified at V_{CC} = 5V, T_A = 25°C. All signals are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Units
D CHANNEL INTERFACE ***(Figure 11 & 12)***					
t_{SDDC}	Set Up Time, D_X Valid to DCLK Low		100		ns
t_{HCD}	Hold Time, DCLK Low to D_X Invalid		100		ns
t_{DDCD}	Delay Time, DCLK High to D_r Data Valid	Load = 100 pF +2 LSTTL Inputs		190	ns
t_{SDCB}	Set-Up Time, DCLK Transitions to BCLK High	Master Mode Only	50		ns
t_{HBDC}	Hold Time, BCLK High to DCLK Transitions	Master Mode Only	50		ns
t_{SDCF}	Set-Up Time, DCLK Transitions to FS_a HIgh	Master Mode Only	100		ns
t_{HFDC}	Hold Time, FS_a HIgh to DCLK Transition	Master Mode Only. Load = 50 pF	50		ns
t_{DDED}	Delay Time, DEN High to D_r Valid			140	ns
t_{SDEB}	Set-Up Time, DEN to BCLK Low		100		ns
t_{SDBC}	Set-Up Time, D_x to BCLK Low		30		ns
t_{HBCD}	Holt Time, BCLK Low to D_x Invalid		50		ns
t_{DBCD}	Delay Time, BCLK High to D_r Valid	Load = 100 pF +2 LSSTL Inputs		190	ns
t_{DCDZ}	Delay Time, DEN Low to D_r High Impedance			140	ns
CONTROL INTERFACE ***(Figure 13)***					
t_{CH}	CCLK High Duration		250		ns
t_{CL}	CCLK Low Duration		250		ns
t_{SIC}	Setup Time, CI Valid to CCLK High		100		ns
t_{HCI}	Hold Time, CCLK High to CI Invalid		0		ns
t_{SSC}	Setup Time from $\overline{CS}$ Low to CCLK High		200		ns
t_{HCS}	Hold Time from CCLK Low to $\overline{CS}$		10		ns
t_{DCO}	Delay Time from CCLK Low to C0 Data Valid	Load = 100 pF +2 LSTTL Inputs		150	ns
t_{DSO}	Delay Time from $\overline{CS}$ Low to CO Valid	1st Bit Only		100	ns
t_{DSZ}	Delay Time from $\overline{CS}$ High to CO Tri-State			100	ns
t_{DCI}	Delay Time from CCLK1 High to $\overline{INT}$ Tri-State			120	ns

Definitions and Timing Conventions

DEFINITIONS

V_{IH}	V_{IH} is the d.c. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.
V_{IL}	V_{IL} is the d.c. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device.
V_{OH}	V_{OH} is the minimum d.c. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum d.c. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between V_{IL} and V_{IH}.
Valid Signal	A signal is Valid if it is in one of the valid logic states, (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid Signal	A signal is Invalid if it is not in a valid logic state, i.e. when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purpose of this timing specification the following conventions apply:

Input Signals	All input signals may be characterized as: $V_L = 0.4V$, $V_{IH} = 2.4V$, $t_R < 10$ ns, $t_F < 10$ ns.
Period	The period of clock signal is designated at t_{Pxx} where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated at t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}.
Pulse Width High	The high width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse width is designed as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as t_{Hxxww}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by mnemonic xx. Hold times are measured from xx Valid to ww invalid.
Delay Time	Delay times are designated as t_{Dxxyy} [|H|L], where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specifiy the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specification section of this data sheet.

National Semiconductor Corporation

ADVANCED INFORMATION

TP3410 "U" Interface Transceiver

General Description

The TP3410 is a microCMOS monolithic digital transceiver which provides voice or data communications capability over a twisted pair of wires in the Public Network. The device functions at either end of the subscriber loop, handling voice and data transmissions between the Network Termination (NT) to the Central Office (CO) line card.

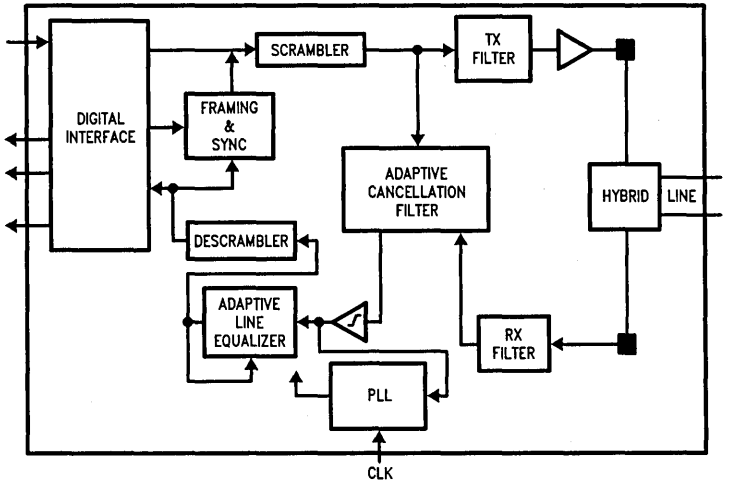
The TP3410 has facilities to transmit and receive using the standard ISDN 2B+D (2 64 kb/s and 1 16 kb/s channels) 144 kb/s full duplex channels plus extra channels (for loop maintenance and performance monitoring) for a total of 160 kb/s. These channels will operate over very long Central office subscriber loops of mixed gauges from #26 to #19 AWG (0.4–0.8 mm), which may include bridge taps.

At the time of this writing, the United States T1D1 committee for the Standardization of the U interface has not yet finalized the performance specification.

Preliminary Features

- 160 kb/s full duplex transmission for 2B+D
- Handles all layer 1 functions
- 2B1Q line coding
- Range at least 18 kft
- #26–#19 AWG (0.4–0.9 mm) mixed gauge wire compatibility
- 70 dB of Echo Cancellation
- Bridge Tap Equalization
- microCMOS, +5V only

Block Diagram



TL/H/9151–1

National Semiconductor Corporation

PRELIMINARY

microCMOS

TP3420 ISDN Transceiver "S" Interface Device

General Description

The TP3420 (S Interface Device) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on National's advanced double metal microCMOS process, and requires only a single +5V supply. All functions specified in CCITT recommendation I.430 for ISDN basic access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in a TE (Terminal Equipment), in an NT-1 or NT-2 (Network Termination) or as a PABX line-card device.

As specified in I.430, full-duplex transmission at 192 kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. Various channels are combined to form the 192 kb/s aggregate rate, including 2 'B' channels, each of 64 kb/s, and 1 'D' channel at 16 kb/s. In addition, the TP3420 provides the 800 b/s multiframe channels for Layer 1 maintenance.

All I.430 wiring configurations are supported by the TP3420 SID, including the "passive bus" for up to 8 TE's distributed within 200 meters of low capacitance cable, and point-to-point and point-to-star connections up to at least 1500 meters. Adaptive receive signal processing enables the device to operate with low bit error rates on any of the standard types of cable pairs commonly found in premise wiring installations.

Features

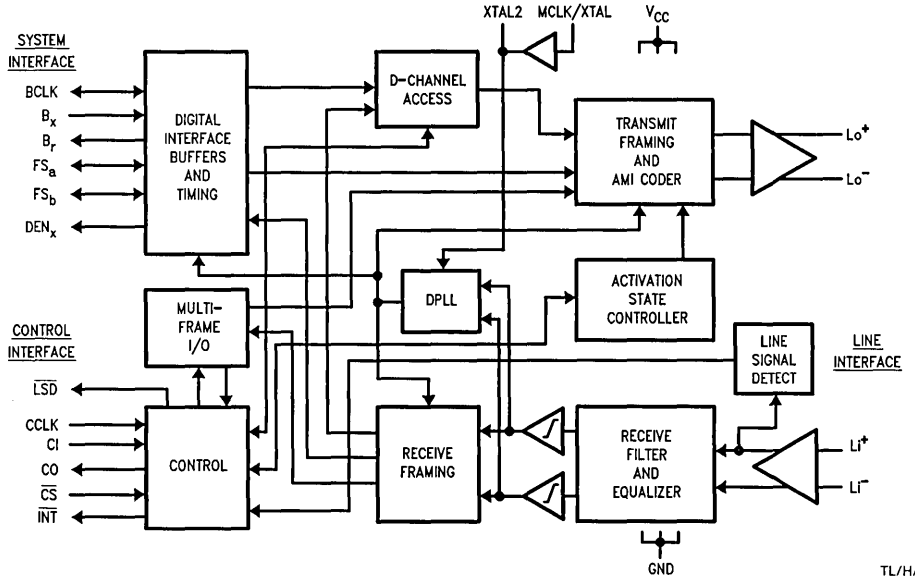
- Single Chip 4 Wire 192 kb/s Transceiver
- Provides all CCITT I.430 Layer 1 Functions
- Exceeds I.430 range: 1.5 km Point-to-Point
- Adaptive and Fixed Timing Options for NT-1
- Clock Resynchronizer and Data Buffers for NT-2
- Multiframe Channel for Layer 1 Maintenance
- Selectable System Interface Formats
- Microwire™ compatible serial control interface
- microCMOS, +5V only
- 20 Pin Package

Applications

- Same Device for NT, TE and PBX Line Card
- Point-to-Point Range Extended to 1.5 km
- Point-to-Multipoint for all I.430 Configurations
- Easy Interface to:

LAPD Processor	HPC16400
Terminal Adapter	HPC16400
Codec/Filter COMBO™	TP3054/7
"U" Interface Device	TP3410
Line Card Backplanes	

Block Diagram



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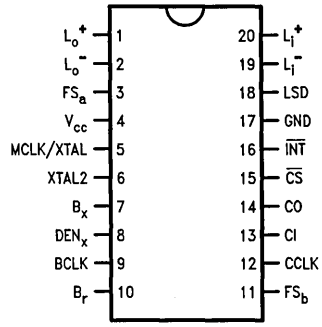
Connection Diagrams

TP3420N SID



TL/H/9143–2

Top View

Order Number TP3420N
See NS Package Number N20A

Pin Descriptions

Name	Description
GND	Negative power supply pin, normally 0V (ground). All analog and digital signals are referred to this pin.
V_{CC}	Positive power supply input, which must be +5V ±5%.
MCLK/XTAL	The 15.36 MHz Master Clock input, which requires either a crystal* to be tied between this pin and XTAL2, or a logic level clock input from a stable source. When using a crystal, no other external loading components are necessary.
XTAL2	The output of the crystal oscillator, which should be connected to one end of the crystal, if used.
BCLK	The Bit Clock pin, which determines the data shift rate for 'B' and 'D' channel data on the digital interface side of the device. When NT mode or TE mode Digital System Interface (DSI) Slave is selected, BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 4.096 MHz. It need not be synchronous with MCLK. When TE mode DSI Master is selected, this pin is an output at frequency selected by the Digital Interface Format. This clock is phase-locked to the received line signal. In TE mode DSI Master this pin is an output clock with the frequency depending on the interface format selected. It is synchronous with the data on B_X and B_r.
FS_a	In NT modes and TE mode DSI Slave, this pin is the Transmit Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time for transmit 'B' and 'D' channel data into B_X. In TE mode DSI Master only, this pin is a digital output pulse which indicates the start of the 'B' channel data transfer at both B_X and B_r.
FS_b	In NT modes and TE mode DSI Slave, this pin is the Receive Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time of the device for receive 'B' and 'D' channel data out from B_r. In TE mode DSI Master only this pin is an 8 bit wide pulse which indicates the active slot for the B2 channel on the digital interface.
B_X	Digital input for 'B' and 'D' channel data to be transmitted to the line; must be synchronous with BCLK.
B_r	Digital output for 'B' and 'D' channel data received from the line; must be synchronous with BCLK.
DEN_X	In TE mode DSI Master, this pin is an output which is normally low and pulses high to indicate the active bit-times for 'D' channel Transmit data at the B_X input. It is intended to be gated with BCLK to control the shifting of data from a Layer 2 device to the TP3420 transmit buffer. In TE mode DSI Slave, this pin is an output BCLK at the frequency selected by the Digital Interface Format. This clock is phased-locked to the received line signal.
CI	MICROWIRE control channel serial data input.
CO	Control channel serial data output for status information. When not enabled by $\overline{CS}$, this output is Tri-state.
CCLK	Clock input for the Control Channel.
$\overline{CS}$	Chip Select input which enables the control channel data to be shifted in and out when pulled low. When high, this pin inhibits the Control interface.
$\overline{INT}$	Interrupt output, a latched output signal which is normally Tri-state, and goes low to indicate a change of status of the loop transmission system.
$\overline{LSD}$	The Line Signal Detect output, which is normally high-impedance, but pulls low when the device is powered down and a received line signal is detected. It is intended to be used to "wake-up" a microprocessor from a low-power idle mode. This output is disabled when the device is powered up.
L_o+, L_o-	Transmit AMI signal differential outputs to the line transformer. When used with a 2:1 step-down transformer, the line signal conforms to the output pulse masks in I.430.
L_i+, L_i-	Receive AMI signal differential inputs from the line transformer. A 1:2 step-up transformer should be used. The L_i- pin is also the internal voltage reference pin, and must be decoupled to GND with a 10 μf capacitor in parallel with a 0.1 μF ceramic capacitor.

*Crystal specification: 15.36 MHz parallel resonant; $R_s \leq 100\Omega$.

Functional Description

POWER-ON INITIALIZATION

Following the initial application of power, the TP3420 SID enters the power-down (de-activated) state, in which all the internal circuits including the Master oscillator are inactive and in a low power state except for the line-signal detect circuit; the line outputs L_o+/L_o- are in a high impedance state and the System Interface is inactive. All bits in the Control Register power-up as indicated in Table 1. A Control Register instruction is required following power-up to define the format of the Digital Interface, and to select TE mode if required, (see Device Modes Section). In both NT and TE modes, a Line-Signal Detect circuit monitors the line while powered-down, to enable loop transmission to be initiated from either end.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate-Mark Inversion (AMI) coding with inverted binary is used, as illustrated in *Figure 1*. This coding rule requires that a binary ONE is represented by 0V high impedance output, whereas a binary ZERO is represented by a positive or negative-going 100% duty-cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c.-balanced line signal.

The frame format used in the TP3420 SID follows the CCITT recommendation specified in I.430 and illustrated in *Figure 2*. Each complete frame consists of 48 bits, with a line bit rate of 192 kb/s, giving a frame repetition rate of 4 kHz. A violation of the AMI coding rule is used to indicate a frame boundary, by using a $0+$ bit followed by a $0-$ balance bit to indicate the start of a frame, and forcing the first binary zero following the balance bit to be of the same polarity as the balance bit.

In the Network Termination (NT-1) to the Terminal Equipment (TE) transmission direction the frame contains an echo channel, the E bit, which is used to retransmit the D bits that are received from the TE. The last bit of this frame is used as a frame balancing bit. In the TE to NT direction, d.c.-balancing is carried out for each channel, as illustrated in *Figure 2*.

LINE TRANSMIT SECTION

The differential line-driver outputs, L_o+ and L_o-, are designed to drive a transformer with an external termination resistor. A 2:1 transformer, terminated in 50Ω, results in a signal amplitude of nominally 750 mV pk on the line. When driving a binary 1 symbol the output presents a high impedance in accordance with I.430. When driving a $0+$ or $0-$ symbol a voltage-limited current source is turned on. Short-circuit protection is included in the output stage; over-voltage protection is required externally, see the Applications section.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1:2 transformer which may be of the same type used for the transmit direction. At the front-end of the receive section is a continuous filter which limits the noise bandwidth. To correct pulse attenuation and distortion caused by the transmission line in point-to-point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics. This equalizer is always enabled when either TE mode or NT Mode Adaptive Sampling is selected, but is disabled for short passive bus applications when NT Mode Fixed Sampling is selected. An adaptive threshold circuit maximizes the Signal-to-Noise ratio in the eye at the detector for all loop conditions.

A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols.

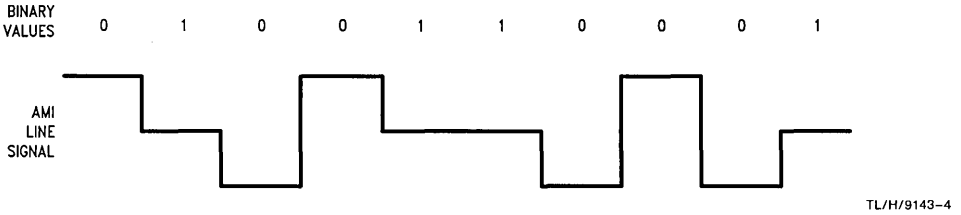


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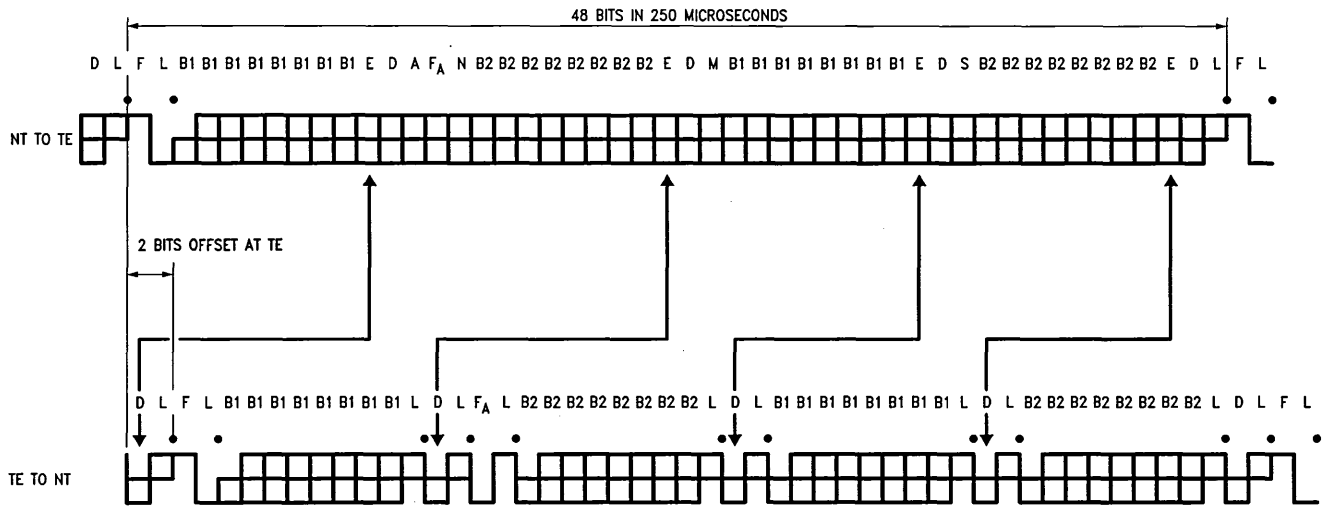
FIGURE 1. Inverted AMI Line-Coding Rule



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Legend:

F	= Framing bit	**N**	= bit set to a binary value N = $\overline{F_A}$
L	= DC Balancing bit	**B1**	= bit within B-channel 1
D	= D-channel bit	**B2**	= bit within B-channel 2
E	= D-echo-channel bit	**A**	= bit used for activation
F_A	= Auxiliary framing bit or Q Channel bit	**S**	= S Channel bit
M	= Multiframe Sync bit		

• Dots mark the boundaries of those parts of the frame that are independently DC-balanced

FIGURE 2. Frame Format

Functional Description (Continued)

The MCLK input provides the reference clock for the DPLL at 15.36 MHz. Clocks for the digital interface timing may either be locked to this recovered clock, as in TE mode Digital System Interface Master, or may be slaved to an external source, as in the T-interface side of an NT-2. In this latter mode, and when the device is in NT mode, re-timing circuitry on the TP3420/1 allows the MCLK frequency to be plesiochronous with respect to the network clock, i.e. the 8 kHz FS_x input, provided the frequency inaccuracy of the network clock plus that of the MCLK source does not exceed 500 ppm from nominal.

When the device is powered-down, a Line-Signal Detect circuit, which can discriminate a valid line signal from noise, is enabled to detect the presence of incoming data if the far-end starts to activate the loop.

DIGITAL SYSTEM INTERFACE

The digital system interface (DSI) on the TP3420 combines 'B' and 'D' channel data onto common pins to provide maximum flexibility with minimum pin count. Several multiplexed formats of the B and D channel data are available as shown in *Figure 3*. Selection is made via the Control Register. At this interface, phase skew between transmit and receive directions may be accommodated at the line card or NT-1/2 end since separate frame sync inputs, FS_a and FS_b, are provided. Each of these synchronizes a counter which gates the transfer of B1 and B2 channels in consecutive time-slots across the digital interface. The serial shift rate is determined by the BCLK input, and may be any frequency from 256 kHz to 4.096 MHz. Thus, for applications on a PABX line-card (in NT mode), the 'B' and 'D' channel slots can be interfaced to a TDM bus and assigned to a time-slot.

At the TE end, FS_a is an output indicating the start of both transmit and receive 'B' channel data transfers. BCLK is also an output at the serial data shift rate, which is dependent on the format selected.

CONTROL INTERFACE

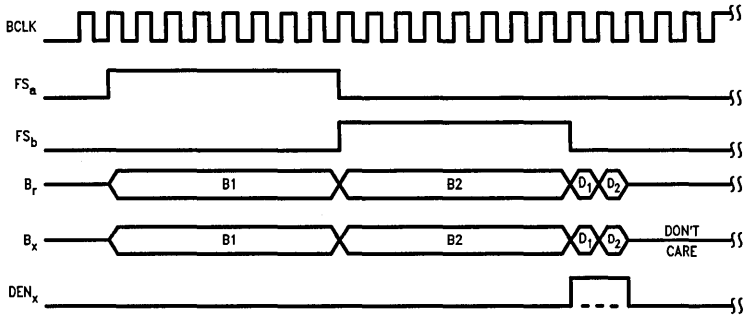
A serial interface, which can be clocked independently from the 'B' and 'D' channel system interface, is provided for microprocessor control of various functions in the TP3420. All data transfers consist of a single byte shifted into the Control Register via the CI pin, simultaneous with a single byte shifted out from the Status Register via the CO pin.

Data shifts in to CI on rising edges of CCLK and out from CO on falling edges when $\overline{CS}$ is pulled low for 8 cycles of CCLK. An Interrupt output, $\overline{INT}$ goes low to alert the microprocessor whenever a change occurs in one or more of the conditions indicated in the Status Register. This latched output is cleared to a high impedance state by the first rising CCLK edge after $\overline{CS}$ goes low. When reading the Status Register the CI input is ignored.

Figure 4 shows the timing for this interface, and Tables I and II list the control functions and status indicators.

Functional Description (Continued)

Format 1



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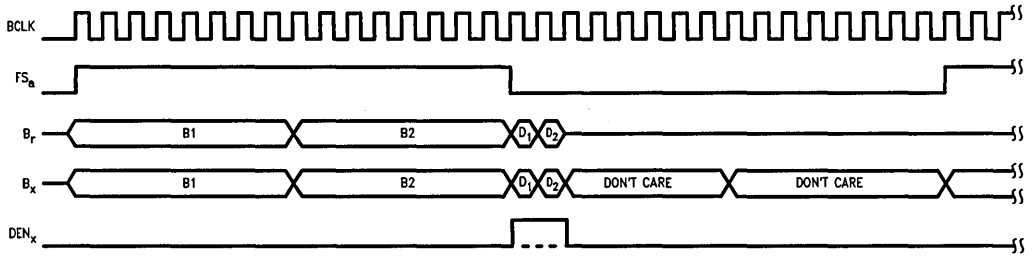
Format 2



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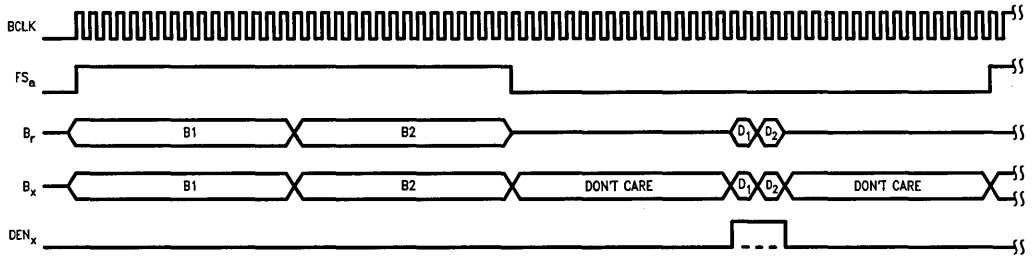
Format 3



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Format 4

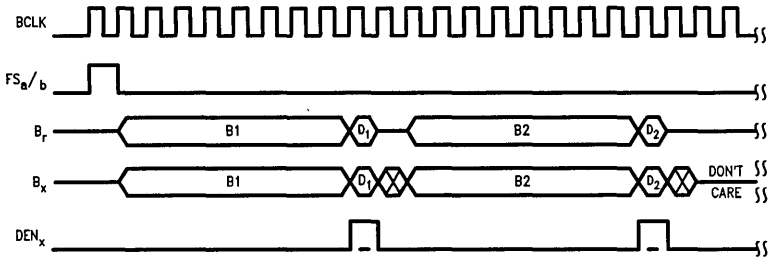

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FIGURE 3. Digital System Interface Formats

Note: The DEN$_X$ output functions in TE Master Mode only.

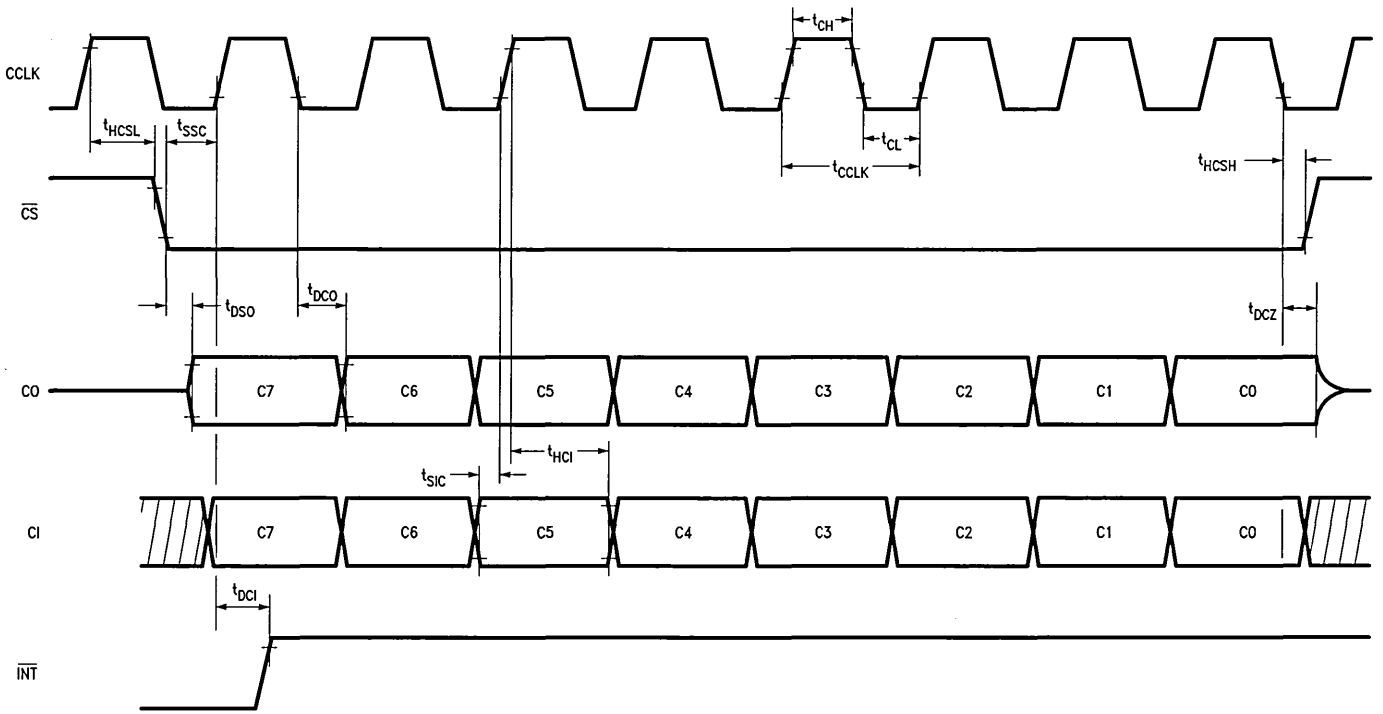


FIGURE 4. Control Interface Timing

Functional Description (Continued)

TABLE I. Control Register Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Activation/Deactivation									
*Power-Down	PDN	0	0	0	0	0	0	0	0
Power-Up	PUP	0	0	1	0	0	0	0	0
Deactivation Request	DR	0	0	0	0	0	0	0	1
Timer 1 (NI) or Timer 3 (TE) Expired	T13	0	0	0	0	0	0	1	0
Activation Request	AR	0	0	0	0	0	0	1	1
Device Modes									
*NT Mode Adaptive Sampling	NTA	0	0	0	0	0	1	0	0
NT Mode Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Mode Digital System Interface Slave	TES	0	0	0	0	0	1	1	0
TE Mode Digital System Interface Master	TEM	0	0	0	0	0	1	1	1
Digital Interface Formats									
*Digital System Interface Format 1	DIF1	0	0	0	0	1	0	0	0
Digital System Interface Format 2	DIF2	0	0	0	0	1	0	0	1
Digital System Interface Format 3	DIF3	0	0	0	0	1	0	1	0
Digital System Interface Format 4	DIF4	0	0	0	0	1	0	1	1
B Channel Exchange									
*B Channels Mapped Direct, B1 to B1, B2 to B2	BDIR	0	0	0	0	1	1	0	0
B Channels Exchanged, B1 to B2, B2 to B1	BEX	0	0	0	0	1	1	0	1
D Channel Access									
D Channel Request, Class 1 Message	DREQ1	0	0	0	0	1	1	1	0
D Channel Request, Class 2 Message	DREQ2	0	0	0	0	1	1	1	1
End of Message Interrupt									
*EOM Interrupt Enabled	EIE	0	0	0	1	0	0	0	0
EOM Interrupt Disabled	EIO	0	0	0	1	0	0	0	1
Multiframe Circuit and Interrupt									
Multiframe Circuit and Interrupt Enabled	MIE	0	0	0	1	0	0	1	0
*Multiframe Circuit and Interrupt Disabled	MID	0	0	0	1	0	0	1	1
Multiframe Transmit Register									
Write to Multiframe Transmit Register	MFT	0	0	1	1	M1	M2	M3	M4
B1 Channel Enable/Disable									
B1 Channel Enabled	B1E	0	0	0	1	0	1	0	0
*B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enable/Disable									
*B2 Channel Enabled	B2E	0	0	0	1	0	1	1	0
B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1

* Indicates initial state following Power-on Initialization.

Functional Description (Continued)

TABLE I. Control Register Functions (Continued)

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Loopback Test Modes									
Loopback B1 Towards Line Interface	LBL1	0	0	0	1	1	0	0	0
Loopback B2 Towards Line Interface	LBL2	0	0	0	1	1	0	0	1
Loopback 2B + D Towards System Interface	LBS	0	0	0	1	1	0	1	0
*Clear All Loopbacks	CAL	0	0	0	1	1	0	1	1

TABLE II. Status Register Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
No Change	NOC	0	0	0	0	0	0	0	0
Line Signal Detected from Far-End	LSD	0	0	0	0	0	0	1	0
Activation Pending	AP	0	0	0	0	0	0	1	1
End of Message	EOM	0	0	0	0	0	1	1	0
Lost Contention	CON	0	0	0	0	0	1	1	1
Multiframe Receive Buffer Requires Service	MFR	0	0	1	1	M1	M2	M3	M4
Activation Indication	AI	0	0	0	0	1	1	0	0
Error Indication	EI	0	0	0	0	1	1	1	0
Deactivation Indication	DI	0	0	0	0	1	1	1	1

STATUS INDICATOR DESCRIPTIONS

LSD If set, indicates that the far-end of the line is attempting to Activate the interface. May be used as an alternative to the LSD pin to "wake-up" a microprocessor.

AP If set, indicates that either INFO 1 frames have been identified in an NT receiver, or INFO 2 or INFO 4 frames have been identified in a TE receiver. Requires an AR control instruction to allow Activation to be completed.

EOM Set when the closing flag of a D-channel message has been transmitted by a TE on the S interface, indicating successful completion of a packet. The Interrupt associated with this bit can be disabled via the Control Register if desired.

CON Set when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit, indicating a lost collision.

MFR Set when the Multiframe receive data buffer requires servicing, after 3 consecutive identical Multiframe words have been detected. All Multiframing functions can be disabled via the Control Register if desired.

AI If set, indicates that the interface has been successfully Activated in response to an Activation Request.

EI Set when loss of frame alignment is detected.

DI If set, indicates that the interface has been Deactivated.

CONTROL FUNCTION DESCRIPTIONS

The Control Functions listed in Table I have been separated into groups to indicate that only 1 function within each group should be selected at a time.

ACTIVATION/DEACTIVATION

PUP This power-up command enables all analog circuitry, starts the XTAL and resets the state machines to the de-activated state, i.e. transmitting INFO 0 (no signal). It also inhibits the LSD output.

PDN This power-down command immediately forces the device to a low power state, without sequencing through any of the de-activation states. It should therefore only be used after the TP3420 has been put in a known state, e.g. in a TE after a DI status indication has been reported.

AR Activation Request, which initiates the specified Activation sequence. It is recommended that an AR be delayed at least 2 ms after the device is powered-up.

DR Deactivation Request, which forces the device through the appropriate deactivation sequence specified in I.430. Should be used at the NT end only.

T13 Indicates that the appropriate Activation Timer has expired without Activation being achieved, and forces an orderly deactivation.

Functional Description (Continued)

DEVICE MODES

NTA NT Mode, Adaptive Sampling should be selected when the device is in an NT on any wiring configuration up to the maximum specified length for operation. Multiple terminals, if required, must be grouped within approximately 50 meters of each other (depending on cable capacitance, see I.430). The Digital System Interface is a slave to external BCLK and FS sources.

NTF NT Mode Fixed Sampling should be selected when the device is in an NT on a passive bus wiring configuration up to approximately 200 meters in length (depending on cable type). In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed, to enable multiple terminals (nominally up to 8) to be connected anywhere along the passive bus. Again, the DSI is a slave to external BCLK and FS sources.

TEM TE Mode DSI Master should be selected when the device is in a TE. The TP3420 is then the source of the BCLK and FS signals, and access to the Transmit D channel, including the priority and contention resolution control, is enabled as described in the section on TE Mode D-Channel Access.

TES TE Mode DSI Slave should be selected when the device is used on the T-interface side of an NT-2. The TP3420 System Interface is then driven by BCLK and FS sources in the NT-2. Data buffers and a clock re-synchronizer enable this interface to function with jittering sources for BCLK and FS. All D Channel access control circuitry is disabled, i.e. D Channel data at the Bx input is continuously transmitted to the line; there is no monitoring of the D-echo channel from the network direction, and DREQ instructions are ignored.

DIGITAL INTERFACE FORMATS

DIF1) DIF2) DIF3) DIF4) These instructions select the format of the Digital Interface timing, see *Figure 3*.

B CHANNEL CONTROL

BDIR) BEX) These commands provide for the exchange of data between the B1 and B2 channels as it passes through the device.

B1E) B1D) B2E) B2D) When either or both B channels are disabled, binary 1s are transmitted on the line in those B channel bit positions, regardless of data at the Bx input, and the Br output is Tri-state in those bit positions.

D CHANNEL ACCESS

DREQ1) DREQ2) This is a request from Layer 2 to the TP3420 in a TE (in Mode TEM only) to attempt to access the transmit D channel at the S interface. The correct priority class for the pending message must also be selected.

LOOPBACK TEST MODES

Two classes of loopback mode are available on the SID, selected by writing the appropriate Control instruction.

LBS This loopback at the system interface is a full loopback of the 2B + D channels from the Bx input to the Br output. It may be set when the device is either activated, in which case it is transparent (i.e. the composite signal is also transmitted to the line), or when it is deactivated.

LBL1/2 These loopbacks turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.

MULTIFRAME TRANSMIT REGISTER

MFT With the device in TE Mode, data entered in bit positions M1, M2, M3 and M4 is transmitted towards the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT Mode, data entered in the M bit positions is transmitted towards the TE in multiframe bit positions S1, S2, S3 and S4 respectively. The Multiframe Channel and Interrupt must be enabled by an MIE command to use these channels.

ACTIVATION/DE-ACTIVATION: TP3420 IN NT MODE

Activation (i.e. transmission and loop synchronization) may be initiated from either end of the loop. With the TP3420 configured in an NT, the device must be powered up, using a PUP command, followed 2 ms later by an AR instruction to the Control Register. Network timing, i.e., an 8 kHz input to FS_a, must be present at this time. The device then begins to send data framed as INFO 2 type, in which bits in the B, D and D-echo channels are set to binary 0. These frames are detected by the TE, which replies with data framed as INFO 3 type, synchronized to received frames. A flywheel circuit in the TP3420 NT searches for 3 consecutive correctly formatted receive frames to acquire full loop synchronization. When it is correctly in sync with received bursts, the NT sends INFO 4 frames, in which the B and D channels are enabled for transmission; Status Indication type AI is set, and the $\overline{INT}$ output is pulled low to indicate Activation complete.

When Activation is initiated by a TE, the TP3420 in NT mode will detect the incoming INFO 1 signal and, if it is powered-down will pull the $\overline{LSD}$ pin and $\overline{INT}$ low, either of which can be used to "wake-up" a microprocessor. A PUP command must then be written to power-up the TP3420. Upon identifying the INFO 1 signal, the device will set Status Indication type AP and pull $\overline{INT}$ low to indicate that Activation is pending. No INFO 2 frames will be transmitted until a Control instruction type AR is written to the device, which allows the Activation sequence to proceed as described above.

Once Activated, loss of frame alignment is assumed by the TP3420 when a time which is equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the NT does detect alignment loss it will start to transmit INFO 2. At this point the Error Indication (EI) primitive is set, the $\overline{INT}$ output is pulled low and the receiver searches to identify the incom-

Functional Description (Continued)

ing signal and attempt to re-acquire loop synchronization. If it successfully re-establishes synchronization with the incoming signal (INFO 3 frames), a further interrupt is generated with Status Indication type AI. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, the loop is de-activated and the transmitter output set to INFO 0. Status Indication type DI is set and the $\overline{INT}$ output pulled low to indicate De-activation.

If required, a PDN instruction may be written to the Control Register to power-down the device and enable the LSD output.

I.430 recommends 2 timers should be available in an NT. An Activation Request to the TP3420 should be associated with the start of an external Timer 1, if required. Timer 1 should be stopped when the AI interrupt is generated following successful Activation. If Timer 1 expires before AI is generated, however, Control Instruction type T13 should be written to the device to force de-activation. Timer 2, which is specified to prevent unintentional reactivation, is not required since the TP3420 can uniquely recognise INFO 1 frames.

ACTIVATION/DE-ACTIVATION: TP3420 IN TE MODE

To activate the loop with the TP3420 at the TE end the device must first be powered-up by a PUP command, followed 2 ms later by a Control Instruction type AR, which is the Activation Request to begin transmission of INFO 1 frames after verifying that INFO 0 is being received from the NT. INFO 1 is a continuous pattern of 0+, 0−, and 6 '1's repeated. At this point the TE is running from its local oscillator and is not receiving any sync information from the NT. When the NT recognises this "wake-up" signal, it begins to transmit INFO 2, synchronized to the network clock. This enables the phase-locked loop in the TE's receiver to correctly identify bit timing from the NT and to synchronize its own transmission to that of the NT. On identifying INFO 2 for 3 consecutive frames, the TE changes its transmit data to INFO 3 and awaits the return of INFO 4 from the NT. Identification of INFO 4 completes the Activation sequence, so Status Indication type AI is set, and the $\overline{INT}$ output pulled low.

When Activation is initiated by the NT, if the TP3420 in TE mode is powered down, it will pull the $\overline{LSD}$ pin and $\overline{INT}$ low on receiving a line signal. Either of these can be used to "wake-up" a microprocessor. A PUP command is required to enable the device to power-up, identify the received signal, and acquire bit and frame synchronization. Once INFO 2 has been identified, the TP3420 will pull $\overline{INT}$ low, with Status Indication type AP set, to alert the microprocessor that Activation is pending. The microprocessor must respond by writing Control Instruction type AR in order for Activation to proceed. INFO 3 frames are then transmitted with active data.

As in NT mode, once Activated, loss of frame alignment is assumed by the TP3420 when a time equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the TE does detect alignment loss it will cease transmitting immediately. At this point the Error Indication (EI) primitive is set in the Status Register, the $\overline{INT}$ output is pulled low and the receiver searches to re-acquire loop synchronization if INFO 2 or INFO 4 frames are still being received. If synchronization is re-established, a further interrupt is generated, with Status Indication type AI. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, the loop is de-activated, Status Indication type DI is set and the $\overline{INT}$ output pulled low to indicate De-activation.

I.430 does not provide for Deactivation to be initiated by a TE. However, a Power-down state may be forced if required, normally after Deactivation has been established by the network.

If required, an external Timer 3 should be started when an Activation Request is sent to the TP3420. The subsequent AI interrupt, indicating Activation is complete, should be used to stop the timer. If the timer expires before an AI is generated, Control Instruction type T13 must be written to the device to force the transmission of INFO 0.

TE MODE D-Channel Access

In TE mode DSI Master only, the TP3420 SID arbitrates access for Layer 2 Transmit frames to the D-channel bit positions in accordance with the I.430 Priority Mechanism (I.430 Section 6.1). The shifting of D-channel transmit data from the Layer 2 device into the SID buffer is controlled by gating the DEN_X output with BCLK. When no Layer 2 frame is pending, "1"s are always transmitted by the SID in D-bit positions at the S interface. DEN_X output pulses are inhibited and no D-channel data is shifted into the B_X input. An external Layer 2 device requiring to start transmission of a packet should first prime its Transmit buffer such that the opening flag is ready to be shifted across the digital interface. Then a Control instruction, type DREQ, will initiate the D-channel access sequence. DREQ instructions require either that a Priority Class 1 (signalling) packet, or a Priority Class 2 packet, is selected.

In response to the DREQ instruction, the DEN_X output is enabled to pre-fetch the opening flag from the Layer 2 device into the D-channel buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S interface (in a point-to-multipoint wiring configuration) is transmitting in the D-channel. This is assured by counting consecutive "1"s in the E-bit position of frames received from the NT. At least 8 consecutive "1"s must be detected before transmission of the pending D-channel frame begins, in accordance with Table III.

TABLE III. D-Channel Access Criteria

Number of Consecutive "1"s in the E-Channel	D-Channel Access
7	Abort. Possible re-try by the transmitting TE.
8	Signalling packet (Priority Class 1) may begin (Note 1).
9	Signalling packet may begin unconditionally.
10	Any packet type may begin (Note 2).
11	Any packet type may begin unconditionally

Note 1: Only if, since the SID last transmitted a complete Class 1 packet, a sequence of ≥ 9 consecutive "1"s has been detected in the E-channel.

Note 2: Only if, since the SID last transmitted a complete packet of either class, a sequence of ≥ 11 consecutive "1"s has been detected in the E-channel.

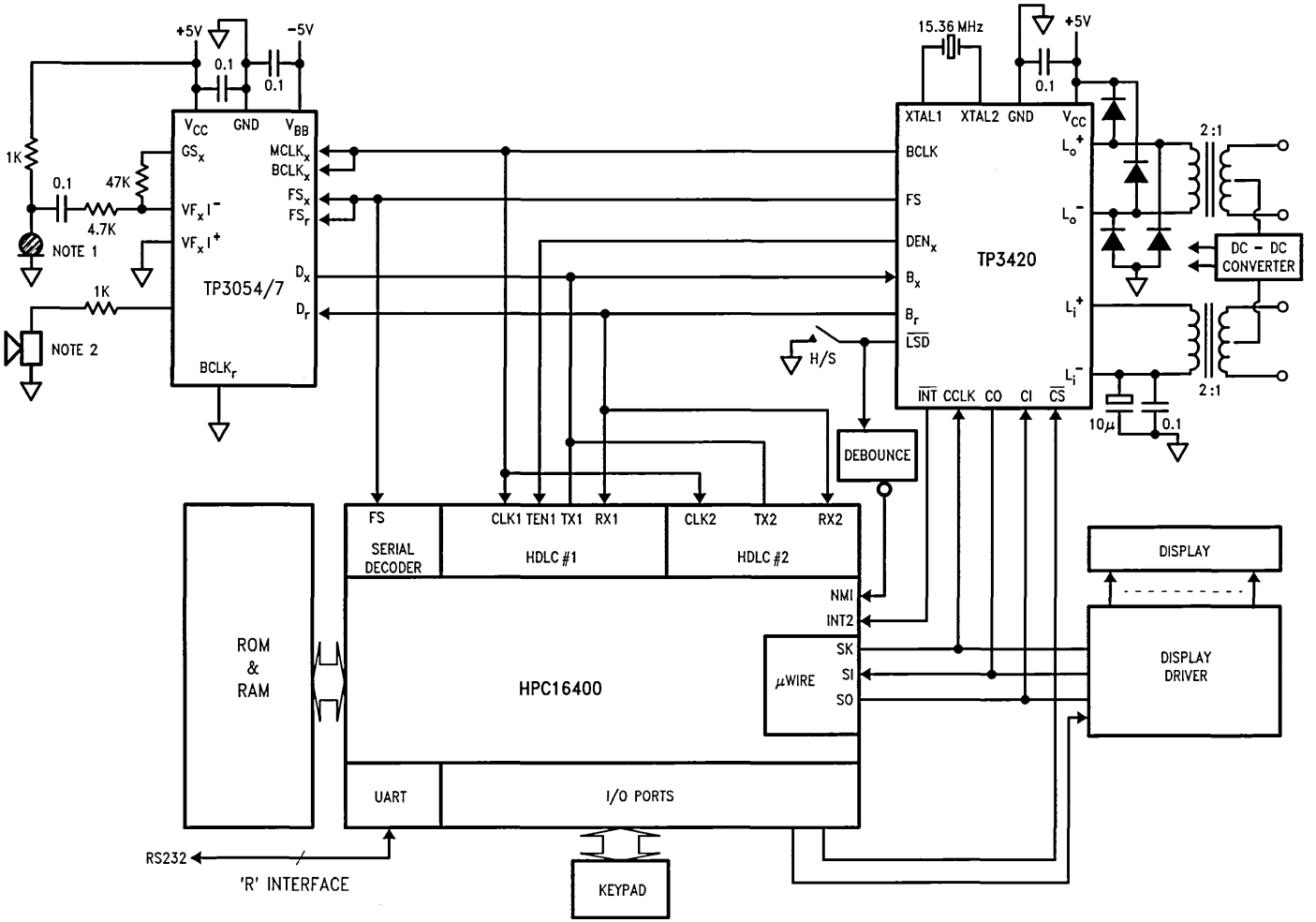
Functional Description (Continued)

If another TE is active in the D-channel, DEN_X pulses are inhibited once the opening flag is in the Transmit buffer, to prevent further fetching of transmit data from the Layer 2 device until D-channel access is achieved. As soon as the required number of consecutive E-channel "1"s has been counted, the leading 0 of the opening flag is transmitted in the next D-bit position towards the NT. DEN_X pulses are also re-enabled in order to shift D-channel bits from the Layer 2 device into the SID transmit buffer. No interrupts are necessary for local flow control between the Layer 2 processor and the TP3420.

During transmission in the D-channel the TP3420 SID continues to compare each E-bit received from the NT with the D-channel bit previously transmitted before proceeding to send the next D-bit. In the event of a mis-match, a contention for the previous D-bit is assumed to have been won by another TE. Transmission of the current packet therefore ceases and "1"s are transmitted in all following D-bit positions. Status Indication type CON is set, and the $\overline{INT}$ output is pulled low to interrupt the Layer 2 transmit processor. DEN_X output pulses are again inhibited.

In order to retransmit the lost packet, the Layer 2 device must begin as before, by priming its Transmit buffer with the packet header and writing a DREQ instruction into the Control Register.

Successful completion of a transmit packet is detected by the TP3420 when the closing flag is transmitted in the D channel. '1's are then transmitted in the following D bit positions, with the DEN_X output held low to prevent further transfer of data from the Layer 2 device. The $\overline{INT}$ output is pulled Low (if enabled), with Status Indication type EOM set, to indicate the End of Message.



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Note 1: Primotype EM80-PMI2 or similar.

Note 2: Primotype DH31 or similar.

FIGURE 5. Typical Application in a TE and/or TA

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at L_i, L_O	V_{CC} +1V to GND −1V
Voltage at any Digital Input	V_{CC} +1V to GND −1V
Storage Temperature Range	−65°C to +150°C
Current at L_O	±100 mA
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics

Unless otherwise noted: V_{CC} = 5V±5%, GND = 0V, T_A = 0°C to 70°C. Typical characteristics are specified at V_{CC} = 5V, T_A = 25°C. All signals are referenced to GND

Symbol	Parameter	Conditions	Limits		Units
			Min	Max	
DIGITAL INTERFACES					
V_{IL}	Input Low Voltage	All Digital Inputs		0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2.2		V
V_{OL}	Output Low Voltage	B_x, I_L = −3.2 mA All Other Digital Outputs, I_L = −1 mA		0.4	V
V_{OH}	Output High Voltage	B_x, I_L = −3.2 mA All Other Digital Outputs, I_L = −1 mA	2.4		V
I_I	Input Current	Any Digital Input, GND < V_{IN} < V_{CC}	−10	10	µA
I_{OZ}	Output Current in High Impedance State (Tri-State)	B_x GND < V_{OUT} < V_{CC}	−10	10	µA
LINE INTERFACES					
I_{Li}	Input Leakage	0V < L_i+, L_i− < 5.0V	−1.0	1.0	µA
R_{Li}	Input Resistance	0V < L_i+, L_i− < 5.0V	20		kΩ
V_{Li}	Input Voltage Range		−0.5	V_{CC} + 0.5V	V
RL_{LO}	Load Resistance	Between L_O+ and L_O−	200		Ω
CL_{LO}	Load Capacitance			200	pF
VOS	Differential Output Offset Voltage at L_O+, L_O−	Driving Binary 1s	−20	+20	mV
POWER DISSIPATION					
$I_{CC}0$	Power Down Current (Deactivated)	All Outputs Open-Circuit		600	µA
$I_{CC}1$	Power Up Current	As Above		15.0	mA
TRANSMISSION PERFORMANCE					
	Transmit Pulse Amplitude	R_L = 200 Ω Between L_o+ and L_o−	±1.4	±1.6	Vpk
	Input Pulse Amplitude	Differential Between L_i+ and L_i−	±100		mVpk
	MCLK/XTAL Input Clock Jitter			50	ns
	Timing Recovery Jitter	BCLK Output at TE Relative to MCLK at NT	−130	+130	ns

Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL SYSTEM INTERFACE						
F_{MCK}	Master Clock Frequency			15.36		MHz
F_{BCK}	Bit Clock Frequency		256		4096	kHz
t_{MH}, t_{ML}	Clock Pulse Width Hi & Low for MCLK	V_{IH} = 2.0V V_{IL} = 0.8V	20			ns
t_{BH}, t_{BL}	Clock Pulse Width Hi & Low for BCLK	V_{IH} = 2.0V V_{IL} = 0.8V	60			ns
t_{MR}, t_{MF}	Rise and Fall Time of MCLK	Used as a Logic Input			10	ns
t_{BR}, t_{BF}	Rise and Fall Time of BCLK				15	ns
t_{SBC}	Set up Time, B_x Valid to BCLK Low		30			ns
t_{HCB}	Hold Time, BCLK Low to B_x Invalid		20			ns
t_{HCF}	Hold Time, BCLK High to FS_a and FS_b		0			ns
t_{SFC}	Set up Time, FS_a to BCLK Low	NT and TES Modes only	30			ns
t_{HCF}	Hold Time, BCLK Low to FS_b Low	NT and TES Modes only	20			ns
t_{DBF}	Delay Time, BCLK High to FS_a and FS_b Transitions	TEM mode only			30	ns
t_{DCB}	Delay Time, BCLK High to Data Valid		20		80	ns
t_{DCBZ}	Delay Time, BCLK Low to Data Invalid	TEM Mode only	50		120	ns
t_{DCD}	Delay Time, BCLK High to DEN_x Transition	TEM Mode only			30	ns
CONTROL INTERFACE						
t_{CH}	CCLK High Duration		100			ns
t_{CL}	CCLK Low Duration		100			ns
t_{SIC}	Setup Time, CI Valid to CCLK High		50			ns
t_{HCI}	Hold Time, CCLK High to CI Invalid		20			ns
t_{SSC}	Setup Time from $\overline{CS}$ Low to CCLK High		50			ns
t_{DSO}	Delay Time from $\overline{CS}$ Low to CO Valid	Bit C7 only			50	ns
t_{DCO}	Delay Time from CCLK Low to CO Data Valid				20	ns
t_{DCZ}	Delay Time from CCLK 8 Low to CO Tri-State				50	ns

Timing Information

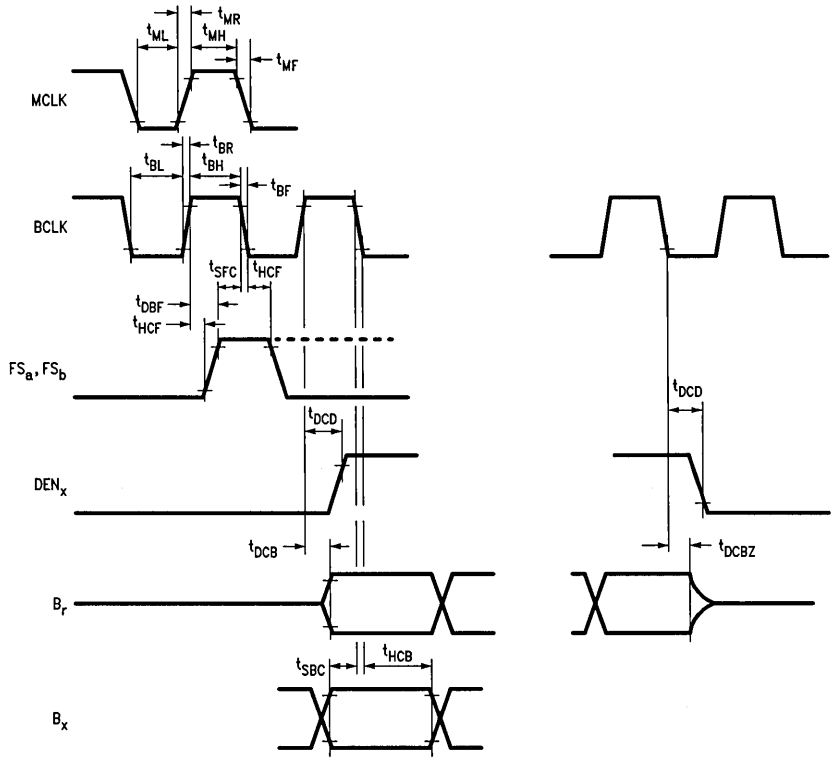

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FIGURE 6. Timing Details for Digital System Interface

Definitions and Timing Conventions

DEFINITIONS

V_{IH} — V_{IH} is the d.c. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.

V_{IL} — V_{IL} is the d.c. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device.

V_{OH} — V_{OH} is the minimum d.c. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.

V_{OL} — V_{OL} is the maximum d.c. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.

Threshold Region — The threshold region is the range of input voltages between V_{IL} and V_{IH}.

Valid Signal — A signal is Valid if it is in one of the valid logic states, (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.

Invalid Signal — A signal is Invalid if it is not in a valid logic state, i.e. when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purposes of this timing specification the following conventions apply:

Input Signals — All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ ns.

Period — The period of clock signal is designated as t_{Pxx} where xx represents the mnemonic of the clock signal being specified.

Rise Time — Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}.

Fall Time — Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}.

Pulse Width High — The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.

Pulse Width Low — The low pulse width is designated as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.

Setup Time — Setup times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.

Hold Time — Hold times are designated as t_{Hxxww}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by mnemonic xx. Hold times are measured from xx Valid to ww Invalid.

Delay Time — Delay times are designated as $t_{Dxxyy}[\ |H|L]$, where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this data sheet.

National Semiconductor Corporation

PRELIMINARY

HPC16040/HPC26040/HPC36040/HPC46040/HPC16030/ HPC36030/HPC46030 High-Performance Microcontrollers

General Description

The HPC16040 is a member of the HPC™ family of High Performance microControllers. Each member of the family has the same identical core CPU with a unique memory and I/O configuration to suit specific applications. Each part is fabricated in National's advanced microCMOS technology. This process combined with an advanced architecture provides fast, flexible I/O control, efficient data manipulation, and high speed computation.

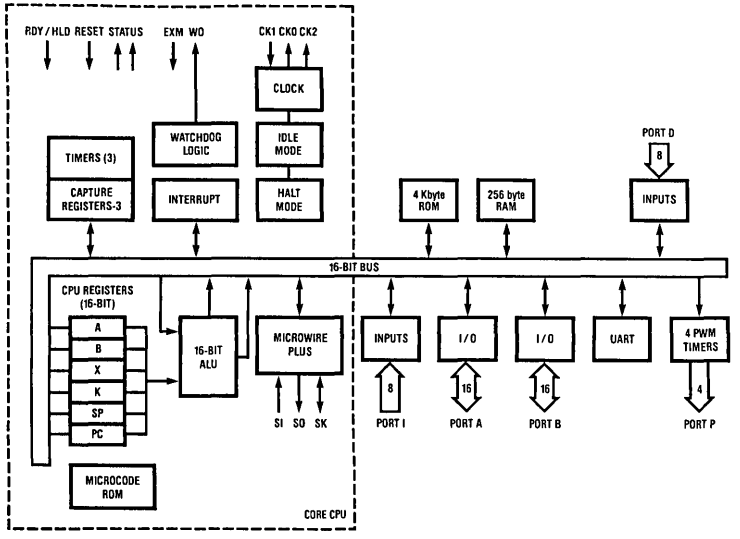
The HPC16040 is a complete microcomputer on a single chip. All system timing, internal logic, ROM, RAM, and I/O are provided on the chip to produce a cost effective solution for high performance applications. On-chip functions such as UART, eight 16-bit timers, vectored interrupts, WATCHDOG™ logic and MICROWIRE/PLUS™ provide a high level of system integration. The ability to address up to 64k bytes of external memory enables the HPC16040 to be used in powerful applications typically performed by microprocessors and expensive peripheral chips.

The microCMOS process results in very low current drain and enables the user to select the optimum speed/power product for his system. The IDLE and HALT modes provide further current savings. The HPC16040 is available in 68-pin PCC, LCC and PGA packages.

Features

- HPC family—core features:
  - — 16-bit architecture, both byte and word
  - — 16-bit data bus, ALU, and registers
  - — 64k bytes of external memory addressing
  - — FAST!—240 ns for register instructions when using 17.0 MHz clock
  - — High code efficiency—most instructions are single byte
  - — 16 x 16 multiply and 32 x 16 divide
  - — Eight vectored interrupt sources
  - — Four 16-bit timer/counters with 3 input capture registers and 4 synchronous outputs
  - — WATCHDOG logic monitors processor
  - — MICROWIRE/PLUS serial I/O interface
  - — CMOS—very low power with two power save modes: IDLE and HALT (2 mA, 250 μA—typ.)
- UART—full duplex, programmable baud rate
- Four additional 16-bit timer/counters with pulse width modulated outputs
- 52 general purpose I/O lines (memory mapped)
- 4k bytes of ROM, 256 bytes of RAM on chip
- ROMless versions available
- Wide voltage supply range: 3V to 5.5V
- Industrial (−40°C to +85°C) and military (−55°C to +125°C) temperature ranges

Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Allowable Source or Sink Current	100 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
V_{CC} with Respect to GND	−0.5V to 7.0V
All Other Pins	(V_{CC} + 0.5)V to (GND − 0.5)V

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

V_{CC} = 5.0V ±10% unless otherwise specified, T_A = 0°C to +70°C for HPC46040, −40°C to +85°C for HPC36040, −40°C to +105°C for HPC26040, −55°C to +125°C for HPC16040

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC_1}	Supply Current	V_{CC} = 5.0V, f_{in} = 17.0 MHz*		20		mA
		V_{CC} = 5.0V, f_{in} = 2.0 MHz		2.4		mA
I_{CC_2}	IDLE Mode Current	V_{CC} = 5.0V, f_{in} = 17.0 MHz, T_A = 25°C*		2		mA
		V_{CC} = 5.0V, f_{in} = 2.0 MHz, T_A = 25°C		0.2		mA
I_{CC_3}	HALT Mode Current	V_{CC} = 5.0V, f_{in} = 0 kHz, T_A = 25°C*		250		μA
		V_{CC} = 2.5V, f_{in} = 0 kHz, T_A = 25°C		150		μA
INPUT VOLTAGE LEVELS RESET, NMI, CKI AND WO (SCHMITT TRIGGERED)						
V_{IH_1}	Logic High		0.9 V_{CC}			V
V_{IL_1}	Logic Low				0.1 V_{CC}	V
ALL OTHER INPUTS						
V_{IH_2}	Logic High		0.7 V_{CC}			V
V_{IL_2}	Logic Low				0.2 V_{CC}	V
I_{LI}	Input Leakage Current				±1	μA
C_I	Input Capacitance			10		pF
C_{IO}	I/O Capacitance			20		pF
OUTPUT VOLTAGE LEVELS CMOS OPERATION						
V_{OH_1}	Logic High	I_{OH} = −10 μA	V_{CC} − 0.1			V
V_{OL_1}	Logic Low	I_{OH} = 10 μA			0.1	V
V_{OH_2}	Port A/B Drive, CK2 (A_0–A_{15}, B_{10}, B_{11}, B_{12}, B_{15})	I_{OH} = −7 mA, V_{CC} = 5.0V	2.4			V
V_{OL_2}		I_{OL} = 3 mA			0.4	V
V_{OH_3}	Other Port Pin Drive, WO (open drain) (B_0–B_9, B_{13}, B_{14}, P_0–P_3)	I_{OH} = −1.6 mA, V_{CC} = 5.0V	2.4			V
V_{OL_3}		I_{OL} = 0.5 mA			0.4	V
V_{OH_4}	ST1 and ST2 Drive	I_{OH} = −6 mA, V_{CC} = 5.0V	2.4			V
V_{OL_4}		I_{OL} = 1.6 mA			0.4	V
V_{RAM}	RAM Keep-Alive Voltage			2.5		V
I_{OZ}	TRI-STATE Leakage Current			±5		μA

*Note: I_{CC_1}, I_{CC_2}, I_{CC_3} measured with no external drive (I_{OH} and I_{OL} = 0, I_{IH} and I_{IL} = 0).

AC Electrical Characteristics

V_{CC} = 5.0V ±10%, f_C = 17.0 MHz, T_A = 0°C to +70°C for HPC46040, −40°C to +85°C for HPC36040

Symbol	Parameter	Min	Typ	Max	Units
f_C = CKI freq.	Operating Frequency	2		17.0	MHz
$t_{C1} = 1/f_C$	Clock Period	59			ns
$t_C = 2/f_C$	Timing Cycle	118	120		ns
$t_{LL} = \frac{1}{2} t_C - 9$	ALE Pulse Width	50	60		ns
$t_{ST} = \frac{1}{4} t_C - 6$	Address Valid to ALE Trailing Edge	23	30		ns
$t_{WAIT} = t_C = WS$	Wait State Period	118	120		ns
$f_{XIN} = \frac{1}{19\, t_{C1}}$	External Timer Input Frequency		877		kHz
$t_{XIN} = 3\, t_{C1}$	Pulse Width for Timer Inputs		180		ns
$f_{XOUT} = \frac{1}{16\, t_{C1}}$	Timer Output Frequency		1.04		MHz
$f_{MW} = \frac{1}{19\, t_{C1}}$	External MICROWIRE/PLUS Clock Input Frequency		877		kHz
$f_U = \frac{1}{19\, t_{C1}}$	External UART Clock Input Frequency		877		kHz
t_{DC1C2}	CK2 Delay from CK1			55	ns

Read Cycle Timing with One Wait State

Symbol	Parameter	Min	Typ	Max	Units
$t_{ARR} = \frac{1}{4} t_C - 5$	ALE Trailing Edge to $\overline{RD}$ Falling Edge	24			ns
$t_{RW} = \frac{1}{2} t_C + WS - 10$	$\overline{RD}$ Pulse Width	167			ns
$t_{DR} = \frac{3}{4} t_C - 15$	Data Hold after Rising Edge of $\overline{RD}$	0		75	ns
$t_{ACC} = t_C + WS - 55$	Address Valid to Input Data Valid			181	ns
$t_{RD} = \frac{1}{2} t_C + WS - 65$	$\overline{RD}$ Falling Edge to Data in Valid			112	ns
$t_{RDA} = t_C - 5$	$\overline{RD}$ Rising Edge to Address Valid	111			ns
$t_{VPR} = \frac{1}{4} t_C - 5$	Address Valid from ALE Trailing Edge Prior to $\overline{RD}$	24	35		ns

Write Cycle Timing with One Wait State

Symbol	Parameter	Min	Typ	Max	Units
$t_{ARW} = \frac{1}{2} t_C - 5$	ALE Trailing Edge to $\overline{WR}$ Falling Edge	54			ns
$t_{WW} = \frac{3}{4} t_c + WS - 15$	$\overline{WR}$ Pulse Width	192			ns
$t_{HW} = \frac{1}{4} t_C - 5$	Data Hold after Trailing Edge of $\overline{WR}$	24			ns
$t_V = \frac{1}{2} t_C + WS - 5$	Data Valid before Trailing Edge of $\overline{WR}$	172			ns
$t_{VPW} = \frac{1}{4} t_C + 20$	Address Valid from Trailing Edge Prior to $\overline{WR}$	50			ns

Note: Bus Output (Port A) C_L = 100 pF, CK2 Output C_L = 50 pF, other Outputs C_L = 80 pF.

Ready/Hold Timing f_C = 16.78 MHz with One Wait State

Symbol	Parameter	Min	Typ	Max	Units
$t_{DAR} = 1/4\ t_C + WS - 50$	Falling Edge of ALE to Falling Edge of $\overline{RDY}$		100		ns
$t_{RWP} = t_C$	$\overline{RDY}$ Pulse Width		120		ns
$t_{SALE} = 1/4\ t_C + 40$	Falling Edge of $\overline{HLD}$ to Rising Edge of ALE		70		ns
$t_{HWP} = t_C + 10$	$\overline{HLD}$ Pulse Width		130		ns
t_{HAD}	Rising Edge on $\overline{HLD}$ to Rising Edge on $\overline{HLDA}$		120		ns
$t_{HAE} = t_C + 100$	Falling Edge on $\overline{HLD}$ to Falling Edge on $\overline{HLDA}$		220	*	ns
$t_{BF} = t_C + 30$	Bus Float before Falling Edge on $\overline{HLDA}$		150		ns
$t_{BE} = 2\ t_C + 50$	Bus Enable from Rising Edge of $\overline{HLD}$		290		ns

*Note: t_{HAE} may be as long as ($3t_C$ + 4ws + $72t_C$ + 90) depending on which instruction is being executed, the addressing mode and number of wait states.

Status Timing f_C = 16.78 MHz

Symbol	Parameter	Min	Typ	Max	Units
$t_{SRS2} = 40 - (1/4\ t_C + 25)$	Setup Time for ST2 on Rising Edge of ALE		−15		ns
$t_{HRS2} = 3/4\ t_C - 15$	Hold Time for ST2 on Rising Edge of ALE		75		ns
$t_{SFS2} = 40 - (1/4\ t_C + 25)$	Setup Time for ST2 on Falling Edge of ALE		−15		ns
$t_{HFS2} = 3/4\ t_C - 15$	Hold Time for ST2 on Falling Edge of ALE		75		ns
t_{SFS1}	Setup Time for ST1 on Falling Edge of $\overline{RD}$		20		ns
$t_{HRS1} = 1/2\ t_C - 15$	Hold Time for ST1 on Rising Edge of $\overline{RD}$		45		ns

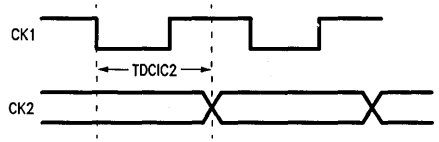
UPI Read/Write Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{UAS}	Address Setup Time to Falling Edge of $\overline{UPIRD}$		5		ns
t_{UAH}	Address Hold Time from Rising Edge of $\overline{UPIRD}$		5		ns
t_{RPW}	$\overline{UPIRD}$ Pulse Width		100		ns
t_{OE}	$\overline{UPIRD}$ Falling Edge to Data Out Valid		60		ns
t_{OD}	End of $\overline{UPIRD}$ to Data Out Valid		35		ns
t_{DRDY}	$\overline{RDRDY}$ Delay from Trailing Edge of $\overline{UPIRD}$		70		ns
t_{WDW}	$\overline{UPIWR}$ Pulse Width		40		ns
t_{UDS}	Data in Valid before Trailing Edge of $\overline{UPIWR}$		10		ns
t_{UDH}	Data in Hold after Trailing Edge of $\overline{UPIWR}$		15		ns
t_A	$\overline{WRRDY}$ Delay from Trailing Edge of $\overline{UPIWR}$		70		ns

Note: Bus Output (Port A) C_L = 100 pF, CK2 Output C_L = 50 F, other Outputs C_L = 80 pF.

Timing Waveforms

CK2 Delay Timing Diagram



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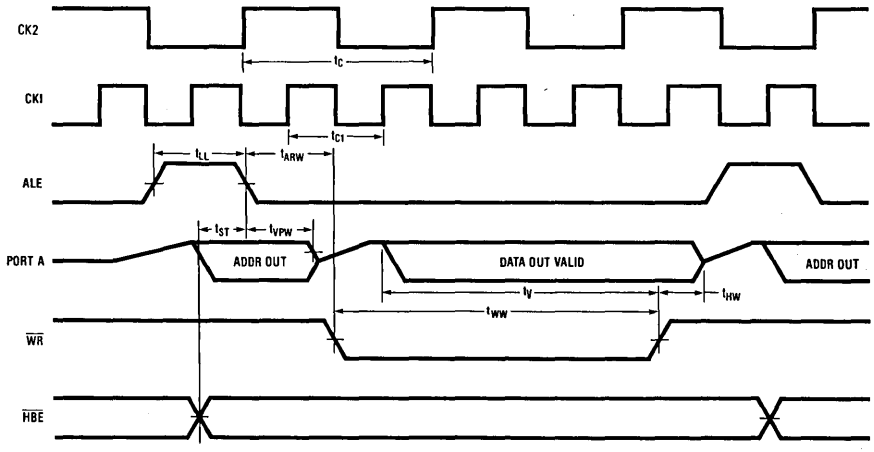

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FIGURE 1. Write Cycle

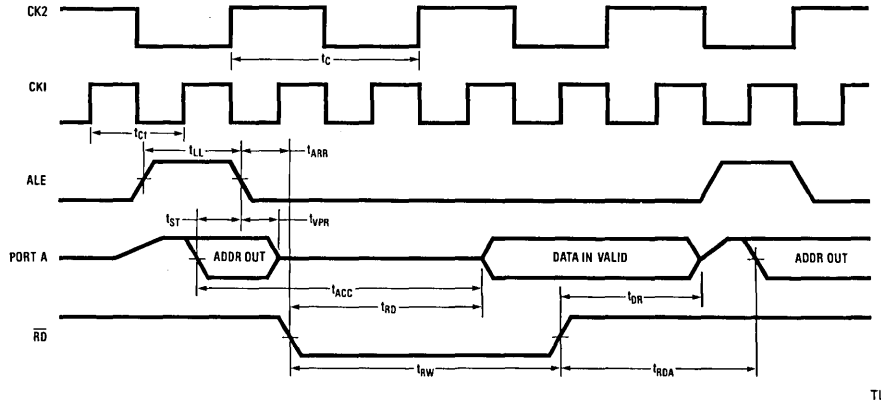

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FIGURE 2. Read Cycle

Timing Waveforms (Continued)

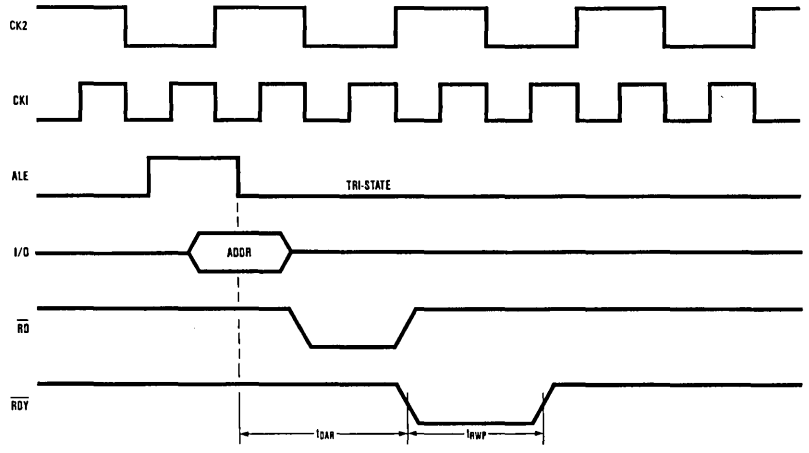

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FIGURE 3. Ready Mode Timing

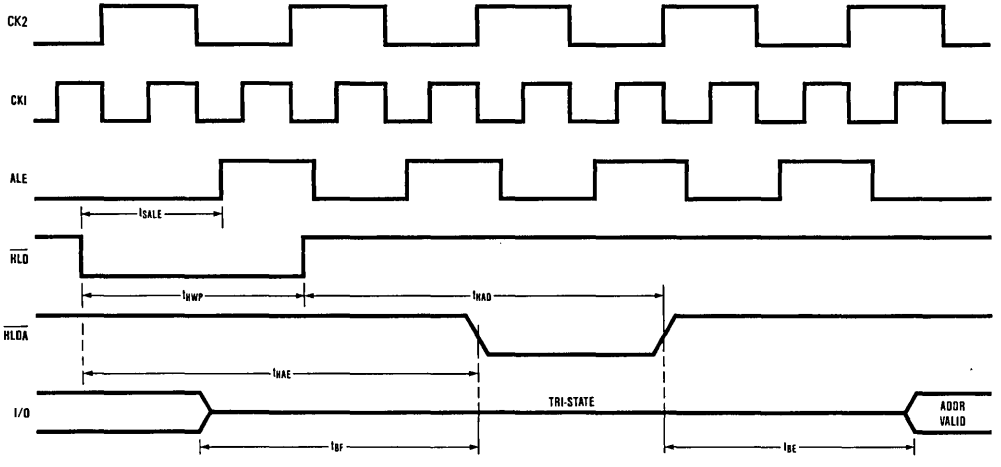

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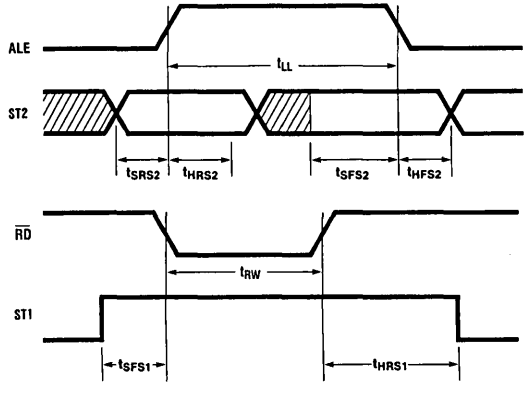
FIGURE 4. Hold Mode Timing



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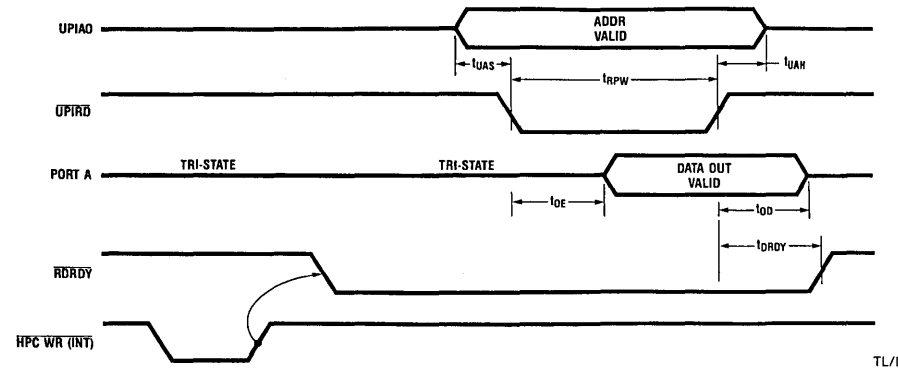
TL/DD/8340-7

FIGURE 5. Status Timing

Timing Waveforms (Continued)



TL/DD/8340-8

FIGURE 6. UPI Read Timing

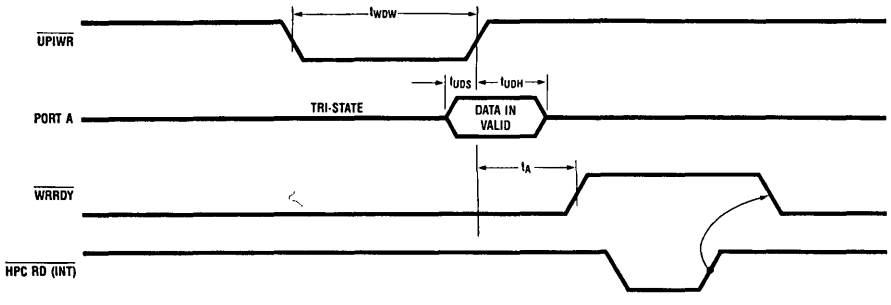


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FIGURE 7. UPI Write Timing

Pin Descriptions

The HPC16040 is available in 68-pin PCC and LCC packages, and a 48-pin ceramic DIP.

I/O PORTS

Port A is a 16-bit bidirectional I/O port with a data direction register to enable each separate pin to be individually defined as an input or output. When accessing external memory, port A is used as the multiplexed address/data bus.

Port B is a 16-bit port with 12 bits of bidirectional I/O similar in structure to Port A. Pins B10, B11, B12 and B15 are general purpose outputs only in this mode. Port B may also be configured via a 16-bit function register BFUN to individually allow each pin to have an alternate function.

B0:	TDX	UART Data Output
B1:		
B2:	CKX	UART Clock (Input or Output)
B3:	T2IO	Timer2 I/O Pin
B4:	T3IO	Timer3 I/O Pin
B5:	SO	MICROWIRE/PLUS Output
B6:	SK	MICROWIRE/PLUS Clock (Input or Output)
B7:	$\overline{\text{HLDA}}$	Hold Acknowledge Output
B8:	TS0	Timer Synchronous Output
B9:	TS1	Timer Synchronous Output
B10:	UA0	Address 0 Input for UPI Mode
B11:	$\overline{\text{WRRDY}}$	Write Ready Output for UPI Mode
B12:		
B13:	TS2	Timer Synchronous Output
B14:	TS3	Timer Synchronous Output
B15:	$\overline{\text{RDRDY}}$	Read Ready Output for UPI Mode

When accessing external memory, four bits of port B are used as follows:

B10:	ALE	Address Latch Enable Output
B11:	$\overline{\text{WR}}$	Write Output
B12:	$\overline{\text{HBE}}$	High Byte Enable Output/Input (sampled at reset)
B15:	$\overline{\text{RD}}$	Read Output

Port I is an 8-bit input port that can be read as general purpose inputs and is also used for the following functions:

I0:		
I1:	NMI	Nonmaskable Interrupt Input
I2:	INT2	Maskable Interrupt/Input Capture/$\overline{\text{URD}}$
I3:	INT3	Maskable Interrupt/Input Capture/$\overline{\text{UWR}}$
I4:	INT4	Maskable Interrupt/Input Capture
I5:	SI	MICROWIRE/PLUS Data Input
I6:	RDX	UART Data Input
I7:		

Port D is an 8-bit input port that can be used as general purpose digital inputs.

Port P is a 4-bit output port that can be used as general purpose data, or selected to be controlled by timers 4

Pin Descriptions (Continued)

through 7 in order to generate frequency, duty cycle and pulse width modulated outputs.

POWER SUPPLY PINS

V_{CC} Positive Power Supply (3V to 5.5V)

GND Ground for On-Chip Logic

DGND Ground for Output Buffers

Note: There are two electrically connected V_{CC} pins on the chip, GND and DGND are electrically isolated. Both V_{CC} pins and both ground pins must be used.

CLOCK PINS

CKI The Chip System Clock Input

CKO The Chip System Clock Output (inversion of CKI)

Pins CKI and CKO are usually connected across an external crystal.

CK2 Clock Output (CKI divided by 2)

OTHER PINS

WO This is an active low open drain output that signals an illegal situation has been detected by the Watch Dog logic.

ST1 Bus Cycle Status Output: indicates first opcode fetch.

ST2 Bus Cycle Status Output: indicates machine states (skip, interrupt and first instruction cycle).

RESET is an active low input that forces the chip to restart and sets the ports in a TRI-STATE® mode.

RDY/HLD has two uses, selected by a software bit. It's either a READY input to extend the bus cycle for slower memories, or a HOLD request input to put the bus in a high impedance state for DMA purposes.

NC (no connection) unused at this time.

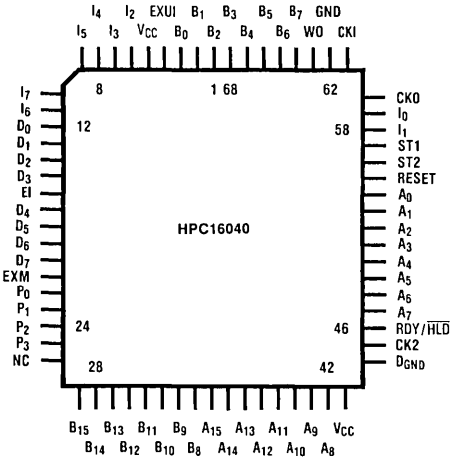
EXM External memory enable (active high) disables internal ROM and maps it to external memory.

EI External interrupt with vector address FFF1:FFF0. (active high)

EXUI External interrupt which is internally OR'ed with the UART interrupt with vector address FFF3:FFF2 (Active Low).

Connection Diagrams

Plastic and Leadless Chip Carriers

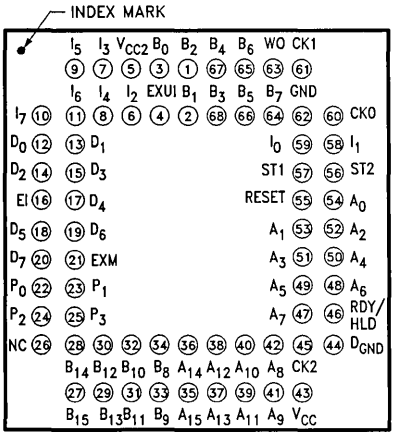


TL/DD/8340-10

Top View

Order Number HPC16040E or V
See NS Package Number E68B or V68A

Pin Grid Array Pinout



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Top View
(looking down on component side of PC Board)

Order Number HPC16040U
See NS Package Number U68A

Ports A and B

The highly flexible A and B ports are similarly structured. The Port A (see *Figure 9*), consists of a data register and a direction register. Port B (see *Figure 10*) has an alternate function register in addition to the data and direction registers. All the control registers are read/write registers.

The associated direction registers allow the port pins to be individually programmed as inputs or outputs. Port pins selected as inputs, are placed in a TRI-STATE mode by resetting corresponding bits in the direction register.

A write operation to a port pin configured as an input causes the value to be written into the data register, a read operation returns the value of the pin. Writing to port pins configured as outputs causes the pins to have the same value, reading the pins returns the value of the data register.

Primary and secondary functions are multiplexed onto Port B through the alternate function register (BFUN). The secondary functions are enabled by setting the corresponding bits in the BFUN register.

Operating Modes

To offer the user a variety of I/O and expanded memory options, the HPC16040 has four operating modes. The four modes are Single-Chip, Expanded, Single-Chip ROMless, and Expanded ROMless. The four modes are determined by the state of both the External Memory (EXM) pin and the External Access (EA) bit in the PSW Register. The HPC16040 System bus consists of port A and four bits of port B. Port A is defined as the address/data bus and the four bits of port B are referred to as the control bus.

SINGLE-CHIP MODE

In this mode, the HPC16040 functions as a self-contained microcomputer. It can address internal memory consisting of 256 bytes of RAM and 4 kbytes of ROM. All ports are configured as memory mapped I/O ports. The HPC16040 reads 8 bits or 16 bits of data from the ports, depending on whether a byte or word format instruction is used (see *Figure 11*). The EXM pin and EA bit of the PSW Register are both logic "0" during Single-Chip mode signifying that on-chip ROM is being addressed and the range is limited to 4k (see Table II).

TABLE II. Operating Modes

External Memory Pin (EXM)	External Access Bit (EA)	Operation Mode
0	0	Single Chip
0	1	Expanded
1	0	Single Chip ROMless
1	1	Expanded ROMless

EXPANDED MODE

The Expanded mode (see *Figures 12* and *13*) is entered by setting the EA bit in the PSW Register. The HPC16040 can operate within the full 64 kbytes of address space. The 64 kbytes of addressable memory includes all on-chip memory because the EXM pin is grounded during this mode. The external memory may be any combination of RAM and ROM. External memory can be accessed with the data bus defined as either 8 bits wide or 16 bits wide. The System bus may be configured in the 8-bit mode by pulling the $\overline{\text{HBE}}$ pin high at reset. Upon entering the expanded mode, port A

Operating Modes (Continued)

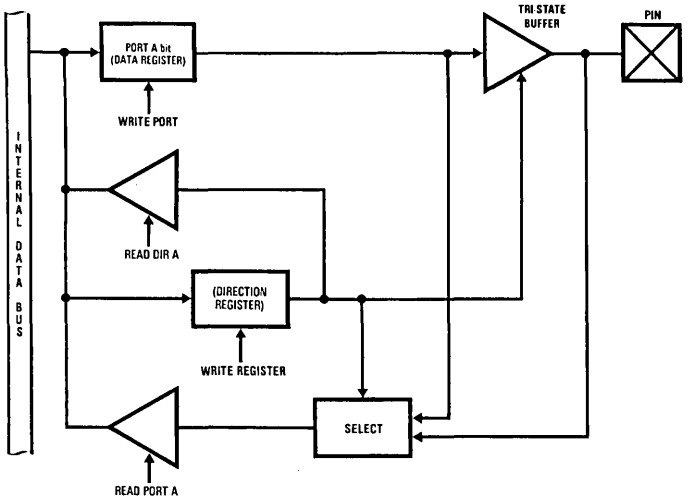

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FIGURE 9. Port A: I/O Structure

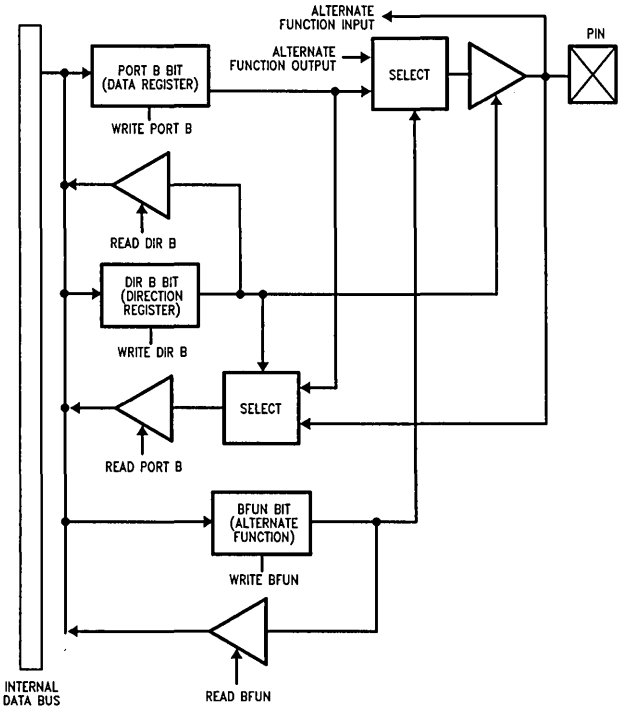

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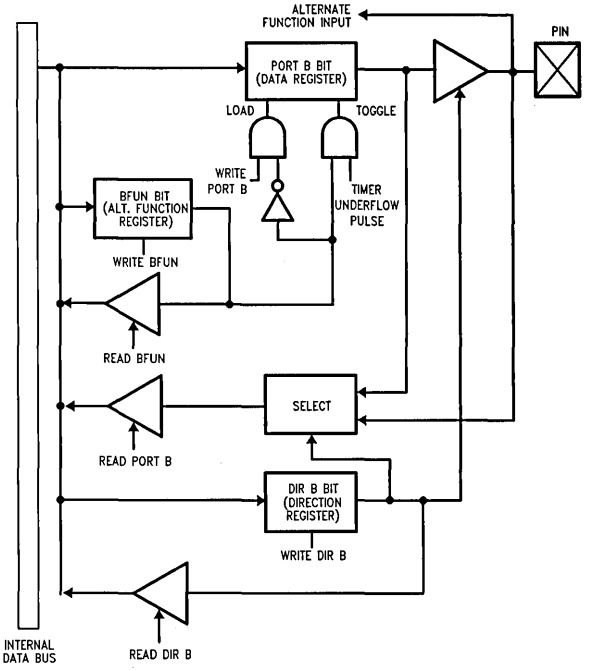
FIGURE 10a. Structure of Port B Pins B0, B1, B2, B5, B6 and B7 (Typical Pins)

2

Operating Modes (Continued)



TL/DD/8340-33

FIGURE 10b. Structure of Port B Pins B3, B4, B8, B9, B13 and B14 (Timer Synchronous Pins)

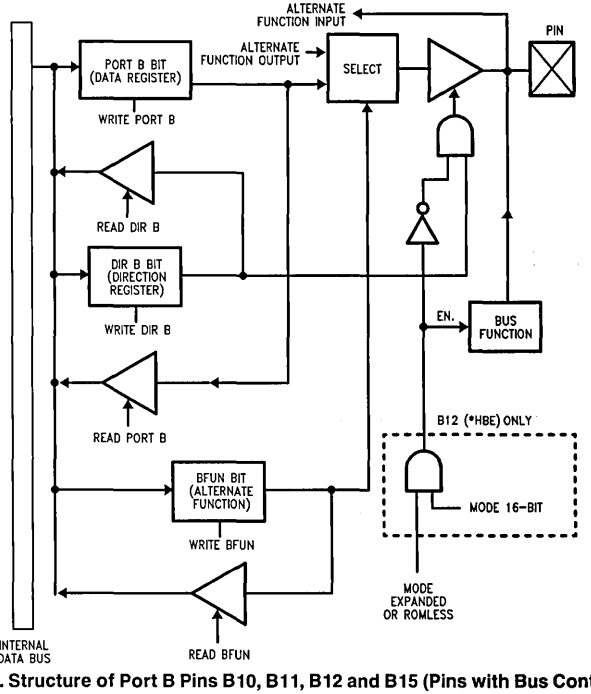


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FIGURE 10c. Structure of Port B Pins B10, B11, B12 and B15 (Pins with Bus Control Roles)

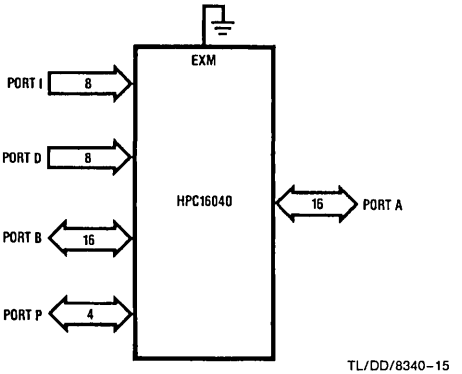
Operating Modes (Continued)

becomes the Address/Data bus. Four bits of port B become ALE, $\overline{WR}$, $\overline{HBE}$ and $\overline{RD}$ signals. The $\overline{RD}$ and $\overline{WR}$ signals are generated only if the selected address is off-chip. The $\overline{HBE}$ is generated only in the 16-bit bus configuration.

ROMless MODES

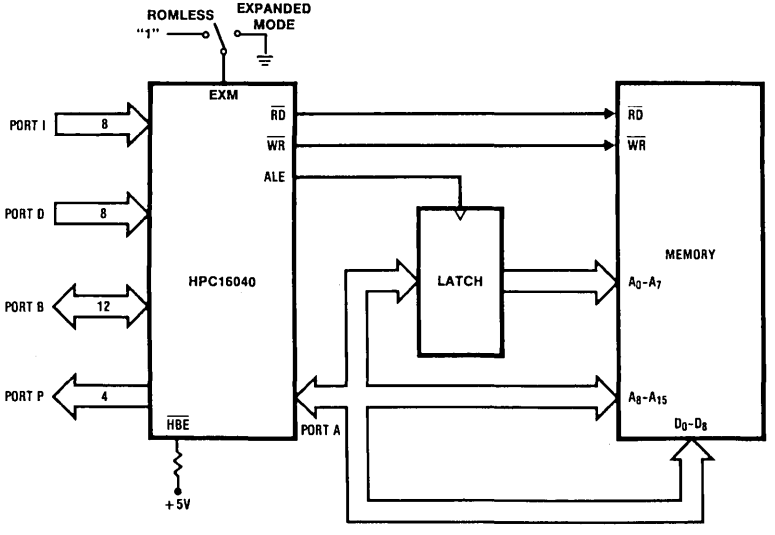
There are two ROMless modes; Single-Chip ROMless and Expanded ROMless. Both ROMless modes are entered by pulling the EXM pin high, (see *Figure 12* and *13*). The EA bit in the PSW Register determines whether the HPC16040 addresses the Single-Chip memory range of 4 kbytes or the Expanded range of 64 kbytes, (see Table II for this information). In both ROMless modes, the HPC16040 continues to use the internal 256 bytes of RAM. The external 4k or 64k of addressed memory may be any combination of RAM and ROM. The address space corresponding to internal ROM is mapped into external memory.

Note: The HPC16040 uses 16-bit words for stack memory. Therefore, when using the 8-bit mode, User's Stack must be in internal RAM.



TL/DD/8340–15

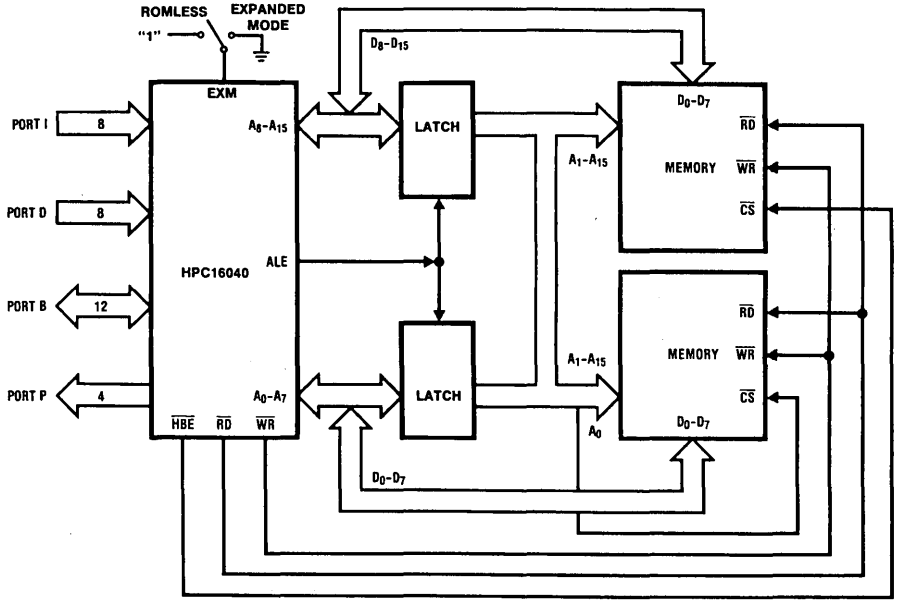
FIGURE 11. Single-Chip Mode



TL/DD/8340–16

FIGURE 12. 8-Bit External Memory

Operating Modes (Continued)



TL/DD/8340-17

FIGURE 13. 16-Bit External Memory

Wait States

The HPC16040 provides four software selectable Wait States that allow access to slower memories. The Wait States are selected by the state of two bits in the PSW register. Additionally, the RDY input may be used to extend the instruction cycle, allowing the user to interface with slow memories and peripherals.

Power Save Modes

Two power saving modes are available on the HPC16040: HALT and IDLE. In the HALT mode, all processor activities are stopped. In the IDLE mode, the on-board oscillator and timer T0 are active but all other processor activities are stopped. In either mode, all on-board RAM, registers and I/O are unaffected.

HALT MODE

The HPC16040 is placed in the HALT mode under software control by setting bits in the PSW. All processor activities, including the clock and timers, are stopped. In the HALT mode, power requirements for the HPC16040 are minimal and the applied voltage (V_{CC}) may be decreased without altering the state of the machine. There are two ways of exiting the HALT mode: via the RESET or the NMI. The RESET input reinitializes the processor. Use of the NMI input will generate a vectored interrupt and resume operation from that point with no initialization. The HALT mode can be enabled or disabled by means of a control register HALT enable. To prevent accidental use of the HALT mode the HALT enable register can be modified only once.

IDLE MODE

The HPC16040 is placed in the IDLE mode through the PSW. In this mode, all processor activity, except the on-board oscillator and Timer T0, is stopped. External interrupt (EXUI) is shared with the UART interrupt. This interrupt is level-low sensitive. To select this interrupt disable the ERI and ETI UART interrupt bits in the ENUI register. To select the UART interrupt leave this pin floating or tie it high. As with the HALT mode, the processor is returned to full operation by the RESET or NMI inputs, but without waiting for oscillator stabilization. A timer T0 overflow will also cause the HPC16040 to resume normal operation.

HPC16040 Interrupts

Complex interrupt handling is easily accomplished by the HPC16040's vectored interrupt scheme. There are eight possible interrupt sources as shown in Table III.

TABLE III. Interrupts

Vector Address	Interrupt Source	Arbitration Ranking
$FFFF:FFFE	RESET	0
$FFFD:FFFC	Nonmaskable external on rising edge of I1 pin	1
$FFFB:FFFA	External interrupt on I2 pin	2
$FFF9:FFF8	External interrupt on I3 pin	3
$FFF7:FFF6	External interrupt on I4 pin	4
$FFF5:FFF4	Overflow on internal timers	5
$FFF3:FFF2	Internal on the UART transmit/receive complete or external on EXUI	6
$FFF1:FFF0	External interrupt on EI pin	7

Interrupt Arbitration

The HPC16040 contains arbitration logic to determine which interrupt will be serviced first if two or more interrupts occur simultaneously. The arbitration ranking is given in Table III. The interrupt on Reset has the highest rank and is serviced first.

Interrupt Processing

Interrupts are serviced after the current instruction is completed except for the RESET, which is serviced immediately.

RESET and EXUI are level-LOW-sensitive interrupts and EI is level-HIGH-sensitive. All other interrupts are edge-sensitive. NMI is positive-edge sensitive. The external interrupts on I2, I3 and I4 can be software selected to be rising or falling edge.

Interrupt Control Registers

The HPC16040 allows the various interrupt sources and conditions to be programmed. This is done through the various control registers. A brief description of the different control registers is given below.

INTERRUPT ENABLE REGISTER (ENIR)

RESET and the External Interrupt on I1 are non-maskable interrupts. The other interrupts can be individually enabled or disabled. Additionally, a Global Interrupt Enable Bit in the ENIR Register allows the Maskable interrupts to be collectively enabled or disabled. Thus, in order for a particular interrupt to be serviced, both the individual enable bit and the Global Interrupt bit (GIE) have to be set.

INTERRUPT PENDING REGISTER (IRPD)

The IRPD register contains a bit allocated for each interrupt vector. The occurrence of specified interrupt trigger conditions causes the appropriate bit to be set. There is no indication of the order in which the interrupts have been received. The bits are set independently of the fact that the interrupts may be disabled. IRPD is a Read/Write register. The bits corresponding to the maskable, external interrupts are normally cleared by the HPC16040 after servicing the interrupts.

For the interrupts from the on-board peripherals, the user has the responsibility of resetting the interrupt pending flags through software.

The NMI bit is read only and I2, I3, and I4 are designed as to only allow a zero to be written to the pending bit (writing a one has no affect). A LOAD IMMEDIATE instruction is to be the only instruction used to clear a bit or bits in the IRPD register. This allows a mask to be used, thus ensuring that the other pending bits are not affected.

INTERRUPT CONDITION REGISTER (IRCD)

Three bits of the register select the input polarity of the external interrupt on I2, I3, and I4.

Servicing the Interrupts

The Interrupt, once acknowledged, pushes the program counter (PC) onto the stack thus incrementing the stack pointer (SP) twice. The Global Interrupt Enable bit (GIE) is copied into the CGIE bit of the PSW register; it is then reset, thus disabling further interrupts. The program counter is loaded with the contents of the memory at the vector address and the processor resumes operation at this point. At the end of the interrupt service routine, the user does a RETI instruction to pop the stack and re-enable interrupts if the CGIE bit is set, or RET to just pop the stack if the CGIE bit is clear, and then returns to the main program. The GIE bit can be set in the interrupt service routine to nest interrupts if desired. *Figure 14* shows the Interrupt Enable Logic.

Reset

The RESET input initializes the processor and sets ports A, B, and P in the TRI-STATE condition. RESET is an active-low Schmitt trigger input. The processor vectors to FFFF:FFFE and resumes operation at the address contained at that memory location (which must correspond to an on board location).

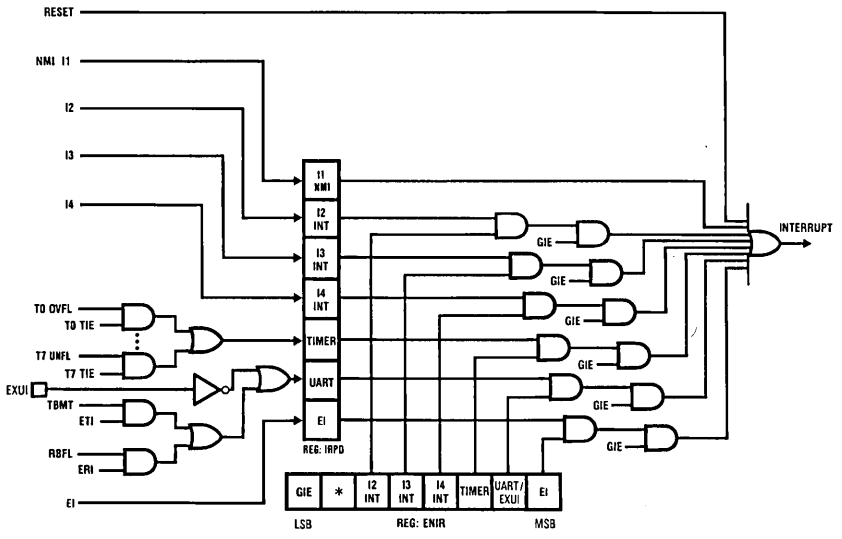


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FIGURE 14. Interrupt Enable Logic

Timer Overview

The HPC16040 contains a powerful set of flexible timers enabling the HPC16040 to perform extensive timer functions; not usually associated with microcontrollers.

The HPC16040 contains eight 16-bit timers. Each timer has an associated 16-bit register. Timer T0 is a free-running timer, counting up at a fixed CKI/16 (Clock Input/16) rate. It is used for Watch Dog logic, high speed event capture, and to exit from the IDLE mode. Consequently, it cannot be stopped or written to under software control. Timer T0 permits precise measurements by means of the capture registers I2CR, I3CR, and I4CR. A control bit in the register TMMODE configures timer T1 and its associated register R1 as capture registers I3CR and I2CR. The capture registers I2CR, I3CR, and I4CR respectively, record the value of timer T0 when specific events occur on the interrupt pins I2, I3, and I4. The control register IRCD programs the capture registers to trigger on either a rising edge or a falling edge of its respective input. The specified edge can also be programmed to generate an interrupt (see *Figure 15*).

The timers T2 and T3 have selectable clock rates. The clock input to these two timers may be selected from the following two sources: an external pin, or derived internally by dividing the clock input. Timer T2 has additional capability of being clocked by the timer T3 underflow. This allows the user to cascade timers T3 and T2 into a 32-bit timer/counter. The control register DIVBY programs the clock input to timers T2 and T3 (see *Figure 16*).

The timers T1 through T7 in conjunction with their registers form Timer-Register pairs. The registers hold the pulse duration values. All the Timer-Register pairs can be read from or written to. Each timer can be started or stopped under software control. Once enabled, the timers count down, and upon underflow, the contents of its associated register are automatically loaded into the timer.

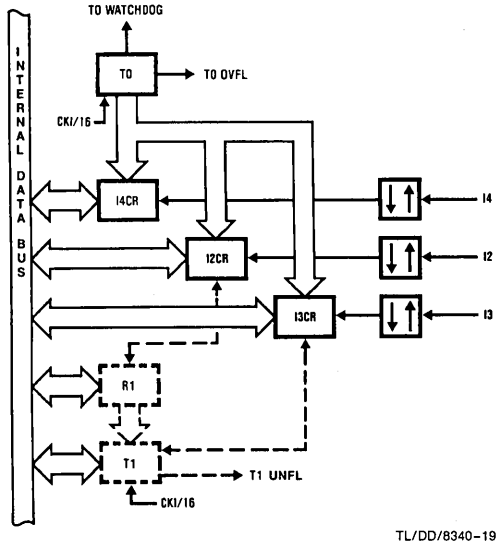

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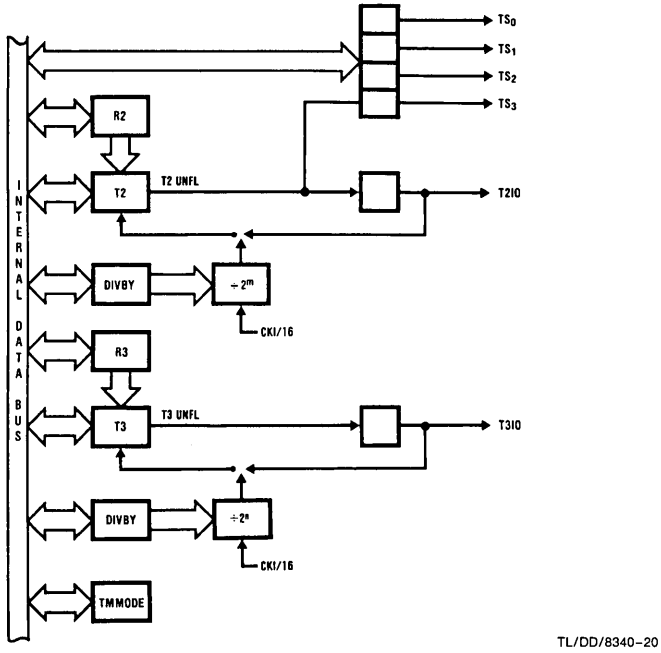
FIGURE 15. Timers T0–T1 Block

SYNCHRONOUS OUTPUTS

The flexible timer structure of the HPC16040 simplifies pulse generation and measurement. There are four synchronous timer outputs (TS0 through TS3) that work in conjunction with the timer T2. The synchronous timer outputs can be used either as regular outputs or individually programmed to toggle on timer T2 underflows (see *Figure 16*).

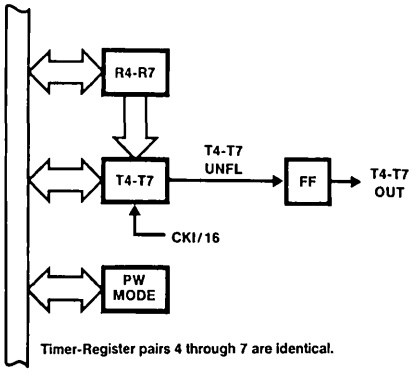
Timer/register pairs 4–7 form four identical units which can generate synchronous outputs on port P (see *Figure 17*).



TL/DD/8340-20

FIGURE 16. Timers T2–T3 Block

Timer Overview (Continued)



TL/DD/8340-21

FIGURE 17. Timers T4–T7 Block

Timer Registers

There are four control registers that program the timers. The divide by (DIVBY) register programs the clock input to timers T2 and T3. The timer mode register (TMMODE) contains control bits to start and stop timers T1 through T3. It also contains bits to latch and enable interrupts from timers T0 through T3. The control register PWMODE similarly programs the pulse width timers T4 through T7 by allowing them to be started, stopped, and to latch and enable interrupts on underflows. The PORTP register contains bits to preset the outputs and enable the synchronous timer output functions.

Timer Applications

The use of Pulse Width Timers for the generation of various waveforms is easily accomplished by the HPC16040.

Frequencies can be generated by using the timer/register pairs. A square wave is generated when the register value is a constant. The duty cycle can be controlled simply by changing the register value.

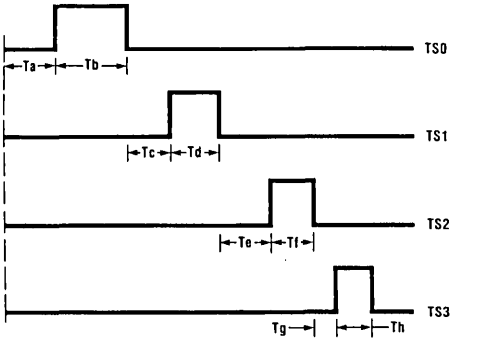
TL/DD/8340-22

FIGURE 18. Square Wave Frequency Generation

Synchronous outputs based on Timer T2 can be generated on the 4 outputs TS0–TS3. Each output can be individually programmed to toggle on T2 underflow. Register R2 contains the time delay between events. *Figure 19* is an example of synchronous pulse train generation.

Watch Dog Logic

The Watch Dog Logic monitors the operations taking place and signals upon the occurrence of any illegal activity. The illegal conditions that trigger the Watch Dog logic are potentially infinite loops and illegal addresses. Should the Watch Dog register not be written to before Timer T0 overflows



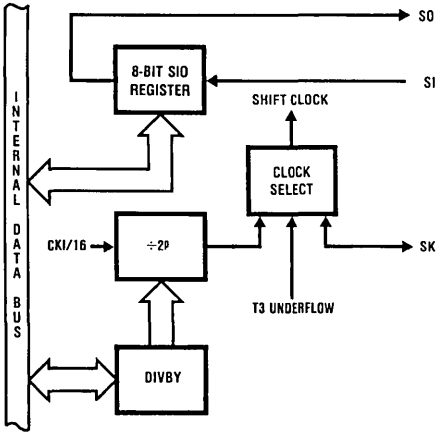
TL/DD/8340-23

FIGURE 19. Synchronous Pulse Generation

twice, or more often than once every 4096 counts, an infinite loop condition is assumed to have occurred. An illegal condition also occurs when the processor generates an off-chip address when in the Single-Chip mode. The illegal condition forces the Watch Out (WO) pin low. The WO pin is an open drain output and can be connected to the RESET or NMI inputs or to the users external logic.

MICROWIRE/PLUS

MICROWIRE/PLUS is used for synchronous serial data communications (see *Figure 20*). MICROWIRE/PLUS has an 8-bit parallel-loaded, serial shift register using SI as the input and SO as the output. SK is the clock for the serial shift register (SIO). The SK clock signal can be provided by an internal or external source. The internal clock rate is programmable by the DIVBY register. A DONE flag indicates when the data shift is completed.



TL/DD/8340-24

FIGURE 20. MICROWIRE/PLUS

The MICROWIRE/PLUS capability enables it to interface with any of National Semiconductor's MICROWIRE peripherals (i.e., A/D converters, display drivers, EEPROMs).

2

MICROWIRE/PLUS Operation

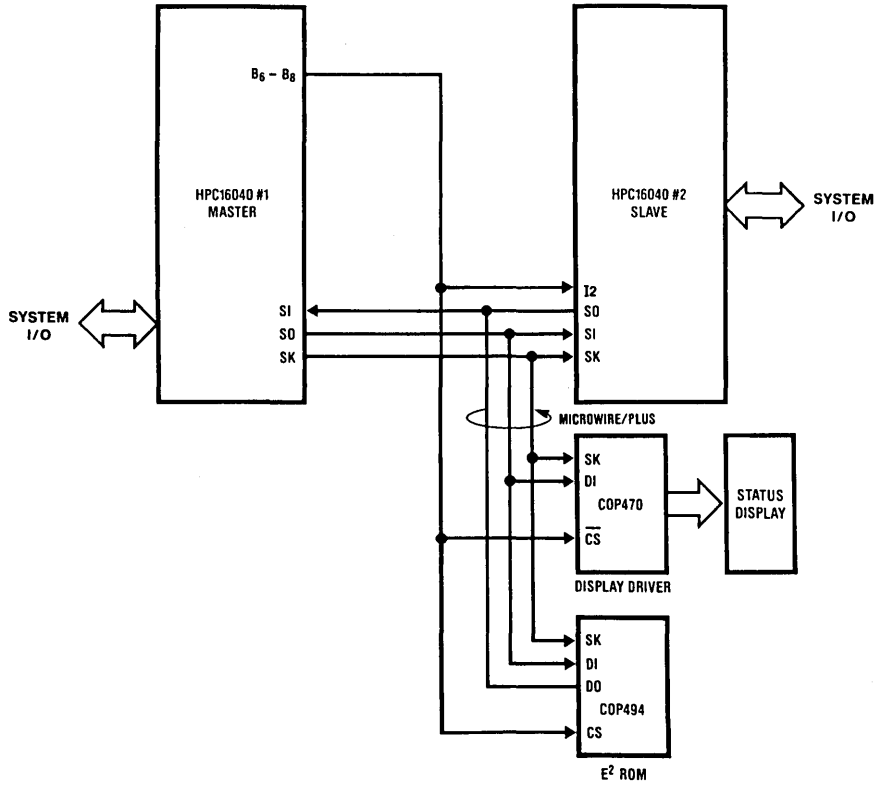
The HPC16040 can enter the MICROWIRE/PLUS mode as the master or a slave. A control bit in the IRCD register determines whether the HPC16040 is the master or slave. The shift clock is generated when the HPC16040 is configured as a master. An externally generated shift clock on the SK pin is used when the HPC16040 is configured as a slave. When the HPC16040 is a master, the DIVBY register programs the frequency of the SK clock. The DIVBY register allows the SK clock frequency to be programmed in 15 selectable steps from 64 Hz to 1 MHz with CKI at 16.0 MHz.

The contents of the SIO register may be accessed through any of the memory access instructions. Data waiting to be transmitted in the SIO register is clocked out on the falling edge of the SK clock. Serial data on the SI pin is clocked in on the rising edge of the SK clock.

MICROWIRE/PLUS Application

Figure 21 illustrates a MICROWIRE/PLUS arrangement for an automotive application. The microcontroller-based system could be used to interface to an instrument cluster and various parts of the automobile. The diagram shows two HPC16040 microcontrollers interconnected to other MICROWIRE peripherals. HPC16040 #1 is set up as the master and initiates all data transfers. HPC16040 #2 is set up as a slave answering to the master.

The master microcontroller interfaces the operator with the system and could also manage the instrument cluster in an automotive application. Information is visually presented to the operator by means of a VF display controlled by the COP470 display driver. The data to be displayed is sent serially to the COP470 over the MICROWIRE/PLUS link. Data such as accumulated mileage could be stored and retrieved from the EEPROM COP494. The slave HPC16040 could be used as a fuel injection processor and generate timing signals required to operate the fuel valves. The master processor could be used to periodically send updated values to the slave via the MICROWIRE/PLUS link. To speed up the response, chip select logic is implemented by connecting an output from the master to the external interrupt input on the slave.



TL/DD/8340–25

FIGURE 21. MICROWIRE/PLUS Application

HPC16040 UART

The HPC16040 contains a software programmable UART. The UART (see *Figure 22*) consists of a transmit shift register, a receiver shift register and five addressable registers, as follows: a transmit buffer register (TBUF), a receiver buffer register (RBUF), a UART control and status register (ENU), a UART receive control and status register (ENUR) and a UART interrupt and clock source register (ENUI). The ENU register contains flags for transmit and receive functions; this register also determines the length of the data frame (8 or 9 bits) and the value of the ninth bit in transmission. The ENUR register flags framing and data overrun errors while the UART is receiving. Other functions of the ENUR register include saving the ninth bit received in the data frame and enabling or disabling the UART's Wake-up Mode of operation. The determination of an internal or external clock source is done by the ENUI register, as well as selecting the number of stop bits and enabling or disabling transmit and receive interrupts.

The baud rate clock for the Receiver and Transmitter can be selected for either an internal or external source using two bits in the ENUI register. The internal baud rate is programmed by the DIVBY register. The baud rate may be selected from a range of 8 Hz to 64 kHz in binary steps or T3 underflow. By selecting a 9.83 MHz crystal, all standard baud rates from 75 baud to 38.4 kBaud can be generated. The external baud clock source comes from the CKX pin. The Transmitter and Receiver can be run at different rates by selecting one to operate from the internal clock and the other from an external source.

The HPC16040 UART supports two data formats. The first format for data transmission consists of one start bit, eight data bits and one or two stop bits. The second data format for transmission consists of one start bit, nine data bits, and one or two stop bits. Receiving formats differ from transmission only in that the Receiver always requires only one stop bit in a data frame.

UART Wake-up Mode

The HPC16040 UART features a Wake-up Mode of operation. This mode of operation enables the HPC16040 to be networked with other processors. Typically in such environments, the messages consist of addresses and actual data. Addresses are specified by having the ninth bit in the data frame set to 1. Data in the message is specified by having the ninth bit in the data frame reset to 0.

The UART monitors the communication stream looking for addresses. When the data word with the ninth bit set is received, the UART signals the HPC16040 with an interrupt. The processor then examines the content of the receiver buffer to decide whether it has been addressed and whether to accpet subsequent data.

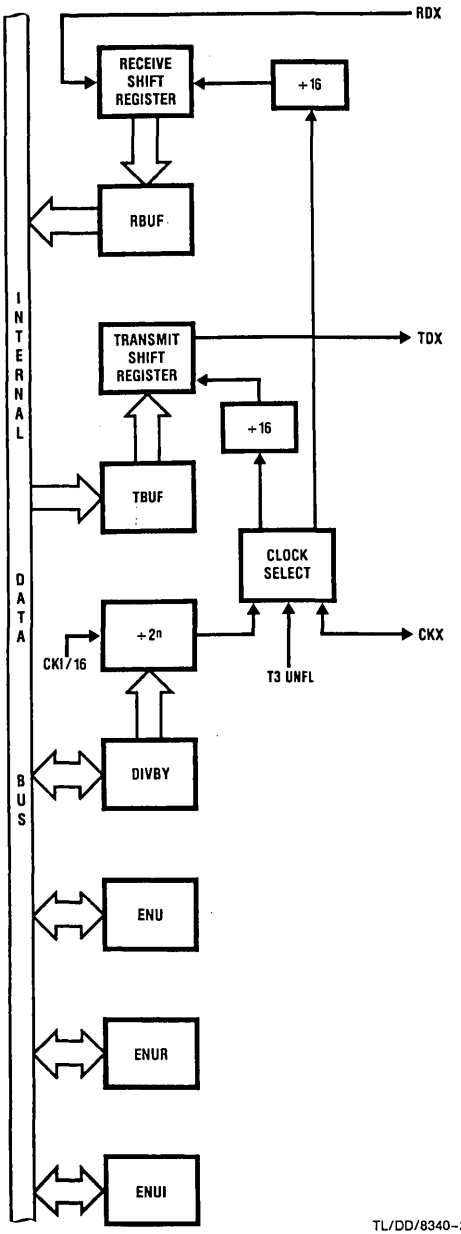


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FIGURE 22. UART Block Diagram

Universal Peripheral Interface

The Universal Peripheral Interface (UPI) allows the HPC16040 to be used as an intelligent peripheral to another processor. The UPI could thus be used to tightly link two HPC16040's and set up systems with very high data exchange rates. Another area of application could be where a HPC16040 is programmed as an intelligent peripheral to a host system such as the Series 32000 microprocessor. *FIGURE 23* illustrates how a HPC16040 could be used an an intelligent peripherial for a Series 32000-based application.

The interface consists of a Data Bus (port A), a Read Strobe ($\overline{URD}$), a Write Strobe ($\overline{UWR}$), a Read Ready Line ($\overline{RDRDY}$), a Write Ready Line ($\overline{WRRDY}$) and one Address Input (UA0). The data bus can be either eight or sixteen bits wide.

The $\overline{URD}$ and $\overline{UWR}$ inputs may be used to interrupt the HPC16040. The $\overline{RDRDY}$ and $\overline{WRRDY}$ outputs may be used to interrupt the host processor.

The UPI contains an Input Buffer (IBUF), an Output Buffer (OBUF) and a Control Register (UPIC). In the UPI mode, port A on the HPC16040 is the data bus. UPI can only be used if the HPC16040 is in the Single-Chip mode.

Shared Memory Support

Shared memory access provides a rapid technique to exchange data. It is effective when data is moved from a peripheral to memory or when data is moved between blocks of memory. A related area where shared memory access proves effective is in multiprocessing applications where two CPUs share a common memory block. The HPC16040 supports shared memory access with two pins. The pins are the RDY/$\overline{HLD}$ input pin and the $\overline{HLDA}$ output pin. The user can software select either the Hold or Ready function by the state of a control bit. The $\overline{HLDA}$ output is multiplexed onto port B.

The host uses DMA to interface with the HPC16040. The host initiates a data transfer by activating the $\overline{HLD}$ input of the HPC16040. In response, the HPC16040 places its system bus in a TRI-STATE Mode, freeing it for use by the host. The host waits for the acknowledge signal ($\overline{HLDA}$) from the HPC16040 indicating that the sytem bus is free. On receiving the acknowledge, the host can rapidly transfer data into, or out of, the shared memory by using a conventional DMA controller. Upon completion of the message transfer, the host removes the HOLD request and the HPC16040 resumes normal operations.

FIGURE 24 illustrates an application of the shared memory interface between the HPC16040 and a Series 32000 system.

Memory

The HPC16040 has been designed to offer flexibility in memory usage. A total address space of 64 kbytes can be addressed with 4096 bytes of ROM and 256 bytes of RAM available on the chip itself. The ROM may contain program instructions, constants or data. The ROM and RAM share the same address space allowing instructions to be executed out of RAM.

Program memory addressing is accomplished by the 16-bit program counter on a byte basis. Memory can be addressed directly by instructions or indirectly through the B, X and SP registers. Memory can be addressed as words or bytes. Words are always addressed on even-byte boundaries. The HPC16040 uses memory-mapped organization to support registers, I/O and on-chip peripheral functions.

The HPC16040 memory address space extends to 64 kbytes and registers and I/O are mapped as shown in Table IV.

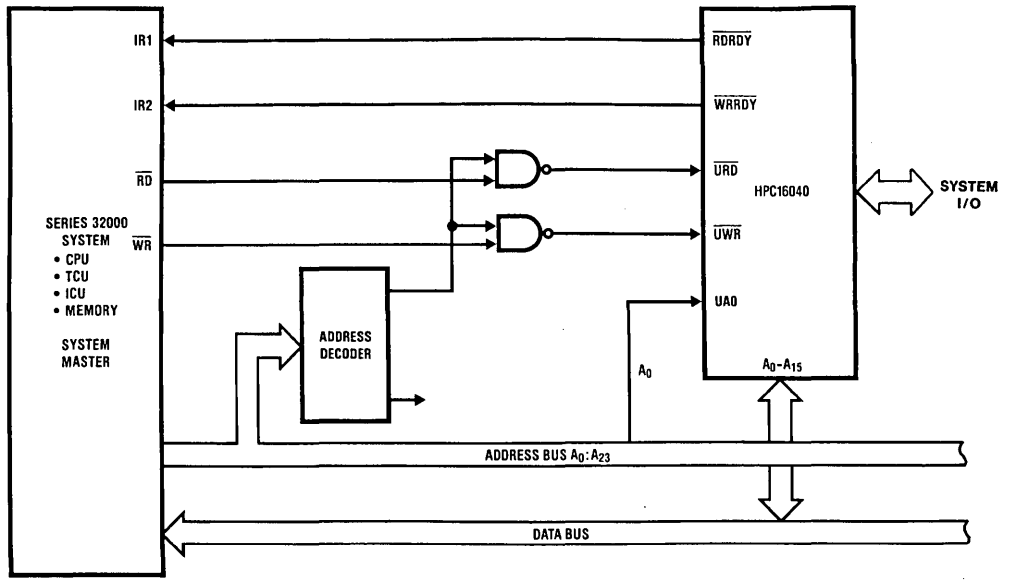

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FIGURE 23. HPC16040 as a Peripheral: (UPI Interface to Series 32000 Application)

Shared Memory Support (Continued)

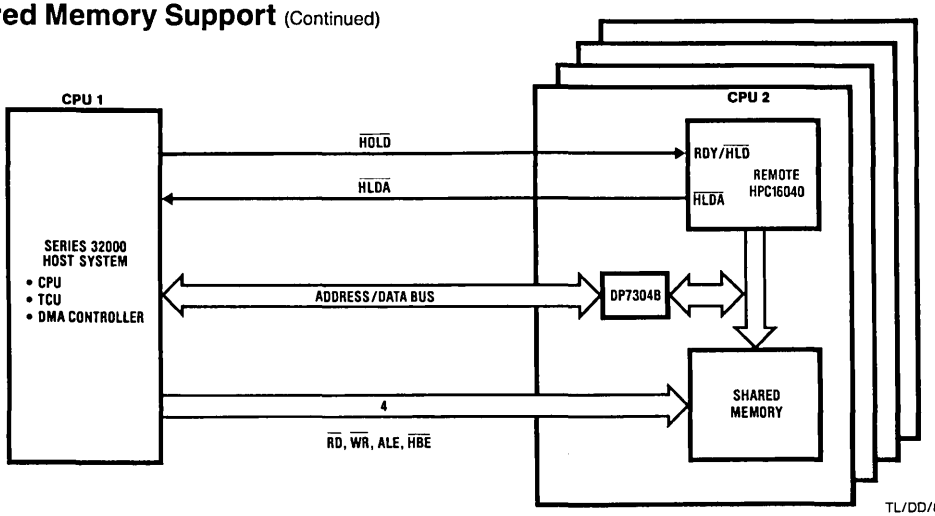

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FIGURE 24. Shared Memory Application: HPC16040 Interface to Series 32000 System

TABLE IV. Memory Map

FFFF:FFF0 FFEF:FFD0 FFCF:FFCE : : F001:F000	Interrupt Vectors JSRP Vectors On-Chip ROM	USER MEMORY
EFFF:EFFE : : 0201:0200	External Expansion Memory	
01FF:01FE : : 01C1:01C0	On-Chip RAM	
0195:0194	Watchdog Address	Watchdog Logic
0192 0191:0190 018F:018E 018D:018C 018B:018A 0189:0188 0187:0186 0185:0184 0183:0182 0181:0180	T0CON Register TMMODE Register DIVBY Register T3 Timer R3 Register T2 Timer R2 Register I2CR Register/ R1 I3CR Register/ T1 I4CR Register	Timer Block T0:T3
0153:0152 0151:0150 014F:014E 014D:014C 014B:014A 0149:0148 0147:0146 0145:0144 0143:0142 0141:0140	Port P Register PWMODE Register R7 Register T7 Timer R6 Register T6 Timer R5 Register T5 Timer R4 Register T4 Timer	Timer Block T4:T7

0128 0126 0124 0122 0120	ENUR Register TBUF Register RBUF Register ENUI Register ENU Register	UART
0104	Port D Input Register	
00F5:00F4 00F3:00F2 00F1:00F0	BFUN Register DIR B Register DIR A Register / IBUF	PORTS A & B CONTROL
00E6	UPIC Register	UPI CONTROL
00E3:00E2 00E1:00E0	Port B Port A / OBUF	PORTS A & B
00DE 00DD:00DC 00D8 00D6 00D4 00D2 00D0	Microcode ROM Dump HALT Enable Register Port I Input Register SIO Register IRCD Register IRPD Register ENIR Register	PORT CONTROL & INTERRUPT CONTROL REGISTERS
00CF:00CE 00CD:00CC 00CB:00CA 00C9:00C8 00C7:00C6 00C5:00C4 00C3:00C2 00C0	X Register B Register K Register A Register PC Register SP Register (reserved) PSW Register	HPC16040 CORE REGISTERS
00BF:00BE : : 0001:0000	On-Chip RAM	USER RAM

2

HPC16040 CPU

The HPC16040 CPU has a 16-bit ALU and six 16-bit registers

Arithmetic Logic Unit (ALU)

The ALU is 16 bits wide and can do 16-bit add, subtract and shift or logic AND, OR and exclusive OR in one timing cycle. The ALU can also output the carry bit to a 1-bit C register.

Accumulator (A) Register

The 16-bit A register is the source and destination register for most I/O, arithmetic, logic and data memory access operations.

Address (B and X) Registers

The 16-bit B and X registers can be used for indirect addressing. They can automatically count up or down to sequence through data memory.

Boundary (K) Register

The 16-bit K register is used to set limits in repetitive loops of code as register B sequences through data memory.

Stack Pointer (SP) Register

The 16-bit SP register is the pointer that addresses the stack. The SP register is incremented by two for each push or call and decremented by two for each pop or return. The stack can be placed anywhere in user memory and be as deep as the available memory permits.

Program (PC) Register

The 16-bit PC register addresses program memory.

Addressing Modes

ADDRESSING MODES—ACCUMULATOR AS DESTINATION

Register Indirect

This is the "normal" mode of addressing for the HPC16040 (instructions are single-byte). The operand is the memory addressed by the B register (or X register for some instructions).

Direct

The instruction contains an 8-bit or 16-bit address field that directly points to the memory for the operand.

Indirect

The instruction contains an 8-bit address field. The contents of the WORD addressed points to the memory for the operand.

Indexed

The instruction contains an 8-bit address field and an 8- or 16-bit displacement field. The contents of the WORD addressed is added to the displacement to get the address of the operand.

Immediate

The instruction contains an 8-bit or 16-bit immediate field that is used as the operand.

Register Indirect (Auto Increment and Decrement)

The operand is the memory addressed by the X register. This mode automatically increments or decrements the X register (by 1 for bytes and by 2 for words).

Register Indirect (Auto Increment and Decrement) with Conditional Skip

The operand is the memory addressed by the B register. This mode automatically increments or decrements the B register (by 1 for bytes and by 2 for words). The B register is then compared with the K register. A skip condition is generated if B goes past K.

ADDRESSING MODES—DIRECT MEMORY AS DESTINATION

Direct Memory to Direct Memory

The instruction contains two 8- or 16-bit address fields. One field directly points to the source operand and the other field directly points to the destination operand.

Immediate to Direct Memory

The instruction contains an 8- or 16-bit address field and an 8- or 16-bit immediate field. The immediate field is the operand and the direct field is the destination.

Double Register Indirect Using the B and X Registers

Used only with Reset, Set and IF bit instructions; a specific bit within the 64 kbyte address range is addressed using the B and X registers. The address of a byte of memory is formed by adding the contents of the B register to the most significant 13 bits of the X register. The specific bit to be modified or tested within the byte of memory is selected using the least significant 3 bits of register X.

HPC Instruction Set Description

Mnemonic	Description	Action
ARITHMETIC INSTRUCTIONS		
ADD	Add	MA + Meml → MA carry → C
ADC	Add with carry	MA + Meml + C → MA carry → C
DADC	Decimal add with carry	MA + Meml + C → MA (Decimal) carry → C
SUBC	Subtract with carry	MA − Meml + C → MA carry → C
DSUBC	Decimal subtract w/carry	MA − Meml + C → MA (Decimal) carry → C
MULT	Multiply (unsigned)	MA*Meml → MA & X, 0 → K, 0 → C
DIV	Divide (unsigned)	MA/Meml → MA, rem. → X, 0 → K, 0 → C
IFEQ	If equal	Compare MA & Meml, Do next if equal
IFGT	If greater than	Compare MA & Meml, Do next if MA > Meml
AND	Logical and	MA and Meml → MA
OR	Logical or	MA or Meml → MA
XOR	Logical exclusive-or	MA xor Meml → MA
MEMORY MODIFY INSTRUCTIONS		
INC	Increment	Mem + 1 → Mem
DECSZ	Decrement, skip if 0	Mem − 1 → Mem, Skip next if Mem = 0

HPC Instruction Set Description (Continued)

Mnemonic	Description	Action
BIT INSTRUCTIONS		
SET	Set bit	1 → Mem.bit (bit is 0 to 7 immediate)
RESET	Reset bit	0 → Mem.bit
IF	If bit	If Mem.bit is true, do next instr.
MEMORY TRANSFER INSTRUCTIONS		
LD	Load	Meml → MA
	Load, incr/decr X	Mem(X) → A, X ±1 (or 2) → X
ST	Store to Memory	A → Mem
X	Exchange	A ⟷ Mem
	Exchange, incr/decr X	A ⟷ Mem(X), X ±1 (or 2) → X
PUSH	Push Memory to Stack	W → W(SP), SP+2 → SP
POP	Pop Stack to Memory	SP−2 → SP, W(SP) → W
LDS	Load A, incr/decr B, Skip on condition	Mem(B) → A, B ±1 (or 2) → B, Skip next if B greater/less than K
XS	Exchange, incr/decr B, Skip on condition	Mem(B) ⟷ A,B±1 (or 2) → B, Skip next if B greater/less than K
REGISTER LOAD IMMEDIATE INSTRUCTIONS		
LD A	Load A immediate	imm → A
LD B	Load B immediate	imm → B
LD K	Load K immediate	imm → K
LD X	Load X immediate	imm → X
LD BK	Load B and K immediate	imm → B,imm' → K
ACCUMULATOR AND C INSTRUCTIONS		
CLR A	Clear A	0 → A
INC A	Increment A	A + 1 → A
DEC A	Decrement A	A − 1 → A
COMP A	Complement A	1's complement of A → A
SWAP A	Swap nibbles of A	A15:12 ← A11:8 ← A7:4 ⟷ A3:0
RRC A	Rotate A right thru C	C → A15 → ... → A0 → C
RLC A	Rotate A left thru C	C ← A15 ← ... ← A0 ← C
SHR A	Shift A right	0 → A15 → ... → A0 → C
SHL A	Shift A left	C ← A15 ← ... ← A0 ← 0
SET C	Set C	1 → C
RESET C	Reset C	0 → C
IF C	IF C	Do next if C = 1
IFN C	IF not C	Do next if C = 0
TRANSFER OF CONTROL INSTRUCTIONS		
JSRP	Jump subroutine from table	PC → W(SP),SP+2 → SP W(table#) → PC
JSR	Jump subroutine relative	PC → W(SP),SP+2 → SP,PC+ # → PC (#is +1025 to −1023)
JSRL	Jump subroutine long	PC → W(SP),SP+2 → SP,PC+ # → PC
JP	Jump relative short	PC+ # → PC(# is +32 to −31)
JMP	Jump relative	PC+ # → PC(#is +257 to −255)
JMPL	Jump relative long	PC+ # → PC
JID	Jump indirect at PC + A	PC+A+1 → PC
JIDW		then Mem(PC)+PC → PC
NOP	No Operation	PC + 1 → PC
RET	Return	SP−2 → SP,W(SP) → PC
RETS	Return then skip next	SP−2 → SP,W(SP) → PC, & skip
RETI	Return from interrupt	SP−2 → SP,W(SP) → PC, interrupt re-enabled

Note: W is 16-bit word of memory
MA is Accumulator A or direct memory (8 or 16-bit)
Mem is 8-bit byte or 16-bit word of memory
Meml is 8- or 16-bit memory or 8 or 16-bit immediate data
imm is 8-bit or 16-bit immediate data

Memory Usage

Number Of Bytes For Each Instruction (number in parenthesis is 16-Bit field)

	Using Accumulator A						To Direct Memory			
	Reg Indir. (B)	Reg Indir. (X)	Direct	Indir	Index	Immed.	Direct *	Direct **	Immed. *	Immed. **
LD	1	1	2(4)	3	4(5)	2(3)	3(5)	5(6)	3(4)	5(6)
X	1	1	2(4)	3	4(5)	—	—	—	—	—
ST	1	1	2(4)	3	4(5)	—	—	—	—	—
ADC	1	2	3(4)	3	4(5)	4(5)	4(5)	5(6)	4(5)	5(6)
SBC	1	2	3(4)	3	4(5)	4(5)	4(5)	5(6)	4(5)	5(6)
DADC	1	2	3(4)	3	4(5)	4(5)	4(5)	5(6)	4(5)	5(6)
DSBC	1	2	3(4)	3	4(5)	4(5)	4(5)	5(6)	4(5)	5(6)
ADD	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
MULT	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
DIV	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
IFEQ	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
IFGT	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
AND	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
OR	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
XOR	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)

*8-bit direct address
**16-bit direct address

Instructions that modify memory directly

	(B)	(X)	Direct	Indir	Index	B&X
SET	1	2	3(4)	3	4(5)	1
RESET	1	2	3(4)	3	4(5)	1
IF	1	2	3(4)	3	4(5)	1
DECSZ	3	2	2(4)	3	4(5)	
INC	3	2	2(4)	3	4(5)	

Immediate Load Instructions

	Immed.
LD B,*	2(3)
LD X,*	2(3)
LD K,*	2(3)
LD BK,*,*	3(5)

Register Indirect Instructions with Auto Increment and Decrement

Register B With Skip		
	(B+)	(B−)
LDS A,*	1	1
XS A,*	1	1

Register X		
	(X+)	(X−)
LD A,*	1	1
X A,*	1	1

Instructions Using A and C

CLR	A	1
INC	A	1
DEC	A	1
COMP	A	1
SWAP	A	1
RRC	A	1
RLC	A	1
SHR	A	1
SHL	A	1
SET	C	1
RESET	C	1
IF	C	1
IFN	C	1

Transfer of Control Instructions

JSRP	1
JSR	2
JSRL	3
JP	1
JMP	2
JMPL	3
JID	1
JIDW	1
NOP	1
RET	1
RETS	1
RETI	1

Stack Reference Instructions

	Direct
PUSH	2
POP	2

Code Efficiency

One of the most important criteria of a single chip microcontroller is code efficiency. The more efficient the code, the more features that can be put on a chip. The memory size on a chip is fixed so if code is not efficient, features may have to be sacrificed or the programmer may have to buy a larger, more expensive version of the chip.

The HPC16040 has been designed to be extremely code-efficient. The HPC16040 looks very good in all the standard coding benchmarks; however, it is not realistic to rely only on benchmarks. Many large jobs have been programmed onto the HPC16040, and the code savings over other popular microcontrollers has been considerable—often the jobs take less than one-half the memory!

Reasons for this saving of code include the following:

SINGLE BYTE INSTRUCTIONS

The majority of instructions on the HPC16040 are single-byte. There are two especially code-saving instructions:

JP is a 1-byte jump. True, it can only jump within a range of plus or minus 32, but many loops and decisions are often within a small range of program memory. Most other micros need 2-byte instructions for any short jumps.

JSRP is a 1-byte call subroutine. The user makes a table of his 16 most frequently called subroutines and these calls will only take one byte. Most other micros require two and even three bytes to call a subroutine. The user does not have to decide which subroutine addresses to put into his table; the assembler can give him this information.

EFFICIENT SUBROUTINE CALLS

The 2-byte JSR instructions can call any subroutine within plus or minus 1k of program memory.

MULTIFUNCTION INSTRUCTIONS FOR DATA MOVEMENT AND PROGRAM LOOPING

The HPC16040 has single-byte instructions that perform multiple tasks. For example, the XS instruction will do the following:

1. Exchange A and memory pointed to by the B register
2. Increment the B register
3. Compare the B register versus the K register
4. Generate a conditional skip if B is greater than K

The value of this multipurpose instruction becomes evident when looping through sequential areas of memory and exiting when the loop is finished.

BIT MANIPULATION INSTRUCTIONS

Any bit of memory, I/O or registers can be set, reset or tested by the single byte bit instructions. The bits can be addressed directly or indirectly. Since all registers and I/O are mapped into the memory, it is very easy to manipulate specific bits to do efficient control.

The one exception to the above is with the IRPD register. A LOAD IMMEDIATE instruction is to be the only instruction used to clear a bit or bits in this register (see Interrupt Pending Register section).

DECIMAL ADD AND SUBTRACT

This instruction is needed to interface with the decimal user world.

It can handle both 16-bit words and 8-bit bytes.

The 16-bit capability saves code since many variables can be stored as one piece of data and the programmer does not have to break his data into two bytes. Many applications store most data in 4-digit variables. The HPC16040 supplies 8-bit byte capability for 2-digit variables and literal variables.

MULTIPLY AND DIVIDE INSTRUCTIONS

The HPC16040 has 16-bit multiply, 16-bit by 16-bit divide, and 32-bit by 16-bit divide instructions. This saves both code and time. Multiply and divide can use immediate data or data from memory. The ability to multiply and divide by immediate data saves code since this function is often needed for scaling, base conversion, computing indexes of arrays, etc.

Development Support

The MOLE (Microcontroller On-Line Emulator) is a low cost development system and emulator for all microcontroller products. These include COPs, TMP, 8050U and the HPC Family of Products. The MOLE consists of a BRAIN Board, Personality Board and optional host software.

The purpose of a MOLE is to provide the user with a tool to write and assemble code, emulate code for the target microcontroller and assist in both the software & hardware debugging of the system.

It is a self-contained computer with its own firmware which provides for all system operation, emulation control, communication, PROM programming and diagnostic operations.

It contains three serial ports because multiple ports are usually needed to optionally connect to a terminal, a host system, a printer or modem, or to connect to other MOLEs in a multi-MOLE environment.

MOLE can be used in either a stand alone mode or in conjunction with selected host systems, i.e., those using CP/M or PC-DOS. Communicating via RS-232 port.

Dial-A-Helper is a service provided by the MOLE applications group. If a user is having difficulty in getting a MOLE to operate in a particular mode or it is acting peculiar, he can contact us via his system and a modem. He can leave messages on our electronic bulletin board which we will respond to, or he can arrange for us to actually take control of his system via modem for debugging purposes.

The applications group can then cause his system to execute various commands and try to resolve the customer's problem by actually getting the customer's system to respond. 99% of the time the problem is resolved. This allows us to respond in minutes instead of days when applications help is needed.

The system can also be used to download available applications software.

Part Selection

The HPC family includes devices with many different options and configurations to meet various application needs. The number HPC16040 has been generically used throughout this datasheet to represent the whole family of parts. The following chart explains how to order various options available when ordering HPC family members.

Note: All options may not currently be available.

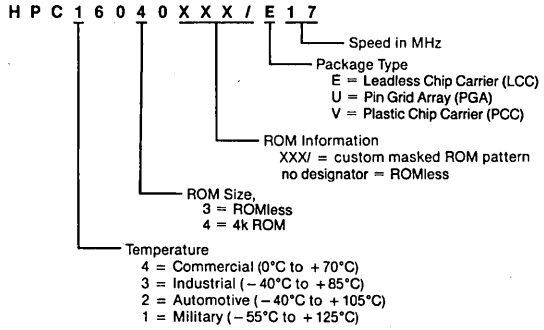

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FIGURE 8. HPC Family Part Numbering Scheme

Examples

HPC46030E17 — ROMless, Commercial temp. (0°C to 70°C), LCC

HPC16040XXX/U17 — 4k masked ROM, Military temp. (−55°C to +125°C), PGA

HPC26040XXX/V17 — 4k masked ROM, Automotive temp. (−40°C to +105°C), PCC

National Semiconductor Corporation

PRELIMINARY

HPC16400/HPC36400/HPC46400 High-Performance Microcontrollers with HDLC Controller

General Description

The HPC16400 is a member of the HPC™ family of High Performance microControllers. Each member of the family has the same identical core CPU with a unique memory and I/O configuration to suit specific applications. Each part is fabricated in National's advanced microCMOS technology. This process combined with an advanced architecture provides fast, flexible I/O control, efficient data manipulation, and high speed computation.

The HPC16400 has 4 functional blocks to support a wide range of communication application-2 HDLC channels, 4 channel DMA controller to facilitate data flow for the HDLC channels, programmable serial interface and UART.

The serial interface decoder allows the 2 HDLC channels to be used with devices using interchip serial link for point-to-point & multipoint data exchanges. The decoder generates enable signals for the HDLC channels allowing multiplexed D and B channel data to be accessed.

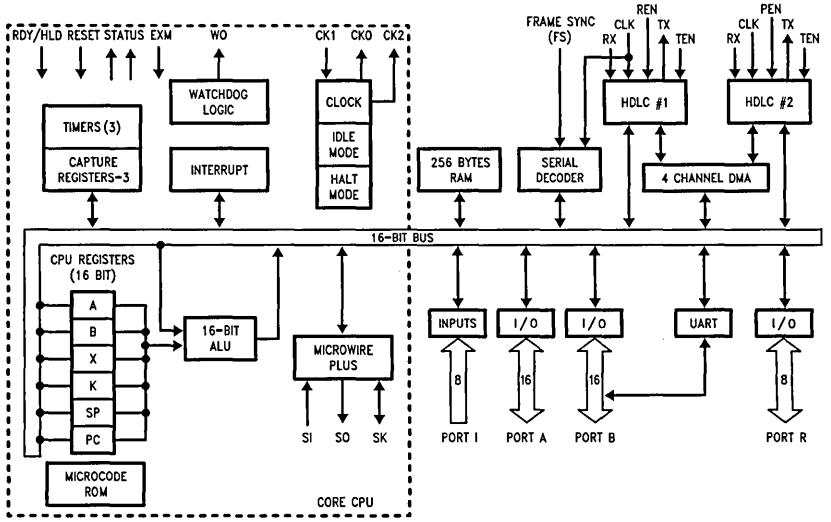
The HDLC channels manage the link by providing sequencing using the HDLC framing along with error control and retransmission based upon a cyclic redundancy check (CRC). Multiple frame addressing, and both bit and byte modes of operation are supported.

The HPC16400 is available in 68-pin PCC, LCC and PGA packages.

Features

- HPC family—core features:
  - — 16-bit data bus, ALU, and registers
  - — 64 kbytes of external memory addressing
  - — FAST!—17.0 MHz system clock
  - — High code efficiency
  - — 16 x 16 multiply and 32 x 16 divide
  - — Eight vectored interrupt sources
  - — Four 16-bit timer/counters with WATCHDOG logic
  - — MICROWIRE/PLUS serial I/O interface
  - — CMOS—low power with two power save modes
- Two full duplex HDLC channels
  - — Optimized or X.25 and LAPD applications
  - — Programmable frame address recognition
  - — Up to 4.1 Mbps aggregate serial data rate
  - — Built in diagnostics
- Programmable interchip serial data decoder
- Four channel DMA controller
- UART—full duplex, programmable baud rate
- 544 kbytes of extended addressing
- Easy interface to National's 'U' and 'S' transceiver—TP3400, TP3410 and TP3420
- Wide voltage supply range: 3 to 5.5V
- Industrial (−40°C to +85°C) and military (−55°C to +125°C) temperature ranges

Block Diagram



TL/DD/8802-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Allowable Source or Sink Current	100 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
V_{CC} with Respect to GND	−0.5V to 7.0V
All Other Pins	(V_{CC} + 0.5)V to (GND − 0.5)V

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

V_{CC} = 5.0V ±10% unless otherwise specified, T_A = 0°C to +70°C for HPC46040, −40°C to +85°C for HPC36040, −40°C to +105°C for HPC26040, −55°C to +125°C for HPC16400

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC_1}	Supply Current	V_{CC} = 5.0V, f_{in} = 17.0 MHz*		20		mA
		V_{CC} = 5.0V, f_{in} = 2.0 MHz		2.4		mA
I_{CC_2}	IDLE Mode Current	V_{CC} = 5.0V, f_{in} = 17.0 MHz, T_A = 25°C*		2		mA
		V_{CC} = 5.0V, f_{in} = 2.0 MHz, T_A = 25°C		0.2		mA
I_{CC_3}	HALT Mode Current	V_{CC} = 5.0V, f_{in} = 0 kHz, T_A = 25°C*		25		μA
		V_{CC} = 2.5V, f_{in} = 0 kHz, T_A = 25°C		10		μA
INPUT VOLTAGE LEVELS RESET, NMI, CKI AND WO (SCHMITT TRIGGERED)						
V_{IH_1}	Logic High			0.9 V_{CC}		V
V_{IL_1}	Logic Low			0.1 V_{CC}		V
ALL OTHER INPUTS						
V_{IH_2}	Logic High			0.7 V_{CC}		V
V_{IL_2}	Logic Low			0.2 V_{CC}		V
I_{LI}	Input Leakage Current			±1		μA
C_I	Input Capacitance			10		pF
C_{IO}	I/O Capacitance			20		pF
OUTPUT VOLTAGE LEVELS CMOS OPERATION						
V_{OH_1}	Logic High	I_{OH} = −10 μA		V_{CC} − 0.2		V
V_{OL_1}	Logic Low	I_{OH} = 10 μA		0.2		V
V_{OH_2}	Port A/B Drive (A_0–A_{15}, B_{10}, B_{11}, B_{12}, B_{15})	I_{OH} = −7 mA, V_{CC} = 5.0V		2.4		V
V_{OL_2}		I_{OL} = 3 mA		0.4		V
V_{OH_3}	Other Port Pin Drive (B_0–B_9, B_{13}, B_{14}, P_0–P_3)	I_{OH} = −1.6 mA, V_{CC} = 5.0V		2.4		V
V_{OL_3}		I_{OL} = 0.5 mA		0.4		V
V_{OL_4}	WO (Watchdog Out) Drive	I_{OL} = 0.5 mA, V_{CC} = 5.0V		0.4		V
V_{OH_6}	CK2 Drive	I_{OH} = −12 mA, V_{CC} = 5.0V		2.4		V
V_{OL_6}		I_{OL} = 3.5 mA		0.4		V
V_{OH_7}	ST1 and ST2 Drive	I_{OH} = −6 mA, V_{CC} = 5.0V		2.4		V
V_{OL_7}		I_{OL} = 1.6 mA		0.4		V
V_{RAM}	RAM Keep-Alive Voltage			2.5		V
I_{OZ}	TRI-STATE Leakage Current			±5		μA

***Note:** I_{CC_1}, I_{CC_2}, I_{CC_3} measured with no external drive (I_{OH} and I_{OL} = 0, I_{IH} and I_{IL} = 0).

AC Electrical Characteristics

V_{CC} = 5.0V ±10%, f_C = 16.78 MHz, T_A = 0°C to +70°C for HPC46040, −40°C to +85°C for HPC36040, −40°C to +105°C for HPC26040, −55°C to +125°C for HPC16400

Symbol	Parameter	Min	Typ	Max	Units
f_C = CKI freq.	Operating Frequency		16.78	17.0	MHz
$t_{C1} = 1/f_C$	Clock Period		60		ns
$t_C = 2/f_C$	Timing Cycle		120		ns
$t_{LL} = 1/2\ t_C$	ALE Pulse Width		60		ns
$t_{ST} = 1/4\ t_C$	Address Valid to ALE Trailing Edge		30		ns
$t_{WAIT} = t_C = WS$	Wait State Period		120		ns
$f_{XIN} = 1/19\ t_{C1}$	External Timer Input Frequency		877		kHz
$t_{XIN} = 3\ t_{C1}$	Pulse Width for Timer Inputs		180		ns
$f_{XOUT} = 1/16\ t_{C1}$	Timer Output Frequency		1.04		MHz
$f_{MW} = 1/19\ t_{C1}$	External MICROWIRE/PLUS Clock Input Frequency		877		kHz
$f_U = 1/19\ t_{C1}$	External UART Clock Input Frequency		877		kHz

Read Cycle Timing

f_C = 16.78 MHz with One Wait State

Symbol	Parameter	Min	Typ	Max	Units
$t_{ARR} = 1/4\ t_C + 5$	ALE Trailing Edge to $\overline{RD}$ Falling Edge		35		ns
$t_{RW} = 1/2\ t_C + WS$	$\overline{RD}$ Pulse Width		180		ns
t_{DR}	Data Valid before Trailing Edge of $\overline{RD}$		15		ns
$t_{ACC} = t_C + WS - 55$	Address Valid to Input Data Valid		185		ns
$t_{RD} = 1/2\ t_C + WS - 65$	$\overline{RD}$ Falling Edge to Data in Valid		115		ns
$t_{RDA} = WS = t_C$	$\overline{RD}$ Falling Edge to Address Valid		120		ns
$t_{VPR} = 1/4\ t_C + 5$	Address Valid from ALE Trailing Edge Prior to $\overline{RD}$		35		ns
$t_{HZ} = 3/4\ t_C - 10$	End of $\overline{RD}$ to Input Data Float		80		ns

Write Cycle Timing

f_C = 16.78 MHz with One Wait State

Symbol	Parameter	Min	Typ	Max	Units
$t_{ARW} = 1/2\ t_C$	ALE Trailing Edge to $\overline{WR}$ Falling Edge		60		ns
$t_{WW} = 3/4\ t_C + WS + 5$	$\overline{WR}$ Pulse Width		215		ns
t_{HW}	Data Hold after Trailing Edge of $\overline{WR}$		20		ns
$t_V = 1/2\ t_C + WS + 5$	Data Valid before Trailing Edge of $\overline{WR}$		185		ns
$t_{VPW} = 1/4\ t_C + 25$	Address Valid from Trailing Edge Prior to $\overline{WR}$		55		ns

Ready/Hold Timing f_C = 16.78 MHz with One Wait State

Symbol	Parameter	Min	Typ	Max	Units
$t_{DAR} = 1/4\ t_C + WS - 50$	Falling Edge of ALE to Falling Edge of $\overline{RDY}$		100		ns
$t_{RWP} = t_C$	$\overline{RDY}$ Pulse Width		120		ns
$t_{SALE} = 1/4\ t_C + 40$	Falling Edge of $\overline{HLD}$ to Rising Edge of ALE		70		ns
$t_{HWP} = t_C + 10$	$\overline{HLD}$ Pulse Width		130		ns
t_{HAD}	Rising Edge on $\overline{HLD}$ to Rising Edge on $\overline{HLDA}$		120		ns
$t_{HAE} = t_C + 100$	Falling Edge on $\overline{HLD}$ to Falling Edge on $\overline{HLDA}$		220	*	ns
$t_{BF} = t_C + 30$	Bus Float before Falling Edge on $\overline{HLDA}$		150		ns
$t_{BE} = 2\ t_C + 50$	Bus Enable from Rising Edge of $\overline{HLD}$		290		ns

*Note: t_{HAE} may be as long as ($3t_C$ + 4ws + $72t_C$ + 90) depending on which instruction is being executed, the addressing mode and number of wait states.

Status Timing f_C = 16.78 MHz

Symbol	Parameter	Min	Typ	Max	Units
$t_{SRS2} = 40 - (1/4\ t_C + 25)$	Setup Time for ST2 on Rising Edge of ALE		−15		ns
$t_{HRS2} = 3/4\ t_C - 15$	Hold Time for ST2 on Rising Edge of ALE		75		ns
$t_{SFS2} = 40 - (1/4\ t_C + 25)$	Setup Time for ST2 on Falling Edge of ALE		−15		ns
$t_{HFS2} = 3/4\ t_C - 15$	Hold Time for ST2 on Falling Edge of ALE		75		ns
t_{SFS1}	Setup Time for ST1 on Falling Edge of $\overline{RD}$		20		ns
$t_{HRS1} = 1/2\ t_C - 15$	Hold Time for ST1 on Rising Edge of $\overline{RD}$		45		ns

Timing Waveforms

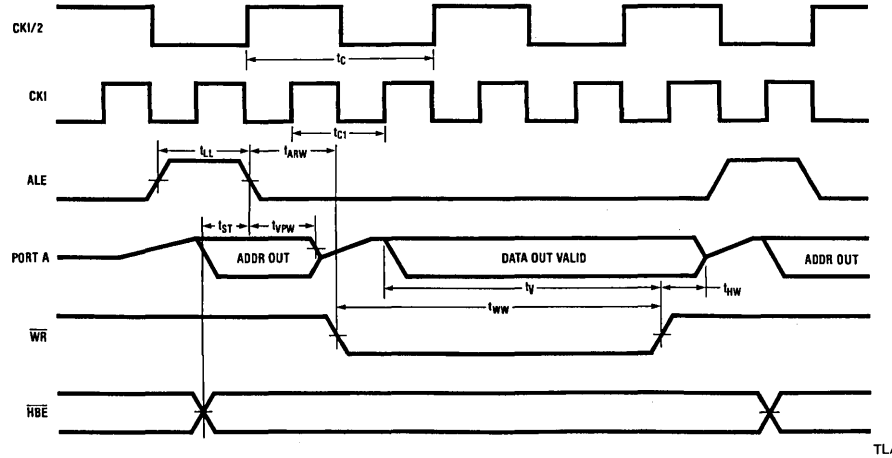


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FIGURE 1. Write Cycle

Timing Waveforms (Continued)

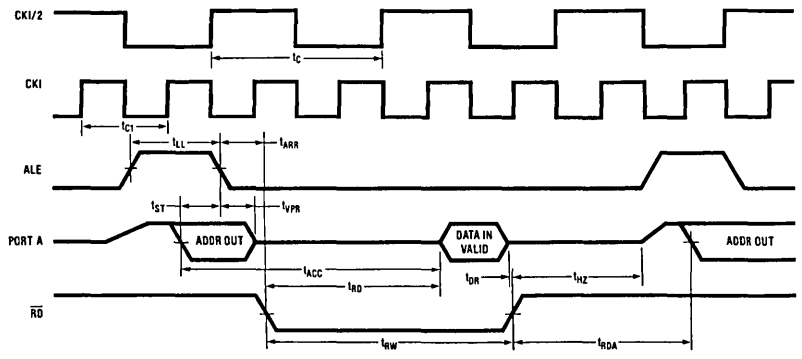

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FIGURE 2. Read Cycle

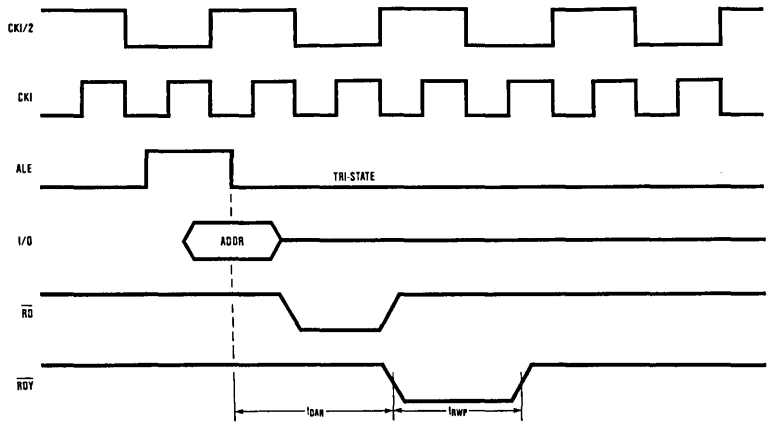

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FIGURE 3. Ready Mode Timing

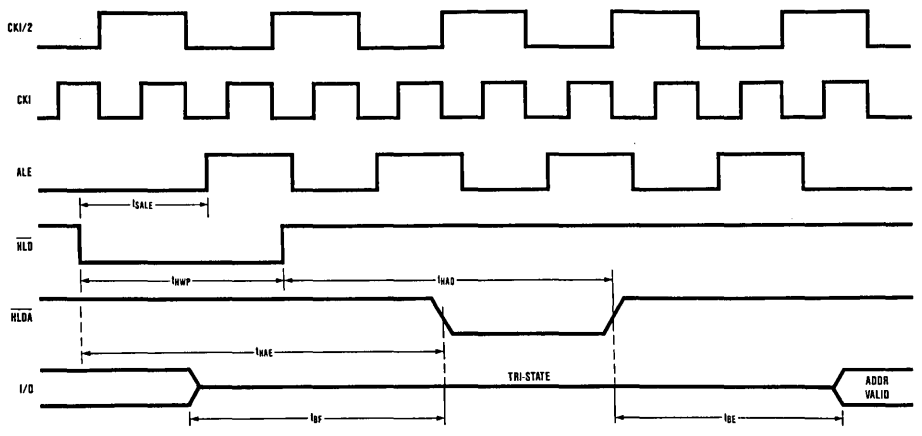

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FIGURE 4. Hold Mode Timing

2

Timing Waveforms (Continued)

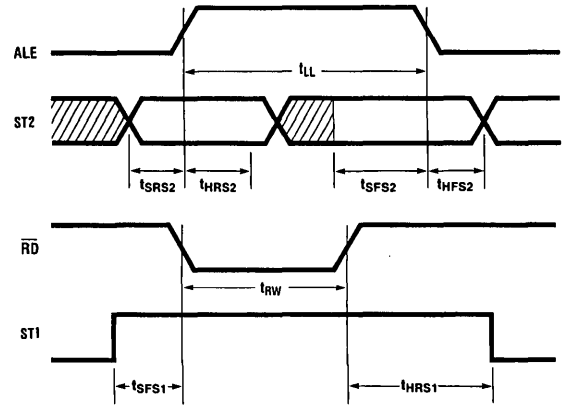


FIGURE 5. Status Timing

Pin Descriptions†

I/O PORTS

Port A is a 16-bit multiplexed address/data bus used for accessing external program and data memory. Four associated bus control signals are available on port B. The Address Latch Enable (ALE) signal is used to provide timing to demultiplex the bus. Reading from and writing to external memory are signalled by RD* and WR* respectively. External memory can be addressed as either bytes or words with the decoding controlled by two lines, Bus High Byte enable (HBE*) and Address/Data Line 0 (A0).

Port B is a 16-bit port, with 12 bits of bidirectional I/O similar in structure to port A. Pins B10, B11, B12 and B15 are the control bus signals for the address/data bus. Port B may also be configured via a function register BFUN to individually allow each bidirectional I/O pin to have an alternate function.

B0:	TDX	UART Data Output
B1:		
B2:	CKX	UART Clock (Input or Output)
B3:	T2IO	Timer2 I/O Pin
B4:	T3IO	Timer3 I/O Pin
B5:	SO	MICROWIRE/PLUS Output
B6:	SK	MICROWIRE/PLUS Clock (Input or Output)
B7:	HLDA*	Hold Acknowledge Output
B8:	TS0	Timer Synchronous Output
B9:	TS1	Timer Synchronous Output
B10:	ALE	Address Latch Enable Output for Address/Data Bus
B11:	WR*	Address/Data Bus Write Output
B12:	HBE*	High Byte Enable Output for Address/Data Bus
B13:	TS2	Timer Synchronous Output
B14:	TS3	Timer Synchronous Output
B15:	RD*	Address/Data Bus Read Output

When operating in the extended memory addressing mode, four bits of port B can are used as follows—

B8:	BS0	Memory bank switch output 0 (LSB)
B9:	BS1	Memory bank switch output 1
B13:	BS2	Memory bank switch output 2
B14:	BS3	Memory bank switch output 3 (MSB)

Port I is an 8-bit input port that can be read as general purpose inputs and can also be used for the following functions:

I0:		
I1:	NMI	Nonmaskable Interrupt Input
I2:	INT2	Maskable Interrupt/Input Capture
I3:	INT3	Maskable Interrupt/Input Capture
I5:	SI	MICROWIRE/PLUS Data Input
I6:	RDX	UART Data Input
I7:	FS	IDL Frame Sync Input Signal

Port D is an 8-bit input port that is used for the following functions:

D0:	RX1	HDLC # 1 Receive Data Input
D1:	CLK1	HDLC # 1 Clock Input
D2:	REN1	HDLC # 1 Receiver Enable Input
D3:	TEN1	HDLC # 1 Transmit Enable Input
D4:	RX2	HDLC # 2 Receive Data Input
D5:	CLK2	HDLC # 2 Clock Input
D6:	REN2	HDLC # 2 Receiver Enable Input
D7:	TEN2	HDLC # 2 Transmit Enable Input

Port R is an 8-bit bidirectional I/O port available for general purpose I/O operation. Additional functions are present as indicated.

R0:	TX1	HDLC #1 Transmit Output
R1:	TX2	HDLC #2 Transmit Output
R2:		
R3:		
R4:		
R5:		
R6:		
R7:		

†The formation of the various functions into specified ports has changed. Please contact factory for updated port configurations.

Pin Descriptions (Continued)

POWER SUPPLIES

V_{CC} Positive Power Supply (two pins)

GND Ground for On-Chip Logic

DGND Ground for Output Buffers

CLOCK PINS

CKI The System Clock Input

CKO The System Clock Output (Inversion of CKI)

Pins CKI and CKO are usually connected across an external crystal.

CK2 Clock Output (CKI divided by 2)

OTHER PINS

WO This is an active low open drain output which signals an illegal situation has been detected by the Watch Dog logic.

ST1 Bus Cycle Status Output indicates first opcode fetch.

ST2 Bus Cycle Status Output indicates machine states (skip and interrupt).

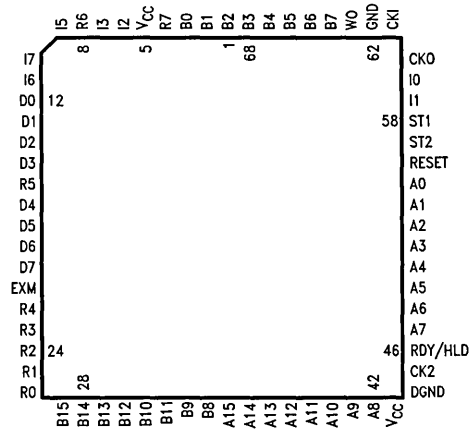
RESET Active low input that forces the chip to restart and sets the ports in a TRI-STATE mode.

RDY/HLD Has two uses, selected by a software bit. This pin is either a READY input to extend the bus cycle for slower memories or a HOLD-REQUEST input to put the bus in a high impedance state for external DMA purposes.

EXM External memory enable which must be tied high for normal operation.

Connection Diagram *

Plastic and Leadless Chip Carriers



Order Number HPC16400E or V
See NS Package Number
E68B or V68A

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Top View

*The Pin Configuration has changed. Please contact factory for updated pin placement information.

Wait States

The HPC16400 provides four software selectable Wait States that allow access to slower memories. The Wait States are selected by the state of two bits in the PSW register. Additionally, the RDY input may be used to extend the instruction cycle, allowing the user to interface with slow memories and peripherals.

Power Save Modes

Two power saving modes are available on the HPC16400: HALT and IDLE. In the HALT mode, all processor activities are stopped. In the IDLE mode, the on-board oscillator and timer T0 are active but all other processor activities are stopped. In either mode, all on-board RAM, registers and I/O are unaffected.

HALT MODE

The HPC16400 is placed in the HALT mode under software control by setting bits in the PSW. All processor activities, including the clock and timers, are stopped. In the HALT mode, power requirements for the HPC16400 are minimal and the applied voltage (V_{CC}) may be decreased without altering the state of the machine. There are two ways of exiting the HALT mode: via the RESET or the NMI. The RESET input reinitializes the processor. Use of the NMI input will generate a vectored interrupt and resume operation from that point with no initialization. The HALT mode can be enabled or disabled by means of a control register HALT enable. To prevent accidental use of the HALT mode the HALT enable register can be modified only once.

IDLE MODE

The HPC16400 is placed in the IDLE mode through the PSW. In this mode, all processor activity, except the on-board oscillator and Timer T0, is stopped. The HPC16400 resumes normal operation upon timer T0 overflow. As with the HALT mode, the processor is returned to full operation by the RESET or NMI inputs, but without waiting for oscillator stabilization.

HPC16400 Interrupts

Complex interrupt handling is easily accomplished by the HPC16400's vectored interrupt scheme. There are eight possible interrupt sources as shown in Table I.

TABLE I. Interrupts

Vector/ Address	Interrupt Source	Arbitration Ranking
FFFF|FFFE	Reset	0
FFFD|FFFC	Nonmaskable Ext (NMI)	1
FFFB|FFFA	External on I2	2
FFF9|FFF8	External on I3	3
FFF7|FFF6	HDLC/DMA Error	4
FFF5|FFF4	Overflow on Timers	5
FFF3|FFF2	Internal on UART	6
FFF1|FFF0	End of Message (EOM)	7

The 16400 contains arbitration logic to determine which interrupt will be serviced first if two or more interrupts occur simultaneously. Interrupts are serviced after the current instruction is completed except for the RESET which is serviced immediately.

The NMI interrupt will immediately stop DMA activity-byte transfers in progress will finish thereby allowing an orderly transition to the interrupt service vector (see DMA description). The HDLC channels continue to operate, and the user must service data errors that might have occurred during the NMI service routine.

Interrupt Processing

Interrupts are serviced after the current instruction is completed except for the RESET, which is serviced immediately.

RESET is a level-sensitive interrupt. All other interrupts are edge-sensitive. NMI is positive-edge sensitive. The external interrupts on I2, I3 can be software selected to be rising or falling edge.

Interrupt Control Registers

The HPC16400 allows the various interrupt sources and conditions to be programmed. This is done through the various control registers. A brief description of the different control registers is given below.

INTERRUPT ENABLE REGISTER (ENIR)

RESET and the External Interrupt on I1 are non-maskable interrupts. The other interrupts can be individually enabled or disabled. Additionally, a Global Interrupt Enable Bit in the ENIR Register allows the Maskable interrupts to be collectively enabled or disabled. Thus, in order for a particular interrupt to be serviced, both the individual enable bit and the Global Interrupt bit (GIE) have to be set.

INTERRUPT PENDING REGISTER (IRPD)

The IRPD register contains a bit allocated for each interrupt vector. The occurrence of specified interrupt trigger conditions causes the appropriate bit to be set. There is no indication of the order in which the interrupts have been received. The bits are set independently of the fact that the interrupts may be disabled. IRPD is a Read/Write register. The bits corresponding to the maskable, external interrupts are normally cleared by the HPC16400 after servicing the interrupts.

For the interrupts from the on-board peripherals, the user has the responsibility of resetting the interrupt pending flags through software.

INTERRUPT CONDITION REGISTER (IRCD)

Three bits of the register select the input polarity of the external interrupt on I2, I3, and I4.

Servicing the Interrupts

The Interrupt, once acknowledged, pushes the program counter (PC) onto the stack thus incrementing the stack pointer (SP) twice. The Global Interrupt Enable (GIE) bit is reset, thus disabling further interrupts. The program counter is loaded with the contents of the memory at the vector address and the processor resumes operation at this point. At the end of the interrupt service routine, the user does a RETI instruction to pop the stack, set the GIE bit and return to the main program. The GIE bit can be set in the interrupt service routine to nest interrupts if desired. *Figure 6* shows the Interrupt Enable Logic.

Reset

The RESET input initializes the processor and sets ports A, B, and P in the TRI-STATE condition. RESET is an active-low Schmitt trigger input. The processor vectors to FFFF:FFFE and resumes operation at the address contained at that memory location.

Timer Overview

The HPC16400 contains a powerful set of flexible timers enabling the HPC16400 to perform extensive timer functions; not usually associated with microcontrollers.

The HPC16400 contains eight 16-bit timers. Each timer has an associated 16-bit register. Timer T0 is a free-running timer, counting up at a fixed CKI/16 (Clock Input/16) rate. It is used for Watch Dog logic, high speed event capture, and to exit from the IDLE mode. Consequently, it cannot be stopped or written to under software control. Timer T0 permits precise measurements by means of the capture registers I2CR, I3CR, and I4CR. A control bit in the register TMMODE configures timer T1 and its associated register R1 as capture registers I3CR and I2CR. The capture registers I2CR, I3CR, and I4CR respectively, record the value of timer T0 when specific events occur on the interrupt pins I2, I3, and I4. The control register IRCD programs the capture registers to trigger on either a rising edge or a falling edge of its respective input. The specified edge can also be programmed to generate an interrupt (see *Figure 7*).

The timers T2 and T3 have selectable clock rates. The clock input to these two timers may be selected from the following two sources: an external pin, or derived internally by dividing the clock input. Timer T2 has additional capability of being clocked by the timer T3 underflow. This allows the user to cascade timers T3 and T2 into a 32-bit timer/counter. The control register DIVBY programs the clock input to timers T2 and T3 (see *Figure 8*).

The timers T1 through T7 in conjunction with their registers form Timer-Register pairs. The registers hold the pulse duration values. All the Timer-Register pairs can be read from or written to. Each timer can be started or stopped under software control. Once enabled, the timers count down, and upon underflow, the contents of its associated register are automatically loaded into the timer.

Timer Overview (Continued)

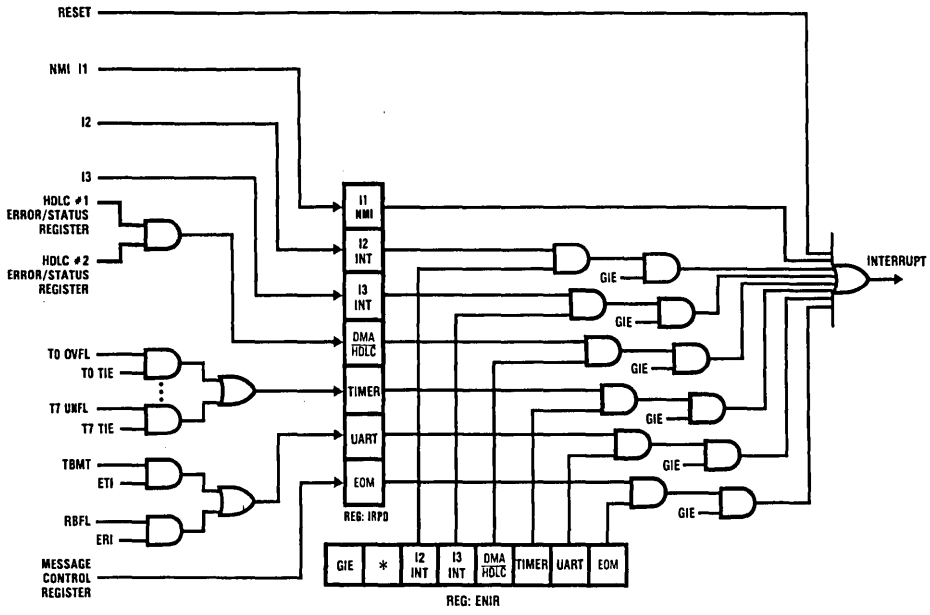

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FIGURE 6. Interrupt Enable Logic

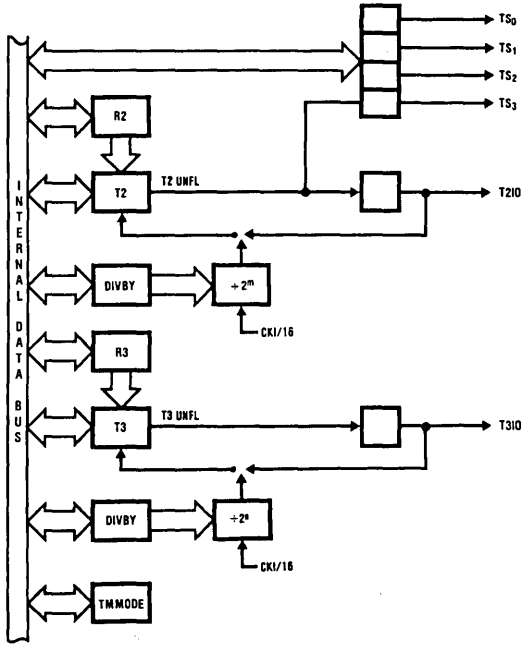

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FIGURE 8. Timers T2–T3 Block

Timer Overview (Continued)

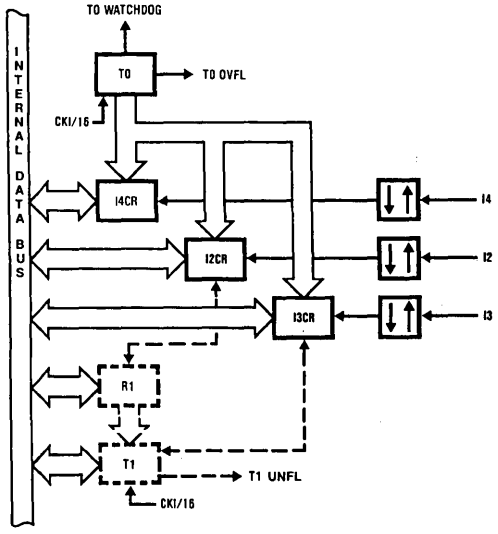

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FIGURE 7. Timers T0–T1 Block

SYNCHRONOUS OUTPUTS

The flexible timer structure of the HPC16400 simplifies pulse generation and measurement. There are four synchronous timer outputs (TS0 through TS3) that work in conjunction with the timer T2. The synchronous timer outputs can be used either as regular outputs or individually programmed to toggle on timer T2 underflows (see *Figure 8*).

Timer/register pairs 4–7 form four identical units which can generate synchronous outputs on port P (see *Figure 9*).

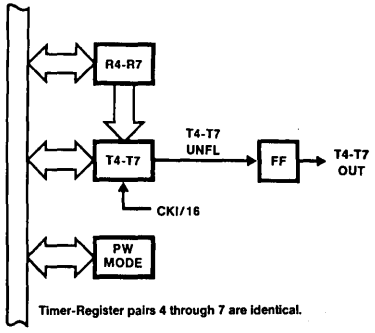

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FIGURE 9. Timers T4–T7 Block

Timer Registers

There are four control registers that program the timers. The divide by (DIVBY) register programs the clock input to timers T2 and T3. The timer mode register (TMMODE) contains control bits to start and stop timers T1 through T3. It also contains bits to latch and enable interrupts from timers T0 through T3. The control register PWMODE similarly programs the pulse width timers T4 through T7 by allowing them to be started, stopped, and to latch and enable interrupts on underflows. The PORTP register contains bits to preset the outputs and enable the synchronous timer output functions.

Timer Applications

The use of Pulse Width Timers for the generation of various waveforms is easily accomplished by the HPC16400.

Frequencies can be generated by using the timer/register pairs. A square wave is generated when the register value is a constant. The duty cycle can be controlled simply by changing the register value.

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FIGURE 10. Square Wave Frequency Generation

Synchronous outputs based on Timer T2 can be generated on the 4 outputs TS0–TS3. Each output can be individually programmed to toggle on T2 underflow. Register R2 contains the time delay between events. *Figure 11* is an example of synchronous pulse train generation.

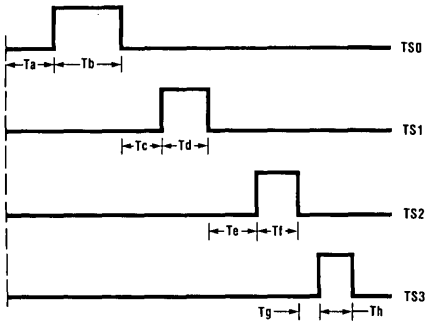

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FIGURE 11. Synchronous Pulse Generation

Watch Dog Logic

The Watch Dog Logic monitors the operations taking place and signals upon the occurrence of any illegal activity. The illegal conditions that trigger the Watch Dog logic are potentially infinite loops and illegal addresses. Should the Watch Dog register not be written to before Timer T0 overflows twice, or more often than once every 4096 counts, an infinite loop condition is assumed to have occurred. The illegal condition forces the Watch Out (WO) pin low. The WO pin is an open drain output and can be connected to the RESET or NMI inputs or to the users external logic.

MICROWIRE/PLUS

MICROWIRE/PLUS is used for synchronous serial data communications (see *Figure 12*). MICROWIRE/PLUS has an 8-bit parallel-loaded, serial shift register using SI as the input and SO as the output. SK is the clock for the serial shift register (SIO). The SK clock signal can be provided by an internal or external source. The internal clock rate is programmable by the DIVBY register. A DONE flag indicates when the data shift is completed.

The MICROWIRE/PLUS capability enables it to interface with any of National Semiconductor's MICROWIRE peripherals (i.e., A/D converters, display drivers, EEPROMs).

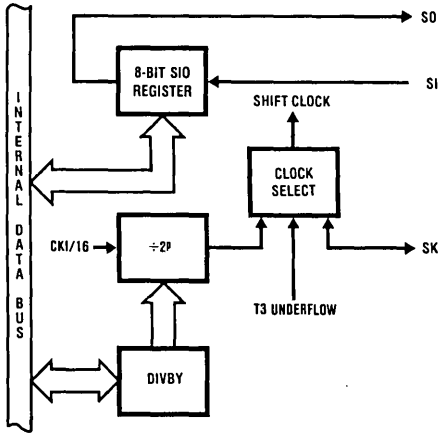

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FIGURE 12. MICROWIRE/PLUS

MICROWIRE/PLUS Operation

The HPC16400 can enter the MICROWIRE/PLUS mode as the master or a slave. A control bit in the IRCD register determines whether the HPC16400 is the master or slave. The shift clock is generated when the HPC16400 is configured as a master. An externally generated shift clock on the SK pin is used when the HPC16400 is configured as a slave. When the HPC16400 is a master, the DIVBY register programs the frequency of the SK clock. The DIVBY register allows the SK clock frequency to be programmed in 15 selectable steps from 64 Hz to 1 MHz with CKI at 17.0 MHz.

The contents of the SIO register may be accessed through any of the memory access instructions. Data waiting to be transmitted in the SIO register is clocked out on the falling edge of the SK clock. Serial data on the SI pin is clocked in on the rising edge of the SK clock.

HPC16400 UART

The HPC16400 contains a software programmable UART. The UART (see *Figure 13*) consists of a transmit shift register, a receiver shift register and five addressable registers, as follows: a transmit buffer register (TBUF), a receiver buffer register (RBUF), a UART control and status register (ENU), a UART receive control and status register (ENUR) and a UART interrupt and clock source register (ENUI). The ENU register contains flags for transmit and receive functions; this register also determines the length of the data frame (8 or 9 bits) and the value of the ninth bit in transmission. The ENUR register flags framing and data overrun errors while the UART is receiving. Other functions of the ENUR register include saving the ninth bit received in the data frame and enabling or disabling the UART's Wake-up Mode of operation. The determination of an internal or external clock source is done by the ENUI register, as well as selecting the number of stop bits and enabling or disabling transmit and receive interrupts.

The baud rate clock for the Receiver and Transmitter can be selected for either an internal or external source using two bits in the ENUI register. The internal baud rate is programmed by the DIVBY register. The baud rate may be selected from a range of 8 Hz to 128 kHz in binary steps or T3 underflow. By selecting a baud rate crystal, all standard baud rates from 75 baud to 38.4 kbaud can be generated. The external baud clock source comes from the CKX pin. The Transmitter and Receiver can be run at different rates by selecting one to operate from the internal clock and the other from an external source.

The HPC16400 UART supports two data formats. The first format for data transmission consists of one start bit, eight

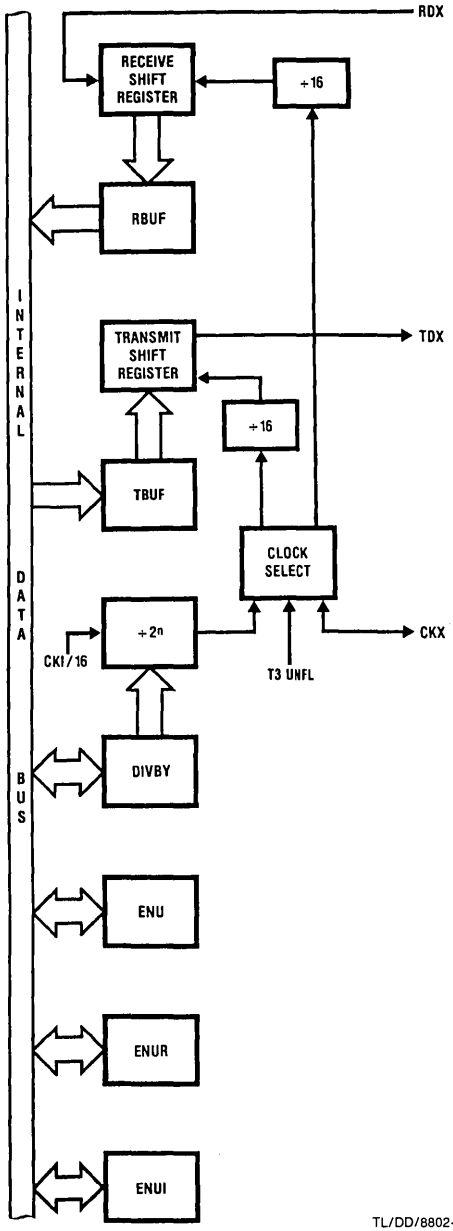

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FIGURE 13. UART Block Diagram

HPC16400 UART (Continued)

data bits and one or two stop bits. The second data format for transmission consists of one start bit, nine data bits, and one or two stop bits. Receiving formats differ from transmission only in that the Receiver always requires only one stop bit in a data frame.

UART Wake-up Mode

The HPC16400 UART features a Wake-up Mode of operation. This mode of operation enables the HPC16400 to be networked with other processors. Typically in such environments, the messages consist of addresses and actual data. Addresses are specified by having the ninth bit in the data frame set to 1. Data in the message is specified by having the ninth bit in the data frame reset to 0.

The UART monitors the communication stream looking for addresses. When the data word with the ninth bit set is received, the UART signals the HPC16400 with an interrupt. The processor then examines the content of the receiver buffer to decide whether it has been addressed and whether to accept subsequent data.

Programmable Serial Decoder Interface

The programmable serial decoder interface allows the two HDLC channels to be used with devices employing several popular serial protocols for point-to-point and multipoint data exchanges. These protocols combine the 'B' and 'D' channels onto common pins—received data, transmit data, clock and Sync, which normally occurs at an 8 KHz rate and provides framing for the particular protocol.

The decoder uses the serial link clock and Sync signals to generate internal enables for the 'D' and 'B' channels, thereby allowing the HDLC channels to access the appropriate channel data from the multiplexed link.

HDLC Channel Description

HDLC/DMA Structure

HDLC 1		HDLC 2	
HDLC1 Receive	HDLC1 Transmit	HDLC2 Receive	HDLC2 Transmit
DMAR1	DMAT1	DMAR2	DMAT2

GENERAL INFORMATION

Both HDLC channels on the HPC16400 are identical and operate up to 4.1 Mbps. When used in an ISDN basic access application, HDLC channel #1 has been designated for use with the 16 Kbps D-channel or the B1 channel and HDLC #2 can be used with either of the 64 Kbps B-channels. If the 'D' and 'B' channels are present on a common serial link, the programmable serial decoder interface generates the necessary enable signals needed to access the D and B channel data.

LAPD, the Link Access Protocol for the D channel is derived from the X.25 packet switching LAPB protocol. LAPD specifies the procedure for a terminal to use the D channel for the transfer of call control or user-data information. The procedure is used in both point-to-point and point-to-multipoint configurations. On the 16400, the HDLC controller contains user programmable features that allow for the efficient processing of LAPD Information.

HDLC Channel Pin Description

RX — Receive Serial Data Input. Data clocked in on positive CLK edge.

CLK — HDLC Channel Clock Input Signal.

REN — HDLC Channel Receiver Enable Input.

TX — Transmit Serial Data Output. Data clocked out on negative CLK edge.

TEN — HDLC Channel Transmitter Enable Input.

HDLC Functional Description

TRANSMITTER DESCRIPTION

Data information is transferred from external memory through the DMA controller into the transmit buffer register from where it is loaded into a 8-bit serial shift registers. The CRC is computed and appended to the frame prior to the closing flag being transmitted. Data is output at the TX output pin. If no further transmit commands are given the transmitter sends out continous flags or the idle pattern as selected by the control register.

An interrupt is generated when the transmit shift register is empty or on a transmit error condition. An assoicated transmit status register will contain the status information indicating the specific interrupt source.

TRANSMITTER FEATURES

Interframe fill: the transmitter can send either continuous '1's or repeated flags between the closing flag or one packet and the opening flag of the next. When the CPU commands the transmitter to open a new frame, the interframe fill is terminated immediately.

Abort: the 7 '1's abort sequence will be immediately sent on command from the CPU. If required it may be followed by a new opening flag to resend the aborted packet.

Bit/Byte boundaries: The message length between packet headers may have any number of bits and is not confined to byte boundaries. Three bits in the control register are used to indicate the number of valid bits in the last byte when operating in the bit mode. These bits are loaded by the users software.

RECEIVER DESCRIPTION

Data is input to the receiver on the RX pin. The receive clock can be externally input at the HDLC CLK pin, or it can be internally generated via the programmable timer chain.

Incoming data is routed through one of several paths depending on whether it is the flag, data, or CRC.

Once the receiver is enabled it waits for the opening flag of the incoming frame, then starts the zero bit deletion, addressing handling and CRC checking. All data between the flags is shifted through two 8-bit serial shift registers before being loaded into the buffer register. The user programmable address register values are compared to the incoming data while it resides in the shift registers. If an address match occurs or if operating in the transparent mode, the DMA channel is signaled that attention is required and the byte is transferred by it to external memory. Appropriate interrupts are generated to the CPU on the reception of a complete frame as indicated by a correct CRC, or on the occurance of a frame error.

HDLC Functional Description

(Continued)

There are two sources for the receive channel enable signal. It can be internally generated from the serial interface or it can be externally enabled.

The receive interrupt, in conjunction with status data in the control registers allows interrupts to be generated on the following conditions—CRC error, receive error and receive complete.

RECEIVER FEATURES

Flag sharing: the closing flag of one packet may be shared as the opening flag of the next. Receiver will be able to share a zero between flags—011111101111110 is a valid two flag sequence for receive (not transmit).

Interframe fill: the receiver automatically accepts either repeated flags or all '1's as the interframe fill.

Idle: Reception of successive 1's as the interframe fill sequence to be signaled to the user by setting the Idle bit in the Receive control and status register.

Short Frame Rejection: Reception of less than 4 bytes between flags will generate a frame error, terminating reception of the current frame and setting the Frame Error (FER) status bit in the Receive Control and Status register.

Abort: the 7 '1's abort sequence (received with no zero insertion) will be immediately recognized and will cause the receiver to reinitialize and return to searching the incoming data for an opening flag. Reception of the abort will cause the abort status bit in the Interrupt Error Status register to be set.

Bit/Byte boundaries: The message length between packet headers may have any number of bits and it is not confined to byte boundaries. Three bits in the status register are used to indicate the number of valid bits in the last byte when operating in the bit mode.

Addressing: Two user programmable bytes are available to allow frame address recognition on the two bytes immediately following the opening flag. When the received address matches the programmed value(s), the frame is passed through to the DMA channel. If no match occurs, the received frame address information is disregarded and he receiver returns to searching for the next opening flag and the address recognition process starts anew.

Support is provided to allow recognition of the broadcast address sequence of seven consecutive 1's. Additionally, a transparent mode of operation is available where no address decoding is done.

HDLC INTERRUPT CONDITIONS

The end of message interrupt (EOM) indicates that a complete frame has been received or transmitted by the HDLC controller. Thus, there are four separate sources for this interrupt, two each from each HDLC channel. The Message Control Register contains the pending bits for each source.

The HDLC/DMA error interrupt groups several related error conditions. Error conditions from both transmit/receiver channels can cause this interrupt, and the possible sources each have a status bit in the below register that is set on the occurrence of an error. The bit must then be serviced by the user.

HDLC CHANNEL CLOCK

Each HDLC channel uses the rising edge of the clock to sample the receive data. Outgoing transmit data is shifted out on the falling edge of the external clock. The maximum data rate when using the externally provided clocks is 4.1 Mb/s.

CYCLIC REDUNDACY CHECK

There are two standard CRC codes used in generating the 16-bit Frame Check Sequence (FCS) that is appended to the end of the data frame. Both codes are supported and the user selects the error checking code to be used through software control (Configuration reg). The two error checking polynomials available are:

(1) CRC—16 (x16 + x15 + x2 +1)

(2) CCITT CRC (x16 + x12 + x5 + 1)

LOOP BACK OPERATIONAL MODE

The user has the ability, by appropriately configuring the control registers, to internally route the transmitter output at the TX pin to the receiver input at the RX pin. The transmit clock would then be internally connected to the receive clock.

DMA Controller*

GENERAL INFORMATION

The HPC16400 uses Direct Memory Access (DMA) logic to facilitate data transfer between the 2 full Duplex HDLC channels and external packet RAM. There are four DMA channels to support the four individual HDLC channels. Control of the DMA channels is accomplished through registers which are configured by the CPU. These control registers define specific operation of each channel and changes are immediately reflected in DMA operation. In addition to individual control registers, a global control bit (MSS in Message Control Register) is available so that the HDLC channels may be globally controlled.

The DMA issues a bus request to the CPU when one or more of the individual HDLC channels request service. Upon receiving a bus acknowledge from the CPU, the DMA completes all requests pending and any requests that may have occurred during DMA operation before returning control to the CPU. If no further DMA transfers are pending, the DMA relinquishes the bus and the CPU can again initiate a bus cycle.

Four memory expansion bits have been added for each of the four channels to support data transfers into the expanded memory bank areas.

The DMA has priority logic for a DMA requesting service. The priorities are:

1st priority .....Receiver channel 1
2nd priority .....Transmit channel 1
3rd priority .....Receive channel 2
4th priority .....Transmit channel 2

RECEIVER DMA OPERATION

A receiver DMA operation is initiated by the Buffer register. Once a byte has been placed in the Buffer register from the HDLC, it generates a request and upon obtaining control of the bus, the DMA places the byte in external memory.

RECEIVER REGISTERS

All the following registers are Read/Write

A. Frame Length Register

This user programmable 16-bit register contains the maximum number of bytes to be placed in a data "block". If

*The specific registers and/or register names may have changed. Please contact the factory for updated information.

DMA Controller (Continued)

this number is exceeded, a Frame Too Long (FTLR1, FTLR2) error is generated. This register is decremented by one each Receiver DMA cycle.

B. CNTRL ADDR 1 / DATA ADDR 1 / CNTRL ADDR 2 / DATA ADDR 2 — The CNTRL ADDR register contains the external memory address where the Frame Header (Control & Address fields) are to be stored and the DATA ADDR register contains an equivalent address for the Information field.

TRANSMITTER DMA OPERATION

A transmitter DMA cycle is initiated by the TX Data Buffer (TDB). The TX Data Buffer generates a request when empty and the DMA responds by placing a Byte in the TDB. The HDLC transmitter can then accept the Byte to send when needed, upon which the TDB will issue another request, resulting in a subsequent DMA cycle.

TRANSMITTER REGISTERS

The following registers are Read/Write:

A. Field Address 1 (FA1) / # Bytes Field 1 (NBF1) / Field Address (FA2) / # Bytes Field 2 (NBF2) — FA1 and FA2 are starting addresses of blocks of information to transmitter. NBF1 and NBF2 are the number of bytes in the block to be transmitted starting the FA1.

The following registers are Read only:

B. Working Field Address (WFA)

Working Number of Bytes (WNB)

WFA is the present value of the Field address and will be the next memory location where the next byte will be accessed. WNB is the present value of the number of bytes to be transmitted. The value will be the number of bytes to be fetched from memory before the block information transfer is completed. On each transmit DMA cycle, WFA is incremented and WNB is decremented.

Shared Memory Support

Shared memory access provides a rapid technique to exchange data. It is effective when data is moved from a peripheral to memory or when data is moved between blocks of memory. A related area where shared memory access proves effective in multiprocessing applications where two CPUs share a common memory block. The HPC16400 supports shared memory access with two pins. The pins are the RDY/$\overline{HLD}$ input pin and the $\overline{HLDA}$ output pin. The user can software select either the Hold or Ready function by the state of a control bit. The $\overline{HLDA}$ output is multiplexed onto port B.

The host uses DMA to interface with the HPC16400. The host initiates a data transfer by activating the $\overline{HLD}$ input of the HPC16400. In response, the HPC16400 places its system bus in a TRI-STATE Mode, freeing it for use by the host. The host waits for the acknowledge signal ($\overline{HLDA}$) from the HPC16400 indicating that the sytem bus is free. On receiving the acknowledge, the host can rapidly transfer data into, or out of, the shared memory by using a conventional DMA controller. Upon completion of the message transfer, the host removes the HOLD request and the HPC16400 resumes normal operations.

Figure 14 illustrates an application of the shared memory interface between the HPC16400 and a Series 32000 system.

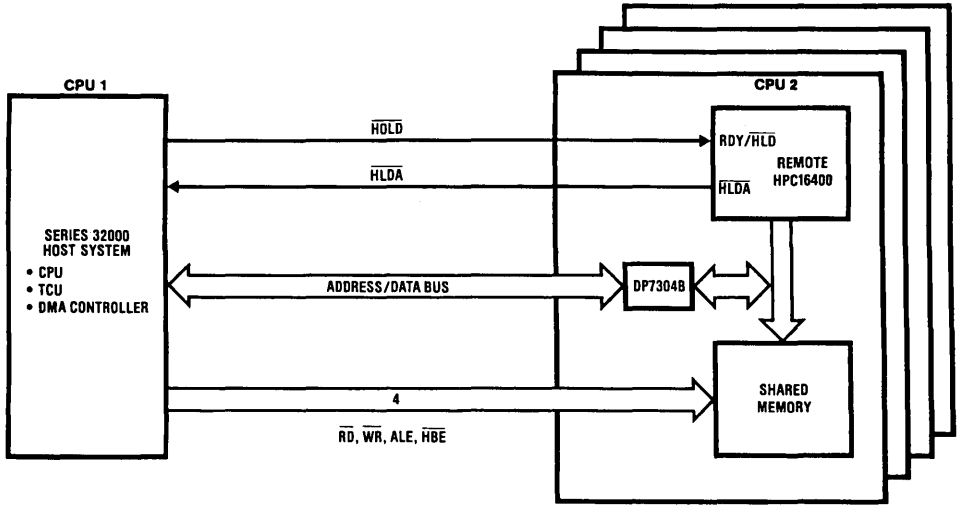

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FIGURE 14. Shared Memory Application: HPC16400 Interface to Series 32000 System

Memory

The HPC16400 has been designed to offer flexibility in memory usage. A total address space of 64 kbytes can be addressed with 256 bytes of RAM available on the chip itself.

Program memory addressing is accomplished by the 16-bit program counter on a byte basis. Memory can be addressed directly by instructions or indirectly through the B, X and SP registers. Memory can be addressed as words or bytes. Words are always addressed on even-byte boundaries. The HPC16400 uses memory-mapped organization to support registers, I/O and on-chip peripheral functions.

The HPC16400 memory address space extends to 64 kbytes and registers and I/O are mapped as shown in Table II.

Extended Memory Addressing

If more than 64k of addressing is desired in a HPC16400 system, on board bank select circuitry is available that allows four I/O lines of Port B (B9, B10, B13, B14) to be used in extending the address range. This gives the user a main routine area of 32k and 16 banks of 32k each for subroutine and data, thus getting a total of 544k of memory.

The Extended Memory Addressing mode is entered by setting the EMA control bit in the Message Control Register. If this bit is not set, the port B lines (B9, B10, B13, B14) are available as general purpose I/O or synchronous outputs as selected by the BFUN register.

The main memory area contains the interrupt vectors & service routines, stack memory, and common memory for the bank subroutines to use. The 16 banks of memory can contain program or data memory (note- since the on chip resources are mapped into addresses 0000-01FF, the first 512 bytes of each bank are not usable).

TABLE II. Memory Map*

FFFF:FFF0 FFEF:FFD0	Interrupt Vectors JSRP Vectors	
FFCF:FFCE : : : : 0201:0200	External expansion Memory	USER MEMORY
01FF:01FE : : 01C1:01C0	On Chip RAM	
01BB:01BA 01B9:01B8 01B7:01B6 01B5:01B4 01B3:01B2 01B1:01B0	Configuration Reg Rec Addr Comp Reg 2 Rec Addr Comp Reg 1 Interrupt Error Stat Xmit Cntrl & Status Recv Cntrl & Status	HDLC # 2
01AB:01AA 01A9:01A8 01A7:01A6 01A5:01A4 01A3:01A2 01A1:01A0	Configuration Reg Rec Addr Comp Reg 2 Rec Addr Comp Reg 1 Interrupt Error Stat Xmit Cntrl & Status Recv Cntrl & Status	HDLC # 1
0195:0194	Watch Dog Address	Watch Dog Logic
0193:0192 0191:0190 018F:018E 018D:018C 018B:018A 0189:0188 0187:0186 0185:0184 0183:0182 0181:0180	T0CON Register TMMODE Register DIVBY Register T3 Timer R3 Register T2 Timer R2 Register I2CR Register/ R1 I3CR Register/ T1 I4CR Register	Timer Block T0:T3
017D:017C 017B:017A 0179:0178 0177:0176 0175:0174 0173:0172 0171:0170	Working # Bytes Working Field Addr # Bytes 2 Field Addr 2 # Bytes 1 Field Addr 1 Xmit Cntrl & Status	DMAT # 2 (Xmit)
016B:016A 0169:0168 0167:0166 0165:0164 0163:0162 0161:0160	Frame Length Data Addr 2 Cntrl Addr 2 Data Addr 1 Cntrl Addr 1 Recv Cntrl & Status	DMAR # 2 (Recv)
015D:015C 015B:015A 0159:0158 0157:0156 0155:0154 0153:0152 0151:0150	Working # Bytes Working Field Addr # Bytes 2 Field Addr 2 # Bytes 1 Field Addr 1 Xmit Cntrl & Status	DMAT # 1 (Xmit)
014B:014A 0149:0148 0147:0146 0145:0144 0143:0142 0141:0140	Frame Length Data Addr 2 Cntrl Addr 2 Data Addr 1 Cntrl Addr 1 Recv Cntrl & Status	DMAR # 1 (Recv)
0131:0130	Message Control	
0128 0126 0124 0122 0120	ENUR register TBUF register RBUF register ENIU register ENU register	UART
0107:0106 0105:0104 0103:0102 0101:0100	DIR R register Port R register Serial Decoder Port D register	PORTS
00F5:00F4 00F3:00F2 00F1:00F0	BFUN register DIR B register DIR A register	PORTS A & B CONTROL
00E7:00E6	Reserved	
00E3:00E2 00E1:00E0	Port B Port A	PORTS A & B
00DE 00DD:00DC 00D8 00D6 00D4 00D2 00D0	Microcode ROM dump Halt Enable register Port I input register SIO register IRCD register IRPD register ENIR register	PORT CONTROL & INTERRUPT CONTROL REGISTERS
00CF:00CE 00CD:00CC 00CB:00CA 00C9:00C8 00C7:00C6 00C5:00C4 00C3:00C2 00C1:00C0	X register B register K register A register PC register SP register (reserved) PSW register	HPC10640 CORE REGISTERS
00BF:00BE : : 0001:0000	On Chip RAM	USER RAM

*The Memory Map has changed. Please contact factory for an updated version of the Memory Map.

HPC16400 CPU

The HPC16400 CPU has a 16-bit ALU and six 16-bit registers.

Arithmetic Logic Unit (ALU)

The ALU is 16 bits wide and can do 16-bit add, subtract and shift or logic AND, OR and exclusive OR in one timing cycle. The ALU can also output the carry bit to a 1-bit C register.

Accumulator (A) Register

The 16-bit A register is the source and destination register for most I/O, arithmetic, logic and data memory access operations.

Address (B and X) Registers

The 16-bit B and X registers can be used for indirect addressing. They can automatically count up or down to sequence through data memory.

Boundary (K) Register

The 16-bit K register is used to set limits in repetitive loops of code as register B sequences through data memory.

Stack Pointer (SP) Register

The 16-bit SP register is the stack pointer that addresses the stack. The SP register is incremented by two for each push or call and decremented by two for each pop or return. The stack can be placed anywhere in user memory and be as deep as the available memory permits.

Program (PC) Register

The 16-bit PC register addresses program memory.

Addressing Modes

ADDRESSING MODES—ACCUMULATOR AS DESTINATION

Register Indirect

This is the "normal" mode of addressing for the HPC16400 (instructions are single-byte). The operand is the memory addressed by the B register (or X register for some instructions).

Direct

The instruction contains an 8-bit or 16-bit address field that directly points to the memory for the operand.

Indirect

The instruction contains an 8-bit address field. The contents of the WORD addressed points to the memory for the operand.

Indexed

The instruction contains an 8-bit address field and an 8- or 16-bit displacement field. The contents of the WORD addressed is added to the displacement to get the address of the operand.

Immediate

The instruction contains an 8-bit or 16-bit immediate field that is used as the operand.

Register Indirect (Auto Increment and Decrement)

The operand is the memory addressed by the X register. This mode automatically increments or decrements the X register (by 1 for bytes and by 2 for words).

Register Indirect (Auto Increment and Decrement) with Conditional Skip

The operand is the memory addressed by the B register. This mode automatically increments or decrements the B register (by 1 for bytes and by 2 for words). The B register is then compared with the K register. A skip condition is generated if B goes past K.

ADDRESSING MODES—DIRECT MEMORY AS DESTINATION

Direct Memory to Direct Memory

The instruction contains two 8- or 16-bit address fields. One field directly points to the source operand and the other field directly points to the destination operand.

Immediate to Direct Memory

The instruction contains an 8- or 16-bit address field and an 8- or 16-bit immediate field. The immediate field is the operand and the direct field is the destination.

Double Register Indirect using the B and X Registers

Used only with Reset, Set and IF bit instructions; a specific bit within the 64 kbyte address range is addressed using the B and X registers. The address of a byte of memory is formed by adding the contents of the B register to the most significant 13 bits of the X register. The specific bit to be modified or tested within the byte of memory is selected using the least significant 3 bits of register X.

HPC Instruction Set Description

Mnemonic	Description	Action
ARITHMETIC INSTRUCTIONS		
ADD	Add	MA + Meml → MA carry → C
ADC	Add with carry	MA + Meml + C → MA carry → C
DADC	Decimal add with carry	MA + Meml + C → MA (Decimal) carry → C
SUBC	Subtract with carry	MA − Meml + C → MA carry → C
DSUBC	Decimal subtract w/carry	MA − Meml + C → MA (Decimal) carry → C
MULT	Multiply (unsigned)	MA*Meml → MA & X, 0 → K, 0 → C
DIV	Divide (unsigned)	MA/Meml → MA, rem. → X, 0 → K, 0 → C
IFEQ	If equal	Compare MA & Meml, Do next if equal
IFGT	If greater than	Compare MA & Meml, Do next if MA → Meml
AND	Logical and	MA and Meml → MA
OR	Logical or	MA or Meml → MA
XOR	Logical exclusive-or	MA xor Meml → MA
MEMORY MODIFY INSTRUCTIONS		
INC	Increment	Mem + 1 → Mem
DECSZ	Decrement, skip if 0	Mem − 1 → Mem, Skip next if Mem = 0
BIT INSTRUCTIONS		
SET	Set bit	1 → Mem.bit (bit is 0 to 7 immediate)
RESET	Reset bit	0 → Mem.bit
IF	If bit	If Mem.bit is true, do next instr.
MEMORY TRANSFER INSTRUCTIONS		
LD	Load	Meml → MA
	Load, incr/decr X	Mem(X) → A, X ±1 (or 2) → X
ST	Store to Memory	MA → Mem
X	Exchange	A ↔ Mem; Mem ↔ Mem
	Exchange, incr/decr X	A ↔ Mem(X), X ±1 (or 2) → X
PUSH	Push Memory to Stack	W → W(SP), SP + 2 → SP
POP	Pop Stack to Memory	SP − 2 → SP, W(SP) → W
LDS	Load A, incr/decr B, Skip on condition	Mem(B) → A, B ±1 (or 2) → B, Skip next if B greater/less than K
XS	Exchange, incr/decr B, Skip on condition	Mem(B) ↔ A,B ±1 (or 2) → B, Skip next if B greater/less than K
REGISTER LOAD IMMEDIATE INSTRUCTIONS		
LD A	Load A immediate	imm → A
LD B	Load B immediate	imm → B
LD K	Load K immediate	imm → K
LD X	Load X immediate	imm → X
LD BK	Load B and K immediate	imm → B,imm' → K
ACCUMULATOR AND C INSTRUCTIONS		
CLR A	Clear A	0 → A
INC A	Increment A	A + 1 → A
DEC A	Decrement A	A − 1 → A
COMP A	Complement A	1's complement of A → A
SWAP A	Swap nibbles of A	A15:12 ← A11:8 ← A7:4 ↔ A3:0
RRC A	Rotate A right thru C	C → A15 → ... → A0 → C
RLC A	Rotate A left thru C	C ← A15 ← ... ← A0 ← C
SHR A	Shift A right	0 → A15 → ... → A0 → C
SHL A	Shift A left	C ← A15 ← ... ← A0 ← 0
SET C	Set C	1 → C
RESET C	Reset C	0 → C
IF C	IF C	Do next if C = 1
IFN C	IF not C	Do next if C = 0

HPC Instruction Set Description (Continued)

Mnemonic	Description	Action
TRANSFER OF CONTROL INSTRUCTIONS		
JSRP	Jump subroutine from table	PC → W(SP),SP+2 → SP W(table#) → PC
JSR	Jump subroutine relative	PC → W(SP),SP+2 → SP,PC+ # → PC (#is +1024 to −1023)
JSRL	Jump subroutine long	PC → W(SP),SP+2 → SP,PC+ # → PC
JP	Jump relative short	PC+ # → PC(# is +32 to −31)
JMP	Jump relative	PC+ # → PC(#is +256 to −255)
JMPL	Jump relative long	PC+ # → PC
JID	Jump indirect at PC + A	PC+A+1 → PC
JIDW		then Mem(PC)+PC → PC
NOP	No Operation	PC ← PC + 1
RET	Return	SP−2 → SP,W(SP) → PC
RETS	Return then skip next	SP−2 → SP,W(SP) → PC, & skip
RETI	Return from interrupt	SP−2 → SP,W(SP) → PC, interrupt re-enabled

Note: W is 16-bit word of memory
MA is Accumulator A or direct memory (8 or 16-bit)
Mem is 8-bit byte or 16-bit word of memory
MemI is 8- or 16-bit memory or 8 or 16-bit immediate data
imm is 8-bit or 16-bit immediate data

Memory Usage

Number Of Bytes For Each Instruction (number in parenthesis is 16-Bit field)

	Using Accumulator A						To Direct Memory			
	Reg Indir. (B)	Reg Indir. (X)	Direct	Indir	Index	Immed.	Direct *	Direct **	Immed. *	Immed. **
LD	1	1	2(4)	3	4(5)	2(3)	3(5)	5(6)	3(4)	5(6)
X	1	1	2(4)	3	4(5)	—	—	—	—	—
ST	1	1	2(4)	3	4(5)	—	—	—	—	—
ADC	1	2	3(4)	3	4(5)	4(5)	4(5)	5(6)	4(5)	5(6)
SBC	1	2	3(4)	3	4(5)	4(5)	4(5)	5(6)	4(5)	5(6)
DADC	1	2	3(4)	3	4(5)	4(5)	4(5)	5(6)	4(5)	5(6)
DSBC	1	2	3(4)	3	4(5)	4(5)	4(5)	5(6)	4(5)	5(6)
ADD	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
MULT	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
DIV	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
IFEQ	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
IFGT	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
AND	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
OR	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)
XOR	1	2	3(4)	3	4(5)	2(3)	4(5)	5(6)	4(5)	5(6)

*8-bit direct address
**16-bit direct address

Instructions that modify memory directly

	(B)	(X)	Direct	Indir	Index	B&X
SET	1	2	3(4)	3	4(5)	1
RESET	1	2	3(4)	3	4(5)	1
IF	1	2	3(4)	3	4(5)	1
DDSZ	3	3	2(4)	3	4(5)	
INCD	3	3	2(4)	3	4(5)	

Immediate Load Instructions

	Immed.
LD B,*	2(3)
LD X,*	2(3)
LD K,*	2(3)
LD BK,*,*	3(5)

Memory Usage (Continued)

Register Indirect Instructions with Auto Increment and Decrement

Register B With Skip		
	(B+)	(B−)
LDS A,*	1	1
XS A,*	1	1

Register X		
	(X+)	(X−)
LD A,*	1	1
X A,*	1	1

Instructions Using A and C

CLR	A	1
INC	A	1
DEC	A	1
COMP	A	1
SWAP	A	1
RRC	A	1
RLC	A	1
SHR	A	1
SHL	A	1
SET	C	1
RESET	C	1
IF	C	1
IFN	C	1

Transfer of Control Instructions

JSRP	1
JSR	2
JSRL	3
JP	1
JMP	2
JMPL	3
JID	1
JIDW	1
NOP	1
RET	1
RETS	1
RETI	1

Stack Reference Instructions

	Direct
PUSH	2
POP	2

Code Efficiency

One of the most important criteria of a single chip microcontroller is code efficiency. The more efficient the code, the more features that can be put on a chip. The memory size on a chip is fixed so if code is not efficient, features may have to be sacrificed or the programmer may have to buy a larger, more expensive version of the chip.

The HPC16400 has been designed to be extremely code-efficient. The HPC16400 looks very good in all the standard coding benchmarks; however, it is not realistic to rely only on benchmarks. Many large jobs have been programmed onto the HPC16400, and the code savings over other popular microcontrollers has been considerable—often the jobs take less than one-half the memory!

Reasons for this saving of code include the following:

SINGLE BYTE INSTRUCTIONS

The majority of instructions on the HPC16400 are single-byte. There are two especially code-saving instructions:

JP is a 1-byte jump. True, it can only jump within a range of plus or minus 32, but many loops and decisions are often within a small range of program memory. Most other micros need 2-byte instructions for any short jumps.

JSRP is a 1-byte call subroutine. The user makes a table of his 16 most frequently called subroutines and these calls will only take one byte. Most other micros require two and even three bytes to call a subroutine. The user does not have to decide which subroutine addresses to put into his table; the assembler can give him this information.

EFFICIENT SUBROUTINE CALLS

The 2-byte JSR instructions can call any subroutine within plus or minus 1k of program memory.

MULTIFUNCTION INSTRUCTIONS FOR DATA MOVEMENT AND PROGRAM LOOPING

The HPC16400 has single-byte instructions that perform multiple tasks. For example, the XS instruction will do the following:

1. Exchange A and memory pointed to by the B register
2. Increment the B register
3. Compare the B register versus the K register
4. Generate a conditional skip if B is greater than K

The value of this multipurpose instruction becomes evident when looping through sequential areas of memory and exiting when the loop is finished.

BIT MANIPULATION INSTRUCTIONS

Any bit of memory, I/O or registers can be set, reset or tested by the single byte bit instructions. The bits can be addressed directly or indirectly. Since all registers and I/O are mapped into the memory, it is very easy to manipulate specific bits to do efficient control.

DECIMAL ADD AND SUBTRACT

This instruction is needed to interface with the decimal user world.

It can handle both 16-bit words and 8-bit bytes.

The 16-bit capability saves code since many variables can be stored as one piece of data and the programmer does not have to break his data into two bytes. Many applications store most data in 4-digit variables. The HPC16400 supplies 8-bit byte capability for 2-digit variables and literal variables.

MULTIPLY AND DIVIDE INSTRUCTIONS

The HPC16400 has 16-bit multiply and divide instructions. This saves both code and time. Multiply and divide can use immediate data or data from memory. The ability to multiply and divide by immediate data saves code since this function is often needed for scaling, base conversion, computing indexes of arrays, etc.

Development Support

The MOLE (Microcontroller On-Line Emulator) is a low cost development system and emulator for all microcontroller products. These include COPs, TMP, 8050U and the HPC Family of Products. The MOLE consists of a BRAIN Board, Personality Board and optional host software.

The purpose of a MOLE is to provide the user with a tool to write and assemble code, emulate code for the target microcontroller and assist in both the software & hardware debugging of the system.

It is a self-contained computer with its own firmware which provides for all system operation, emulation control, communication, PROM programming and diagnostic operations.

It contains three serial ports because multiple ports are usually needed to optionally connect to a terminal, a host system, a printer or modem, or to connect to other MOLEs in a multi-MOLE environment.

MOLE can be used in either a stand alone mode or in conjunction with selected host systems, i.e., those using CP/M or PC-DOS. Communicating via RS-232 port.

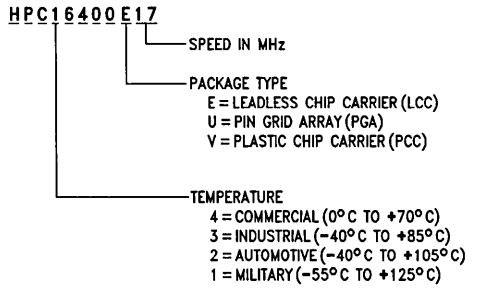
Dial-A-Helper is a service provided by the MOLE applications group. If a user is having difficulty in getting a MOLE to operate in a particular mode or it is acting peculiar, he can contact us via his system and a modem. He can leave messages on our electronic bulletin board which we will respond to, or he can arrange for us to actually take control of his system via modem for debugging purposes.

The applications group can then cause his system to execute various commands and try to resolve the customer's problem by actually getting the customer's system to respond. 99% of the time the problem is resolved. This allows us to respond in minutes instead of days when applications help is needed.

Part Selection

The HPC family includes devices with many different options and configurations to meet various application needs. The number HPC16400 has been generally used throughout this datasheet to represent the whole family of parts. The following chart explains how to order various options available when ordering HPC family members.

Note: All options may not currently be available.



TL/DD/8802–18

FIGURE 15. HPC Family Part Numbering Scheme

Examples

HPC46400V17—Commercial temp (0° to +70°C), PCC

HPC16400E17—Military temp (−55°C to +125°C), LCC

"B" Channel, or DS0 Channel

A "B" (for Basic) channel is a 64 kb/s full-duplex transparent data channel. It is octet (=byte) oriented, that is it can be considered as a channel bearing 8k octets/sec. "B" channels are synchronized to the network and are generally circuit-switched (not packet switched). The 64 kb/s rate is also known as a DS0 interface.

"D" Channel

The "D" channel is a packet-mode message-oriented channel on which the data-link layer (layer 2) protocol is carried in HDLC frames. At a basic access point the "D" channel runs at 16 kb/s, while at a primary access point it runs at 64 kb/s. (There is no reason why a "D" channel could not be defined to run at even higher speeds, e.g., 1.544 or 2.048 Mb/s, though that does not seem to be a part of current standardization work.)

Three types of data may be handled by a "D" channel:

1. Type "s" (signaling) using layer 3 of the LAPD protocol.
2. Type "p" (packet) user's packet-oriented data.
3. Type "t" (telemetry) data, typically alarms and energy monitoring functions operating at a low scan rate.

   The data type is identified by the SAPI (Service Access Point Identifier) in the HDLC extended address field.

Basic Access to the ISDN

Two independent "B" channels (B1 and B2) together with a "D" channel operating at 16 kb/s form the basic access structure. A minimum transmission rate of 144 kb/s full duplex is therefore required for basic access transport, although in some applications additional bits are used for localized functions.

Figure 1 shows the names of the functional blocks and interfaces as defined in CCITT specifications.

The 'U' interface is the single twisted pair loop between a customer's premises and the local central office. To transmit 144 kb/s or more full-duplex over this link, which may be several miles long and have over 40 dB of attenuation of the data signal, requires a complex transceiver. Adaptive echo-cancellation techniques are necessary and, although the transmission format is not yet specified by CCITT, considerable work is in progress in the U.S. T1D1.3 ISDN Study Group to establish a standard for North America. 160 kb/s is the likely transmission rate, while the line code will be 2B1Q.

The 'S' interface passes the same 2 'B' channels and the 'D' channel on to the terminals, together with some additional bits used for synchronization, contention control in the 'D' channel, and other housekeeping functions. CCITT specification I.430 defines the physical layer of this interface. A transceiver is required for transmission at the 192 kb/s bit rate, over separate transmit and receive twisted pairs (which already exist in both office and residential telephone wiring within the premises in many countries). Alternate Mark Inversion coding is used.

2 additional pairs are specified as an option, 1 for power and 1 for spare, making this an 8 wire interface. A plug and jack have been standardized so that the 'S' interface can be a "universal portability point" for ISDN terminals from any manufacturer in the world.

Primary Access to the ISDN

Primary access is provided at a DS1 interface, consisting of either:

1. Twenty-three "B" channels plus one 64 kb/s "D" channel at 1.544 Mb/s (North America), or :
2. Thirty "B" channels plus one 64 kb/s "D" channel at 2.048 Mb/s (Europe and Rest of World).

CCITT specification I.431 defines the multiplexing and control schemes for primary access.

TE—Terminal Equipment

Two sub-groups of terminals are defined:

1. TE-1 is a full ISDN terminal which is synchronized to the network channels (not just the far-end terminal) and uses LAPD signaling. It connects to the ISDN at the "S" reference point, which is intended to be the point in the network at which any type of **basic** access terminal can be connected, i.e., the "portability" point.
2. TE-2 is a non-ISDN terminal, generally one of today's asynchronous or synchronous terminals operating at rates < 64 kb/s. This includes terminals which have RS232C, RS449, V.21, V.24, V.35, X.21 or X.25 packet-mode interfaces. Each type of interface must be adapted from the "R" reference point to the "S" reference point by means of a Terminal Adapter (TA).

TA—Terminal Adapter

A terminal adapter converts either asynchronous or synchronous data from non-ISDN terminals into data which is synchronized with ISDN B or D channels. The data rate must be adapted by means of stuffing extra bits in a prescribed pattern into the bit stream to adapt the data rate to 64 kb/s.

Terminal adaption also requires the conversion of modem handshaking signals to ISDN compatible signaling, and currently there are 2 competing schemes: either using LAPD in the D channel (i.e. out-of-band signaling) or applying LAPD-type messages but passing them end-to-end via the B channel (i.e. in-band). There are strong arguments for both methods, mostly concerned with how signaling is converted at the boundary between an ISDN and today's network ("interworking"), and it remains to be seen which will win as a standard.

NT—Network Termination

The NT terminates the network at the user's end of the 2 wire loop at the customer's premises. It converts the "U" interface to the "S" and "T" interface (see *Figure 1*) and acts as the "master" end of the user's passive bus. B and D channels must pass transparently through the NT, and there is no capability for intercepting LAPD messages in the NT.

Thus a typical NT for **basic** access will consist of an 'S' interface transceiver and a 'U' interface transceiver connected back-to-back with appropriate power supplies and fault monitoring capability.

An NT can also be an intelligent controller such as a PABX, LAN access node, or a terminal cluster controller.

LT—Line Termination

Typically, the LT consists of the "U" interface tranceiver and power feeding functions on the ISDN line card. These functions must interface to the switch at the "V" reference point, which is not currently being standardized by CCITT. It could be a proprietary backplane interface or a nationally specified interface which would allow the LT to be physically and electrically separated from the switch.

ISO Layered Protocol Model

The ISO (International Standards Organization) has defined a 7 layer model structure which describes convenient break points between various parts of the hardware and software in any data communications system.

Layer 1: Physical layer, that is the hardware which transports bits across interfaces. This includes ISDN transceivers, modems etc., power supplies, methods of activating and de-activating a transmission link, and also the transmission medium itself, such as wire, fiber, plugs and sockets, etc.

Layer 2: Data Link layer, which describes a basic framing structure and bit assignments to enable higher layer messages to be passed across a physical link. HDLC framing, addressing and error control are the major elements of this layer in ISDN.

Layer 3: Network layer, that is those parts of a message associated with setting-up, controlling and tearing-down a call through the network. These are all software control functions, and generally this is the highest layer in the ISO protocol model which is considered in chip development.

The top 4 layers relate to the structure of the actual application programs;

Layer 4: Transport layer, concerned with defining sources and destinations within an operating system for the transfer of application programs.

Layer 5: Session layer.

Layer 6: Presentation layer.

Layer 7: Application layer.

These layers are generally running on a high level machine, and discussion regarding this machine is outside the scope of this document.

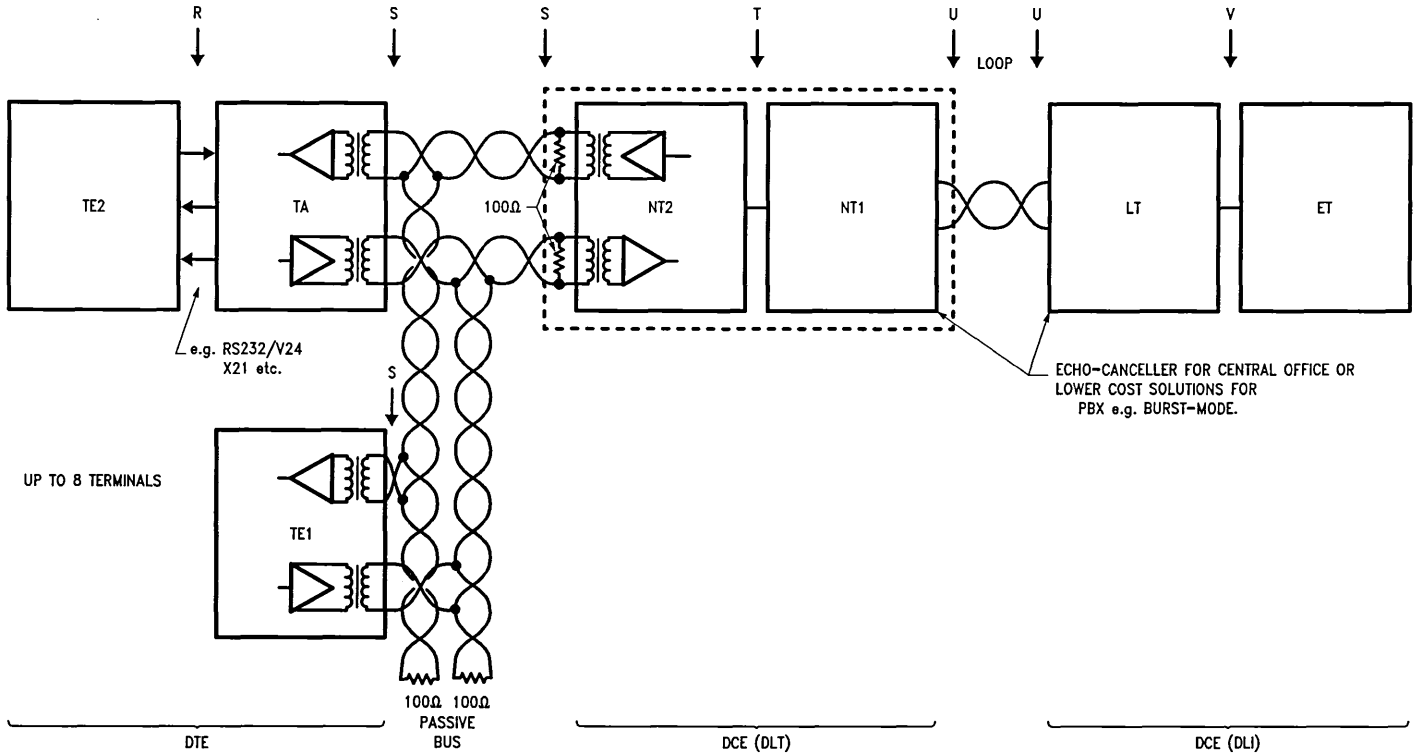
LAPD

Link Access Protocol in the "D" channel is the name given to the packet-mode signaling protocol defined in CCITT specs Q920 and Q921 for the data link layer (layer 2) and Q930 and Q931 for the network layer (layer 3 in the ISO 7 layer reference model). At layer 2, LAPD uses the HDLC framing format. This protocol defines the bits, bytes and sequence of states necessary between the user and the network to establish, control and terminate calls using any of the 100 or more types of services which may be available via an ISDN. If the users at both ends of the call are connected to the ISDN and there is a through path for the D channel then end-to-end call control is available.

Because of this extensive range of services, implementation of full LAPD requires considerable memory and processing power. Standards work has recently focused on definition of a minimal subset of LAPD to cover the basic requirements of call control.

Activation/De-activation

Activation is the process of powering up the 'S' and 'U' interfaces from their standby (i.e. de-activated) states and sending specific signals across the interfaces to get the whole loop synchronized to the network. A small state machine in each TE and the NT controls this sequence of events, and uses timers to ensure that, if the activation attempt should fail for any reason, the user or network is alerted. At the end of a call an orderly exit from the network is effected by sending de-activation sequences before any equipment can power-down.



TE: Terminal Equipment
TA: Terminal Adaptor (Protocol Conversion & Rate Adaption for Non-ISDN Terminals)
NT2: Network Termination 2 (Protocol for Link Control, MUX/DEMVX etc)
NT1: Network Termination 1 (Loop Transceiver, Power Extraction)
LT: Line Termination (Loop Transceiver, Power Feed)
ET: Exchange Termination (Protocol Handling, MUX/DEMUX, Switching)

FIGURE 1. The ISDN Interfaces

Section 3

Modems

Section 3 Contents

*Devices not covered in last publication

National Semiconductor Corporation

PRELIMINARY

microCMOS

MM74HC942 300 Baud Modem

General Description

The MM74HC942 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC942 utilizes microCMOS Technology, 2 layers of polysilicon and 1 layer of metal P-well CMOS. Switched capacitor techniques are used to perform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600Ω phone line. They can perform two-to-four-wire conversion and drive the line at a maximum of 0 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

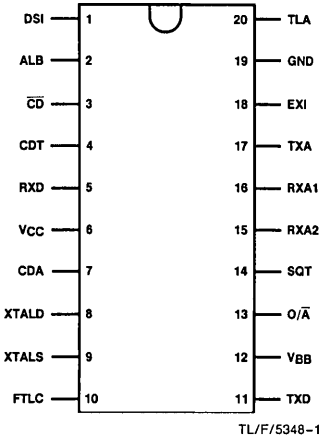
- Drives 600Ω at 0 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- ±5V supplies
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signalling systems
- Remote process control

Connection and Block Diagrams

Dual-In-Line Package



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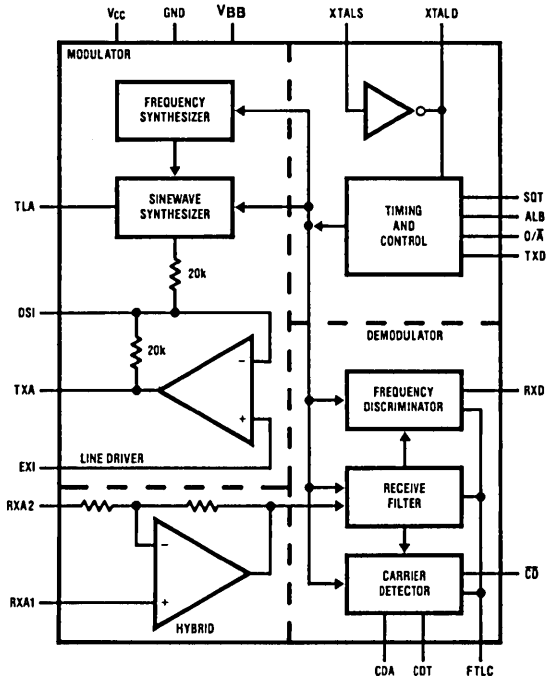
Top View

Order Number MM74HC942J, N
See NS Package J20A or N20A



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Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
Supply Voltage (V_{BB})	+0.5 to −7.0V
DC Input Voltage (V_{IN})	V_{BB}−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	V_{BB}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Supply Voltage (V_{BB})	−4.5	−5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A) MM74HC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics

Symbol	Parameter	Conditions	T = 25°C		74HC T = −40 to 85°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|=20\ \mu A$ $\|I_{OUT}\|=4.0$ mA, $V_{CC}=4.5V$	V_{CC}	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.7	V V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|=20\ \mu A$ $\|I_{OUT}\|=4.0$ mA, $V_{CC}=4.5V$		0.1 0.26	0.1 0.4	V V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	μA
I_{OZ}	Output TRI-STATE® Leakage Current RXD and $\overline{CD}$ Outputs	ALB = SQT = V_{CC}			±5	μA
I_{CC}, I_{BB}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$, V_{IL} = GND ALB or SQT = GND Transmit Level = −9 dBm	8.0	12.0	12.0	mA
I_{CC}, I_{BB}	Power Down Supply Current	ALB = SQT = V_{CC} $V_{IH}=V_{CC}$, V_{IL} = GND			300	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

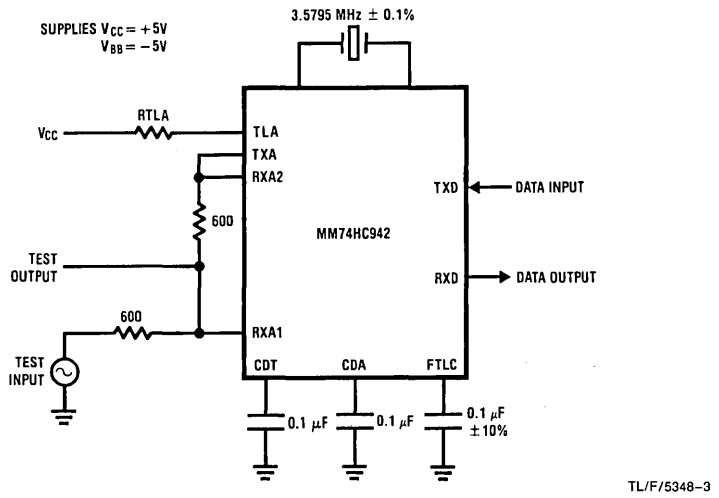
*The demodulator specifications apply to the MM74HC942 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC942 modulator.

AC Electrical Characteristics

Unless otherwise specified, all specifications apply to the MM74HC942 over the range −40°C to +85°C using a V_{CC} = +5V ±10%, a V_{BB} = −5V ±10% and a 3.579MHz ±0.1% crystal.*

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER							
F_{CE}	Carrier Frequency Error					4	Hz
	Power Output	V_{CC}=5.0V	R_{TLA} = 0	−3	−1.5	0	dBm
		R_L=1.2 kΩ	R_{TLA} = 5.49 kΩ	−12	−10.5	−9	dBm
	2nd Harmonic Energy				−62	−56	dBm
RECEIVE FILTER AND HYBRID							
	Hybrid Input Impedance (Pins 15 and 16)			50			kΩ
	FTLC Output Impedance			5	10	50	kΩ
	Adjacent Channel Rejection	RXA2=GND TXA=GND or V_{CC} Input to RXA1		60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)							
	Carrier Amplitude			−48		−9	dBm
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud			100	200	μS
	Bit Bias	Alternating 1-0 Pattern			5	10	%
	Carrier Detect Trip Points	CDA=1.2V	Off to On	−45	−42	−40	dBm
		V_{CC}=5.0V	On to Off	−47	−45	−42	dBm
	Carrier Detect Hysteresis	V_{CC}=5V		2	3	4	dB

AC Specification Circuit



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Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data output pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system, XTALD can be driven.
9	XTALS	Crystal Sense: Refer to Pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receive filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	V_{BB}	Negative Supply: The recommended supply is −5V.
13	O/$\overline{A}$	Originate/$\overline{Answer}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded.
19	GND	Ground: This defines the chip 0V.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC942 uses frequency shift keying (FSK) of an audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC942 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC942 is capable of transmitting and receiving data simultaneously.

The tone allocation by the MM74HC942 and other Bell 103 compatible modems is shown in Table I. The terms "originate" and "answer" which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

TABLE I. BELL 103 Allocation

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switched capacitor nine-pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60 Hz, a common noise component.

The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques. The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency produces one of four tones depending on the O/$\overline{A}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter. The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

TRANSMIT LEVEL ADJUSTMENT

The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source impedances.

The transmit level is programmable by placing a resistor from TLA to VCC. With a 5.5k resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the MM74HC942 will interface to most telephones. This arrangement is called the "permissive arrangement." The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

SNR can be maximized by adjusting the transmit level until the level at the exchange reaches −12 dBm. This must be done with the cooperation of the telephone company. The programming resistor used is specific for a given installation and is often included in the telephone jack at the installation. The modem is thus programmable and can be used with any jack correctly wired. This arrangement is called the universal registered jack arrangement and is possible with the MM74HC942. The values of resistors required to program the MM74HC942 follow the most common code in use; the universal service order code. The required resistors are given in Table II.

TABLE II. Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ohms)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490
4	−8	3,610
5	−7	2,520
6	−6	1,780
7	−5	1,240
8	−4	866
9	−3	562
10	−2	336
11	−1	150
12	0	0

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used;

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on Pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$T_{\overline{CDL}} \cong 6.4 \times C_{CDT}$ for $\overline{CD}$ going low

$T_{\overline{CDH}} \cong 0.54 \times C_{CDT}$ for $\overline{CD}$ going high

Where $T_{\overline{CDL}}$ & $T_{\overline{CDH}}$ are in seconds, and C_{CDT} is in μF.

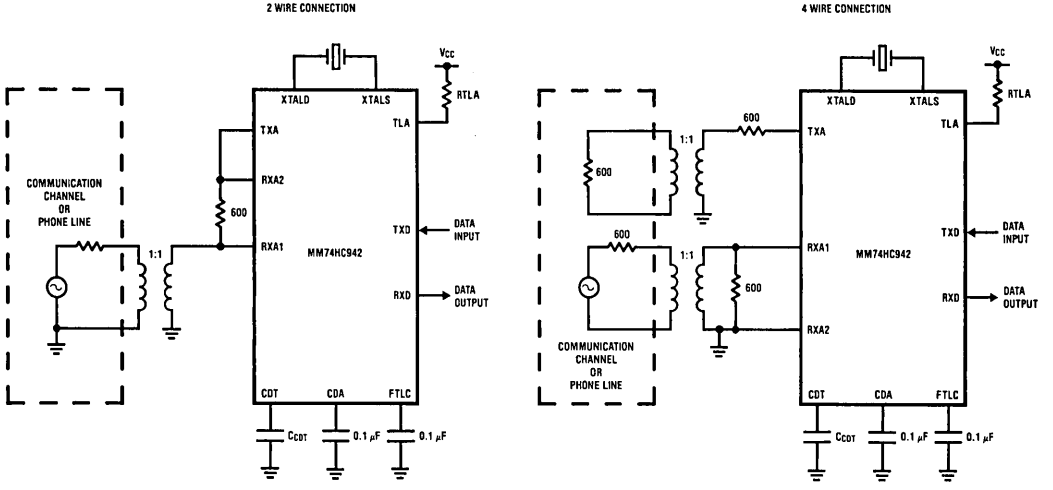
3

Applications Information (Continued)

DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC942 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout. Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

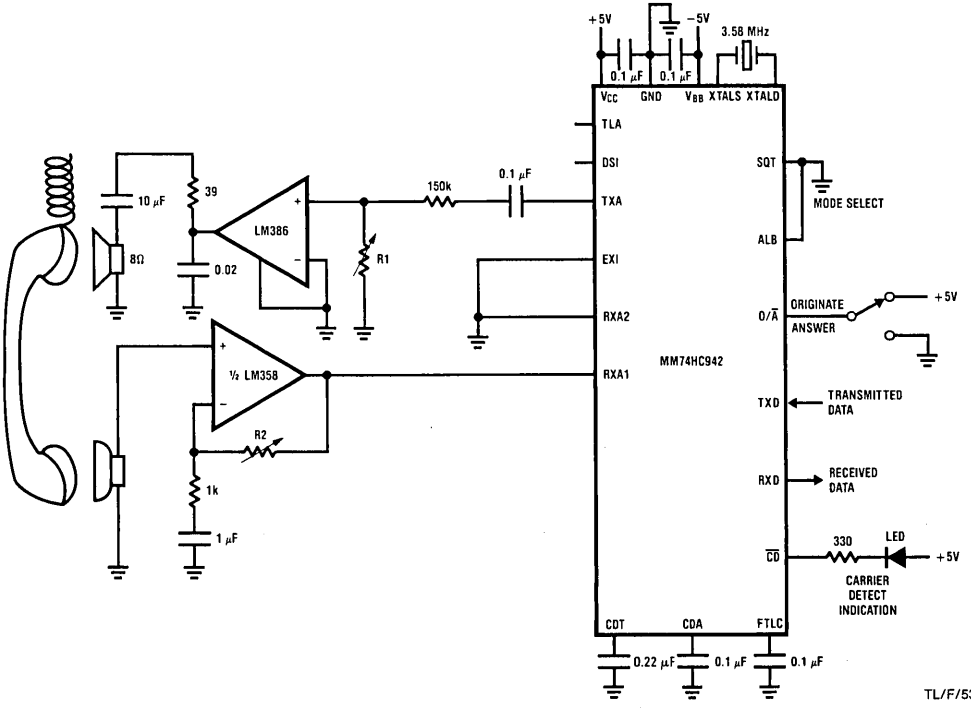
Interface Circuits for MM74HC942 300 Baud Modem



TL/F/5348–4

C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.

Complete Acoustically Coupled 300 Baud Modem



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Note: The efficiency of the acoustic coupling will set the valves of R1 and R2.

National Semiconductor Corporation

PRELIMINARY

microCMOS

MM74HC943 300 Baud Modem

General Description

The MM74HC943 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC943 utilizes microCMOS Technology, 2 layers of polysilicon and 1 layer metal P-well CMOS. Switched capacitor techniques are used to peform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600Ω phone line. They can perform two to four wire conversion and drive the line at a maximum of −9 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine-pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

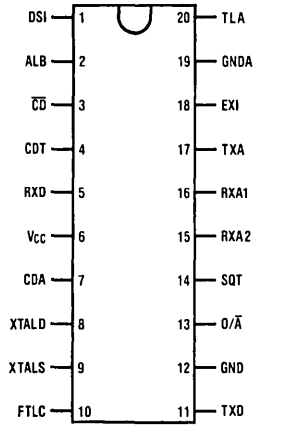
- 5V supply
- Drives 600Ω at −9 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signaling systems
- Remote process control

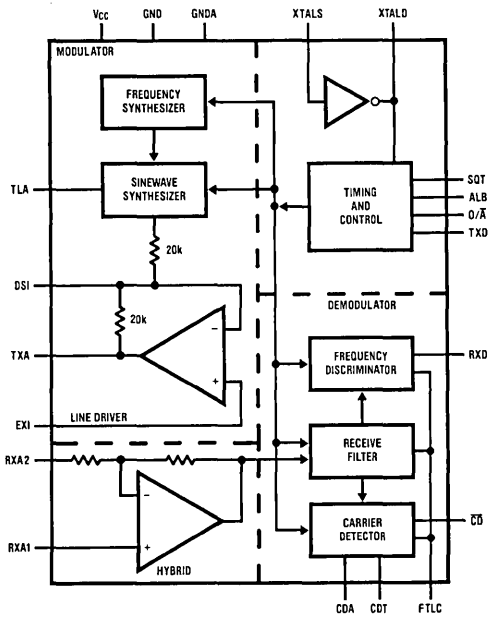
Connection and Block Diagrams

Dual-In-Line Package



TOP VIEW TL/F/5349–1

Order Number MM74HC943J
or MM74HC943N
See NS Package J20A or N20A



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Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A) MM74HC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HC T_A = −40 to 85°C		Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	V_{CC-EE}	V_{CC} − 0.1 3.84	V_{CC} − 0.1 3.7	V V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V		0.1 0.33	0.1 0.4	V V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	μA
I_{OZ}	Output TRI-STATE® Leakage Current, RXD and $\overline{CD}$ Outputs	ALB = SQT = V_{CC}			±5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IH} = V_{CC}, V_{IL} = GND ALB or SQT = GND Transmit Level = −9 dBm	8.0		10.0	mA
I_{GNDA}	Analog Ground Current		1.0		2.0	mA
I_{CC}	Power Down Supply Current	ALB = SQT = V_{CC} V_{IH} = V_{CC}, V_{IL} = GND			300	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

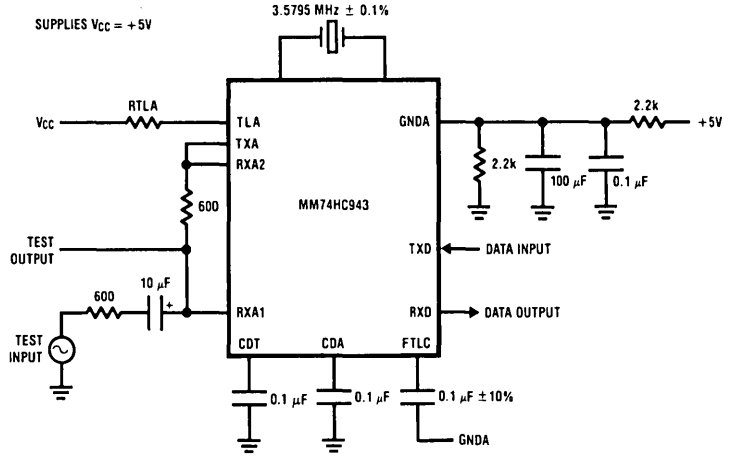
*The demodulator specifications apply to the MM74HC943 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC943 modulator.

AC Electrical Characteristics

Unless otherwise specified, all specifications apply to the MM74HC943 over the range −40°C to +85°C using a V_{CC} of +5V ±10%, and a 3.579 MHz ±0.1% crystal.*

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER							
F_{CE}	Carrier Frequency Error					4	Hz
	Power Output	V_{CC} = 5.0V R_L = 1.2 kΩ	R_{TLA} = 5490Ω	−12	−10.5	−9	dBm
	2nd Harmonic Energy				−62	−56	dBm
RECEIVE FILTER AND HYBRID							
	Hybrid Input Impedance (Pins 15 and 16)			50			kΩ
	FTLC Output Impedance			5	10	50	kΩ
	Adjacent Channel Rejection	RXA2 = GNDA, TXD = GND or V_{CC} Input to RXA1		60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)							
	Carrier Amplitude			−48		−12	dBm
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud			100	200	μS
	Bit Bias	Alternating 1-0 Pattern			5	10	%
	Carrier Detect Trip Points	CDA = 1.2V	Off to On	−45	−42	−40	dBm
		V_{CC} = 5.0V	On to Off	−47	−45	−42	dBm
	Carrier Detect Hystereisis	V_{CC} = 5.0V		2	3	4	dB

AC Specification Circuit



TL/F/5349–3

Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This input may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data output pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system. XTALD can be driven.
9	XTALS	Crystal Sense: Refer to pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receiver filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	GND	Ground: This defines the chip 0V.
13	O/$\overline{A}$	Originate/$\overline{Answer}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded to GNDA.
19	GNDA	Analog Ground: Analog signals within the chip are referred to this pin.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC943 uses frequency shift keying (FSK) of audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC943 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC943 is capable of transmitting and receiving data simultaneously.

The tone allocation used by the MM74HC943 and other Bell 103 compatible modems is shown in Table I. The terms "originate" and "answer" which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

TABLE I. Bell 103 Tone Allocation

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switch capacitor nine pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60Hz, a common noise component.

The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency synthesizer produces one of four tones depending on the O/$\overline{A}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter.

The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

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The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source inpedances.

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TABLE II. Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ω)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used:

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on Pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$$T_{\overline{CDL}} \cong 6.4 \times C_{CDT} \quad \text{for } \overline{CD} \text{ going low}$$

$$T_{\overline{CDH}} \cong 0.54 \times C_{CDT} \quad \text{for } \overline{CD} \text{ going high}$$

Where $T_{\overline{CDL}}$ & $T_{\overline{CDH}}$ are in seconds, and C_{CDT} is in μF.

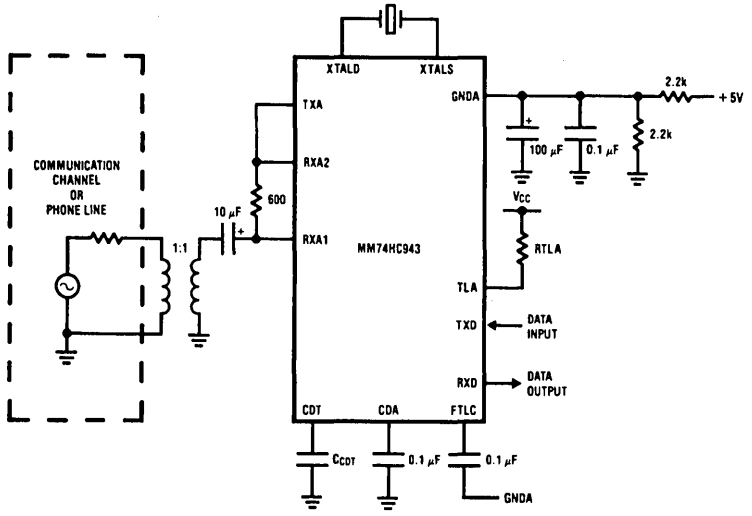
DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC943 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout. Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

Applications Information (Continued)

Interface Circuits for MM74HC943 300 Baud Modem

2 Wire Connection



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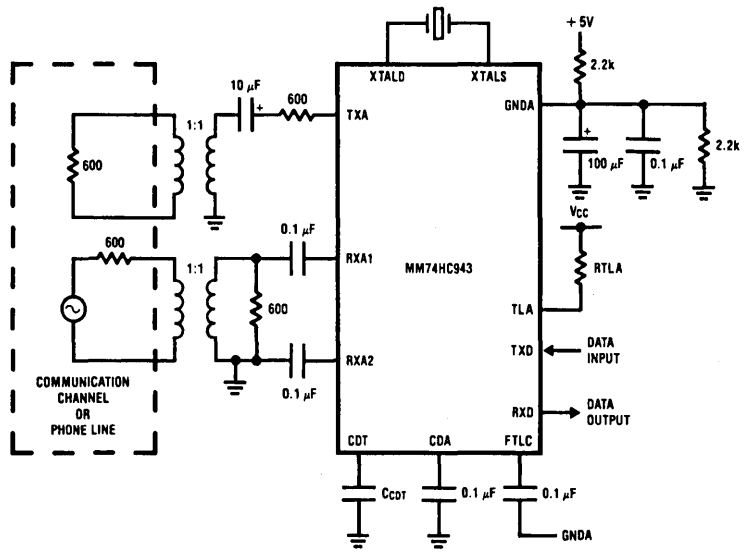
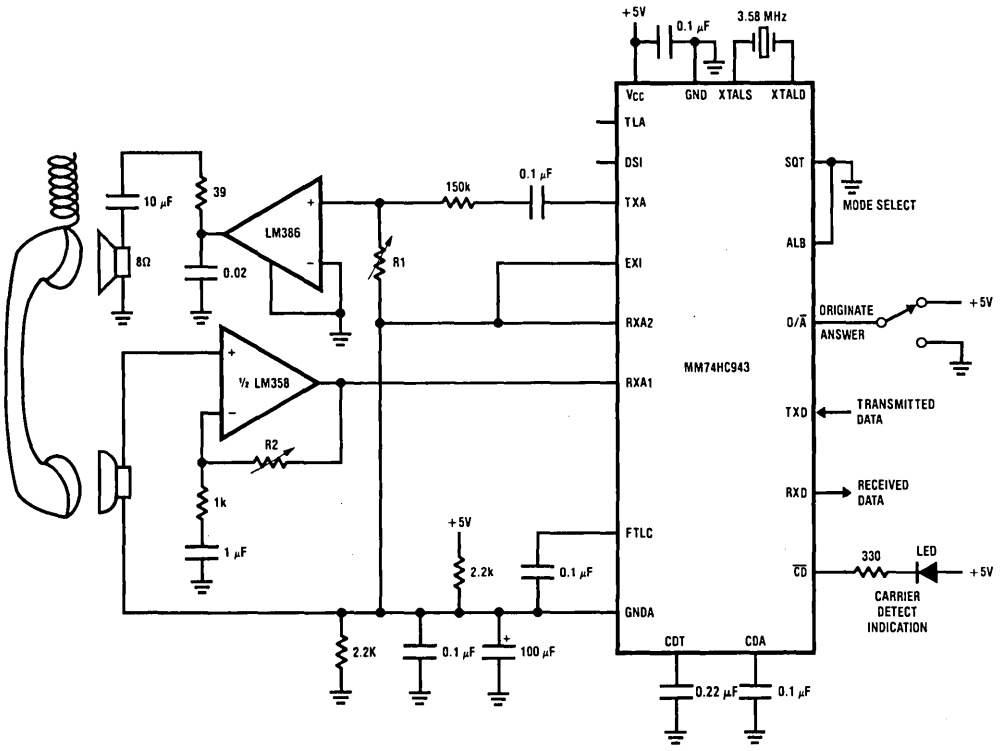
4 Wire Connection



TL/F/5349–5

C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.

Complete Acoustically Coupled 300 Baud Modem



TL/F/5349–6

Note: The efficiency of the acoustic coupling will set the values of R1 and R2.

National Semiconductor Corporation

PRELIMINARY

microCMOS

TP3330 Monolithic Full Duplex 1200/600/300 BPS Bell 212A/V.22 Modem

General Description

The TP3330 is a single chip full duplex 1200/600/300 BPS voiceband modem that operates over two wire voice-grade phone lines. It is compatible with Bell 212A, Bell 103/113 (1200/300 BPS) and CCITT V.22 A,B (1200/600 BPS) modem standards. All modulation, demodulation and filtering functions are performed on-chip.

The TP3330 contains an on-chip USART that performs serial-to-parallel and parallel-to-serial conversions on data characters. It can be connected directly to the host processor or controller through a standard microprocessor bus. The device provides status information on error conditions (parity, overrun, framing and break detect) as well as modem status conditions to the CPU. Also included on-chip is a full prioritized interrupt system which reduces software overhead in the CPU. When operating in asynchronous mode, it is functionally equivalent to the INS8250A UART.

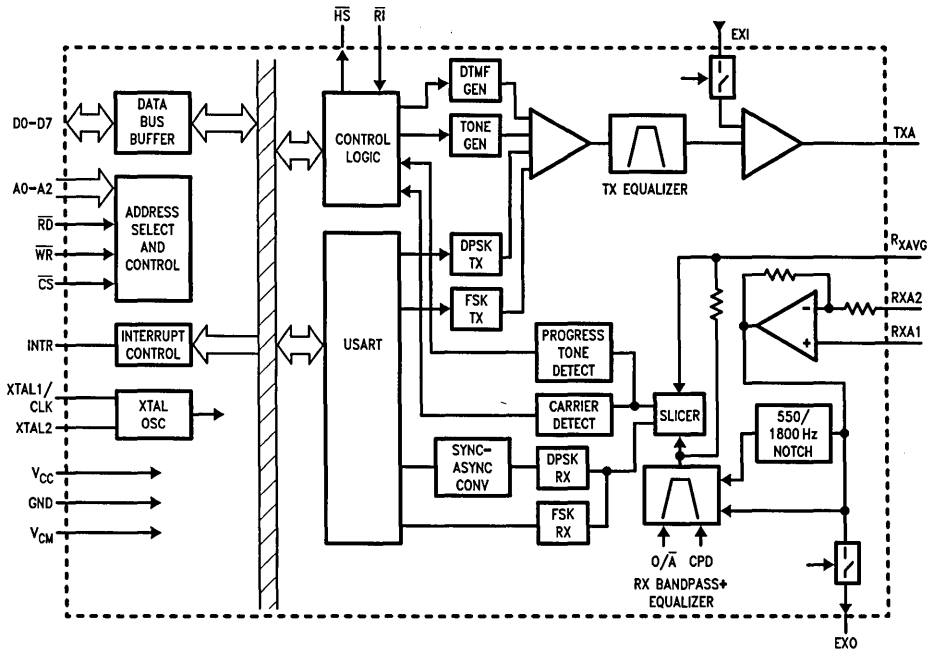
Additional functions on the device are an on-chip DTMF generator and call progress tone detector to facilitate auto-dialing. Hook-switch control output and an interrupt input for Ring Detect are provided to facilitate auto-answering. Interfacing to the phone line is simplified by the on-chip hybrid circuit.

The TP3330 is implemented with National's advanced dual-metal silicon gate microCMOS process. The device operates from a single +5V supply, and is ideal for portable or battery operated systems.

Features

- Bell 212A and Bell 103/113 compatible
- CCITT V.22 A,B compatible
- On-chip USART with full prioritized interrupt system
- Synchronous transmission: 1200/600 BPS
- Asynchronous transmission: 1200/600/300 BPS
- Hybrid and line driver with switched audio access
- DTMF generator
- Call progress tone detection
- Loopback test modes
- +5V only single supply operation
- LSTTL and CMOS compatible logic

Block Diagram



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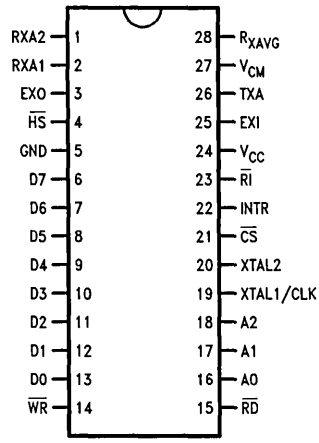
Connection Diagrams

Dual-In-Line Package



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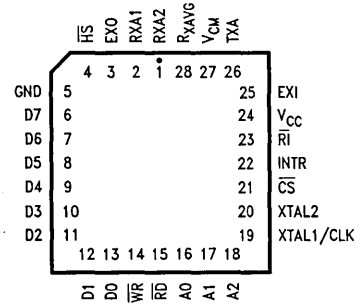
Top View

Order Number TP3330N
See NS Package Number N28B
Plastic Chip Carrier (PCC)



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Top View

Order Number TP3330V
See NS Package Number V28A

Pin Descriptions

Pin Number	Name	Function
21	$\overline{CS}$	**Chip Select:** When $\overline{CS}$ is low, the device is selected, enabling communication between the TP3330 and the CPU. When $\overline{CS}$ is high, the Data Bus is in TRI-STATE, $\overline{RD}$ and $\overline{WR}$ will have no effect on the device.
15	$\overline{RD}$	**Read Strobe:** With $\overline{CS}$ low, a logic low at $\overline{RD}$ input allows the CPU to read data or status information from the TP3330.
14	$\overline{WR}$	**Write Strobe:** With $\overline{CS}$ low, a logic low at $\overline{WR}$ input allows the CPU to write data or control words into the TP3330.
16–18	A0, A1, A2	**Register Select:** These 3 inputs are the address selects to a particular internal register of the TP3330 to read from or write to during a read or write operation. A0 is the LSB.
6–13	D7–D0	**Data Bus:** This data bus is comprised of 8 TRI-STATE input/output lines. The bus provides bidirectional communications between the CPU and the TP3330. Data, control words and status information are transferred via this bus. D0 is the LSB and D7 is the MSB. Serial data on the line is LSB first.
22	INTR	**Interrupt Output:** This line goes high whenever any one of the interrupt types has an active high condition and is enabled via the Interrupt Enable Register. The INTR output is TRI-STATE when Bit 3 of MCR2 is set to logic 0.
19	XTAL1/ CLK	This is the input of the on-chip oscillator circuit which requires an external 4.91520 MHz crystal. It can also be used as the input for an external 4.91520 MHz clock signal.
20	XTAL2	This is the output of the on-chip oscillator high gain inverter.
24	V_{CC}	Positive power supply pin. The supply voltage is +5V ±5% referenced to GND. A 0.1 μF bypass capacitor is required to be connected from V_{CC} to GND.
5	GND	**Ground:** All digital signals are referenced to this pin.
27	V_{CM}	**Analog Common Mode:** This pin is biased to ½ V_{CC} by an internal resistor divider and must be AC bypassed by an external 100 μF electrolytic and a 0.1 μF ceramic capacitor. All analog signals are referenced to this pin.
26	TXA	Transmit analog output of the line driver amplifier.
2, 1	RXA1, RXA2	**Receive Analog Inputs:** RXA1 and RXA2 are analog high impedance inputs to the receiver buffer amplifier. When connected as recommended, they produce a 600Ω hybrid circuit.

Pin Descriptions (Continued)

Pin Number	Name	Function
25	EXI	**External Audio Input:** This is a high impedance input to the line driver amplifier which can be used to transmit an externally generated tone or voice. The EXI input is switched on or off by Bit 5 of the Handshaking Control Register. The input signal from EXI is not filtered by the Transmit filter, and should be less than 1 Vp-p in order to prevent output clipping. When not used, it should be connected to V_{CM}.
3	EXO	**External Audio Output:** This is a buffered audio output of the receiver, capable of driving a 10 kΩ load. The EXO output is switched on or off by Bit 4 of the Handshaking Control Register.
28	R_{XAVG}	This is the comparator input of the internal slicer circuit. An external 0.01 μF capacitor must be connected from this pin to V_{CM}.
4	$\overline{HS}$	**Hook Switch Output:** This logical latched output may be used to drive an external relay driver for hook-switch control. It is programmed by Bit 7 of the Dialing Control Register. A logic high at Bit 7 will set the $\overline{HS}$ output to logic low level.
23	$\overline{RI}$	**Ring Indicator:** A logical low at this input indicates the presence of ringing signal received by an external ring detector. The CPU can monitor the $\overline{RI}$ input by reading Bit 6 of the Modem Status Register 2. Whenever the $\overline{RI}$ input changes from a low to high state, an interrupt is generated if the Modem Status Interrupt is enabled.

Functional Description

POWER-UP INITIALIZATION

When power is first applied, the internal power-on reset circuitry initializes the TP3330. Internal registers (except the Receive Buffer, Transmitter Holding and Sync-character Registers) are reset to their initial conditions. The state of the output signals are also set to their inactive conditions. (Refer to Table I.) A Master Reset can be generated by setting Bit 2 of the Modem Control Register 2.

TRANSMITTER

The transmitter section consists of a digital modulator and spectrum controller, a switched capacitor transmit equalizer, a post filter, and a line driver amplifier. At 1200/600 BPS, the modulator is a DPSK (Differential Phase Shift-Keyed) modulator with a scrambler circuit that prevents loss of synchronization. At 300 BPS, the modulator is a phase-coherent FSK (Frequency Shift-Keyed) modulator. Data information from the CPU is converted into a phase modulated or a frequency modulated sine wave that can be transmitted over the switched telephone network.

Half-channel fixed compromised equalization is provided by the transmit equalizer, which also attenuates any unwanted frequency components, so that the out-of-band emission is within the limits of FCC and CCITT specifications. *Figure 1* shows the out-of-band energy relative to the transmit carrier.

The line driver is a low distortion power amplifier that outputs the transmit carrier or the DTMF signal and is able to drive a −9 dBm signal into a 600Ω line. When the modem is not transmitting data or DTMF signals, externally generated tones or voice can be transmitted to the line from the EXI input. It is enabled by setting Bit 5 of the Handshaking Control Register. When not used, this input should be connected to V_{CM}.

Table II shows the frequency assignments of the Transmit Carrier.

TABLE I. Reset Functions

Register/Signals	Reset State
Interrupt Enable Register	All Bits Low
Interrupt Identification Register	Bit 0 is High, Bits 1–7 are Low
Line Control Register 1	All Bits Low
Modem Control Register 2	All Bits Low
Line Status Register	All Bits Low, Except Bits 5 & 6 which are High
Modem Status Register 2	All Bits Low, Except Bit 6 which is an input
Line Control Register 2	All Bits Low
Modem Control Register 1	All Bits Low
Dialing Control Register	All Bits Low
Handshaking Control Register	All Bits Low
Modem Status Register 1	All Bits Low
Test Mode Register	All Bits Low
INTR	Low
$\overline{HS}$	High

Functional Description (Continued)

TABLE II. Transmit Carrier Frequency Assignment

Standard	Data Rate	Nominal Carrier Frequency (Hz)	Actual Carrier Frequency (Hz)	% Deviation from Nominal
Bell 212A	300 BPS Originating Mark	1270	1265.625	−0.34
	300 BPS Originating Space	1070	1068.750	−0.12
	300 BPS Answering Mark	2225	2221.875	−0.14
	300 BPS Answering Space	2025	2025	0
	1200 BPS Low Band	1200	1200	0
	1200 BPS High Band	2400	2400	0
	Answer Tone	2225	2221.875	−0.14
CCITT V.22	600/1200 BPS Low Band	1200	1200	0
	600/1200 BPS High Band	2400	2400	0
	Answer Tone	2100	2100	0
	Guard Tone	550	553.125	+0.57
		1800	1800	0

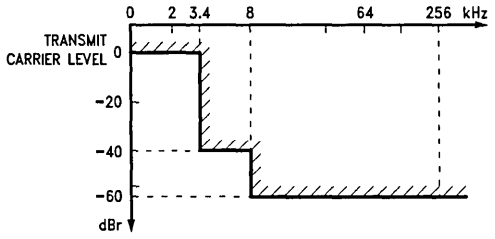

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FIGURE 1. Out-of-Band Energy Relative to Transmit Carrier

RECEIVER

The receiver consists of a 2-to-4 wire hybrid amplifier, an anti-alias filter, a switched capacitor receive bandpass filter and a low distortion digital demodulator. When connected as recommended, the input buffer amplifier performs as a 2-to-4 wire converter, canceling the transmitted signal from the incoming received signal.

An audio output is provided at EXO for audio monitoring of the received signals from the line. It can be used to drive an external power amplifier, such as the LM386, for audio monitoring of call progress. It is enabled by setting Bit 4 of the Handshaking Control Register.

The receive filter is a 22-pole switched capacitor bandpass filter which can be programmed to operate in the low band or high band channel. It rejects out-of-band transmission, noise components and the undesirable adjacent channel echo signals which can be fed from the transmitter section to the receiver section over the 2-wire phone line. For CCITT V.22 operation, a programmable 550 Hz or 1800 Hz notch filter is also included to reject the guard tone that is transmitted along with the high band carrier. A half channel amplitude and group delay equalizer is also included to ensure low bit error rate and low bit length distortion when connected to any voice grade phone line.

At 1200/600 BPS, the demodulator is a DPSK demodulator with a phase-locked loop clock recovery circuit. The received data is descrambled using the inverse of the transmit scrambler polynomial. In the asynchronous mode, the sync-to-async converter re-inserts the stop bit deleted by the transmitting modem. At 300 BPS, the demodulator is a FSK demodulator.

CARRIER DETECTOR

The carrier detector monitors the level of the receive signal. To prevent transmission of erroneous data to the CPU, the receive data output from the demodulator is clamped to logic high when the carrier falls below the receive threshold level for a time greater than $t_{CD\ OFF}$. Whenever the receive signal is above the threshold level for a time greater than $t_{CD\ ON}$, Bit 7 in the Modem Status Register 2 (CD) is set to logic 1, indicating the presence of valid carrier, and the demodulator output is enabled.

When the Call Progress Tone Detector is enabled, the sampling clock frequency of the receive bandpass filter is scaled down by 2.5 times, so that it covers the passband (350 Hz to 620 Hz) of the precise call progress tones. CD ON indicates the presence of tones, while CD OFF indicates the absence of tones. Such a cadence is easily monitored by the CPU, which can discriminate between the types of call progress tones as shown in the following table:

Dial Tone	350 Hz + 440 Hz	Continuous
Busy Tone	480 Hz + 620 Hz	0.5s ON /0.5s OFF
Re-Order Tone	480 Hz + 620 Hz	0.25s ON /0.25s OFF
Ringback Tone from Central Office:	440 Hz + 480 Hz	2s ON /4s OFF
from PBX:	440 Hz + 480 Hz	1s ON /3s OFF

The Modem Answer Tone is detected by the Answer Tone Detector, which is reflected by Bit 1 of the Modem Status Register 2.

DTMF GENERATOR

An on-chip DTMF generator facilitates auto-dialing. It accepts BCD input from the CPU, and is able to generate all 16 standard DTMF tone pairs. With DTMF ENABLE (Bit 4 of the Dialing Control Register) set to logic high, a 4-bit binary number previously loaded into locations Bits 0–3 is decoded and sets the high group and low group programmable counters to the appropriate divider ratios. The output voltage at TXA is the sum of the high and low group sine waves superimposed on a DC level of approximately ½ V_{CC}. The modulator and EXI are disabled, and the gain of the receive buffer amplifier is reduced by 20 dB in order to prevent overloading the receive filter section.

Table III shows the output tone frequencies, and Table IV is the functional truth table.

Functional Description (Continued)

TABLE III. DTMF Output Frequency Accuracy

Tone Group	Standard DTMF Frequency (Hz)	Tone Output Frequency (Hz)	% Deviation
Low Group f_L	697	693.750	−0.47
	770	768.750	−0.16
	852	853.125	+0.13
	941	937.500	−0.37
High Group f_H	1209	1209.375	+0.03
	1336	1340.625	+0.35
	1477	1481.250	+0.29
	1633	1631.250	−0.11

TABLE IV. Functional Truth Table for DTMF Dialing

Keyboard Equivalence	BCD Inputs				DTMF Enable Bit 4	DTMF Output	
	Bit 3	Bit 2	Bit 1	Bit 0		f_L(Hz)	f_H(Hz)
x	x	x	x	x	0	0	0
1	0	0	0	1	1	697	1209
2	0	0	1	0	1	697	1336
3	0	0	1	1	1	697	1477
4	0	1	0	0	1	770	1209
5	0	1	0	1	1	770	1336
6	0	1	1	0	1	770	1477
7	0	1	1	1	1	852	1209
8	1	0	0	0	1	852	1336
9	1	0	0	1	1	852	1477
0	1	0	1	0	1	941	1336
*	1	0	1	1	1	941	1209
#	1	1	0	0	1	941	1477
A	1	1	0	1	1	697	1633
B	1	1	1	0	1	770	1633
C	1	1	1	1	1	852	1633
D	0	0	0	0	1	941	1633

TEST MODES

The TP3330 provides several test modes to allow the user or the CPU to verify that the modem is operating properly.

Analog Loopback

In the Analog Loopback mode, the receive bandpass filter and demodulator are configured to process the same channel as the transmitter. The transmitted carrier output is looped back to the receiver input via an internal attenuator, while still maintaining the modulated carrier to the output pin TXA.

Digital Loopback

When the Digital Loopback mode is enabled, the digital output of the demodulator is looped back to the digital input of the modulator. At 1200/600 BPS, the recovered clock of the receiver is also looped back internally to the transmit clock. The serial data input to the receive shift register of the USART is clamped to logic high, and the transmit data from the USART is ignored.

Remote Digital Loopback

The TP3330 supports Remote Digital Loopback by providing the Dotting Pattern detector for the originator. A Dotting Pattern Generator and an unscramble mark detector are provided for the remote modem for the handshaking process.

USART Digital Loopback

This test mode allows the user to test the USART's functions and interrupt system independently of the rest of the circuit. In this test mode, the serial data output from the transmit shift register is looped internally to the serial data input of the receive shift register. The data input from the demodulator is ignored. The four modem control bits (RTS, DTR, OUT1 and OUT2) are internally connected to the four modem status bits (CTS, DSR, RI and CD).

Functional Description (Continued)

USART

The on-chip USART performs serial-to-parallel conversion on data characters received from the line and parallel-to-serial conversion on data characters received from the CPU. Status information on error conditions (parity, overrun, framing or break interrupt) is provided to the CPU at any time during the functional operation. In asynchronous transmission, the USART is functionally equivalent to National's INS8250A UART, providing start-stop framing to the data. In synchronous transmission, the programmable synchronous characters are transmitted at the beginning or during data transmission in order to achieve synchronization.

ACCESSIBLE REGISTERS

The operation of TP3330 is programmable via the internal accessible registers. Table V summarizes those registers which are used to control and monitor the modem's operation. The registers listed in Table VI are used to control the USART's operations in data transfer and monitor the error conditions.

Modem Control Register 1

This register specifies the general operating conditions for the TP3330.

Bit 0: In combination with Bit 1, this bit selects the data rate of transmission.

Bit 1	Bit 0	Data Rate
0	0	1200 BPS DPSK
0	1	300 BPS FSK
1	0	1200 BPS DPSK
1	1	600 BPS DPSK

Bit 1: A logic low selects the Bell 212A and logic high selects the CCITT V.22 modem standard. The answer tone is automatically set to 2225 Hz for Bell 212A, and 2100 Hz for V.22.

Bits 2, 3: These 2 bits specify the threshold level for the carrier detector and call progress tone detector.

Bit 3	Bit 2	Carrier ON Threshold (dBm)	Carrier OFF Threshold (dBm)
0	0	−43	−46
0	1	−38	−41
1	0	−33	−36
1	1	−33	−36

Bits 4, 5: These 2 bits specify the nominal transmit carrier amplitude and DTMF levels at the TXA output.

Bit 5	Bit 4	Carrier (mVrms)	DTMF V_L/V_H (mVrms)
0	0	550	615/775
0	1	435	490/615
1	0	345	390/490
1	1	275	310/390

Bit 6: This bit selects the guard tone frequency to be transmitted along with the DPSK high band carrier when TP3330 is operating at V.22 mode. A logic low selects 1800 Hz, and a logic high selects 550 Hz.

Bit 7: A logic 0 for this bit selects the Asynchronous transmission with start-stop bits. A logic 1 selects the Synchronous transmission mode. At 300 BPS, this bit is ignored and transmission is always in Asynchronous mode only.

Dialing Control Register

This register controls the operation of TP3330 in the DTMF dialing mode.

Bits 0–3: These bits specify a 4 bit BCD digit defined in Table IV. The di it is decoded to generate the corresponding DTMF tone pair.

TABLE V. Summary of Modem Registers

AL3	1	1	1	1	1
A0–A2	0	1	2	2	3
	Modem Control Register 1	Dialing Control Register	Handshake Control Register (Write Only)	Modem Status Register 1 (Read Only)	Test Mode Register
Bit	MCR1	DCR	HCR	MSR1	TMR
0	LOW/$\overline{\text{HIGH}}$ Speed	DTMF No Bit 0	Transmit Output Enable	Receive Speed Indicator $\overline{1200}$/300 BPS	Power Up Enable
1	$\overline{\text{Bell 212A}}$/ V.22	DTMF No Bit 1	Transmit Scrambler Enable	2225 Hz/High Band Unscrambled Mark Detect	ALB Enable
2	Carrier Threshold Select	DTMF No Bit 2	Guard Tone Enable	Scrambled Mark Detect	DLB Enable
3	Carrier Threshold Select	DTMF No Bit 3	Answer Tone Enable	Low Band Unscrambled Mark Detect	0
4	Level Adjust	DTMF Enable	EXO Enable	Dotting Pattern Detect	0
5	Level Adjust	Enable Call Progress Tone Detect	EXI Enable	0	0
6	Guard Tone Select	Receive Mute Enable	ORIG/$\overline{\text{ANS}}$ Mode Select	0	0
7	$\overline{\text{ASYNC}}$/ SYNC Select	Hook Switch Control	Dotting Pattern Enable	0	0

TABLE VI. Summary of USART Registers

AL3	0	0	0	0	0	X	0	0	0	1	1	1
A0–2	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	3	4	5	6	7	5	6	7
	Receive Buffer Register (Read Only)	Transmit Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	Line Control Register 1	Modem Control Register 2	Line Status Register	Modem Status Register 2	Scratch Pad Register	Line Control Register 2	Sync Character Register 1	Sync Character Register 2
Bit	RBR	THR	IER	IIR	LCR 1	MCR2	LSR	MSR2	SCR	LCR2	SYNC1	SYNC2
0	Data Bit 0	Data Bit 0	Enable Receive Data Ready Interrupt	0 If Interrupt Pending	Word Length Bit 0	Data Terminal Ready (DTR)	Receive Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Transmit Enable	Bit 0	Bit 0
1	Data Bit 1	Data Bit 1	Enable Transmit Holding Register Empty Interrupt	Interrupt ID Bit 0	Word Length Bit 1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Receive Enable	Bit 1	Bit 1
2	Data Bit 2	Data Bit 2	Enable Line Status Interrupt	Interrupt ID Bit 1	Stop Bit Select (ASYNC Mode)	OUT 1 (Reset)	Parity Error (PE)	Trailing Edge of Ring Indicator (TERI)	Bit 2	Sync Character Select	Bit 2	Bit 2
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt	Interrupt ID Bit 2	Parity Enable	OUT 2 (INTR Output Enable)	Framing Error (FE)	Delta Carrier Detect (DCD)	Bit 3	Int/Ext Syndet Select	Bit 3	Bit 3
4	Data Bit 4	Data Bit 4	0	0	Even Parity	Loop	Break Interrupt (ASYNC)/ SYNDET (SYNC)	Clear to Send (CTS)	Bit 4	Ext Syndet Input	Bit 4	Bit 4
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	THRE Empty	Data Set Ready (DSR)	Bit 5	Enter Hunt	Bit 5	Bit 5
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	TEMT	Ring Indicator (RI)	Bit 6	Slave Timing Enable	Bit 6	Bit 6
7	Data Bit 7	Data Bit 7	0	0	DLAB	AL3	0	Carrier Detect (CD)	Bit 7	0	Bit 7	Bit 7

Note: Bit 0 is the least significant bit.
It is the first bit serially transmitted or received.

Functional Description (Continued)

Bit 4: When this bit is set to logic 1, the DTMF generator is enabled.

Bit 5: When set to logic 1, the Call Progress Tone Detector is enabled. Bit 7 (CD) of Modem Status Register 2 indicates the presence (logic 1) or absence (logic 0) of call progress tones within the passband of 350 Hz to 620 Hz. After ringback tone is detected by the CPU, Bit 5 should be reset to logic 0, putting the TP3330 in normal data mode.

Bit 6: A logic high for this bit mutes the receiver buffer amplifier. Muting is useful during pulse dialing to prevent transient overloading of the receiver.

Bit 7: This bit controls the $\overline{HS}$ output signal for hookswitch control, and can be used for pulse dialthrough by setting and resetting this bit with the right timing. The following table shows the timing requirement for pulse dialing in North America.

Pulsing Rate	8 to 11	pps
Percentage Break	58 to 64	%
Inter-Digital Pause	0.6 to 1	Sec

Handshaking Control Register

This register controls the handshaking process of the TP3330.

Bit 0: A logic high enables the transmission of carrier or DTMF signals at the TXA output. A logic low will set TXA at the V_{CM} voltage.

Bit 1: When this bit is set to logic 1, it enables the scrambler circuit inserted in the data path for the DPSK modulator. Setting this bit low bypasses the scrambler.

Bit 2: A logic high enables the transmission of the guard tone frequency selected by Bit 6 of the Modem Control Register 1. The carrier amplitude is automatically reduced by about 1 dB in order to maintain the same total transmitted power output.

Bit 3: A logic high enables the transmission of the modem answer tone, which is 2225 Hz for Bell 212A, or 2100 Hz for V.22.

Bit 4: A logic high enables the receiver audio output at EXO. When disabled by a logic low, the EXO output is set to V_{CM} voltage.

Bit 5: A logic high enables the external audio input at EXI to the line driver amplifier.

Bit 6: A logic high selects the originating mode. The TP3330 transmits at the low band and receives at the high band frequency. A logic low selects the answer mode, transmitting at the high band and receiving at the low band frequency.

Bit 7: A logic high enables the transmission of the Dotting Pattern (scrambled alternating one's and zero's) for the handshaking process required to initialize a Remote Digital Loopback for 600 BPS or 1200 BPS. Bit 1 must also be set to logic 1 to enable the transmitter's scrambler.

Modem Status Register 1

This register provides status information regarding the incoming received signal from the phone line. When the Modem Status Interrupt is enabled, the low to high transition of the status bits in this register will generate an interrupt output at INTR. It is reset by a read operation on the Modem Status Register 1.

Bit 0: This status bit is the received data speed indicator for the Bell 212A answering mode only. A logic low indicates receiving at 1200 BPS, while a logic high indicates receiving at 300 BPS. Bit 0 is reset to logic 0 whenever CD (Bit 7 of MSR2) changes from logic 1 to logic 0.

Bit 1: This bit is the answer tone indicator. It goes high whenever a 2225 Hz answer tone or high band unscrambled mark has been received for more than 160 ms during handshaking.

Bit 2: This bit is the DPSK scrambled mark indicator. It goes high whenever a scrambled mark is received for 267 ms. (t_{SM})

Bit 3: This bit is the Low band DPSK unscrambled mark indicator. It goes high when an unscrambled mark is detected for more than 160 ms.

Bit 4: This bit is the Dotting Pattern indicator. It goes high whenever a pattern of DPSK scrambled alternating 1's and 0's are received for 267 ms, indicating that a Remote Digital Loopback is being acknowledged by the far end modem.

Bits 5,6,7: These bits are not used.

Note: Bits 1 to 4 are reset to logic 0 whenever the CPU reads the content of the Modem Status Register 1.

Test Mode Register

This register programs the modes of operation of the TP3330.

Bit 0: When this bit is programmed to logic low, the TP3330 is put in the power-down mode, minimizing current consumption. All non-essential circuits are de-activated, analog outputs TXA and EXO are TRI-STATE and the digital output $\overline{HS}$ is at inactive state. The internal registers are unaffected, and the $\overline{RI}$ input and its associate interrupt function as normal. When power is first applied to TP3330, the user should program a logic high in Bit 0 to set the device in the power-up mode.

Bit 1: A logic high enables the Analog Loopback test mode.

Bit 2: A logic high enables the Digital Loopback test mode.

Bits 3–7: These bits are not used, and should be set to logic 0.

Functional Description (Continued)

Line Control Register 1

The Line Control Register 1 specifies the format of asynchronous data communication. The programmer may retrieve the contents of both Line Control Registers for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory.

Bits 0,1: These 2 bits specify the number of data bits in each transmitted or received serial character. In the asynchronous mode for 1200 BPS/600 BPS, the sync-to-async converter allows 8, 9, 10, or 11 character length (start bit + data bits + parity bit + stop bits), the selections for word length, parity bit and stop bits must be matched to these requirements. Table VII shows the valid combinations for character lengths.

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted character for asynchronous communication. If Bit 2 is a logic 0, one stop bit is generated in the transmitted data. If Bit 2 is a logic 1 when a 5-bit word length is selected via Bits 0 and 1, one and a half stop bits are generated. If Bit 2 is a logic 1 when either a 6-, 7- or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.

Bit 3: This is the Parity Enable bit. When Bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data.

Bit 4: This is the Even Parity Select bit. When Parity is enabled via Bit 3, a logic 0 at Bit 4 selects the Odd Parity and a logic 1 selects the Even Parity.

Bit 5: This is the Stick Parity select bit. When Parity is enabled via Bit 3, a logic 1 at Bit 5 enables the Stick Parity. If Bit 4 is a logic 1, the Parity bit is transmitted and checked by the receiver as a logic 0. If Bit 4 is a logic 0, then the Parity bit is transmitted as a logic 1.

Bit 6: This is the Break Control bit. When it is set to a logic 1, the serial output of the USART is forced to the Spacing (logic 0) state. The break is disabled by resetting bit 6 to a logic 0.

Note: To prevent any erroneous characters being transmitted because of the break, the following sequence is recommended:

1. Load an all 0's pad character in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle (TEMT = 1) and clear break when normal transmission has been restored.

Bit 7: This bit is the Access Bit (DLAB). It must be set to logic 0 to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

Line Control Register 2

The Line Control Register 2 specifies the format of Synchronous transmission.

Bit 0: A logic 1 enables the transmitter of the USART. Data begins to shift serially into the modulator circuit. A logic 0 disables the transmitter of the USART, and the serial data input to the modulator is clamped at logic high. When disabled while the modem is in operation, all the data that was previously loaded into the USART will be transmitted before the USART is shut down.

Bit 1: A logic high enables the receiver of the USART.

Bit 2: A logic low at this input selects double synchronization characters to be transmitted or received. A logic high selects single synchronization character.

Bit 3: A logic high at this input selects the external sync-detect mode. A logic low selects the internal sync-detect mode.

Bit 4: This bit is the External Sync-detect Input. When external sync-detect mode is selected via Bit 3, synchronization is achieved by applying a logic high at Bit 4, which forces the USART to exit the Hunt mode and start assembling serial data into the parallel format.

Bit 5: When Bit 5 is set to logic high, the Hunt mode is enabled. If internal sync-detect mode is programmed by Bit 3, the received data in the buffer register is compared at each bit boundary with the first sync character until a match is found. If the USART is programmed for double sync characters, the subsequent character is also compared. If both sync characters are detected, the USART exits the Hunt mode and is in synchronization.

Bit 6: A logic high selects the Slave Timing mode for Synchronous Transmission. The transmit clock is phase-locked to the recovery clock of the DPSK demodulator.

Bit 7: This bit is always at logic 0.

Sync-Character Registers 1,2

Bits 0–7: These registers are used to store the programmable synchronization characters for insertion at the beginning of, or during the transmission of synchronous messages. If the CPU does not respond to the TEMT and the USART is programmed for single sync-character, the content of Sync-Character Register 1 will be transmitted before the normal data transmission resumes. If dual sync-characters are being programmed, the contents of both Sync-Character Registers 1 and 2 will be transmitted.

Functional Description (Continued)

TABLE VII. Asynchronous Character Formats for 600/1200 BPS

Bit 2	Bit 3	Bit 1	Bit 0	Character Length (Bits)								
				Start	+	Data	+	Parity	+	Stop		
0	0	0	1	1	+	6	+	0	+	1		= 8
0	0	1	0	1	+	7	+	0	+	1		= 9
0	0	1	1	1	+	8	+	0	+	1		= 10
0	1	0	0	1	+	5	+	1	+	1		= 8
0	1	0	1	1	+	6	+	1	+	1		= 9
0	1	1	0	1	+	7	+	1	+	1		= 10
0	1	1	1	1	+	8	+	1	+	1		= 11
1	0	0	1	1	+	6	+	0	+	2		= 9
1	0	1	0	1	+	7	+	0	+	2		= 10
1	0	1	1	1	+	8	+	0	+	2		= 11
1	1	0	1	1	+	6	+	1	+	2		= 10
1	1	1	0	1	+	7	+	1	+	2		= 11

Line Status Register

The Line Status Register provides status information to the CPU concerning the data transfer. It is intended for read operation only, writing to this register is not recommended.

Bit 0: This is the Receive Data Ready (DR) indicator. It is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receive Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receive Buffer Register.

Bit 1: This is the Overrun Error (OE) indicator. A logic 1 at Bit 1 indicates that data in the Receive Buffer Register was not read by the CPU before the next character was transferred into the Receive Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This is the Parity Error (PE) indicator. Bit 2 is set to a logic 1 whenever the received data character does not have the correct even or odd parity, as selected by the parity select bit. It is reset to logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid stop bit. It is set to a logic 1 whenever the stop bit following the last data bit or parity bit is at the spacing level. Bit 3 is reset whenever the CPU reads the contents of the Line Status Register.

Bit 4: When asynchronous transmission is selected, this bit is the Break Interrupt (BI) indicator. It is set to a logic 1 whenever the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits). When Synchronous transmission is selected, this bit is the sync-detect indicator. It is set to logic 1 whenever the USART detects a valid sync-character (or two consecutive sync-characters when in dual sync mode). Bit 4 is reset whenever the CPU reads the contents of the Line Status Register.

Note: Bits 1 through 4 are the error conditions that produce a receiver Line Status Interrupt whenever any of the corresponding conditions is detected.

Bit 5: This is the Transmitter Holding Register Empty (THRE) indicator. It is set to logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register, indicating that the USART is ready to accept a new character for transmission. It also issues an interrupt to the CPU if the Transmitter Holding Register Empty Interrupt is enabled. Bit 5 is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This is the Transmitter Empty (TEMT) indicator. It is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Interrupt Enable Register

This register enables the 4 types of interrupts to separately activate the Interrupt (INTR) output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Enable Register. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTR output from the device. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The interrupt output signal can be put into TRI-STATE by resetting Bit 3 of the Modem Control Register 2 to logic 0.

Bit 0: A logic 1 enables the Received Data Available Interrupt.

Bit 1: A logic 1 enables the Transmitter Holding Register Empty Interrupt.

Bit 2: A logic 1 enables the Line Status Interrupt.

Bit 3: A logic 1 enables the Modem Status Interrupt (Interrupt sourced from either Modem Status Register 1 or 2).

Bits 4–7: These four bits are always at logic 0.

Interrupt Identification Register

Information indicating that a prioritized interrupt is pending and the type of that interrupt is stored in the Interrupt Identification Register (IIR). In order to provide minimum software

Functional Description (Continued)

overhead during data transfer, the TP3330 prioritizes interrupts into five levels. When addressed during chip-select time, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When Bit 0 is a logic 0, an interrupt is pending and the IIR content may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1–3: These 3 bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table VIII.

Bits 4–7: These 4 bits of the IIR are always at logic 0.

Modem Control Register 2

This register controls the modem interface with the TP3330.

Bit 0: This bit is the Data Terminal Ready indicator. A logic high indicates that the CPU is ready for data transfer. When Bit 0 is reset from a high to low state for more than 50 ms, a loss of DTR disconnect sequence is generated.

Bit 1: This bit is the Request to Send indicator. It is not used by the TP3330.

Bit 2: This bit is the Output 1 (OUT1) signal. It is internally connected to generate a Master Reset to the TP3330 when this bit is set to a logic 1. During normal operation, this bit must be kept at logic low.

Bit 3: This bit is the Output 2 (OUT2) signal. When Bit 3 is set to logic 0, it is internally connected to disable the interrupt (INTR) output signal, and INTR is in TRI-STATE. Bit 3 should be set to logic 1 to enable the Interrupt output line.

TABLE VIII. Interrupt Control Functions

Interrupt Identification Register					Interrupt Set and Reset Functions		
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun, or Parity, or Framing Error, or Break Interrupt, or Sync-Detect	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register, (If Source of Interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	Modem Status	Clear to Send, Data Set Ready, Ring Indicator, Carrier Detect, Call Progress Tone Detect	Reading the Modem Status Register 2
1	0	0	0	Fifth	Modem Status	2225 Hz Answer Tone, Scrambled 1, Unscrambled 1, Receive Speed, Dotting Pattern Detected	Reading the Modem Status Register 1

Functional Description (Continued)

Bit 4: A logic 1 enables the USART Digital Loopback test mode. It should be reset to logic 0 for normal data transfer.

Bits 5,6: These bits are permanently set to logic 0.

Bit 7: This is the Address Select Bit for the internal registers of TP3330. (Refer to Tables V and VI.)

Modem Status Register 2

This register provides information on the current state of the interface control signals from the modem to the CPU.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. A logic 1 indicates that the Clear to Send (CTS) status bit has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the Data Set Ready status bit has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the device has changed from a low to a high state.

Bit 3: This bit is the Delta Carrier Detect (DCD) indicator. Bit 3 indicates that the Carrier Detect or Call Progress Tone Detect (CD) indicator has changed state.

Bit 4: This bit is the Clear to Send Indicator. It goes to a logic 1 when the TP3330 completes the modem handshaking process, and is ready for data transfer. When Bit 4 (Loop) of the MCR2 is set to a logic 1, this bit is equivalent to RTS in the MCR2.

Bit 5: This bit is the Data Set Ready indicator. Bit 4 indicates to the CPU that the TP3330 is ready. It is set to logic 1 when the TP3330 is in power up mode, and reset to logic 0 when the device is powered down. When Bit 4 of the MCR2 is set to a logic 1, this bit is equivalent to DTR of the MCR2.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If Bit 4 of the MCR2 is set to a logic 1, this bit is equivalent to OUT1 in the MCR2.

Bit 7: This bit is the Carrier Detect (CD) indicator. A logic 1 indicates that a valid carrier signal exceeding the pre-selected threshold level is received for a period exceeding t_{CDON}. When the Call Progress Tone Detector is enabled by setting Bit 5 of the Dialing Control Register, Bit 7 indicates the presence of the call progress tones within the passband of 350–620 Hz. When Bit 4 of the MCR is set to a logic 1, this bit is equivalent to OUT2 of the MCR2.

Scratchpad Register

This 8-bit Read/Write register is intended as a scratchpad register to be used by the programmer to hold data temporarily. It does not control the device's function in any way.

Typical Application

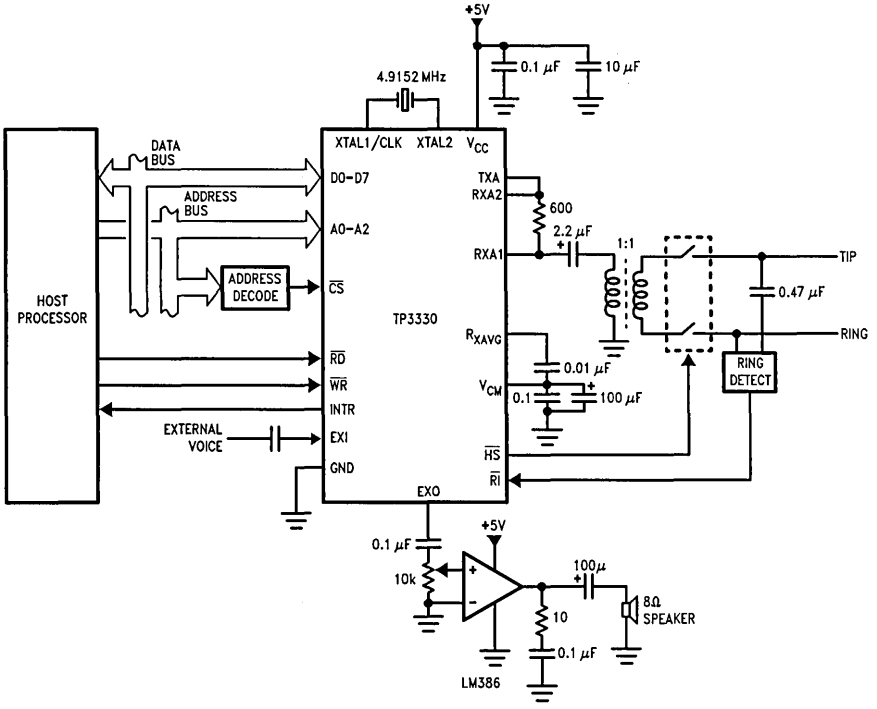

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FIGURE 2. Typical Application for an Integral Modem

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Operating Temperature Range	−25°C to +80°C
Storage Temperature Range	−65°C to +150°C
V_{CC} with Respect to GND	+7V
Voltage at Any Input	V_{CC} + 0.3V to GND − 0.3V
Voltage at Any Output	V_{CC} + 0.3V to GND − 0.3V
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

ESD Rating is to be determined

DC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.7	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = +1.0 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.1 mA	2.4			V
I_{IL}	Input Low Current All Digital Inputs	GND < V_{IN} < V_{IL}	−10		10	μA
I_{IH}	Input High Current All Digital Inputs	V_{IH} < V_{IN} < V_{CC}	−10		10	μA
I_{OZ}	TRI-STATE® Output Leakage Current	D0–D7, INTR, GND < V_O < V_{CC}	−20		20	μA
$I_{CC}0$	Power-Down Current	Outputs Open		0.4		mA
$I_{CC}1$	Power-Up Current	Outputs Open		30		mA

AC Electrical Characteristics (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMITTER						
V_{OXA}	Output Level at TXA	V_{CC} = 5.0V, R_{LXA} = 1.2 kΩ Bit 4, 5 of MCR1 = 0 High Band Carrier 2100/2225 Hz Answer Tone 550/1800 Hz Guard Tone DTMF, High Group DTMF, Low Group		 550 550 275 775 615		 mVrms mVrms mVrms mVrms mVrms
P_E	DTMF High Group Pre-Emphasis		1.0	2.0	3.0	dB
V_{OS}	Mean Output DC Offset Voltage at TXA	V_{CC} = 5.0V		2.5		V
E_{OX}	Out-of-Band Spectral Density Reference to Carrier	3.4 kHz < f < 8 kHz 8 kHz < f < 256 kHz		−45 −65		dB dB
THD	DTMF Distortion	V_{CC} = 5.0V, R_{LXA} = 1.2 kΩ, 300 Hz–3.4 kHz	−20			dB
G_{XI}	Voltage Gain from EXI to TXA	Input = 100 mVrms, f = 1 kHz Bit 5 of HCR = 1	dB	9.5		
R_{OXA}	Output Dynamic Resistance		Ω	1		
R_{LXA}	Load Resistance		1	1.2		kΩ
C_{LXA}	Load Capacitance				100	pF

Note 1: Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, GND = 0V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at V_{CC} = 5.0V, T_A = 25°C.

Note 2: All tests on AC parameters of Transmitter and Receiver are based on test circuit shown in *Figure 3.*

Note 3: 0 dBm into 600Ω = 0.775 Vrms.

Note 4: Crystal specification: Parallel Resonant 4.9152 MHz, R_S < 150Ω, L = 67.6 MH, C_M = 0.015 pF, C_H = 5 pF.

AC Electrical Characteristics (Note 1) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER						
R_{RIN}	Input Resistance	From RXA1 to GND		10		kΩ
		From RXA2 to GND		100		kΩ
S_R	Input Signal Level		−43		−12	dBm
TH_{CD}	Carrier Detect Threshold	Bits 3, 2 or MCR1 = 0, 0 ON		−43		dBm
		OFF		−46		dBm
		Bits 3, 2 of MCR1 = 0, 1 ON		−38		dBm
		OFF		−41		dBm
		Bits 3, 2 of MCR1 = 1, 0 ON		−33		dBm
		OFF		−36		dBm
H_{CD}	Carrier Detect Hysteresis	Measured from TH_{CD} ON to TH_{CD} OFF	2	3	5	dB
I_D	Peak Intersymbol Distortion (Isochronous ± Bias)	Back-to-Back, Received Level at −12 dBm, 300 BPS, 511-Bit Pattern		5		%
BER	Bit Error Rate	Back-to-Back, with Additive 300 Hz–3.4 kHz Flat Noise, Received Level at −12 dBm 511-Bit Pattern				
		300 BPS, S/N = 5 dB		10^{-5}		
		600 BPS, S/N = 10 dB		10^{-6}		
		1200 BPS, S/N = 12 dB		10^{-6}		
G_{RO}	Voltage Gain from RXA1 to EXO	Input = 200 mVrms, f = 1 kHz Bit 4 of HCR = 1		6		dB
R_{LEXO}	Load Resistance at EXO		10			kΩ
C_{LEXO}	Load Capacitance at EXO				100	pF
t_{CDON}	Carrier Detector Acquisition Time	300 BPS	100	160	200	ms
		600/1200 BPS				
		Originating Mode	230	267	310	ms
		Answering Mode	755	765	775	ms
t_{CDOFF}	Carrier Detector Release Time		10	17	24	ms
t_{PDON}	Call Progress Tone Detector Acquisition Time	350 Hz < f < 620 Hz		40		ms
t_{PDOFF}	Call Progress Tone Detector Release Time	350 Hz < f < 620 Hz		40		ms
t_{CTSON}	CTS ON Acquisition Time	300 BPS,				
		Originating Mode	755	765	775	ms
		Answering Mode	100	160	200	ms
		600 BPS/1200 BPS,				
		Originating/Answering Mode	755	765	775	ms
t_{DTRD}	Loss of DTR Disconnect Time	From DTR OFF to CD or CTS OFF	57	68	77	ms
t_{CDD}	Loss of Carrier Disconnect Time	From CD OFF to CTS OFF	405	415	425	ms

Note 1: Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, GND = 0V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at V_{CC} = 5.0V, T_A = 25°C.

AC Electrical Characteristics (Note 1) (Continued)

Symbol	Parameter	Conditions	Min	Max	Units
BUS TIMING READ CYCLE					
t_{SCR}	Chip Select Setup before $\overline{RD}$		50		ns
t_{HRC}	Chip Select Hold Time after $\overline{RD}$		20		ns
t_{SAR}	Address Setup before $\overline{RD}$		60		ns
t_{HRA}	Address Hold Time after $\overline{RD}$		20		ns
t_{WRD}	$\overline{RD}$ Pulse Width		125		ns
t_{DRD}	Data Delay from $\overline{RD}$	C_L = 100 pF		125	ns
t_{ZRD}	$\overline{RD}$ Invalid to Data Floating	C_L = 100 pF	0	100	ns
t_{RC}	Read Cycle Time		360		ns
WRITE CYCLE					
t_{SCW}	Chip Select Setup before $\overline{WR}$		50		ns
t_{HWC}	Chip Select Hold Time after $\overline{WR}$		20		ns
t_{SAW}	Address Setup before $\overline{WR}$		60		ns
t_{HWA}	Address Hold Time after $\overline{WR}$		20		ns
t_{WWR}	$\overline{WR}$ Pulse Width		100		ns
t_{SDW}	Data Set Up before $\overline{WR}$		40		ns
t_{HWD}	Data Hold Time after $\overline{WR}$		40		ns
t_{WC}	Write Cycle Time		360		ns

Note 1: Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, GND = 0V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at V_{CC} = 5.0V, T_A = 25°C.

Note 2: All tests on AC parameters of Transmitter and Receiver are based on test circuit shown in *Figure 3.*

Note 3: 0 dBm into 600Ω = 0.775 Vrms

Note 4: Crystal specification: Parallel Resonant 4.9152 MHz, R_S < 150Ω, L = 67.6 mH, C_M = 0.015 pF, C_H = 5 pF.

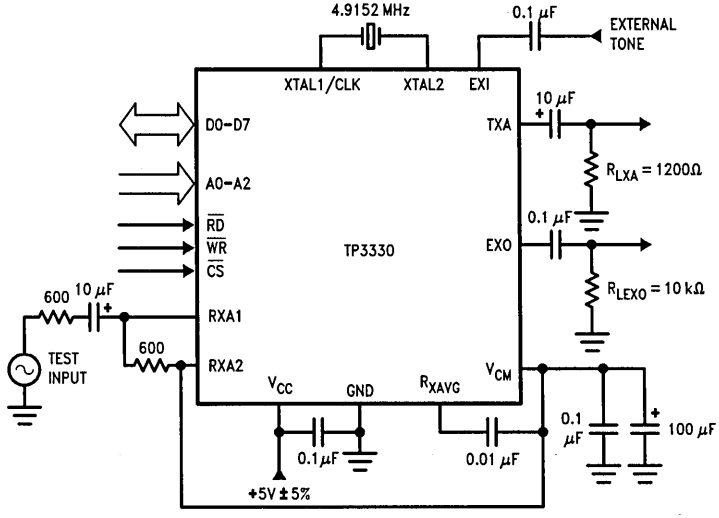

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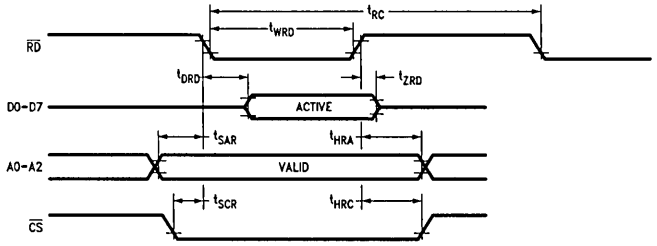
FIGURE 3. AC Test Circuit

Timing Waveforms

READ CYCLE



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WRITE CYCLE

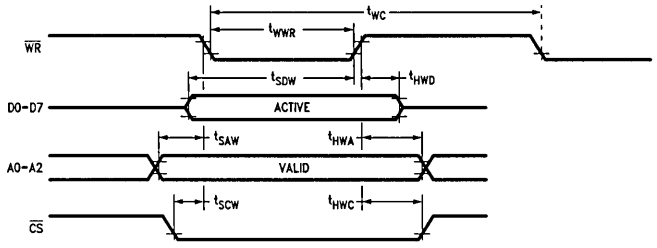

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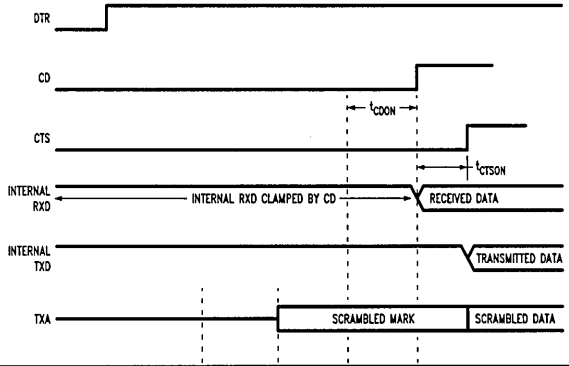
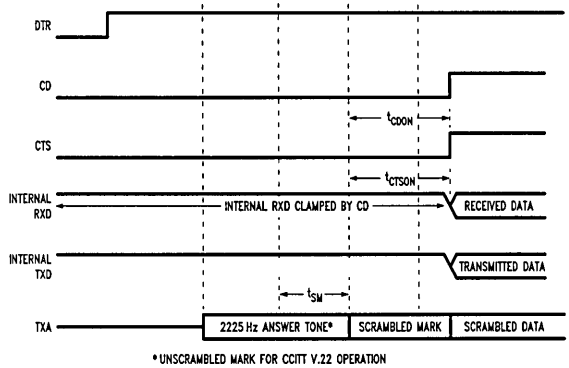
FIGURE 4. Data Bus Timing Diagram

ORIGINATING MODEM



ANSWERING MODEM



*UNSCRAMBLED MARK FOR CCITT V.22 OPERATION

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FIGURE 5. TP3330 Configured in Bell 212A 1200 BPS Mode

Timing Waveforms (Continued)

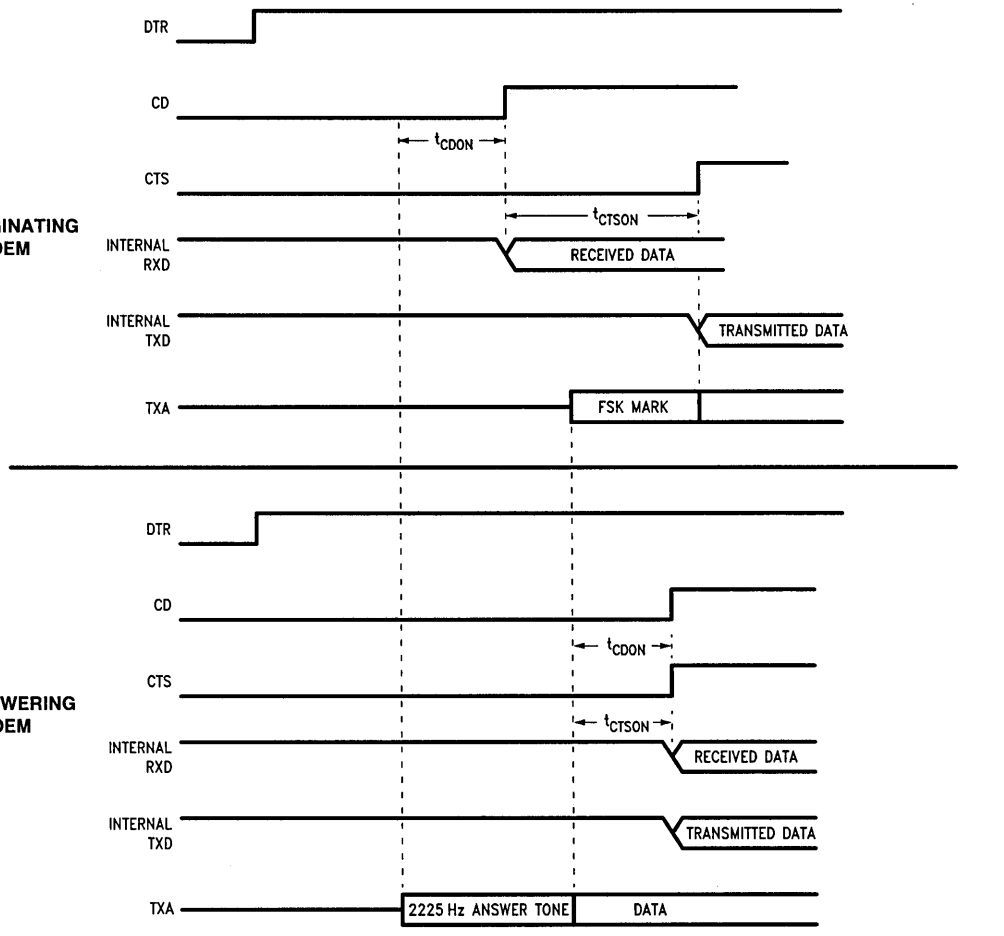

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FIGURE 6. TP3330 Configured in Bell 212A 300 BPS Mode

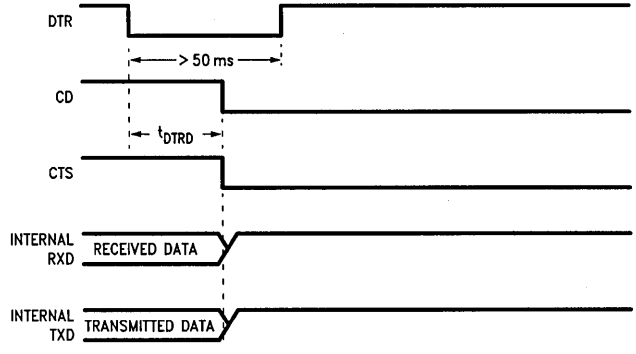

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FIGURE 7. Loss of DTR Disconnect Sequence

Timing Waveforms (Continued)

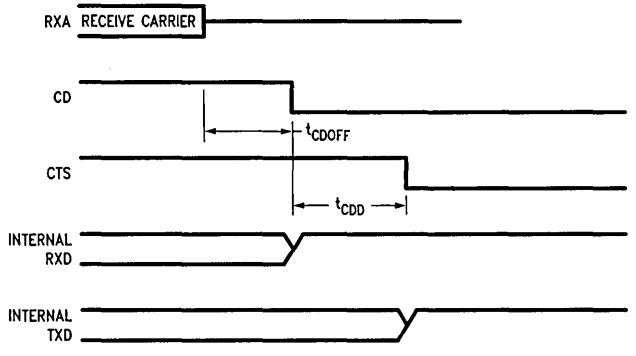

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FIGURE 8. Loss of Carrier Disconnect Sequence

National Semiconductor Corporation

PRELIMINARY

microCMOS

TP7515 Full Modem Duplex 1200 Baud Bell 212A/V.22 Serial Modem

General Description

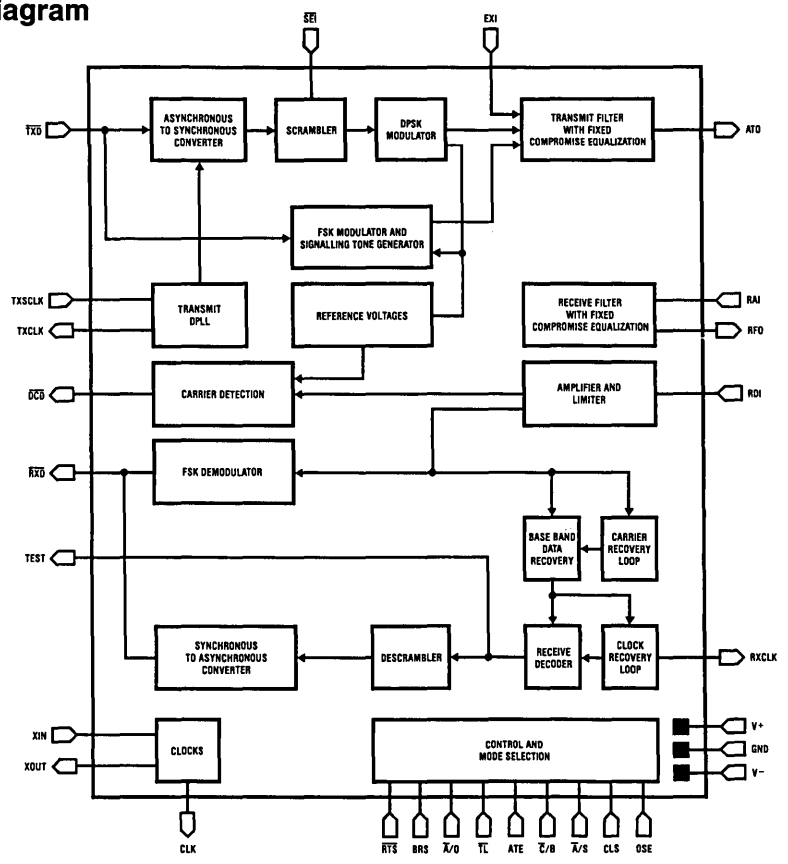
The TP7515 is a complete general purpose monolithic DPSK and FSK modem implemented in microCMOS process technology. It may be configured to either generate and receive phase modulated signals at data rates of 1200 bits per second or 600 bits per second or frequency modulated signals at data rates up to 300 bits per second on voice grade telephone lines. It is capable of operating to meet three pin selectable standards; CCITT V.22 A/B, Bell 212A and its low speed mode, or Bell 103.

All filtering functions required for frequency generation, out of band noise rejection and demodulation are performed by on-chip switched-capacitor filters. In phase modulation mode, the modem provides all data buffering and scrambling function necessary for bit synchronous format and asynchronous character format modes of operation. Internal frequencies are generated from a 4.9152 MHz crystal reference.

Features

- Meets popular 1200 bps full duplex specifications:
  - CCITT V.22
  - Bell 212A
  - Bell 103
- Includes all filtering
- Serial data interface
- Answer tone selection
- Synchronous/Asynchronous selection
- Channel selection (answer/originate)
- Low speed mode selection
- Low power CMOS, ±5V power supplies
- 28-pin dual in-line or surface mount package

Block Diagram



TL/H/9244–1

Section 4

Analog Telephone Components

Section 4 Contents

National Semiconductor Corporation

PRELIMINARY

TP5088 DTMF Generator for Binary Data

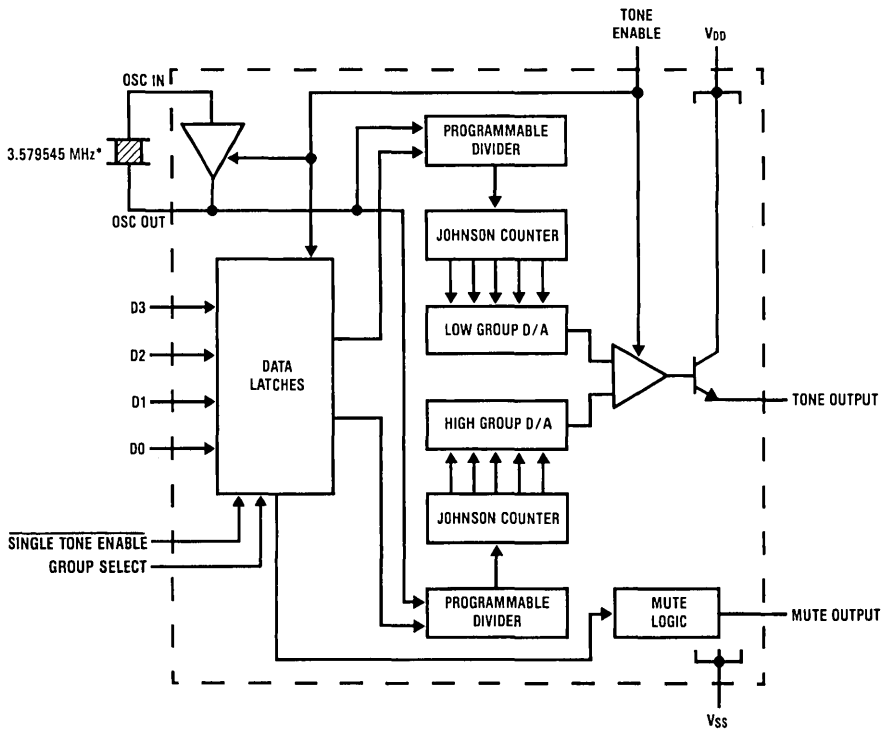
General Description

This CMOS device provides low cost tone-dialing capability in microprocessor-controlled telephone applications. 4-bit binary data is decoded directly, without the need for conversion to simulated keyboard inputs required by standard DTMF generators. With the TONE ENABLE input low, the oscillator is inhibited and the device is in a low power idle mode. On the low-to-high transition of TONE ENABLE, data is latched into the device and the selected tone pair from the standard DTMF frequencies is generated. An open-drain N-channel transistor provides a MUTE output during tone generation.

Features

- Direct microprocessor interface
- Binary data inputs with latches
- Generates 16 standard tone pairs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Better than 0.64% frequency accuracy
- High group pre-emphasis
- Low harmonic distortion
- MUTE output interfaces to speech network
- Low power idle mode
- 3.5V–8V operation

Block Diagram



TL/H/5004–1

*Crystal Specification: Parallel Resonant 3.579545 MHz, $R_S \leq 150\Omega$, L = 100 mH, C_0 = 5 pF, C_1 = 0.02 pF.

4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V_{DD} - V_{SS}$)	12V
$\overline{MUTE}$ Voltage	12V
Maximum Voltage at Any Other Pin	V_{DD} + 0.3V to V_{SS} − 0.3V

Operating Temperature, T_A	−30°C to +70°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation	500 mW

Electrical Characteristics

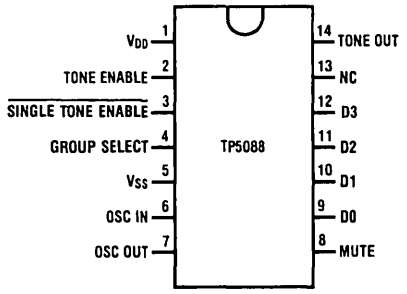
Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = 3.5V to 8V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/ or product design and characterization.

Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage, V_{DD} (min)	Generating Tones	**3.5**			V
Minimum Supply Voltage for Data Input, TONE ENABLE and MUTE Logic Functions		2			V
Operating Current					
Idle	R_L = ∞, D0–D3 Open		55	**350**	μA
Generating Tones	V_{DD} = 3.5V, Mute Open		1.5	**2.5**	mA
Input Pull-Up Resistance					
D0–D3			100		kΩ
TONE ENABLE			50		kΩ
Input Low Level					
TONE ENABLE, D0–D3				**0.2 V_{DD}**	V
Input High Level					
TONE ENABLE, D0–D3		**0.8 V_{DD}**			V
MUTE OUT Sink Current (TONE ENABLE LOW)	V_{DD} = 3.5V V_o = 0.5V	**0.4**			mA
MUTE OUT Leakage Current (TONE ENABLE HIGH)	V_{DD} = 3.5V V_o = V_{DD}		1		μA
Output Amplitudes	R_L = 240 Ω				
Low Group	V_{DD} = 3.5V	**130**	170	**220**	mVrms
High Group	T_A = 25°C	**180**	230	**310**	mVrms
Mean Output DC Offset	V_{DD} = 3.5V		1.2		V
	V_{DD} = 8V		3.6		V
High Group Pre-Emphasis		**2.2**	2.7	**3.2**	dB
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth, V_{DD} = 5V R_L = 240Ω	**−20**			dB
Start-Up Time (to 90% Amplitude), t_{OSC}			4		ms
Data Set-Up Time, t_S (*Figure 2*)	V_{DD} = 5V	100			ns
Data Hold Time, t_H	V_{DD} = 5V	280			ns
Data Duration t_W	V_{DD} = 5V	600			ns

Note 1: R_L is the external load resistor connected from TONE OUT to V_{SS}.

Connection Diagram

Dual-In-Line Package



TL/H/5004–2

Top View

Order Number TP5088M or TP5088N
See NS Package M14B or N14A

Functional Description

With the TONE ENABLE pin pulled low, the device is in a low power idle mode, with the oscillator inhibited and the output transistor turned off. Data on inputs D0–D3 is ignored until a rising transition on TONE ENABLE. Data meeting the timing specifications is latched in, the oscillator and output stage are enabled, and tone generation begins. The decoded data sets the high group and low group programmable counters to the appropriate divide ratios. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine wave cycle. On-chip regulators ensure good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with preemphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}.

Table I shows the accuracies of the tone output frequencies and Table II is the Functional Truth Table.

TABLE I. Output Frequency Accuracy

Tone Group	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	697	694.8	−0.32
	770	770.1	+0.02
	852	852.4	+0.03
	941	940.0	−0.11
High Group f_H	1209	1206.0	−0.24
	1336	1331.7	−0.32
	1477	1486.5	+0.64
	1633	1639.0	+0.37

Pin Descriptions

V_{DD} (Pin 1): This is the positive supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is also connected to this pin.

V_{SS} (Pin 5): This is the negative voltage supply. All voltages are referenced to this pin.

OSC IN, OSC OUT (Pins 6 and 7): All tone generation timing is derived from the on-chip oscillator circuit. A low-cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 6 and 7. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator is stopped when the TONE ENABLE input is pulled to logic low.

TONE ENABLE Input (Pin 2): This input has an internal pull-up resistor. When TONE ENABLE is pulled to logic low, the oscillator is inhibited and the tone generators and output transistor are turned off. A low to high transition on TONE ENABLE latches in data from D0–D3. The oscillator starts, and tone generation continues until TONE ENABLE is pulled low again.

MUTE (Pin 8): This output is an open-drain N-channel device that sinks current to V_{SS} when TONE ENABLE is low and no tones are being generated. The device turns off when TONE ENABLE is high.

D0, D1, D2, D3 (Pins 9, 10, 11, 12): These are the inputs for binary-coded data, which is latched in on the rising edge of TONE ENABLE. Data must meet the timing specifications of *Figure 2*. At all other times these inputs are ignored and may be multiplexed with other system functions.

TONE OUT (Pin 14): This output is the open emitter of an NPN transistor, the collector of which is connected internally to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group tones superimposed on a DC offset. When not generating tones, this output transistor is turned off to minimize the device idle current.

$\overline{\text{SINGLE TONE ENABLE}}$ (Pin 3): This input has an internal pull-up resistor. When pulled to V_{SS}, the device is in single tone mode and only a single tone will be generated at pin 14 (for testing purposes). For normal operation, leave this pin open-circuit or pull to V_{DD}.

GROUP SELECT (Pin 4): This pin is used to select the high group or low group frequency when the device is in single tone mode. It has an internal pull-up resistor. Leaving this pin open-circuit or pulling it to V_{DD} will generate the high group, while pulling to V_{SS} will generate the low group frequency at the TONE OUT pin.

TABLE II. Functional Truth Table

Keyboard Equivalent	Data Inputs				TONE ENABLE	TONES OUT		MUTE
	D3	D2	D1	D0		f_L (Hz)	f_H(Hz)	
X	X	X	X	X	0	0V	0V	0V
1	0	0	0	1	⎍	697	1209	O/C
2	0	0	1	0	⎍	697	1336	O/C
3	0	0	1	1	⎍	697	1477	O/C
4	0	1	0	0	⎍	770	1209	O/C
5	0	1	0	1	⎍	770	1336	O/C
6	0	1	1	0	⎍	770	1477	O/C
7	0	1	1	1	⎍	852	1209	O/C
8	1	0	0	0	⎍	852	1336	O/C
9	1	0	0	1	⎍	852	1477	O/C
0	1	0	1	0	⎍	941	1336	O/C
*	1	0	1	1	⎍	941	1209	O/C
#	1	1	0	0	⎍	941	1477	O/C
A	1	1	0	1	⎍	697	1633	O/C
B	1	1	1	0	⎍	770	1633	O/C
C	1	1	1	1	⎍	852	1633	O/C
D	0	0	0	0	⎍	941	1633	O/C

Timing Diagram

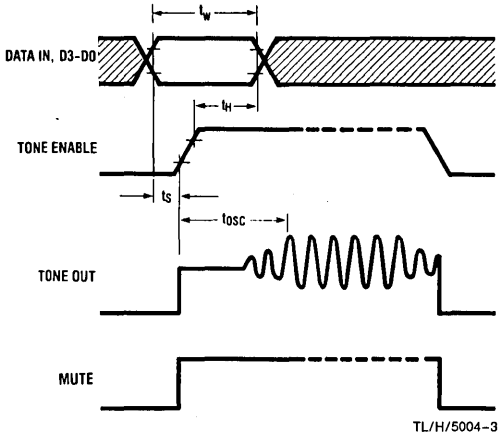
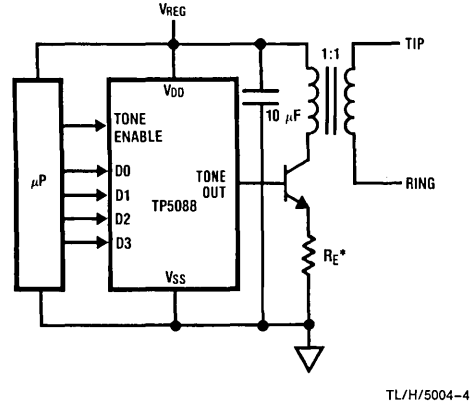


FIGURE 2

Typical Application



*Adjust R_E for desired tone amplitude.

FIGURE 3

National Semiconductor Corporation

PRELIMINARY

TP5089 DTMF (TOUCH-TONE) Generator

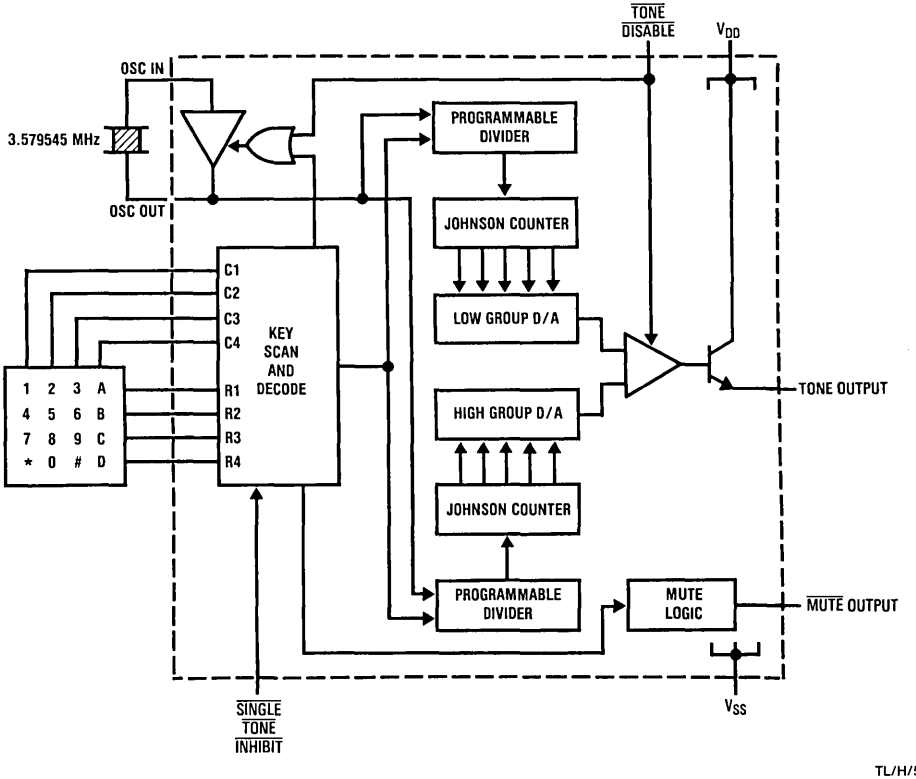
General Description

The TP5089 is a low threshold voltage, field-implanted, metal gate CMOS integrated circuit. It interfaces directly to a standard telephone keypad and generates all dual tone multi-frequency pairs required in tone-dialing systems. The tone synthesizers are locked to an on-chip reference oscillator using an inexpensive 3.579545 MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A $\overline{\text{MUTE}}$ OUT logic signal, which changes state when any key is depressed, is also provided.

Features

- 3.5V–10V operation when generating tones
- 2V operation of keyscan and $\overline{\text{MUTE}}$ logic
- Static sensing of key closures or logic inputs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Output amplitudes proportional to supply voltage
- High group pre-emphasis
- Low harmonic distortion
- Open emitter-follower low-impedance output
- $\overline{\text{SINGLE TONE INHIBIT}}$ pin

Block Diagram



TL/H/5057–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V_{DD} - V_{SS}$) 15V

Maximum Voltage at Any Pin $V_{DD} + 0.3V$ to $V_{SS} - 0.3V$

Operating Temperature −30°C to +60°C

Storage Temperature −55°C to + 150°C

Maximum Power Dissipation 500 mW

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = 3.5V to 10V, T_A = 0°C to +60°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

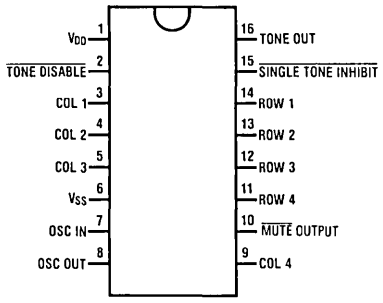
Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage for Keysense and $\overline{\text{MUTE}}$ Logic Functions		2			V
Minimum Operating Voltage for generating tones		**3.5**			V
Operating Current Idle Generating Tones	Mute open $R_L = \infty$ $V_{DD} = 3.5V$	**25** **2.5**	2 1.1		μA mA
Input Resistors COLUMN and ROW (Pull-Up) $\overline{\text{SINGLE TONE INHIBIT}}$ (Pull-Down) $\overline{\text{TONE DISABLE}}$ (Pull-Up)		 25 120	 50		 kΩ kΩ
Input Low Level				**0.2 V_{DD}**	V
Input High Level		**0.8 V_{DD}**			V
$\overline{\text{MUTE}}$ OUT Sink Current (COLUMN and ROW Active)	$V_{DD} = 3.5V$ $V_o = 0.5V$	**0.4**			mA
$\overline{\text{MUTE}}$ Out Leakage Current	$V_o = V_{DD}$		1		μA
Output Amplitude Low Group	$R_L = 240\ \Omega$ $V_{DD} = 3.5V$	**190**	250	**340**	mVrms
	$R_L = 240\Omega$ $V_{DD} = 10V$	**510**	700	**880**	mVrms
Output Amplitude High Group	$R_L = 240\Omega$ $V_{DD} = 3.5V$	**270**	340	**470**	mVrms
	$R_L = 240\Omega$ $V_{DD} = 10V$	**735**	955	**1265**	mVrms
Mean Output DC Offset	$V_{DD} = 3.5V$ $V_{DD} = 10V$		1.3 4.6		V V
High Group Pre-Emphasis		**2.2**	2.7	**3.2**	dB
Dual Tone/Total Harmonic Distortion Ratio	$V_{DD} = 4V$, $R_L = 240\Omega$ 1 MHz Bandwidth	**−22**	−23		dB
Start-Up Time (to 90% Amplitude)			3	5	mS

Note 1: R_L is the external load resistor connected from TONE OUT to V_{SS}.

Note 2: Crystal specification: Parallel resonant 3.579545 MHz, $R_S \leq 150\ \Omega$, L = 100 mH, C_O = 5 pF, C_I = 0.02 pF.

Connection Diagram

Dual-In-Line Package



TL/H/5057–2

Top View

Order Number TP5089N
See NS Package N16A

Pin Descriptions

Symbol	Description
V_{DD}	This is the positive voltage supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is connected to this pin.
V_{SS}	This is the negative voltage supply. All voltages are referenced to this pin.
OSC IN, OSC OUT	All tone generation timing is derived from the on-chip oscillator circuit. A low cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when column inputs are sensed with no valid input having been detected. The oscillator is also stopped when the $\overline{\text{TONE DISABLE}}$ input is pulled to logic low.
Row and Column Inputs	When no key is pushed, pull-up resistors are active on row and column inputs. A key closure is recognized when a single row and a single column are connected to V_{SS}, which starts the oscillator and initiates tone generation. Negative-true logic signals simulating key closures can also be used.
$\overline{\text{TONE DISABLE}}$ Input	The $\overline{\text{TONE DISABLE}}$ input has an internal pull-up resistor. When this input is open or at logic high, the normal tone output mode will occur. When $\overline{\text{TONE DISABLE}}$ input is at logic low, the device will be in the inactive mode, TONE OUT will be at an open circuit state.
$\overline{\text{MUTE}}$ Output	The $\overline{\text{MUTE}}$ output is an open-drain N-channel device that sinks current to V_{SS} with any key input and is open when no key input is sensed. The $\overline{\text{MUTE}}$ output will switch regardless of the state of the $\overline{\text{SINGLE TONE INHIBIT}}$ input.
$\overline{\text{SINGLE TONE INHIBIT}}$ Input	The $\overline{\text{SINGLE TONE INHIBIT}}$ input is used to inhibit the generation of other than valid tone pairs due to multiple row-column closures. It has a pull-down resistor to V_{SS}, and when left open or tied to V_{SS} any input condition that would normally result in a single tone will now result in no tone, with all other functions operating normally. When tied to V_{DD}, single or dual tones may be generated, see Table II.
TONE OUT	This output is the open emitter of an NPN transistor, the collector of whch is connected to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group sine-waves superimposed on a DC offset. When not generating tones, this output transistor is turned OFF to minimize the device idle current. Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sinewave signal current through the output transistor, and the output distortion. Increasing values of load resistance decrease both the signal current and distortion.

Functional Description

With no key inputs to the device the oscillator is inhibited, the output transistor is pulled OFF and device current consumption is reduced to a minimum. Key closures are sensed statically. Any key closure activates the $\overline{\text{MUTE}}$ output, starts the oscillator and sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine-wave cycle. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistor.

The amplitude of the output tones is directly proportional to the device supply voltage.

Functional Description (Continued)

TABLE I. Output Frequency Accuracy

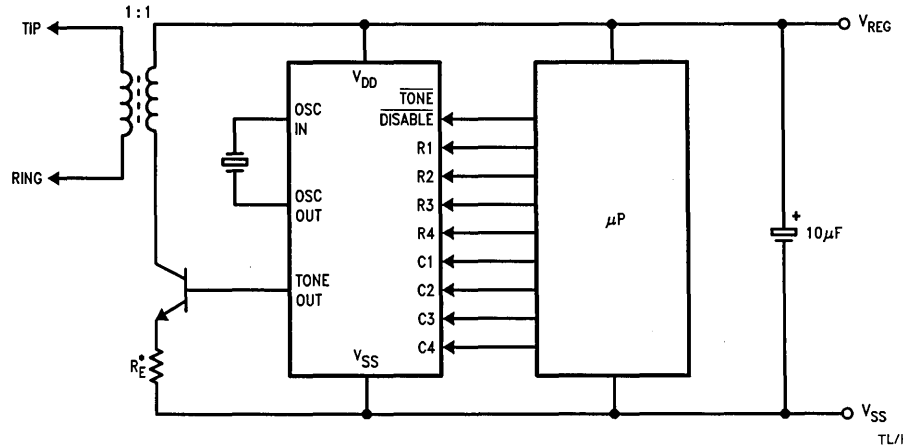
Tone Group	Valid Input	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	R1	697	694.8	−0.32
	R2	770	770.1	+0.02
	R3	852	852.4	+0.03
	R4	941	940.0	−0.11
High Group f_H	C1	1209	1206.0	−0.24
	C2	1336	1331.7	−0.32
	C3	1477	1486.5	+0.64
	C4	1633	1639.0	+0.37

TABLE II. Functional Truth Table

SINGLE TONE INHIBIT	TONE DISABLE	ROW	COLUMN	TONE OUT		MUTE
				Low	High	
X	O	O/C	O/C	0V	0V	O/C
X	X	O/C	O/C	0V	0V	O/C
X	0	One	One	V_{OS}	V_{OS}	O
X	1	One	One	f_L	f_H	O
1	1	2 or More	One	—	f_H	O
1	1	One	2 or More	f_L	—	O
1	1	2 or More	2 or More	V_{OS}	V_{OS}	O
0	1	2 or More	One	V_{OS}	V_{OS}	O
0	1	One	2 or More	V_{OS}	V_{OS}	O
0	1	2 or More	2 or More	V_{OS}	V_{OS}	O

Note 1: X is don't care state.

Note 2: V_{OS} is the output offset voltage.



TL/H/5057–3

*Adjust R_E for desired tone amplitude.

FIGURE 2. Typical Application

National Semiconductor Corporation

PRELIMINARY

TP5700A
Telephone Speech Circuit

General Description

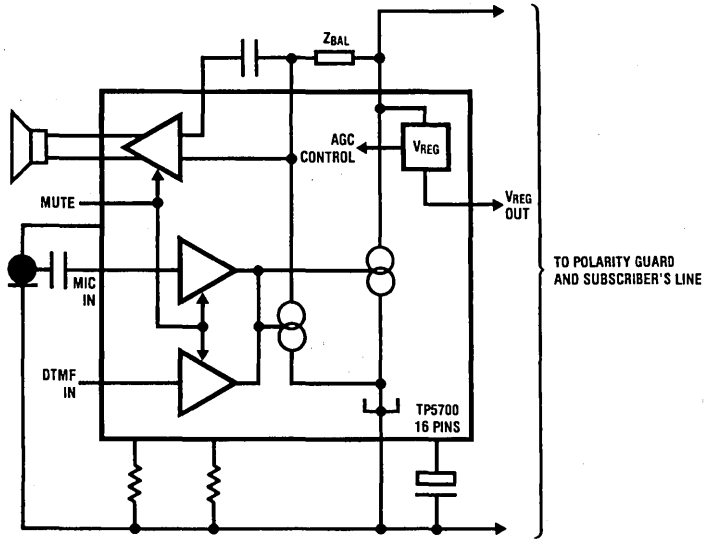
The TP5700A is a linear bipolar device which includes all the functions required to build the speech circuit of a telephone. It replaces the hybrid transformer, compensation circuit and sidetone network used in traditional designs. When used with an electret microphone (with integral FET buffer) and dynamic receiver, superior audio linearity, distortion and noise performance are obtained. Loop attenuation compensation is also included.

The low voltage design enables the circuit to work over a wide range of operating conditions, including long loops, extension telephones and subscriber carrier applications. Operating power is derived from the telephone line.

Features

- 5 mA–120 mA loop operation
- Voltage swing down to 1.0V
- Electret microphone amplifier
- Receive amplifier with push-pull outputs
- Automatic gain compensation for loop length
- Sidetone impedance independent of input impedance
- DTMF interface with muting
- Voltage regulator outputs for DTMF generator etc.
- Works in parallel with a standard phone on 20 mA loop
- Available in small outline surface mount package

Simplified Block Diagram



TL/H/5201–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V^+ with Respect to V^-	20V
Voltage at Any Other Pin	$V^+ + 0.3V$ to $V^- - 0.3V$
Operating Temperature, T_A	−25°C to +70°C
Power Dissipation (Note 3)	1W
Storage Temperature, T_S	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

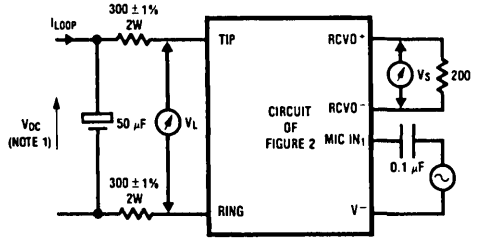
Unless otherwise specified, all tests based on the test circuits shown in *Figure 1*, all limits printed in bold characters are guaranteed at T_A = 0°C to +60°C by correlation with 100% testing at T_A = 25°C. All other limits are assured by by correlation with other production tests, and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{T-R}	Tip-Ring Voltage including nominal 1.4V polarity guard (See *Figure 1*)	I_{LOOP} = 5 mA = 20 mA = 50 mA = 80 mA = 120 mA		2.8 7 10.5 15	 **4.5** 	V V V V V
V_I	Minimum Instantaneous Voltage Swing	V^+ to V^- I_{LOOP} = 5mA		1.0		V
TRANSMIT AMPLIFIER						
R_{XIN}	Input Resistance	From Pin 7 to V^-	15	30	50	kΩ
G_{XA}	Gain at 1 kHz	R_{AGC} = 0Ω to V^- I_{LOOP} = 20 mA, T_A = 25°C only	**33**	35	**37**	dB
G_{XT}	Gain Variation v. T_A			±1		dB
G_{XI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
N_X	Transmit Noise	MIC IN_1 = 0V		12	**18**	dBrnC
S/D_X	Signal/Total Harmonic Distortion	$I_{LOOP} \geq$ 20 mA V_L = 800 mVrms		2	10	%
G_{XM}	Gain Change when MUTED	MUTE IN ≥ V_{MON}		−55		dB
DTMF AMPLIFIER						
R_{DIN}	Input Resistance	From Pin 8 to V^-	10	20	55	kΩ
G_{XD}	Gain at 1 kHz	R_{AGC} = 0Ω to V^- I_{LOOP} = 20 mA, T_A = 25°C only	**3.5**	5.5	**7.5**	dB
S/D_{XD}	Signal/Total Harmonic Distortion	I_{LOOP} = 20 mA V_L = 1.06 Vrms, T_A = 25°C only		3	**10**	%
G_{XDT}	Gain Variation v. T_A			±1		dB
G_{XDI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
MUTE INPUT						
I_{MIN}	Input Current	Pin 9 = 1.5V		40		μA
V_{MOFF}	MUTE OFF Input Voltage				0.5	V
V_{MON}	MUTE ON Input Voltage		1.5			V

DC Electrical Characteristics (Continued)

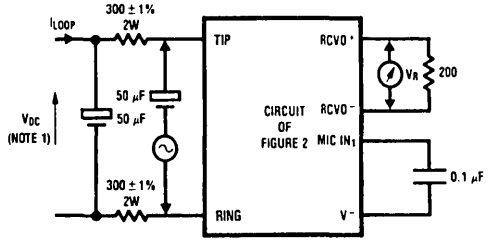
Unless otherwise specified, all tests based on the test circuits shown in *Figure 1*, all limits printed in bold characters are guaranteed at T_A = 0°C to +60°C by correlation with 100% testing at T_A = 25°C. All other limits are assured by by correlation with other production tests, and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE AMPLIFIER						
R_{RIN}	Input Resistance	From Pin 12 to V−	20	35	55	kΩ
G_{RA}	Gain at 1 kHz	R_{AGC} = 0Ω, MUTE IN ≤ V_{MOFF} I_{LOOP} = 20 mA, T_A = 25°C only	**−5.5**	−4	**−2.5**	dB
G_{RT}	Gain Variation v. T_A			±0.5		dB
G_{RI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
G_{RM}	Gain Change when MUTED	MUTE IN ≥ V_{MON}	−15	−20	−23	dB
N_R	Receive Noise	V_{RCVIN} = 0V		0	**10**	dBrnC
S/D_R	Signal/Total Harmonic Distortion	V_R = 200 mVrms I_{LOOP} ≥ 20 mA		2	**10**	%
V_RC	Output Clipping Level	I_{LOOP} ≥ 20 mA		1		Vp-p
V_{ROS}	Output Offset Voltage				±100	mV
SIDETONE CHARACTERISTICS						
STC	Sidetone Cancellation at 1kHz	20 mA ≤ I_{LOOP} ≤ 100 mA, (Note 2)	**11**	15		dB
VOLTAGE REGULATOR OUTPUTS						
V_{REG1}	Output Voltage, Pin 10	I_{LOOP} ≥ 20 mA MUTE IN ≤ V_{MOFF} MUTE IN ≥ V_{MON}	 **2** **3**	 3.2		 V V
I_{REG1}	Maximum Output Current, Pin 10	MUTE IN ≤ V_{MOFF} MUTE IN ≥ V_{MON}		200 2.7		µA mA
V_{REG2}	Output Voltage, Pin 11	I_{LOOP} ≥ 20 mA	1.1	1.2		V
I_{REG2}	Maximum Output Current, Pin 11	I_{LOOP} ≥ 20 mA	300	500		µA



TL/H/5201–2

1a. Test Circuit for Transmit and Sidetone



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1b. Test Circuit for Receive

FIGURE 1. Test Circuits for Electrical Characteristics

Note 1. Adjust V_{DC} to set specified I_{LOOP} current.

Note 2. To measure Sidetone Cancellation, set oscillator in *Fig. 1a* for V_L = 100 mVrms; measure V_S. Then in *Fig. 1b* set oscillator = 100 mVrms; measure V_R. STC = 20log V_R/V_S.

Note 3. For operation above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 70°C/W junction to ambiant.

Functional Description

The TP5700A Telephone Speech Circuits are powered from the telephone Tip and Ring terminals via a full-wave rectifier bridge to protect against loop polarity reversals. The devices provide the following functions:

LINE REGULATOR

A DC regulator sinks current from the loop in order to maintain a DC slope resistance similar to that of a standard phone.

R_{DC} provides an adjustment for the slope resistance.

MICROPHONE AMPLIFIER

A single-ended input amplifier on the TP5700A enables a low cost electret microphone to be used. This provides superior distortion, linearity and noise performance compared to a traditional carbon microphone. The electret should be capacitively coupled to the amplifier input. The acoustic sensitivity of the microphone is intended to be in the range of −60 to −70 dBV/µBar.

Loss can be inserted if required by adding a resistive potentiometer either at MIC IN_1 or the connection between the pre-amp output and driver stage input. The driver stage pro-

Functional Description (Continued)

vides automatic gain compensation to reduce the gain as loop length decreases. The AGC range can be adjusted by means of R_{AGC} to limit the maximum loss on a short loop from 0 to 6 dB.

RECEIVE AMPLIFIER

This buffer amplifier provides the necessary gain or loss for the receive signal. RCV IN should be AC coupled to SIDETONE (pin 4). Automatic gain control is built into the amplifier to reduce the gain as loop length decreases. The AGC range is adjusted in common with the transmit AGC range with a range of adjustment for maximum loss from 0 to 6 dB. Push-pull complementary outputs provide balanced direct drive to a dynamic transducer, which may have an impedance as low as 100Ω. The effective receive gain can be reduced by adding a resistor in series with the transducer. The receive gain is automatically reduced by 20 dB when the MUTE input is pulled high.

SIDETONE CIRCUIT

The level of Sidetone cancellation may be adjusted by connecting an external balance impedance to SIDETONE (pin 4) and coupling this point to V^+. For good sidetone cancellation the balance impedance should be approximately 10 times the subscriber line input impedance. Some typical component values to match a precise 600Ω termination for test purposes are shown in *Figure 2*. Use the component values shown in the Applications Section for better results over a wide range of telephone line impedances.

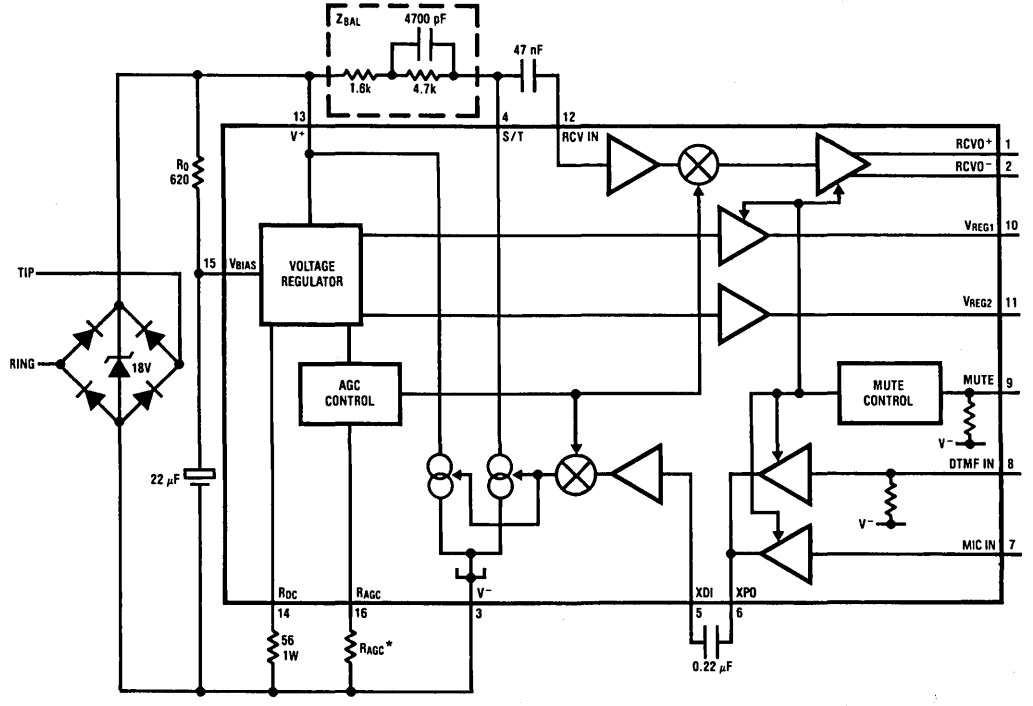
DTMF AMPLIFIER

An additional transmit amplifier is included to enable the open-emitter output of a conventional DTMF generator to be connected to the line via the transmit output stage. This path includes the transmit AGC section. When the MUTE input is pulled high, the DTMF input is enabled and the MIC input disabled. When MUTE IN is open-circuit or pulled to V^- the DTMF input is switched off and the MIC input is enabled.

VOLTAGE REGULATOR OUTPUTS

A precision band-gap voltage reference controls a regulator to provide bias for internal circuits. Two auxiliary outputs are also available. V_{REG1} is provided specifically for powering a low voltage pulse dialer or DTMF generator. In order to protect this output in low voltage situations where the instantaneous voltage across the Speech Circuit may swing below the V_{REG1} output voltage, an internal switch controls the maximum available output current. In speech mode, MUTE IN is low, V_{REG1} output will track approximately ½ the Tip-Ring voltage and the available output current is limited to 200 μA. This is adequate to power a DTMF generator in standby mode. When MUTE IN is pulled high to switch the Speech Circuit to the DTMF dialing mode, V_{REG1} is switched to a 3V regulated output and up to 2 mA may be drawn from it to power the active DTMF generator.

A 1.2V regulated output is also provided at V_{REG2} to power a low voltage 2-wire electret microphone such as the Primo EM80-PMI$_2$.



TL/H/5201–4

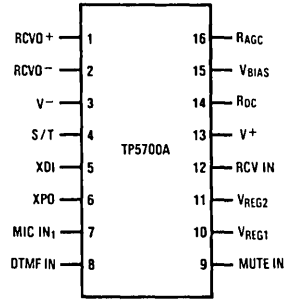
* See Figure 3

Note: Z_{BAL} circuit shown is for test purposes with a resistive line termination. See Applications Information for suggested component values for normal reactive line applications.

FIGURE 2. TP5700A Telephone Speech Circuits

Connection Diagram

Dual-In-Line Package



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Top View

Order Number TP5700AM, TP5700AN or TP5700N
See NS Package M16B or N16A

Pin Descriptions

Pins 1, 2 RCV0+ and RCV0−

The push-pull complementary outputs of the receive amplifier. Dynamic transducers with a minimum impedance of 100 Ω can be directly driven by these outputs.

Pin 3 V−

This is the negative supply input to the device and should be connected to the negative output of the polarity guard. All other voltages on the device are referred to this pin.

Pin 4 S/T

This is the output of the Sidetone cancellation signal, which requires a balance impedance of approximately 10 times the subscriber's line impedance to be connected from this pin to V+ (pin 13).

Pin 5 XDI

The input to the line output driver amplifier. Transmit AGC is applied in this stage.

Pin 6 XPO

This is the transmit pre-amp output which is normally capacitively coupled to pin 5.

Pin 7 MIC IN_1

This is the inverting input to the transmit pre-amplifier and is intended to be capacitively coupled to an FET-buffered electret microphone.

Pin 8 DTMF IN

The DTMF input which has an internal resistor to V− to provide the emitter load resistor for a CMOS DTMF generator. This input is only active when MUTE IN (pin 9) is pulled high.

Pin 9 MUTE IN

The MUTE Input, which must be pulled at least 1.5V higher than V− to mute MIC IN and enable DTMF IN.

Pin 10 V_{REG1}

The regulated output for biasing a pulse dialer or DTMF generator. A 4.7 μF decoupling capacitor to V− should be fitted if this output is used.

Pin 11 V_{REG2}

A 1.2V regulated output suitable for powering a low-voltage electret microphone. A 1μF decoupling capacitor to V− should be fitted if this output is used.

Pin 12 RCV IN

The receive AGC amplifier input.

Pin 13 V+

This is the positive supply input to the device and should be connected to the positive output of the polarity guard. The current through this pin is modulated by the transmit signal.

Pin 14 R_{DC}

An external 1W resistor is required from this pin to V− to control the DC input impedance of the circuit. The nominal value is 56Ω for low voltage operation. Values up to 82Ω may be used to increase the available transmit output voltage swing at the expense of low voltage operation.

Pin 15 V_{BIAS}

This internal voltage bias line must be connected to V+ via an external resistor, R_o, and decoupled to V− with a 22 μF capacitor. R_o dominates the AC input impedance of the circuit and should be 620Ω for a 600Ω input impedance or 910Ω for a 900Ω input impedance.

Pin 16 R_{AGC}

The range of transmit and receive gain variations between short and long loops may be adjusted by connecting a resistor from this pin to V− (pin 3). *Figure 3* shows the relationship between the resistor value and the AGC range. This pin may be left open-circuit to defeat AGC action.

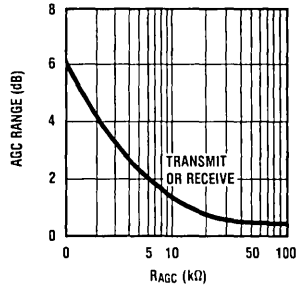

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FIGURE 3

Applications Information

The TP5700A and TP5700 are flexible circuits designed with several user adjustments to enable the performance to be optimized for different applications. The choice of transducer types and the cavities in which they are mounted will also greatly influence the acoustic performance of the telephone. Some of the consequences of circuit adjustments are as follows:

R_{DC} ADJUSTMENT

56Ω is the recommended value for R_{DC} if it is required to meet a maximum Tip-Ring voltage of 4.5V on a 20 mA loop (assuming no more than 1.4V is dropped across the polarity guard). If a higher Tip-Ring voltage is acceptable, R_{DC} may be increased, which will provide a small increase in the available transmit output voltage swing before clipping occurs. R_{DC} should be less than 82Ω to avoid exceeding the maximum rated voltage on a short loop.

R_{AGC} ADJUSTMENT

The available AGC range is more than adequate to compensate for the loss of most loops. R_{AGC} should be chosen only to partly compensate for the anticipated maximum loop loss, as over-compensation may tend to exaggerate the variations of sidetone with loop length.

SIDETONE ADJUSTMENT

The component values used for Z_{BAL} should be selected to provide a clear sidetone sound without excessive "hollowness." The capacitor value and ratio of the two resistors will fix the pole location. To avoid reducing the low voltage performance of the circuit the sum of the two resistors should not exceed 10 kΩ.

POWERING ELECTRET MICROPHONES

Electret microphones with integral FET buffers are available in both two-wire and three-wire versions and a range of operating voltage ranges. There are four methods of powering the microphone.

1. The 1.2V V_{REG2} output provides the lowest voltage method for microphones rated down to 1V. V_{REG2} must be decoupled with a 1 μF capacitor to ground. (See *Figure 5.*)
2. If V_{REG1} is not required for DTMF generator operation, it may be used to provide up to 200 μA for microphone power.
3. V_{BIAS} (pin 15) may be used as a decoupled, but unregulated, supply for electrets requiring a higher operating voltage than V_{REG1} or V_{REG2}. The additional current drawn through R_0 will, however, raise the minimum operating voltage of the Speech Circuit. If this method is used the decoupling capacitor must be increased to at least 100 μF to maintain good low frequency return loss. (See *Figure 4.*)
4. An electret type with a good power supply rejection ratio can be powered from V+, or a regulated and decoupled supply dropped from V+.

TONE DIALING TELEPHONE

Figure 4 shows the TP5700 directly interfacing to a low voltage DTMF generator. V_{REG1} supplies the necessary 2V minimum bias to enable the low voltage tone dialer to sense key closures and pull its MUTE output high. V_{REG1} then switches to a 3V regulated output to sustain the Tone Dialer during tone generation. The TP5700A DTMF input incorporates the necessary load resistor to V− and provides gain plus AGC action to compensate for loop length. A muted tone level is heard in the receiver. For DTMF generators with a higher output level, a resistive potentiometer should

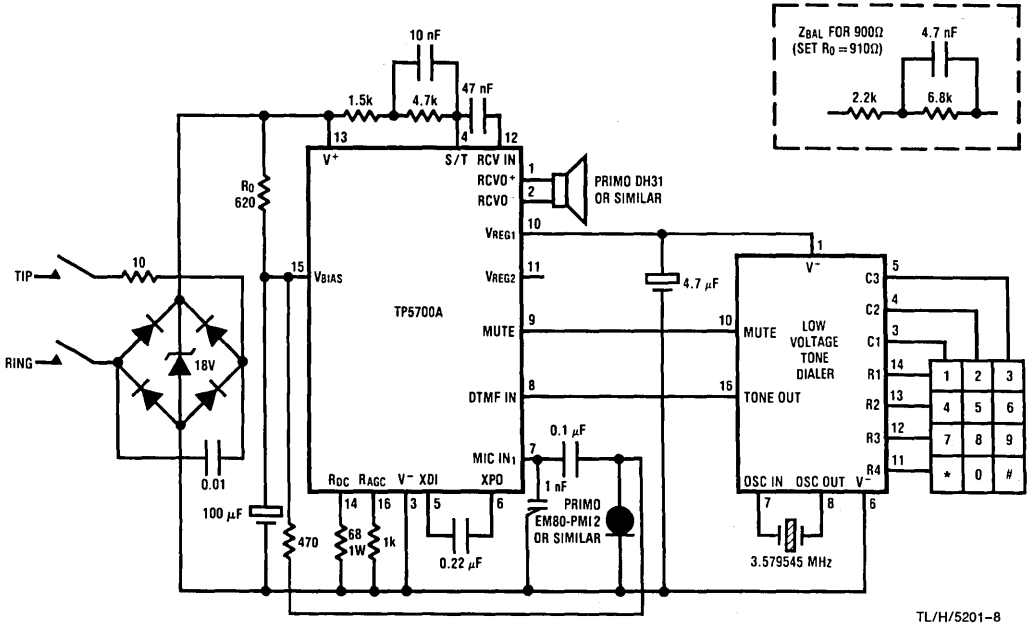

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FIGURE 4. Typical Tone Dialing Telephone

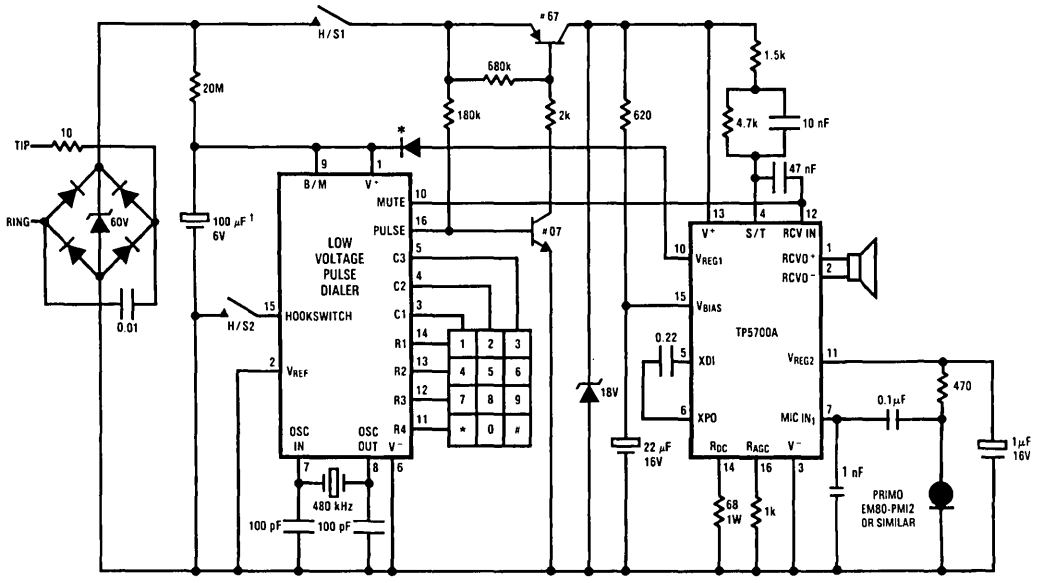
Applications Information (Continued)

be added to reduce the level at the speech circuit DTMF Input. For application requiring higher DTMF level, the signal swing across the device can be raised by using 620Ω in series with 270Ω for R_O. The 270Ω has to be bypassed by a 10 μf capacitor in order to maintain same AC off hook impedance.

PULSE DIALING TELEPHONE

The TP5700A can reduce the number of components required to build a pulse dialing telephone, as shown in *Figure 5*. The usual current source can be eliminated by using the V_{REG1} output to power a low-voltage (1.7V) series mode pulse dialer via a blocking diode. A low forward-voltage drop diode such as a Schottky type is necessary because V_{REG1} is used in its non-regulated mode and its output voltage may fall to 2V on a 20 mA loop. A 100 μF decoupling capacitor is required to hold up the pulse dialer supply voltage during dialing. This capacitor will take about one second to charge up when the telephone is first connected to the line, but thereafter the 20 MΩ resistor required to retain the last-number dialed memory will keep this capacitor charged. Partial muting is obtained by directly connecting the N-channel open-drain MUTE output of the pulse dialer to the RCV IN pin on the Speech Circuit.

A fully muted pulse dialer design requires the use of a shunt-mode dialer.



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*Low voltage drop diode (e.g. Schottky)

† Low leakage type

# Indicates National Semiconductor discrete transistor process number

FIGURE 5. Typical Pulse Dialing Telephone

Section 5

Application Notes

Section 5 Contents

Understanding Integrated Circuit Package Power Capabilities

National Semiconductor Corp.
Application Note 336
Charles Carinalli
Josip Huljev

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

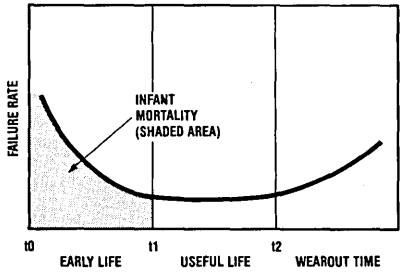

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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

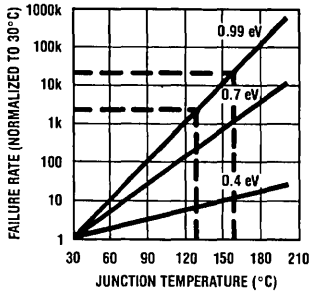

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All interface circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using interface components.

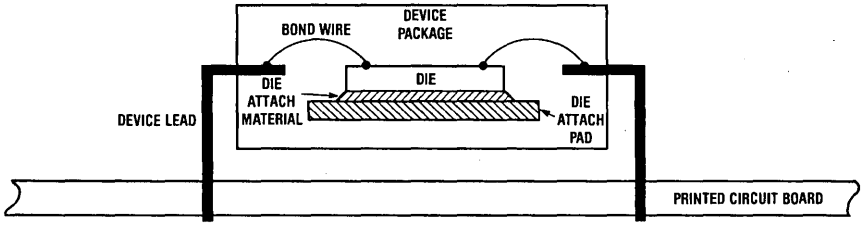

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FIGURE 3. Integrated Circuit Soldered Into a Printed Circuit Board (Cross-Sectional View)

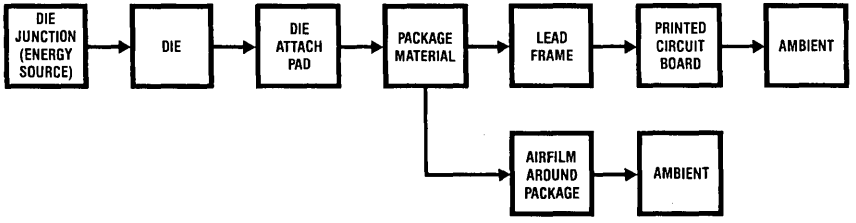

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

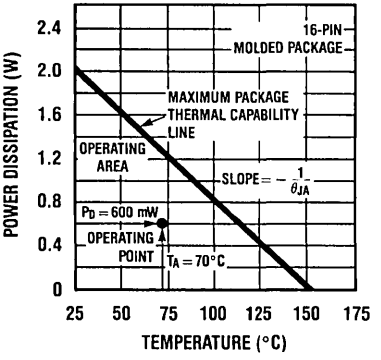

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FIGURE 5. Package Power Capability vs Temperature

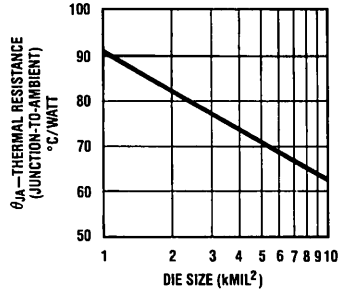
The thermal capabilities of all interface circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

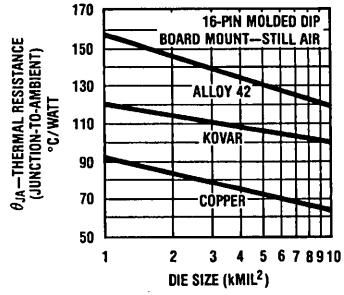


TL/F/5280–6

FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 43 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

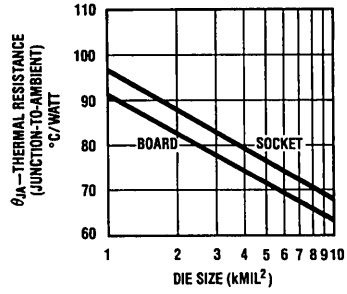


TL/F/5280–7

FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

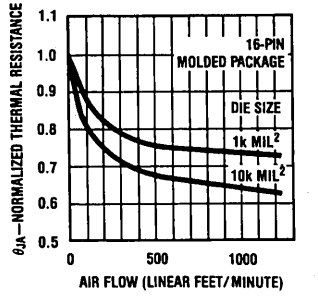


TL/F/5280–8

FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.



TL/F/5280–9

FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Interface Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Interface Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the interface data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

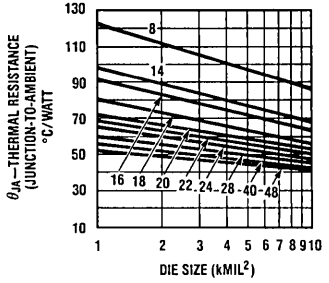
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D \text{ @ } 70°C = 1476 \text{ mW} - (11.8 \text{ mW}/°C) \times (70°C - 25°C)$$
$$= 945 \text{ mW}$$

Molded (N Package) DIP* Copper Leadframe—HTP Die Attach Board Mount—Still Air

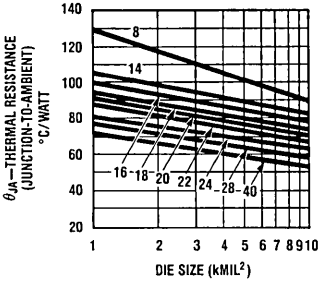


*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

TL/F/5280–10

FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Cavity (J Package) DIP* Poly Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

TL/F/5280–11

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

MM74HC942 and MM74HC943 Design Guide

National Semiconductor Corp.
Application Note 347
Peter Single
Steve Munich

SECTIONS

1) TIMING AND CONTROL

a) Input and Output Thresholds

The MM74HC942/943 may be used in a CMOS or TTL environment. In a CMOS environment, no interfacing is required. If the MM74HC942/943 is interfaced to NMOS or bipolar logic circuits, standard interface techniques may be used. These are discussed in detail in National Semiconductor Application Note AN-314. This note is included in the National Semiconductor MM54HC/74HC High Speed micro-CMOS Logic Family Databook.

b) Logic States and Control Pin Function

Transmitted Data

TXD (pin 11) in conjunction with O/A selects the frequency of the transmitted tone and thus controls the transmitted data.

TXD = V_{CC} selects a "mark" and thus the high tone of the tone pair. This is discussed further in the following section.

Originate and Answer Mode

This is controlled by O/A (pin 13). O/A = V_{CC} selects originate mode. O/A = GND selects answer mode. These modes refer to the tone allocation used by the modem. When two modems are communicating with each other one will be in originate mode and one will be in answer mode. This assures that each modem is receiving the tone pair that the other modem is transmitting. The modem on the phone that originated the phone call is called the originate modem. The other modem is the answer modem.

The other pin controlling the transmitted tone is TXD (pin 11).

Bell 103 Tone Allocation				
Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz

Squelch Transmitter

Transmitter squelch is achieved by putting SQT = V_{CC} (SQT is pin 14). The line driver remains active in this state (assuming ALB = GND).

This state is commonly used during the protocol of establishing a call. The originate user initiates a phone call with its transmitter squelched, and waits for a tone to be received before beginning transmission. During the wait time, the modem is active to allow tone detection, but no tone may be transmitted.

The state SQT = V_{CC} may also be used if the line driver is required but a signal other than modem tones (e.g., DTMF tones or voice) is to be transmitted. This is discussed further in Transmission of Externally Generated Tones (section 3d).

Analog Loop Back

ALB = V_{CC}, SQT = GND selects the state "analog loop back". (The state ALB = SQT = V_{CC} is discussed in the following section.)

In analog loop back mode, the modulator output (at the line driver) is connected to the demodulator input (at the hybrid), and the demodulator is tuned to the transmitted frequency tone set. Thus the data on the TXD pin will, after some

delay, appear at the RXD pin. This provides a simple "self test" of the modem.

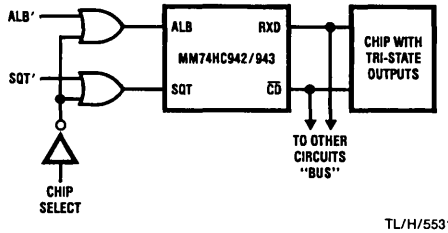
The signal applied to the demodulator during analog loop back is sufficient to cause the carrier detect output CD to go low indicating receipt of carrier.

In analog loop back mode, the modulator and transmitter are active, so the transmitted tone is not squelched.

Power-Down Mode

The state SQT = ALB = V_{CC} puts the MM74HC942/943 in power-down mode. In this state, the entire circuit except the oscillator is disabled. (The oscillator is left running in case it is required for a system clock). In power-down mode the supply current falls from 8 mA (typ) to 180 μA (typ), and all outputs, both analog and digital, TRI-STATE (become Hi-Z).

Using TRI-STATE Capability



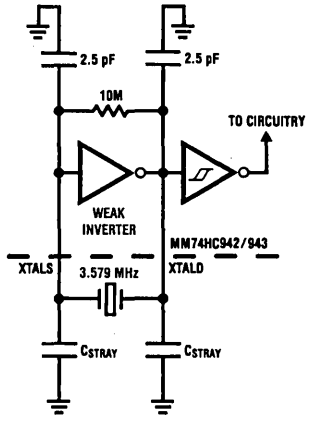
TL/H/5531–1

The ability of the outputs to TRI-STATE allows the modem to be connected to other circuitry in a bus-like configuration with the state SQT or ALB = GND being the modem chip select.

c) The Oscillator

The oscillator is a Pierce crystal oscillator. The crystal used in such an oscillator is a parallel resonant crystal.

The Oscillator



TL/H/5531–2

The capacitors used on each end of the crystal are a combination of on-chip and stray capacitances. This generally means the crystal is operating with less than the specified parallel capacitance. This causes the oscillator to run faster than the frequency of the crystal. This is not a problem as the frequency shift is small (approximately 0.1%).

The oscillator is designed to run with equal capacitive loading on each side of the crystal. This should be taken into consideration when designing PC layouts. This need not be exact.

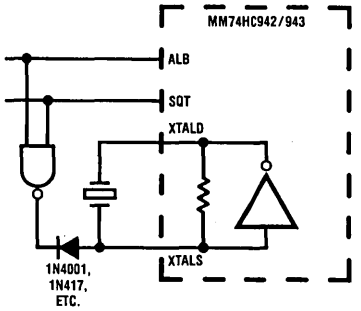
If a 3.58 MHz oscillator is available, the XTALD pin may be driven. The internal inverter driving this pin is very weak and can be overpowered by any CMOS gate output.

The Oscillator and Power-Down Mode

When the chip powers down, all circuits except the oscillator are switched off. The oscillator is left running so it may be used as a clock to drive other circuits within the system.

It is possible to shut the oscillator down by clamping the XTALS pin to V_{CC} or GND. This will cause the total chip current to fall to less than 5 μA. This may be useful in battery powered systems where minimizing supply current is important.

Powering Down the Oscillator



TL/H/5531–3

2) MODULATOR SECTION

a) Operation

The modulator receives data from the transmit data (TXD) pin and synthesizes a frequency shift keyed, phase coherent sine wave to be transmitted by the line driver through the transmit analog (TXA) pin. Four different sine wave frequencies are generated, depending on whether the modem is set to the originate or answer mode and whether the data input to TXD is a logical high or low. See Timing and Control (section 1) for more information.

The TXD and O/A pins set the divisor of a dual modulus programmable divider. This produces a clock frequency which is sixteen times the frequency of the carrier to be transmitted. The clock signal is then fed to a four bit counter whose outputs go to the sine ROM. The ROM acts like a four-to-sixteen decoder that selects the appropriate tap on the D/A converter to synthesize a staircase-approximated sine wave. A switched capacitor filter and a low pass filter smooth the sine wave, removing high frequency components and insuring that noise levels are below FCC regulations.

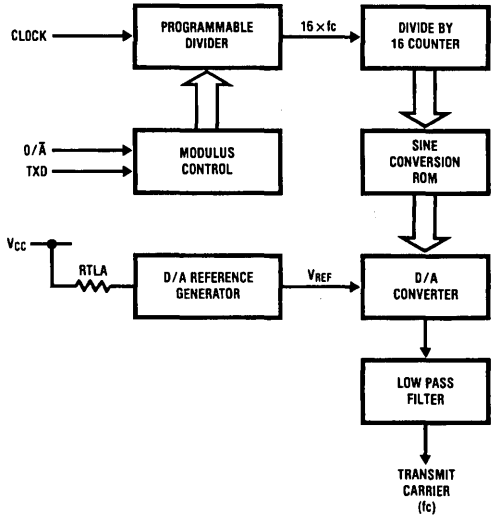
b) Transmit Level Adjustment

The maximum transmit level of the MM74HC943 is −9dBm. Since most phone lines attenuate the signal by 3 dB, the maximum level that will be received at the exchange is −12 dBm. This level is also the maximum allowed by most phone companies. The MM74HC942 has a maximum transmit level of 0 dBm, making possible adjustments for line losses up to −12 dB. The resistor values required to adjust the transmit level for both the MM74HC942 and the MM74HC943 follow the Universal Service Order Code and can be found in the data sheets.

This resistor added between the TLA pin and V_{CC} serves to control the voltage reference at the top of the D/A ladder, adjusting output levels accordingly.

Note that for transmission above −9 dBm the required resistor must be chosen with the co-operation of the relevant phone company. This resistor is usually wired into the phone jack at the installation as the resistor value is specific to the particular phone line. This is called the Universal Registered Jack Arrangement. This arrangement is possible only with the MM74HC942 because of the dynamic range constraints of the MM74HC943.

The Modulator



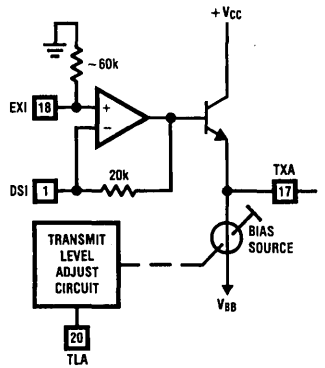
TL/H/5531–4

3) THE LINE DRIVER

a) Operation

The line driver is a class A power amplifier for transmitting the carrier signals from the modulator. It can also be used to transmit externally generated tones such as DTMF signals, as discussed in section 3d. When used for transmitting modem-produced tones, the external input (EXI) pin should be grounded to pin 19 for both the MM74HC942 and the MM74HC943. The line driver output is the transmit analog (TXA) pin.

The Line Driver Equivalent Schematic



TL/H/5531–5

b) Second Harmonic Distortion

If the modem is operating in the originate mode, the line driver output has frequencies of 1070 Hz for a space and 1270 Hz for mark. The second harmonic for a space frequency is at 2140 Hz, and this falls in the originate modem's receive frequency band from 2025 Hz to 2225 Hz. While the modulator produces very little second harmonic energy, the amplifier has been designed not to degrade the analog output any further. The result is that the second harmonic is below −56 dBm. Thus it is well below the minimum carrier amplitude recognized by the demodulator.

c) Dynamic Range

The decision to use the MM74HC942 or the MM74HC943 is a tradeoff between output dynamic range and power supply constraints. The power supply is discussed in another section. The MM74HC942 will transmit at 0 dBm while the maximum transmit level of the MM74HC943 is −9 dBm. This level applies to externally generated tones as well as the standard modem tone set.

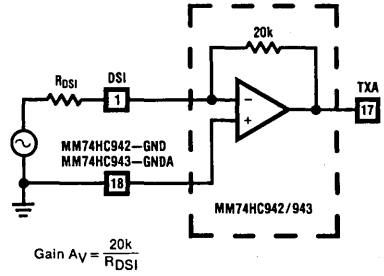
It is important to realize that the signal levels referred to above, and in the data sheet's specifications, are the levels referred to a 600Ω load resistor (representing the phone line) when driven from the external 600Ω source resistor. Also, the transmit levels discussed previously are maximum values. Typical values are 1 dB to 2 dB below these.

d) Transmission of Externally Generated Tones

Since a phone line connection is usually made on the TXA pin, it may be useful to use the line driver to transmit DTMF, voice or other externally generated tones. Both the inverting and non-inverting inputs to the line driver are available for this purpose. A DTMF tone generator with a TRI-STATE output may instead be directly connected to the same node as the TXA pin rather than the line driver. The choice of which method to use depends on whether the MM74HC942 or MM74HC943 is being used and the signal level of the transmission. Most phone companies allow DTMF tone generation at 0 dBm. This level is the maximum that the MM74HC942 can produce and is beyond the range of the MM74HC943.

If the line driver is to be used for external tone generation, the modem must be powered up and the transmission must be squelched by the SQT pin being held high. This will disable the output of the modulator section. The choice between the EXI pin and DSI pin is up to the user. The EXI pin gives a fixed gain of about 2. The DSI input allows for adjustable gain as a series resistor is necessary.

Using the DSI Input

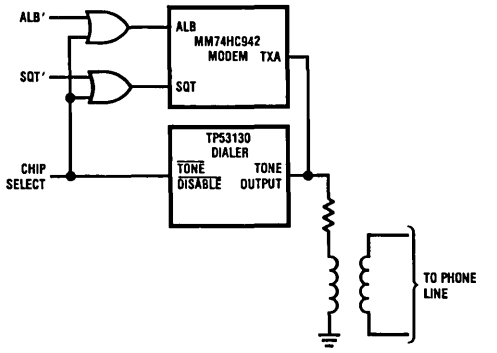


TL/H/5531–6

A better solution may be to use the power-down mode of the MM74HC942/943 with a DTMF tone generator that has a TRI-STATE output. Such a device is a TP53130 and is

shown in the diagram following. When the tone generator is not in use and the modem is not squelched, the DTMF generator's output is in TRI-STATE. Rather than using the line driver, the tone generator's output is instead connected to the same node as the TXA pin. The tone generator is active when the modem is in power-down. Power-down TRI-STATEs the TXA output.

Interfacing to DTMF Generator Using TRI-STATE Feature



TL/H/5531–7

4) THE HYBRID

The MM74HC942/943 has an on-chip hybrid. (A hybrid in this context refers to a circuit which performs two-to-four wire conversion.)

Under ideal conditions the phone line and isolation network have an equivalent input impedance of 600Ω. Under these conditions the gain from the transmitter to the op amp output is zero, while the gain from the phone line to the op amp output is unity. Thus the hybrid, by subtracting the transmitted signal from the total signal on the phone line, has removed the transmitted component.

Unfortunately, these ideal conditions rarely exist and filtering is used to remove the remaining transmitted signal component. This is discussed further in the next section.

Note that the signals into the hybrid must be referred to GND in the MM74HC942 and GNDA in the case of the MM74HC943. Thus blocking capacitors are required in the latter case. This is discussed further in DC Levels and Analog Interface (section 9a).

5) THE RECEIVE FILTER

The signal from the hybrid is a mixture of transmitted and received signals. The receive filter removes the transmitted signals so only received signal goes to the discriminator.

The receive filter may be characterized by driving RXA1 or RXA2 with a signal generator. The filter response may then be observed at the FTLC pin with the capacitor removed. In this state the output impedance of the FTLC pin is 16 kΩ nominal.

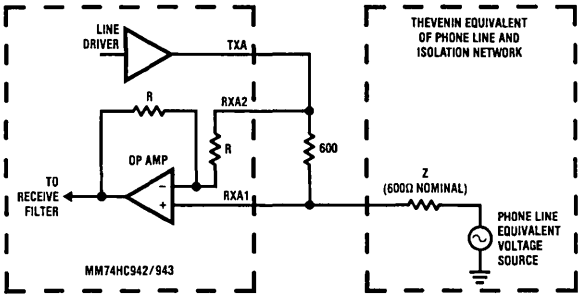
6) THE FTLC PIN

The FTLC pin is at the point of the circuit where the receive filter output goes to the hard limiter input and the carrier detect circuit input.

The signal at the output of the receive filter may be as low as 7 mVrms. It is thus important that the wiring to the FTLC pin and the associated circuit be clean. Ideally the track from the capacitor to pin 19 (GND on the MM74HC942, GNDA on the MM74HC943) should be shared by no other devices.

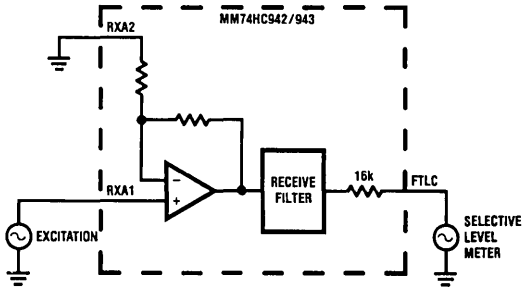
If these precautions are not observed, circuit performance may be unnecessarily degraded.

The Hybrid



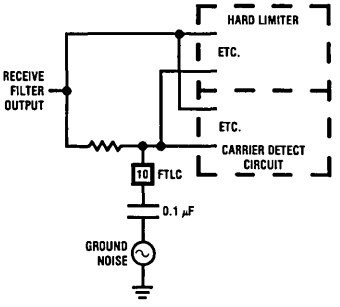
TL/H/5531–8

Characterizing the Receive Filter



TL/H/5531–9

The FTLC Pin and Associated Circuitry



TL/H/5531–10

7) THE CARRIER DETECT CIRCUIT

a) Operation

The carrier detect circuit senses if there is carrier present on the line. If carrier is not present, the data output is clamped high.

The RC circuit filters the DC from the output of the receive filter. The comparator inputs are thus the filter output, and the DC level of the receive filter minus the controlled offset. The controlled offset sets the amount that the AC signal must exceed the DC level (and thus the AC amplitude) before the comparator switches. When this happens, the comparator output sets a resettable one-shot which converts the periodic comparator output to a continuous signal. This signal then controls the time delay set by the CDT pin. After the preset time delay the CD bar output goes low. This shifts the comparator offset providing hysteresis to the overall circuit.

b) Threshold Control

The carrier detect threshold may be adjusted by adjusting the voltage on the CDA pin.

The carrier detect trip points are nominally set at −43 dBm and −46 dBm. The CDA pin sits at a nominal 1.2V. The carrier detect trip points are directly proportional to the voltage on this pin, so doubling the voltage causes a 6 dB increase in the carrier detect trip points. Similarly, halving the voltage causes a 6 dB decrease in carrier detect trip points.

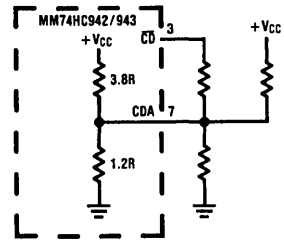
Note that as the carrier detect trip point is reduced, the system noise will approach the carrier level, and the accuracy and predictability of the carrier detect trip points will decrease.

The output impedance of the CDA pin is high. It is constant (±10%) from die to die but has a very high temperature coefficient. It is thus advisable, if the CDA pin is driven, to drive from a low source impedance.

Because the output impedance of the CDA pin is high, capacitive coupling from the adjacent XTALD pin can present a problem. For this reason a 0.1 μF capacitor is usually connected from the CDA pin to ground. If the CDA pin is driven from a low impedance source, this capacitor may be omitted.

If a resistor is connected from the CD bar pin to the CDA pin, the CDA voltage will vary depending on whether carrier is detected. This will effectively increase the carrier detect hysteresis.

Increased Carrier Detect Hysteresis



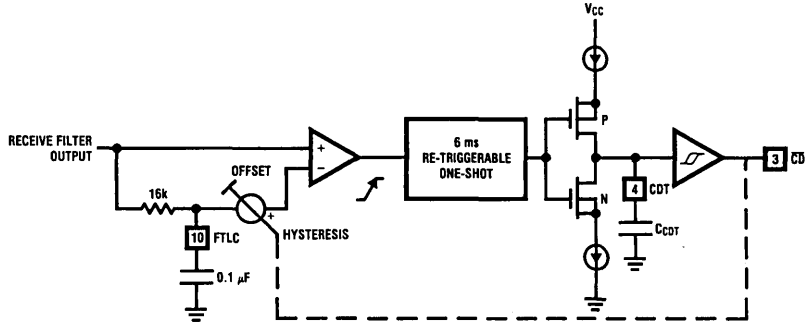
TL/H/5531–11

Similarly an inverter and a resistor from the CD bar pin to the CDA pin will reduce the hysteresis. This is not recommended as the 3 dB nominal figure chosen is close to the minimum value useable for stable operation.

c) Timing Control

The capacitor on the CDT pin adjusts the amount of time that carrier must be present before the carrier is recognized as valid.

Carrier Detect Block Diagram



TL/H/5531–12

This circuit is designed for a long off-to-on time compared to the on-to-off time. This means carrier must be present and stable to be acknowledged, and that if carrier is marginal it will be rejected quickly.

The equations for the capacitor value are

$T_{on\text{-}to\text{-}off} = C \times 0.54$ seconds

and

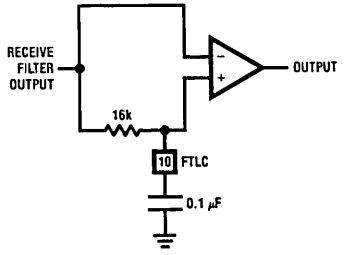
$T_{off\text{-}to\text{-}on} = C \times 6.4$ seconds.

The ratio of on-to-off and off-to-on times may be adjusted over a narrow range by the addition of pull-up or pull-down resistors on the CDT pin.

The repeatability of the times is high from die to die at fixed temperature, but is strongly temperature dependent. The times will shift by approximately ±30% over process and temperature.

8) THE DISCRIMINATOR

a) The Hard Limiter



TL/H/5531–13

The signal to the inverting input of the comparator has the same DC component as the signal to the non-inverting input. The differential input to the comparator is thus the AC component of the filter output. The comparator has very low input offset and so the limiter will operate with very low input signal levels.

The demodulator employed requires an input signal having equal amplitude for a mark and a space. It also requires a high level signal. The hard limiter converts all signals to a square wave. All amplitude information is lost but frequency information is retained.

By removing the capacitor from the FTLC pin, the hard limiter ceases to operate, but the filter output may be observed. This is useful for circuit evaluation and testing.

b) Discriminator Operation

The discriminator separates the incoming energy into mark and space energy. This occurs in the band pass filters which are tuned to the mark and space frequencies. The outputs of the mark and space band pass filters are rectified to extract the output amplitudes. The rectifier outputs are filtered to remove ripple. The low pass filter outputs are compared to determine if the mark or space path is receiving greater energy, and thus if the incoming data is a mark or a space.

The output of the discriminator is only valid if carrier is being received. If carrier is not being received (as determined in the carrier detect circuit) the RXD output is clamped high. This stops the discriminator from attempting to demodulate a signal which is too low for reliable operation.

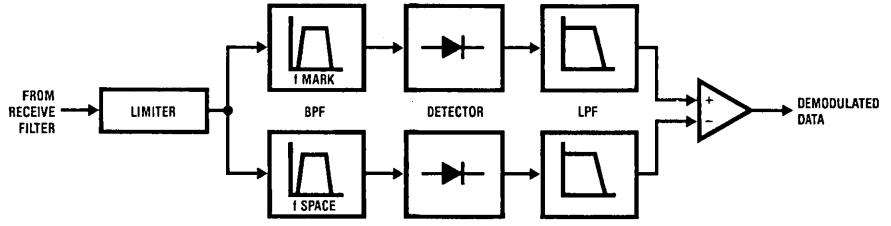
9) POWER SUPPLIES

a) DC Levels and Analog Interface

The MM74HC942 refers all analog inputs and outputs to GND (pin 19). The analog interface thus requires no DC blocking capacitors.

The MM74HC943 refers all analog inputs and outputs to GNDA (pin 19) which requires a nominal 2.5V supply. The current requirements of GNDA are low, so the GNDA supply may be derived with a simple resistive divider. The GNDA supply can then be referenced to GND using capacitors. This GNDA supply will have poor load regulation so the high current interface must be connected to GND and a DC blocking capacitor used.

As the FTLC capacitor is connected to the input of the hard limiter, any noise on the FTLC ground return will couple directly into this circuit. The signal on FTLC may be only millivolts, so it is important that the FTLC capacitor ground be at the same potential as the chip's ground reference. Thus when using the MM74HC943 the FTLC capacitor ground return should go directly to GNDA (pin 19). For both the MM74HC942 and MM74HC943 this ground return should be shared by no other circuits. Failure to observe this precaution could result in unnecessary reduction of dynamic range and carrier detect accuracy, and an increase in error rate.



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b) Power Supply Noise

It is important that the power supplies to the MM74HC942/943 be stable supplies, having low noise, particularly in the frequency band from 50 kHz to 10 MHz.

The MM74HC942/943 use switched capacitor techniques extensively. A feature of switched capacitor circuits is their ability to translate noise from high frequency bands to low frequency bands. At the same time it is difficult to design op amps with high power supply rejection at high frequencies. (The MM74HC942/943 has 19 op amps internally.) As a result the high frequency PSSR of the MM74HC942/943 is not high, so high frequency noise on the power supply can degrade circuit operation.

This should not cause a problem if the circuits are powered from a three terminal regulator, and no other circuitry shares the regulator. Power supply noise could be a problem if:

a) One or both of the power supplies are switching regulator circuits. Switching regulators can produce a lot of supply noise.

b) The modem shares its supply with a large digital circuit. Digital circuits, particularly high speed CMOS (the HC family) can produce large spikes on the supplies. These spikes have wide spectral content.

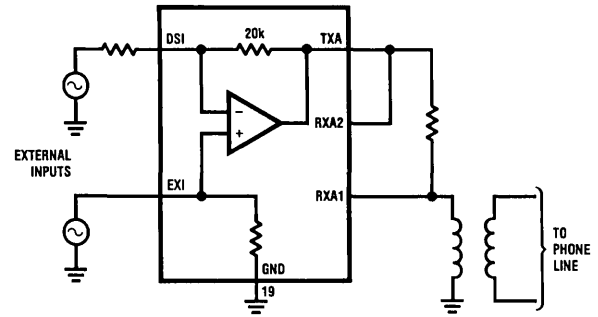
Ideally the modem could have its own supply. This may not be cost effective, so in some applications power supply filters may be necessary. These may just be RC filters but LC filters may be necessary depending on the extent of the supply noise. Miniature inductors in half watt resistor packages are cheap, lend themselves to automatic insertion, and are ideal for these filters.

It is difficult to set specifications for a "clean" supply because spectral density considerations are important. The following guidelines should be taken as "rule of thumb":

a) From 50 kHz to 20 MHz the ripple should not exceed −60 dBV.

b) From DC to 50 kHz the ripple should not exceed −50 dBV.

MM74HC942 Analog Interface



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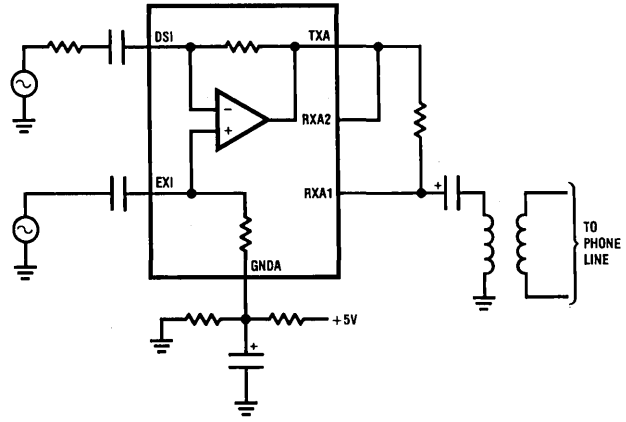
MM74HC943 Analog Interface



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CMOS 300 Baud Modem

National Semiconductor Corp.
Application Note 349
Anthony Chan
Peter Single
Daniel Deschene

INTRODUCTION

The advent of low cost microprocessor based systems has created a strong demand for low cost, reliable means of data communication via the dial-up telephone network. The most widespread means for this task is the Bell 103 type modem, which has become the de facto standard of low speed modems. This type of modem uses frequency shift keying (FSK) to modulate binary data asynchronously at speeds up to 300 baud.

The success of this type of modem, despite its modest transmission speed, is largely due to its ability to provide full duplex data transmission at low error rates even with unconditioned telephone lines. It also has a significant cost advantage over the other types of modems available today. Advances in CMOS and circuit design technology have made possible the MM74HC942—a high performance, low power, Bell 103 compatible single chip modem. This chip combines both digital and linear circuitry to bring the benefits of system level integration to modem and system designers.

THE PROCESS—microCMOS

The chip was designed with National's double poly CMOS (microCMOS) process used extensively for its line of PCM CODECs and filters. This is a self-aligned, silicon gate CMOS process with two layers of polysilicon, one of which is primarily used for gates of the MOS transistors. Thus there are three layers of interconnect available (two polysilicon and one metal layer) making possible a very dense layout.

The two polysilicon layers also offer a near perfect capacitor structure which is used to advantage in the linear portions of the chip. The self-aligned silicon gate P and N-channel MOSFETs combine high gain with minimal parasitic gate-to-drain overlap capacitance, facilitating the design of operational amplifiers with high gain-bandwidth product and excellent dynamic range.

CHIP ARCHITECTURE

The chip architecture was arrived at after critically evaluating several trial system partitionings of the Bell 103 type data set. The overriding goal was to integrate as much of the function as possible without sacrificing versatility and cost effectiveness in new applications. The resulting chip architecture reflects this philosophy. Since the majority of users of this device would probably be digital designers unfamiliar with filter design and analog signal processing, inclusion of these functions was thus mandatory. The precision filters needed for a high performance modem also make discrete implementations expensive. On the other hand, the majority of new systems will typically include a microprocessor which is quite capable of handling the channel establishment protocol. Besides, different systems may require different protocols. Circuitry for this task was therefore omitted.

A block diagram illustrating the chip architecture is shown in *Figure 1*. The on-chip line driver and line hybrid greatly simplify interfacing to the phone line by saving two external op amps. The output of the line hybrid, which is used to reduce

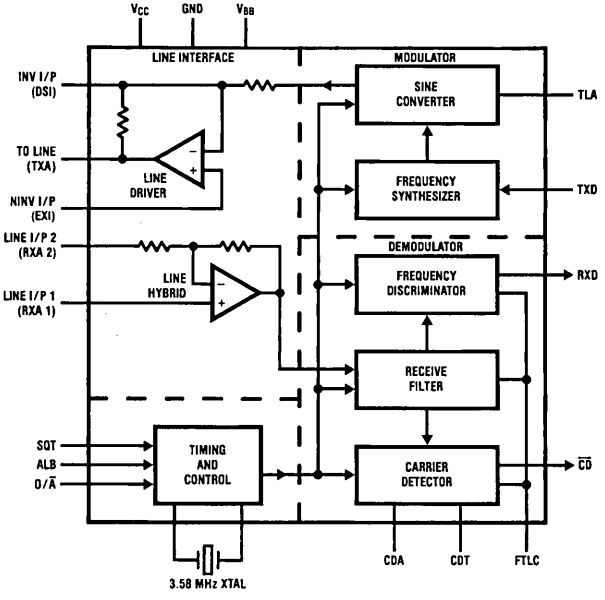

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FIGURE 1. Chip Architecture of the MM74HC942

Reprinted from Midcon/82

the effect of the local transmit signal on the received signal, goes to a programmable receive bandpass filter. This filter improves the signal-to-noise ratio at the input of the frequency discriminator, which performs the actual FSK demodulation. The output of the receive filter is also monitored by a carrier detector which compares the amplitude of the received signal to an externally adjustable threshold level.

The modulator consists of a frequency synthesizer which generates a clock at a frequency determined by the TXD (transmit data) and O/$\overline{A}$ (originate/answer) inputs. This is subsequently shaped by the sine converter into the final modulated transmit carrier signal.

All internal clocks and control signals are derived from an on-chip oscillator operating from a common 3.58 MHz TV crystal. On-chip control logic allows the modem to be set to answer or originate mode operation, or to an analog loopback mode via the O/$\overline{A}$ and ALB inputs respectively. The line driver can be squelched via the SQT input, which typically occurs during the channel establishment sequence.

Another feature of this design not obvious from the block diagram of *Figure 1* is that the chip can be powered down by asserting the ALB and SQT inputs simultaneously, a condition that does not occur during normal operation. This cuts power consumption to typically under 50 μA, making it very suitable for battery operation.

DEMODULATOR

Receive Filter

This is a nine pole, switched capacitor[1,2] bandpass filter. It is programmable by internal logic to one of two passbands, corresponding to originate or answer mode operation. The measured frequency response of the filter is shown in *Figure 2.* It shows that better than 60 dB of adjacent channel rejection has been achieved. Note also the deep notches at the frequencies of the locally transmitted tone pair.

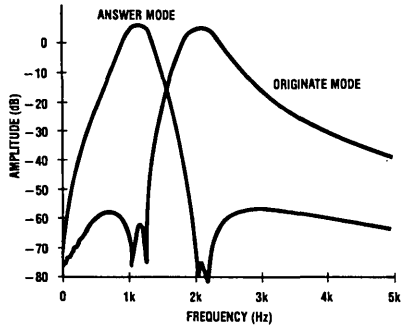

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FIGURE 2. Measured Frequency Response of the Receive Filter

A key design goal was to minimize the delay distortion of the filter. This has also been met as evidenced by the delay response curves shown in *Figures 3a* and *3b.* These curves have been normalized to the delays at 1170 Hz and 2125 Hz respectively. They show that the delay distortion in the 1020 Hz to 1320 Hz band is approximately 70 μs, while that in the 1975 Hz to 2275 Hz band is approximately 110 μs. These bands contain all the significant sidebands of a 300 baud FSK signal. The low delay distortion of the receive filter translates directly into low jitter in the demodulated data.

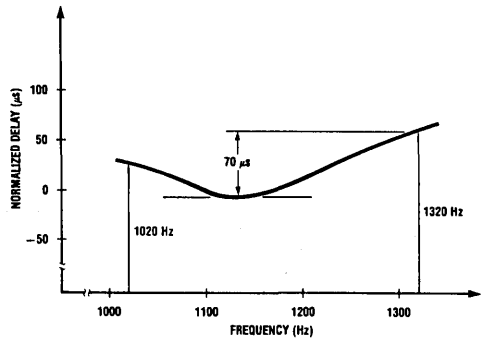

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FIGURE 3a. Normalized Delay Response of the Receive Filter in Answer Mode

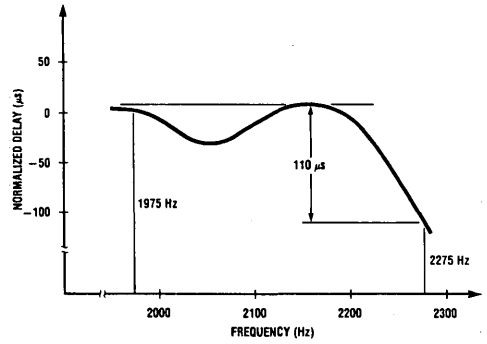

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FIGURE 3b. Normalized Delay Response of the Receive Filter in Originate Mode

An on-chip, second order, real time anti-aliasing filter precedes the receive filter. This masks the sampled data nature of the switched capacitor design from the user, contributing to the ease of use of the chip.

Frequency Discriminator

Referring to *Figure 4*, the filtered receive carrier is first hard limited to remove any residual amplitude modulation. It is then split into two parallel, functionally indentical paths, each consisting of a second order bandpass filter (BPF), a full wave detector and a post detection lowpass filter (LPF).

The bandpass filter in the upper path is tuned to the 'mark' frequency, and that in the lower path to the 'space' frequency. The detectors are full wave rectifier circuits which, together with the post detection filters, measure the energy in the mark and space frequencies. These are compared by the trailing comparator to decide whether a mark or space has been received.

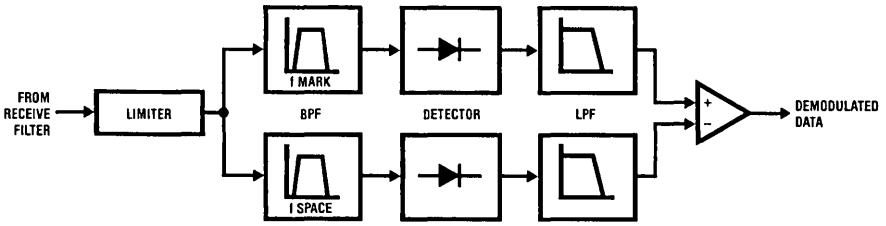

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FIGURE 4. Block Diagram of the Frequency Discriminator

Carrier Detector

The carrier detector compares the output of the receive filter against an externally adjustable threshold voltage. Referring back to *Figure 1*, if the CDA (carrier detect adjust) pin is left floating, the threshold is nominally set to ON at −44 dBm, and OFF at −47 dBm. This can be modified by forcing an external voltage at the CDA input. If the received carrier exceeds the set threshold, the $\overline{CD}$ (carrier detect) output will go low after a preset time delay. This delay is set externally by a timing capacitor connected to the CDT (carrier detect timing) pin.

MODULATOR

As shown in *Figure 5*, the modulator consists of a frequency synthesizer and a sine wave converter. The transmit data (TXD) and mode (O/$\overline{A}$) inputs set the divisor of a dual modulus programmable divider. This produces a clock at sixteen times the frequency of the transmitted tone. This then clocks a four bit counter, whose states represent the voltage levels corresponding to the sixteen time slots in one cycle of a staircase approximated sine wave. The sine ROM decodes the state of the counter and drives a digital-to-analog converter to synthesize the frequency shift keyed sine wave. This modulator design also preserves phase coherence in the transmit carrier across frequency excursions.

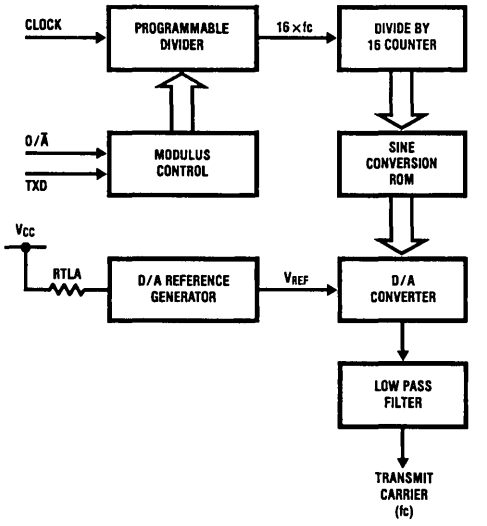

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FIGURE 5. Modulator Block Diagram

The reference voltage for the digital-to-analog converter is derived from a reference generator controlled by an external resistor (RTLA). This allows the transmit signal level to be programmable in accordance with the Universal Service Order Code. This code specifies the programming resistances corresponding to various transmit levels. If no external resistor is connected, the transmit level defaults to −12 dBm.

The synthesized sine wave is filtered by a second order, real time low pass filter to remove spurious harmonics before being fed to the line driver amplifier.

LINE INTERFACE

Line Driver

This is a class A power amplifier designed to drive a 600Ω line through an external 600Ω terminating resistor. With the proper transmit level programming resistor installed, it will drive the line at 0 dBm when operated from ±5V supplies. The quiescent current of the output stage of the driver varies with the programmed transmit level to maximize the efficiency of the amplifier. A class A design was chosen mainly because it can tolerate a wider range of reactive loads.

As shown in *Figure 6*, both inverting and non-inverting inputs of the driver amplifier are accessible externally, making it easy to accommodate an external signal source, such as a tone dialer. An external capacitor can also be connected between the inverting input and the amplifier output to give it a lowpass response.

Line Hybrid

The line hybrid is essentially a difference amplifier which, when connected as shown in *Figure 6*, causes the transmit carrier to appear as common-mode signal and be cancelled from the output. If the termination resistor (R_T) and phone line impedance are perfectly matched, the output of the line hybrid would be just the received carrier. In practice, perfect matching is impossible and 10 dB to 20 dB of transmit carrier rejection is more realistic. The residual is more than adequately rejected by the receive filter of the demodulator.

TIMING AND CONTROL

This includes an oscillator amplifier, divider chain and internal control logic. The oscillator, in conjunction with an external 3.58 MHz TV crystal and the divider chain, provides all the internal clocks for the switched capacitor circuits and the frequency synthesizer. The control logic orchestrates the various operating modes of the chip (e.g., originate, answer or analog loop-back modes).

APPLICATIONS

Figure 7 shows the MM74HC942 in an acoustically coupled modem application. It demonstrates the simplicity of the resulting design and a dramatic reduction in parts count. *Figure 8* shows two typical direct connect modem applications. The simplicity of these circuits is again evident.

The simple power supply requirement (±5V), low power (60 mW when transmitting at −9 dBm, 0.5 mW standby) and low external component count makes the MM74HC942 an efficient implementation of the 300 baud modem function.

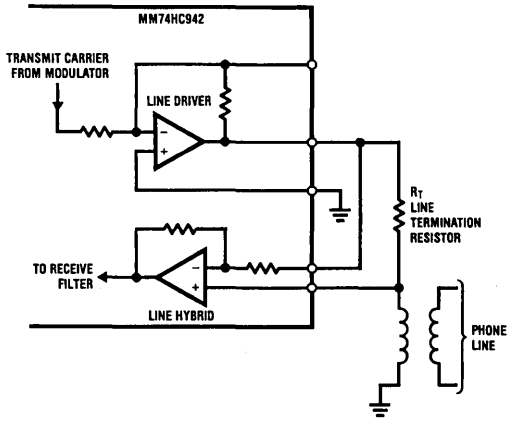

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FIGURE 6. Typical Interface Between the MM74HC942 and the Phone Line

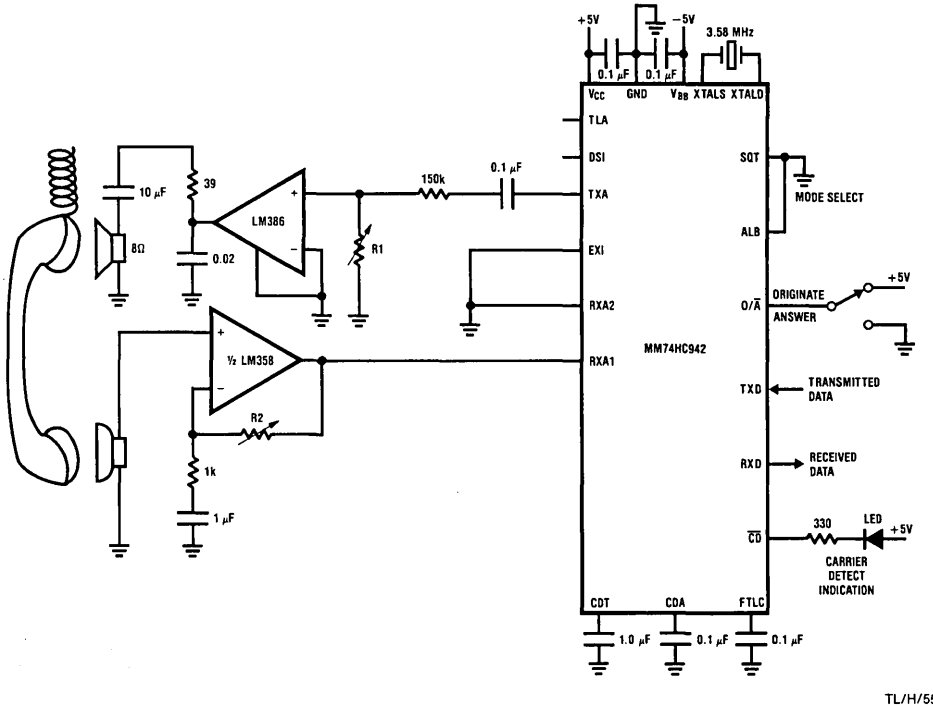

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FIGURE 7. Typical Implementation of an Acoustically Coupled Modem Using the MM74HC942

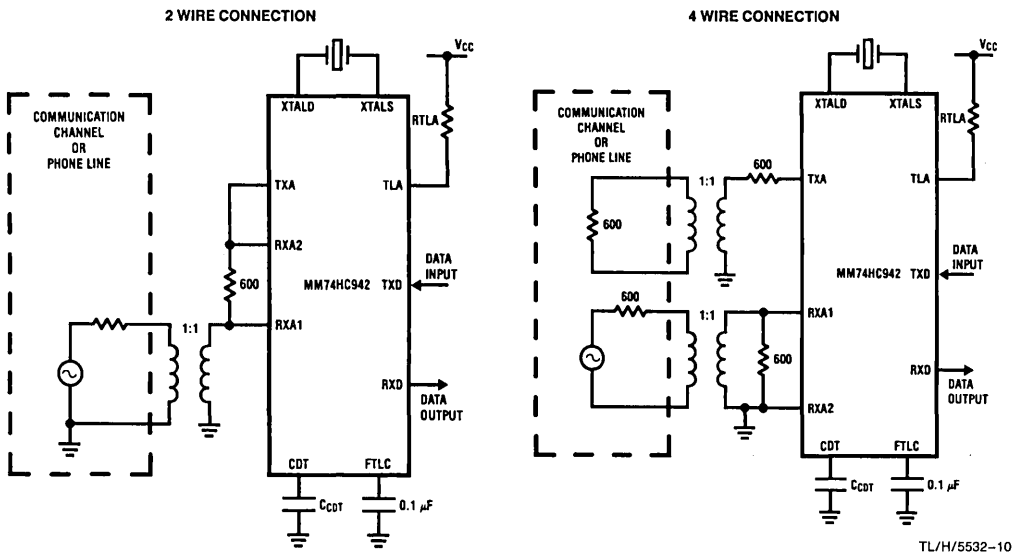

FIGURE 8. Typical Implementations of Direct Connect Modems Using the MM74HC942

SUMMARY

In conclusion, the MM74HC942 integrates the entire data path of a Bell 103 type data set into a 20-pin package with the following features:

- On-chip 9 pole receive filter
- Carrier detector with adjustable threshold
- Analog demodulator with low bit jitter and bias
- Phase coherent modulator with low spurious harmonics
- 600Ω line driver with adjustable transmit level
- On-chip line hybrid
- Full duplex originate or answer mode operation
- Low power operation, power-down mode
- Simple supply requirements (±5V)

REFERENCES

1. J. Caves et al., "Sampled Analog Filtering using Switched Capacitors as Resistor Equivalents", *IEEE Journal of Solid State Circuits,* Vol. SC-12, No. 6, Dec. 1977

2. W. Black et al., "A High Performance Low Power CMOS Channel Filter", *IEEE Journal of Solid State Circuits,* Vol. SC-15, No. 6, Dec. 1980.

Techniques for Designing with Codec/Filter Combo Circuits

National Semiconductor Corp.
Application Brief
Chris Stacey

PCM CODEC/Filter Combo devices are complex analog and digital sub-systems on a single chip. They contain, for example, an A/D and a D/A converter, each with 13 bit (for u-law) resolution at low signal levels on the bottom chord of the companding characteristic. The TP3050/60 family of microCmos Combos are, however, capable of providing extremely high performance even in the unfriendly electrical environment of a multi-channel subscriber line card so long as the printed circuit board is carefully designed as an integral part of the system. Indeed, this family can achieve performance superior to that of other 1 or 2 chip CODEC/Filter circuits due to two key factors;superior Power Supply Rejection Ratio, particularly at high frequencies, and the fact that the critical connection between the transmit filter and the encoder is carefully shielded inside the device. Nevertheless, the following guidelines should be adhered to in order to maintain this high performance in any switching or transmission system.

GROUND AND POWER SUPPLY LAYOUT

1. Different techniques are necessary for the layout of analog circuits on the card (Combo, SLIC and any external gain sections) and the digital control and switching circuits. Use the GNDA pin of each Combo device as the Ground Reference Point (GRP) for each channel. All ANALOG ground connections for each channel should connect as close as possible to the reference point. This includes:
   a. The analog ground from the 4-wire side of the SLIC circuit.
   b. The ground for the transmit op amp connection.
   c. The ground side of the 0.1 μF decoupling capacitors for the +5V and −5V Combo power supplies.
   d. The analog ground for any external gain or loss adjustment stage.
2. Ground return currents from logic circuits, relays and other audio channels must not flow into or out from the channel GRPs to avoid generating noise voltages. Therefore a separate ground return should be run from each channel GRP to a common point close to the ground pin on the card connector, commonly called the MECCA. Thus there is a STAR formation from the MECCA to each channel GRP. It is NOT recommended to run separate analog and digital ground returns to the shelf power supply. Relays and other circuits operating from the station battery should, however, have a separate return bus to the battery ground.
3. Decouple the +5V and −5V power supplies to the MECCA close to the card connector. A minimum of 10 μF should be used for each supply, and a capacitor type with a low Effective Series Resistance should be selected. Beware of the effects of the inrush current charging these capacitors as the card is plugged into a "hot" socket. This current flowing through the wire and trace inductance can cause voltage spikes which easily exceed the absolute maximum ratings of various devices on the card and may even damage the connector contacts. The trace length from the connector to the capacitors should be kept short, and excessive values of decoupling capacitor avoided.
4. The +5V and −5V supply busses to the Combo circuits should be routed adjacent to a ground bus to help ensure that any r.f. noise pick-up is common mode. Each supply must be decoupled by 0.1μF capacitors with short traces to the GRP of each Combo. Ceramic capacitors are best for good high frequency decoupling.
5. The +5V bus for the switching and control logic circuits should be a separate connection from the decoupled point close to the card connector. It should not share any common path with the +5V connection to the Combo circuits. Each logic circuit should be decoupled with a 0.01 μF ceramic capacitor from +5V to ground close to the device.
6. The ground connections for the logic circuits and low voltage relays may use a ground bus or, better still, a ground grid system to maintain good noise margins on digital signals. This logic ground should connect directly to the card MECCA such that logic ground currents do not share common paths with any channel GRP returns.
7. TTL and LSTTL logic families draw considerably different supply currents when their outputs are in the high and low logic states, causing large switching currents to flow through the busses and decoupling capacitors. In contrast, CMOS logic circuits only draw significant currents during state transitions, and these currents are substantially balanced. A CMOS logic system therefore generates far less electrical noise than a similar TTL System.

   The use of the 74HC CMOS logic family is highly recommended for line card design. It helps to preserve high transmission performance in the analog circuits and offers better noise margins than TTL in the presence of transient voltages induced by relays and ringing signals.

NOISE CONSIDERATIONS

1. Logic signals should be routed well away from the analog circuits and their power supply connections wherever possible to minimize high frequency noise being capacitively coupled into the channel and aliased down into the audio passband by the sampling action of the filters and encoder.
2. All signals and circuits capable of inducing large emf's into the audio signals should be located around the edge of the card wherever possible. This includes:
   a. Relay drive and output signals
   b. Ringing distribution
   c. The 2-wire side of the SLIC circuits.
   d. −48V battery
   e. d.c. to d.c. converters
3. Ground planes may be used to shield audio signals from noise sources such as clock and data signals and the high voltages listed above. A ground plane is only effective, however, if it carries NO NOISE-INDUCING CURRENTS itself. A single point connection from the ground plane to a quiet return is the best way to assure this.
4. The transmit op amp connections become a potential noise source particularly if a high gain is required. The feedback resistor value should not exceed 50K ohms, and the bodies of the feedback and input resistorsshould

be close to the op amp input to minimize capacitive noise pick-up.

5. In asynchronous applications (typically transmission systems) the best idle channel noise and signal/distortion performance will be achieved if the transmit and receive filters are clocked synchronously. Thus the $MCLK_R$/PDN input on the TP3050/60 Combo devices should either be connected to $MCLK_X$ or controlled solely by logic signals as a PDN input only (the Combo will automatically use $MCLK_X$ internally). Note that $MCLK_R$ does not need to be synchronized to $BCLK_R$ and FS_R.

CIRCUIT PROTECTION

CMOS CODEC/Filter Combos are capable of providing extremely reliable and stable long-term performance provided a few simple precautions are followed:

1. Normal CMOS handling techniques should be used to prevent build-up of static charge on the device. These include the use of conductive carriers, and grounding personnel while handling devices.
2. Ensure that ground is always connected to each device before any other supplies or signals. An extended ground pin should be used on line card connectors.
3. Buffer all digital input and output signals between Combo circuits and the line card backplane. This both protects the Combo circuits from backplane transients and preserves good logic signal transition times and noise margins.
4. CMOS inputs, outputs and supply connections must be protected against even momentary transitions outside the supply voltages. Schottky diodes should be fitted on each card between +5V and GND, and between GND and −5V to clamp transient power supply reversals during power-up. Type 1N5820 is a good choice.
5. If the Combo circuit is connected to a transformer-type of SLIC circuit additional protection is required against line transients. An input resistor of 5K ohms or more is adequate to protect the transmit op amp inputs, VF_XI^+ and VF_XI^-. If this is not possible, silicon diodes or a pair of back-to-back 3.9V zener diodes (depending on the required dynamic range) should be connected between the vulnerable input and GND.
6. A pair of back-to-back 3.9V zener diodes may also be necessary to protect the receive power amplifier output(s). Select a zener type with a sharp "knee" on the V-I characteristic, and low leakage current at voltages below the knee to avoid impairing the gain-tracking of the receive channel at high signal levels.

Figure 1 illustrates an idealized circuit card layout embodying many of the above techniques. While space constraints may limit the application of some of these techniques, the closer they can be followed, the better the system performance will be.

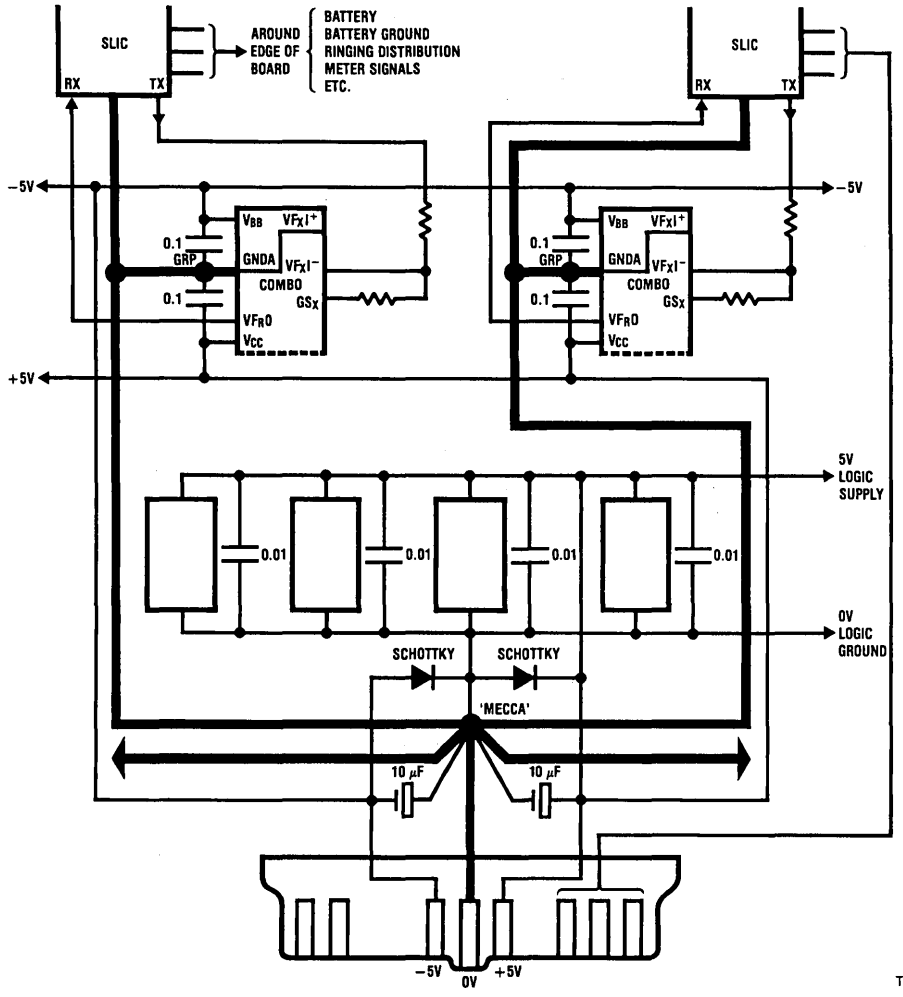

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FIGURE 1. Suggested Combo PCB Layout

1. Use **'STAR'** Connection For Each Channel To The **'CHANNEL GRP'** At GNDA (Pin 2)
2. Use **'STAR'** Connections From Each **'CHANNEL GRP'** To The PCB **'MECCA'**

TP3200 MC-SLIC Application Guide

National Semiconductor Corp.
Application Note 439
T. K. Chin
John Shaw

INTRODUCTION

In a Central Office or Private Branch Exchange, each subscriber's telephone line is interfaced to the switching equipment through a Subscriber Line Interface Circuit (SLIC) on the line card. To integrate the SLIC function has been a challenge for IC designers. The requirements for the SLIC function are very stringent in that they involve an environment of 48V battery feed and up to 150 Vrms of ringing voltage on the line, not to mention the ability to withstand 1500V lightning surges. Another particularly difficult problem to solve is the maintenance of a good longitudinal balance against common mode current induced by adjacent power cables.

Several implementations of an all-monolithic SLIC have been demonstrated, although they require a somewhat expensive high voltage process and involves tradeoffs in performance. A transformer-based SLIC, on the other hand, offers the most cost-effective and reliable solution for many applications.

The TP3200, TP3202 and TP3204 Magnetic Compensation SLIC are intended to reduce both the size and cost of implementing the SLIC while retaining all the advantages of a transformer-based design. The MC-SLIC also provides on-chip supervision and ring trip functions together with three relay drivers with latched inputs.

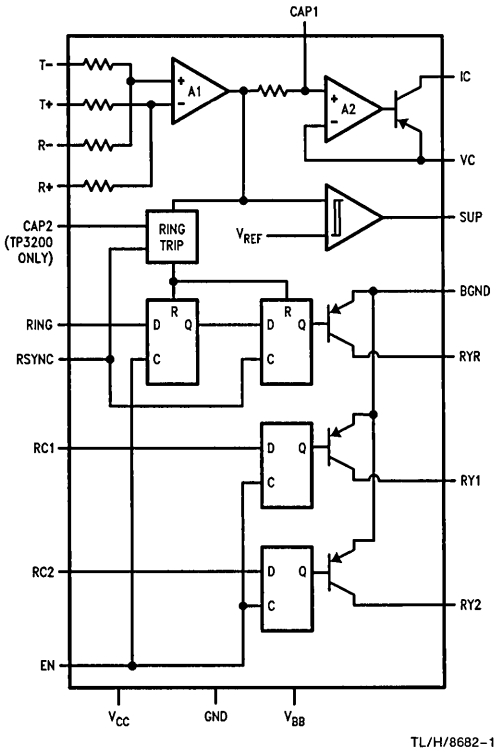
This applications note provides line card designers with a thorough understanding of the device's operation as well as some application hints that are useful to the circuit designer.

A block diagram illustrating the device's architecture is shown in *Figure 1*. TP3200 and TP3202 are designed with PNP relay drivers, while TP3204 is designed with NPN relay drivers.

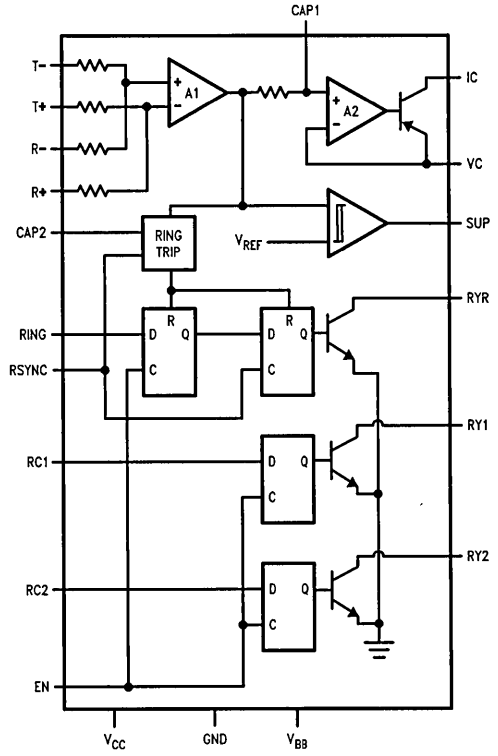
MAGNETIC COMPENSATION

The TP3200 family of MC-SLIC's reduces the size of the line interface transformer by using a flux cancellation technique. The device senses the loop current magnitude by means of a differential amplifier A1 (see *Figure 2*) and an on-chip high precision sensing resistor bridge across the external feeding resistor pair Rs.

The output of the amplifier A1 produces a voltage proportional to the instantaneous loop current. And the low pass filter formed by R1 and external capacitor CAP1 prevents the AC component of the loop current from disturbing the



TP3200 and TP3202



TP3204

FIGURE 1. Simplified Block Diagram

flux cancellation. For a typical CAP1 of 1 μF, the cutoff frequency is approximately 2 Hz.

The voltage follower A2 and output transistor Q1 reproduce a voltage at VC output, proportional to the average DC loop current. A resistor R_L connected from VC to GND creates a current flow from the IC pin into the compensation winding of the transformer. By proper selection of R_L and the transformer winding ratio, the flux created by the compensation current can exactly cancel the flux produced by the DC loop current. The output current source requires a high output impedance at IC (typically 5 MΩ) in order to ensure that the reflected impedance from the compensation winding to the line will not create a loading effect on the line impedance. The IC pin should be connected to the finish of the compensation winding in order to reduce the capacitive loading of the transformer, thereby, increasing the effective reflected impedance from the compensation winding. It is recommended to connect R_L and CAP1 to the same ground point in order to prevent ground noise from injecting into the subscriber loop via the compensation winding.

With the DC flux removed, the hybrid transformer can be wound on a small ferrite core without an air gap, yet can maintain a large inductance without running into magnetic saturation.

Figure 2 shows a simplified schematic of the magnetic compensation circuit and *Figure 3* is a plot of V_C versus the loop current.

Equations relating to the magnetic compensation circuit are:

$$V_C = A_V \times 2 \times R_S \times I_{LOOP} \quad (1)$$

$$I_C = V_C/R_L$$

$$= A_V \times 2 \times R_S \times I_{LOOP}/R_L \quad (2)$$

For perfect flux cancellation,

$$I_{LOOP} \times 2 \times N_P = I_C \times N_C$$

or,

$$R_L = A_V \times R_S \times N_C/N_P \quad (3)$$

The reflected impedance from the compensation winding is:

$$Z_C = R_{IC} \times (2N_P/N_C)^2$$

$$CAP1 = 1.6/f\ \mu F$$

Where R_{IC} is the output impedance at IC, f is the upper cutoff frequency.

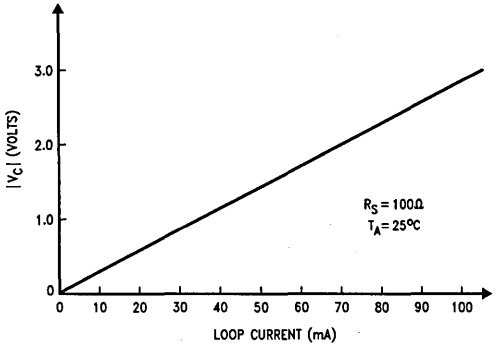


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FIGURE 3. V_C Output vs Loop Current

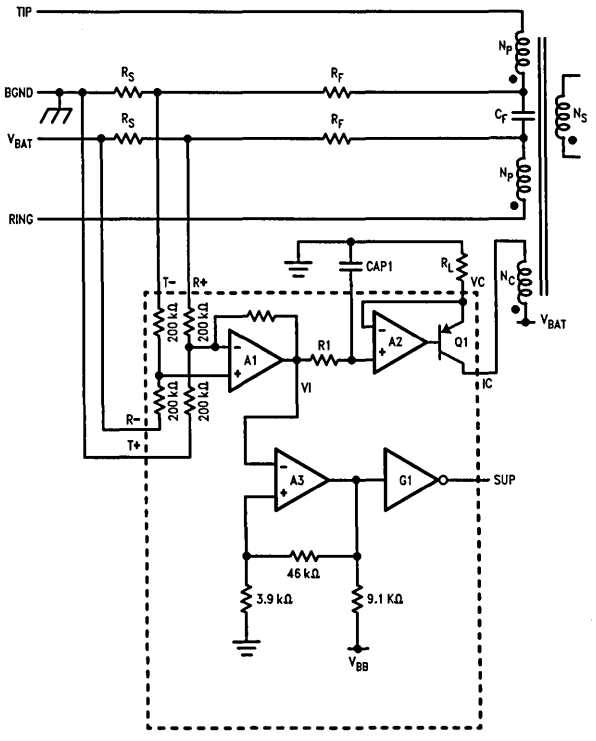

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FIGURE 2. Magnetic Compensation and Supervision Circuit

SUPERVISION

The supervision circuit of the TP3200 family consists of a loop current comparator with hysteresis. It provides status information on off-hook detection, dial pulse replication and ring-trip detection.

Referring back to *Figure 2*, the input to the comparator A3 is taken from the output of amplifier A1, which represents the instantaneous loop current. In the on-hook condition, the SUP output is at logic high. When the loop current rises above 13 mA, the SUP output switches low, indicating off-hook. When the loop current falls below approx. 11 mA, the SUP output will go high, indicating an on-hook condition. These comparator thresholds are selected so that in the extreme case of a very short loop, any possible cable leakage will not be misinterpreted as an off-hook. At the other extreme of a very long loop, there is enough safety margin for reliable detection of off-hook for very weak loop current of less than 15 mA.

During pulse dialing, the loop current changes from 0 mA during the break period and goes back to normal magnitude during the make period. The SUP output will produce a logic-replication of the dial pulses. However, under the worst case condition of a line loaded with 5 ringers, and with a cable leakage of 15 kΩ, the heavy capacitive loading of the ringers will cause excessive delay in loop current decay during break interval, creating dial pulse distortion. This results in shortening of the break period as reflected at the SUP output. *Figure 4* shows the relationship between SUP and the loop current under this condition.

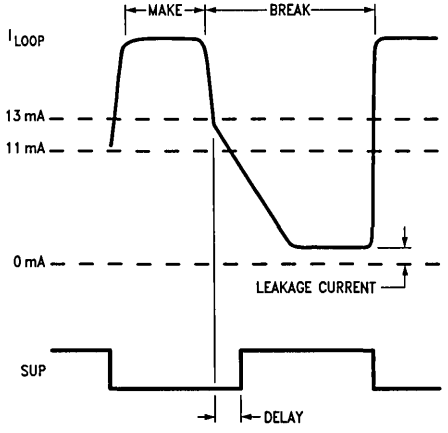

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FIGURE 4. SUP Output Under 5 Ringers and 15 kΩ Cable Leakage

To repeat these dial pulses through the switching system, a software routine is recommended to be included in the call-control processor, which monitors the SUP output and reconstructs the dial pulses in the appropriate break-make ratio.

During ringing, the comparator A3 will detect the instantaneous AC ringing current through the loop and create a waveform at SUP output. During on-hook, the waveform is a square wave with a mark-to-space ratio of larger than 50%. When the telephone goes off-hook, the DC loop current superimposed on the AC ringing current will cause the comparator to generate a waveform with less than 50% duty cycle. This change in duty cycle can be easily monitored by the call-control processor as a test for ring-trip.

This is the most flexible way to detect ring-trip as it is independent of the ringing frequency. However, the CPU must be fast enough to make the detection within 200 mS.

AUTOMATIC RING-TRIP

The automatic ring-trip circuit consists of a ring-trip detection circuit and a double-latched ring relay driver. *Figure 5* shows a simplified schematic diagram.

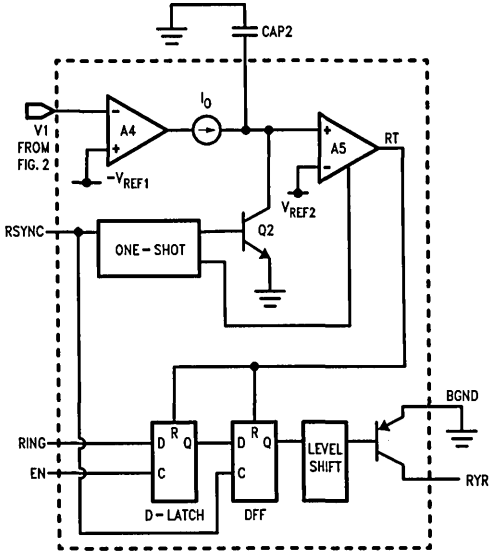

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FIGURE 5. Automatic Ring-Trip Circuit

Based on the state of the RING input, the D-latch is set or reset while the strobe EN is active high, and latched on the falling edge of EN. RSYNC is the clock input to the ring flip-flop. It is driven by the output of the external zero-crossing detector of the ringing voltage on the line. Based upon the state of the output of the D-latch, the ring flip-flop is set or reset at the rising edge of RSYNC. This scheme ensures that the ring relay is turned on or off near the zero crossing of the ringing current to prevent arcing and minimize relay contact wear.

The ring-trip circuit takes its input from the output of amplifier A1, which represents the instantaneous AC ringing current superimposed on the DC off-hook loop current. The comparator A4 compares this instantaneous loop current against a threshold equivalent to approximately 12 mA. Depending upon the polarity of the comparator's output, the constant current source I_O either sources or sinks 10 μA into CAP2. This results in charging and then discharging CAP2 in each ring cycle. Depending on the duty cycle of the output from A4, this charging and discharging process creates a resultant voltage on CAP2 after one ringing cycle, which is then compared against a threshold of about 50 mV at comparator A5. When the DC loop current increases to above 12 mA, the duty cycle of the output of amplifier A4 is less than 50%. The resultant voltage at CAP2 after a

complete ring cycle then exceeds the 50 mV threshold. As a result, the A5 amplifier generates an output at the next rising edge of RSYNC, which resets the ring latches.

Each positive transition of RSYNC enables the comparator A5 for 20 μS via the one-shot circuit, after which CAP2 is discharged to GND for 100 μS via Q2 to ensure that CAP2 always charges up from 0V. The reset pulse from A5 will always appear at the rising edge of RSYNC to ensure that the ring relay is reset at the zero-crossing of the ringing current. *Figure 6* shows the timing diagram for ring-trip.

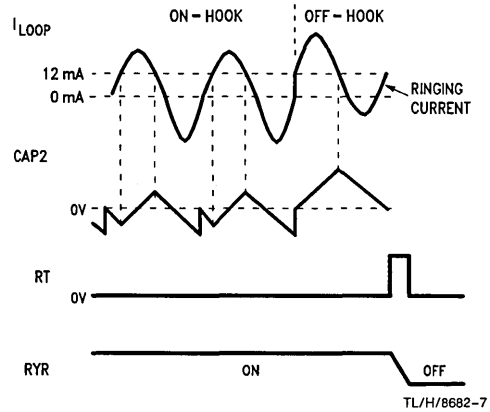

FIGURE 6. Timing Diagram for Ring-Trip

CAP2 is selected such that the constant current source I_O (approx. 10 μA) when integrated over half of one ringing cycle, will not create a charging voltage at CAP2 exceeding ±3V. A 0.1 μF is recommended for ringing frequency range of 16 Hz to 40 Hz, and 0.033 μF for 30 Hz to 70 Hz.

The automatic ring-trip circuit provides a reliable ring-trip detection. Normally, one ring cycle is needed for detection, and the second ring cycle to generate the reset pulse. The worst case ring-trip detection time will be within 3 ringing cycles. If the SUP output is used to detect ring-trip externally, the input at CAP2 should be grounded. Or the TP3202 could be used.

The RING or EN inputs should be kept at logic low after the ring relay is turned on in order to prevent relay chattering when the loop current is near to the 12 mA threshold. This is the condition where the automatic ring-trip tries to turn off the ring relay and the RING and EN inputs try to turn it on again. This results in relay chattering which may cause damage to the relay.

COMPENSATION ACCURACY

The accuracy of flux cancellation is one of the critical factors determining the size of the hybrid transformer. On chip Si-chrome resistors are used for the sensing resistor bridge to ensure high accuracy in loop current tracking. The offset voltage at V_C is zener trimmed to within 30 mV to further minimize the compensation error.

The tolerances of resistors R_S and R_L also contribute to compensation error. The feeding resistors R_S, however, are normally matched to each other to within ±0.1%, as are feeding resistors R_F, to ensure 60 dB longitudinal balance.

The following table shows a list of parameters that contribute to compensation errors:

Parameter	Typical	Tolerance
A_V	0.15 V/V	2%
V_{OS}	0	30 mV
R_S	100Ω	0.1%
R_L	150Ω	0.5%
N_C/N_P	10	0.05%

From Equation 2 above, the compensation error can be derived as follows:

Compensation

$$\text{Error} = I_{LOOP} - I_C \times N_C/2N_P$$
$$= I_{LOOP} - (N_C/2N_P) \times (A_V \times 2R_S \times I_{LOOP} \pm V_{OS})/R_L$$
$$= (1 - N_C/N_P \times A_V \times R_S/R_L) \times I_{LOOP} \pm V_{OS}/R_L$$
$$= \pm(0.026 \times I_{LOOP} + 0.2)\ \text{mA} \quad (4)$$

For a maximum loop current of 100 mA for Central Office application, the worst case compensation error is ±2.8 mA. For a maximum loop current of 60 mA for PBX application, the worst case compensation error is ±1.8 mA. The ferrite material of the hybrid transformer must be able to handle this uncompensated DC current before magnetic saturation starts.

TRANSFORMER DESIGN

The size and design of the hybrid transformer is influenced by the following factors:

1. Low frequency Return Loss, which in turn determines the minimum inductance of the primary windings.
2. The worst case compensation error, which determines the ampere-turn before magnetic saturation occurs.
3. The permeability and magnetization characteristics of the ferrite material.
4. Insertion loss and frequency response.

Figure 7 shows a simplified equivalent circuit for a hybrid transformer. r_p and r_s are the coil resistance of the primary and secondary windings. R_T and C_T are the terminating impedances of the secondary winding, and L is the total primary inductance. As the compensation winding is driven by a high impedance current source, it can be ignored from the equivalent circuit.

The return loss against a reference impedance Z_O can be calculated from the equation:

$$\text{Return Loss} = 20 \log \left| \frac{Z_I + Z_O}{Z_I - Z_O} \right|$$

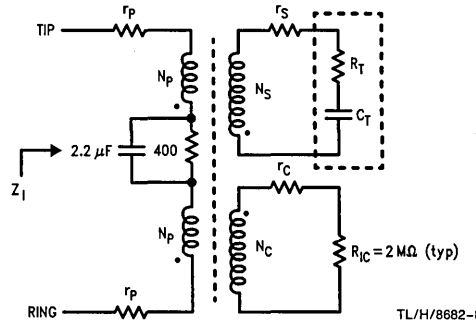

FIGURE 7. Simplified Equivalent Circuit of Hybrid Transformer

Figure 8 is a plot of return loss against a reference impedance of 600Ω + 2.16 μF. To achieve a 20 dB return loss, it can be seen from the plot that it requires a primary inductance of more than 0.8H even under the worst case compensation error of 2.8 mA. An acceptable ferrite is Siemens RM8-T35 ferrite core with a typical inductance factor of 8400 nH/T^2. Following similar calculation, it can be found that it requires a minimum primary inductance of 1.4H in order to achieve a 20 dB return loss against a reference impedance of 900Ω + 2.16 μF. A suitable ferrite is Siemens RM10-T35 ferrite core with a typical inductance factor of 11000 nH/T^2.

To ensure a 60 dB longitudinal balance, the two primary windings must be carefully wound for symmetry. Usually this is done by winding the two primary windings with bifilar wires of the same gauge. Furthermore, to prevent heating up the ferrite core for a 0 K ft loop, the primary resistance has to be kept to a minimum and is recommended to be below 30Ω.

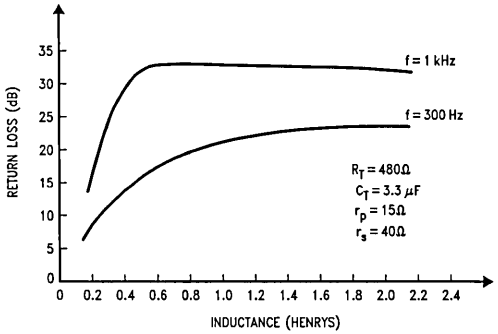

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FIGURE 8. Return Loss Against 600Ω + 2.16 μF

OUTPUT BIASING

The AC line voltage across the subscriber loop will appear at the IC output and is amplified by the turns ratio $N_C/2N_P$. A suitable DC bias voltage must be provided for the compensation winding to ensure sufficient swing for the AC signals.

At minimum loop current (see *Figure 9a*), the DC bias at IC must be sufficiently positive with respect to the zener voltage to allow negative swing without clipping. Thus:

$$I_{CMIN} \times (R_C + r_C) > N \times V_P - (V_{ZMIN} - |V_{BAT}|_{MAX})$$

or,

$$(R_C + r_C) \times I_{LOOPMIN}/N > N \times V_P - V_{ZMIN} + |V_{BAT}|_{MAX} \quad (5)$$

Where, V_{ZMIN} is the minimum zener voltage at IC

V_{BATMAX} is the maximum battery voltage

R_C is the filtering resistor for the compensation winding

r_C is the coil resistance of the compensation winding

N is the transformer turn ratio $N_C/2N_P$

V_P is the AC peak voltage swing across Tip and Ring

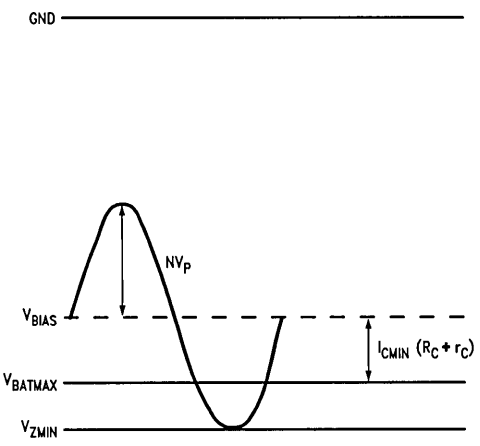

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FIGURE 9a. IC At Minimum Loop Current

At the other extreme with maximum loop current (see *Figure 9b*), the output transistor must not be saturated at the positive peak swing at IC. This requires:

$$|V_{BAT}|_{MIN} > I_{CMAX} \times (R_C + r_C) + V_{CMAX} + |V_{ICSAT}| + N \times V_P$$
$$> (R_C + r_C)\, I_{LOOPMAX}/N + I_{LOOPMAX} \times 2R_S \times A_V + |V_{ICSAT}| + N \times V_P \quad (6)$$

Substituting for (R_C + r_C) from equation 5:

$$|V_{BAT}|_{MIN} > (N \times V_P - V_{ZMIN} + |V_{BAT}|_{MAX}) \times I_{LOOPMAX}/I_{LOOPMIN} + I_{LOOPMAX} \times 2R_S \times A_V + |V_{ICSAT}| + N \times V_P$$

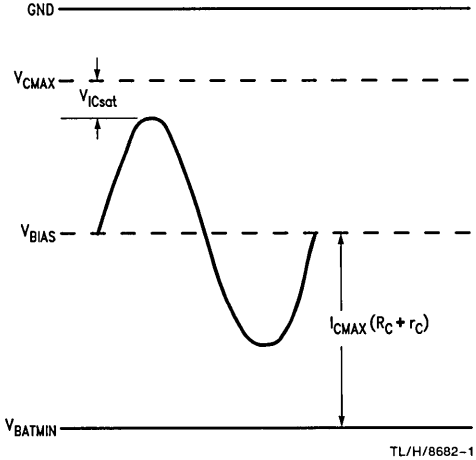

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FIGURE 9b. IC At Maximum Loop Current

The maximum current range of IC of 25 mA places a constraint on the minimum compensation to primary turn-ratio of the transformer.

$$N = N_C/2N_P$$
$$= I_{LOOP}/I_C$$

Thus,

$$N_{MIN} = I_{LOOPMAX}/25 \quad (7)$$

To allow for a +3 dBm line signal over loop current from 20 mA to 100 mA, with a zener voltage of 62V ±5%, and battery voltage of −42V to −54V, the compensation turn ratio and total resistance ($R_C + r_C$) can be calculated from the above equations and is shown in the following table:

	Line Impedance	
	600Ω	900Ω
Minimum N	4.0	4.0
Maximum N	6.67	5.45
Minimum ($R_C + r_C$) for N = 5	712.5Ω	1143.8Ω
Maximum ($R_C + r_C$) for N = 5	1487.5Ω	1401.3Ω

INPUT COMMON MODE RANGE

Consideration should be given to the various subscriber line voltages and currents, such that the magnetic compensation circuitry only operates within its dynamic range.

The A1 amplifier's differential input is biased using negative feedback so that it works within the range of V_{BB} + 0.5V to V_{CC} − 1V, where V_{CC} = +5V ±5%, and V_{BB} = −5V ±5%. The input common mode voltage V_{IN} is given by the following expression:

$$V_{IN} = 0.0155 \times (V_{BAT} + V_R \sin wt + 2R_S \times I_{CM}) - 0.05R_S \times (I_{LOOP} + I_R \sin (wt + A)) \quad (8)$$

where, V_{BAT} is the battery voltage

I_{LOOP} is the DC loop current

V_R is the peak ringing voltage

I_R is the peak ringing current

I_{CM} is the peak longitudinal current of arbitrary phase

It should be noted that for short subscriber loops, the component of voltage at V_{IN} due to the ringing current is in antiphase to the ringing voltage. For longer loops, the phase angle A between the ringing voltage and the ringing current increases. Thus the resulting voltage for V_{IN} will be a vector summation. Under the latter condition, however, the subscriber loop resistance is greater, which will reduce I_{LOOP} and I_R, and consequently reduce their influence on V_{IN}.

As an example, consider an application with V_{BAT} = −48V, V_R = 110V rms at 60 Hz, I_{LOOP} = 100 mA, I_{CM} = 30 mA peak, and a ringer impedance of 2 kΩ + 4.7 μF. During on-hook ringing, the voltage swing at V_{IN} can be derived from equation (8) as follows:

$$-2.93V < V_{IN} < 1.45V$$

When the telephone goes off-hook, and at the point before ring trip, the voltage swing at V_{IN} becomes :

$$-2.86V < V_{IN} < 0.38V$$

This reduction in voltage swing is due to the small phase angle A and the increase of AC ringing current.

OVER-VOLTAGE PROTECTION

The TP3200 family has been designed on a standard 70V bipolar process requiring no expensive dielectric isolation. In fact, any possible line transient voltage is scaled down through the feeding resistors R_S and R_F, insuring that the device will never see more than one half of the line transient. However, to prevent excessively high transient voltage induced by lightning or from nearby power cables, it is essential to provide some protective device across Tip and Ring. It is recommended to put a 10Ω current-limit resistor and a 300V peak transcient suppressor from Tip to GND and from Ring to GND.

Moreover, any transient voltage on the line will also be reflected into the compensated winding as well as the secondary winding. Such a transient in the compensation winding is especially significant as it is boosted up by the turn ratio $N_C/2N_P$. A fast actuating 62V zener diode is necessary to connect from IC output to GND for protection. On the secondary winding, two 3.9V zener diodes connected back-to-back will insure the COMBO will never see any transient voltage exceeding its supply voltages.

The on-chip relay driver has been designed to sink 30 mA for TP3200 and TP3202, and 80 mA for TP3204. When the relay is turned off, the back emf in the coil winding may possibly cause damage to the output driver. Each relay driver should be protected by a rectifier diode connected close to the relay coil in order to dissipate the stored energy in the coil.

A TYPICAL LINE CARD

Figure 10 shows a typical line card architecture with 16 subscriber lines. The on-chip receive power amplifier and transmit buffer amplifier of the TP3051/56 COMBO is connected as a simple 2-to-4 wire converter. To provide sufficient swing to +3 dBm to the line, a 900: 600Ω hybrid transformer is used. This ensures that the receive output VFrO of the COMBO will always drive a 600Ω load at less than 3V peak to peak.

Ringing voltage is inserted into the line by breaking the battery feed path and superimposing the AC ringing voltage via a 4-pole relay connected to RYR output. To prevent the feed decoupling capacitor from shunting the ringing current, a break contact is placed in series with C_F. Furthermore, to prevent the primary windings from attenuating the ringing voltage or introducing distortion, make contacts are connected in shunt with the transformer primary. The two general purpose relay drivers RY1 and RY2 can be used to control battery reversal and testing by connecting to 2-pole relays.

The DLIC TP3110/20 controls the flow of data between each subscriber COMBO and the TDM highways. Typically they run at 2.048 Mb/s with 32 64 Kb/s channels, or at 1.536 Mb/s with 24 64 Kb/s channels. All time slot assignments are loaded by the line card microprocessor into a RAM, know as the Time-Slot Map on the DLIC to provide non-blocking access to as many as 128 channels on these highways.

The line card microprocessor is typically from the INS 8048 family. It controls the COMBO's through the DLIC's interface register, and controls each SLIC by scanning the digital inputs (RING,RC1,RC2 and EN) and SUP output via the P1 and P2 ports.

For additional information on design of a suitable zero crossing detector, see National Semiconductor Linear Application Note AN-74.

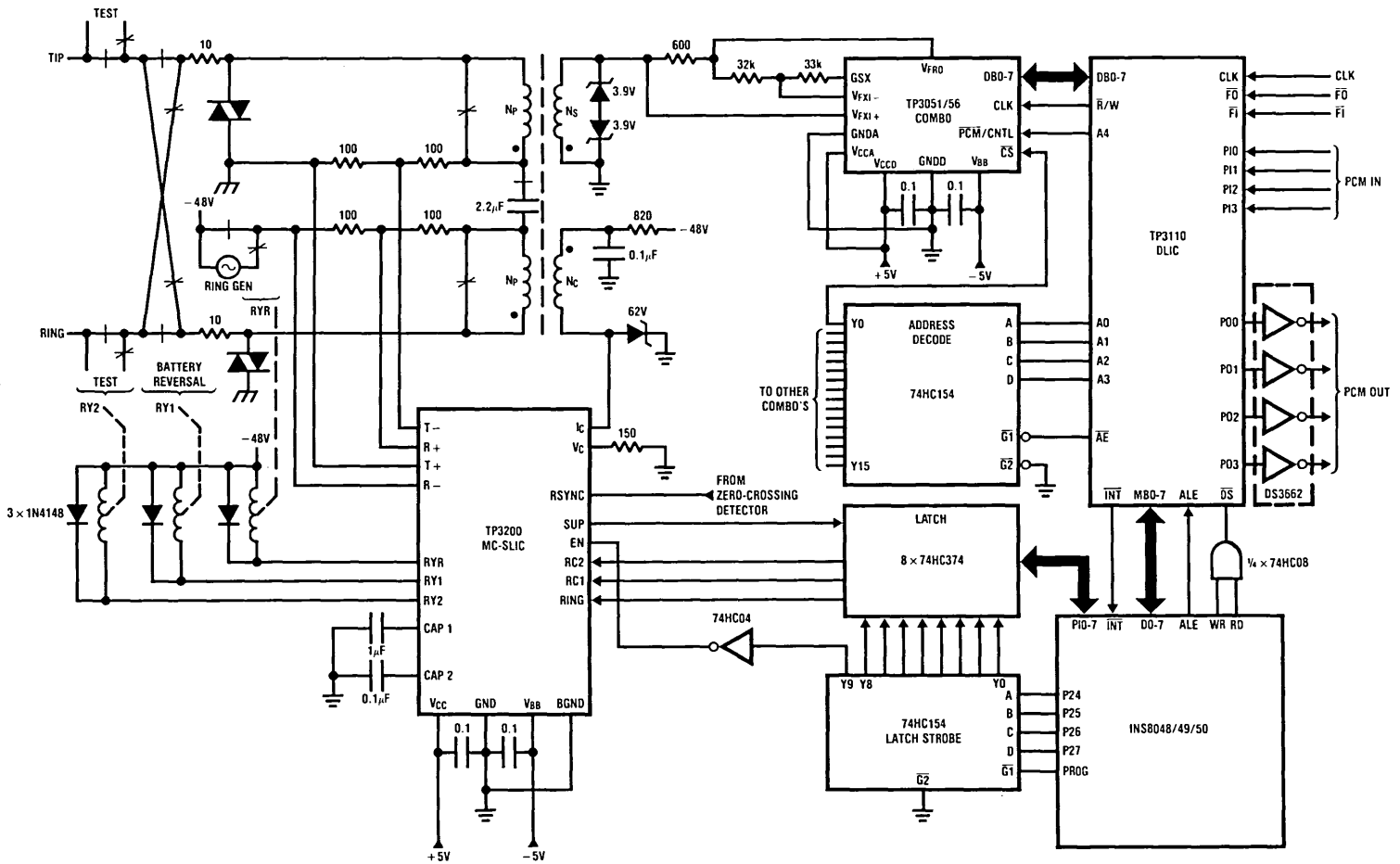

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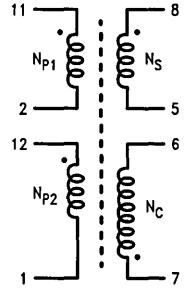
FIGURE 10. A Typical Line Card Application (Showing 1/16 SLIC Only)

APPENDIX A: Transformer Specification for 600Ω Line Impedance

1. Turn Ratio

Np1:	Start 11,	end 2,	210 T,	AWG #36
Np2:	Start 12,	end 1,	210 T,	AWG #36
Ns :	Start 8,	end 5,	440 T,	AWG #38
Nc :	Start 7,	end 6,	2100T,	AWG #42

2. Ferrite Core
   Siemens RM8-T35 or equivalent
   AL = 8400 nH/T^2 +30/−20%
3. DC Resistance
   Np1: 15Ω max
   Np2: 15Ω max
   Ns : 45Ω max
   Nc : 650Ω max
4. Inductance
   (total primary inductance with Np1 and Np2 in series aiding)
   1.5 H typical at 0 mA primary current
   0.7 H min at 3 mA DC primary current
5. Impedance: 600Ω to 600Ω
6. Frequency response
   ±0.5 dB reference to 1 kHz, 300–3500 Hz
7. Longitudinal Balance
   60 dB min with 2–12 grounded, 6–7 AC decoupled, 5 or 8 grounded
8. Dielectric
   1500 Vrms from primary to any other conductors



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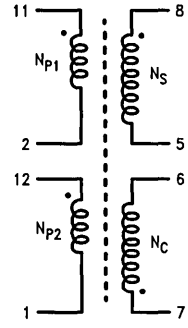
P/N 328-0036
AIE Magnetics
701 Murfreesboro Road
Nashville, Tennessee 37210
(615) 244-9024

APPENDIX B: Transformer Specification for 900Ω Line Impedance

1. Turn Ratio

Np1:	Start 11,	end 2,	255 T,	AWG #36
Np2:	Start 12,	end 1,	255 T,	AWG #36
Ns :	Start 8,	end 5,	440 T,	AWG #38
Nc :	Start 7,	end 6,	2550T,	AWG #41

2. Ferrite Core
   Siemens RM10-T35 or equivalent
   AL = 11000 nH/T^2 +30/−20%
3. DC Resistance
   Np1 : 20Ω max
   Np2 : 20Ω max
   Ns : 55Ω max
   Nc : 800Ω max
4. Inductance
   (total primary inductance with Np1 and Np2 in series aiding)
   2.5 H typical at 0 mA DC primary current
   1.3 H min at 3 mA DC primary current
5. Impedance: 900Ω to 600Ω
6. Frequency response
   ±0.5 dB reference to 1 kHz, 300–3500 Hz
7. Longitudinal Balance
   60 dB min with 2–12 grounded, 6–7 AC decoupled, 5 or 8 grounded
8. Dielectric
   1500 Vrms from primary to any other conductors



TL/H/8682–15

P/N 328-0035

Appendix C: Transformer Specification for a Center Tap Transformer

1. Turns Ratio

Np1:	Start 1,	End 4,	175 T
Np2:	Start 3,	End 6,	175 T
Ns1:	Start 12,	End 11,	175 T
Ns2:	Start 11,	End 9,	175 T
Nc :	Start 10,	End 7,	1750T

2. Wire Gauge

   Np1, Np2 wound by Bifilar wires, 0.125 mm
   Ns1, Ns2 wound by Bifilar wires, 0.125 mm
   Nc wound by 0.06 mm wires

3. Ferrite Core

   Siemens RM8-T38 or equivalent,
   A_L = 12500 nH/T^2 +30/−40%

4. Resistance matching of coils

   Np1 to Np2: 1% max
   Ns1 to Ns2: 1% max

5. Inductance

   (total primary inductance with Np1 and Np2 in series aiding)
   0.8H min at 3 mA DC primary current. f = 300 Hz.

6. High Voltage Isolation

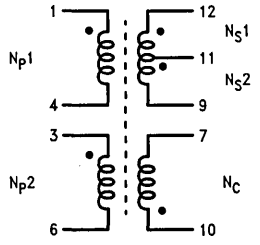
   1500V between all coils

7. Suggested Vendors

   Ferroglen Research Ltd.
   20 Tanfield Road
   Croyden Surrey
   CRO 1 AL

   or

   Gardners Transformers Ltd.
   Christchurch
   Dorset
   BH23 3PN



TL/H/8682–17

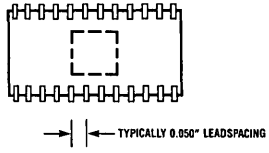
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliabilty

National Semiconductor Corp.
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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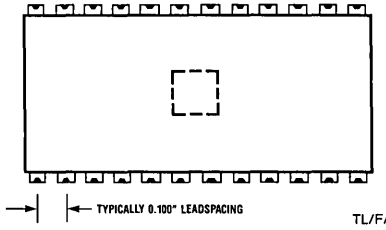
Standard DIP Package



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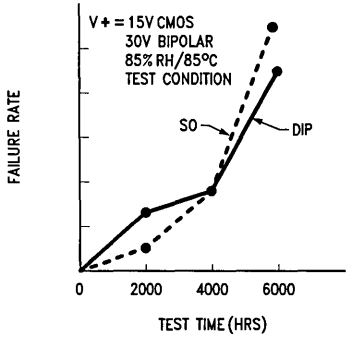
Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.



TL/F/8766-3

FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

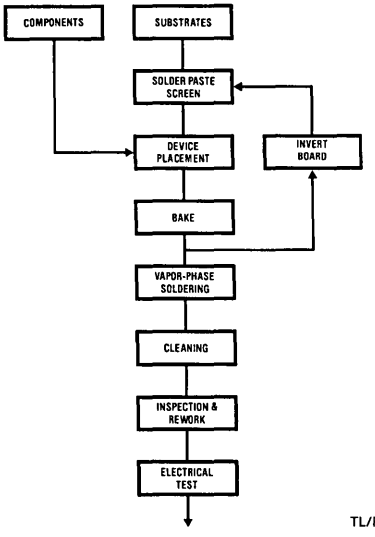
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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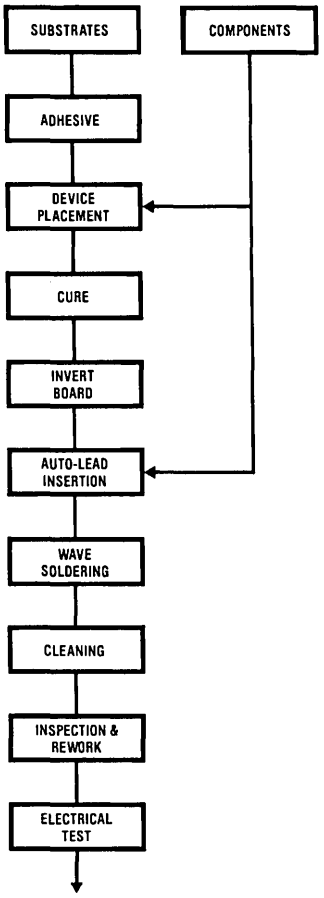
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



TL/F/8766-5

Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

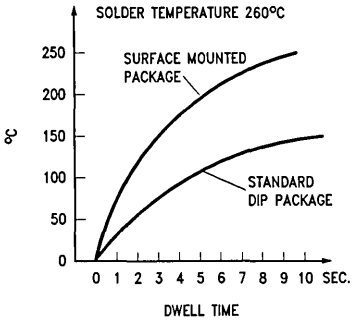


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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C*. At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

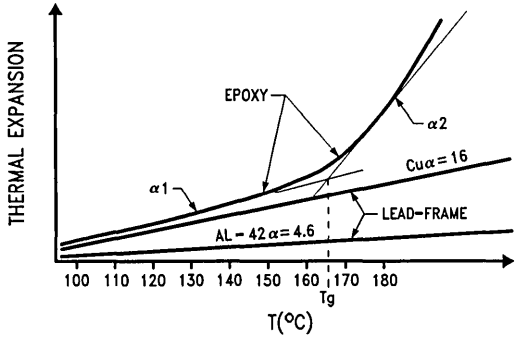

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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

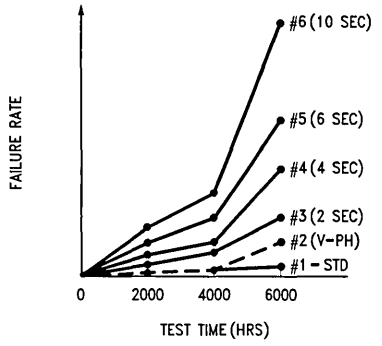

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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

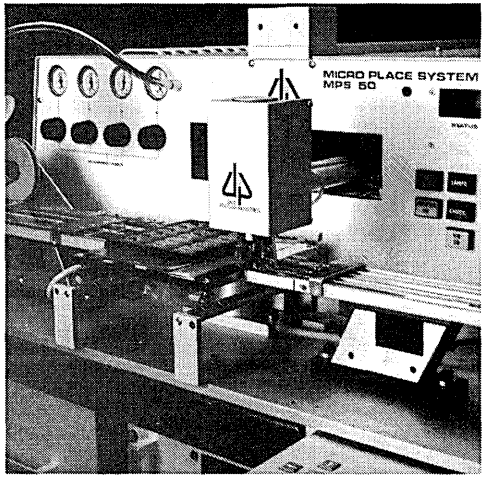
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

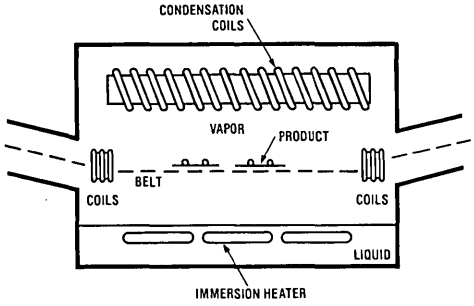
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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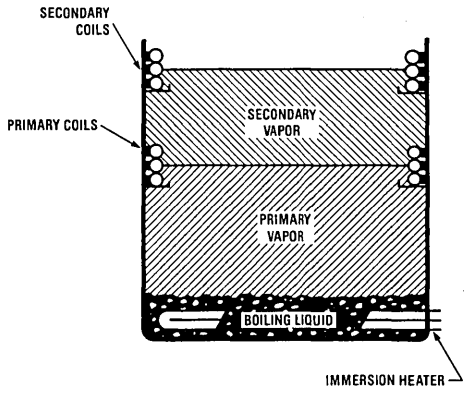
The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

TL/F/8766–10

Batch-Fed Production Vapor-Phase Soldering Unit



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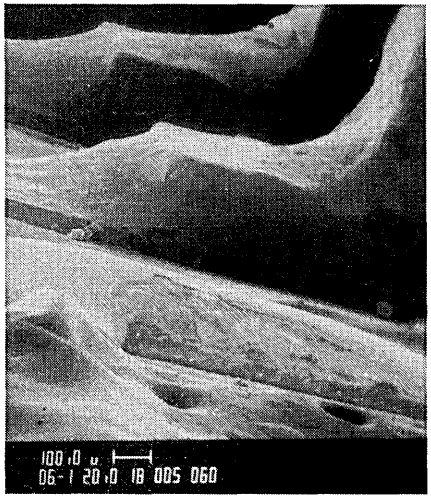
Solder Joints on a SO-14 Package on PCB



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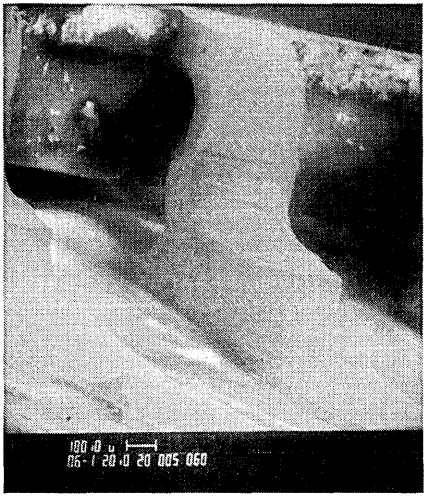
Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050" lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005" usually used to achieve a solder paste thickness (wet) of about 0.008" typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed $\frac{1}{8}$", to avoid damage to screens and minimize distortion.

SOLDER PASTE

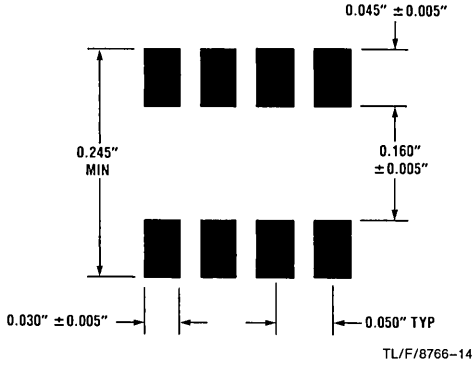
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



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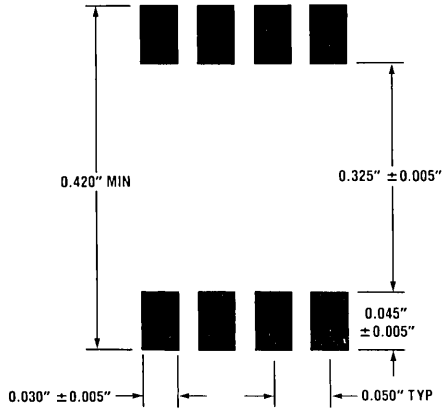
SO-16L, SO-20



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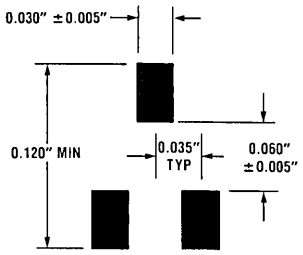
SOT-23



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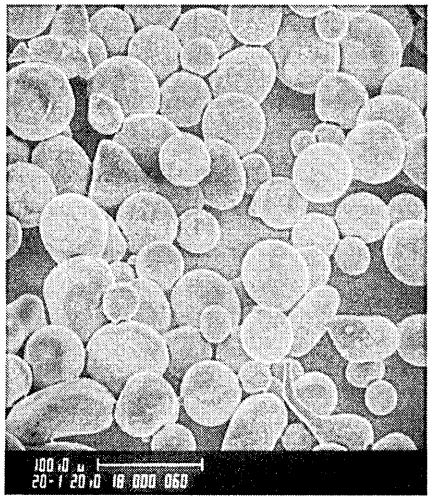
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



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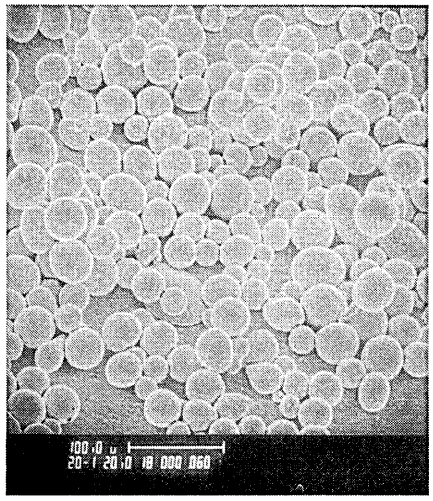
200 × Kester (63/37)



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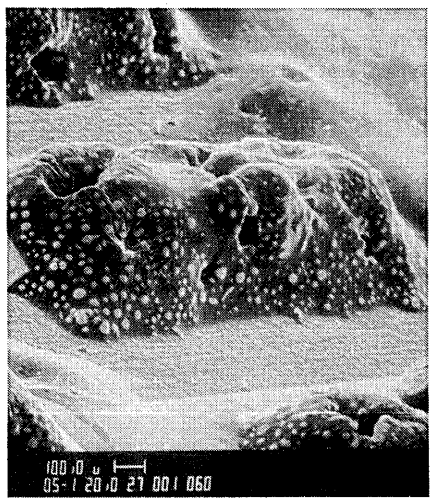
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



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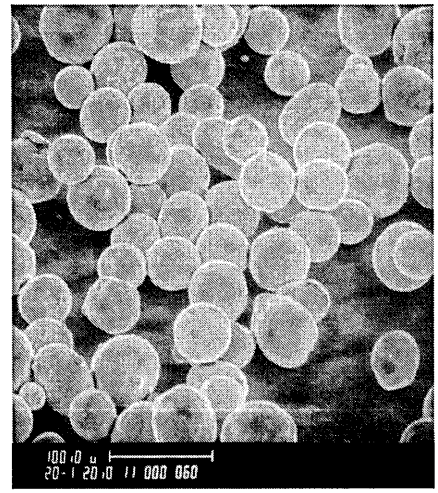
200 × Fry Metal (63/37)



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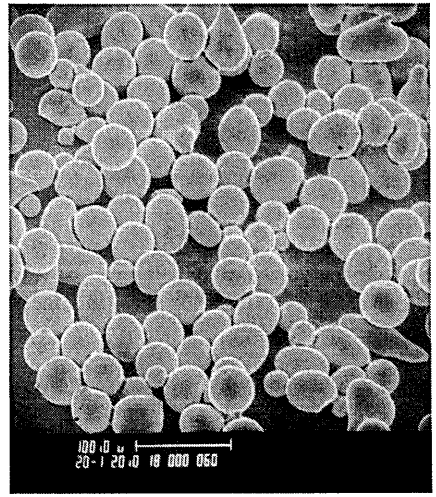
200 ESL (63/37)



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CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

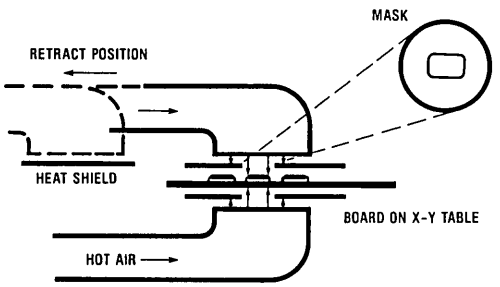
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

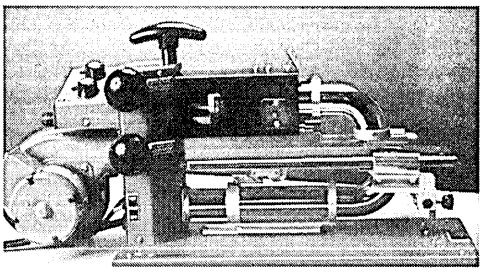
When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



TL/F/8766–22

Hot-Air Rework Machine



TL/F/8766–23

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

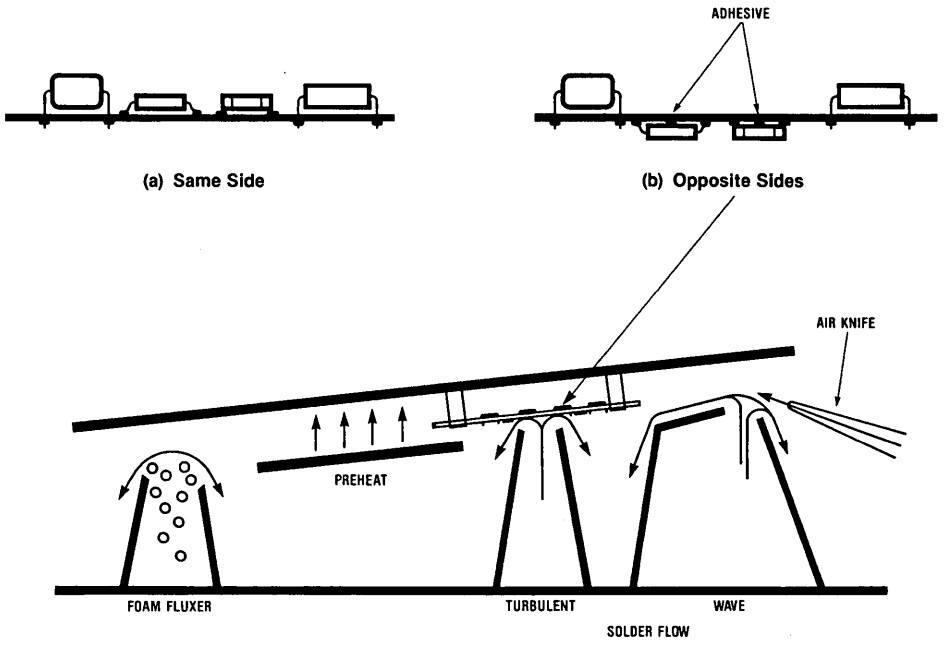
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% w.dth of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050" vs 0.100" for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



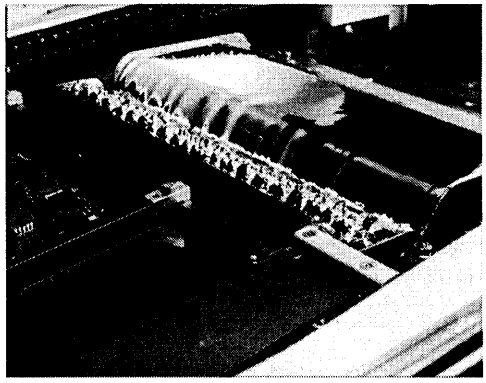
TL/F/8766–24

A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/F/8766–25

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

Improving The Performance Of A High Speed PBX Backplane

National Semiconductor Corp.
Application Note 466
Ramiro Calvo

ABSTRACT

This article will provide solutions to performance problems associated with PBX backplanes. Some of these problems are: long settling time, excessive propagation delay, low impedance bus lines, crosstalk, and electromagnetic radiation (EMR). These problems are caused by high output capacitance drivers that use TTL signal levels. National's solution to these problems is the Backplane Transceiver Logic (BTL) family of devices.

INTRODUCTION

To be able to meet the bandwidth and high system reliability requirements of the next generation PBXs, the industry must use parallel, high speed Pulse Code Modulation (PCM) highways. This article will deal with the following problems encountered by these high speed PCM highways.

- Crosstalk
- Power Consumption
- Noise Margin
- Bus Impedance
- Signal Settling Time
- Propagation Delays
- Propagation Delay Skew
- Live Insertion
- Extending A Bus Beyond The Rack
- Bus Termination
- Pin Layout

I. REDUCING CROSSTALK

Crosstalk can reduce the data integrity of the system or even cause a total shutdown. Crosstalk amplitude is proportional to the slew rate, signal swing, and physical layout of the board. To reduce crosstalk, the DS3890/92/98: shrink the standard TTL three volt swing to the Backplane Transceiver Logic (BTL) one volt swing; slow down the rise and fall time to 6 ns; use low pass filters and precision thresholds on the receivers.

II. REDUCING POWER CONSUMPTION

Because of excessive heat dissipation and a mandatory battery backup, power consumption must be kept to a minimum. Low impedance, open collector busses that use TTL signal levels need drivers capable of sinking approximately 300 mA. By using the BTL one volt signal swing, the drivers need only sink 50 mA. Refer to the section **Signal Settling Time** for more details. The reduction in power consumption will enable PBXs to coexist with other office equipment in "normal" office environments.

III. NOISE MARGIN

Noise margins protect the system from crosstalk, ground noise, and external EMR. The magnitude of the absolute noise margin is a good measure of how well protected the system is against external electro magnetic interference (EMI) and ground noise. The relative noise margin is a good measure as to how well protected the system is against crosstalk, assuming most signals within the system have the

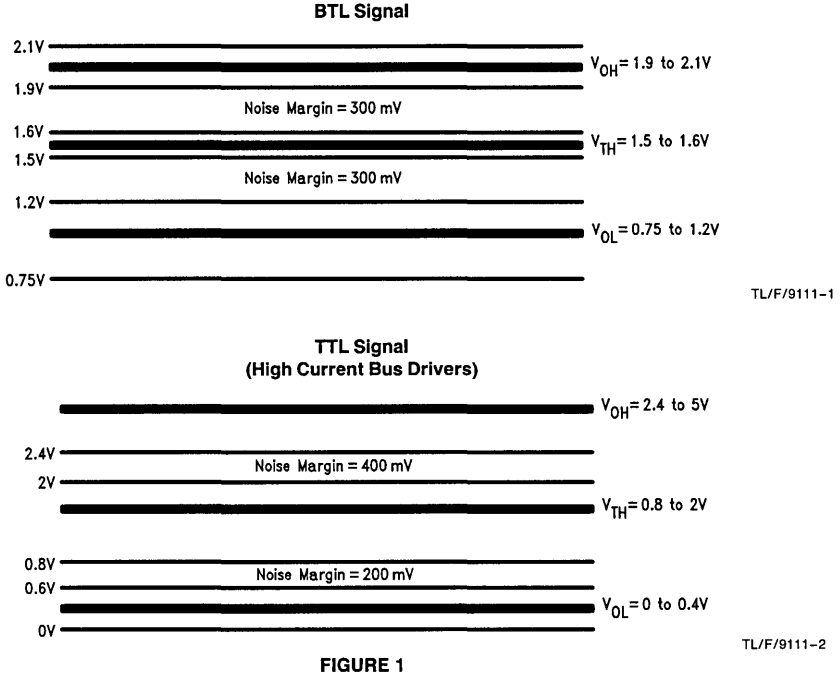


FIGURE 1

same voltage swing. As shown below, BTL signals improve both the absolute and relative noise margins

- Absolute Noise Margin

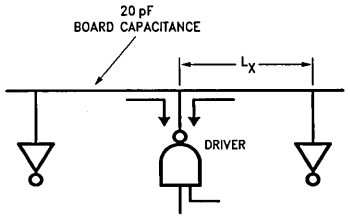
Despite the smaller signal swing, BTL signals have a 300 mV noise margin, as compared to the 200 or 400 mV guaranteed noise margin in TTL signals (see *Figure 1*). The absolute noise margin is usually not very critical since PBXs are usually well protected from external EMR by the metallic racks.

- Relative Noise Margin

Based on the data sheet guaranteed limits, BTL signals have a 30% [(300 mV absolute noise margin)/(1V signal swing)] relative noise margin, as compared to 7% [(200 mV absolute noise margin)/(3V swing)] in standard TTL signals.

IV. IMPROVING BUS IMPEDANCE

Standard TTL drivers do not have sufficient drive current to drive a heavily loaded backplane. A larger output transistor is needed to increase the drive current. The large TTL output transistor, however, increases the capacitance loading, which decreases the bus impedance, which in turn requires more drive current. The BTL drivers have a Schottky diode in series with the driver transistor's collector. When the driver transistor is off, the diode is reverse biased, which reduces the output capacitance to only 1–2 pF. As shown below, the reduced output capacitance greatly improves the overall bus impedance.



TL/F/9111–3

FIGURE 2

L_X = Board Spacing = 0.6 in

L_{foot} = 20 loads per foot

$C_{x\text{-}TTL}$ = Capacitance per TTL Driver
= Transceiver Capacitance + PC Trace and Connector Capacitance
= 15 pF + 5 pF
= 20 pF per load

$C_{x\text{-}BTL}$ = Capacitance per BTL Driver
= Driver Capacitance + Receiver Capacitance + PC Trace and Connector Capacitance
= 2 pF + 2 pF + 1 pF + 5 pF
= 10 pF per load

$C_{L\text{-}TTL}$ = (20 load per foot) × (20 pF per load)
= 400 pF per Foot

$C_{L\text{-}BTL}$ = (20 load per foot) × (10 pF per load)
= 200 pF per Foot

- Unloaded Bus Impedance

L = Standard PC Board Inductance Per Foot
= 0.2 μH per foot

C = Standard PC Board Capacitance Per Foot
= 20 pF per foot

$Z_O = (L/C)^{1/2}$
$= (0.2\ \mu H/20\ pF)^{1/2} = 100\Omega$

- Loaded Bus Impedance (for a uniform capacitive loading C_X spaced at equal intervals)

$Z_L = Z_O/(1 + C_L/C)^{1/2}$

$Z_{L\text{-}TTL} = 100/(1 + 400/20)^{1/2} = 22\Omega$

$Z_{L\text{-}BTL} = 100/(1 + 200/20)^{1/2} = 30\Omega$

Note that each driver sees TWO loaded line impedances in parallel (see *Figure 2*). This reduces the bus impedance by half.

V. PROPAGATION DELAYS (related to excessive capacitance loading)

Since the DS3890 reduces the backplane capacitance loading, the propagation delay through the bus lines is improved by 28%, as shown below.

- Unloaded Bus Propagation Delay (data based on a single strip line PC board)

$T_P = (LC)^{1/2} = [(0.2\ \mu H/ft) \times (20\ pF/ft)]^{1/2}$
$= 2$ ns per foot

- Loaded Bus Propagation Delay (data based on a single strip line PC board)

$T_{PL} = (T_P) \times (1 + C_L/C)^{1/2}$

$T_{PL\text{-}TTL} = (2\ ns) \times [1 + (400\ pF\ per\ Foot)(20\ pF)]^{1/2}$
$= 9.2$ ns/ft

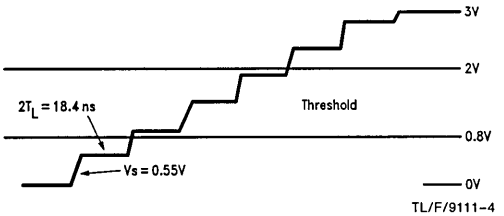
$T_{PL\text{-}BTL} = T_P \times (1 + C_L/C)^{1/2} = (2\ ns) \times [1 + (200\ pF\ per\ Foot)/(20\ pF)]^{1/2} = 6.6$ ns/ft

Improvement = (6.6 ns per foot)/(9.2 ns per foot) × (100)
= 28%

VI. SIGNAL SETTLING TIME

The signal settling time refers to the amount of time the signal takes to cross the threshold. In low impedance busses, the signaling settling time depends NOT ONLY on the slew rate, but more importantly, on the current driving capability of the driver, bus impedance, reflections, and bus length.

For example, in a fully loaded open collector TTL bus ($Z_{O\text{-}TTL} = 22\Omega$) with 50 mA drivers, the first output transition is $[V_1 = (I_L) \times (Z_O \| Z_O) = (50\ mA) \times (11\Omega)]$ 0.55V. This means that the signal does NOT cross the threshold region (V_{TH} = 0.8 to 2V) on the first signal transition (see *Figure 3*). The second transition appears after a round trip prop delay [R.T.D. = (2) × ($T_{L\text{-}TTL}$)]. In a one foot fully loaded bus, the delay can be 18.4 ns [R.T.D. = (2) × (9.2 ns per foot)]. If it takes several signal transitions to cross the threshold, the ACTUAL signal settling time consists of several round trip prop delays. Also note that the signal crosses the threshold in a staircase fashion, which may cause false triggering.



TL/F/9111–4

FIGURE 3

$V_{I\text{-}TTL}$ = (50 mA) × (11Ω) = 0.55V

Round Trip Prop Delay of the Bus = (2) × ($T_{L\text{-}TTL}$)

= (2) × (2 ns per foot)

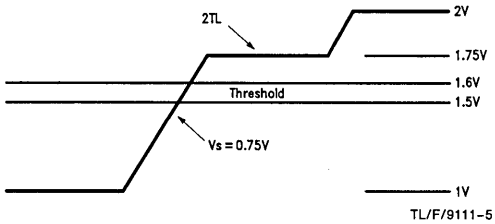
= 4 ns/ft (unloaded bus)

= (2) × (9.2 ns per foot)

= 18.4 ns/ft (loaded bus)

In a fully loaded BTL bus ($Z_{O\text{-}BTL}$ = 30Ω), the first output transition is 0.75V [V1 = (50 mA) × (15Ω)]. Since V_{TH} is between 1.5V and 1.6V, the FIRST output transition crosses the threshold (see *Figure 4*). The actual settling time consists of ONLY the slew rate. The danger of false triggering is eliminated because the reflections are not seen as the signal crosses the threshold.

$V_{I\text{-}BTL}$ = (50 mA)* (15Ω) = 0.75V



TL/F/9111–5

FIGURE 4

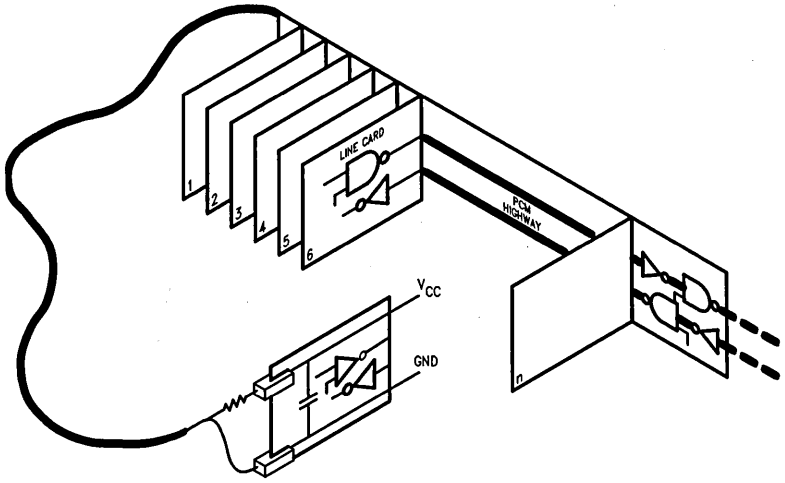
Therefore, despite the slower slew rate, the BTL devices have a much shorter settling time due to the lower output capacitance, one volt signal swing, and precision threshold. This improves the data integrity and speed of the bus.

VII. PROPAGATION DELAY SKEW

The propagation delay consists of the delays through the driver, receiver, and transmission medium (PC strip). These delays can vary if the ICs have differences in their process, temperature, V_{CC}, or PC board layout. In parallel address/data lines, propagation delay skews are very critical. If the signals arrive at their destination at different times, the system must delay all signals to assume for a worst case delay. Therefore, if the propagation delay skew is small, the worst case delay is also small. It is safe to assume that ICs on a single board or system have the same temperature, same V_{CC}, and similar PC board layout configurations. This reduces the propagation delay skew to only the variations in the process.

VIII. LIVE INSERTION GUIDELINES

Live insertion of line cards is a must for PBX maintenance without interrupting customer service. The DS3890/92/98 support live insertion by guaranteeing glitch-free power up/down. However, uncharged by-pass capacitors and board static can bring the system down when plugging in a line card. One way of avoiding these problems is to use an umbilical cord (temporary power line) to discharge static and slowly charge by-pass capacitors. This method will set the line card V_{CC} and GND equal to the levels of the system before it is plugged in.



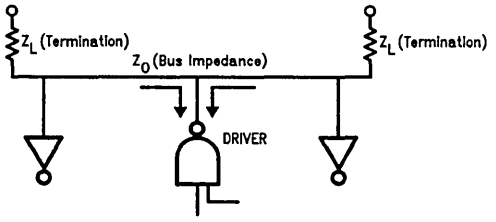
TL/F/9111–6

FIGURE 5. Temporary Power Cord

IX. EXTENDING A BUS BEYOND THE RACK

The DS3898 (BTL repeater) is ideal for cases where the system bus must be extended. If the bus is of considerable length, the repeaters regenerate the signal levels. The repeaters also isolate, or separate, different electrical environments. For example, if a ribbon cable is used to connect one rack to another, the repeaters will isolate the different impedance and noise levels present in a ribbon cable from the bus on the rack.

X. USING THE PROPER BUS TERMINATION



TL/F/9111–7

FIGURE 6

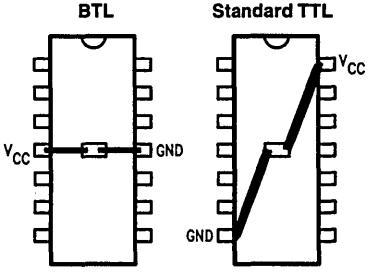
An ideal termination (Z_L) should match the bus impedance (Z_O) in order to eliminate reflections. If the termination matches the impedance of a fully loaded bus, then $Z_L = Z_O = 30\Omega$. With the 30Ω terminations, the driver is required to drive a ($Z_L \| Z_L = 30 \| 30$) 15Ω load. However, the lowest load that a standard TTL driver will guarantee is (5V/50 mA) 100Ω. If the designer uses the ($Z_L \| Z_L = 200 \| 200 = 100\Omega$ load) 200Ω terminations on the 30Ω bus, the reflections will be very large. On the other hand, BTL drivers can guarantee a (1V/50 mA) 20Ω load. In this case, the ($Z_L \| Z_L = 40 \| 40 = 20\Omega$ load) 40Ω terminations will have small reflections. Note that the improvement of the guaranteed load (from 100Ω to 20Ω) was achieved by reducing the voltage swing and driver output capacitance, NOT by increasing the current capabilities of the drivers.

XI. TWO VOLT RAIL

There are many ways of supplying the two volt rail needed for the 90/92/98. Four possibilities are: a separate two volt power supply; a voltage divider; a voltage regulator; and a high current voltage follower. The two volt power supply is very expensive to implement and does not track the five volt supply voltage, thereby reducing the effectiveness of the precision threshold. However, it is very efficient in terms of power consumption, making it appropriate for very large systems. The voltage divider is inexpensive, tracks the five volt supply voltage, but consumes too much current when the line is high. The voltage regulator is moderately efficient with current consumption, but does not track the five volt supply voltage. Finally, the high current voltage follower does not waste current when the line is high; is inexpensive to implement; and tracks the five volt supply voltage. Therefore, the high current voltage follower seems to be the best choice for small systems where cost is a major consideration.

XII. NOISE REDUCTION THROUGH IMPROVED PIN LAYOUT

In order to reduce ground noise caused by long lead inductance, one must make V_{CC} and GND lead lengths as short as possible. The packaging of National's BTL circuits contributes to shorter V_{CC} and GND lead inductance by placing the power pins in the center of the IC package, instead of the corners.



TL/F/9111–8

Top View

FIGURE 7

XIII. OVERVIEW OF THE BTL TRAPEZOIDAL PRODUCT LINE

The BTL Trapezoidal products have low output capacitance (5 pF max), one volt signal swing, and noise immunity features which make them ideal for driving parallel, low impedance bus lines with minimum power dissipation.

- DS3890

The DS3890 is an octal BTL driver. It is designed specifically to overcome problems associated with driving densely populated backplanes. The trapezoidal wave forms and the one volt swing reduces noise coupling to adjacent lines. The open collector driver output allows for wired-OR connections.

- DS3892

The DS3892 is an octal receiver. The receivers have precision thresholds to increase the noise margins, and low pass filters to filter out crosstalk.

- DS3898

The DS3898 is an octal repeater. It combines the BTL characteristics of the DS3890 and DS3892. The part is ideal for extending backplanes.

- DS3896

The DS3896 is an octal high speed schottky bus transceiver with common control signals. It provides high package density for data/address lines.

- DS3897

The DS3897 is a quad transceiver with independent driver input and receiver output pins. It has a separate driver disable for each driver.

- DS3893

The DS3893 is the newest member of the family. It is designed to drive and receive signals at data rates of up to 100 MBaud. The trapezoidal feature has been removed to reduce the propagation delay down to 15 ns for the driver and receiver combination.

National's BTL drivers, receivers, and transceivers offer the most complete approach for operating high speed parallel backplanes.

+5 to −15 Volts DC Converter

National Semiconductor Corp.
Linear Brief 18

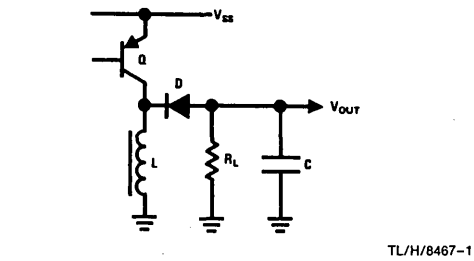
INTRODUCTION

It is frequently necessary to convert a DC voltage to another higher or lower DC-voltage while maximizing efficiency. Conventional switching regulators are capable of converting from a high input DC voltage to a lower output voltage and satisfying the efficiency criteria. The problem is a little more troublesome if a higher output voltage than the input voltage is desired. Particularly, generating DC voltage with opposite polarity to the input voltage usually involves a complicated design.

This brief demonstrates the use of the switching regulator idea for a +5 volts to −15 volts converter. The converter has an application as a power supply for MOS memories in a logic system where only +5 volts is available. However, the principle used can be amplied for almost any input output combination.

OPERATION

The method by which the regulator generates the opposite polarity is explained in *Figure 1*. The transistor Q is turned ON and OFF with a given duty cycle. If the base drive is sufficient the voltage across the inductor is equal to the



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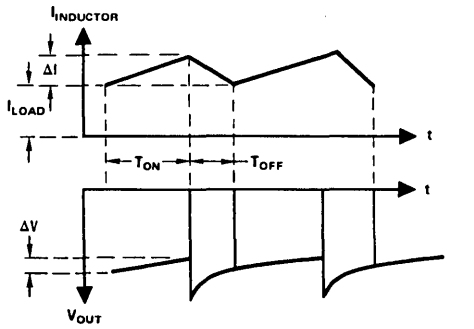


TL/H/8467–2

FIGURE 1. Switching Circuit for Voltage Conversion

supply voltage minus V_{SAT}. The current change in the inductor is given by:

$$\Delta I = \frac{V_{SS} - V_{SAT}}{L} \times T_{ON} \approx \frac{V_{SS}}{L} T_{ON} \qquad (1)$$

Turning OFF the transistor the inductor current has a path through the catch diode and this in turn builds up a negative voltage across R_L.

The figure also shows the current and voltage levels versus time. A capacitor in parallel to the resistor will prevent the voltage from dropping to zero during the transistor ON time.

Assuming a large capacitor, we can also write the current change as:

$$\Delta I = \frac{V_{OUT} - V_D}{L} \times T_{OFF} \approx \frac{V_{OUT}}{L} \times T_{OFF} \qquad (2)$$

In order to get a general idea of the operation for certain input output conditions, we will develop a set of equations.

During the transistor ON time, energy is loaded into the inductor. In the same time interval, the capacitor is drained due to the load resistor R_L.

Drop in capacitor voltage:

$$\Delta V = \frac{I_{LOAD} \times T_{ON}}{C} \qquad (3)$$

During the T_{OFF} time the stored energy in the inductor is transferred to the load and capacitor. A rough estimate of T_{OFF} can be expressed as:

$$T_{OFF} = \frac{V_{SS}}{V_{OUT}} \times T_{ON} \qquad (4)$$

The capacitor voltage will be restored with a average current given by:

$$I_C = \frac{\Delta V \times C}{T_{OFF}} = \frac{I_{LOAD} \times V_{OUT}}{V_{SS}} \qquad (5)$$

The total inductor current during the OFF time can be written as:

$$I_{INDUCTOR} = I_{LOAD} + I_C \qquad (6)$$

Inspecting *Figure 1*. We find:

$$I_C = \frac{\Delta I}{2} = \frac{V_{SS} \times T_{ON}}{2 \times L} \qquad (7)$$

which yields:

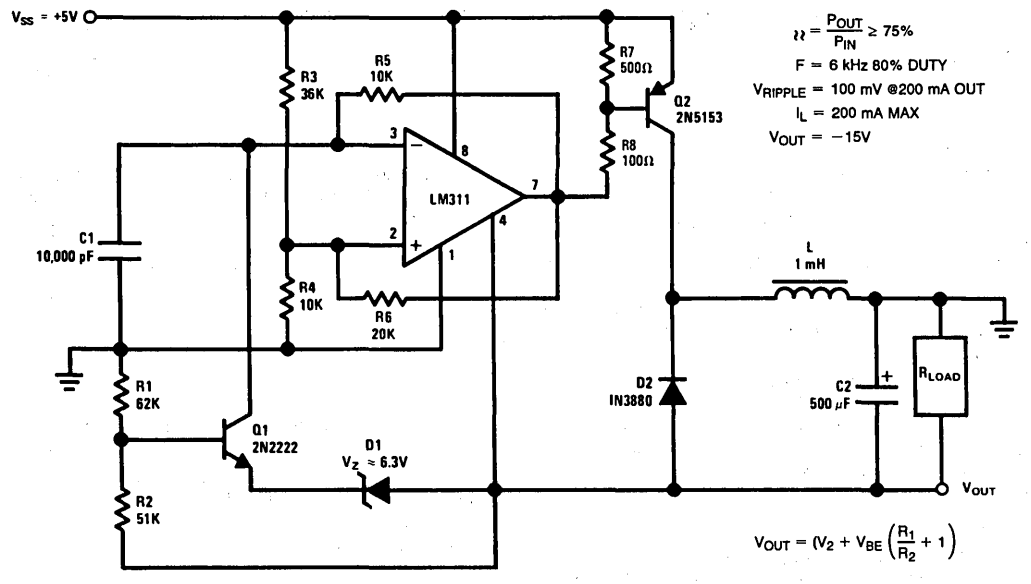
$$T_{ON} = \frac{2 \times L \times I_{LOAD} \times V_{OUT}}{V_{SS}^2} \qquad (8)$$

Taking into account that the efficiency is in the order of 75% the final expression is:

$$T_{ON} = \frac{1.5 \times L \times I_{LOAD} \times V_{OUT}}{V_{SS}^2} \qquad (9)$$

The above equations will be applied to the regulator shown at *Figure 2*. The regulator must deliver −15 volts at 200 mA from a +5 volt supply. Using a 1 mH inductor the T_{ON} time for Q_2 is 0.18 ms from equation 9. T_{OFF} is 60 μs from equation 4 and the oscillator frequency to:

$$F = \frac{1}{T_{ON} + T_{OFF}} \approx 4\ \text{kHz}$$



TL/H/8467–3

FIGURE 2. Switching Regulator for Voltage Conversion

The LM311 performs like a free running multivibrator with high duty cycle. The IC is designed to operate from a standard single 5 volt supply and has a high output current capability for driving the switching transistor Q_2. The duty cycle is given by the voltage divider R_3 and R_4 and the frequency of C_1 in conjunction with R_5.

By setting the duty cycle higher than first calculated, the output voltage will tend to increase above the desired output voltage of 15 volts. However, an extra loop performed by Q_1 and the zener diode in conjunction with the resistor network will modify the oscillator duty cycle until the desired output level is obtained.

The output voltage is given by:

$$V_{OUT} = \left(V_Z + V_{BE}\right)\left(\frac{R_1}{R_2} + 1\right)$$

Data and results obtained with the design:

V_{IN} = 5 volts
V_{OUT} = −15 volts
I_{OUT} = max 200 mA
Efficiency ≅ 75%
Frequency ≅ 6 kHz 80% duty cycle
V_{RIPPLE} ≅ 100 mV @ 200 mA load
Line regulation: V_{IN} = 5V to 10V < 3% V_{OUT}
I_{LOAD} = 200 mA
Load regulation: V_{IN} = 5V < 3% V_{OUT}
I_{LOAD} = 0 – 100 mA

Section 6

Reliability of Telecom Devices/ Physical Dimensions

Section 6 Contents

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RELIABILITY OF TELECOM DEVICES

To insure maximum reliability of the field, all of the line card devices which contain mixed analog and digital functions on the same integrated circuit are subjected to a dynamic burn in for 22 hours at 156 degrees centigrade. This time and temperature directly correlates and is equal to a 96 hour 125 degree burn in, and allows a complete burn in rotation within a 24 hour period. This flow maximizes the production output of the devices, while at the same time removes any devices which might be candidates for infant mortality.

MIXED ANALOG/DIGITAL DEVICE PRODUCT FLOW INCLUDING 100% BURN IN

WAFER FAB

↓

WAFER SORT

↓

ASSEMBLY

↓

100% DYNAMIC BURN IN

↓

100% FINAL TEST

↓

SHIP

Devices burined in: TP3020 TP3021
TP5116A TP5156A
TP3040 Family
TP3051 TP3052
TP3053 TP3054
TP3056 TP3057
TP3058 TP3059
TP3064 TP3067
TP3070 TP3071
TP3400 TP3420
TP3330

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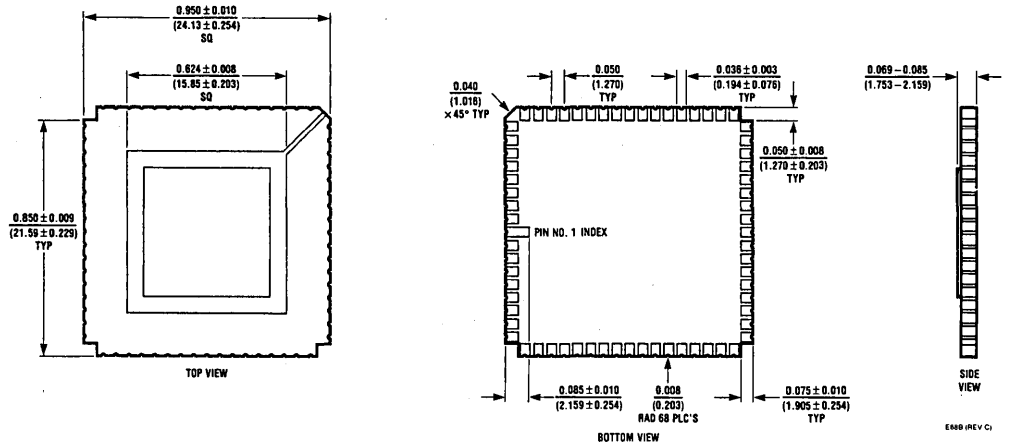
All dimensions are in inches (millimeters)



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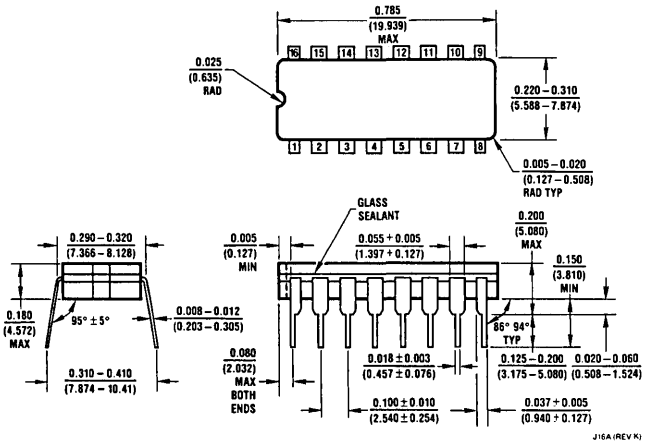

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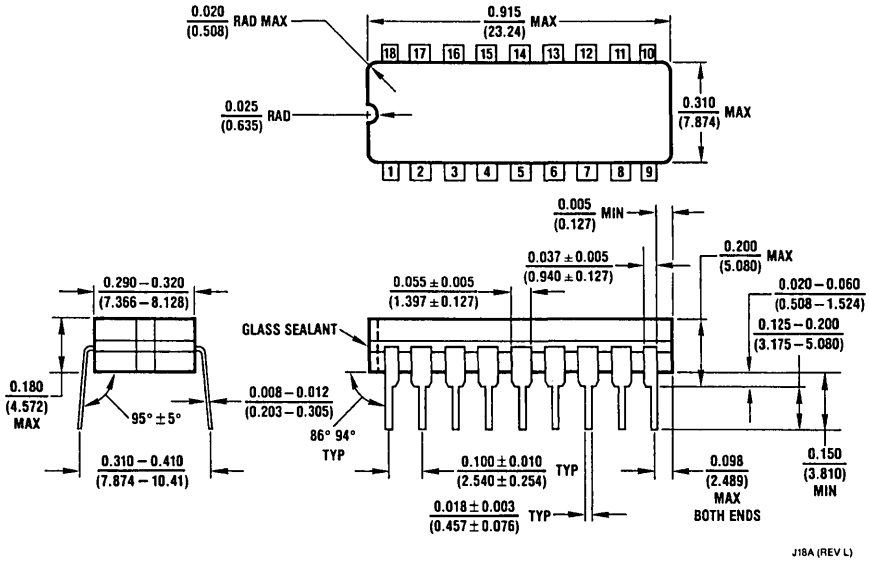

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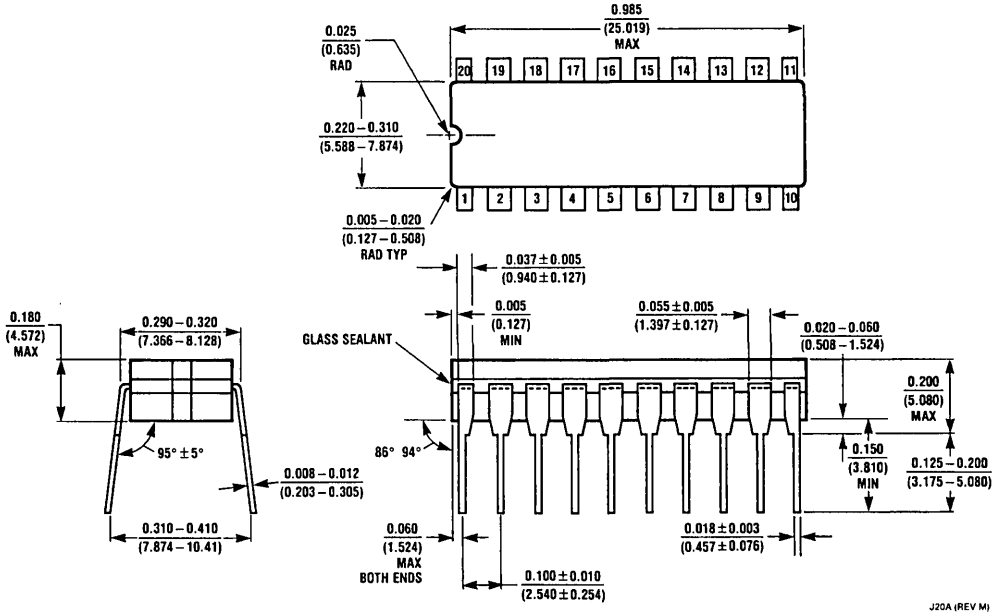

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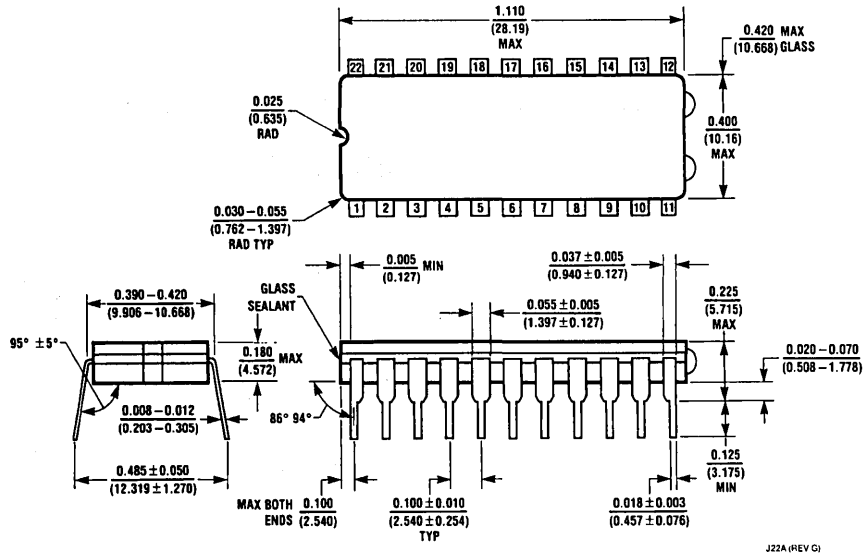

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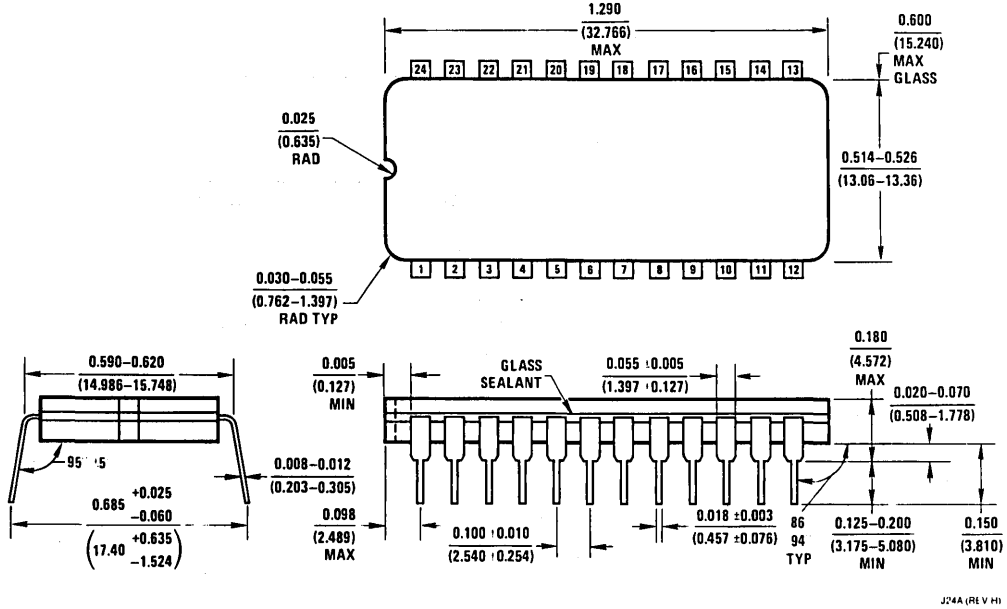

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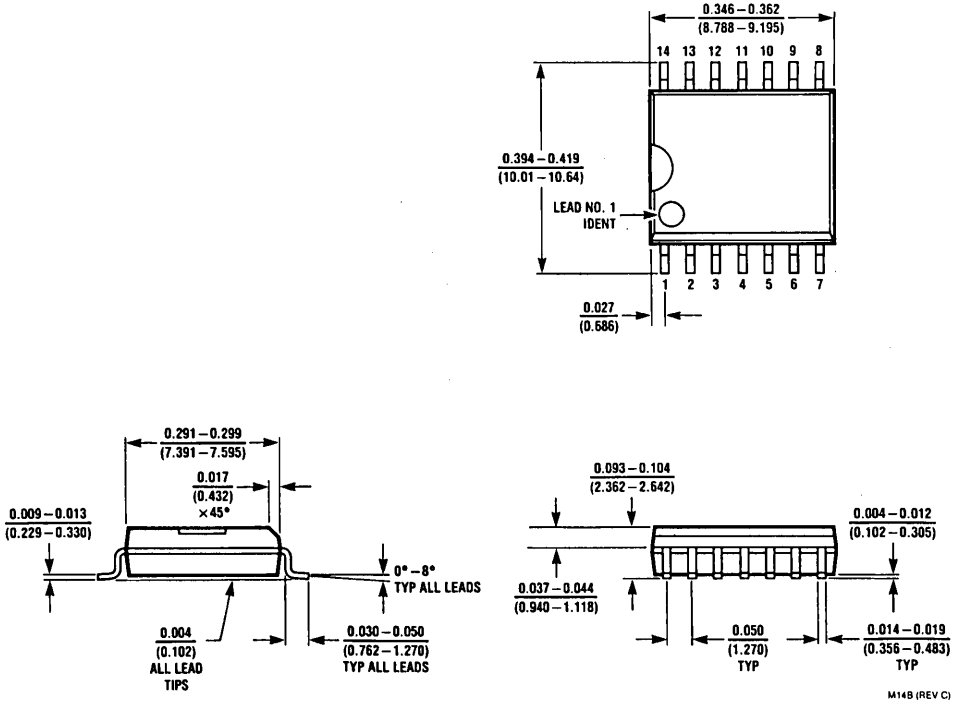

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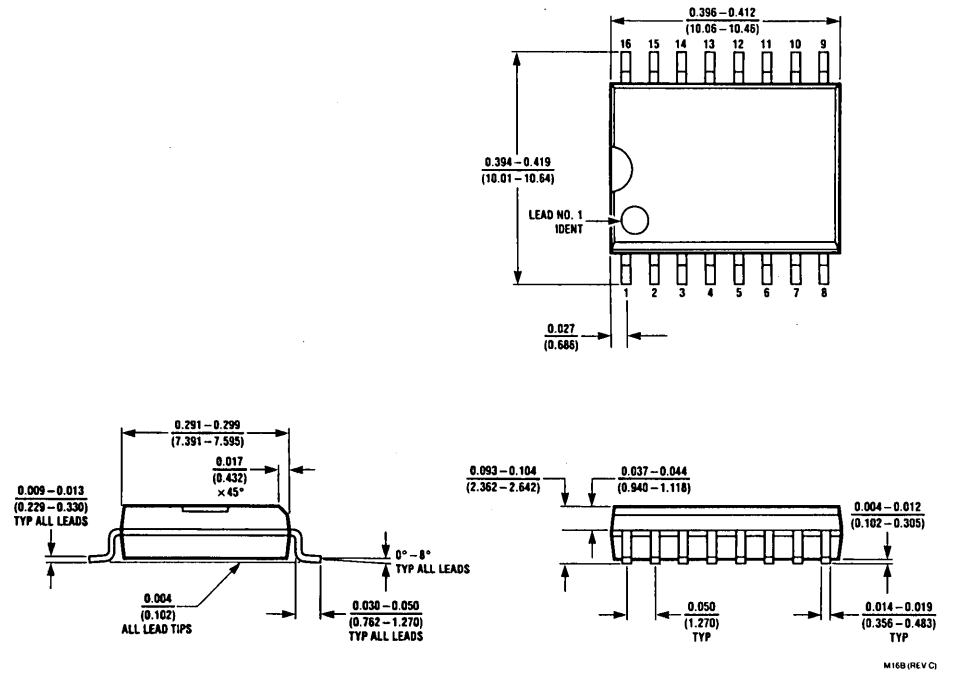

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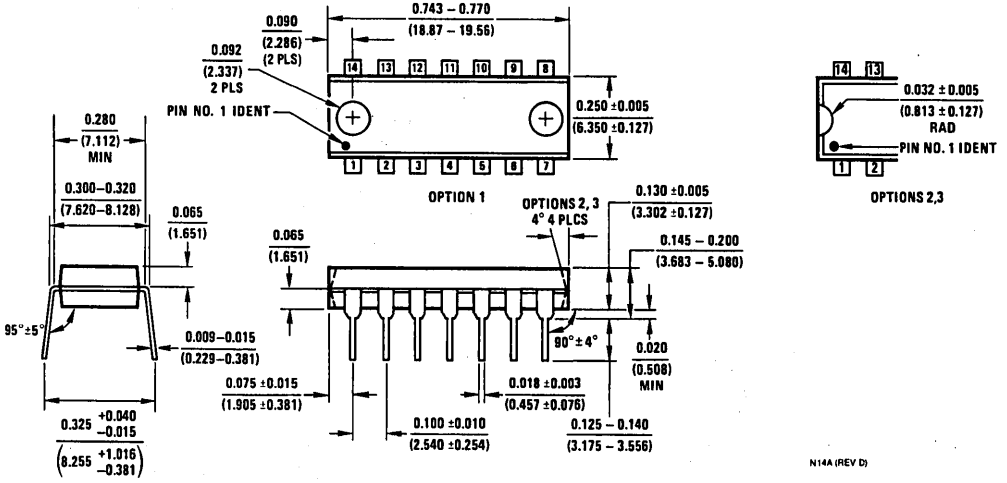

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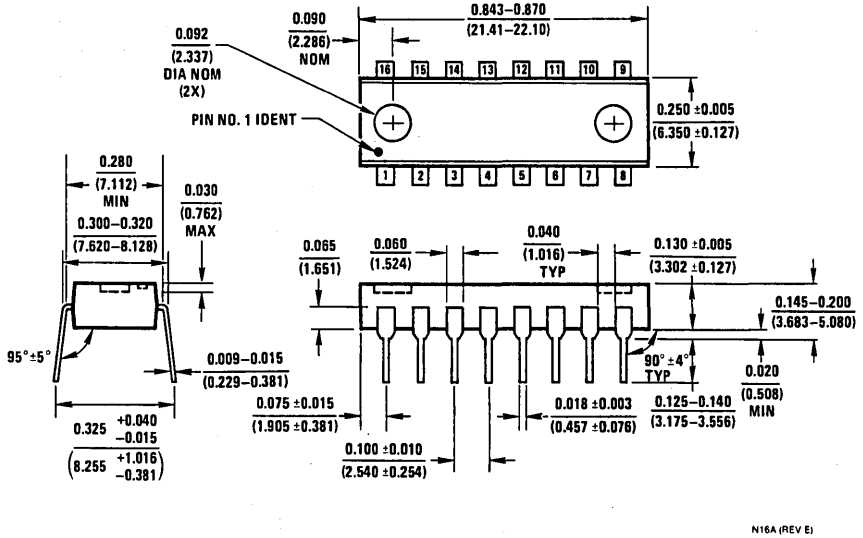

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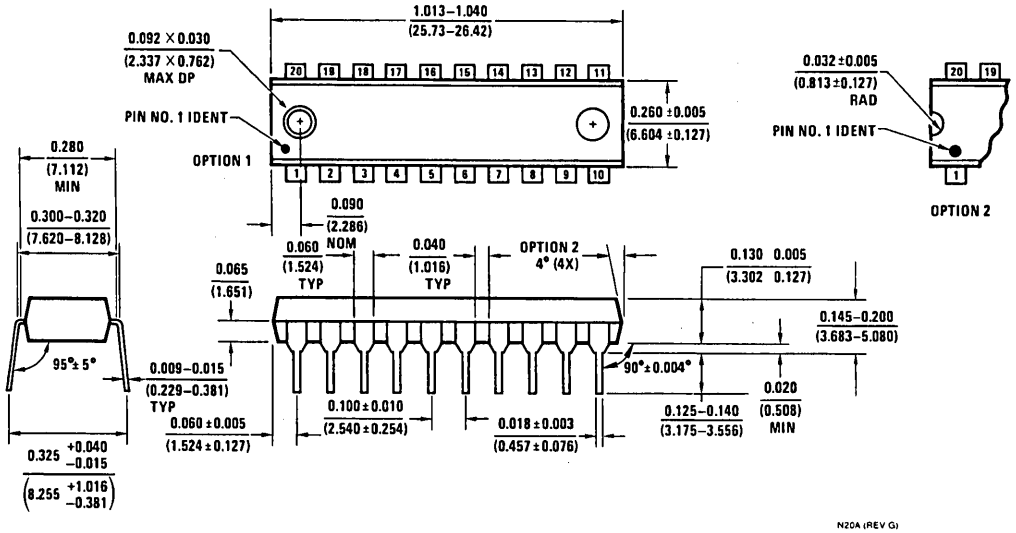

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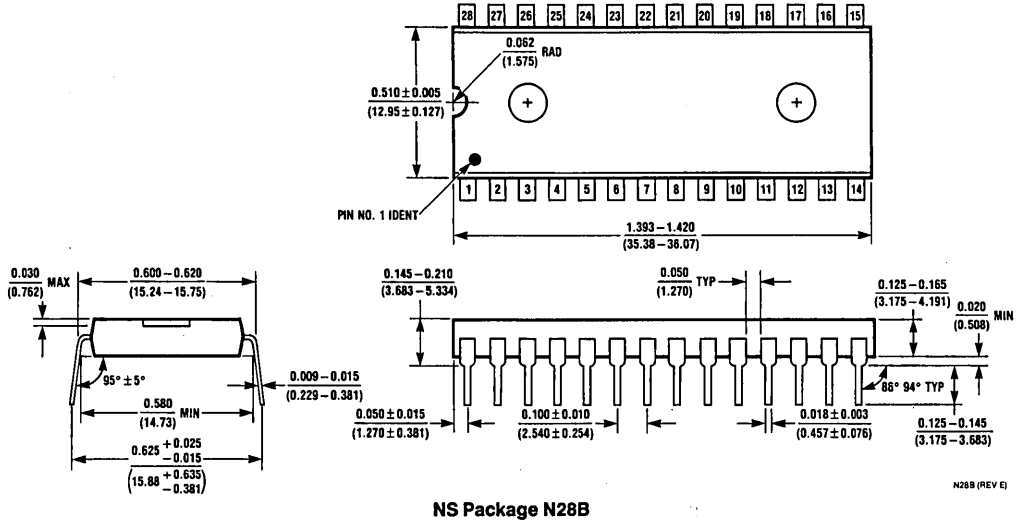

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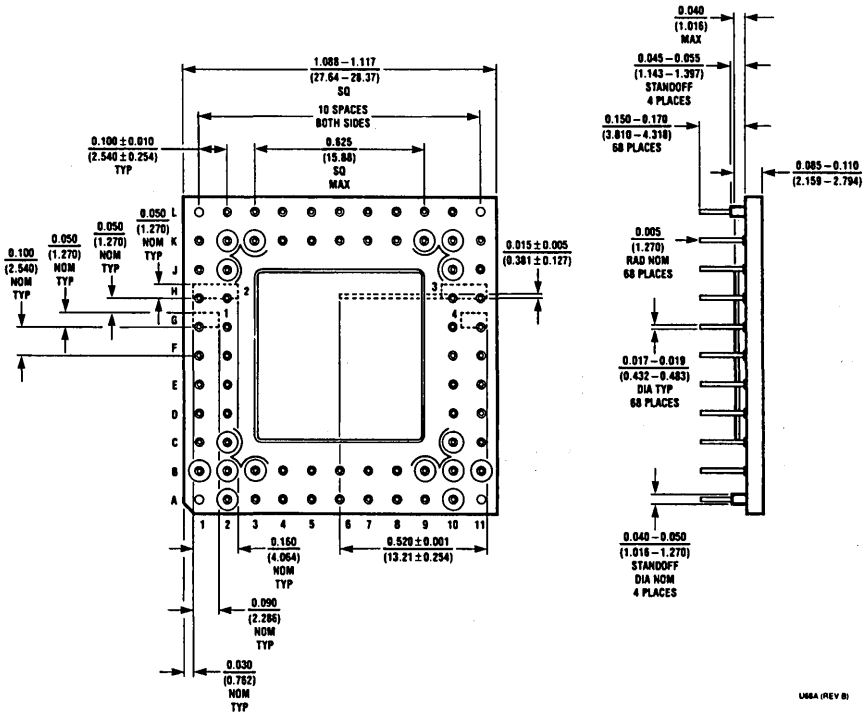

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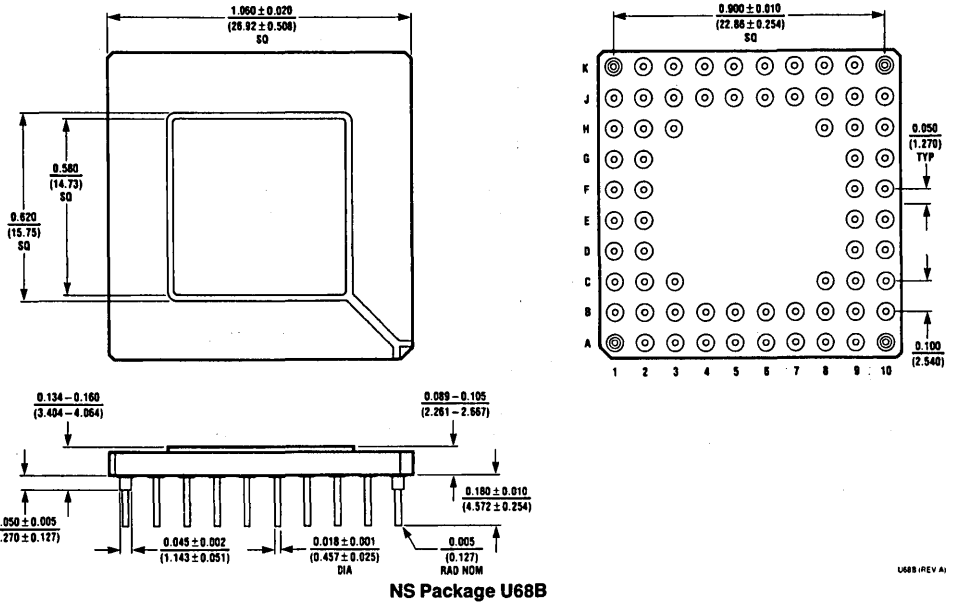

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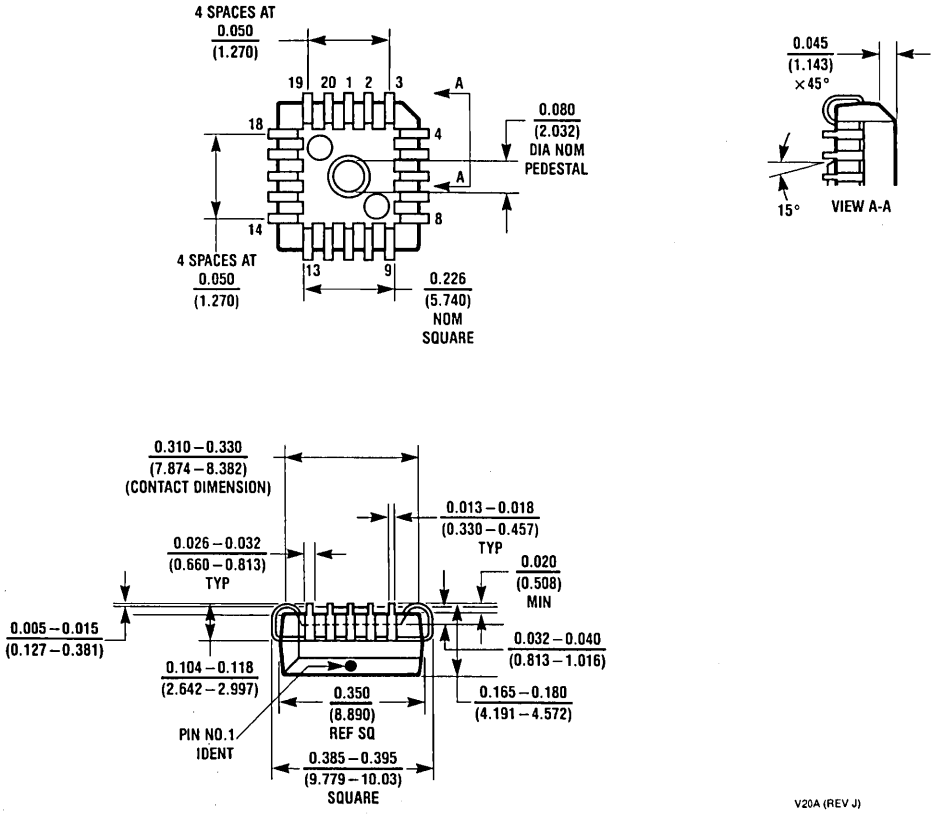

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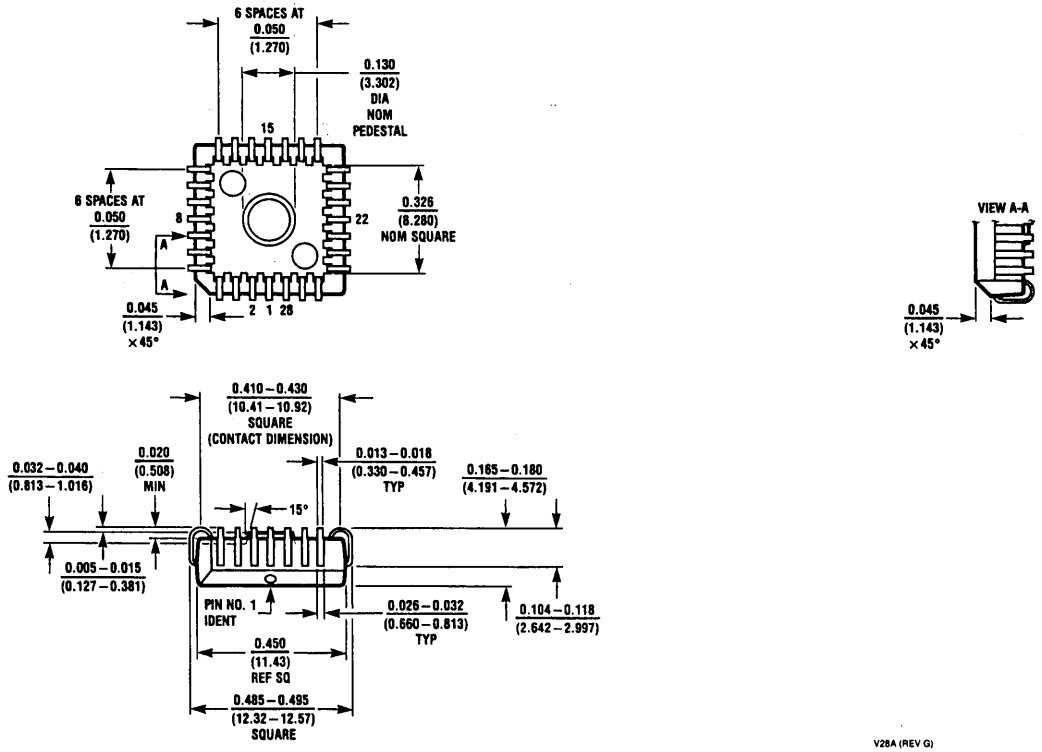

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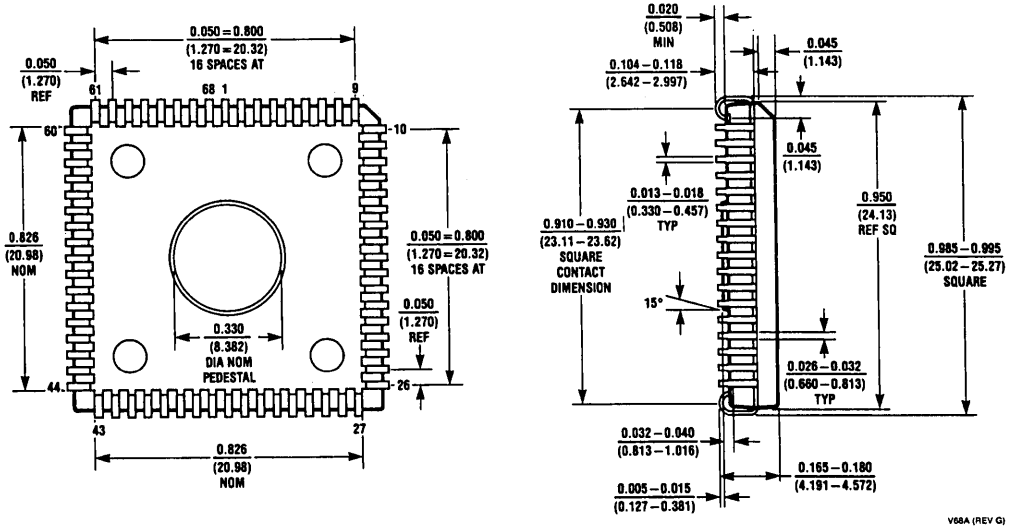

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