1984
LINEAR SUPPLEMENT
DATABOOK

NATIONAL
SEMICONDUCTOR
CORPORATION

LINEAR SUPPLEMENT

DATABOOK

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Introduction

The 1984 Linear Supplement provides the most recent information available on National's new linear products. This supplement also provides a comprehensive index of product listings published in the master databook. New products described herein are indicated by an asterisk and bold type. Revised datasheets are listed in bold type. National's master/supplement databook system allows you to make product selections based on your knowledge of our latest product offerings.

This supplement edition presents approximately 500 pages of specifications. It includes applications, descriptions, features, and diagrams of voltage regulators; op amps; voltage comparators; A/D and D/A converters; industrial building blocks; audio, radio, and TV circuits; advanced telecommunications devices; and DIGITALKER® speech synthesis circuits, as well as other analog products. National's linear products offer economy, quality, and reliability. For further information on any of our new products, contact your National Semiconductor sales representative.

Einleitung

Der Ergänzungsband Lineare Produkte 1984 enthält die aktuellsten Informationen über Nationals neue lineare Produkte. Dieser Zusatzband bietet ebenfalls ein umfassendes Verzeichnis aller Produktaufstellungen, die im Hauptdatenbuch enthalten sind. Hier beschriebene neue Produkte sind in Fettdruck, mit ein *. Überarbeitete Datenblätter sind in Fettdruck aufgeführt. National-Datenbücher - Hauptbände und Zusatzbände - geben Ihnen die Möglichkeit, Ihre Produktwahl gemäß unserer jüngsten Produktangebote zu treffen.

Die vorliegende Ergänzungsausgabe umfaßt etwa 500 Seiten Spezifikationen. Sie enthält Angaben zu Anwendungen, Beschreibungen, Zusätzen und Diagramme von Spannungsreglern, op amps, Spannungsvergleicher, A/D- und D/A-Wandler, industrielle Bausteine, Audio-, Rundfunk- und Fernsehschaltungen, neueste Telecombauteile, DIGITALKER®- Sprachsynthese-Schaltungen sowie andere analoge Produkte. Nationals lineare Produkte sind kostengünstig, von hoher Qualität und zuverlässig. Sollten Sie weitere Informationen über unsere neuen Produkte wünschen, setzen Sie Sich bitte mit Ihrem National Semiconductor-Vertreter in Verbindung.

Introduction

Afin de permettre à sa clientèle une mise à jour plus facile, National Semiconductor propose en plus de sa documentation classique un Additif Linéaire 1984. Ce dernier comporte les informations les plus récentes sur les produits nouvellement sortis ainsi qu'un index récapitulatif de ceux déjà exposés dans le livre principal.

Les produits nouveaux qu'il comporte sont signales par une astérisque et des caractères gras. Les fiches techniques mises a jour sont imprimées en caractère gras. Ce nouveau système a pour but d'orienter la clientèle sur les produits les plus récents.

L'edition supplémentaire contient à peu près 500 pages de specifications. Elle comprend possibilités d'application, descriptions, unités supplémentaires, courbes caracteristiques de regulateurs de tension, op amps, comparateurs de tension, convertisseurs A/D et D/A, modules industriels, circuits audio, radio et TV, dispositifs avancés de télecommunication, circuits de synthèse de parole Digitalker, ainsi que d'autres produits analogiques. Les produits linéaires de National sont économiques, de haute qualite et fiables. Si vous désirez des renseignements supplémentaires sur nos produits nouveaux, veuillez vous adresser a votre représentant local de National Semiconductor.

Introduzione

Il supplemento 1984 al catalogo "LINEAR" della National fornisce le più aggiornate informazioni sui nuovi prodotti lineari. Questo supplemento presenta, inoltre, un indice completo di tutti i prodotti che sono pubblicati sul catalogo principale. I nuovi prodotti descritti nel supplemento sono caratterizzati in neretto, con una *.

I fogli tecnici (datasheets) corretti sono pubblicati in neretto. Il sistema catalogo principale/supplemento permette una perfetta scelta dei prodotti, grazie alle più recenti ed aggiornate informazioni disponibili sugli stessi.

Questo supplemento presenta circa 500 pagine di specifiche. Esso comprende applicazioni, descrizioni, caratteristiche e diagrammi su: regolatori di tensione, amplificatori operazionali, convertitori A/D e D/A, circuiti dedicati per sistemi industriali, circuiti audio e radio/TV, dispositivi avanzati per telecomunicazioni, circuiti per la sintesi del parlato DIGITALKER oltre a numerosi altri.

I prodotti lineari della National Semiconductor offrono qualità, affidabilità e soluzioni economiche.

Per ulteriori informazioni sui prodotti elencati Vi preghiamo di contattare il nostro ufficio vendite più vicino.

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Devices listed in Boldface are included in this supplement with changes. Devices listed in Boldface with an asterisk (*) are new parts.

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Section 1

Amplifiers

Amplifiers

Section Contents

National Semiconductor

PRELIMINARY

LH0032, LH0032A, LH0032C, LH0032AC
Ultra Fast FET-Input Operational Amplifier

General Description

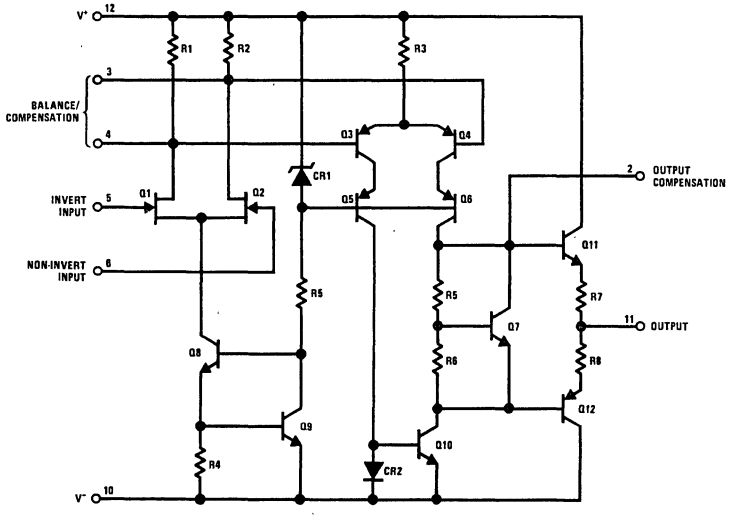
The LH0032/LH0032A is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- As low as 2 mV max input offset voltage
- FET input
- Offset null with single pot
- No compensation for gains above 50
- Peak output current to 100 mA

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A converters, buffers in data acquisition systems and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 and LH0032A are guaranteed for operation over the temperature range −55°C to +125°C, the LH0032C and LH0032AC are guaranteed for −25°C to +85°C.

Block and Connection Diagrams



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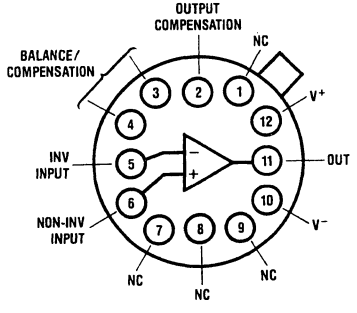

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Order Number LH0032, LH0032A, LH0032C, LH0032AC
See NS Package H12B

Absolute Maximum Ratings

Supply Voltage, V_S	±18V	Operating Temperature Range, T_A	
Input Voltage, V_{IN}	$\pm V_S$	LH0032G/AG	−55°C to +125°C
Differential Input Voltage	±30V or $\pm 2V_S$	LH0032CG/ACG	−25°C to +85°C
Power Dissipation, P_D		Operating Junction Temperature, T_J	175°C
T_A = 25°C	1.5W, derate 100°C/W to 125°C (Note 1)	Storage Temperature Range	−65°C to +150°C
T_C = 25°C	2.2W, derate 70°C/W to 125°C (Note 1)	Lead Temp. (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted (Note 2)

Symbol	Parameter	Test Conditions		LH0032A			LH0032AC			LH0032			LH0032C			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage		$T_A = T_J = 25°C$ (Note 3)		2	2 5		2	5 7		2	5 10		2	15 20	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift		(Note 4)		15	30		15	30		15	50		15	50	µV/°C
I_{OS}	Input Offset Current	$V_{IN} = 0$	$T_J = 25°C$ (Note 3) $T_A = 25°C$ (Note 5)			10 250 10			30 500 3			25 250 25			50 500 5	pA pA nA
I_B	Input Bias Current		$T_J = 25°C$ (Note 3) $T_A = 25°C$ (Note 5)			50 1 25			150 5 10			100 1 50			500 5 15	pA nA nA
*V_{INCM}	Input Voltage Range			±10	±12		±10	±12		±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = \pm 10V$		50	60		50	60		50	60		50	60		dB
A_{VOL}	Open-Loop Voltage Gain	$V_O = \pm 10V$, f = 1 kHz R_L = 1 kΩ (Note 6)	$T_J = 25°C$	60	70		60	70		60	70		60	70		dB
				57			57			57			57			
V_O	Output Voltage Swing	R_L = 1 kΩ		±10	±13.5		±10	±13		±10	±13.5		±10	±13		V
I_S	Power Supply Current	$T_A = 25°C$, $I_O = 0$ (Note 6)			18	20		20	22		18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	$\Delta V_S = 10V$ (±5 to ±15V)		50	60		50	60		50	60		50	60		dB

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1k\Omega$, $T_J = 25°C$ (Note 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
S_R	Slew Rate	$A_V = +1$	$\Delta V_{IN} = 20V$	350	500		V/µs
t_s	Settling Time to 1% of Final Value	$A_V = -1$,			100		
t_s	Settling Time to 0.1% of Final Value				300		ns
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$			8	20	
t_D	Small Signal Delay Time				10	25	

Note 1. In order to limit maximum junction temperature to +175°C, it may be necessary to operate with VS < ±15V when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See applications notes AN-277, "Applications of Wide-Band Buffer Amplifiers" and AN-253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2. LH0032AG/G are 100% production tested as specified at 25°C, 125°C, and −55°C. LH0032ACG/CG are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 3. Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25 C. When supply voltages are ± 15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 4. LH0032AG/G are 100% production tested for this parameter. LH0032ACG/CG are sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 5. Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

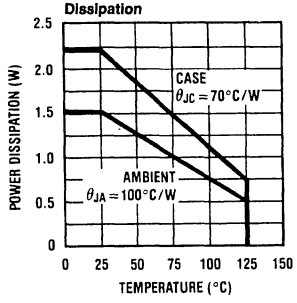
Note 6. Guaranteed thru correlated automatic pulse testing at T_J = 25°C.

Note 7. Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

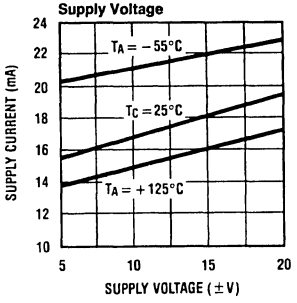
* Limits at high/low temp. are sample tested to LTPD = 10 on LH0032CG/ACG.

Typical Performance Characteristics

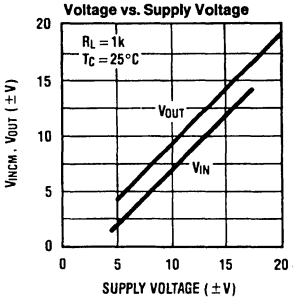
Maximum Power Dissipation



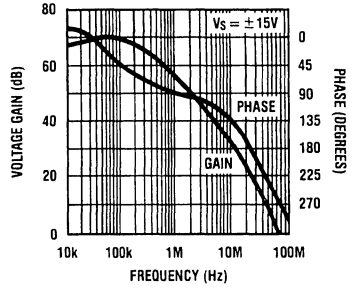
Supply Current vs. Supply Voltage



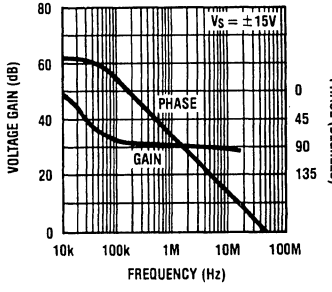
Input Voltage Range and Output Voltage vs. Supply Voltage



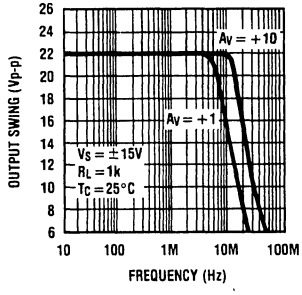
Bode Plot (Uncompensated)



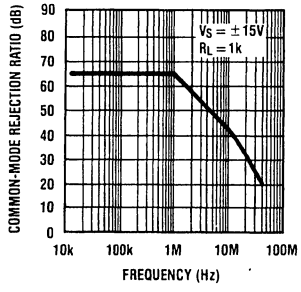
Bode Plot (Unity Gain Compensation)



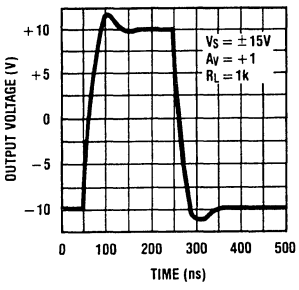
Large Signal Frequency Response



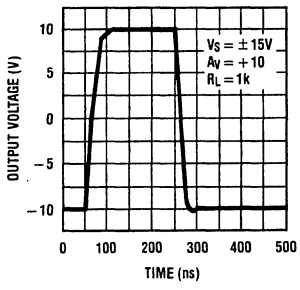
Common Mode Rejection Ratio vs. Frequency



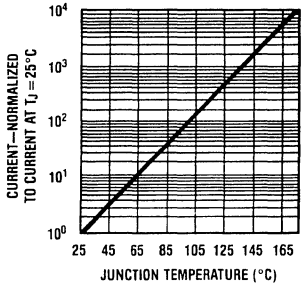
Large Signal Pulse Response



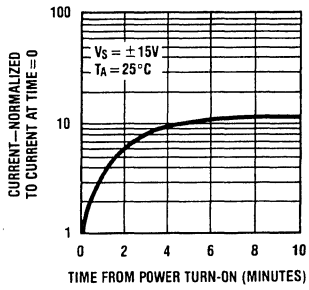
Large Signal Pulse Response



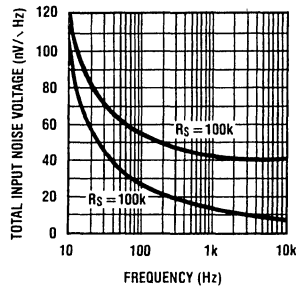
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up



Input Bias Current vs. Input Voltage



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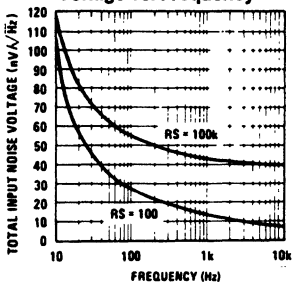
Typical Performance Characteristics (Continued)

Total Input Noise Voltage vs. Frequency*



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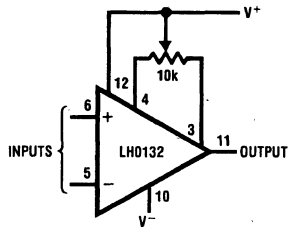
*Noise voltage includes contribution from source resistance.

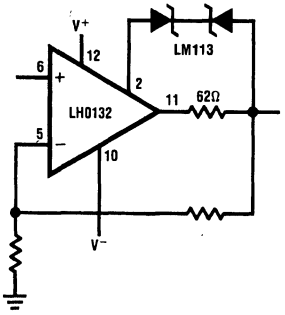
Auxiliary Circuits

Offset Null



TL/K/5265–15

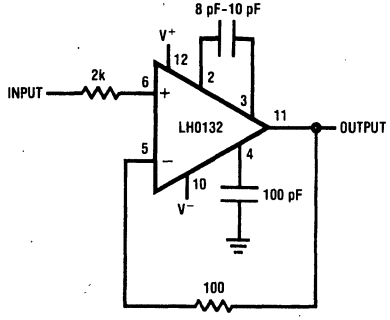
Output Short Circuit Protection



TL/K/5265–16

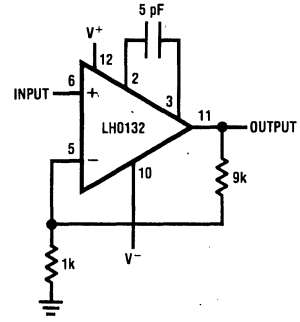
Typical Applications

Unity Gain Amplifier



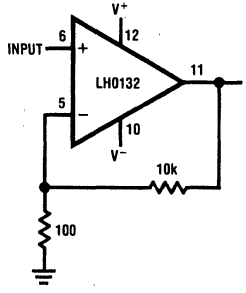
TL/K/5265–17

10X Buffer Amplifier



TL/K/5265–18

100X Buffer Amplifier



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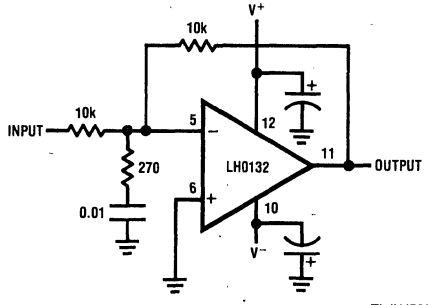
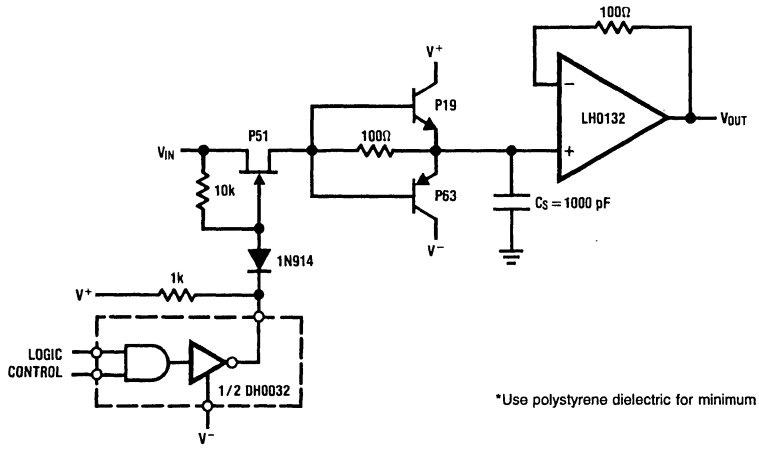
Non-Compensated Unity Gain Inverter



TL/K/5265–20

Typical Applications (Continued)

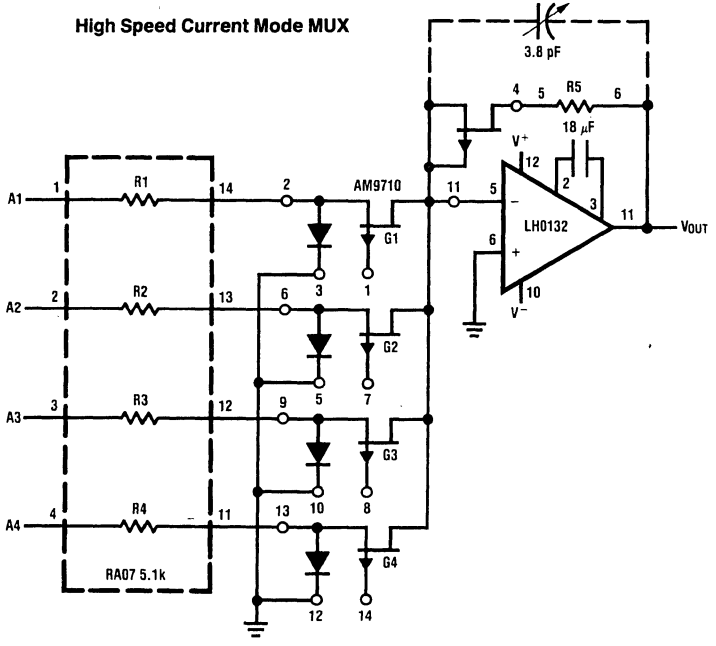
High Speed Sample and Hold



TL/K/5265-21

*Use polystyrene dielectric for minimum drift

High Speed Current Mode MUX



TL/K/5265-22

Applications Information

POWER SUPPLY DECOUPLING

The LH0032/LH0032A, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be by passed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

INPUT CURRENT

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40–60°C above free-air ambient temperature when supplies are ±15V. The de-

Applications Information (Continued)

vice temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

INPUT CAPACITANCE

The input capacitance to the LH0032/LH0032C is typically 5pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

HEAT SINKING

While the LH0032/LH0032A is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information request Application Note AN-253.

National Semiconductor

LH0033/LH0033A/LH0033C/LH0033AC,LH0063/LH0063C Fast and Damn Fast Buffer Amplifiers

General Description

The LH0033/LH0033A and LH0063 are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH0033/LH0033A will provide ±10 mA into 1 kΩ loads (±100 mA peak) at slew rates of 1500V/μs. The LH0063 will provide ±250 mA into 50Ω loads (±500 mA peak) at slew rates up to 6000V/μs. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high speed A to Ds and comparators. In addition, the LH0063 can continuously drive 50Ω coaxial cables or be used as a yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

Advantages

- Only 10V supply needed for 5 Vp-p video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems
- Output drive adequate for most loads
- Single pre-calibrated package

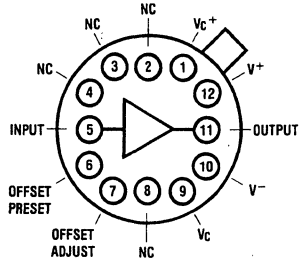
Features

- Damn fast (LH0063): 6000 V/μs
- Wide range single or dual supply operation
- Wide power bandwidth: DC to 100 MHz
- High output drive: ±10V with 50Ω load
- Low phase non-linearity: 2 degrees
- Fast rise times: 2 ns
- High current gain: 120 dB
- High input resistance: $10^{10}\Omega$

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH0033/LH0033A and LH0063 are specified for operation from −55°C to +125°C; whereas, the LH0033C/LH0033AC and LH0063C are specified from −25°C to +85°C. The LH0033/LH0033A is available in either a 1.5W metal TO-8 package or an 8-pin ceramic dual-in-line package. The LH0063 is available in a 5W 8-pin TO-3 package.

Connection Diagrams

Metal Can Package

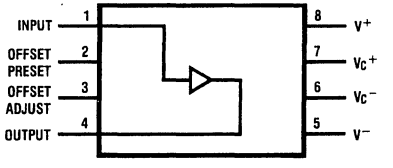


TOP VIEW

TL/K/5507-1

Case is electrically isolated

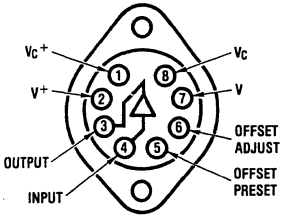
Dual-In-Line Package



TOP VIEW

TL/K/5507-2

Metal Can Package



TOP VIEW

TL/K/5507-3

Case is electrically isolated

Order Numbers LH0033/LH0033A/LH0033C/ LH0033AC, LH0063/LH0063C
See NS Packages H12B, HY08A, K08A

Teflon is a trademark of E. I. DuPont Corp.

Absolute Maximum Ratings

Supply Voltage($V^+ - V^-$)	40V	Peak Output Current	
Maximum Power Dissipation (See Curves)		LH0063/LH0063C	±500 mA
LH0063/LH0063C	5W	LH0033A/LH0033AC/LH0033/LH0033C	±250 mA
LH0033A/LH0033AC/LH0033/LH0033C	1.5W	Operating Temperature Range	
Maximum Junction Temperature	175°C	LH0033A/LH0033 and LH0063	−55°C to + 125°C
Input Voltage	$\pm V_S$	LH0033AC/LH0033C and LH0063C	−25°C to + 85°C
Continuous Output Current		Storage Temperature Range	−65° to + 150°C
LH0063/LH0063C	±250 mA	Lead Temperature (Soldering, 10 seconds)	300°C
LH0033A/LH0033AC/LH0033/LH0033C	±100 mA		

DC Electrical Characteristics

$V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage	$R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ (Note 2)		1	5		6	15		5.0	10		12	20	mV
	$R_S = 100\Omega$			10			20			15			25	mV
Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3)		50	100		50	100		50	100		50	100	µV/°C
Input Bias Current	$V_{IN} = 0V$													
	$T_J = 25°C$ (Note 2)			100			250			250			500	pA
	$T_A = 25°C$ (Note 4)			1.5			2.5			2.5			5.0	nA
	$T_J = T_A = T_{MAX}$			7.5			10			10			20	nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0k\Omega$	0.97	0.98	1.00	0.96	0.98	1.00	0.97	0.98	1.00	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1\ k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k$		6.0	10		6.0	10		6.0	10		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k$	±12			±12			±12			±12			V
	$V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±9.0			±9.0			±9.0			±9.0			V
Supply Current	$V_{IN} = 0V$ (Note 5)		20	22		21	24		20	22		21	24	mA
Power Consumption	$V_{IN} = 0V$		600	660		630	720		600	660		630	720	mW

AC Electrical Characteristics

$T_C = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0\ K\Omega$ (Note 6)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	$V_{IN} = \pm 10V$	1000	1500		1000	1400		1000	1500		1000	1400		V/µs
Bandwidth	$V_{IN} = 1.0$ Vrms		100			100			100			100		MHz
Phase Non-Linearity	BW = 1.0Hz to 20 MHz		2.0			2.0			2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		2.9			3.2			2.9			3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2			1.5			1.2			1.5		ns
Harmonic Distortion	f > 1 kHz		<0.1			<0.1			<0.1			<0.1		%

Note 1: LH0033A is 100% production tested as specified at 25° C, 125°C, and −55°C. LH0033AC/C are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limited are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

Note 3: LH0033A is 100% production tested for this parameter. LH0033AC/C are sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 4: Measured in still air 7 minutes after application of power. Guaranteed through correlated automatic pulse testing.

Note 5: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	LH0063			LH0063C			Units
		Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage	$R_S \leq 100k\Omega$, $T_J = 25°C$ $R_L = 100\Omega$ (Note 2)		10	25 100		10	50 100	mV mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100\ k\Omega$ (Note 3)		300			300		$\mu V/°C$
Input Bias Current	$T_J = 25°C$ (Note 2)		0.1	0.5		0.1	0.5	nA
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 1\ k\Omega$	0.94	0.96	1.0	0.94	0.96	1.0	V/V
Voltage Gain	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 50\Omega$ $T_J = 25°C$	0.92	0.93	0.98	0.91	0.93	0.98	V/V
Input Capacitance	Case Shorted to Output		8.0			8.0		pF
Output Impedance	$V_{OUT} = \pm 10V$, $R_S \leq 100\ k\Omega$, $R_L = 50\Omega$		1.0	4.0		1.0	4.0	Ω
Output Current Swing	$V_{IN} = \pm 10V$, $R_S \leq 100\ k\Omega$	0.2	0.25		0.2	0.25		A
Output Voltage Swing	$R_L = 50\Omega$	± 10	± 13		± 10	± 13		V
Output Voltage Swing	$V_S = \pm 5.0V$, $R_L = 50\Omega$, $T_J = 25°C$	5.0	7.0		5.09	7.0		V
Supply Current	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$ (Note 4)		35	65		35	65	mA
Supply Current	$V_S = \pm 5.0V$ (Note 4)		50			50		mA
Power Consumption	$T_J = 25°C$, $R_L = \infty$, $V_S = \pm 15V$		1.05	1.95		1.05	1.95	W
Power Consumption	$V_S = \pm 5.0V$		500			500		mW

AC Electrical Characteristics $T_J = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 50\Omega$ (Note 5)

Parameter	Conditions	LH0063			LH0063C			Units
		Min	Typ	Max	Min	Typ	Max	
Slew Rate	$R_L = 1.0\ k\Omega$, $V_{IN} = \pm 10V$		6000			6000		$V/\mu s$
Slew Rate	$R_L = 50\Omega$, $V_{IN} = \pm 10V$, $T_J = 25°C$	2000	2400		2000	2400		$V/\mu s$
Bandwidth	$V_{IN} = 1.0$ Vrms		200			200		MHz
Phase Non-Linearity	BW = 1.0 Hz to 20 MHz		2.0			2.0		degrees
Rise Time	$\Delta V_{IN} = 0.5V$		1.6			1.9		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.9			2.1		ns
Harmonic Distortion			<0.1			<0.1		%

Note 1: LH0063 is 100% production tested as specified at 25°C, 125°C, and −55°C. LH0063C is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B ans I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs temperature graph for expected values.

Note 3: LH0063 is 100% production tested for this parameter. LH0063C is sample tested only. Limits are not used to calculate outgoing quality levels.

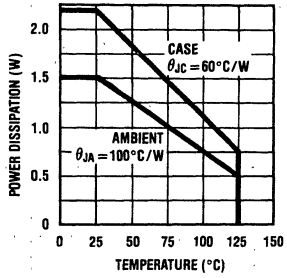
$\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 4: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

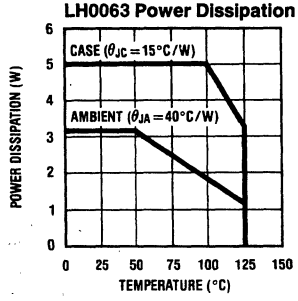
Note 5: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Typical Performance Characteristics

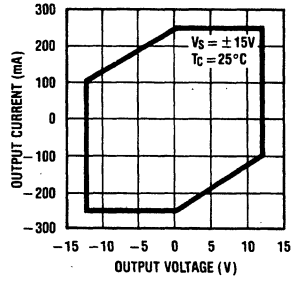
LH0033 Power Dissipation



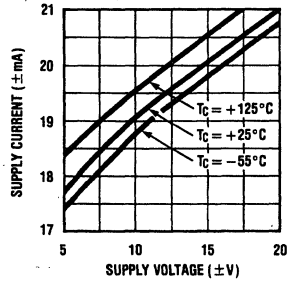
LH0063 Power Dissipation



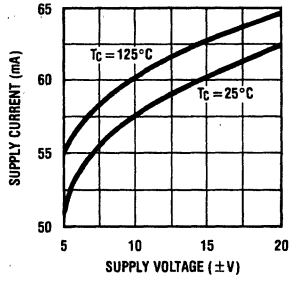
LH0063 DC Safe Operating Area



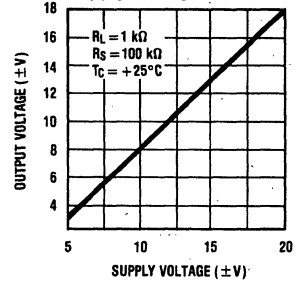
LH0033 Supply Current vs Supply Voltage



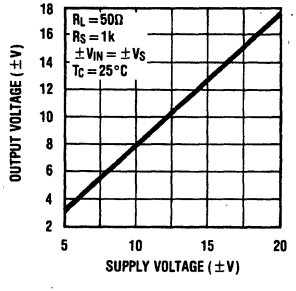
LH0063 Supply Center vs Supply Voltage



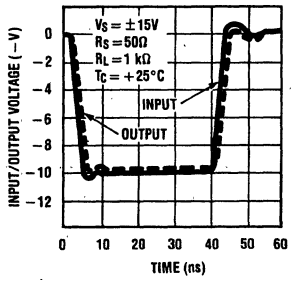
LH0033 Output Voltage vs Supply Voltage



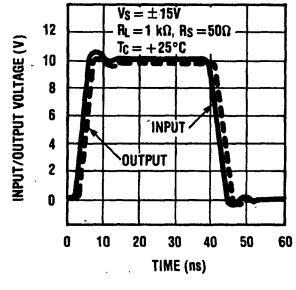
LH0063 Output Voltage vs Supply Voltage



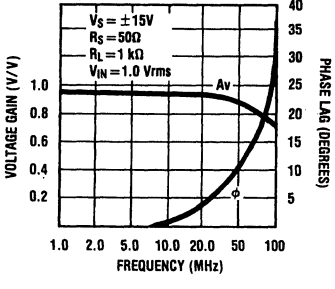
LH0033 Negative Pulse Response



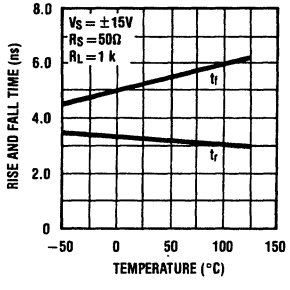
LH0033 Positive Pulse Response



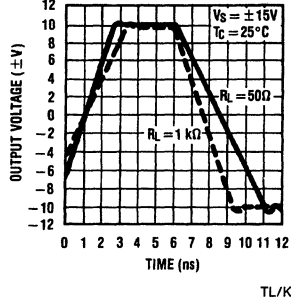
LH0033 Frequency Response



LH0033 Rise and Fall Time vs Temperature



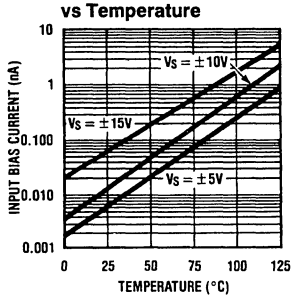
LH0063 Large Signal Pulse Response



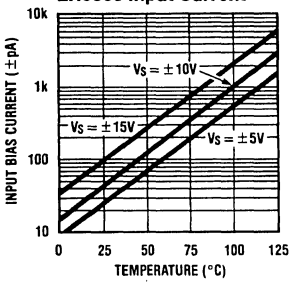
TL/K/5507–4

Typical Performance Characteristics (Continued)

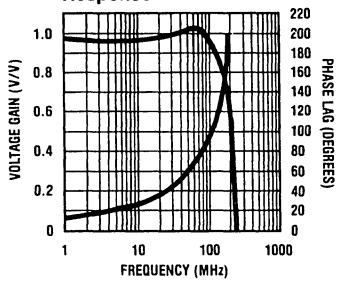
LH0033 Input Bias Current vs Temperature



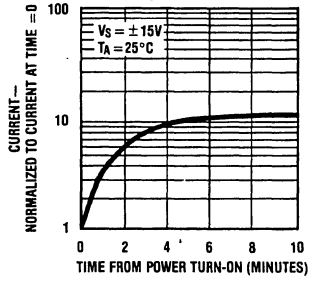
LH0063 Input Current



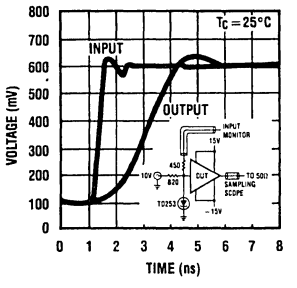
LH0063 Frequency Response



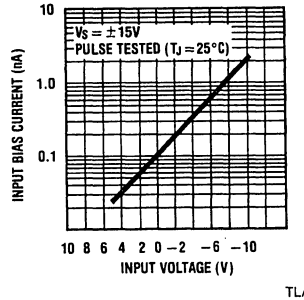
LH0033 Normalized Input Bias Current During Warm-Up



LH0063 Small Signal Rise Time



LH0033 Input Bias Current vs Input Voltage



TL/K/5507–5

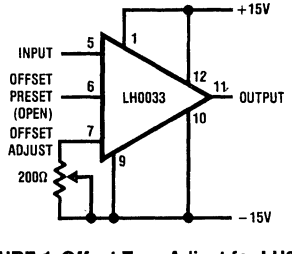
Application Hints

RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the LH0033 and LH0063 since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

OFFSET VOLTAGE ADJUSTMENT

Both the LH0033's and LH0063's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω for the LH0033 or 1 kΩ for the LH0063 between the offset adjust pin and V⁻, as illustrated in *Figures 1* and *2*.



TL/K/5507–6

FIGURE 1. Offset Zero Adjust for LH0033 (Pin numbers shown for TO-8)

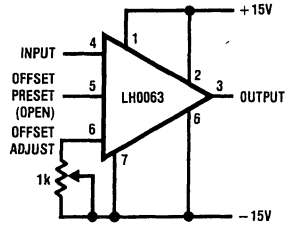


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FIGURE 2. Offset Zero Adjust for LH0063

Application Hints (Continued)

OPERATION FROM SINGLE OR ASYMMETRICAL POWER SUPPLIES

Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.005(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be $-35mV$. This may be adjusted to zero as described in *Figure 2*. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the Typical Applications section.

SHORT CIRCUIT PROTECTION

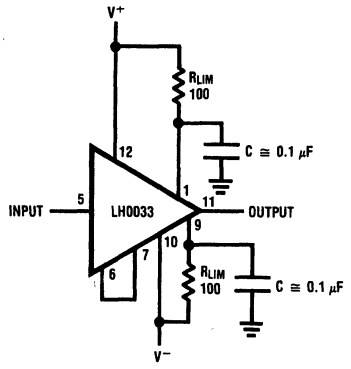
In order to optimize transient response and output swing, output current limit has been omitted from the LH0033 and LH0063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in *Figures 3 and 4*. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where:

$I_{SC} \leq 100$ mA for LH0033

$I_{SC} \leq 250$ mA for LH0063



TL/K/5507–8

FIGURE 3. LH0033 Using Resistor Current Limiting

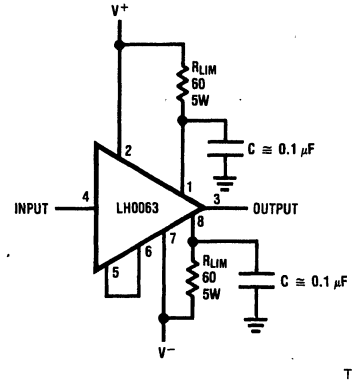


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FIGURE 4. LH0063 Using Resistor Current Limiting

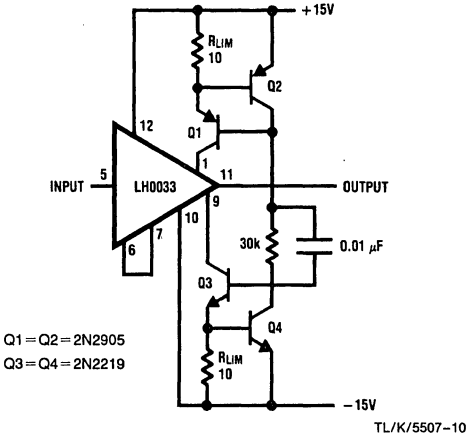
The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C^+ and V_C^- pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in *Figures 5* and *6*. In *Figures 5* and *6*, the current sources are saturated during normal operation, thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

For *Figure 5:*

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\ mA} = 10\Omega$$

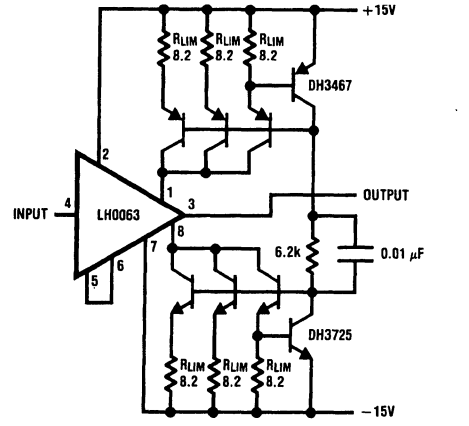
In *Figure 6*, quad transistor arrays are used to minimize can count and:

$$R_{LIM} = \frac{V_{BE}}{1/3(I_{SC})} = \frac{0.6V}{1/3(200\ mA)} = 8.2\Omega$$



TL/K/5507–10

FIGURE 5. LH0033 Current Limiting Using Current Sources



TL/K/5507–11

FIGURE 6. LH0063 Current Limiting Using Current Sources

CAPACITIVE LOADING

Both the LH0033 and LH0063 are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times dV/dt)$ should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH0033:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250\ mA$$

and for the LH0063:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500\ mA$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below total package power rating:

$$P_D pkg. \geq P_{DC} + P_{AC}$$

$$P_D pkg. \geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} \cong (Vp\text{-}p)^2 \times f \times C_L$$

where:

Vp-p = Peak-to-peak output voltage swing

f = Frequency

C_L = Load Capacitance

OPERATION WITHIN AN OP AMP LOOP

Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LH0032, LH0062, or LM118. An isolation resistor of 47Ω should be used between the op amp output and the input of LH0033. The wide bandwidths and high slew rates of the LH0033 and LH0063 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

HARDWARE

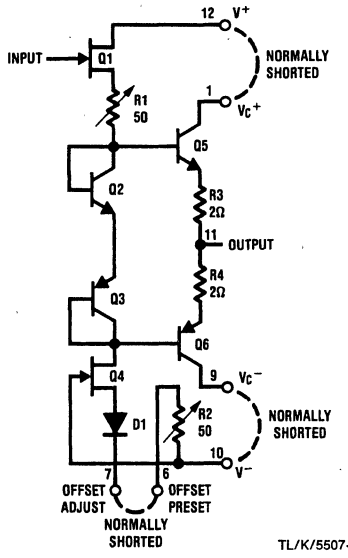
In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to the system chassis.

DESIGN PRECAUTION

Power supply bypassing is necessary to prevent oscillation with both the LH0033 and LH0063 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within $<1/4$ to $1/2$" of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel for the LH0033; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances. For the LH0063, two 0.1 μF ceramic and one 4.7 μF solid tantalum capacitors in parallel will be necessary on each supply lead.

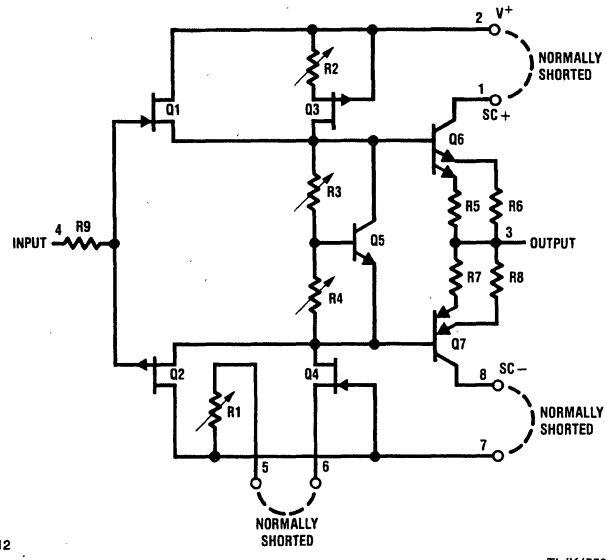
Schematic Diagrams

LH0033/LH0033A



TL/K/5507–12

LH0063

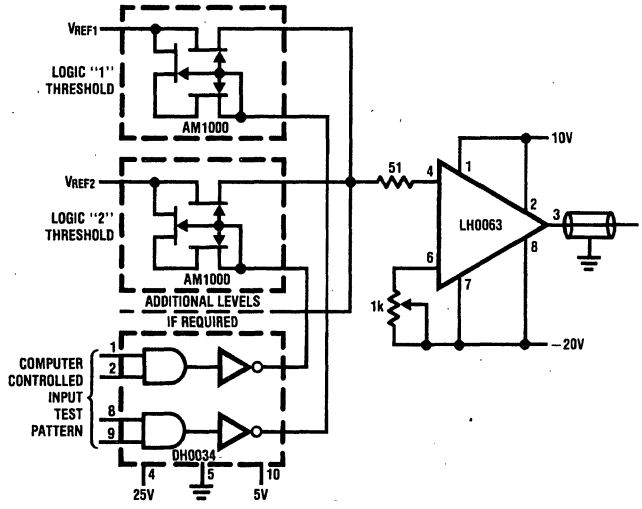


TL/K/5507–13

Pin numbers shown for TO-8 ("G") package.

Typical Applications

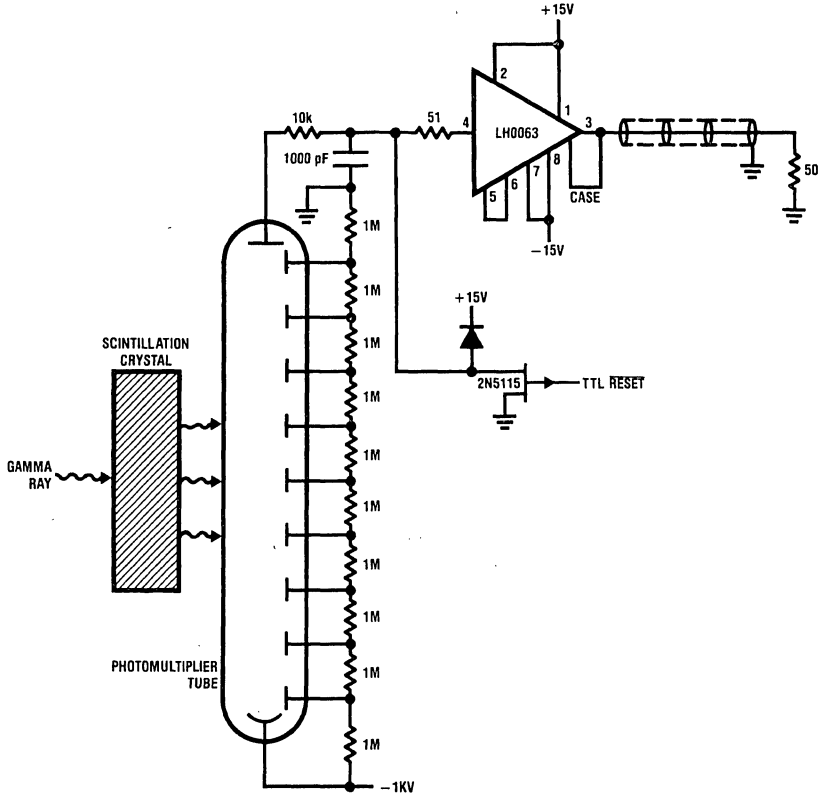
High Speed Automatic Test Equipment
Forcing Function Generator



TL/K/5507–14

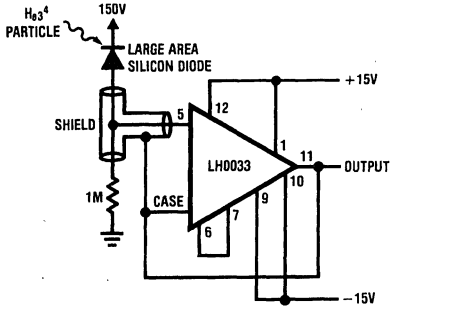
Typical Applications (Continued)

Gamma Ray Pulse Integrator



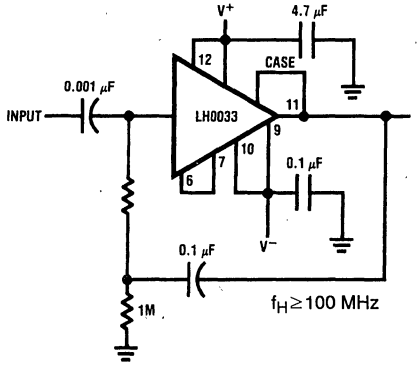
TL/K/5507–15

Nuclear Particle Detector



TL/K/5507–16

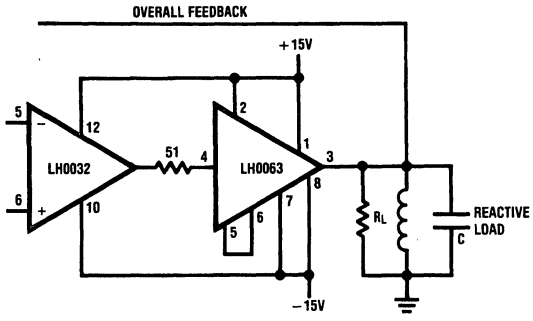
High Input Impedance AC Coupled Amplifier



TL/K/5507–17

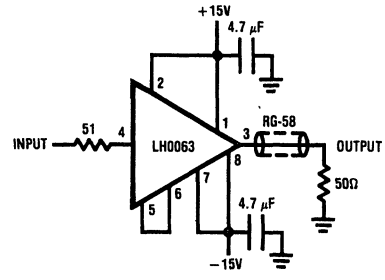
Typical Applications (Continued)

Isolation Buffer



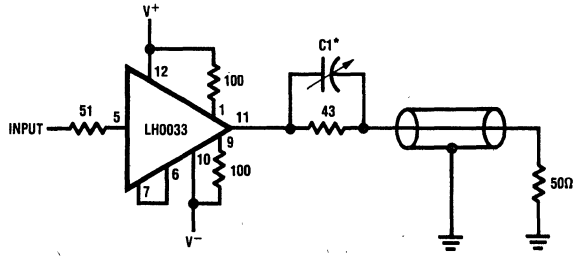
TL/K/5507–18

Coaxial Cable Driver



TL/K/5507–19

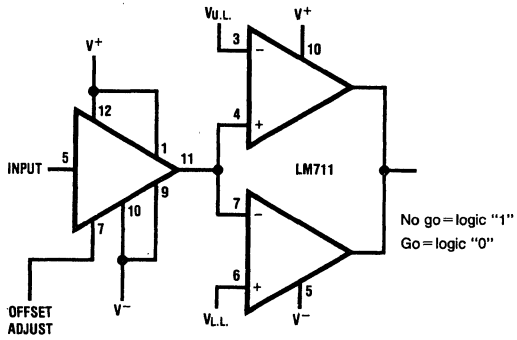
Coaxial Cable Driver



TL/K/5507–20

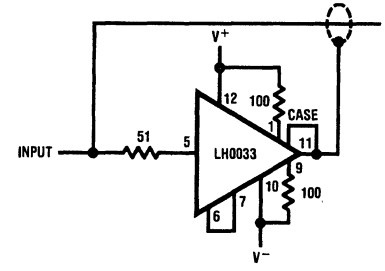
*Select C1 for optimum pulse response

High Input Impedance Comparator with Offset Adjust



TL/K/5507–21

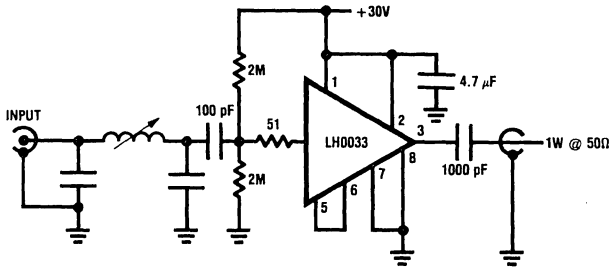
Instrumentation Shield/Line Driver



TL/K/5507–22

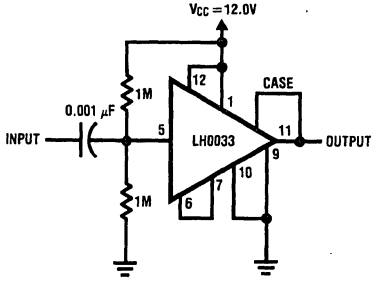
Typical Applications (Continued)

1W CW Final Amplifier



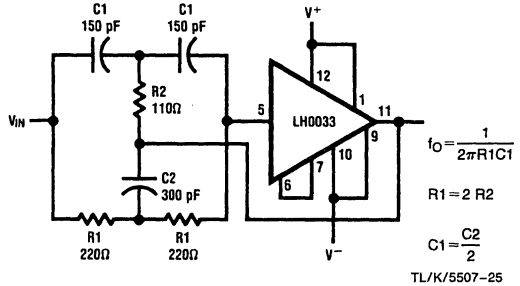
TL/K/5507-23

Single Supply AC Amplifier



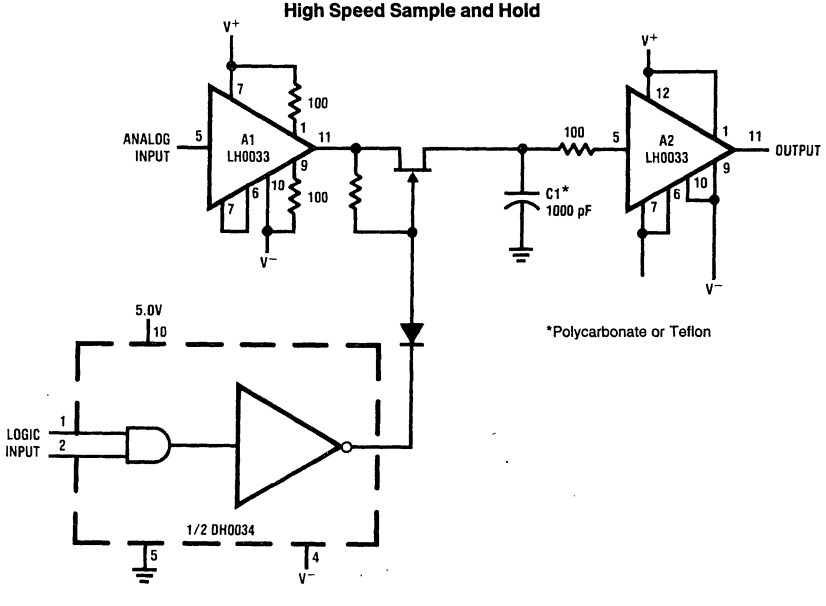
TL/K/5507-24

4.5 MHz Notch Filter



TL/K/5507-25

High Speed Sample and Hold



*Polycarbonate or Teflon

TL/K/5507-26

National Semiconductor

LH0132, LH0132C
Ultra-Fast FET-Input Operational Amplifier

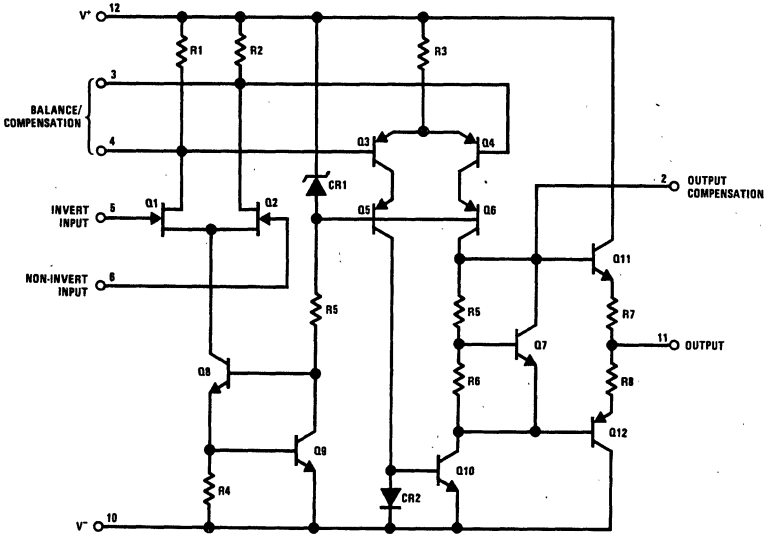
General Description

The LH0132 is a high slew rate, high input impedance differential amplifier. It was developed specifically for sample and hold and other fast signal handling applications which require very low input currents over the full input voltage range. Input offset and bias currents are guaranteed over a full input common mode range of −10 volts to +10 volts.

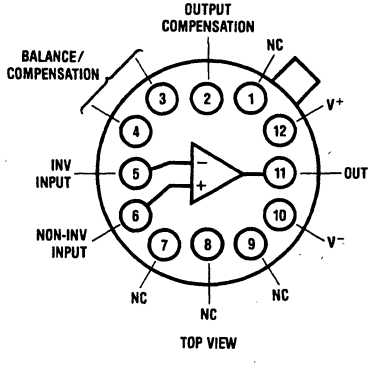
Features

- 600 pA I_{bias} at V_{IN} = ±10V
- 500 V/μs slew rate
- 70 MHz bandwidth
- 5 mV offset voltage
- FET input
- No compensation for gains above 50
- Peak output current to 100 mA

Block and Connection Diagrams



TL/K/5499–4



TL/K/5499–5

Order Number LH0132G or LH0132CG
See NS Package H12B

Absolute Maximum Ratings

Supply Voltage, V_S	±18V	Operating Temperature Range, T_A	
Input Voltage, V_{IN}	$\pm V_S$	LH0132G/AG	−55°C to +125C°C
Differential Input Voltage	±30V or $\pm 2V_S$	LH0132CG/ACG	−25°C to +85°C
Power Dissipation, P_D		Operating Junction Temperature, T_J	175°C
T_A = 25°C	1.5W, derate 100°C/W to 125°C (Note 1)	Storage Temperature Range	−65°C to +150°C
T_C = 25°C	2.2W, derate 70°C/W to 125°C (Note 1)	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted (Note 2)

Parameter		Test Conditions		LHO132G			LHO132CG			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OS}	Input Offset Voltage	V_{IN}=0	$T_A=T_J$=25°C (Note 3)		2	5 10		2	10 20	mV
$\Delta V_{OS}\Delta T$	Average Offset Voltage Drift		(Note 4)		25	50		25	50	µV/°C
I_{OS}	Input Offset Current	−10V≤$_{IN}$≤10V	T_J=25°C (Note 3) T_A=25°C (Note 5) $T_J=T_A=T_{MAX}$			15 150 15			30 300 5	pA pA nA
I_B	Input Bias Current		T_J=25°C (Note 3) T_A=25°C (Note 5) $T_J=T_A=T_{MAX}$			75 1 25			150 5 15	pA nA nA
*V_{INCM}	Input Voltage Range			±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	ΔV_{IN} = ±10V		50	60		45	60		dB
A_{VOL}	Open-Loop Voltage Gain	V_O = ±10 V f=70 kHZ	T_J=25°C	60	70		50	70		dB
		R_L=1 kΩ	(Note 6)	57			47			
V_O	Output Voltage Swing	R_L=1 kΩ		±10	±13.5		±10	±13		V
I_S	Power Supply Current	T_J=25°C, I_O=0	(Note 6)		18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	AV_S=10V (±5 to ±15)		50	60		45	60		dB

AC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ, T_J = 25°C (Note 7)

Parameter		Conditions		Min.	Typ.	Max.	Units
S_R	Slew Rate	A_V=+1		350	500		V/µS
t_s	Settling Time to 1% of Final Value	A_V=−1,	ΔV_{IN}=20V		100		ns
t_s	Settling Time to 0.1% of Final Value				300		ns
t_R	Small Signal Rise Time	A_V=+1, ΔV_{IN}=1V			8	20	ns
t_D	Small Signal Delay Time				10	25	ns

Note 1. In order to limit maximum junction temperature to +175°C, it may be necessary to operate with VS < ±15V when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See Applications Notes AN-277, "Applications of Wide-Band Buffer Amplifiers" and AN-253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2. LH0132G is 100% production tested as specified at 25°C, 150°C, and −55°C. LH0132CG is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 3. Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25° C. When supply voltages are ± 15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 4. LH0132G is 100% production tested for this parameter. LH0132CG is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 5. Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

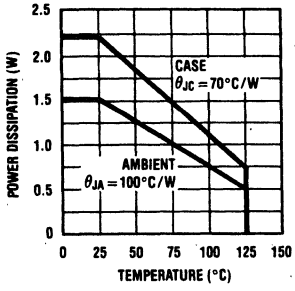
Note 6. Guaranteed thru correlated automatic pulse testing at T_J = 25°C.

Note 7. Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

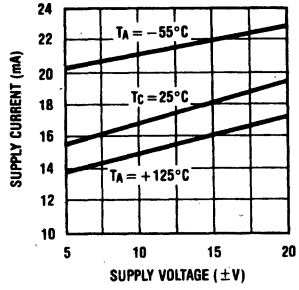
* Limits at high/low temp. are sample tested to LTPD=10 on LH0132CG/ACG.

Typical Performance Characteristics

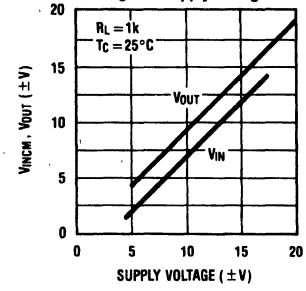
Maximum Power Dissipation



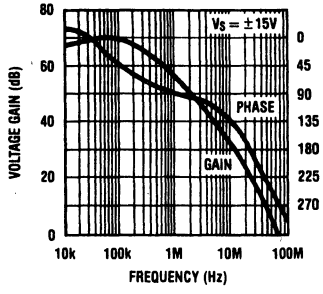
Supply Current vs. Supply Voltage



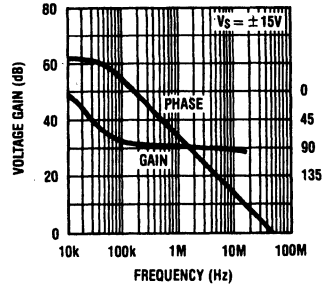
Input Voltage Range and Output Voltage vs. Supply Voltage



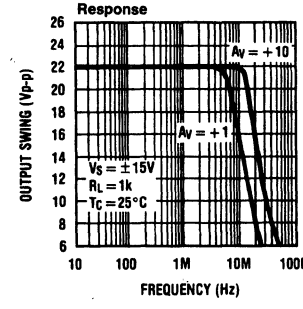
Bode Plot (Uncompensated)



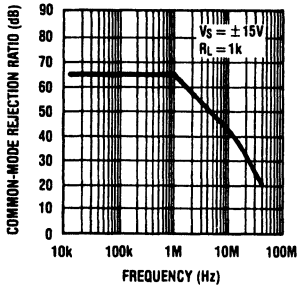
Bode Plot (Unity Gain Compensation)



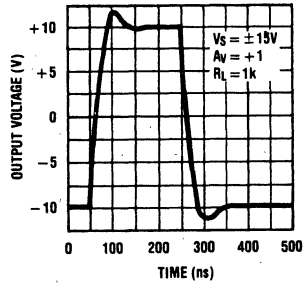
Large Signal Pulse Response



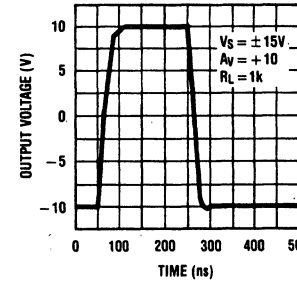
Common Mode Rejection Ratio vs. Frequency



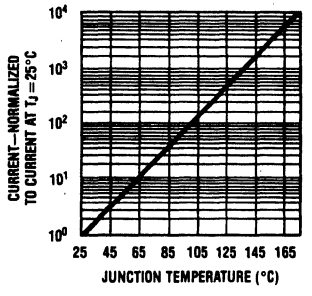
Large Signal Frequency Response



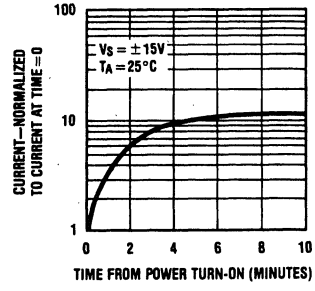
Large Signal Pulse Response



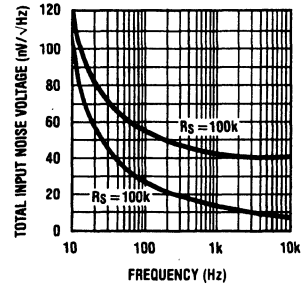
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up



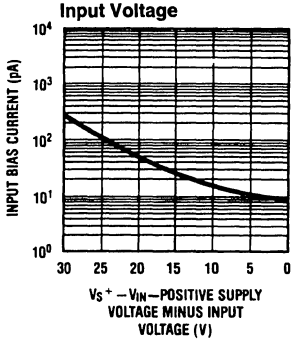
Total Input Noise Voltage vs. Frequency*



TL/K/5499–6

Typical Performance Characteristics (Continued)

Input Bias Current vs. Input Voltage



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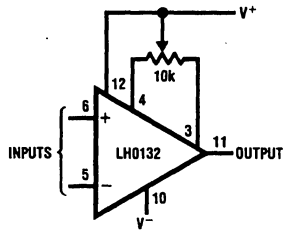
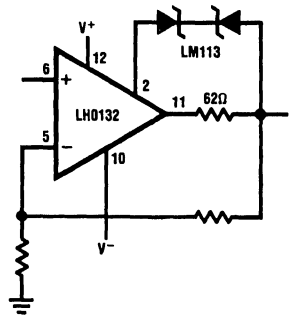
Auxiliary Circuits

Offset Null



TL/K/5499-8

Output Short Circuit Protection

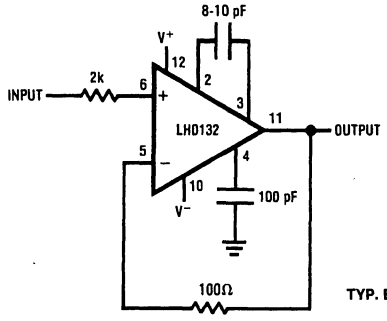


TL/K/5499-9

*Noise voltage includes contribution from source resistance.

Typical Applications

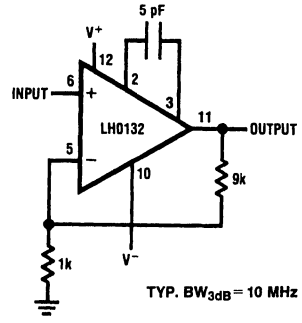
Unity Gain Amplifier



TYP. $BW_{3ddBB} = 45$ MHz

TL/K/5499-1

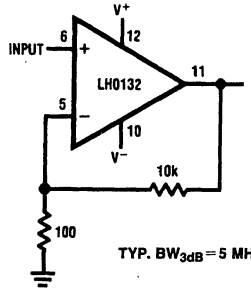
10X Buffer Amplifier



TYP. $BW_{3dB} = 10$ MHz

TL/K/5499-10

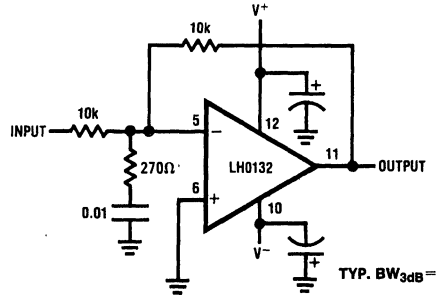
100X Buffer Amplifier



TYP. $BW_{3dB} = 5$ MHz

TL/K/5499-11

Non-Compensated Unity Gain Inverter

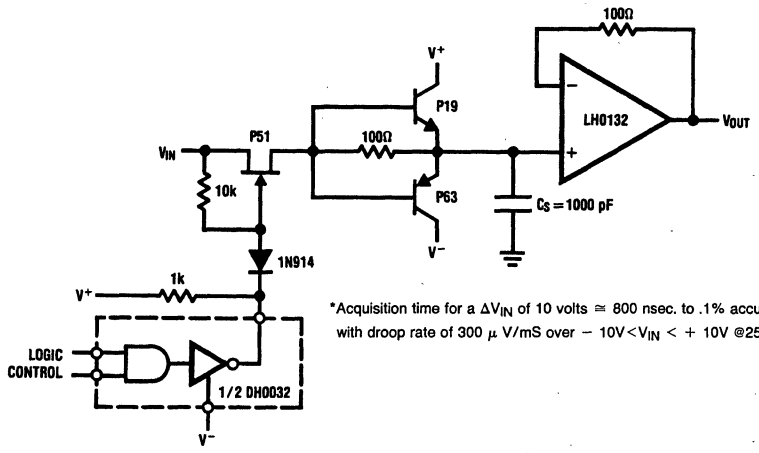


TYP. $BW_{3dB} = 70$ MHz

TL/K/5499-2

Typical Applications (Continued)

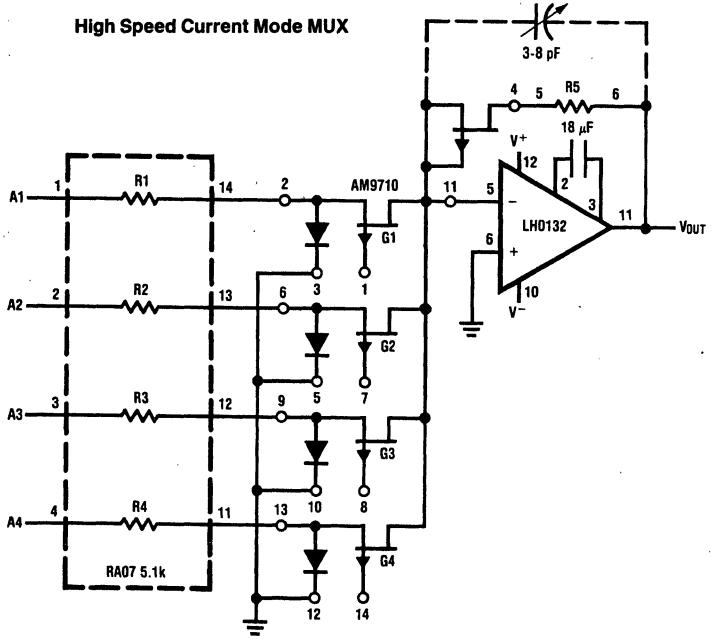
High Speed Sample and Hold



*Acquisition time for a ΔV_{IN} of 10 volts ≅ 800 nsec. to .1% accuracy with droop rate of 300 μ V/mS over − 10V<V_{IN} < + 10V @25°C.

TL/K/5499–12

High Speed Current Mode MUX



TL/K/5499–3

Applications Information

POWER SUPPLY DECOUPLING

The LH0132, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

INPUT CURRENT

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40–60°C above free-

air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels.

Due to the cascoded FET input stage design of the LH0132, the gate-to-drain voltage is kept below this threshold, and the bias current remains relatively constant over the entire common-mode input voltage range.

INPUT CAPACITANCE

The input capacitance to the LH0132/LH0132C is typically 5 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

HEAT SINKING

While the LH0132 is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information request Application Note AN-253.

National Semiconductor

LM163/LM363 Precision Instrumentation Amplifier

General Description

The LM163 is a monolithic true instrumentation amplifier. It requires no external parts for fixed gains of 10, 100 and 1000. High precision is attained by on-chip trimming of offset voltage and gain. A super-beta biopolar input stage gives very low input bias current and voltage noise, extremely low offset voltage drift, and high common-mode rejection ratio. A new two-stage amplifier design yields an open loop gain of 10,000,000 and a gain bandwidth product of 30 MHz, yet remains stable for all closed loop gains. The LM163 operates with supply voltages from ±5V to ±18V with only 1.5 mA current drain.

The LM163's low voltage noise, low offset voltage and offset voltage drift make it ideal for amplifying low-level, low-impedance transducers. At the same time, its low bias current and high input impedance (both common-mode and differential) provide excellent performance at high impedance levels. These features, along with its ultra-high common-mode rejection, allow the LM163 to be used in the most demanding instrumentation amplifier applications, replacing expensive hybrid, module or multi-chip designs. Because the LM163 is internally trimmed, precision external resistors and their associated errors are eliminated.

The 16-pin dual-in-line package provides pin-strappable gains of 10, 100 or 1000. Its twin differential shield drivers eliminate bandwidth loss due to cable capacitance. Compensation pins allow overcompensation to reduce bandwidth and output noise, or to provide greater stability with capacitive loads. Separate output force, sense and reference pins permit gains between 10 and 10,000 to be programmed using external resistors.

On the 8-pin TO-5 and miniDIP packages, gain is internally set at 10, 100 or 500 but may be increased with external resistors. The shield driver and offset adjust pins are omitted on the 8-pin versions.

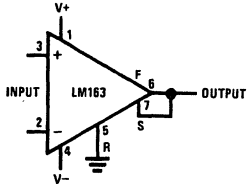
The LM163/LM163A is rated for −55°C to +125°C. The LM363/LM363A is rated for 0°C to 70°C.

Features

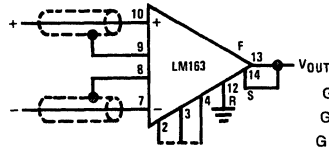
- Offset and gain pretrimmed
- 12 nV/√Hz input noise (G = 500/1000)
- 130 dB CMRR tyical (G = 500/1000)
- 2 nA bias current typical
- No external parts required
- Dual shield drivers
- Available at 0.5 μV/°C maximum drift
- Can be used as a high performance op amp
- Low supply current (1.5 mA typ)

Typical Connections

8-Pin Package



16-Pin Package

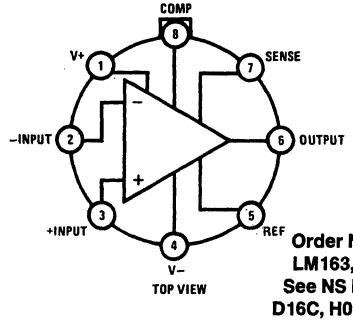


G = 10 2, 3, 4, open
G = 100 3–4 shorted
G = 1000 2–4 shorted

TL/H/5609–1

Connection Diagrams

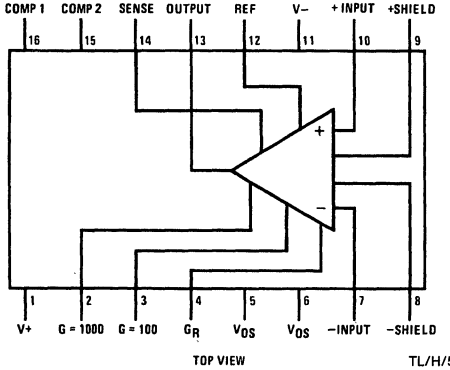
Metal Can Package*



*Pinout same for 8-pin DIP

Order Number LM163, LM363
See NS Package D16C, H08C, N08A, N16A

16-Pin Dual-In-Line Package



TL/H/5609–2

Absolute Maximum Ratings (Notes 3 and 9)

Supply Voltage	±18V	Input Voltage	Equal to Supply Voltage
Differential Input Voltage	±10V	Reference and Sense Voltage	±25V
Input Current	±20 mA		

LM163A/LM163 Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	LM163A		LM163		Units
		Typ	Tested Limit	Typ	Tested Limit	
FIXED GAIN (8-PIN)						
Input Offset Voltage	G=500	10	50	20	50	μV
			100		**150**	μV
	G=100	25	100	35	100	μV
			300		**400**	μV
	G=10	0.2	1.0	0.3	10	mV
			2.5		**4**	mV
Input Offset Voltage Drift	G=500	0.2	**0.5**	1	**2**	μV/°C
	G=100	1	**2**	2	**5**	μV/°C
	G=10	10	**15**	20	**50**	μV/°C
Gain Error (±10V Swing, 2 kΩ Load)	G=500	0.5	0.2	0.05	0.3	%
			0.4		**0.6**	%
	G=100	0.05	0.2	0.05	0.3	%
			0.35		**0.5**	%
	G=10	0.05	0.2	0.05	0.3	%
			0.3		**0.4**	%
PROGRAMMABLE GAIN (16-PIN)						
Input Offset Voltage	G=1000	10	50	25	100	μV
			100		**200**	μV
	G=100	25	150	50	300	μV
			300		**500**	μV
	G=10	0.3	1	0.5	2	mV
			3		**6**	mV
Input Offset Voltage Drift	G=1000	0.2	**0.5**	0.5	**3**	μV/°C
	G=100 (Note 4)	0.5	**2**	2	**6**	μV/°C
	G=10 (Note 4)	5	**25**	10	**50**	μV/°C
Gain Error (±10V Swing, 2 kΩ Load)	G=1000	1.0	1.5	1.0	1.5	%
			2.0		**2.0**	%
	G=100	0.05	0.2	0.05	0.3	%
			0.35		**0.5**	%
	G=10	0.4	1.0	0.4	1.0	%
			1.1		**1.1**	%
FIXED GAIN AND PROGRAMMABLE						
Gain Temperature Coefficient	G=1000	40		40		ppm/°C
	G=500	20		20		ppm/°C
	G=100, 10	10		10		ppm/°C
Gain Non-Linearity (±10V Swing, 2 kΩ Load)	G=10, 100	0.005	0.001	0.005	0.02	%
			0.02		**0.03**	%
	G=500, 1000	0.007	0.02	0.007	0.03	%
			0.04		**0.05**	%

LM163A/LM163 Electrical Characteristics (Continued) (Notes 1 and 2)

Parameter	Conditions	LM163A		LM163		Units
		Typ	Tested Limit	Typ	Tested Limit	
Common-Mode Rejection Ratio ($-11V \le V_{CM} \le 13V$)	G = 1000, 500	140	126	130	120	dB
			115		**106**	dB
	G = 100	103	112	125	106	dB
			100		**94**	dB
	G = 10	115	100	110	94	dB
			88		**82**	dB
Positive Supply Rejection Ratio (5V to 15V)	G = 1000, 500	130	120	130	120	dB
			110		**110**	dB
	G = 100	120	105	120	105	dB
			95		**95**	dB
	G = 10	100	90	100	90	dB
			78		**78**	dB
Negative Supply Rejection Ratio (−5V to −15V)	G = 1000, 500	120	110	120	105	dB
			100		**95**	dB
	G = 100	106	96	106	90	dB
			86		**80**	dB
	G = 10	86	80	86	75	dB
			68		**62**	dB
Input Bias Current		2	5	2	5	nA
			15		**15**	nA
Input Offset Current		1	2	1	2	nA
			3		**3**	nA
Common-Mode Input Resistance		100	20	100	15	GΩ
Differential Mode Input Resistance	G = 1000, 500	0.2		0.2		GΩ
	G = 100	2		2		GΩ
	G = 10	20		20		BΩ
Input Offset Current Change	$-11V \le V_{CM} \le 13V$	10	50	20	100	pA/V
			150		**300**	pA/V
Reference and Sense Resistance		50		50		kΩ
	Min		35, **30**		35, **30**	kΩ
	Max		70, **75**		70, **75**	kΩ
Open Loop Gain	$G_{CL} = 1000, 500$	10	2	10	2	V/μV
Supply Current	Positive	1.2	1.8	1.2	1.8	mA
			2.8		**2.8**	mA
	Negative	1.6	2.2	1.6	2.2	mA
			3.3		**3.3**	mA

Note 1: These conditions apply unless otherwise noted: $V^+ = V^- = 15V$, $V_{CM} = 0V$, $R_L = 2\ k\Omega$, reference pin grounded, sense pin connected to output and $T_j = 25°C$.

Note 2: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range is −55°C to +125°C for the LM163/LM163A.

Note 3: Maximum rated junction temperature is 150°C for the LM163/LM163A. Thermal resistance, junction to ambient, is 150°C/W for the TO-99 (H) package and 100°C/W for the ceramic DIP (D).

Note 4: These limits are guaranteed by correlation but not 100% production tested. They are not used in determining outgoing quality levels.

LM363A/LM363 Electrical Characteristics (Notes 5 and 6)

Parameter	Conditions	LM363A			LM363			Units
		Typ	Tested Limit (Note 7)	Design Limit (Note 8)	Typ	Tested Limit (Note 7)	Design Limit (Note 8)	
FIXED GAIN (8-PIN)								
Input Offset Voltage	G = 500	10	50		30	100	**300**	μV
			75					μV
	G = 100	25	100		50	200	**600**	μV
			200					μV
	G = 10	0.2	1.0		0.5	2.0	**5**	mV
			1.75					mV
Input Offset Voltage Drift	G = 500	0.2	**0.5**		1		**4**	μV/°C
	G = 100	1	**2**		2		**8**	μV/°C
	G = 10	10	**15**		20		**75**	μV/°C
Gain Error	G = 500	0.5	0.2	**0.4**	0.1	0.5	**0.8**	%
(±10V Swing, 2 kΩ Load)	G = 100	0.05	0.2	**0.35**	0.05	0.5	**0.7**	%
	G = 10	0.05	0.2	**0.3**	0.05	0.5	**0.6**	%
PROGRAMMABLE GAIN (16-PIN)								
Input Offset Voltage	G = 1000	10	50		50	200	**400**	μV
			100					μV
	G = 100	25	150		100	400	**800**	μV
			300					μV
	G = 10	0.3	1		1	3	**7**	mV
			3					mV
Input Offset Voltage Drift	G = 1000	0.2	**0.5**		1		**5**	μV/°C
	G = 100	0.5		**2**	2		**10**	μV/°C
	G = 10	5		**25**	10		**100**	μV/°C
Gain Error	G = 1000	1.0	1.5	**2.0**	2.0	2.5	**3.0**	%
(±10V Swing, 2 kΩ Load)	G = 100	0.05	0.2	**0.35**	0.1	0.5	**0.7**	%
	G = 10	0.4	1.0	**1.1**	0.6	1.5	**1.7**	%
FIXED GAIN AND PROGRAMMABLE								
Gain Temperature Coefficient	G = 1000	40			40			ppm/°C
	G = 500	20			20			ppm/°C
	G = 100, 10	10			10			ppm/°C
Gain Non-Linearity	G = 10, 100	0.005	0.01	**0.02**	0.01	0.03	**0.04**	%
(±10V Swing, 2 kΩ Load)	G = 500, 1000	0.007	0.02	**0.03**	0.01	0.05	**0.06**	%

LM363A/LM363 Electrical Characteristics (Continued) (Notes 5 and 6)

Parameter	Conditions	LM363A			LM363			Units
		Typ	Tested Limit (Note 7)	Design Limit (Note 8)	Typ	Tested Limit (Note 7)	Design Limit (Note 8)	
Common-Mode Rejection Ratio ($-11V \le V_{CM} \le 13V$)	G = 1000, 500	140	126	**115**	130	114	**104**	dB
	G = 100	130	112	**100**	120	94	**84**	dB
	G = 10	115	100	**88**	105	90	**80**	dB
Positive Supply Rejection Ratio (5V to 15V)	G = 1000, 500	130	120	**110**	130	110	**100**	dB
	G = 100	120	105	**95**	120	100	**95**	dB
	G = 10	100	90	**78**	100	85	**78**	dB
Negative Supply Rejection Ratio (−5V to −15V)	G = 1000, 500	120	110	**100**	120	100	**90**	dB
	G = 100	106	96	**86**	106	85	**75**	dB
	G = 10	86	80	**68**	86	70	**60**	dB
Input Bias Current		2	5	**10**	2	10	**20**	nA
Input Offset Current		1	2	**3**	1	3	**5**	nA
Common-Mode Input Resistance		100	20		100	8		GΩ
Differential Mode Input Resistance	G = 1000, 500	0.2			0.2			GΩ
	G = 100	2			2			GΩ
	G = 10	20			20			GΩ
Input Offset Current Change	$-11V \le V_{CM} \le 13V$	10	50	**150**	20	100	**300**	pa/V
Reference and Sense Resistance		50			50			kΩ
	Min		35	**30**		30	**27**	kΩ
	Max		70	**75**		80	**83**	kΩ
Open Loop Gain	G_{CL} = 1000, 500	10	2		10	1		V/μV
Supply Current	Positive	1.2	1.8	**2.8**	1.2	2.4	**3.0**	mA
							2.8	mA
	Negative	1.6	2.2	**3.3**	1.6	2.8	**3.4**	mA

Note 5: These conditions apply unless otherwise noted; $V^+ = V^- = 15V$, $V_{CM} = 0V$, $R_L = 2\ k\Omega$, reference pin grounded, sense pin connected to output and $T_j = 25°C$.

Note 6: Boldface limits are guaranteed over full temperature range. Operating ambient temperature range is 0°C to 70°C for the LM363/LM363A.

Note 7: Guaranteed and 100% production tested.

Note 8: Guaranteed but not 100% tested. These limits are not used in determining outgoing quality levels.

Note 9: Maximum rated junction temperature is 100°C for the LM363/LM363A. Thermal resistance, junction to ambient, is 150°C/W for the TO-99(H) package and the miniDIP (N), and 100°C/W for the ceramic DIP (D).

Typical Performance Characteristics $T_A = 25°C$

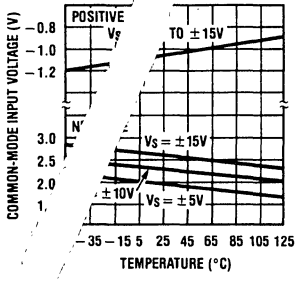
Parameter	Fixed Gain and Programmable			Units
	1000/500	100	10	
Input Voltage Noise, rms, 1 kHz	12	18	90	nV/√Hz
Input Voltage Noise (Note 6)	0.4	1.5	10	μVp-p
Input Current Noise, rms, 1 kHz	0.2	0.2	0.2	pA/√Hz
Input Current Noise (Note 6)	40	40	40	pAp-p
Bandwidth	30	100	200	kHz
Slew Rate	1	0.36	0.24	V/μS
Settling Time, 0.1% of 10V	70	25	20	μS
Offset Voltage Warm-Up Drift (Note 7)	5	15	50	μV
Offset Voltage Stability (Note 8)	5	10	100	μV
Gain Stability (Note 8)	0.01	0.005	0.05	%

Note 6: Measured for 100 seconds in a 0.01 Hz to 10 Hz bandwidth.

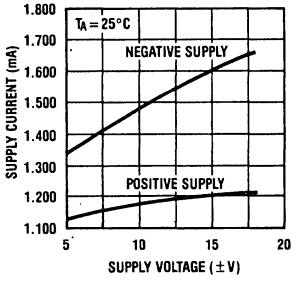
Note 7: Measured for 5 minutes in still air, $V^+ = V^- = -15V$. Warm-up drift is proportionally reduced at lower supply voltages.

Note 8: Change in 1000 hours of operation at 125°C ambient.

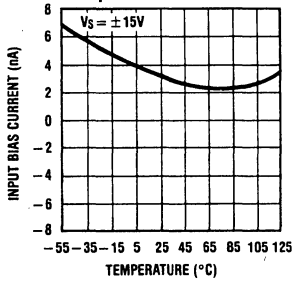
Common-Mode Input Voltage



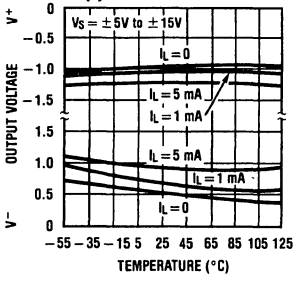
Supply Current vs Supply Voltage



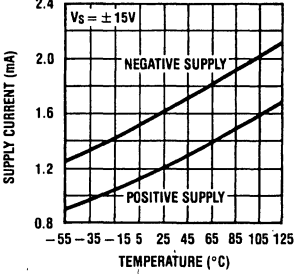
Input Bias Current vs Temperature



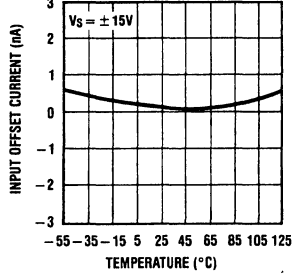
Output Swing Referred to Supplies



Supply Current vs Temperature



Input Offset Current vs Temperature



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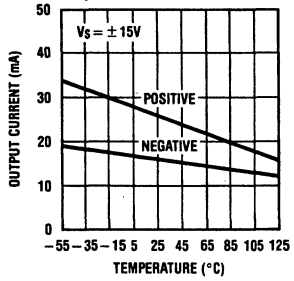
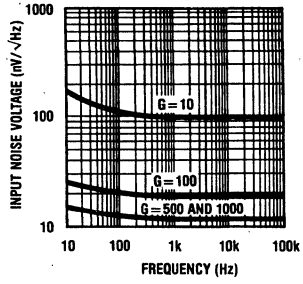
Typical Performance Characteristics (Continued)

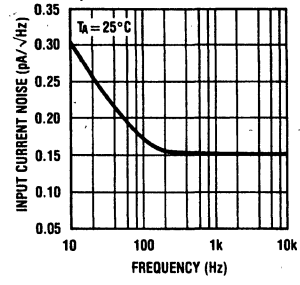
Output Current Limit



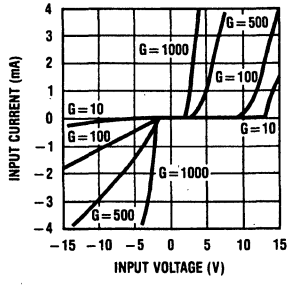
Input Noise Voltage



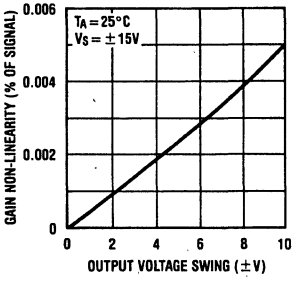
Input Current Noise



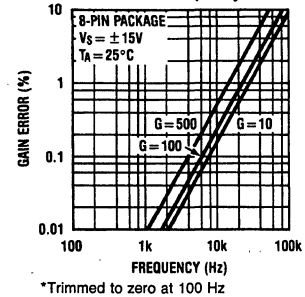
Input Current vs Voltage Overdrive



Gain Non-Linearity

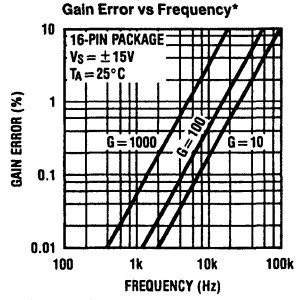


Gain Error vs Frequency*



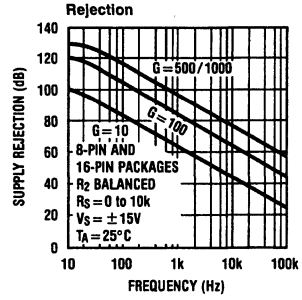
*Trimmed to zero at 100 Hz

Gain Error vs Frequency*

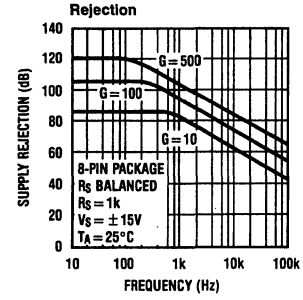


*Trimmed to zero at 100 Hz

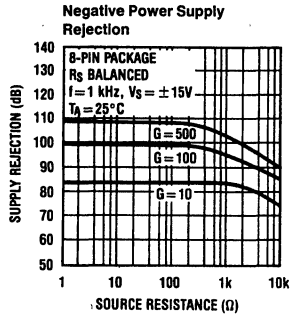
Positive Power Supply Rejection



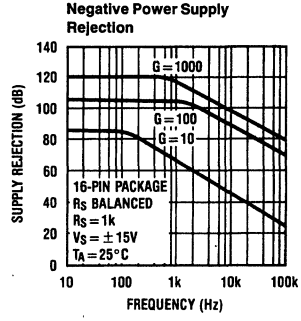
Negative Power Supply Rejection



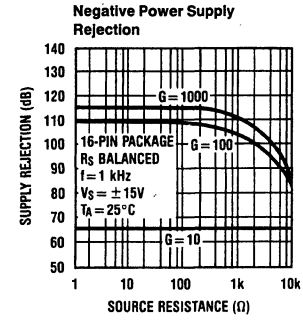
Negative Power Supply Rejection



Negative Power Supply Rejection



Negative Power Supply Rejection



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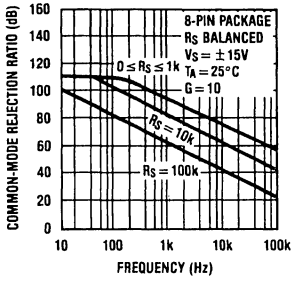
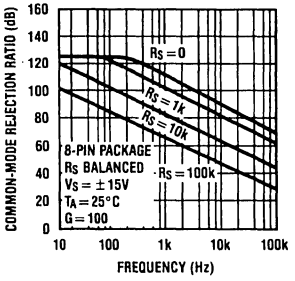
Typical Performance Characteristics (Continued)

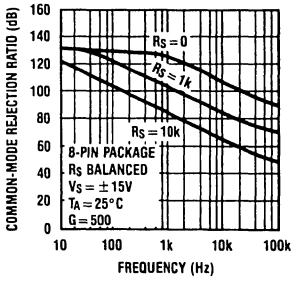
CMRR with Balanced Source Resistance



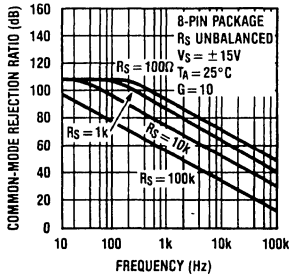
CMRR with Balanced Source Resistance



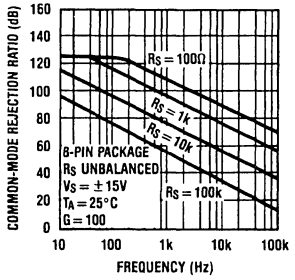
CMRR with Balanced Source Resistance



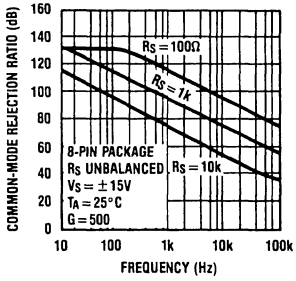
CMRR with Unbalanced Source Resistance



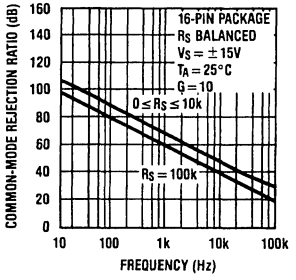
CMRR with Unbalanced Source Resistance



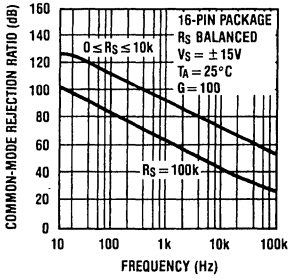
CMRR with Unbalanced Source Resistance



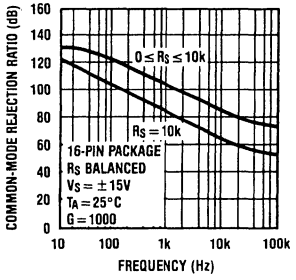
CMRR with Balanced Source Resistance



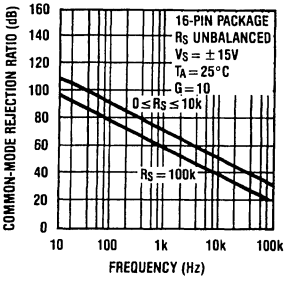
CMRR with Balanced Source Resistance



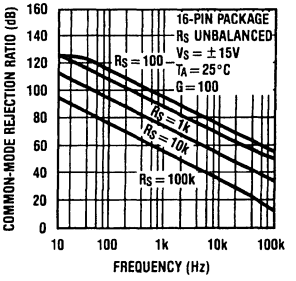
CMRR with Balanced Source Resistance



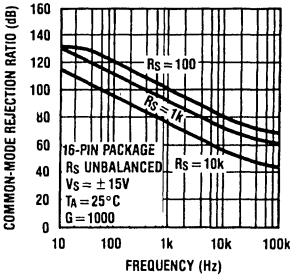
CMRR with Unbalanced Source Resistance



CMRR with Unbalanced Source Resistance



CMRR with Unbalanced Source Resistance



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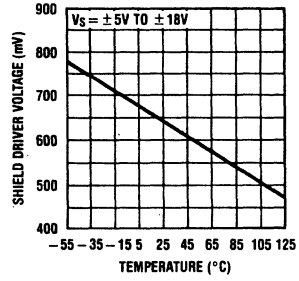
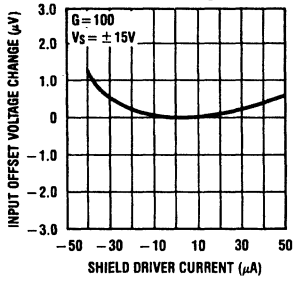
Typical Performance Characteristics (Continued)

Shield Driver Bias Voltage*

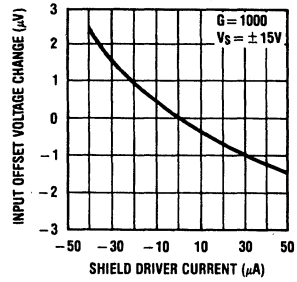


*Measured between either input and its respective shield driver.

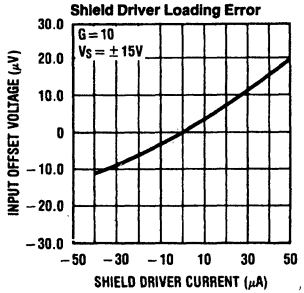
Shield Driver Loading Error



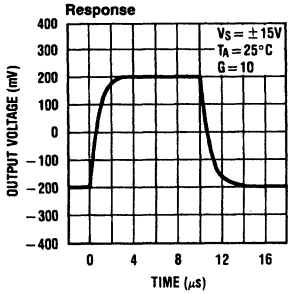
Shield Driver Loading Error



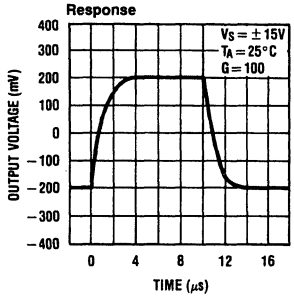
Shield Driver Loading Error



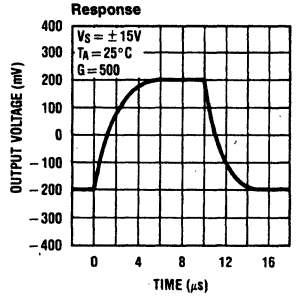
Small Signal Transient Response



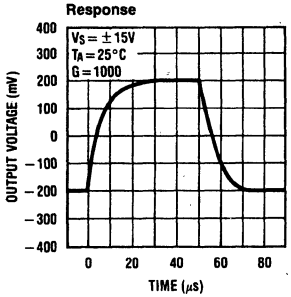
Small Signal Transient Response



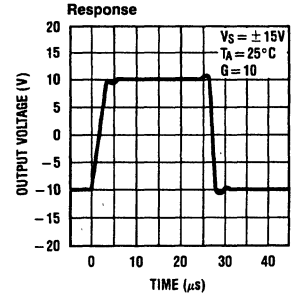
Small Signal Transient Response



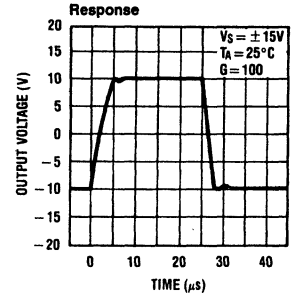
Small Signal Transient Response



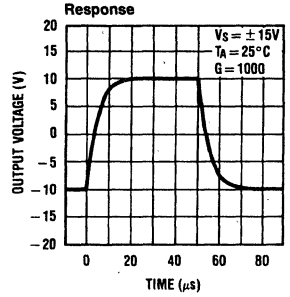
Large Signal Transient Response



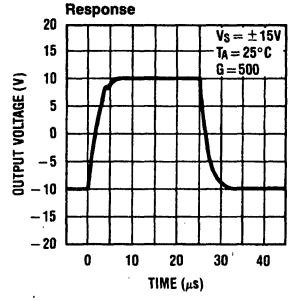
Large Signal Transient Response



Large Signal Transient Response



Large Signal Transient Response



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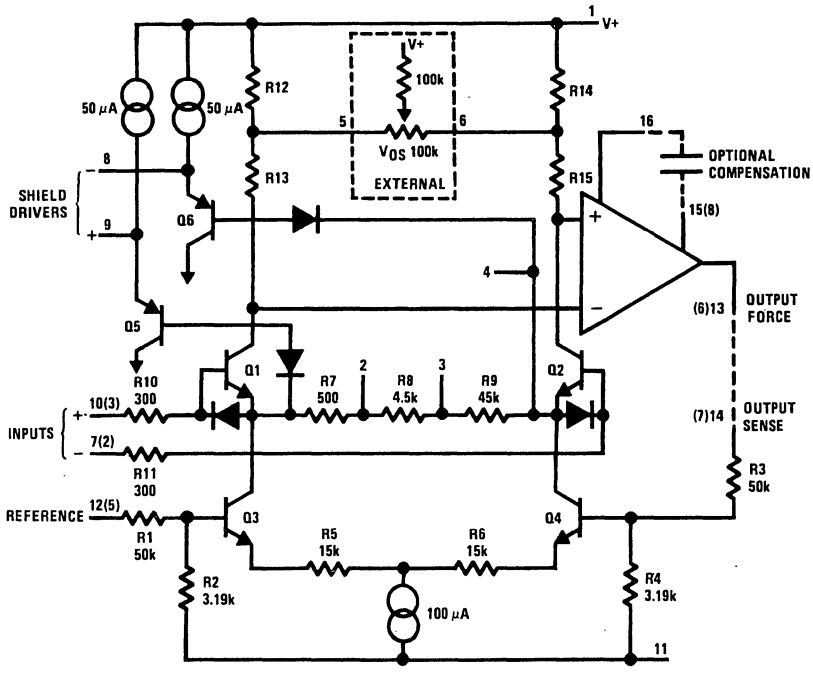
Simplified Schematic (pin numbers in parentheses are for 8-pin package)



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Theory of Operation

Referring to the Simplified Schematic, it can be seen that the input voltage is applied across the bases of Q1 and Q2 and appears between their emitters. If R_{E1-2} is the resistance across these emitters, a differential current equal to V_{IN}/R_{E1-2} flows from Q1's emitter to Q2's. The second stage amplifier shown maintains Q1 and Q2 at equal collector currents by negative feedback to Q4. The emitter currents of Q3 and Q4 must therefore be unbalanced by an amount equal to the current flow across R_{E1-2}. Defining $R_{E3-4} = R5 + R6$, the differential voltage across the emitters of Q4 to Q3 is equal to

$$\frac{V_{IN}}{R_{E\,1-2}} \times R_{E3-4}.$$

This voltage divided by the attenuation factor

$$\frac{R4}{R3+R4} = \frac{R2}{R1+R2}$$

is equal to the output-to-reference voltage. Hence, the overall gain is given by

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{R3+R4}{R4} \times \frac{R_{E3-4}}{R_{E1-2}}.$$

Application Hints

The LM163 was designed to be as simple to use as possible, but several general precautions must be taken. The differential inputs are directly coupled and need a return path to power supply common. Worst-case bias currents are only 10 nA for the LM363, so the return impedance can be as high as 100 MΩ. Ground drops between signal return and IC supply common should not be ignored. While the LM163 has excellent common-mode rejection, signals must remain within the proper common-mode range for this specification to apply. Operating common-mode range is guaranteed from −11V to +13V with ±15V supplies.

The high-gain (500 or 1000) versions have large gain-bandwidth products (15 MHz or 30 MHz) so board layout is fairly critical. The differential input leads should be kept away from output force and sense leads, especially at high impedances. Only 1 pF from output to positive input at 100 kΩ source impedance can cause oscillations. The gain adjust leads on the 16-pin package should be treated as inputs and kept away from the output wiring.

POWER SUPPLY

The LM163 may be powered from split supplies from ±5V to ±18V (or single-ended supplies from 10V to 36V). Positive supply current is typically 1.2 mA independent of supply voltage. The negative supply current is higher than the positive by the current drawn through the voltage dividers for the reference and sense inputs (typ 600 μA total). The LM163's excellent PSRR often makes regulated supplies unnecessary. Actually, supply voltage can be as low as 7V total but PSRR is severely degraded, so that well-regulated supplies are recommended below 10V total. Split supplies need not be balanced; output swing and input common-mode range will simply not be symmetrical with unbalanced supplies. For example, at +12V and −5V supplies, input common-mode range is typically +10.5V to −2V and output swing is +11V to −4V.

When using ultra-low offset versions, best results are obtained at ±15V supplies. For example, the LM363A-500's offset voltage is guaranteed within 30 μV at ±15V at 25°C. Running at ±5V results in a worst-case negative PSRR error of 10V (−15V to −5V) multiplied by 3.2×10^{-6} (110 dB) or 32 μV, doubling the worst-case offset. Positive PSRR results in another 10 μV worst-case change.

INPUTS

The LM163 input circuitry is depicted in the Simplified Schematic. The input stage is run relatively rich (50 μA) for low voltage noise and wide bandwidth; super-beta transistors and bias-current cancellation (not shown) keep bias currents low. Due to the bias-current cancellation circuitry, bias current may be either polarity at either input. While input current noise is high relative to bias current, it is not significant until source resistance approaches 100 kΩ.

Input common-mode range is typically from 3V above V^- to 1.5V below V^+, so that a large potential drop between the input signal and output reference can be accommodated. However, a return path for the input bias current must be provided; the differential input stage is not isolated from the supplies. Differential input swing in the linear region is equal to output swing divided by gain, and typically ranges from 1.3V at G = 10 to 13 mV at G = 1000.

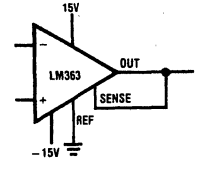
Clamp diodes are provided to prevent zener breakdown and resulting degradation of the input transistors. At large input overdrives these diodes conduct, greatly increasing input currents. This behavior is illustrated in the I_{IN} VS V_{IN} plot in the Typical Performance Characteristics. (The graph is not symmetrical because at large input currents a portion of the current into the device flows out the V^- terminal.)

The input protection resistors allow a full 10V differential input voltage without degradation even at G = 1000. At input voltages more than one diode drop below V^- or two diode drops above V^+ input, current increases rapidly. Diode clamps to the supplies, or external resistors to limit current to 20 mA, will prevent damage to the device.

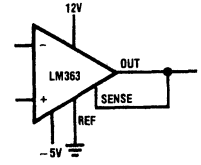
REFERENCE AND SENSE INPUTS

The equivalent circuit is shown in the schematic diagram. Limitations for correct operation are as follows. Maximum *differential* swing between reference and sense pins is typically ±15V (±10V guaranteed). If this limit is exceeded, the sense pin no longer controls the output, which pegs high or low. The *negative* common-mode limit is 1.5V below V^-. (This is permissible because R2 and R4 are returned to a node biased higher than V^-.) If large *positive* voltages are applied to the reference and sense pins, the common-mode range of the signal inputs begins to suffer as the drop across R13 and R16 increases. For example, at ±15V supplies, $V_{REF} = V_{SENSE} = 0V$, signal input range is typically −12V to + 13.5V. at $V_{REF} = V_{SENSE} = 15V$, signal input range drops to −11V to +13.5V. The reference and sense pin can be as much as 10V above V^+ as long as a restricted signal common-mode range (−10V min) can be tolerated.

For maximum bipolar output swing at ± 15V supplies, the reference pin should be returned to a voltage close to ground. At lower supply voltages, the reference pin need not be halfway between the supplies for maximum output swing. For example, at $V^+ = +12V$ and $V^- = -5V$, grounding the reference pin still allows a +11V to −4V swing. For single-supply systems, the reference pin can be tied to either supply if a single output polarity is all that is required. For a bipolar input and output, create a low impedance reference with an op amp and voltage divider or a regulator (e.g., LM336, LM385, LM317L). This forms the reference for all succeeding signal-processing stages. (Don't connect the reference terminal directly to a voltage divider; this degrades gain error.) See *Figure 1*.



a. Usual configuration maximizes bipolar output swing.



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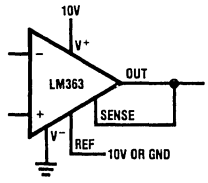
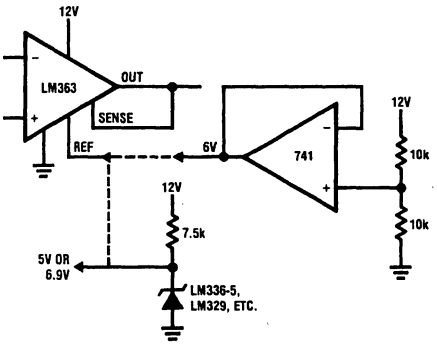
b. Unequal supplies, output ground referred. Full output swing preserved referred to supplies.

FIGURE 1. Reference Connections

Application Hints (Continued)



c. Single Supply, Unipolar Output



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d. Single Supply, Bipolar Output

FIGURE 1. Reference Connections (Continued)

OUTPUTS

The LM163's output can typically swing within 1V of the supplies at light loads. While specified to drive a 2 kΩ load to ±10V, current limit is typically 15 mA at room temperature. The output can stably drive capacitive loads up to 400 pF. For higher load capacitance, the amplifier may be overcompensated. The output may be continuously shorted to ground without damaging the device.

OFFSET VOLTAGE

The LM163's offset voltage is internally trimmed to a very low value. Note that data sheet values are given at $T_j = 25°C$, $V_{CM} = 0V$ and $V^+ = V^- = 15V$. For other conditions, warm-up drift, temperature drift, common-mode rejection and power supply rejection must be taken into account. Warm-up drift, due to chip and package thermal gradients, is an effect separate from temperature drift. Typical warm-up drift is tabulated in the Electrical Characteristics; settling time is approximately 5 minutes in still air. At load currents up to 5 mA, thermal feedback effects are negligible ($\Delta V_{OS} \leq 2\mu V$ at $G = 1000$).

Care must be taken in measuring the extremely low offset voltages of the high gain amplifiers. Input leads must be held isothermal to eliminate thermocouple effects. Oscillations, due to either heavy capacitive loading or stray capacitance from input to output, can cause erroneous readings. In either case, overcompensation will help. High frequency noise fed into the inputs may be rectified internally, and produce an offset shift. A simple low-pass RC filter will usually cure this problem (*Figure 2*). Use film type resistors for their low thermal EMF. In highly noisy environments, LC filters can be substituted for increased RF attenuation.

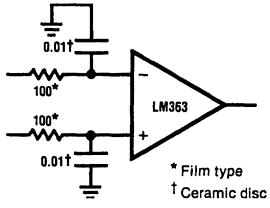

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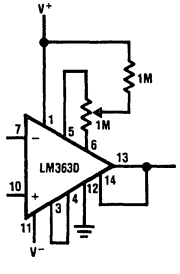
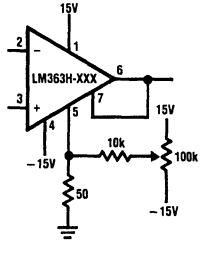
FIGURE 2. Low Pass Filter Prevents RF Rectification

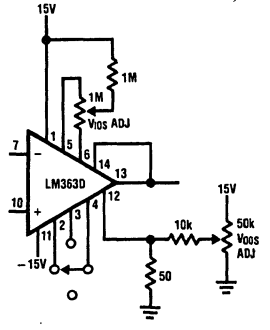
Instrumentation amplifiers have both an input offset voltage (V_{IOS}) and an output offset voltage (V_{OOS}). The total input-referred offset voltage (V_{OSRTI}) is related to the instrumentation amplifier gain (G) as follows: $V_{OSRTI} = V_{IOS} + V_{OOS}/G$. The offset voltage given in the LM163 specifications is the total input-referred offset. As long as only one gain is used, offset voltage can be nulled at either input or output as shown in *Figures 3a* and *3b*. When the 16-pin device is used at multiple gain settings, both V_{IOS} and V_{OOS} should be nulled to get minimum offset at all gains, as shown in *Figure 3c*. The correct procedure is to trim V_{OOS} for zero output at $G = 10$, then trim V_{IOS} at $G = 1000$.



a. Input Offset Adj. for 16-Pin Package



b. Output Offset Adj. for 8-Pin Package



c. Input and Output Offset Adjustment for 16-Pin Package

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FIGURE 3. Offset Voltage Trimming

Application Hints (Continued)

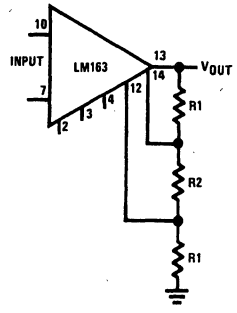
Because the LM163's offset voltage is so low to begin with, offset nulling has a negligible effect on offset temperature drift. For example, zeroing a 100 μV offset, assuming external resistor TC of 200 ppm/°C and worst-case internal resistor TC, results in an additional drift component of 0.08 μV/°C. For this reason, drift specifications are guaranteed, with or without external offset nulling.

GAIN ADJUSTMENT

Gain may be increased by adding an external voltage divider between output force and sense and reference; the preferred connection is shown in *Figure 4*. Since both the sense and reference pins look like 50 kΩ (±20 kΩ) to V−, impedances presented to both pins must be equal to avoid offset error. For example, a 100Ω imbalance can create a worst-case output offset of 50 mV, creating an input-referred error of 5 mV at G = 10 or 50 μV at G = 1000.

Increasing gain this way increases output offset error. An LM363H-100 may have an output offset of 5 mV, resulting in input referred offset component of 50 μV. Raising the gain to 200 yields a 10 mV error at the output and changes input referred error by an additional 50 μV.

External resistors connected to the reference and sense pins can only *increase* the gain. If ultra-low output impedance is not critical, the technique in *Figure 5* can be used to trim the gain to nominal value. Alternatively, the V_{OS} adjustment terminals on the 16-pin package may be used to trim the gain (*Figure 10b*).



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R1 and R2 should be as low as possible to avoid errors due to 50 kΩ input impedance of reference and sense pins. Total resistance (R2+2R1) should be above 4 kΩ, however, to prevent excessive load on the LM163 output. The exact formula for calculating gain (G) is:

$$G = G_O\left(1 + \frac{2R1}{R2} + \frac{R1}{50k}\right)$$

G_O = preset gain

The last term may be ignored in applications where gain accuracy is not critical. The table below gives suggested values for R1 and R2 along with the calculated error due to "closest value" standard 1% resistors. Total gain error tolerance includes contributions from LM163 G_O error and resistor tolerance (±1%) and works out to approximately 2.5% in every case.

Gain Increase	1.5	2	2.5	3	4	5	6	7	8	9	10
R1	1.21k	1.21k	2k	2k	1.78k	2k	2.49k	2.94k	3.48k	3.92k	4.42k
R2	5k	2.49k	2.74k	2.05k	1.21k	1k	1k	1k	1k	1k	1k
Error (typ)	+0.6%	−0.2%	0	−0.3%	−0.6%	+0.8%	+0.5%	−0.9%	+0.4%	−0.9%	−0.7%

FIGURE 4. Increasing Gain

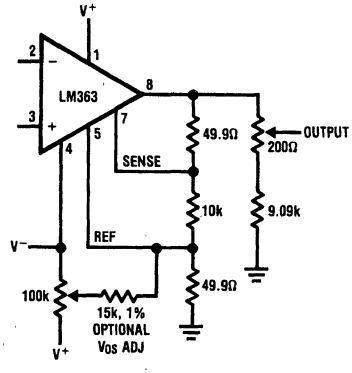

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FIGURE 5. Adjusting Gain (8-Pin Package)

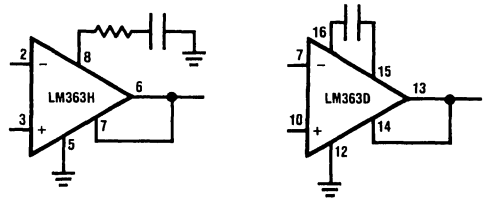
Application Hints (Continued)

COMPENSATION AND OUTPUT CLAMPING

The LM163 is internally compensated for unity feedback from output to sense. Increasing gain with external dividers will decrease the bandwidth and increase stability margin. Without external compensation, the amplifier can stably drive capacitive loads up to 400 pF. When used as an op amp (sense and reference pins grounded, feedback to inverting input), the LM163 is stable for gains of 100 or more. For greater stability, the device may be over-compensated as in *Figure 6*. Tables I and II depict suggested compensation components along with the resulting changes in large and small signal bandwidth for the 8-pin and 16-pin packages, respectively.

Note that the RC network from pin 8 of the 8-pin device to ground has a large effect on power bandwidth, especially at low gains. The Miller capacitance utilized for the 16-pin device permits higher slew rate and larger load capacitance for the same bandwidth, and is preferred when bandwidth must be greatly reduced (e.g., to reduce output noise).

Heavy Miller overcompensation on the 16-pin package can degrade AC PSRR. A large capacitor between pins 15 and 16 couples transients on the positive supply to the output buffer. Since the amplifier bandwidth is severely rolled off it cannot keep the output at the correct state at moderate frequencies. Hence, for good PSRR, either keep the Miller capacitance under 1000 pF or use the pin 15-to-ground compensation.



a. 8-Pin Package b. 16-Pin Package

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FIGURE 6. Overcompensation

TABLE I. Overcompensation on 8-Pin Package

Gain	Compensation Network (Pin 8 to Ground)†	Small Signal 3 dB Bandwidth (kHz)	Power Bandwidth (±10V Swing) (Hz)	Maximum Capacitive Load (pF)
500	—	125	100k	400
	100 pF, 15k	95	15k	600
	1000 pF, 5k	45	1.8k	800
	0.01 μF,500Ω	10	200	1000*
	0.1 μF	1	20	1000*
100	—	240	100k	400
	100 pF, 15k	170	15k	900
	1000 pF, 5k	80	1.8k	1200
	0.01 μF, 500Ω	20	200	1600*
	0.1 μF	2	20	2000*
10	—	240	100k	400
	100 pF, 15k	170	15k	900
	1000 pF, 5k	90	1.8k	1200
	0.01 μF, 500Ω	20	200	1600*
	0.1 μF	2	20	2000*

*Also stable for $C_L \geq 0.05\ \mu F$ †Pin 15 to round on 16-pin package

TABLE II. Overcompensation on 16-Pin Package

Gain	Compensation Capacitor (Pin 15 to 16)	Small Signal 3 dB Bandwidth (Hz)	Power Bandwidth (±10V Swing) (Hz)	Maximum Capacitive Load (pF)
1000	0	45k	45k	1000*
	10 pF	16k	16k	2000*
	100 pF	2.5k	2.5k	2500*
	1000 pF	250	250	3000*
	0.01 μF	25	25	3000*
100	0	140k	100k	900
	10 pF	50k	50k	1600
	100 pF	7.5k	7.5k	2000*
	1000 pF	750	750	2000*
	0.01 μF	76	75	2000*
10	0	180k	90k	600
	10 pF	60k	50k	1100
	100 pF	9k	9k	1600
	1000 pF	900	900	2000*
	0.01 μF	90	90	2000*

*Also stable for $C_L \geq 0.05\ \mu F$

Application Hints (Continued)

Because the LM163's output voltage is approximately one diode drop below the voltage at pin 15 (pin 8 for the 8-pin device), this point may be used to limit output swing as seen in *Figure 7a*. Current available from this pin is only 50 μA, so that zeners must have a sharp breakdown to clamp accurately. Alternatively, a diode tied to a voltage source could be used as in *Figure 7b*.

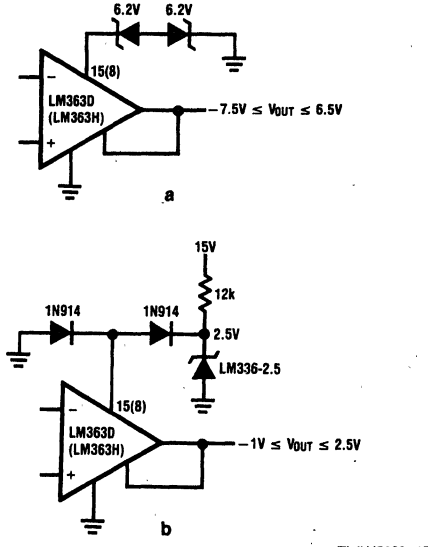

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FIGURE 7. Output Clamp

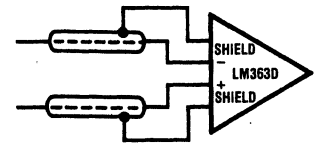
SHIELD DRIVERS

When differential signals are sent through long cables, three problems occur. First, noise, both common-mode and differential, is picked up. Second, signal bandwidth is reduced by the RC low-pass filter formed by the source impedance and the cable capacitance. Finally, when these RC time constants are not identical (unbalanced source impedance and/or unbalanced capacitance), AC common-mode rejection is degraded, amplifying both induced noise and "ground" noise. Either filtering at the amplifier inputs or slowing down the amplifier by overcompensating will indeed reduce the noise, but the price is slower response. The LM163's dual shield drivers can actually increase bandwidth while reducing noise.

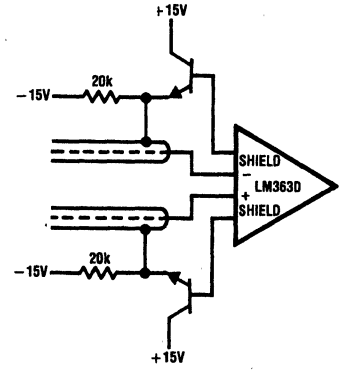
The way this is done is by bootstrapping out shield capacitance. The shield drivers follow the input signal. Since both sides of the shield capacitance swing the same amount, it is effectively out of the circuit at frequencies of interest. Hence, the input signal is not rolled off and AC CMRR is not degraded (*Figure 8*). The LM163's shield drivers can handle capacitances (shield to center conductor) as high as 1000 pF with source resistances up to 100 kΩ.

For best results, identical shielded cables should be used for both signal inputs, although small mismatches in shield driver to ground capacitance (≤500 pF) do not cause problems. At certain low values of cable capacitance (50 pF–200 pF), high frequency oscillations can occur at high source resistance (≥ 10 kΩ). This is alleviated by adding 50 pF to ground at both shield driver outputs. Do not use only one shield driver for a single-ended signal as oscillations can result; shield driver to input capacitance must be roughly balanced (±30%). To further reduce noise pickup, the shielded signal lines may be enclosed together in a grounded shield. If a large amount of RF noise is the problem, the only sure cure is a filter capacitor at both inputs; otherwise the RFI may be internally rectified, producing an offset.

DC loading on the shield drivers should be minimized. The drivers can only source approximately 40 μA; above this value the input stage bias voltages change, degrading V_{OS} and CMRR. While the shield drivers can sink several mA, V_{OS} may degrade severely at loads above 100 μA (see Shield Driver Loading Error curve in Typical Performance Characteristics). Because the shield drivers are one diode drop above the input levels, unbalanced leakage paths from shield to input can produce an input offset at high source impedances. Buffering with emitter-followers (*Figure 8b*) reduces this leakage current by reducing the voltage differential and eliminates any loading on the amplifier.



a. Standard Configuration



b. NPN Followers to Reduce Offsets

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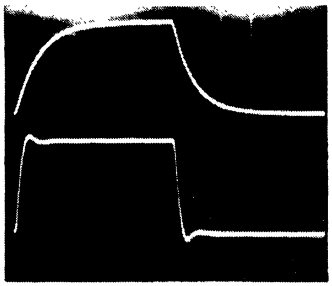
FIGURE 8. Driving Shielded Cables

MISCELLANEOUS TRIMMING

The V_{OS} adjust and shield driver pins available on the 16-pin package may be used to trim the other parameters besides offset voltage, as illustrated in *Figure 10*. The bias-current trim relies on the fact that the voltage on the shield driver and gain setting pins is one diode drop respectively above and below the input voltage. Input bias current can be held to within 100 pA over the entire common-mode range, and input offset current always stays under 30 pA. The CMRR trims use the shield driver pins to drive the V_{OS} adjust pins, thus maintaining the LM163's ultra-high input impedance.

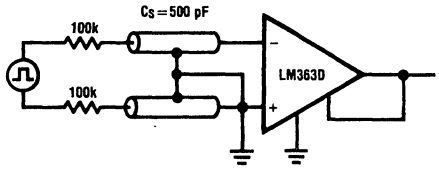
Application Hints (Continued)

If power supply rejection is critical, frequently only the negative PSRR need be adjusted, since the positive PSRR is more tightly specified. Any or all of the trim schemes of *Figure 10* can be combined as desired. As long as the center tap of the 100k trimpot is returned to a voltage 200 mV below V^+, the trim schemes shown will not greatly affect V_{OS}. Both the gain and DC CMRR trims can degrade positive PSRR; the positive PSRR can then be nulled out if desired. The correct order of trimming from first to last is bias current, gain, CMRR, negative PSRR, positive PSRR and V_{OS}.

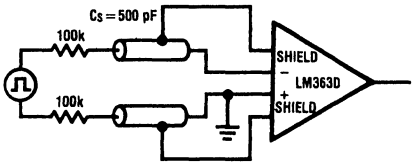


TL/H/5609–17

Top Trace: Cable Shield Grounded

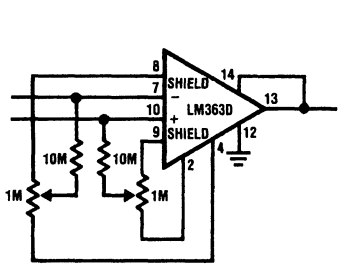


Bottom Trace: Cable Shield Bootstrapped

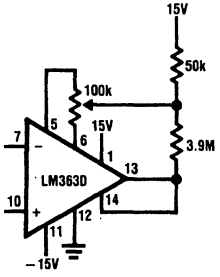


TL/H/5609–18

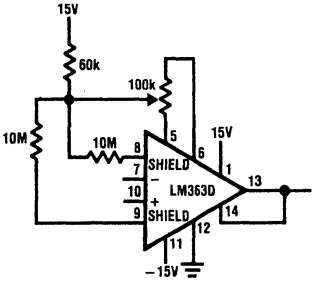
FIGURE 9. Improved Response using Shield Drivers



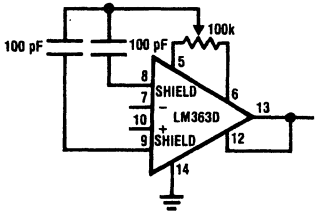
a. Bias Current



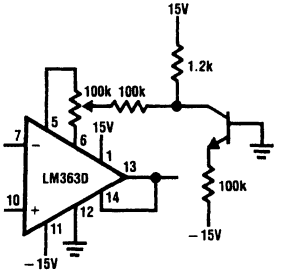
b. Gain



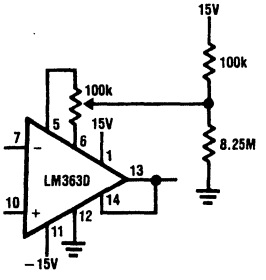
c. DC CMRR



d. AC CMRR



e. Negative PSRR



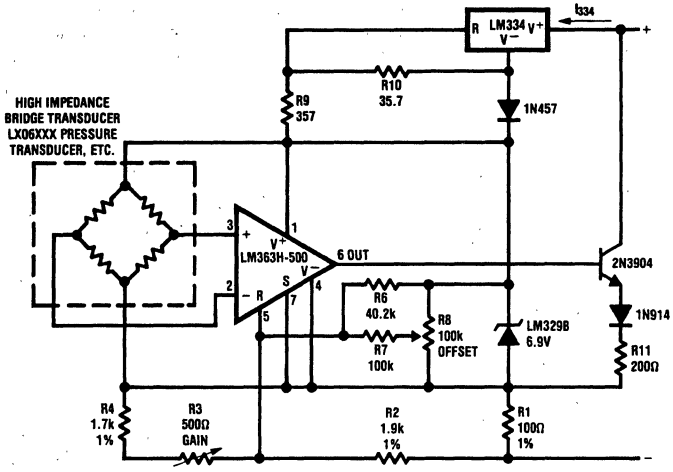
f. Positive PSRR

TL/H/5609–19

FIGURE 10. Other Trims for 16-Pin Package

Typical Applications

4 mA-20 mA Two Wire Current Transmitter



TL/H/5609–20

The LM329 reference provides excellent line regulation and gain stability. When bridge is balanced (I_{OUT} = 4 mA), there's no drop across R3 and R4, so that gain and offset adjustments are non-interactive. The LM334 configured as a zero-TC current source supplies quiescent current to circuit. R11 provides current limiting.

Design Equations

$$I_{OS} = (I_{R6} + I_{R7})\left(1 + \frac{R2}{R1}\right) = 4\text{ mA}$$

$$\text{Gain} = \frac{\Delta I_{OUT}}{\Delta V_{IN}} \cong \frac{A_V}{R1} \times \frac{R2+R3+R4}{R3+R4} \cong \frac{10\text{ mA}}{\text{mV}}$$

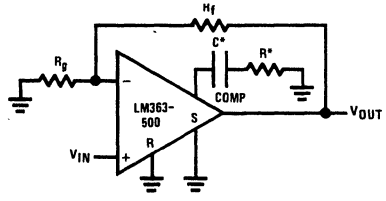
when A_V = LM363 voltage gain

$$\text{Pick } I_{334} = \frac{0.68V}{R9} + \frac{68\text{ mV}}{R10} \cong 3.8\text{ mA}$$

$$I_{MAX} = I_{334} + \frac{V_Z - 2.4V}{R11} = 26\text{ mA}$$

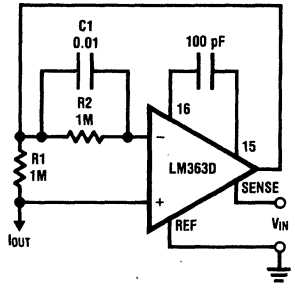
$$I_{BRIDGE(MAX)} \cong I_{334} - I_{363} - I_Z \cong 1.5\text{mA}$$

Precision Op Amp



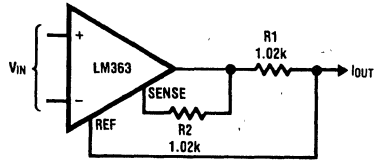
Select for optimum square wave response. Omit for closed loop gains above 100. Not required for instrumentation amplifier configuration.

Precision Current Source (Low Output Current)



TL/H/5609–21

Precision Voltage to Current Converter (Low Input Voltage)



TL/H/5609–22

$$R1 = R2$$

$$\text{Req} = R1 \| 50\text{ k}\Omega$$

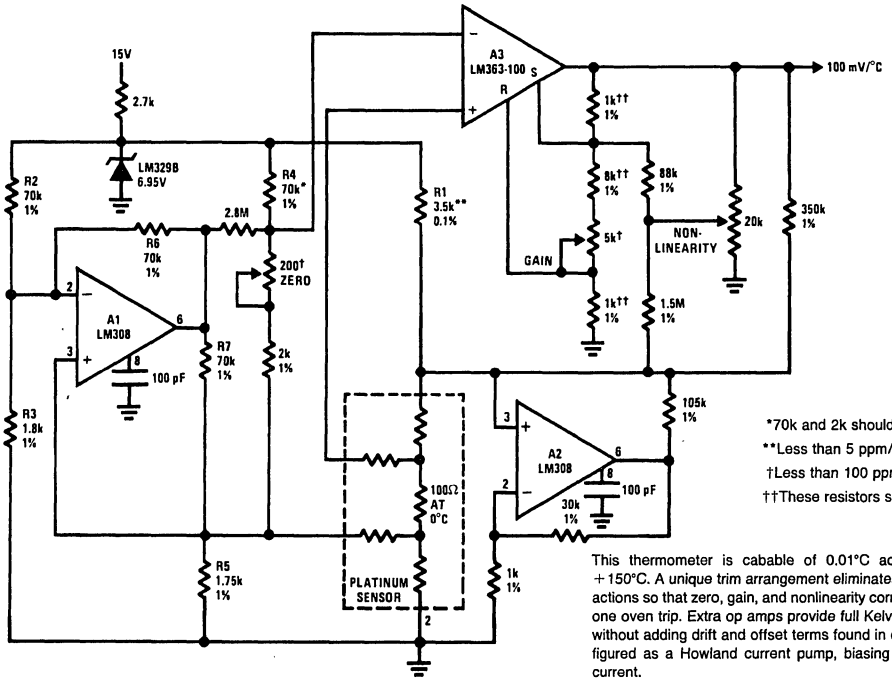
$$I_{OUT} = \frac{G\,V_{IN}}{\text{Req}} = \frac{G\,V_{IN}}{1\text{ k}\Omega}$$

$$R1 = R2$$

$$I_{OUT} = \frac{V_{IN}}{GR1}$$

Typical Applications (Continued)

Curvature Corrected Platinum RTD Thermometer



TL/H/5609-23

*70k and 2k should track to 5 ppm/°C

**Less than 5 ppm/°C drift

†Less than 100 ppm/°C drift

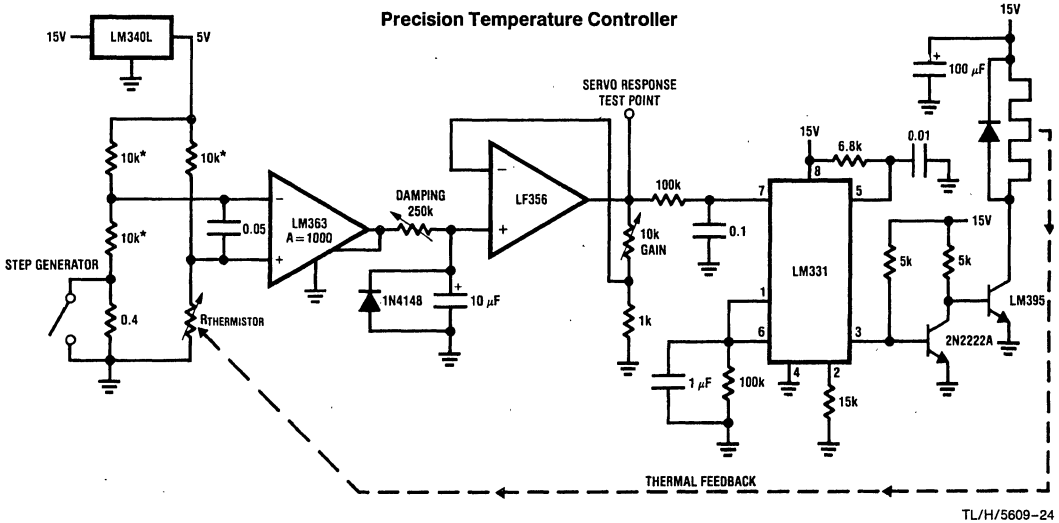
††These resistors should track to 20 ppm/°C

This thermometer is cabable of 0.01°C accuracy over −50°C to +150°C. A unique trim arrangement eliminates cumbersome trim interactions so that zero, gain, and nonlinearity correction can be trimmed in one oven trip. Extra op amps provide full Kelvin sensing on the sensor without adding drift and offset terms found in other designs. A2 is configured as a Howland current pump, biasing the sensor with a fixed current.

Resistors R2, R3, R4 and R5 from a bridge driven into balance by A1. In balance, both inputs of A1 are at the same voltage. Since R6 = R7, A1 draws equal currents from both legs of the bridge. Any loading of the R4/R5 leg by the sensor would unbalance the bridge; therefore, both bridge taps are given to the sensor open circuit voltage and no current is drawn.

For details, request Application Note AN-304.

Precision Temperature Controller



TL/H/5609-24

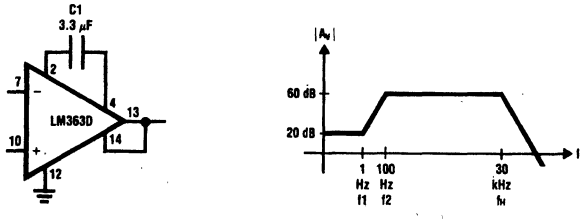
*Ultronix 105A wirewound

Thermistor = Yellow Springs #44032

Setpoint stability = 2.5X10⁻⁴°C/Hr

Typical Applications (Continued)

Low Frequency Rolloff (AC Coupling)

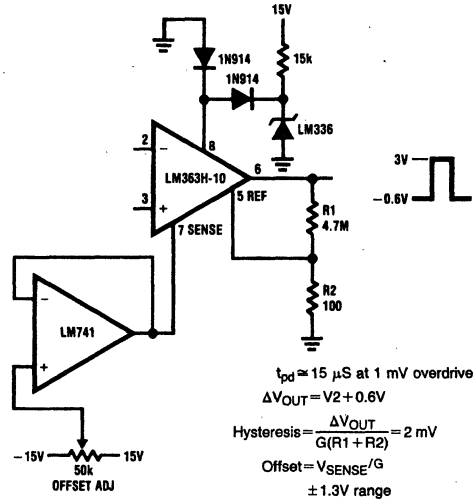


$$f1 = \frac{1}{2\pi C1(50\ k\Omega)} = 1\ Hz$$

f2 = 100 f1 = 100Hz
Reduced DC voltage gain attenuates offset error and 1/f noise by a factor of 100.

TL/H/5609-25

Precision Comparator with Balanced Inputs and Variable Offset



$t_{pd} \simeq 15\ \mu S$ at 1 mV overdrive

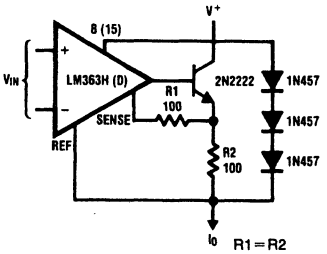
$\Delta V_{OUT} = V2 + 0.6V$

$$\text{Hysteresis} = \frac{\Delta V_{OUT}}{G(R1 + R2)} = 2\ mV$$

$\text{Offset} = V_{SENSE}/G$

±1.3V range

Boosted Current Source with Limiting



$R1 = R2$

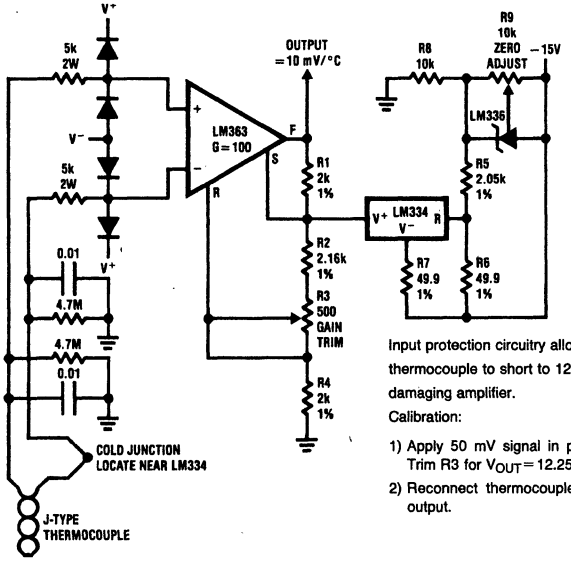
$$I_O = \frac{G\ V_{IN}}{R2}$$

$$I_{MAX} = \frac{V_{BE}}{R2}$$

$\simeq 60$ mA

TL/H/5609-26

Thermocouple Amplifier with Cold Junction Compensation



Input protection circuitry allows thermocouple to short to 120 V_{AC} without damaging amplifier.

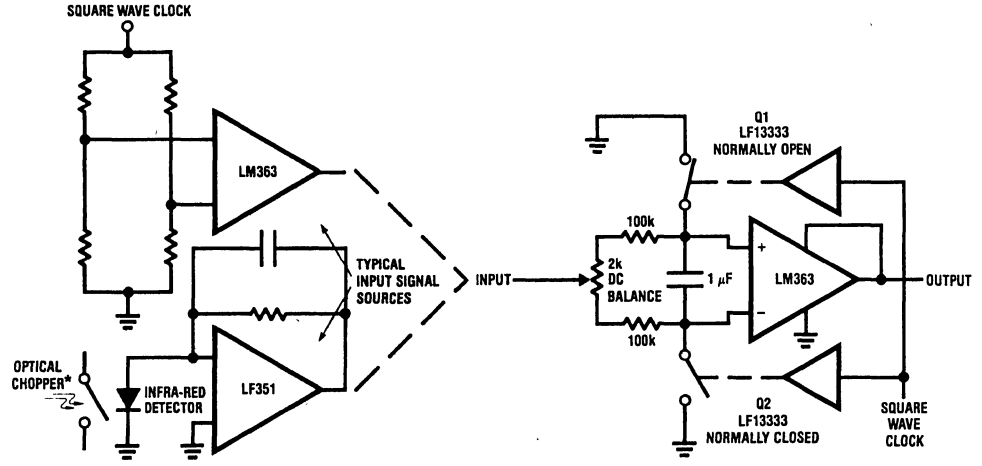
Calibration:

1) Apply 50 mV signal in place of thermocouple. Trim R3 for $V_{OUT} = 12.25V$.
2) Reconnect thermocouple. Trim R9 for correct output.

TL/H/5609-27

Typical Applications (Continued)

Synchronous Demodulator



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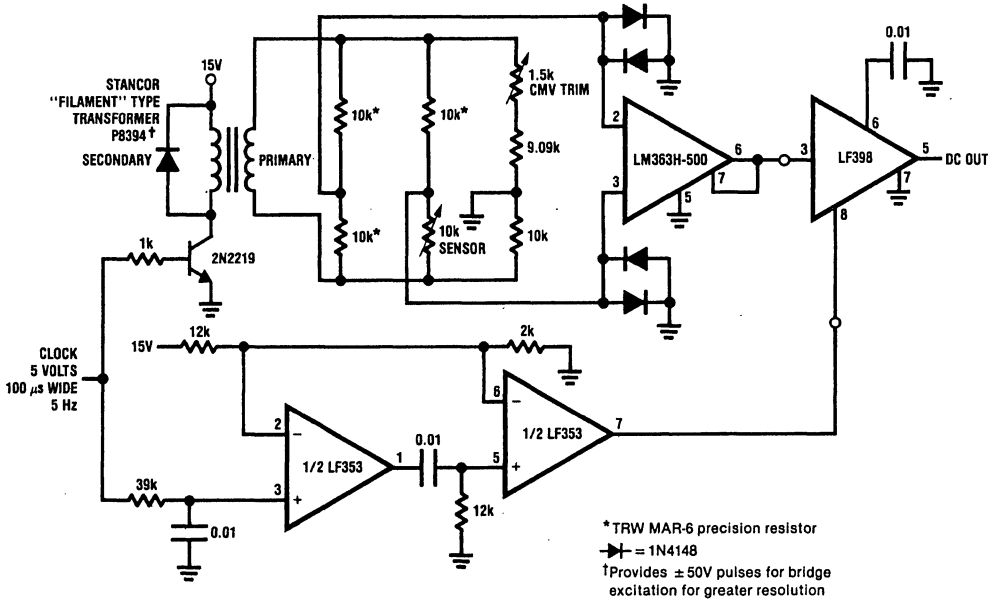
*Use square wave drive produced by optical chopper to run LF13333 switch inputs.

Pulsed Bridge Driver/Amplifier



*TRW MAR-6 precision resistor

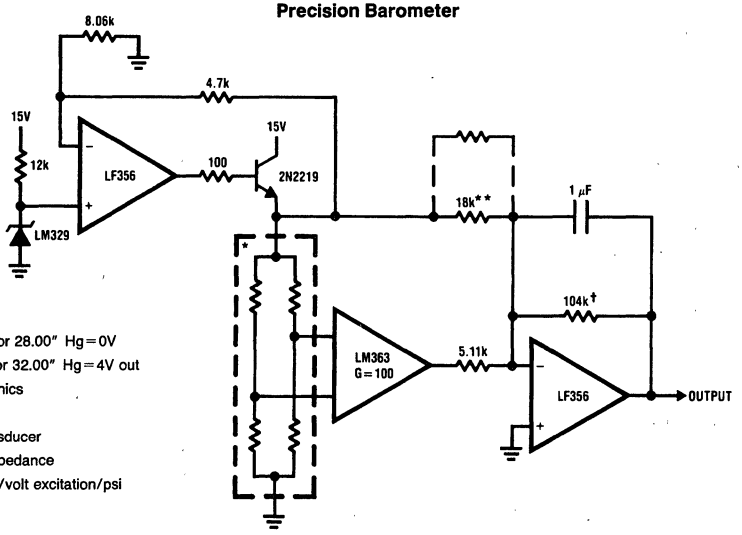
= 1N4148

†Provides ± 50V pulses for bridge excitation for greater resolution without overdissipation

TL/H/5609–29

Typical Applications (Continued)

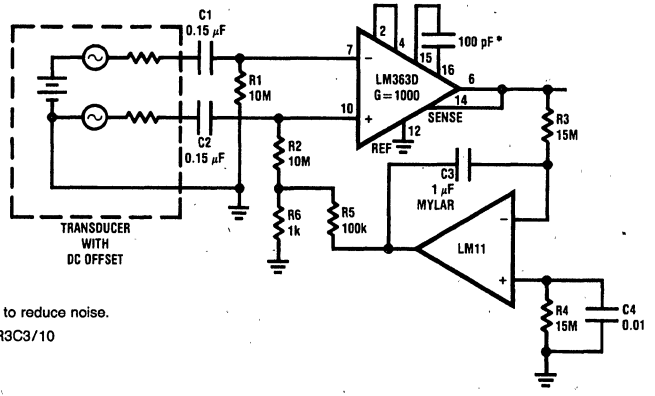
Precision Barometer



**Parallel trim for 28.00" Hg=0V
†Parallel trim for 32.00" Hg=4V out
*B.L.H. Electronics
#DHF-444114
Pressure Transducer
350Ω input impedance
Output=1 mV/volt excitation/psi

TL/H/5609–30

Removing Large DC Offsets



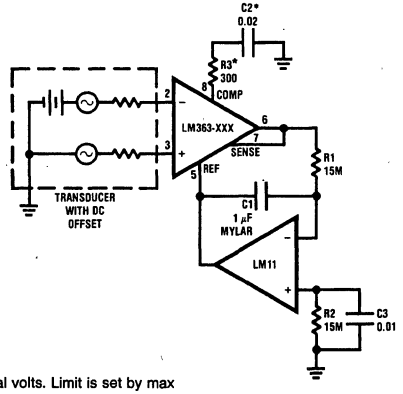
*Optional bandlimiting to reduce noise.
Pick R1C1=R2C2=R3C3/10

$$=\frac{1}{2\pi f_l}$$

f_l=0.1 Hz for values shown. Integrator nulls out offset error to LM363 bias currents flowing into R1 and R2.

TL/H/5609–31

Removing Small DC Offsets



*Optional bandlimiting to reduce noise.
Low frequency break

$$\text{frequency } f_l=\frac{1}{2\pi R1C1}=0.01 \text{ Hz}$$

Accommodates out referred offset of several volts. Limit is set by max differential between reference and sense terminals.

TL/H/5609–32

National Semiconductor

PRELIMINARY

LM833 Dual Audio Operational Amplifier

General Description

The LM833 and LM833A are dual general purpose operational amplifiers designed with particular emphasis on performance in audio systems.

These dual amplifier ICs utilize new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833 and LM833A are internally compensated for all closed loop gains and are therefore optimized for all preamp and high level stages in PCM and HiFi systems.

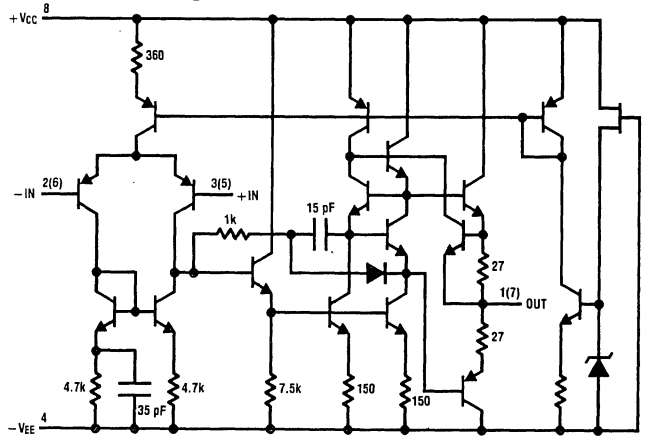
The LM833 and LM833A are pin for pin compatible with industry standard dual operational amplifiers.

The LM833A guarantees low noise for noise critical applications by 100% noise testing.

Features

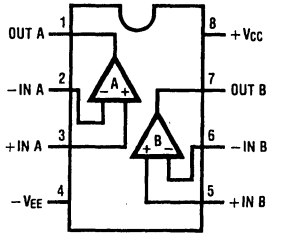
■ Wide dynamic range	> 140 dB
■ Low input noise voltage	4.5 nV/√Hz
■ High slew rate	7 V/μs (typ) 5 V/μs (min)
■ High gain bandwidth product	15 MHz (typ) 10 MHz (min)
■ Wide power bandwidth	120 kHz
■ Low distortion	0.002%
■ Low offset voltage	0.3 mV
■ Large phase margin	60°

Schematic Diagram (1/2 LM833)



TL/H/5218-1

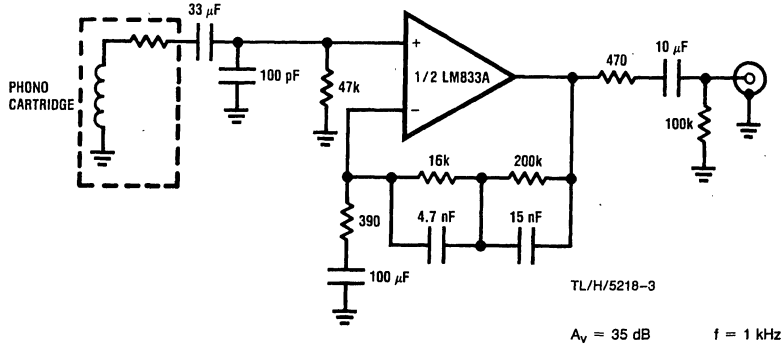
Connection Diagram



TL/H/5218-2

Order Number LM833N
See NS Package N08E

Typical Application RIAA Preamp



TL/H/5218-3

A_V = 35 dB f = 1 kHz
E_n = 0.33 μV A Weighted
S/N = 90 dB A Weighted, V_{IN} = 10 mV @ f = 1 kHz

Absolute Maximum Ratings

Supply Voltage	V_{CC}/V_{EE}	±18V	Power Dissipation (Note 2)	P_D	500 mW
Differential Input Voltage (Note 1)	V_{ID}	±30V	Operating Temperature Range	T_{OPR}	−40 ~ 85°C
Input Voltage Range (Note 1)	V_{IC}	±15V	Storage Temperature Range	T_{STG}	−60 ~ 150°C

DC Electrical Characteristics (T_A = 25°C, V_S = ±15V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10Ω		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Voltage Gain	R_L = 2 kΩ, V_O = ±10V	90	110		dB
V_{OM}	Output Voltage Swing	R_L = 10 kΩ R_L = 2 kΩ	±12 ±10	±13.5 ±13.4		V V
V_{CM}	Input Common-Mode Range		±12	±14.0		V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 15~5V, −15~−5V	80	100		dB
I_Q	Supply Current	V_O = 0V, Both Amps		5	8	mA

AC Electrical Characteristics (T_A = 25°C, V_S = ±15V, R_L = 2 kΩ)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	R_L = 2 kΩ	5	7		V/μs
GBWP	Gain Bandwidth Product	f = 100 kHz	10	15		MHz
e_{n1}	LM833A Equivalent Input	RIAA, R_S = 470Ω		0.5	0.8	μV
	Noise Voltage (Note 3)					

Design Electrical Characteristics (T_A = 25°C, V_S = ±15V)

The following parameters are not tested or guaranteed.

Symbol	Parameter	Conditions	Typ	Units
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		2	μV/°C
THD	Distortion	R_L = 2 kΩ, f = 20~20 kHz V_{OUT} = 3 Vrms, A_V = 1	0.002	%
e_n 2	Input Referred Noise Voltage 2	R_S = 100Ω, JISA	0.5	μV
e_n 3	Input Referred Noise Voltage 3	R_S = 100Ω, f = 1 kHz	4.5	nV/√Hz
i_n	Input Referred Noise Current	f = 1 kHz	0.7	pA/√Hz
PBW	Power Bandwidth	V_O = 27 V_{pp}, R_L = 2 kΩ, THD ≤ 1%	120	kHz
f_U	Unity Gain Frequency	Open Loop	9	MHz
ϕ_M	Phase Margin	Open Loop	60	deg
	Input Referred Cross Talk	f = 20~20 kHz	−120	dB

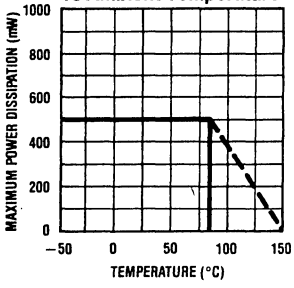
Note 1: If supply voltage is less than 15V, it is equal to supply voltage.

Note 2: This is the permissible value at $T_A \leq 85°C$.

Note 3: Only the LM833A is noise tested and guaranteed.
See "Noise Measurement Circuit" for test conditions.

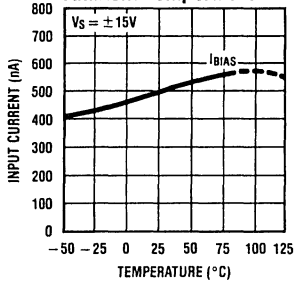
Typical Performance Characteristics

Maximum Power Dissipation vs Ambient Temperature



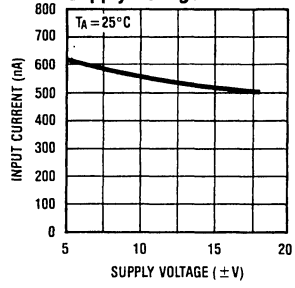
TL/H/5218–4

Input Bias Current vs Ambient Temperature



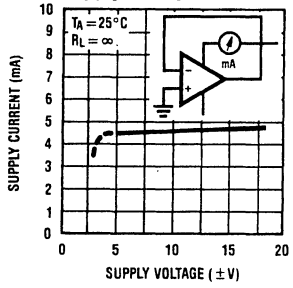
TL/H/5218–5

Input Bias Current vs Supply Voltage



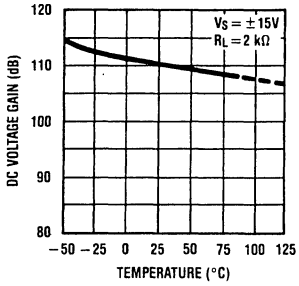
TL/H/5218–6

Supply Current vs Supply Voltage



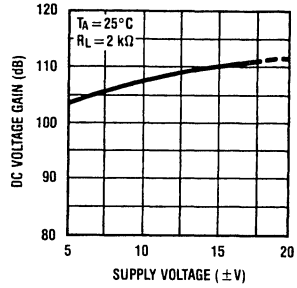
TL/H/5218–7

DC Voltage Gain vs Ambient Temperature



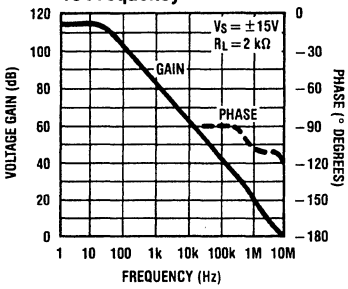
TL/H/5218–8

DC Voltage Gain vs Supply Voltage



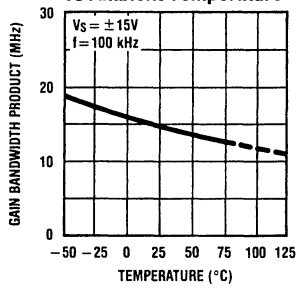
TL/H/5218–9

Voltage Gain & Phase vs Frequency



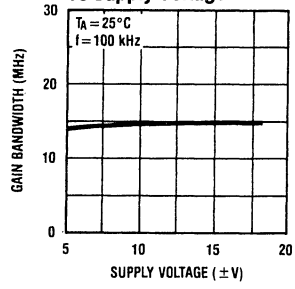
TL/H/5218–10

Gain Bandwidth Product vs Ambient Temperature



TL/H/5218–11

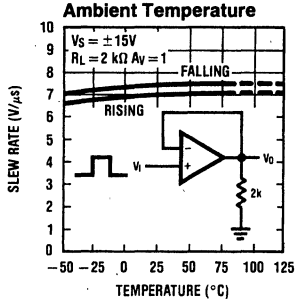
Gain Bandwidth vs Supply Voltage



TL/H/5218–12

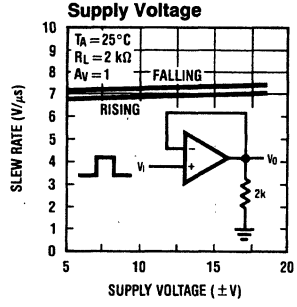
Typical Performance Characteristics (Continued)

Slew Rate vs Ambient Temperature



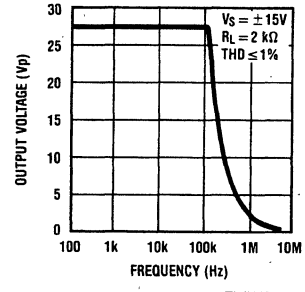
TL/H/5218–13

Slew Rate vs Supply Voltage



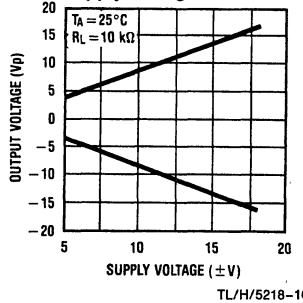
TL/H/5218–14

Power Bandwidth



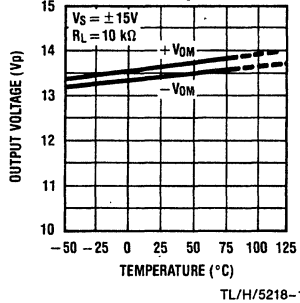
TL/H/5218–15

Maximum Output Voltage vs Supply Voltage



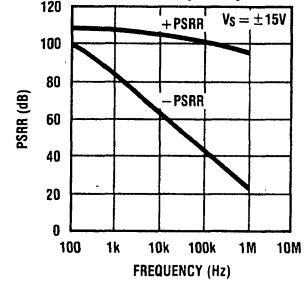
TL/H/5218–16

Maximum Output Voltage vs Ambient Temperature



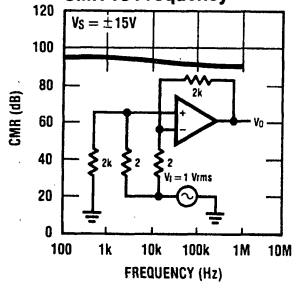
TL/H/5218–17

PSRR vs Frequency



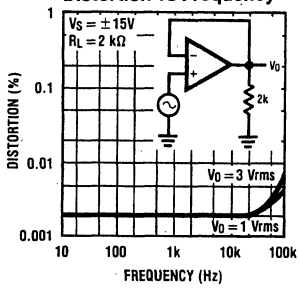
TL/H/5218–18

CMR vs Frequency



TL/H/5218–19

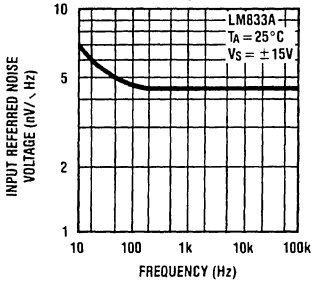
Distortion vs Frequency



TL/H/5218–20

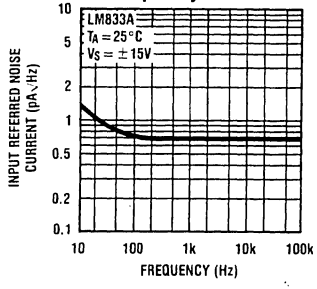
Typical Performance Characteristics (Continued)

Spot Noise Voltage vs Frequency



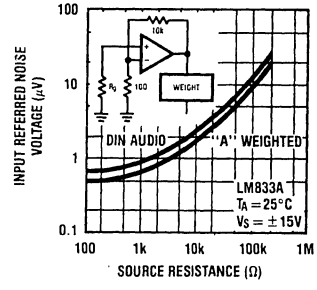
TL/H/5218–21

Spot Noise Current vs Frequency



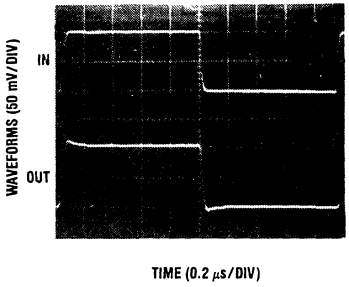
TL/H/5218–22

Input Referred Noise Voltage vs Source Resistance



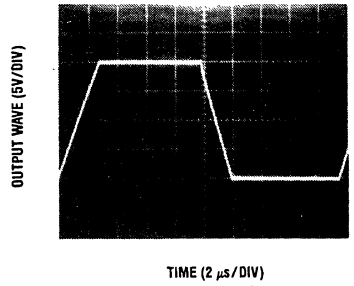
TL/H/5218–23

Noninverting Amp



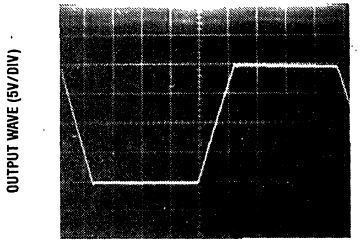
TL/H/5218–24

Noninverting Amp



TL/H/5218–25

Inverting Amp



TL/H/5218–26

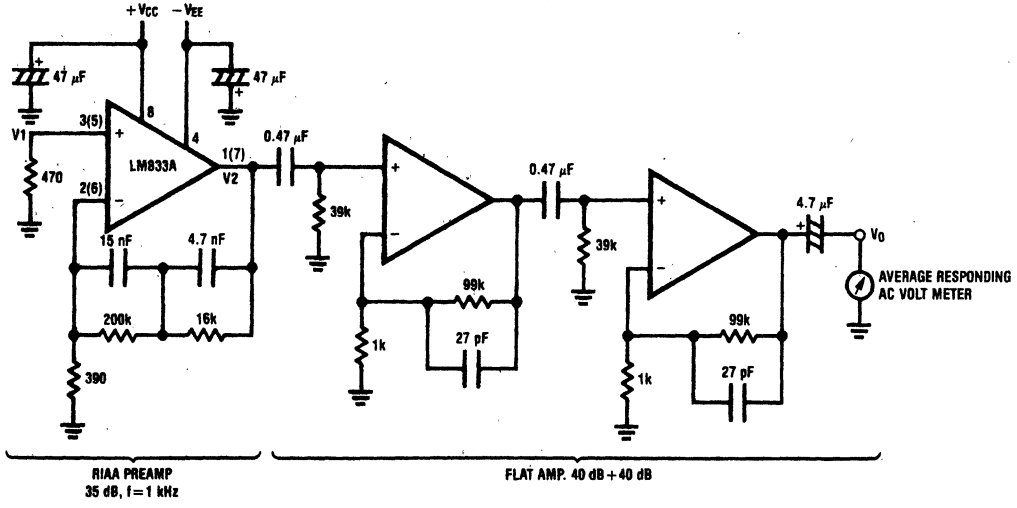
Application Hints

The LM833 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 50 pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 50 pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

Noise Measurement Circuit

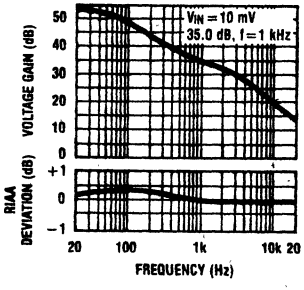
Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.



TL/H/5218–27

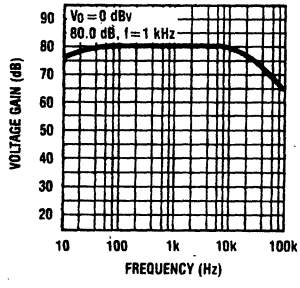
Total Gain: 115 dB @f = 1 kHz
Input Referred Noise Voltage: e_n = V0/560,000 (V)

RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency



TL/H/5218–28

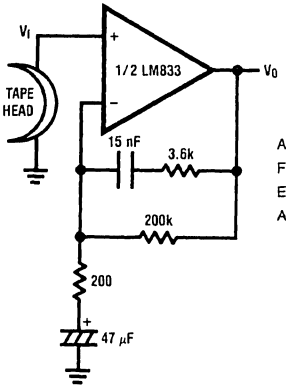
Flat Amp Voltage Gain vs Frequency



TL/H/5218–29

Typical Applications

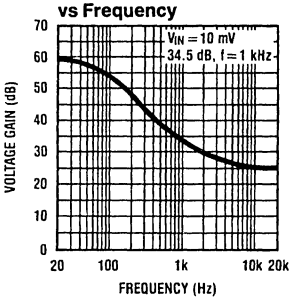
NAB Preamp



A_V = 34.5
F = 1 kHz
E_n = 0.38 µV
A Weighted

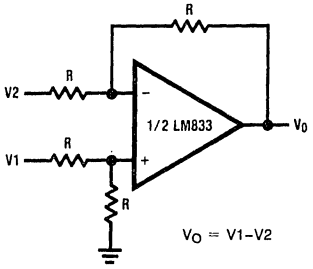
TL/H/5218–30

NAB Preamp Voltage Gain vs Frequency



TL/H/5218–31

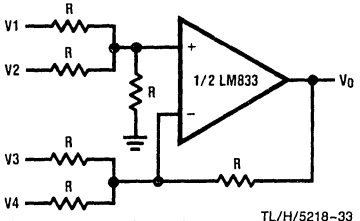
Balanced to Single Ended Converter



$V_O = V1 - V2$

TL/H/5218–32

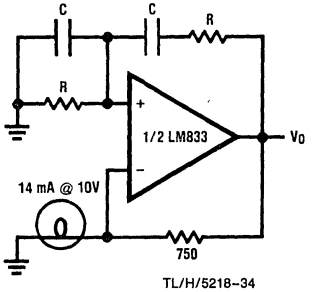
Adder/Subtracter



$V_O = V1 + V2 - V3 - V4$

TL/H/5218–33

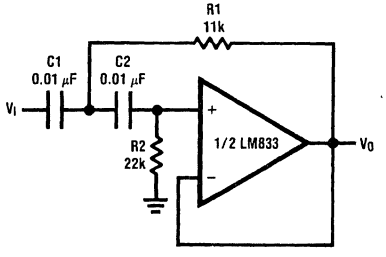
Sine Wave Oscillator



TL/H/5218–34

$$f_o = \frac{1}{2\pi R_C}$$

Second Order High Pass Filter (Butterworth)



TL/H/5218–35

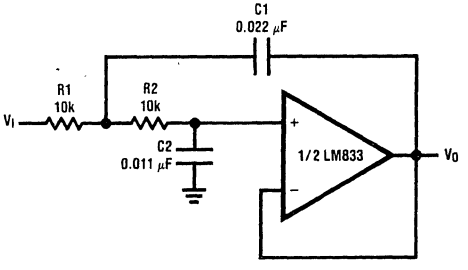
if C1 = C2 = C

$$R1 = \frac{\sqrt{2}}{2\omega_o C}$$

R2 = 2•R1

Illustration is f_0 = 1 kHz

Second Order Low Pass Filter (Butterworth)



TL/H/5218–36

if R1 = R2 = R

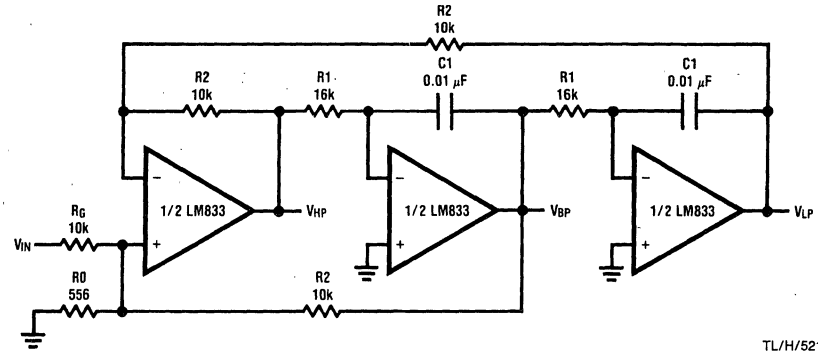
$$C1 = \frac{\sqrt{2}}{\omega_o R}$$

$$C2 = \frac{C1}{2}$$

Illustration is f_0 = 1 kHz

Typical Applications (Continued)

State Variable Filter

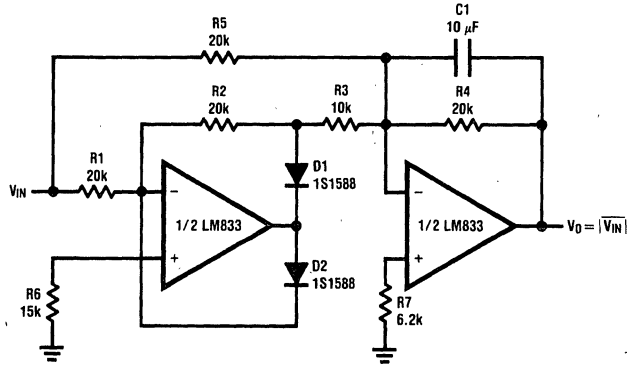


TL/H/5218–37

$$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{RQ} + \frac{R2}{RQ}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

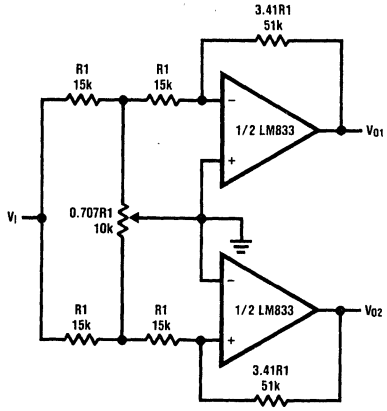
Illustration is f_0 = 1 kHz, Q = 10, A_{BP} = 1

AC/DC Converter



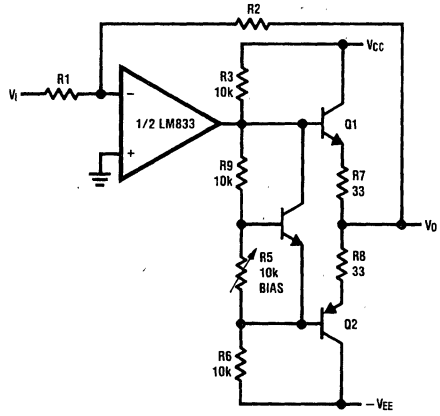
TL/H/5218–38

2 Channel Panning Circuit (Pan Pot)



TL/H/5218–39

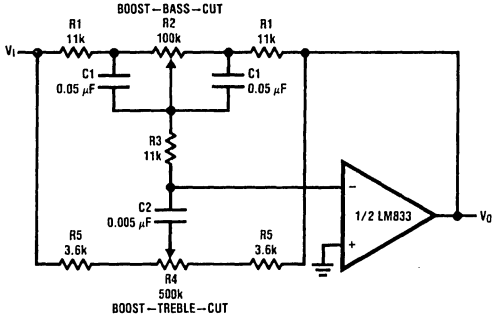
Line Driver



TL/H/5218–40

Typical Application (Continued)

Tone Control



TL/H/5218-41

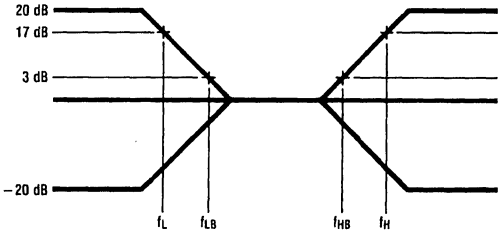
$$f_L = \frac{1}{2\pi R2C1},\ f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2},\ f_{HB} = \frac{1}{2\pi (R1+2R3)C2}$$

Illustration is:

f_L = 32 Hz, f_{LB} = 320 Hz

f_H = 11 kHz, f_{HB} = 1.1 kHz



TL/H/5218-42

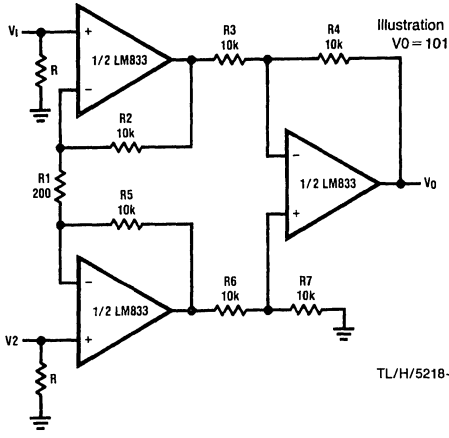
Balanced Input Mic Amp

If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

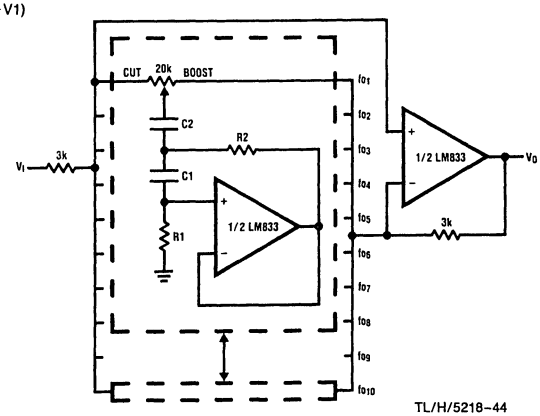
Illustration is:

V0 = 101(V2 – V1)



TL/H/5218-43

10 Band Graphic Equalizer



TL/H/5218-44

fo(Hz)	C_1	C_2	R_1	R_2
32	0.12μF	4.7μF	75kΩ	500Ω
64	0.056μF	3.3μF	68kΩ	510Ω
125	0.033μF	1.5μF	62kΩ	510Ω
250	0.015μF	0.82μF	68kΩ	470Ω
500	8200pF	0.39μF	62kΩ	470Ω
1k	3900pF	0.22μF	68kΩ	470Ω
2k	2000pF	0.1μF	68kΩ	470Ω
4k	1100pF	0.056μF	62kΩ	470Ω
8k	510pF	0.022μF	68kΩ	510Ω
16k	330pF	0.012μF	51kΩ	510Ω

At volume of change = ±12dB

Q = 1.7

Reference: "AUDIO/RADIO HANDBOOK", National Semiconductor, 1980, Page 2-61

Section 2

Comparators

Comparators

Section Contents

Voltage Comparators

National Semiconductor

PRELIMINARY

LP165/LP365 Micropower Programmable Quad Comparator

General Description

The LP165 series consists of four independent voltage comparators. The comparators can be programmed, four at the same time, for various supply currents, input currents, response times and output current drives. This is accomplished by connecting a single resistor between the V_{CC} and I_{SET} pins.

These comparators can be operated from split power supplies or from a single power supply over a wide range of voltages. The input can sense signals at ground level even with single supply operation. The unique output NPN transistor stages are uncommitted to either power supply. They can be connected directly to various logic system supplies so that they are highly flexible to interface with various logic families.

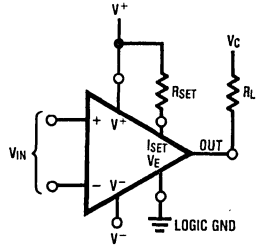
Application areas include battery power circuits, threshold detectors, zero crossing detectors, simple serial A/D converters, VCO, multivibrators, voltage converters, power sequencers, and high performance V/F converters, and RTD linearization.

Features

- Single programming resistor to tailor power consumption, input current, speed and output current drive capability
- Wide single supply voltage range or dual supplies (4 V_{DC} to 36 V_{DC} or ± 2.0 V_{DC} to ± 18 V_{DC})
- Low supply current drain (10 μA) and low power consumption (10 μW/comparator)@$I_{SET}=0.5$ μA $V_{CC}=5V_{DC}$
- Uncommitted output stage—selectable output levels
- Output directly compatible with DTL, TTL, CMOS, MOS or other special logic families
- Input common-mode range includes ground
- Differential input voltage equal to the power supply voltage

S 2

Typical Connection



TL/H/5023–1

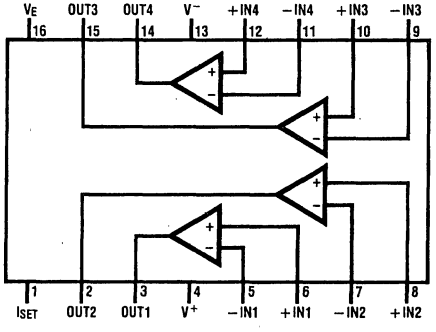
Programming Equation

$$I_{SET}=\frac{(V^+)-(V^-)-1.3V}{R_{SET}}$$

$$I_{SUPPLY}\approx 22\times I_{SET}$$

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5023–2

Order Numbers LP165D,N or LP365D,N
See NS Packages D16A, N16A

Absolute Maximum Ratings

Supply Voltage	36 V_{DC} or ± 18 V_{DC}
Differential Input Voltage	± 36 V_{DC}
Input Voltage (Note 1)	−0.3V to +36 V_{DC}
Output Short Circuit to V_E (Note 2)	Continuous
V_{OUT} with Respect to V_E	$V_E - 7V \le V_{OUT} \le V_E + 36V$

	D Package	N Package
Power Dissipation (Note 3)	670 mW	500 mW
$T_j$max	150°C	115°C
θ_{jA}	90° C/W	90° C/W
Operating Temperature Range	(Note 4)	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (Note 5) Low power $V_S = 5V$, $I_{SET} = 10\ \mu A$

Symbol	Parameter	Conditions	LP165			LP365A			LP365			Units (Limit)
			Typ	Tested Limit (Note 6)	Design Limit (Note 7)	Typ	Tested Limit (Note 6)	Design Limit (Note 7)	Typ	Tested Limit (Note 6)	Design Limit (Note 7)	
V_{OS}	Input Offset Voltage	V_{CM}=0V, R_S=100	1	3 **6**		1	3	**6**	3	6	**9**	mV (Max)
I_{OS}	Input Offset Current	V_{CM}=0V	2	20 **50**		2	20	**50**	4	25	**75**	nA (Max)
I_B	Input Bias Current	V_{CM}=0V	10	50 **125**		10	50	**125**	15	75	**200**	nA (Max)
A_{VOL}	Large Signal Voltage Gain	R_L=100k	500	**50**		500	50	**50**	300	25	**25**	V/mV (Min)
V_{CM}	Input Common-Mode Voltage Range			**0**			0	**0**		0	**0**	V (Max)
				3			3	**3**		3	**3**	V (Min)
CMRR	Common-Mode Rejection Ratio	$0 \le V_{CM} \le 3V$	85	75 **70**		85	75	**70**	80	75	**70**	dB (Min)
PSRR	Supply Voltage Rejection Ratio	$\pm 2.5V \le V_S \le \pm 3.5V$	75	**65**		75	65	**65**	70	65	**65**	dB (Min)
I_S	Supply Current	All Inputs=0V, $R_L = \infty$	215	250 **300**		215	250	**300**	225	275	**300**	μA (Max)
V_{OH}	Output Voltage High	V_C=5V, V_E=0V, R_L=100k		4.9 **4.5**			4.9	**4.5**		4.9	**4.5**	V (Min)
V_{OL}	Output Voltage Low	V_E=0V		**0.4**			0.4	**0.4**		0.4	**0.4**	V (Max)
I_{SINK}	Output Sink Current	V_E=0V, V_O=0.4V	2.4	1.2 **0.6**		2.4	1.2	**0.6**	2.0	0.8	**0.4**	mA (Min)
I_{LEAK}	Output Leakage Current	V_C=5V, V_E=0V	2	50 **5000**		2	50	**5000**	2	100	**5000**	nA (Max)
t_R	Response Time	V_{CC}=5V, V_E=0V, R_L=5k, C_L=10 pF (Note 8)	4			4			4			μS

Electrical Characteristics (Continued) (Note 9) High power $V_S = \pm 15V$, $I_{SET} = 100\ \mu A$

Symbol	Parameter	Conditions	LP165			LP365A			LP365			Units (Limit)
			Typ	Tested Limit (Note 6)	Design Limit (Note 7)	Typ	Tested Limit (Note 6)	Design Limit (Note 7)	Typ	Tested Limit (Note 6)	Design Limit (Note 7)	
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $R_S = 100$	1	3 **6**		1	3	**6**	3	6	**9**	mV (max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$	5	50 **100**		5	50	**100**	10	90	**200**	nA (Max)
I_B	Input Bias Current	$V_{CM} = 0V$	60	200 **500**		60	200	**500**	80	300	**500**	nA (Max)
A_{VOL}	Large Signal Voltage Gain	$R_L = 15k$	500	**100**		500	100	**100**	500	100	**100**	V/mV (Min)
V_{CM}	Input Common-Mode Voltage Range			**−15**			−15	**−15**		−15	**−15**	V (Max)
				13			13	**13**		13	**13**	V (Min)
CMRR	Common-Mode Rejection Ratio	$-15V \le V_{CM} \le 13V$	85	75 **70**		85	75	**70**	80	75	**70**	dB (Min)
PSRR	Supply Voltage Rejection Ratio	$\pm 10V \le V_S \le \pm 15V$	80	**70**		80	70	**70**	75	70	**70**	dB (Min)
I_S	Supply Current	All Inputs = 0V, $R_L = \infty$	2.6	3 **3.3**		2.6	3	**3.3**	2.8	3.5	**3.7**	mA (Max)
V_{OH}	Output Voltage High	$V_C = 5V$, $V_E = 0V$, $R_L = 100k$		4.9 **4.5**			4.9	**4.5**		4.9	**4.5**	V (Min)
V_{OL}	Output Voltage Low	$V_E = 0V$		**0.4**			0.4	**0.4**		0.4	**0.4**	V (Max)
I_{SINK}	Output Sink Current	$V_E = 0V$, $V_O = 0.4V$	10	8 **5.5**		10	8	**5.5**	7.5	6	**4**	mA (Min)
I_{LEAK}	Output Leakage Current	$V_C = 15V$, $V_E = -15V$	5	50 **5000**		5	50	**5000**	5	50	**5000**	nA (Max)
t_R	Response Time	$V_{CC} = 5V$, $V_E = 0V$, $R_L = 5k$, $C_L = 10$ pF (Note 8)	1.0			1.0			1.0			μs

Note 1: The input voltage is not allowed to go 0.3V above V^+ or −0.3V below V^- as this will turn on a parasitic transistor causing large currents to flow through the device.

Note 2: Short circuits from the output to V^+ may cause excessive heating and eventual destruction. The current in the output leads and the V_E lead should not be allowed to exceed 30 mA. The output should not be shorted to V^- if $V_E \le (V^-) + 7V$.

Note 3: For operating at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{jA} and T_j max. $T_j = T_A + \theta_{jA} P_D$.

Note 4: The LP165 may be operated from $-55°C \le T_A \le +125°C$ and the LP365A/LP365 may be operated from $0°C \le T_A \le +70°C$.

Note 5: Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = T_j = 25°C$. $V^+ = 5V$, $V^- = 0V$, $I_{SET} = 10\mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

Note 6: Guaranteed and 100% production tested.

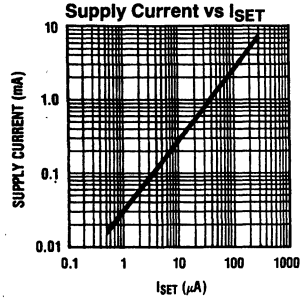
Note 7: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate out-going quality levels.

Note 8: The response time specified is for a 100 mV input step with 5 mV overdrive.

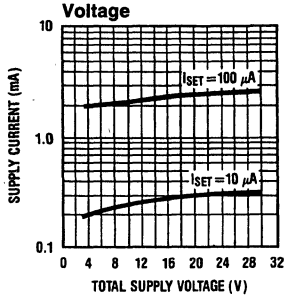
Note 9: Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = T_j = 25°C$. $V^+ = +15V$, $V^- = -15V$, $I_{SET} = 100\ \mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

Typical Performance Characteristics

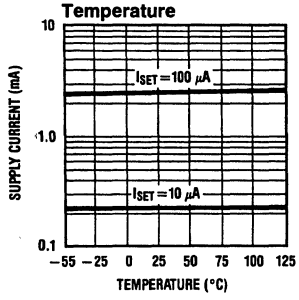
Supply Current vs I_{SET}



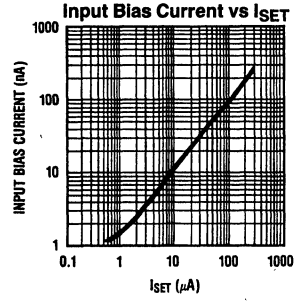
Supply Current vs Supply Voltage



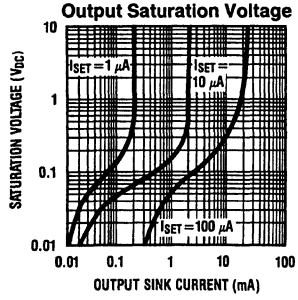
Supply Current vs Temperature



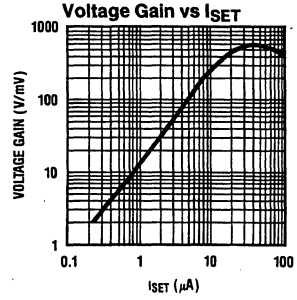
Input Bias Current vs I_{SET}



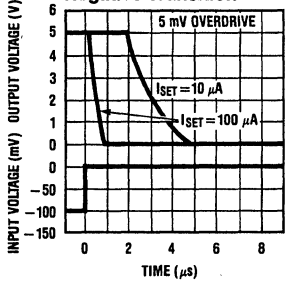
Output Saturation Voltage



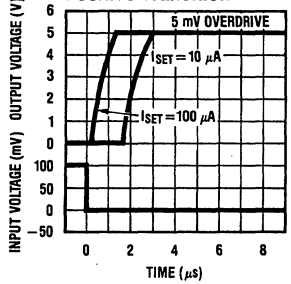
Voltage Gain vs I_{SET}



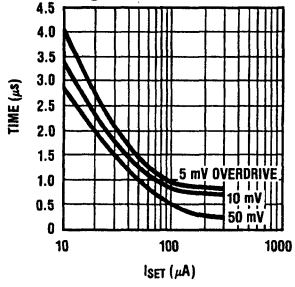
Response Time Negative Transition



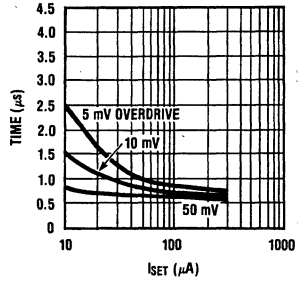
Response Time Positive Transition



Response Time Negative Transition



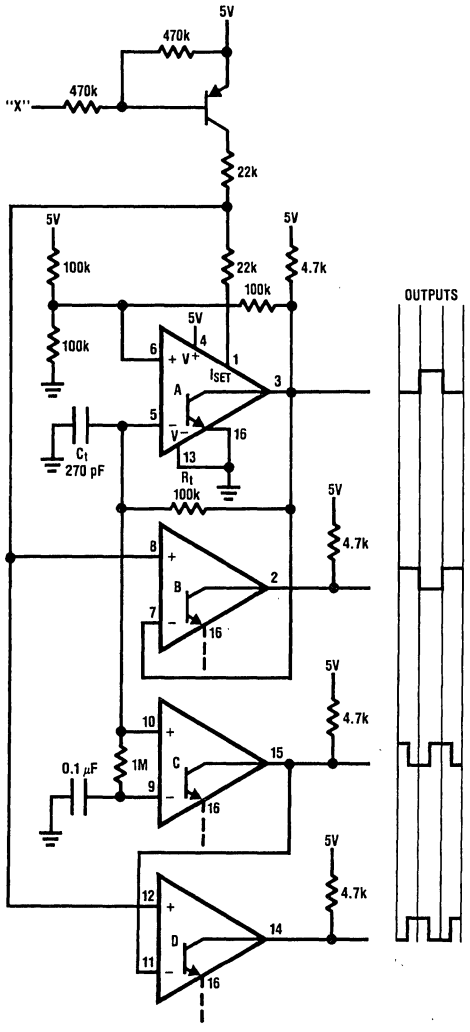
Response Time Positive Transition



TL/H/5023–3

Typical Applications

Gated 4-Phase Oscillator



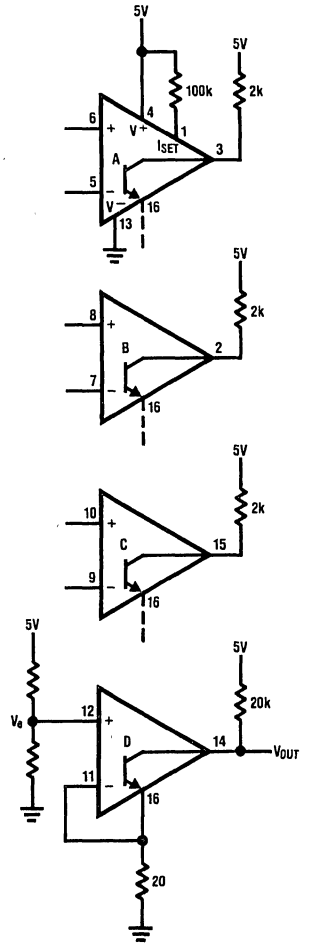
TL/H/5023–4

$f = 20$ kHz

$$f = \frac{1}{1.6 \bullet R_t \bullet C_t}$$

All four phases run when X is low. When X is high, oscillation stops and power drain is zero.

Voltage Comparator

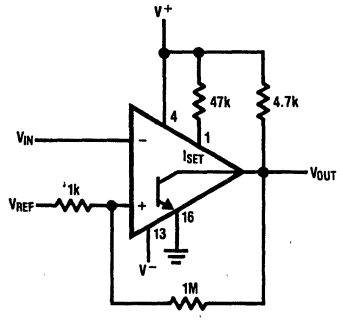


TL/H/5023–5

If you choose $V_e = 25$ mV, 75 mV, or 125 mV, then V_{OUT} will fall if 1/3, 2/3 or all of the other three outputs are low.

Typical Applications (Continued)

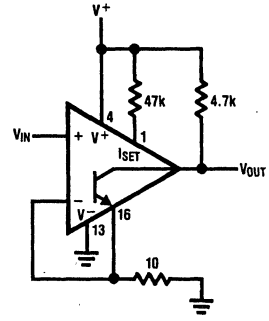
Ordinary Hysteresis



TL/H/5023–6

It is a good practice to add a few millivolts of positive feedback to prevent oscillation when the input voltage is near the threshold.

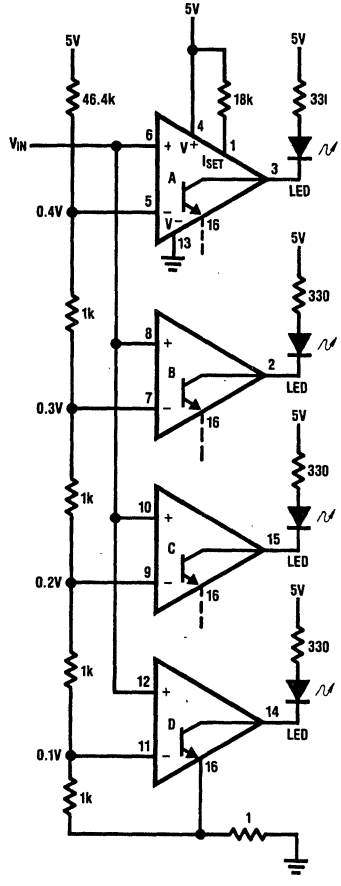
Hysteresis from Emitter



TL/H/5023–7

Positive feedback from the emitter can also prevent oscillations when V_{IN} is near the threshold.

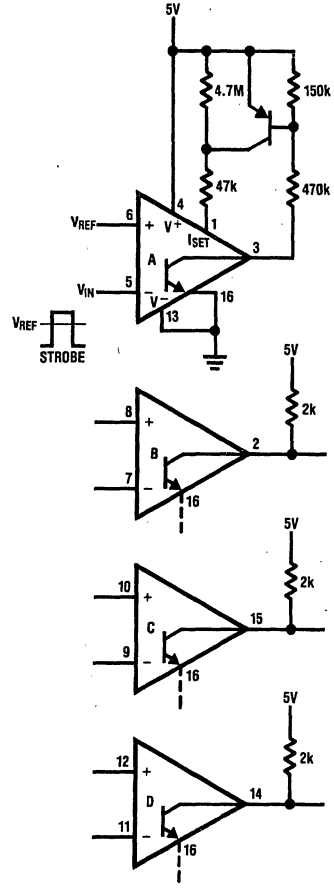
Bar-Graph Display



TL/H/5023–8

The positive feedback from pin 16 provides hysteresis.

Level-Sensitive Strobe

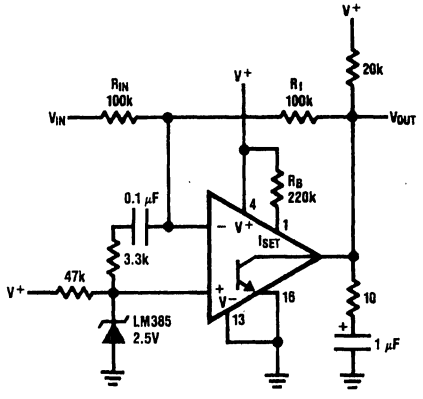


TL/H/5023–9

Comparators B, C, and D do not respond until activated by the signal applied to comparator A.

Typical Applications (Continued)

Slow Op Amp (Inverter)

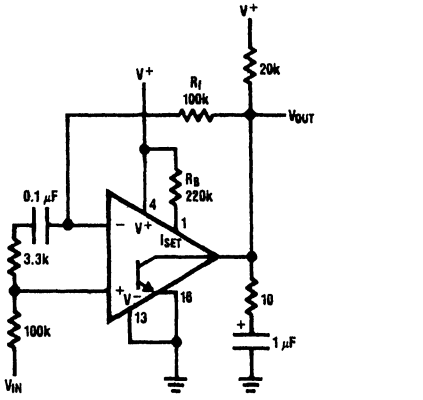


TL/H/5023–10

$R_B = V^+/20\ \mu A$

Unlike most comparators, the LP165 can be used as an op amp, if suitable R-C damping networks are used.

Slow Op Amp (Unity-Gain Follower)

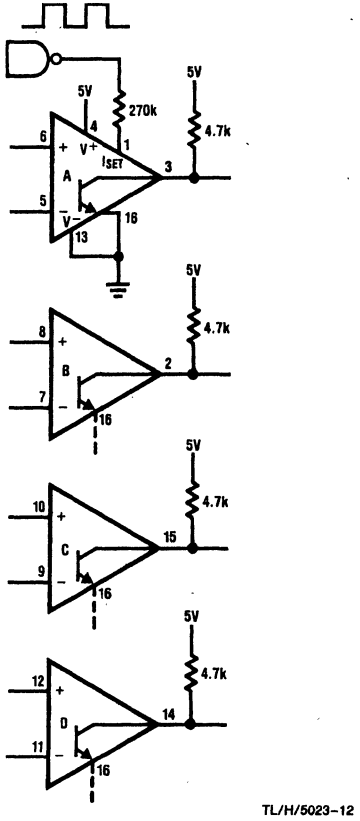


TL/H/5023–11

$R_B = V^+/20\ \mu A$

The LP165 can also be used as a high-input-impedance follower-amplifier with the damping components shown.

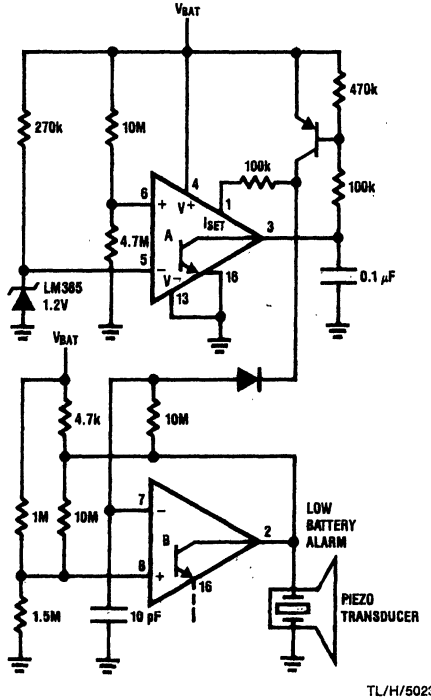
Chopping Outputs



TL/H/5023–12

Chopping the outputs by modulating the I_{SET} current allows data to be transmitted via opto-couplers, transformers, etc.

Low Battery Detector



TL/H/5023–13

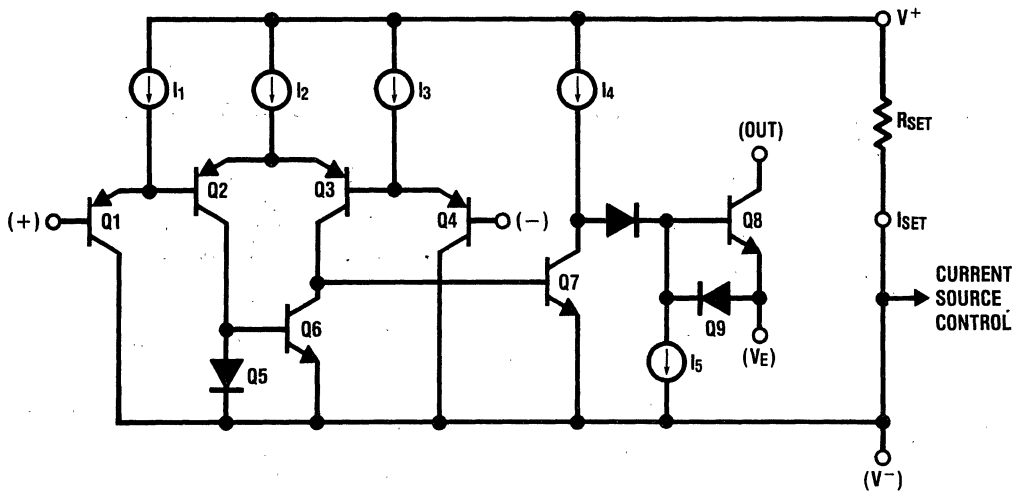
I_S @ 6V = 45 µA

I_S @ 3.6V = 1 µA

f = 3 kHz

Comparator A detects when the supply voltage drops to 4V and enables comparator B to drive a piezoelectric alarm.

Simplified Schematic



TL/H/5023–14

Current sources are programmed by I_{SET}

V_E is common to all 4 comparators

National Semiconductor

PRELIMINARY

LP311 Voltage Comparator

General Description

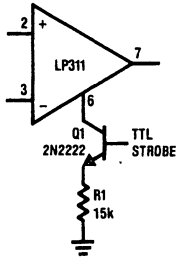
The LP311 is a low power version of the industry-standard LM311. It takes advantage of stable high-value ion-implanted resistors to perform the same function as an LM311, with a 30:1 reduction in power drain, but only a 6:1 slowdown of response time. Thus the LP311 is well suited for battery-powered applications, and all other applications where fast response is not needed. It operates over a wide range of supply voltages from 36V down to a single 3V supply, with less than 200 μA drain, but it is still capable of driving a 25 mA load. The LP311 is quite easy to apply without any oscillation, if ordinary precautions are taken to minimize stray coupling from the output to either input or to the trim pins. (See the LM311 section of the Linear Databook.)

Features

- Low power drain, 900 μW on 5V supply
- Operates from ±15V or a single supply as low as 3V
- Output can drive 25 mA
- Emitter output can swing below negative supply
- Response time: 1.2 μs
- Same pin-out as LM311
- Low input currents: 2 nA of offset, 15 nA of bias
- Large common-mode input range: −14.6V to 13.6V with ±15V supply

Auxiliary Circuits

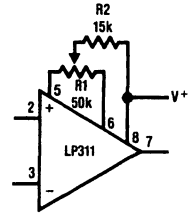
Strobing



TL/H/5711–1

Note: Do not ground strobe pin.

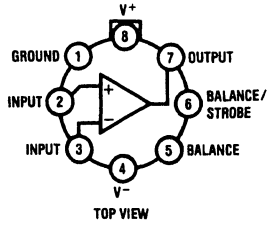
Offset Balancing



TL/H/5711–2

Connection Diagrams

Metal Can Package

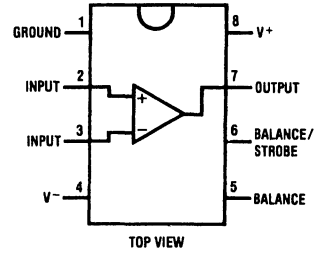


TL/H/5711–3

Note: Pin 4 connected to case.

Order Number LP311H
See NS Package Number H08C

Dual-In-Line Package



TL/H/5711–4

Order Number LP311N
See NS Package Number N08B

Absolute Maximum Ratings

Total Supply Voltage (V84)	36V	Power Dissipation (Note 2)	500 mW
Collector Output to Negative Supply Voltage (V74)	40V	Output Short Circuit Duration	10 sec
Collector Output to Emitter Output	40V	Operating Temperature Range	0°C to 70°C
Emitter Output to Negative Supply Voltage (V14)	±30V	Storage Temperature Range	−65°C to 150°C
Differential Input Voltage	±30V	Lead Temperature (Soldering, 10 seconds)	300°C
Input Voltage (Note 1)	±15V		

Electrical Characteristics (Note 3)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 100k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		2.0	25	nA
Input Bias Current	$T_A = 25°C$		15	100	nA
Voltage Gain	$T_A = 25°C$, $R_L = 5k$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		1.2		μs
Saturation Voltage (Note 6)	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.4	1.5	V
Strobe Current (Note 7)	$T_A = 25°C$		100	300	μA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$		0.2	100	nA
Input Offset Voltage (Note 4)	$R_S \leq 100k$			10	mV
Input Offset Current (Note 4)				35	nA
Input Bias Current				150	nA
Input Voltage Range		$V^- + 0.5$	+13.7, −14.7	$V^+ - 1.5$	V
Saturation Voltage (Note 6)	$V^+ \geq 4.5V$, $V^- = 0V$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 1.6$ mA		0.1	0.4	V
Positive Supply Current	$T_A = 25°C$		150	300	μA
Negative Supply Current	$T_A = 25°C$		80	180	μA
Minimum Operating Voltage	$T_A = 25°C$		3.0	3.5	V

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LP311 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 160°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 4V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Note 6: Saturation voltage specification applied to collector-emitter voltage (V7-1) for $V_{COLLECTOR} \leq (V+ - 3V)$.

Note 7: Do not short the strobe pin to ground. It should be current driven, 100 μA to 300 μA.

National Semiconductor

PRELIMINARY

LP339 Ultra-Low Power Quad Comparator

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 μA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

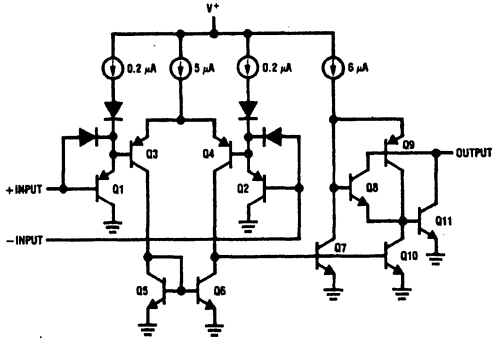
Advantages

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

Features

- Ultra-low power supply current drain (60 μA) — independent of the supply voltage (75 μW/comparator at +5 V_{DC})
- Low input biasing current 3 nA
- Low input offset current ±0.5 nA
- Low input offset voltage ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at V_O=2 V_{DC})
- Supply Input protected against reverse voltages

Schematic and Connection Diagrams



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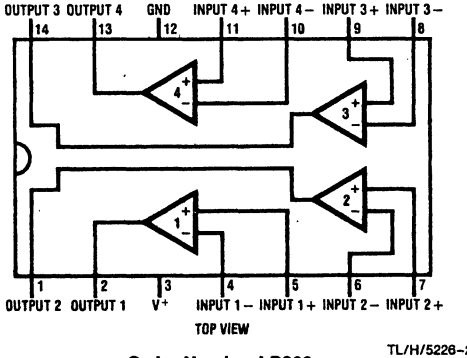
Dual-In-Line Package

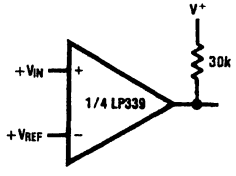


TL/H/5226–2

Order Number LP339
See NS Packages N14A, M14A

Typical Applications (V^+ = 5.0 V_{DC})

Basic Comparator



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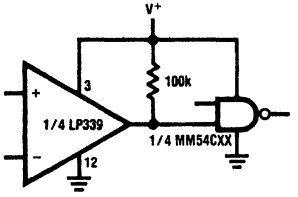
Driving CMOS



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Absolute Maximum Ratings

Supply Voltage	36 V_{DC} or ±18 V_{DC}	Input Current $V_{IN} < -0.3\ V_{DC}$ (Note 3)	50 mA
Differential Input Voltage	±36 V_{DC}	Operating Temperature Range	0°C to 70°C
Input Voltage	−0.3 V_{DC} to 36 V_{DC}	Storage Temperature Range	−65° to +150°C
Power Dissipation (Note 1) Molded DIP	570 mW	Lead Temperature (Soldering, 5 seconds)	260°C
Output Short Circuit to GND (Note 2)	Continuous		

Electrical Characteristics ($V+ = 5\ V_{DC}$, Note 4)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	$T_A = 25°C$ (Note 9)		±2	±5	mV_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with the Output in the Linear Range, $T_A = 25°C$, (Note 5)		2.5	25	nA_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$, $T_A = 25°C$		±0.5	±5	nA_{DC}
Input Common-Mode Voltage Range	$T_A = 25°C$ (Note 6)	0		V+ −1.5	V_{DC}
Supply Current	R_L = Infinite on all Comparators, $T_A = 25°C$		60	100	μA_{DC}
Voltage Gain	$R_L = 15\ k\Omega$, $V+ = 15\ V_{DC}$, $T_A = 25°C$		500		V/mV
Large Signal Reponse Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		1.3		μSec
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 7)		8		μSec
Output Sink Current	$V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $V_O = 2\ V_{DC}$, $T_A = 25°C$, (Note 11)	20	30		mA_{DC}
	$V_O = 0.4\ V_{DC}$	0.20	0.70		mA_{DC}
Output Leakage Current	$V_{IN}(+) = 1\ V_{DC}$, $V_{IN}(-) = 0$, $V_O = 5\ V_{DC}$, $T_A = 25°C$		0.1		nA_{DC}
Input Offset Voltage	(Note 9)			±9	mV_{DC}
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$		±1	±15	nA_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range		4	40	nA_{DC}
Input Common-Mode Voltage Range	Single Supply	0		V+ −2.0	V_{DC}
Output Sink Current	$V_{IN}(-) = 1\ V_{DC}$, $V_{IN}(+) = 0$, $V_O = 2\ V_{DC}$	15			mA_{DC}
Output Leakage Current	$V_{IN}(+) = 1\ V_{DC}$, $V_{IN}(-) = 0$, $V_O = 30\ V_{DC}$			1.0	μA_{DC}
Differential Input Voltage	All V_{IN}'s ≥ 0 V_{DC} (or V− on split supplies) (Note 8)			36	V_{DC}

Note 1: For operation at high temperatures, the LP339 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V+ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0.3 V_{DC} ($T_A = 25°C$).

Note 4: These specifications apply for $V+ = 5V_{DC}$ and $0°C \leq T_A \leq 70°$ C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

Note 6: The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V ($T_A = 25°C$), but either or both inputs can go to 30 V_{DC} without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 μs can be obtained. See Typical Performance Characteristics section.

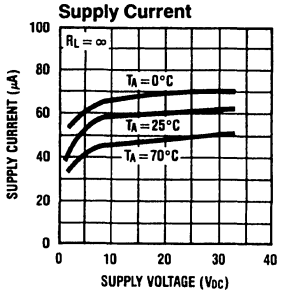
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) at $T_A = 25°C$.

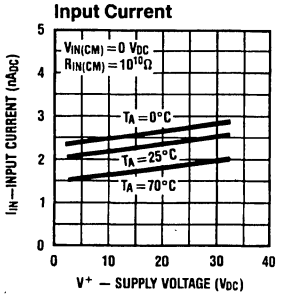
Note 9: At output switch point, $V_O = 2V_{DC}$, $R_S = 0\Omega$ with V+ from 5 V_{DC}; and over the full input common-mode range (0 V_{DC} to V+ −1.5 V_{DC}).

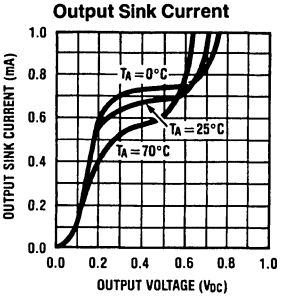
Note 10: For input signals that exceed V+, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

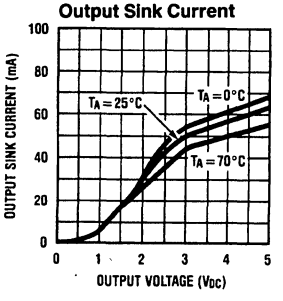
Note 11: The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately 1.5 V_{DC} and sink lower currents below this point. (See typical characteristics section and applications section).

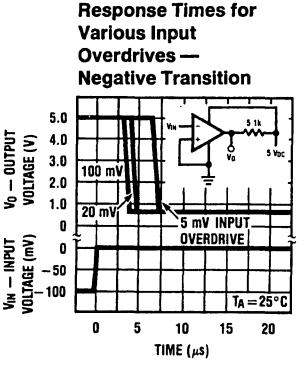
Typical Performance Characteristics

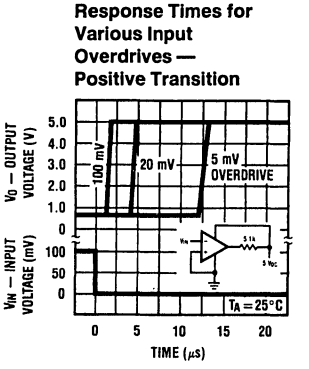












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Application Hints

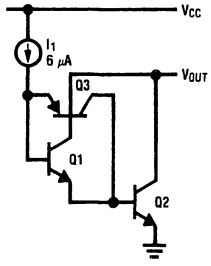
All pins of any unused comparators should be grounded.

The bias network of the LP339 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the application section.

The output section of the LP339 has two distinct modes of operation-a Darlington mode and a grounded emitter mode. This unique drive circuit permits the LP339 to sink 30 mA at $V_O = 2\ V_{DC}$ (Darlington mode) and 700 μA at $V_O = 0.4\ V_{DC}$ (grounded emitter mode). *Figure 1* is a simplified schematic diagram of the LP339 output section.



TL/H/5226–11

FIGURE 1

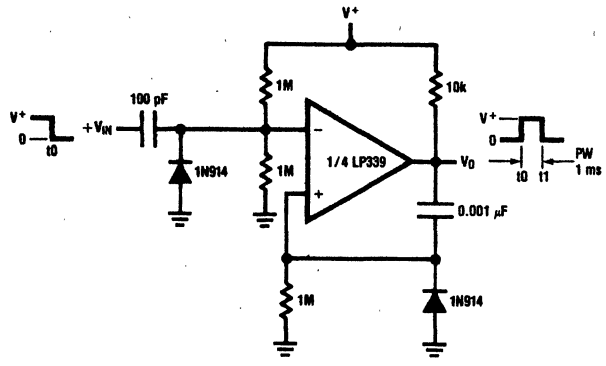
Notice that the output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough ($V_O \geq 1\ V_{DC}$), Q1 is not saturated and the output current is limited only by the product of the betas of Q1, Q2 and I1 (and the 60Ω R_{SAT} of Q2). The LP339 is thus capable of driving LED's, relays, etc. in this mode while maintaining an ultra-low power supply current of typically 60 μA.

If transistor Q3 were omitted, and the output voltage allowed to drop below about 0.8 V_{DC}, transistor Q1 would saturate and the output current would drop to zero. The circuit would, therefore, be unable to 'pull' low current loads down to ground (or the negative supply, if used). Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the beta of Q2 (700 μA at $V_O = 0.4\ V_{DC}$). The output of the LP339 exhibits a bi-modal characteristic with a smooth transition between modes. (See Output Sink Current graphs in Typical Performance Characteristics section.)

It is also important to note that in both cases the output is an uncommitted collector. Therefore, many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V+ terminal of the LP339 package.

Typical Applications ($V^+ = 15\ V_{DC}$)

One-Shot Multivibrator



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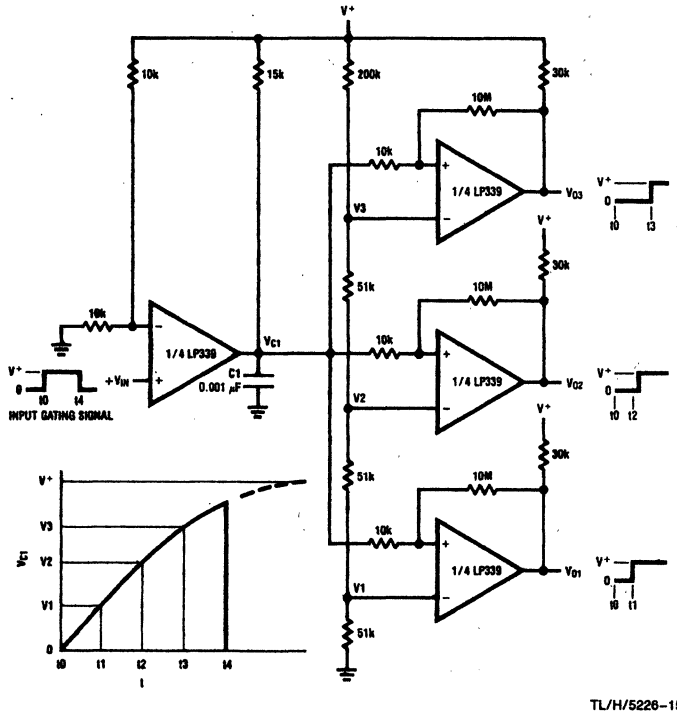
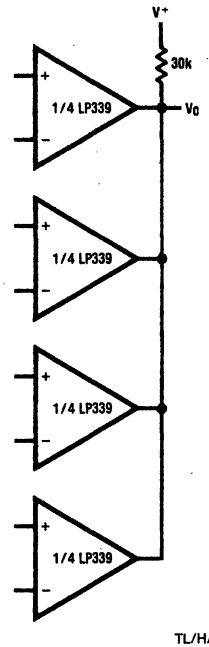
Time Delay Generator



TL/H/5226–15

ORing the Outputs



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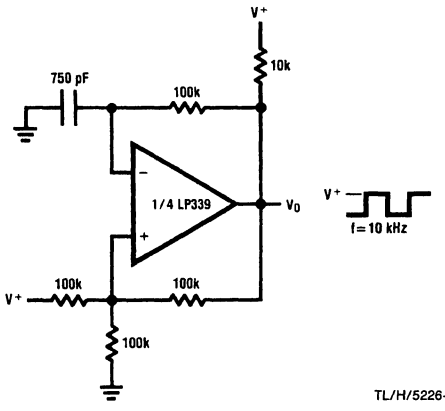
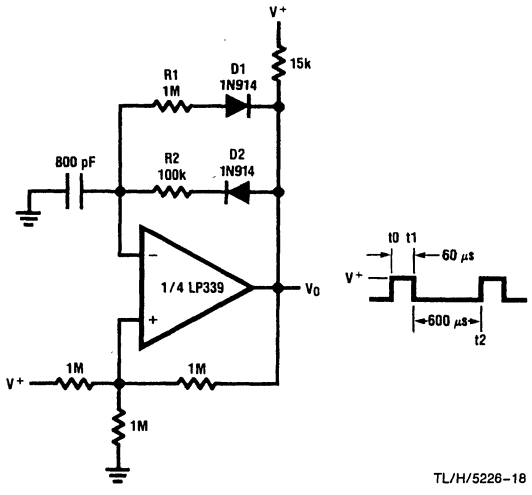
Typical Applications (Continued) ($V^+ = 15\ V_{DC}$)

Squarewave Oscillator



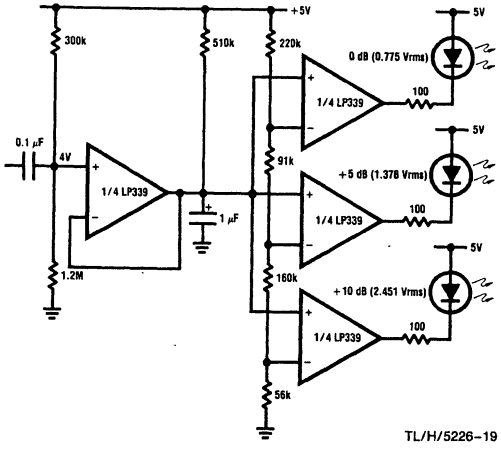
TL/H/5226–17

Pulse Generator



TL/H/5226–18

Three Level Audio Peak Indicator



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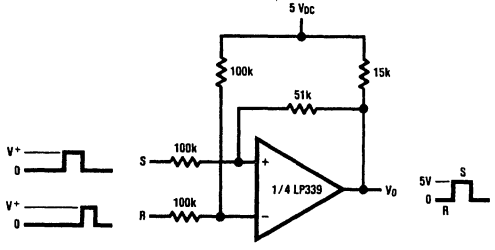
Bi-Stable Multivibrator



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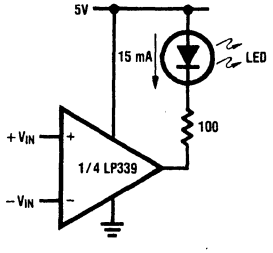
LED Driver



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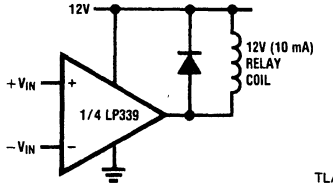
Relay Driver



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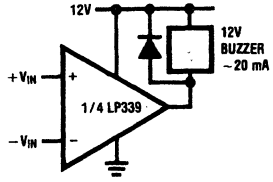
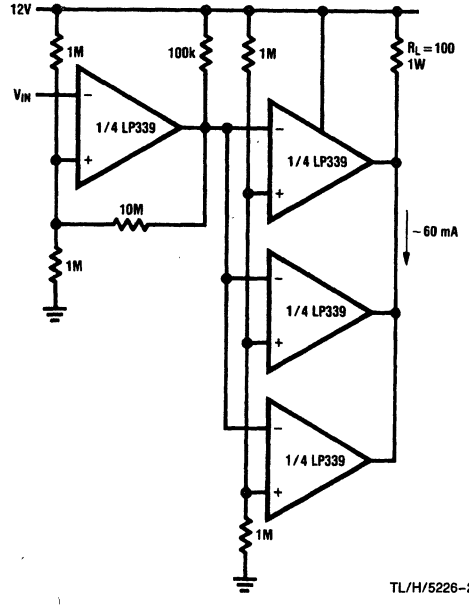
Typical Applications (Continued) (Single Supply)

Buzzer Driver



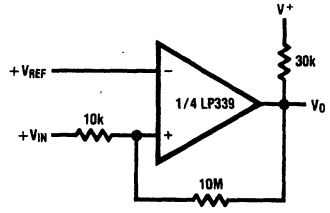
TL/H/5226-24

Comparator With 60 mA Sink Capability



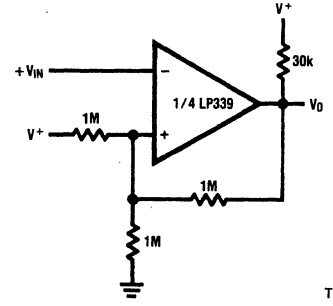
TL/H/5226-25

Non-Inverting Comparator with Hysteresis



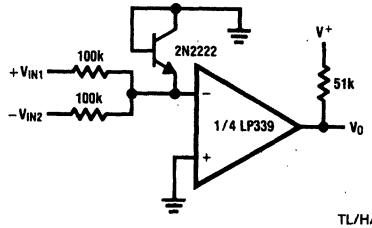
TL/H/5226-26

Inverting Comparator with Hysteresis



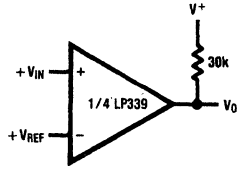
TL/H/5226-27

Comparing Input Voltages of Opposite Polarity



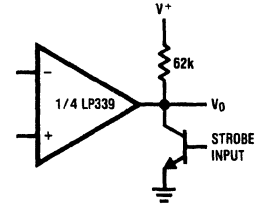
TL/H/5226-28

Basic Comparator



TL/H/5226-29

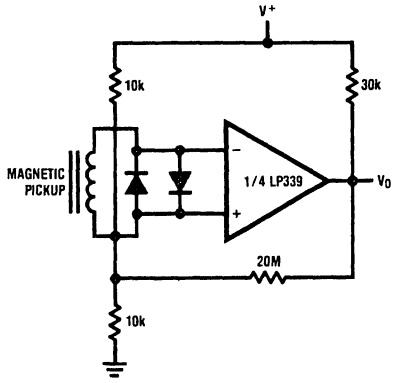
Output Strobing



TL/H/5226-30

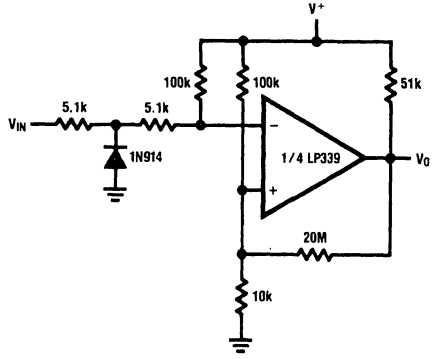
Typical Applications (Continued) (Single Supply)

Transducer Amplifier



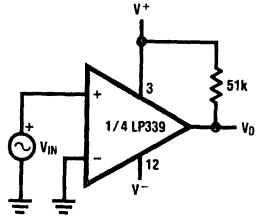
TL/H/5226–31

Zero Crossing Detector (Single Power Supply)



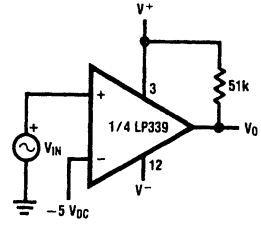
TL/H/5226–32

Split-Supply Applications Zero Crossing Detector



TL/H/5226–33

Comparator With a Negative Reference



TL/H/5226–34

S 2

Section 3

Voltage Regulators

Voltage Regulators

Section Contents

National Semiconductor

LM2930 3-Terminal Positive Regulator

General Description

The LM2930 3-terminal positive regulator features an ability to source 150 mA of output current with an input-output differential of 0.6V or less. Efficient use of low input voltages obtained, for example, from an automotive battery during cold crank conditions, allows 5V circuitry to be properly powered with supply voltages as low as 5.6V. Familiar regulator features such as current limit and thermal overload protection are also provided.

Designed primarily for automotive applications, the LM2930 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (40V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2930 cannot be harmed by temporary mirror-image insertion.

Fixed outputs of 5V and 8V are available in the plastic TO-220 power package.

Features

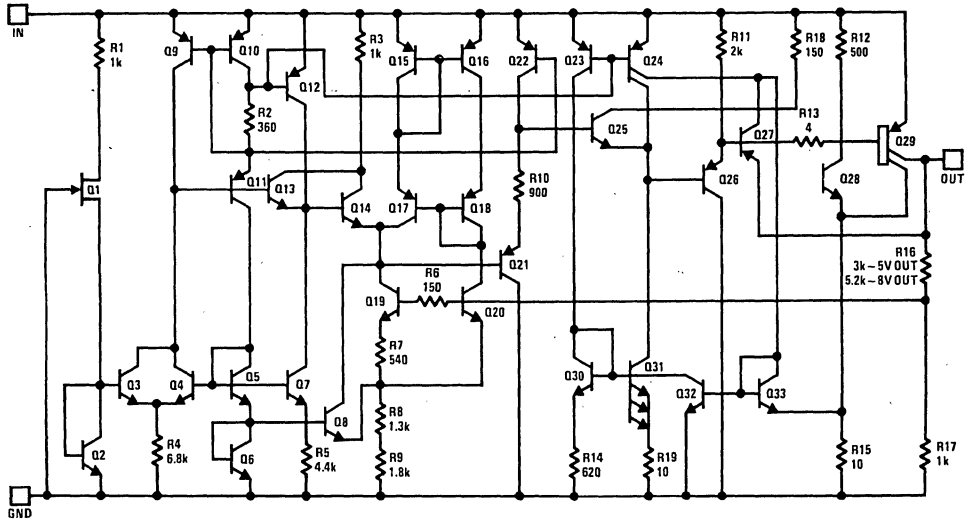
- Input-output differential less than 0.6V
- Output current in excess of 150 mA
- Reverse battery protection
- 40V load dump protection
- Internal short circuit current limit
- Internal thermal overload protection
- Mirror-image insertion protection
- 100% electrical burn-in in thermal limit

Voltage Range

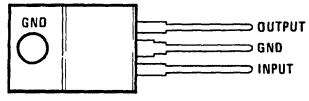
LM2930T-5.0	5V
LM2930T-8.0	8V

S 3

Schematic and Connection Diagrams



(TO-220)
Plastic Package



FRONT VIEW

TL/H/5539–1

Order Number LM2930T-5.0 or LM2930T-8.0
See NS Package T03B

Absolute Maximum Ratings

Input Voltage		Internal Power Dissipation (Note 1)	Internally Limited
Operating Range	26V	Operating Temperature Range	−40°C to +85°C
Overvoltage Protection	40V	Maximum Junction Temperature	125°C
Reverse Voltage (100 ms)	−12V	Storage Temperature Range	−65°C to +150°C
Reverse Voltage (DC)	−6V	Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics (Note 2)

LM2930T-5.0 (V_{IN} = 14V, I_O = 150 mA, T_J = 25°C, C2 = 10 µF, unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	6V ≤ V_{IN} ≤ 26V, 5 mA ≤ I_O ≤ 150 mA, T_J = 25°C	4.5	5	5.5	V
Line Regulation	9V ≤ V_{IN}16V, I_O = 5 mA 6V ≤ V_{IN} ≤ 26V, I_O = 5 mA		7 30	25 80	mV mV
Load Regulation	5 mA ≤ I_O ≤ 150 mA		14	50	mV
Output Impedance	100 mA_{DC} & 10 mArms, 100 Hz−10 kHz		200		mΩ
Quiescent Current	I_O = 10 mA I_O = 150 mA		4 18	7 40	mA mA
Output Noise Voltage	10 Hz−100 kHz		140		µVrms
Long Term Stability			20		mV/1000 hr
Ripple Rejection	f_O = 120 Hz		56		dB
Current Limit		150	400	700	mA
Dropout Voltage	I_O = 150 mA		0.32	0.6	V
Output Voltage Under Transient Conditions	−12V ≤ V_{IN} ≤ 40V, R_L = 100Ω	−0.3		5.5	V

Electrical Characteristics (Note 2)

LM2930T-8.0 (V_{IN} = 14V, I_O = 150 mA, T_J = 25°C, C2 = 10 µF, unless otherwise specified)

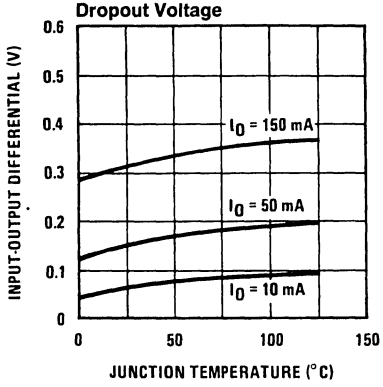
Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	9.4V ≤ V_{IN} ≤ 26V, 5 mA ≤ I_O ≤ 150 mA, T_J = 25°C	7.2	8	8.8	V
Line Regulation	9.4V ≤ V_{IN} ≤ 16V, I_O = 5 mA 9.4V ≤ V_{IN}26V, I_O = 5 mA		12 50	50 100	mV mV
Load Regulation	5 mA ≤ I_O ≤ 150 mA		25	50	mV
Output Impedance	100 mA_{DC} & 10 mArms, 100 Hz−10 kHz		300		mΩ
Quiescent Current	I_O = 10 mA 1_O = 150 mA		4 18	7 40	mA mA
Output Noise Voltage	10 Hz−100 kHz		170		µVrms
Long Term Stability			30		mV/1000 hr
Ripple Rejection	f_O = 120 Hz		52		dB
Current Limit		150	400	700	mA
Dropout Voltage	I_O = 150 mA		0.32	0.6	V
Output Voltage Under Transient Conditions	−12V ≤ V_{IN} ≤ 40V, R_L = 100Ω	−0.3		8.8	V

Note 1: Thermal resistance without a heat sink for junction to case temperature is 4°C/W and for case to ambient temperature is 50°C/W.

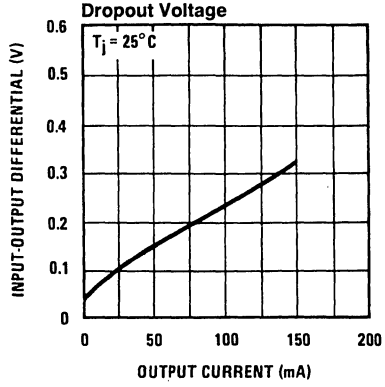
Note 2: All characteristics are measured with a capacitor across the input of 0.1 µF and a capacitor across the output of 10 µF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

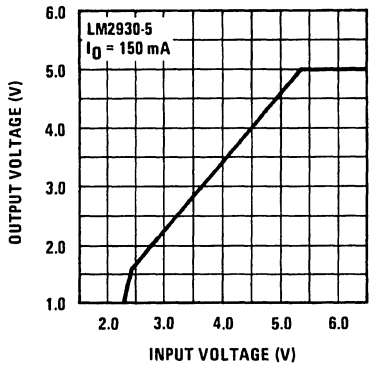
Dropout Voltage



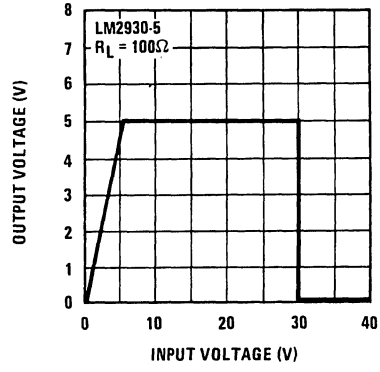
Dropout Voltage



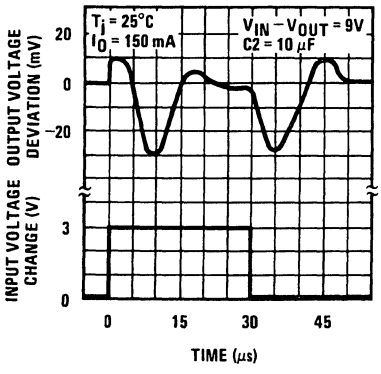
Low Voltage Behavior



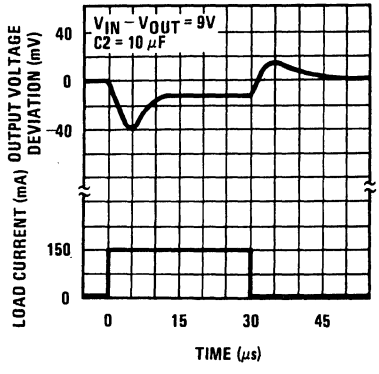
High Voltage Behavior



Line Transient Response



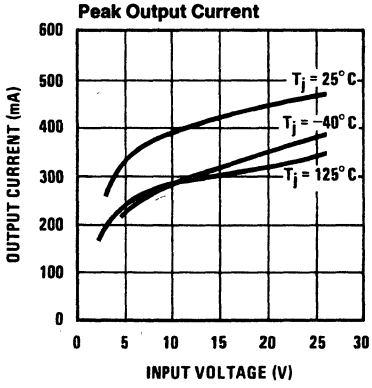
Load Transient Response



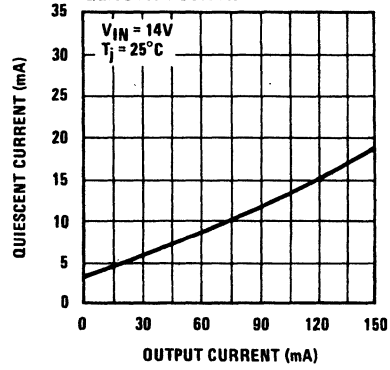
TL/H/5539–2

Typical Performance Characteristics (Continued)

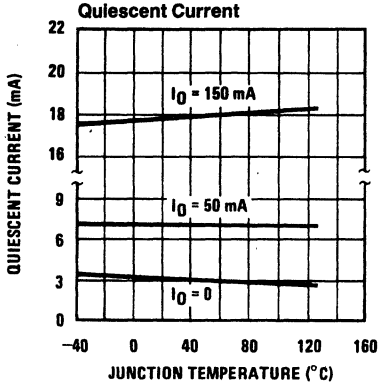
Peak Output Current



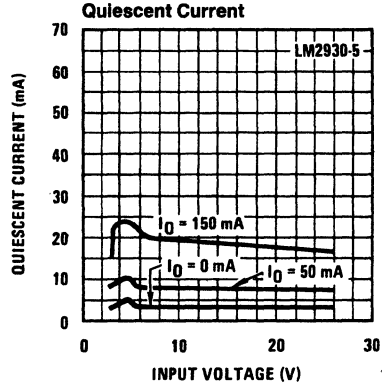
Quiescent Current



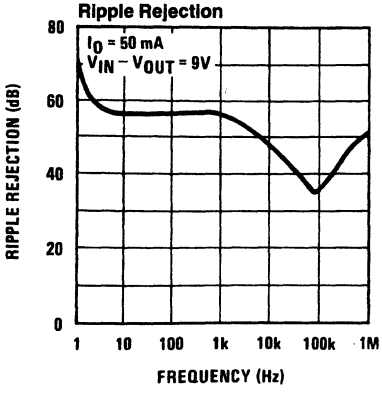
Quiescent Current



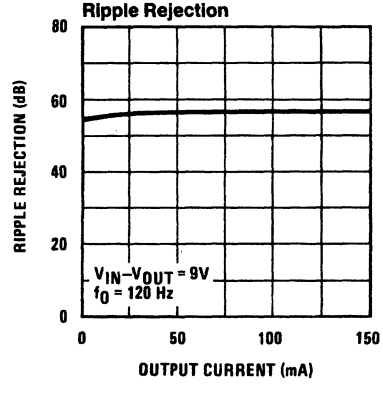
Quiescent Current



Ripple Rejection



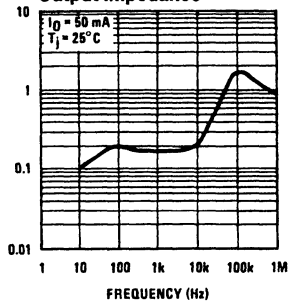
Ripple Rejection



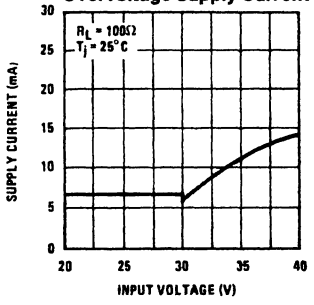
TL/H/5539–3

Typical Performance Characteristics (Continued)

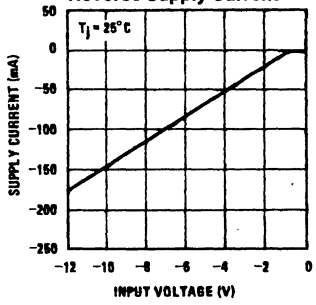
Output Impedance



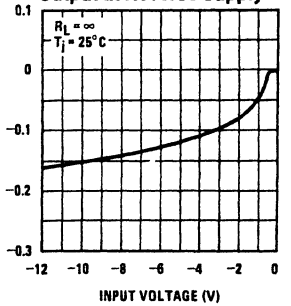
Overvoltage Supply Current



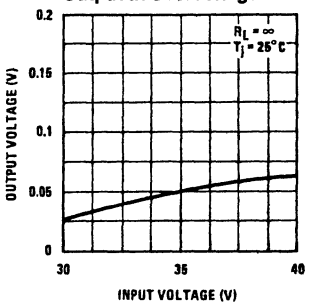
Reverse Supply Current



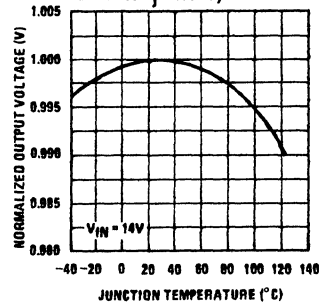
Output at Reverse Supply



Output at Overvoltage

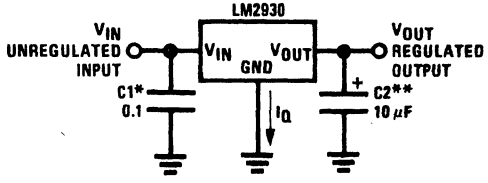


Output Voltage (Normalized to 1V at T_j = 25°C)



TL/H/5539–4

Typical Application



TL/H/5539–5

*Required if regulator is located far from power supply filter.

**C2 may be either an Aluminum or Tantalum type capacitor but must be rated to operate at −40°C to guarantee regulator stability to that temperature extreme. 10 μF is the minimum value required for stability and may be increased without bound. Locate as close as possible to the regulation.

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

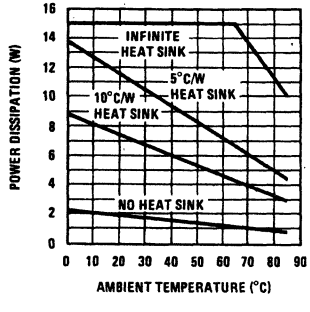
Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Maximum Average Power Dissipation



TL/H/5539–6

National Semiconductor

LM2931 Series Low Dropout Regulators

General Description

The LM2931 positive voltage regulator features a very low quiescent current of 1 mA or less when supplying 10 mA loads. This unique characteristic and the extremely low input-output differential required for proper regulation (0.2V for output currents of 10 mA) make the LM2931 the ideal regulator for standby power systems. Applications include memory standby circuits, CMOS and other low power processor power supplies as well as systems demanding as much as 150 mA of output current.

Designed primarily for automotive applications, the LM2931 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2931 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Fixed output of 5V is available in the plastic TO-220 power package or the popular TO-92 package. An adjustable output version, with on/off switch, is available in a 5-lead TO-220 package.

Features

- Very low quiescent current
- Output current in excess of 150 mA
- Input-output differential less than 0.6V
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Mirror-image insertion protection
- Available in plastic TO-220 or TO-92
- Available as adjustable with TTL compatible switch

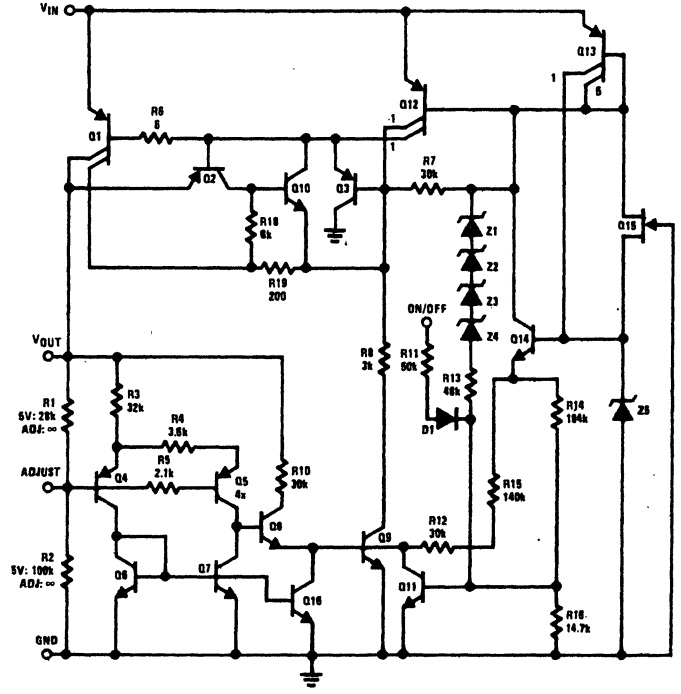
Output Voltage Options

LM2931T-5.0	5V	LM2931AT-5.0	5V
LM2931AT-5.0	5V	LM2931AZ-5.0	5V
LM2931CT	Adjustable		

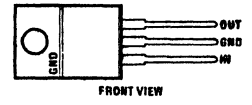
(Contact factory for other fixed output options.)

S 3

Schematic and Connection Diagrams

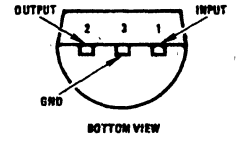


TO-220 3-Lead

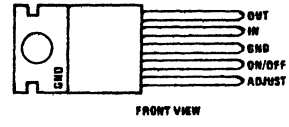


Order Number LM2931
See NS Package T03B, Z03A, T05A

TO-92



TO-220 5-Lead



TL/H/5254–1

Absolute Maximum Ratings

Input Voltage	26V	Internal Power Dissipation (Note 1)	Internally Limited
Operating Range		Operating Temperature Range	−40°C to +85°C
Overvoltage Protection		Maximum Junction Temperature	125°C
LM2931A, LM2931CT Adjustable	60V	Storage Temperature Range	−65°C to +150°C
LM2931	50V	Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics for 5V (V_{IN} = 14V, I_O = 10 mA, T_j = 25°C unless otherwise specified)

Parameter	Conditions	LM2931A-5.0			LM2931-5.0			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	6.0V ≤ V_{IN} ≤ 26V, I_O ≤ 150 mA, T_j = 25°C	4.75	5	5.25	4.5	5	5.5	V
Line Regulation	9V ≤ V_{IN} ≤ 16V 6V ≤ V_{IN} ≤ 26V		2 4	10 30		2 4	10 30	mV mV
Load Regulation	5 mA ≤ I_O ≤ 150 mA		14	50		14	50	mV
Output Impedance	100 mA_{DC} and 10 mArms, 100 Hz-10 kHz		200			200		mΩ
Quiescent Current	I_O ≤ 10 mA, 6V ≤ V_{IN} ≤ 26V, T_j = 25°C I_O = 150 mA, V_{IN} = 14V, T_j = 25°C		0.4 15	1		0.4 15	1	mA mA
Output Noise Voltage	10 Hz-100 kHz		500			500		μVrms
Long Term Stability			20			20		mV/1000 hr
Ripple Rejection	f_o = 120 Hz		80			80		dB
Dropout Voltage	I_O = 10 mA I_O = 150 mA		0.05 0.3	0.2 0.6		0.05 0.3	0.2 0.6	V V
Maximum Operational Input Voltage		26	33		26	33		V
Maximum Line Transient	R_L = 500Ω, V_O ≤ 5.5V, 100 ms	60	70		50	70		V
Reverse Polarity Input Voltage, DC	V_O ≥ −0.3V	−15	−30		−15	−30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ ≤ 100 ms	−50	−80		−50	−80		V

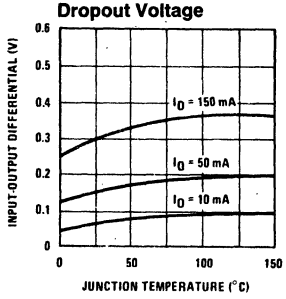
Electrical Characteristics for Adjustable

($V_{IN} \geq V_{OUT} + 0.6V$, $I_O = 10$ mA, $T_j = 25°C$ unless otherwise specified)

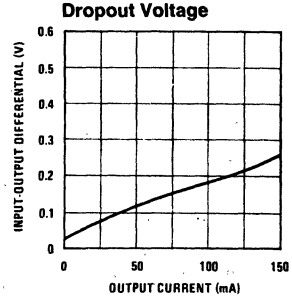
Parameter	Conditions	LM2931CT			Units
		Min	Typ	Max	
Reference Voltage	$I_O \leq 100$ mA, $T_j = 25°C$, R1 = 27k Measured from V_{OUT} to Adjust Pin, $V_O = 3V$	1.08	1.20	1.32	V
Output Voltage Range	R1 = 27k	3		23	V
Line Regulation	$V_{OUT} + 0.6V \leq V_{IN} \leq 26V$		0.2	1.5	mV/V
Load Regulation	$5\text{ mA} \leq I_O \leq 100$ mA		0.3	1	%
Output Impedance	100 mA_{DC} and 10 mArms, 100 Hz-10 kHz		40		mΩ/V
Quiescent Current	$I_O = 10$ mA, $T_j = 25°C$ $I_O = 150$ mA During Shutdown $R_L = 500\Omega$		0.4 15 0.8	1 1	mA mA mA
Output Noise Voltage	10 Hz-100 kHz		100		μVrms/V
Long Term Stability			0.4		%/1000 hr
Ripple Rejection	$f_o = 120$ Hz		0.002		%/V
Dropout Voltage	$I_O = 10$ mA $I_O = 100$ mA		0.05 0.3	0.2 0.6	V V
Maximum Operational Input Voltage		26	33		V
Maximum Line Transient	$I_O = 10$ mA, Reference Voltage ≤ 1.5V	60	70		V
Reverse Polarity Input Voltage, DC	$V_O \geq -0.3V$	−15	−30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, $\tau \leq 100$ ms	−50	−80		V
On/Off Threshold Voltage On Off	$T_j = 25°C$, $V_O = 3V$	 3.25	 2.0 2.2	 1.2 	 V V
On/Off Threshold Current			20	50	μA

Typical Performance Characteristics

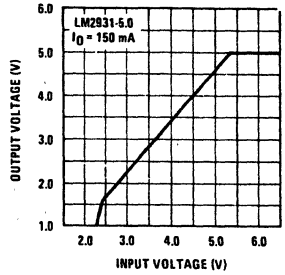
Dropout Voltage



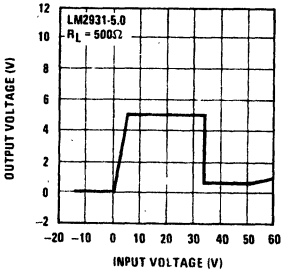
Dropout Voltage



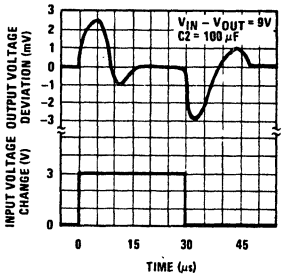
Low Voltage Behavior



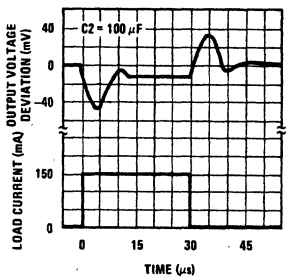
Output at Voltage Extremes



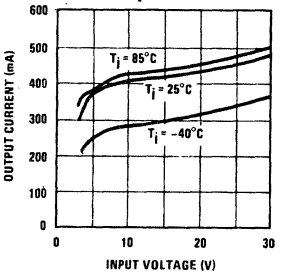
Line Transient Response



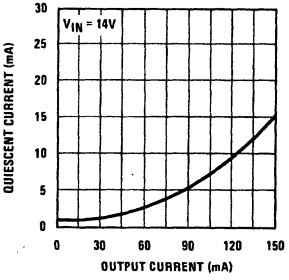
Load Transient Response



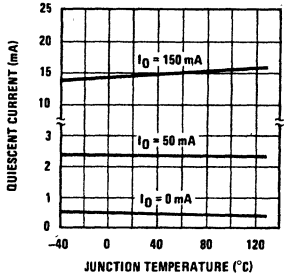
Peak Output Current



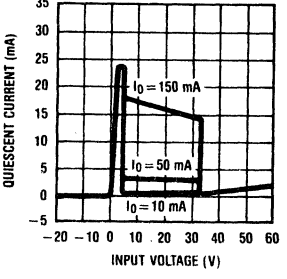
Quiescent Current



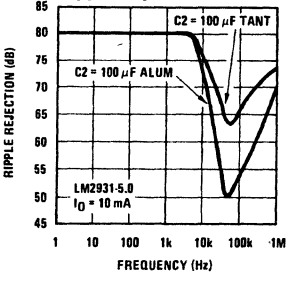
Quiescent Current



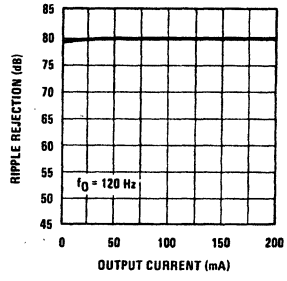
Quiescent Current



Ripple Rejection



Ripple Rejection



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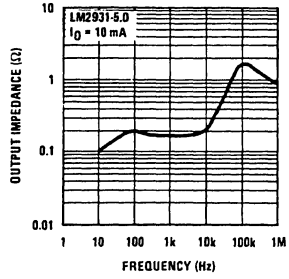
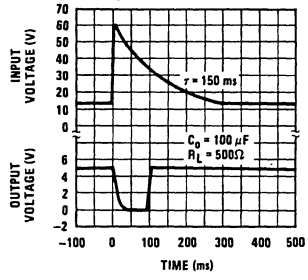
Typical Performance Characteristics (Continued)

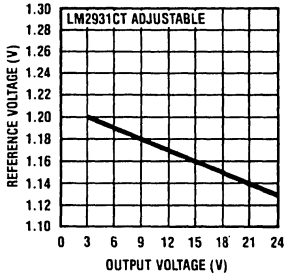
Output Impedance



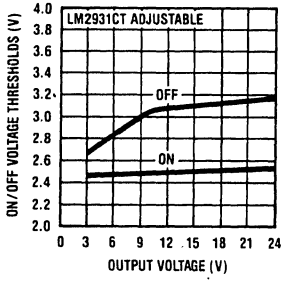
Operation During Load Dump



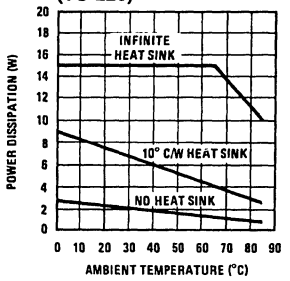
Reference Voltage



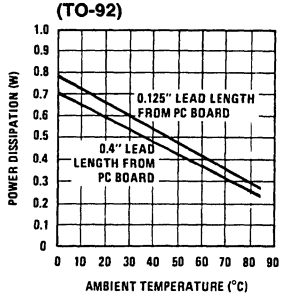
On/Off Threshold



Maximum Power Dissipation (TO-220)



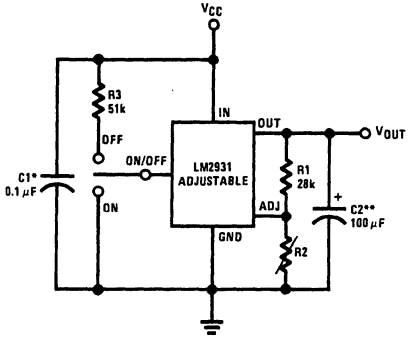
Maximum Power Dissipation (TO-92)



TL/H/5254–3

Typical Applications

LM2931 Adjustable



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$$V_{OUT} = \text{Reference Voltage} \times \frac{R1 + R2}{R1}$$

Note: Using 28k for R1 will automatically compensate for errors in V_{OUT} due to the input bias current of the ADJ pin (approximately 1 μA).

*Required if regulator is located far from power supply filter.

**C2 may be either an Aluminum or Tantalum type capacitor but must be rated to operate at −40°C to guarantee regulator stability to that temperature extreme. 100μF is the minimum value required for stability and may be increased without bound. Locate as close as possible to the regulator.

Application Hints

One of the distinguishing factors of the LM2931 series regulators is the necessity of the output capacitor required for device stability. The value required varies greatly depending upon the application circuit and other factors. Thus some comments on the characteristics of both capacitors and the regulator are in order.

High frequency characteristics of electrolytic capacitors depend greatly on the type and even the manufacturer. As a result, a value of capacitance that works well with the LM2931 for one brand or type may not necessary be sufficient with an electrolytic of different origin. Sometimes actual bench testing, as described later, will be the only means to determine the proper capacitor and value. Experience has shown that, as a rule of thumb, the more expensive and higher quality electrolytics generally require a smaller value for regulator stability. As an example, while a quality 100 μF aluminum electrolytic covers all general application circuits, similar stability can be obtained with a tantalum electrolytic of only 47 μF. This factor of two can generally be applied to any special application circuits also.

Another critical characteristic of electrolytics is their performance over temperature. While the LM2931 is designed to operate to $-40°C$, the same is not always true with all electrolytics (hot is generally not a problem). The electrolyte in many aluminum types will freeze around $-30°C$, reducing their effective value to zero. Since the capacitance is needed for regulator stability, the natural result is oscillation (and lots of it) at the regulator output. For all application circuits where cold operation is necessary, the output capacitor must be rated to operate at the minimum temperature. By coincidence, worst-case stability for the LM2931 also occurs at minimum temperatures. As a result, in applications where the regulator junction temperature will never be less than 25°C, the output capacitor can be reduced approximately by a factor of two over the value needed for the entire temperature range. To continue our example with the tantalum electrolytic, a value of only 22 μF would probably thus suffice. For quality aluminum, 47 μF would be adequate in such an application.

Another regulator characteristic that is noteworthy is that stability decreases with higher output currents. This sensible fact has important connotations. In many applications, the LM2931 is operated at only a few milliamps of output current or less. In such a circuit, the output capacitor can be further reduced in value. As a rough estimation, a circuit that is required to deliver a maximum of 10 mA of output current from the regulator would need an output capacitor of only half the value compared to the same regulator required to deliver the full output current of 150 mA. If the example of the tantalum capacitor in the circuit rated at 25°C junction temperature and above were continued to include a maximum of 10 mA of output current, then the 22 μF output capacitor could be reduced to only 10 μF.

In the case of the LM2931CT adjustable regulator, the minimum value of output capacitance is a function of the output voltage. As a general rule, the value decreases with higher output voltages, since internal loop gain is reduced.

At this point, the procedure for bench testing the minimum value of an output capacitor in a special application circuit should be clear. Since worst-case occurs at minimum operating temperatures and maximum operating currents, the entire circuit, including the electrolytic, should be cooled to the minimum temperature. The input voltage to the regulator should be maintained at 0.6V above the output to keep internal power dissipation and die heating to a minimum. Worst-case occurs just after input power is applied and before the die has had a chance to heat up. Once the minimum value of capacitance has been found for the brand and type of electrolytic in question, the value should be doubled for actual use to account for production variations both in the capacitor and the regulator. (All the values in this section and the remainder of the data sheet were determined in this fashion.)

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

National Semiconductor

LM2935 Low Dropout Dual Regulator

General Description

The LM2935 positive voltage regulator features a low quiescent current of 3 mA or less when supplying 10 mA loads from the standby regulator output. This unique characteristic and the extremely low input-output differential required for proper regulation (0.55V for output currents of 10 mA) make the LM2935 the ideal regulator for power systems that include standby memory. Applications include processor power supplies demanding as much as 750 mA of output current.

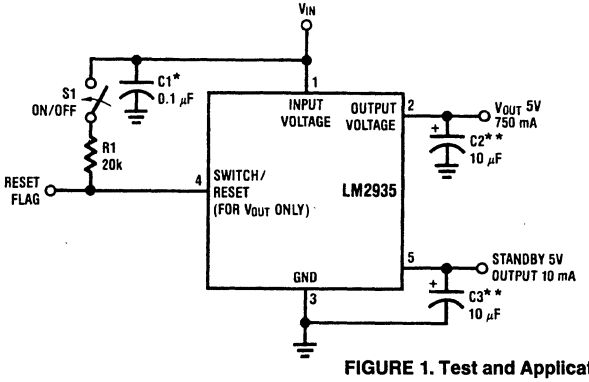
Designed primarily for automotive applications, the LM2935 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the 0.75A regulator will automatically shut down to protect both internal circuits and the load while the standby regulator will continue to power any standby load. The LM2935 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Fixed outputs of 5V are available in the plastic TO-220 power package.

Features

- Two regulated outputs
- Output current in excess of 750 mA
- Low quiescent current standby regulator
- Input-output differential less than 0.6V at 0.5A
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Available in plastic TO-220
- ON/OFF switch for high current output
- Reset error flag
- 100% electrical burn-in

Typical Application Circuit



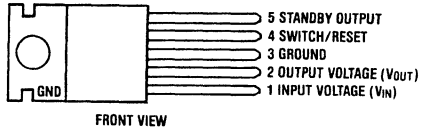
*Required if regulator is located far from power supply filter.

**Required for stability. May be increased without bound. Capacitor must be rated to operate at the minimum temperature expected for the regulator system.

FIGURE 1. Test and Application Circuit

Connection Diagram

TO-220 5-Lead



FRONT VIEW

TL/H/5232–1

Order Number LM2935T

See NS Package Number T05A

Absolute Maximum Ratings

Input Voltage		Operating Temperature Range	−40°C to + 125°C
Operating Range	26V	Maximum Junction Temperature	150°C
Overvoltage Protection	60V	Storage Temperature Range	−65°C to + 150°C
Internal Power Dissipation (Note 1)	Internally Limited	Lead Temp. (Soldering, 10 seconds)	230°C

Electrical Characteristics FOR V_{OUT} (V_{IN} = 14V, I_O = 500 mA, T_j = 25°C unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	6V≤V_{IN}≤26V, I_O≤500 mA, T_j=25°C	4.75	5.00	5.25	V
Line Regulation	9V≤V_{IN}≤16V, I_O=5 mA 6V≤V_{IN}≤26V, I_O=5 mA		4 10	25 50	mV mV
Load Regulation	5 mA≤I_O≤500 mA		10	50	mV
Output Impedance	500 mA_{DC} and 10 mArms, 100 Hz-10 kHz		200		mΩ
Output Impedance	500 mA_{DC} and 10 mArms, 100 Hz-10 kHz		200		mΩ
Quiescent Current	I_O≤10 mA, No Load on Standby I_O=500 mA, No Load on Standby I_O=750 mA, No Load on Standby		3 55 120	 100	mA mA mA
Output Noise Voltage	10 Hz-100 kHz		100		μVrms
Long Term Stability			20		mV/1000 hr
Ripple Rejection	f_o=120 Hz		66		dB
Dropout Voltage	I_O=500 mA I_O=750 mA		0.45 0.82	0.6	V V
Current Limit		0.75	1.4		A
Maximum Operational Input Voltage		26	31		V
Maximum Line Transient	V_O≤5.5V	60	70		V
Reverse Polarity Input Voltage, DC	V_O−0.6V, 10Ω Load	−15	−30		V
Reverse Polarity Input Voltage, Transient	1% Duty Cycle, τ≤100 ms, V_O≥−6V, 10Ω Load	−50	−80		V
Reset Output Voltage Low High	 R1=20k, V_{IN}=4.5V R1=20k, V_{IN}=14V	 4.5	 0.8 5.0	 1 5.5	 V V
Reset Output Current	V_{IN}=4.5V, Reset in Low State		5		mA
ON/OFF Resistor	R1 (± 10% Tolerance)		20	30	kΩ

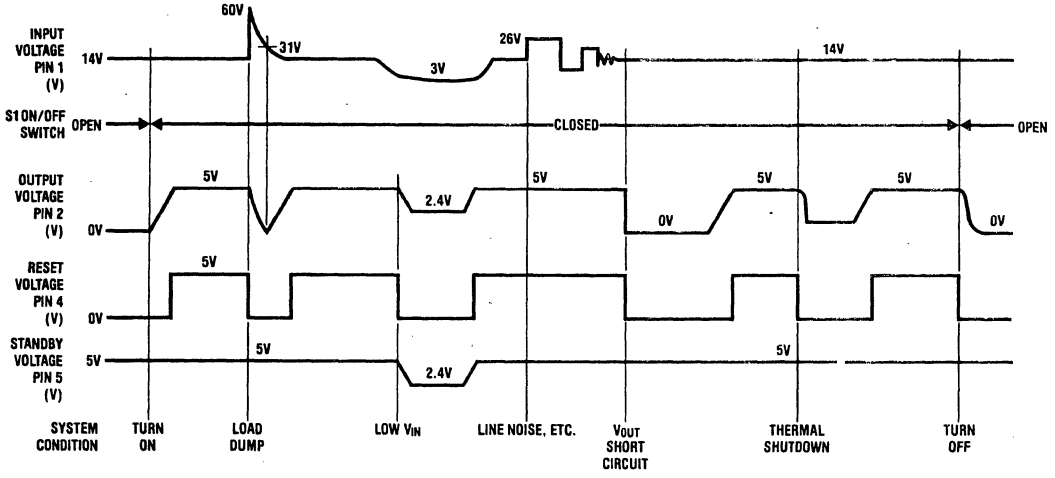
Note 1: Thermal resistance without a heat sink for junction to case temperature is 4°C/W(TO-220). Thermal resistance for TO-220 case to ambient temperature is 50° C/W.

Electrical Characteristics FOR STANDBY OUTPUT (Continued)

(V_{IN} = 14V, I_O = 10 mA, T_j = 25°C unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	$I_O \leq 10$ mA, $T_j = 25°C$, $6V \leq V_{IN} \leq 26V$ (Note 2)	4.75	5.0	5.25	V
Tracking	V_{OUT}–Standby Output Voltage		50	200	mV
Line Regulation	$6V \leq V_{IN} \leq 26V$		4	50	mV
Load Regulation	$1\ mA \leq I_O \leq 10$ mA		10	50	mV
Output Impedance	10 mA_{DC} and 1 mArms, 100 Hz-10 kHz		1		Ω
Quiescent Current	$I_O \leq 10$ mA, $T_j = 25°C$ V_{OUT}OFF		2	3	mA
Output Noise Voltage	10 Hz–100 kHz		300		μV
Long Term Stability			20		mV/1000 hr
Ripple Rejection	$f_o = 120$ Hz		66		dB
Dropout Voltage	$I_O \leq 10$ mA		0.55	0.7	V
Current Limit		25	70		mA
Maximum Operational Input Voltage	$4.5V \leq V_O \leq 6V$	60	70		V
Reverse Polarity Input Voltage, DC	$V_O \geq -0.3V$, 510Ω Load	−15	−30		V
Reverse Polarity Input	1% Duty Cycle, $\tau \geq 100$ ms, $V_O \leq -6V$	−50	−80		V
Voltage, Transient	500Ω Load				

Typical Circuit Waveforms

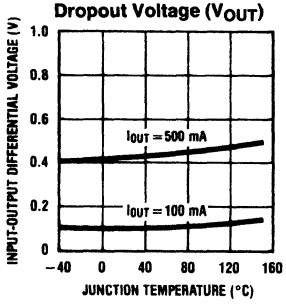


TL/H/5232–2

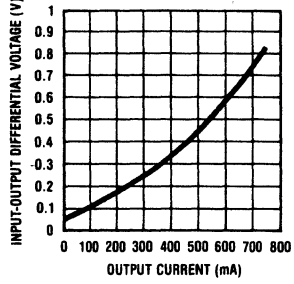
FIGURE 2.

Typical Performance Characteristics

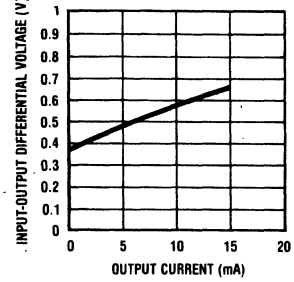
Dropout Voltage (V_{OUT})



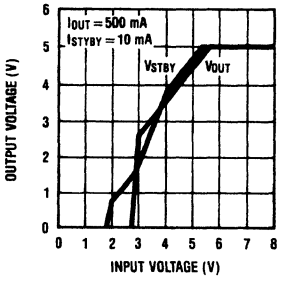
Dropout Voltage (V_{OUT})



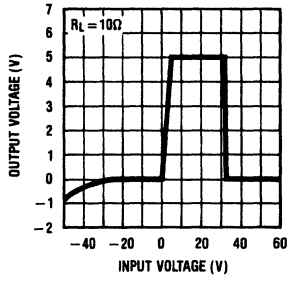
Dropout Voltage (V_{STBY})



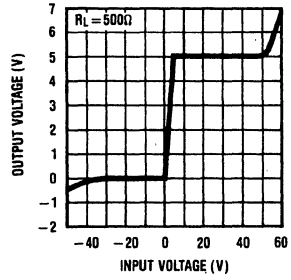
Low Voltage Behavior



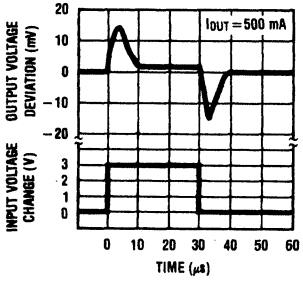
Output Voltage (V_{OUT})



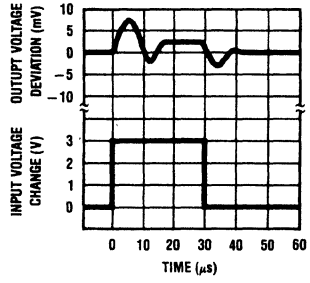
Output Voltage (V_{STBY})



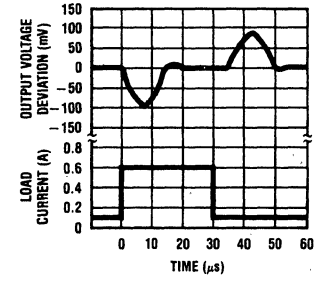
Line Transient Response (V_{OUT})



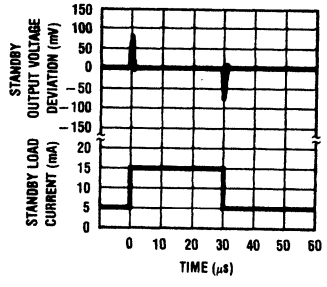
Line Transient Response (V_{STBY})



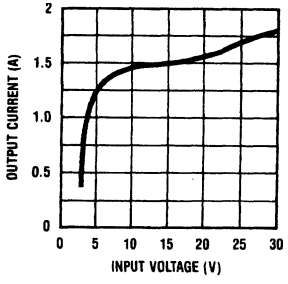
Load Transient Response (V_{OUT})



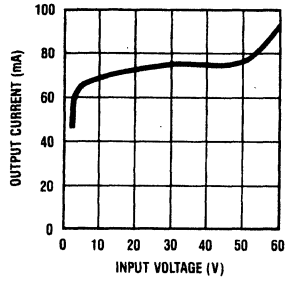
Load Transient Response (V_{STBY})



Peak Output Current (V_{OUT})



Peak Output Current (V_{STBY})



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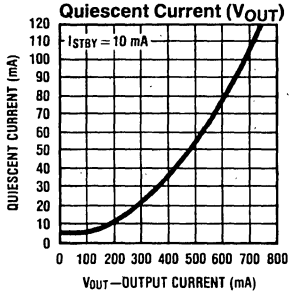
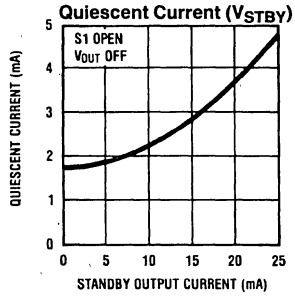
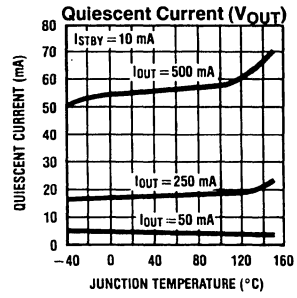
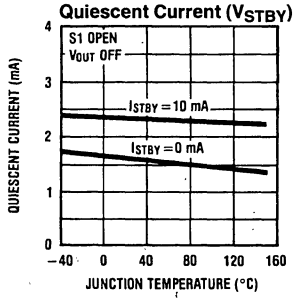
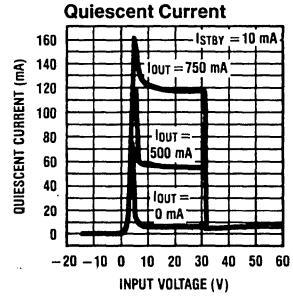
Typical Performance Characteristics (Continued)

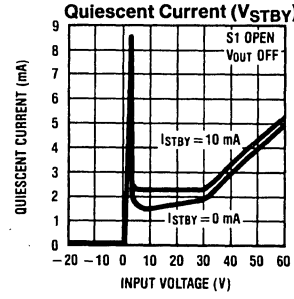


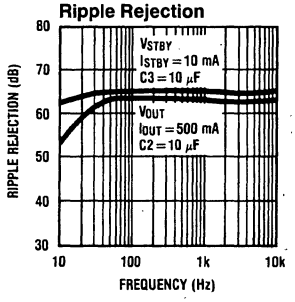


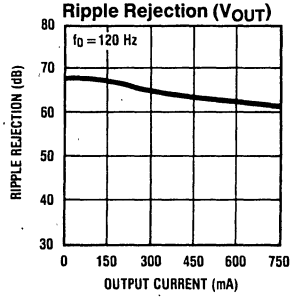


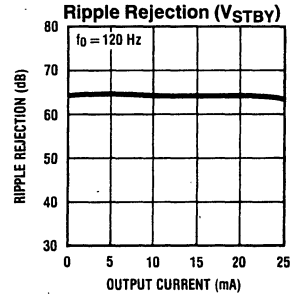


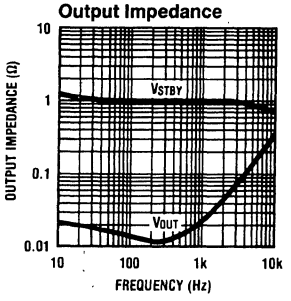


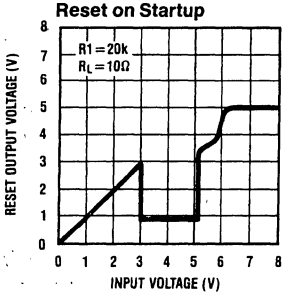


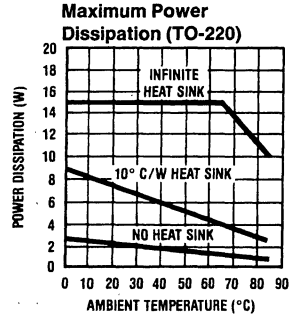












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Circuit Schematic

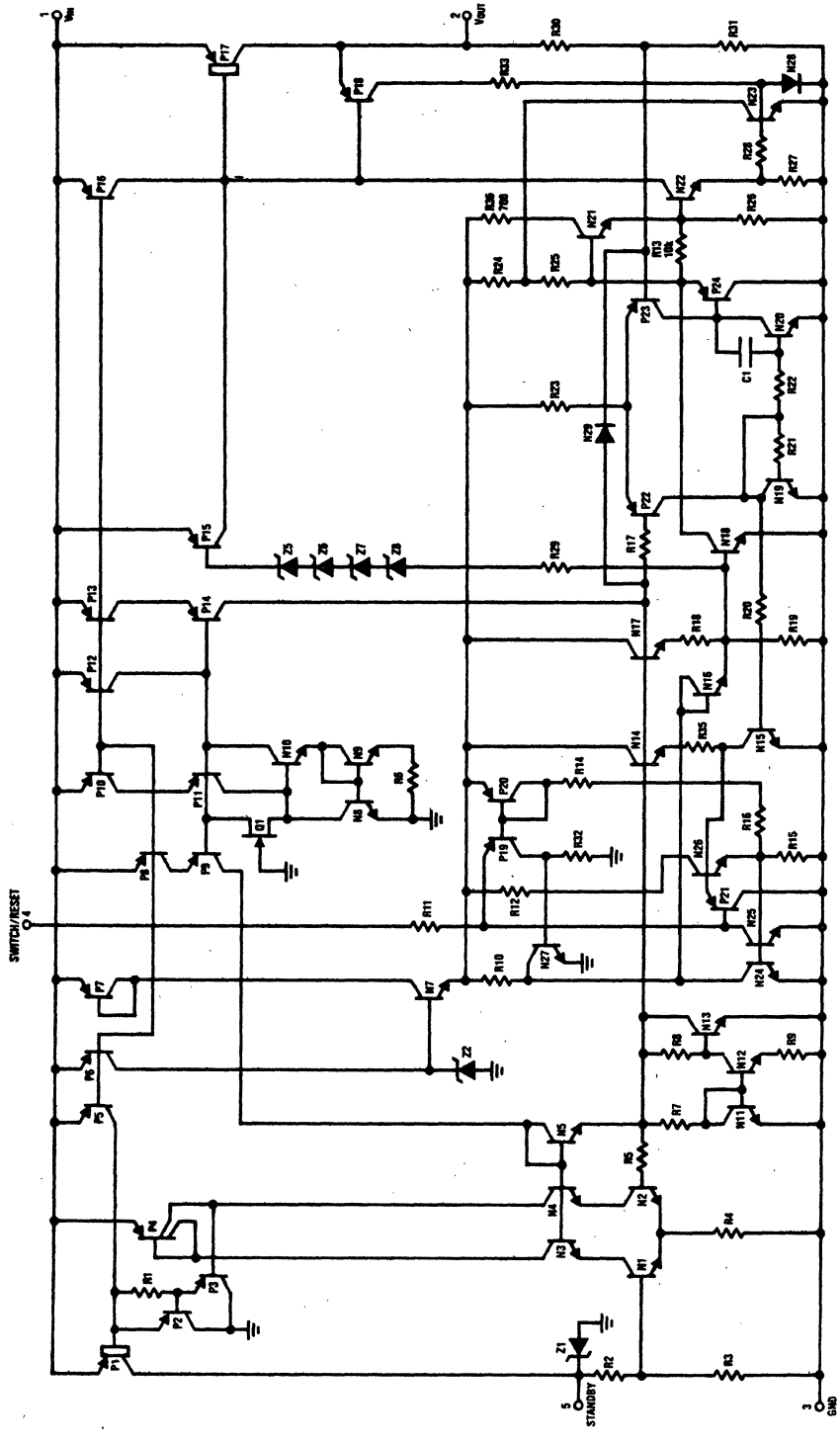

FIGURE 3.

TL/H/5232–5

Definition of Terms

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at 14V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Application Hints

EXTERNAL CAPACITORS

The LM2935 output capacitors are required for stability. Without them, the regulator outputs will oscillate, sometimes by many volts. Though the 10μF shown are the minimum recommended values, actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) also factors in the IC stability. Since ESR varies from one brand to the next, some bench work may be required to determine the minimum capacitor value to use in production. Worst-case is usually determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. Many aluminum type electrolytics will freeze at temperatures less than −30°C, reducing their effective capacitance to zero. To maintain regulator stability down to −40°C, capacitors rated at that temperature (such as tantalums) must be used.

No capacitor must be attached to the ON/OFF and ERROR FLAG pin. Due to the internal circuits of the IC, oscillation on this pin could result.

STANDBY OUTPUT

The LM2935 differs from most fixed voltage regulators in that it is equipped with two regulator outputs instead of one. The additional output is intended for use in systems requiring standby memory circuits. While the high current regulator output can be controlled with the ON/OFF pin described below, the standby output remains on under all conditions as long as sufficient input voltage is applied to the IC. Thus, memory and other circuits powered by this output remain unaffected by positive line transients, thermal shutdown, etc.

The standby regulator circuit is designed so that the quiescent current to the IC is very low (<3 mA) when the other regulator output is off.

In applications where the standby output is not needed, it may be disabled by connecting a resistor from the standby output to the supply voltage. This eliminates the need for a more expensive capacitor on the output to prevent unwanted oscillations. The value of the resistor depends upon the minimum input voltage expected for a given system. Since the standby output is shunted with an internal 5.7V zener (*Figure 3*), the current through the external resistor should be sufficient to bias R2 and R3 up to this point. Approximately 60 μA will suffice, resulting in a 10k external resistor for most applications (*Figure 4*).

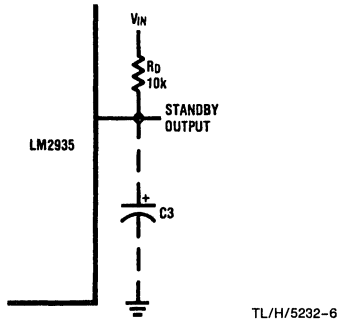

FIGURE 4. Disabling Standby Output to Eliminate C3

HIGH CURRENT OUTPUT

Unlike the standby regulated output, which must remain on whenever possible, the high current regulated output is fault protected against overvoltage and also incorporates thermal shutdown. If the input voltage rises above approximately 30V (e.g., load dump), this output will automatically shutdown. This protects the internal circuitry and enables the IC to survive higher voltage transients than would otherwise be expected. Thermal shutdown is effective against die overheating since the high current output is the dominant source of power dissipation in the IC.

ON/OFF AND ERROR FLAG PIN

This pin has the ability to serve a dual purpose if desired. When controlled in the manner shown in *Figure 1* (common in automotive systems where S1 is the ignition switch), the pin also serves as an output flag that is active low whenever a fault condition is detected with the high current regulated output. In other words, under normal operating conditions, the output voltage of this pin is high (5V). This is set by an internal clamp. If the high current

Application Hints (Continued)

output becomes unregulated for any reason (line transients, short circuit, thermal shutdown, low input voltage, etc.) the pin switches to the active low state, and is capable of sinking several milliamps. This output signal can be used to initiate any reset or start-up procedure that may be required of the system.

The ON/OFF pin can also be driven directly from logic circuits. The only requirement is that the 20k pull-up resistor remain in place *(Figure 5)*. This will not affect the logic gate since the voltage on this pin is limited by the internal clamp in the LM2935 to 5V. The error flag is sacrificed in this arrangement since the maximum sink capability of the pin in the active low state (approximately 5 mA) is usually not sufficient to pull down the active high logic gate. Of course, the flag can be retained if the driving gate is open collector logic.

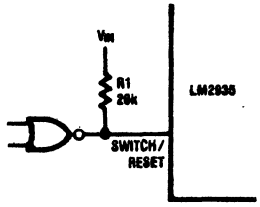

FIGURE 5. Controlling ON/OFF Terminal with a Typical CMOS or TTL Logic Gate

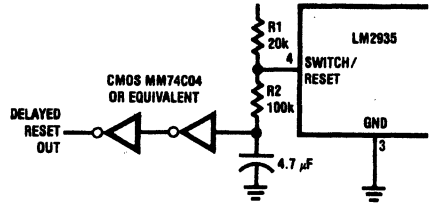

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FIGURE 6. Reset Pulse on Power-Up (with approximately 300 ms delay)

Section 4

Voltage References

Voltage References

Section Contents

National Semiconductor

PRELIMINARY

LM168/LM268/LM368 Precision Voltage Reference

General Description

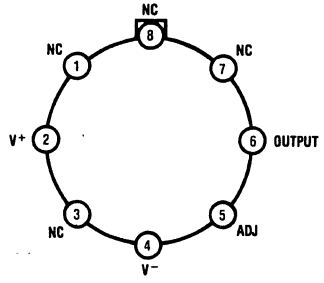
The LM168/LM368 are precision, monolithic, temperature-compensated voltage references. The LM168 makes use of thin-film technology enhanced by the discrete laser trimming of resistors to achieve excellent Temperature coefficient (Tempco) of V_{OUT} (as low as 5ppm/°C), along with tight initial tolerance, (as low as 0.02%). The trim scheme is such that individual resistors are cut open rather than being trimmed (partially cut), to avoid resistor drift caused by electromigration in the trimmed area. The LM168 also provides excellent stability vs. changes in input voltage and output current (both sourcing and sinking). This device is available in several output voltage options including 5.0V, 6.2V, and 10.0V and will operate in both series or shunt mode. The devices are short circuit proof when sourcing current. A trim pin is made available for fine trimming of V_{OUT} or for obtaining intermediate values without greatly affecting the Tempco of the device.

Features

- 300 μA operating current
- Low output impedance
- Excellent line regulation (.0001%/V typical)
- Single-supply operation
- Externally trimmable
- Low temperature coefficient
- Operates in series or shunt mode
- 10.0, 6.2, or 5.0 volts
- Excellent initial accuracy (0.02% typical)
- Replaces 1N821-1N827 zeners

Connection Diagram

Metal Can Package



TL/H/5522–1

Top View

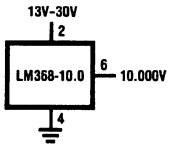
*case connected to V−

Order Number LM168BYH-10, LM168BYH-6.2, LM168BYH-5.0, LM268BYH-10, LM268BYH-6.2, LM268BYH-5.0, LM368YH-10, LM368YH-6.2, LM368YH-5.0, LM368H-10, LM368H-6.2, LM368H-5.0

See NS Package Number H08C

Typical Applications

Series Regulator



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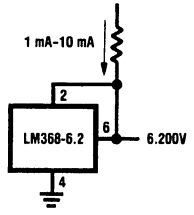
Shunt Regulator



TL/H/5522–3

(Replaces 1N827-type Zener)

Absolute Maximum Ratings

Input Voltage (Series Mode)	35V	Operating Temperature Range	
Reverse Current (Shunt Mode)	50 mA	LM168	−55°C to +125°C
Power Dissipation	600 mW	LM268	−40°C to +85°C
Storage Temperature Range	−60°C to +150°C	LM368	0°C to +70°C
		Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	LM168/LM268/LM368			
		Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Max. unless noted)
V_{OUT} Error: LM168B, LM268B		±0.02	±0.05		%
LM368		±0.02	±0.1		%
Line Regulation	$(V_{OUT} + 3V) \le V_{IN} \le 30V$	±0.0001	±0.0005		%/V
Load Regulation	$0\ mA \le I_{SOURCE} \le 10\ mA$	±0.0003	±0.001		%/mA
(Note 4)	$-10\ mA \le I_{SINK} \le 0\ mA$	±0.003	±0.008		%/mA
Thermal Regulation	T=20 mS (Note 5)	±0.005	±0.01		%/100 mW
Quiescent Current		250	350		μA
Change of Quiescent Current vs. V_{IN}	$(V_{OUT} + 3V) \le V_{IN} \le 30V$	3	5		μA/V
Temperature Coefficient of V_{OUT} (see graph): LM168BY	$-55°C \le T_A \le 125°C$	±5	±10		ppm/°C
(Note 6) LM268BY	$-40°C \le T_A \le 85°C$	±7.5	±15		ppm/°C
LM368Y	$0°C \le T_A \le 70°C$	±11	±20		ppm/°C
LM368	$0°C \le T_A \le 70°C$	±15		±30	ppm/°C
Short Circuit Current	$V_{OUT} = 0$	30	70	100	mA
Noise: 10.0V: 0.1 - 10Hz		30			uVp-p
100Hz - 10 kHz		1100			$nV/\sqrt{Hz}$
6.2V: 0.1 - 10Hz		20			uVp-p
100Hz - 10 kHz		700			$nV/\sqrt{Hz}$
5.0V: 0.1 - 10Hz		16			uVp-p
100Hz - 10 kHz		575			$nV/\sqrt{Hz}$
V_{OUT} Adjust Range: 10.000V	R_{TRIM} = 100k	4.5-17.0		6.0-15.5	V min.
6.200V		4.0-9.5		5.0-8.5	V min.
5.000V		3.5-7.0		4.0-6.0	V min.

Note 1: Unless otherwise noted, these specifications apply: T_A = 25°C, V_{IN} = 15V, I_{LOAD} = 0, Circuit is operating in Series Mode.

Note 2: Tested Limits are guaranteed and 100% tested in production.

Note 3: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

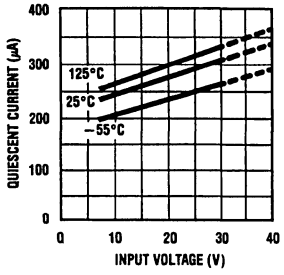
Note 4: The LM168 has a Class B output, and will exhibit transients at the crossover point. This point occurs when the device is asked to sink approximately 120 μA. In some applications it may be advantageous to preload the output to either V_{IN} or Ground, to avoid this crossover point.

Note 5: Thermal Regulation is defined as the change in the output Voltage at a time T after a step change in power dissipation of 100 mW.

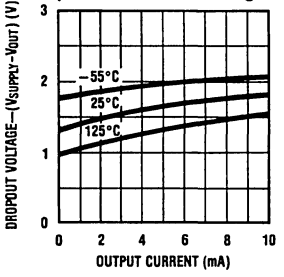
Note 6: Temperature Coefficient of V_{OUT} is defined as the worst case delta-V_{OUT} measured at Specified Temperatures divided by the total span of the Specified Temperature Range (See graphs). There is no guarantee that the Specified Temperatures are exactly at the minimum or maximum deviation.

Typical Performance Characteristics (Note 1)

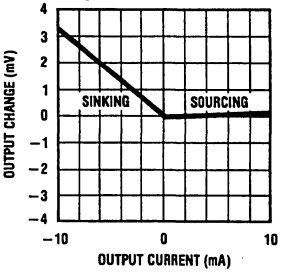
Quiescent Current vs. Input Voltage and Temperature



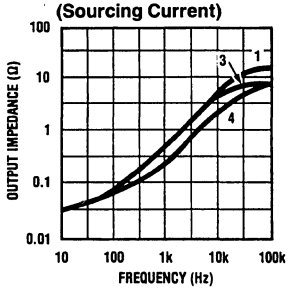
Dropout Voltage vs. Output Current (Series Mode Sourcing Current)



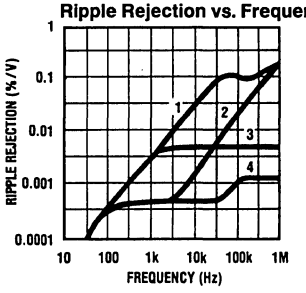
Output Change vs. Output Current



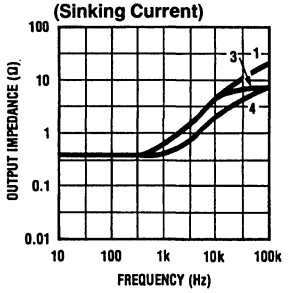
Output Impedance vs. Frequency (Sourcing Current)



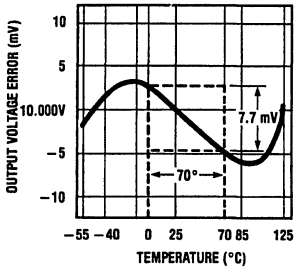
Ripple Rejection vs. Frequency



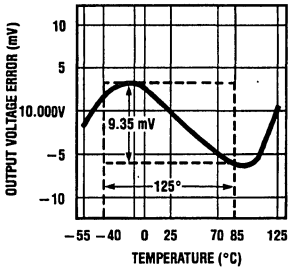
Output Impedance vs. Frequency (Sinking Current)



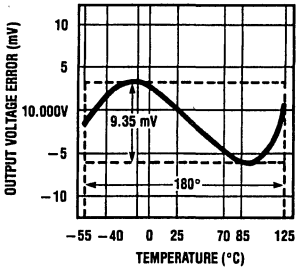
Temperature Coefficient: LM368-10 (Curve A)



Temperature Coefficient: LM268-10 (Curve B)



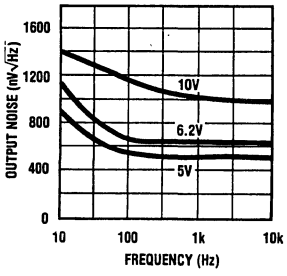
Temperature Coefficient: LM168-10 (Curve C)



TL/H/5522–4

(1) LM368 as is.
(2) with 0.01 μf Mylar, Trim to Gnd.
(3) with 10Ω in series with 10 μf, V_{OUT} to Gnd.
(4) with Both.

Output Noise vs. Frequency



Typical Temperature Coefficient Calculations:

LM368-10 (see Curve A)

T.C. = 7.7 mV/(70° × 10V)
= 11 × 10E-6 = 11ppm/°C

LM268-10 (see Curve B)

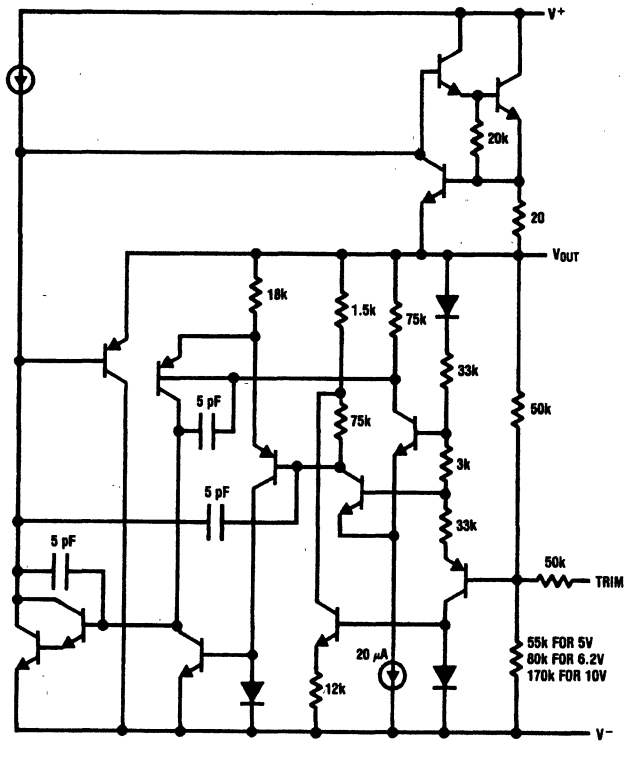
T.C. = 9.35 mV/(125° × 10V)
= 7.5 × 10E-6 = 7.5ppm/°C

LM168-10 (see Curve C)

T.C. = 9.35 mV/(180° × 10V)
= 5.2 × 10E-6 = 5.2ppm/°C

TL/H/5522–5

Simplified Schematic Diagram

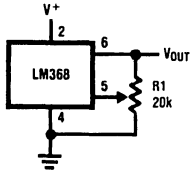


TL/H/5522–6

*Reg. U.S. Pat. Off.

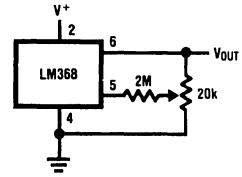
Typical Applications

Wide Range Trimmable Regulator



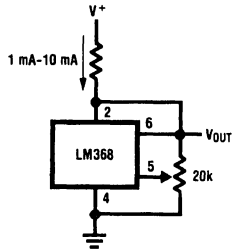
TL/H/5522–7

Narrow Range Trimmable Regulator (±1% min.)



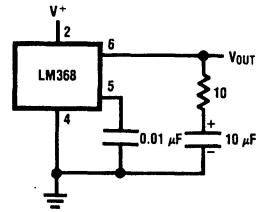
TL/H/5522–8

Adjustable Zener



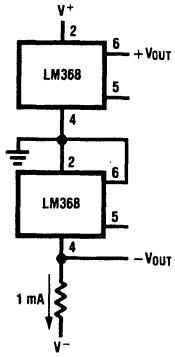
TL/H/5522–9

Improved Noise Performance



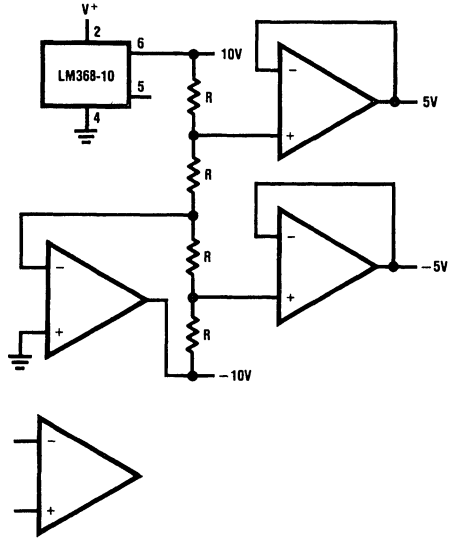
TL/H/5522–10

± Reference



TL/H/5522–11

±10V, ±5V References

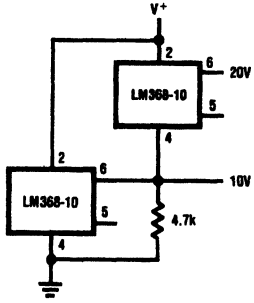


TL/H/5522–12

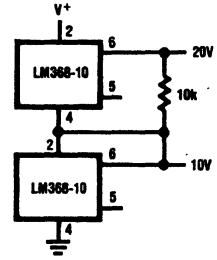
R= Thin Film Resistor Network,
±0.05% Matching and 5ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
or similar.

Typical Applications (Continued)

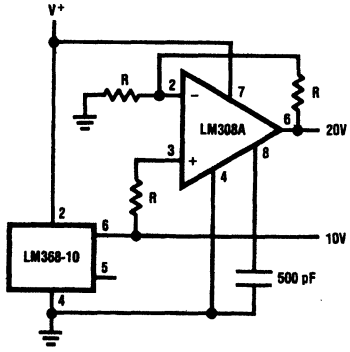
Multiple Output Voltages



TL/H/5522–13



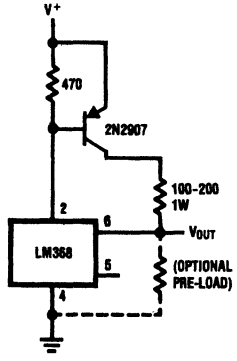
TL/H/5522–14



TL/H/5522–15

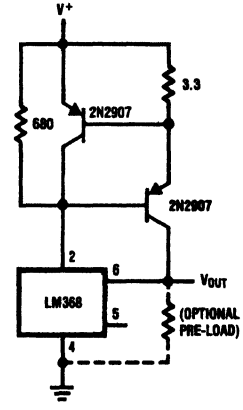
R = Thin Film Resistor Network
0.05% Matching and 5ppm Tracking
(Beckman 694-3-R-10K-A),
(Caddock T-914-10K-100-05)
or similar.

Reference with Booster



TL/H/5522–16

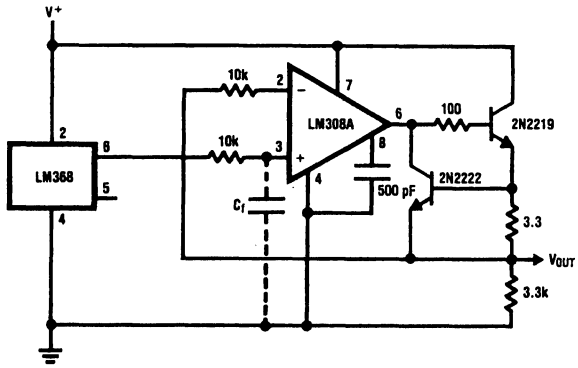
100 mA Boosted Reference



TL/H/5522–17

Typical Applications (Continued)

Buffered High-Current Reference with Filter



TL/H/5522–18

National Semiconductor

PRELIMINARY

LM185/285/385 Adjustable Micropower Voltage Reference

General Description

The LM185/LM285/LM385 are micropower 3-terminal adjustable band-gap voltage reference diodes. Operating from 1.24 to 5.3V and over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185 band-gap reference uses only transistors and resistors, low noise and good long-term stability result.

Careful design of the LM185 has made the device tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

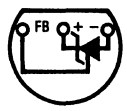
The LM185 is rated for operation over a −55°C to 125°C temperature range, while the LM285 is rated −40°C to 85°C and the LM385 0°C to 70°C. The LM185 is available in a hermetic TO-46 package and the LM285/LM385 are available in a low-cost TO-92 molded package.

Features

- Adjustable from 1.24V to 5.30V
- Operating current of 10 μA to 20 mA
- 1% and 2% initial tolerance
- 1 ohm dynamic impedance
- Low temperature coefficient

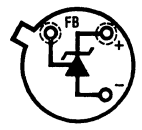
Connection Diagrams

TO-92
Plastic Package



Bottom View

TO-46
Metal Can Package



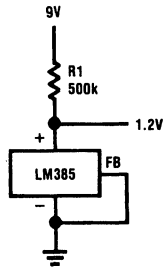
Bottom View

TL/H/5250–1

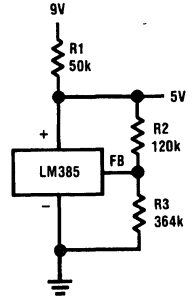
Order Number LM185, LM285 or LM385
See NS Packages H03H and Z03A

Typical Applications

1.2V Reference



5.0V Reference



$$V_{OUT} = 1.24\left(\frac{R3}{R2} + 1\right)$$

TL/H/5250–2

Absolute Maximum Ratings

Reverse Current	30 mA	LM285 Series	−40°C to 85°C
Forward Current	10 mA	LM385 Series	0°C to 70°C
Operating Temperature Range		Storage Temperature	−55°C to 150°C
LM185 Series	−55°C to 125°C	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	LM185BX, LM185BY LM185B, LM285BX LM285BY, LM285			LM385BX, LM385BY LM385			Unit Limit
		Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
Reference Voltage	$I_R = 100\ \mu A$	1.240	1.252 **1.255**		1.240	1.252	**1.255**	V_{max}
	B-Series		1.228 **1.215**			1.228	**1.215**	V_{min}
	LM285 and LM385	1.240	1.265 1.215	**1.270** **1.205**		1.265 1.215	**1.270** **1.205**	V_{max} V_{min}
Reference Voltage Change with Current	$Min < I_R < 1$ mA	0.2	1	**1.5**	0.2	1	**1.5**	mV max
	$1\ mA < I_R < 20$ mA	4	10	**20**	5	15	**25**	mV max
Dynamic Output Impedance	$I_R = 100\ \mu A$, f = 100 Hz $I_{AC} = 0.1\ I_R$ $V_R = V_{REF}$	0.3			0.4			ohm
	$V_R = 5.3V$	0.7			1			ohm
Reference Voltage Change with Output Voltage	$I_R = 100\ \mu A$	1	3	**6**	2	5	**10**	mV max
Feedback Current		13	20	**25**	16	30	**35**	nA max
Minimum Operating Current (see curve)	$V_R = V_{REF}$	6	9	**10**	7	11	**13**	μA min
	$V_R = 5.3V$	30	45	**50**	35	55	**60**	μA min
Output Wideband Noise	$I_R = 100\ \mu A$, 10 Hz < f < 10 kHz $V_{OUT} = V_{REF}$	50			50			μV rms
	$V_{OUT} = 5.3V$	170			170			μV rms
Average Temperature Coefficient (Note 4)	$I_R = 100\ \mu A$ X-Series		**30**			**30**		ppm/°C max
	Y-Series		**50**			**50**		ppm/°C max
	LM185B, LM285 and LM385			**150**			**150**	ppm/°C max
Long Term Stability	$I_R = 100\ \mu A$, T = 1000 hr $T_R = 25°C \pm 0.1°C$	20			20			ppm

Note 1: Parameters identified with **boldface type apply at temperature extremes** and for min < I_R < 20 mA and for V_{REF} < V_{OUT} < 5.3V. All other numbers apply at $T_A = T_j = 25°C$. Thermal resistance of the TO-46 package is 440°C/W junction to ambient and 80°C/W junction to case. Thermal resistance in the TO-92 package is 180°C/W junction to ambient.

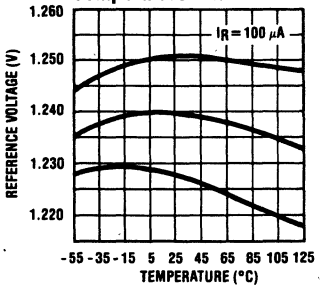
Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not to be used to calculate outgoing quality levels.

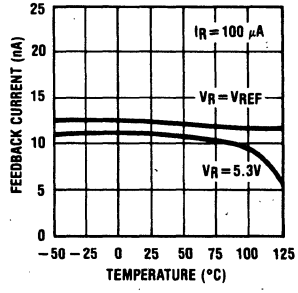
Note 4: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures from T_{min} to T_{max}, divided by $T_{max} - T_{min}$. The measured temperatures are −55, −40, 0, 25, 70, 85, 125°C.

Typical Performance Characteristics

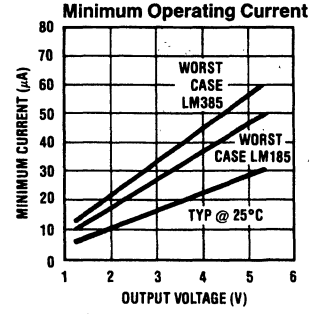
Temperature Drift



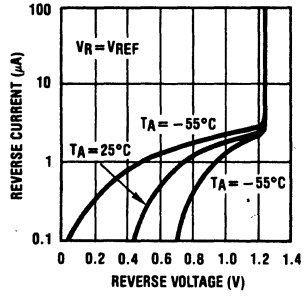
Feedback Current



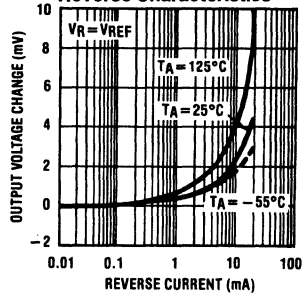
Minimum Operating Current



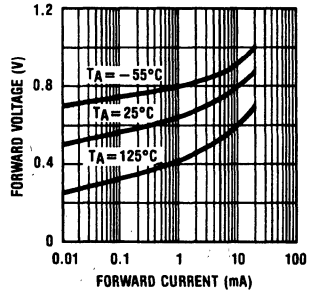
Reverse Characteristics



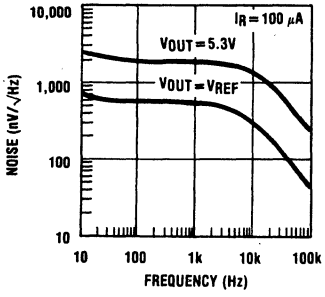
Reverse Characteristics



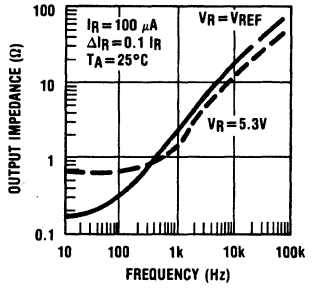
Forward Characteristics



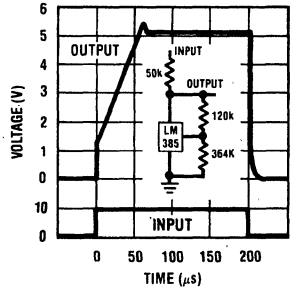
Output Noise Voltage



Dynamic Output Impedance

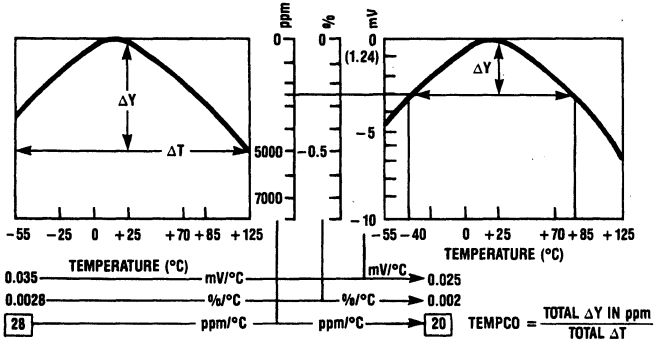


Response Time



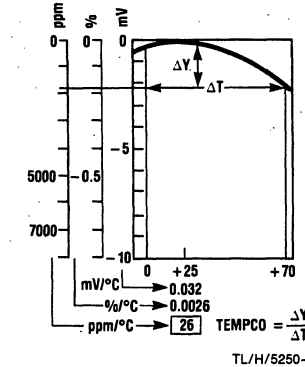
TL/H/5250-3

LM185
Temperature Coefficient Typical



LM285
Temperature Coefficient Typical

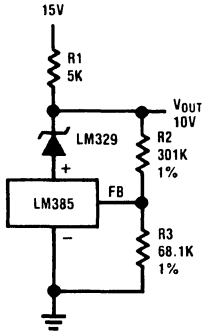
LM385
Temperature Coefficient Typical



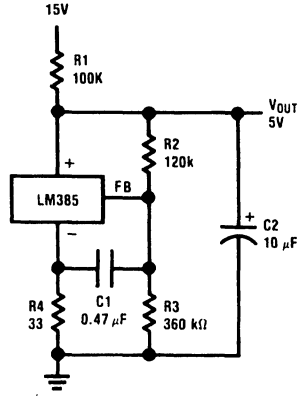
TL/H/5250-4

Typical Applications (Continued)

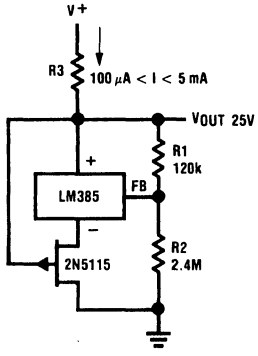
Precision 10V Reference



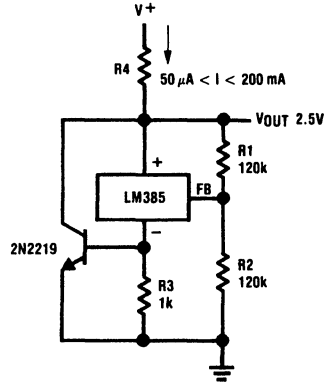
Low AC Noise Reference



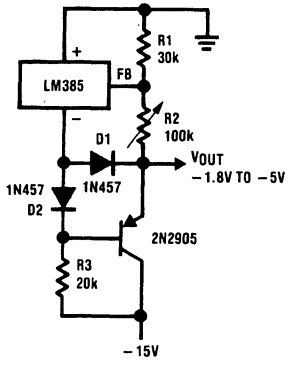
25V Low Current Shunt Regulator



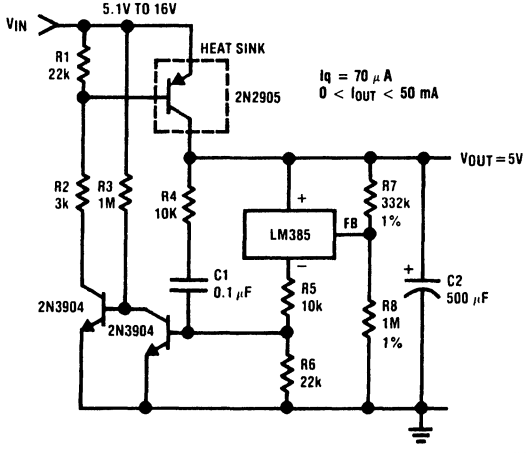
200 mA Shunt Regulator



Series-Shunt 20 mA Regulator



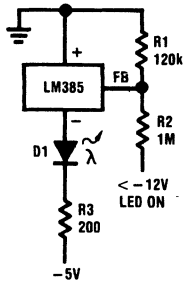
High Efficiency Low Power Regulator



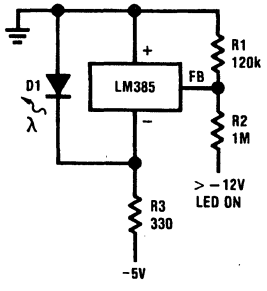
TL/H/5250–5

Typical Applications (Continued)

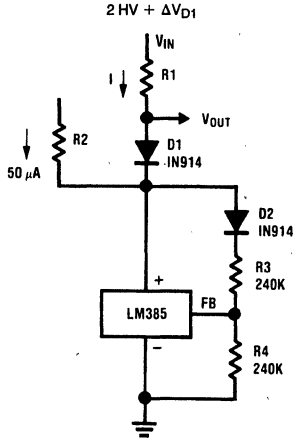
Voltage Level Detector



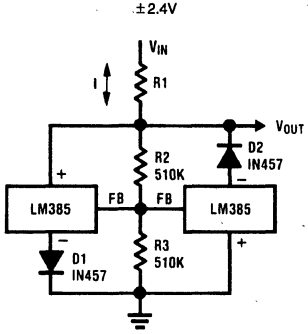
Voltage Level Detector



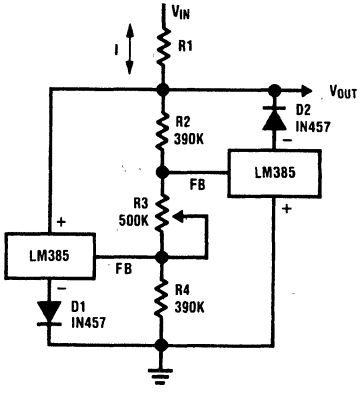
Fast Positive Clamp



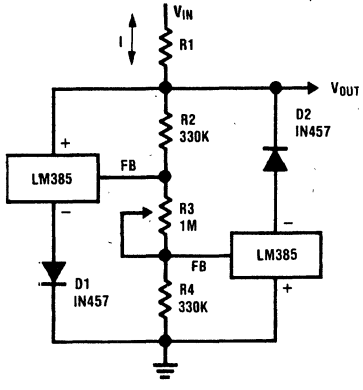
Bidirectional Clamp



Bidirectional Adjustable Clamp
±1.8V to ±2.4V



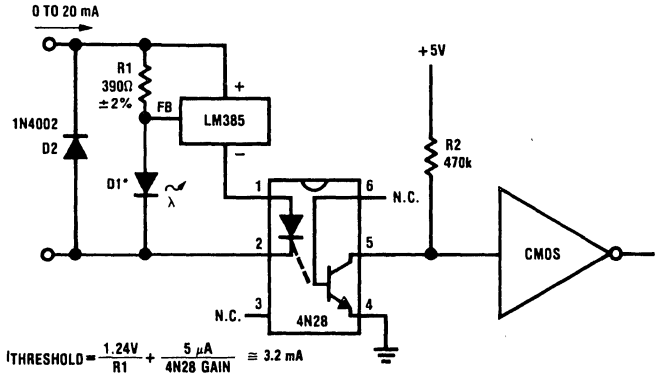
Bidirectional Adjustable Clamp
±2.4V to ±6V



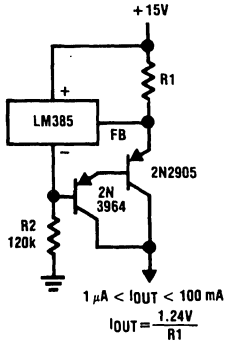
TL/H/5250–6

Typical Applications (Continued)

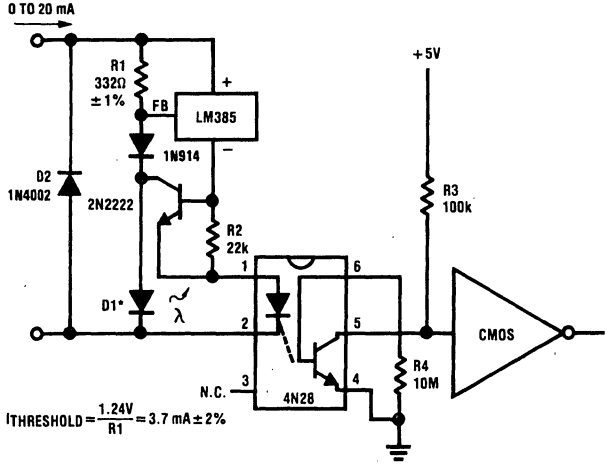
Simple Floating Current Detector



Current Source



Precision Floating Current Detector

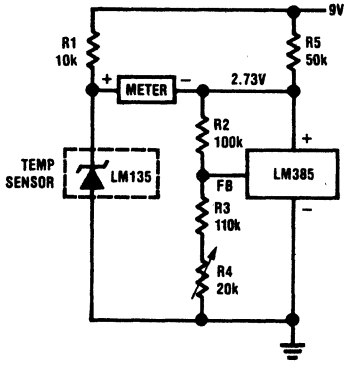


TL/H/5250–7

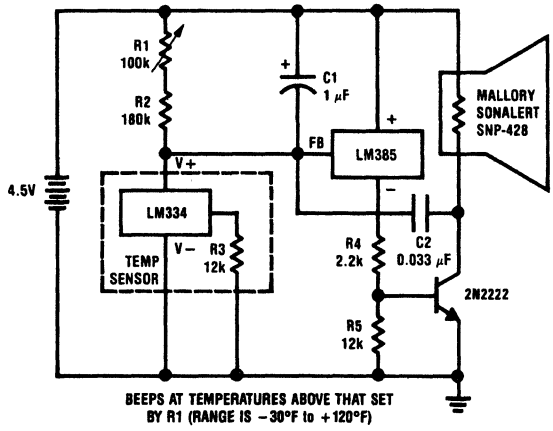
* D1 can be any LED, $V_F = 1.5V$ to 2.2V at 3 mA. D1 may act as an indicator. D1 will be on if $I_{THRESHOLD}$ falls below the threshold current, except with I = O.

Typical Application (Continued)

Centigrade Thermometer, 10 mV/°C

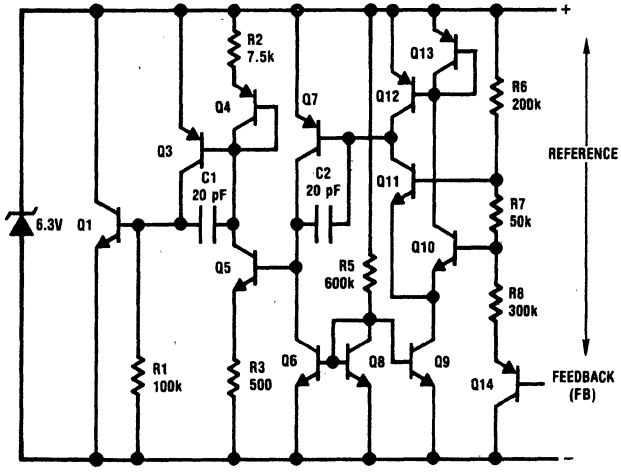


Freezer Alarm



BEEPS AT TEMPERATURES ABOVE THAT SET BY R1 (RANGE IS −30°F to +120°F)

Schematic Diagram



TL/H/5250–8

National Semiconductor

LM185-1.2/LM285-1.2/LM385-1.2 Micropower Voltage Reference Diode

General Description

The LM185-1.2/LM285-1.2/LM385-1.2 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 10 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185-1.2 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-1.2 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

Features

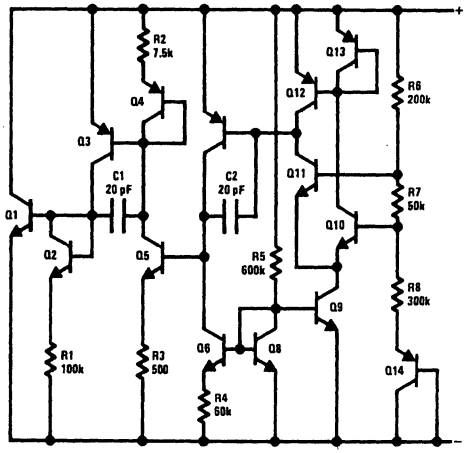
- Operating current of 10 μA to 20 mA
- 1% and 2% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient
- Low voltage reference—1.235V
- 2.5V device also available—LM385-2.5

The extremely low power drain of the LM185-1.2 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

The LM185-1.2 is rated for operation over a −55°C to 125°C temperature range while the LM285-1.2 is rated −40°C to 85°C and the LM385-1.2 0°C to 70°C. The LM185-1.2/LM285-1.2/LM385-1.2 are available in a hermetic TO-46 package and the LM385-1.2 is also available in a low-cost TO-92 molded package.

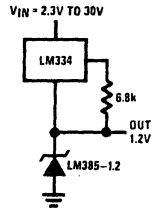
S 4

Schematic Diagram

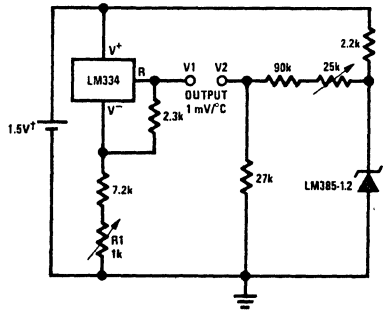


Applications

Wide Input Range Reference



Centigrade Thermometer



Calibration

1. Adjust R1 so that V1 = temp at 1 mV/°K
2. Adjust V2 to 273.2 mV

†I_Q for 1.3V to 1.6V battery voltage = 50 μA to 150 μA

TL/H/5518–1

Absolute Maximum Ratings

Reverse Current	30mA	Storage Temperature	−55°C to + 150°C
Forward Current	10mA	Lead Temp. (Soldering, 10 seconds)	300°C
Operating Temperature Range			
LM185-1.2	−55°C to + 125°C		
LM285-1.2	−40°C to + 85°C		
LM385-1.2	0°C to 70°C		

Electrical Characteristics (Note 1)

Parameter	Conditions	LM185-1.2 LM185BX-1.2 LM185BY-1.2 LM285-1.2 LM285BX-1.2 LM285BY-1.2			LM385-1.2 LM385B-1.2 LM385BX-1.2 LM385BY-1.2			Units Limit
		Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_{MIN} \le I_R \le I_{MAX}$ LM185-1.2/LM285-1.2/LM385B-1.2 LM385-1.2	1.235	1.223 1.247		1.235 1.235	1.223 1.247 1.205 1.260		V_{MIN} V_{MAX} V_{MIN} V_{MAX}
Minimum Operating Current		8	10	**20**	8	15	**20**	μA
Reverse Breakdown	$I_{MIN} \le I_R \le 1$ mA		1	**1.5**		1	**1.5**	mV
Voltage Change with Current	1 mA ≤ I_R ≤ 20 mA		10	**20**		20	**25**	mV
Reverse Dynamic Impedance	$I_R = 40$ μA. f = 20 Hz	1			1			Ω
Wideband Noise (rms)	$I_R = 100$ μA 10 Hz ≤ f ≤ 10 kHz	60			60			μV
Long Term Stability	$I_R = 100$ μA, T = 1000 Hr $T_A = 25°C \pm 0.1°C$	20			20			ppm
Average Temperature Coefficient (Note 4)	$I_R = 100$ μA X Series Y Series Other Versions		**30** **50** 	 **150**		**30** **50** 	 **150**	ppm/°C ppm/°C ppm/°C

Note 1: Parameters identified with **boldface type** apply at temperature extremes and for $I_{MIN} < I_R < 20$ mA, unless otherwise specified. All other numbers apply at $T_A = T_J = 25°C$. Thermal resistance of the TO-46 package is 440°C/W junction to ambient and 80°C/W junction to case. Thermal resistance in the TO-92 package is 180°C/W junction to ambient.

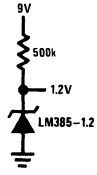
Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not used to calculate outgoing quality levels.

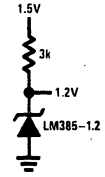
Note 4: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures between the operating T_{MAX} and T_{MIN}, divided by $T_{MAX} - T_{MIN}$. The measured temperatures are −55°C, −40°C, 0°C, 25°C, 70°C, 85°C, 125°C.

Applications (Continued)

Micropower Reference from 9V Battery



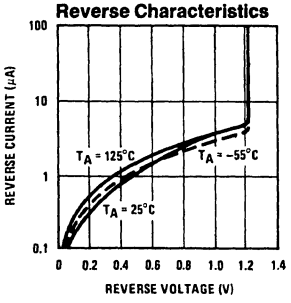
Reference from 1.5V Battery



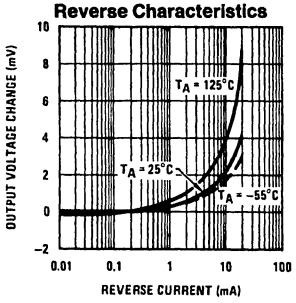
TL/H/5518–2

Typical Performance Characteristics

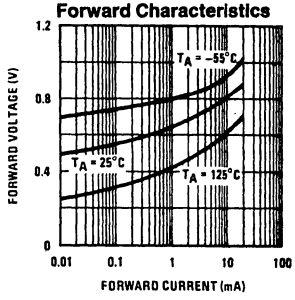
Reverse Characteristics



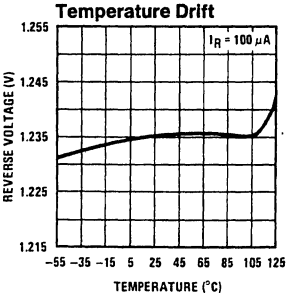
Reverse Characteristics



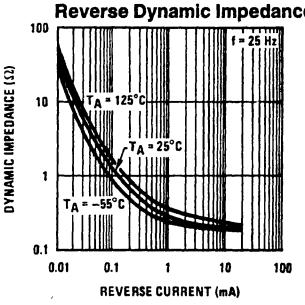
Forward Characteristics



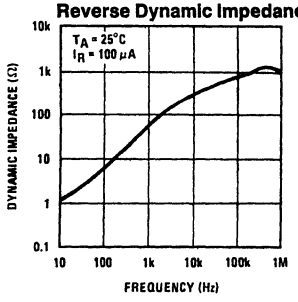
Temperature Drift



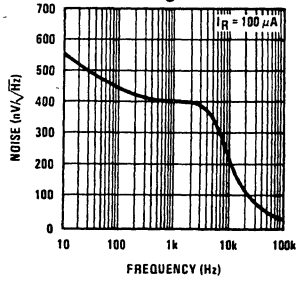
Reverse Dynamic Impedance



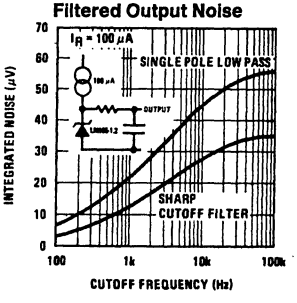
Reverse Dynamic Impedance



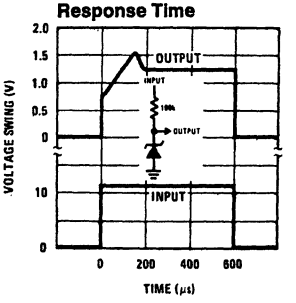
Noise Voltage



Filtered Output Noise



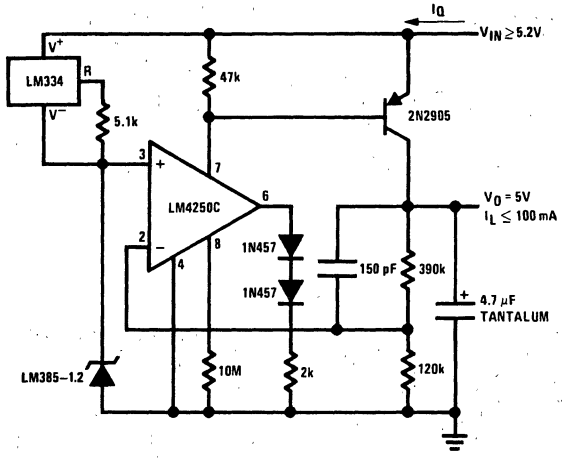
Response Time



TL/H/5518–3

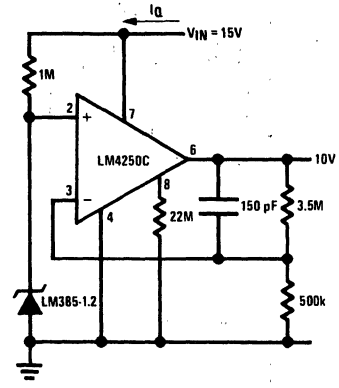
LM385 Applications

Micropower* 5V Regulator



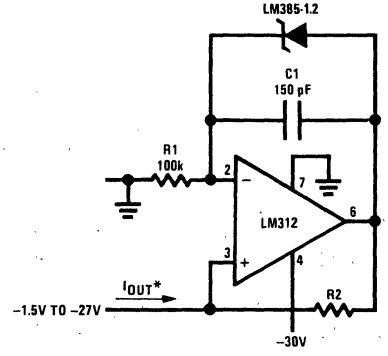
* $I_Q \cong 30\ \mu A$

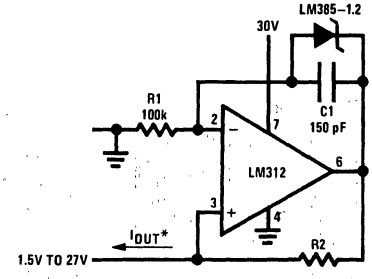
Micropower* 10V Reference



* $I_Q \cong 20\ \mu A$ standby current

Precision 1 μA to 1 mA Current Sources





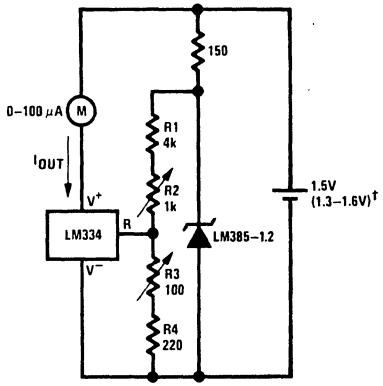
TL/H/5518–4

* $I_{OUT} = \frac{1.23V}{R2}$

LM385 Applications (Continued)

METER THERMOMETERS

0°C – 100°C Thermometer

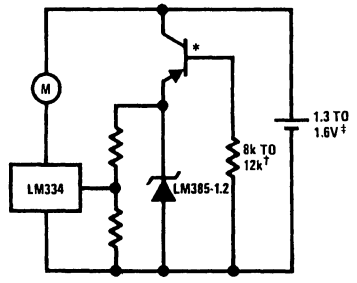


Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1 μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

†I_Q at 1.3V ≅ 500 μA
I_Q at 1.6V ≅ 2.4 mA

Lower Power Thermometer

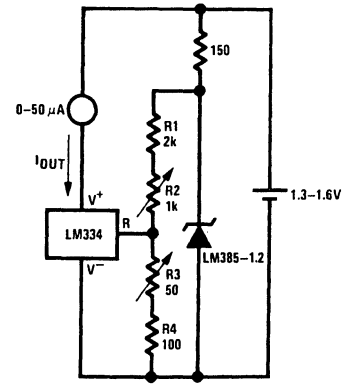


* 2N3638 or 2N2907 select for inverse H_{FE} ≅ 5

† Select for operation at 1.3V

‡ I_Q ≅ 600 μA to 900 μA

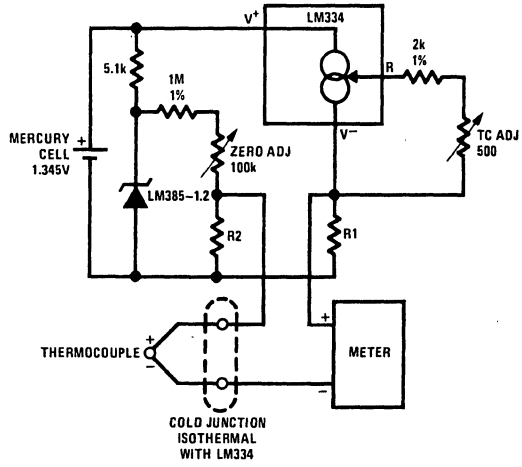
0°F – 50°F Thermometer



Calibration

1. Short LM385-1.2, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

Micropower Thermocouple Cold Junction Compensator



TL/H/5518–5

Adjustment Procedure

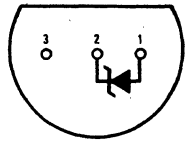
1. Adjust TC ADJ pot until voltage across R1 equals kelvin temperature multiplied by the thermocouple seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple seedbeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Coefficient (μV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @ 25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

Typical supply current 50 μA

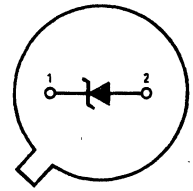
Connection Diagrams

TO-92
Plastic Package



BOTTOM VIEW

TO-46
Metal Can Package



BOTTOM VIEW

TL/H/5518–6

Order Numbers LM185-1.2, LM285-1.2, LM385-1.2
See NS Packages H02A, Z03A

National Semiconductor

LM185-2.5/LM285-2.5/LM385-2.5 Micropower Voltage Reference Diode

General Description

The LM185-2.5/LM285-2.5/LM385-2.5 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 20 μA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM-185-2.5 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-2.5 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

Features

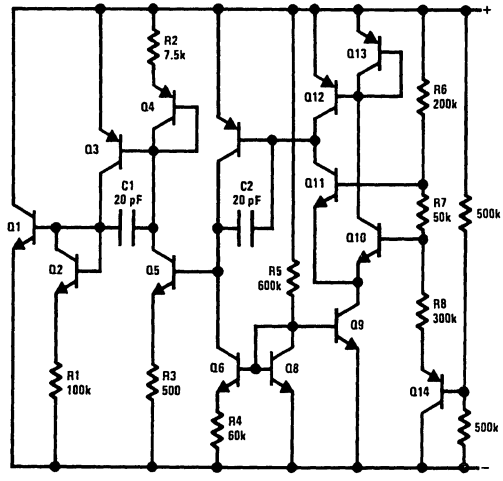
- Operating current of 20 μA to 20 mA
- 1.5% and 3% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient
- Low voltage reference—2.5V

The extremely low power drain of the LM185-2.5 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part. For applications requiring 1.2V see LM185-1.2.

The LM185-2.5 is rated for operation over a −55°C to 125°C temperature range while the LM285-2.5 is rated −40°C to 85°C and the LM385-2.5 0°C to 70°C. The LM185-2.5/LM285-2.5/LM385-2.5 are available in a hermetic TO-46 package and the LM385-2.5 is also available in a low-cost TO-92 molded package.

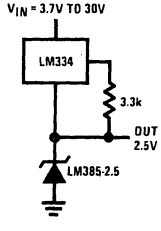
S 4

Schematic Diagram



Applications

Wide Input Range Reference



TL/H/5519–1

Absolute Maximum Ratings

Reverse Current	30 mA	LM285-2.5	−40°C to + 85°C
Forward Current	10 mA	LM385-2.5	0°C to 70°C
Operating Temperature Range		Storage Temperature	−55°C to + 150°C
LM185-2.5	−55°C to + 125°C	Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	LM185-2.5 LM185BX-2.5 LM185BY-2.5 LM285-2.5 LM285BX-2.5 LM285BY-2.5			LM385-2.5 LM385B-2.5 LM385BX-2.5 LM385BY-2.5			Units Limit
		Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
Reverse Breakdown Voltage	$T_A = 25°C$, $I_{MIN} \le I_R \le I_{MAX}$ LM185-2.5/LM285-2.5/LM385B-2.5 LM385-2.5	2.5	2.462 2.538		2.5 2.5	2.462 2.538 2.425 2.575		V_{MIN} V_{MAX} V_{MIN} V_{MAX}
Minimum Operating Current		13	20	**30**	13	20	**30**	μA
Reverse Breakdown Voltage Change with Current	20 μA ≤ I_R ≤ 1 mA 1 mA ≤ I_R ≤ 20 mA		1 10	**1.5** **20**		2.0 20	**2.5** **25**	mV mV
Reverse Dynamic Impedance	I_R = 100 μA. f = 20 Hz	1			1			Ω
Wideband Noise (rms)	I_R = 100 μA 10 Hz ≤ f ≤ 10 kHz	120			120			μV
Long Term Stability	I_R = 100 μA, T = 1000 Hr $T_A = 25°C \pm 0.1°C$	20			20			ppm
Average Temperature Coefficient (Note 4)	I_R = 100 μA X Series Y Series Other Versions		**30** **50**	 **150**		**30** **50**	 **150**	 ppm/°C ppm/°C ppm/°C

Note 1: Parameters identified with **boldface type** apply at temperature extremes and for $I_{MIN} < I_R < 20$ mA, unless otherwise specified. All other numbers apply at $T_A = T_J = 25°C$. Thermal resistance of the TO-46 package is 440° C/W junction to ambient and 80° C/W junction to case. Thermal resistance in the TO-92 package is 180° C/W junction to ambient.

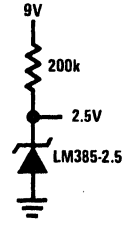
Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and input current ranges. These limits are not used to calculate outgoing quality levels.

Note 4: The average temperature coefficient is defined as the maximum deviation of reference voltage at all measured temperatures between the operating T_{MAX} and T_{MIN}, divided by $T_{MAX} - T_{MIN}$. The measured temperatures are −55°C, −40°C, 0°C, 25°C, 70°C, 85°C, 125°C.

Applications (Continued)

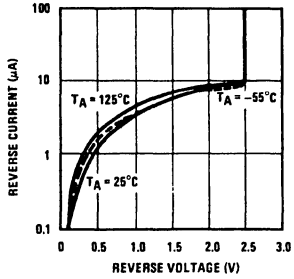
Micropower Reference from 9V Battery



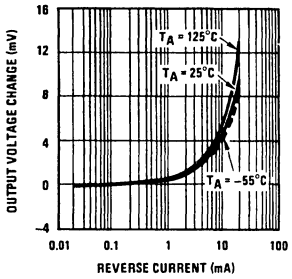
TL/H/5519–2

Typical Performance Characteristics

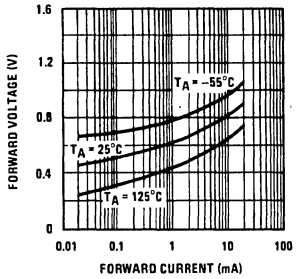
Reverse Characteristics



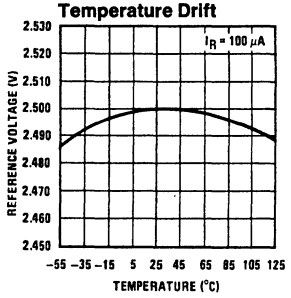
Reverse Characteristics



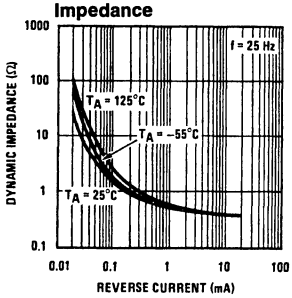
Forward Characteristics



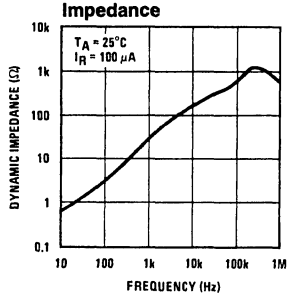
Temperature Drift



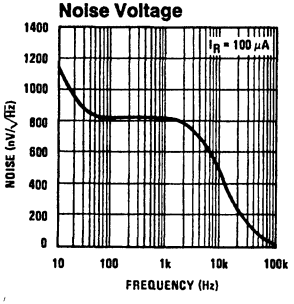
Reverse Dynamic Impedance



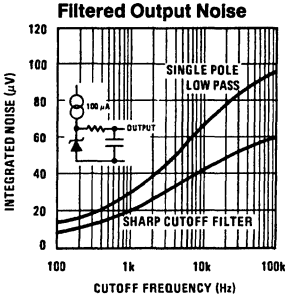
Reverse Dynamic Impedance



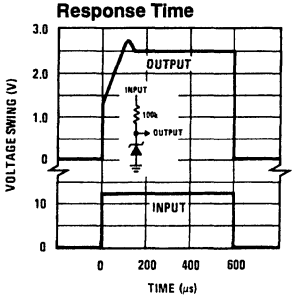
Noise Voltage



Filtered Output Noise



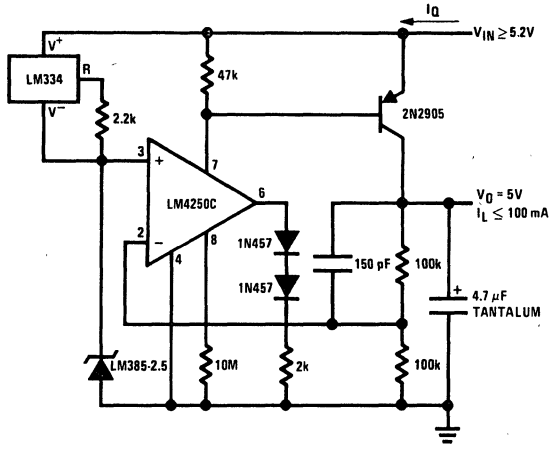
Response Time



TL/H/5519–3

LM385-2.5 Applications

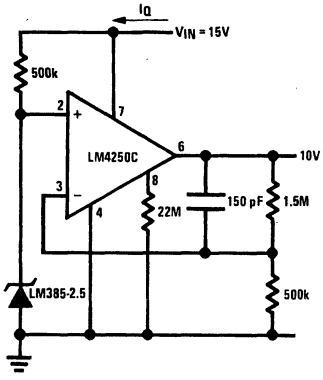
Micropower* 5V Regulator



*$I_Q \cong 40$ μA

TL/H/5519–9

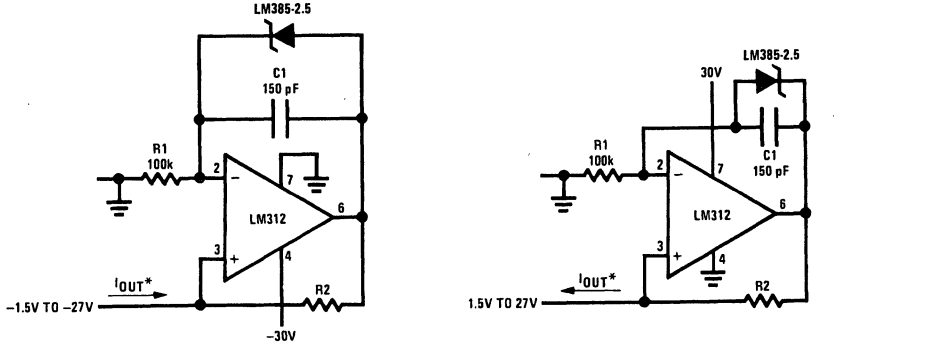
Micropower* 10V Reference



TL/H/5519–10

*$I_Q \cong 30$ μA standby current

Precision 1 μA to 1 mA Current Sources

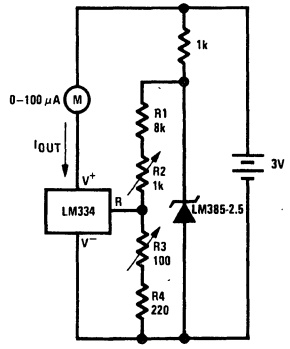


TL/H/5519–4

$$*I_{OUT} = \frac{2.5V}{R2}$$

METER THERMOMETERS

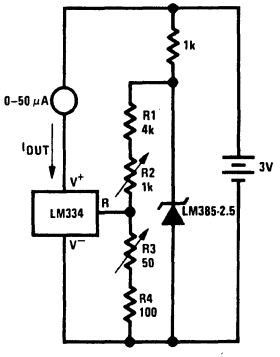
0°C–100°C Thermometer



Calibration

1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1μA/°K
2. Remove short, adjust R2 for correct reading in centigrade

0°F–50°F Thermometer



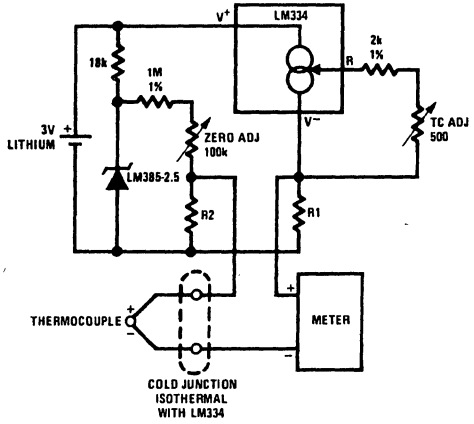
TL/H/5519–5

Calibration

1. Short LM385-2.5, adjust R3 for I_{OUT} = temp at 1.8 μA/°K
2. Remove short, adjust R2 for correct reading in °F

LM385-2.5 Applications (Continued)

Micropower Thermocouple Cold Junction Compensator



TL/H/5519–6

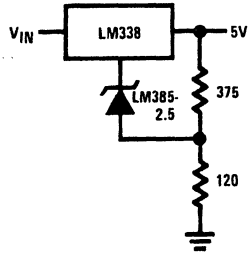
Adjustment Procedure

1. Adjust TC ADJ pot until voltage across R1 equals Kelvin temperature multiplied by the thermocouple Seebeck coefficient.
2. Adjust zero ADJ pot until voltage across R2 equals the thermocouple Seebeck coefficient multiplied by 273.2.

Thermocouple Type	Seebeck Coefficient (μV/°C)	R1 (Ω)	R2 (Ω)	Voltage Across R1 @25°C (mV)	Voltage Across R2 (mV)
J	52.3	523	1.24k	15.60	14.32
T	42.8	432	1k	12.77	11.78
K	40.8	412	953Ω	12.17	11.17
S	6.4	63.4	150Ω	1.908	1.766

Typical supply current 50 μA

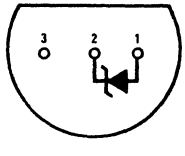
Improving Regulation of Adjustable Regulators



TL/H/5519–7

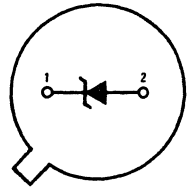
Connection Diagrams

TO-92
Plastic Package



BOTTOM VIEW

TO-46
Metal Can Package



BOTTOM VIEW

TL/H/5519–8

Order Numbers LM185-2.5,
LM285-2.5, LM385-2.5
See NS Packages H02A, Z03A

National Semiconductor

LM199AH-20, LM299AH-20, LM399AH-50 Ultra-Stable References

General Description

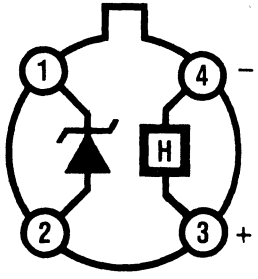
The National Semiconductor LM199AH-20, LM299AH-20, and LM399AH-50 are ultra-stable Zener references specially selected from the production runs of LM199AH, LM299AH, LM399AH and tested to confirm a long-term stability of 20, 20, or 50 PPM per 1000 hours, respectively. The devices are measured every 168 hours and the voltage of each device is logged and compared in such a way as to show the deviation from its initial value. Each measurement is taken with a probable-worst-case deviation of ±2 ppm, compared to the Reference Voltage, which is derived from several groups of NBS-traceable references such as LM199AH-20's, 1N827's, and saturated standard cells, so that the deviation of any one group will not cause false indications. Indeed, this comparison process has recently been automated using a specially prepared computer program which is custom-designed to reject noisy data (and require a repeat reading) and to record the average of the best 5 of 7 readings, just as a sagacious standards engineer will reject unbelievable readings.

The typical characteristic for the LM199AH-20 is shown on the next page. This computerized print-out form of each reference's stability is shipped with the unit. For typical application circuits, refer to the LM199 data sheet on preceding pages. For typical performance characteristics, refer to the LM199A data sheet on preceding pages.

Features

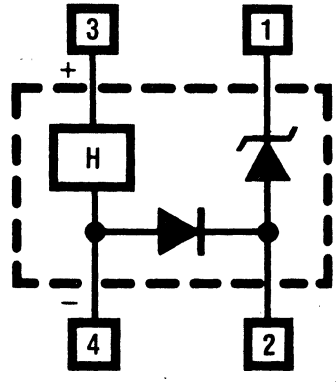
- Sub-surface zener is not degraded by surface-contamination
- Proven reliability, low-stress packaging in TO-46 integrated-circuit hermetic package, for low hysteresis after thermal cycling. 33 million hours MTBF at $T_A = +25°C$ ($T_J = +86°C$)
- Low noise guaranteed.
- Low temperature coefficient, ½ ppm/°C guaranteed.

Connection and Functional Block Diagrams



TL/H/6762–1

Order Number LM199AH-20, LM299AH-20, or LM399AH-50
See NS Pkg. H04D



TL/H/6762–2

Absolute Maximum Ratings

Temperature Stabilizer Voltage	40V	Operating Temperaure Range	
Reverse Breakdown Current	20 mA	LM199A	−55°C to +125°C
Forward Current	1 mA	LM299A	−25°C to +85°C
Reference to Substrate Voltage $V_{(RS)}$ (Note 1)	+40V	LM399A	0°C to +70°C
	−0.1V	Storage Temperature Range	−55°C to +150°C
		Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 2)

Parameter	Conditions	LM199AH-20, LM299AH-20			LM399AH-50			Units
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage	$0.5\ mA \le I_R \le 10\ mA$	6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5\ mA \le I_R \le 10\ mA$		6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1\ mA$		0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \le T_A \le 85°C$ LM199A		0.00002	0.00005				%/°C
	$85°C \le T_A \le 125°C$ LM199A		0.0005	0.0010				%/°C
	$-25°C \le T_A \le 85°C$ LM299A		0.00002	0.00005				%/°C
	$0°C \le T_A \le 70°C$ LM399A					0.00003	0.0001	%/°C
RMS Noise	$10\ Hz \le f \le 10\ kHz$		7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \le T_A \le 28°C$, 1000 Hours, $I_R = 1\ mA \pm 0.1\%$		8	20		9	50	ppm
Temperature Stabilizer	$T_A = 25°C$, Still Air, $V_S = 30V$		8.5	14		8.5	15	mA
Supply Current	$T_A = -55°C$		22	28				mA
Temperature Stabilizer Supply Voltage		9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$		3			3		s
Initial Turn-on Current	$9 \le V_S \le 40$, $T_A = 25°C$		140	200		140	200	mA

Note 1: The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.

Note 2: These specifications apply for 30V applied to the temperature stabilizer and $-55°C \le T_A \le +125°C$ for the LM199A; $-25°C \le T_A \le +85°C$ for the LM299A and $0°C \le T_A \le +70°C$ for the LM399A.

Typical Characteristics

National Semiconductor
Certified Long Term Drift

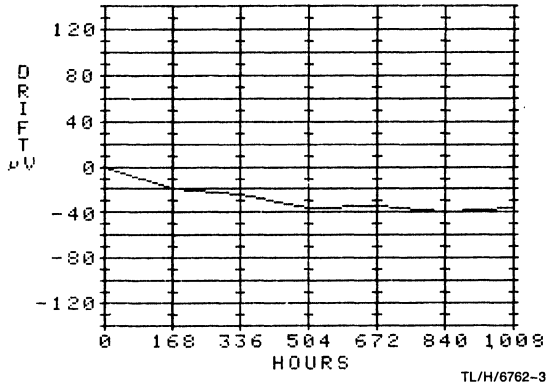
HRS	DRIFT
168	−20
336	−24
504	−36
672	−34
840	−40
1008	−36

LM199AH-20
Part #6849

Limits
LM199AH-20 140 μV
LM299AH-20 140 μV
LM399AH-50 350 μV

Testing Conditions

Heater Voltage	30V
Zener Current	1 mA
Ambient Temp.	25C



TL/H/6762–3

Section 5

Converters

Converters

Section Contents

National Semiconductor

ADC0816, ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

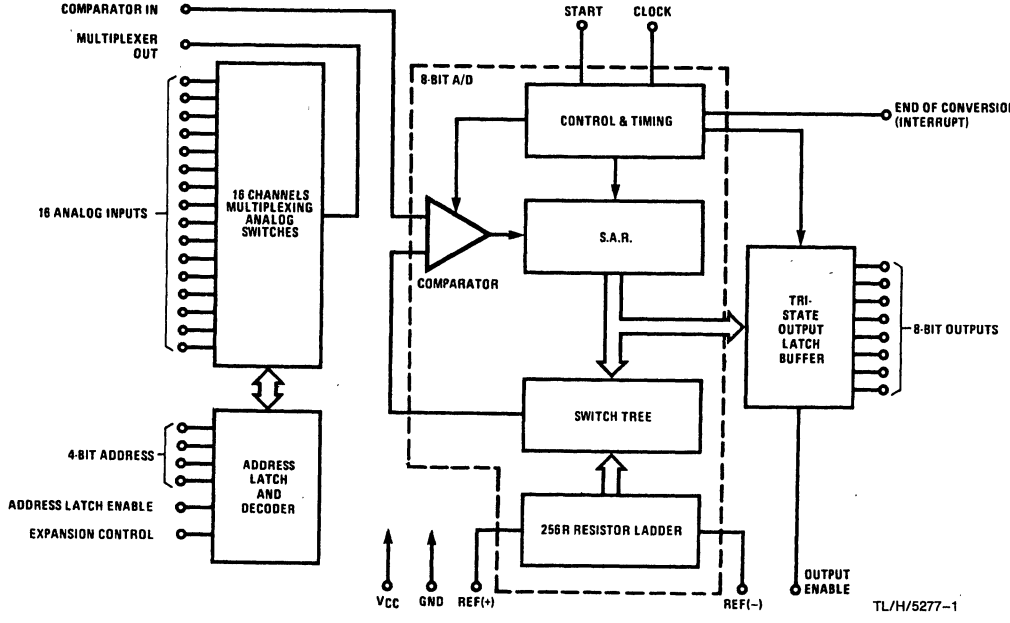
The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

Features

- Resolution—8-bits
- Total unadjusted error—±½ LSB and ± 1 LSB
- No missing codes
- Conversion time—100 μS
- Single supply—5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption—15 mW
- Latched TRI-STATE output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning

S 5

Block Diagram



Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC}+0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	−0.3V to 15V
Storage Temperature Range	−65°C to + 150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Notes 1 & 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0816CJ	$-55°C \le T_A + 125°C$
ADC0816CCJ, ADC0816CCN, ADC0817CCN	$-40°C \le T_A \le +85°C$
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}
Voltage at Any Pin Except Control Inputs	0V to V_{CC}
Voltage at Control Inputs (START, OE, CLOCK, ALE, EXPANSION CONTROL, ADD A, ADD B, ADD C, ADD D)	0V to 15V

Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}= $V_{REF(+)}$, $V_{REF(-)}$=GND, V_{IN}=$V_{COMPARATOR\ IN}$, $T_{MIN} \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0816 Total Unadjusted Error (Note 5)	 25°C T_{MIN} to T_{MAX}			 ±½ ±¾	 LSB LSB
	ADC0817 Total Unadjusted Error (Note 5)	 0°C to 70°C T_{MIN} to T_{MAX}			 ±1 ±1¼	 LSB LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	4.5		kΩ
	Analog Input Voltage Range	(Note 4)V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		$V_{CC}/2-0.1$	$V_{CC}/2$	$V_{CC}/2+0.1$	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0816CJ 4.5V≤V_{CC}≤5.5V, −55°C≤T_A≤+ 125°C unless otherwise noted.
ADC0816CCJ, ADC0816CCN, ADC0817CCN 4.75V≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel) T_A=25°C, R_L=10k T_A=85°C T_A=125°C		1.5	 3 6 9	 kΩ kΩ kΩ
ΔR_{ON}	ΔON Resistance Between Any 2 Channels	(Any Selected Channel) R_L=10k		75		Ω
I_{OFF+}	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V, T_A=25°C T_{MIN} to T_{MAX}		10	200 1.0	nA μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0, T_A=25°C T_{MIN} to T_{Max}	 −200 −1.0			 nA μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			μA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0816CJ—4.5V≤V_{CC}≤5.5V, −55°C≤T_A≤+125°C unless otherwise noted.
ADC0816CCJ, ADC0816CCN, ADC0817CCN—4.75V≤V_{CC} ≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O=−360 μA, T_A=85°C I_O=−300 μA, T_A=125°C	V_{CC}−0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=V_{CC} V_O=0	 −3.0		3.0	μA μA

Electrical Characteristics

Timing Specifications: V_{CC}=$V_{REF(+)}$=5V, $V_{REF(-)}$=GND, t_r=t_f=20 ns and T_A=25°C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)* (Note 7)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_S	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
T_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time from ALE	R_S=0Ω *(Figure 5)*		1	2.5	μS
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k *(Figure 8)*		125	250	ns
t_{1H},t_{0H}	OE Control to Hi-Z	C_L=10 pF, R_L=10k *(Figure 8)*		125	250	ns
t_C	Conversion Time	f_c=640 kHz, *(Figure 5)* (Note 8)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8+2μs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs (Note 8)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, and linearity errors. See *Figure 3.* None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13.*

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6).* See paragraph 4.0.

Note 7: If start pulse is asynchronous with converter clock the minimum start pulse width is 8 clock periods plus 2 μS.

Note 8: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table 1 shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1

Selected Analog Channel	Address Line				Expansion Control
	D	C	B	A	
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs using the expansion control. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + ½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

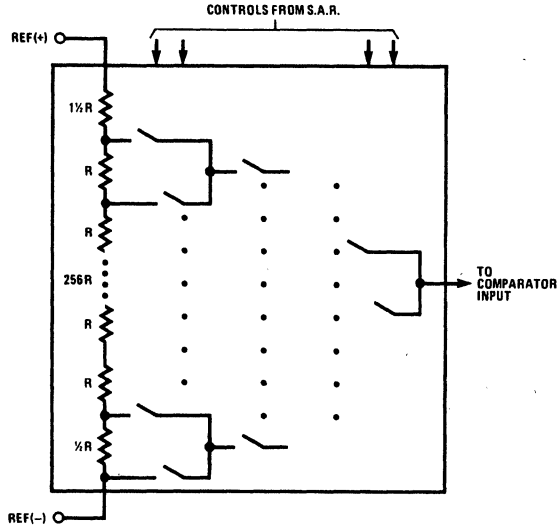


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FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ulimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179.

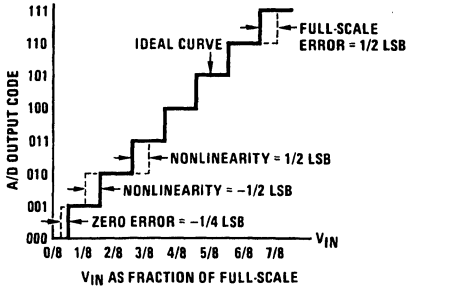

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FIGURE 2. 3-Bit A/D Transfer Curve

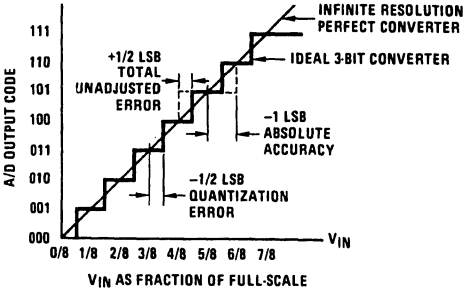

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FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

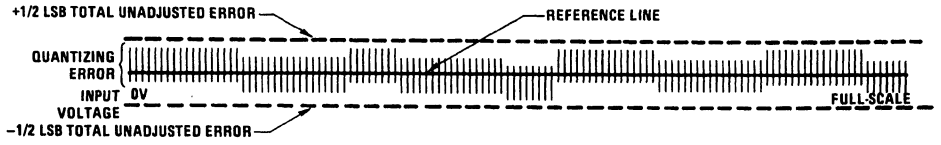

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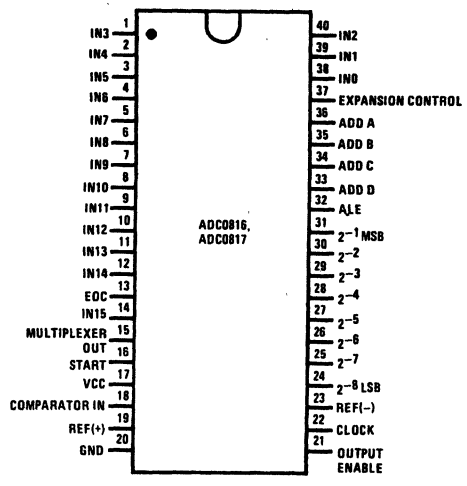
FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Package



TOP VIEW

See Ordering Information

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Timing Diagram

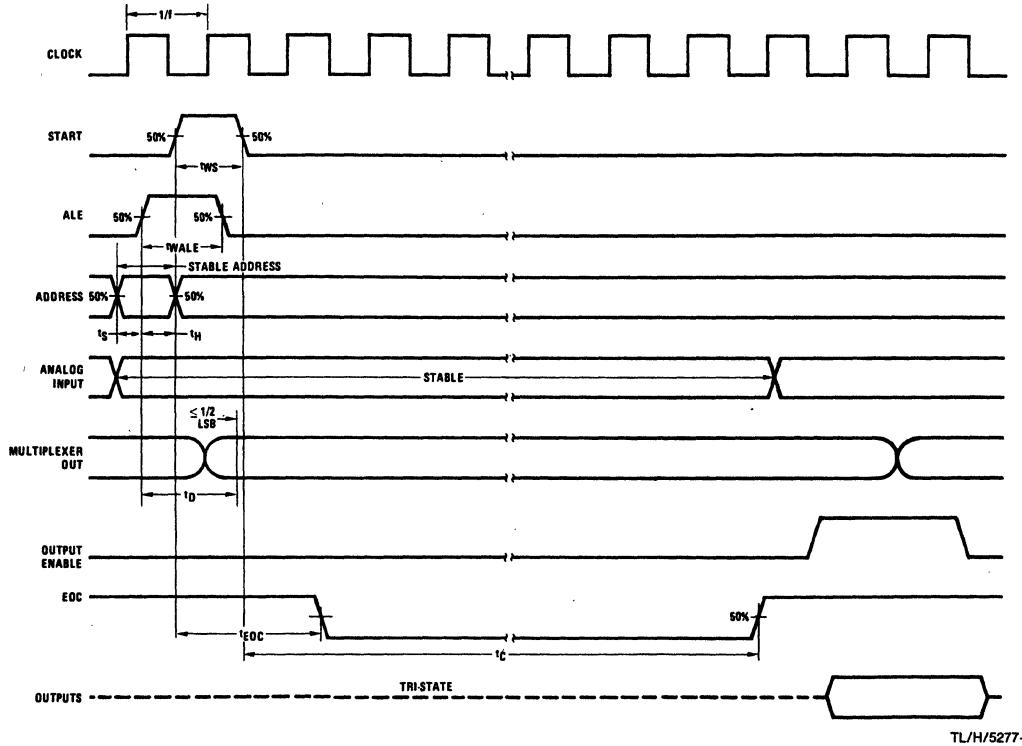

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FIGURE 5

Typical Performance Characteristics

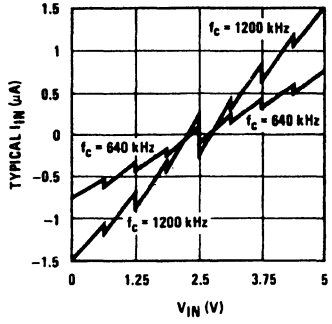

FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

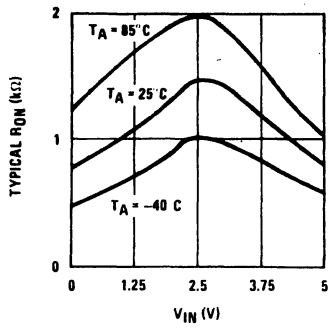

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FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE Test Circuits and Timing Diagrams

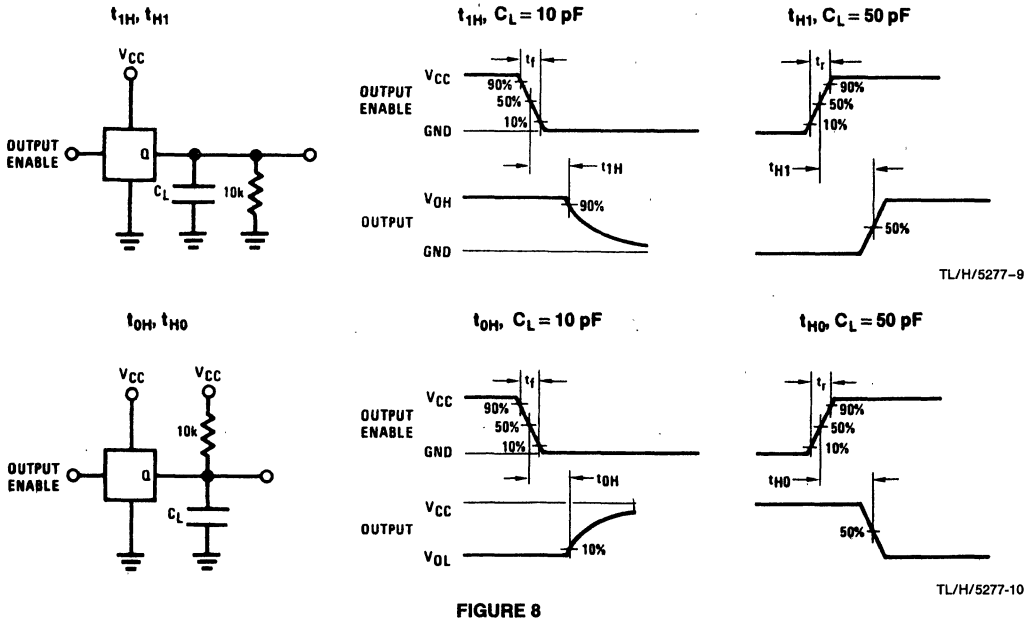

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FIGURE 8

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0816

V_{fs} = Full-scale voltage

V_Z = Zero voltage

D_X = Data point being measured

D_{MAX} = Maximum data limit

D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} =$ 5.12V, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches These limitations are automaticaly satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

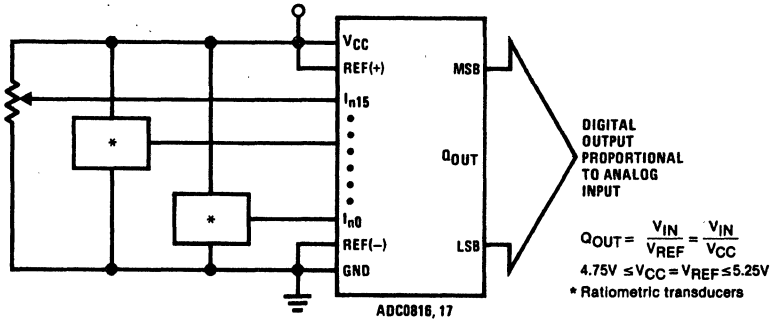

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FIGURE 9. Ratiometric Conversion System

Applications Information (Continued)

The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground references system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the millliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB to be half the size of the LSB in a 5V reference system.

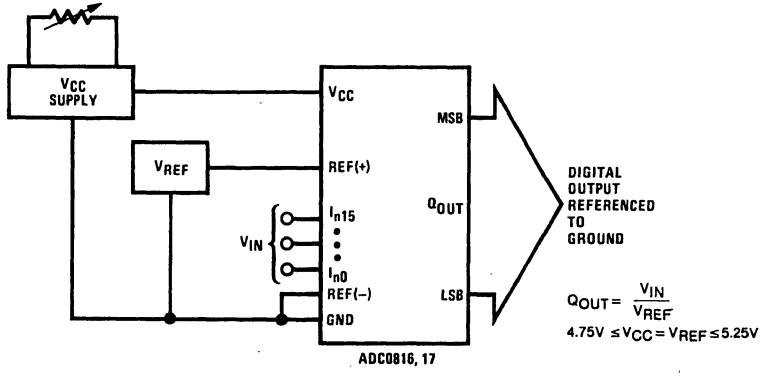

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FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

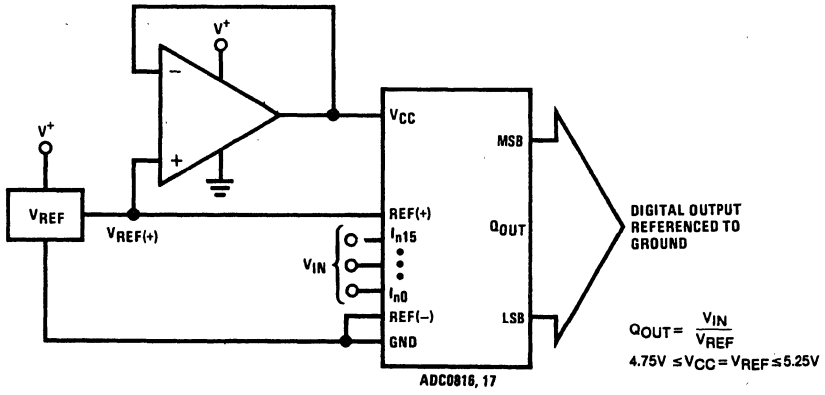

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FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

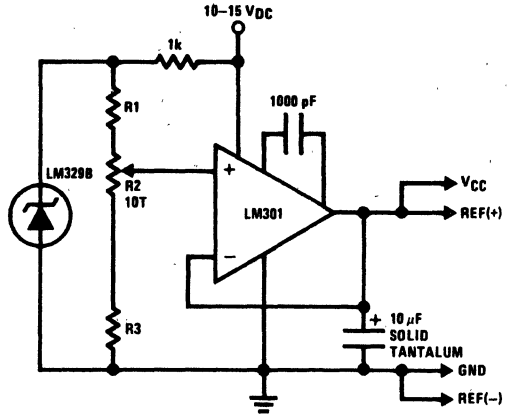

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FIGURE 12. Typical Reference and Supply Circuit

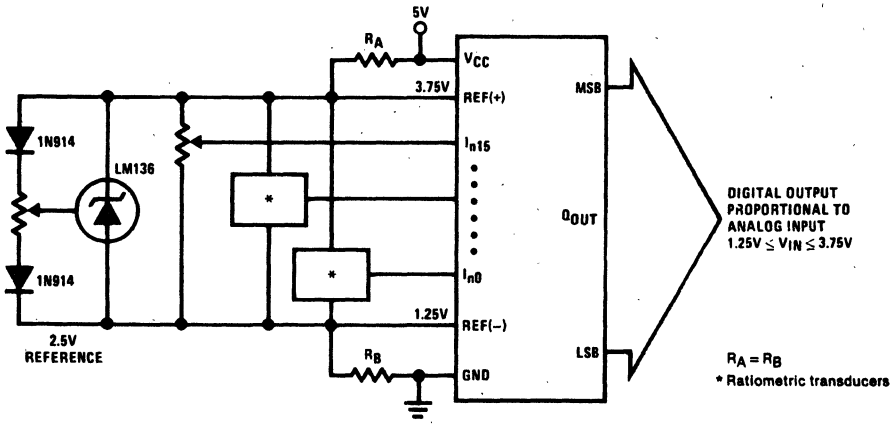

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FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN}=\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}+\frac{1}{512}\right]\pm V_{TUE}\right\}+V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN}=\left\{(V_{REF(+)}-V_{REF(-)})\left[\frac{N}{256}\right]\pm V_{TUE}\right\}+V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N=\frac{V_{IN}-V_{REF(-)}}{V_{REF(+)}-V_{REF(-)}}\times 256\pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input

V_{REF} = Voltage at Ref(+)

V_{REF} = Voltage at Ref(−)

V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

Applications Information (Continued)

4.0 ANALOG COMPARATOR INPUTS

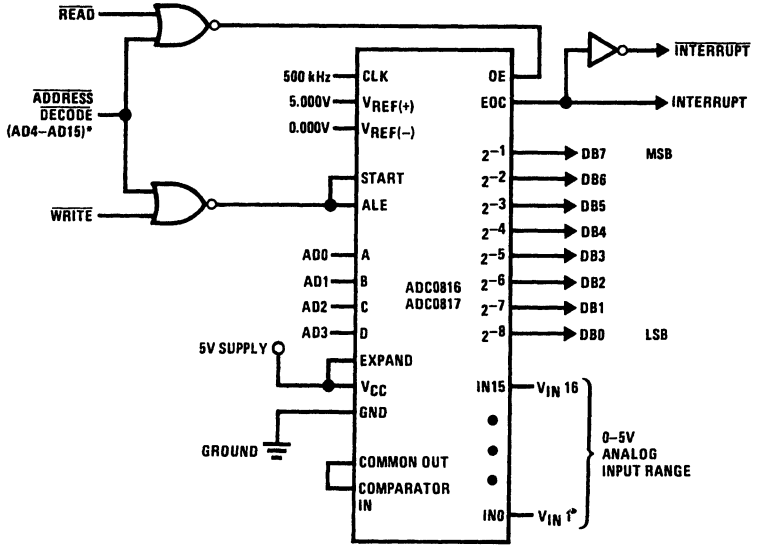
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog or comparator inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally. See AN-258 for further discussion.

Typical Application



TL/H/5277-16

*Address latches needed for 8085 and SC/MP interfacing the ADC0816, 17 to a microprocessor

Microprocessor Interface Table

PROCESSOR	READ	WRITE	INTERRUPT (COMMENT)
8080	$\overline{MEMR}$	$\overline{MEMW}$	INTR (Thru RST Circuit)
8085	$\overline{RD}$	$\overline{WR}$	INTR (Thru RST Circuit)
Z-80	$\overline{RD}$	$\overline{WR}$	$\overline{INT}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•ϕ 2•R/W	VMA•Q_2•$\overline{R/W}$	$\overline{IRQA}$ or $\overline{IRQB}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to + 125°C
Error	±½ Bit Unadjusted	ADC0816CCN	ADC0816CCJ	ADC0816CJ
	±1 Bit Unadjusted	ADC0817CCN		
Package Outline		N40A Molded DIP	J40A Hermetic DIP	J40A Hermetic DIP

S 5

National Semiconductor

microCMOS

ADC0820 8-Bit High Speed μP Compatible A/D Converter with Track/Hold Function

General Description

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5 μs conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/μs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

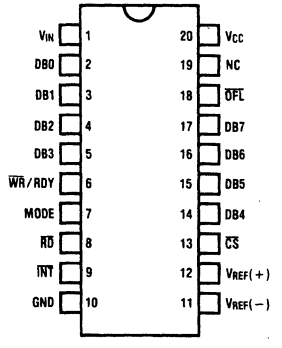
- Resolution — 8 Bits
- Conversion Time — 2.5 μs Max (RD Mode); 1.5 μs Max (WR-RD Mode)
- Input signals with slew rate of 100 mV/μs converted without external sample-and-hold to 8 bits
- Low Power — 75 mW Max
- Total Unadjusted Error — ± ½ LSB and ± 1 LSB

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5 V_{DC}
- Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE® output
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP

Connection and Functional Diagrams

Dual-In-Line Package



TOP VIEW

TL/H/5501-1

Order Number ADC0820D or ADC0820N
See NS Package D20A or N20A

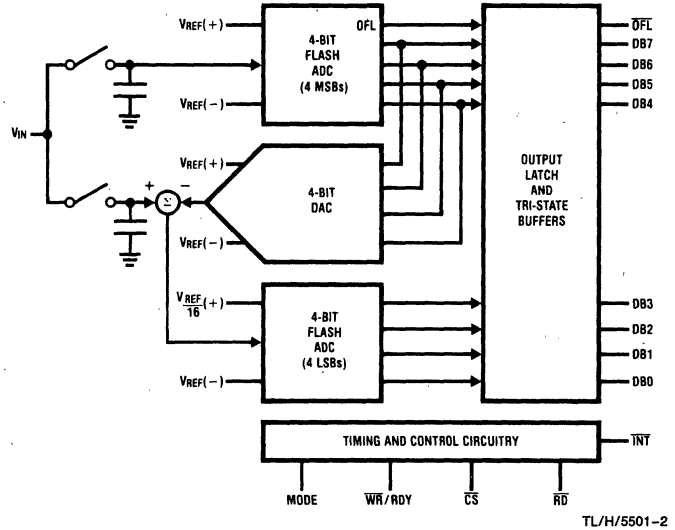


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FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	10V
Logic Control Inputs	−0.2V to V_{CC} +0.2V
Voltage at Other Inputs and Output	−0.2V to V_{CC} +0.2V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0820BD, ADC0820CD	$-55°C \le T_A \le +125°C$
ADC0820BCD, ADC0820CCD	$-40°C \le T_A \le +85°C$
ADC0820BCN, ADC0820CCN	$0°C \le T_A \le 70°C$
V_{CC} Range	4.5V to 8V

Converter Characteristics

The following specifications apply for RD mode (pin 7 = 0), V_{CC} = 5V, $V_{REF}(+)$ = 5V, and $V_{REF}(-)$ = GND unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	ADC0820BD, ADC0820CD ADC0820BCD, ADC0820CCD			ADC0820BCN, ADC0820CCN			Limit Units
		Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
Resolution			**8**			8	**8**	Bits
Total Unadjusted Error (Note 3)	ADC0820BD, BCD		**±½**					LSB
	ADC0820BCN					**±½**	**±½**	LSB
	ADC0820CD, CCD		**±1**					LSB
	ADC0820CCN					**±1**	**±1**	LSB
Minimum Reference Resistance		2.3	**1.25**		2.3	1.4	**1.25**	kΩ
Maximum Reference Resistance		2.3	**6**		2.3	5.3	**6**	kΩ
Maximum $V_{REF}(+)$ Input Voltage			**V_{CC}**			V_{CC}	**V_{CC}**	V
Minimum $V_{REF}(-)$ Input Voltage			**GND**			GND	**GND**	V
Minimum $V_{REF}(+)$ Input Voltage			**$V_{REF}(-)$**			$V_{REF}(-)$	**$V_{REF}(-)$**	V
Maximum $V_{REF}(-)$ Input Voltage			**$V_{REF}(+)$**			$V_{REF}(+)$	**$V_{REF}(+)$**	V
Maximum V_{IN} Input Voltage			**V_{CC}+0.1**			V_{CC}+0.1	**V_{CC}+0.1**	V
Minimum V_{IN} Input Voltage			**GND−0.1**			GND−0.1	**GND−0.1**	V
Maximum Analog Input Leakage Current	$\overline{CS} = V_{CC}$							
	$V_{IN} = V_{CC}$		**3**			0.3	**3**	μA
	V_{IN} = GND		**−3**			−0.3	**−3**	μA
Power Supply Sensitivity	V_{CC} = 5V ± 5%	±1/16	±¼		±1/16	±¼	±¼	LSB

DC Electrical Characteristics

The following specifications apply for $V_{CC}=5V$, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A=T_J=25°C$.

Parameter	Conditions		ADC0820BD, ADC0820CD ADC0820BCD, ADC0820CCD			ADC0820BCN, ADC0820CCN			Limit Units
			Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
$V_{IN(1)}$, Logical "1"	$V_{CC}=5.25V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**2.0**			2.0	**2.0**	V
Input Voltage		Mode		**3.5**			3.5	**3.5**	V
$V_{IN(0)}$, Logical "0"	$V_{CC}=4.75V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		**0.8**			0.8	**0.8**	V
Input Voltage		Mode		**1.5**			1.5	**1.5**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN(1)}=5V$; $\overline{CS}$, $\overline{RD}$		0.005	**1**		0.005		**1**	μA
	$V_{IN(1)}=5V$; $\overline{WR}$		0.1	**3**		0.1	0.3	**3**	μA
	$V_{IN(1)}=5V$; Mode		50	**200**		50	170	**200**	μA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN(0)}=0V$; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		−0.005	**−1**		−0.005		**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC}=4.75V$, $I_{OUT}=-360$ μA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**2.4**			2.8	**2.4**	V
	$V_{CC}=4.75V$, $I_{OUT}=-10$ μA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			**4.5**			4.6	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage	$V_{CC}=4.75V$, $I_{OUT}=1.6$ mA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY			**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current	$V_{OUT}=5V$; DB0–DB7, RDY		0.1	**3**		0.1	0.3	**3**	μA
	$V_{OUT}=0V$; DB0–DB7, RDY		−0.1	**−3**		−0.1	−0.3	**−3**	μA
I_{SOURCE}, Output Source Current	$V_{OUT}=0V$; DB0–DB7, $\overline{OFL}$		−12	**−6**		−12	−7.2	**−6**	mA
	$\overline{INT}$		−9	**−4.5**		−9	−5.3	**−4.5**	mA
I_{SINK}, Output Sink Current	$V_{OUT}=5V$; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		14	**7**		14	8.4	**7**	mA
I_{CC}, Supply Current	$\overline{CS}=\overline{WR}=\overline{RD}=0$		7.5	**15**		7.5	13	**15**	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20$ ns, $V_{REF}(+)=5V$, $V_{REF}(-)=0V$ and $T_A=25°C$ unless otherwise specified.

Parameter		Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_{CRD}, Conversion Time for RD Mode		Pin 7 = 0, *(Figure 2)*	1.6		2.5	μs
t_{ACC0}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = 0, *(Figure 2)*	$t_{CRD}+20$		$t_{CRD}+50$	ns
t_{CWR-RD}, Conversion Time for WR-RD Mode		Pin 7 = V_{CC}; t_{WR} = 600 ns, t_{RD} = 600 ns; *(Figures 3a* and *3b)*			1.52	μs
t_{WR}, Write Time	Min	Pin 7 = V_{CC}; *(Figures 3a* and *3b)*		600		ns
	Max	(Note 4) See Graph	50			μs
t_{RD}, Read Time	Min	Pin 7 = V_{CC}; *(Figures 3a* and *3b)* (Note 4) See Graph		600		ns
t_{ACC1}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD}<t_l$; *(Figure 3a)* $C_L=15$ pF	190		280	ns
		$C_L=100$ pF	210		320	ns
t_{ACC2}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD}>t_l$; *(Figure 3b)* $C_L=15$ pF	70		120	ns
		$C_L=100$ pF	90		150	ns

AC Electrical Characteristics (Continued) The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20$ ns, $V_{REF}(+)=5V$, $V_{REF}(-)=0V$ and $T_A=25°C$ unless otherwise specified.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_I, Internal Comparison Time	Pin 7 = V_{CC}; *(Figures 3b* and *4)* $C_L=50$ pF	800		1300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L=1k$, $C_L=10$ pF	100		200	ns
$t_{\overline{INT}L}$, Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	Pin 7 = V_{CC}, $C_L=50$ pF $t_{RD}>t_I$; *(Figure 3b)* $t_{RD}<t_I$; *(Figure 3a)*	 $t_{RD}+200$		 t_I $t_{RD}+290$	 ns ns
$t_{\overline{INT}H}$, Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	*(Figures 2, 3a* and *3b)* $C_L=50$ pF	125		225	ns
$t_{\overline{INT}HWR}$, Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	*(Figure 4)*, $C_L=50$ pF	175		270	ns
t_{RDY}, Delay from $\overline{CS}$ to RDY	*(Figure 2)*, $C_L=50$ pF, Pin 7 = 0	50		100	ns
t_{ID}, Delay from $\overline{INT}$ to Output Valid	*(Figure 4)*	20		50	ns
t_{RI}, Delay from $\overline{RD}$ to $\overline{INT}$	Pin 7 = V_{CC}, $t_{RD}<t_I$ *(Figure 3a)*	200		290	ns
t_P, Delay from End of Conversion to Next Conversion	*(Figures 2, 3a, 3b* and *4)* (Note 4) See Graph			500	ns
Slew Rate, Tracking		0.1			V/μs
C_{VIN}, Analog Input Capacitance		45			pF
C_{OUT}, Logic Output Capacitance		5			pF
C_{IN}, Logic Input Capacitance		5			pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 4: Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Accuracy vs t_{WR} and Accuracy vs t_{RP} graphs.

Note 5: The voltage at these pins should never go higher than V_{CC} nor lower than GND.

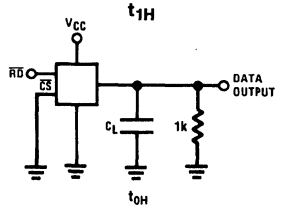
Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Guaranteed and 100% production tested.

Note 8: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

TRI-STATE Test Circuits and Waveforms

t_{1H}



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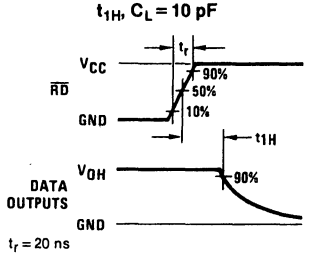
t_{1H}, $C_L=10$ pF



$t_r=20$ ns

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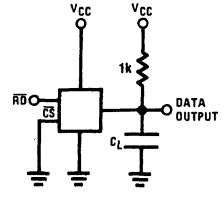
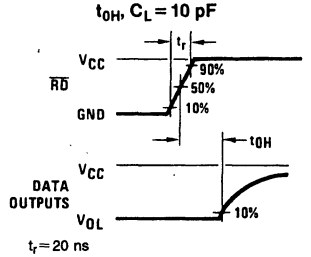
t_{0H}



TL/H/5501–5

t_{0H}, $C_L=10$ pF



$t_r=20$ ns

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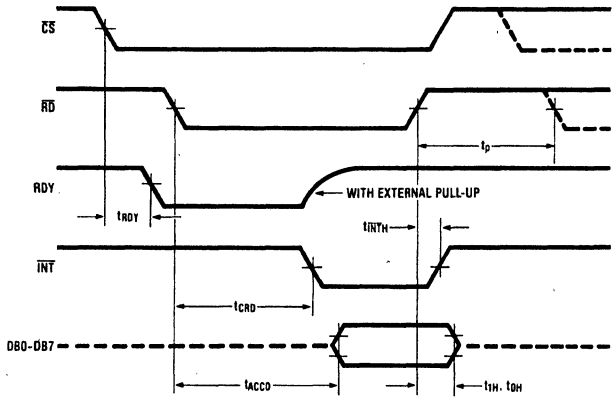
Timing Diagrams



TL/H/5501–7

FIGURE 2. RD Mode (Pin 7 is Low)

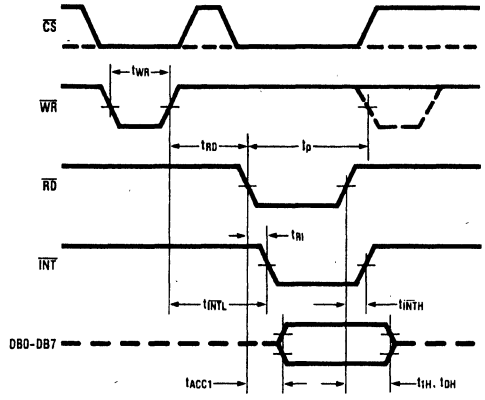


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FIGURE 3a. WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)

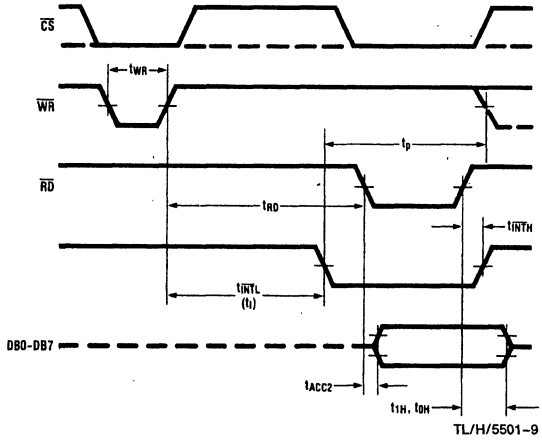

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FIGURE 3b. WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

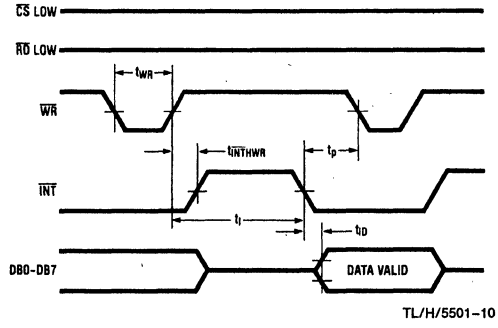

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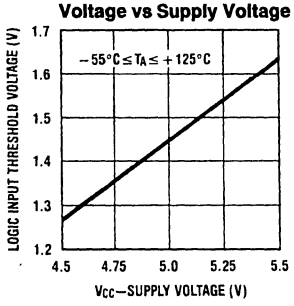
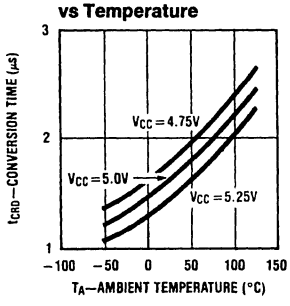
FIGURE 4. WR-RD Mode (Pin 7 is High) Stand-Alone Operation

Typical Performance Characteristics

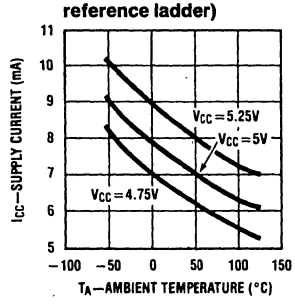
Logic Input Threshold Voltage vs Supply Voltage



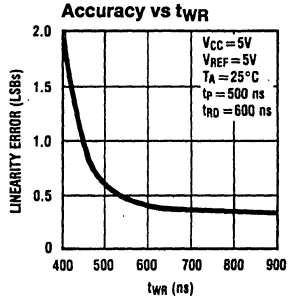
Conversion Time (RD Mode) vs Temperature



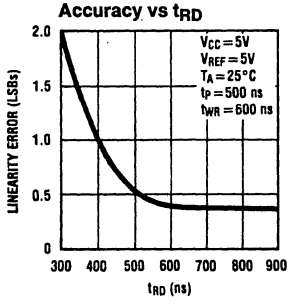
Power Supply Current vs Temperature (not including reference ladder)



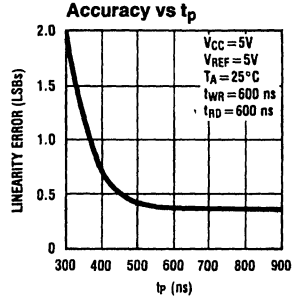
Accuracy vs t_{WR}



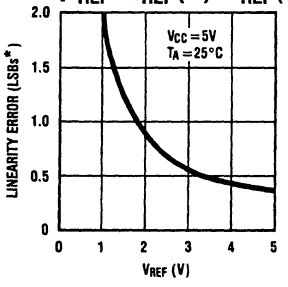
Accuracy vs t_{RD}



Accuracy vs t_p

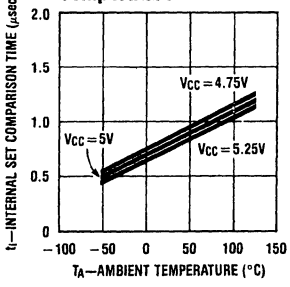


Accuracy vs V_{REF}
[$V_{REF} = V_{REF}(+) - V_{REF}(-)$]

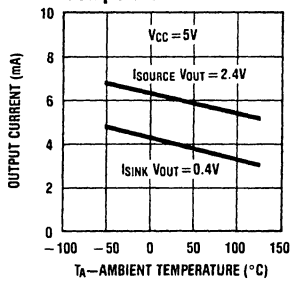


*1 LSB = $\frac{V_{REF}}{256}$

t_I, Internal Time Delay vs Temperature



Output Current vs Temperature



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Description of Pin Functions

Pin	Name	Function
1	V_{IN}	Analog input; range $= GND \leq V_{IN} \leq V_{CC}$
2	DB0	TRI-STATE data output—bit 0 (LSB)
3	DB1	TRI-STATE data output—bit 1
4	DB2	TRI-STATE data output—bit 2
5	DB3	TRI-STATE data output—bit 3
6	$\overline{WR}$/RDY	**WR-RD Mode** **$\overline{WR}$:** With $\overline{CS}$ low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800 ns (the preset internal time out, t_I) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (see *Figures 3a* and *3b*). **RD Mode** **RDY:** This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see *Figure 2*).
7	Mode	**Mode:** Mode selection input—it is internally tied to GND through a 50 μA current source. **RD Mode:** When mode is low **WR-RD Mode:** When mode is high
8	$\overline{RD}$	**WR-RD Mode** With $\overline{CS}$ low, the TRI-STATE data outputs (DB0-DB7) will be activated when $\overline{RD}$ goes low (see *Figure 4*). $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (t_I, ~800 ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (see *Figures 3a* and *3b*). **RD Mode** With $\overline{CS}$ low, the conversion will start with $\overline{RD}$ going low, also $\overline{RD}$ will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and $\overline{INT}$ going low indicates the completion of the conversion (see *Figure 2*).
9	$\overline{INT}$	**WR-RD Mode** $\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ will go low, ~800 ns (the preset internal time out, t_I) after the rising edge of $\overline{WR}$ (see *Figure 3b*); or $\overline{INT}$ will go low after the falling edge of $\overline{RD}$, if $\overline{RD}$ goes low prior to the 800 ns time out (see *Figure 3a*). $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see *Figures 3a* and *3b*). **RD Mode** $\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see *Figure 2*).
10	GND	Ground
11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: $GND \leq V_{REF}(-) \leq V_{REF}(+)$ (Note 5)
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-) \leq V_{REF}(+) \leq V_{CC}$ (Note 5)
13	$\overline{CS}$	$\overline{CS}$ must be low in order for the $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	TRI-STATE data output—bit 4
15	DB5	TRI-STATE data output—bit 5
16	DB6	TRI-STATE data output—bit 6
17	DB7	TRI-STATE data output—bit 7 (MSB)
18	$\overline{OFL}$	Overflow output—If the analog input is higher than the $V_{REF}(+)$, $\overline{OFL}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit).
19	NC	No connection
20	V_{CC}	Power supply voltage

1.0 Functional Description

1.1 GENERAL OPERATION

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (*Figure 1*). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled-data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

1.0 Functional Description (Continued)

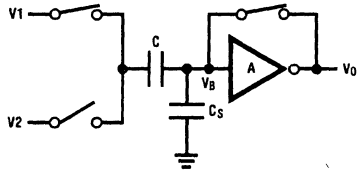
1.2 THE SAMPLED-DATA COMPARATOR

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively coupled input (*Figure 5*). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (*Figure 5a*) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_B, approximately 1.2V). In the second cycle (*Figure 5b*), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input (V_B') becomes

$$V_B - (V1 - V2)\frac{C}{C+C_S}$$

and the output will go high or low depending on the sign of $V_B' - V_B$.



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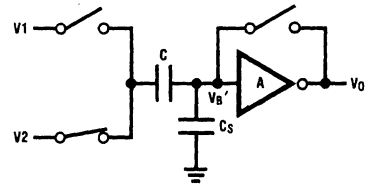
- $V_O = V_B$
- V on C = $V1 - V_B$
- C_S = stray input node capacitor
- V_B = inverter input bias voltage

FIGURE 5a. Zeroing Phase



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- $V_B' - V_B = (V2 - V1)\frac{C}{C+C_S}$
- $V_O' = \frac{-A}{C+C_S}[CV2 - CV1]$
- V_O' is dependent on V2 − V1

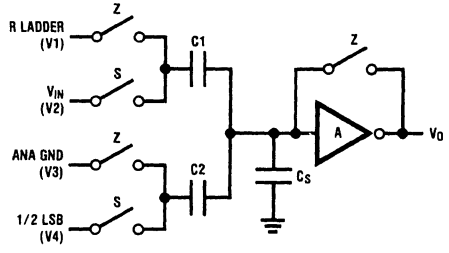
FIGURE 5b. Compare Phase

FIGURE 5. Sampled-Data Comparator

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (*Figure 6*), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor and opening all of the other switches (S switches). The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

1.3 ARCHITECTURE

In the ADC0820, one bank of 15 comparators is used in each 4-bit flash A/D converter (*Figure 7*). The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.



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$$V_O = \frac{-A}{C1+C2+C_S}[C1(V2-V1)+C2(V4-V3)]$$

$$= \frac{-A}{C1+C2+C_S}[\Delta Q_{C1}+\Delta Q_{C2}]$$

FIGURE 6. ADC0820 Comparator (from MS Flash ADC)

1.0 Functional Description (Continued)

Detailed Block Diagram

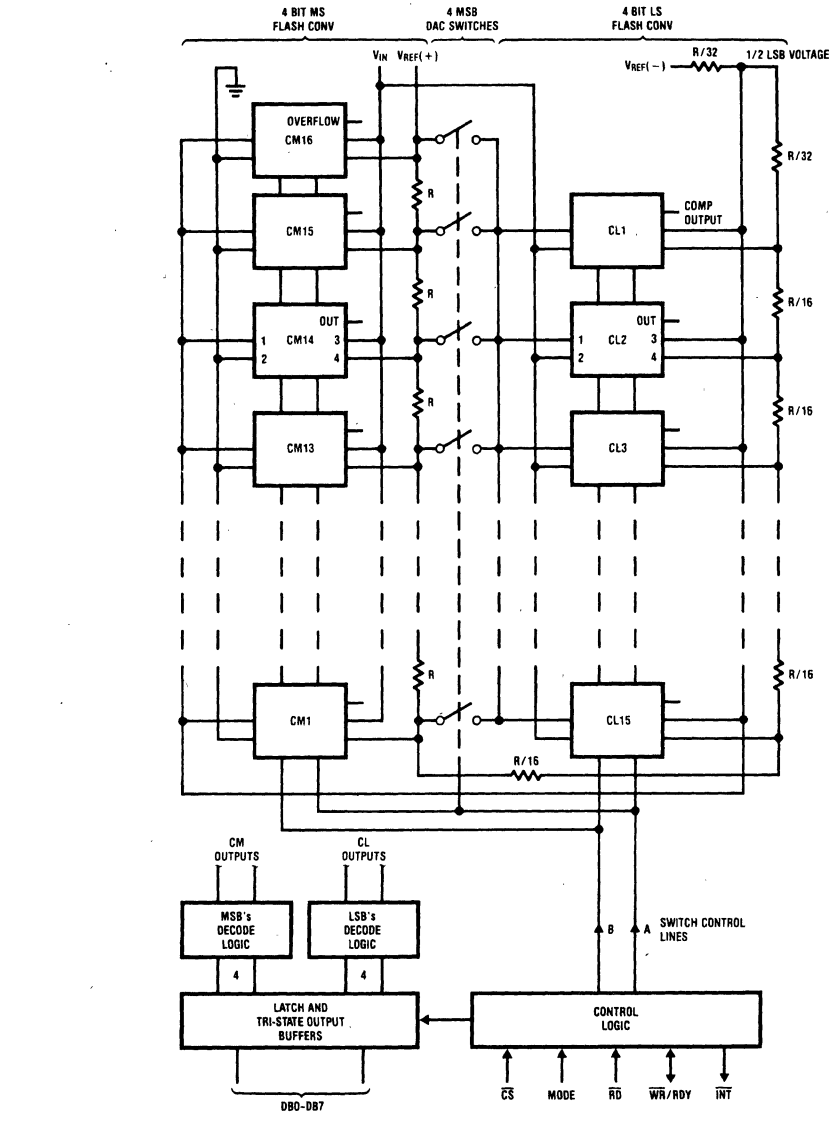

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FIGURE 7

1.0 Functional Description (Continued)

When a typical conversion is started, the $\overline{WR}$ line is brought low. At this instant the MS comparators go from zeroing to comparison mode (*Figure B*). When $\overline{WR}$ is returned high after at least 600 ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600 ns later, the $\overline{RD}$ line may be pulled low to latch the lower 4 data bits and finish the 8-bit conversion. When $\overline{RD}$ goes low, the flash A/Ds change state once again in preparation for the next conversion.

Figure B also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{WR}$ is low. In RD mode, sampling occurs during the first 800 ns of $\overline{RD}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant (Section 2.4), despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{WR}$ is low the MS flash is in compare mode (connected to V_{IN}), and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

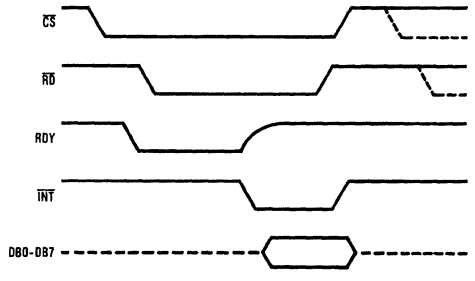
1.4 DIGITAL INTERFACE

The ADC0820 has two basic interface modes which are selected by strapping the MODE pin high or low.

RD Mode

With the MODE pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{RD}$ low until output data appears. An $\overline{INT}$ line is provided which goes low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

RD Mode (Pin 7 is Low)



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When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{RD}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800 ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800 ns, the lower 4 bits are recovered.

WR then RD Mode

With the MODE pin tied high, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{WR}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt driven scheme is desired, the user can wait for $\overline{INT}$ to go low before reading the conversion result (*Figure B*). $\overline{INT}$ will typically go low 800 ns after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 600 ns (*Figure A*). If this is done, $\overline{INT}$ will immediately go low and data will appear at the outputs.

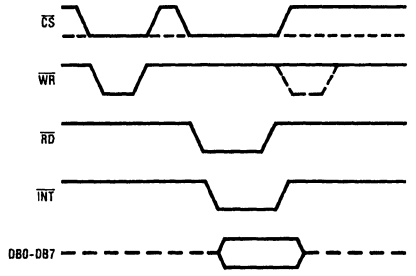

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FIGURE A. WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)

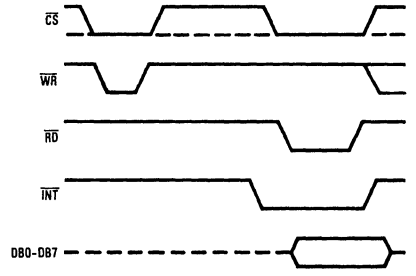

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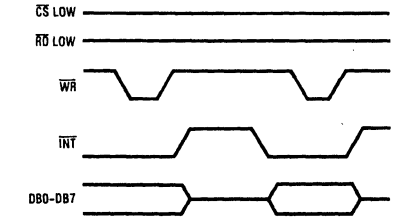
FIGURE B. WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

Stand-Alone

For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800 ns following $\overline{WR}$'s rising edge.

WR-RD Mode (Pin 7 is High) Stand-Alone Operation



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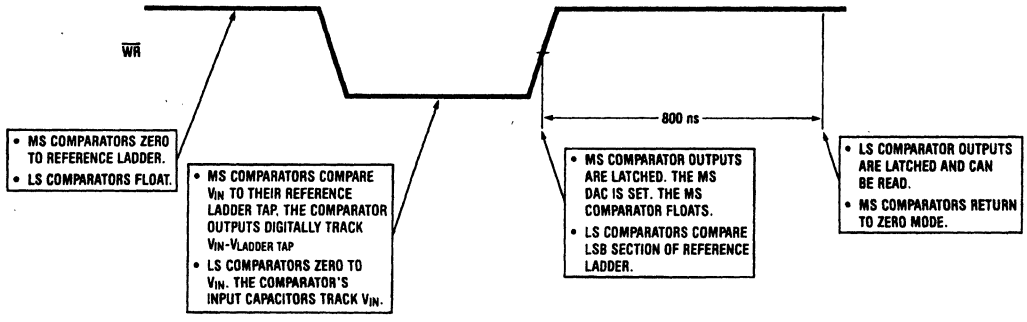
1.0 Functional Description (Continued)



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Note: MS means most significant
LS means least significant

FIGURE 8. Operating Sequence (WR-RD Mode)

OTHER INTERFACE CONSIDERATIONS

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50 μs. When the MS flash ADC's sampled-data comparators (Section 1.2) are in comparison mode ($\overline{WR}$ is low), the input capacitors (C, *Figure 6*) must hold their charge. Switch leakage and inverter bias current can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion (Section 1.3), a new conversion cannot be started until this phase is complete. The minimum spec for this time (t_P, *Figures 2, 3a, 3b,* and *4*) is 500 ns.

2.0 Analog Considerations

2.1 REFERENCE AND INPUT

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing $V_{REF}(V_{REF}=V_{REF}(+)-V_{REF}(-))$ to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF}=2V$ then 1 LSB=7.8 mV). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. *Figure 9* shows some of the configurations that are possible.

2.2 INPUT CURRENT

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

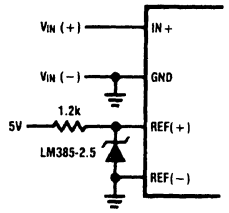
The equivalent input circuit of the ADC0820 is shown in *Figure 10a*. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, connecting V_{IN} to thirty-one 1 pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase (Section 1.3). In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5 kΩ to 10 kΩ). In addition, about 12 pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in *Figure 10b*. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800 ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is low. Since other factors force this time to be at least 600 ns, input time constants of 100 ns can be accommodated without special consideration. Typical total input capacitance values of 45 pF allow R_S to be 1.5 kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

2.0 Analog Considerations (Continued)

External Reference 2.5V Full-Scale



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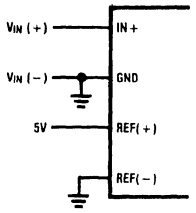
Power Supply as Reference



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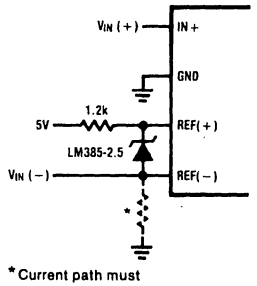
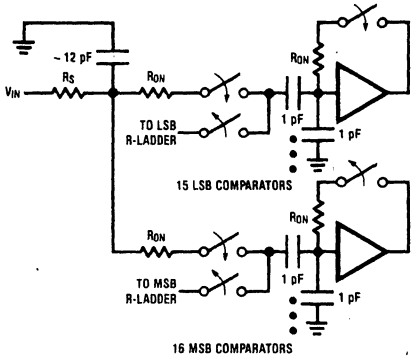
Input Not Referred to GND



*Current path must still exist from $V_{IN}(-)$ to ground

TL/H/5501–23

FIGURE 9. Analog Input Options



TL/H/5501–24

FIGURE 10a

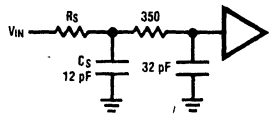


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FIGURE 10b

2.3 INPUT FILTERING

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600 ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal.

2.4 INHERENT SAMPLE-HOLD

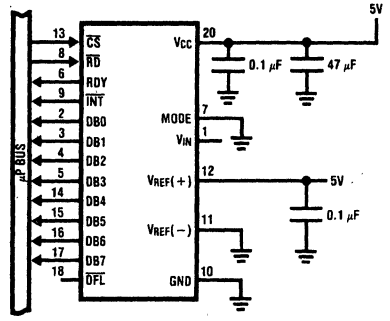
Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least ½ LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled-data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5 μs, the time through which V_{IN} must be 1/2 LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is low (Sections 1.3 and 2.2). Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100 ns after the rising edge of $\overline{WR}$ (100 ns due to internal logic prop delay) will be the measured value.

Input signals with slew rates typically below 100 mV/μs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1 μs would still not be able to measure a 5V 1 kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7 kHz waveforms.

3.0 Typical Applications

8-Bit Resolution Configuration



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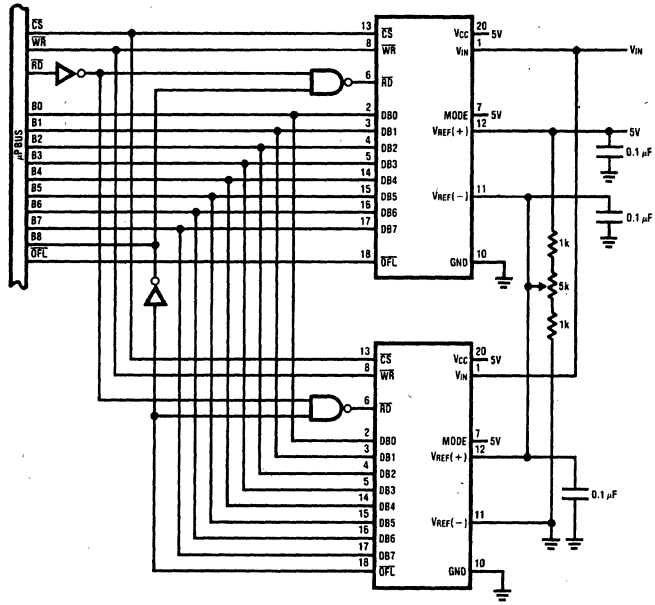
9-Bit Resolution Configuration



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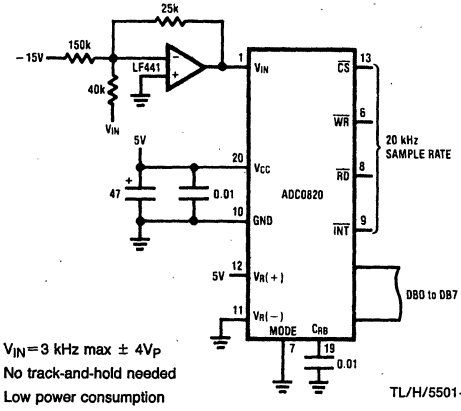
Telecom A/D Converter



- V_{IN} = 3 kHz max ± $4V_P$
- No track-and-hold needed
- Low power consumption

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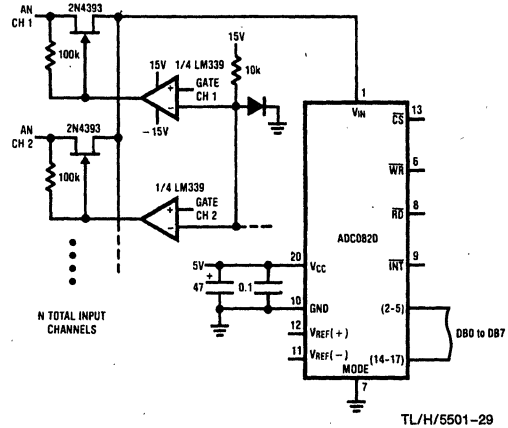
Multiple Input Channels



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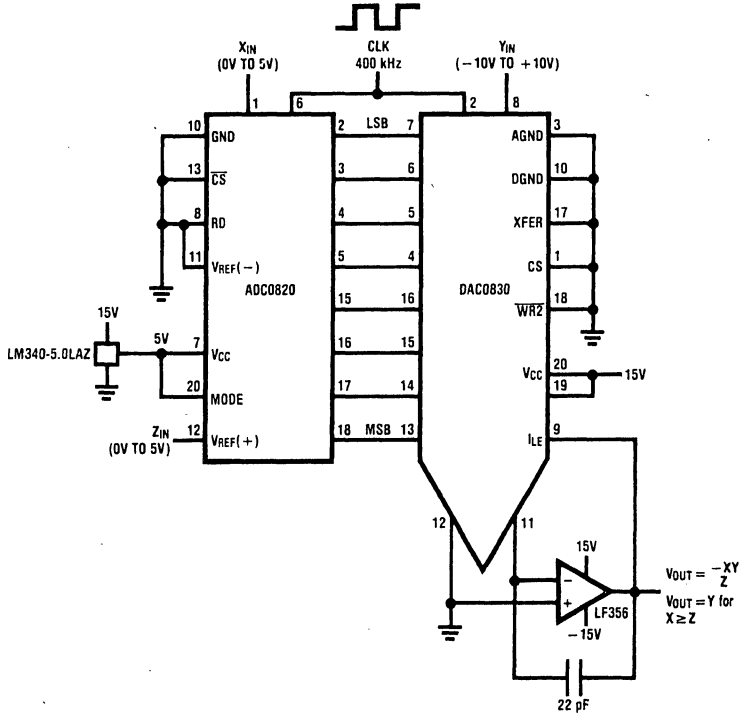
3.0 Typical Applications (Continued)

8-Bit 2-Quadrant Analog Multiplier



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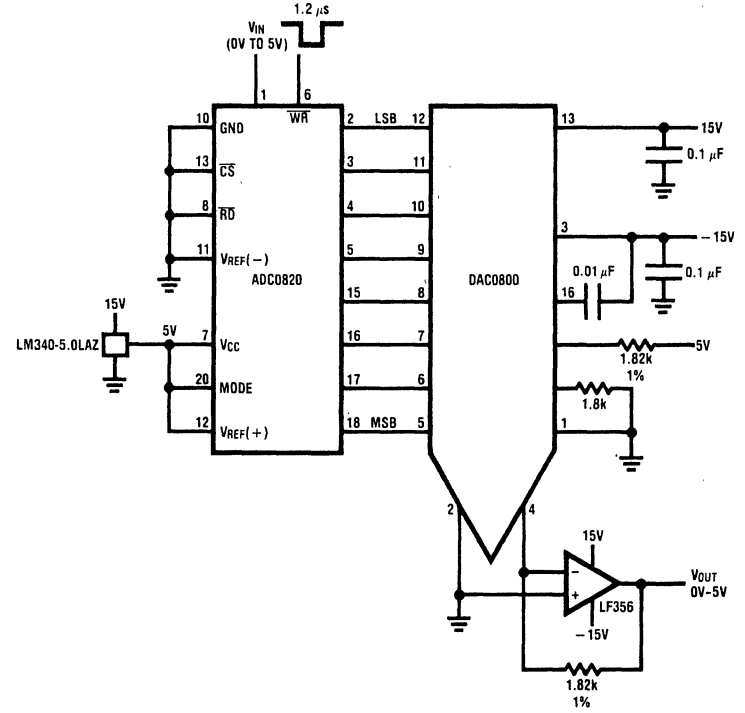
Fast Infinite Sample-and-Hold



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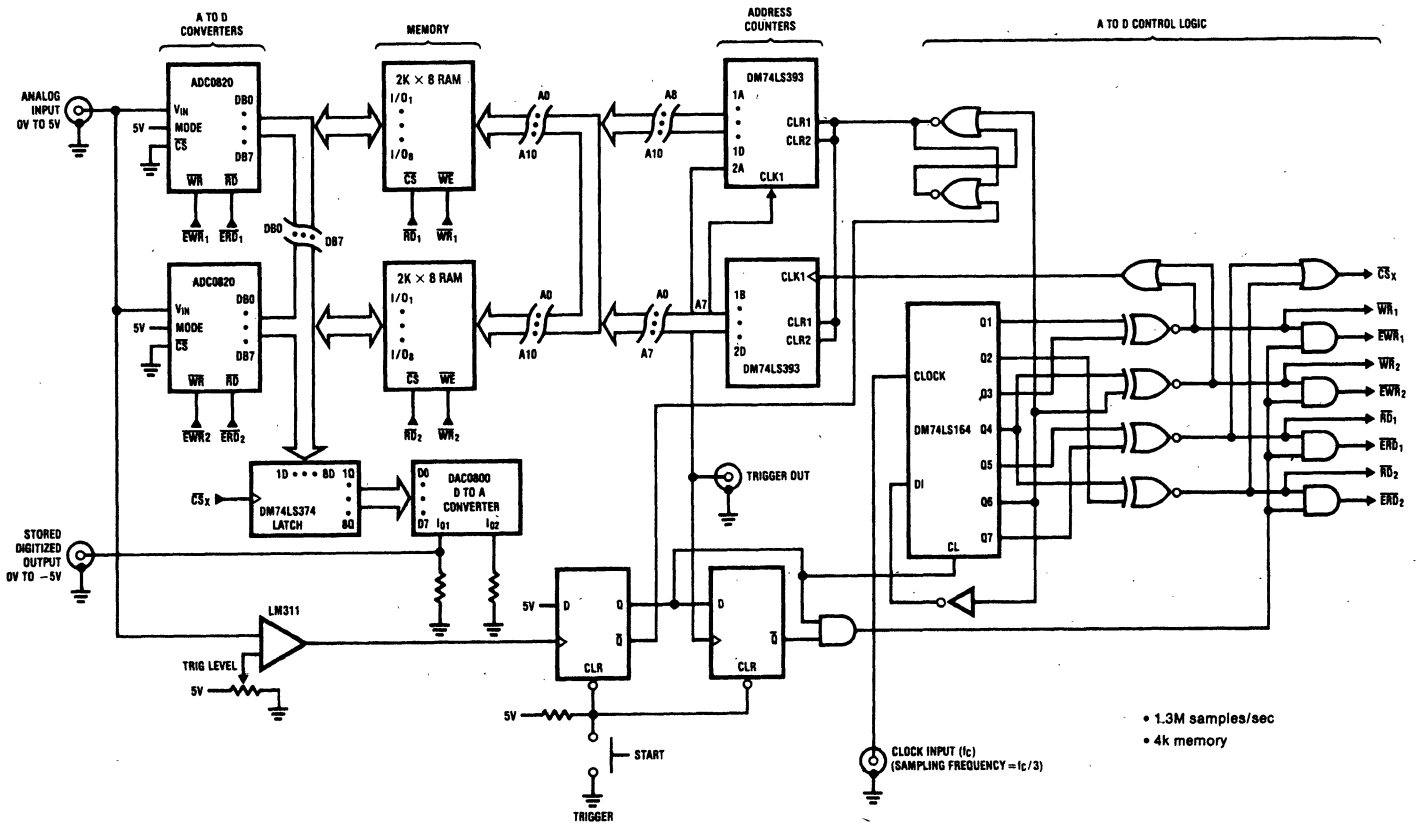
Digital Waveform Recorder



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Ordering Information

Temperature Range		0°C to +70°C	−40°C to +85°C	−55°C to +125°C
Error	±1/2 LSB Unadjusted	ADC0820BCN	ADC0820BCD	ADC0820BD
	±1 LSB Unadjusted	ADC0820CCN	ADC0820CCD	ADC0820CD
Package Outline		N20A—Molded DIP	D20A—Cavity DIP	D20A—Cavity DIP

National Semiconductor

ADC0829 μP Compatible 8-Bit A/D with 11-Channel MUX/Digital Input

General Description

The ADC0829 is an 8-bit successive approximation A/D converter with an 11-channel multiplexer of which six can be used as digital inputs, as well as, analog inputs.

This A/D is designed to operate from the μP data bus using a single 5V supply.

Channel selection, conversion control, software configuration and bus interface logic are all contained on this monolithic CMOS device.

This device contains three 16-bit registers which are accessed via double byte instructions. The control register is a write only register which controls the start of a new conversion, selects the channel to be converted, configures the 8-bit I/O port as input or output, and provides information for the 8-bit output register.

The conversion results register is a read only register which contains the current status and most recent conversion results. The discrete input register is also a read only register which contains the four address bits of the selected channel, and the six discrete inputs which are connected to the analog multiplexer.

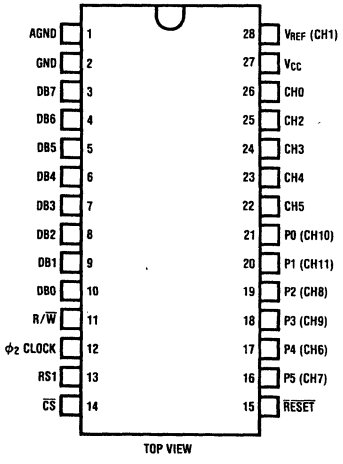
Key Specification

- Resolution 8 Bits
- Total Unadjusted Error ±½ LSB and ±1 LSB
- Conversion Time 256 μS
- Single Supply $5V_{DC}$
- Low Power 50 mW

Features

- No missing codes
- Operates ratiometrically or with analog span adjusted voltage reference
- 11-Channel multiplexer with latched control logic of which six can be used as digital inputs
- Easy interface to all microprocessors or operates "stand alone"
- 0 to 5V analog input range with single 5V supply
- T^2 L/MOS input/output compatible
- No zero or full scale adjusts required
- Standard 28-pin DIP
- Temperature range −40°C to +85°C

Connection and Block Diagrams



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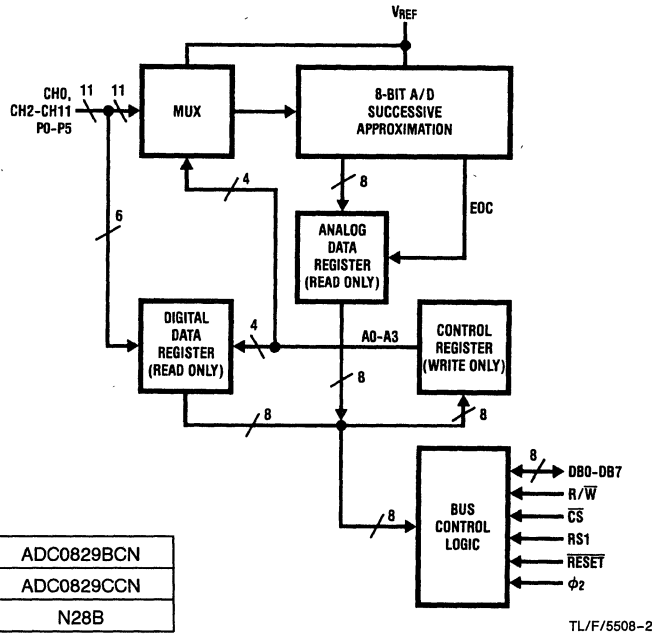


TL/F/5508–2

Ordering Information

Error	± 1/2 Bit Unadjusted	ADC0829BCN
	± 1 Bit Unadjusted	ADC0829CCN
Package Outline		N28B

Absolute Maximum Ratings

(Notes 1 and 2)

Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to V_{CC} + 0.3V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Storage Temperature	−65°C to + 150°C
Package Dissipation at T_A = 25°C (Board Mount)	
Lead Temp. (Soldering, 10 seconds)	300°C
Input Current Per Pin	±5 mA
Package	+20 mA

Operating Conditions (Notes 1 and 2)

Supply Voltage, V_{CC}	4.75 V_{DC} to 5.5 V_{DC}
Temperature Range	−40°C to + 85°C

Converter and Multiplexer Electrical Characteristics

$V_{CC}=5V_{DC}=V_{REF}(+)$, $V_{REF}(-)=GND$, SCLK $\phi_2=1.048$ MHz, $-40°C \le T_A + 85°C$ unless otherwise noted.

Parameter	Conditions		Min	Typ (Notes)	Max	Units
Total Unadjusted Error; (Note 3)						
ADC0829BCN	V_{REF} Forced to 5.000 V_{DC}				±½	LSB
ADC0829CCN	V_{REF} Forced to 5.000 V_{DC}				±1	LSB
Reference Input Resistance			1.0	4.5		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)		GND-0.10		V_{CC}+0.10	V
$V_{REF}(+)$ Voltage, Top of Ladder	Measured at REF(+)			V_{CC}	V_{CC}+0.01	V
$\frac{V_{REF}(+)+V_{REF}(-)}{2}$ Voltage, Center of Ladder			$V_{CC/2}-0.1$	$V_{CC/2}$	$V_{CC/2}+0.01$	V
$V_{REF}(-)$ Voltage, Bottom of Ladder	Measured at REF(−)		−0.1	0		V
I_{OFF}, Off Channel	ON Channel=5V	ADC0829BCN			±400	nA
Leakage Current (Note 6)	OFF Channel=0V	ADC0829CCN			±1	μA
I_{ON}, On Channel	ON Channel=0V	ADC0829BCN			±400	nA
Leakage Current (Note 6)	OFF Channel=5V	ADC0829CCN			±1	μA

AC Characteristics

$V_{CC}=V_{REF}(+)=5V$, $t_r=t_f=20$ ns and $T_A=25°C$ (Note 7) unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
$t_{CYC}(\phi_2)$, ϕ_2 Clock Cycle Time ($1/f_{\phi 2}$)		0.943		10.0	μs
$PW_H(\phi_2)$, ϕ_2 Clock Pulse Width, High		440			ns
$PW_L(\phi_2)$, ϕ_2 Clock Pulse Width, Low		410			ns
$t_r(\phi_2)$, ϕ_2 Rise Time				25	ns
$t_f(\phi_2)$, ϕ_2 Fall Time				30	ns
t_{AS}, Address Set Up Time	RS1, R/$\overline{W}$, $\overline{CS}$	145			ns
t_{DDR}, Data Delay (Read)	DB0-DB7			335	ns
t_{DSW}, Data Delay Setup (Write)	DB0-DB7	185			ns
t_{AH}, Address Hold Time	RS1, R/$\overline{W}$, $\overline{CE}$	20			ns
t_{DHW}, Input Data Hold Time	DB0-DB7	20			ns
t_{DHR}, Output Data Hold Time	DB0-DB7	10			ns
Analog Channel Settling Time		32			Clocks
t_c, Conversion Time		256			Clocks

Digital and DC Characteristics V_{CC} = 4.5V to 5.5V and $-40°C \leq T_A \leq 85°C$ unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Bus Control Inputs (R/$\overline{W}$, ENABLE $\overline{RESET}$, RS1, $\overline{CS}$) and Peripheral Inputs (P0-P5)					
$V_{IN}(1)$, Logical "1" Input Voltage		2.0			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.8	V
I_{IN}, Input Leakage Current				±1	μA
ϕ_2 CLOCK INPUT					
$V_{IN}(1)$, Logical "1" Input Voltage		$V_{CC}-0.8$			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.4	V
Data Bus (DB0-DB7)					
$V_{IN}(1)$, Logical "1" Input Voltage		2.0			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.8	V
I_{OUT}, TRI-STATE® Output Current	$V_{OUT}=0V$			−10	μA
	$V_{OUT}=5V$			10	μA
$V_{OUT}(1)$, Logical "1" Output Voltage	$I_{OUT}=-1.6$ mA	2.4			V
$V_{OUT}(0)$, Logical "0" Output Voltage	$I_{OUT}=1.6$ mA			0.4	V
Power Supply Requirements					
I_{CC}, Supply Current				10	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of device may be impaired.

Note 2: All voltages are measured with respect to ground.

Note 3: Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.

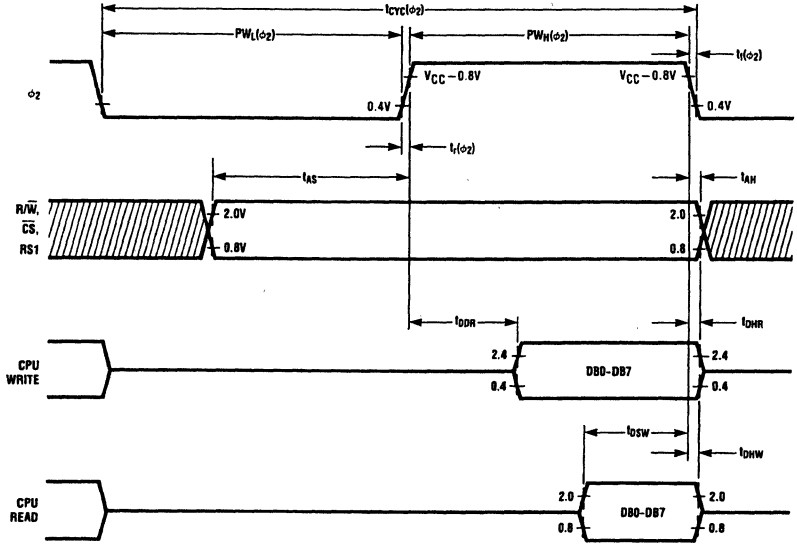
Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.90 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Off channel leakage current is measured after the channel selection.

Note 7: The temperature coefficient is 0.3%/°C.

Timing Diagram



TL/F/5508–3

Pin Description

ANALOG AND DIGITAL INPUTS

CH0, CH2-CH5—These are dedicated analog inputs. They are fed directly to the internal 12 to 1 multiplexer which feeds the A/D converter.

P0-P5/CH6-CH11—These 6 pins are dual purpose and may be used as either TTL compatible digital inputs, or analog inputs. When used as digital inputs they may be read via the discrete input register. When they are used as analog inputs they function like CH-0, CH2-5.

MICROPROCESSOR INTERFACE SIGNALS

DB0-DB7—The bi-directional data lines for the data bus connect to the μP's main data bus to enable data transfer to and from the μP. DB0-DB7 remain in a high impedance state unless the ADC0829 is read.

ϕ_2 Clock—This signal is used for two purposes. First it synchronizes data transfer in and out of the ADC. Second, it is the master clock for the A/D converter logic and all other timing signals are derived from it.

R/$\overline{W}$—The read/write pin controls the direction of data transfer on D0-D7.

$\overline{RESET}$—A low on this pin forces the ADC0829 into a known state. The start bit is cleared, Channel CH0 is selected and the internal byte counter is reset to the MS Byte. The A/D data register is not reset. Reset must be held low for at least 3 clocks.

$\overline{CS}$—Chip Select must be low in order for data transfer between the ADC0829 and the μP to occur.

RS1—The Register Select pin is used to address the internal registers.

POWER SUPPLY PINS

V_{CC}—This is the positive 5V supply pin. It powers the digital load and the sample data comparator. Care should be exercised to ensure that supply noise on this pin is adequately filtered, by using a bypass capacitor from V_{CC} to D_{GND}.

D_{GND}—Digital ground should be connected to the systems digital ground.

V_{REF} and A_{GND}—The positive reference pin attaches to the top of the 256R resistor ladder and sets the full scale conversion voltage value. The A_{GND} connects to the bottom of the ladder. The conversion result is ratiometric to V_{REF} - A_{GND} and hence both V_{REF} and A_{GND} should be noise free. Ideally the V_{REF} and A_{GND} should be single point connected to the analog transducer's supply. The V_{REF} and A_{GND} voltages typically are 5V and Ground but they may be varied so long as $(V_{REF}-A_{GND})/2 = V_{CC}/2 \pm 0.1V$.

Functional Description

1.0 CONTROL LOGIC

The Control Logic interprets the microprocessor control signals and decodes these signals to perform the actual functions of selecting, reading, writing, enabling the outputs, etc.

2.0 STATE DESCRIPTIONS

There are three internal states within the A/D converter: the NO OP state; the sample state; and the converting state.

The NO OP state is a stable state since the external stimulus (e.g. start conversion signal) is needed for a state transition.

The first transient state is sampling the input. The first 32 clocks of the conversion are used for acquiring the channel; this settling time allows any transients to decay before conversion begins. The second transient state is the actual conversion. The conversion is completed in 256 clocks and the conversion results register is updated. The converter then returns to the stable NO OP state awaiting further instructions.

The device has no comparator bias current and draws minimal power during the NO OP state.

3.0 INITIALIZATION

The device is initialized by an active low on $\overline{RESET}$. All outputs are initialized to the inactive state and the converter placed in its NO OP state. The data register is not affected by $\overline{RESET}$. System TRI-STATE outputs are initialized to the high impedance state.

4.0 CONVERSION CONTROL

The program normally initiates a conversion cycle with a double write command. (See control word format.) The control word selects a channel, configures the peripheral I/O, and provides peripheral data information. The conversion is initiated by setting the SC bit in the control word high.

The converter then resets the start conversion bit and begins the conversion cycle.

When the conversion is complete and the new conversion results transferred to the data register, the status bit is set. The status bit is not reset when the conversion status is read. A full double byte write into the control word will reset the status bit, or a low level at master $\overline{RESET}$.

If a new conversion command occurs during a conversion, the conversion is aborted and a new channel acquisition phase will immediately begin.

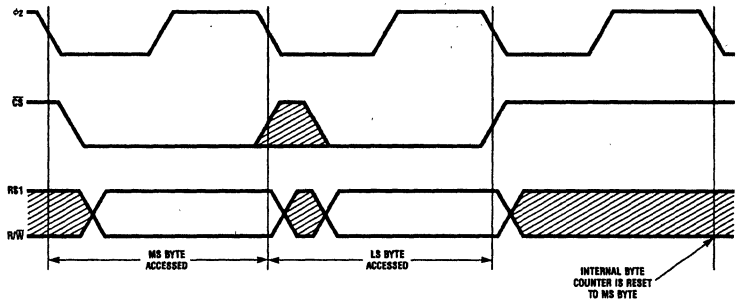
5.0 CONTROL STRUCTURE

The control logic continually monitors the control bus waiting for $\overline{CS}$ to go low and ϕ_2 to go high. When this condition occurs, the internal decoder, which has already selected the proper function, activitates.

The byte counter will always select the most significant (MS) half first, and the least significant (LS) half second. Single byte instructions will always access the MSB portion of any word. After a single byte instruction the byte counter will return to the MSB portion of a word when $\overline{CS}$ is high for a full clock cycle. A 16-bit read or write is accomplished by using a 16-bit load or store instruction which transfers each byte on consecutive clock cycles. This timing is shown in *Figure 1*. A single byte instruction is especially useful for reading the status bit during a polled interrupt. *Figure 2* shows the basic A/D conversion timing sequence and flow.

Functional Description (Continued)

Timing for a Typical μP 16 Byte Access



Timing for a Typical μP 8 Byte Access

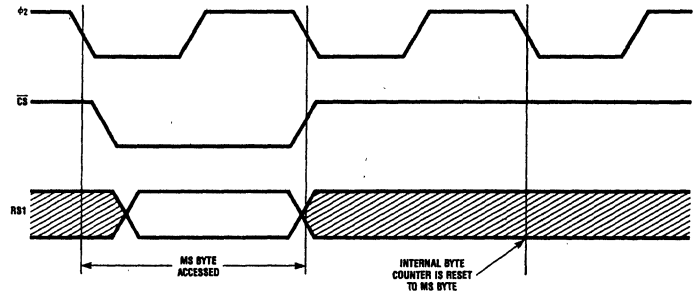


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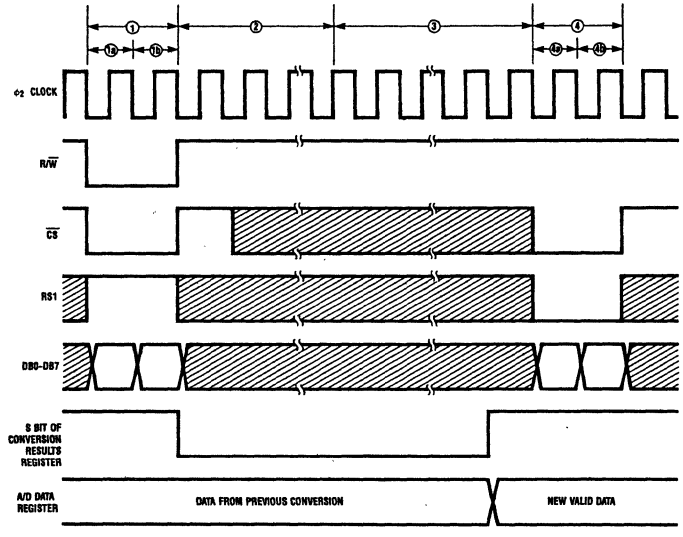
FIGURE 1



① START CONVERSION
  ⓐ SET SC BIT TO A 1
  ⓑ LOAD ADDRESS
② ANALOG INPUT SETTLING TIME ALLOWS INTERNAL MULTIPLEXER TO SELECT A CHANNEL AND STABILIZE (~32 CLOCKS).
③ A/D CONVERSION TIME (~256 CLOCKS)
④ READ END OF CONVERSION DATA
  ⓐ EOC BIT READ IF A 1 CONVERSION COMPLETE.
  ⓑ A/D DATA REGISTER READ. IF EOC = 1, THEN NEW VALID DATA.

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FIGURE 2. A/D Conversion Timing Sequence

Functional Description (Continued)

6.0 WORD FORMAT

6.1 Control Register Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
X	X	X	X	X	X	X	(LSB) SC	X	X	X	X	A3 CH3	A2 CH2	A1 CH1	A0 CH0

X: Don't Care

SC: Start Conversion
1 = Start new conversion
0 = Do not start new conversion

CH3-CH0: Channel Address

Hex Value	Definition
0	Select CH0
1	Select $V_{ref}(+)$
2-5	Select Channels CH2-CH5
6-9	Undefined
A-F	Select CH7-CH10

6.2 Conversion Results Register Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
S	0	0	0	0	0	0	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

S: Status
1 = Data is valid (conversion complete)
0 = Data is not valid

C_7-C_0: 8 bit converted result

6.3 Discrete Input Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
P5	P4	P3	P2	P1	P0	CH3	CH2	CH1	CH0	0	0	0	0	0	0

CH3-CH0: Status of channel address

P5-P0: Status of P5-P0 interpreted as discrete digital inputs

ADU ADDRESS SELECTION

CSO*	R/W	RSI	Description
1	X	X	Do not respond
0	0	0	Write NO OP
0	0	1	Write Control Word
0	1	0	Read Conversion Results
0	1	1	Read Discrete Inputs

Note: All words are transferred as two 8-bit bytes, MSB transferred first LSB transferred second.

7.0 ANALOG TO DIGITAL CONVERTER

The ADC0829 A/D Converter is composed of three major sections: the successive approximation register (SAR); the 256R ladder and analog decoder; and the sample-data comparator.

7.1 Successive Approximation

The analog signal at the A/D input is compared eight times to various ladder voltages to determine which of the 256 voltages in the ladder most closely approximates the input voltage. This stochastic technique is accomplished by converging on the proper tap in the ladder by simple iterative convergence. There are nine posting registers in the SAR which contain the position of the bit being tested and eight latching registers which remember if the comparison was high or low. Starting with the MSB and continuing downward each bit is set high by the posting register. The analog tree decoder selects the corresponding tap in the ladder and the A/D input is compared to that voltage. If the comparison is positive the latch remains set, so higher voltages in the ladder are checked next. If the comparison is negative the bit is reset so lower ladder voltages are sought.

After all eight comparisons are made, the contents of the latching register are transferred to a data register, thus the A/D can perform a new conversion while the previous results remain available.

7.2 256R Ladder

The ladder is a very accurate voltage divider which divides the reference voltage into 256 equal steps. Special consideration was given to the ladder terminations at each end, and also the center, to ensure consistent and accurate voltage steps. The use of a 256R ladder guarantees monotonicity since only a single voltage gradient across the ladder exists. Shorted or unequal resistors in the ladder may cause non-uniform steps but cannot cause a nonmonotonic response so often fatal in closed loop system applications. (See *Figure 3.*)

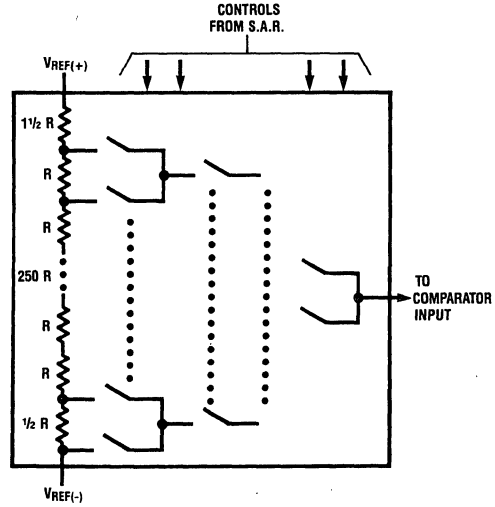

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FIGURE 3. Resistor Ladder and Switch Tree

Functional Description (Continued)

Actually of the 256 resistors in the ladder, 254 have the same value while the end point resistors are equal to 1-1/2R and 1/2R. This ensures the system output characteristic is symmetrical with the zero and full scale points of its input to output, or transfer curve.

The tree decoder routes the 256 voltages from the ladder to a single point at the comparator input. This allows comparisons between the A/D input and any voltage the SAR directs the decoder to route to the comparator.

Since the ladder is dependent upon only the matching of resistors, the voltages it generates are very stable with temperature and have excellent repeatability and long term drift.

8.0 MULTIPLEXER

8.1 Analog Inputs

The analog multiplexer selects one of 11 channels and directs them to the input of the A/D converter. The multiplexer was designed to minimize the effects of leakage currents and multiplexer output capacitance.

Special input protection is used to prevent damage from static voltages or voltages exceeding the specified range from $-0.3V$ to $V_{CC}+0.3V$. However, normal precautions are recommended to avoid such situations whenever possible.

8.2 Digital Inputs

Six of the analog inputs can also be used as digital inputs to sense TTL voltage levels. Care must be taken when these inputs are interpreted since TTL levels may not always be present.

8.3 A/D Comparator

Probably the most important section of the A/D converter is the comparator since the comparator's offset voltage and stability determine the converter's ultimate accuracy. The low voltage offset of the chopper-stabilized comparator of this converter optimizes performance by minimizing temperature dependent input offset errors as well as drift.

The dc signal appearing at the amplifier input is converted to an ac signal, amplified by an ac amplifier and restored to a dc signal. The drift of the comparator is minimized since the drift signal is a dc component blocked by the ac amplifier.

The comparator has very high input impedance to dc voltages since it looks like a capacitor. Because the comparator is chopping the dc voltages at the input, the difference between the A/D input voltage and ladder voltage appears on the comparator's input capacitor. The input voltage difference, chopping frequency, and comparator input capacitor causes a CVF current. The CVF current is a small bias current which will not produce any error when the A/D input is connected to a low impedance voltage source. If the voltage source has an output impedance of less than 10k, the error is still insignificant since the bias current exponentially decays.

Adding a capacitor to the input of the comparator integrates the exponential charging current converting it into dc bias current. (See Figure 1.) Two main considerations on the integration capacitor are charge sharing with a filter capacitor and settling time.

9.0 BUS INTERFACE

The ADC0829 communicates to the microprocessor through an 8-bit I/O port. The I/O port is composed of a TTL to CMOS buffer and a TRI-STATE® output driver.

The TTL to CMOS Buffer translates the TTL voltage levels into CMOS levels very rapidly and is quite stable with supply and temperature. The buffer has a small amount of hysteresis (about 100 mV) to improve both noise immunity and internal rise and fall times.

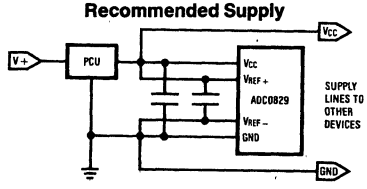
The TRI-STATE bus driver is a bipolar and N-channel pair that easily drive the bus capacitance. Since the bus drivers collectively can sink or source a quarter of an amp total, a non-overlap circuit is used which guarantees that only one of the two drive transistors is on at a time.

Since this output drives the bus capacitance, even the non-overlapping circuit cannot prevent noise on V_{CC}. The amount of noise depends on the V_{CC} current used to charge the bus capacitance.

The external filter capacitor on V_{CC} provides some of the transient current while the bus is being driven. A capacitor with good ac characteristics and low series resistance is a good choice to prevent V_{CC} transients from affecting accuracy.

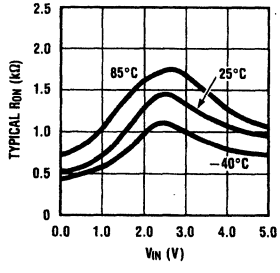
Application Information

Recommended Supply



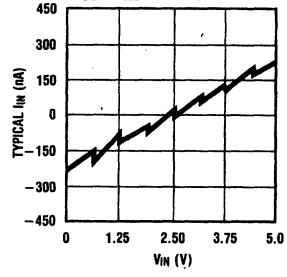
TL/F/5508-7

Multiplexer R_{ON} vs V_{IN} ($V_{CC}=V_{REF}=5V$)



TL/F/5508-8

Comparator I_{IN} vs V_{IN} ($V_{CC}=V_{REF}=5V$, $f_C=1.048$ MHz)



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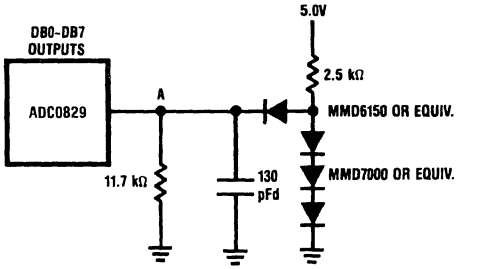
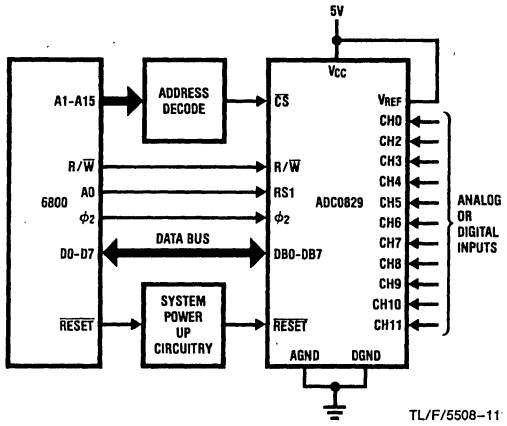
Data Bus Test Circuit



TL/F/5508–10

Typical Application



TL/F/5508–11

National Semiconductor

ADC0831, ADC0832, ADC0834 and ADC0838 (COP431, COP432, COP434 and COP438) 8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or μPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

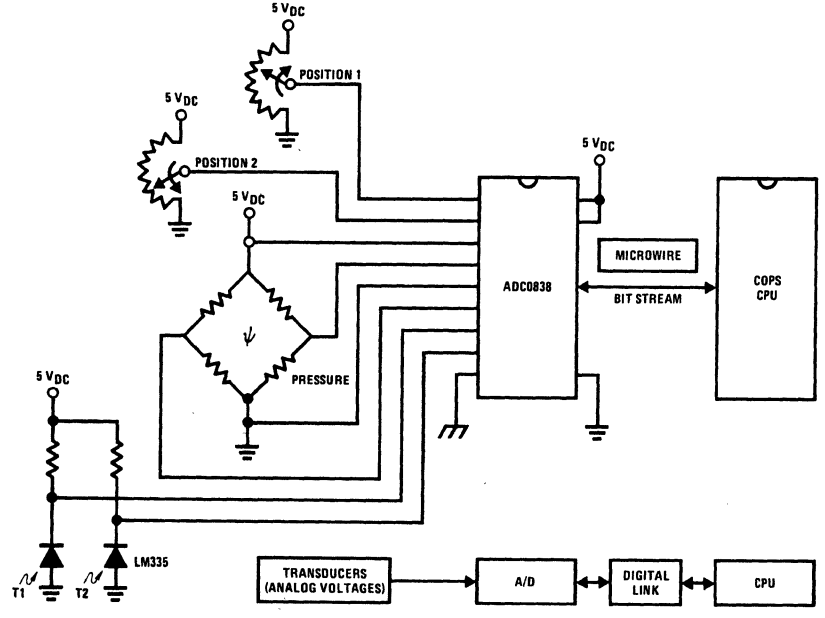
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T^2L/MOS input/output compatible
- 0.3" standard width, 8-, 14- or 20-pin DIP package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	32 μs

Typical Application



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Absolute Maximum Ratings (Notes 1 & 2)

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to +15V
Analog Inputs	−0.3V to V_{CC} +0.3V
Input Current per Pin	±5 mA
Package	±20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0831/2/4/8BJ	−55°C to +125°C
ADC0831/2/4/8CJ	
ADC0831/2/4/8BCJ	−40°C to +85°C
ADC0831/2/4/8CCJ	
ADC0831/2/4/8BCN	−0°C to +70°C
ADC0831/2/4/8CCN	

Converter and Multiplexer Electrical Characteristics

The following specifications apply for $V_{CC} = V+ = 5V$, $T_A = T_j = 25°C$, and $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BCJ and CCJ Devices			BCN and CCN Devices			Units
		Typ (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	Typ (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Total Unadjusted Error	V_{REF} = 5.00 V (Note 4)							
ADC0831/2/4/8BCN			+½			±½	±½	LSB
ADC0831/2/4/8BJ			±½			±½		
ADC0831/2/4/8BCJ			±½					
ADC0831/2/4/8CCN						±1	±1	
ADC0831/2/4/8CJ			±1					
ADC0831/2/4/8CCJ			±1					
Minimum Reference Input Resistance		2.4	**1.3**		2.4	1.3	**1.3**	kΩ
Maximum Reference Input Resistance		2.4	**5.9**		2.4	5.4	**5.4**	kΩ
Maximum Common-Mode Input Range (Note 5)			**V_{CC} +0.05**			V_{CC} +0.05	**V_{CC} +0.05**	V
Minimum Common-Mode Input Range (Note 5)			**GND −0.05**			GND −0.05	**GND −0.05**	V
DC Common-Mode Error		±1/16	±¼	±¼	±1/16	±¼	±¼	LSB
Change in zero error from V_{CC} = 5V to internal zener operation (Note 3)	15 mA into V+ V_{CC} = N.C. V_{REF} = 5V		**1**			1	**1**	LSB
V_Z, internal diode breakdown (at V+) (Note 3) MIN	15 mA into V+		**6.3**			6.3	**6.3**	V
MAX			**8.5**			8.5	**8.5**	
Power Supply Sensitivity	V_{CC} = 5V ± 5%	±1/16	±¼	±¼	±1/16	±¼	±¼	LSB
I_{OFF}, Off Channel Leakage Current (Note 6)	On Channel = 5V Off Channel = 0V		**−1**			−1	**−1**	µA
	On Channel = 0V Off Channel = 5V		**+1**			+1	**+1**	µA
I_{ON}, On Channel Leakage Current (Note 6)	On Channel = 0V Off Channel = 5V		**−1**			−1	**−1**	µA
	On Channel = 5V Off Channel = 0V		**+1**			+1	**+1**	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to ground.

Note 3: Internal zener diodes (6.3 to 8.5V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore guaranteed for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+. (See *Figure 3*)

Note 4: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

Converter and Multiplexer Electrical Characteristics (Continued)

The following specifications apply for $V_{CC}=V+=5V$, $T_A=T_j=25°C$, and $f_{CLK}=250$ kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BCJ and CCJ Devices			BCN and CCN Devices			Units
		Typ (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	Typ (Note 9)	Tested Limit (Note 10)	Design Limit (Note 11)	
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	$V_{CC}=5.25V$		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	$V_{CC}=4.75V$		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	$V_{IN}=5.0V$	0.005	**1**		0.005	1	**1**	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	$V_{IN}=0V$	−0.005	**−1**		−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	$V_{CC}=4.75V$ $I_{OUT}=-360$ μA $I_{OUT}=-10$ μA		**2.4** **4.5**			2.4 4.5	**2.8** **4.6**	V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	$V_{CC}=4.75V$ $I_{OUT}=1.6$ mA		**0.4**			0.4	**0.34**	V
I_{OUT}, TRI-STATE Output Current (Max)	$V_{OUT}=0V$ $V_{OUT}=5V$	−0.01 0.01	**−3** **3**		−0.01 0.01	−3 +3	**−3** **+3**	μA μA
I_{SOURCE}, Output Source Current (Min)	$V_{OUT}=0V$	−14	**−6.5**		−14	−6.5	**−7.5**	mA
I_{SINK}, Output Sink Current (Min)	$V_{OUT}=V_{CC}$	16	**8.0**		16	8.0	**9.0**	mA
I_{CC}, Supply Current (Max) ADC0831, ADC0834, ADC0838		1	**2.5**		1	2.5	**2.5**	mA
ADC0832	Includes Ladder Current	3	**7.2**		3	7.2	**7.2**	mA

AC Characteristics

The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20$ ns and 25°C unless otherwise specified.

Parameter		Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
f_{CLK}, Clock Frequency	Min Max			10	 400	kHz kHz
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 7)	Min Max				40 60	% %
t_{SET-UP}, CS Falling Edge or Data Input Valid to CLK Rising Edge					250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge					90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 8)		$C_L=100$ pF Data MSB First Data LSB First	 650 250		 1500 600	 ns ns
t_{1H}, t_{0H},—Rising Edge of CS to Data Output and SARS Hi-Z		$C_L=10$ pF, $R_L=10k$ (see TRI-STATE® Test Circuits)	125		250	ns
		$C_L=100$ pf, $R_L=2k$		500		ns
C_{IN}, Capacitance of Logic Input			5			pF
C_{OUT}, Capacitance of Logic Outputs			5			pF

Note 5: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 6: Leakage current is measured with the clock not switching.

Note 7: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 1 μs.

Note 8: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

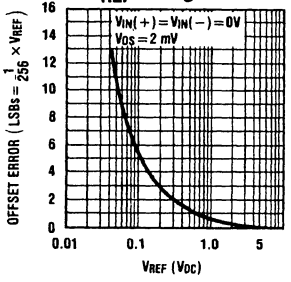
Note 9: Typicals are at 25°C and represent most likely parametric values.

Note 10: Guaranteed and 100% production tested.

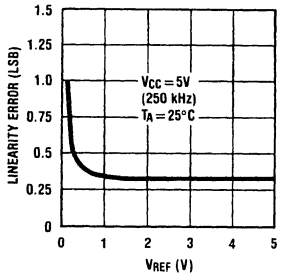
Note 11: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Performance Characteristics

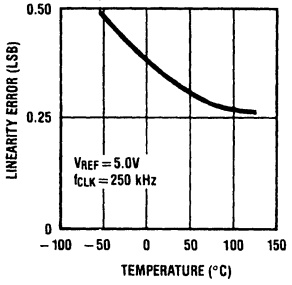
Unadjusted Offset Error vs V_{REF} Voltage



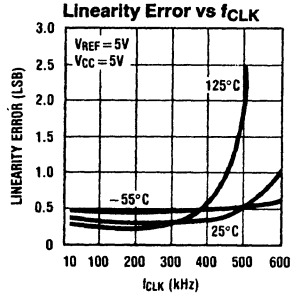
Linearity Error vs V_{REF} Voltage



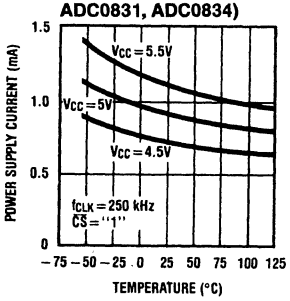
Linearity Error vs Temperature



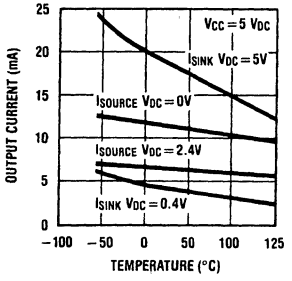
Linearity Error vs f_{CLK}



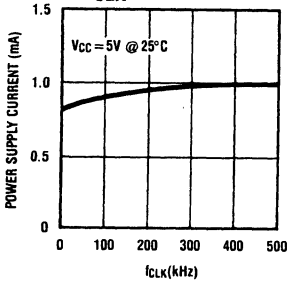
Power Supply Current vs Temperature (ADC0838, ADC0831, ADC0834)



Output Current vs Temperature



Power Supply Current vs f_{CLK}



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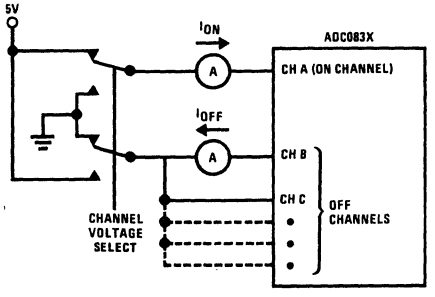
Note: For ADC0832 and I_{REF}

Leakage Current Test Circuit



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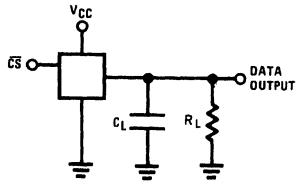
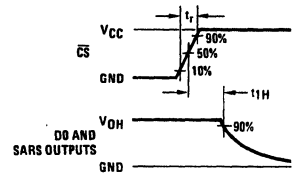
TRI-STATE Test Circuits and Waveforms

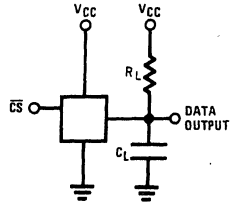
t_{1H}



t_{1H}



t_{0H}



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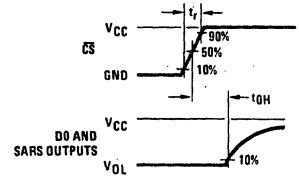
t_{0H}



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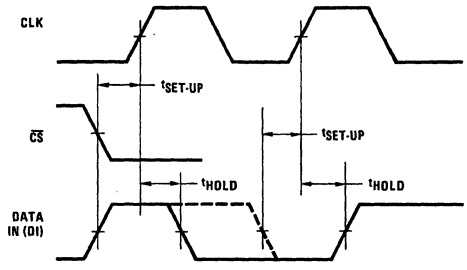
Timing Diagrams

Data Input Timing



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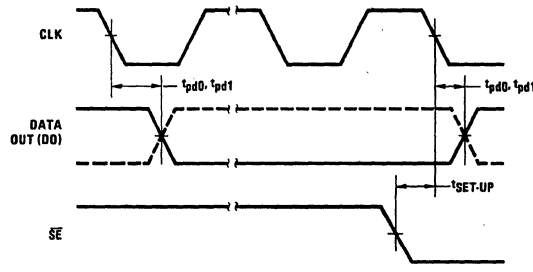
Data Output Timing



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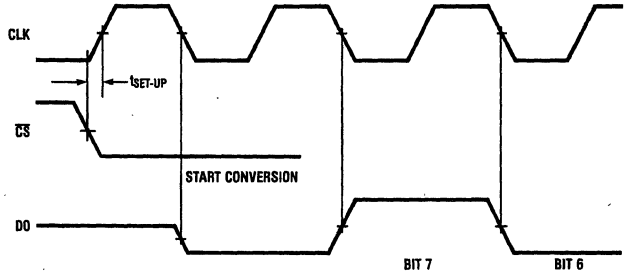
ADC0831 Start Conversion Timing



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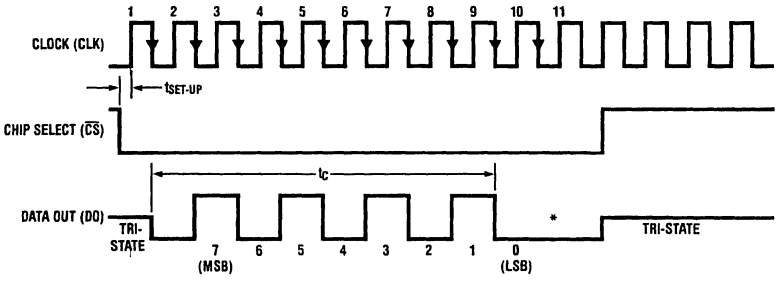
Timing Diagrams (Continued)

ADC0831 Timing



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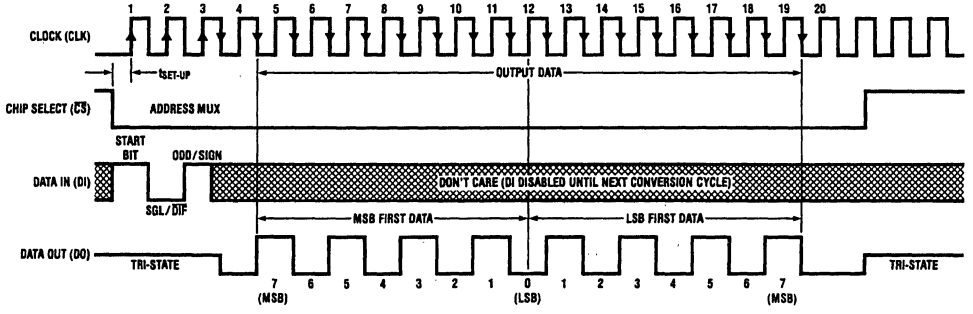
ADC0832 Timing



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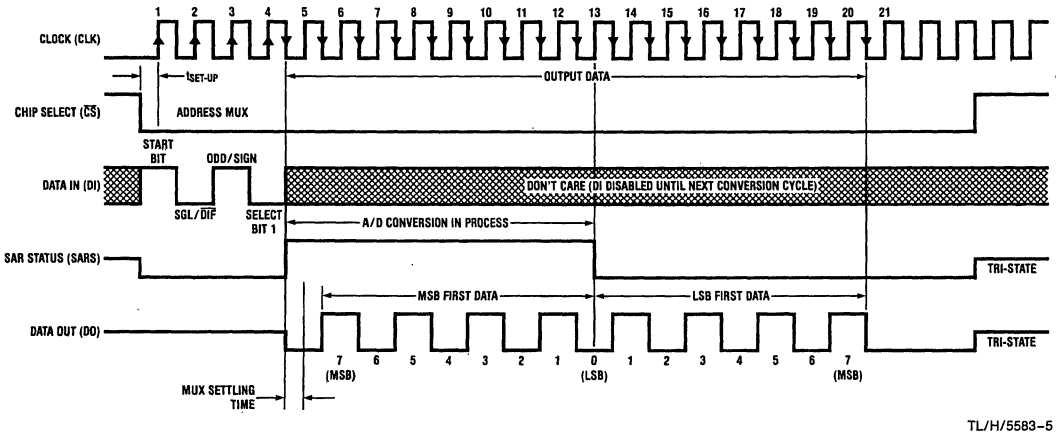
ADC0834 Timing



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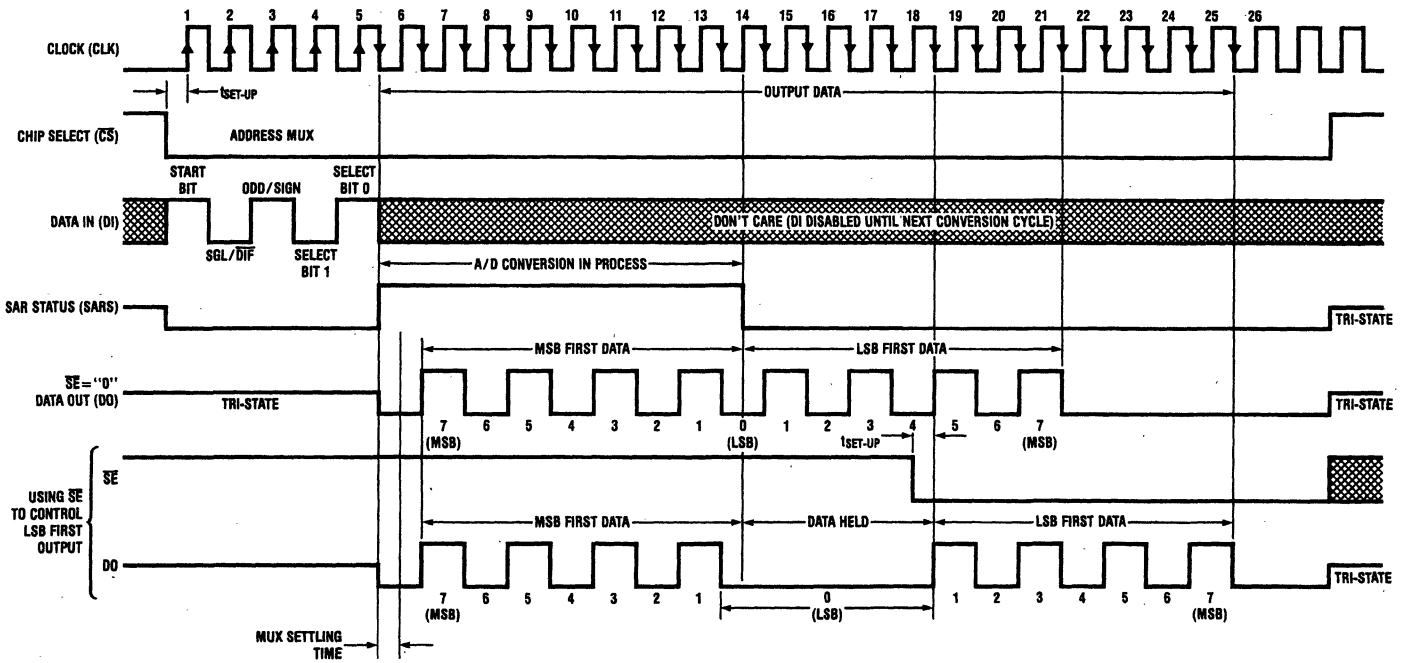
ADC0838 Timing



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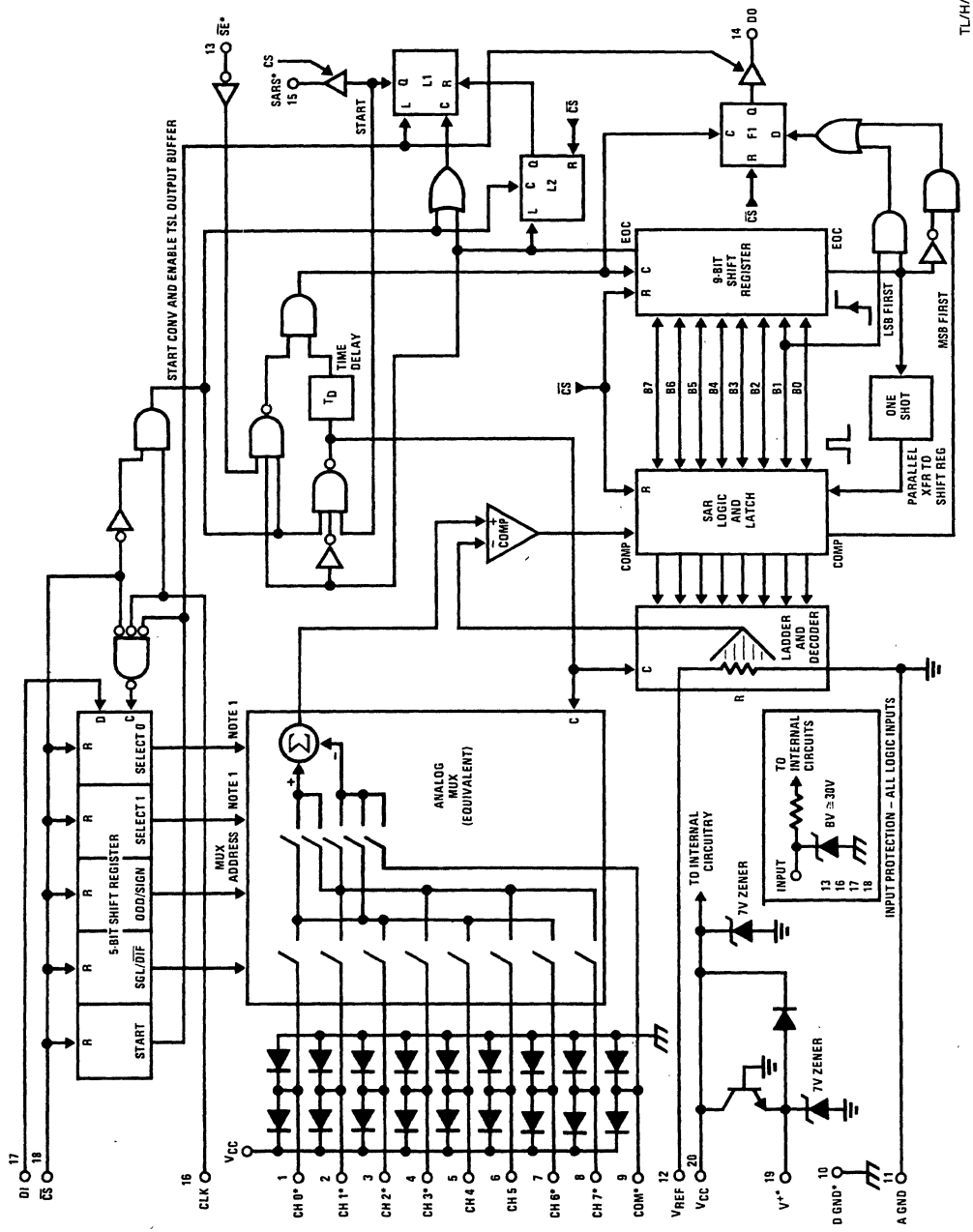
* Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

ADC0838 Functional Block Diagram



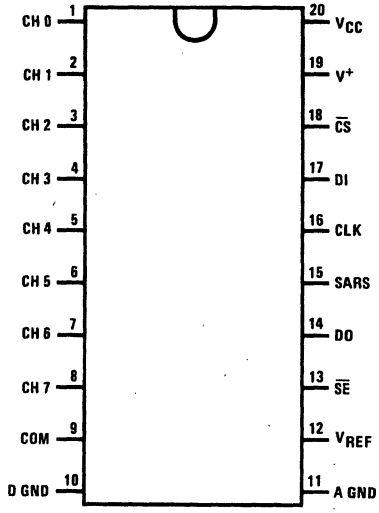
*Some of these functions/pins are not available with other options.

Note 1: For the ADC0834, D1 is input directly to the D input of SELECT 1. SELECT 0 is forced to a "1". For the ADC0832, DI is input directly to the DI input of ODD/SIGN. SELECT 0 is forced to a "0" and SELECT 1 is forced to a "1".

Connection Diagrams

ADC0838 8-Channel MUX

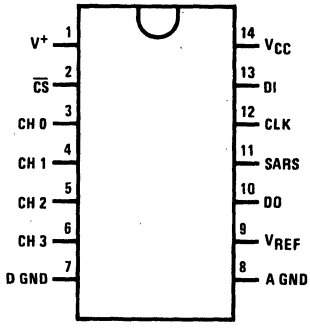
Dual-In-Line Package



TOP VIEW

ADC0834 4-Channel MUX

Dual-In-Line Package

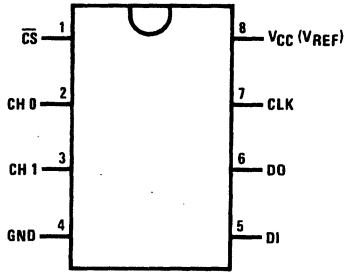


TOP VIEW

COM internally connected to A GND

ADC0832 2-Channel MUX

Dual-In-Line Package



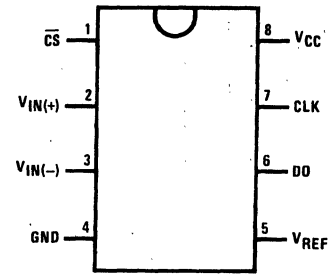
TOP VIEW

COM internally connected to GND.

REF internally connected to V_{CC}.

ADC0831 Single Differential Input

Dual-In-Line Package



TOP VIEW

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Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or a new pseudo-differential option which will convert the difference between the voltage at any analog input and a common terminal. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a different pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC0831 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line on the ADC0838 can be used as a pseudo-differential input. In this mode, the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply application where the analog circuitry may be biased up to a potential other than ground and the output signals are all referred to this potential.

TABLE I. Multiplexer/Package Options

Part Number	Alternate Part Number	Number of Analog Channels		Number of Package Pins
		Single-Ended	Differential	
ADC0831	COP431	1	1	8
ADC0832	COP432	2	1	8
ADC0834	COP434	4	2	14
ADC0838	COP438	8	4	20

Functional Description (Continued)

TABLE II. MUX Addressing: ADC0838

Single-Ended MUX Mode

MUX Address				Analog Single-Ended Channel #								
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

Differential MUX Mode

MUX Address				Analog Differential Channel-Pair #							
SGL/$\overline{\text{DIF}}$	ODD/SIGN	SELECT 1	SELECT 0	0		1		2		3	
				0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

TABLE III. MUX Addressing: ADC0834

Single-Ended MUX Mode

MUX Address			Channel #			
SGL/DIF	ODD/SIGN	SELECT 1	0	1	2	3
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

COM is internally tied to A GND

Differential MUX Mode

MUX Address			Channel #			
SGL/DIF	ODD/SIGN	SELECT 1	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

TABLE IV. MUX Addressing: ADC0832

Single-Ended MUX Mode

MUX Address		Channel #	
SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to A GND

Differential MUX Mode

MUX Address		Channel #	
SGL/$\overline{\text{DIF}}$	ODD/SIGN	0	1
0	0	+	−
0	1	−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

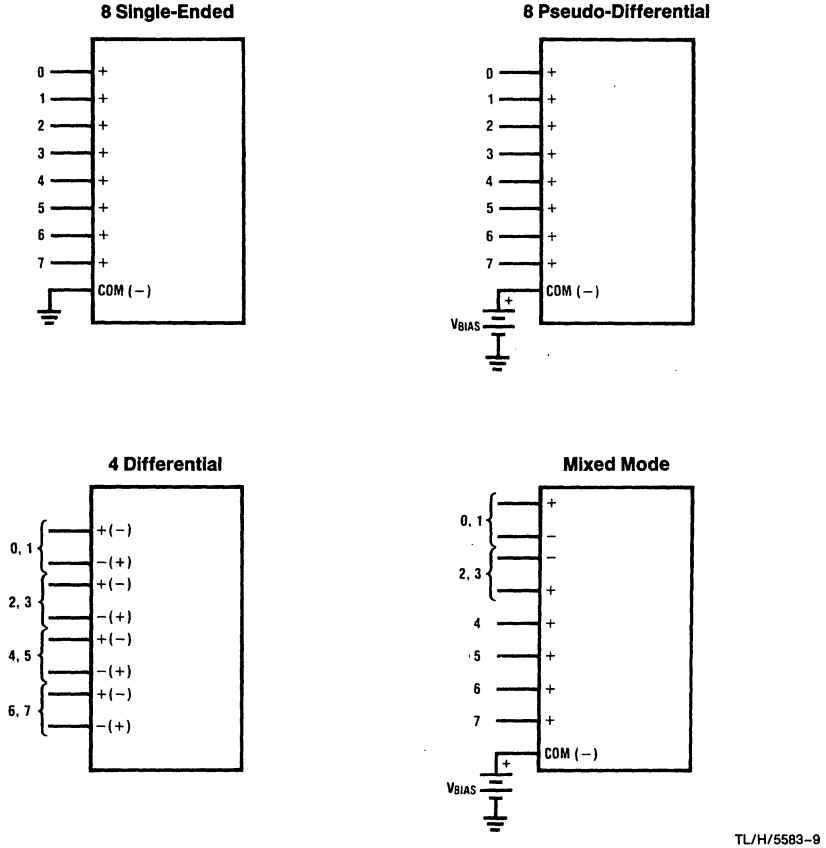
A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate diagram is shown of each device.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.



TL/H/5583–9

FIGURE 1. Analog Input Multiplexer Options for the ADC0838

Functional Description (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

8. If the programmer prefers, the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. All 8 bits of the result are stored in an output shift register. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. On the ADC0838 the $\overline{SE}$ line is brought out and if held high, the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low, the data is then clocked out LSB first. The ADC0831 is an exception in that its data is only output in MSB first format.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

All of the logic inputs can be taken to 15V independent of the magnitude of the supply voltage, V_{CC}.

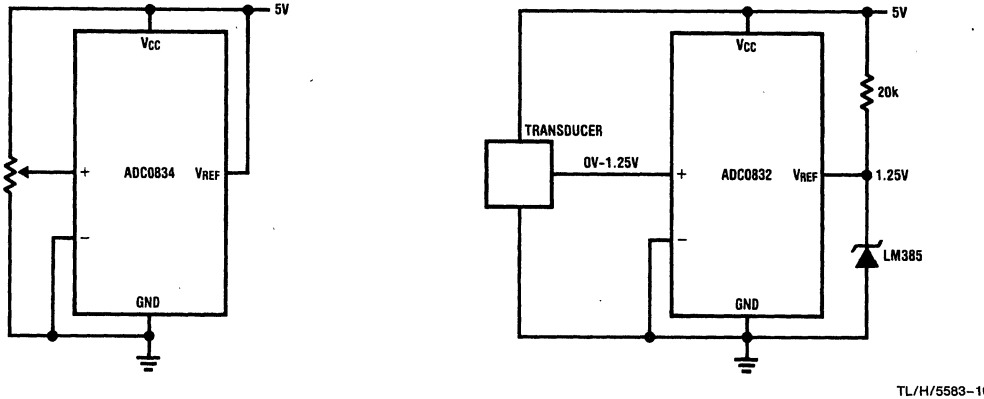
3.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 2.4 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC} (done internally on the ADC0832). This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals V_{REF}/256).



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a) Ratiometric **b) Absolute with a Reduced Span**

FIGURE 2. Reference Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{peak}(2\pi f_{CM}) \left(\frac{0.5}{f_{CLK}} \right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{peak} is its peak voltage value

and f_{CLK}, is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ±1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for V_{REF} = 5.000 V_{DC}).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{256} \right]$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0838 and ADC0834 is the inclusion of a zener diode connected from the V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3*. (See Note 3)

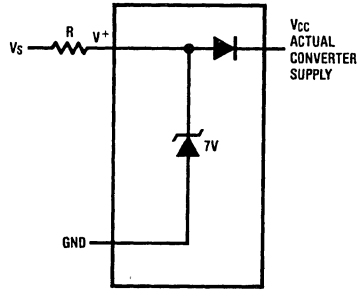

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FIGURE 3. An On-Chip Shunt Regulator Diode

Functional Description (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4 and 5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V+ and V_{CC} is shown in *Figures 6 and 7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D and the relatively high clock frequencies used (typically in the range of 10k–400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under ¼ of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of V_Z. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V+ pin.

Applications

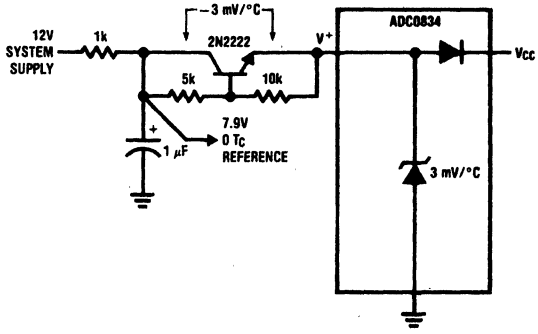

FIGURE 4. Operating with a Temperature Compensated Reference

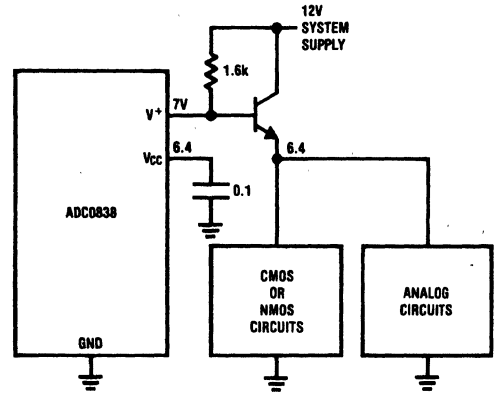

FIGURE 5. Using the A/D as the System Supply Regulator

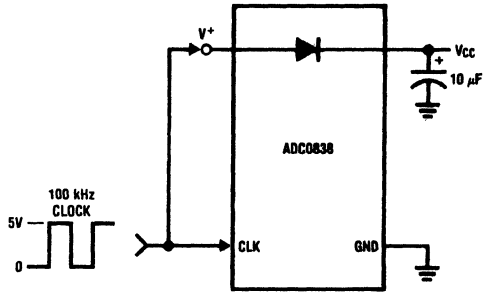

FIGURE 6. Generating V_{CC} from the Converter Clock

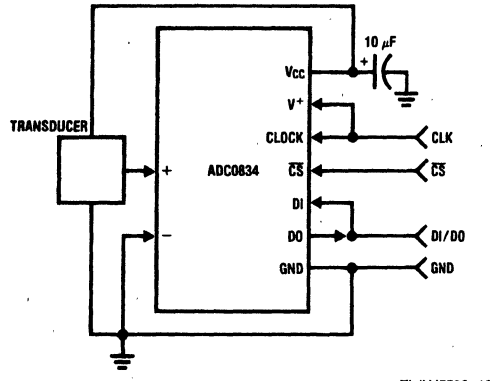

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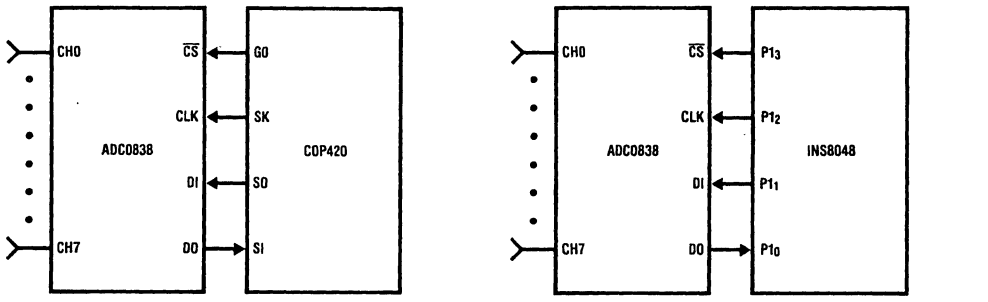
FIGURE 7. Remote Sensing—Clock and Power on 1 Wire

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048



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COP CODING EXAMPLE

Mnemonic	Instruction
LEI	ENABLES SIO's INPUT AND OUTPUT
SC	C = 1
OGI	G0 = 0 ($\overline{CS}$ = 0)
CLR A	CLEARS ACCUMULATOR
AISC 1	LOADS ACCUMULATOR WITH 1
XAS	EXCHANGES SIO WITH ACCUMULATOR AND STARTS SK CLOCK
LDD	LOADS MUX ADDRESS FROM RAM INTO ACCUMULATOR
NOP	—
XAS	LOADS MUX ADDRESS FROM ACCUMULATOR TO SIO REGISTER
↑ 8 INSTRUCTIONS ↓	
XAS	READS HIGH ORDER NIBBLE (4 BITS) INTO ACCUMULATOR
XIS	PUTS HIGH ORDER NIBBLE INTO RAM
CLR A	CLEARS ACCUMULATOR
RC	C = 0
XAS	READS LOW ORDER NIBBLE INTO ACCUMULATOR AND STOPS SK
XIS	PUTS LOW ORDER NIBBLE INTO RAM
OGI	G0 = 1 ($\overline{CS}$ = 1)
LEI	DISABLES SIO's INPUT AND OUTPUT

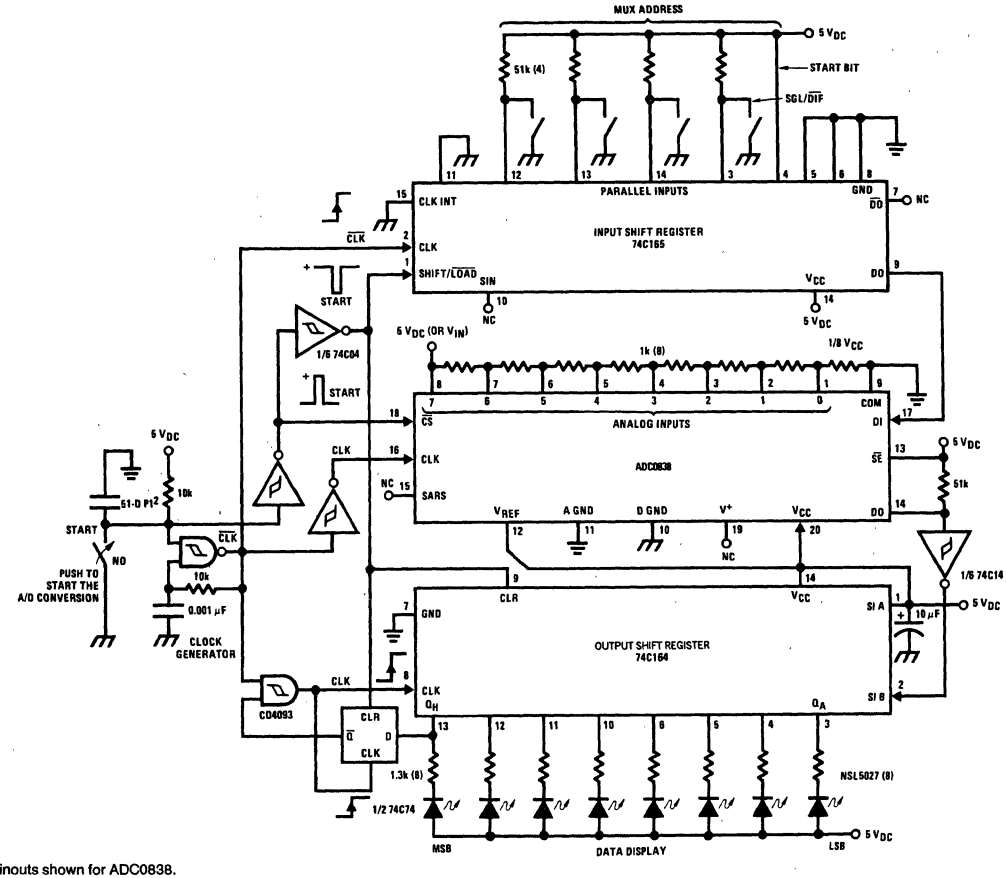
8048 CODING EXAMPLE

	Mnemonic		Instruction
START:	ANL	P1, #0F7H	;SELECT A/D ($\overline{CS}$ = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX ADDRESS
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT
			;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	JMP	CONT	;CONTINUE
			;BIT = 1
ONE:	ORL	P1, #1	;DI ← 1
CONT:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	CALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	IN	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETR			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

S 5

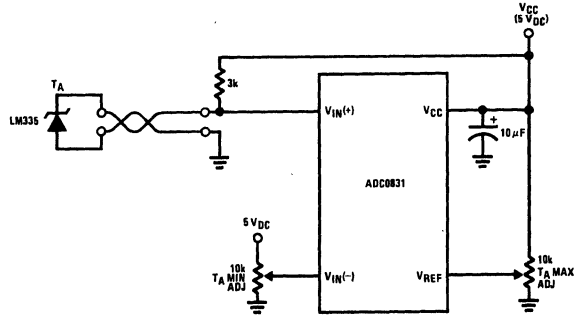
Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0838 Evaluation



*Pinouts shown for ADC0838.
For all other products tie to pin functions as shown.

Low-Cost Remote Temperature Sensor



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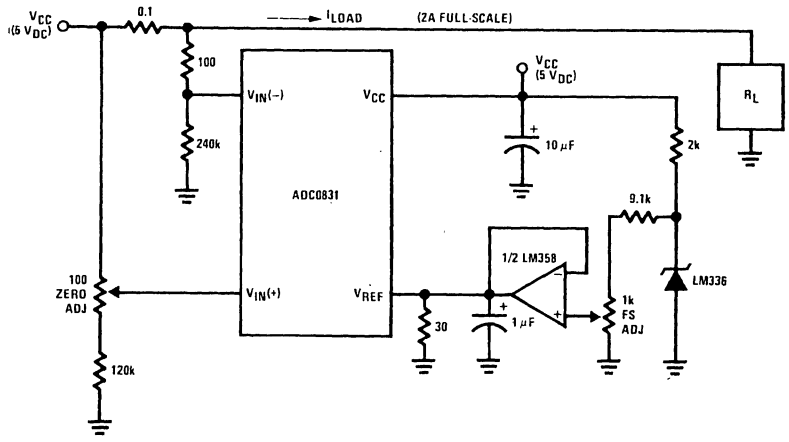
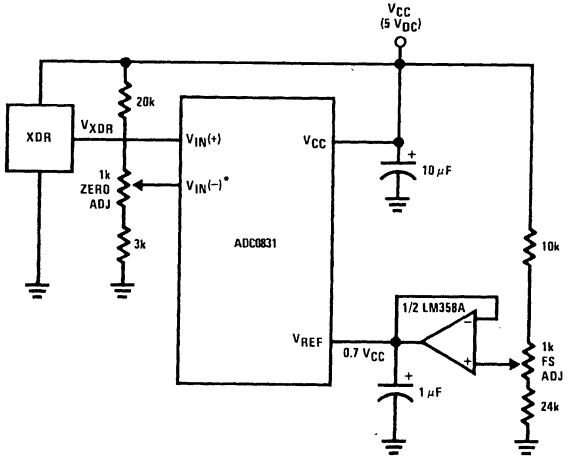
Applications (Continued)

Digitizing a Current Flow



Operating with Ratiometric Transducers



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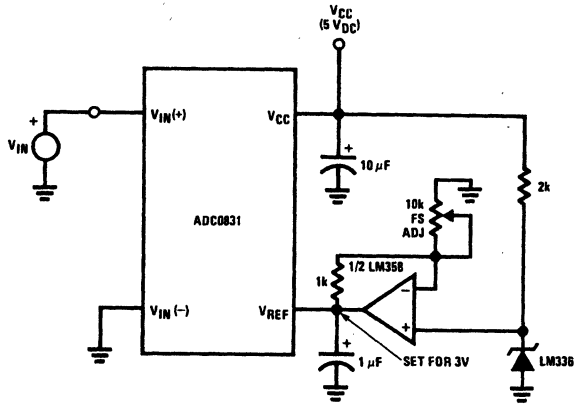
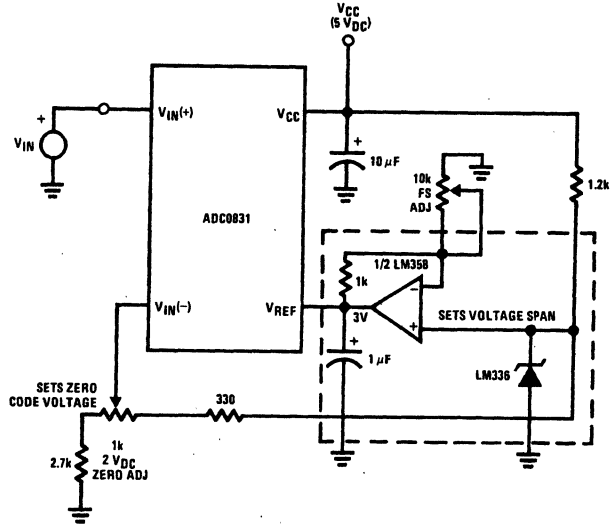
* $V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Applications (Continued)

Span Adjust: $0V \leq V_{IN} \leq 3V$



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



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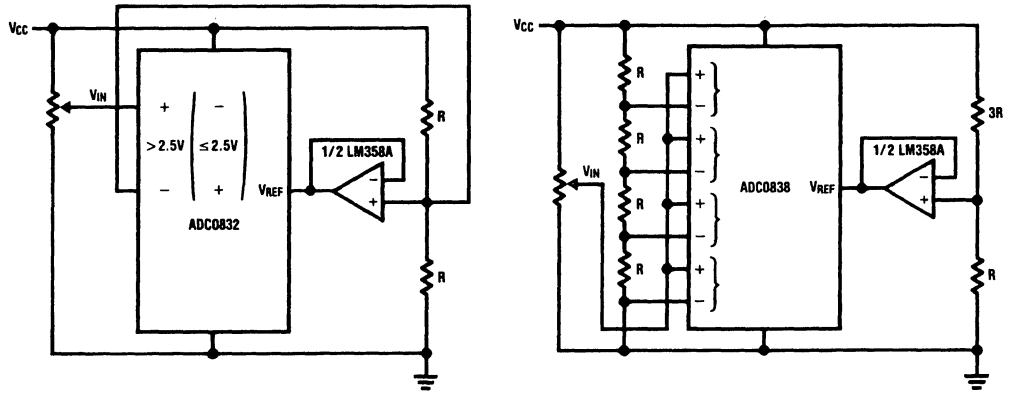
Applications (Continued)

Obtaining Higher Resolution



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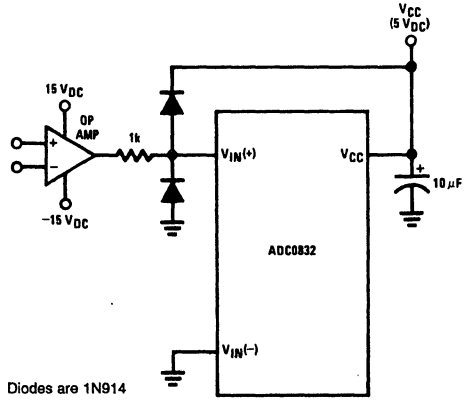
Controller performs a routine to determine which input polarity (9-bit example) or which channel pair (10-bit example) provides a non-zero output code. This information provides the extra bits.

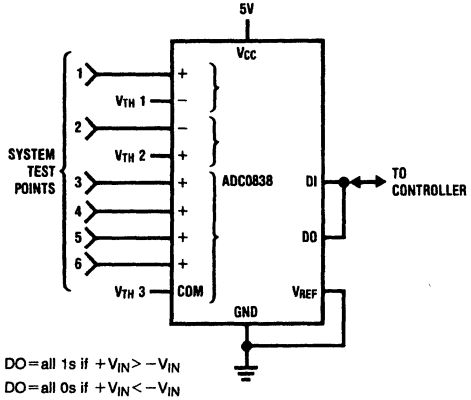
a) 9-Bit A/D **b)10-Bit A/D**

Protecting the Input



Diodes are 1N914

High Accuracy Comparators



DO = all 1s if $+V_{IN} > -V_{IN}$

DO = all 0s if $+V_{IN} < -V_{IN}$

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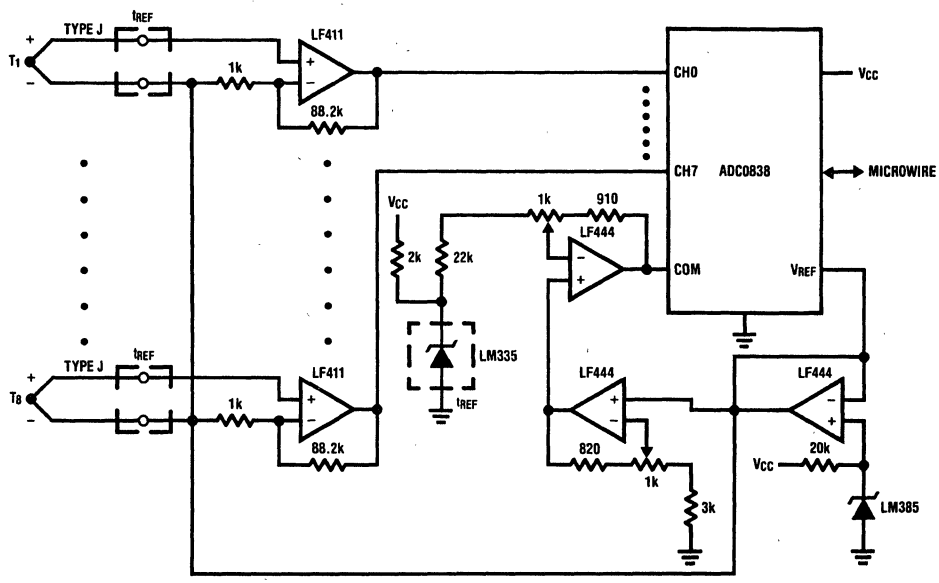
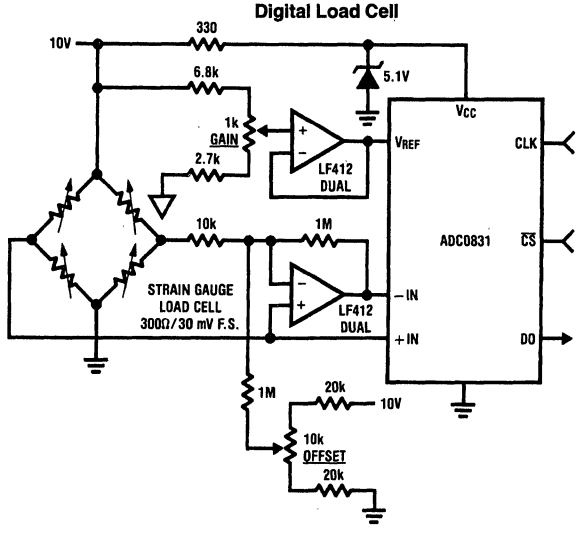
Applications (Continued)

Convert 8 Thermocouples with only One Cold-Junction Compensator



Uses the pseudo-differential mode to keep the differential inputs constant with changes in reference temperature (T_{REF}).

Digital Load Cell



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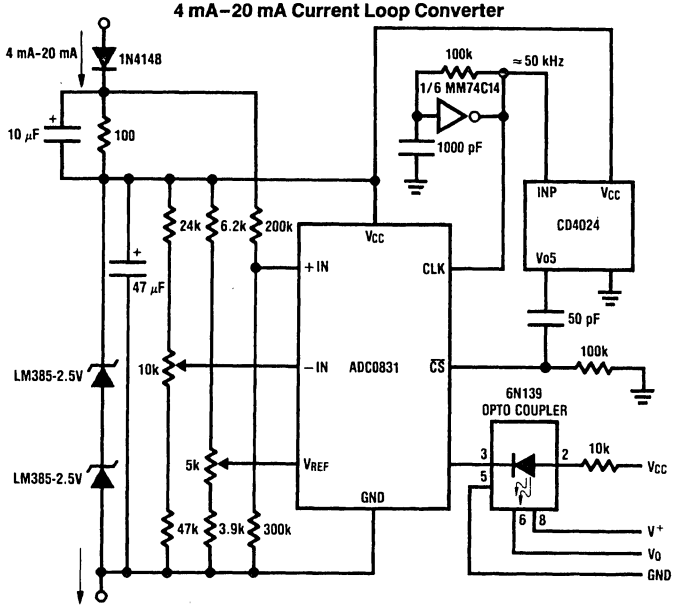
- Uses one more wire than load cell itself
- Two mini-DIPs could be mounted inside load cell for digital output transducer
- Electronic offset and gain trims relax mechanical specs for gauge factor and offset
- Low level cell output is converted immediately for high noise immunity

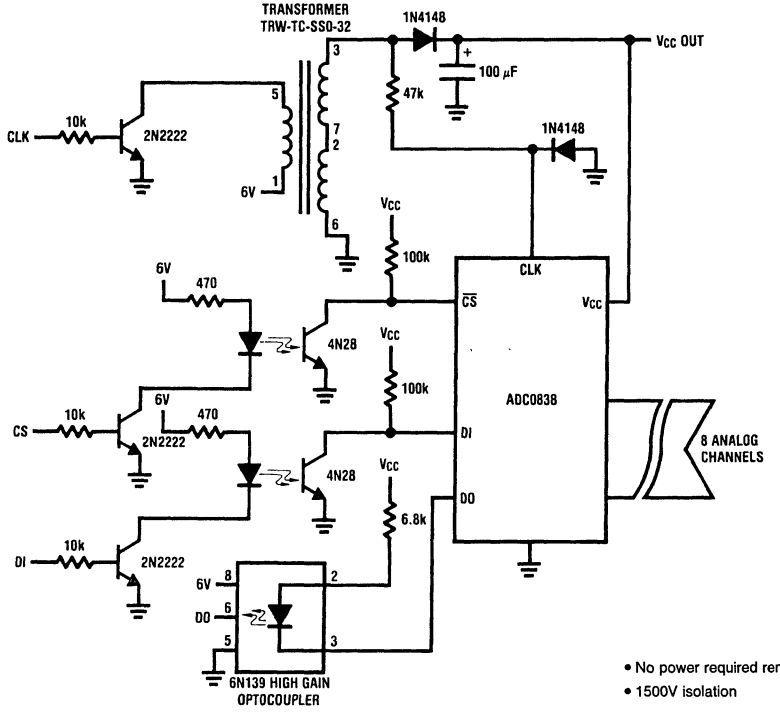
Applications (Continued)

4 mA–20 mA Current Loop Converter



- All power supplied by loop
- 1500V isolation at output

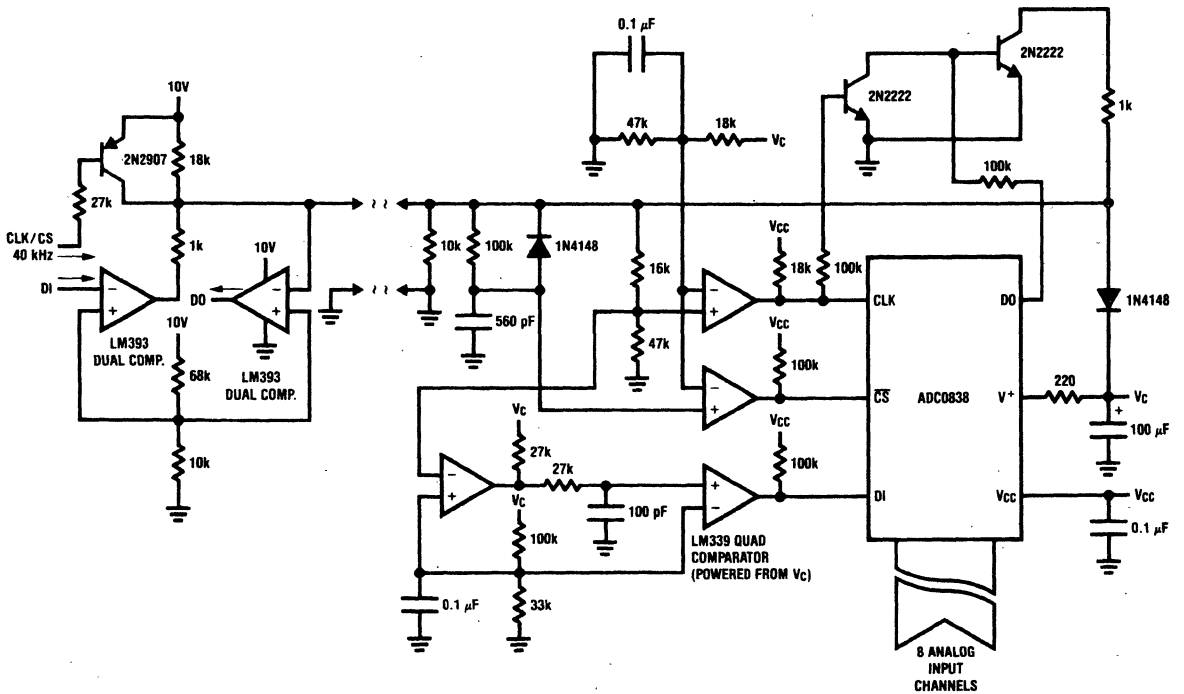
Isolated Data Converter



TL/H/5583–20

- No power required remotely
- 1500V isolation

Two Wire Interface for 8 Channels



- No additional connections
- $\overline{CS}$ derived from extended high on CLK line > 100 μs
- Timing arranged for 40 kHz, could be changed up or down by component change
- 10% CLK frequency change without component change OK

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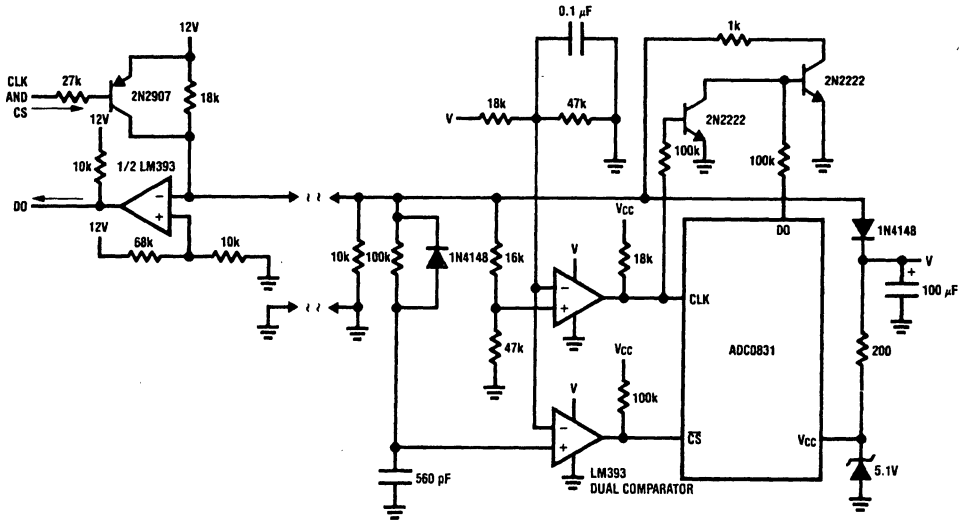
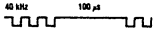
Applications (Continued)

Two Wire 1-Channel Interface



- Simpler version of 8-channel
- $\overline{CS}$ derived long CLK pulse



TL/H/5583–22

Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0831BJ	1	±½	Hermetic (J)	−55°C to +125°C
ADC0831BCJ			Hermetic (J)	−40°C to +85°C
ADC0831BCN (COP431BN)			Molded (N)	−0°C to +70°C
ADC0831CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0831CCN (COP431CN)			Molded (N)	−0°C to +70°C
ADC0832BJ	2	±½	Hermetic (J)	−55°C to +125°C
ADC0832BCJ			Hermetic (J)	−40°C to +85°C
ADC0832BCN (COP432BN)			Molded (N)	−0°C to +70°C
ADC0832CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0832CCN (COP432CN)			Molded (N)	−0°C to +70°C
ADC0834BJ	4	±½	Hermetic (J)	−55°C to +125°C
ADC0834BCJ			Hermetic (J)	−40°C to +85°C
ADC0834BCN (COP434BN)			Molded (N)	−0°C to +70°C
ADC0834CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0834CCN (COP434CN)			Molded (N)	−0°C to +70°C
ADC0838BJ	8	±½	Hermetic (J)	−55°C to +125°C
ADC0838BCJ			Hermetic (J)	−40°C to +85°C
ADC0838BCN (COP438BN)			Molded (N)	−0°C to +70°C
ADC0838CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0838CCN (COP438CN)			Molded (N)	−0°C to +70°C

See NS Packages J08A, J14A, J20A, N08E, N14A, N20A

National Semiconductor

ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

General Description

The ADC0833 series is an 8-bit successive approximation A/D converter with a serial I/O and configurable input multiplexer with 4 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, as well as with standard shift registers or μPs.

The 4-channel multiplexer is software configured for single-ended or differential inputs when channel assigned by a 4-bit serial word.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

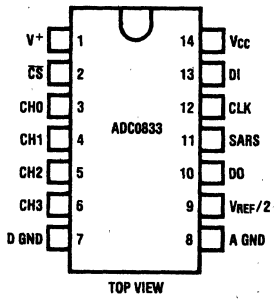
- NSC MICROWIRE compatible–direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand alone"
- Works with 2.5V (LM336) voltage reference
- No full-scale or zero adjust required
- Differential analog voltage inputs
- 4-channel analog multiplexer
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- T²L/MOS input/output compatible
- 0.3" standard width 14-pin DIP package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	± ½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	25 mW
■ Conversion Time	32 μs

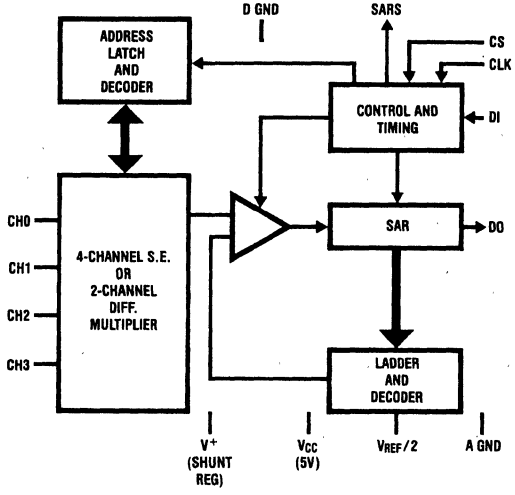
Connection and Functional Diagrams

Dual-In-Line Package



TOP VIEW

See NS Packages J14A, N14A



TL/H/5607–1

Absolute Maximum Ratings (Notes 1 & 2)

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to + 15V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per Pin	±5 mA
Storage Temperature	−65°C to + 150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0833BJ, ADC0833CJ	$-55°C \le T_A \le 125°C$
ADC0833BCJ, ADC0833CCJ	$-40°C \le T_A \le 85°C$
ADC0833BCN, ADC0833CCN	$0°C \le T_A \le 70°C$

Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from t_{MIN} to t_{MAX};** all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Total Unadjusted Error	$V_{REF}/2$ Forced to 2.500 V_{DC}				
ADC0833BCN			±½	±½	LSB
ADC0883BJ, BCJ			±½		LSB
ADC0833CCN			±1	±1	LSB
ADC0833CJ, CCJ			±1		LSB
Minimum Total Ladder Resistance (Note 7)					
ADC0833BCJ/CCJ/BJ/CJ		4.8	**2.2**		kΩ
ADC0833BCN/CCN		4.8	2.2	**2.2**	kΩ
Maximum Total Ladder Resistance (Note 7)					
ADC0833BCJ/CCJ/BJ/CJ		4.8	**8.2**		kΩ
ADC0833BCN/CCN		4.8	8.2	**8.2**	kΩ
Minimum Common-Mode Input Range (Note 8)	All MUX Inputs and COM Input				
ADC0833BCJ/CCJ/BJ/CJ			**GND−0.05**		V
ADC0833BCN/CCN			GND−0.05	**GND−0.05**	V
Maximum Common-Mode Input Range (Note 8)	All MUX Inputs and COM Input				
ADC0833BCJ/CCJ/BJ/CJ			**V_{CC}+0.05**		V
ADC0833BCN/CCN			V_{CC}+0.05	**V_{CC}+0.05**	V
DC Common-Mode Error					
ADC0833BCJ/CCJ/BJ/CJ		±1/16	±¼		LSB
ADC0833BCN/CCN		±1/16	±¼	±¼	LSB
Change In Zero Error From V_{CC} = 5V To Internal Zener Operation (Note 3)	15mA Into V+ V_{CC} = N.C. V_{REF} = 5V				
ADC0833BCJ/CCJ/BJ/CJ			**1**		LSB
ADC0833BCN/CCN			1	**1**	LSB
V_Z, Minimum Internal Diode Breakdown (At V+) (Note 3)	15mA Into V+				
ADC0833BCJ/CCJ/BJ/CJ			**6.3**		V
ADC0833BCN/CCN			6.3	**6.3**	V
V_Z, Minimum Internal Diode Breakdown (At V+) (Note 3)	15mA Into V+				
ADC0833BCJ/CCJ/BJ/CJ			**8.5**		V
ADC0833BCN/CCN			8.5	**8.5**	V

Electrical Characteristics (Continued) The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from t_{MIN} to t_{MAX};** all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)					
Power Supply Sensitivity	$V_{CC} = 5V \pm 5\%$				
ADC0833BCJ/CCJ/BJ/CJ		$\pm 1/16$	$\pm 1/4$		LSB
ADC0833BCN/CCN		$\pm 1/16$	$\pm 1/4$	$\pm 1/4$	LSB
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V				
ADC0833BCJ/CCJ/BJ/CJ			−1		μA
			−50		nA
ADC0833BCN/CCN				−1	μA
			−50		nA
	On Channel = 0V, Off Channel = 5V				
ADC0833BCJ/CCJ/BJ/CJ			−1		μA
			−50		nA
ADC0833BCN/CCN				−1	μA
			−50		nA
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V				
ADC083BCJ/CCJ/BJ/CJ			−1		μA
			−200		nA
ADC0833BCN/CCN				−1	μA
			−200		nA
	On Channel = 0V, Off Channel = 5V				
ADC083BCJ/CCJ/BJ/CJ			−1		μA
			−200		nA
ADC0833BCN/CCN				−1	μA
			−200		nA
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$				
ADC0833BCJ/CCJ/BJ/CJ			**2.0**		V
ADC0833BCN/CCN			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$				
ADC0833BCJ/CCJ/BJ/CJ			**0.8**		V
ADC0833BCN/CCN			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$				
ADC0833BCJ/CCJ/BJ/CJ		0.005	**1**		μA
ADC0833BCN/CCN		0.005	1	**1**	μA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$				
ADC0833BCJ/CCJ/BJ/CJ		−0.005	**−1**		μA
ADC0833BCN/CCN		−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$				
ADC0833BCJ/CCJ/BJ/CJ	$I_{OUT} = -360\mu A$		**2.4**		V
ADC0833BCN/CCN			2.4	**2.4**	V
ADC0833BCJ/CCJ/BJ/CJ	$I_{OUT} = -10\mu A$		**4.5**		V
ADC0833BCN/CCN4.54			4.5	**4.5**	V

Electrical Characteristics (Continued) The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz unless otherwise specified. **Boldface limits apply from t_{MIN} to t_{MAX};** all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
DIGITAL AND DC CHARACTERISTICS (Continued)					
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 1.6mA$, $V_{CC} = 4.75V$				
ADC0833BCJ/CCJ/BJ/CJ			**0.4**		V
ADC0833BCN/CCN			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (DO, SARS)					
ADC0833BCJ/CCJ/BJ/CJ	$V_{OUT} = 0.4V$	−0.1	**−3**		μA
ADC0833BCN/CCN		−0.1	−3	**−3**	μA
ADC0833BCJ/CCJ/BJ/CJ	$V_{OUT} = 5V$	0.1	**3**		μA
ADC0833BCN/CCN		0.1	3	**3**	μA
I_{SOURCE}	V_{OUT} Short to GND				
ADC0833BCJ/CCJ/BJ/CJ		14	**7.5**		mA
ADC0833BCN/CCN		14	7.5	**7.5**	mA
I_{SINK}	V_{OUT} Short to V_{CC}				
ADC0833BCJ/CCJ/BJ/CJ		16	**9.0**		mA
ADC0833BCN/CCN		16	9.0	**9.0**	mA
I_{CC}, Supply Current (Note 3)	$V_{REF}/2$ Open Circuit				
ADC0833BCJ/CCJ/BJ/CJ		2	**5**		mA
ADC0833BCN/CCN		2	5	**5**	mA
I^+, Current into V^+ (Note 3)					
ADC0833BCJ/CCJ/BJ/CJ			**15**		mA
ADC0833BCN/CCN			15	**15**	mA

AC Characteristics $t_r = t_f = 20$ ns

Parameter	Conditions	Typ (Note 4)	Tested Limit (Note 5)	Design Limit (Note 6)	Limit Units
f_{CLK}, Clock Frequency	Min Max		10	 400	kHz kHz
T_C, Conversion Time	Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 10)	Min Max			40 60	% %
t_{SET-UP}, CS Falling Edge or Data Input Valid to CLK Rising Edge				250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge				90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 11)	$C_L = 100$ pF Data MSB First Data LSB First	 650 250		 1500 600	 ns ns
t_{1H}, T_{OH}—Rising Edge of CS to Data Output and SARS Hi-Z	$C_L = 10$ pF, $R_L = 10$k (see TRI-STATE Test Circuits)	125		250	ns
C_{IN}, Capacitance of Logic Input		5			pF
C_{OUT}, Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to ground.

Note 3: Internal zener diodes (approx. 7V) are connected from V^+ to GND and V_{CC} to GND. The zener at V^+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V^+. Functionality is therefore guaranteed for V^+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max. of 6.5V. It is recommended that a resistor be used to limit the max. current into V^+.

Note 4: Typicals are at 25°C and represent most likely parametric norm.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: See Applications, section 3.0.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

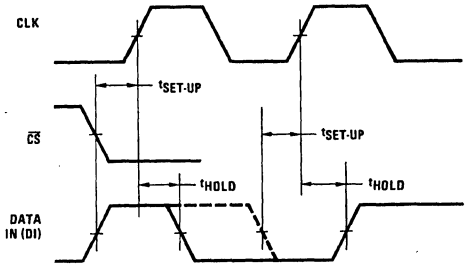
Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 1 μs.

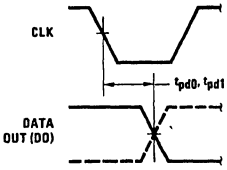
Note 11: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Timing Diagrams

Data Input Timing

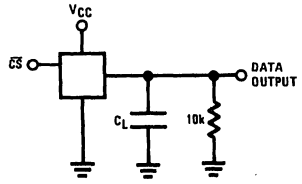


Data Output Timing

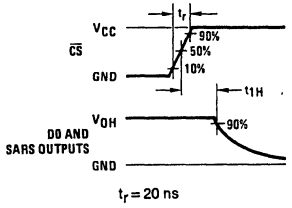


TRI-STATE Test Circuits and Waveforms

t_{1H}

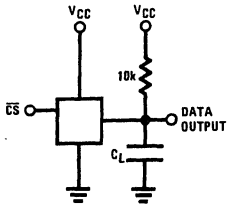


t_{1H}, $C_L = 10$ pF

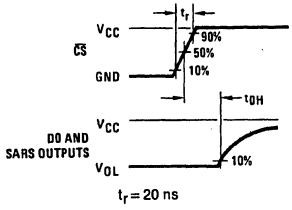


$t_r = 20$ ns

t_{0H}

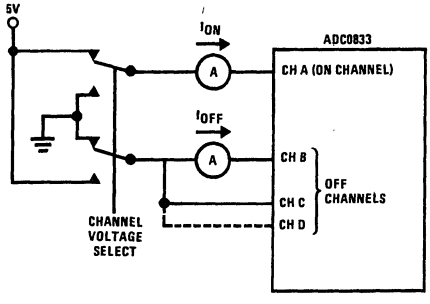


t_{0H}, $C_L = 10$ pF



$t_r = 20$ ns

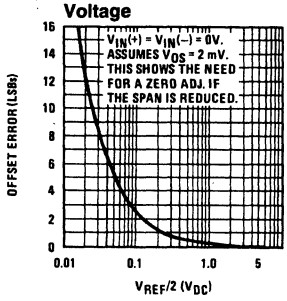
Leakage Current Test Circuit



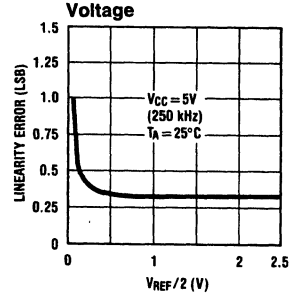
TL/H/5607–2

Typical Performance Characteristics

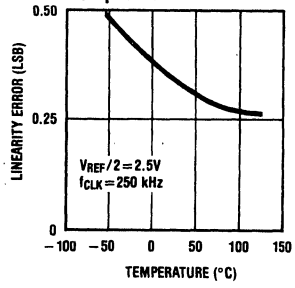
Effect of Unadjusted Offset Error vs $V_{REF}/2$ Voltage



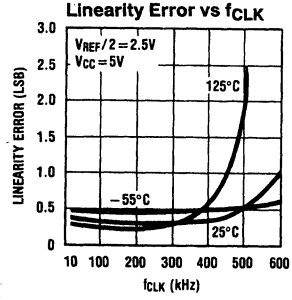
Linearity Error vs V_{REF} Voltage



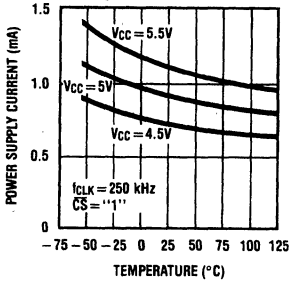
Linearity Error vs Temperature



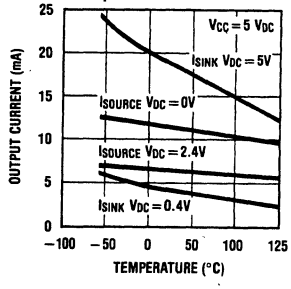
Linearity Error vs f_{CLK}



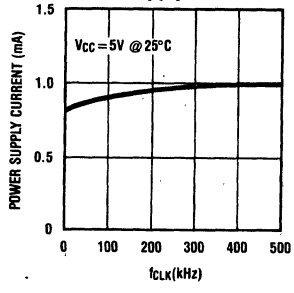
Power Supply Current vs Temperature



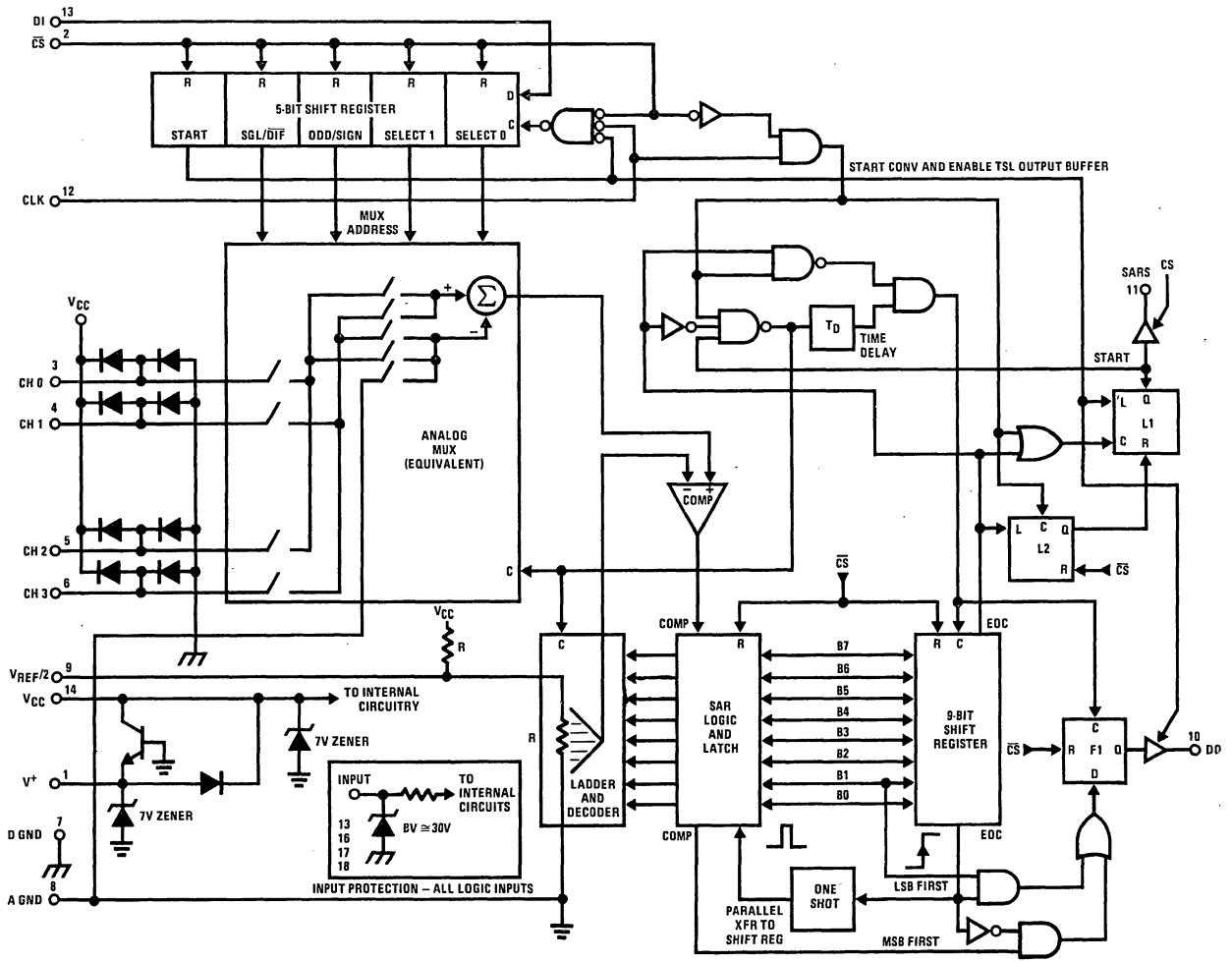
Output Current vs Temperature



Power Supply Current vs f_{CLK}

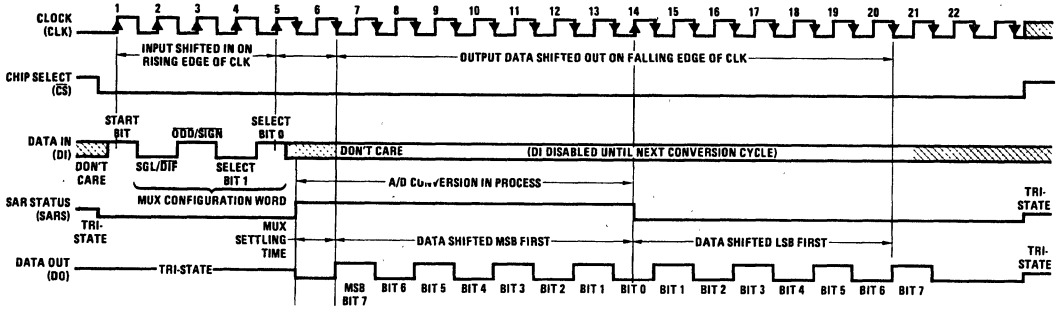


TL/H/5607–3


DI
CS
CLK
5-BIT SHIFT REGISTER
START
SGL/DIF
ODD/SIGN
SELECT 1
SELECT 0
MUX ADDRESS
START CONV AND ENABLE TSL OUTPUT BUFFER
SARS
CS
START
TIME DELAY
ANALOG MUX (EQUIVALENT)
CH 0
CH 1
CH 2
CH 3
COMP
L1
L2
VREF/2
VCC
TO INTERNAL CIRCUITRY
7V ZENER
V+
D GND
A GND
INPUT
TO INTERNAL CIRCUITS
BV ≅ 30V
INPUT PROTECTION – ALL LOGIC INPUTS
LADDER AND DECODER
SAR LOGIC AND LATCH
B7
B6
B5
B4
B3
B2
B1
B0
9-BIT SHIFT REGISTER
EOC
PARALLEL XFR TO SHIFT REG
ONE SHOT
LSB FIRST
MSB FIRST
F1
DO

TL/H/5607–4

Timing Diagram



TL/H/5607–5

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of the ADC0833 utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended (ground referred) or differential inputs. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a differential pair. Channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following table. The MUX address is shifted into the converter through the DI line.

TABLE I. MUX Addressing

Single-Ended MUX Mode

Address				Channel #			
SGL/ $\overline{\text{DIF}}$	$\overline{\text{ODD}}$/ $\overline{\text{SIGN}}$	SELECT 1	SELECT 0	0	1	2	3
1	0	0	1	+			
1	0	1	1			+	
1	1	0	1		+		
1	1	1	1				+

COM is internally ties to a GND

Differential MUX Mode

Address				Channel #			
SGL/ $\overline{\text{DIF}}$	$\overline{\text{ODD}}$/ $\overline{\text{SIGN}}$	SELECT 1	SELECT 0	0	1	2	3
0	0	0	1	+	−		
0	0	1	1			+	−
0	1	0	1	−	+		
0	1	1	1			−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50mV above V_{CC}(typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagram and Functional Block Diagram and to follow a complete conversion sequence.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 4 bits to be the MUX assignment word.

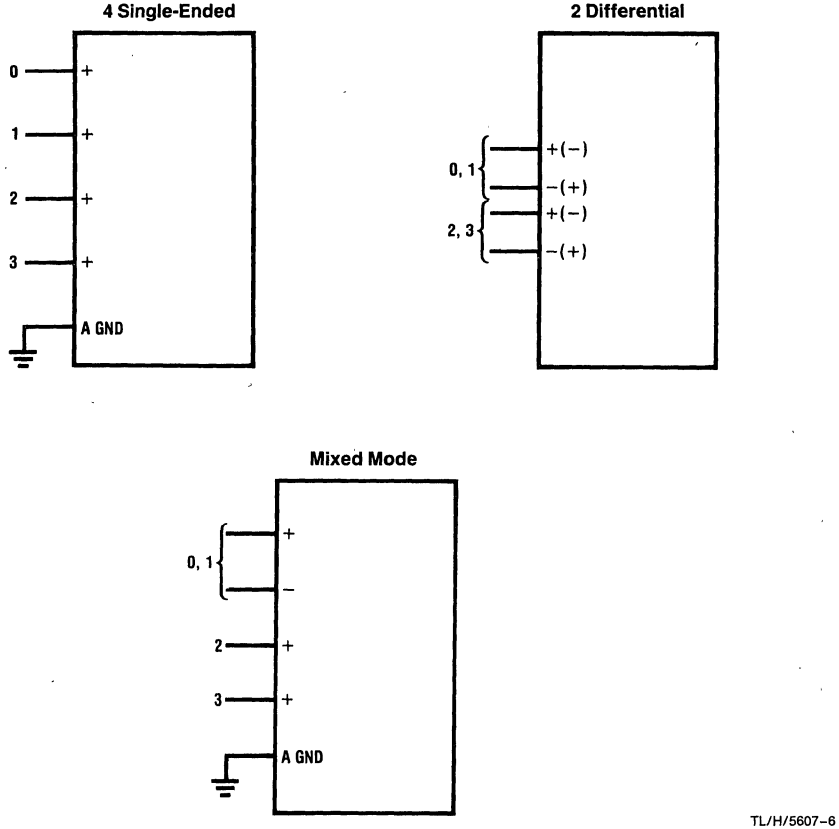


FIGURE 1. Analog Input Multiplexer Options for the ADC0833

Functional Description (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

8. If the programmer prefers, the data can be read in an LSB first format. All 8 bits of the result are stored in an output shift register. The conversion result, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

All of the logic inputs can be taken to 15V independent of the magnitude of the supply voltage, V_{CC}.

3.0 REFERENCE CONSIDERATIONS

The ADC0833 is intended primarily for use in circuits requiring absolute accuracy. In this type of system, the analog inputs vary between very specific voltage limits and the reference voltage for the A/D converter must remain stable with time and temperature. For ratiometric applications, an ADC0834 is a pin-for-pin compatible alternative.

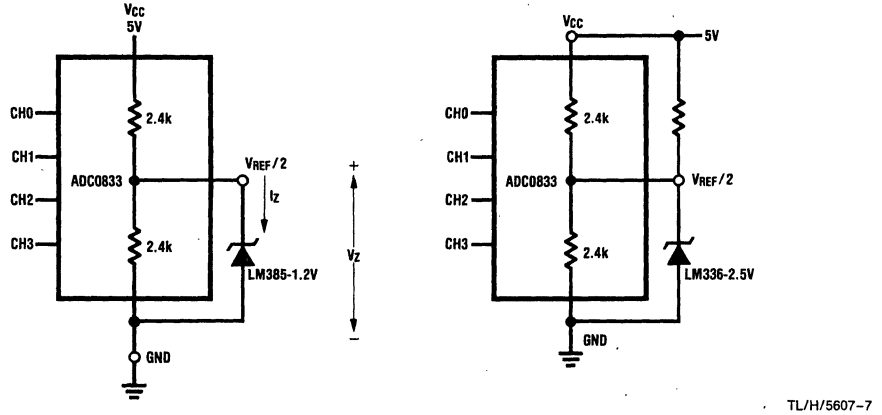
The voltage applied to the $V_{REF}/2$ pin defines the voltage span of the analog input [the difference between $V_{IN}(+)$ and $V_{IN}(-)$] over which the 256 possible output codes apply. A full-scale conversion (an all 1s output code) will result when the voltage difference between a selected "+" input and "−" input is approximately *twice* the voltage at the $V_{REF}/2$ pin. This internal gain of 2 from the applied reference to the full-scale input voltage allows biasing a low voltage reference diode from the $5V_{DC}$ converter supply. To accommodate a 5V input span, only a 2.5V reference is required. The LM385 and LM336 reference diodes are good low current devices to use with these converters. The output code changes in accordance with the following equation:

$$\text{Output Code} = 256 \left(\frac{V_{IN}(+) - V_{IN}(-)}{2(V_{REF}/2)} \right)$$

where the output code is the decimal equivalent of the 8-bit binary output (ranging from 0 to 255) and the term $V_{REF}/2$ is the voltage from pin 9 to ground.

The $V_{REF}/2$ pin is the center point of a two resistor divider (each resistor is 2.4 kΩ) connected from V_{CC} to ground. Total ladder input resistance is the sum of these two equal resistors. As shown in *Figure 2,* a reference diode with a voltage less than $V_{CC}/2$ can be connected without requiring an external biasing resistor if its current requirements meet the indicated level.

The minimum value of $V_{REF}/2$ can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).



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$V_{FULL\text{-}SCALE} \cong 2.4V$ $V_{FULL\text{-}SCALE} \cong 5.0V$

Note: No external biasing resistor needed if $V_Z < \frac{V_{CC}}{2}$ and I_Z min $< \frac{V_{CC}/2 - V_Z}{1.2\ k\Omega}$

FIGURE 2. Reference Biasing Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error(max)} = V_{peak}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK} is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the %clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ± 1 μA over temperature will create a 1 mV inut error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input as this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transaction.

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ fs\ adj = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The $V_{REF}/2$ voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0833 is the inclusion of a 7V zener diode connected from the V+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3.*

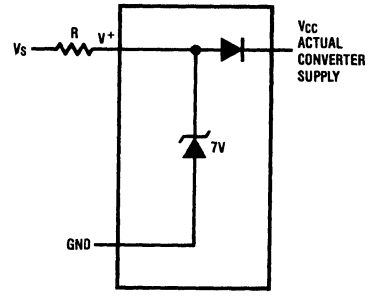

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FIGURE 3. An On-Chip Shunt Regulator Diode

Functional Description (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4* and *5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V^+ and V_{CC} is shown in *Figures 6* and *7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D (~3 mA) and the relatively high clock frequencies used (typically in the range of 10k-400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under 1/4 of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of 7V. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V^+ pin.

Applications

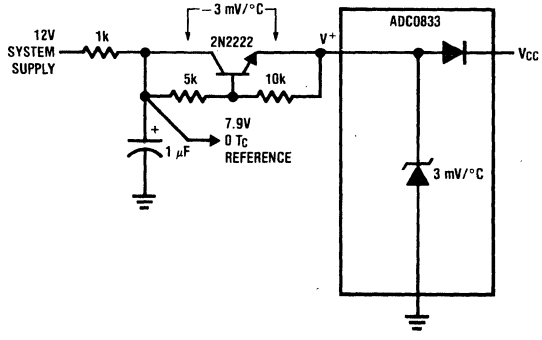

FIGURE 4. Operating with a Temperature Compensated Reference

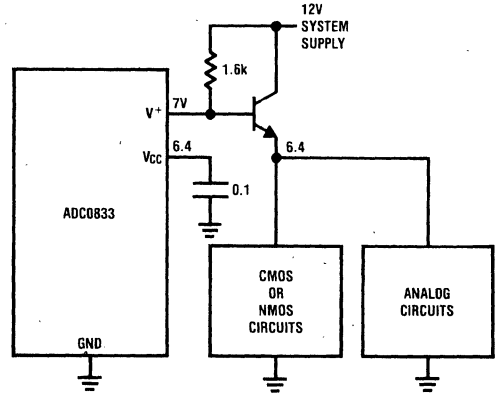

FIGURE 5. Using the A/D as the System Supply Regulator

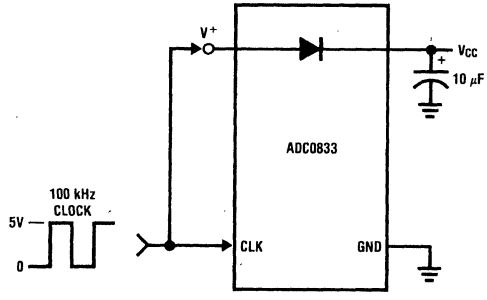

FIGURE 6. Generally V_{CC} from the Converter Clock

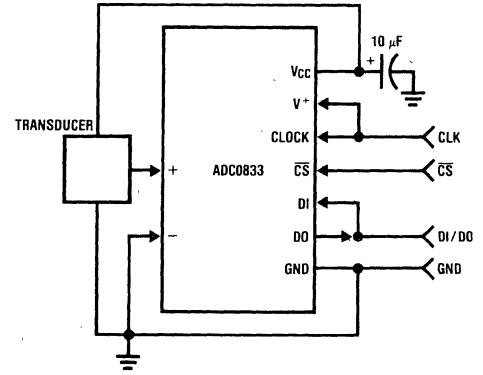

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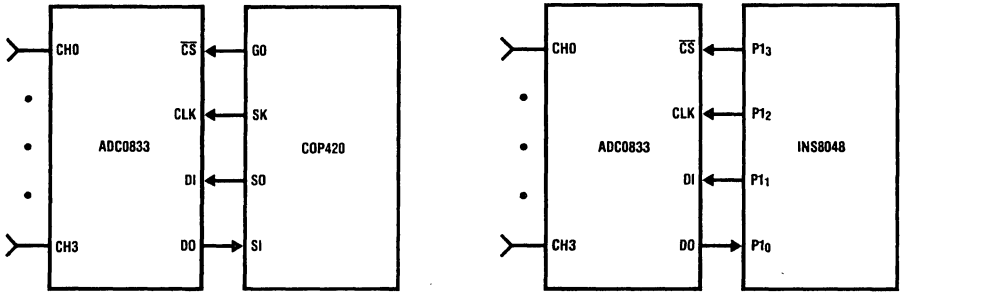
FIGURE 7. Remote Sensing—Clock and Power on 1 Wire

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048



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COP CODING EXAMPLE

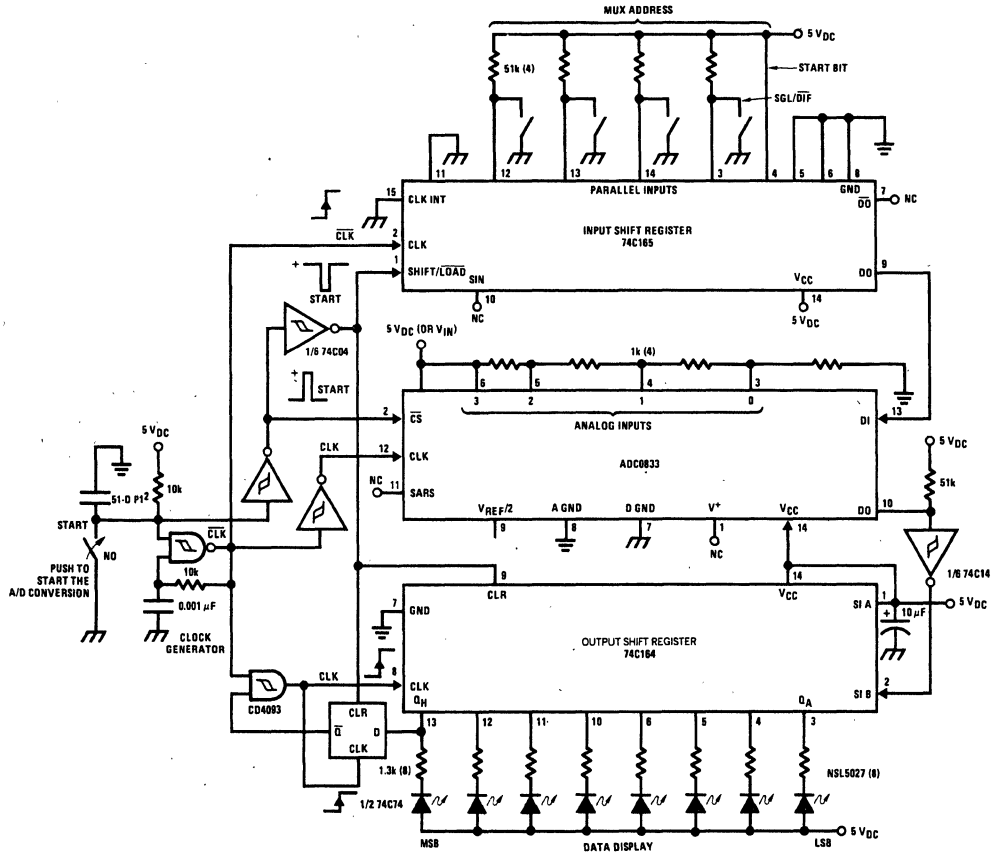
Mnemonic	Instruction
LEI	ENABLES SIO's INPUT AND OUTPUT
SC	C = 1
OGI	G0 = 0 ($\overline{CS}$ = 0)
CLR A	CLEARS ACCUMULATOR
AISC 1	LOADS ACCUMULATOR WITH 1
XAS	EXCHANGES SIO WITH ACCUMULATOR AND STARTS SK CLOCK
LDD	LOADS MUX ADDRESS FROM RAM INTO ACCUMULATOR
NOP	—
XAS	LOADS MUX ADDRESS FROM ACCUMULATOR TO SIO REGISTER
↑ 8 INSTRUCTIONS ↓	
XAS	READS HIGH ORDER NIBBLE (4 BITS) INTO ACCUMULATOR
XIS	PUTS HIGH ORDER NIBBLE INTO RAM
CLR A	CLEARS ACCUMULATOR
RC	C = 0
XAS	READS LOW ORDER NIBBLE INTO ACCUMULATOR AND STOPS SK
XIS	PUTS LOW ORDER NIBBLE INTO RAM
OGI	G0 = 1 ($\overline{CS}$ = 1)
LEI	DISABLES SIO's INPUT AND OUTPUT

8048 CODING EXAMPLE

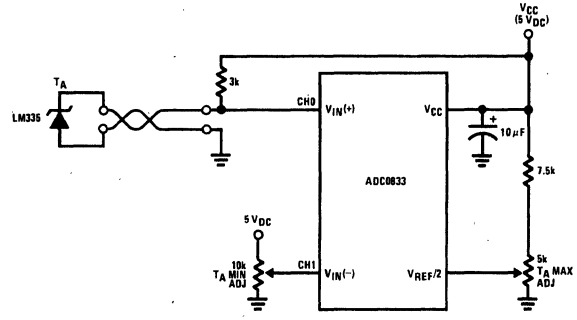
	Mnemonic		Instruction
START:	ANL	P1, #0F7H	;SELECT A/D ($\overline{CS}$ = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX ADDRESS
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT
			;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	JMP	CONT	;CONTINUE
			;BIT = 1
ONE:	ORL	P1, #1	;DI ← 1
CONT:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	CALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	IN	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETR			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0833 Evaluation



Low Cost Remote Temperature Sensor



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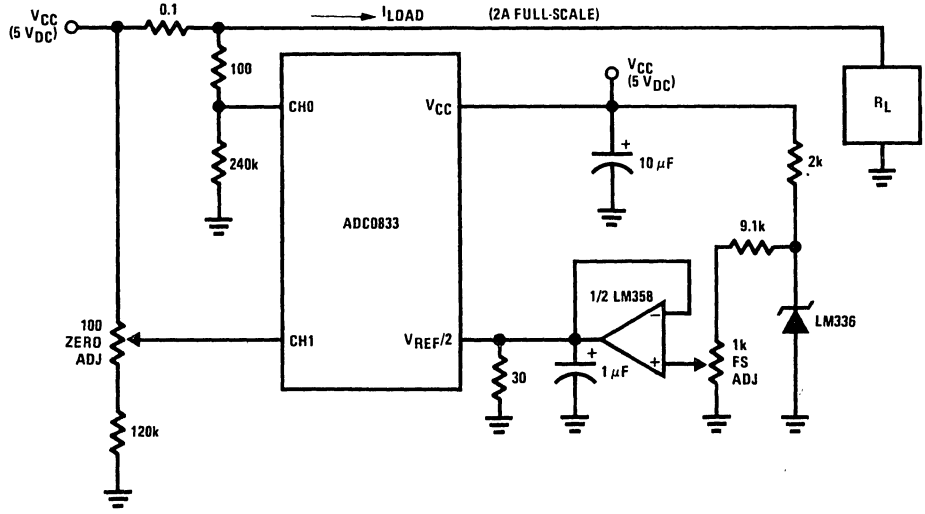
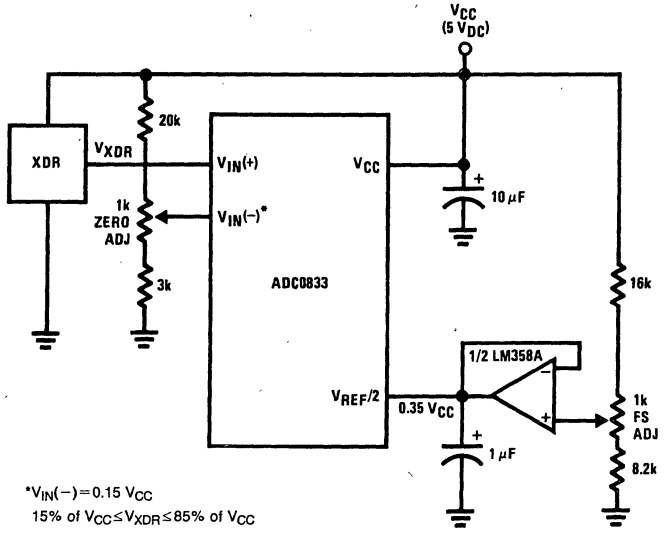
Applications (Continued)

Digitizing a Current Flow



Operating with Automotive Ratiometric Transducers



*VIN(−)=0.15 VCC
15% of VCC≤VXDR≤85% of VCC

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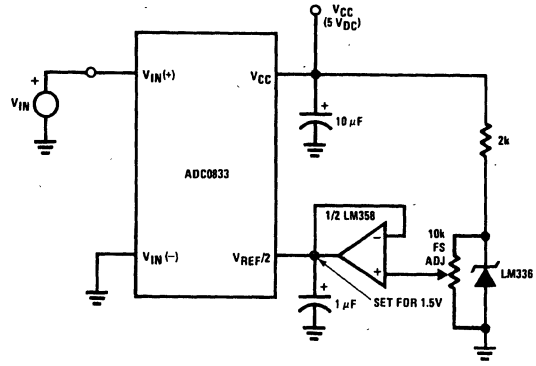
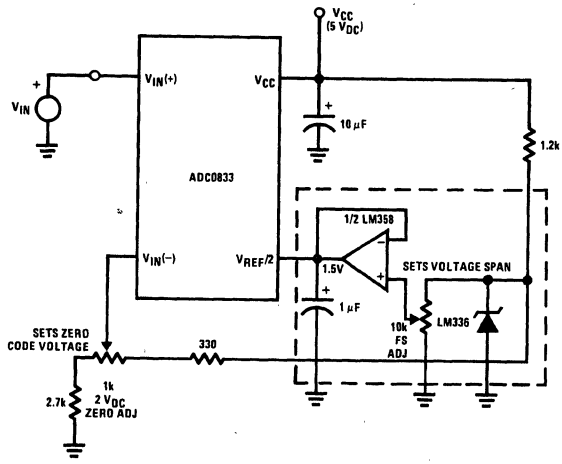
Applications (Continued)

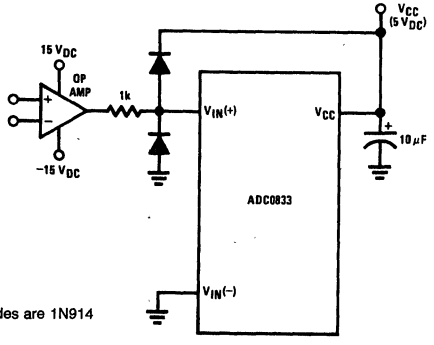
Span Adjust: $0V \leq V_{IN} \leq 3V$



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$

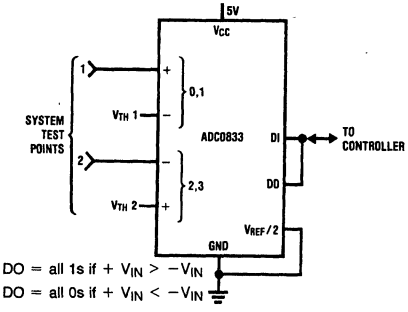


Protecting the Input



Diodes are 1N914

High Accuracy Comparators



DO = all 1s if + V_{IN} > − V_{IN}
DO = all 0s if + V_{IN} < − V_{IN}

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For additional application ideas, refer to the data sheet for the ADC0831 family of serial data converters.

Ordering Information

Part Number	Temperature Range	Total Unadjusted Error
ADC0833BCJ	−40°C to +85°C	±1/2 LSB
ADC0833BCN	0°C to +70°C	
ADC0833BJ	−55°C to +125°C	
ADC0833CCJ	−40°C to +85°C	±1 LSB
ADC0833CCN	0°C to +70°C	
ADC0833CJ	−55°C to +125°C	

National Semiconductor

ADC0844 8-Bit μP Compatible A/D Converter with 4-Channel Multiplexer

General Description

The ADC0844 is a CMOS 8-bit successive approximation A/D converter with a versatile analog input multiplexer. The 4-channel multiplexer can be software configured for single-ended, differential or pseudo-differential modes of operation.

The differential mode provides low frequency input common-mode rejection and allows offsetting the analog range of the converter. In addition, the A/D's reference can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

This A/D is designed to operate from the control bus of the NSC800™ and the wide variety of 8080 μP derivatives. TRI-STATE® output latches that directly drive the data bus permit this A/D to be configured as a memory location or as an I/O device to the microprocessor with no interface logic necessary.

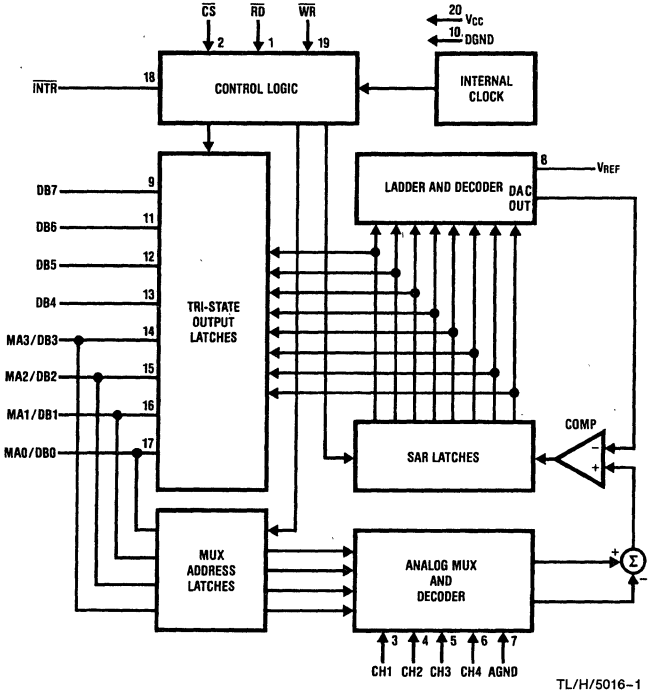
Features

- Compatible with 8080 μP derivatives—no interface logic needed
- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 4-channel multiplexer with address logic
- Internal clock
- 0V to 5V input range with single 5V power supply
- T^2L/MOS input/output compatible
- 0.3" standard width 20-pin DIP

Key Specifications

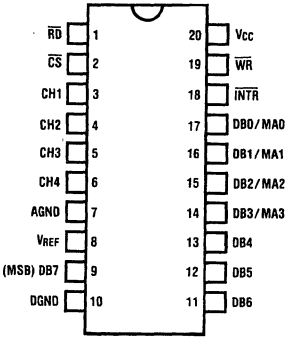
■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	10 mW
■ Conversion Time	40 μS

Block and Connection Diagrams



TL/H/5016–1

Dual-In-Line Package



TOP VIEW
TL/H/5016–2

See Ordering Information

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	6.5V
Voltage	
Logic Control Inputs	−0.3V to +15V
At Other Inputs and Outputs	−0.3V to V_{CC}+0.3V
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions (Notes 1 & 2)

Supply Voltage (V_{CC})	4.5 V_{DC} to 6.0 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0844BCN, ADC0844CCN	0°C≤T_A≤70°C
ADC0844BCJ, ADC0844CCJ	−40°C≤T_A≤85°C
ADC0844BJ, ADC0844CJ	−55°C≤T_A≤125°C

Electrical Characteristics

The following specifications apply for V_{CC}=5 V_{DC} unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	ADC0844BJ, ADC0844BCJ ADC0844CJ, ADC0844CCJ			ADC0844BCN, ADC0844CCN			Limit Units
		Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Maximum Total Unadjusted Error	V_{REF} = 5.00 V_{DC} (Note 3)							
ADC0844BCN						±½	±½	LSB
ADC0844BJ, BCJ			±½					LSB
ADC0844CCN						±1	±1	LSB
ADC0844CJ, CCJ			±1					LSB
Minimum Reference Input Resistance		2.4	**1.1**		2.4	1.2	**1.1**	kΩ
Maximum Reference Input Resistance		2.4	**4.1**		2.4	3.8	**4.1**	kΩ
Maximum Common-Mode Input Range	(Note 4)		**V_{CC}+0.05**			V_{CC}+0.05	**V_{CC}+0.05**	V
Minimum Common-Mode Input Range	(Note 4)		**GND−0.05**			GND−0.05	**GND−0.05**	V
DC Common-Mode Error	Differential Mode	±1/16	±¼		±1/16	±¼	±¼	LSB
Power Supply Sensitivity	V_{CC} = 5V±5%	±1/16	±⅛		±1/16	±⅛	±⅛	LSB
Off Channel Leakage Current	(Note 8)							
	On Channel = 5V, Off Channel = 0V		−1			−0.1	−1	μA
	On Channel = 0V, Off Channel = 5V		1			0.1	1	μA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC} = 5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC} = 4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN} = 5.0V	0.005	1		0.005		1	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN} = 0V	−0.005	−1		−0.005		−1	μA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC} = 4.75V							
	I_{OUT} = −360 μA		**2.4**			2.8	**2.4**	V
	I_{OUT} = −10 μA		**4.5**			4.6	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**			0.34	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT} = 0V	−0.01	−3		−0.01	−0.3	−3	μA
	V_{OUT} = 5V	0.01	3		0..01	0.3	3	μA
I_{SOURCE}, Output Source Current (Min)	V_{OUT} = 0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SNK}, Output Sink Current (Min)	V_{OUT} = V_{CC}	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max)	$\overline{CS}$ = 1, V_{REF} Open	1	**2.5**		1	2.3	**2.5**	mA

AC Characteristics

Parameter	Conditions	Typ (Note 5)	Tested Limit (Note 6)	Design Limit (Note 7)	Units
t_C, Maximum Conversion Time (See Graph)		30	40		μS
$t_{W(WR)}$, Minimum $\overline{WR}$ Pulse Width	(Note 9)	50		150	ns
t_{ACC}, Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF (Note 9)	145		225	ns
t_{1H}, t_{0H}, TRI-STATE Control (Maximum Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (Note 9)	125		200	ns
t_{WI}, t_{RI}, Maximum Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$	(Note 9)	200		400	ns
t_{DS}, Minimum Data Set-Up Time	(Note 9)	50		100	ns
t_{DH}, Minimum Data Hold Time	(Note 9)	0		50	ns
C_{IN}, Capacitance of Logic Inputs		5			pF
C_{OUT}, Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of device may be impaired.

Note 2: All voltages are measured with respect to ground.

Note 3: Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Guaranteed and 100% production tested.

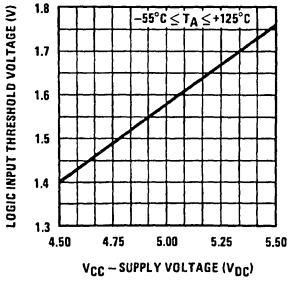
Note 7: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 8: Off channel leakage current is measured after the channel selection.

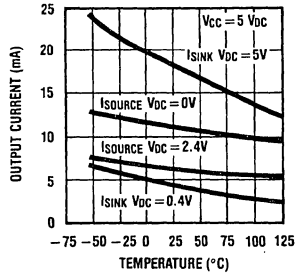
Note 9: The temperature coefficient is 0.3%/°C.

Typical Performance Characteristics

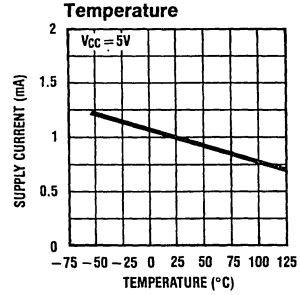
Logic Input Threshold Voltage vs Supply Voltage



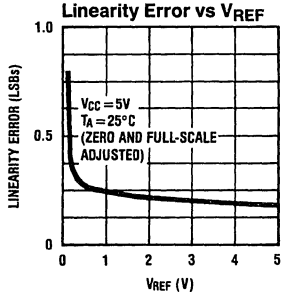
Output Current vs Temperature



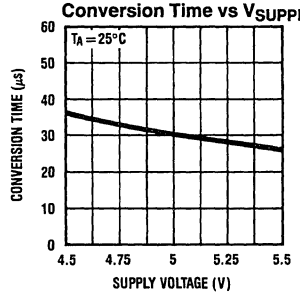
Power Supply Current vs Temperature



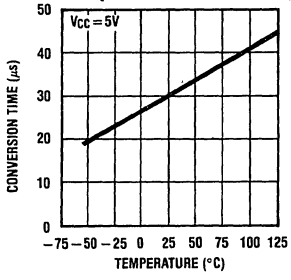
Linearity Error vs V_{REF}



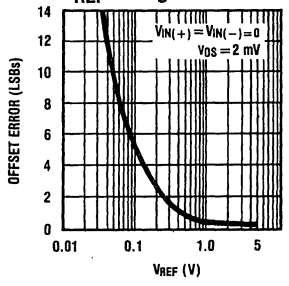
Conversion Time vs V_{SUPPLY}



Conversion Time vs Temperature



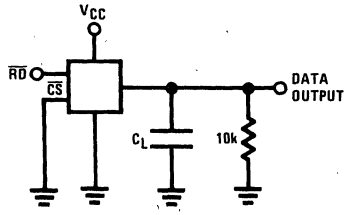
Unadjusted Offset Error vs V_{REF} Voltage



TL/H/5016–3

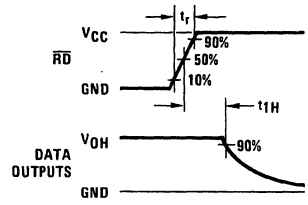
TRI-STATE Test Circuits and Waveforms

t_{1H}



TL/H/5016-4

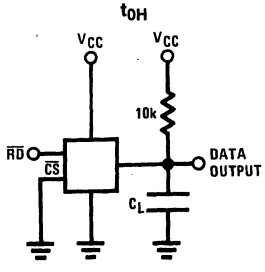
t_{1H}, C_L = 10 pF



TL/H/5016-5

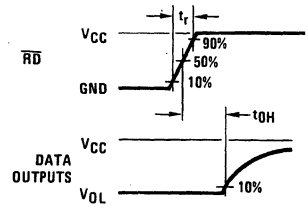
t_r = 20 ns

t_{0H}



TL/H/5016-6

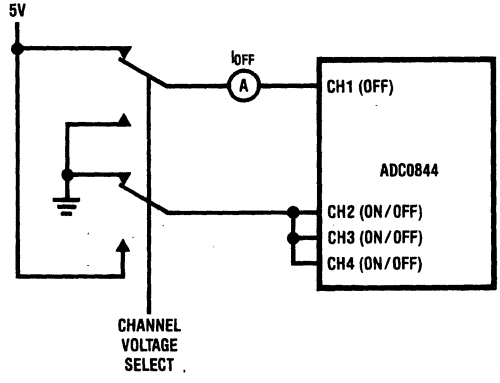
t_{0H}, C_L 10 pF



TL/H/5016-7

t_r = 20 ns

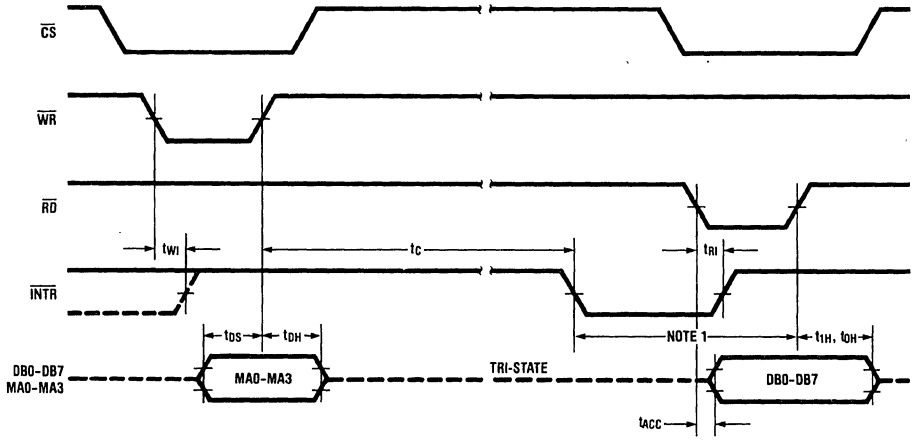
Leakage Current Test Circuit



TL/H/5016-8

Timing Diagrams

Programming New Channel Configuration and Starting a Conversion

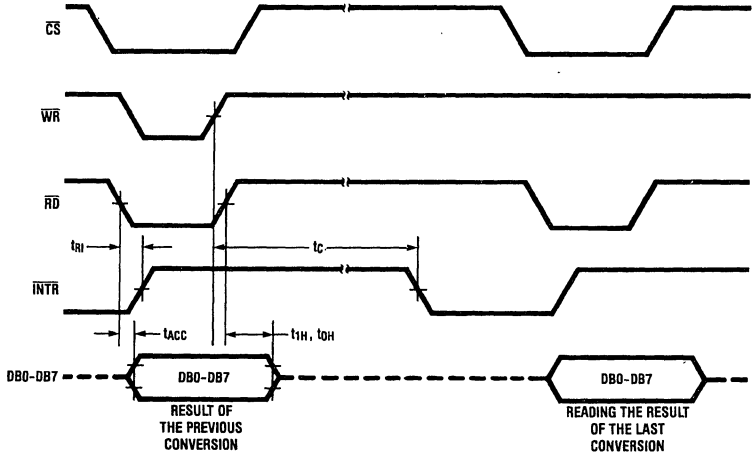


TL/H/5016-9

Note 1: Read strobe must occur at least 600 ns after the assertion of interrupt to guarantee reset of $\overline{INTR}$.

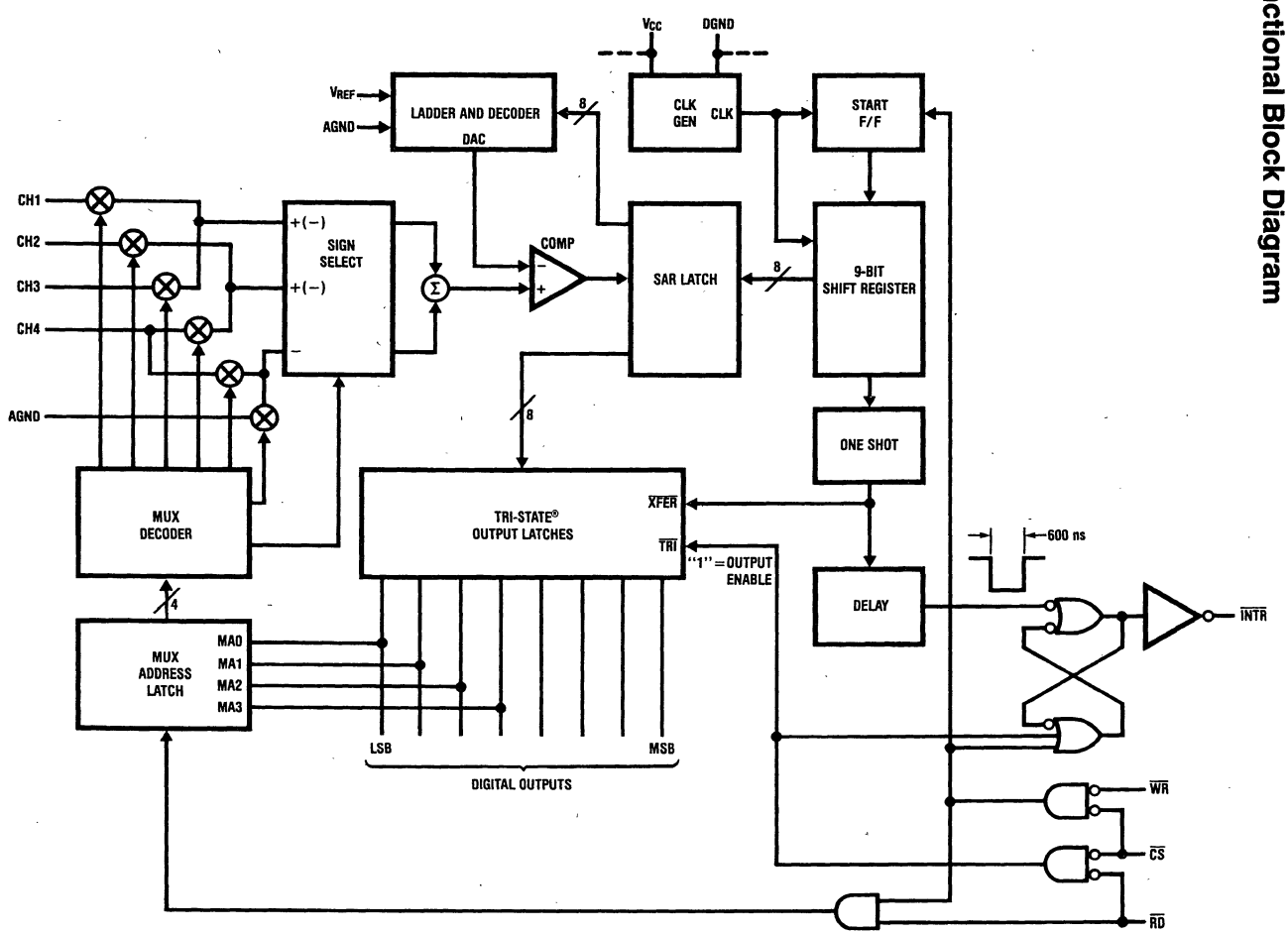
Note 2: MA stands for MUX address.

Using the Previously Selected Channel Configuration and Starting a Conversion



TL/H/5016-10

Functional Block Diagram



TL/H/5016–11

Functional Description

The ADC0844 contains a 4-channel analog multiplexer (MUX) which can be configured in a single-ended, differential, or pseudo-differential mode (Table 1). The specific mode is selected by loading the MUX address latch with the proper address. Inputs to the MUX address latch (MA0-MA3) are common with data bus lines (DB0-DB3) and are enabled when the $\overline{RD}$ line is high. A conversion is initiated via the $\overline{CS}$ and $\overline{WR}$ lines. If the data from a previous conversion is not read, the $\overline{INTR}$ line will be low. The falling edge of $\overline{WR}$ will reset the $\overline{INTR}$ line high and ready the A/D for a conversion cycle. The rising edge of $\overline{WR}$, with $\overline{RD}$ high, strobes the data on the MA0/DB0-MA3/DB3 inputs into the MUX address latch to select a new input configuration and start a conversion. If the $\overline{RD}$ line is held low during the entire low period of $\overline{WR}$ the previous MUX configuration is retained, and the data of the previous conversion is the output on lines DB0-DB7. After the conversion cycle ($t_C \leq 40\ \mu S$), which is set by the internal clock frequency, the digital data is transferred to the output latch and the $\overline{INTR}$ is asserted low. Taking $\overline{CS}$ and $\overline{RD}$ low resets $\overline{INTR}$ output high and outputs the conversion result on the data lines (DB0-DB7).

Applications Information

1.0 MULTIPLEXER CONFIGURATION

The design of these converters utilizes a sample-data comparator structure which allows a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single-

TABLE I. ADC0844 MUX ADDRESSING

MUX Address				$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	Channel #					MUX Mode
MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	AGND	
X	L	L	L	L	↓	H	+	−				Differential
X	L	L	H	L		H	−	+				
X	L	H	L	L		H			+	−		
X	L	H	H	L		H			−	+		
L	H	L	L	L	↓	H	+				−	Single-Ended
L	H	L	H	L		H		+			−	
L	H	H	L	L		H			+		−	
L	H	H	H	L		H				+	−	
H	H	L	L	L	↓	H	+				−	Pseudo-Differential
H	H	L	H	L		H		+			−	
H	H	H	L	L		H			+		−	
X	X	X	X	L	↓	L	Previous Channel Configuration					

X = don't care

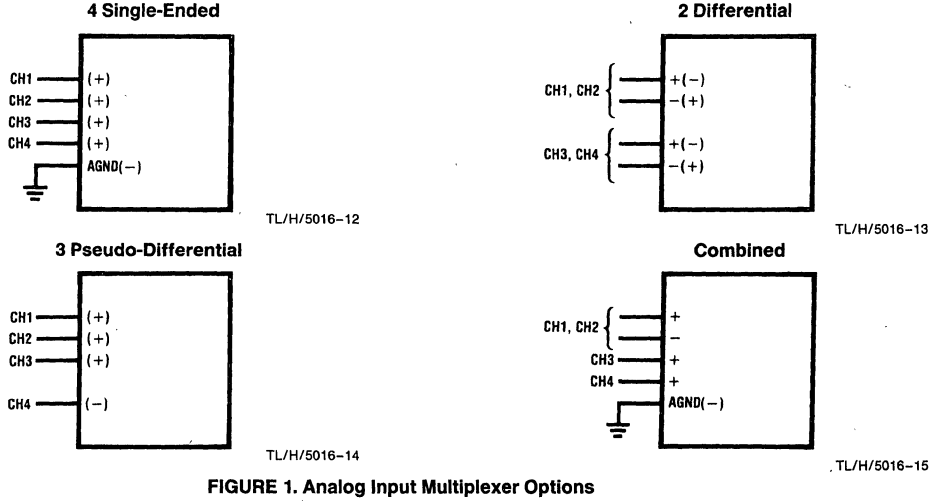


FIGURE 1. Analog Input Multiplexer Options

Applications Information (Continued)

ended, or pseudo-differential (*Figure 1*). In the differential mode, the channel inputs are grouped in pairs, CH1 with CH2 and CH3 with CH4. The polarity assignment of each channel in the pair is interchangeable. The single-ended mode has CH1–CH4 assigned as the positive input with the negative input being the analog ground (AGND) of the device. Finally, in the pseudo-differential mode CH1–CH3 are positive inputs referenced to CH4 which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 2.4 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (*Figure 2a*), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy (*Figure 2b*), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).

3.0 THE ANALOG INPUTS

3.1 Analog Differential Voltage Inputs and Common-Mode Rejection

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" inputs is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

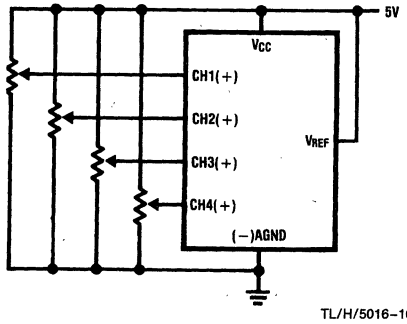
$$V_{ERROR(MAX)} = V_{peak}\,(2\pi\, f_{CM}) \times 0.5 \times \left(\frac{t_C}{8}\right)$$

where f_{CM} is the frequency of the common-mode signal, Vpeak is its peak voltage value and t_C is the conversion time.

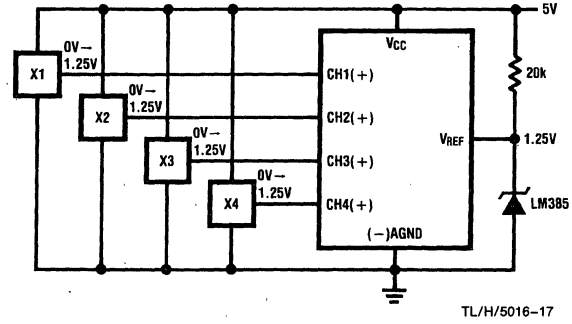
For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 40 μS, its peak value would have to be 5.43V. This large a common-mode signal is much greater than that generally found in a well designed data acquisition system.

3.2 Input Current

Due to the sampling nature of the analog inputs short duration spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.



a) Ratiometric



b) Absolute with a Reduce Span

FIGURE 2. Referencing Examples

Applications Information (Continued)

3.3 Input Source Resistance

The limitation of the input source resistance due to the DC leakage currents of the input multiplexer is important. A worst-case leakage current of ± 1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

4.0 OPTIONAL ADJUSTMENTS

4.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This is useful for either differential or pseudo-differential modes of input channel configuration.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the V^- input and applying a small magnitude positive voltage to the V^+ input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF} = 5.000\ V_{DC}$).

4.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input for a digital output code changing from 1111 1110 to 1111 1111.

4.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper V_{IN} (+) voltage applied] by forcing a voltage to the $V_{IN}(-)$ input which is given by:

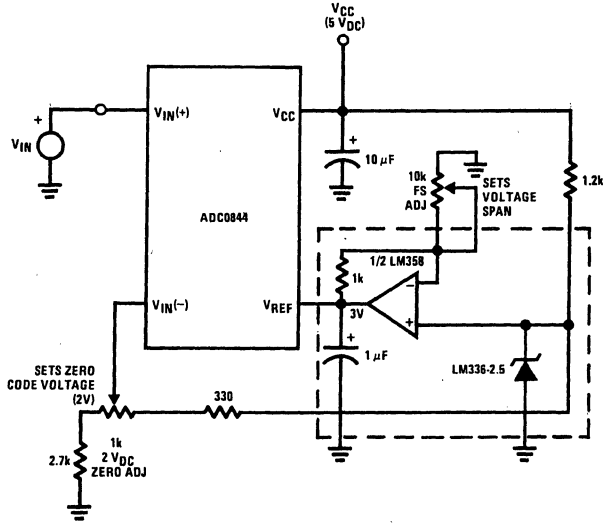
$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where V_{MAX} = the high end of the analog input range and V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

For an example see the Zero-Shift and Span Adjust circuit below.

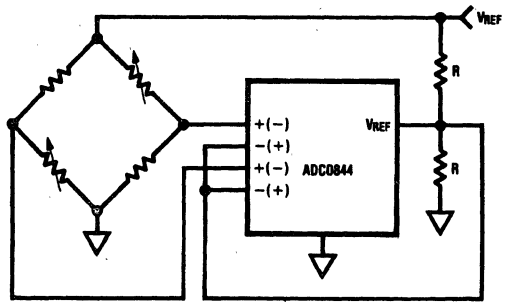
Zero-Shift and Span Adjust (2V ≤ V_{IN} ≤ 5V)



TL/H/5016–18

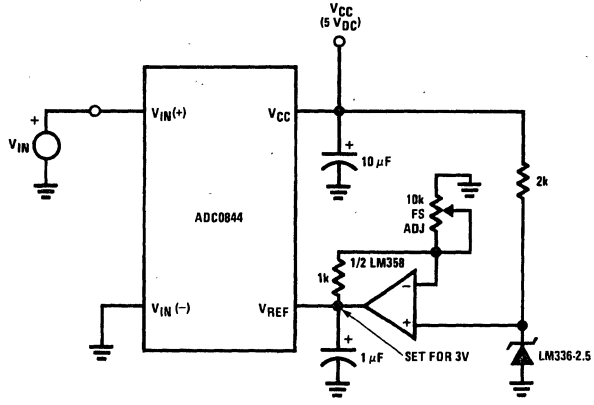
Applications Information (Continued)

Differential Voltage Input 9-Bit A/D



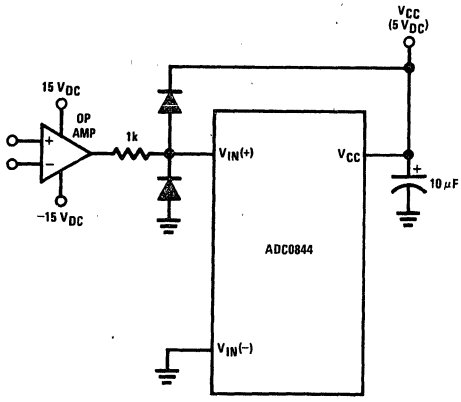
TL/H/5016–19

Span Adjust $0V \leq V_{IN} \leq 3V$



TL/H/5016–20

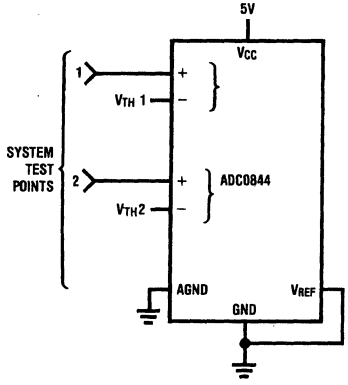
Protecting the Input



TL/H/5016–21

Diodes are 1N914

High Accuracy Comparators

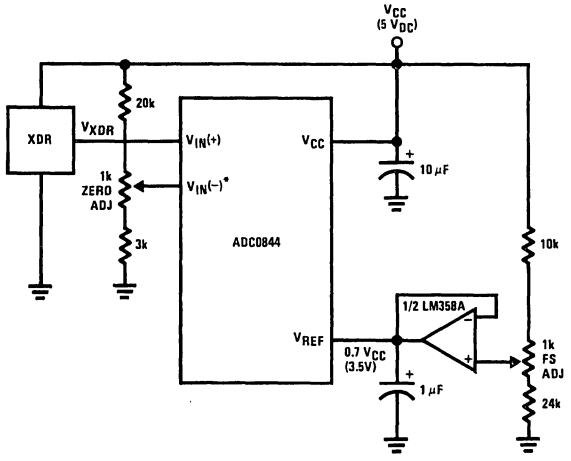


TL/H/5016–22

DO = all 1s if $V_{IN}(+) > V_{IN}(-)$
DO = all 0s if $V_{IN}(+) < V_{IN}(-)$

Applications Information (Continued)

Operating with Automotive Ratiometric Transducers

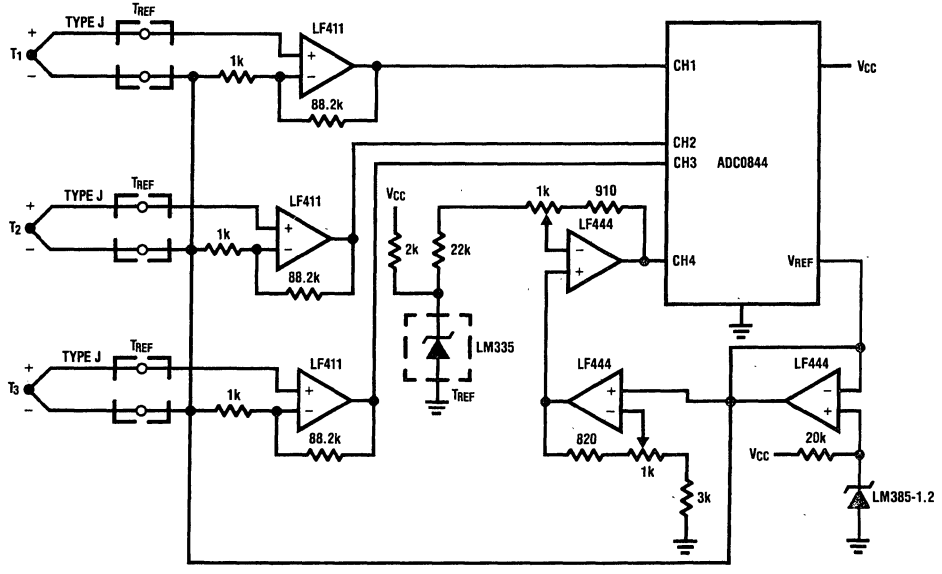


TL/H/5016–23

*$V_{IN}(-) = 0.15\ V_{CC}$

15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Converting 3 Thermocouples with only One Cold-Junction Compensator

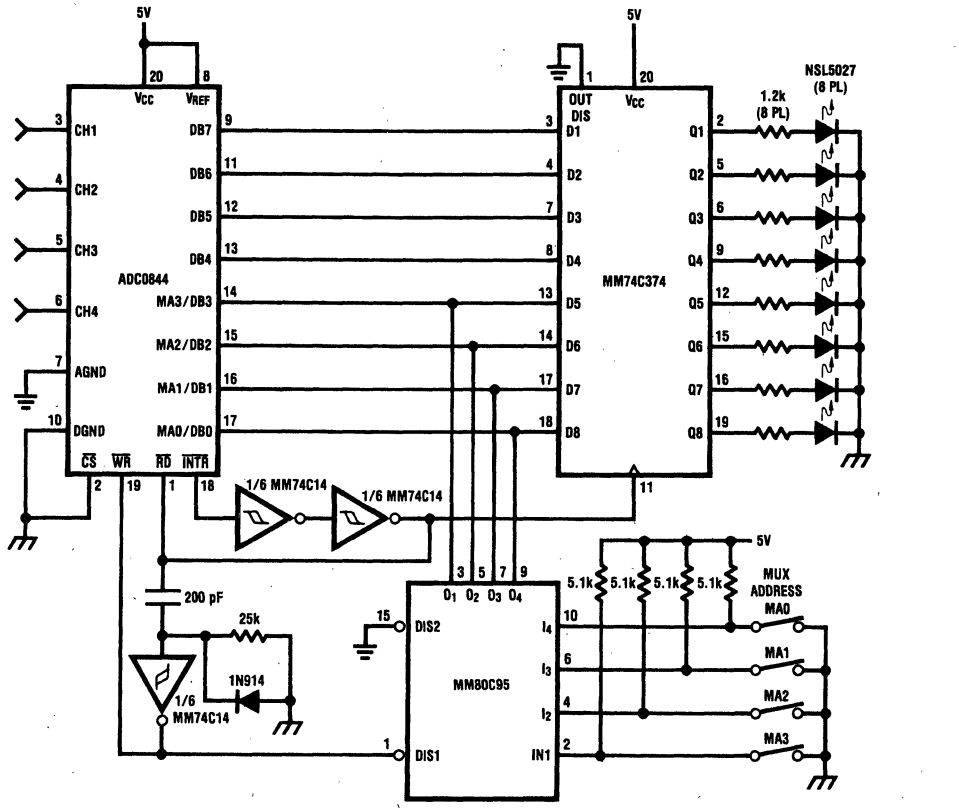


TL/H/5016–24

Uses the pseudo-differential mode to keep the differential inputs constant with changes in reference temperature (T_{REF}).

Applications Information (Continued)

A Stand Alone Circuit



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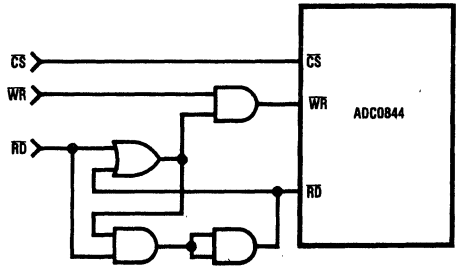
Start a Conversion without Updating the Channel Configuration



TL/H/5016–26

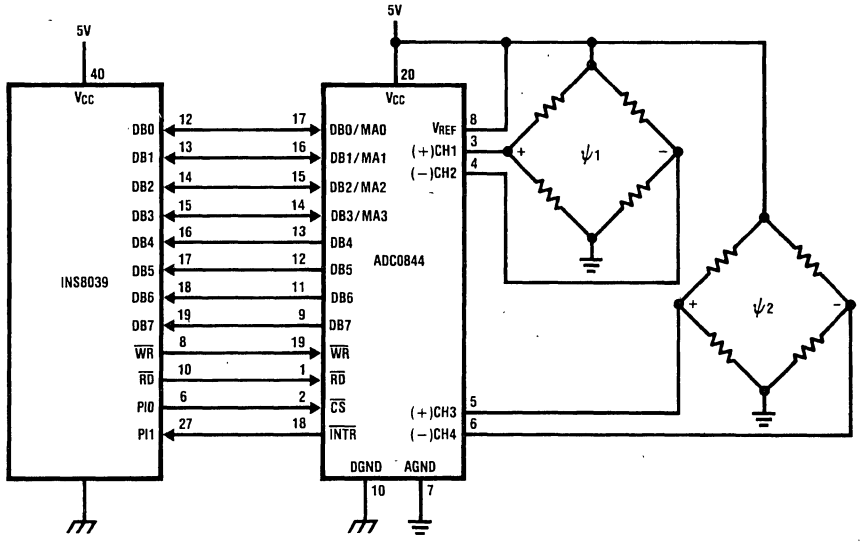
$\overline{CS}$•$\overline{WR}$ will update the channel configuration and start a conversion.

$\overline{CS}$•$\overline{RD}$ will read the conversion data and start a new conversion without updating the channel configuration.

Waiting for the end of this conversion is not necessary. A $\overline{CS}$•$\overline{WR}$ can immediately follow the $\overline{CS}$•$\overline{RD}$.

Applications Information (Continued)

ADC0844—INS8039 Interface



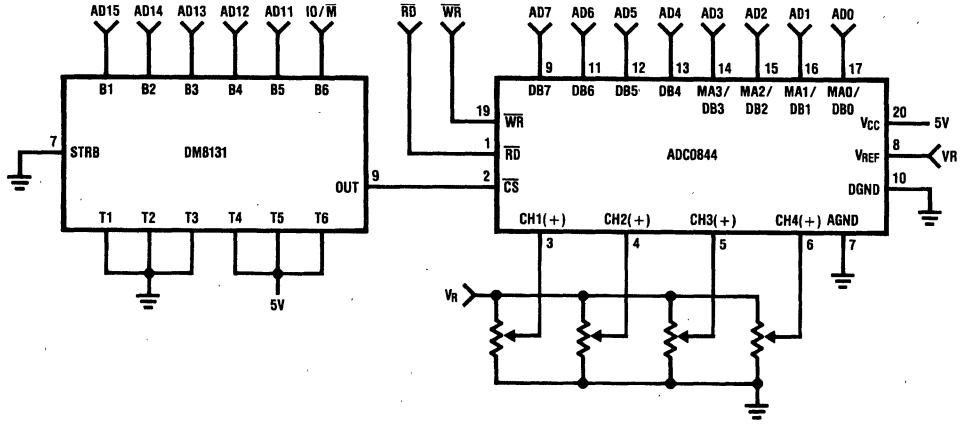
TL/H/5016–27

SAMPLE PROGRAM FOR ADC0844—INS8039 INTERFACE
CONVERTING TWO RATIOMETRIC, DIFFERENTIAL SIGNALS

```
                        ORG     0H
0000    04 10           JMP     BEGIN       ;START PROGRAM AT ADDR 10
                        ORG     10H         ;MAIN PROGRAM
0010    B9 FF   BEGIN:  MOV     R1,#0FFH    ;LOAD R1 WITH A UNUSED ADDR
                                            ;LOCATION
0012    B8 20           MOV     R0#20H      ;A/D DATA ADDRESS
0014    89 FF           ORL     P1,#0FFH    ;SET PORT 1 OUTPUTS HIGH
0016    23 00           MOV     A,00H       ;LOAD THE ACC WITH A/D MUX DATA
                                            ;CH1 AND CH2 DIFFERENTIAL
0018    14 50           CALL    CONV        ;CALL THE CONVERSION SUBROUTINE
001A    23 02           MOV     A,#02H      ;LOAD THE ACC WITH A/D MUX DATA
                                            ;CH3 AND CH4 DIFFERENTIAL
001C    18              INC     R0          ;INCREMENT THE A/D DATA ADDRESS
001D    14 50           CALL    CONV        ;CALL THE CONVERSION SUBROUTINE

                        ;CONTINUE MAIN PROGRAM

                        ;CONVERSION SUBROUTINE
                        ;ENTRY:ACC—A/D MUX DATA
                        ;EXIT: ACC—CONVERTED DATA

                        ORG     50H
0050    99 FE   CONV:   ANL     P1,#0FEH    ;CHIP SELECT THE A/D
0052    91              MOVX    @R1,A       ;LOAD A/D MUX & START CONVERSION
0053    09      LOOP:   IN      A,P1        ;INPUT INTR STATE
0054    32 53           JB1     LOOP        ;IF INTR = 1 GOTO LOOP
0056    81              MOVX    A,@R1       ;IF INTR = 0 INPUT A/D DATA
0057    89 01           ORL     P1 &01H     ;CLEAR THE A/D CHIP SELECT
0059    A0              MOV     @R0,A       ;STORE THE A/D DATA
005A    83              RET                 ;RETURN TO MAIN PROGRAM
```

Applications Information (Continued)

I/O Interface to NSC800



TL/H/5016–28

SAMPLE PROGRAM FOR ADC0844—NSC800 INTERFACE

```
0008                    NCONV       EQU     8
000F                    DEL         EQU     15          ;DELAY 50 μsec CONVERSION
001F                    CS          EQU     1FH         ;THE BOARD ADDRESS
3C00                    ADDTA       EQU     003CH       ;START OF RAM FOR A/D
                                                        ;DATA
0000'   0B 0A 09        MUXDTA:     DB      0BH,0AH,09H ;MUX DATA
0003'   08              START:      DB      08H
0004'   0E 1F                      LD      C,CS
0006'   06 08                      LD      B,NCONV
0008'   21 0000'                   LD      HL,MUXDTA
000B'   11 003C                    LD      DE,ADDTA
000E'   ED A3           STCONV:     OUTI                ;LOAD A/D'S MUX DATA
                                                        ;AND START A CONVERSION
0010'   EB                          EX      DE,HL       ;HL=RAM ADDRESS FOR THE
                                                        ;A/D DATA
0011'   3E 0F                      LD      A,DEL
0013'   3D             WAIT:       DEC     A           ;WAIT 50 μsec FOR THE
0014'   C2 0013'                    JP      NZ,WAIT     ;CONVERSION TO FINISH
0017'   ED A2                      INI                 ;STORE THE A/D'S DATA
                                                        ;CONVERTED ALL INPUTS?
0019'   EB                          EX      DE,HL
001A'   C2 000E'                    JP      NZ,STCONV   ;IF NOT GOTO STCONV

                                    END
```

Note: This routine sequentially programs the MUX data latch in the signal-ended mode. For CH1-CH4 a conversion is started, then a 50 μS wait for the A/D to complete a conversion and the data is stored at address ADDTA for CH1, ADDTA + 1 for CH2, etc.

Ordering Information

Temperature Range	0°C to 70°C	−40°C to +85°C	−55°C to +125°C
±½ LSB Unadjusted	ADC0844BCN	ADC0844BCJ	ADC0844BJ
±1 LSB Unadjusted	ADC0844CCN	ADC0844CCJ	ADC0844CJ
Package Outline	N20A—Molded DIP	J20A—CERDIP	J20A—CERDIP

National Semiconductor

ADC1210, ADC1211 12-Bit CMOS A/D Converters

General Description

The ADC1210, ADC1211 are low power, medium speed, 12-bit successive approximation, analog-to-digital converters. The devices are complete converters requiring only the application of a reference voltage and a clock for operation. Included within the device are the successive approximation logic, CMOS analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator.

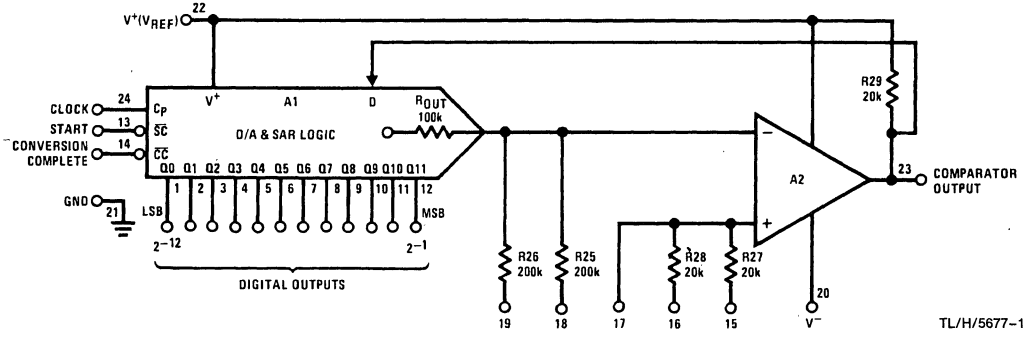
The ADC1210 offers 12-bit resolution and 12-bit accuracy, and the ADC1211 offers 12-bit resolution with 10-bit accuracy. The inverted binary outputs are directly compatible with CMOS logic. The ADC1210, ADC1211 will operate over a wide supply range, convert both bipolar and unipolar analog inputs, and operate in either a continuous conversion mode or logic-controlled START-STOP conversion mode. The devices are capable of making a 12-bit conversion in 100 μs typ, and can be connected to convert 10 bits in 30 μs.

Both devices are available in military and industrial temperature ranges.

Features

- 12-bit resolution
- ±¾ LSB or ±2 LSB nonlinearity
- Single +5V to ±15V supply range
- 100 μs 12-bit, 30 μs 10-bit conversion rate
- CMOS compatible outputs
- Bipolar or unipolar analog inputs
- 200 kΩ analog input impedance

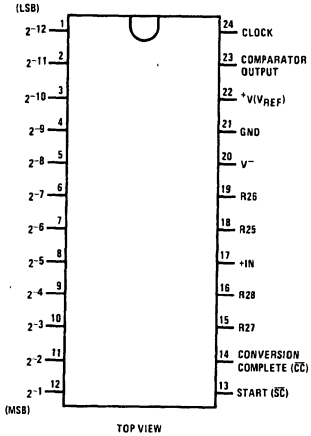
Block Diagram



TL/H/5677–1

Connection Diagram

Dual-In-Line Package



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Order Number ADC1210HD, ADC1210HCD, ADC1211HD, ADC1211HCD
See NS Package D24D

Absolute Maximum Ratings

Maximum Reference Supply Voltage (V^+)	16V	Power Dissipation	See Curves
Maximum Negative Supply Voltage (V^-)	−20V	Operating Temperature Range	
Voltage At Any Logic Pin	$V^+ + 0.3V$	ADC1210HD, ADC1211HD	−55°C to +125°C
Analog Input Voltage	±15V	ADC1210HCD, ADC1211HCD	−25°C to +85°C
Maximum Digital Output Current	±10 mA	Storage Temperature Range	−65°C to +150°C
Maximum Comparator Output Current	50 mA	Lead Temperature (Soldering, 10 seconds)	300°C
Comparator Output Short-Circuit Duration	5 Seconds		

DC Electrical Characteristics (Notes 1 and 2)

Parameter	Conditions	ADC1210			ADC1211			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		12			12			Bits
Linearity Error	(Note 3) $f_{CLK}=65$ kHz, $T_A=25°C$ $f_{CLK}=65$ kHz			 ±0.0183 ±0.0366			 ±0.0488	 % FS % FS
Full Scale Error	$T_A=25°C$, Unadjusted			0.20			0.50	% FS
Zero Scale Error	$T_A=25°C$, Unadjusted			0.20			0.50	% FS
Quantization Error				±1/2			±1/2	LSB
Input Resistor Values	R27, R28		20			20		kΩ
Input Resistor Values	R25, R26		200			200		kΩ
Input Resistor Ratios	R25/R26, R27/R28			0.8			0.8	%
Logic "1" Input Voltage		8			8			V
Logic "0" Input Voltage				2			2	V
Logic "1" Input Current	$V_{IN}=10.24V$			1			1	μA
Logic "0" Input Current	$V_{IN}=0V$			−1			−1	μA
Logic "1" Output Voltage	$I_{OUT}\leq -1$ μA	9.2			9.2			V
Logic "0" Output Voltage	$I_{OUT}\leq 1$ μA			0.5			0.5	V
Positive Supply Current	$V^+=15V$, $f_{CLK}=65$ kHz, $T_A=25°C$		5	8		5	8	mA
Negative Supply Current	$V^-=-15V$, $T_A=25°C$		4	6		4	6	mA

AC Electrical Characteristics $T_A=25°C$, (Notes 1 and 2)

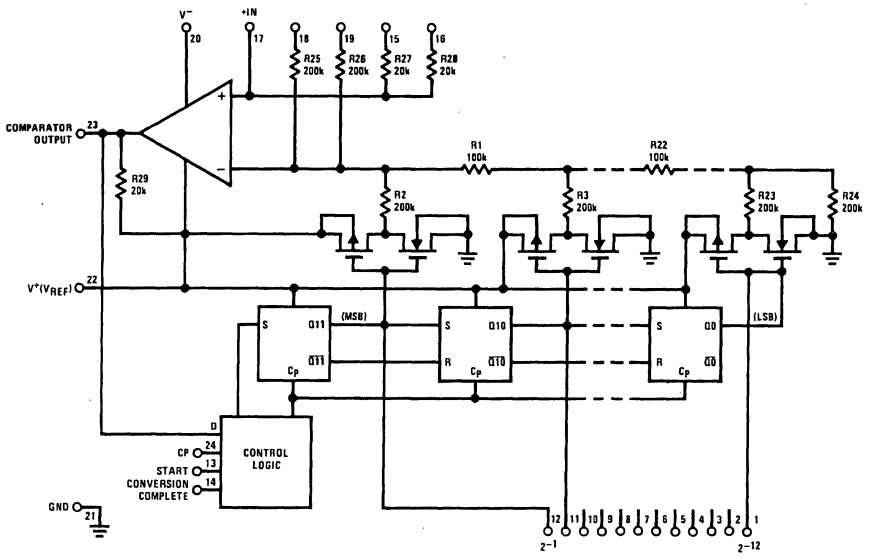
Parameter	Conditions	Min	Typ	Max	Units
Conversion Time			100	200	μs
Maximum Clock Frequency			130	65	kHz
Clock Pulse Width		100	50		ns
Propagation Delay From Clock to Data Output	$t_r\leq t_f\leq 10$ ns		60	150	ns
(Q0 to Q11)					
Propagation Delay from Clock to Conversion	$t_r\leq t_f\leq 10$ ns		60	150	ns
Complete					
Clock Rise and Fall Time				5	μs
Input Capacitance			10		pF
Start Conversion Set-Up Time		30			ns

Note 1: Unless otherwise noted, these specifications apply for $V^+=10.240V$, $V^-=-15V$, over the temperature range −55°C to +125°C for the ADC1210HD, ADC1211HD, and −25°C to +85°C for the ADC1210HCD, ADC1211HCD.

Note 2: All typical values are for $T_A=25°C$.

Note 3: Unless otherwise noted, this specification applies over the temperature range −25°C to +85°C. Provision is made to adjust zero scale error to 0V and full-scale to 10.2375V during testing. Standard linearity test circuit is shown in *Figure 5a*.

Schematic Diagram



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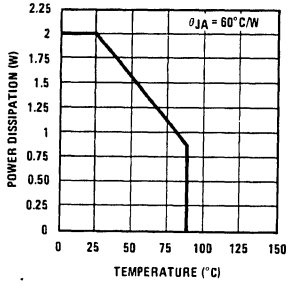
Note: 3 bits shown for clarity

Power Dissipation vs Temperature



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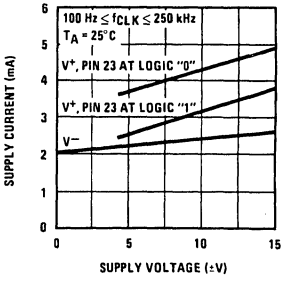
Supply Current vs Supply Voltage

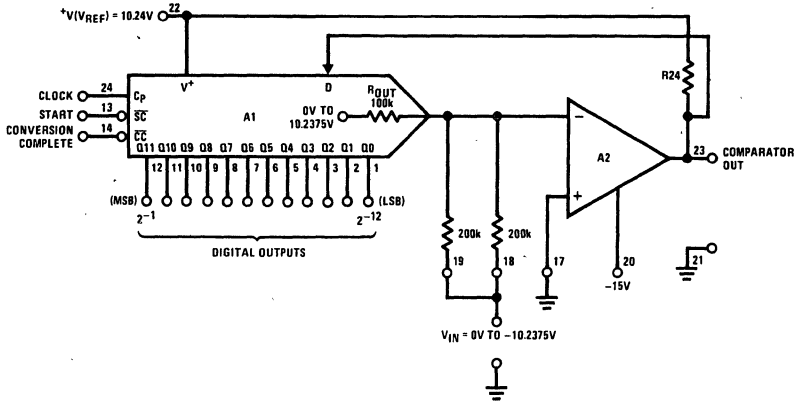


TL/H/5677–5

1.0 THEORY OF OPERATION

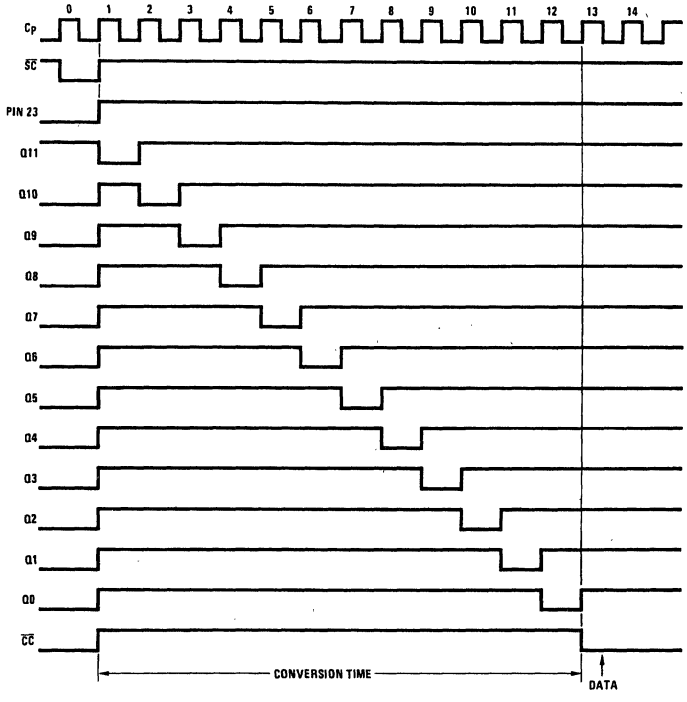
The ADC1210, ADC1211 are successive approximation analog-to-digital converters, i.e., the conversion takes place 1 bit at a time by comparing the output of the internal D/A to the (unknown) input voltage. The START input (pin 13), when taken low, causes the register to reset synchronously on the next CLOCK low-to-high transition. The MSB, Q11 is set to the low state, and the remaining bits, Q0 through Q10, will be set to the high state. The register will remain in this state until the $\overline{SC}$ input is taken high. When START goes high, the conversion will begin on the low-to-high transition of the CLOCK pulse. Q11 will then assume the state of pin 23. If pin 23 is high, Q11 will be high; if pin 23 is low, Q11 will remain low. At the same time, the next bit Q10 is set low. All remaining bits, Q0–Q9 will remain unchanged (high). This process will continue until the LSB (Q0) is found. When the conversion process is completed, it is indicated by CONVERSION COMPLETE ($\overline{CC}$) (pin 14) going low. The logic levels at the data output pins (pins 1–12) are the complemented-binary representation of the converted analog signal with Q11 being the MSB and Q0 being the LSB. The register will remain in the above state until the $\overline{SC}$ is again taken low.

An application example is shown in *Figure 1*. In this case, a 0 to −10.2375V input is being converted using the ADC1210 with $V^+ = 10.240V$, $V^- = -15V$. *Figure 1b* is the timing diagram for full scale input. *Figure 1c* is the timing diagram for zero scale input, *Figure 1d* is the timing diagram for −3.4125V input (010101010101 = output).



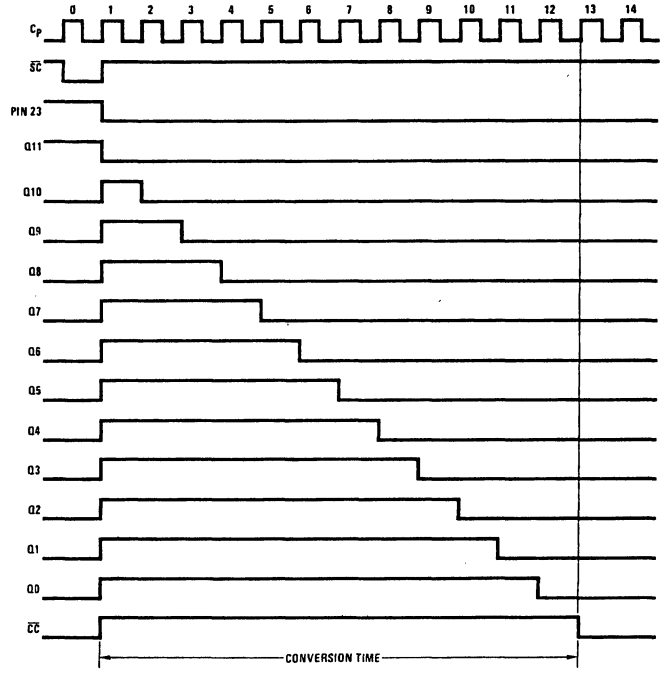
TL/H/5677–6

FIGURE 1a. ADC1210 Connected for 0V to −10.2375V (Natural Binary Output)



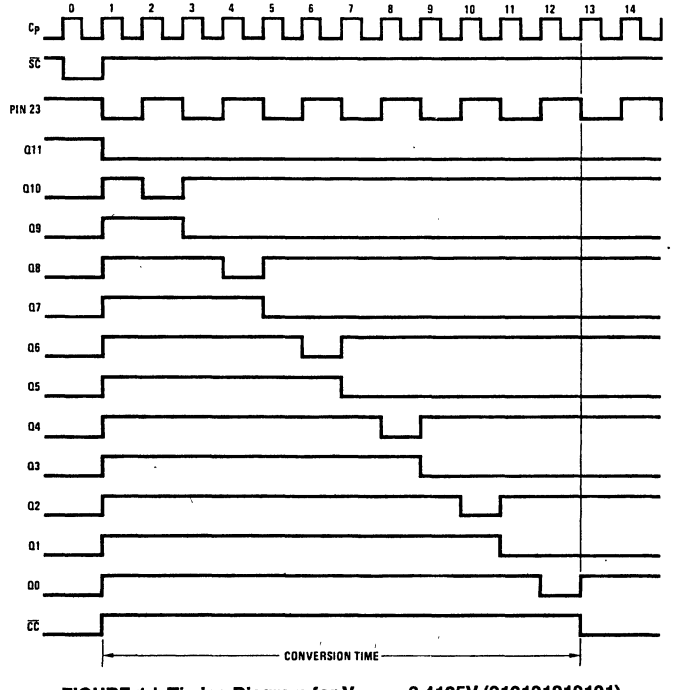
TL/H/5677–7

FIGURE 1b. Timing Diagram for V_{IN} = Full Scale Input



TL/H/5677–8

FIGURE 1c. Timing Diagram for V_{IN} = Zero Scale



TL/H/5677–9

FIGURE 1d. Timing Diagram for V_{IN} = −3.4125V (010101010101)

TABLE 1. Pin Assignments and Explanations

Pin Number	Mnemonic	Function
1–12	Q11–Q0	Digital (data) output pins. This information is a parallel 12-bit complemented binary representation of the converted analog signal. All data is valid when "Conversion Complete" goes low. Logic levels are ground and V+.
13	$\overline{SC}$	Start Conversion is a logic input which causes synchronous reset of the successive approximation register and initiates conversion. Logic levels are ground and V+.
14	$\overline{CC}$	"Conversion Complete" is a digital output signal which indicates the status of the converter. When $\overline{CC}$ is high, conversion is taking place, when low conversion is completed. Logic levels are ground and V+.
15, 16	R27, R28	R27 and R28 are two application resistors connected to the comparator non-inverting input. The resistors may be used in various modes of operation. Their nominal values are 20 kΩ each. See Applications section.
17	+IN	Non-inverting input of the analog comparator. This node is used in various configurations and for compensation of the loop. See Applications section.
18, 19	R25, R26	R25 and R26 are two application resistors that are tied internally to the inverting input of the comparator. Their nominal values are 200 kΩ each. See Applications section. The R-2R ladder network will have the same temperature coefficient as these resistors.
20	V−	Negative supply voltage for bias of the analog comparator. Optionally may be grounded or operated with voltages to −20V.
21	GND	Ground for both digital and analog signals.
22	V+ (V_{REF})	V+ sets both maximum full scale and input and output logic levels.
23	CO	Comparator output.
24	C_P	Clock is an input which causes the successive approximation (shift) register to advance through the conversion sequence. Logic levels are ground and V+.

2.0 APPLICATIONS

2.1 Power Supply Considerations and Decoupling

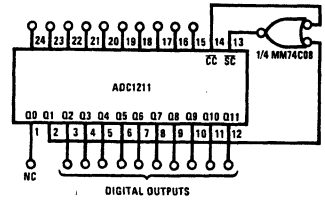
Pin 22 is both the positive supply and voltage reference input to the ADC1210, ADC1211. The magnitude of V+ determines the input logic "1" threshold and the output voltage from the CMOS SAR. The device will operate over a range of V+ from 5V to 15V. However, in order to preserve 12-bit accuracy, V+ should be well regulated (0.01%) and isolated from external switching transients. It is therefore recommended that pin 22 be decoupled with a 4.7 μF tantalum capacitor in parallel with a 0.1 μF ceramic disc capacitor.

The V− supply (pin 20) provides negative bias for the FET comparator. Although pin 20 may be grounded in some applications, it must be at least 2V more negative than the most negative analog input signal. When a negative supply is used, pin 20 should also be bypassed with 4.7 μF in parallel with 0.1 μF.

Grounding and circuit layout are extremely important in preserving 12-bit accuracy. The user is advised to employ separate digital and analog returns, and to make these PC board traces as "heavy" as practical.

2.2 Short Cycle for Improved Conversion Time (Figure 2)

The ADC1210, ADC1211 counting sequence may be truncated to decrease conversion time. For example, when using the ADC1211, 2 clock intervals may be "saved" if 10-bit conversion accuracy is taking place. The Q2 output should be "OR'd" with CONVERSION COMPLETE ($\overline{CC}$) in order to ensure that the register does not lock-up upon power turn-on.



TL/H/5677–10

FIGURE 2. Short Cycling the ADC1211 to Improve 10-Bit Conversion Time (Continuous Conversion)

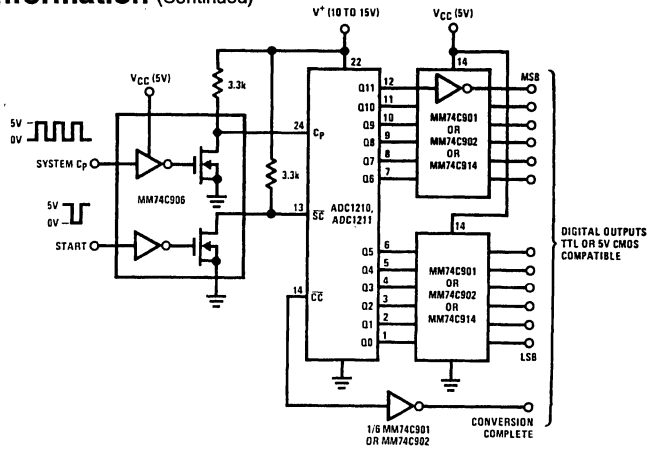
2.3 Logic Compatibility

The ADC1210, ADC1211 is intended to interface with CMOS logic levels: i.e., the logic inputs and outputs are directly compatible with series 54C/74C and CD4000 family of logic components. The outputs of the ADC1210, ADC1211 will not drive LPTTL, TTL or PMOS logic directly without degrading accuracy. Various recommended interface techniques are shown in *Figures 3 and 4*.

2.4 Operating Configurations

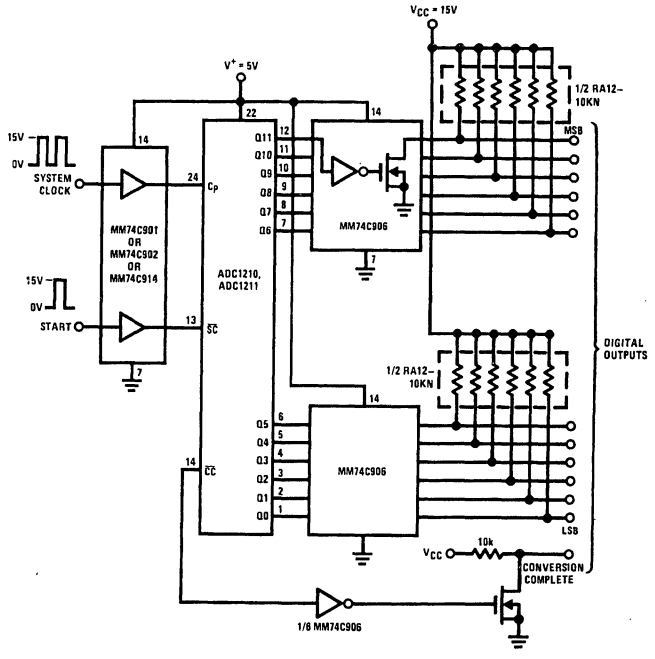
Several recommended operating configurations are shown in *Figure 5*.

Applications Information (Continued)



TL/H/5677–11

FIGURE 3. Interfacing an ADC1210, ADC1211 Running on $V^+ > V_{CC}$. Example: $V^+ = 10.24V$, System $V_{CC} = 5V$



TL/H/5677–12

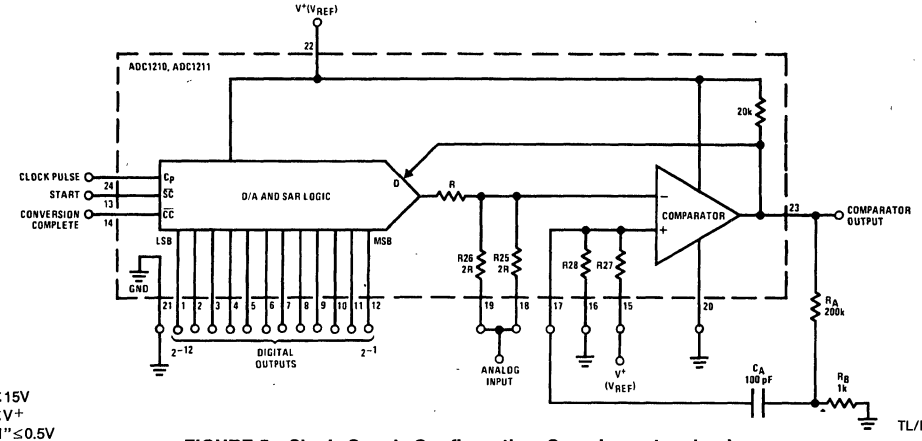
FIGURE 4. Interfacing an ADC1210, ADC1211 Running on $V^+ < V_{CC}$. Example: $V^+ = 5V$, $V_{CC} = 15V$

2.5 Offset and Full Scale Adjust

A variety of techniques may be employed to adjust Offset and Full Scale on the ADC1210, ADC1211. A straight-forward Full Scale Adjust is to incrementally vary V^+ (V_{REF}) to match the analog input voltage. A recommended technique is shown in *Figure 6*. An LM199 and low drift op amp(e.g., the LH0044) are used to provide the precision reference. The ADC1210, ADC1211 is put in the continuous convert mode by shorting pins 13 and 14. An analog voltage equal to V_{REF} minus 1½ LSB (10.23625V) is applied to pins 18 and 19, and R1 is adjusted until the LSB flickers equally between logic "1" and logic "0" (all other outputs must be stable logic "0"). Offset Null is accomplished by then applying an analog input voltage equal to ½ LSB at pins 18 and 19. R2 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other bits are stable). In the circuit of *Figure 6*, the ADC1210, ADC1211 is configured for Complementary Binary logic and the values shown are for $V^+ = 10.240V$, $V_{FS} = 10.2375V$, LSB = 2.5 mV.

An alternate technique is shown in *Figure 7*. In this instance, an LH0071 is used to provide the reference voltage. An analog input voltage equal to V_{REF} minus 1½ LSB (10.23625V) is applied to pins 18 and 19.

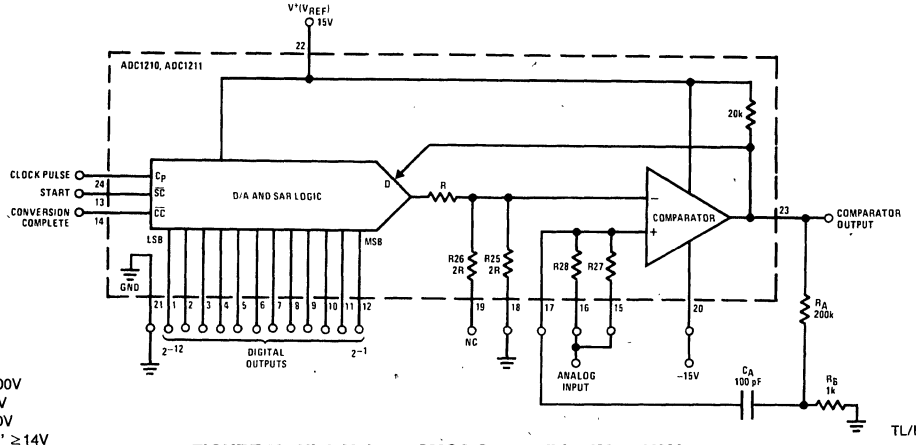
Applications Information (Continued)



TL/H/5677–13

$5V \leq V^+ \leq 15V$
$0V \leq V_{IN} \leq V^+$
Logical "1" $\leq 0.5V$
Logical "0" $\cong V^+$

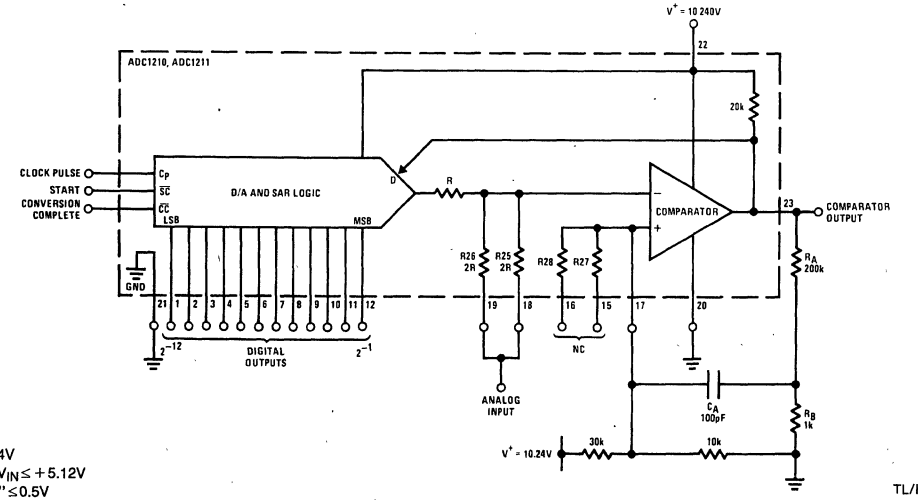
FIGURE 5a. Single Supply Configuration, Complementary Logic



TL/H/5677–14

$V^+ = 15.000V$
$V^- = -15V$
$0 \leq V_{IN} \leq 10V$
Logical "1" $\geq 14V$
Logical "0" $\leq 0.5V$

FIGURE 5b. High Voltage CMOS Compatible, 0V to 10V Input

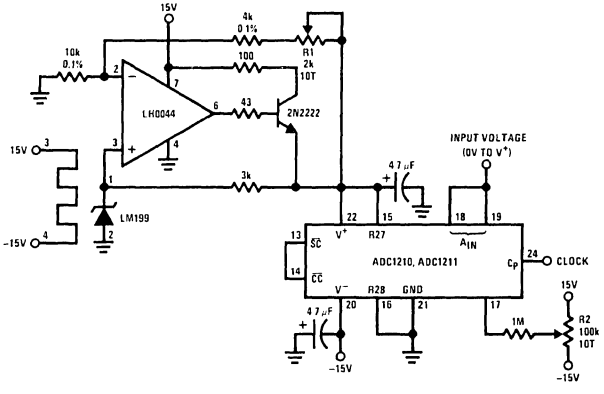


TL/H/5677–15

$V^+ = 10.24V$
$-5.12V \leq V_{IN} \leq +5.12V$
Logical "1" $\leq 0.5V$
Logical "0" $\cong 10V$

FIGURE 5c. Bipolar Input, Complementary Logic

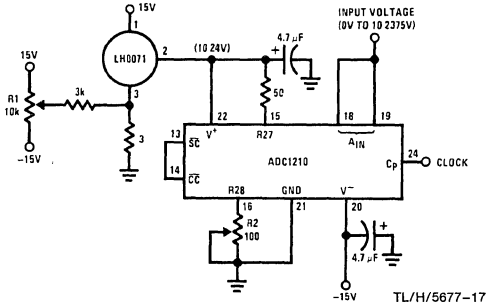
Applications Information (Continued)



TL/H/5677–16

FIGURE 6. Offset and Full Scale Adjustment for Complementary Binary

R1 is adjusted until the LSB output flickers equally between logic "1" and logic "0" (all other outputs must be a stable logic "0"). For Offset Null, an analog voltage equal to 1/2 LSB (1.25 mV) is then applied to pins 18 and 19, and R2, is adjusted until the LSB output flickers equally between logic "1" and "0".



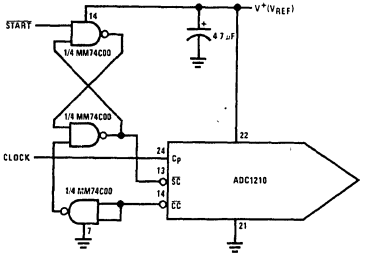
TL/H/5677–17

FIGURE 7. Offset and Full-Scale Adjustment Technique Using LH0071

In both techniques shown, adjusting the Full-Scale first and then Offset minimizes adjustment interaction. At least one iteration is recommended as a self-check.

2.6 START PULSE CONSIDERATIONS

To assure reliable conversion accuracy, the $\overline{\text{START}}$ ($\overline{\text{SC}}$) pulse applied to pin 13 of the ADC1210 should be synchronized to the conversion clock. One simple way to do that is the circuit shown in *Figure 8*. Note that once a conversion cycle is initiated, the $\overline{\text{START}}$ signal cannot effect the conversion operation until it is completed.



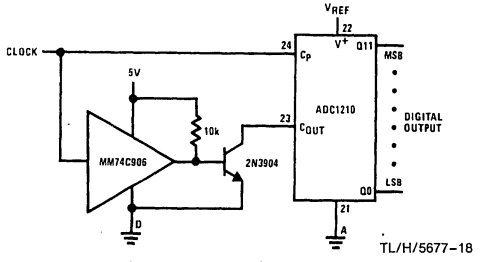
TL/H/5677–19

FIGURE 8. Synchronizing the $\overline{\text{START}}$ Pulse

The circuit insures that in no case can the ADC1210 make an error in the Most Significant Bit (MSB) decision. Without the circuit, it is possible for energy from the trailing edge of an asynchronous $\overline{\text{START}}$ pulse to be coupled into the ADC1210's comparator. If the analog input is near half-scale, the charge injected can force an error in the MSB decision. The circuit allows one clock period for this energy to dissipate before the decision is recorded.

2.7 ADC1210 CONVERSION AT 26 µs

The ADC1210 can run at 500 kHz clock frequency, or 12-bit conversion time of 26 µs (*Figure 9*). The comparator output is clamped low until the successive approximation register (SAR) is ready to strobe in the data at the rising edge of the conversion clock. Comparator oscillation is suppressed and kept from influencing the conversion decisions, eliminating the need for the AC hysteresis circuit above clock frequency of 65 kHz that is recommended.



TL/H/5677–18

FIGURE 9. Conversion at 26 µs

A complementary phased clock is required. The positive phase is used to clock the converter SAR as is normally the case. The same signal is buffered and inverted by the transistor. The open collector is wire-ORed to the output of the comparator. During the first half of the clock cycle (50% duty cycle), the comparator output is clamped and disabled, though its internal operation is still in normal working order. The last half cycle of the clock unclamps the comparator output. Thus, the output is permitted to slew to the final logic state just before the decision is logged into the SAR. The MM74C906 buffer (or with two inverting buffers) provides adequate propogation delay such that the comparator output data is held long enough to resolve any internal logic setup time requirements.

S 5

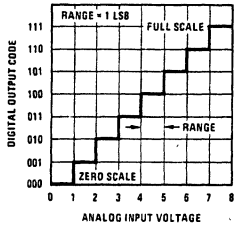
Applications Information (Continued)

The 500 kHz clock implies that the absolute minimum amount of time for the comparator output is *unclamped* is 1 μs. Therefore, if the clock is not 50% duty cycle, this 1 μs requirement must be observed.

3.0 DEFINITION OF TERMS

Resolution: The Resolution of an A/D is an expression of the smallest change in input which will increment (or decrement) the output from one code to the next adjacent code. It is defined in number of bits, or 1 part in 2^n. The ADC1210 and ADC1211 have a resolution of 12 bits or 1 part in 4,096 (0.0244%).

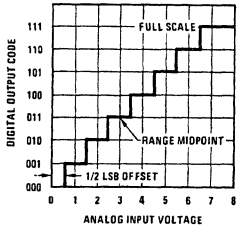
Quantization Uncertainty: Quantization Uncertainty is a direct consequence of the resolution of the converter. All analog voltages within a given range are represented by a single digital output code. There is, therefore, an inherent conversion error even for a perfect A/D. As an example, the transfer characteristic of a perfect 3-bit A/D is shown in *Figure 10*.



TL/H/5677–21

FIGURE 10. Quantization Uncertainty of a Perfect 3-Bit A/D

As can be seen, all input voltages between 0V and 1V are represented by an output code of 000. All input voltages between 1V and 2V are represented by an output code of 001, etc. If the midpoint of the range is assumed to be the nominal value (e.g., 0.5V), there is an Uncertainty of ±1/2 LSB. It is common practice to offset the converter 1/2 LSB in order to reduce the Uncertainty to ±1/2 LSB is shown in *Figure 11*, rather than +1, −0 shown in *Figure 10*. Quantization Uncertainty can only be reduced by increasing Resolution. It is expressed as ±1/2 LSB or as an error percentage of full scale (±0.0122% FS for the ADC1210).

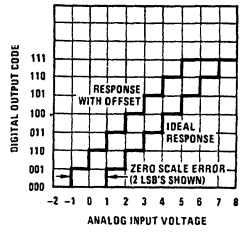


TL/H/5677–22

FIGURE 11. Transfer Characteristic Offset 1/2 LSB to Minimize Quantizing Uncertainty

Linearity Error: Linearity Error is the maximum deviation from a straight line passing through the end points of the A/D transfer characteristic. It is measured after calibrating Zero and Full Scale Error. Linearity is a performance characteristic intrinsic to the device and cannot be externally adjusted.

Zero Scale Error (or Offset): Zero Scale Error is a measure of the difference between the output of an ideal and the actual A/D for zero input voltage. As shown in *Figure 12*, the effect of Zero Scale Error is to shift the transfer characteristic to the right or left along the abscissa. Any voltage more negative than the LSB transition gives an output code of 000. In practice, therefore, the voltage at which the 000 to 001 transition takes place is ascertained, this input voltage's departure from the ideal value is defined as the Zero Scale Error (Offset) and is expressed as a percentage of FS. In the example of *Figure 12*, the offset is 2 LSB's or 0.286% of FS.

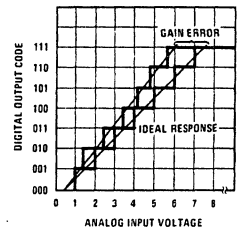


TL/H/5677–20

FIGURE 12. A/D Transfer Characteristic with Offset

The Zero Scale Error of the ADC1210, ADC1211 is caused primarily by offset voltage in the comparator. Because it is common practice to offset the A/D 1/2 LSB to minimize Quantization Error, the offsetting techniques described in the Applications Section may be used to null Zero Scale Error and accomplish the 1/2 LSB offset at the same time.

Full Scale Error (or Gain Error): Full Scale Error is a measure of the difference between the output of an ideal A/D converter and the actual A/D for an input voltage equal to full scale. As shown in *Figure 13*, the Full Scale Error effect is to rotate the transfer characteristic angularly about the origin. Any voltage more positive than the Full Scale transition gives an output code of 111. In practice, therefore, the voltage at which the transition from 111 to 110 occurs is ascertained. The input voltage's departure from the ideal value is defined as Full Scale Error and is expressed as a percentage of FS. In the example of *Figure 13*, Full Scale Error is 1 1/2 LSB's or 0.214% of FS.



TL/H/5677–23

FIGURE 13. Full Scale (Gain Error)

Full Scale Error of the ADC1210, ADC1211 is due primarily to mismatch in the R-2R ladder equivalent output impedance and input resistors R25, R26, R27, and R28. The gain error may be adjusted to zero as outlined in section 2.5.

Applications Information (Continued)

Monotonicity and Missing Codes: Monotonicity is a property of a D/A which requires an increasing or constant output voltage for an increasing digital input code. Monotonicity of a D/A converter does not, in itself, guarantee that an A/D built with that D/A will not have missing codes. However, the ADC1210 and ADC1211 are guaranteed to have no missing codes.

Conversion Time: The ADC1210, ADC1211 are successive approximation A/D converters requiring 13 clock intervals for a conversion to specified accuracy for the ADC1210 and 11 clocks for the ADC1211. There is a trade-off between accuracy and clock frequency due to settling time of the ladder and propagation delay through the comparator. By modifying the hysteresis network around the comparator, conversions with 10-bit accuracy can be made in 30 μs. Replace R_A, R_B and C_A in *Figure 5* with a 10 MΩ resistor between pin 23 (Comparator Output) and pin 17 (+ IN), and increase the clock rate to 366 kHz.

In order to prevent errors during conversion, the analog input voltage should not be allowed to change by more than $\pm$1/2 LSB. This places a maximum slew rate of 12.5 μV/μs on the analog input voltage. The usual solution to this restriction is to place a Sample and Hold in front of the A/D. For additional application information, refer to application note AN245.

National Semiconductor

DAC0830, DAC0831, DAC0832
8-Bit μP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DACs (MICRO-DAC™). For applications demanding higher resolution, the DAC1000 series (10-bits) and the DAC1208 and DAC1230 (12-bits) are available alternatives.

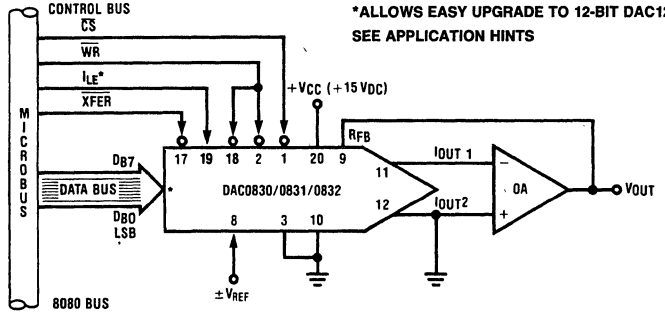
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates "STAND ALONE" (without μP) if desired

Key Specifications

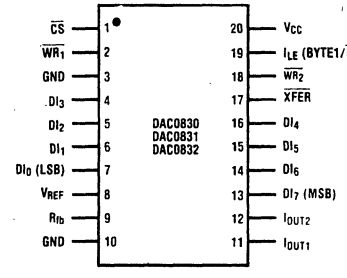
■ Current settling time	1μs
■ Resolution	8-bits
■ Linearity (guaranteed over temp.)	8, 9, or 10 bits
■ Gain Tempco	0.0002% FS/°C
■ Low power dissipation	20 mW
■ Single power supply	5 to 15 V_{DC}

Typical Application



*ALLOWS EASY UPGRADE TO 12-BIT DAC1230, SEE APPLICATION HINTS

Connection Diagram



See NS Packages D20A and N20A

Top View

†THIS IS NECESSARY FOR THE 12-BIT DAC1230 SERIES TO PERMIT INTERCHANGING FROM AN 8-BIT TO A 12-BIT DAC WITH **NO PC BOARD CHANGES AND NO SOFTWARE CHANGES,** SEE APPLICATIONS SECTION.

TL/H/5608–1

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
Lead Temp. (soldering, 10 seconds)	300°C

Operating Conditions

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
Part numbers with 'LCN' suffix	0°C to 70°C
Part numbers with 'LCD' suffix	−40°C to +85°C
Part numbers with 'LD' suffix	−55°C to +125°C
Voltage at Any Digital Input	V_{CC} TO GND

Electrical Characteristics

V_{REF} = 10.000 V_{DC} unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits T_A = 25°C.

Parameter	Conditions	See Note	V_{CC} = 12 V_{DC} ±5% to 15 V_{DC} ±5%			V_{CC} = 5 V_{DC} ±5%			Limit Units
			Typ. (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	Typ. (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
Converter Characteristics									
Resolution			8	8		8	8		bits
Linearity Error Max.	Zero and full scale adjusted −10V ≤ V_{REF} ≤ +10V	4, 7 8							
DAC0830LD & LCD				**0.05**			**0.05**		% FSR
DAC0832LD & LCD				**0.2**			**0.2**		% FSR
DAC0830LCN				0.05	**0.05**		0.05	**0.05**	% FSR
DAC0831LCN				0.1	**0.1**		0.1	**0.1**	% FSR
DAC0832LCN				0.2	**0.2**		0.2	**0.2**	% FSR
Differential Nonlinearity Max.	Zero and full scale adjusted −10V ≤ V_{REF} ≤ +10V	4, 7 8							
DAC0830LD & LCD				**0.1**			**0.1**		% FSR
DAC0832LD & LCD				**0.4**			**0.4**		% FSR
DAC0830LCN				0.1	**0.1**		0.1	**0.1**	% FSR
DAC0831LCN				0.2	**0.2**		0.2	**0.2**	% FSR
DAC0832LCN				0.4	**0.4**		0.4	**0.4**	% FSR
Monotonicity	−10V ≤ V_{REF} ≤ +10V LD & LCD LCN	4, 7		**8** 8	 **8**		**8** 8	 **8**	bits bits
Gain Error Max.	Using Internal R_{fb} −10V ≤ V_{REF} ≤ +10V	7	±0.2	±1		±0.2	±1		% FS
Gain Error Tempco Max.	Using internal R_{fb}		**0.0002**		**0.0006**	**0.0002**		**0.0006**	% FS/°C
Power Supply Rejection	All digital inputs latched high V_{CC} = 14.5V to 15.5V 11.5V to 12.5V 4.5V to 5.5V		 0.0002 0.0006			 0.0130			% FSR/V
Reference Input Max.			15	20		15	20		kΩ
Reference Input Min.			15	10		15	10		kΩ
Output Feedthrough Error	V_{REF} = 20 Vp-p, f = 100 kHz All data inputs latched low	9	3			3			mVp-p
Output Leakage Current Max. I_{OUT1}	All data inputs latched low LD & LCD LCN	10		**100** 50	 **100**		**100** 50	 **100**	nA
Output Leakage Current Max. I_{OUT2}	All data inputs latched high LD & LCD LCN			**100** 50	 **100**		**100** 50	 **100**	nA
Output Capacitance I_{OUT1} I_{OUT2}	All data inputs latched low		45 115			45 115			pF
Output Capacitance I_{OUT1} I_{OUT2}	All data inputs latched high		130 30			130 30			pF

Electrical Characteristics $V_{REF}=10.000\ V_{DC}$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A=25°C$. (Continued)

Parameter		Conditions	See Note	$V_{CC}=12\ V_{DC}\pm5\%$ to $15\ V_{DC}\pm5\%$			$V_{CC}=5\ V_{DC}\pm5\%$			Limit Units
				Typ. (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	Typ. (Note 12)	Tested Limit (Note 5)	Design Limit (Note 6)	
Digital and DC Characteristics										
Digital Input Voltages	Max.	Logic Low LD			**0.8**			**0.6**		V_{DC}
		LCD			**0.8**			**0.8**		
		LCN			1.0	**0.8**		1.0	**0.8**	
	Min.	Logic High LD & LCD			**2.0**			**2.0**		V_{DC}
		LCN			1.9	**2.0**		1.9	**2.0**	
Digital input Currents	Max.	Digital inputs <0.8V LD & LCD		−50	**−200**		−50	**−200**		μA_{DC}
		LCN			−160	**−200**		−160	**−200**	
		Digital inputs>2.0V LD & LCD		0.1	**+10**		0.1	**+10**		μA_{DC}
		LCN			+8	**+10**		+8	**+10**	
Supply Current Drain	Max.	LD & LCD		1.2	**2.0**		1.2	**2.0**		mA
		LCN			1.7	**2.0**		1.7	**2.0**	

Symbol	Parameter	Conditions	See Note	$V_{CC}=12\ V_{DC}\pm5\%$ to $15\ V_{DC}\pm5\%$			$V_{CC}=5\ V_{DC}\pm5\%$			Limit Units
				Typ.	Tested Limit (Note 5)	Design Limit (Note 6)	Typ.	Tested Limit (Note 5)	Design Limit (Note 6)	
AC Characteristics										
t_S	Current Setting Time	$V_{IL}=0V, V_{IH}=5V$		1.0			1.0			μs
t_W	Write and XFER Pulse Width Min.	$V_{IL}=0V, V_{IH}=5V$	11	100		320	375		600	ns
				180		**320**	**500**		**900**	
t_{DS}	Data Setup Time Min.	$V_{IL}=0V, V_{IH}=5V$		100		320	375		600	
				180		**320**	**500**		**900**	
t_{DH}	Data Hold Time Min.	$V_{IL}=0V, V_{IH}=5V$		**10**		**50**	**10**		**50**	
t_{CS}	Control Setup Time Min.	$V_{IL}=0V, V_{IH}=5V$		110		320	400		650	
				200		**320**	**500**		**900**	
t_{CH}	Control Hold Time Min.	$V_{IL}=0V, V_{IH}=5V$				**10**			**10**	

Note 1: "*Absolute Maximum Ratings*" are those values beyond which the safety of the device cannot be guaranteed. These specifications are not meant to imply that the devices should be operated at these "*Absolute Maximum*" limits.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: Max. T_J for the D suffix package is 150°C with $\theta_{JA}=80°C/W$. Max. T_J for the N suffix package is 125°C with $\theta_{JA}=120°C/W$.

Note 4: For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if $V_{REF}=10V$ then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 7: Guaranteed at $V_{REF}=\pm10\ V_{DC}$ and $V_{REF}=\pm1\ V_{DC}$.

Note 8: The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC0830 is "0.05% of FSR (MAX)". This guarantees that after performing a zero and full scale adjustment (see Sections 2.5 and 2.6), the plot of the 256 analog voltage outputs will each be within $0.05\% \times V_{REF}$ of a straight line which passes through zero and full scale.

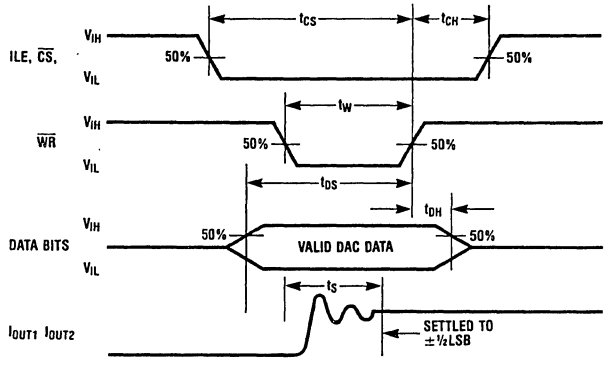
Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating, the feedthrough is typically 6mV.

Note 10: A 100nA leakage current with $R_{fb}=20k$ and $V_{REF}=10V$ corresponds to a zero error of $(100\times10^{-9}\times20\times10^{3})\times100/10$ which is 0.02% of FS.

Note 11: The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Note 12: Typicals are at 25°C and represent most likely parametric norm.

Switching Waveform



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Definition of Package Pinouts

Control Signals (All control signals level actuated)

$\overline{CS}$: **Chip Select** (active low). The $\overline{CS}$ in combination with ILE will enable $\overline{WR_1}$.

ILE: **Input Latch Enable** (active high). The ILE in combination with $\overline{CS}$ enables $\overline{WR_1}$.

$\overline{WR_1}$: **Write 1.** The active low $\overline{WR_1}$ is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR_1}$ is high. To update the input latch—$\overline{CS}$ and $\overline{WR_1}$ must be low while ILE is high.

$\overline{WR_2}$: **Write 2** (active low). This signal, in combination with $\overline{XFER}$, causes the 8-bit data which is available in the input latch to transfer to the DAC register.

$\overline{XFER}$: **Transfer control signal** (active low). The $\overline{XFER}$ will enable $\overline{WR_2}$.

Other Pin Functions

DI_0-DI_7: **Digital Inputs.** DI_0 is the least significant bit (LSB) and DI_7 is the most significant bit (MSB).

I_{OUT1}: **DAC Current Output 1.** I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in DAC register.

I_{OUT2}: **DAC Current Output 2.** I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} =$ constant (I full scale for a fixed reference voltage).

R_{fb}: **Feedback Resistor.** The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: **Reference Voltage Input.** This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of +10 to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: **Digital Supply Voltage.** This is the power supply pin for the part. V_{CC} can be from +5 to $+15V_{DC}$. Operation is optimum for $+15V_{DC}$.

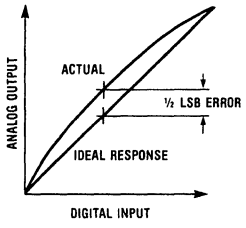
GND: The pin 10 voltage must be at the same ground potential as I_{OUT1} and I_{OUT2} for current switching applications. Any difference of potential (V_{OS} pin 10) will result in a linearity change of

$$\frac{V_{OS} \text{ pin } 10}{3V_{REF}}$$

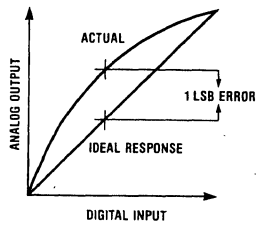
For example, if V_{REF} = 10V and pin 10 is 9mV offset from I_{OUT1} and I_{OUT2} the linearity change will be 0.03%.

Pin 3 can be offset ±100mV with no linearity change, but the logic input threshold will shift.

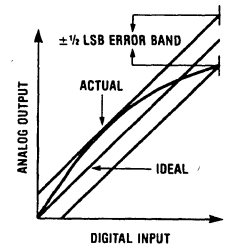
Linearity Error



a) End point test after zero and fs adj.



b) Best straight line



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c) Shifting fs adj. to pass best straight line test

Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC0830 has 2^8 or 256 steps and therefore has 8-bit resolution.

Linearity Error: Linearity Error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity "end point test" (a) and the "best straight line" test (b,c) used by other suppliers are illustrated above. The "end point test" greatly simplifies the adjustment procedure by eliminating the need for multiple iterations of checking the linearity and then adjusting full scale until the linearity is met. The "end point test" guarantees that linearity is met after a single full scale adjust. (One adjustment vs. multiple iterations of the adjustment.) The "end point test" uses a standard zero and F.S. adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within ±½LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full-Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC0830 series, full-scale is $V_{REF} - 1LSB$. For $V_{REF} = 10V$ and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 39mV = 9.961V$. Full-scale error is adjustable to zero.

Differential Nonlinearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential nonlinearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. An 8-bit DAC which is monotonic to 8 bits simply means that increasing digital input codes will produce an increasing analog output.

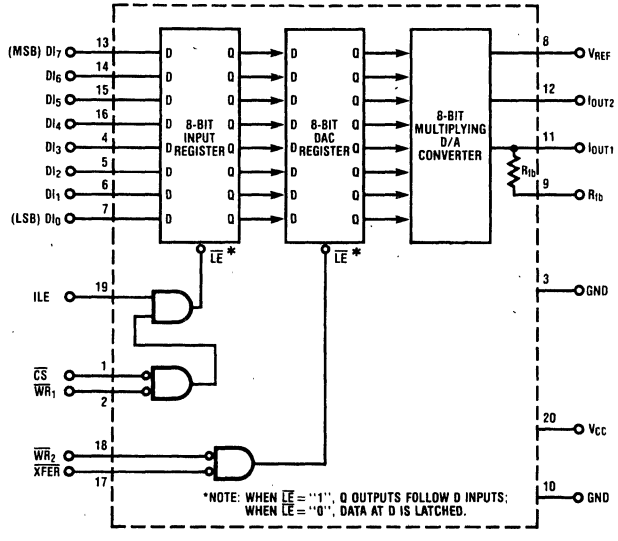

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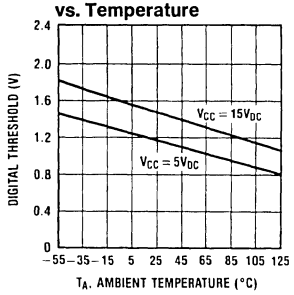
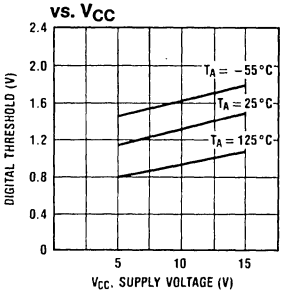
FIGURE 1. DAC0830 Functional Diagram

Typical Performance Characteristics

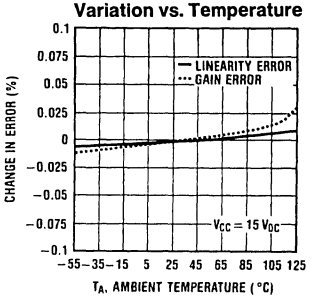
Digital Input Threshold vs. Temperature



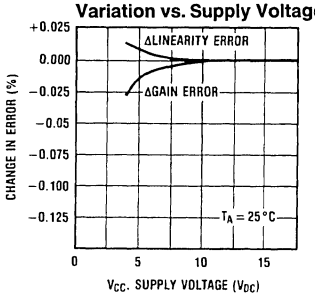
Digital Input Threshold vs. V_{CC}



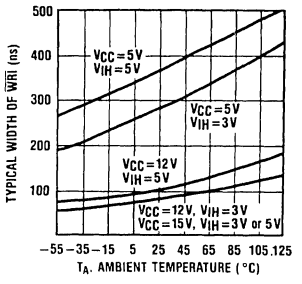
Gain and Linearity Error Variation vs. Temperature



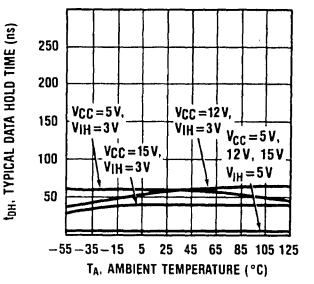
Gain and Linearity Error Variation vs. Supply Voltage



Write Pulse Width



Data Hold Time



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DAC0830 Series Application Hints

These DAC's are the industry's first *microprocessor* compatible, double-buffered 8-bit multiplying D to A converters. Double-buffering allows the utmost application flexibility from a digital control point of view. This 20-pin device is also pin for pin compatible (with one exception) with the DAC1230, a 12-bit MICRO-DAC. In the event that a system's analog output resolution and accuracy must be upgraded, substituting the DAC1230 can be easily accomplished. By tying address bit A_0 to the ILE pin, a two-byte μP write instruction (double precision) which automatically increments the address for the second byte write (starting with A_0 = "1") can be used. This allows either an 8-bit or the 12-bit part to be used with no hardware or software changes. For the simplest 8-bit application, this pin should be tied to V_{CC} (also see other uses in section 1.1).

Analog signal control versatility is provided by a precision R-2R ladder network which allows full 4-quadrant multiplication of a wide range bipolar reference voltage by an applied digital word.

1.0 DIGITAL CONSIDERATIONS

A most unique characteristic of these DAC's is that the 8-bit digital input byte is double-buffered. This means that the data must transfer through two independently controlled 8-bit latching registers before being applied to the R-2R ladder network to change the analog output. The addition of a second register allows two useful control features. First, any DAC in a system can simultaneously hold the current DAC data in one register (DAC register) and the next data word in the second register (input register) to allow fast updating of the DAC output on demand. Second, and probably more important, double-buffering allows any number of DAC's in a system to be updated to their new analog output levels simultaneously via a common strobe signal.

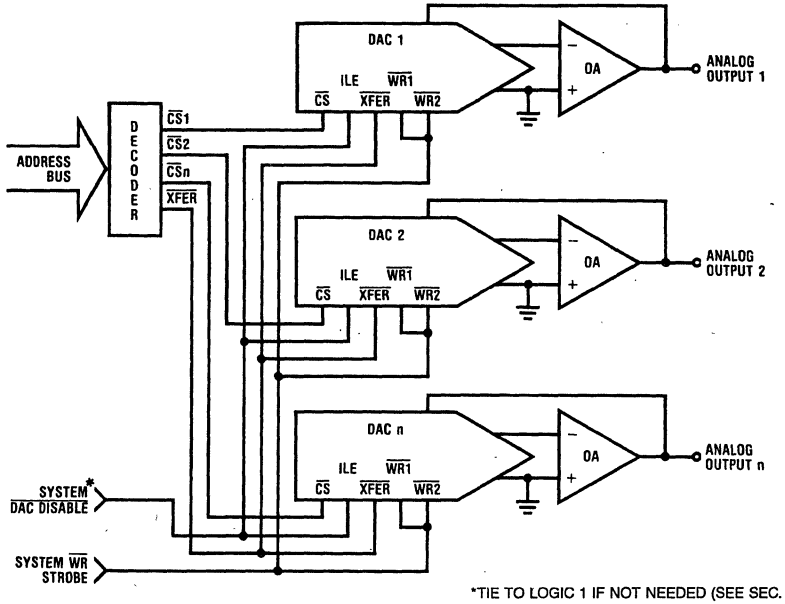
The timing requirements and logic level convention of the register control signals have been designed to minimize or eliminate external interfacing logic when applied to most popular microprocessors and development systems. It is easy to think of these converters as 8-bit "write-only" memory locations that provide an analog output quantity. All inputs to these DAC's meet TTL voltage level specs and can also be driven directly with high voltage CMOS logic in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. If any of the digital inputs are inadvertantly left floating, the DAC interprets the pin as a logic "1".

1.1 Double-Buffered Operation

Updating the analog output of these DAC's in a double-buffered manner is basically a two step or double write operation. In a microprocessor system two unique system addresses must be decoded, one for the input latch controlled by the $\overline{CS}$ pin and a second for the DAC latch which is controlled by the $\overline{XFER}$ line. If more than one DAC is being driven, *Figure 2*, the $\overline{CS}$ line of each DAC would typically be decoded individually, but all of the converters could share a common $\overline{XFER}$ address to allow simultaneous updating of any number of DAC's. The timing for this operation is shown, *Figure 3*.

It is important to note that the analog outputs that will change after a simultaneous transfer are those from the DAC's whose input register had been modified prior to the $\overline{XFER}$ command.

DAC0830 Series Application Hints (Continued)



*TIE TO LOGIC 1 IF NOT NEEDED (SEE SEC. 1.1).

FIGURE 2. Controlling Mutiple DACs

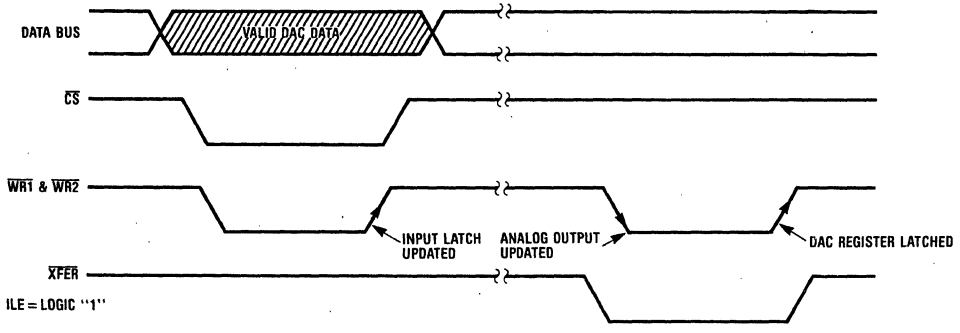


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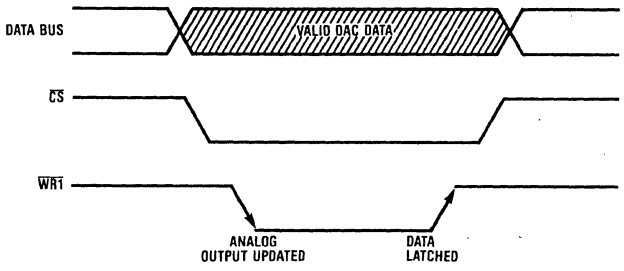
FIGURE 3

The ILE pin is an active high chip select which can be decoded from the address bus as a qualifier for the normal $\overline{CS}$ signal generated during a write operation. This can be used to provide a higher degree of decoding unique control signals for a particular DAC, and thereby create a more efficient addressing scheme.

Another useful application of the ILE pin of each DAC in a multiple DAC system is to tie these inputs together and use this as a control line that can effectively "freeze" the outputs of all the DAC's at their present value. Pulling this line low latches the input register and prevents new data from being written to the DAC. This can be particularly useful in multiprocessing systems to allow a processor other than the one controlling the DAC's to take over control of the data bus and control lines. If this second system were to use the same addresses as those decoded for DAC control (but for a different purpose) the ILE function would prevent the DAC's from being erroneously altered.

In a "Stand-Alone" system the control signals are generated by discrete logic. In this case double-buffering can be controlled by simply taking $\overline{CS}$ and $\overline{XFER}$ to a logic "0", ILE to a logic "1" and pulling $\overline{WR_1}$ low to load data to the input latch. Pulling $\overline{WR_2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.

DAC0830 Series Application Hints (Continued)



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ILE = LOGIC "1"; $\overline{WR2}$ and $\overline{XFER}$ GROUNDED

FIGURE 4

1.2 Single-Buffered Operation

In a microprocessor controlled system where maximum data throughout to the DAC is of primary concern, or when only one DAC of several needs to be updated at a time, a single-buffered configuration can be used. One of the two internal registers allows the data to flow through and the other register will serve as the data latch.

Digital signal feedthrough (see Section 1.5) is minimized if the input register is used as the data latch. Timing for this mode is shown in *Figure 4*.

Single-buffering in a "stand-alone" system is achieved by strobing $\overline{WR_1}$ low to update the DAC with $\overline{CS}$, $\overline{WR_2}$ and $\overline{XFER}$ grounded and ILE tied high.

1.3 Flow-Through Operation

Though primarily designed to provide microprocessor interface compatibility, the MICRO-DAC's can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary up-down counter, or in function generation circuits where a ROM is continuously providing DAC data.

Simply grounding $\overline{CS}$, $\overline{WR_1}$, $\overline{WR_2}$, and $\overline{XFER}$ and tying ILE high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

1.4 Control Signal Timing

When interfacing these MICRO-DAC to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 900 ns for all valid operating conditions of supply voltage and ambient temperature, but typically a pulse width of only 180ns is adequate if $V_{CC} = 15V_{DC}$. A second consideration is that the guaranteed minimum data hold time of 50ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulsewidth. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in *Figure 5* for an exemplary system which provides a 250ns $\overline{WR}$ strobe time with a data hold time of less than 10ns.

The proper data set-up time prior to the latching edge (LO to HI transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulsewidth is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

1.5 Digital Signal Feedthrough

When data is latched in the internal registers, but the digital inputs are changing state, a narrow spike of current may flow out of the current output terminals. This spike is caused by the rapid switching of internal logic gates that are responding to the input changes.

There are several recommendations to minimize this effect. When latching data in the DAC, always use the input register as the latch. Second, reducing the V_{CC} supply for the DAC from +15V to +5V offers a factor of 5 improvement in the magnitude of the feedthrough, but at the expense of internal logic switching speed. Finally, increasing C_C (*Figure 8*) to a value consistent with the actual circuit bandwidth requirements can provide a substantial damping effect on any output spikes.

DAC0830 Series Application Hints (Continued)

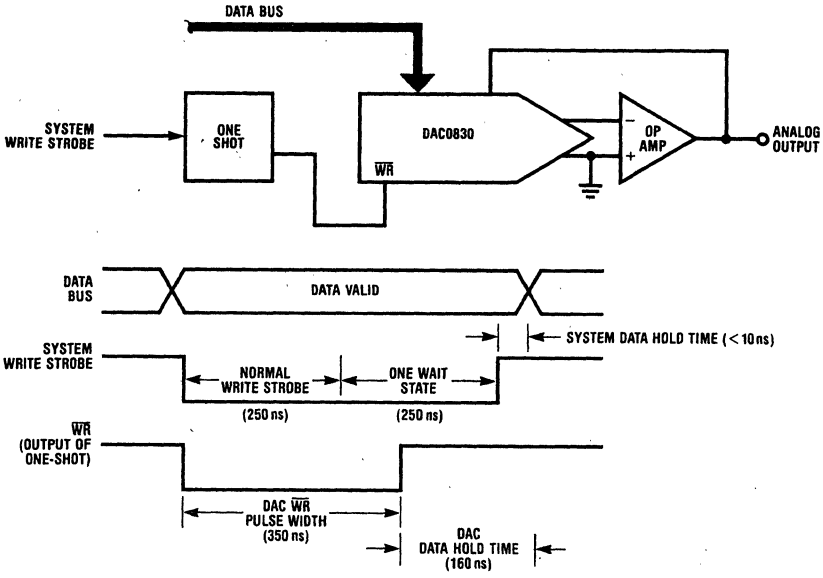

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FIGURE 5. Accommodating a High Speed System

2.0 ANALOG CONSIDERATIONS

The fundamental purpose of any D to A converter is to provide an accurate analog output quantity which is representative of the applied digital word. In the case of the DAC0830, the output, I_{OUT1}, is a current directly proportional to the product of the applied reference voltage and the digital input word. For application versatility, a second output, I_{OUT2}, is provided as a current directly proportional to the complement of the digital input. Basically:

$$I_{OUT1} = \frac{V_{REF}}{15\ k\Omega} \times \frac{\text{Digital Input}}{256};$$

$$I_{OUT2} = \frac{V_{REF}}{15\ k\Omega} \times \frac{255 - \text{Digital Input}}{256}$$

where the digital input is the decimal (base 10) equivalent of the applied 8-bit binary word (0 to 255), V_{REF} is the voltage at pin 8 and 15 kΩ is the nominal value of the internal resistance, R, of the R-2R ladder network (discussed in Section 2.1).

Several factors external to the DAC itself must be considered to maintain analog accuracy and are covered in subsequent sections.

2.1 The Current Switching R-2R Ladder

The analog circuitry, *Figure 6*, consists of a silicon-chromium (SiCr or Si-chrome) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there are no parasitic diode problems with the ladder (as there may be with diffused resistors) so the reference voltage, V_{REF}, can range −10V to +10V even if V_{CC} for the device is $5V_{DC}$.

The digital input code to the DAC simply controls the position of the SPDT current switches and steers the available ladder current to either I_{OUT1} or I_{OUT2} as determined by the logic input level ("1" or "0") respectively, as shown in *Figure 6*. The MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

2.2 Basic Unipolar Output Voltage

To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential ($0V_{DC}$) as possible. With $V_{REF} = +10V$ every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in *Figure 7*.

The inverting input of the op amp is a "virtual ground" created by the feedback from its output through the internal 15 kΩ resistor, R_{fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than or equal to the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

DAC0830 Series Application Hints (Continued)

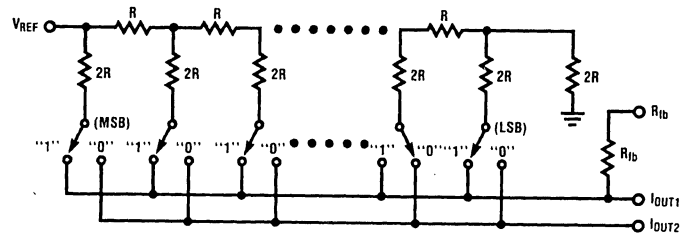

FIGURE 6

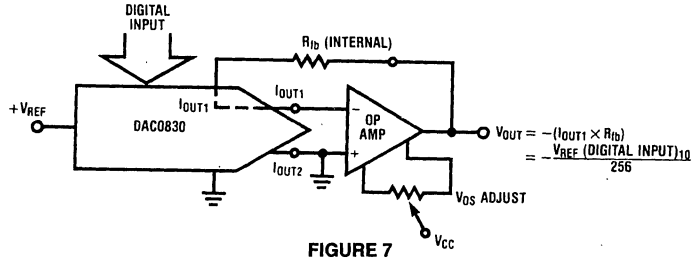

FIGURE 7

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2.3 Op Amp Considerations

The op amp used in *Figure 7* should have offset voltage nulling capability (See Section 2.5).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET op amps are highly recommended for use with these DACs because of their very low input current.

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in *Figure 8*, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

Finally, the output voltage swing of the amplifier must be greater than V_{REF} to allow reaching the full scale output voltage. Depending on the loading on the output of the amplifier and the available op amp supply voltages (only ±12 volts in many development systems), a reference voltage less than 10 volts may be necessary to obtain the full analog output voltage range.

2.4 Bipolar Output Voltage with a Fixed Reference

The addition of a second op amp to the previous circuitry can be used to generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word and allows two-quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication: $\pm V_{REF} \times \pm$ Digital Code $= \mp V_{OUT}$. This circuit is shown in *Figure 9*.

This configuration features several improvements over existing circuits for bipolar outputs with other multiplying DACs. Only the offset voltage of amplifier 1 has to be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp (although a constant output voltage error) has no effect on linearity. It should be nulled only if absolute output accuracy is required. Finally, the values of the resistors around the second amplifier do not have to match the internal DAC resistors, they need only to match and temperature track each other. A thin film 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. These resistors are matched to 0.1% and exhibit only 5 ppm/°C resistance tracking tempco. Two of the four available 10 kΩ resistors can be paralleled to form R in *Figure 9* and the other two can be used independently as the resistances labeled 2R.

2.5 Zero Adjustment

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near $0V_{DC}$ as possible. This is accomplished for the typical DAC — op amp connection (*Figure 7*) by shorting out R_{fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all one's for I_{OUT2}). The short around R_{fb} is then removed and the converter is zero adjusted.

S 5

DAC0830 Series Application Hints (Continued)

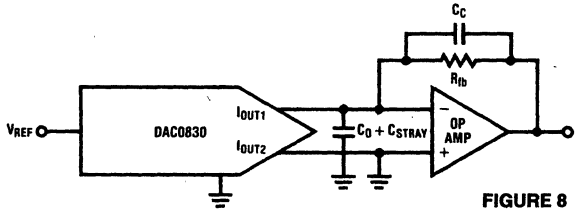
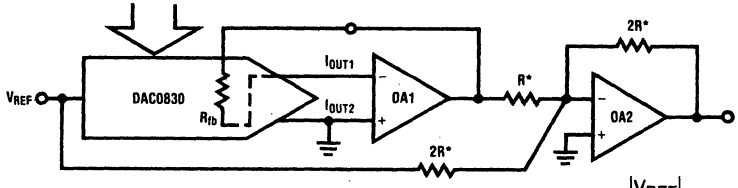


FIGURE 8

OP Amp	C_C	t_s (0 to Full Scale)
LF356	22 pF	4 μs
LF351	22 pF	5 μs
LF357*	10 pF	2 μs

*2.4 kΩ RESISTOR ADDED FROM −INPUT TO GROUND TO INSURE STABILITY



$$V_{OUT} = V_{REF} \frac{(\text{DIGITAL CODE} - 128)}{128}$$

$$1\ \text{LSB} = \frac{|V_{REF}|}{128}$$

TL/H/5608–10

*THESE RESISTORS ARE AVAILABLE FROM BECKMAN INSTRUMENTS, INC. AS THEIR PART NO. 694-3-R10K-D

Input Code MSB ..... LSB	IDEAL V_{OUT} $+V_{REF}$	IDEAL V_{OUT} $-V_{REF}$
1 1 1 1 1 1 1 1	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
1 1 0 0 0 0 0 0	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1 0 0 0 0 0 0 0	0	0
0 1 1 1 1 1 1 1	-1 LSB	$+1$ LSB
0 0 1 1 1 1 1 1	$-\frac{\lvert V_{REF}\rvert}{2} - 1$ LSB	$\frac{\lvert V_{REF}\rvert}{2} + 1$ LSB
0 0 0 0 0 0 0 0	$-\lvert V_{REF}\rvert$	$+\lvert V_{REF}\rvert$

FIGURE 9

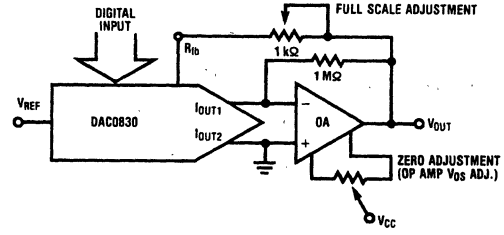
2.6 Full-Scale Adjustment

In the case where the matching of R_{fb} to the R value of the R-2R ladder (typically ±0.2%) is insufficient for full-scale accuracy in a particular application, the V_{REF} voltage can be adjusted or an external resistor and potentiometer can be added as shown in *Figure 10* to provide a full-scale adjustment.

The temperature coefficients of the resistors used for this adjustment are an important concern. To prevent degradation of the gain error tempco by the external resistors, their temperature coefficients ideally would have to match that of the internal DAC resistors, which is a highly impractical constraint. For the values shown in *Figure 10*, if the resistor and the potentiometer each had a temperature coefficient of ±100 ppm/°C maximum, the overall gain error tempco would be degraded a maximum of 0.0025%/°C for an adjustment pot setting of less than 3% of R_{fb}.

2.7 Using the DAC0830 in a Voltage Switching Configuration

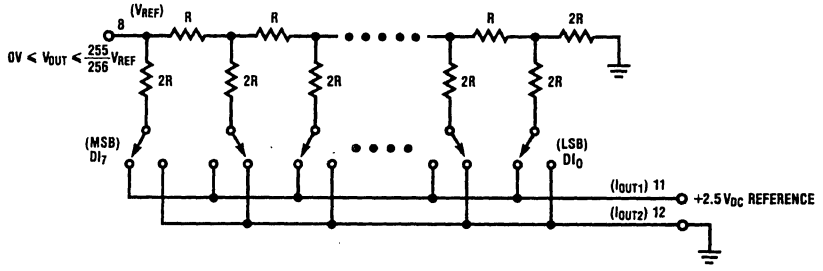
The R-2R ladder can also be operated as a voltage switching network. In this mode the ladder is used in an inverted manner from the standard current switching configuration. The reference voltage is connected to one of the current output terminals (I_{OUT1} for true binary digital control, I_{OUT2} is for complementary binary) and the output voltage is taken from the normal V_{REF} pin. The converter output is now a voltage in the range from 0V to 255/256 V_{REF} as a function of the applied digital code as shown in *Figure 11*.



TL/H/5608–11

FIGURE 10. Adding Full-Scale Adjustment

DAC0830 Series Application Hints (Continued)

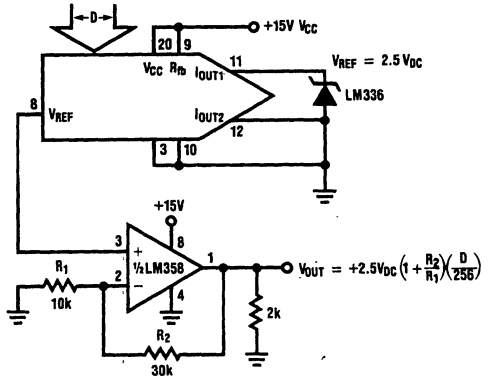


TL/H/5608–12

FIGURE 11. Voltage Mode Switching

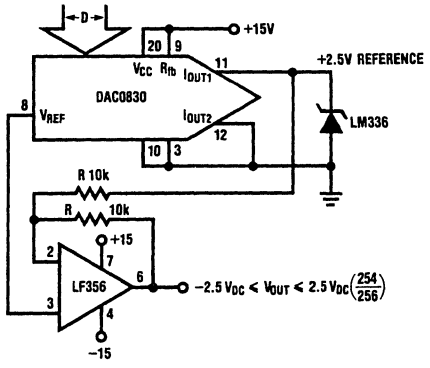
This configuration offers several useful application advantages. Since the output is a voltage, an external op amp is not necessarily required but the output impedance of the DAC is fairly high (equal to the specified reference input resistance of 10 kΩ to 20 kΩ) so an op amp may be used for buffering purposes. Some of the advantages of this mode are illustrated in *Figures 12, 13, 14* and *15*.

There are two important things to keep in mind when using this DAC in the voltage switching mode. The applied reference voltage must be positive since there are internal parasitic diodes from ground to the I_{OUT1} and I_{OUT2} terminals which would turn on if the applied reference went negative. There is also a dependence of conversion linearity and gain error on the voltage difference between V_{CC} and the voltage applied to the normal current output terminals. This is a result of the voltage drive requirements of the ladder switches. To ensure that all 8 switches turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) it is recommended that the applied reference voltage be kept less than $+5V_{DC}$ and V_{CC} be at least 9V more positive than V_{REF}. These restrictions ensure less than 0.1% linearity and gain error change. *Figures 16, 17* and *18* characterize the effects of bringing V_{REF} and V_{CC} closer together as well as typical temperature performance of this voltage switching configuration.



- Voltage switching mode eliminates output signal inversion and therefore a need for a negative power supply.
- Zero code output voltage is limited by the low level output saturation voltage of the op amp. The 2 kΩ pull-down resistor helps to reduce this voltage.
- V_{OS} of the op amp has no effect on DAC linearity.

FIGURE 12. Single Supply DAC



TL/H/5608–13

- $V_{OUT} = 2.5V \left(\frac{D}{128} - 1\right)$
- Slewing and settling time for a full scale output change is ≈ 1.8 μs

FIGURE 13. Obtaining a Bipolar Output from a Fixed Reference with a Single Op Amp

DAC0830 Series Application Hints (Continued)

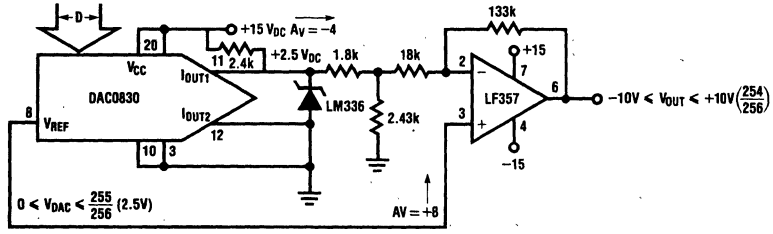
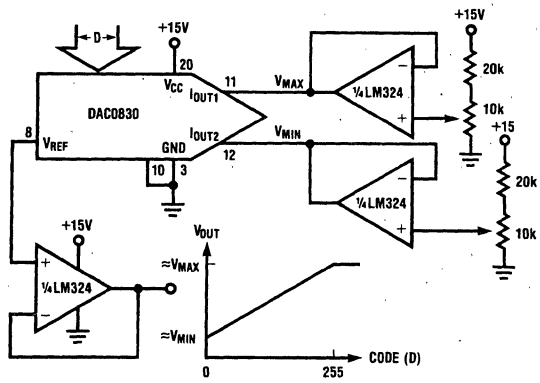


FIGURE 14. Bipolar Output with Increased Output Voltage Swing



TL/H/5608–14

- Only a single +15V supply required
- Non-interactive full-scale and zero code output adjustments
- V_{MAX} and V_{MIN} must be ≤ +5VDC and ≥0V.
- Incremental Output Step $= \frac{1}{256}(V_{MAX} - V_{MIN})$.
- $V_{OUT} = \frac{D}{256}(V_{MAX} - V_{MIN}) + \frac{255}{256}V_{MIN}$

FIGURE 15. Single Supply DAC with Level Shift and Span-Adjustable Output

Gain and Linearity Error Variation vs. Supply Voltage

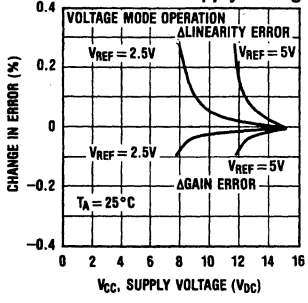


FIGURE 16

Gain and Linearity Error Variation vs. Reference Voltage

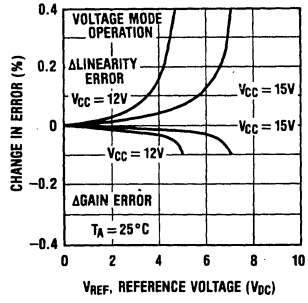
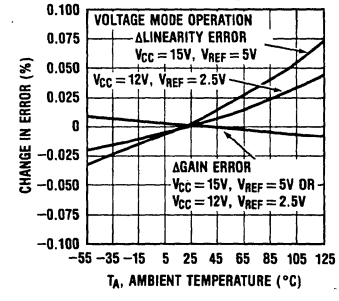


FIGURE 17

Note: For these curves, V_{REF} is the voltage applied to pin 11 (I_{OUT1}) with pin 12 (I_{OUT2}) grounded.

Gain and Linearity Error Variation vs. Temperature



TL/H/5608–15

FIGURE 18

DAC0830 Series Application Hints (Continued)

2.8 Miscellaneous Application Hints

These converters are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to static discharge.

Conversion accuracy is only as good as the applied reference voltage so providing a stable source over time and temperature changes is an important factor to consider.

A "good" ground is most desirable. A single point ground distribution technique for analog signals and supply returns keeps other devices in a system from affecting the output of the DACs.

During power-up supply voltage sequencing, the −15V (or −12V) supply of the op amp may appear first. This will cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is internally clamped to one diode drop below ground.

Careful circuit construction with minimization of lead lengths around the analog circuitry, is a primary concern. Good high frequency supply decoupling will aid in preventing inadvertant noise from appearing on the analog output.

Overall noise reduction and reference stability is of particular concern when using the higher accuracy versions, the DAC0830 and DAC0831, or their advantages are wasted.

3.0 GENERAL APPLICATION IDEAS

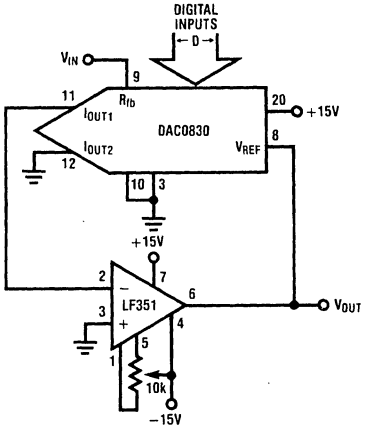
The connections for the control pins of the digital input registers are purposely omitted. Any of the control formats discussed in Section 1 of the accompanying text will work with any of the circuits shown. The method used depends on the overall system provisions and requirements.

The digital input code is referred to as D and represents the decimal equivalent value of the 8-bit binary input, for example:

Binary Input								
Pin 13							Pin 7	D
MSB							LSB	Decimal Equivalent
1	1	1	1	1	1	1	1	255
1	0	0	0	0	0	0	0	128
0	0	0	1	0	0	0	0	16
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0

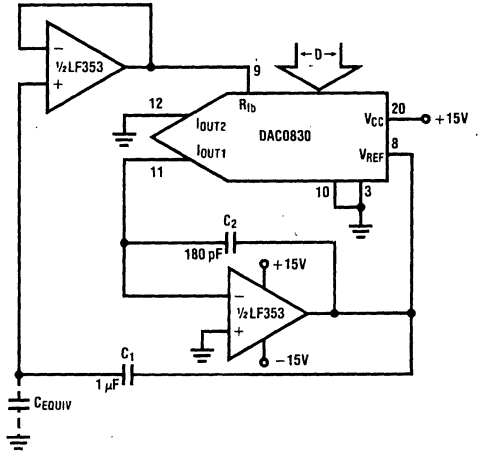
Applications

DAC Controlled Amplifier (Volume Control)



- $V_{OUT} = \frac{-V_{IN}\,(256)}{D}$
- When D = 0, the amplifier will go open loop and the output will saturate.
- Feedback impedance from the −input to the output varies from 15 kΩ to ∞ as the input code changes from full-scale to zero.

Capacitance Multiplier

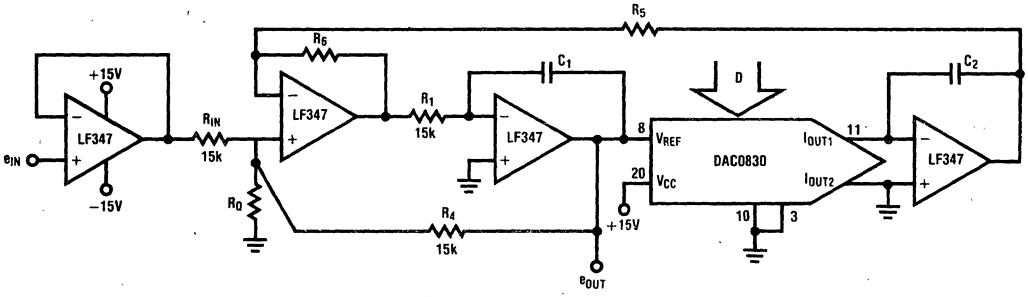


TL/H/5608–16

- $C_{EQUIV} = C_1\left(1 + \frac{256}{D}\right)$
- Maximum voltage across the equivalent capacitance is limited to $\frac{V_{O\,MAX}\,(\text{op amp})}{1 + \frac{256}{D}}$
- C_2 is used to improve settling time of op amp.

Applications (Continued)

Variable f_O, Variable Q_O, Constant BW Bandpass Filter

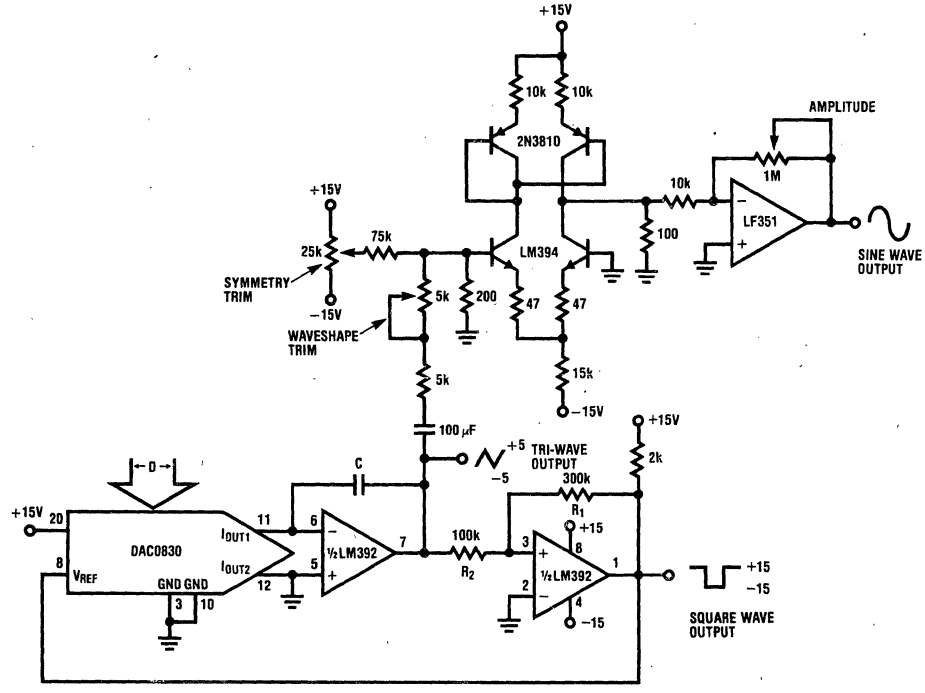


TL/H/5608–17

- $f_O = \frac{\sqrt{\frac{KD}{256}}}{2\pi R_1 C}$; $Q_O = \sqrt{\frac{KD}{256}}\,\frac{(2R_Q + R_1)}{R_Q(K+1)}$; $3dbBW = \frac{R_Q(K+1)}{2\pi R_1 C(2R_Q + R_1)}$

  where $C_1 = C_2 = C$; $K = \frac{R_6}{R_5}$ and R_1 = R of DAC = 15k
- $H_O = 1$ for $R_{IN} = R_4 = R_1$
- Range of f_O and Q is ≈ 16 to 1 for circuit shown. The range can be extended to 255 to 1 by replacing R_1 with a second DAC0830 driven by the same digital input word.
- Maximum $f_O \times Q$ product should be ≤200 kHz.

DAC Controlled Function Generator

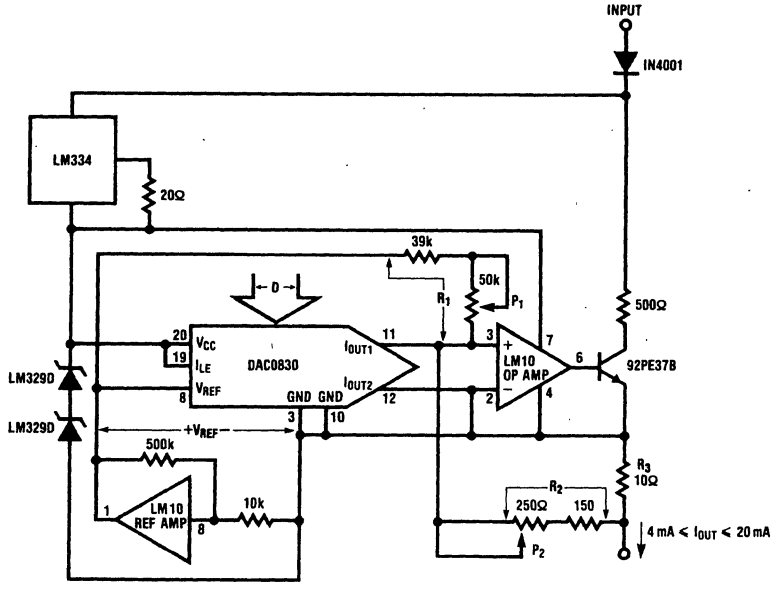


TL/H/5608–16

- DAC controls the frequency of sine, square, and triangle outputs.
- $f = \frac{D}{256(20k)C}$ for $V_{OMAX} = V_{OMIN}$ of square wave output and $R_1 = 3\,R_2$.
- 255 to 1 linear frequency range; oscillator stops with D = 0
- Trim symmetry and wave-shape for minimum sine wave distortion.

Applications (Continued)

Two Terminal Floating 4 to 20 mA Current Loop Controller

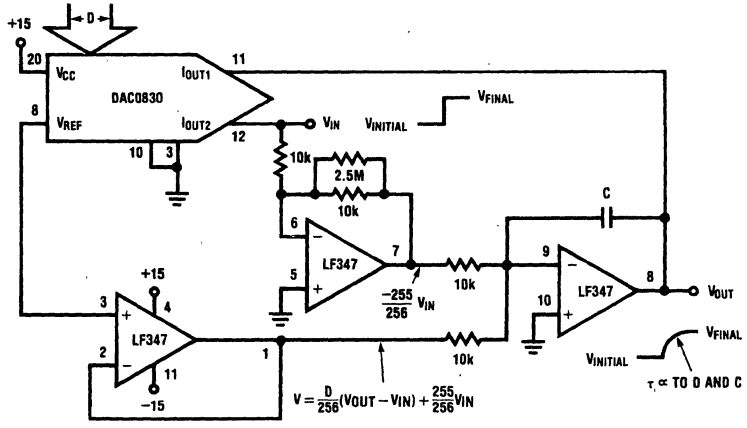


TL/H/5608–19

$$I_{OUT} = V_{REF}\left[\frac{1}{R_1} + \frac{D}{256\,R_{fb}}\right]\left[1 + \frac{R_2}{R_3}\right]$$

- DAC0830 linearly controls the current flow from the input terminal to the output terminal to be 4 mA (for D=0) to 19.94 mA (for D=255).
- Circuit operates with a terminal voltage differential of 16V to 55V.
- P_2 adjusts the magnitude of the output current and P_1 adjusts the zero to full scale range of output current.
- Digital inputs can be supplied from a processor using opto isolators on each input or the DAC latches can flow-through (connect control lines to pins 3 and 10 of the DAC) and the input data can be set by SPST toggle switches to ground (pins 3 and 10).

DAC Controlled Exponential Time Response



TL/H/5608–20

- Output responds exponentially to input changes and automatically stops when $V_{OUT} = V_{IN}$
- Output time constant is directly proportional to the DAC input code and capacitor C
- Input voltage must be positive (See section 2.7)

S 5

National Semiconductor

DAC1265A, DAC1265 Hi-Speed 12-Bit D/A Converter with Reference

General Description

The DAC1265A and DAC1265 are fast 12-bit digital to analog converters with internal voltage reference. These DACs use 12 precision high speed bipolar current steering switches, control amplifier, thin film resistor network, and buried zener voltage reference to obtain a high accuracy, very fast analog output current. The DAC1265A and DAC1265 have 10%–90% full-scale transition time under 35 ns and settle to less than ½ LSB in 200 ns. The buried zener reference has long-term stability and temperature drift characteristics comparable to the best discrete or separate IC references.

These digital to analog converters are recommended for applications in CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5 MHz for full range transitions.

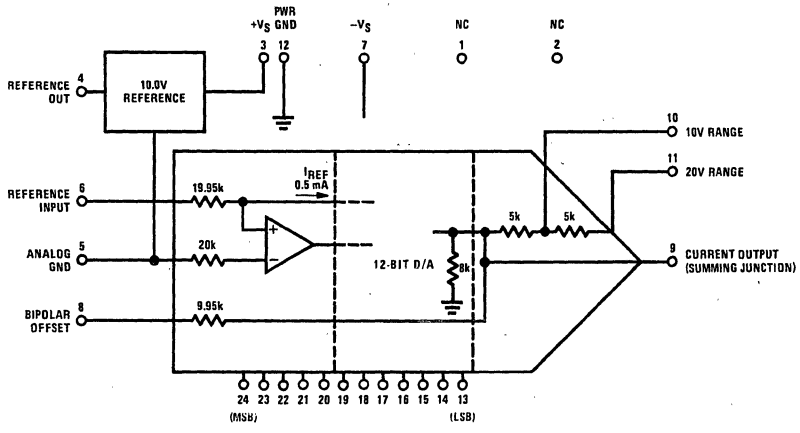
Features

- Bipolar current output DAC and voltage reference
- Fully differential, non-saturating precision current switch — R_{OUT} and C_{OUT} do not change with digital input code
- Internal buried zener reference — 10V ± 1% max
- Precision thin film resistors for use with external op amp for voltage out or as input resistors for a successive approximation A/D converter
- Superior replacement for 12-bit D/A converters of this type

Key Specifications

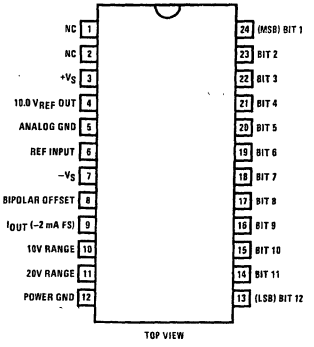
- Resolution and Monotonicity — 12 Bits
- Linearity — 12 Bits
  (Guaranteed over temperature)
- Output Current Settling Time — 400 ns max to 0.01%
- Gain Tempco — ±15 ppm/°C max
- Power Supply Sensitivity — ±10 ppm of FS/% V_{SUPPLY}

Block and Connection Diagrams



TL/H/5242–1

Dual-In-Line Package



TL/H/5242–2

See Ordering Information NS Package J24A

Absolute Maximum Ratings

Supply Voltage (V^+ and V^-)	±18V	Power Dissipation (Note 1)	1000 mW
Current Output (Pin 9) Voltage	−3V, 12V	Short-Circuit Duration (Pins 4 to 12)	Continuous
Logic Input Voltage	−1V, 7V	Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
Reference Input Voltage (Pin 6)	±12V	DAC1265AJ, DAC1265LJ	−55°C to +125°C
Analog GND to Power GND	±1V	DAC1265ACJ, DAC1265LCJ	0°C to +70°C
Bipolar Offset	±12V	Storage Temperature Range	−65°C to +150°C
10V Range	±12V	Maximum Junction Temperature	150°C
20V Range	V^- to +24V	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$V_{SUPPLY} = \pm 15V \pm 5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions		See Note	DAC1265A Typ (Note 11)	DAC1265A Tested Limit (Note 2)	DAC1265A Design Limit (Note 3)	DAC1265 Typ (Note 11)	DAC1265 Tested Limit (Note 2)	DAC1265 Design Limit (Note 3)	Units
CONVERTER CHARACTERISTICS										
Resolution					12			12		Bits
Linearity Error Max	Zero and Full-Scale Adjusted		4	±1/8	±1/4		±1/4	±1/2		LSB
	AJ and LJ Suffix Parts				±1/2			±3/4		
	ACJ and LCJ Suffix Parts					±1/2			±3/4	
Differential Non-Linearity Max	Zero and Full-Scale Adjusted			±1/4	±1/2		±1/2	±3/4		
Monotonicity	AJ and LJ Suffix Parts				**12**			**12**		Bits
	ACJ and LCJ Suffix Parts				12	**12**		12	**12**	
Full-Scale (Gain) Error Max	R2 = 50Ω in *Figure 1*		5	±0.1	±0.20		±0.1	±0.20		% Full-Scale
Offset Error Max All Bits OFF, Logic "0"	Unipolar (*Figure 1* Pin 8 Open)		6	±0.01	±0.05		±0.01	±0.05		
	Bipolar (R1 and R2 = 50Ω in *Figure 2*)		7	±0.05	±0.1		±0.05	±0.15		
Zero Error Max MSB ON	Bipolar (R1 and R2 = 50Ω in *Figure 2*)		8	±0.05	±0.1		±0.05	±0.15		
Gain Adjustment Range Min	R2 = 50Ω ± 50Ω in *Figure 1*				±0.2			±0.2		
Bipolar Offset Adjustment Range Min	R1 = 50Ω ± 50Ω and R2 = 50Ω in *Figure 2*				±0.15			±0.15		
Full-Scale (Gain) Temperature Coefficients Max	Using the Internal Reference	AJ and LJ Suffix	9	10	**15**		15	**30**		ppm/°C
		ACJ and LCJ Suffix		10		**20**	15		**50**	
Unipolar Offset Temperature Coefficients Max		AJ and LJ Suffix		1	**2**		1	**2**		
		ACJ and LCJ Suffix		1		**2**	1		**2**	
Bipolar Zero Temperature Coefficients Max		AJ and LJ Suffix		5	**10**		5	**10**		
		ACJ and LCJ Suffix		5		**10**	5		**10**	
Output Resistance	Exclusive of Offset and Range R_S			7.5	6 to 10		7.5	6 to 10		kΩ

Electrical Characteristics (Continued) $V_{SUPPLY} = \pm 15V \pm 5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter		Conditions	See Note	DAC1265A Typ (Note 11)	DAC1265A Tested Limit (Note 2)	DAC1265A Design Limit (Note 3)	DAC1265 Typ (Note 11)	DAC1265 Tested Limit (Note 2)	DAC1265 Design Limit (Note 3)	Units
Current Output		Unipolar		−2	−1.6 to −2.4		−2	−1.6 to −2.4		mA
		Bipolar		±1.0	±0.8 to ±1.2		±1.0	±0.8 to ±1.2		
Output Capacitance				25			25			pF
Output Noise (FS, 10V Range)		10 Hz to 100 kHz with Internal Reference		40			40			μVrms
Typ Output Voltage Ranges		Using Internal Offset and Range R_S		±2.5, ±5, ±10, 0 to 5, 0 to 10						V
Reference Input Resistance				20.8	15 to 25		20.8	15 to 25		kΩ
Output Compliance Voltage						**−1.5 to 10**			**−1.5 to 10**	V
REFERENCE OUTPUT CHARACTERISTICS										
Reference Voltage	Min	$I_{REF} = 1.5$ mA		10.00	9.90		10.00	9.90		V
	Max				10.10			10.10		
Temperature Coefficient				±8			±12			ppm/°C
Reference Output Current Min					3.0			3.0		mA
Output Resistance Max		$f_O = 1$ kHz, 0.5 mA ≤ I_{REF} ≤ 3 mA		0.05	1.0		0.05	1.0		Ω
DIGITAL AND DC CHARACTERISTICS										
Logic Input Voltage		Logic High Bit ON — AJ and LJ Suffix			**2 to 5.5**			**2 to 5.5**		V
		Logic High Bit ON — ACJ and LCJ Suffix			1.9 to 5.5	**2 to 5.5**		1.9 to 5.5	**2 to 5.5**	
	Max	Logic Low Bit OFF — AJ and LJ Suffix			**0.8**			**0.8**		
		Logic Low Bit OFF — ACJ and LCJ Suffix			1.0	**0.8**		1.0	**0.8**	
Logic Input Current Max		Logic High — AJ and LJ Suffix		150	**300**		150	**300**		μA
		Logic High — ACJ and LCJ Suffix		150	280	**300**	150	280	**300**	
		Logic Low — AJ and LJ Suffix		45	**100**		45	**100**		
		Logic Low — ACJ and LCJ Suffix		45	90	**100**	45	90	**100**	
Power Supply Current Max	$I+$	$V+$ Supply = 15V ± 10%		3	5		3	5		mA
	$I-$	$V-$ Supply = −15V ± 10%		−12	−18		−12	−18		
Power Dissipation Max		$V_{SUPPLY} = \pm 15V$		225	345		225	345		mW
Power Supply Sensitivity Max		$V+$ Supply = 15V ± 10%	10	±3	±10		±3	±10		ppm of FS/% V_{SUPPLY}
		$V-$ Supply = −15V ± 10%	10	±15	±25		±15	±25		

Electrical Characteristics (Continued) $V_{SUPPLY} = \pm 15V \pm 5\%$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	DAC1265A			DAC1265			Units
			Typ (Note 11)	Tested Limit (Note 2)	Design Limit (Note 3)	Typ (Note 11)	Tested Limit (Note 2)	Design Limit (Note 3)	
AC CHARACTERISTICS									
Settling Time Max	FSR Change		200		400	200		400	ns
Full-Scale Transition Max	10% to 90% Rise Time Plus Delay Time		15		30	15		30	ns
	90% to 10% Fall Time Plus Delay Time		30		50	30		50	

Note 1: The typical θ_{JA} of the 24-pin package is 80° C/W.

Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 4: Linearity error $= \frac{V_{OUT} - V_{OFFSET} - (D \times V_{LSB})}{V_{LSB}}$ where $V_{LSB} = \frac{V_{FS} - V_{OFFSET}}{4095}$ and D is the digital input (0 to 4095) which produced V_{OUT}.

Note 5: Percent gain error for 10V range $= \frac{(V_{FS} - V_{OFFSET}) - (4095/4096)10V}{10V} \times 100$.

Note 6: Unipolar offset error for 10V range $= (V_{OUT}/10V) \times 100$ in percent of full-scale.

Note 7: Bipolar offset error for 10V range $= \frac{V_{OUT} - (-5V)}{10V} \times 100$ in percent of full-scale.

Note 8: Bipolar zero error for 10V range $= (V_{OUT}/10V) \times 100$ in percent of full-scale.

Note 9: Gain error tempco $= \frac{(V_{FS} - V_{OFFSET}) \text{at } (T_{MAX} \text{ or } T_{MIN}) - (V_{FS} - V_{OFFSET}) \text{ at } 25°C}{10V \text{ range} \times (T_{MAX} \text{ or } T_{MIN} - 25°C)} \times 10^6$ in ppm/°C.

Note 10: Power supply sensitivity for 10V range $= 10^6 \times \frac{(V_{FS} - V_{OFFSET}) \text{ at } (16.5V \text{ or } -13.5V) - (V_{FS} - V_{OFFSET}) \text{ at } (13.5V \text{ or } -16.5V)}{10V \times 20\%}$ in ppm of FS/%V_S.

The opposite supply is held at −15V or +15V respectively.

Note 11: Typicals are at 25°C and represent most likely parametric norm.

Functional Description and Applications

1.0 BUFFERED VOLTAGE OUTPUT CONNECTION

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (LF411A) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV maximum offset voltage should be used to keep offset errors below ½ LSB). Unipolar zero will typically be within ±½ LSB (plus op amp offset), and if a 50Ω fixed resistor is substituted for the 100Ω trimmer (R2, *Figure 1*), full-scale accuracy will be within 0.1% (0.20% maximum). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer (R1, *Figure 2*) will give a bipolar zero error typically within ±2 LSB (0.05%).

1.1 Unipolar Configuration *(Figure 1)*

This configuration will provide a unipolar 0V to 9.9976V output range.

Step 1—Offset Adjust (Zero)

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000V (1 LSB = 2.44 mV). In most cases this trim is not needed.

Step 2—Gain Adjust

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976V (full-scale adjusted to 1 LSB less than nominal full-scale of 10.000V). If a 10.2375V full-scale is desired (exactly 2.5 mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

1.2 Bipolar Configuration *(Figure 2)*

This configuration will provide a bipolar output voltage from — 5.000V to 4.9976V, with positive full-scale occurring with all bits ON (all 1s).

Step 1—Offset Adjust

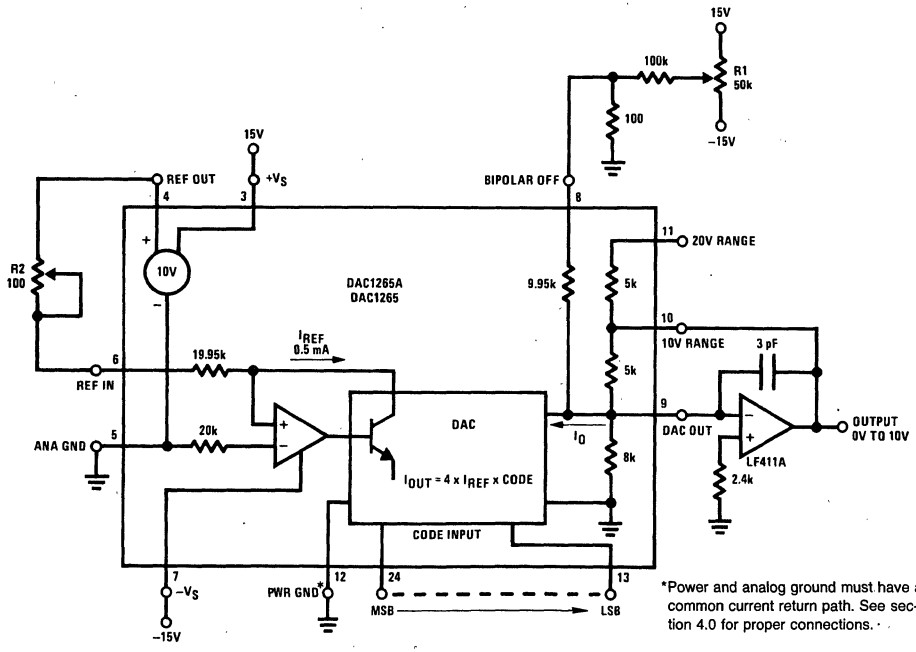
Turn OFF all bits. Adjust 100Ω offset trimmer, R1, to give −5.000V output.

Step 2—Gain Adjust

Turn ON all bits. Adjust 100Ω gain trimmer, R2, to give a reading of 4.9976V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive. Bipolar zero error (MSB bit ON) is not adjusted separately and is typically < ±0.05% of FS after offset and gain adjust.

Functional Description and Applications (Continued)



*Power and analog ground must have a common current return path. See section 4.0 for proper connections.

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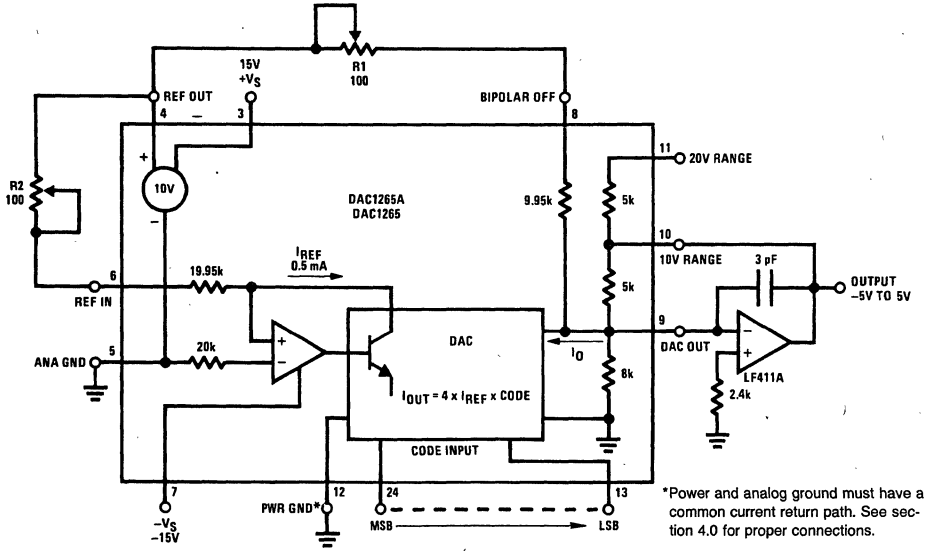
FIGURE 1. 0V to 10V Unipolar Voltage Output



*Power and analog ground must have a common current return path. See section 4.0 for proper connections.

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FIGURE 2. ±5V Bipolar Voltage Output

Functional Description and Applications (Continued)

1.3 Other Voltage Ranges *(Figure 3)*

The DAC1265A and DAC1265 can also be easily configured for a unipolar 0V to 5V range or ±2.5V and ±10V bipolar ranges by using the additional 5k application resistor provided at the 20V range R terminal, pin 11. For a 5V range (0V to 5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either left open for unipolar or connected through a 100Ω pot to the REF OUT for the bipolar range. For the ± 10V range use the 5k resistors in series by connecting only pin 11 to the op amp output and connecting the bipolar offset as shown. The ±10V option is shown in *Figure 3.*

2.0 INTERNAL/EXTERNAL REFERENCE USE

The performance of the DAC1265A and DAC1265 is specified with the internal reference driving the DAC since all trimming and testing (especially for full-scale and bipolar) is done in this configuration.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5 mA to REF IN and 1.0 mA to BIPOLAR OFFSET, if used). A minimum of 1.5 mA is available for driving external circuits. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% maximum error. The temperature coefficient is comparable to that of the full-scale TC for a particular grade.

3.0 DIGITAL INPUT

The DAC1265A and DAC1265 use a standard positive true straight binary code for unipolar outputs (all 1s give full-scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0s on the inputs, the output will go to negative full-scale; with 100...00 (only the MSB on), the output will be 0.00V; with all 1s, the output will go to positive full-scale.

The threshold of the digital input circuitry is set at 1.4V and does not vary with supply voltage. The input lines can interface with any type of 5V logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in *Figure 4*. The input line can be modeled as a 30 kΩ resistance connected to a −0.7V rail.

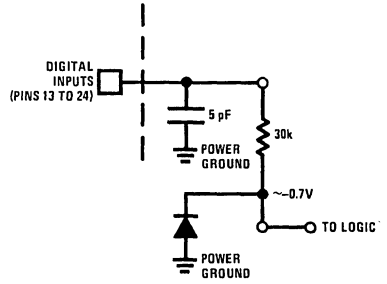

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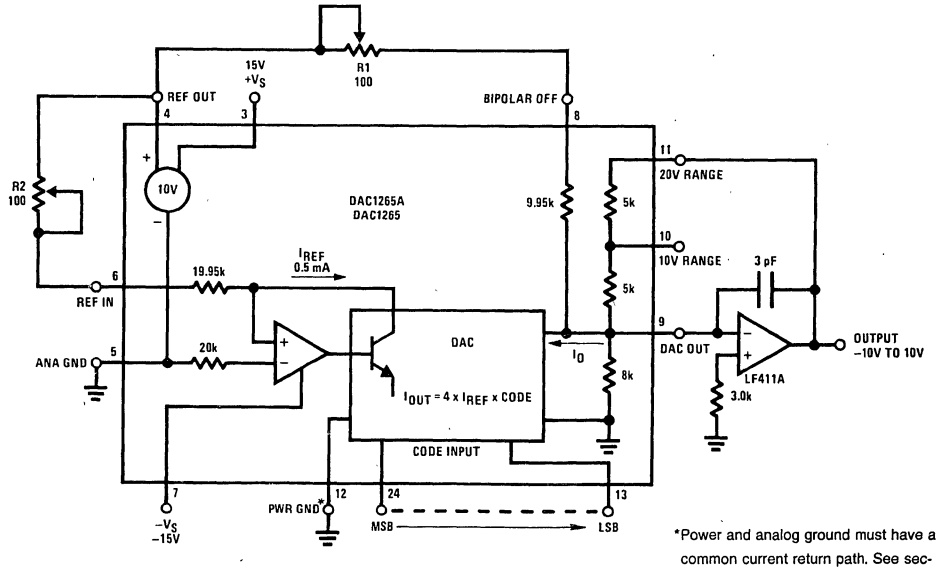
FIGURE 4. Equivalent Digital Input Circuit



*Power and analog ground must have a common current return path. See section 4.0 for proper connections.

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FIGURE 3. ±10V Voltage Output

Functional Description and Applications (Continued)

4.0 APPLICATION OF ANALOG AND POWER GROUNDS

The DAC1265A and DAC1265 bring out separate analog and power grounds to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 mV without any loss in performance. There may be some loss in linearity beyond that level. If these DACs are to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog ground at pin 5 is the ground reference point for the internal reference and is thus the "high quality" ground; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If power ground contains high frequency noise beyond 200 mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

5.0 OUTPUT VOLTAGE COMPLIANCE

The DAC1265A and DAC1265 have a typical output compliance range from −2V to 10V. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25 pF at the output terminal which produces an equivalent error current if the voltage deviates from power ground. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in non-linear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply.

6.0 DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. *Figure 5* shows a connection using the gain and bipolar output resistors to give a ±1.60V bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 mA to −2 mA unipolar output current and using the 10.0V reference voltage for bipolar offset. For example, setting $R_X = 2.67\ k\Omega$ gives a ±1V range with a 1 kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. Using a 50Ω resistor for R_X would allow interface to a 50Ω cable with a ±50 mV full-scale swing.

7.0 HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the DAC1265A and DAC1265 make them ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 12-bit converter system to be constructed with a minimum parts count. Shown in *Figure 6* is a configuration using standard components; this system completes a full 12-bit conversion in 10 μs unipolar or bipolar. This converter will be accurate to ±½ LSB of 12 bits and have a typical gain TC of 10 ppm/°C.

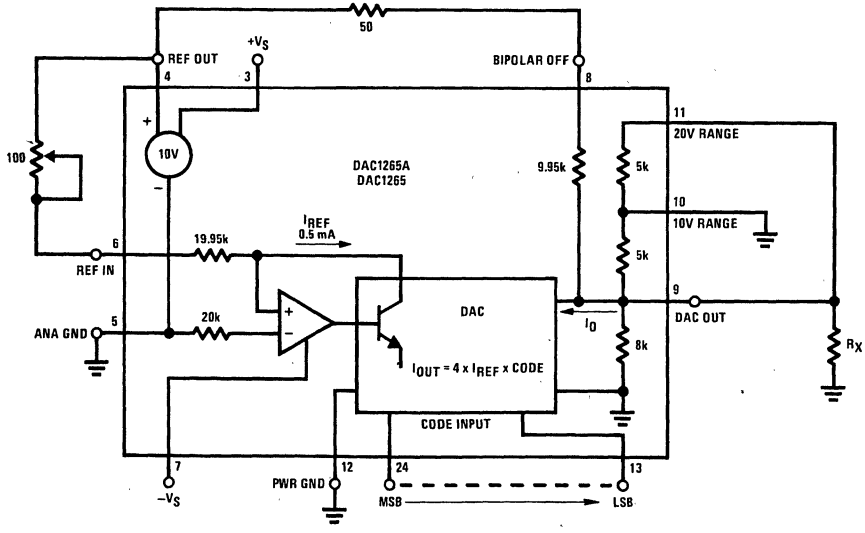

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FIGURE 5. Unbuffered Bipolar Voltage Output

Functional Description and Applications (Continued)

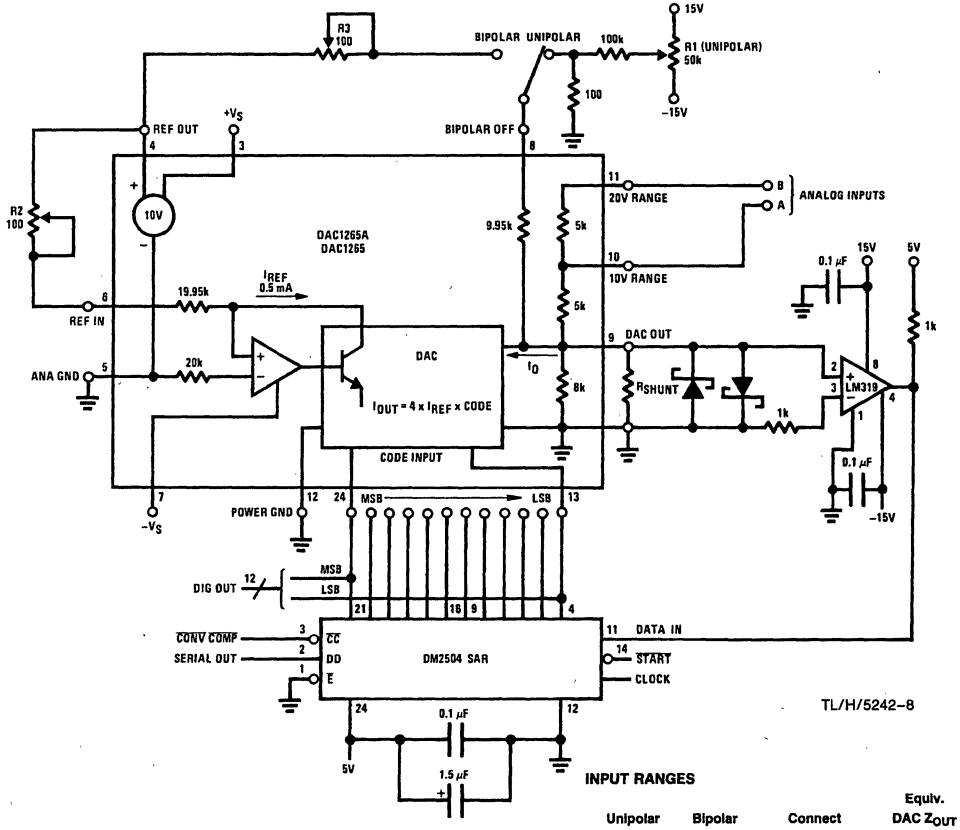
In the unipolar mode, the system range is 0V to 9.9976V, with each bit having a value of 2.44 mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from ½ LSB below to ½ LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of 1.22 mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full-scale, use an input voltage of 9.9963V (10V-1 LSB-½ LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is −5.0V to 4.9976V. Bipolar offset trimming is done by applying a −4.9988V input signal and trimming R3 for the LSB transition (all other bits "0").

Full-scale is set by applying 4.9963V and trimming R2 for the LSB transition (all other bits "1"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 12-bit ±½ LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1 kΩ, 1 LSB = 0.5 mV), to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will vary with the input configuration (*Figure 6,* Input Ranges Table).

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the LF411A op amp.



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INPUT RANGES

Unipolar	Bipolar	Connect	Equiv. DAC Z_{OUT}
0 to 5	±2.5	Input to A B to DAC OUT	1.60 kΩ
0 to 10	±5	Input to A	2.35 kΩ
0 to 20	±10	Input to B	3.08 kΩ

FIGURE 6. Fast Precision Analog to Digital Converter

Definition of Terms

Digital Inputs: The DAC1265A and DAC1265 accept digital input codes in binary format and may be user connected for any one of three binary codes: straight binary, two's complement, or offset binary.

Digital Input MSB LSB	Analog Output		
	Straight Binary	Offset Binary	Two's Complement*
000..000	zero	−FS (Full-Scale)	zero
011...111	½ FS−1 LSB	zero−1 LSB	+FS−1 LSB
100..000	½ FS	zero	−FS
111...111	+FS−1 LSB	+FS−1 LSB	zero−1 LSB

*Invert MSB with external inverter to obtain Two's Complement coding

Linearity Error: Linearity error of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full-scale (all bits ON).

Differential Non-Linearity: For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one-bit change in code. A differential non-linearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input. It is guaranteed by testing the major carry transitions, i.e., 100...000 to 011...111, etc.

Settling Time: Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full-scale or major carry transition.

Gain Tempco: The change in full-scale analog output over the specified temperature range expressed in parts per million of full-scale per °C (ppm of FS/°C). Gain error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Gain tempco is calculated for both high ($T_{MAX}-25°C$) and low ($25°C-T_{MIN}$) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst-case drift.

Offset Tempco: The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full-scale per °C (ppm of FS/°C). Offset error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Offset tempco is calculated for both high ($T_{MAX}-25°C$) and low ($25°C-T_{MIN}$) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity: Power supply sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V or + 15V supplies. It is specified under DC conditions and expressed as parts per million of full-scale per percent of change in power supply (ppm of FS/%).

Ordering Information

Temperature Range		0°C to 70°C	−55°C to + 125°C
Linearity Error Over Temperature	±½ Bit	DAC1265ACJ	DAC1265AJ
	±¾ Bit	DAC1265LCJ	DAC1265LJ

National Semiconductor

DAC1266A, DAC1266 Hi-Speed 12-Bit D/A Converter

General Description

The DAC1266A and DAC1266 are fast 12-bit digital to analog converters. These DACs use 12 precision high speed bipolar current steering switches, control amplifier, and a thin film resistor network to obtain a high accuracy, very fast analog output current. The DAC1266A and DAC1266 have 10%–90% full-scale transition time under 30 ns and settle to less than ½ LSB in 200 ns.

These digital to analog converters are recommended for applications in CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5 MHz for full range transitions.

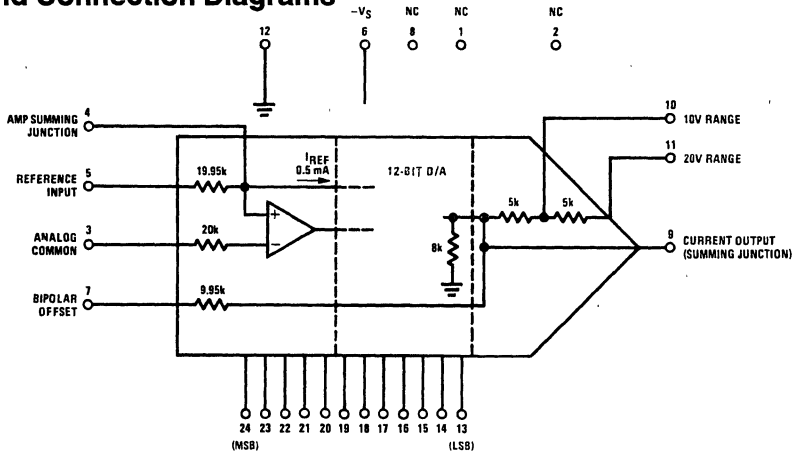
Features

- Bipolar current output DAC
- Fully differential, non-saturating precision current switch — R_{OUT} and C_{OUT} do not change with digital input code
- Precision thin film resistors for use with external op amp for voltage out or as input resistors for a successive approximate A/D converter
- Superior replacement for 12-bit D/A converters of this type

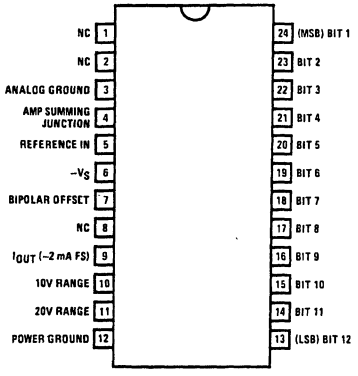
Key Specifications

- Resolution and Monotonicity 12 Bits
- Linearity 12 Bits
  (Guaranteed over temperature)
- Output Current Settling Time 400 ns max to 0.01%
- Full-Scale Transition Time (10%–90%) 30 ns
- Power Supply Sensitivity ±15 ppm of FS/% V_{SUPPLY}

Block and Connection Diagrams



Dual-In-Line Package



Top View

See Ordering Information NS Package J24A

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Absolute Maximum Ratings

Supply Voltage (V^-)	0V to −18V	Power Dissipation (Note 1)	1000 mW
Current Output (Pin 9) Voltage	−3V, 12V	Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
Logic Input Voltage	−1V, 7V	DAC1266AJ, DAC1266LJ	−55°C to +125°C
Reference Input Voltage (Pin 5)	±12V	DAC1266ACJ, DAC1266LCJ	0°C to +70°C
Analog GND to Power GND	±1V	Storage Temperature Range	−65°C to +150°C
Bipolar Offset	±12V	Maximum Junction Temperature	150°C
10V Range	±12V	Lead Temp. (Soldering, 10 sec.)	300°C
20V Range	V^- to +24V		

Electrical Characteristics

$V_{SUPPLY} = -15V \pm 5\%$ and $V_{REF} = 10.000V$ unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	DAC1266A Typ	DAC1266A Tested Limit (Note 2)	DAC1266A Design Limit (Note 3)	DAC1266 Typ	DAC1266 Tested Limit (Note 2)	DAC1266 Design Limit (Note 3)	Units
CONVERTER CHARACTERISTICS									
Resolution				12			12		Bits
Linearity Error Max	Zero and Full-Scale Adjusted	4	±1/8	±1/4		±1/4	±1/2		LSB
	AJ and LJ Suffix Parts			±1/2			±3/4		
	ACJ and LCJ Suffix Parts				±1/2			±3/4	
Differential Non-Linearity Max	Zero and Full-Scale Adjusted		±1/4	±1/2		±1/2	±3/4		
Monotonicity	AJ and LJ Suffix Parts			**12**			**12**		Bits
	ACJ and LCJ Suffix Parts			12	**12**		12	**12**	
Full-Scale (Gain) Error Max	R2 = 50Ω in *Figure 1*	5	±0.1	±0.20		±0.1	±0.20		% Full-Scale
Offset Error Max All Bits OFF, Logic "0"	Unipolar (*Figure 1* Pin 7 Open)	6	±0.01	±0.05		±0.01	±0.05		
	Bipolar (R1 and R2 = 50Ω in *Figure 2*)	7	±0.05	±0.1		±0.05	±0.15		
Zero Error Max MSB ON	Bipolar (R1 and R2 = 50Ω in *Figure 2*)	8	±0.05	±0.1		±0.05	±0.15		
Gain Adjustment Range Min	R2 = 50Ω ± 50Ω in *Figure 1*			±0.2			±0.2		
Bipolar Offset Adjustment Range Min	R1 = 50Ω ± 50Ω and R2 = 50Ω in *Figure 2*			±0.15			±0.15		
Full-Scale (Gain) Temperature Coefficients Max	AJ and LJ Suffix	9	1	**3**		5	**10**		ppm/°C
	ACJ and LCJ Suffix		1		**3**	5		**10**	
Unipolar Offset Temperature Coefficients Max	AJ and LJ Suffix		1	**2**		1	**2**		
	ACJ and LCJ Suffix		1		**2**	1		**2**	
Bipolar Zero Temperature Coefficients Max	AJ and LJ Suffix		5	**10**		5	**10**		
	ACJ and LCJ Suffix		5		**10**	5		**10**	
Output Resistance	Exclusive of Offset and Range R_S		7.5	6 to 10		7.5	6 to 10		kΩ
Current Output	Unipolar		−2	−1.6 to −2.4		−2	−1.6 to −2.4		mA
	Bipolar		±1.0	±0.8 to ±1.2		±1.0	±0.8 to ±1.2		

Electrical Characteristics (Continued) $V_{SUPPLY} = -15V \pm 5\%$ and $V_{REF} = 10.000V$ unless otherwise noted.

Boldface limits apply over temperature, $T_{MIN} \leq T_A \leq T_{MAX}$. For all other limits $T_A = 25°C$.

Parameter	Conditions	See Note	DAC1266A Typ	DAC1266A Tested Limit (Note 2)	DAC1266A Design Limit (Note 3)	DAC1266 Typ	DAC1266 Tested Limit (Note 2)	DAC1266 Design Limit (Note 3)	Units
Output Capacitance			25			25			pF
Typ Output Voltage Ranges	Using Internal Offset and Range R_S		±2.5, ±5, ±10, 0 to 5, 0 to 10						V
Reference Input Resistance			20.8	15 to 25		20.8	15 to 25		kΩ
Output Compliance Voltage					**−1.5 to 10**			**−1.5 to 10**	V
DIGITAL AND DC CHARACTERISTICS									
Logic Input Voltage	Logic High Bit ON — AJ and LJ Suffix			**2 to 5.5**			**2 to 5.5**		V
	Logic High Bit ON — ACJ and LCJ Suffix			1.9 to 5.5	**2 to 5.5**		1.9 to 5.5	**2 to 5.5**	
Max	Logic Low Bit OFF — AJ and LJ Suffix			**0.8**			**0.8**		
Max	Logic Low Bit OFF — ACJ and LCJ Suffix			1.0	**0.8**		1.0	**0.8**	
Logic Input Current Max	Logic High — AJ and LJ Suffix		150	**300**		150	**300**		µA
	Logic High — ACJ and LCJ Sufix		150	280	**300**	150	280	**300**	
	Logic Low — AJ and LJ Suffix		45	**100**		45	**100**		
	Logic Low — ACJ and LCJ Suffix		45	90	**100**	45	90	**100**	
Power Supply Current Max	V^- Supply = −15V ± 10%		−12	−18		−12	−18		mA
Power Dissipation Max	V^- Supply = −15V		180	270		180	270		mW
Power Supply Sensitivity Max	V^- Supply = −12V ± 5%	10	±15	±25		±15	±25		ppm of FS/ % V_{SUPPLY}
	V^- Supply = −15V ± 10%	10	±15	±25		±15	±25		
AC CHARACTERISTICS									
Settling Time Max	FSR Change		200		400	200		400	ns
Full-scale Transition Max	Delay Plus 10% to 90% Rise Time		15		30	15		30	
	Delay Plus 90% to 10% Fall Time		30		50	30		50	ns

Note 1: The typical θ_{JA} of the 24-pin package is 80° C/W.

Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed, but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Note 4: Linearity error $= \frac{V_{OUT} - V_{OFFSET} - (D \times V_{LSB})}{V_{LSB}}$ where $V_{LSB} = \frac{V_{FS} - V_{OFFSET}}{4095}$ and D is the digital input (0 to 4095) which produced V_{OUT}.

Note 5: Percent gain error for 10V range $= \frac{(V_{FS} - V_{OFFSET}) - (4095/4096)V_{REF}}{V_{REF}} \times 100$.

Note 6: Unipolar offset error for 10V range $= (V_{OUT}/V_{REF}) \times 100$ in percent of full-scale.

Note 7: Bipolar offset error for 10V range $= \frac{V_{OUT} - (-V_{REF}/2)}{V_{REF}} \times 100$ in percent of full-scale.

Note 8: Bipolar zero error for 10V range $= (V_{OUT}/V_{REF}) \times 100$ in percent of full-scale.

Note 9: Gain error tempco $= \frac{(V_{FS} - V_{OFFSET}) \text{ at } (T_{MAX} \text{ or } T_{MIN}) - (V_{FS} - V_{OFFSET}) \text{ at } 25°C}{10V \text{ range} \times (T_{MAX} \text{ or } T_{MIN} - 25°C)} \times 10^6$ in ppm/°C.

Note 10: Power supply sensitivity for 10V range $= 10^6 \times \frac{(V_{FS} - V_{OFFSET}) \text{ at } (-13.5V) - (V_{FS} - V_{OFFSET}) \text{ at } (-16.5V)}{V_{REF} \times 20\%}$ in ppm of FS/% V_S.

Functional Description and Applications

1.0 BUFFERED VOLTAGE OUTPUT CONNECTION

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (LF411A) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV maximum offset voltage should be used to keep offset errors below ½ LSB). Unipolar zero will typically be within ±½ LSB (plus op amp offset), and if a 50Ω fixed resistor is substituted for the 100Ω trimmer (R2, *Figure 1*), full-scale accuracy will be within 0.1% (0.20% maximum). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer (R1, *Figure 2*) will give a bipolar zero error typically within ±2 LSB (0.05%).

1.1 Unipolar Configuration (*Figure 1*)

This configuration will provide a unipolar 0V to 9.9976V output range.

Step 1—Offset Adjust (Zero)

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000V (1 LSB = 2.44 mV). In most cases this trim is not needed.

Step 2—Gain Adjust

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976V (full-scale adjusted to 1 LSB less than nominal full-scale of 10.000V). If a 10.2375V full-scale is desired (exactly 2.5 mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output or use the LH0071 voltage reference.

1.2 Bipolar Configuration (*Figure 2*)

This configuration will provide a bipolar output voltage from −5.000V to 4.9976V, with positive full-scale occurring with all bits ON (all 1s).

Step 1—Offset Adjust

Turn OFF all bits. Adjust 100Ω offset trimmer, R1, to give −5.000V output.

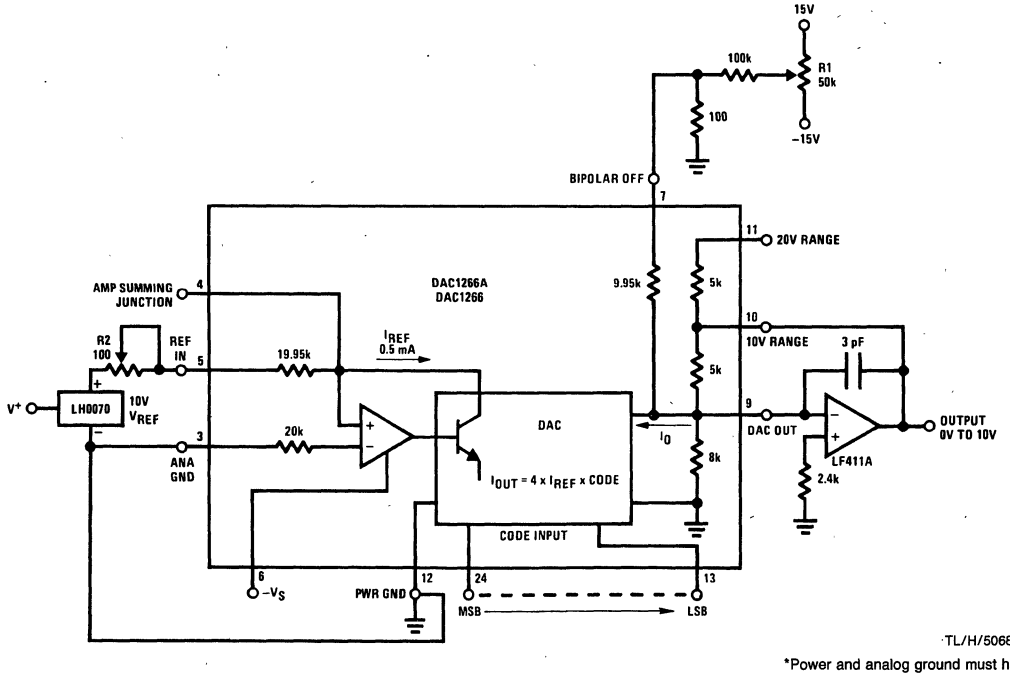
Step 2—Gain Adjust

Turn ON all bits. Adjust 100Ω gain trimmer, R2, to give a reading of 4.9976V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive. Bipolar zero error (MSB bit ON) is not adjusted separately and is typically < ±0.05% of FS after offset and gain adjust.

1.3 Other Voltage Ranges (*Figure 3*)

The DAC1266A and DAC1266 can also be easily configured for a unipolar 0V to 5V range or ±2.5V and ±10V bipolar ranges by using the additional 5k application resistor provided at the 20V range R terminal, pin 11. For a 5V span (0V to 5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either left open for unipolar or connected through a 100Ω pot to the external



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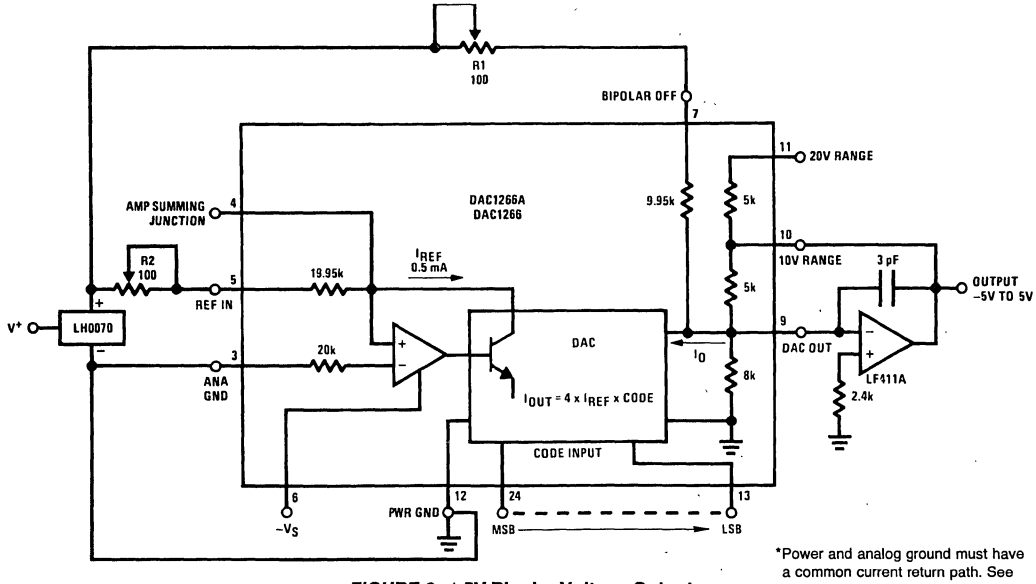
*Power and analog ground must have a common current return path. See section 3.0 for proper connections.

FIGURE 1. 0V to 10V Unipolar Voltage Output

Functional Description and Applications (Continued)



*Power and analog ground must have a common current return path. See section 3.0 for proper connections.

FIGURE 2. ±5V Bipolar Voltage Output

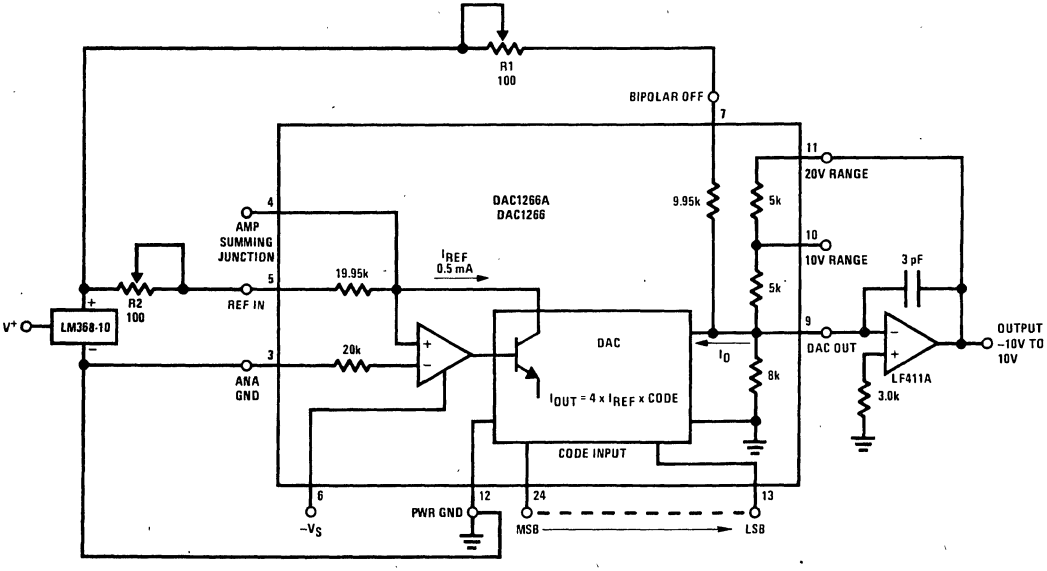


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FIGURE 3. ±10V Voltage Output

*Power and analog ground must have a common current return path. See section 3.0 for proper connections.

Functional Description and Applications (Continued)

reference for the bipolar range. For the ±10V range use the 5k resistors in series by connecting only pin 11 to the op amp output and connecting the bipolar offset as shown. The ±10V option is shown in *Figure 3*.

2.0 DIGITAL INPUT

The DAC1266A and DAC1266 use a standard positive true straight binary code for unipolar outputs (all 1s give full-scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0s on the inputs, the output will go to negative full-scale; with 100...00 (only the MSB on), the output will be 0.00V; with all 1s, the output will go to positive full-scale.

The threshold of the digital input circuitry is set at 1.4V and does not vary with supply voltage. The input lines can interface with any type of 5V logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in *Figure 4*. The input line can be modelled as a 30 kΩ resistance connected to a −0.7V rail.

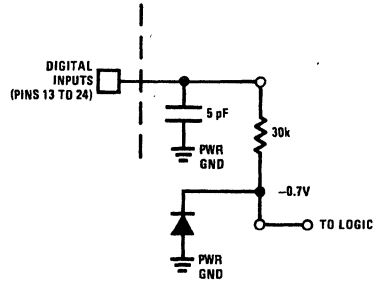

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FIGURE 4. Equivalent Digital Input Circuit

3.0 APPLICATION OF ANALOG AND POWER GROUND

The DAC1266A and DAC1266 bring out separate analog and power grounds to allow optimum connections for low noise and high speed performance. The two ground lines can be separated by up to 200 mV without any loss in performance. There may be some loss in linearity beyond that level. If these DACs are to be used in a system in which the two grounds will be ultimately connected at some distance from the device, it is recommended that parallel back-to-back diodes be connected between the ground lines near the device to prevent a fault condition.

The analog ground at pin 3 is the ground reference point for the internal reference and is thus the "high quality" ground; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground reference point; analog power return is preferred, but digital ground is acceptable. If power ground contains high frequency noise beyond 200 mV, this noise may feed through the converter, so that some caution will be required in applying these grounds.

4.0 OUTPUT VOLTAGE COMPLIANCE

The DAC1266A and DAC1266 have a typical output compliance range from −2V to 10V. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25 pF at the output terminal which produces an equivalent error current if the voltage deviates from power ground. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in non-linear performance. Compliance limits are a function of output current and negative supply.

5.0 DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. *Figure 5* shows a connection using the gain and bipolar output resistors to give a ±1.60V bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 mA to −2 mA unipolar output current and using the 10.0V reference voltage for bipolar offset. For example, setting $R_X = 2.67$ kΩ give a ±1V range with a 1 kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. Using a 50Ω resistor for R_X would allow interface to a 50Ω cable with a ±50 mV full-scale swing.

6.0 HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the DAC1266A and DAC1266 make them ideal for high speed successive approximation A/D converters. Shown in *Figure 6* is a configuration using standard components; this system completes a full 12-bit conversion in 10 μs unipolar or bipolar. This converter will be accurate to ±½ LSB of 12 bits and have a typical gain TC of 10 ppm/°C.

Functional Description and Applications (Continued)

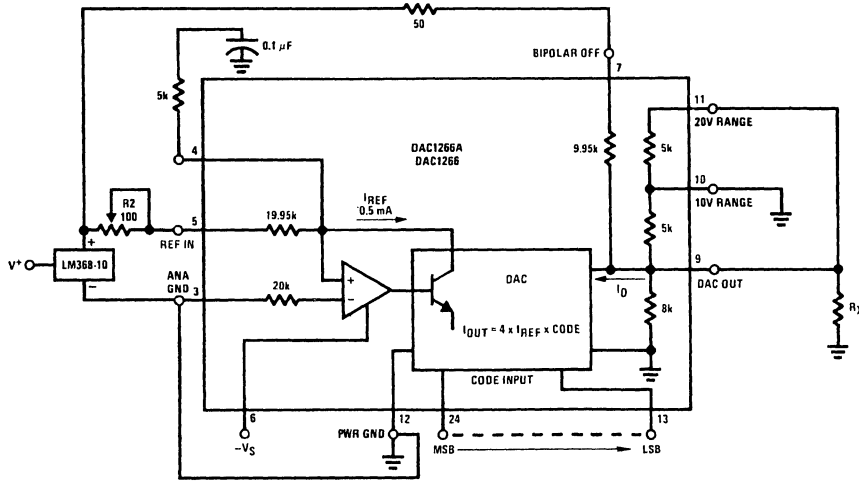
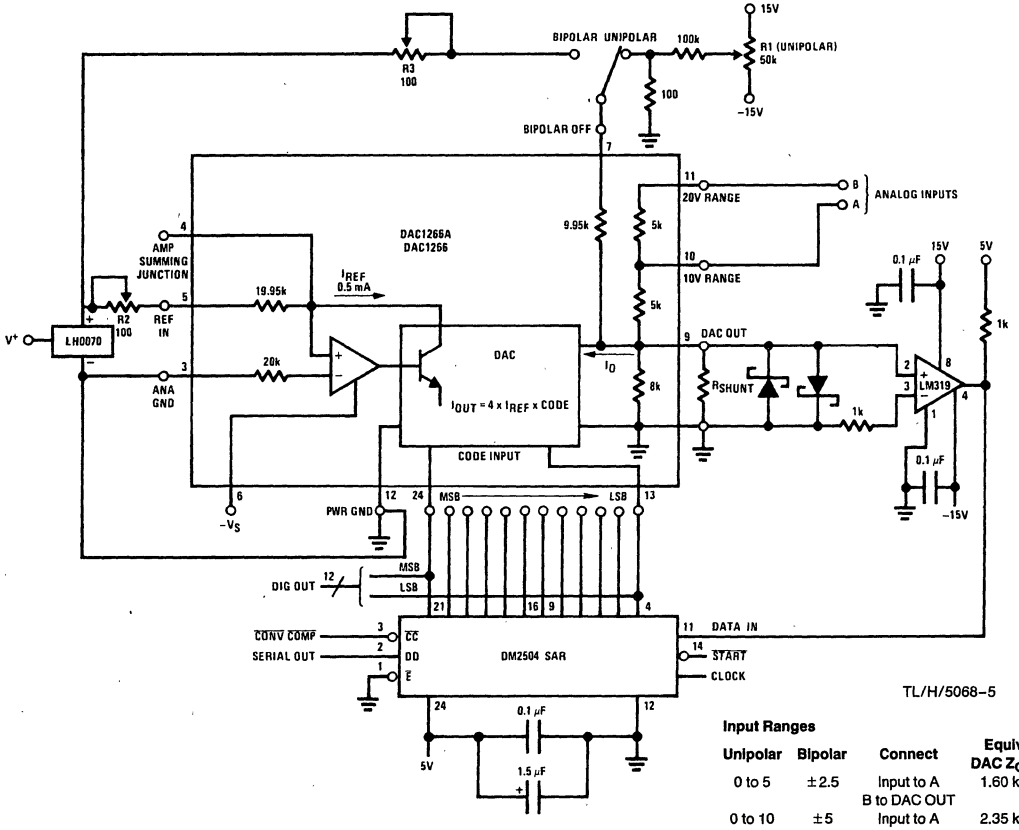


FIGURE 5. Unbuffered Bipolar Voltage Output



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Input Ranges

Unipolar	Bipolar	Connect	Equiv. DAC Z_{OUT}
0 to 5	±2.5	Input to A B to DAC OUT	1.60 kΩ
0 to 10	±5	Input to A	2.35 kΩ
0 to 20	±10	Input to B	3.08 kΩ

FIGURE 6. Fast Precision Analog to Digital Converter

Functional Description and Applications (Continued)

In the unipolar mode, the system range is 0V to 9.9976V, with each bit having a value of 2.44 mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from ½ LSB below to ½ LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of 1.22 mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full-scale, use an input voltage of 9.9963V (10V-1 LSB-½ LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is −5.0V to 4.9976V. Bipolar offset trimming is done by applying a −4.9988V input signal and trimming R3 for the LSB transition (all other bits "0").

Full-scale is set by applying a 4.9963V and trimming R2 for the LSB transition (all other bits "1"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 12-bit ±½ LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1 kΩ, 1 LSB = 0.5 mV), to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will vary with the input configuration (*Figure 6*, Input Ranges Table).

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the LF411A op amp.

Definition of Terms

Digital Inputs: The DAC1266A and DAC1266 accept digital input codes in binary format and may be user connected for any one of three binary codes: straight binary, two's complement, or offset binary.

Digital Input MSB LSB	Analog Output		
	Straight Binary	Offset Binary	Two's Complement*
000...000	zero	−FS (Full-Scale)	zero
011...111	½ FS-1 LSB	zero-1 LSB	+FS-1 LSB
100...000	½ FS	zero	−FS
111...111	+FS-1 LSB	+FS-1 LSB	zero-1 LSB

*Invert MSB with external inverter to obtain Two's Complement coding

Linearity Error: Linearity Error of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full-scale (all bits ON).

Differential Non-Linearity: For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one-bit change in code. A differential non-linearity of ± 1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input. It is guaranteed by testing the major carry transitions; i.e., 100...000 to 011...111 etc.

Settling Time: Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full-scale or major carry transition.

Gain Tempco: The change in full-scale analog output over the specified temperature range expressed in parts per million of full-scale per °C (ppm of FS/°C). Gain error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Gain tempco is calculated for both high (T_{MAX}-25°C) and low (25°C-T_{MIN}) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst-case drift.

Offset Tempco: The change in analog output with all bits OFF over the specified temperature expressed in parts per million of full-scale per °C (ppm of FS/°C). Offset error is measured with respect to 25°C at high (T_{MAX}) and low (T_{MIN}) temperatures. Offset tempco is calculated for both high (T_{MAX}−25°C) and low (25°C−T_{MIN}) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity: Power supply sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V supply. It is specified under DC conditions and expressed as parts per million of full-scale per percent of change in power supply (ppm of FS/%).

Ordering Information

Temperature Range		0°C to 70°C	−55°C to +125°C
Linearity Error Over Temperature	±½ Bit	DAC1266ACJ	DAC1266AJ
	±¾ Bit	DAC1266LCJ	DAC1266LJ

National Semiconductor

LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

General Description

The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100 kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

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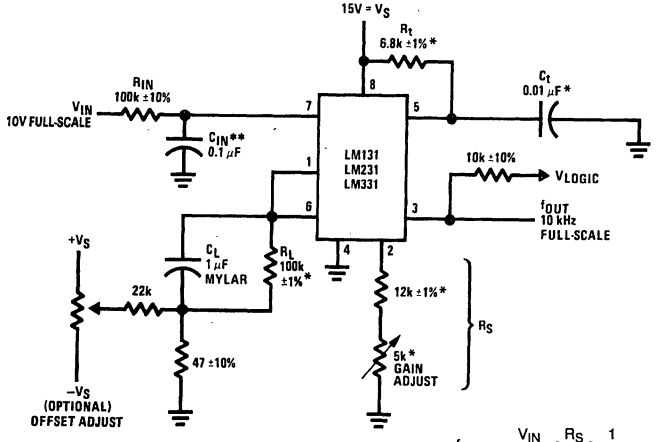
Typical Applications



$$f_{OUT} = \frac{V_{IN}}{2.09\,V} \bullet \frac{R_S}{R_L} \bullet \frac{1}{R_t C_t}$$

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*Use stable components with low temperature coefficients. See Typical Applications section.

**0.1μF or 1μF, See "Principles of Operation."

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

Absolute Maximum Ratings

	LM131A/LM131	LM231A/LM231	LM331A/LM331
Supply Voltage	40V	40V	40V
Output Short Circuit to Ground	Continuous	Continuous	Continuous
Output Short Circuit to V_{CC}	Continuous	Continuous	Continuous
Input Voltage	−0.2V to +V_S	−0.2V to +V_S	−0.2V to +V_S
	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}
Operating Ambient Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{jA})			
(H Package) P_D	670 mW	570 mW	570 mW
θ_{jA}	150°C/W	150°C/W	150°C/W
(N Package) P_D		500 mW	500 mW
θ_{jA}		155°C/W	155°C/W

Electrical Characteristics T_A = 25°C unless otherwise specified. (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
VFC Non-Linearity (Note 2)	4.5V ≤ V_S ≤ 20V		±0.003	±0.01	% Full-Scale
	T_{MIN} ≤ T_A ≤ T_{MAX}		±0.006	±0.02	% Full-Scale
VFC Non-Linearity In Circuit of *Figure 1*	V_S = 15V, f = 10 Hz to 11 kHz		±0.024	±0.14	%Full-Scale
Conversion Accuracy Scale Factor (Gain)	V_{IN} = −10V, R_S = 14 kΩ				
LM131, LM131A, LM231, LM231A		0.95	1.00	1.05	kHz/V
LM331, LM331A		0.90	1.00	1.10	kHz/V
Temperature Stability of Gain	T_{MIN} ≤ T_A ≤ T_{MAX}, 4.5V ≤ V_S ≤ 20V				
LM131/LM231/LM331			±30	±150	ppm/°C
LM131A/LM231A/LM331A			±20	±50	ppm/°C
Change of Gain with V_S	4.5V≤V_S ≤ 10V		0.01	0.1	%/V
	10V ≤ V_S ≤ 40V		0.006	0.06	%/V
Rated Full-Scale Frequency	V_{IN} = −10V	10.0			kHz
Overrange (Beyond Full-Scale) Frequency	V_{IN} = −11V	10			%
INPUT COMPARATOR					
Offset Voltage			±3	±10	mV
LM131/LM231/LM331	T_{MIN} ≤ T_A ≤ T_{MAX}		±4	±14	mV
LM131A/LM231A/LM331A	T_{MIN} ≤ T_A ≤ T_{MAX}		±3	±10	mV
Bias Current			−80	−300	nA
Offset Current			±8	±100	nA
Common-Mode Range	T_{MIN} ≤ T_A ≤ T_{MAX}	−0.2		V_{CC}−2.0	V
TIMER					
Timer Threshold Voltage, Pin 5		0.63	0.667	0.70	× V_S
Input Bias Current, Pin 5	V_S = 15V				
All Devices	0V≤$V_{PIN\,5}$ ≤ 9.9V		±10	±100	nA
LM131/LM231/LM331	$V_{PIN\,5}$ = 10V		200	1000	nA
LM131A/LM231A/LM331A	$V_{PIN\,5}$ = 10V		200	500	nA
$V_{SAT\ PIN\ 5}$ (Reset)	I = 5 mA		0.22	0.5	V

Electrical Characteristics (Continued) $T_A = 25°C$ unless otherwise specified (Note 1)

Parameter	Conditions	Min	Typ	Max	Units
CURRENT SOURCE (Pin 1)					
Output Current	$R_S = 14\ k\Omega$, $V_{PIN\ 1} = 0$				
LM131, LM131A, LM231, LM231A		126	135	144	μA
LM331, LM331A		116	136	156	μA
Change with Voltage	$0V \le V_{PIN\ 1} \le 10V$		0.2	1.0	μA
Current Source OFF Leakage					
LM131, LM131A			0.01	1.0	nA
LM231, LM231A, LM331, LM331A			0.02	10.0	nA
All Devices	$T_A = T_{MAX}$		2.0	50.0	nA
Operating Range of Current (Typical)			(10 to 500)		μA
REFERENCE VOLTAGE (Pin 2)					
LM131, LM131A, LM231, LM231A		1.76	1.89	2.02	V_{DC}
LM331, LM331A		1.70	1.89	2.08	V_{DC}
Stability vs Temperature			±60		ppm/°C
Stability vs Time, 1000 Hours			±0.1		%
LOGIC OUTPUT (Pin 3)					
V_{SAT}	$I = 5$ mA		0.15	0.50	V
	$I = 3.2$ mA (2 TTL Loads), $T_{MIN} \le T_A \le T_{MAX}$		0.10	0.40	V
OFF Leakage			±0.05	1.0	μA
SUPPLY CURRENT					
LM131, LM131A, LM231,	$V_S = 5V$	2.0	3.0	4.0	mA
LM231A	$V_S = 40V$	2.5	4.0	6.0	mA
LM331, LM331A	$V_S = 5V$	1.5	3.0	6.0	mA
	$V_S = 40V$	2.0	4.0	8.0	mA

Note 1: All specifications apply in the circuit of *Figure 3*, with $4.0V \le V_S \le 40V$, unless otherwise noted.

Note 2: Nonlinearity is defined as the deviation of f_{OUT} from $V_{IN} \times (10\ kHz/-10\ V_{DC})$ when the circuit has been trimmed for zero error at 10 Hz and at 10 kHz, over the frequency range 1 Hz to 11 kHz. For the timing capacitor, C_T, use NPO ceramic, Teflon®, or polystyrene.

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Functional Block Diagrams

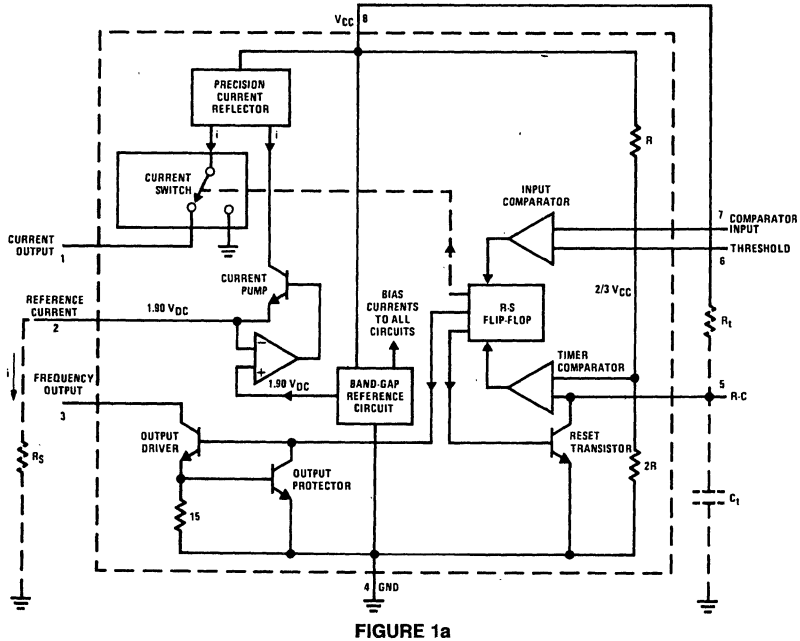

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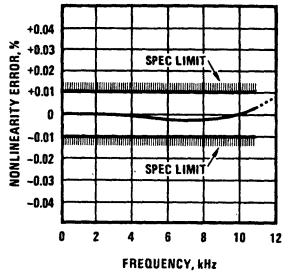
FIGURE 1a

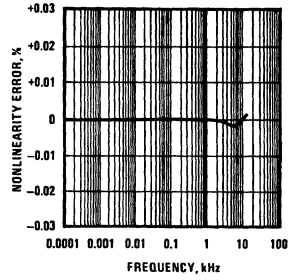
Typical Performance Characteristics

(All electrical characteristics apply for the circuit of *Figure 3*, unless otherwise noted.)

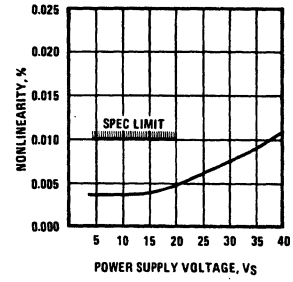
Nonlinearity Error, LM131 Family, as Precision V-to-F Converter (*Figure 3*)



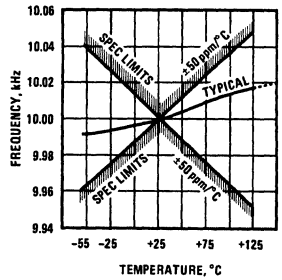
Nonlinearity Error, LM131 Family



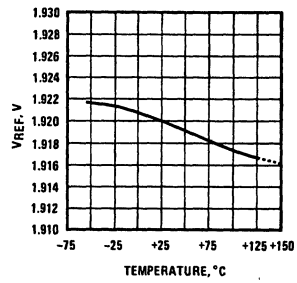
Nonlinearity vs Power Supply Voltage



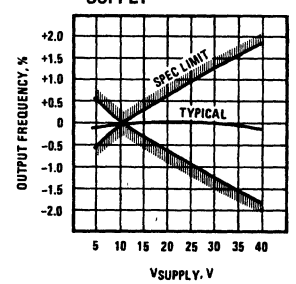
Frequency vs Temperature, LM131A



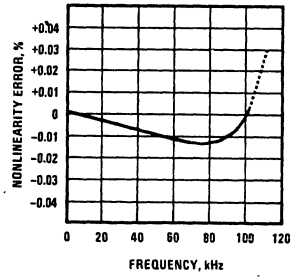
V_{REF} vs Temperature, LM131A



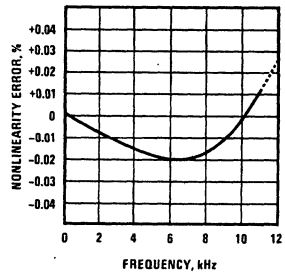
Output Frequency vs V_{SUPPLY}



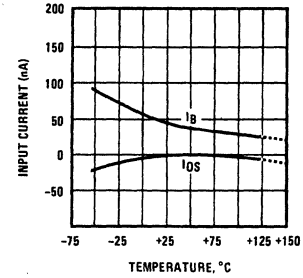
100 kHz Nonlinearity Error, LM131 Family (*Figure 4*)



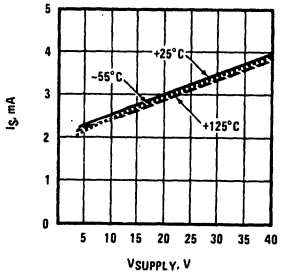
Nonlinearity Error, LM131 (*Figure 1*)



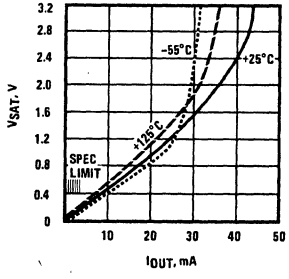
Input Current (Pins 6, 7) vs Temperature



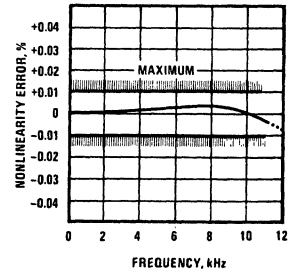
Power Drain vs V_{SUPPLY}



Output Saturation Voltage vs I_{OUT} (Pin 3)



Nonlinearity Error, Precision F-to-V Converter (*Figure 6*)



TL/H/5680–3

Typical Applications (Continued)

PRINCIPLES OF OPERATION OF A SIMPLIFIED VOLTAGE-TO-FREQUENCY CONVERTER

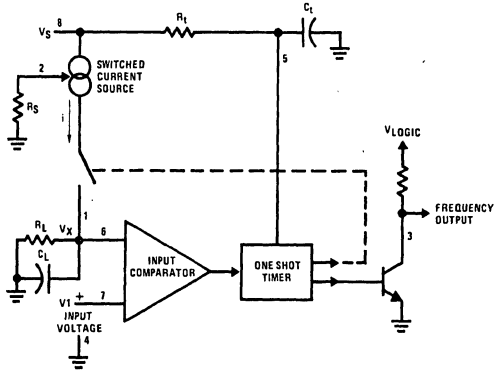
The LM131 is a monolithic circuit designed for accuracy and versatile operation when applied as a voltage-to-frequency (V-to-F) converter or as a frequency-to-voltage (F-to-V) converter. A simplified block diagram of the LM131 is shown in *Figure 2* and consists of a switched current source, input comparator, and 1-shot timer.

The operation of these blocks is best understood by going through the operating cycle of the basic V-to-F converter, *Figure 2*, which consists of the simplified block diagram of the LM131 and the various resistors and capacitors connected to it.

The voltage comparator compares a positive input voltage, V1, at pin 7 to the voltage, V_X, at pin 6. If V1 is greater, the comparator will trigger the 1-shot timer. The output of the timer will turn ON both the frequency output transistor and the switched current source for a period $t = 1.1\ R_tC_t$. During this period, the current i will flow out of the switched current source and provide a fixed amount of charge, $Q = i \times t$, into the capacitor, C_L. This will normally charge V_X up to a higher level than V1. At the end of the timing period, the current i will turn OFF, and the timer will reset itself.

Now there is no current flowing from pin 1, and the capacitor C_L will be gradually discharged by R_L until V_X falls to the level of V1. Then the comparator will trigger the timer and start another cycle.

The current flowing into C_L is exactly $I_{AVE} = i \times (1.1 \times R_tC_t) \times f$, and the current flowing out of C_L is exactly $V_X/R_L \cong V_{IN}/R_L$. If V_{IN} is doubled, the frequency will double to maintain this balance. Even a simple V-to-F converter can provide a frequency precisely proportional to its input voltage over a wide range of frequencies.



TL/H/5680–4

FIGURE 2. Simplified Block Diagram of Stand-Alone Voltage-to-Frequency Converter Showing LM131 and External Components

DETAIL OF OPERATION, FUNCTIONAL BLOCK DIAGRAM (*FIGURE 1a*)

The block diagram shows a band gap reference which provides a stable 1.9 V_{DC} output. This 1.9 V_{DC} is well regulated over a V_S range of 3.9V to 40V. It also has a flat, low temperature coefficient, and typically changes less than ½% over a 100°C temperature change.

The current pump circuit forces the voltage at pin 2 to be at 1.9V, and causes a current $i = 1.90V/R_S$ to flow. For $R_S = 14k$, $i = 135\ \mu A$. The precision current reflector provides a current equal to i to the current switch. The current switch switches the current to pin 1 or to ground depending on the state of the R_S flip-flop.

The timing function consists of an R_S flip-flop, and a timer comparator connected to the external R_tC_t network. When the input comparator detects a voltage at pin 7 higher than pin 6, it sets the R_S flip-flop which turns ON the current switch and the output driver transistor. When the voltage at pin 5 rises to ⅔ V_{CC}, the timer comparator causes the R_S flip-flop to reset. The reset transistor is then turned ON and the current switch is turned OFF.

However, if the input comparator still detects pin 7 higher than pin 6 when pin 5 crosses ⅔ V_{CC}, the flip-flop will not be reset, and the current at pin 1 will continue to flow, in its attempt to make the voltage at pin 6 higher than pin 7. This condition will usually apply under start-up conditions or in the case of an overload voltage at signal input. It should be noted that during this sort of overload, the output frequency will be 0; as soon as the signal is restored to the working range, the output frequency will be resumed.

The output driver transistor acts to saturate pin 3 with an ON resistance of about 50Ω. In case of overvoltage, the output current is actively limited to less than 50 mA.

The voltage at pin 2 is regulated at 1.90 V_{DC} for all values of i between 10 μA to 500 μA. It can be used as a voltage reference for other components, but care must be taken to ensure that current is not taken from it which could reduce the accuracy of the converter.

PRINCIPLES OF OPERATION OF BASIC VOLTAGE-TO-FREQUENCY CONVERTER (*FIGURE 1*)

The simple stand-alone V-to-F converter shown in *Figure 1* includes all the basic circuitry of *Figure 2* plus a few components for improved performance.

A resistor, $R_{IN} = 100\ k\Omega \pm 10\%$, has been added in the path to pin 7, so that the bias current at pin 7 (−80 nA typical) will cancel the effect of the bias current at pin 6 and help provide minimum frequency offset.

The resistance R_S at pin 2 is made up of a 12 kΩ fixed resistor plus a 5 kΩ (cermet, preferably) gain adjust rheostat. The function of this adjustment is to trim out the gain tolerance of the LM131, and the tolerance of R_t, R_L and C_t.

S 5

Typical Applications (Continued)

For best results, all the components should be stable low-temperature-coefficient components, such as metal-film resistors. The capacitor should have low dielectric absorption; depending on the temperature characteristics desired, NPO ceramic, polystyrene, Teflon or polypropylene are best suited.

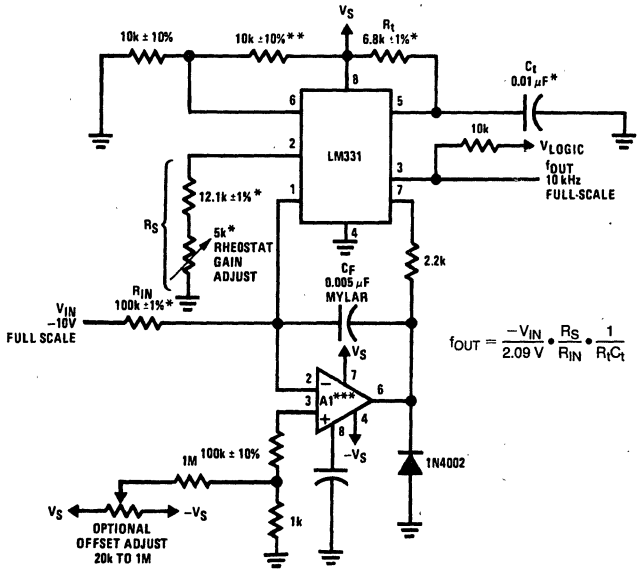
A capacitor is added from pin 7 to ground to act as a filter for V_{IN}. A value of 0.01 μF to 0.1 μF will be adequate in most cases; however, in cases where better filtering is required, a 1 μF capacitor can be used. When the RC time constants are matched at pin 6 and pin 7, a voltage step at V_{IN} will cause a step change in f_{OUT}. If C_{IN} is much less than C_L, a step at V_{IN} may cause f_{OUT} to stop momentarily. A 47Ω resistor, in series with the 1 μF C_L, is added to give hysteresis effect which helps the input comparator provide the excellent linearity (0.03% typical).

DETAIL OF OPERATION OF PRECISION V-TO-F CONVERTER (*FIGURE 3*)

In this circuit, integration is performed by using a conventional operational amplifier and feedback capacitor, C_F. When the integrator's output crosses the nominal threshold level at pin 6 of the LM131, the timing cycle is initiated. The average current fed into the op amp's summing point (pin 2) is $i \times (1.1\ R_tC_t) \times f$ which is perfectly balanced with $-V_{IN}/R_{IN}$. In this circuit, the voltage offset of the LM131 input comparator does not affect the offset or accuracy of the V-to-F converter as it does in the stand-alone V-to-F converter; nor does the LM131 bias current or offset current. Instead, the offset voltage and offset current of the operational amplifier are the only limits on how small the signal can be accurately converted. Since op amps with voltage offset well below 1 mV and offset currents well below 2 nA are available at low cost, this circuit is recommended for best accuracy for small signals. This circuit also responds immediately to any change of input signal (which a stand-alone circuit does not) so that the output frequency will be an accurate representation of V_{IN}, as quickly as 2 output pulses' spacing can be measured.

In the precision mode, excellent linearity is obtained because the current source (pin 1) is always at ground potential and that voltage does not vary with V_{IN} or f_{OUT}. (In the stand-alone V-to-F converter, a major cause of non-linearity is the output impedance at pin 1 which causes i to change as a function of V_{IN}).

The circuit of *Figure 4* operates in the same way as *Figure 3*, but with the necessary changes for high speed operation.



TL/H/5680–5

*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

***Use low offset voltage and low offset current op amps for A1: recommended types LM108, LM308A, LF411A

FIGURE 3. Standard Test Circuit and Applications Circuit, Precision Voltage-to-Frequency Converter

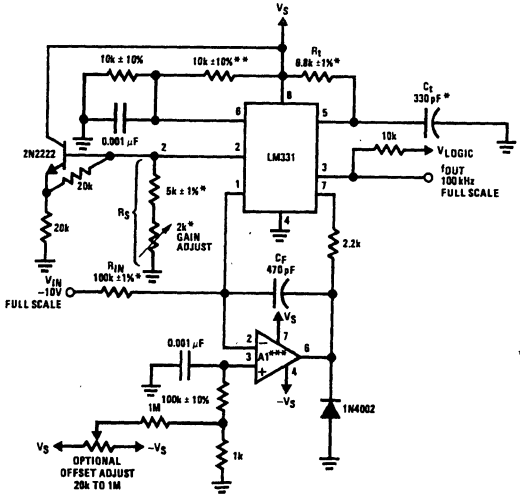
Typical Applications (Continued)

DETAILS OF OPERATION, FREQUENCY-TO-VOLTAGE CONVERTERS *FIGURES 5 AND 6)*

In these applications, a pulse input at f_{IN} is differentiated by a C-R network and the negative-going edge at pin 6 causes the input comparator to trigger the timer circuit. Just as with a V-to-F converter, the average current flowing out of pin 1 is $I_{AVERAGE} = i \times (1.1\ R_tC_t) \times f$.

In the simple circuit of *FIGURE 5*, this current is filtered in the network $R_L = 100\ k\Omega$ and 1 μF. The ripple will be less than 10 mV peak, but the response will be slow, with a 0.1 second time constant, and settling of 0.7 second to 0.1% accuracy.

In the precision circuit, an operational amplifier provides a buffered output and also acts as a 2-pole filter. The ripple will be less than 5 mV peak for all frequencies above 1 kHz, and the response time will be much quicker than in *Figure 5*. However, for input frequencies below 200 Hz, this circuit will have worse ripple than *Figure 5*. The engineering of the filter time-constants to get adequate response and small enough ripple simply requires a study of the compromises to be made. Inherently, V-to-F converter response can be fast, but F-to-V response can not.



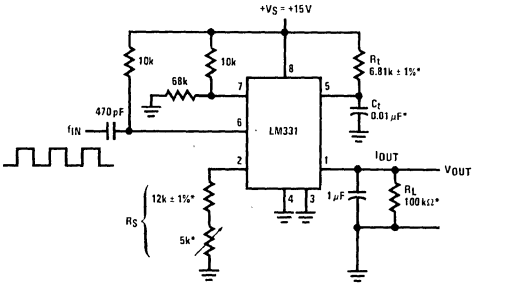
*Use stable components with low temperature coefficients. See Typical Applications section.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

***Use low offset voltage and low offset current op amps for A1: recommended types LF411A or LF356.

TL/H/5680–6

FIGURE 4. Precision Voltage-to-Frequency Converter, 100 kHz Full-Scale, ±0.03% Non-Linearity

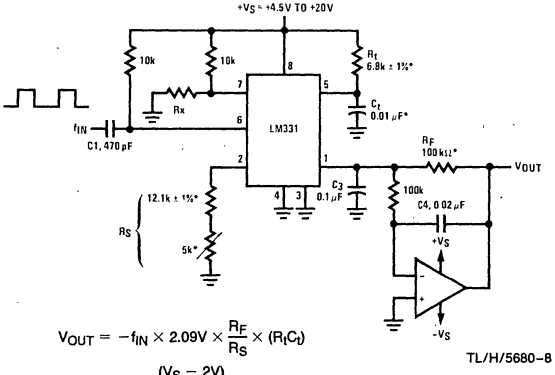


TL/H/5680–7

$$V_{OUT} = f_{IN} \times 2.09V \times \frac{R_L}{R_S} \times (R_tC_t)$$

*Use stable components with low temperature coefficients.

FIGURE 5. Simple Frequency-to-Voltage Converter, 10 kHz Full-Scale, ±0.06% Non-Linearity



TL/H/5680–8

$$V_{OUT} = -f_{IN} \times 2.09V \times \frac{R_F}{R_S} \times (R_tC_t)$$

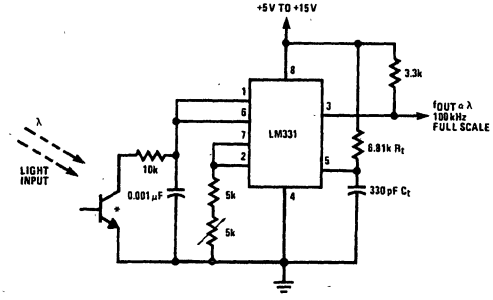
$$\text{SELECT } R_X = \frac{(V_S - 2V)}{0.2\ mA}$$

*Use stable components with low temperature coefficients.

FIGURE 6. Precision Frequency-to-Voltage Converter, 10 kHz Full-Scale with 2-Pole Filter, ±0.01% Non-Linearity Maximum

Typical Applications (Continued)

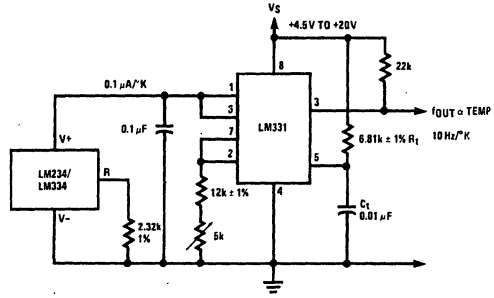
Light Intensity to Frequency Converter



TL/H/5680–9

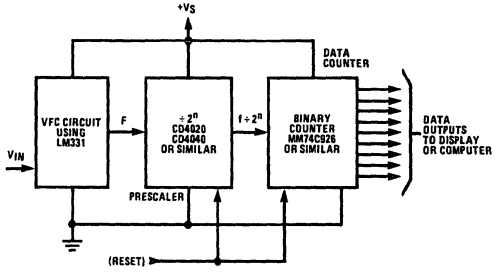
*L14F-1, L14G-1 or L14H-1, photo transistor (General Electric Co.) or similar

Temperature to Frequency Converter



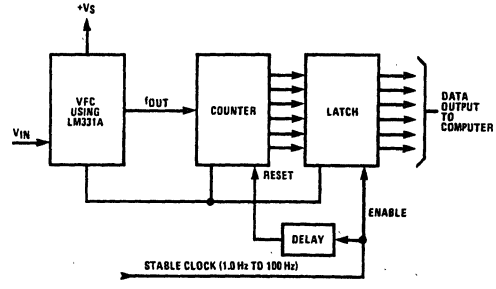
TL/H/5680–10

Long-Term Digital Integrator Using VFC



TL/H/5680–11

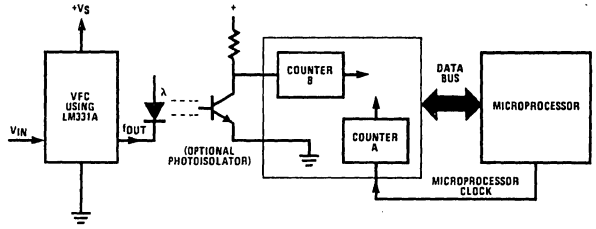
Basic Analog-to-Digital Converter Using Voltage-to-Frequency Converter



TL/H/5680–12

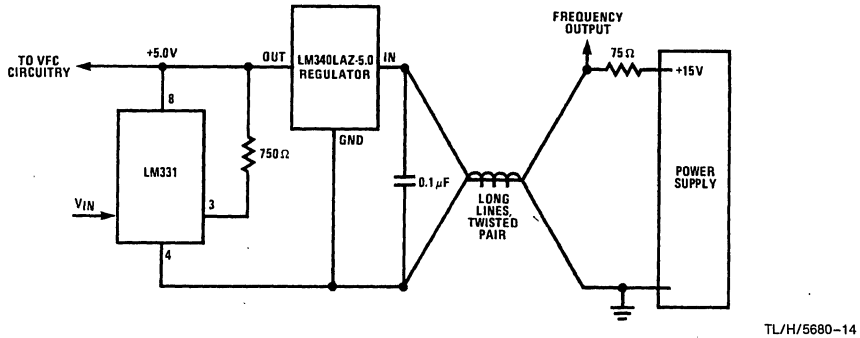
Typical Applications (Continued)

Analog-to-Digital Converter with Microprocessor



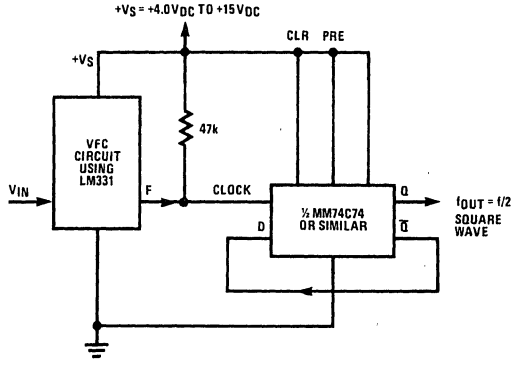
TL/H/5680–13

Remote Voltage-to-Frequency Converter with 2-Wire Transmitter and Receiver



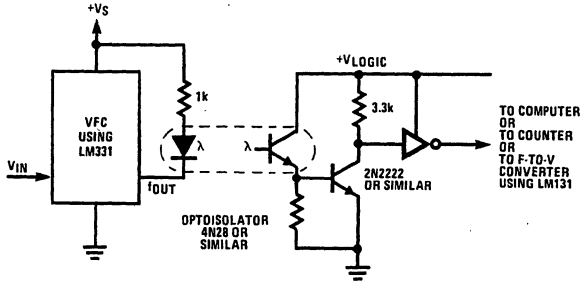
TL/H/5680–14

Voltage-to-Frequency Converter with Square-Wave Output Using ÷ 2 Flip-Flop



TL/H/5680–15

Voltage-to-Frequency Converter with Isolators

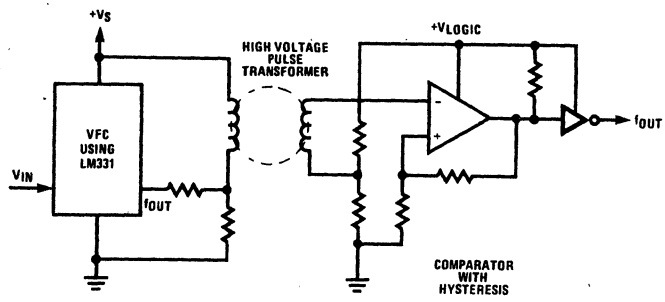


TL/H/5680–16

S 5

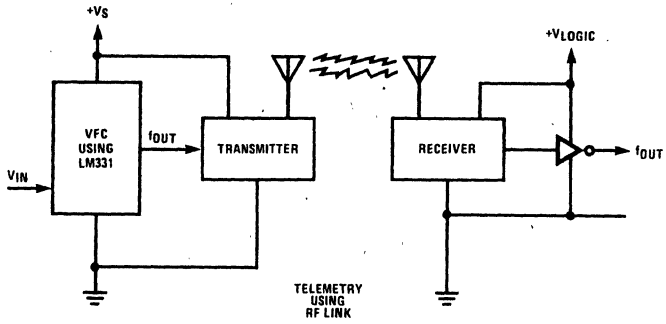
Typical Applications (Continued)

Voltage-to-Frequency Converter with Isolators



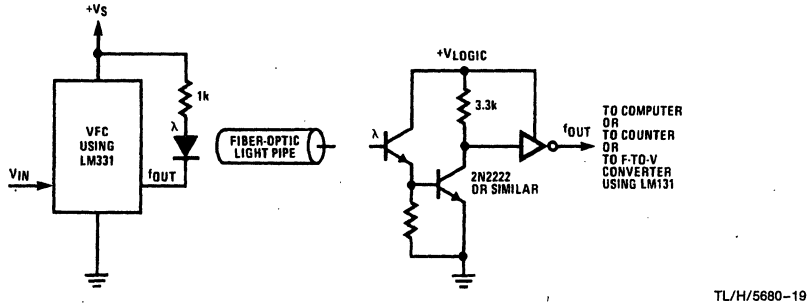
TL/H/5680–17

Voltage-to-Frequency Converter with Isolators



TL/H/5680–18

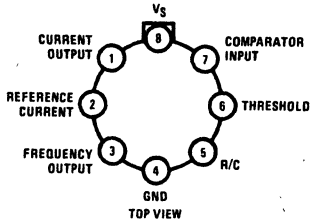
Voltage-to-Frequency Converter with Isolators



TL/H/5680–19

Connection Diagrams

Metal Can Package



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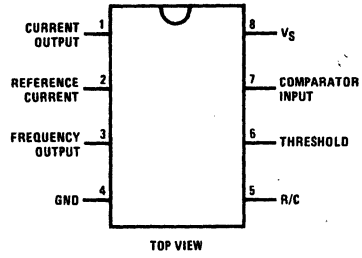
Order Number LM131AH, LM131H, LM231AH, LM231H, LM331AH or LM331H
See NS Package H08C

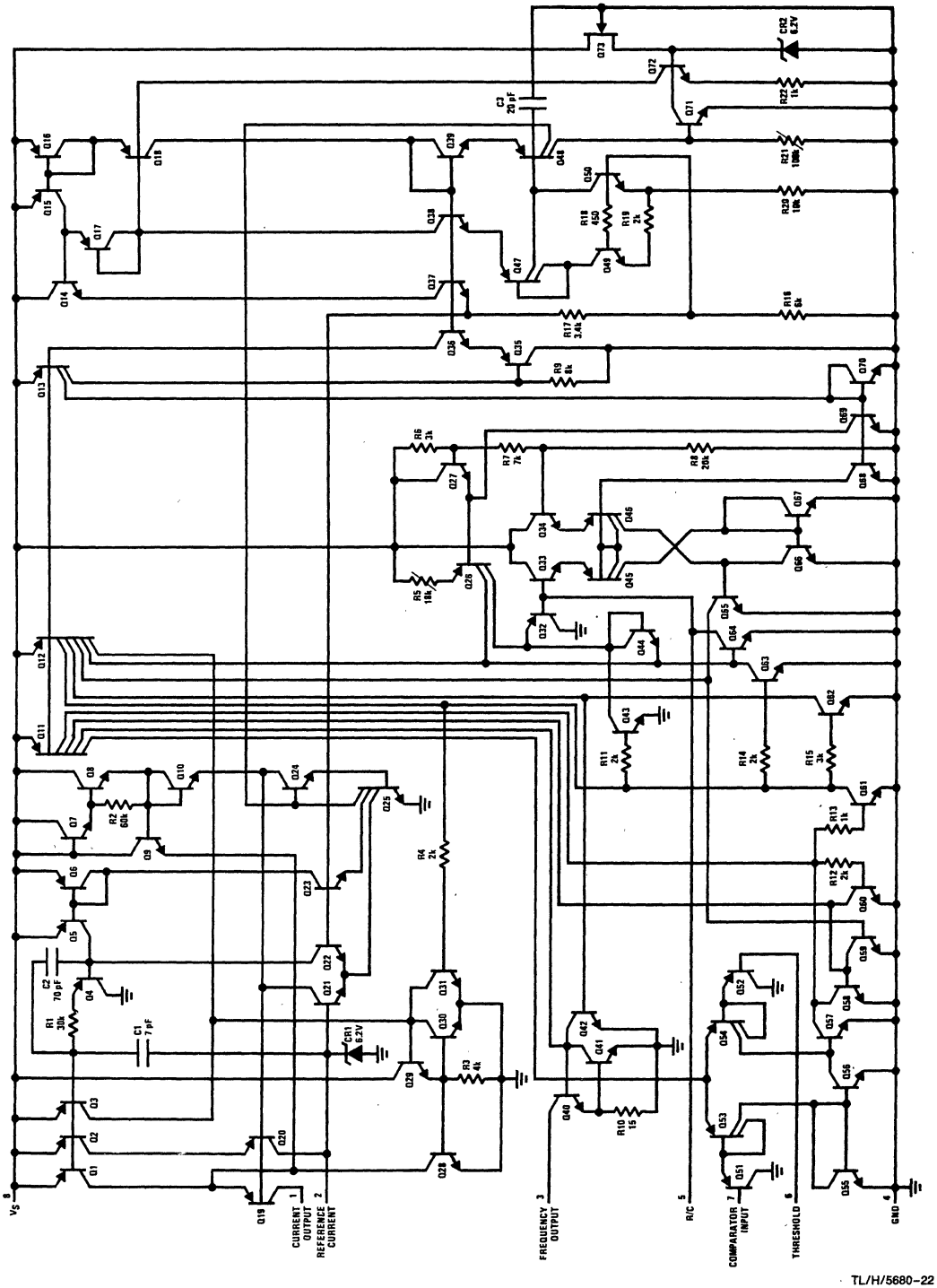
Dual-In-Line Package



TL/H/5680–21

Order Number LM231AN, LM231N, LM331AN, or LM331N
See NS Package N08E

Schematic Diagram



TL/H/5680–22

Section 6

Analog Switches

Analog Switches

Section Contents

National Semiconductor

AH5020C Monolithic Analog Current Switch

General Description

A versatile dual monolithic JFET analog switch economically fulfills a wide variety of multiplexing and analog switching applications.

These switches may be driven directly from standard 5V logic.

The monolithic construction guarantees tight resistance match and track.

Features

■ Interfaces with standard TTL	
■ "ON" resistance match	2Ω
■ Low "ON" resistance	150Ω
■ Very low leakage	50 pA
■ Large analog signal range	±10V peak
■ High switching speed	150 ns
■ Excellent isolation between channels	80 dB at 1 kHz

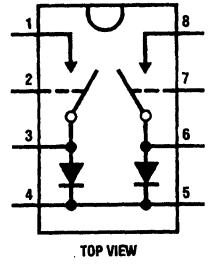
Applications

- AD/DA converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition
- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

For voltage switching applications see LF13331, LF13332, and LF13333 Analog Switch Family.

Connection and Schematic Diagrams

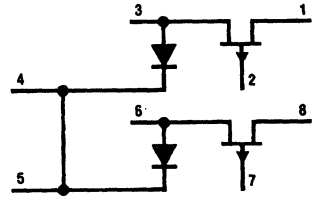
Dual-In-Line Package



TOP VIEW

TL/H/5166–1

Order Number AH5020C
See NS Package J08A



TL/H/5166–2

Note: All diode cathodes are internally connected to the substrate.

Absolute Maximum Ratings

Input Voltage	30V	Power Dissipation	500 mW
Positive Analog Signal Voltage	30V	Operating Temp. Range	−25°C to +85°C
Negative Analog Signal Voltage	−15V	Storage Temperature Range	−65°C to +150°C
Diode Current	10 mA	Lead Temp. (Soldering, 10 seconds)	300°C
Drain Current	30 mA		

Electrical Characteristics (Notes 1 and 2)

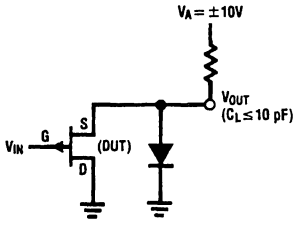
Symbols	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	V_{GD} = 4.5V, V_{SD} = 0.7V V_{GD} = 11V, V_{SD} = 0.7V T_A = 85°C, V_{GD} = 11V, V_{SD} = 0.7V	0.01 0.01	0.1 0.2 10	nA nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	V_{SD} = 0.7V, V_{GS} = 3.8V T_A = 85°C	0.01	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 1 mA T_A = 85°C	0.08	1 200	nA nA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = 2 mA T_A = 85°C	0.13	5 10	nA μA
$I_{G(ON)}$	Leakage Current "ON"	V_{GD} = 0V, I_S = −2 mA T_A = 85°C	0.1	10 20	nA μA
$r_{DS(ON)}$	Drain-Source Resistance	V_{GS} = 0.5V, I_S = 2 mA T_A = +85°C	90	150 240	Ω Ω
V_{DIODE}	Forward Diode Drop	I_D = 0.5 mA		0.8	V
$r_{DS(ON)}$	Match	V_{GS} = 0, I_D = 1 mA	2	20	Ω
T_{ON}	Turn "ON" Time	See ac Test Circuit	150	500	ns
T_{OFF}	Turn "OFF" Time	See ac Test Circuit	300	500	ns
CT	Cross Talk	See ac Test Circuit	120		dB

Note 1: Test conditions 25°C unless otherwise noted.

Note 2: "OFF" and "ON" notation refers to the conduction state of the FET switch.

Test Circuits

AC Test Circuit



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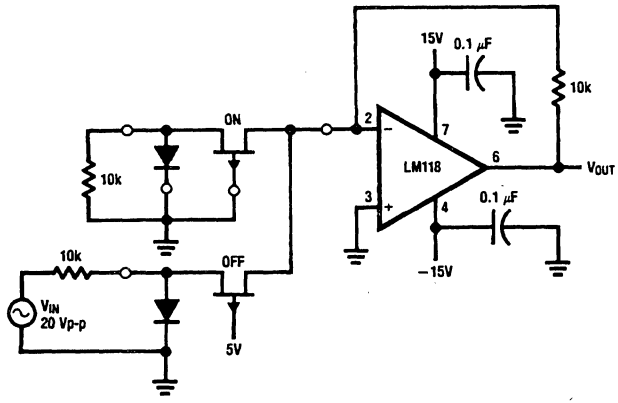
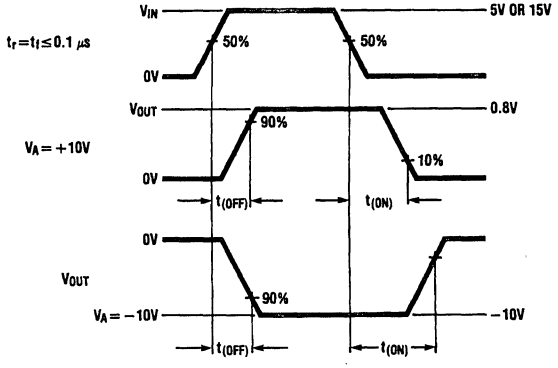
Cross Talk Test Circuit



TL/H/5166–3

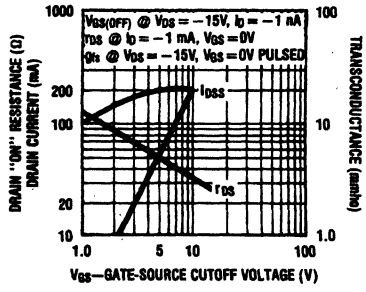
Switching Time Waveforms



TL/H/5166–5

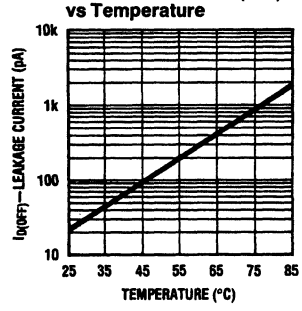
Typical Performance Characteristics

Parameter Interaction



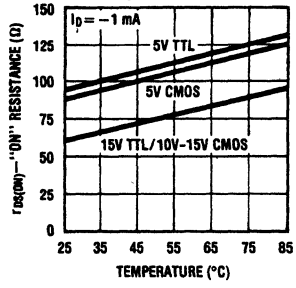
TL/H/5166–6

Leakage Current, $I_{D(OFF)}$ vs Temperature



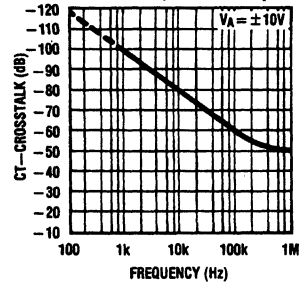
TL/H/5166–7

"ON" Resistance, $r_{DS(ON)}$ vs Temperature



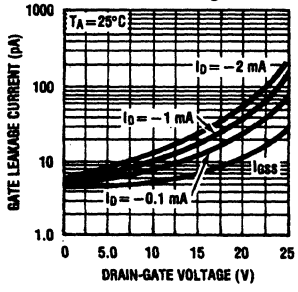
TL/H/5166–8

Cross Talk, CT vs Frequency



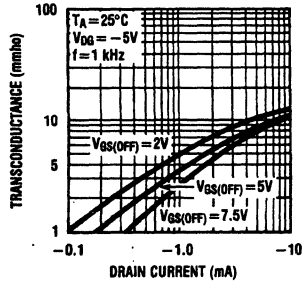
TL/H/5166–9

Leakage Current vs Drain-Gate Voltage



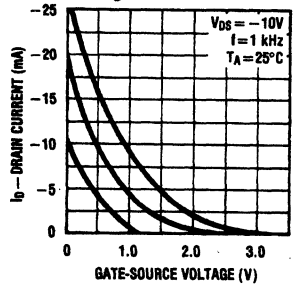
TL/H/5166–10

Transconductance vs Drain Current



TL/H/5166–11

Drain Current vs Bias Voltage



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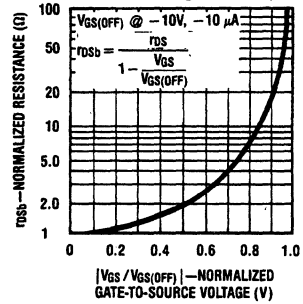
Normalized Drain Resistance vs Bias Voltage



TL/H/5166–13

Applications Information

THEORY OF OPERATION

The AH5020 analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL.

If only one of the two switches in each package is used to apply an input signal to the input of an op amp, the other switch FET can be placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = -\frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 2Ω resulting in a gain accuracy of 0.02% (for R1 = R2 = 10 kΩ).

NOISE IMMUNITY

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With V_{IN} = 15V and the V_A = 10V, the source of Q1 is clamped to about 0.7V by the diode (V_{GS} = 14.3V) ensuring that ac signals imposed on the 10V will not gate the FET "ON".

SELECTION OF GAIN SETTING RESISTORS

Since the AH5020 analog switches are operated current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*, $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than 1/10 of I_{DSS}.

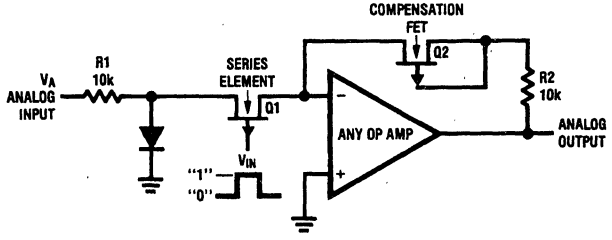
Combining the criteria from the above discussion yields:

$$R1_{(MIN)} \geq \frac{V_{A(MAX)}\, A_D}{I_{G(ON)}} \quad (2a)$$

or:

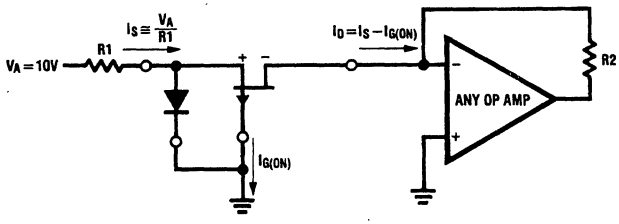
$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \quad (2b)$$

whichever is larger.



TL/H/5166-14

FIGURE 1. Use of Compensation FET



TL/H/5166-15

FIGURE 2. On Leakage Current, $I_{G(ON)}$

Applications Information (Continued)

Where $V_{A(MAX)}$ = Peak amplitude of the analog input signal
A_D = Desired accuracy
$I_{G(ON)}$ = Leakage at a given I_S
I_{DSS} = Saturation current of the FET switch = 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, 0°C ≤ T_A ≤ 85°C. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{10V}{\frac{20\ mA}{10}} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\mu A$ at 85°C for the AH5020. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3*, the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\ A_D}{(N)\ I_{D(OFF)}}$$

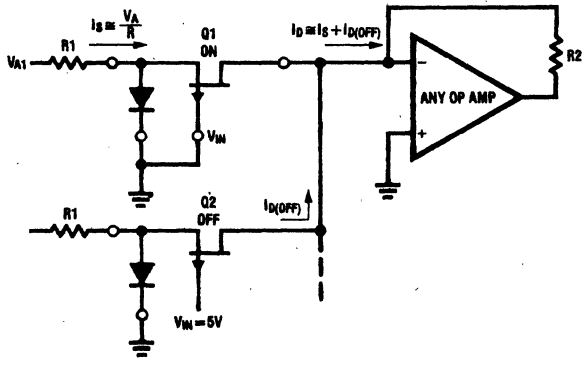
Where $V_{A(MIN)}$ = Minimum value for the analog input signal
A_D = Desired accuracy
N = Number of channels
$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)} \leq$ 10 nA at 85°C for the AH5020. $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp — all of which should be considered in setting the overall gain accuracy of the circuit.



TL/H/5166–16

FIGURE 3. Off Leakage Current, $I_{D(OFF)}$

Applications Information (Continued)

TTL COMPATIBILITY

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the AH5020, a pull-up resistor, R_{EXT} of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4*.

DEFINITION OF TERMS

The terms referred to in the electrical characteristics tables are as defined in *Figure 5*.

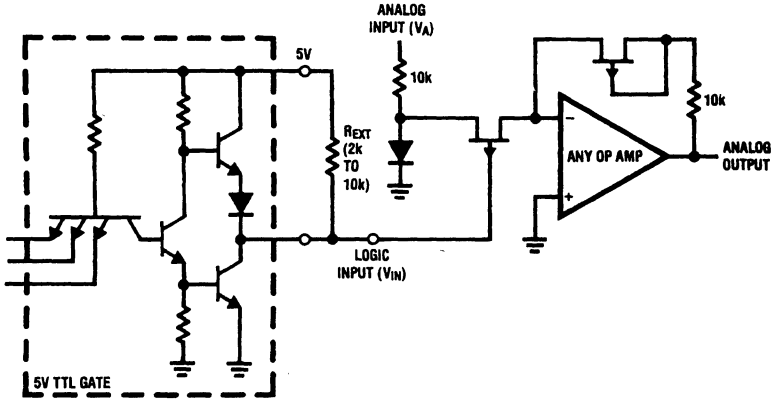


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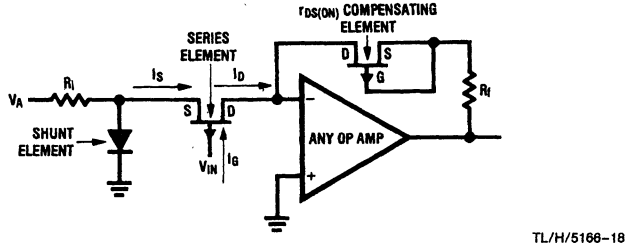
FIGURE 4. Interfacing with +5V TTL

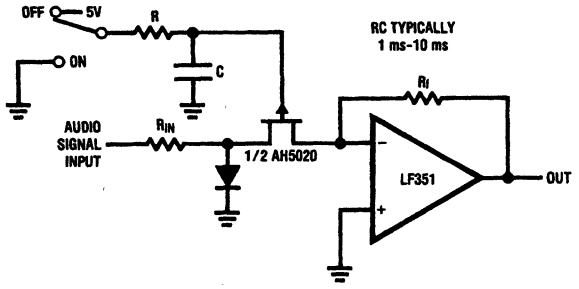


TL/H/5166–18

FIGURE 5. Definition of Terms

Typical Applications

Deglitched Switch for Noiseless Audio Switching



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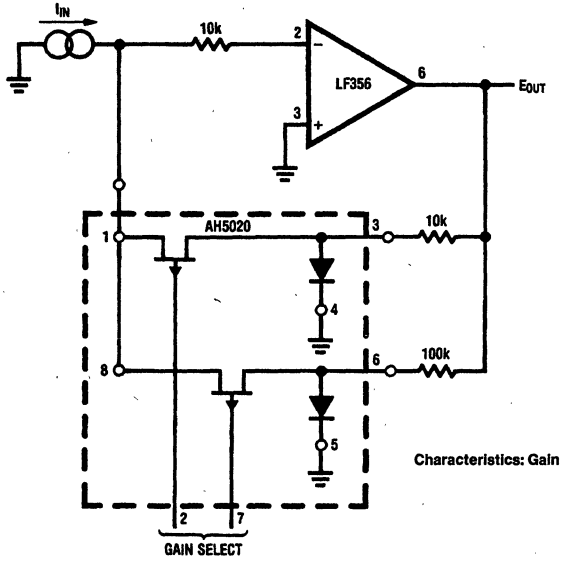
Gain Programmable Amplifier



Characteristics: Gain $= \frac{-E_{OUT}}{I_{IN}} = R_{FS}$

TL/H/5166-20

National Semiconductor

LM1037 Dual Four-Channel Analog Switch

General Description

The LM1037 is a dual, electronically controlled, analog switch with an internal muting facility. Any one of four stereo signal sources may be selected by means of four control inputs.

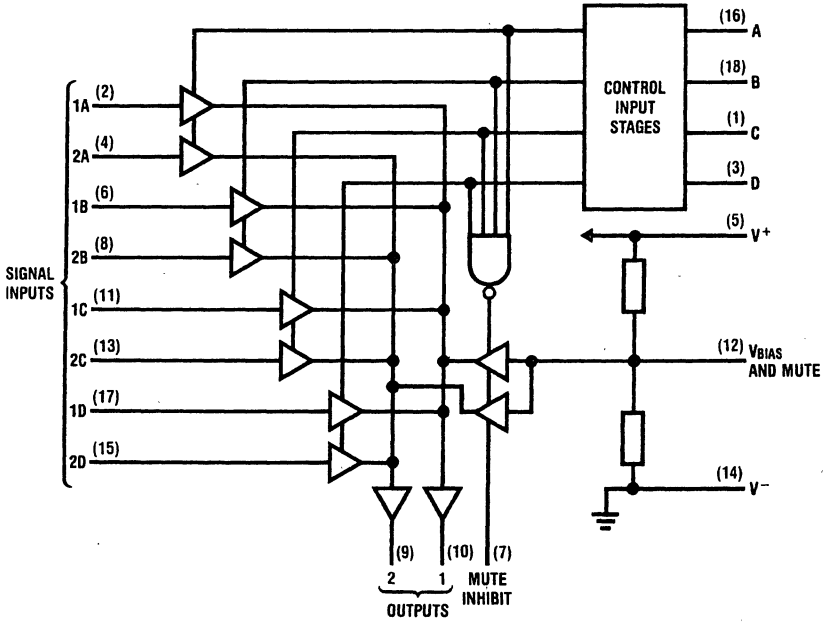
Its features make it ideal for stereo source selection in audio equipment and for use in a wide range of industrial, automotive, multiplexing or sampling applications.

An additional pin is included to allow parallel connection of two or more integrated circuits.

Features

- Wide supply voltage range, 5V–28V
- Low distortion, 0.04% typical
- Low noise, typically 5 μV
- High input impedance
- Low output impedance
- TTL compatible control inputs
- Very low control current

Block Diagram



TL/H/5199–1

Order Package Number LM1037
See NS Package N18A

Absolute Maximum Ratings

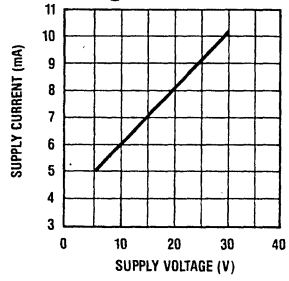
Supply Voltage	28V	Storage Temperature Range	−65°C to +150°C
Pin 7 Input Current	5 mA	Power Dissipation (Note 1)	1.3W
Operating Temperature Range	−20°C to +70°C	Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = 12V$, $T_A = 25°C$

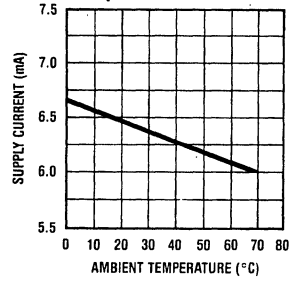
Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range		5		28	V
Supply Current	$V_{SUPPLY} = 12V$		6.4	8.5	mA
	$V_{SUPPLY} = 28V$		10	14	mA
Voltage Gain		−0.7	0	0.7	dB
Signal Handling (Notes 2, 6)	$V_{SUPPLY} = 12V$	2.8	3.0		Vrms
Small-Signal Bandwidth			300		kHz
Distortion THD	$V_{SIGNAL} = 1$ Vrms @ 1 kHz		0.04	0.1	%
Noise Voltage at Output	CCIR/ARM $R_S = 2k$		5	12	μV
Channel Separation (Note 4)	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−70	−95		dB
Relative Output in Muted State	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−70	−90		dB
Output Impedance			10		Ω
Signal Input Impedance			30		MΩ
Logic Low Input Level				0.8	V
Logic High Input Level		2.0		50	V

Typical Performance Characteristics ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

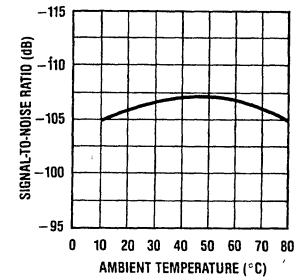
Supply Current vs Supply Voltage



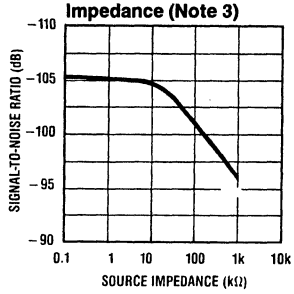
Supply Current vs Temperature



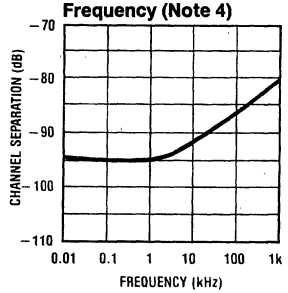
Signal-to-Noise vs Temperature (Note 3)



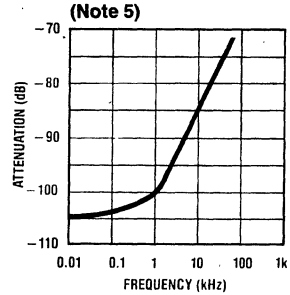
Signal-to-Noise vs Source Impedance (Note 3)



Channel Separation vs Frequency (Note 4)



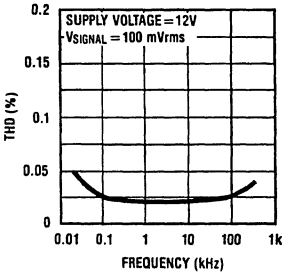
Attenuation of Unselected Inputs vs Frequency (Note 5)



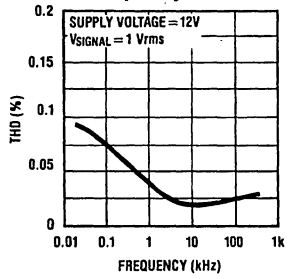
TL/H/5199–2

Typical Performance Characteristics (Continued) ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

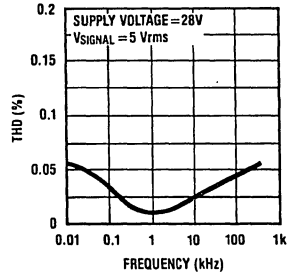
Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency

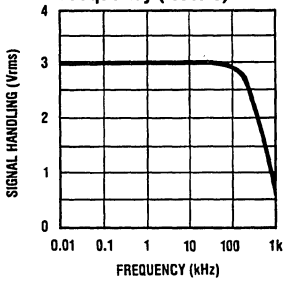


Total Harmonic Distortion vs Frequency



TL/H/5199–3

Signal Handling vs Frequency (Note 6)



TL/H/5199–4

Note 1: Above $T_A = 25°C$ derate based on T_J max = 150°C and $\theta_{JA} = 90°C/W$.

Note 2: The instantaneous maximum voltage difference between any two input pins of one channel is 9.6V. Voltages in excess of this level may cause increased distortion and degraded channel separation.

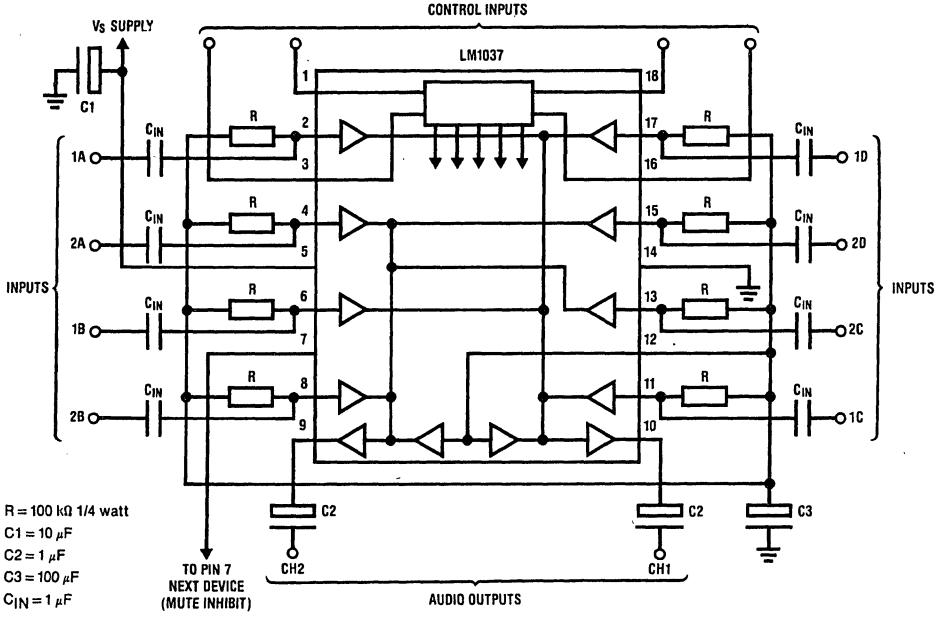
Note 3: Signal-to-noise measurement referred to a 1 Vrms input signal using a CCIR filter referenced to 2 kHz and an average responding meter.

Note 4: The level of output signal of a selected undriven amplifier with respect to the output level of a selected driven amplifier. For test purposes, signal is applied to only one input and all other inputs are decoupled to eliminate stray pick-up through external components. Channel separation is then defined as the ratio of signal levels of the two output pins.

Note 5: For test purposes, signals are connected to three unselected input pins of one channel group and all other inputs are decoupled to eliminate stray pick-up through external components.

Note 6: Supply voltage 12V; signal handling defined at 1% distortion, 1 kHz.

Typical Application



TL/H/5199–5

Truth Tables

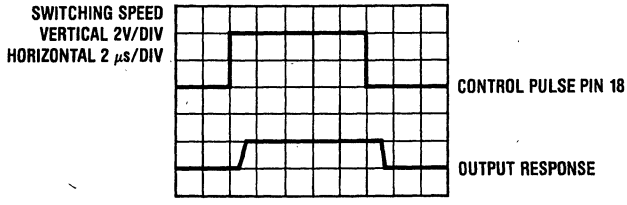
LM1037

Channel selection is achieved by the application of DC voltages to the control pins. Unselected control pins should be held low.

DC Control Pin in HIGH State	Input Pair Switched to Output Pins (10, 9)	
16	A	(2,4)
18	B	(6,8)
1	C	(11,13)
3	D	(17,15)
None	Mute	(12)

Low switching level (V_L) < 0.8V

High switching level (V_H) > 2.0V and up to 50V



TL/H/5199–6

2 DEVICES CONNECTED IN PARALLEL

To increase the channel switching capacity, two or more devices can be connected together by the direct coupling of the mute inhibit pin 7 and the output pins 9 and 10. Only one output capacitor is required for each common output.

	DC Control Pin in HIGH State	Input Pair Switched to Output Pins (10,9)	
Device Number 1	16	A	(2,4)
	18	B	(6,8)
	1	C	(11,13)
	3	D	(17,15)
Device Number 2	16	A	(2,4)
	18	B	(6,8)
	1	C	(11,13)
	3	D	(17,15)
	None	Mute	(12)

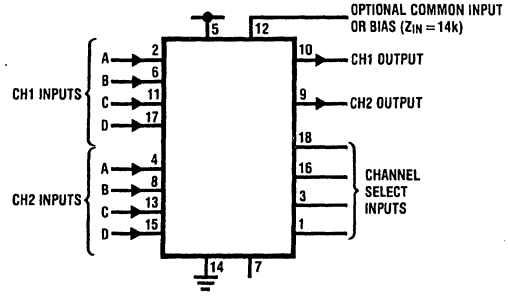
Pin Function Description

Device Pins	Description
Pin 16—Inputs A Select Pin 18—Inputs B Select Pin 1—Inputs C Select Pin 3—Inputs D Select	A high input level selects the corresponding channel. Only one channel should be selected at a time. Unselected channels should have their select inputs at a low level. Open circuit pins represent a high input level.
Pins 2, 6, 11, 17— Inputs for Output 1 (Pin 10) Pins 4, 8, 13, 15— Inputs for Output 2 (Pin 9)	Two sets of four high impedance channel inputs for the connection of signals to be switched.
Pin 12—Mute Bias Level	The DC level at this pin is applied to the outputs when no input is selected and pin 7 is open. The level is internally set by a 25 kΩ and 33 kΩ potential divider at 0.6 V_S. This level may be adjusted by means of external resistors. Pin 12 may also be used as an additional common input in which case this signal is present on both outputs when no control input is applied.
Pin 7—Mute Inhibit Input	With this pin unconnected and no channel selection input is present; the mute level at pin 12 is applied to the outputs. With pin 7 grounded and no channel selection input present, the device output emitter-followers are disabled allowing parallel connection to other device outputs. This pin is a current input and any current applied should be limited to 5 mA maximum. Pin 7 of several devices may be directly connected for parallel operation.
Pin 9—Output 2 Pin 10—Output 1	These are common output pins for each channel. There are three possible output conditions: 1) Signal selected from 1 of 4 inputs. 2) Mute level output. 3) Device not selected—internal 6 kΩ pull-down resistors to ground.
Pin 5	Positive supply voltage.
Pin 14	Negative or ground supply voltage.

Application Hints

The basic circuit arrangement with minimum external components for use with DC coupled signals is shown in *Figure 1*. This arrangement may be used in a normal signal selection system or in the feedback path of DC coupled amplifiers for example to make a simple dual programmable power supply. By switching feedback connections dual programmable gain or frequency response amplifiers may be obtained.

For switching between signal sources in stereo systems the LM1037 may be connected as shown in the typical application circuit. The input bias is obtainable from pin 12 or an alternative source may be used. If split supply operation is required, pin 12 may be grounded and the signals referenced to ground.

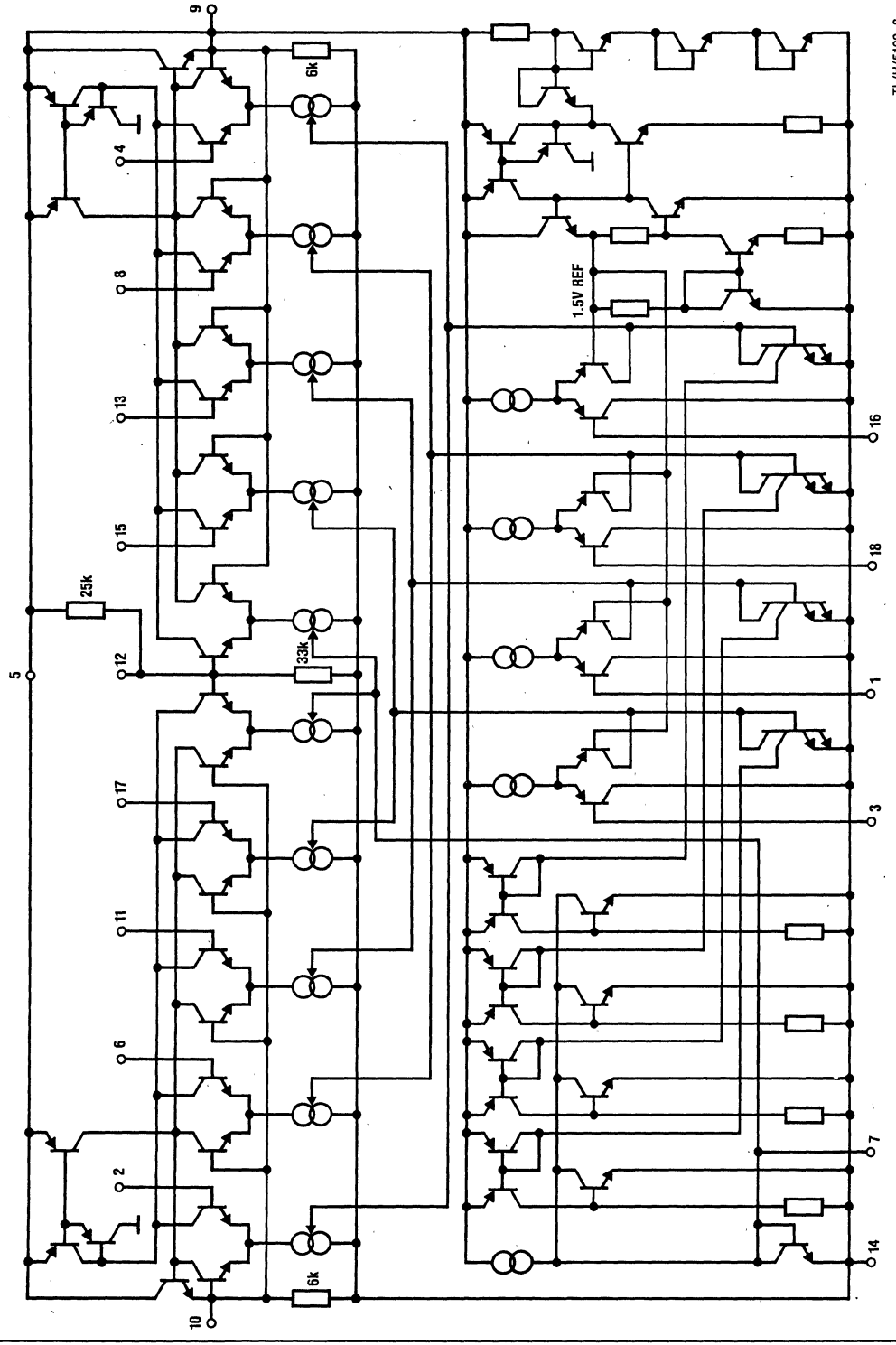


TL/H/5199–7

DC coupled signals $1.2V < V_{IN} < V_S - 1V$

FIGURE 1

Simplified Circuit Schematic



National Semiconductor

LM1038 Dual Four-Channel Analog Switch

General Description

The LM1038 is a dual, electronically controlled, four-channel analog switch with an internal muting facility.

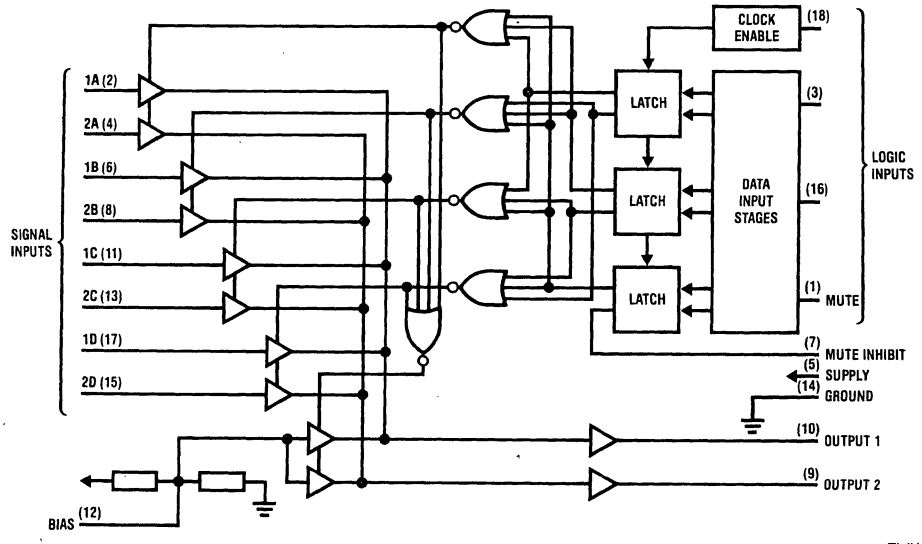
Its features make it ideal for stereo source selection in audio equipment and for use in a wide range of industrial, automotive, multiplexing or sampling applications.

Channel selection is achieved via two logic data pins with clock enabled latches. Muting is also selectable under clock control.

Features

- Wide supply voltage range, 5V-28V
- Low distortion, 0.04% typical
- High input impedance
- Low output impedance
- TTL compatible control Inputs
- Very low control current
- 2 control pins accept BCD input pulses
- Clock enable input may be strobed from a bus

Block Diagram



TL/H/5200–1

Order Number LM1038
See NS Package N18A

Absolute Maximum Ratings

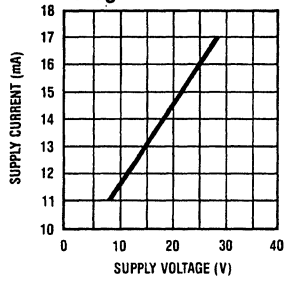
Supply Voltage	28V	Storage Temperature Range	−65°C to +150°C
Pin 7 Input Current	5 mA	Power Dissipation (Note 1)	1.3W
Operating Temperature Range	−20°C to +70°C	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_S = 12V$, $T_A = 25°C$.

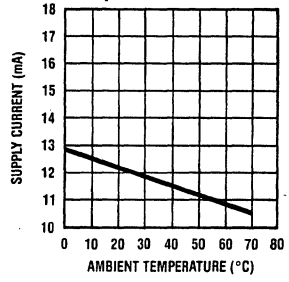
Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range		5		28	V
Supply Current	$V_{SUPPLY} = 12V$		12	17	mA
	$V_{SUPPLY} = 28V$		17	28	mA
Voltage Gain		−0.7	0	**0.7**	dB
Signal Handling (Notes 2, 6)	$V_{SUPPLY} = 12V$	2.8	3.0		Vrms
Small-Signal Bandwidth			300		kHz
Distortion THD	$V_{SIGNAL} = 1$ Vrms @ 1 kHz		0.04	**0.1**	%
Noise Voltage at Output	CCIR/ARM $R_S = 2k$		5	**12**	μV
Channel Separation (Note 4)	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−70	−95		dB
Relative Output in Muted State	$V_{SIGNAL} = 1$ Vrms @ 1 kHz	−70	−90		dB
Output Impedance			10		Ω
Signal Input Impedance			30		MΩ
Logic Low Input Level				**0.8**	V
Logic High Input Level		2.0		50	V

Typical Performance Characteristics ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

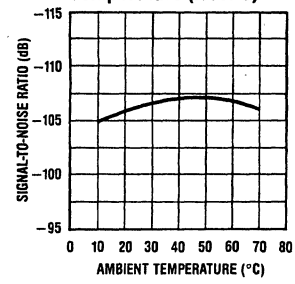
Supply Current vs Supply Voltage



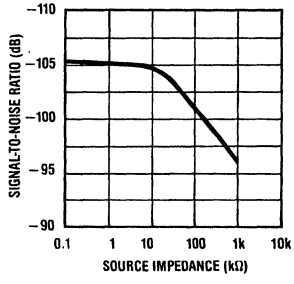
Supply Current vs Temperature



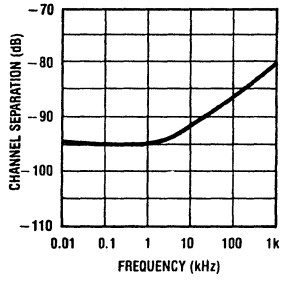
Signal-to-Noise vs Temperature (Note 3)



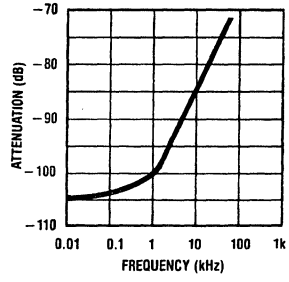
Signal-to-Noise vs Source Impedance (Note 3)



Channel Separation vs Frequency (Note 4)



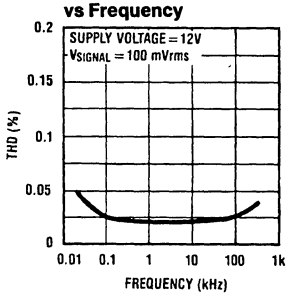
Attenuation of Unselected Inputs vs Frequency (Note 5)



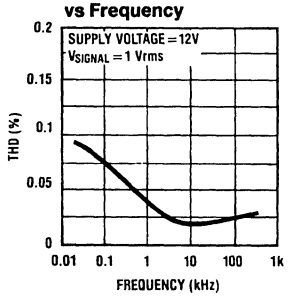
TL/H/5200–2

Typical Performance Characteristics (Continued) ($V_S = 12V$, $T_A = 25°C$ unless otherwise noted)

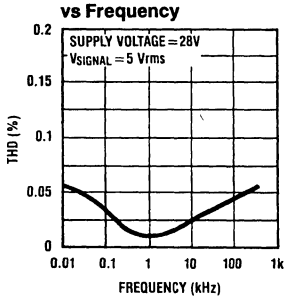
Total Harmonic Distortion vs Frequency



Total Harmonic Distortion vs Frequency

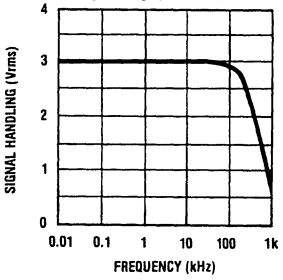


Total Harmonic Distortion vs Frequency



TL/H/5200–3

Signal Handling vs Frequency (Note 6)



TL/H/5200–4

Note 1: Above $T_A = 25°C$ derate based on T_J max = 150°C and $\theta_{JA} = 90°C/W$.

Note 2: The instantaneous maximum voltage difference between any two input pins of one channel is 9.6V. Voltages in excess of this level may cause increased distortion and degraded channel separation.

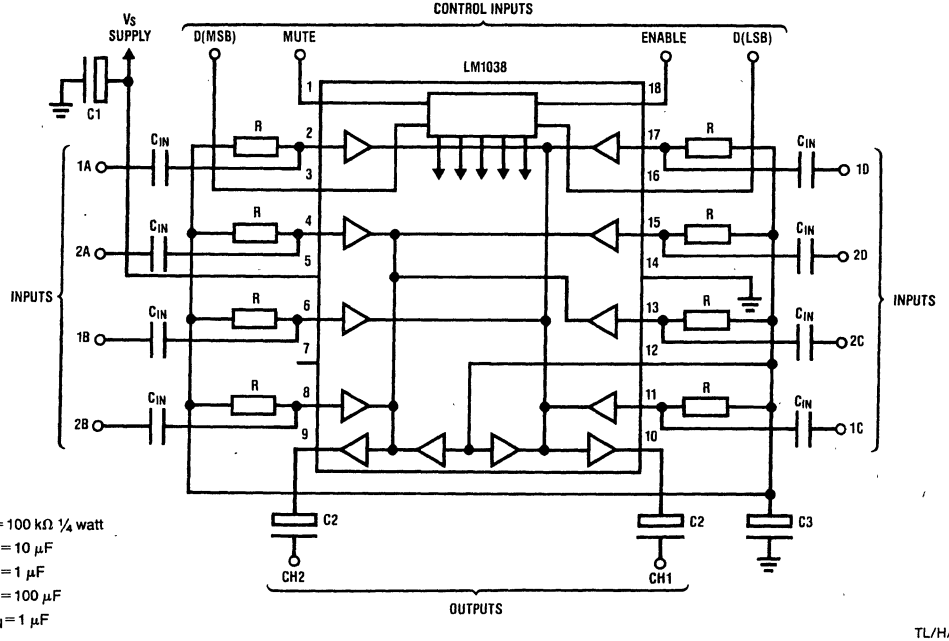
Note 3: Signal-to-noise measurement referred to a 1 Vrms input signal using a CCIR filter referenced to 2 kHz and an average responding meter.

Note 4: The level of output signal of a selected undriven amplifier with respect to the output level of a selected driven amplifier. For test purposes, signal is applied to only one input and all other inputs are decoupled to eliminate stray pick-up through external components. Channel separation is then defined as the ratio of signal levels of the two output pins.

Note 5: For test purposes, signals are connected to three unselected input pins of one channel group and all other inputs are decoupled to eliminate stray pick-up through external components.

Note 6: Supply voltage 12V; signal handling defined at 1% distortion, 1 kHz.

Typical Application



R = 100 kΩ ¼ watt
C1 = 10 μF
C2 = 1 μF
C3 = 100 μF
C_{IN} = 1 μF

TL/H/5200–5

Truth Table

Logic Inputs				Input Pin Selected	
Latch Enable Pin 18	Mute Pin 1	Channel Select Data Pin 3	Pin 16	Output 1 Pin 10	Output 2 Pin 9
1	0	0	0	D Pin 17	D Pin 15
1	0	0	1	A Pin 2	A Pin 4
1	0	1	0	B Pin 6	B Pin 8
1	0	1	1	C Pin 11	C Pin 13
1	1	X	X	Pin 12 Mute Bias	
0	X	X	X	Inputs Previously Selected are Retained	

Low (0) < 0.8V
High (1) > 2.0V, up to 50V

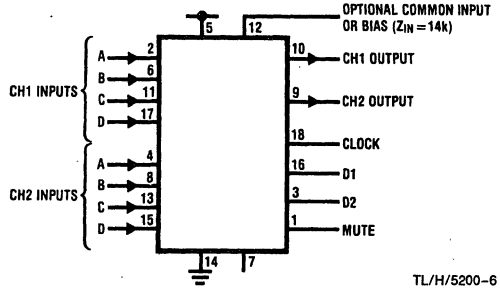
Pin Function Description

Device Pins	Description
Pin 1—Mute	A high level on this input will select the muted condition (outputs = pin 12 voltage) if the latch enable input is low provided pin 7 (mute enable) is open.
Pin 3—Channel Address (MSB) Pin 16—Inputs (LSB)	Binary information on these pins selects the required channel if the mute select input, pin 1, is low.
Pin 18—Latch Enable	With a high level on this pin the data on the channel select pins controls the channel enabled. When the input is low the channel select data is latched. The mute input pin 1 is also controlled by this input. A minimum enable pulse width of typically 3 μs is required.
Pins 2, 6, 11, 17— Inputs for Output 1 (Pin 10) Pins 4, 8, 13, 15— Inputs for Output 2 (Pin 9)	Two sets of four high impedance channel inputs for the connection of signals to be switched.
Pin 12—Mute Bias Level	The DC level at this pin is applied to the outputs when the mute input, pin 1, is activated. The level is internally set by a 25 kΩ and 33 kΩ potential divider to 0.6 V_S. This level may be adjusted by means of external resistors. Pin 12 may also be used as an additional common signal input.
Pin 7—Mute Inhibit	This is a current input and any control current into this pin must be externally limited to 5 mA maximum. With this pin open the mute input, pin 1, is enabled. With a current into this pin the mute facility is disabled and with no signal channel selected the output emitter-followers are disabled.
Pin 9—Output 2 Pin 10—Output 1	These are common output pins for each channel. There are three possible output conditions: 1) Signal selected from 1 of 4 inputs. 2) Mute level output. 3) Device not selected—internal 6 kΩ pull-down resistors to ground.
Pin 5	Positive supply voltage.
Pin 14	Negative or ground supply voltage.

Application Hints

The basic circuit arrangement with minimum external components for use with DC coupled signals is shown in *Figure 1*. This arrangement may be used in a normal signal selection system or in the feedback path of DC coupled amplifiers for example to make a simple dual programmable power supply. By switching feedback connections dual programmable gain or frequency response amplifiers may be obtained.

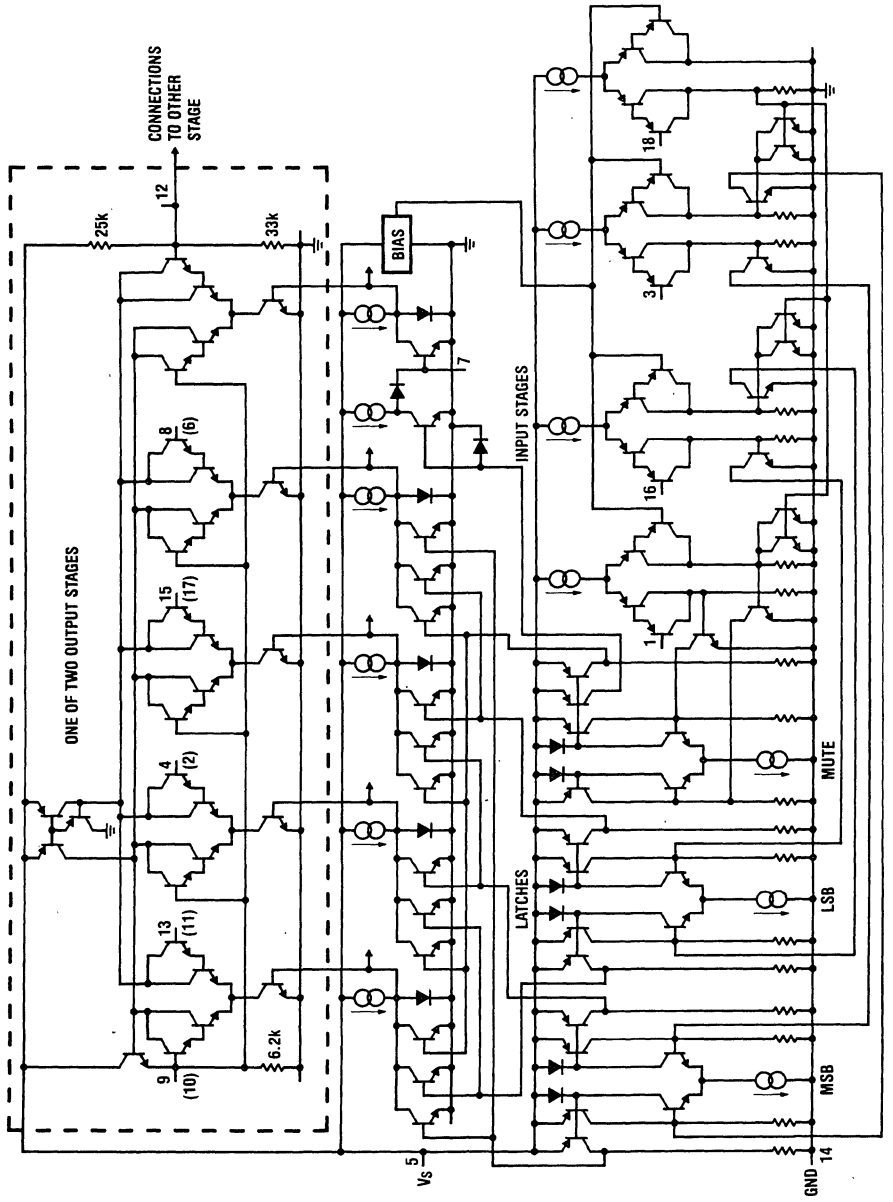
For switching between signal sources in stereo systems the LM1038 may be connected as shown in the typical application circuit. The input bias is obtainable from pin 12 or an alternative source may be used. If split supply operation is required, pin 12 may be grounded and the signals referenced to ground.



DC coupled signals $1.2V < V_{IN} < V_S - 1V$

FIGURE 1

Equivalent Schematic Diagram



TL/H/5200–7

Section 7

Sample and Hold

Sample and Hold

Section Contents

Standard Sample and Hold

There were no changes to Datasheets within this section.

Section 8

Sensors

Section Contents

Temperature

National Semiconductor

PRELIMINARY

LM34/LM34A, LM34C/LM34CA, LM34D Precision Fahrenheit Temperature Sensors

General Description

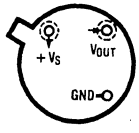
The LM34 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Fahrenheit temperature. The LM34 thus has an advantage over linear temperature sensors calibrated in degrees Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Fahrenheit scaling. The LM34 does not require any external calibration or trimming to provide typical accuracies of ±½°F at room temperature and ±1½°F over a full −50 to +300°F temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM34's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies or with plus and minus supplies. As it draws only 70 μA from its supply, it has very low self-heating, less than 0.2°F in still air. The LM34 is rated to operate over a −50° to +300°F temperature range, while the LM34C is rated for a −40° to +230°F range (0°F with improved accuracy). The LM34 series is available packaged in hermetic TO-46 transistor packages, while the LM34C is also available in the plastic TO-92 transistor package. The LM34 is a complement to the LM35 (Centigrade) temperature sensor.

Features

- Calibrated directly in degrees Fahrenheit
- Linear + 10.0 mV/°F scale factor
- 1.0°F accuracy guaranteed (at +77°F)
- Rated for full −50° to +300°F range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 5 to 30 volts
- Less than 70 μA current drain
- Low self-heating, 0.18°F in still air
- Nonlinearity only ±0.5°F typical
- Low-impedance output, 0.4Ω for 1 mA load

Connection Diagrams

TO-46
Metal Can Package*



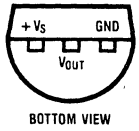
BOTTOM VIEW

TL/H/6685-1

*Case is connected to negative pin.

Order Number LM34H
See NS Package H03H

TO-92
Plastic Package

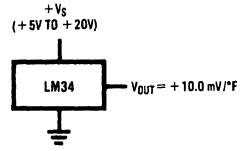


BOTTOM VIEW

TL/H/6685-2

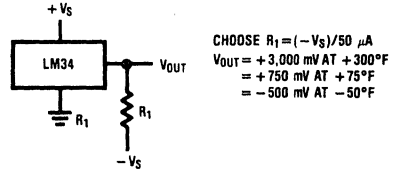
Order Number LM34Z
See NS Package Z03A

Typical Applications



TL/H/6685-3

FIGURE 1. Basic Fahrenheit Temperature Sensor (+5° to +300°F)



TL/H/6685-4

FIGURE 2. Full-Range Fahrenheit Temperature Sensor

S 8

National Semiconductor

PRELIMINARY

LM35/LM35A, LM35C/LM35CA, LM35D Precision Centigrade Temperature Sensors

General Description

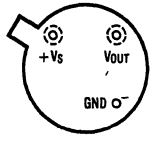
The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 μA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C is also available in the plastic TO-92 transistor package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 μA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Connection Diagrams

TO-46
Metal Can Package*



BOTTOM VIEW

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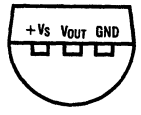
*Case is connected to negative pin

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package H03H

TO-92
Plastic Package



BOTTOM VIEW

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Order Number LM35CZ, or LM35DZ
See NS Package Z03A

Typical Applications

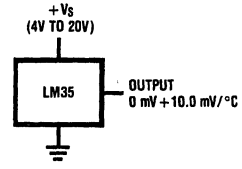

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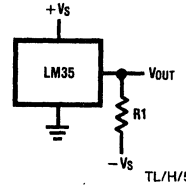
FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)



Choose $R_1 = -VS/50\ \mu A$

$V_{OUT} = +1{,}500$ mV at +150°C
$= +250$ mV at +25°C
$= -550$ mV at −55°C

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FIGURE 2. Full-Range Centigrade Temperature Sensor

Absolute Maximum Ratings

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp., TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
Lead Temp. (Soldering, 10 seconds):	
TO-46 Package,	300°C
TO-92 Package,	260°C

Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)

LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics (Note 1) (Note 6)

Parameter	Conditions	LM35A			LM35CA (Note 10)			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy (Note 7)	$T_A=+25°C$	±0.2	±0.5		0.2	±0.5		°C
	$T_A=-10°C$	±0.3			0.3		1.0	°C
	$T_A=T_{MAX}$	±0.4	1.0		0.4	1.0		°C
	$T_A=T_{MIN}$	±0.4	1.0		0.4		1.5	°C
Nonlinearity (Note 8)	$T_{MIN}\le T_A\le T_{MAX}$	**0.18**		**0.35**	**0.15**		**0.3**	°C
Sensor Gain (Average Slope)	$T_{MIN}\le T_A\le T_{MAX}$	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°C
Load Regulation (Note 3) $0\le I_L\le 1$ mA	$T_A=+25°C$	0.4	1.0		0.4	1.0		mV/mA
	$T_{MIN}\le T_A\le T_{MAX}$	**0.5**		**3.0**	**0.5**		**3.0**	mV/mA
Line Regulation (Note 3)	$T_A=+25°C$	0.01	0.05		0.01	0.05		mV/V
	$4V\le V_S\le 30V$	**0.02**		**0.1**	**0.02**		**0.1**	mV/V
Quiescent Current (Note 9)	$V_S=+5V$, +25°C	56	67		56	67		µA
	$V_S=+5V$	**105**		**131**	**91**		**114**	µA
	$V_S=+30V$, +25°C	56.2	68		56.2	68		µA
	$V_S=+30V$	**105.5**		**133**	**91.5**		**116**	µA
Change of Quiescent Current (Note 3)	$4V\le V_S\le 30V$, +25°C	0.2	1.0		0.2	1.0		µA
	$4V\le V_S\le 30V$	**0.5**		**2.0**	**0.5**		**2.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.5**	**+0.39**		**+0.5**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, $I_L=0$	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	$T_J=T_{MAX}$, for 1000 hours	±0.08			0.08			°C

Note 1: Unless otherwise noted, these specifications apply: $-55°C\le T_J\le +150°C$ for the LM35 and LM35A; $-40°\le T_J\le +110°C$ for the LM35C and LM35CA; and $0°\le T_J\le +100°C$ for the LM35D. $V_S=+5Vdc$ and $I_{LOAD}=50$ µA, in the circuit of *Figure 2.* These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1.* Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 440°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient.

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Electrical Characteristics (Note 1) (Note 6) (Continued)

Parameter	Conditions	LM35			LM35C, LM35D			Units (Max.)
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	
Accuracy, LM35, LM35C (Note 7)	$T_A = +25°C$	±0.4	±1.0		0.4	±1.0		°C
	$T_A = -10°C$	0.5			0.5		1.5	°C
	$T_A = T_{MAX}$	0.8	1.5		0.8		1.5	°C
	$T_A = T_{MIN}$	0.8		1.5	0.8		2.0	°C
Accuracy, LM35D (Note 7)	$T_A = +25°C$				0.6	±1.5		°C
	$T_A = T_{MAX}$				0.9		2.0	°C
	$T_A = T_{MIN}$				0.9		2.0	°C
Nonlinearity (Note 8)	$T_{MIN} \le T_A \le T_{MAX}$	**0.3**		**0.5**	**0.2**		**0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN} \le T_A \le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0 \le I_L \le 1$ mA	$T_A = +25°C$	0.4	2.0		0.4	2.0		mV/mA
	$T_{MIN} \le T_A \le T_{MAX}$	**0.5**		**5.0**	**0.5**		**5.0**	mV/mA
Line Regulation (Note 3)	$T_A = +25°C$	0.01	0.1		0.01	0.1		mV/V
	$4V \le V_S \le 30V$	**0.02**		**0.2**	**0.02**		**0.2**	mV/V
Quiescent Current (Note 9)	$V_S = +5V, +25°C$	56	80		56	80		µA
	$V_S = +5V$	**105**		**158**	**91**		**138**	µA
	$V_S = +30V, +25°C$	56.2	82		56.2	82		µA
	$V_S = +30V$	**105.5**		**161**	**91.5**		**141**	µA
Change of Quiescent Current (Note 3)	$4V \le V_S \le 30V, +25°C$	0.2	2.0		0.2	2.0		µA
	$4V \le V_S \le 30V$	**0.5**		**3.0**	**0.5**		**3.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39)**		**+0.7**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, $I_L = 0$	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	$T_J = T_{MAX}$, for 1000 hours	0.08			0.08			°C

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature. (expressed in °C)

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

Note 10: Consult factory for availability of LM35CAZ.

Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature. The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

Temperature Rise of LM35 Due To Self-heating (Thermal Resistance)

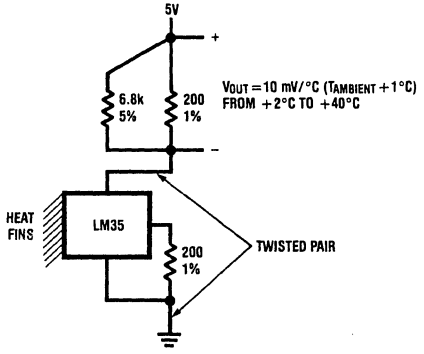
	TO-46, no heat sink	TO-46, small heat fin*	TO-92, no heat sink	TO-92, small heat fin**
Still air	400°C/W	100°C/W	180°C/W	140°C/W
Moving air	100°C/W	40°C/W	90°C/W	70°C/W
Still oil	100°C/W	40°C/W	90°C/W	70°C/W
Stirred oil	50°C/W	30°C/W	45°C/W	40°C/W
(Clamped to metal, Infinite heat sink)	(24°C/W)			

* Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.

** TO-92 package glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

Typical Applications (Continued)

Two-Wire Remote Temperature Sensor (Grounded Sensor)



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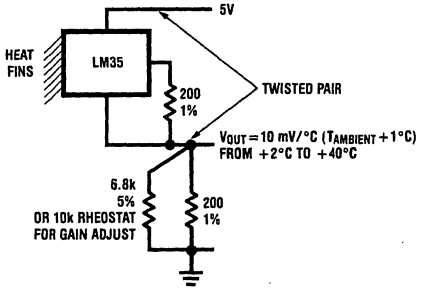
Two-Wire Remote Temperature Sensor (Output Referred to Ground)



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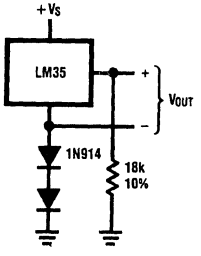
Temperature Sensor, Single Supply, −55° to +150°C



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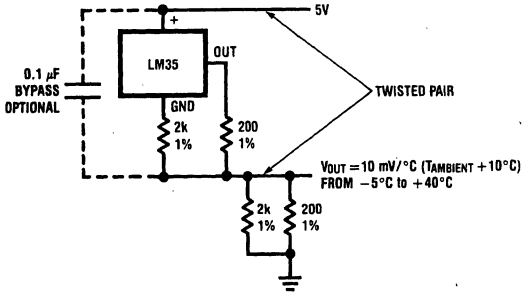
Typical Applications (Continued)

Two-Wire Remote Temperature Sensor (Output Referred to Ground)



0.1 μF bypass, optional.

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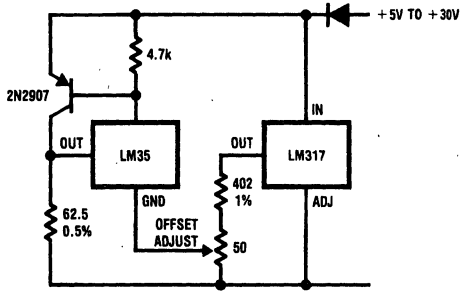
4-To-20 mA Current Source (0°C to + 100°C)



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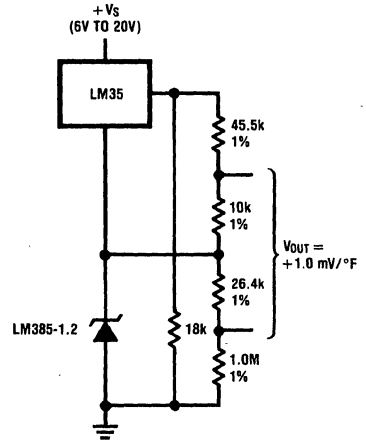
Fahrenheit Thermometer



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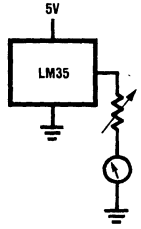
Centigrade Thermometer (Analog Meter)



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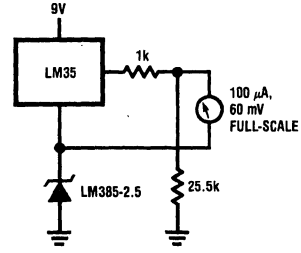
Expanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)



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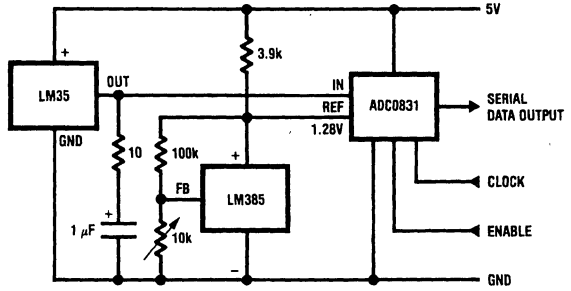
Typical Applications (Continued)

Temperature To Digital Converter (Serial Output) (+ 128°C Full Scale)



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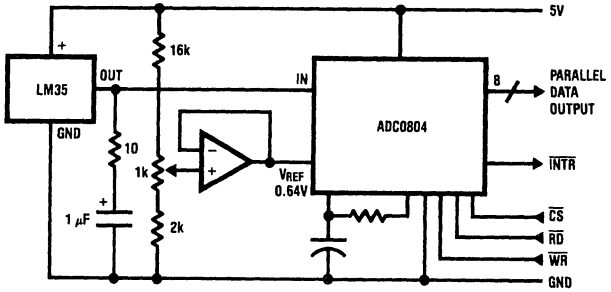
Temperature To Digital Converter (Parallel TRI-STATE® Outputs for Standard Data Bus to μP Interface) (128°C Full Scale)



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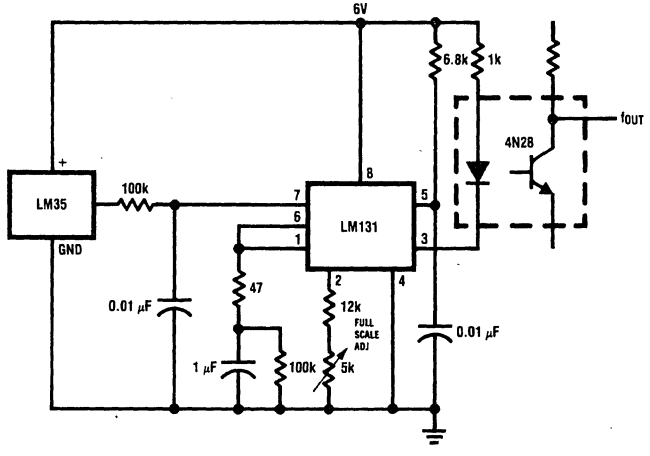
LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to + 150°C; 20 Hz to 1500 Hz)



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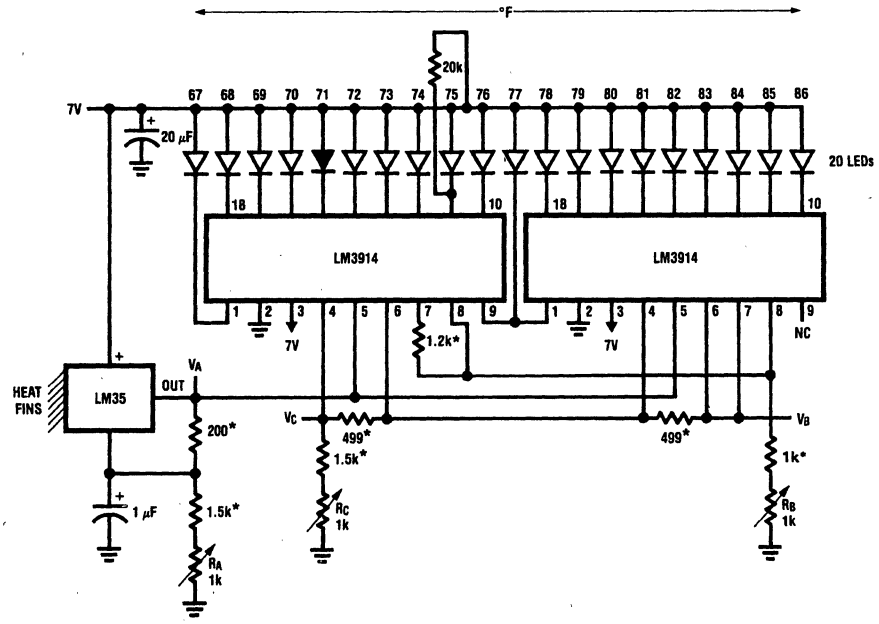
CAPACITIVE LOADS

Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure A*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure B*.

When the LM35 is applied with a 200Ω load resistor as shown under Typical Applications, it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 10Ω in series with 0.1 or 1 μF from output to ground are often useful. These are shown in the above circuits.

Typical Applications (Continued)

Bar-Graph Temperature Display (Dot Mode)



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*=1% or 2% film resistor
-Trim R_B for V_B=3.075V
-Trim R_C for V_C=1.955V
-Trim R_A for V_A=0.075V + 100mV/°C × $T_{ambient}$
-Example, V_A=2.275V at 22°C

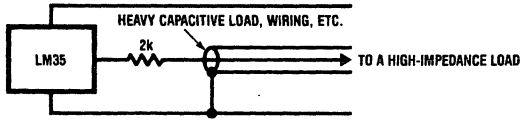

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FIGURE A. LM35 with Decoupling from Capacitive Load

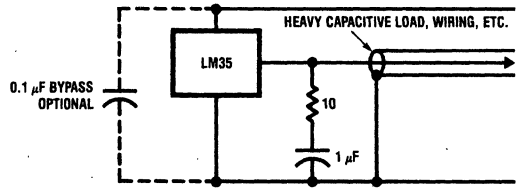

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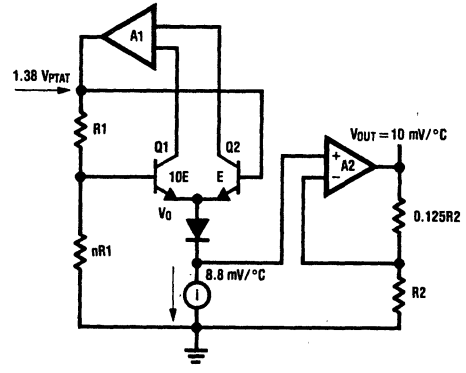
FIGURE B. LM35 with R-C Damper

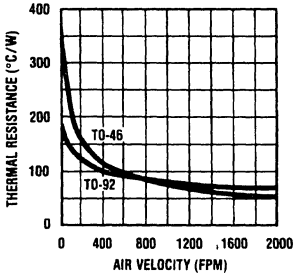
Block Diagram



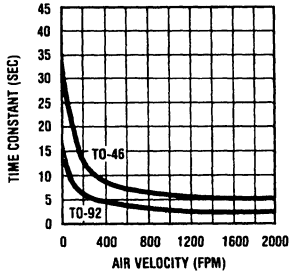
TL/H/5516–21

Typical Performance Characteristics

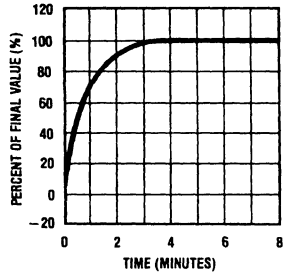
Thermal Resistance Junction to Air



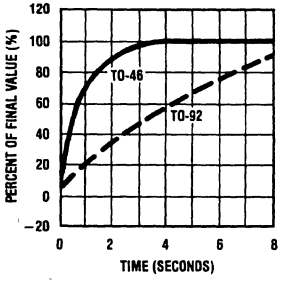
Thermal Time Constant



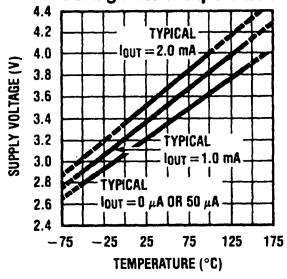
Thermal Response in Still Air



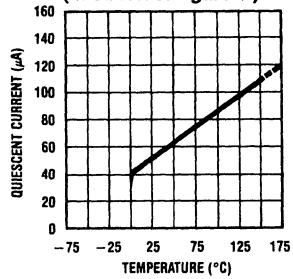
Thermal Response in Stirred Oil Bath



Minimum Supply Voltage vs. Temperature

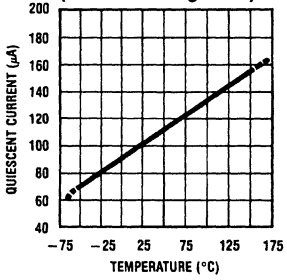


Quiescent Current vs. Temperature (In Circuit of *Figure 1*.)

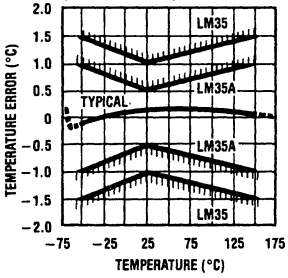


TL/H/5516–17

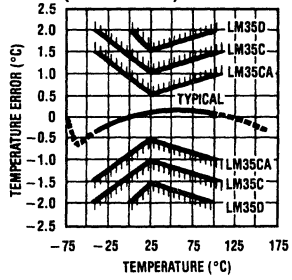
Quiescent Current vs. Temperature (In Circuit of *Figure 2*.)



Accuracy vs. Temperature (Guaranteed)



Accuracy vs. Temperature (Guaranteed)



TL/H/5516–18

S 8

Section 9

Filters

Section Contents

Monolithic

National Semiconductor

PRELIMINARY

MF4 4th Order Switched Capacitor Butterworth Lowpass Filter

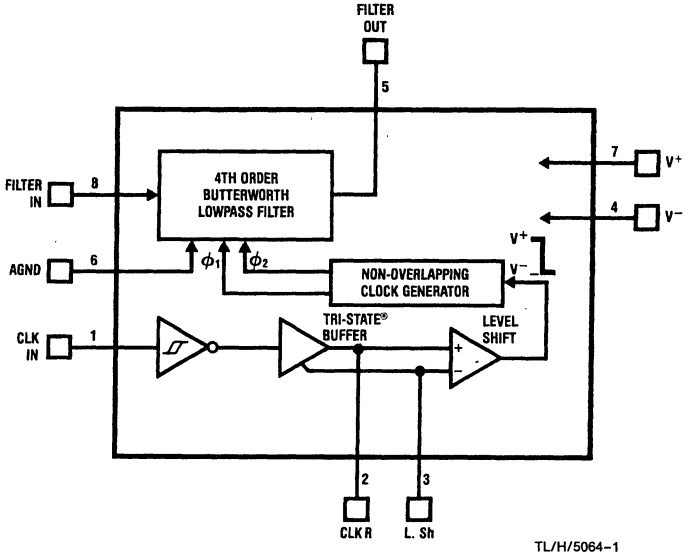
General Description

The MF4 is a versatile, easy to use, precision 4th order Butterworth lowpass active filter. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (MF4-50) or 100 to 1 (MF4-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, a TTL or CMOS logic compatible clock can be directly applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF4 sections for higher order filtering.

Features

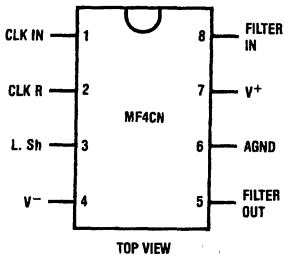
- Low cost
- Easy to use
- No external components
- 8-pin mini-DIP
- Cutoff frequency accuracy of ±0.3%
- Cutoff frequency range of 0.1 Hz to 20 kHz
- 5V to 14V operation
- Cutoff frequency set by external or internal clock

Block and Connection Diagrams



TL/H/5064–1

Dual-In-Line Package



TOP VIEW

TL/H/5064–2

Order Number MF4CN
See NS Package N08E

Absolute Maximum Ratings

Supply Voltage	14V	Storage Temperature	150°C
Power Dissipation	500 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature	0°C to 70°C(MF4CN)		

Electrical Characteristics (Note 7)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units (Limits)
$V^+ = 5V, V^- = -5V$					
Cutoff Frequency Range (f_C) (Note 1)	MF4-50			0.1 20k	Hz (min) Hz (max)
	MF4-100			0.1 10k	Hz (min) Hz (max)
Supply Current	$f_{CLK} = 250$ kHz	2.5	3.5		mA (max)
Clock Feedthrough (Peak-to-Peak)	$T_A = 25°C$ Filter Output	25			mV
$f_{CLK} \leq 250$ kHz (Note 3)					
DC Gain (H_O)	$R_{SOURCE} \leq 2$ kΩ	0.0	±0.15		dB (max)
Clock to Cutoff Frequency Ratio (f_{CLK}/f_C)	$T_A = 25°C$ MF4-50 MF4-100	 49.98 ± 0.3%	 49.98 ± 0.8%	 49.98 ± 0.6%	 (max) (max)
f_{CLK}/f_C Temperature Coefficient	MF4-50 MF4-100	±15			ppm/°C ppm/°C
Stopband Attenuation	At 2 f_C	−25.0	−24.0		dB (min)
DC Offset Voltage	MF4-50 MF4-100	−200 −400			mV mV
Output Swing	$R_L = 5$ kΩ	+4.0 −4.5	+3.5 −4.0		V (min) V (min)
Output Short Circuit Current (Note 6)	$T_A = 25°C$ Source Sink	 50 1.5			 mA mA
Dynamic Range (Note 2)	$T_A = 25°C$ MF4-50 MF4-100	 80 78			 dB dB
Additional Magnitude Response Test Points (Note 4)	$T_A = 25°C$ $f_{CLK} = 250$ kHz				
MF4-50 ($f_C = 5$ kHz) Magnitude at	f = 6000 Hz f = 4500 Hz	−7.57 −1.44	−7.57 ± 0.27 −1.44 ± 0.12		dB (max) dB (max)
MF4-100 ($f_C = 2.5$ kHz) Magnitude at	f = 3000 Hz f = 2250 Hz		±0.2 ±0.1		dB (max) dB (max)

Electrical Characteristics (Note 7) (Continued)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units (Limits)
$V^+ = 2.5V, V^- = -2.5V$					
Cutoff Frequency Range (f_C) (Note 1)	MF4-50			0.1 10k	Hz (min) Hz (max)
	MF4-100			0.1 5k	Hz (min) Hz (max)
Supply Current	$f_{CLK} = 250$ kHz	1.5	2.25		mA (max)
Clock Feedthrough (Peak-to-Peak)	$T_A = 25°C$ Filter Output	15			mV
$f_{CLK} \leq 250$ kHz (Note 3)					
DC Gain (H_O)	$R_{SOURCE} \leq 2$ kΩ	0.0	±0.15		dB (max)
Clock to Cutoff Frequency Ratio (f_{CLK}/f_C)	$T_A = 25°C$ MF4-50 MF4-100	50.07 ± 0.3%	50.07 ± 1.6%	50.07 ± 0.6%	 (max) (max)
f_{CLK}/f_C Temperature Coefficient	MF4-50 MF4-100	±25			ppm/°C ppm/°C
Stopband Attenuation	At 2 f_C	−25.0	−24.0		dB (min)
DC Offset Voltage	MF4-50 MF4-100	−150 −300			mV mV
Output Swing	$R_L = 5$ kΩ	1.5 −2.2	1.0 −1.7		V (min) V (min)
Output Short Circuit Current (Note 6)	$T_A = 25°C$ Source Sink	 28 0.5			 mA mA
Dynamic Range (Note 2)	$T_A = 25°C$ MF4-50 MF4-100	 80 78			 dB dB
Additional Magnitude Response Test Points (Note 4)	$T_A = 25°C$ $f_{CLK} = 250$ kHz				
MF4-50 ($f_C = 5$ kHz) Magnitude at	f = 6000 Hz f = 4500 Hz	−7.57 −1.46	−7.57 ± 0.54 −1.46 ± 0.24		dB (max) dB (max)
MF4-100 ($f_C = 2.5$ kHz) Magnitude at	f = 3000 Hz f = 2250 Hz		±0.2 ±0.1		dB (max) dB (max)

Logic Input-Output Characteristics (Note 7) ($V^- = 0V$, Note 5)

Parameter	Conditions	Typ	Tested Limits	Design Limits	Units (Limits)
SCHMITT TRIGGER					
V_{T+} Positive Going Threshold Voltage	$V^+ = 10V$	7.0	6.1		V (min)
			8.9		V (max)
	$V^+ = 5V$	3.5	3.1		V (min)
			4.4		V (max)
V_{T-} Negative Going Threshold Voltage	$V^+ = 10V$	3.0	1.3		V (min)
			3.8		V (max)
	$V^+ = 5V$	1.5	0.6		V (min)
			1.9		V (max)
Hysteresis ($V_{T+} - V_{T-}$)	$V^+ = 10V$	4.0	2.3		V (min)
			7.6		V (max)
	$V^+ = 5V$	2.0	1.2		V (min)
			3.8		V (max)
Logical "1" Output Voltage ($I_O = -10\ \mu A$) (Pin 2)	$V^+ = 10V$		9.0		V (min)
	$V^+ = 5V$		4.5		V (min)
Logical "0" Output Voltage ($I_O = 10\ \mu A$) (Pin 2)	$V^+ = 10V$		1.0		V (max)
	$V^+ = 5V$		0.5		V (max)
Output Source Current	CLK R Shorted to Ground				
	$V^+ = 10V$	6.0	3.0		mA (min)
	$V^+ = 5V$	1.5	0.75		mA (min)
Output Sink Current	CLK R Shorted to V^+				
	$V^+ = 10V$	5.0	2.5		mA (min)
	$V^- = 5V$	1.3	0.65		mA (min)
TTL CLOCK INPUT (CLK R PIN) (Note 8)					
V_{IL} (Logical "0" Input Voltage)			0.8		V (max)
V_{IH} (Logical "1" Input Voltage)			2.0		V (min)
Leakage Current at CLK R Pin	$T_A = 25°C$, L. Sh Pin Tied to Mid-Supply		2.0		μA (max)

Note 1: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 2: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically μVrms for the MF4-50 and μVrms for the MF4-100. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwidth is typically μVrms for both the MF4-50 and the MF4-100.

Note 3: The specifications for the MF4 have been given for a clock frequency (f_{CLK}) of 250 kHz and less. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±0.6% but the filter still maintains its magnitude characteristics. See Application Hints.

Note 4: Besides checking the cutoff frequency (f_C) and the stopband attenuation at 2 f_C, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB. For a further discussion see Applications Hints.

Note 5: For simplicity all the logic levels have been referenced to $V^- = 0V$ (except for the TTL input logic levels). The logic levels will scale accordingly for ±5V and ±2.5V supplies.

Note 6: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst-case conditions.

Note 7: Unless otherwise stated, these specifications apply over the commercial temperature range of $0°C \le T_A \le 70°C$.

Note 8: The MF4 is operating with symmetrical split supplies and L. Sh is tied to ground.

Missing Values and "Application Hints" section will be added on final data sheet.

Pin Description

FILTER OUT — This is the output of the lowpass filter. It will typically sink 0.90 mA and source 3 mA. Typically, the output will swing to within 1V of each supply rail.

FILTER IN — This is the input to the lowpass filter. To minimize gain errors, the source impedance should be less than 2 kΩ. For more details see Application Hints section. Note that for single supply operation the input signal must be biased to mid-supply or AC coupled.

AGND — This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation, see *Figure 4*. For a further discussion on mid-supply biasing techniques see the Application Hints. For optimum filter performance a "clean" ground must be provided.

V^+, V^- — These are the positive and negative supply pins. The MF4 will operate over a supply range of 5V to 14V. Decoupling the supply pins with 0.1 μF capacitors is highly recommended.

CLK IN — This is the input of a CMOS Schmitt trigger. If an external CMOS logic level clock is to be used, it is applied to this pin.

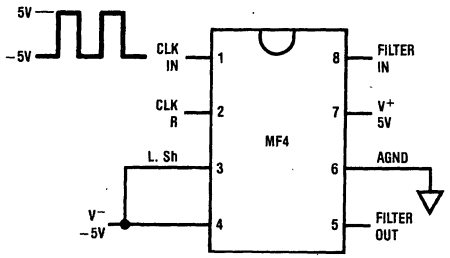
L. Sh — The level shift pin serves two purposes. One, the voltage at this pin sets the input switching threshold of an internal level shift stage. The level shift stage converts either TTL or CMOS logic levels to full V^+ to V^- clock levels that are required by the internal non-overlapping clock generator. The threshold is approximately 2V above the voltage at the level shift pin.

Second, the voltage at this pin enables or disables an internal TRI-STATE buffer between the Schmitt trigger and the level shift stage. When tied to V^-, this buffer is enabled and the Schmitt trigger drives the level shift stage. When tied to mid-supply (ground where the MF4 is operating from symmetrical split supplies) or above, the buffer is disabled and is placed in a high impedance state. This allows an external TTL (if L. Sh is connected to ground) or CMOS logic level to be applied to the level shift stage via the CLK R pin.

CLK R — This pin serves as the input for a TTL logic level clock if the L. Sh pin is tied to ground and the MF4 is operating with dual supplies.

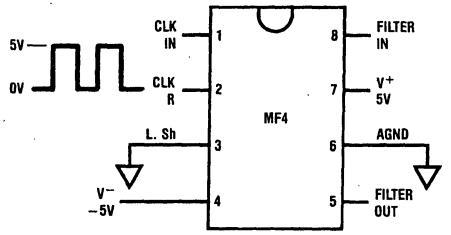
In the self-clocking mode an external resistor is tied from this pin to the CLK IN pin and an external capacitor is tied from the CLK IN pin to ground. This creates a Schmitt trigger oscillator. When using the self-clocking mode the L. Sh pin must be tied to V^-.

DUAL SUPPLY OPERATION



TL/H/5064–3

FIGURE 1. MF4 Driven with CMOS Level Clock ($V_{IH} \geq 0.8\ V_{CC}$* and $V_{IL} \leq 0.2\ V_{CC}$)



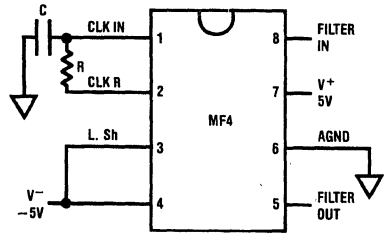
TL/H/5064–4

FIGURE 2. MF4 Driven with TTL Level Clock

*$V_{CC} = V^+ - V^-$

Pin Description (Continued)

DUAL SUPPLY OPERATION



$$f_{CLK} = \frac{1}{RC \text{ in } \left[\left(\frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

Typically for $V_{CC} = 10V$

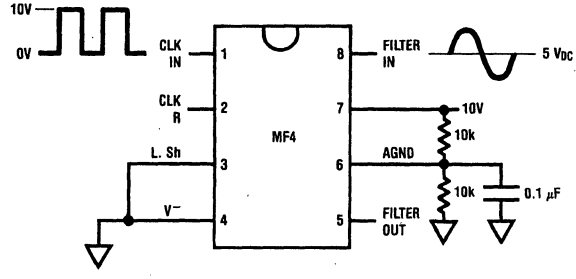
$$f_{CLK} = \frac{1}{1.69\ RC}$$

TL/H/5064–5

FIGURE 3. MF4 Driven with Schmitt Trigger Oscillator

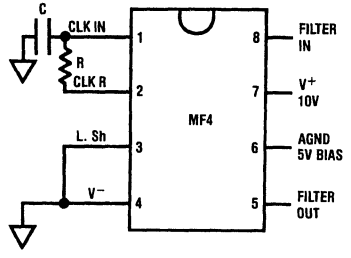
SINGLE SUPPLY OPERATION

If an external clock is used, it has to be of CMOS level because the clock is input to a CMOS Schmitt trigger.
The AGND pin must be biased to mid-supply.
The input signal should be DC biased to mid-supply or AC coupled to the input pin.



TL/H/5064–6

FIGURE 4a. MF4 Driven with an External Clock



$$f_{CLK} = \frac{1}{RC \text{ in } \left[\left(\frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

Typically for $V_{CC} = 10V$

$$f_{CLK} = \frac{1}{1.69\ RC}$$

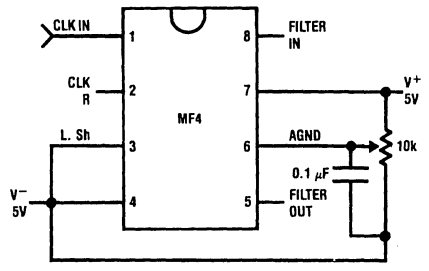
TL/H/5064–7

An external R and C can be used to generate an on-board clock; if so, the L. Sh pin should remain at ground.

FIGURE 4b. MF4 Driven with the Schmitt Trigger Oscillator

Pin Description (Continued)

OFFSET ADJUST



TL/H/5064–8

FIGURE 5. Typical Circuit for Adjusting the DC Offset of the Filter.

(See Application Hints on mid-supply bias generation)
Filter Out should be referenced to AGND.

National Semiconductor

PRELIMINARY

MF5 Universal Monolithic Switched Capacitor Filter

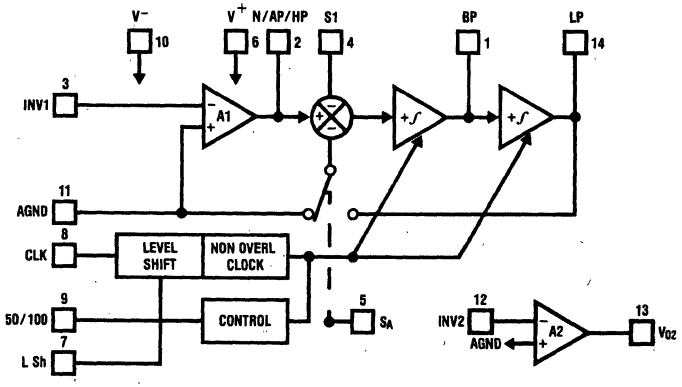
General Description

The MF5 consists of an extremely easy to use, general purpose CMOS active filter building block and an uncommitted op amp. The filter building block, together with an external clock and a few resistors, can produce various second order functions. The filter building block has 3 output pins. One of the output pins can be configured to perform highpass, allpass or notch functions and the remaining 2 output pins perform bandpass and lowpass functions. The center frequency of the filter can be directly dependent on the clock frequency or it can depend on both clock frequency and external resistor ratios. The uncommitted op amp can be used for cascading purposes, for obtaining additional allpass and notch functions, or for various other applications. Higher order filter functions can be obtained by cascading several MF5s or by using the MF5 in conjuction with the MF10 (dual switched capacitor filter building block). The MF5 is functionally compatible with the MF10. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

- Low cost
- 14-pin DIP
- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variations
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_o \times Q$ range up to 200 kHz
- Operation up to 30 kHz (typical)
- Additional uncommitted op-amp

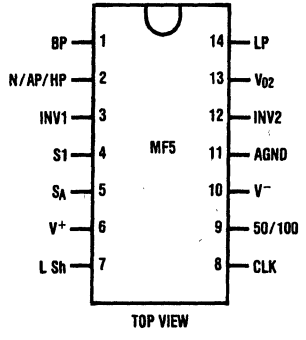
System Block Diagram



TL/H/5066–1

Connection Diagram

Dual-In-Line Package



TL/H/5066–2

Order Number MF5J, N
See NS Packages J14A, N14A

National Semiconductor

PRELIMINARY

MF6 6th Order Switched Capacitor Butterworth Lowpass Filter

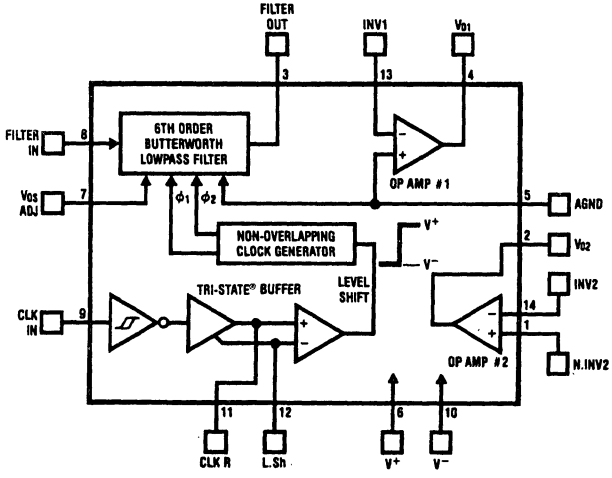
General Description

The MF6 is a versatile easy to use, precision 6th order Butterworth lowpass active filter. Switched capacitor techniques eliminate external component requirements and allow a clock tunable cutoff frequency. The ratio of the clock frequency to the lowpass cutoff frequency is internally set to 50 to 1 (MF6-50) or 100 to 1 (MF6-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, a TTL or CMOS logic compatible clock can be directly applied. The maximally flat passband frequency response together with a DC gain of 1 V/V allows cascading MF6 sections for higher order filtering. In addition to the filter, two independent CMOS op amps are included on the die and are useful for any general signal conditioning applications.

Features

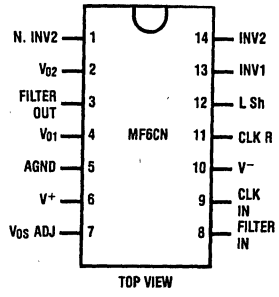
- Low cost
- Easy to use
- Nc external components
- 14-pin DIP
- Cutoff frequency accuracy of ±0.3%
- Cutoff frequency range of 0.1 Hz to 20 kHz
- Two uncommitted op amps available
- 5V to 14V operation
- Cutoff frequency set by external internal clock

Block and Connection Diagrams



TL/H/5065–1

Dual-In-Line Package



TL/H/5065–2

Order Number MF6
See NS Package N14A

Absolute Maximum Ratings

Supply Voltage	14V	Storage Temperature	150°C
Power Dissipation	−500 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature	0°C to 70°C (MF6CN)		

Electrical Characteristics (Filter)

Parameter	Conditions	Typ	Tested Limits (Note 8)	Design Limits (Note 9)	Units (Limits)
$V^+ = 5V, V^- = -5V, T^A = 25°C$					
Cutoff Frequency Range (f_C) (Note 1)	MF6-50			0.1	Hz (min)
				20k	Hz (max)
	MF6-100			0.1	Hz (min)
				10k	Hz (max)
Supply Current	$f_{CLK} = 250$ kHz	4.0	6.0		mA (max)
Clock Feedthrough (Peak-to-Peak)	Filter Output	30			mV
	Op Amp #1 Output	25			mV
	Op Amp #2 Output	20			mV
$f_{CLK} \leq 250$ kHz (Note 3)					
DC Gain (H_O)	$R_{SOURCE} \leq 2$ kΩ	0.0	±0.3		dB (max)
Clock to Cutoff Frequency Ratio (f_{CLK}/f_C)	MF6-50	49.27 ± 0.3%	49.27 ± 1.0%		(max)
	MF6-100	98.97 ± 0.3%	98.97 ± 1.0%		(max)
f_{CLK}/f_C Temperature Coefficient	MF6-50	25			ppm/°C
	MF6-100	25			ppm/°C
Stopband Attenuation	At 2 f_C	−37.5		−36	dB (min)
Unadjusted DC Offset Voltage	MF6-50	−300			mV
	MF6-100	−500			mV
Output Swing	$R_L = 5$ kΩ	+4.0	+3.5		V (min)
		−4.1	−3.8		V (min)
Output Short Circuit Current (Note 6)	Source	50			mA
	Sink	1.5			mA
Dynamic Range (Note 2)	MF6-50	83			dB
	MF6-100	81			dB
Additional Magnitude Response Test Points (Note 4)	$f_{CLK} = 250$ kHz				
MF6-50 ($f_C = 5$ kHz) Magnitude at	f = 6000 Hz	−9.47	−9.47 ± 0.5		dB (max)
	f = 4500 Hz	−0.92	−0.92 ± 0.2		dB (max)
MF6-100 ($f_C = 2.5$ kHz) Magnitude at	f = 3000 Hz	−9.48	−9.48 ± 0.5		dB (max)
	f = 2250 Hz	−0.97	−0.97 ± 0.2		dB (max)
Attenuation Rate MF6-50 ($f_c = 5$ kHz)	$f_1 = 6000$ Hz, $f_2 = 8000$ Hz		−36		dB/octave
MF6-100 ($f_c = 2.5$ kHz)	$f_1 = 3000$ Hz, $f_2 = 4000$ Hz		−36		dB/octave

Electrical Characteristics (Continued) (Filter)

Parameter	Conditions	Typ	Tested Limits (Note 8)	Design Limits (Note 9)	Units (Limits)
$V^+ = 2.5V, V^- = -2.5V, T_A = 25°C$					
Cutoff Frequency Range (f_C) (Note 1)	MF6-50			0.1 10k	Hz (min) Hz (max)
	MF6-100			0.1 5k	Hz (min) Hz (max)
Supply Current	$f_{CLK} = 250$ kHz	2.5	4.0		mA (max)
Clock Feedthrough (Peak-to-Peak)	Filter Output Op Amp #1 Output Op Amp #2 Output	20 10 10			mV mV mV
$f_{CLK} \leq 250$ kHz (Note 3)					
DC Gain (H_O)	$R_{SOURCE} \leq 2$ kΩ	0.0	±0.3		dB (max)
Clock to Cutoff Frequency Ratio (f_{CLK}/f_C)	MF6-50 MF6-100	49.45 ± 0.3% 99.35 ± 0.3%	49.45 ± 1.0% 99.35 ± 1.0%		(max) (max)
f_{CLK}/f_C Temperature Coefficient	MF6-50 MF6-100	−15 90			ppm/°C ppm/°C
Stopband Attenuation	At 2 f_C	−37.5		−36	dB (min)
Unadjusted DC Offset Voltage	MF6-50 MF6-100	−200 −350			mV mV
Output Swing	$R_L = 5$ kΩ	1.5 −2.2	1.0 −1.7		V (min) V (min)
Output Short Circuit Current (Note 6)	Source Sink	28 0.5			mA mA
Dynamic Range (Note 2)	MF6-50 MF6-100	77 77			dB dB
Additional Magnitude Response Test Points (Note 4)	$f_{CLK} = 250$ kHz				
MF6-50 ($f_C = 5$ kHz) Magnitude at	f = 6000 Hz f = 4500 Hz	−9.54 −0.96	−9.54 ± 0.5 −0.96 ± 0.3		dB (max) dB (max)
MF6-100 ($f_C = 2.5$ kHz) Magnitude at	f = 3000 Hz f = 2250 Hz	−9.67 −1.01	−9.67 ± 0.5 −1.01 ± 0.3		dB (max) dB (max)
Attenuation Rate MF6-50 ($f_c = 5$ kHz)	$f_1 = 6000$ Hz $f_2 = 8000$ Hz		−36		dB/octave
MF6-100 ($f_c = 2.5$ kHz)	$f_1 = 3000$ Hz $f_2 = 4000$ Hz		−36		dB/octave

Electrical Characteristics (Both Op Amps)

Parameter	Conditions	Typ	Tested Limits (Note 8)	Design Limits (Note 9)	Units (Limits)
$V^+ = 5V, V^- = -5V, T_A = 25°C$					
DC Open Loop Gain		72		67	dB (min)
Gain Bandwidth Product		1.2			MHz (min)
Input Offset Voltage		±8.0	±20		mV (max)
Output Swing	$R_L = 2.5\ k\Omega$	4.0 −4.5	3.8 −4.0		V (min) V (min)
Output Short Circuit Current (Note 6)	 Source Sink	 45 2.5			 mA mA
CMRR (Op Amp #2 Only)	$V_{CM1} = 1.8V$ $V_{CM2} = -2.2V$	60	55		dB (min)
Input Bias Current		10			pA
Slew Rate		7.0			V/μs
$V^+ = 2.5V, V^- = -2.5V, T_A = 25°C$					
DC Open Loop Gain		67		62	dB (min)
Gain Bandwidth Product		1.2			MHz (min)
Input Offset Voltage		±8.0	±20		mV (max)
Output Swing	$R_L = 2.5\ k\Omega$	1.5 −2.2	1.3 −1.7		V (min) V (min)
Output Short Circuit Current (Note 6)	 Source Sink	 24 1.0			 mA mA
CMRR (Op Amp #2 Only)	$V_{CM1} = 0.5V$ $V_{CM2} = -0.9V$	60	55		dB (min)
Input Bias Current		10			pA
Slew Rate		6			V/μs

Logic Input-Output Characteristics ($V^- = 0V$, Note 5), $T_A = 25°C$

Parameter	Conditions	Typical	Tested Limits (Note 8)	Design Limits (Note 9)	Units (Limits)
SCHMITT TRIGGER					
V_{T+} Positive Going Threshold Voltage	$V^+ = 10V$	7.0	6.1		V (min)
			8.9		V (max)
	$V^+ = 5V$	3.5	3.1		V (min)
			4.4		V (max)
V_{T-} Negative Going Threshold Voltage	$V^+ = 10V$	3.0	1.3		V (min)
			3.8		V (max)
	$V^+ = 5V$	1.5	0.6		V (min)
			1.9		V (max)
Hysteresis ($V_{T+} - V_{T-}$)	$V^+ = 10V$	4.0	2.3		V (min)
			7.6		V (max)
	$V^+ = 5V$	2.0	1.3		V (min)
			3.8		V (max)
Logical "1" Output Voltage ($I_O = -10\ \mu A$) (Pin 11)	$V^+ = 10V$		9.0		V (min)
	$V^+ = 5V$		4.5		V (min)
Logical "0" Output Voltage ($I_O = 10\ \mu A$) (Pin 11)	$V^+ = 10V$		1.0		V (max)
	$V^+ = 5V$		0.5		V (max)
Output Source Current (Pin 11)	CLK R Shorted to Ground				
	$V^+ = 10V$	6.0	3.0		mA (min)
	$V^+ = 5V$	1.5	0.75		mA (min)
Output Sink Current (Pin 11)	CLK R Shorted to V^+				
	$V^+ = 10V$	5.0	2.5		mA (min)
	$V^- = 5V$	1.3	0.65		mA (min)
TTL CLOCK INPUT (CLK R PIN) (NOTE 7)					
V_{IL} (Logical "0" Input Voltage)			0.8		V (max)
V_{IH} (Logical "1" Input Voltage)			2.0		V (min)
Leakage Current at CLK R Pin	L. Sh Pin Tied to Mid-Supply		2.0		μA (max)

Note 1: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 2: For ±5V supplies the dynamic range is referenced to 2.82 Vrms (4V peak) where the wideband noise over a 20 kHz bandwidth is typically 200 μVrms for the MF6-50 and 250 μVrms for the MF6-100. For ±2.5V supplies the dynamic range is referenced to 1.06 Vrms (1.5V peak) where the wideband noise over a 20 kHz bandwith is typically 140 μVrms for both the MF6-50 and the MF6-100.

Note 3: The specifications for the MF6 have been given for a clock frequency (f_{CLK}) of 250 kHz and less. Above this clock frequency the cutoff frequency begins to deviate from the specified error band of ±0.6% but the filter still maintains its magnitude characteristics. See Application Hints.

Note 4: Besides checking the cutoff frequency (f_C) and the stopband attenuation at 2 f_C, two additional frequencies are used to check the magnitude response of the filter. The magnitudes are referenced to a DC gain of 0.0 dB. For a further discussion see Application Hints.

Note 5: For simplicity all the logic levels have been referenced to $V^- = 0V$ (except for the TTL input logic levels). The logic levels will scale accordingly for ±5V and ±2.5V supplies.

Note 6: The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst-case conditions.

Note 7: The MF6 is operating with symmetrical split supplies and L. Sh is tied to ground.

Note 8: Guaranteed and 100% production tested.

Note 9: Guaranteed, but not 100% production tested. These limits are not used to determine outgoing quality levels.

"Application Hints" section will be added on final data sheet.

Pin Description

FILTER OUT — This is the output of the lowpass filter. It will typically sink 0.90 mA and source 3 mA. Typically, the output will swing to within 1V of each supply rail.

V_{OS} ADJ — If needed, this pin is used to adjust the DC offset of the lowpass filter. A typical circuit is shown in *Figure 5*, where a 50 kΩ pot is connected between V^+ and V^- and the wiper is connected to the V_{OS} ADJ pin. If the V_{OS} ADJ pin is not used it must be tied to AGND. The DC gain from the V_{OS} ADJ pin to the output of the filter is 2.5 to 3.0.

FILTER IN — This is the input to the lowpass filter. To minimize gain errors, the source impedance should be less than 2 kΩ. For more details see Application Hints section. Note that for single supply operation the input signal must be biased to mid-supply or AC coupled.

V_{02}, INV2, N. INV2 — V_{02} is the output of op amp #2. INV2 and N. INV2 are the inverting and non-inverting inputs of op amp #2, respectively. These are very high impedance inputs.

V_{01}, INV1 — V_{01} is the output and INV1 is the inverting input of op amp #1. INV1 is also a high impedance input. The non-inverting input is connected to AGND (analog ground) internally. Both op amp #1 and op amp #2 will typically sink 1.8 mA and source 3 mA and will swing to within 1V of each supply rail.

AGND — This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation, see *Figure 4*. For a further discussion on mid-supply biasing techniques see the Application Hints. For optimum filter performance a "clean" ground must be provided.

V^+, V^- — These are the positive and negative supply pins. The MF6 will operate over a supply range of 5V to 14V. Decoupling the supply pins with 0.1 μF capacitors is highly recommended.

CLK IN — This is the input of a CMOS Schmitt trigger. If an external CMOS logic level clock is to be used, it is applied to this pin.

L. Sh — The level shift pin serves two purposes. One, the voltage at this pin sets the input switching threshold of an internal level shift stage. The level shift stage converts either TTL or CMOS logic levels to full V^+ to V^- clock levels that are required by the internal non-overlapping clock generator. The threshold is approximately 2V above the voltage at the level shift pin.
Second, the voltage at this pin enables or disables an internal TRI-STATE buffer between the Schmitt trigger and the level shift stage. When tied to V^-, this buffer is enabled and the Schmitt trigger drives the level shift stage. When tied to mid-supply (ground where the MF6 is operating from symmetrical split supplies) or above, the buffer is disabled and is placed in a high impedance state. This allows an external TTL (if L. Sh is connected to ground) or CMOS logic level to be applied to the level shift stage via the CLK R pin.

CLK R — This pin serves as the input for a TTL logic level clock if the L. Sh pin is tied to ground and the MF6 is operating with dual supplies. In the self-clocking mode an external resistor is tied from this pin to the CLK IN pin and an external capacitor is tied from the CLK IN pin to ground. This creates a Schmitt trigger oscillator. When using the self-clocking mode the L. Sh pin must be tied to V_-.

DUAL SUPPLY OPERATION

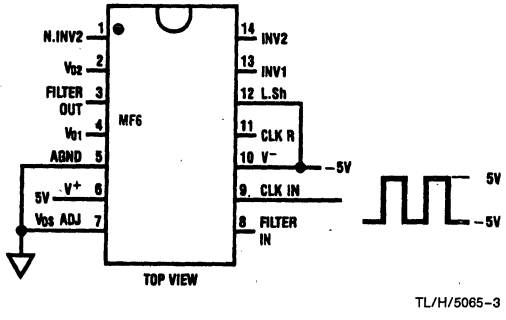


FIGURE 1. MF6 Driven with CMOS Logic Level Clock ($V_{IH} \geq 0.8\ V_{CC}$* and $V_{IL} \leq 0.2\ V_{CC}$)

*$V_{CC} = V^+ - V^-$

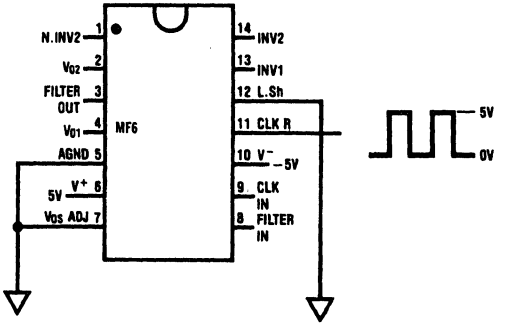
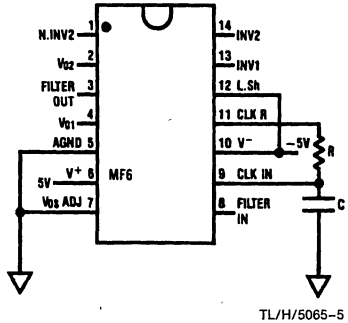


FIGURE 2. MF6 Driven with TTL Logic Level Clock

Pin Description (Continued)

DUAL SUPPLY OPERATION



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$$f_{CLK} = \frac{1}{\left[\left(\frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

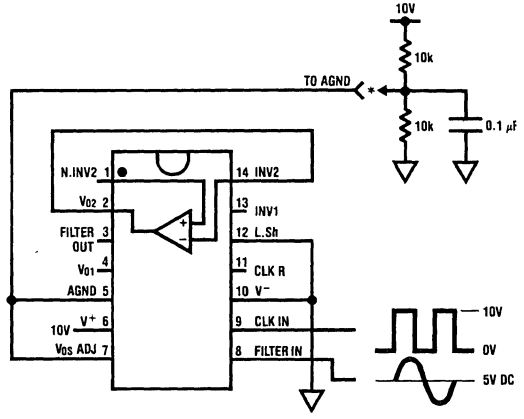
Typically for $V_{CC} = 10V$

$$f_{CLK} = \frac{1}{1.69\,RC}$$

FIGURE 3. MF6 Driven with Schmitt Trigger Oscillator

SINGLE SUPPLY OPERATION

The AGND pin must be biased to mid-supply. The input signal should be DC biased to mid-supply or AC coupled to the input pin.



* or buffer with op amp #2, then apply to AGND

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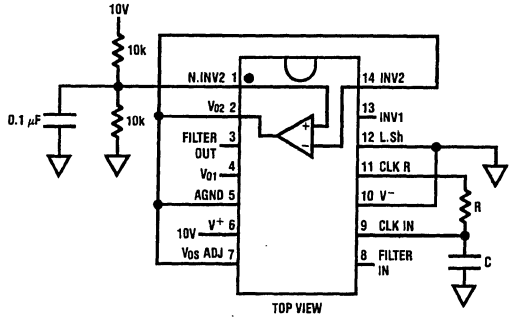
If an external clock is used, it has to be of CMOS logic levels because the clock is input to a CMOS Schmitt trigger.

FIGURE 4a. MF6 Driven with an External Clock



$$f_{CLK} = \frac{1}{\left[\left(\frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}\right)\left(\frac{V_{T+}}{V_{T-}}\right)\right]}$$

Typically for $V_{CC}^* = 10V$

$$f_{CLK} = \frac{1}{1.69\,RC}$$

$*V_{CC} = V^+ - V^-$

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An external R and C can be used to generate an on-board clock, if so the L. Sh pin should remain at ground.

FIGURE 4b. MF6 Driven with the Schmitt Trigger Oscillator

Pin Description (Continued)

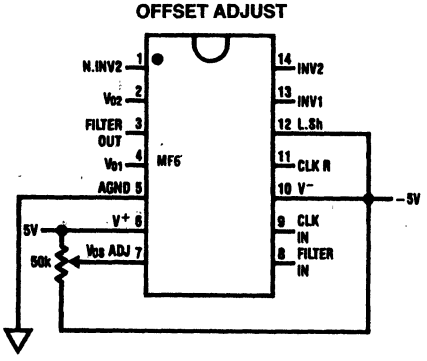

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FIGURE 5. Typical Circuit for Adjusting Filter DC Offset If not used, connect V_{OS} ADJ pin to AGND)

National Semiconductor

MF10 Universal Monolithic Dual Switched Capacitor Filter

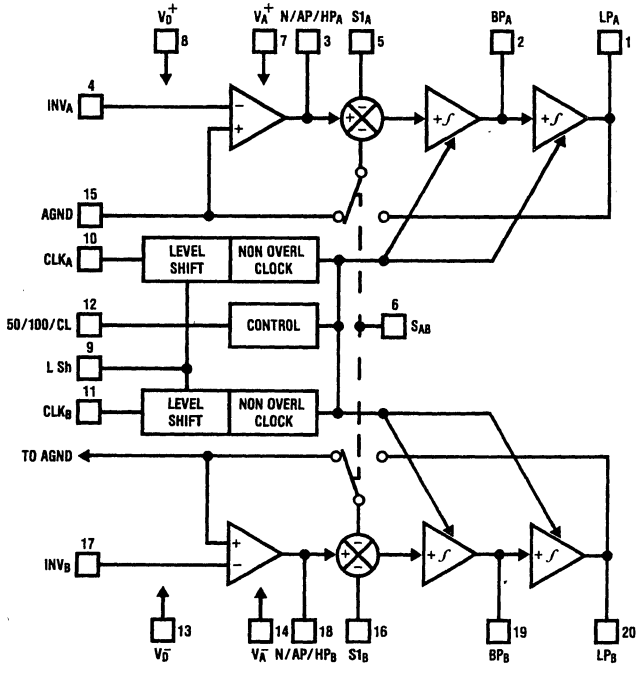
General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages. Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

Features

- Low cost
- 20-pin 0.3″ wide package
- Easy to use
- Clock to center frequency ratio accuracy ± 0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- $f_0 \times Q$ range up to 200 kHz
- Operation up to 30 kHz

System Block Diagram



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Absolute Maximum Ratings

Supply Voltage	14V	Storage Temperature	150°C
Power Dissipation	500 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature	0°C to 70°C		

Electrical Characteristics (Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range	$f_o \times Q < 200$ kHz	20	30		kHz
Clock to Center Frequency Ratio, f_{CLK}/f_o					
MF10BN	Pin 12 High, Q = 10		49.94 ± 0.2%	± 0.6%	
MF10CN	$f_o \times Q < 50$ kHz, Mode 1		49.94 ± 0.2%	± 1.5%	
MF10BN	Pin 12 at Mid Supplies		99.35 ± 0.2%	± 0.6%	
MF10CN	Q = 10, $f_o \times Q < 50$ kHz, Mode 1		99.35 ± 0.2%	± 1.5%	
Q Accuracy (Q Deviation from an Ideal Continuous Filter)	$f_o \times Q < 50$ kHz $f_o < 5$ kHz, Mode 1		± 2%	± 6%	
f_o Temperature Coefficient	Pin 12 High (~ 50:1) Pin 12 Mid Supplies (~ 100:1) $f_o \times Q < 100$ kHz, Mode 1 External Clock Temperature Independent		± 10 ± 100		ppm/°C ppm/°C
Q Temperature Coefficient	$f_o \times Q < 100$ kHz, Q Setting Resistors Temperature Independent		± 500		ppm/°C
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 10k			± 2	%
Crosstalk			50		dB
Clock Feedthrough			10		mV
Maximum Clock Frequency		1	1.5		MHz
Power Supply Current			8	10	mA

Electrical Characteristics (Internal Op Amps) 25°C

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		± 4	± 5		V
Voltage Swing (Pins 1, 2, 19, 20)	$V_S = \pm 5V$, $R_L = 5k$				
MF10BN		± 4.0	± 4.1		V
MF10CN		± 3.8	± 3.9		V
Voltage Swing (Pins 3 and 18)	$V_S = \pm 5V$, $R_L = 3.5k$				
MF10BN		± 4.0	± 4.1		V
MF10CN		± 3.8	± 3.9		V
Output short Circuit Current	$V_S = \pm 5V$				
Source			3		
Sink			1.5		mA
Op Amp Gain BW Product			2.5		MHz
Op Amp Slew Rate			7		V/μS

Definition of Terms

f_{CLK}: the switched capacitor filter external clock frequency.

f_o: center of frequency of the second order function complex pole pair. f_o is measured at the bandpass output of each ½ MF10, and it is the frequency of the bandpass peak occurrence (*Figure 1*).

Q: quality factor of the 2nd order function complex pole pair. Q is also measured at the bandpass output of each ½ MF10 and it is the ratio of f_o over the −3 dB bandwidth of the 2nd order bandpass filter, (*Figure 1*). The value of Q is not measured at the lowpass or highpass outputs of the filter, but its value relates to the possible amplitude peaking at the above outputs.

H_{OBP}: the gain in (V/V) of the bandpass output at $f = f_o$.

H_{OLP}: the gain in (V/V) of the lowpass output of each ½ MF10 at $f \rightarrow 0$ Hz, (*Figure 2*).

H_{OHP}: the gain in (V/V) of the highpass output of each ½ MF10 as $f \rightarrow f_{CLK}/2$, (*Figure 3*).

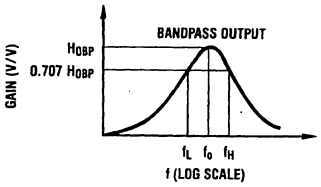
Q_Z: the quality factor of the 2nd order function complex zero pair, if any. (Q_Z is a parameter used when an allpass output is sought and unlike Q it cannot be directly measured).

f_Z: the center frequency of the 2nd order function complex zero pair, if any. If f_Z is different from f_o, and if the Q_Z is quite high it can be observed as a notch frequency at the allpass output.

f_{notch}: the notch frequency observed at the notch output(s) of the MF-10.

H_{ON_1}: the notch output gain as $f \rightarrow 0$ Hz.

H_{ON_2}: the notch output gain as $f \rightarrow f_{CLK}/2$.

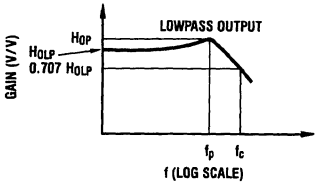


$$Q = \frac{f_o}{f_H - f_L};\ f_o = \sqrt{f_L f_H}$$

$$f_L = f_o\left(\frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

$$f_H = f_o\left(\frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1}\right)$$

FIGURE 1

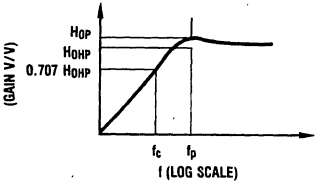


$$f_C = f_O \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_P = f_O\sqrt{1 - \frac{1}{2Q^2}}$$

$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2



$$f_C = f_O \times \left[\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}\right]^{-1}$$

$$f_P = f_o \times \left[\sqrt{1 - \frac{1}{2Q^2}}\right]^{-1}$$

$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

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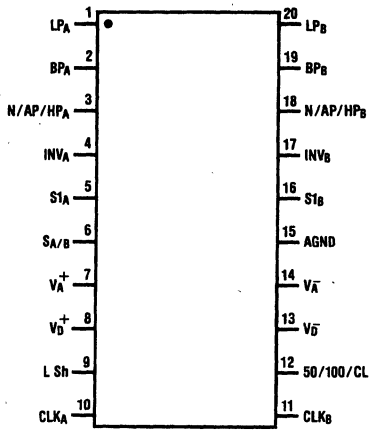
FIGURE 3

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5645–3

Order Number MF10BN or MF10CN
See NS Package N20A

Pin Description

LP, BP, N/AP/HR — These are the lowpass, bandpass, notch or allpass or highpass outputs of each 2nd order section. The LP and BP outputs can sink typically 1 mA and source 3 mA. The N/AP/HP output can typically sink and source 1.5 mA and 3 mA, respectively.

INV — This is the inverting input of the summing op amp of each filter. The pin has static discharge protection.

S1 — S1 is a signal input pin used in the allpass filter configurations (see modes of operation 4 and 5). The pin should be driven with a source impedance of less than 1 kΩ.

$S_{A/B}$ — It activates a switch connecting one of the inputs of the filter's 2nd summer either to analog ground ($S_{A/B}$ low to $V_{\overline{A}}$) or to the lowpass output of the circuit ($S_{A/B}$ high to V_A^+). This allows flexibility in the various modes of operation of the IC. $S_{A/B}$ is protected against static discharge.

V_A^+, V_D^+ — Analog positive supply and digital positive supply. These pins are internally connected through the IC substrate and therefore V_A^+ and V_D^+ should be derived from the same power supply source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can be externally tied together and bypassed by a single capacitor.

$V_{\overline{A}}, V_{\overline{D}}$ — Analog and digital negative supply respectively. The same comments as for V_A^+ and V_D^+ apply here.

L.Sh — Level shift pin; it accommodates various clock levels with dual or single supply operation. With dual ±5V supplies, the MF10 can be driven with CMOS clock levels (±5V) and the L Sh pin should be tied either to the system ground or to the negative supply pin. If the same supplies as above are used but T^2L clock levels, derived from 0V to 5V supply, are only available, the L Sh pin should be tied to the system ground. For single supply operation (0V and 10V) the V_D^-, V_A^- pins should be connected to the system ground, the AGND pin should be biased at 5V and the L Sh pin should also be tied to the system ground. This will accommodate both CMOS and T^2L clock levels.

CLK (A or B) — Clock inputs for each switched capacitor filter building block. They should both be of the same level (T^2L or CMOS). The level shift (L.Sh) pin description discusses how to accommodate their levels. The duty cycle of the clock should preferably be close to 50% especially when clock frequencies above 200 kHz are used. This allows the maximum time for the op amps to settle which yields optimum filter operation.

50/100/CL — By tying the pin high a 50:1 clock to filter center frequency operation is obtained. Tying the pin at mid supplies (i.e., analog ground with dual supplies) allows the filter to operate at a 100:1 clock to center frequency ratio. When the pin is tied low, a simple current limiting circuitry is triggered to limit the overall supply current down to about 2.5 mA. The filtering action is then aborted.

AGND — Analog ground pin; it should be connected to the system ground for dual supply operation or biased at mid supply for single supply operation. The positive inputs of the filter op amps are connected to the AGND pin so "clean" ground is mandatory. The AGND pin is protected against static discharge.

Modes of Operation

The MF10 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain approach will be appropriate. Since this may appear cumbersome and, since the MF10 closely approximates continuous filters, the following discussion is based on the well known frequency domain. The following illustrations refer to ½ of the MF10; the other ½ is identical. Each MF10 can produce a full 2nd order function, so up to 4th order functions can be performed by using cascading techniques.

MODE 1: Notch 1, Bandpass, Lowpass Outputs: $f_{notch} = f_o$ (See *Figure 4*)

f_o = center frequency of the complex pole pair

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_{notch} = center frequency of the imaginary zero pair = f_o.

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) = $-\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_o$) = $-\frac{R3}{R1}$

H_{ON} = Notch output gain as $\begin{cases} f \rightarrow 0 & -\frac{R2}{R1} \\ f \rightarrow f_{CLK}/2 & \end{cases}$

$Q = \frac{f_o}{BW} = \frac{R3}{R2}$

= quality factor of the complex pole pair.

BW = the −3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$H_{OLP} = \frac{H_{OBP}}{Q} \text{ or } H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q.$$

$H_{OLP\ (peak)} \cong Q \times H_{OLP}$ (for high Q's)

The above expressions are important. They determine the swing at each output as a function of the desired Q of the 2nd order function.

MODE 1a: Non-Inverting BP, LP (See *Figure 5*)

$f_o = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$

$Q = \frac{R3}{R2}$

$H_{OLP} = -1$; $H_{OLP\ (peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OBP_1} = -\frac{R3}{R2}$

$H_{OBP_2} = 1$ (non-inverting)

Circuit dynamics: $H_{OBP_1} = Q$

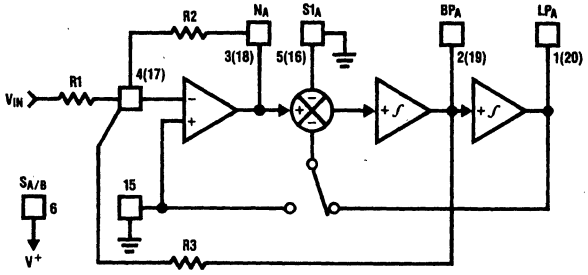


FIGURE 4. MODE 1

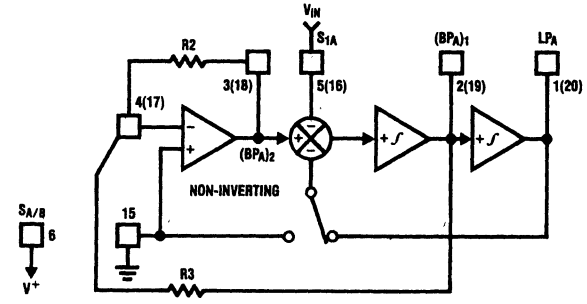


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FIGURE 5. MODE 1a

Modes of Operation (Continued)

MODE 2: Notch 2, Bandpass, Lowpass: $f_{notch} < f_o$
(See *Figure 6*)

f_o = center frequency

$$= \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}+1} \text{ or } \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}+1}$$

$f_{notch} = \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{\frac{R2}{R4}+1}{\frac{R2}{R3}}}$$

H_{OLP} = Lowpass output gain (as $f \rightarrow 0$)

$$= -\frac{\frac{R2}{R1}}{\frac{R2}{R4}+1}$$

H_{OBP} = Bandpass output gain (at $f = f_o$) $= -R3/R1$

H_{ON_1} = Notch output gain (as $f \rightarrow 0$)

$$= -\frac{\frac{R2}{R1}}{\frac{R2}{R4}+1}$$

H_{ON_2} = Notch output gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -R2/R1$

Filter dynamics: $H_{OBP} = Q\sqrt{H_{OLP}\,H_{ON_2}} = Q\sqrt{H_{ON_1}\,H_{ON_2}}$

MODE 3: Highpass, Bandpass, Lowpass Outputs
(See *Figure 7*)

$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}}$ or $\frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$$

H_{OHP} = Highpass gain $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$

H_{OBP} = Bandpass gain (at $f = f_0$) $= -\frac{R3}{R1}$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$) $= -\frac{R4}{R1}$

Circuit dynamics: $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$; $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP} \times Q}$

$H_{OLP\ (peak)} \cong Q \times H_{OLP}$ (for high Q's)

$H_{OHP\ (peak)} \cong Q \times H_{OHP}$ (for high Q's)

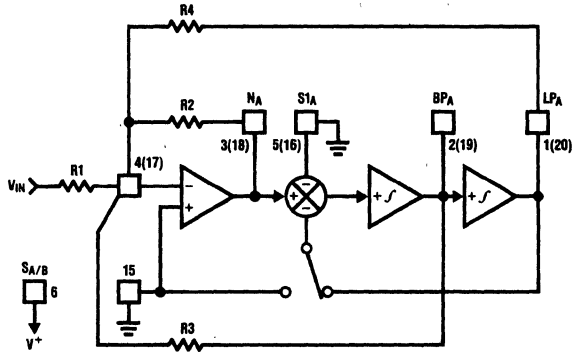

FIGURE 6. MODE 2

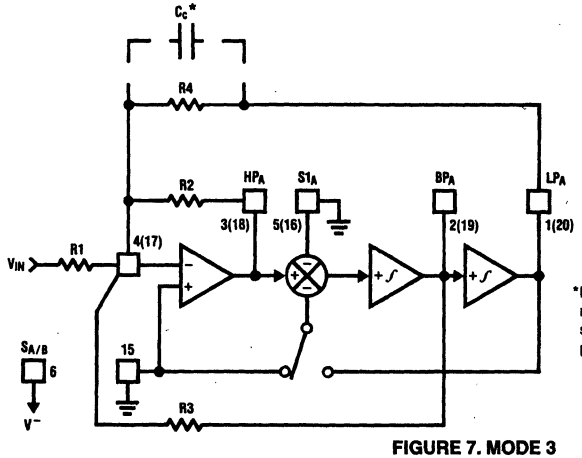

FIGURE 7. MODE 3

*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF–100 pF) across R4 to provide some phase lead.

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Modes of Operation (Continued)

MODE 3a: HP, BP, LP and Notch with External Op Amp
(See *Figure 8*)

$f_o = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}}$ or $\frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$

$Q = \sqrt{\frac{R2}{R4}} \times \frac{R3}{R2}$

$H_{OHP} = -\frac{R2}{R1}$

$H_{OBP} = -\frac{R3}{R1}$

$H_{OLP} = -\frac{R4}{R1}$

f_n = notch frequency $= \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_1}}$ or $\frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_1}}$

H_{ON} = gain of notch at $f = f_o = \left\| Q\left(\frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP}\right) \right\|$

H_{n1} = gain of notch (as $f \rightarrow 0$) $= \frac{R_g}{R_l} \times H_{OLP}$

H_{n2} = gain of notch $\left(\text{as } f \rightarrow \frac{f_{CLK}}{2}\right) = -\frac{R_g}{R_h} \times H_{OHP}$

MODE 4: Allpass, Bandpass, Lowpass Outputs
(See *Figure 9*)

f_o = center frequency

$= \frac{f_{CLK}}{100}$ or $\frac{f_{CLK}}{50}$;

f_z^* = center frequency of the complex zero pair $\approx f_o$

$Q = \frac{f_o}{BW} = \frac{R3}{R2}$;

Q_z = quality factor of complex zero pair $= \frac{R3}{R1}$

For AP output make R1 = R2

H_{OAP} = Allpass gain $\left(\text{at } 0 < f < \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1} = -1$

H_{OLP} = Lowpass gain (as $f \rightarrow 0$)

$= -\left(\frac{R2}{R1} + 1\right) = -2$

H_{OBP} = Bandpass gain (at $f = f_o$)

$= -\frac{R3}{R2}\left(1 + \frac{R2}{R1}\right) = -2\left(\frac{R3}{R2}\right)$

Circuit dynamics: $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$

* Due to the sampled data nature of the filter, a slight mismatch of f_z and f_o occurs causing a 0.4 dB peaking around f_o of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

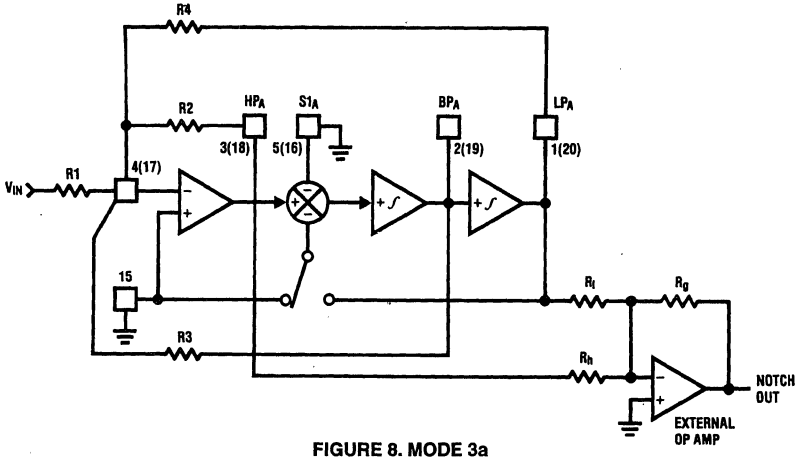

FIGURE 8. MODE 3a

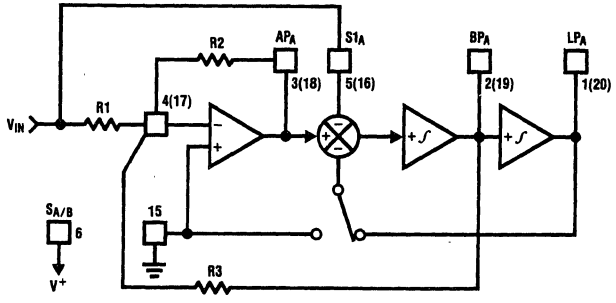

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FIGURE 9. MODE 4

Modes of Operation (Continued)

MODE 5: Numerator Complex Zeros, BP, LP (See *Figure 10*)

$$f_o = \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1+\frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1-\frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1+R2/R4} \times \frac{R3}{R2}$$

$$Q_Z = \sqrt{1-R2/R4} \times \frac{R3}{R1}$$

$$H_{0z1} = \text{gain at C.z output (as } f \longrightarrow 0 \text{ Hz)} = \frac{R2(R4-R1)}{R1(R2+R4)}$$

$$H_{0z2} = \text{gain at C.z output} \left(\text{as } f \longrightarrow \frac{f_{CLK}}{2} \right) = \frac{R2}{R1}$$

$$H_{OBP} = \left(\frac{R2}{R1}+1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = \left(\frac{R2+R1}{R2+R4}\right) \times \frac{R4}{R1}$$

MODE 6a: Single Pole, Hp, LP Filter (See *Figure 11*)

f_c = cutoff frequency of LP or HP output

$$= \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting) (See *Figure 12*)

f_c = cutoff frequency of LP outputs

$$\cong \frac{R2}{R3}\frac{f_{CLK}}{100} \text{ or } \frac{R2}{R3}\frac{f_{CLK}}{50}$$

$H_{OLP_1} = 1$ (non-inverting)

$$H_{OLP_2} = -\frac{R3}{R2}$$

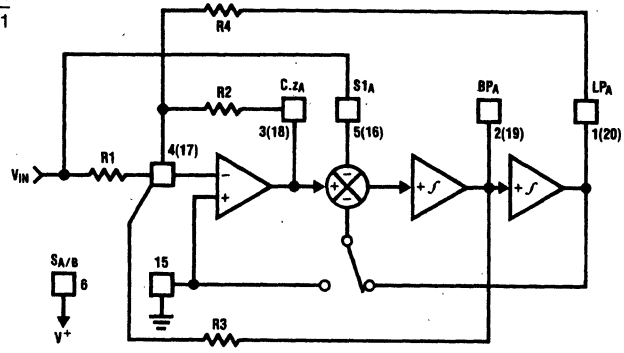

FIGURE 10. MODE 5

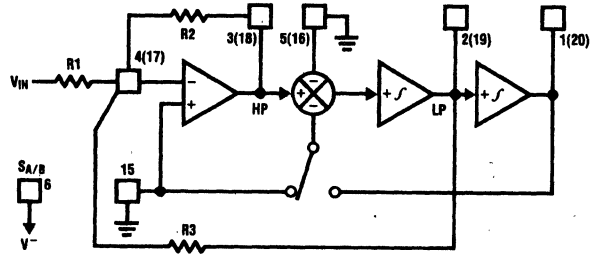

FIGURE 11. MODE 6a

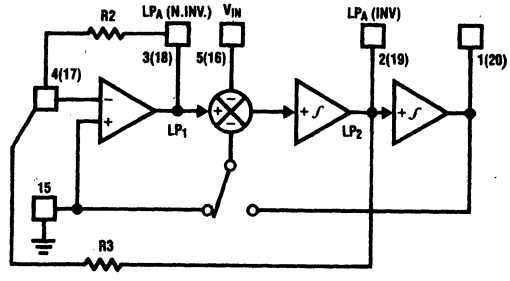

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FIGURE 12. MODE 6b

Applications Information

HOW TO USE THE f_{CLK}/f_o RATIO SPECIFICATION

The MF10 is a switched capacitor filter designed to approximate the response of a 2nd order state variable filter. When the sampling frequency is much larger than the frequency band of interest, the sampled data filter is a good approximation to its continuous time equivalent. In the case of the MF10, this ratio is about 50:1 or 100:1. Nevertheless the filter's response must be examined in the z-domain in order to obtain the actual response. It can be shown that the clock frequency to center frequency ratio, f_{CLK}/f_o and the quality factor, Q, deviate from their ideal values determined in the continuous time domain. These deviations are shown graphically in *Figures 13* and *14*. The ratio, f_{CLK}/f_o, is a function of the ideal Q and the largest errors occur for the lowest values of Q.

The curve for the f_{CLK}/f_o ratio versus the ideal Q has been normalized for a Q of 10 which is the Q value used for the f_{CLK}/f_o ratio testing of the MF10. At this point the f_{CLK}/f_o ratio is 49.94 in the 50:1 mode and 99.35 in the 100:1 mode. These values are within a maximum tolerance of ±0.6% (MF10B) and ±1.5% (MF10C). The above tolerances hold for the entire range of Q's; in other words, at 50:1, an MF10B has a ratio of 49.94±0.6% (Q=10) and this ratio becomes (49.44±0.6%) at Q=2.1. If these small errors cannot be tolerated, the clock frequency or the resistor's ratio, in Mode 3 and Mode 2, can be adjusted accordingly.

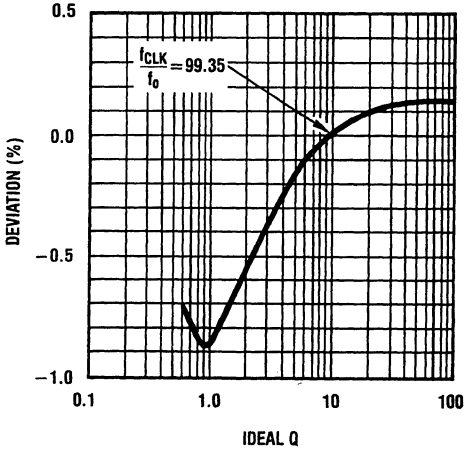


FIGURE 13 TL/H/5645–9

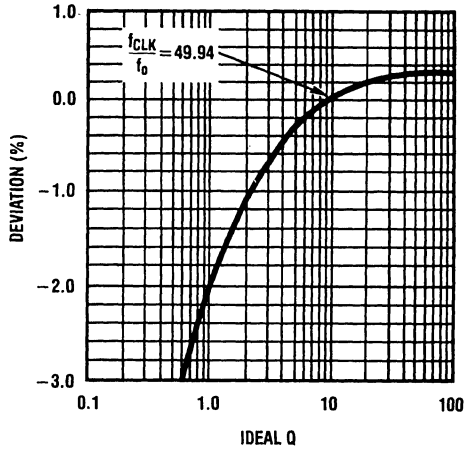


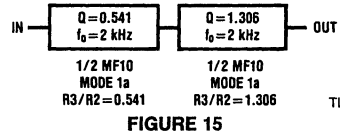
FIGURE 14 TL/H/5645–08

A SIMPLE AND INFORMATIVE FILTER DESIGN USING THE MF10

Example 1: Design a 4th order 2 kHz lowpass maximally flat (Butterworth filter). The overall gain of the filter is desired to be equal to 1V/V.

The 4th order filter can be built by cascading two 2nd order sections of (f_o, Q) equal to: Q=0.541, f_o=2 kHz, Q=1.306, f_o=2 kHz.

Due to the low Q values of the filter, the dynamics of the circuit are very good. Any of the modes of operation can be used but Mode 1a is the most simple:

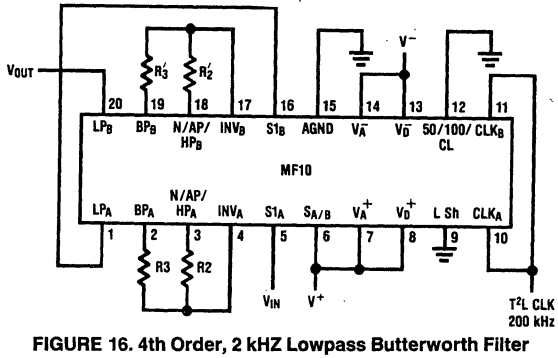


TL/H/5645–10

FIGURE 15

Since for the first section the smallest resistor is R3, choose R3>5k. Assume R3=10k then R2=18.48k. For the second section choose R2=10k and then R3=13.06k. Both clock input pins (10, 11) can be tied together and then driven with a single external clock. If the approximate ratio $f_{CLK}/100$ is chosen (pin 12 is grounded), then with a 200 kHz clock, the cuftoff frequency, f_c, will be at 2 kHz with a 1.5% maximum error.

The filter schematic is shown in *Figure 16*.



TL/H/5645–11

FIGURE 16. 4th Order, 2 kHZ Lowpass Butterworth Filter

Applications Information (Continued)

With a ±5V supply, each output node of the IC (pins 1, 2, 3, 18, 19, 20) will swing to ±3.8V (MF10B) or ±3.2V (MF10C). The maximum gain of 1.306 occurs at pin 19 at $f_o \approx 2$ kHz. The input voltage amplitude should be limited to less than 7.6 Vp-p/1.306 = 5.8 Vp-p. If the Q of 1.306 section of the MF10 precedes the Q of 0.541 section, the maximum gain is at pin 1. This gain can be calculated from the expression for H_{OP} given in Definition of Terms, and equals 1.41.

Getting Optimum Cutoff Frequency, f_c, Accuracy (if needed):

In the previous example, an approximate 100:1 ratio was assumed. The true f_{CLK}/f_o ratio should be read from the curves, *Figures 13* and *14*. At 100:1 the normalized ratio to Q = 10 is: $f_{CLK}/f_o = 99.35$. For Q's of 0.541 and 1.306 this ratio becomes 99.35 − 0.75% = 98.6. For a 2 kHz f_c, the clock frequency should be 2 kHz × 98.6 = 197.2 kHz.

With an MF10B and a 197.2 kHz clock, the maximum error on the 2 kHz cutoff frequency is ±0.6% as indicated in the specs.

If only a 200 kHz is available in Mode 1a, the true value of f_c and its maximum error is: 200 kHz/(98.6 ± 0.6%) = 2028 ∓ 0.6%.

If only a 200 kHz is available and there is need for a tight tolerance cutoff frequency, then Mode 3 should be used instead of Mode 1a. The resistor ratios are:

1st Section, Q = 0.541	2nd Section, Q = 1.306
R2/R4 = 0.972	R2/R4 = 0.972
R3/R2 = 0.548	R3/R2 = 1.324
R4/R1 = 1	R4/R1 = 1

MF10 OFFSETS

The switched capacitor integrators of the MF10 have higher equivalent input offset than the typical R, C integrator of a discrete active filter. These offsets are created by a parasitic charge injection from the switches into the integrating capacitors; they are temperature and clock frequency independent and their sign is shown to be consistent from part to part. The input offsets of the CMOS op amps also add to the overall offset, but their contribution is very small. *Figure 17* shows an equivalent circuit from where output DC offsets can be calculated.

V_{OS1} = 0 mV to ±10 mV

V_{OS2} = charge injected offset plus op amp offset
≅ −120 mV to −170 mV (at 50:1)

V_{OS3} = charge injected offset plus op amp offset
≅ 100 mV to 150 mV (at 50:1)

The V_{OS2} and V_{OS3} numbers approximately double at 100:1.

Output Offsets

The DC offset at the BP output(s) of the MF10 is equal to the input offset of the lowpass switched capacitor integrator, V_{OS3}.

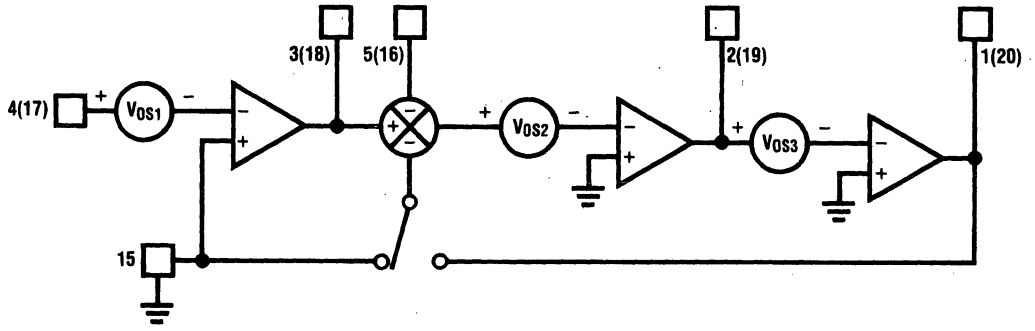
The DC offsets at the remaining outputs are roughly dependent upon the mode of operation and resistor ratios.

Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + \|H_{OLP}\|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$



TL/H/5645–12

FIGURE 17

Applications Information (Continued)

Mode 2 and Mode 5

$$V_{OS(N)} = \left(\frac{R2}{R_p} \pm 1\right) V_{OS1} \times \frac{1}{1+R2/R4} + V_{OS2}\frac{1}{1+R4/R2} - \frac{V_{OS3}}{Q\sqrt{1+R2/R4}};$$

$$R_p = R1//R2//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = -\frac{R4}{R2}\left(\frac{R2}{R3}V_{OS3} + V_{OS2}\right) + \frac{R4}{R2}\left(1+\frac{R2}{R_p}\right) V_{OS1};\ R_p = R1//R3//R4$$

Mode 1a

$$V_{OS(N.INV.BP)} = \left(1+\frac{1}{Q}\right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

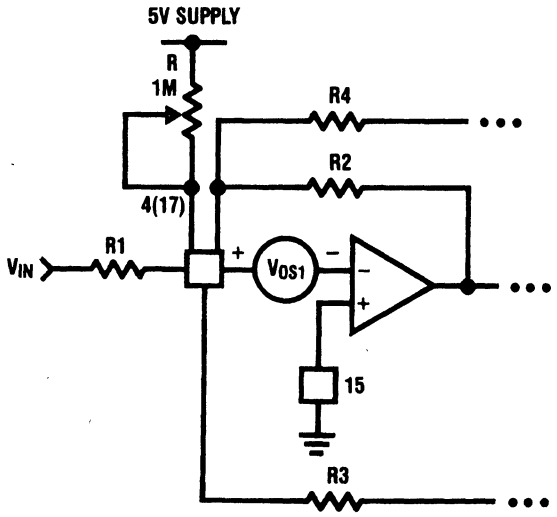
Comments on output DC offsets: For most applications, the outputs are AC coupled and the DC offsets are not bothersome unless large input voltage signals are applied to the filter. For instance, if the BP output is used and it is AC coupled, the remaining two outputs should not be allowed to saturate. If so, gain nonlinearities and f_o, Q errors will occur. For Mode 3 of operation a word of caution is necessary: by allowing small R2/R4 ratios and high Q, the LP output will exhibit a couple of volts of DC offset and an offset adjustment should be made.

An extreme example: Design a 1.76 kHz BP filter with a Q of 21 and a gain equal to unity. The MF10 will be driven with a 250 kHz clock, and it will be switched 50:1.

Resistor values: $\sqrt{\frac{R2}{R4}} = \frac{f_o}{f_{CLK}} \times 50 = 0.352;\ \frac{R2}{R4} = 0.124$

$$\frac{R3}{R2} = 21 \times \frac{1}{0.353} = 59.63;\ \frac{R3}{R1} = 1$$

Since R3/R2 is the highest resistor ratio, start with R2 = 10k, then R3 ≅ 600k, R1 ≅ 600k, R4 = 80k. Assuming $V_{OS1} = 2$ mV, $V_{OS2} = -150$ mV, $V_{OS3} = 150$ mV, the DC offset at the LP output is $V_{OS(LP)} = +1.2$V. The offset adjustment will be done by injecting a small amount of current into the inverting input of the first op amp, *Figure 18*. This will change the effect V_{OS1}, but the output DC offset of the HP and BP will remain unchanged.



TL/H/5645–13

FIGURE 18. V_{OS} Adjust Scheme

National Semiconductor

microCMOS

TP3052/TP3053/TP3054/TP3057 Monolithic Serial Interface CMOS CODEC/FILTER Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

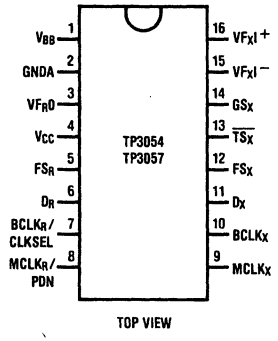
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- Complete CODEC and filtering system (COMBO) including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
- μ-law with signaling, TP3020 timing—TP3052
- μ-law with signaling, TP5116A family timing—TP3053
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- $\pm$5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

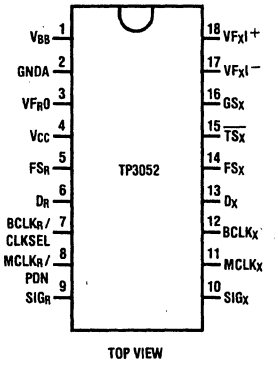
Connection Diagrams

Dual-In-Line Package



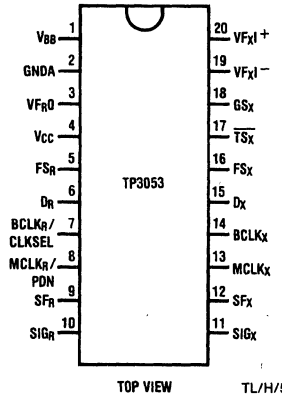
Order Number TP3054J or TP3057J
NS Package Number J16A

Dual-In-Line Package



Order Number TP3052J
NS Package Number J18A

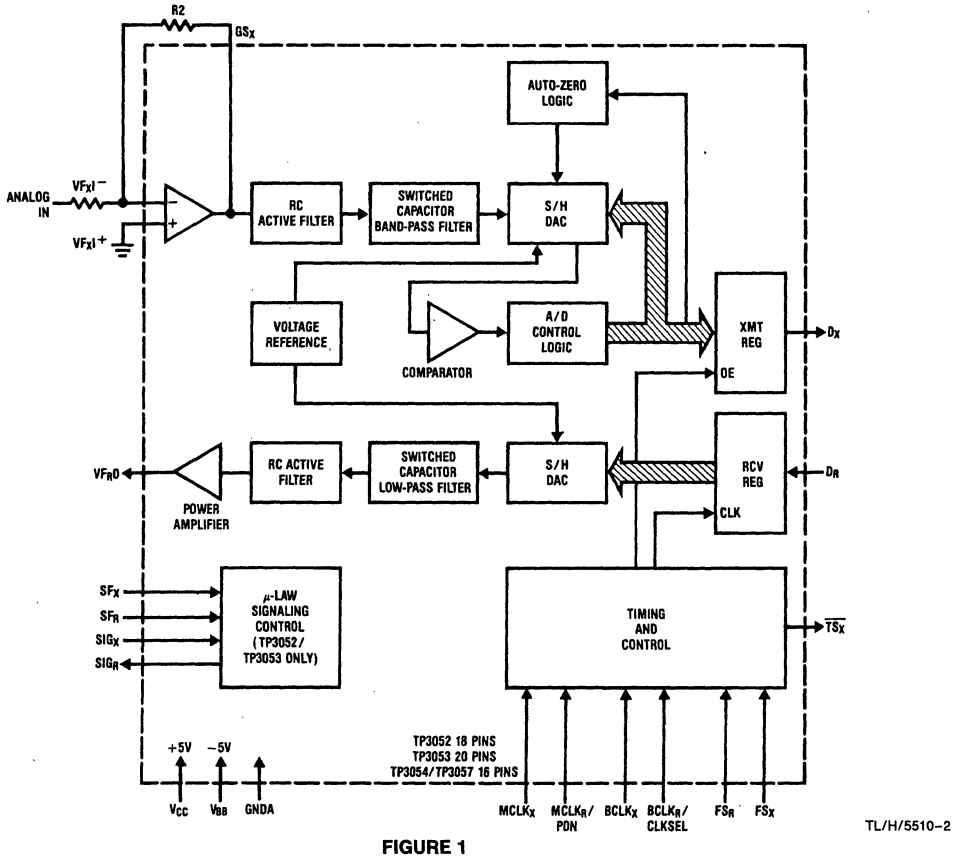
Dual-In-Line Package



TL/H/5510–1

Order Number TP3053J
NS Package Number J20A

Block Diagram



TL/H/5510–2

FIGURE 1

Pin Description

TP3052 Pin No.	TP3053 Pin No.	TP3054 TP3057 Pin No.	Name	Function
1	1	1	V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
2	2	2	GNDA	Analog ground. All signals are referenced to this pin.
3	3	3	VF_RO	Analog output of the receive filter.
4	4	4	V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
5	5	5	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
6	6	6	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
7	7	7	$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1).
8	8	8	$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.

Pin Description (Continued)

TP3052 Pin No.	TP3053 Pin No.	TP3054 TP3057 Pin No.	Name	Function
—	9	—	SF_R	When high during FS_R, this input indicates a receive signal frame.
9	10	—	SIG_R	The eighth bit of the PCM data appears at this output after each receive signaling frame.
10	11	—	SIG_X	Signal data input. Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
—	12	—	SF_X	When high during FS_X, this input indicates a transmit signaling frame.
11	13	9	$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
14	16	12	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
12	14	10	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
13	15	11	D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
15	17	13	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
16	18	14	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
17	19	15	VF_XI^-	Inverting input of the transmit input amplifier.
18	20	16	VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3057	TP3052 TP3053 TP3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

Functional Description (Continued)

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3052, 53, 54, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse (the same as the TP5116A family of CODECs). Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A-type) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

SIGNALING

The TP3052 and TP3053 μ-law COMBOs contain circuitry to insert and extract signaling information in the PCM data stream. The TP3052 is intended for short frame sync applications, and the TP3053 for long frame sync applications, although the TP3053 may also be used in short frame sync applications. The TP3054 and TP3057 have no provision for signaling.

Signaling for the TP3052 is accomplished by applying a frame sync pulse two bit clock periods long, as shown in *Figure 2*. With FS_X two bit clock periods long, the data present at SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With FS_R two bit clock periods long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as "½" to minimize noise and distortion. This short frame signaling may also be implemented using the TP3053, providing SF_R and SF_X are left open circuit or tied low. The TP3052 is not capable of inserting or extracting signaling information in the long frame mode.

Signaling for the TP3053 may be accomplished in either short or long frame sync mode. The short mode signaling is the same as the TP3052. For long frame signaling, two additional frame sync pulses are required, SF_X and SF_R, which indicate transmit and receive signaling frames, respectively. With an SF_X signaling frame sync, the data present at the SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With an SF_R signaling frame sync, the LSB of the PCM data at D_R will be latched and appear on the SIG_R output pin until the next signaling frame. The decoder will also do the "½" step interpretation to compensate for the loss of the LSB.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3052, TP3053, TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μS (due to the transmit filter) plus 125 μS (due to encoding delay), which totals 290 μS. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ-law (TP3052, TP3053, TP3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifer capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μS later the decoder DAC output is updated. The total decoder delay is ~ 10 μS (decoder update) plus 110 μS (filter delay) plus 62.5 μS (½ frame), which gives approximately 180 μS.

Absolute Maximum Ratings

V_{CC} to GNDA	7V	Voltage at any Digital Input or Output	$V_{CC}+0.3V$ to GNDA$-0.3V$
V_{BB} to GNDA	$-7V$	Operating Temperature Range	$-25°C$ to $+125°C$
Voltage at any Analog Input or Output	$V_{CC}+0.3V$ to $V_{BB}-0.3V$	Storage Temperature Range	$-65°C$ to $+150°C$
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Unless otherwise noted: $V_{CC}=5.0V\pm5\%$, $V_{BB}=-5V\pm5\%$, GNDA$=0V$, $T_A=0°C$ to 70°C; typical characteristics specified at $V_{CC}=5.0V$, $V_{BB}=-5.0V$, $T_A=25°C$; all signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, $I_L=3.2$ mA SIG_R, $I_L=1.0$ mA $\overline{TS_X}$, $I_L=3.2$ mA, Open Drain			0.4 0.4 0.4	V V V
V_{OH}	Output High Voltage	D_X, $I_H=-3.2$ mA SIG_R, $I_H=-1.0$ mA	2.4 2.4			V V
I_{IL}	Input Low Current	GNDA$\le V_{IN}\le V_{IL}$, All Digital Inputs	-10		10	μA
I_{IH}	Input High Current	$V_{IH}\le V_{IN}\le V_{CC}$	-10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA$\le V_O\le V_{CC}$	-10		10	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	$-2.5V\le V\le+2.5V$, VF_XI+ or VF_XI-	-200		200	nA
R_IXA	Input Resistance	$-2.5V\le V\le+2.5V$, VF_XI+ or VF_XI-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L\le10$ kΩ	±2.8			V
A_VXA	Voltage Gain	VF_XI+ to GS_X	5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		-20		20	mV
$V_{CM}XA$	Common-Mode Voltage		-2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	$VF_RO=\pm2.5V$	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		-200		200	mV
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current			0.5	1.5	mA
$I_{BB}0$	Power-Down Current			0.05	0.3	mA
$I_{CC}1$	Active Current			6.0	9.0	mA
$I_{BB}1$	Active Current			6.0	9.0	mA

Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	100		100	ns
t_{PB}	Period of Bit Clock		485	488	15,725	ns
t_{WBH}	Width of Bit Clock High	$V_{IH}=2.2V$	160			ns
t_{WBL}	Width of Bit Clock Low	$V_{IL}=0.6V$	160			ns
t_{RB}	Rise Time of Bit Clock	$t_{PB}=488$ ns			50	ns
t_{FB}	Fall Time of Bit Clock	$t_{PB}=488$ ns			50	ns
t_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		140	ns
t_{XDP}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	$C_L=0$ pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	$C_L=0$ pF to 150 pF	20		165	ns
t_{SSFF}	Set-Up Time from $SF_{X/R}$ High to $FS_{X/R}$	TP3053 Only	60			ns
t_{SSFB}	Set-Up Time from Signal Frame Sync High to $BCLK_{X/R}$ Clock	TP3053 Only	60			ns
t_{SSGB}	Set-Up Time from SIG_X to $BCLK_X$	TP3052 and TP3053	100			ns
t_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	TP3052 and TP3053	50			ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		50			ns
t_{DFSSG}	Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	Load = 50 pF plus 2 LSTTL Loads			300	ns
t_{HBSF}	Hold Time from $BCLK_{X/R}$ Low to Signaling Frame Sync	TP3053 Only	100			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

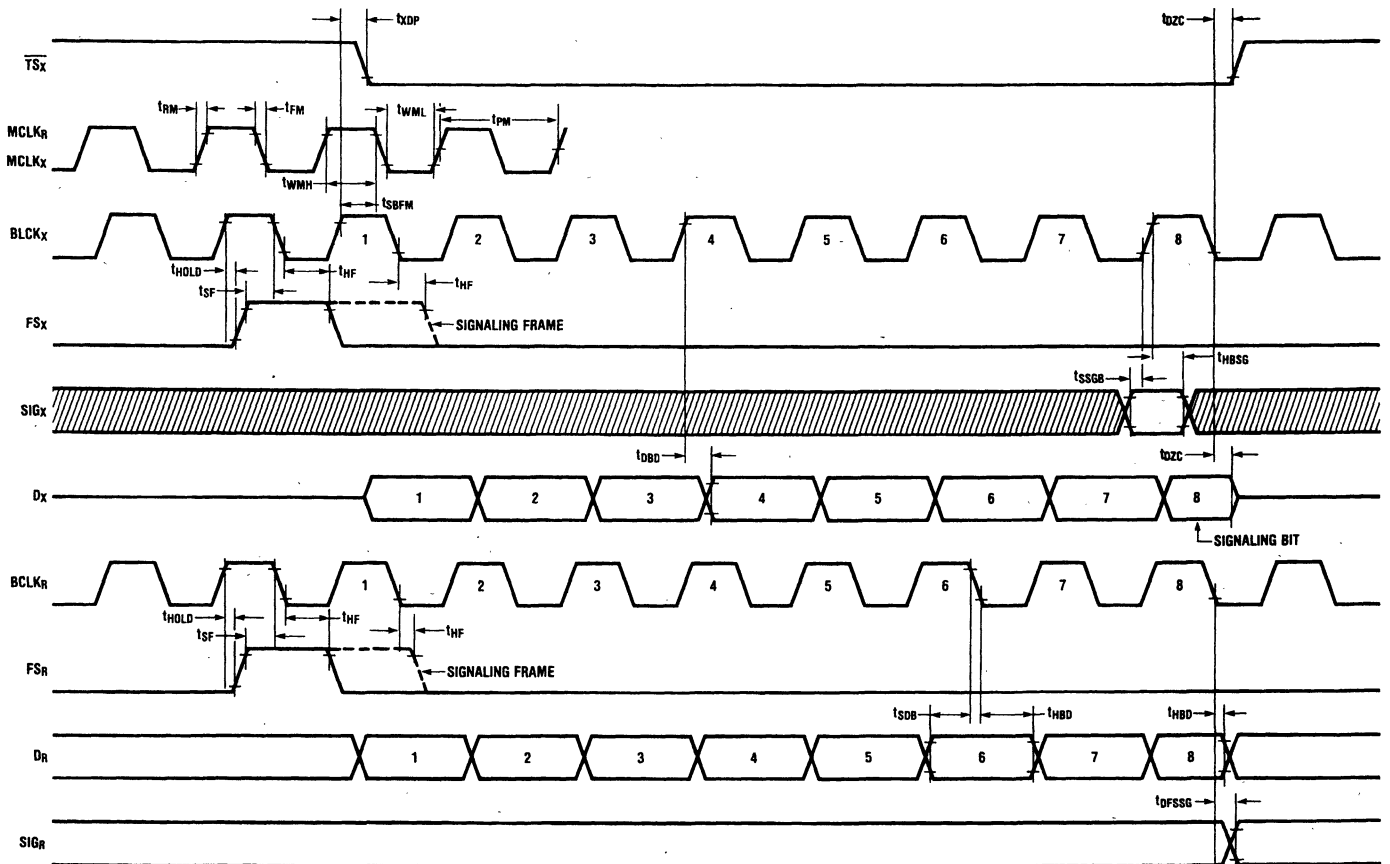
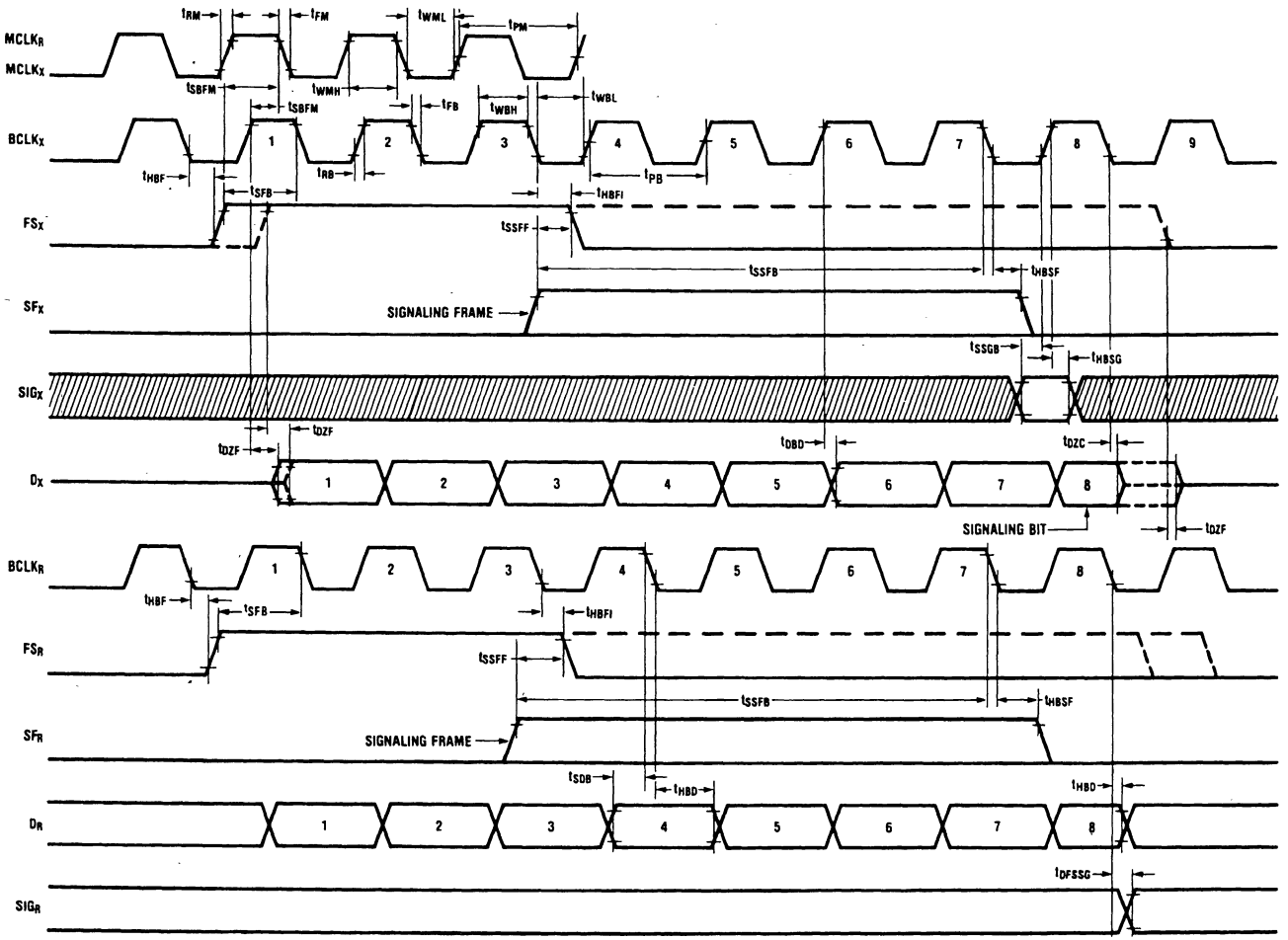


FIGURE 2. Short Frame Sync Timing

TL/H/5510–3



TL/H/5510–4

FIGURE 3. Long Frame Sync Timing

Transmission Characteristics (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0 TP3052, TP3053, TP3054 TP3057		 1.2276 1.2276		 Vrms Vrms
t_{MAX}		Max Overload Level TP3052, TP3053, TP3054 (3.17 dBm0) TP3057 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$ Input at $GS_X = 0$ dBm0 at 1020 Hz	−0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz − 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T_A = 0°C$ to $80°C$			±0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			±0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0 $VF_XI^+ = -40$ dBm0 to +3 dBm0 $VF_XI^+ = -50$ dBm0 to −40 dBm0 $VF_XI^+ = -55$ dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	−0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$T_A = 0°C$ to $80°C$			±0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$			±0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded—10 dBm0 Signal PCM Level = −40 dBm0 to + 3 dBm0 PCM Level = −50 dBm0 to −40 dBm0 PCM Level = −55 dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
V_{RO}	Receive Output Drive Level	$R_L = 600\Omega$	−2.5		2.5	V

Transmission Characteristics (Continued) (All Devices) Unless otherwise specified: $T_A = 0°C$ to 70°C, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μS
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	μS
		f = 600 Hz–800 Hz		120	145	μS
		f = 800 Hz–1000 Hz		50	75	μS
		f = 1000 Hz–1600 Hz		20	40	μS
		f = 1600 Hz–2600 Hz		55	75	μS
		f = 2600 Hz–2800 Hz		80	105	μS
		f = 2800 Hz–3000 Hz		130	155	μS
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μS
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		μS
		f = 1000 Hz–1600 Hz	−30	−20		μS
		f = 1600 Hz–2600 Hz		70	90	μS
		f = 2600 Hz–2800 Hz		100	125	μS
		f = 2800 Hz–3000 Hz		145	175	μS
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3052, TP3053, TP3054 $VF_XI^+ = 0V$		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3057 $VF_XI^+ = 0V$		−74	−67 (Note 1)	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3052, TP3053, TP3054 PCM Code Equals Alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3057 PCM Code Equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI^+ = 0$ Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$VF_XI^+ = 0$ Vrms, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms				
		f = 0 kHz–50 kHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	$VF_XI^+ = 0$ Vrms, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms				
		f = 0 kHz–50 kHz	40			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero, $V_{CC} = 5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz–4000 Hz	40			dBC
		f = 4 kHz–25 kHz	40			dB
		f = 25 kHz–50 kHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero, $V_{BB} = -5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz–4000 Hz	40			dBC
		f = 4 kHz–25 kHz	40			dB
		f = 25 kHz–50 kHz	36			dB

Transmission Characteristics (Continued) (All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz–3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO			−30	dB
		4600 Hz–7600 Hz			−30	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			−30	dB
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method Level = 3.0 dBm0	33			dBC
		= 0 dBm0 to −30 dBm0	36			dBC
		= −40 dBm0 XMT	29			dBC
		RCV	30			dBC
		= −55 dBm0 XMT	14			dBC
		RCV	15			dBC
SFD_X	Single Frequency Distortion, Transmit				−46	dB
SFD_R	Single Frequency Distortion, Receive				−46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, $VF_X^+ = -4$ dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			−41	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Steady PCM Code		−90	−75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz, $VF_XI = 0V$		−90	−70 (Note 2)	dB

Note 1: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Note 2: CT_{R-X} is measured with a −40 dBm0 activating signal applied at VF_XI^+.

ENCODING FORMAT AT D_X OUTPUT

	TP3052, TP3053, TP3054 μ-Law								TP3057 A-Law (Includes Even Bit Inversion)							
V_{IN} (at GS_X) = + Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = − Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Applications Information

POWER SUPPLIES

While the pins of the TP3050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

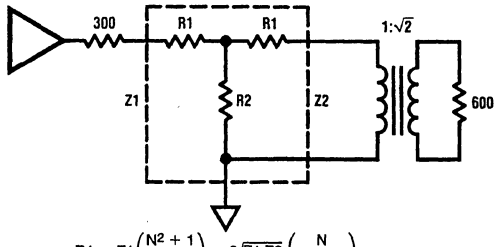
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

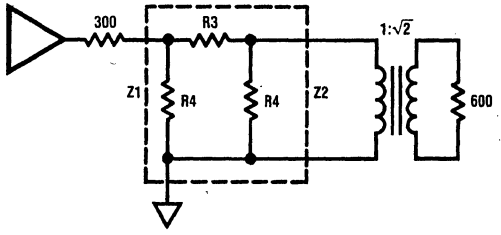
and

$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{SC} \bullet Z_{OC}}$$

Where Z_{SC} = impedance with short circuit termination
and Z_{OC} = impedance with open circuit termination

π-Pad Attenuator



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$$R3 = \sqrt{\frac{Z1 \cdot Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

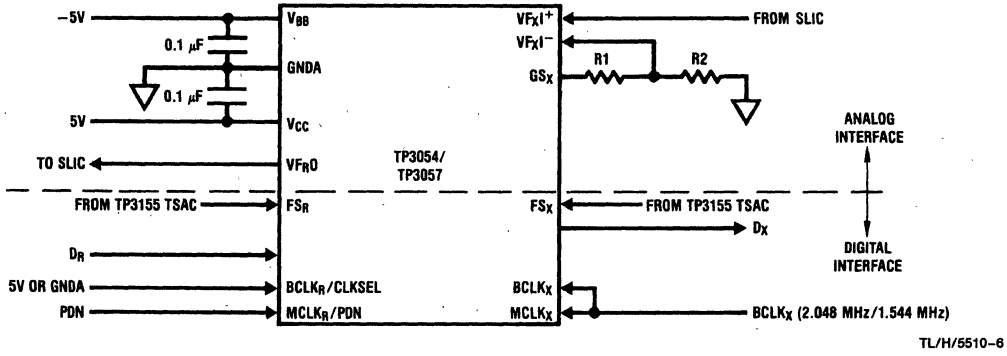
Note: See Application Note 370 for further details.

Applications Information (Continued)

TABLE II. Attentuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6l	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



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Note 1: XMIT gain $= 20 \times \log\left(\frac{R1+R2}{R2}\right)$, $(R1+R2) > 10\ K\Omega$.

FIGURE 4

National Semiconductor

PRELIMINARY

microCMOS

TP3064/TP3067 Monolithic Serial Interface CMOS CODEC/FILTER Combos

General Description

The TP3064 (μ-law) and TP3067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

Similar to the TP3050 family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ±6.6V across a balanced 600Ω load.

Also included is an Analog Loopback switch and $\overline{TS_X}$ output.

Features

- Complete CODEC and filtering system including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
  - — Receive push-pull power amplifiers
- μ-law—TP3064
- A-law—TP3067
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 70 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

Block Diagram

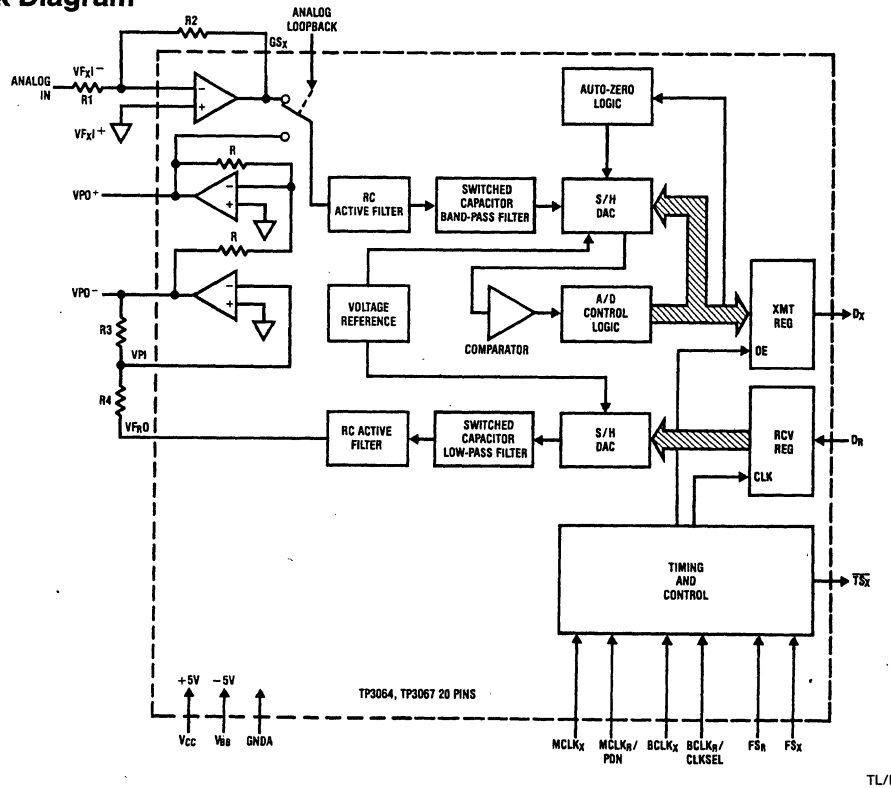

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FIGURE 1

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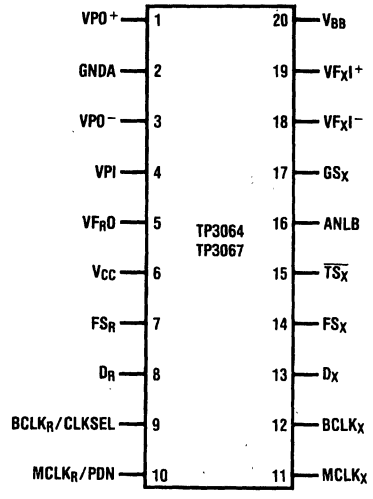
Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5070–2

Order Number TP3064J, TP3067J
See NS Package J20A

Pin Description

TP3064 TP3067 Pin No.	Name	Function
1	VPO+	The non-inverted output of the receive power amplifier.
2	GNDA	Analog ground. All signals are referenced to this pin.
3	VPO−	The inverted output of the receive power amplifier.
4	VPI	Inverting input to the receive power amplifier. Also powers down both amplifiers when connected to V_{BB}.
5	VF_RO	Analog output of the receive filter.
6	V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
7	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
8	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
9	$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table I).
10	$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.

Pin Description (Continued)

TP3064 TP3067 Pin No.	Name	Function
11	$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
12	$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
13	D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
14	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
15	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
16	ANLB	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO^+ output of the receive power amplifier.
17	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
18	VF_XI^-	Inverting input of the transmit input amplifier.
19	VF_XI^+	Non-inverting input of the transmit input amplifier.
20	V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into the power-down mode. All non-essential circuits are deactivated and the D_X, VF_RO, VPO^- and VPO^+ outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BLCK_X$ will be selected as the bit clock for both the transmit and receive directions. Table I indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3067	TP3064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHZ	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.544 MHz

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Functional Description (Continued)

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3067, or 1.536 MHZ, 1.544 MHz for the TP3064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table I are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse (the same as the TP5116A family of CODECs). Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A-type) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$($BCLK_X$ in synchronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 5*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3064) or A-law (TP3067) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

ENCODING FORMAT AT D_X OUTPUT

	TP3064 μ-Law								TP3067 A-Law (Includes Even Bit Inversion)							
V_{IN} = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Functional Description (Continued)

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3067) or μ-law (TP3064) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at VF_RO. The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5V peak output signal from the receive filter up to ±3.3V peak into an unbalanced 300Ω load, or ±4.0V into an unbalanced 15 kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$:1 turns ratio, as shown in *Figure 2*. A total peak power of 15.6 dBm can be delivered to the load plus termination.

Both power amplifiers can be powered down independently from the PDN input by connecting the VPI input to V_{BB}, saving approximately 12 mW of power.

Absolute Maximum Ratings

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	V_{CC}+0.3V to V_{BB}−0.3V
Voltage at any Digital Input or Output	V_{CC}+0.3V to GNDA−0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Unless otherwise noted: V_{CC}=5.0V±5%, V_{BB}=−5V±5%, GNDA=OV, T_A=0°C to 70°C; typical characteristics specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C; all signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current			0.5	1.5	mA
$I_{BB}0$	Power-Down Current			0.05	0.3	mA
$I_{CC}1$	Active Current	Power Amplifiers Active, VPI=0V		7.0	10.0	mA
$I_{BB}1$	Active Current	Power Amplifiers Active, VPI = 0V		7.0	10.0	mA
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, I_L=3.2 mA SIG_R, I_L=1.0 mA $\overline{TS_X}$, I_L=3.2 mA, Open Drain			0.4 0.4 0.4	V V V
V_{OH}	Output High Voltage	D_X, I_H=−3.2 mA SIG_R, I_H=−1.0 mA	2.4 2.4			V V
I_{IL}	Input Low Current	GNDA≤V_{IN}≤V_{IL}, All Digital Inputs	−10		10	μA
I_{IH}	Input High Current	V_{IH}≤V_{IN}≤V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA≤V_O≤V_{CC}	−10		10	μA

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Electrical Characteristics (Continued)

Unless otherwise noted: $V_{CC} = 5.0V \pm 5\%$; $V_{BB} = -5V \pm 5\%$, GNDA = 0V, $T_A = 0°C$ to 70°C; typical characteristics specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$; all signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	$-2.5V \le V \le +2.5V$, VF_XI+ or VF_XI-	−200		200	nA
R_IXA	Input Resistance	$-2.5V \le V \le +2.5V$, VF_XI+ or VF_XI-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L \ge 10$ kΩ	±2.8			V
A_VXA	Voltage Gain	VF_XI+ to GS_X	5000			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		−20		20	mV
$V_{CM}XA$	Common-Mode Voltage		−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	$VF_RO = \pm 2.5V$	10			kΩ
C_LRF	Load Capacitance	VF_RO to GNDA			25	pF
VOS_RO	Output DC Offset Voltage	VF_RO to GNDA	−200		200	mV
ANALOG INTERFACE WITH POWER AMPLIFIERS (ALL DEVICES)						
IPI	Input Leakage Current	$-1.0V \le VPI \le 1.0V$	−100		100	nA
RIPI	Input Resistance	$-1.0V \le VPI \le 1.0V$	10			MΩ
VIOS	Input Offset Voltage		−25		25	mV
ROP	Output Resistance	Inverting Unity-Gain at VPO+ or VPO−		1		Ω
F_C	Unity-Gain Bandwidth	Open Loop (VPO−)		400		kHz
C_LP	Load Capacitance	$R_L \ge 1500\Omega$ VPO+ or VPO− to GNDA			100	pF
		$R_L = 600\Omega$ VPO+ or VPO− to GNDA			500	pF
		$R_L = 300\Omega$ VPO+ or VPO− to GNDA			1000	pF
GA_P+	Gain, VPO− to VPO+	$R_L = 300\Omega$ VPO+ to GNDA, Level at VPO− = 1.77 Vrms (+3 dBm0)		−1		V/V
$PSRR_P$	Power Supply Rejection of V_{CC} or V_{BB}	VPO− Connected to VPI				
		0 kHz−4 kHz	60			dB
		0 kHz−50 kHz	36			dB

Timing Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X				ns
t_{PB}	Period of Bit Clock		485	488	15,725	ns
t_{WBH}	Width of Bit Clock High	$V_{IH}=2.2V$	160			ns
t_{WBL}	Width of Bit Clock Low	$V_{IL}=0.6V$	160			ns
t_{RB}	Rise Time of Bit Clock	$t_{PB}=488$ ns			50	ns
t_{FB}	Fall Time of Bit Clock	$t_{PB}=488$ ns			50	ns
t_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t_{SFB}	Set-Up Time for Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	0		180	ns
t_{XDP}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	$C_L=0$ pF to 150 pF	20		165	ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		50			ns
t_{DFSSG}	Delay Time from $BCLK_{R/X}$ Low to SIG_R Valid	Load = 50 pF plus 2 LSTTL Loads			300	ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

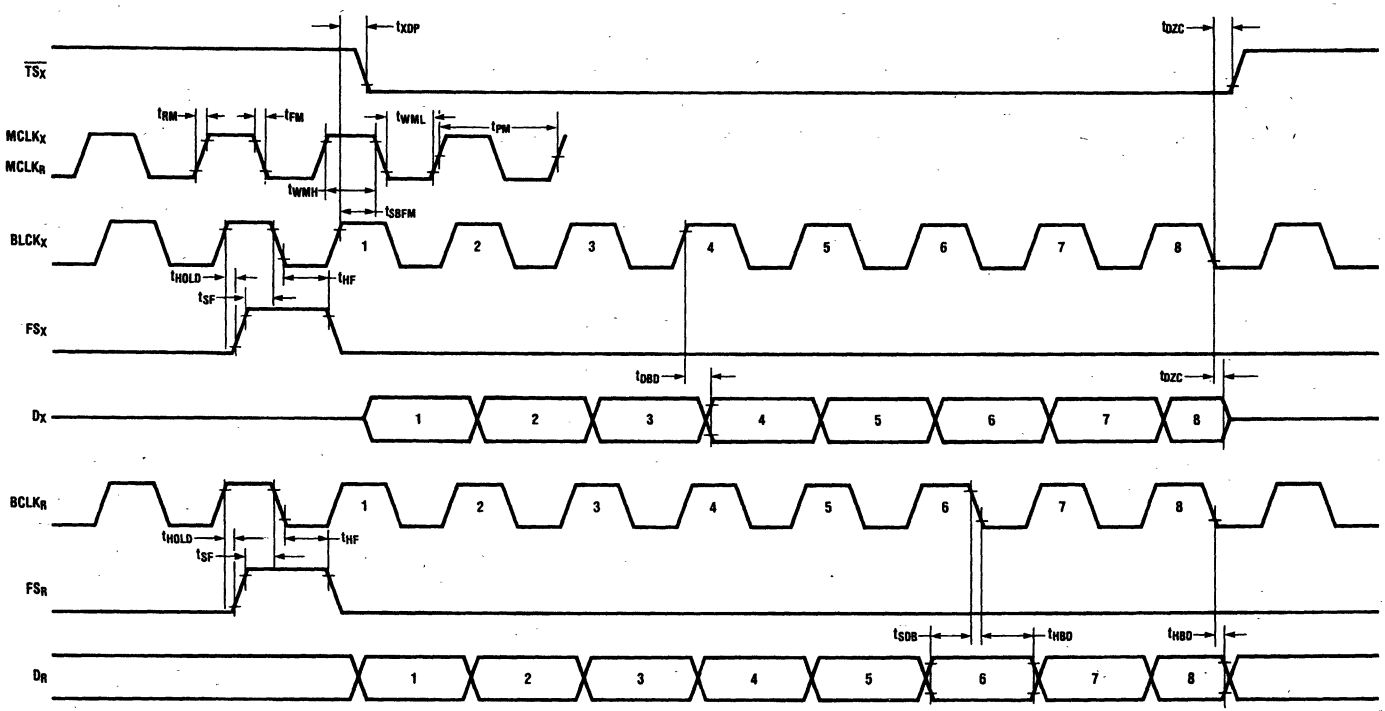

FIGURE 2. Short Frame Sync Timing

TL/H/5970-3

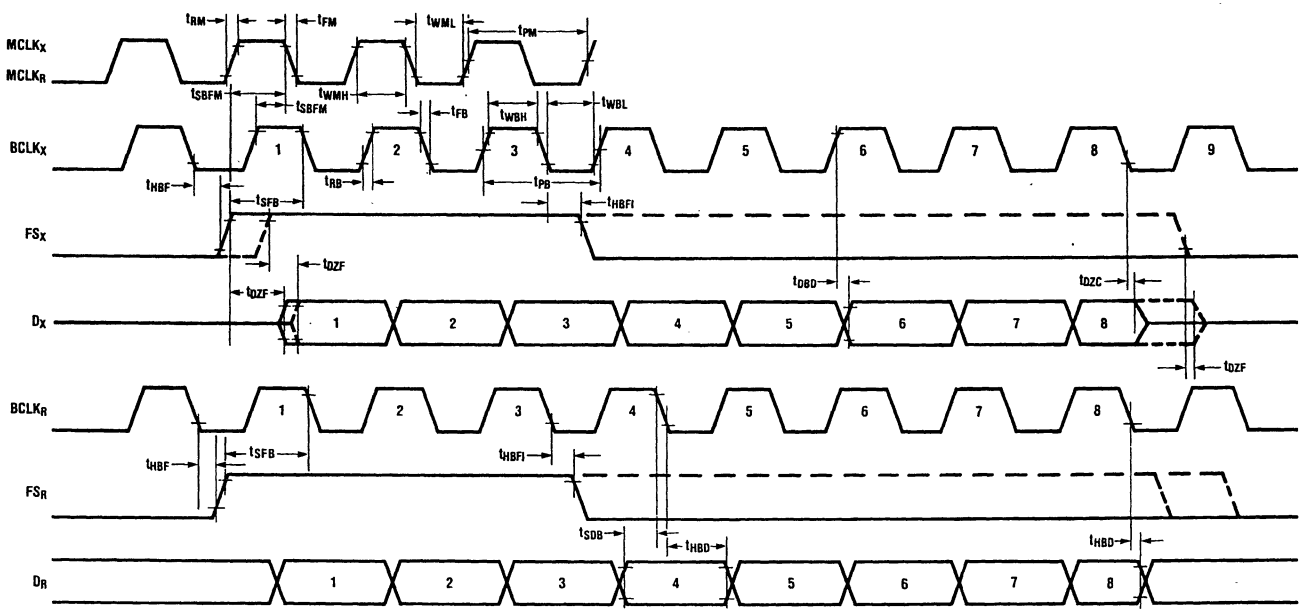

FIGURE 3. Long Frame Sync Timing

TL/H/5070–4

Transmission Characteristics (All Devices) Unless otherwise specified: T_A = 0°C to 70°C, V_{CC} = 5V±5%, V_{BB} = −5V±5%, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0 TP3064 TP3067		 1.2276 1.2276		 Vrms Vrms
t_{MAX}		Max Transmit Overload Level TP3064 (3.17 dBm0) TP3067 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input at GS_X=0 dBm0 at 1020 Hz	−0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16 Hz f=50 Hz f=60 Hz f=200 Hz f=300 Hz-3000 Hz f=3300 Hz f=3400 Hz f=4000 Hz f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 −1.8 −0.15 −0.35 −0.7		−40 −30 −26 −0.1 0.15 0.05 0 −14 −32	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T_A=0°C to 70°C			±0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V_{CC}=5V±5%, V_{BB}=−5V±5%			±0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level=−10 dBm0 VF_XI^+=−40 dBm0 to +3 dBm0 VF_XI^+=−50 dBm0 to −40 dBm0 VF_XI^+=−55 dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	−0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0 Hz to 3000 Hz f=3300 Hz f=3400 Hz f=4000 Hz	−0.15 −0.35 −0.7		0.15 0.05 0 −14	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T_A=0°C to 70°C			±01.	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CC}=5V±5%, V_{BB}=−5V±5%			±0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded - 10 dBm0 Signal PCM Level=−40 dBm0 to +3 dBm0 PCM Level=−50 dBm0 to −40 dBm0 PCM Level=−55 dBm0 to −50 dBm0	 −0.2 −0.4 −1.2		 0.2 0.4 1.2	 dB dB dB
V_{RO}	Receive Filter Output at VF_RO	RL=10 kΩ	−2.5		2.5	V

Transmission Characteristics (Continued) (All Devices) Unless otherwise specified: T_A = 0°C to 70°C, V_{CC} = 5V±5%, V_{BB} = −5V±5%, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f=1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f=500 Hz−600 Hz		195	220	μs
		f=600 Hz−800 Hz		120	145	μs
		f=800 Hz−1000 Hz		50	75	μs
		f=1000 Hz−1600 Hz		20	40	μs
		f=1600 Hz−2600 Hz		55	75	μs
		f=2600 Hz−2800 Hz		80	105	μs
		f=2800 Hz−3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f=1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f=500 Hz−1000 Hz	−40	−25		μs
		f=1000 Hz−1600 Hz	−30	−20		μs
		f=1600 Hz−2600 Hz		70	90	μs
		f=2600 Hz−2800 Hz		100	125	μs
		f=2800 Hz−3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3064 VF_XI^+ = 0V		12	15	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3067 VF_XI^+ = 0V		−74	−69 (Note 1)	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3064 PCM Code Equals Alternating Positive and Negative Zero		8	11	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3067 PCM Code Equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f=0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI^+ = 0 Vrms, V_{CC}=5.0 V_{DC}+100 mVrms f=0 kHz−50 kHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI^+ = 0 Vrms, V_{BB}=−5.0 V_{DC}+ 100 mVrms f=0 kHz−50 kHz	40			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC}=5.0 V_{DC}+100 mVrms				
		f=0 Hz−4000 Hz	40			dBC
		f=4 kHz−25 kHz	40			dB
		f=25 kHz−50 kHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB}=−5.0 V_{DC}+100 mVrms				
		f=0 Hz−4000 Hz	40			dBC
		f=4 kHz−25 kHz	40			dB
		f=25 kHz−50 kHz	36			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz−3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO				
		4600 Hz–7600 Hz			−32	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			−32	dB

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Transmission Characteristics (Continued)

(All Devices) Unless otherwise specified: T_A = 0°C to 70°C, V_{CC} = 5V±5%, V_{BB} − 5V±5%, GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X	Signal to Total Distortion	Sinusoidal Test Method				
STD_R	Transmit or Receive Half-Channel	Level = 3.0 dBm0	33			dBC
		= 0 dBm0 to −30 dBm0	36			dBC
		= −40 dBm0 XMT	29			dBC
		RCV	30			dBC
		= −55 dBm0 XMT	14			dBC
		RCV	15			dBC
SFD_X	Single Frequency Distortion, Transmit				−46	dB
SFD_R	Single Frequency Distortion, Receive				−46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz−3400 Hz			−41	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk	f = 300 Hz−3000 Hz, D_R = Steady PCM Code		−90	−75	dB
CT_{R-X}	Receive to Transmit Crosstalk	f = 300 Hz−3000 Hz, VF_XI = 0V		−90	−70 (Note 2)	dB
POWER AMPLIFIERS						
V_{OL}	Maximum 0 dBm0 Level for Better than ±0.1 dB Linearity Over the Range −10 dBm0 to +3 dBm0	Balanced Load, R_L Connected Between VPO^+ and VPO^-				
		R_L = 600Ω	3.3			Vrms
		R_L = 1200Ω	3.5			Vrms
		R_L = 30 kΩ	4.0			Vrms
S/D_P	Signal/Distortion	R_L = 600Ω, 0 dBm0	50			dB

Note 1: Measured by extrapolation from the distortion test result.

Note 2: CT_{R-X} is measured with a −40 dBm0 activating signal applied at VF_XI^+.

Applications Information

POWER SUPPLIES

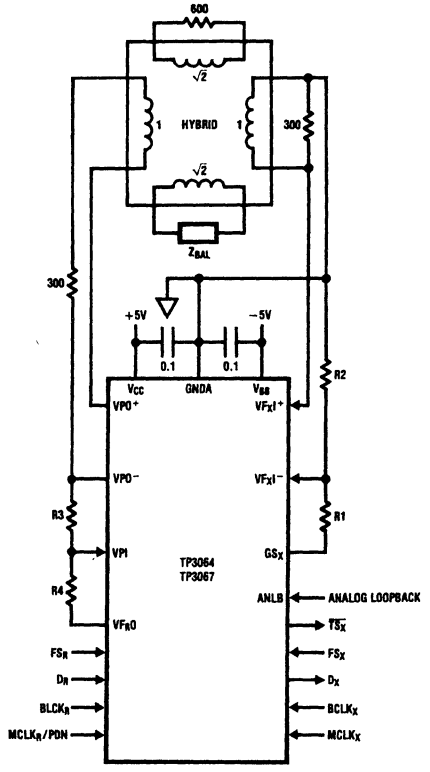
While the pins of the TP3060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in start formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

Note: See Application Note 370 for further details

Typical Asynchronous Application



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Note 1: Transmit gain = $20 \times \log \left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10\ k\Omega$

Note 2: Receive gain = $20 \times \log \left(\frac{2 \times R3}{R4}\right)$, $R4 \geq 10\ k\Omega$

FIGURE 2

Section 10

Building Blocks

Section Contents

Other Building Blocks

National Semiconductor

PRELIMINARY

LF13006, LF13007 Digital Gain Set

General Description

The LF13006, LF13007 are precision digital gain sets used for accurately setting non-inverting op amp gains. Gains are set with a 3-bit digital word which can be latched in with $\overline{WR}$ and $\overline{CS}$ pins. All digital inputs are TTL and CMOS compatible.

The LF13006 shown below will set binary scaled gains of 1, 2, 4, 8, 16, 32, 64, and 128. The LF13007 will set gains of 1, 2, 5, 10, 20, 50, and 100 (a common attenuator sequence). In addition, both versions have several taps and two uncommitted matching resistors which allow customization of the gain.

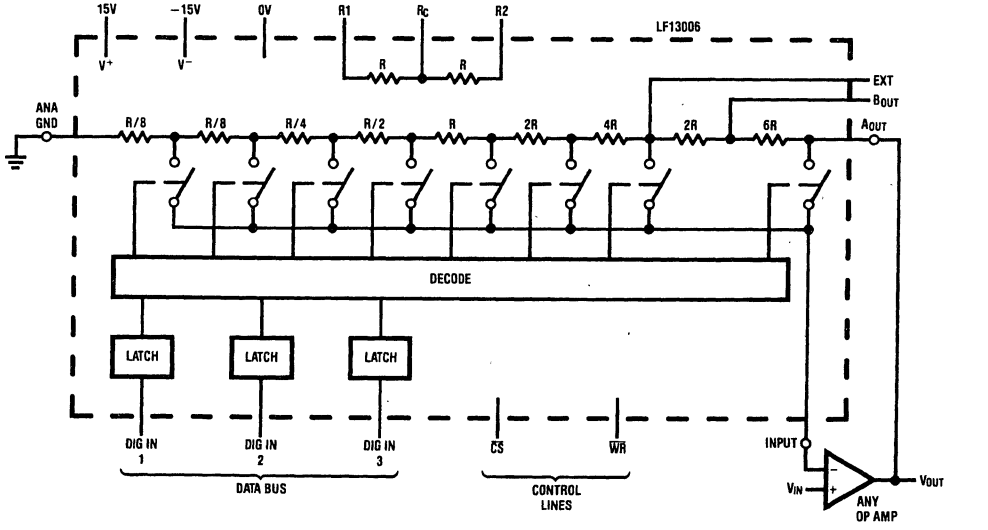
The gains are set with precision thin film resistors. The low temperature coefficient of the thin film resistors and their excellent tracking result in gain ratios which are virtually independent of temperature.

The LF13006, LF13007 used in conjunction with an amplifier not only satisfies the need for a digitally programmable amplifier in microprocessor based systems, but is also useful for discrete applications, eliminating the need to find 0.5% resistors in the ratio of 100 to 1 which track each other over temperature.

Features

- TTL and CMOS compatible logic levels
- Microprocessor compatible
- Gain error 0.5% max
- Binary or scope knob gains
- Wide supply range + 5V to ± 18V
- Packaged in 16-pin DIP

Block Diagram and Typical Application (LF13006)



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Note: R ≅ 15 kΩ

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Absolute Maximum Ratings

Supply Voltage, V+ to V−	36V	Analog Voltage	V+ to V− + 2V
Supply Voltage, V+ to GND	25V	Operating Temperature Range	−40°C to +85°C
Voltage at Any Digital Input	V+ to GND		

Electrical Characteristics (Note 1)

Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limit)
Gain Error	A_{OUT} = ±10V ANA GND = 0V I_{INPUT} < 10 nA	0.3	0.5	**0.5**	%(max)
Gain Temperature Coefficient	A_{OUT} = ±10V ANA GND = 0V	0.001			%/°C
Digital Input Voltage Low High		 1.4 1.6	 0.8 2.0	 **0.8** **2.0**	 V(max) V(min)
Digital Input Current Low High	 V_{IL} = 0V V_{IH} = 5V	 −35 0.0001	 −100 1	 **−100** **1**	 μA(max) μA(max)
Positive Power Supply Current	All Logic Inputs Low	3	5	**5**	mA(max)
Negative Power Supply Current	All Logic Inputs Low	−2	−5	**−5**	mA(max)
$\overline{\text{Write}}$ Pulse Width, t_W	V_{IL} = 0V, V_{IH} = 5V	40		**100**	ns(min)
$\overline{\text{Chip Select}}$ Set-Up Time, t_{CS}	V_{IL} = 0V, V_{IH} = 5V	60		**120**	ns(min)
$\overline{\text{Chip Select}}$ Hold Time, t_{CH}	V_{IL} = 0V, V_{IH} = 5V	0		**0**	ns(min)
DIG IN Set-Up Time, t_{DS}	V_{IL} = 0V, V_{IH} = 5V	80		**150**	ns(min)
DIG IN Hold Time, t_{DH}	V_{IL} = 0V, V_{IH} = 5V	0		**0**	ns(min)
Switching Time for Gain Change	(Note 4)	200			ns(max)
Switch On Resistance		3			kΩ
Unit Resistance, R		15	12–18		kΩ
R1 and R2 Mismatch		0.3	0.5	**0.5**	%(max)
R1/R2 Temperature Coefficient		0.001			%/°C

Note 1: Parameters are specified at V+ = 15V and V− = −15V. Min V+ to ground voltage is 5V. Min V+ to V− voltage is 5V. **Boldface numbers apply at temperature extremes.** All other numbers apply at $T_A = T_j = 25°C$.

Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature. These limits are not used to calculate outgoing quality levels.

Note 4: Settling time for gain change is the switching time for gain change plus settling time (see section on Settling Time).

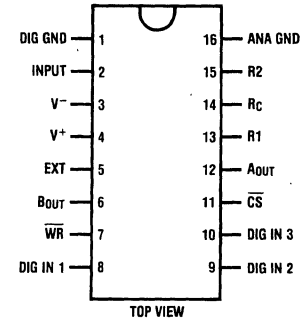
Note 5: $\overline{\text{WR}}$ minimum high threshold voltage increases to 2.4V under the extreme conditions when all three digital inputs are simultaneously taken from 0V to 5V at a slew rate of greater than 500V/μS.

GAIN TABLE

Digital Input	Gain			
	LF13006		LF13007	
	A_{OUT}	B_{OUT}	A_{OUT}	B_{OUT}
000	1	1	1	1
001	2	1.25	1.25	1
010	4	2.5	2	1.6
011	8	5	5	4
100	16	10	10	8
101	32	20	20	16
110	64	40	50	40
111	128	80	100	80

Connection Diagram

Dual-In-Line Package

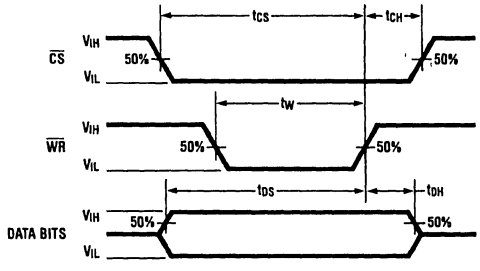


TOP VIEW

TL/H/5114–2

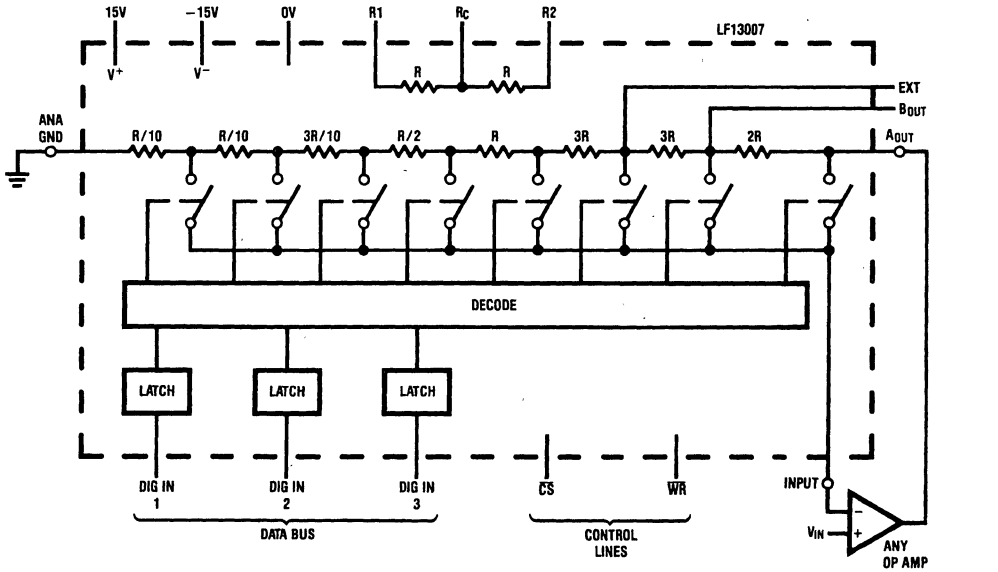
Order Numbers LF13006, LF13007
See NS Packages D16C, N16A

Switching Waveforms



TL/H/5114–3

Block Diagram and Typical Application (Continued) (LF13007)



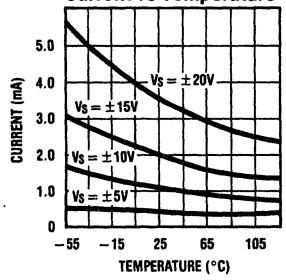
TL/H/5114–4

Note: R ≅ 15 kΩ

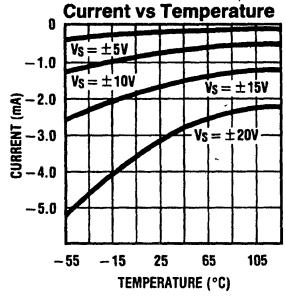
S 10

Typical Performance Characteristics

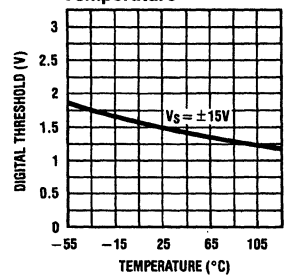
Positive Power Supply Current vs Temperature



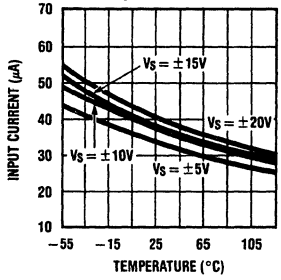
Negative Power Supply Current vs Temperature



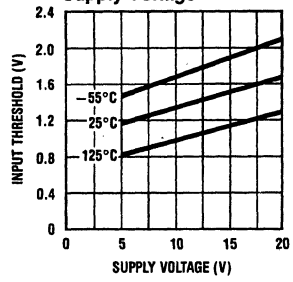
Digital Input Threshold vs Temperature



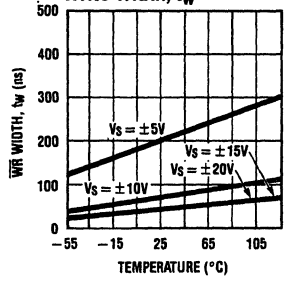
Logical 0 Input Bias Current vs Temperature



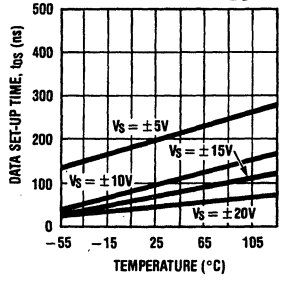
Digital Input Threshold vs Supply Voltage



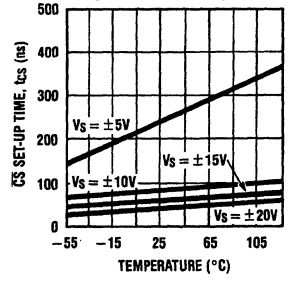
Write Width, t_W



Data Set-Up Time, t_{DS}



Chip Select Set-Up Time, t_{CS}



TL/H/5114–5

Application Information

FLOW-THROUGH OPERATION

THE LF13006, LF13007 can be operated with control lines $\overline{CS}$ and $\overline{WR}$ grounded. In this mode new data on the digital inputs will immediately set the new gain value. Input data cannot be latched in this mode.

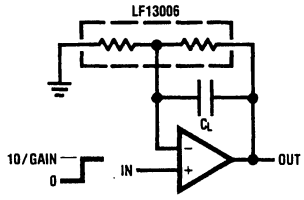
INPUT CURRENT

Current flowing through the input (pin 2) due to bias current of the op amp will result in a gain error due to switch impedance. Normally this error is very small. For example, 10 nA of bias current flowing through 3 kΩ of switch resistance will result in an error of 30 μV at the summing node. However, applications which have significant current flowing through the input must take this effect into account.

SETTLING TIME

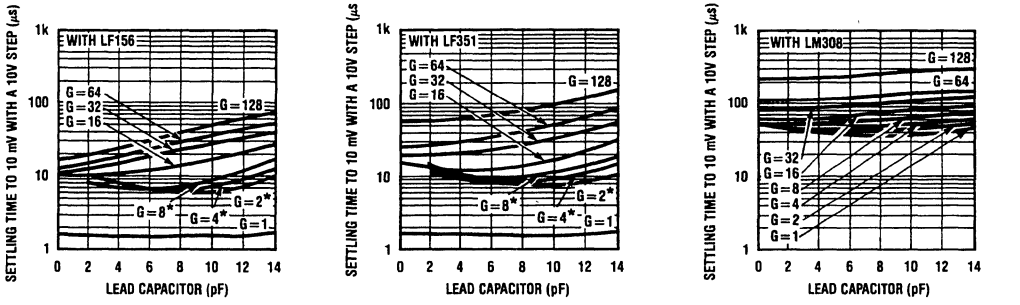
Settling time is a function of the particular op amp used with the LF13006/7 and the gain which is taken. It can be optimized and stability problems can be prevented through the use of a lead capacitor from the inverting input to the output of the amplifier. A lead capacitor is effective whenever the feedback around an amplifier is resistive, whether with discrete resistors or with the LF13006/7. This phenomenon is the result of the feedback pole created by the parallel resistance and capacitance from the inverting input of the op amp to AC ground.

Settling Time Test Circuit



TL/H/5114–6

Typical Settling Time Curves



TL/H/5114–7

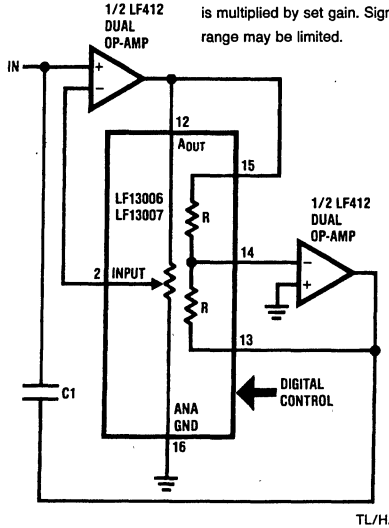
* Unstable at C_L less than 2 pF

Typical Applications

Variable Capacitance Multiplier

$C_{effective}$ = C1(gain set #)

Note: Output swing at input op amp is multiplied by set gain. Signal range may be limited.



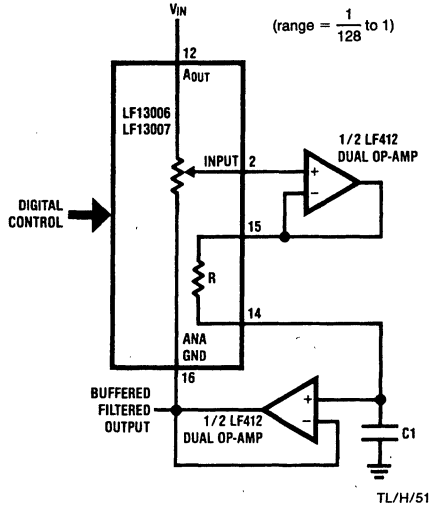
TL/H/5114–8

Variable Time Constant Filter

Time constant = $\frac{R}{N}C1$

N = setting of LF13006

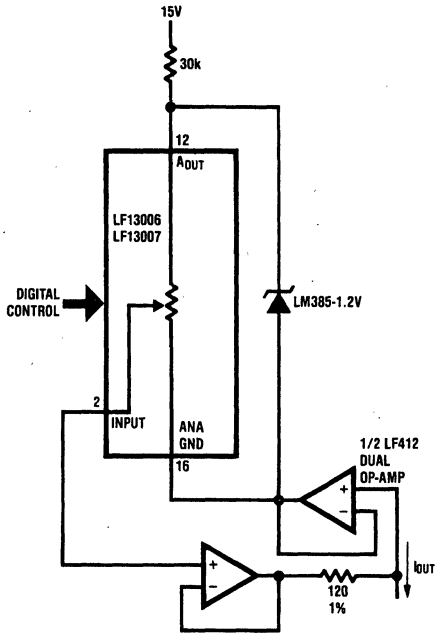
(range = $\frac{1}{128}$ to 1)



TL/H/5114–9

Typical Applications (Continued)

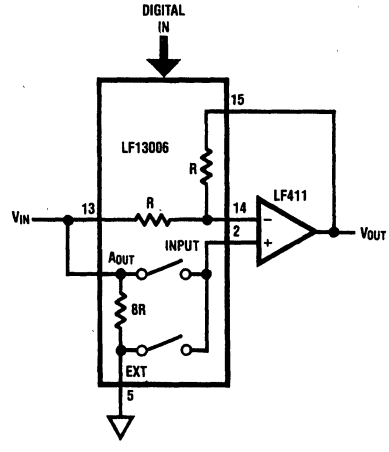
Programmable Current Source



TL/H/5114–10

$$I_{OUT} = \frac{1.2V}{120\Omega}\left[\frac{1}{\text{gain set \#}}\right]$$

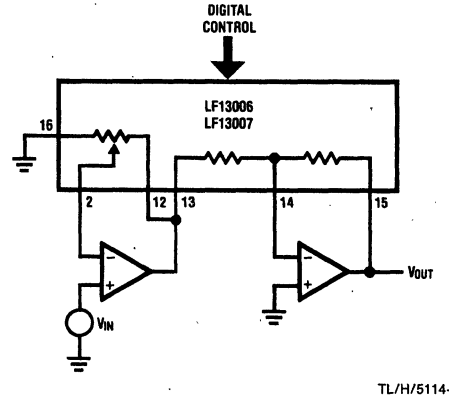
Switchable Gain of ±1



TL/H/5114–11

Note: Digital code = 000, $V_{OUT} = V_{IN}$;
Digital code = 001, $V_{OUT} = -V_{IN}$

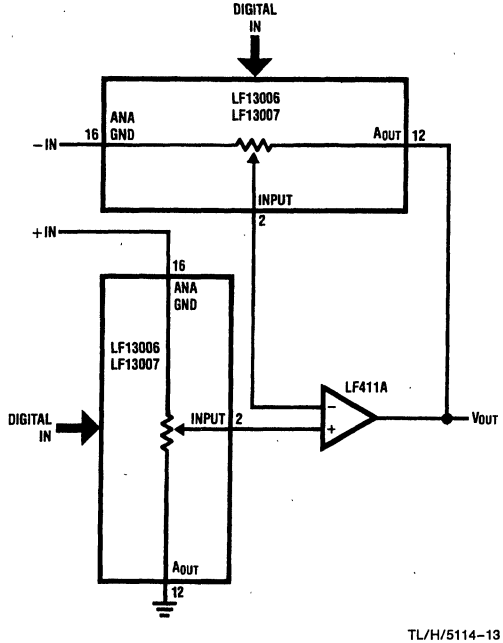
Inverting Gains



TL/H/5114–12

Inverting gain with high input impedance can be obtained with the LF13006, LF13007 by using the two on-board resistors and a dual op amp as shown.

Programmable Differential Amp

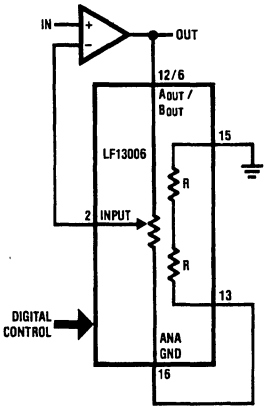


TL/H/5114–13

Note 1: Actual gain = set gain − 1 since LF13006s are in "inverting mode".
Note 2: Set gain must be same on both LF13006s.

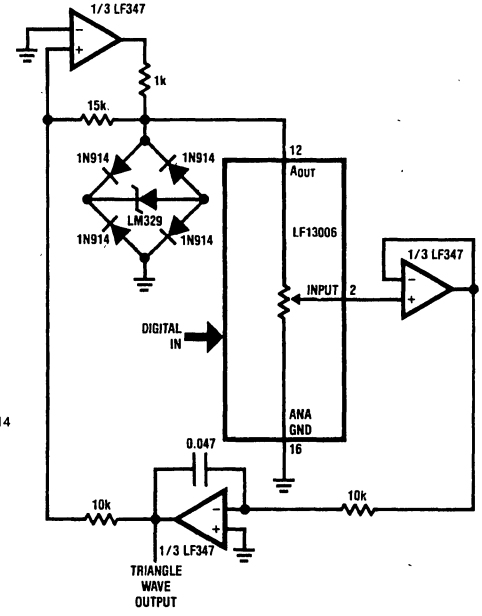
Typical Applications (Continued)

Altered Gain Range



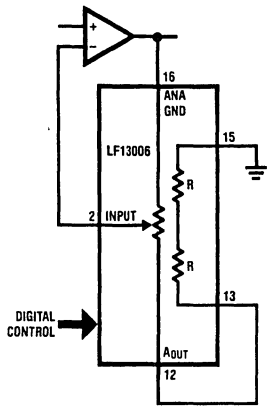
TL/H/5114–14

One Octave per Bit Function Generator



TL/H/5114–15

Variable Gains of Almost 1



TL/H/5114–16

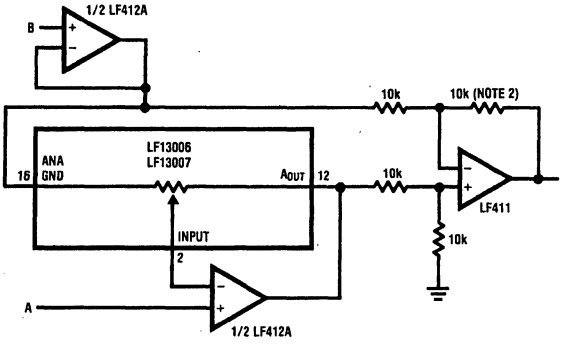
GAINS

A_{OUT}	B_{OUT}
1	1
1.8	1.2
3	2
4.5	3
6	4
7.2	4.8
8	5.33
8.47	5.65

GAINS

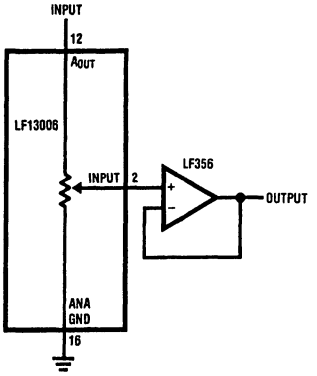
9
1.8
1.29
1.125
1.059
1.029
1.014
1.007

Programmable Instrumentation Amp



TL/H/5114–17

Attenuator (0 dB to −42 dB in 6 dB steps)



TL/H/5114–18

Note 1: $V_{OUT} = N\,(A - B)$, N = set gain.

Note 2: All 10k resistors 0.1% matched.

National Semiconductor

LM1851 Ground Fault Interrupter

General Description

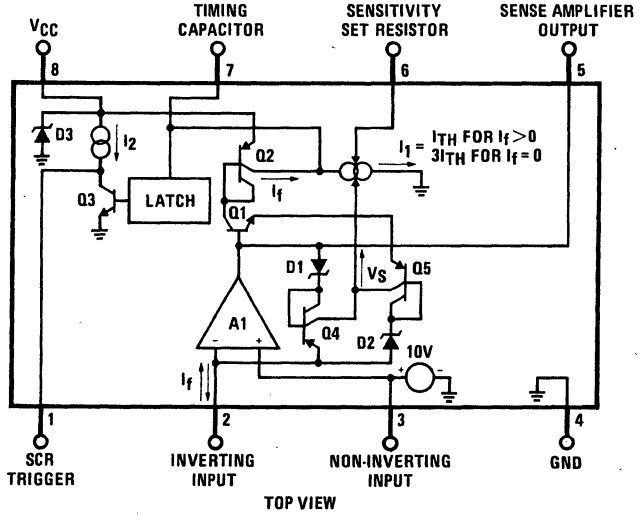
The LM1851 is designed to provide ground fault protection for AC power outlets in consumer and industrial environments. Ground fault currents greater than a presettable threshold value will trigger an external SCR-driven circuit breaker to interrupt the AC line and remove the fault condition. In addition to detection of conventional hot wire to ground faults, the neutral fault condition is also detected.

Full advantage of the U.S. UL943 timing specification is taken to insure maximum immunity to false triggering due to line noise. Special features include circuitry that rapidly resets the timing capacitor in the event that noise pulses introduce unwanted charging currents and a memory circuit that allows firing of even a sluggish breaker on either half-cycle of the line voltage when external full-wave rectification is used.

Features

- Internal power supply shunt regulator
- Externally programmable fault current threshold
- Externally programmable fault current integration time
- Direct interface to SCR
- Operates under line reversal; both load vs line and hot vs neutral
- Detects neutral line faults

Block and Connection Diagram



TL/H/5177–1

Order Number LM1851
See NS Package N08E

Absolute Maximum Ratings

Supply Current	19 mA	Storage Temperature Range	−55°C to +150°C
Power Dissipation (Note 1)	570 mW	Lead Temp. (Soldering, 10 seconds)	300°C
Operating Temperature Range	−40°C to +70°C		

DC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1, With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1, Without Fault		100	240	mV
Output Saturation Resistance	Pin 1, Without Fault		100		Ω
Output External Current Sinking Capability	Pin 1, Without Fault, $V_{pin\ 1}$ Held to 0.3V (Note 4)	2.0	5		mA
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault and Fault Conditions	2.0	2.8	3.6	μA/μA

AC Electrical Characteristics $T_A = 25°C$, $I_{SS} = 5$ mA

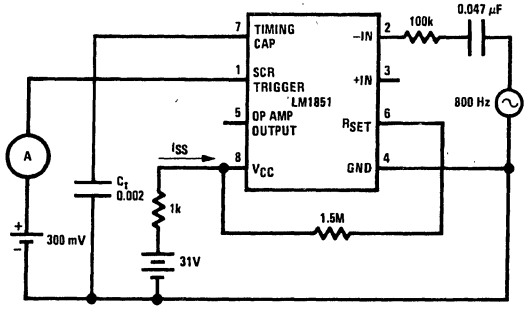
Parameter	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity	*Figure 1* (Note 3)	3	5	7	mA
Normal Fault Trip Time	500Ω Fault, *Figure 2* (Note 2)		18		ms
Normal Fault with Grounded Neutral Fault Trip Time	500Ω Normal Fault, 2Ω Neutral, *Figure 2* (Note 2)		18		ms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

Note 2: Average of 10 trials.

Note 3: Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity will be necessary.

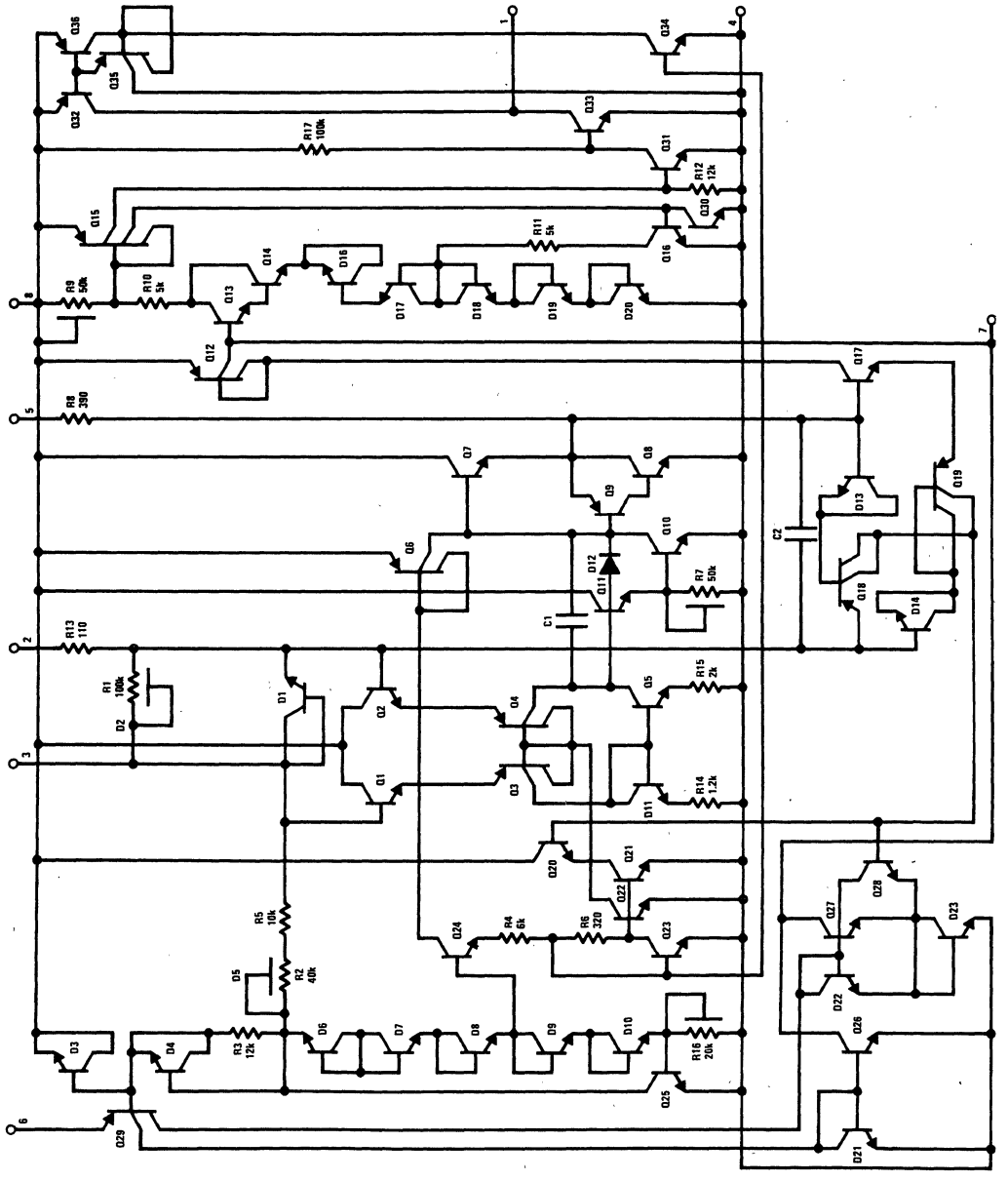
Note 4: This externally applied current is in addition to the internal "output drive current" source.



TL/H/5177–2

FIGURE 1. Normal Fault Sensitivity Test Circuit

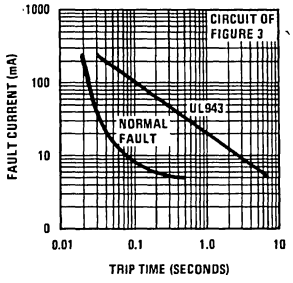
Internal Schematic Diagram



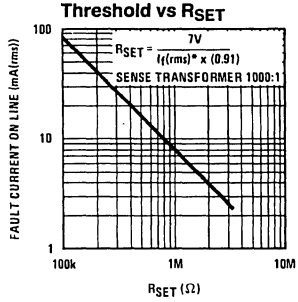
TL/H/5177–3

Typical Performance Characteristics

Average Trip Time vs Fault Current

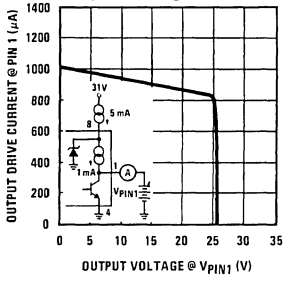


Normal Fault Current Threshold vs R_{SET}

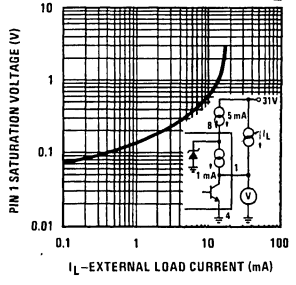


* See Block Diagram

Output Drive Current vs Output Voltage



Pin 1 Saturation Voltage vs External Load Current, I_L



TL/H/5177–4

Circuit Description

(Refer to Block and Connection Diagram)

The LM1851 operates from 26V as set by an internal shunt regulator, D3. In the absence of a fault ($I_f = 0$) the feedback path status signal (V_S) is correspondingly zero. Under these conditions the capacitor discharge current, I_1, sits quiescently at three times its threshold value, I_{TH}, so that noise induced charge on the timing capacitor will be rapidly removed. When a fault current, I_f, is induced in the secondary of the external sense transformer, the operational amplifier, A1, uses feedback to force a virtual ground at the input as it extracts I_f. The presence of I_f during either half-cycle will cause V_S to go high, which in turn changes I_1 from $3I_{TH}$ to I_{TH}. Although I_{TH} discharges the timing capacitor during both half-cycles of the line, I_f only charges the capacitor during the half-cycle in which I_f exits pin 2. Thus during one half-cycle $I_f - I_{TH}$ charges the timing capacitor, while during the other half-cycle I_{TH} discharges it. When the capacitor voltage reaches 17.5V, the latch engages and turns off Q3 permitting I_2 to drive the gate of an SCR.

Application Circuits

A typical ground fault interrupter circuit is shown in *Figure 2*. It is designed to operate on 120 V_{AC} line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the DC power required by the IC. A 1 μF capacitor at pin 8 used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load. At this time no fault current flows and the IC discharge current increases from I_{TH} to $3I_{TH}$ (see Circuit Description and Block Diagram). This quickly resets both the timing capacitor and the output latch. At this time the circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the hot and neutral lines, is stepped down by 1000 and fed into the input pins of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH}=\frac{7V}{R_{SET}}\div 2 \qquad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH}=\frac{I_{f(rms)}}{2}\times 0.91 \qquad (2)$$

where $I_{f(rms)}$ is the rms input fault current to the operational amp and the factor of 2 is due to the fact that I_f charges the timing capacitor only during one half-cycle, while I_{TH} discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have

$$R_{SET}=\frac{7V}{I_{f(rms)}\times 0.91} \qquad (3)$$

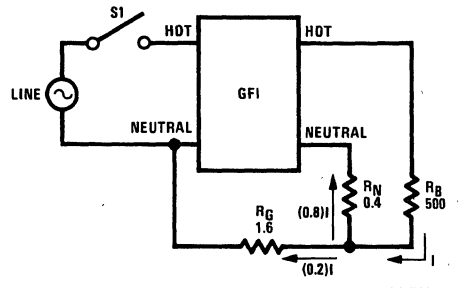
For example, to obtain 5 mA(rms) sensitivity for the circuit in *Figure 2* we have:

$$R_{SET}=\frac{7V}{\frac{5\ mA\times 0.91}{1000}}=1.5M\ \Omega \qquad (4)$$

The correct value for R_{SET} can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of R_{SET} depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA–6 mA, provision should be made to adjust R_{SET} on a per-product basis.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_t. Due to the large number of variables involved, proper selection of C_t is best done empirically. The following design example, then should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GF1 start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagramatically below.



TL/H/5177–5

UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C_t based upon charging currents due to normal fault only is as follows:

≤25 ms Specification

−3 ms GFI turn-on time (15k and 1 μF)

−8 ms Potential loss of one half-cycle due to fault current sense of half-cycles only

−4 ms Time required to open a sluggish circuit breaker

≤10 ms Maximum integration time that could be allowed

8 ms Value of integration time that accommodates component tolerances and other variables

$$C_t=\frac{I\times T}{V} \qquad (5)$$

where T = integration time

V = threshold voltage

I = average fault current into C_t

$$I=\underbrace{\left(\frac{120\ V_{AC(rms)}}{R_B}\right)}_{\text{heavy fault current generated (swamps } I_{TH})}\times\underbrace{\left(\frac{R_N}{R_G+R_N}\right)}_{\text{portion of fault current shunted around GFI}}$$

$$\times\underbrace{\left(\frac{1\ turn}{1000\ turns}\right)}_{\text{current division of input sense transformer}}\times\underbrace{\left(\frac{1}{2}\right)}_{C_t\text{ charging on half-cycles only}}\times\underbrace{(0.91)}_{\text{rms to average conversion}} \qquad (6)$$

therefore:

$$C_t=\frac{\left[\left(\frac{120}{500}\right)\times\left(\frac{0.4}{1.6+0.4}\right)\times\left(\frac{1}{1000}\right)\times\left(\frac{1}{2}\right)\times(0.91)\right]\times 0.0008}{17.5} \qquad (7)$$

$C_t=$ 0.01 μF

Application Circuits (Continued)

in practice, the actual value of C1 will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C1.

For UL943 requirements, 0.015 μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacitor can be used and better noise immunity obtained. The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

In *Figure 2*, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Typical Application

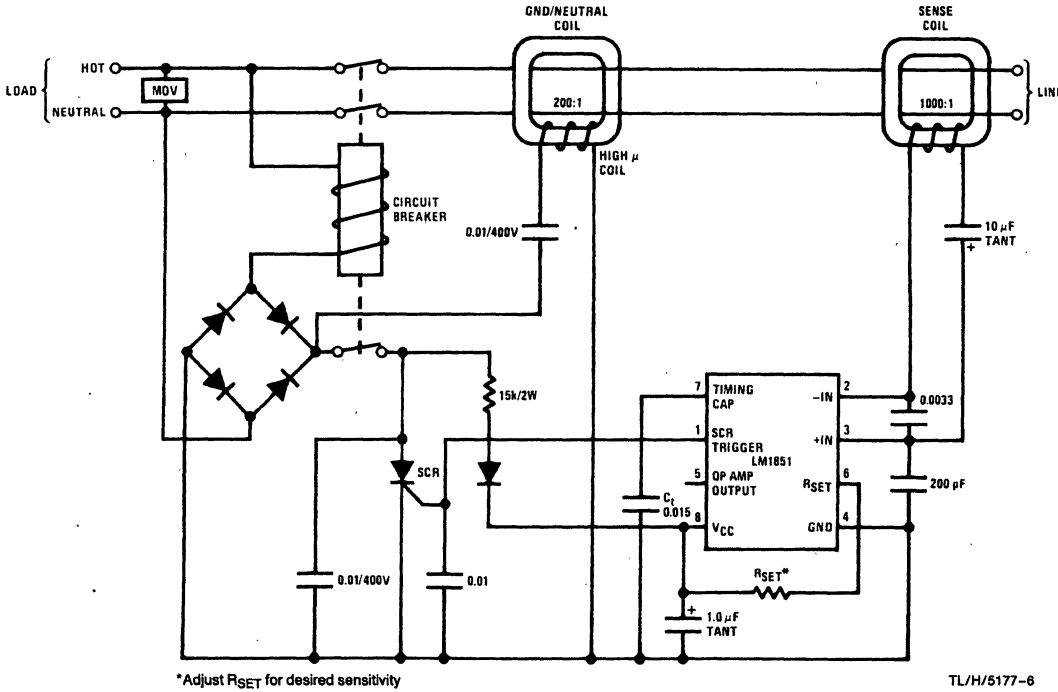
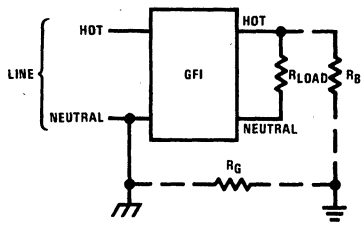


FIGURE 2. 120 Hz Neutral Transformer Approach

Definition of Terms

Normal Fault: An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines.



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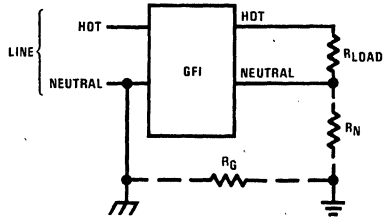
Grounded Neutral Fault: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.



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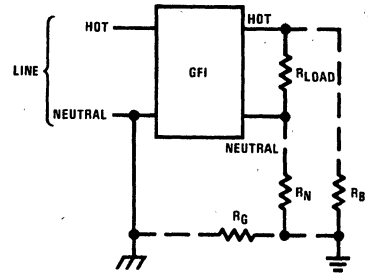
Normal Fault plus Grounded Neutral Fault: The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines.



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Section 11

Motor Controllers

Section Contents

National Semiconductor

LM1014 Motor Speed Regulator

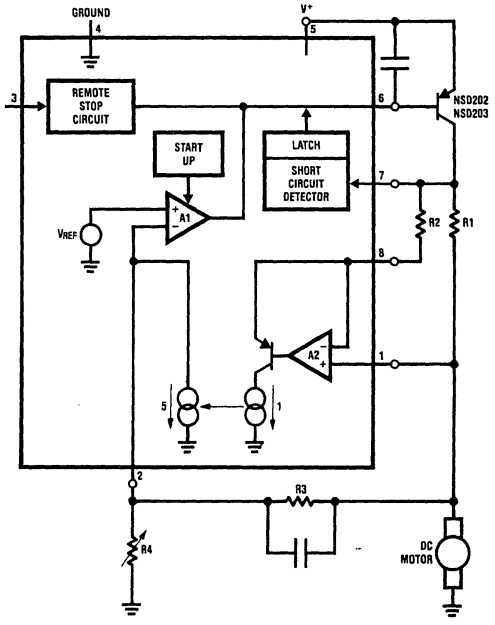
General Description

The LM1014 is a monolithic integrated circuit specifically designed to provide a low cost motor speed regulator for low voltage DC motors.

Features

- 5V to 20V operating voltage range
- Short circuit protection
- Remote pause control
- Saturation voltage 0.1V
- Motor connected to ground for ease of RF suppression
- Motor torque compensation
- Low current consumption

Functional Block Diagram and Typical Connection



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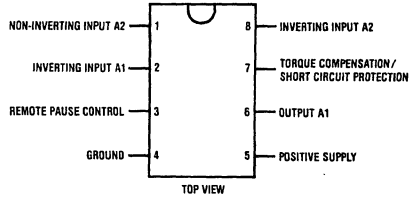
Connection Diagram

Dual-In-Line Package



TL/H/6159–2

Order Number LM1014N-2
See NS Package N08E

Absolute Maximum Ratings

Supply Voltage	24V	Storage Temperature Range	−65 to +150°C
Operating Temperature Range	−20 to +70°C	Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 1)

Parameter	Conditions	Min	Typ	Max	Units	Comments
Supply Voltage Range		5.0		20.0	V	
Supply Current	Current into Pin 5		6.0	8.0	mA	
Reference Voltage			1.33		V	0.3 mV/°C
Line Regulation of Reference Voltage	$V_S = 5V$ to $V_S = 20V$ Pin 2			2.0	% V_{REF}	
Remote Stop Current	Current into Pin 3 when Grounded		125	200	μA	(Note 2)
Output Current A1	$V_S = 5V$ Pin 2 Gnd	15	40		mA	Current into Pin 7
Short Circuit Current Limit	$R1 = 1\Omega$		1.4		A	(Note 3)
Motor Sense	$R1 = 1\Omega$, $R2 = 200\Omega$					
Current Deviation	Current into Pin 2: I2		±3.0		%	(I2/Im−1) Exclusive of External Components Tolerances

Note 1: Unless otherwise specified, $5V \leq V_S \leq 20V$ and $-15°C \leq T_A \leq 55°C$.

Note 2: The remote stop is activated by grounding pin 3. The motor restarts after disconnection of the ground connection.

Note 3: The current limit is set by resistor R1, i.e., $1 \cong 1.4V/R1$. When the output current exceeds this limit, the drive to the output transistor is switched off by a latch circuit. The motor can only be restarted after interruption of the supply voltage.

Typical Performance Characteristics/Application

1. The output voltage V_M is given by:

$$V_M = V_{REF}\left(1 + \frac{R3}{R4}\right) + I_M \frac{R1\ R3}{5R2}$$

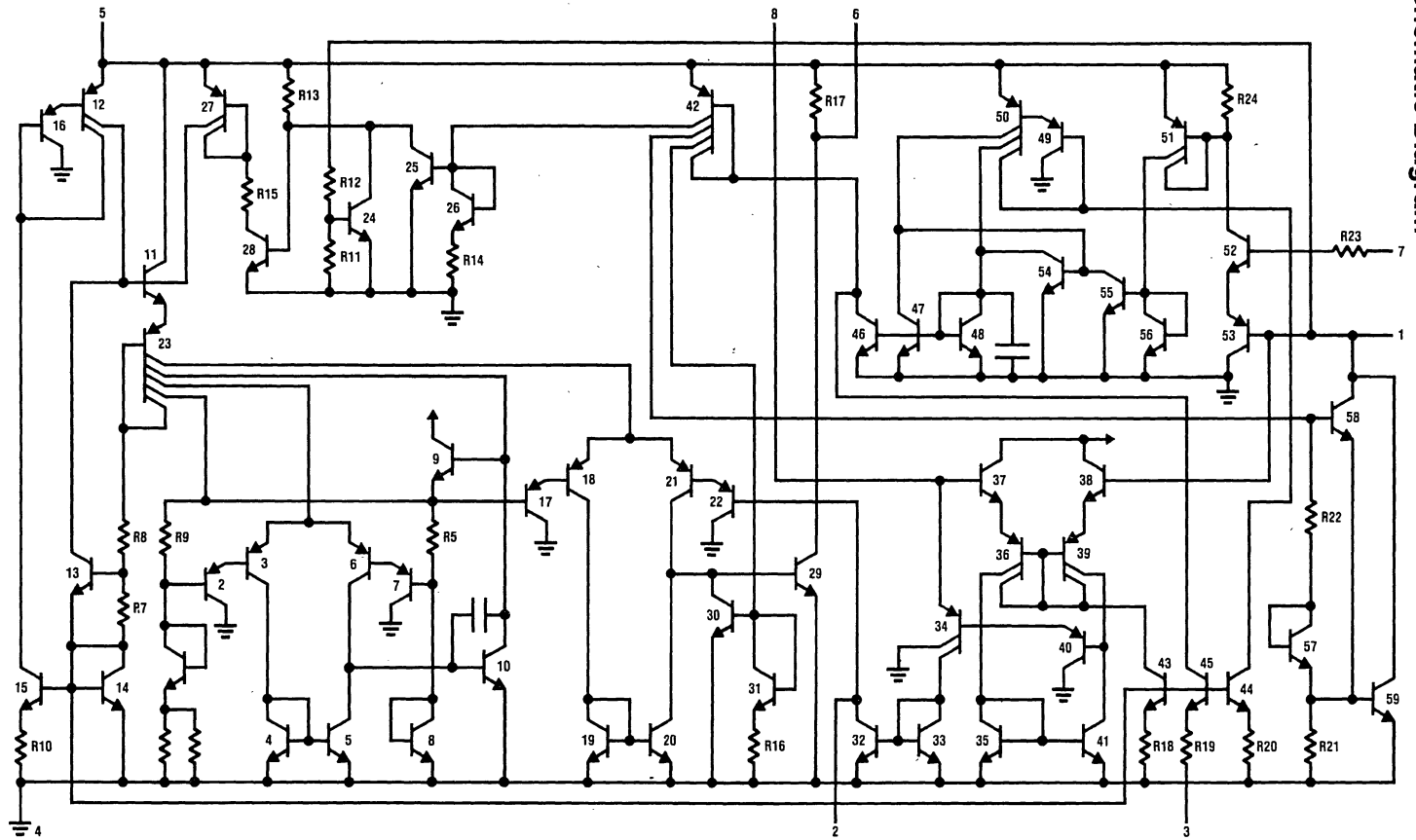
2. R1 R3.R52 must be equal to dynamic motor winding resistance R_M in order to keep the speed constant during load torque variations.

3. Parameter of the motor used for the test results shown below:

$R_M = 16.3\Omega$ and back e.m.f. = 3.25V @2000 r.p.m.; torque constant 5.9 mA/mNm; External components: $R1 = 1\Omega$ Cu, $R2 = 200\Omega$ and $R3 = 16\ k\Omega$; $V_{REF} = 1.33V$

$C_{BE} = 2.2\ \mu F$ and $C3 = 0.47\ \mu F$.

Parameter	Conditions	Max
Motor Speed Deviation (Voltage)	$V_S = 5V$ to $10V$	±0.5%
	$V_S = 5V$ to $20V$	±1.0%
Motor Speed Deviation (Load)	$I_M = 25$ mA to 125 mA	±1.0%
Motor Speed Deviation (Temperature)	$T = +5°C$ to $+35°C$	1.0%
	$T = -15°C$ to $+55°C$	3.0%


5
8
6
12
16
27
R13
42
R17
50
49
R24
51
R15
R12
25
26
24
R11
R14
28
11
R23
52
7
54
55
47
46
48
56
53
1
23
58
9
18
21
37
38
17
22
R22
R8
R9
R5
36
39
13
2
3
6
7
29
R7
30
34
40
57
10
43
45
15
14
31
44
59
R10
4
5
8
19
20
R16
32
33
35
41
R18
R19
R20
R21
4
2
3

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Application Hints

This circuit has been primarily designed for cassette tape recorders, but is suitable for all low voltage DC motors, and performs the functions of motor speed control, remote stop (pause) and output short circuit protection. The circuit achieves good speed regulation under conditions of supply voltage, torque and temperature variations. Five components, a PNP pass transistor and four resistors, are required to match the circuit to the motor. As these are external to the IC a very wide range of motor characteristics can be accommodated.

Motor speed control is by means of a negative output impedance voltage regulator. The negative output impedance is a function of the external resistors.

If the output current exceeds a preset limit, the base drive to the external PNP transistor is switched off and can only be restarted after reconnection of the supply voltage. The remote stop is activated by closing a DC switch.

System Description

The voltage across the terminals of a DC motor is given by:

$$V_M = E_O + R_M I_M$$

E_O = back e.m.f. - proportional to speed

I_M = motor current - proportional to load torque

R_M = motor winding resistance

The regulator must therefore be a source whose voltage can be controlled to maintain the desired back e.m.f., with a negative output resistance whose value equals the motor winding resistance in order to maintain the desired speed during torque variations. (See *Figure 1*)

A block diagram of the system is shown in *Figure 2* with the external components connected. The circuit comprises of a stable voltage reference source, V_{ref}, two high gain differential amplifiers, A_1 and A_2, short circuit detector + latch and remote stop circuit.

Amplifier A_2 is a high gain differential - input amplifier. (DC collector current: 125 μA). Feedback through T_1 maintains the potentials at the input terminals 9 and 10 equal, therefore the collector current of T_1 will be in the ratio of R_1/R_2 of the motor current I_M. This current is mirrored (5 : 1) and will be supplied via R_3. Amplifier A_2 has been designed to work with its inputs at or near the supply voltage.

Amplifier A_1 is also a high gain differential amplifier, but with Darlington inputs. (DC collector current :280 μA). Feedback through T_2, R_1, R_3 and R_4 maintains the potential at pin 1 equal to V_{ref}. The total current through resistor R_3 will be:

$$\frac{V_{ref}}{R_4} + \frac{I_M R_1}{5R_2}$$

The output voltage V_M is thus given by:

$$V_M = V_{ref}\left(1 + \frac{R_3}{R_4}\right) + I_M \frac{R_1 R_3}{5R_2}$$

Therefore by varying R_3/R_4 a no load voltage V_O can be supplied which equals the back e.m.f. E_O of the motor at the desired speed. The value of the negative resistance R_O is given by:

$$R_1\left(\frac{R_3}{5R_2}\right).$$

The increase in output voltage V_M due to an increase in motor current is given by $\Delta I_M R_O$. The increase in the voltage drop across the motor winding resistor R_M is $\Delta I_M R_M$. In order to keep the speed constant during load torque variations the resistance R_O must be equal to R_M.

The reference voltage source is based on the bandgap regulator principle[1] and comprises transistors T_1 to T_{10}. The reference voltage is given by:

$$V_{ref} = V_{be1} + V_T\left(1 + \frac{R_9}{R_6}\right) \ln \frac{R_9}{R_5} \text{ with } \frac{R_9}{R_5} = 10 \text{ with } V_T = \frac{kT}{q}.$$

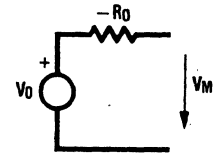
The bandgap regulator is driven from an internally generated 3.8 V regulator. This regulator comprises of T_{11}/T_{16}, T_{23} and resistors R_7 and R_8.

Resistors R_{13} and R_{15}, transistors T_{27} and T_{28} serve the sole purpose of starting this regulator. It only needs to supply enough base current to T_{11} to develop 600 mV across R_7 to ensure start-up. This start-up network is disabled by transistor T_{24} as soon as the output voltage exceeds 3V. Resistors R_{11} and R_{12} are used to sense the output voltage for this purpose.

Current limiting is provided by transistors T_{51}, T_{52} and T_{53}. When the voltage across the external resistor R_1, connected between pin 8 and 10, becomes high enough to turn on T_{52} and T_{53} (approximately 1.4V), current source T_{51} turns on transistor T_{55} and the latch circuit changes state, i.e., T_{47} turns on. Hence transistor T_{30} is turned on by current source T_{42} and sinks all the base current supplied to T_{29}, thereby switching off the external transistor. Transistor T_{25} holds off the start-up circuit. The latch can only be reset by interruption of the supply voltage. The latch circuit is supplied with equal currents from two collectors of T_{50}. The purpose of the capacitor connected to the base of T_{47} is to ensure that the latch always starts in the "T_{47} off and T_{54} on" state.

The remote stop is activated by connecting pin 4 to ground. Transistor T_{45} (collector current 180 μA) activates current source T_{42}. Transistor T_{30} is driven into saturation by T_{42}, switching off the base drive to the external transistor. At the same time, the Darlington connected transistors T_{58} and T_{59} discharge the capacitors of the motorfilter and transistor T_{25} holds off the start-up circuit. After disconnecting pin 4, current source T_{42} turns off and transistor T_{29} will supply the maximum base drive to restart the motor.

(1) R. J. Widlar. "New Developments in IC Voltage Regulators" IEEE Journal of Solid-State Circuits, February 1971.



TL/H/6159–4

FIGURE 1.

System Description

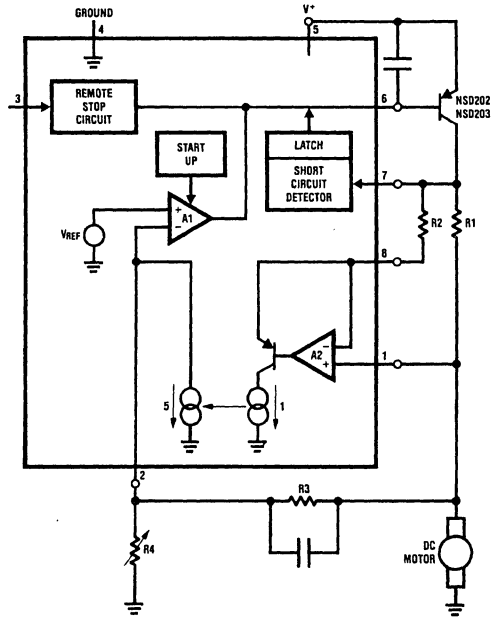


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FIGURE 2. Block Diagram

1. To ensure stable operation of the system the feedback loop requires compensation capacitors between the base-emitter of the power pass transistor and across R_3 (to smooth current spikes caused by commutator brushes).

   Recommended values: C_{be} = 2.2 – 10 mF

   C_3 = 0.47 – 1 μF

2. To minimize the voltage drop between the supply line and the motor, resistor R_1 should be kept to a very low value.

   Recommended values: R_1 = 1–5Ω

   R_2 = 200Ω

3. The output current limit is set by R_1:

   $I_{limit} \cong 1.4v/r_1$

4. An improved performance of the system for supply voltage variations can be achieved by connecting a resistor between pin 1 and the supply voltage line. (V_{ref} 3 and Vref 4 only).

   Recommended values: R (V_{ref} 3) = 6.8 MΩ

   R(V_{ref} 4) = 4 MΩ

5. The overall temperature performance of the regulator system is primarily determined by the matching of the temperature coefficient of the motor voltage and the output voltage V_M. Ideally d R_O/dT is made equal to d R_M/dT and d V_O/dT to dE_O/dT. The temperature coefficient of V_O is a multiple of the temperature coefficient of the reference voltage V_{ref}. Four reference voltages are available, two with a negative – and two with a positive temperature coefficient.

Since dR_M/dT is positive, a copper sensing resistor R_1 (assuming R_2 and R_3 are both of the same type) will then give optimum speed regulation over the full temperature range.

Alternatively, a sensing resistor R_1 with a more negative coefficient than that of R_M can be employed e.g. carbon but then a reference voltage with a positive temperature coefficient must be used. However, care must be taken that the resistance R_1 $R_3/5R_2$ never becomes more than R_M, otherwise the system will overcompensate for torque changes and can become unstable. Therefore, when employing a sensing resistor with a negative temperature coefficient, R_O must be made smaller than R_M (factor 0.9). This will degrade the torque regulation accordingly.

Section 12

Consumer Circuits

Section Contents

National Semiconductor

DNR™ DYNAMIC NOISE REDUCTION SYSTEM

LM832 Dynamic Noise Reduction System DNR™

General Description

The LM832 is a stereo noise reduction circuit for use with audio playback systems. The DNR system is noncomplementary, meaning it does not require encoded source material. The system is compatible with virtually all prerecorded tapes and FM broadcasts. Psychoacoustic masking, and an adaptive bandwidth scheme allow the DNR to achieve 10 dB of noise reduction. DNR can save circuit board space and cost because of the few additional components required.

The LM832 is optimized for low voltage operation with input levels around 30 mVrms.

For higher input levels use the LM1894.

A trademark and licensing agreement is required for the use of this product.

Features

- Low voltage battery operation
- Non-complementary noise reduction, "single ended"
- Low cost external components, no critical matching
- Compatible with all prerecorded tapes and FM
- 10 dB effective tape noise reduction CCIR/ARM weighted
- Wide supply range, 1.5V to 9V
- 150 mVrms input overload
- No royalty requirements
- Cascade connection for 17 dB noise reduction

Applications

- Headphone stereo
- Microcassette players
- Radio cassette players
- Automotive radio/tape players

Application Circuit

Order Number LM832M See NS Package M14A
Order Number LM832N See NS Package N14A

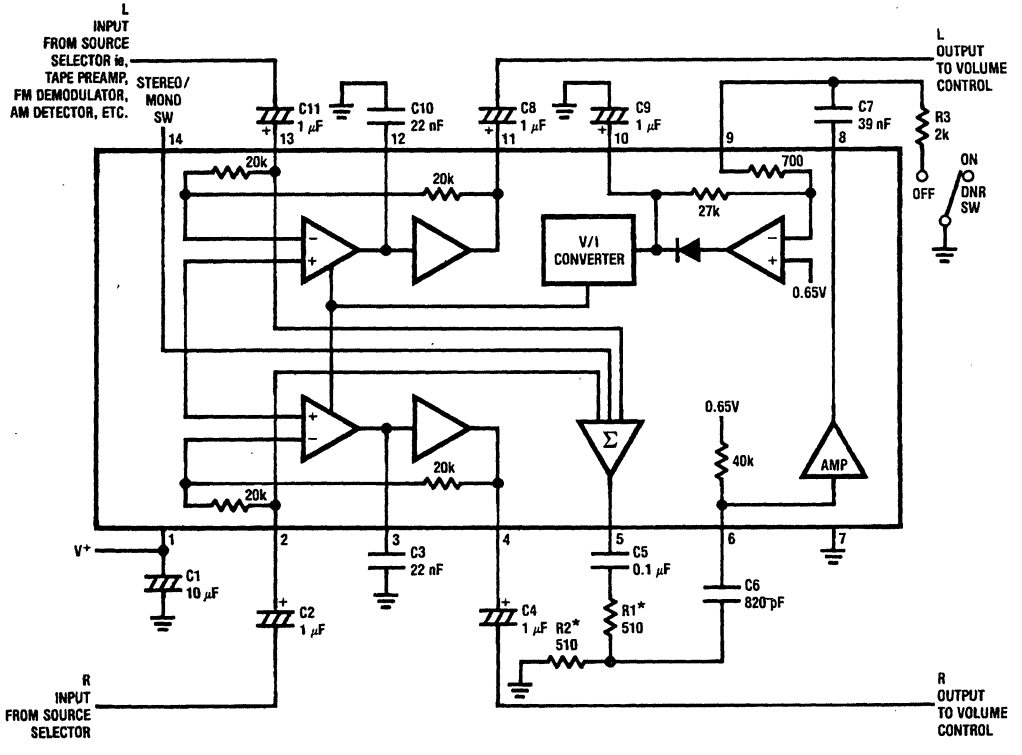

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FIGURE 1. Component Hook-up for Stereo DNR System

Absolute Maximum Ratings

Supply Voltage	10V	Storage Temperature	−65 to +150°C
Power Dissipation (Note 1)	1.2W	Operating Temperature (Note 1)	−40 to +85°
Input Voltage	1.7 Vpp	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = 25°C$ $V_{CC} = 3.0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OP}	Operating Voltage	Supply Voltage for Normal Operation	1.5	3.0	9.0	V
$I_{CC}(1)$	Supply Current (1)	Pin 9 to GND 0.1 μF, BW = Min, Note 2		2.5	4.0	mA
$I_{CC}(2)$	Supply Current (2)	DC GND Pin 9 with 2k, BW = Max, Note 2		5.0	8.0	mA
$V_{IN}(1)$	Input Voltage (1)	Pin 2, Pin 13	0.20	0.36	0.5	V
$V_{IN}(2)$	Input Voltage (2)	Pin 6	0.50	0.65	0.8	V
$V_{IN}(3)$	Input Voltage (3)	Pin 9	0.50	0.65	0.8	V
$V_{OUT}(1)$	Output Voltage (1)	Pin 4, Pin 11	0.20	0.35	0.50	V
$V_{OUT}(2)$	Output Voltage (2)	Pin 5 Stereo Mode	0.15	0.28	0.40	V
$V_{OUT}(3)$	Output Voltage (3)	Pin 5 Monaural Mode, DC Ground Pin 14	0.10	0.20	0.30	V
$V_{OUT}(4)$	Output Voltage (4)	Pin 8	0.25	0.40	0.60	V
$V_{OUT}(5)$	Output Voltage (5)	Pin 10 BW = Max, Note 2	1.00	1.27	1.50	V
$V_{OUT}(6)$	Output Voltage (6)	Pin 10 BW = Min, Note 2	0.50	0.65	0.75	V
V_{OS}	Output DC Shift	Pin 4, PIN 11; Change BW Min to Max		1.0	3.0	mV

AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MAIN SIGNAL PATH (Note 3)						
A_V	Voltage Gain	V_{IN} = 30 mVrms, f = 1 kHz, BW = Max, Note 2	−1.0	0.0	+1.0	dB
C.B.	Channel Balance	V_{IN} = 30 mVrms, f = 1 kHz, BW = Max, Note 2	−1.0	0	+1.0	dB
f_{MIN}	Min Bandwidth	0.1 μF between Pin 9 - GND	600	1000	1500	Hz
f_{MAX}	Max Bandwidth	DC Ground Pin 9 with 2k	24	30	46	kHz
THD	Distortion	V_{IN} = 30 mVrms, f = 1 kHz, BW = Max, Note 2		0.07	0.5	%
MV_{IN}	Max Input Voltage	THD = 3%, f = 1 kHz, BW = Max Note 2	120	150		mVrms
S/N	Signal to Noise	REF = 30 mVrms, BW = Max, CCIR/ARM	60	68		dB
Z_{IN}	Input Impedance	Pin 2, Pin 13	14	20	26	kΩ
C.S.	Channel Separation	Ref = 30 mVrms, f = 1 kHz, BW = Max, Note 2	40	68		dB
P_{SRR}	P_{SRR}	V_{RIPPLE} = 50 mVrms, f = 100 Hz	40	55		dB
CONTROL PATH						
$A_V$sum(1)	Summing Amp Gain (1)	V_{IN} = 30 mVrms at R and L, f = 1 kHz	−3.0	−1.5	0.0	dB
$A_V$sum(2)	Summing Amp Gain (2)	DC Ground Pin 14, f = 1 kHz	−9.0	−6.0	−3.0	dB
A_V 1st	Gain Amp Gain	Pin 6 to Pin 8	25	30	35	dB
Z_{IN} 1st	Input Impedance	Pin 6	28	40	52	kΩ
A_{VPKD}	Peak Detector Gain	AC In, DC Out; Pin 9 to Pin 10	25	30	35	V/V
Z_{INPKD}	Input Impedance	Pin 9	500	800	1100	Ω
V_{RPKD}	Output DC Change	Pin 10, Change BW Min to Max	0.5	0.62	0.8	V

Note 1: For operation in ambient temperature above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance junction to ambient, as follows: LM832N −90° c/w, LM833M −150° c/w.

Note 2: To force the DNR system into maximum bandwidth, connect a 2k resistor from pin 9 to GND. AC ground pin 9 or pin 6 to select minimum bandwidth. To change minimum and maximum bandwidth, see Application Hints.

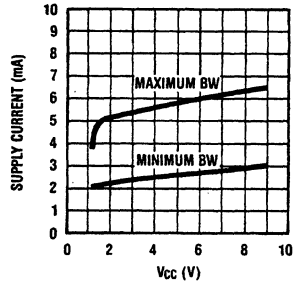
Note 3: The maximum noise reduction CCIR/ARM weighted is about 14 dB. This is accomplished by changing the bandwidth from maximum to minimum. In actual operation, minimum bandwidth is not selected, a nominal minimum bandwidth of about 2 kHz gives 10 dB of noise reduction. See Application Hints.

External Component Guide (See *Figure 1*)

P/N	Recommended Value	Purpose	Effect		Remarks
			Smaller	Larger	
C1	10 μF	Power supply decoupling	Poor supply rejection	Better supply rejection	Do not use less than 10 μF
C2,C11	1 μF	Input coupling capacitor	Increases frequency of low-frequency roll-off	Reduces frequency of low-frequency roll-off	DC voltage at pin 2 and pin 13 is 0.35V $f=\frac{1}{2\pi C_2 R_{IN}}$
C3,C10	22 nF for Stereo, 15 nF for mono	Establishment of Min and Max Bandwidth	Bandwidth becomes wider	Bandwidth becomes narrower	See Note 4
C4,C8	1 μF	Output coupling capacitor	Increases frequency of low-frequency roll-off	Reduces frequency of low-frequency roll-off	DC voltage at pin 4 and pin 11 is 0.35V $f=\frac{1}{2\pi C_4 R_{LOAD}}$
C5	0.1 μF	Works with R1 and R2 to set one of the low-frequency corners in control path	Some high frequency program material may be attenuated	Bandwidth may increase due to low-frequency inputs, causing "Breathing"	$f=\frac{1}{2\pi C_5(R1+R2)}=1.6$ kHz See Note 4
C6	820 pF	Works with input resistance of pin 6 to set one of the low-frequency corners in the control path	Same as above	Same as above	$f=\frac{1}{2\pi C_6 R_{PIN6}}=4.8$ kHz See Note 4
C7	39 nF	Works with input resistance of pin 9 to form part of control path frequency weighing	Same as above	Same as above	$f=\frac{1}{2\pi C_7 R_{PIN7}}=4.8$ kHz See Note 4
C9	1 μF	Sets attack time	Reduces attack and decay time	Increases attack and decay time	See Note 4
R1,R2	$R_1+R_2=1$ kΩ	This voltage divider sets control path sensitivity	—	—	Sensitivity should be set for maximum noise reduction and minimum audible frequency program effect on high
R3	•2 kΩ	Sets gain amp load when DNR is OFF	Loads gain amp output, may cause distortion	Max bandwidth will be reduced	

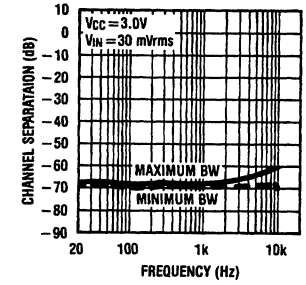
Note 4: The values of the control path filter components (C5, C6, C7, C9, R1, R2) and the integrating capacitors (C3, C10) should not be changed from the recommended values unless the characteristics of the noise or program material differ substantially from that of FM or tape sources. Failure to use the correct values may result in degraded performance, and therefore the application may not be approved for DNR trademark usage. Please contact National Semiconductor for more information and technical assistance.

Typical Performance Characteristics



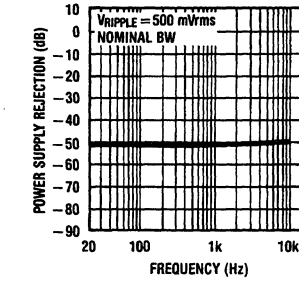
TL/H/5176–2

FIGURE 2. Supply current vs supply voltage



TL/H/5176–3

FIGURE 3. Channel separation vs frequency



TL/H/5176–4

FIGURE 4. Power supply rejection ratio vs frequency

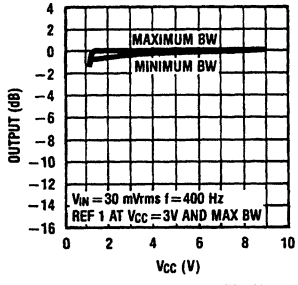


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FIGURE 5. Output level change vs supply voltage

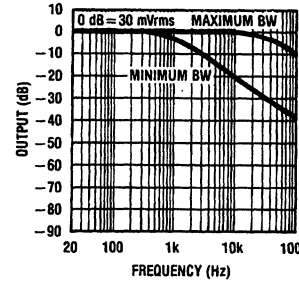

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FIGURE 6. Output level vs frequency

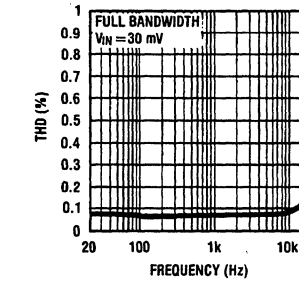

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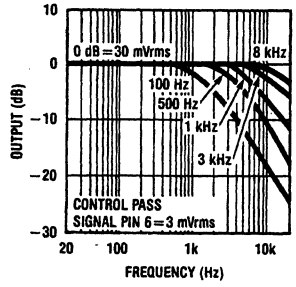
FIGURE 7. THD vs frequency



TL/H/5176–8

FIGURE 8. Output vs frequency and control path signal

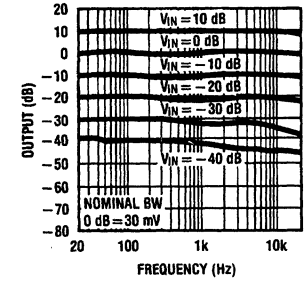


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FIGURE 9. Frequency response for various input levels

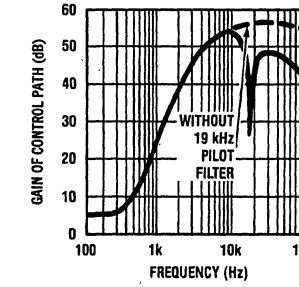

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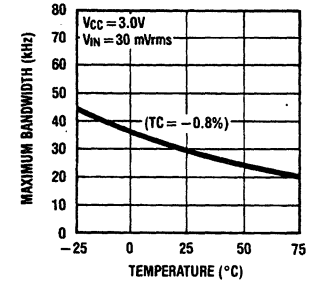
FIGURE 10. Gain of control path vs frequency



TL/H/5176–11

FIGURE 11. Change in main signal path maximum bandwidth vs temperature

Circuit Operation

The LM832 has two signal paths, a main signal path and a bandwidth control path. The main path is an audio low pass filter comprised of a g_m block with a variable current, and a unity gain buffer. As seen in *Figure 1*, DC feedback constrains the low frequency gain to $A_V = -1$. Above the cutoff frequency of the filter, the output decreases at −6 dB/oct due to the action of the 0.022 μF capacitor.

The purpose of the control path is to generate a bandwidth control signal which replicates the ear's sensitivity to noise in the presence of a tone. A single control path is used for both channels to keep the stereo image from wandering. This is done by adding the right and left channels together in the summing amplifier of *Figure 1*. The R1, R2 resistor divider adjusts the incoming noise level to slightly open the bandwidth of the low pass filter. Control path gain is about 60dB and is set by the gain amplifier and peak detector gain. This large gain is needed to ensure the low pass filter bandwidth can be opened by very low noise floors. The capacitors between the summing amplifier output and the peak detector input determine the frequency weighting as shown in the typical performance curves. The 1 μF capacitor at pin 10, in conjunction with internal resistors, sets the attack and decay times. The voltage is converted into a proportional current which is fed into the g_m blocks. The bandwidth sensitivity to g_m current is 70 Hz/μA. In FM stereo applications a 19 kHz pilot filter is inserted between pin 8 and pin 9 as shown in *Figure 16*.

Normal methods of evaluating the frequency response of the LM 832 can be misleading if the input signal is also applied to the control path. Since the control path includes a frequency weighting network, a constant amplitude but varying frequency input signal will change the audio signal path bandwidth in a non-linear fashion. Measurements of the audio signal path frequency response will therefore be in error since the bandwidth will be changing during the measurement. See *Figure 9* for an example of the misleading results that can be obtained from this measurement approach. Although the frequency response is always flat below a single high-frequency pole, the lower curves do not resemble single pole responses at all.

A more accurate evaluation of the frequency response can be seen in *Figure 8*. In this case the main signal path is frequency swept while, the control path has a constant frequency applied. It can be seen that different control path frequencies each give a distinctive gain roll-off.

PSYCHOACOUSTIC BASICS

The dynamic noise reduction system is a low pass filter that has a variable bandwidth of 1 kHz to 30 kHz, dependent on music spectrum. The DNR system operates on three principles of psychoacoustics.

1. Music and speech can mask noise. In the absence of source material, background noise can be very audible. However, when music or speech is present, the human ear is less able to distinguish the noise—the source material is said to mask the noise. The degree of masking is dependent on the amplitude and spectral content (frequencies) of the source material, but in general multiple tones around 1 kHz are capable of providing excellent masking of noise over a very wide frequency range.

2. The ear cannot detect distortion for less than 1 ms. On a transient basis, if distortion occurs in less than 1 ms, the ear acts as an integrator and is unable to detect it. Because of this, signals of sufficient energy to mask noise open the bandwidth to 90% of the maximum value in less than 1 ms. Reducing the bandwidth to within 10% of its minimum value is done in about 60 ms: long enough to allow the ambience of the music to pass through, but not so long as to allow the noise floor to become audible.

3. Reducing the audio bandwidth reduces the audibility of noise. Audibility of noise is dependent on noise spectrum, or how the noise energy is distributed with frequency. Depending on the tape and the recorder equalization, tape noise spectrum may be slightly rolled off with frequency on a per octave basis. The ear sensitivity on the other hand greatly increases between 2 kHz and 10 kHz. Noise in this region is extremely audible. The DNR system low pass filters this noise. Low frequency music will not appreciably open the DNR bandwidth, thus 2 kHz to 20 kHz noise is not heard.

Application Hints

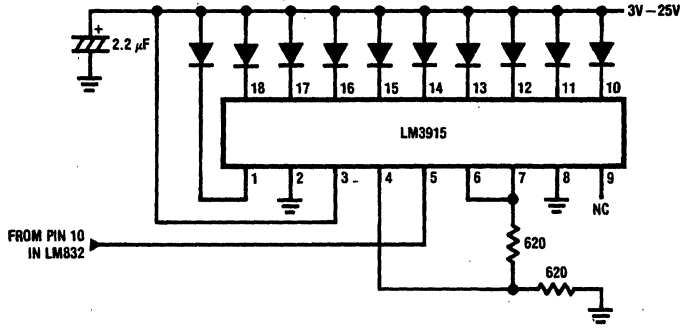
The DNR system should always be placed before tone and volume controls as shown in *Figure 1*. This is because any adjustment of these controls would alter the noise floor seen by the DNR control path. The sensitivity resistors R1 and R2 may need to be switched with the input selector, depending on the noise floors of different sources, i.e., tape, FM, phono. To determine the value of R1 and R2 in a tape system for instance; apply tape noise (no program material) and adjust the ratio of R1 and R2 to slightly open the bandwidth of the main signal path. This can easily be done by viewing the capacitor voltage of pin 10 with an oscilloscope, or by using the circuit of *Figure 12*. This circuit gives an LED display of the voltage on the peak detector capacitor. Adjust the values of R1 and R2 (their sum is always 1 kΩ) to light the LEDs of pin 1 and pin 18. The LED bar graph does not indicate signal level, but rather instantaneous bandwidth of the two filters; it should not be used as a signal-level indicator. For greater flexibility in setting the bandwidth sensitivity, R1 and R2 could be replaced by a 1 kΩ potentiometer.

To change the minimum and maximum value of bandwidth, the integrating capacitors, C3 and C10, can be scaled up or down. Since the bandwidth is inversely proportional to the capacitance, changing this 0.022 μF capacitor to 0.015 μF will change the typical bandwidth from 1 kHz–30 kHz to 1.5 kHz–44 kHz. With C3 and C10 set at 0.022 μF, the maximum bandwidth is typically 30 kHz. A double pole double throw switch can be used to completely bypass DNR.

The capacitor on pin 10 in conjunction with internal resistors sets the attack and decay times. The attack time can be altered by changing the size of C9. Decay times can be decreased by paralleling a resistor with C9, and increased by increasing the value of C9.

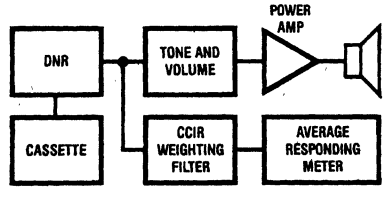
When measuring the amount of noise reduction of DNR in a cassette tape system, the frequency response of the cassette should be flat to 10 kHz. The CCIR weighting network has substantial gain to 8 kHz and any additional roll-off in the cassette player will reduce the benefits of DNR noise reduction. A typical signal-to-noise measurement circuit is shown in *Figure 13*. The DNR system should be switched from maximum bandwidth to nominal bandwidth with tape noise as a signal source. The reduction in measured noise is the signal-to-noise ratio improvement.

Application Hints (Continued)



TL/H/5176–12

FIGURE 12. Bar Graph Display of Peak Detector Voltage



TL/H/5176–13

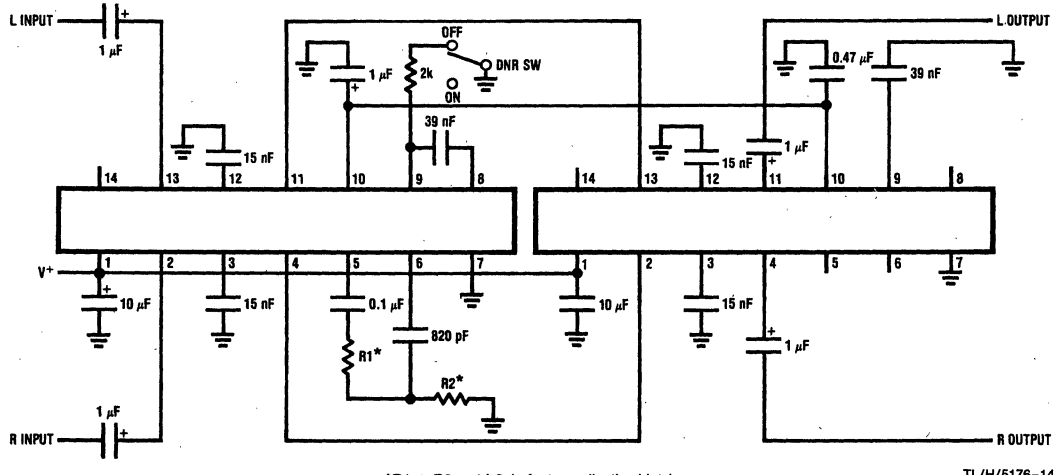
FIGURE 13. Technique for Measuring S/N Improvement of the DNR System

CASCADE CONNECTION

Additional noise reduction can be obtained by cascading the DNR filters. With two filters cascaded the rolloff is 12 dB per octave. For proper operating bandwidth the capacitors on pin 3 and 12 are changed to 15 nF. The resulting noise reduction is about 17 dB.

Figure 15 shows the monaural cascade connection. Note that pin 14 is grounded so only the pin 2 input is fed to the summing amp and therefore the control path.

Figure 14 shows the stereo cascade connection. Note that pin 14 is open circuit as in normal stereo operation.



*R1 + R2 = 1 kΩ (refer to application hints)

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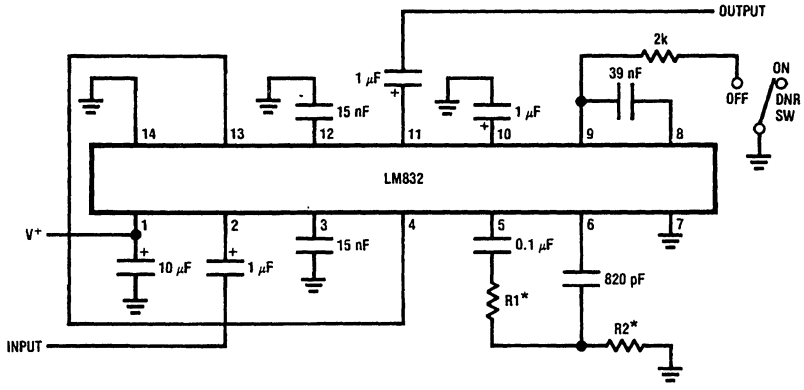
FIGURE 14. Stereo Cascade Connection

Application Hints (Continued)



*R1 + R2 = 1 kΩ (refer to application hints)

TL/H/5176–15

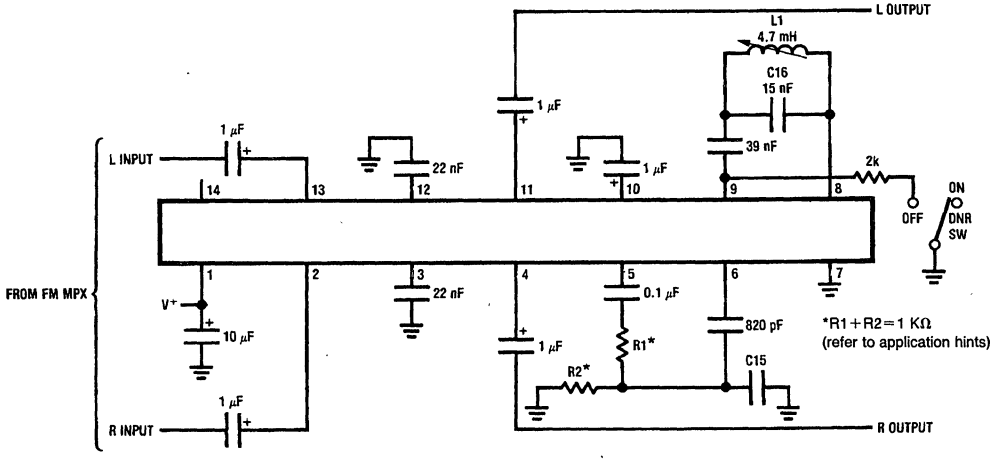
FIGURE 15. Monaural Cascade Connection

FM STEREO

When using the DNR system with FM stereo as the audio source, it is important to eliminate the ultrasonic frequencies that accompany the audio. If the radio has a multiplex filter to remove the ultrasonics there will be no problem.

This filtering can be done at the output of the demodulator, before the DNR system, or in the DNR system control path.

Standard audio multiplex filters are available for use at the output of the demodulator from several filter companies. *Figure 16* shows the additional components L1, C15 and C16 that are added to the control path for FM stereo applications. The coil must be tuned to 19 kHz, the FM pilot frequency.



TL/H/5176–16

FIGURE 16. FM Stereo Application

FOR FURTHER READING

Tape Noise Levels

1. "A Wide Range Dynamic Noise Reduction System" Blackmer, 'dB' Magazine, August-September 1972, Volume 6, #8.

2. "Dolby B-Type Noise Reduction System", Berkowitz and Gundry, Sert Journal, May-June 1974, Volume 8.

3. "Cassette vs Elcaset vs Open Reel", Toole, Audioscene Canada, April 1978.

4. "CCIR/ARM: A Practical Noise Measurement Method", Dolby, Robinson, Gundry, JAES, 1978.

Noise Masking

1. "Masking and Discrimination", Bos and De Boer, JAES, Volume 39, #4, 1966.

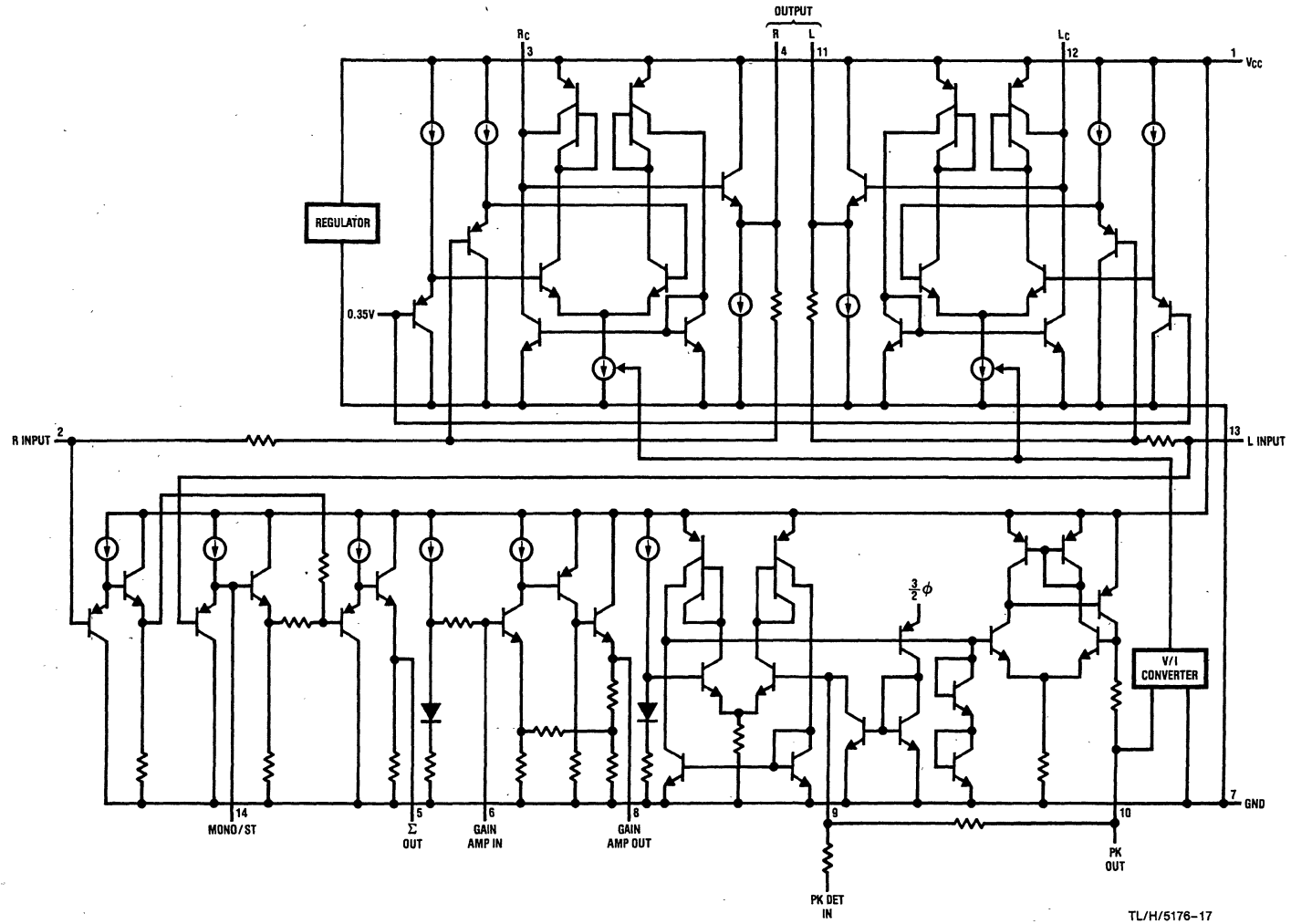
2. "The Masking of Pure Tones and Speech by White Noise", Hawkins and Stevens, JAES, Volume 22, #1, 1950.

3. "Sound System Engineering", Davis, Howard W. Sams and Co.

4. "High Quality Sound Reproduction", Moir, Chapman Hall, 1960.

5. "Speech and Hearing in Communication", Fletcher, Van Nostrand, 1953.

LM832 Simple Circuit Schematic



National Semiconductor

PRELIMINARY

LM1036 Dual DC Operated Tone/Volume/Balance Circuit

General Description

The LM1036 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

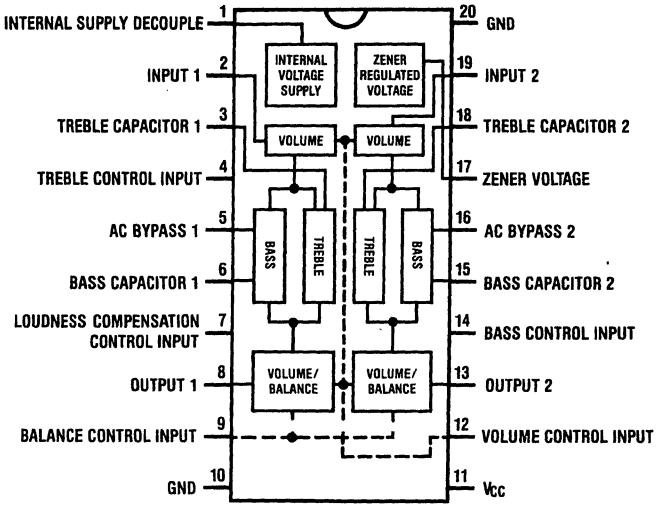
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 9V to 16V
- Large volume control range, 75 dB typical
- Tone control, ±15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 0.3 Vrms
- High signal to noise, 80 dB typical for an input level of 0.3 Vrms
- Few external components required

Block and Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5142–1

Order Number LM1036
See NS Package N20A

S 12

Absolute Maximum Ratings

Supply Voltage	16V	Storage Temperature Range	−65°C to +150°C
Control Pin Voltage (Pins 4, 7, 9, 12, 14)	V_{CC}	Power Dissipation	1W
Operating Temperature Range	0°C to +70°C	Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_{CC}=12V$, $T_A=25°C$ (unless otherwise stated)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range	Pin 11	9		16	V
Supply Current			35	45	mA
Zener Regulated Output Voltage Current	Pin 17		 5.4	 5	 V mA
Maximum Output Voltage	Pins 8, 13; f=1 kHz $V_{CC}=9V$, Maximum Gain $V_{CC}=12V$		 0.8 1.0		 Vrms Vrms
Maximum Input Voltage (Note 1)	Pins 2, 19; f=1 kHz, $V_{CC}=9V$ Flat Response, $V_{CC}=12V$ Gain=−10 dB	 1.3	1.1 1.6		Vrms Vrms
Input Resistance	Pins 2, 19; f=1 kHz	20	30		kΩ
Output Resistance	Pins 8, 13;f=1 kHz		20		Ω
Maximum Gain	V(Pin 12)=V(Pin 17); f=1 kHz	−2	0	2	dB
Volume Control Range	f=1 kHz	70	75		dB
Gain Tracking Channel 1−Channel 2	f=1 kHz 0 dB through −40 dB −40 dB through −60 dB		 1 2	 3	 dB dB
Balance Control Range	Pins 8, 13; f=1 kHz		1 −26	 −20	dB dB
Bass Control Range (Note 2)	f=40 Hz, $C_b=0.39\ \mu F$ V(Pin 14)=V(Pin 17) V(Pin 14)=0V	 12 −12	 15 −15	 18 −18	 dB dB
Treble Control Range (Note 2)	f= 16 kHz, $C_t=0.01\ \mu F$ V(Pin 4)=V(Pin 17) V(Pin 4)=0V	 12 −12	 15 −15	 18 −18	 dB dB
Total Harmonic Distortion	f=1 kHz, $V_{IN}=0.3$ Vrms Gain=0 dB Gain=−30 dB		 0.06 0.03	 0.3	 % %
Channel Separation	f=1 kHz, Maximum Gain	60	75		dB
Signal/Noise Ratio	Unweighted 100 Hz−20 kHz Maximum Gain, 0 dB=0.3 Vrms CCIR/ARM (Note 3) Gain=0 dB, $V_{IN}=0.3$ Vrms Gain=−20 dB, $V_{IN}=1.0$ Vrms	 76	80 79 72	 	dB dB dB
Output Noise Voltage at Minimum Gain	CCIR/ARM (Note 3)		10	16	μV
Supply Ripple Rejection	200 mVrms, 1 kHz Ripple	35	50		dB
Control Input Currents	Pins 4, 7, 9, 12, 14 (V=0V)		−0.6	−2.5	μA
Frequency Response	−1 dB (Flat Response 20 Hz−16 kHz)		250		kHz

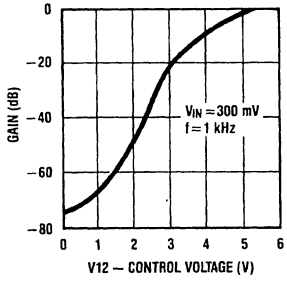
Note 1: The maximum permissible input level is dependent on tone and volume settings. See Application Notes.

Note 2: The tone control range is defined by capacitors C_b and C_t. See Application Notes.

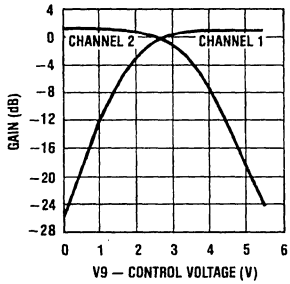
Note 3: Measured with a CCIR filter with a 0 dB level at 2 kHz and an average responding meter.

Typical Performance Characteristics

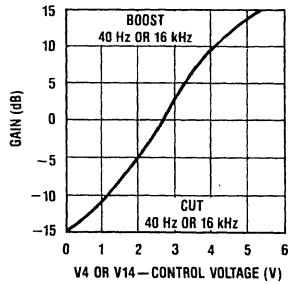
Volume Control Characteristics



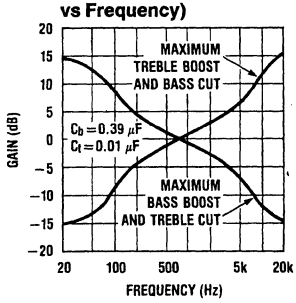
Balance Control Characteristic



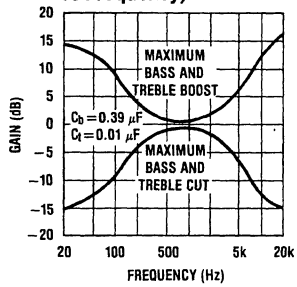
Tone Control Characteristic



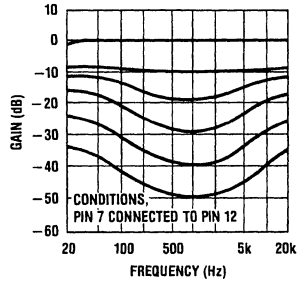
Tone Characteristic (Gain vs Frequency)



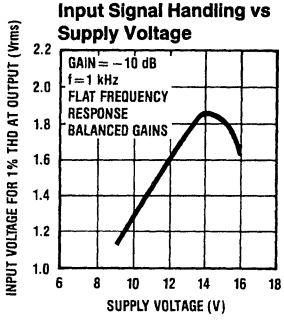
Tone Characteristic (Gain vs Frequency)



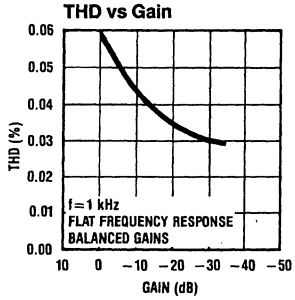
Loudness Compensated Volume Characteristic



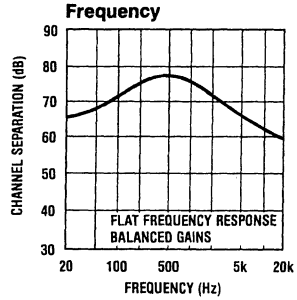
Input Signal Handling vs Supply Voltage



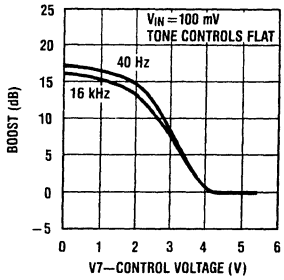
THD vs Gain



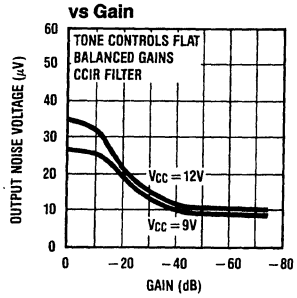
Channel Separation vs Frequency



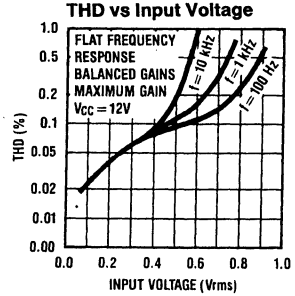
Loudness Control Characteristic



Output Noise Voltage vs Gain



THD vs Input Voltage



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Application Notes

TONE RESPONSE

The maximum boost and cut can be optimized for individual applications by selection of the appropriate values of C_t (treble) and C_b (bass).

The tone responses are defined by the relationships:

$$\text{Bass Response} = \frac{1+\frac{0.00065(1-a_b)}{j\omega C_b}}{1+\frac{0.00065a_b}{j\omega C_b}}$$

$$\text{Treble Response} = \frac{1+j\omega 5500(1-a_t)C_t}{1+j\omega 5500a_tC_t}$$

Where $a_b = a_t = 0$ for maximum bass and treble boost respectively and $a_b = a_t = 1$ for maximum cut.

For the values of C_b and C_t of 0.39 µF and 0.01 µF as shown in the Application Circuit, 15 dB of boost or cut is obtained at 40 Hz and 16 kHz.

ZENER VOLTAGE

A zener voltage (pin 17 = 5.4V) is provided which may be used to bias the control potentiometers. Setting a DC level of one half of the zener voltage on the control inputs, pins 4, 9, and 14, results in the balanced gain and flat response condition. Typical spread on the zener voltage is ±100 mV and this must be taken into account if control signals are used which are not referenced to the zener voltage. If this is the case, then they will need to be derived with similar accuracy.

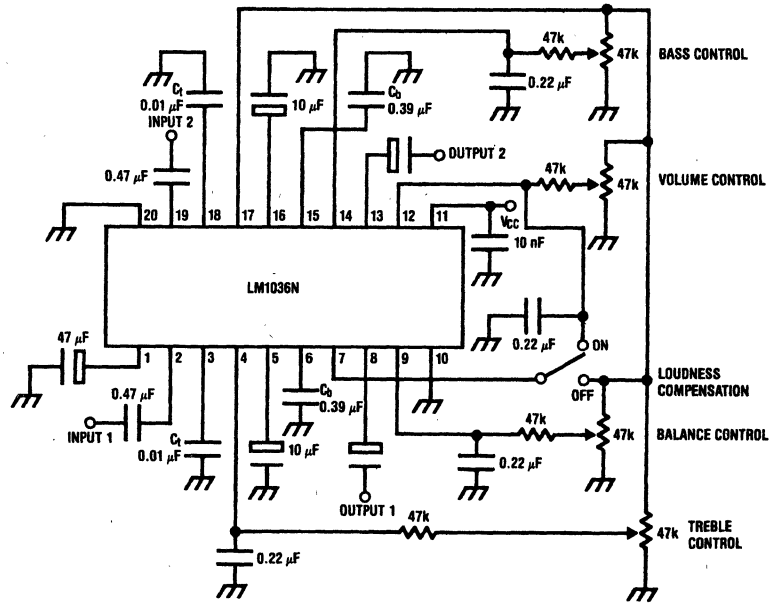
LOUDNESS COMPENSATION

A simple loudness compensation may be effected by applying a DC control voltage to pin 7. This operates on the tone control stages to produce an additional boost limited by the maximum boost defined by C_b and C_t. There is no loudness compensation when pin 7 is connected to pin 17. Pin 7 can be connected to pin 12 to give the loudness compensated volume characteristic as illustrated without the addition of further external components. (Tone settings are for flat response, C_b and C_t as given in Application Circuit.) Modification to the loudness characteristic is possible by changing the capacitors C_b and C_t for a different basic response or, by a resistor network between pins 7 and 12 for a different threshold and slope.

SIGNAL HANDLING

The volume control function of the LM1036 is carried out in two stages, controlled by the DC voltage on pin 12, to improve signal handling capability and provide a reduction of output noise level at reduced gain. The first stage is before the tone control processing and provides an initial 15 dB of gain reduction, so ensuring that the tone sections are not overdriven by large input levels when operating with a low volume setting. Any combination of tone and volume settings may be used provided the output level does not exceed 1 Vrms, V_{CC} = 12V (0.8 Vrms, V_{CC} = 9V). At reduced gain (< −6 dB) the input stage will overload if the input level exceeds 1.6 Vrms, V_{CC} = 12V (1.1 Vrms, V_{CC} = 9V). As there is volume control on the input stages, the inputs may be operated with a lower overload margin than would otherwise be acceptable, allowing a possible improvement in signal to noise ratio.

Application Circuit



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Applications Information

OBTAINING MODIFIED RESPONSE CURVES

The LM1036 is a dual DC controlled bass, treble, balance and volume integrated circuit ideal for stereo audio systems.

In the various applications where the LM1036 can be used, there may be requirements for responses different to those of the standard application circuit given in the data sheet. This application section details some of the simple variations possible on the standard responses, to assist the choice of optimum characteristics for particular applications.

TONE CONTROLS

Summarizing the relationship given in the data sheet, basically for an increase in the treble control range C_t must be increased, and for increased bass range C_b must be reduced.

Figure 1 shows the typical tone response obtained in the standard application circuit. ($C_t = 0.01\ \mu F$, $C_b = 0.39\ \mu F$). Response curves are given for various amounts of boost and cut.

Figures 2 and *3* show the effect of changing the response defining capacitors C_t and C_b to 2Ct, $C_b/2$ and $4C_t$, $C_b/4$ respectively, giving increased tone control ranges. The values of the bypass capacitors may become significant and affect the lower frequencies in the bass response curves.

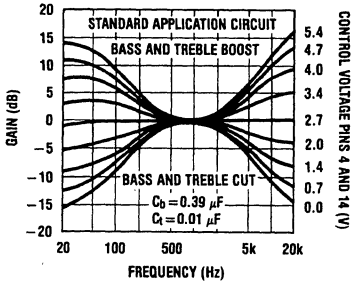

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FIGURE 1. Tone Characteristic (Gain vs Frequency)

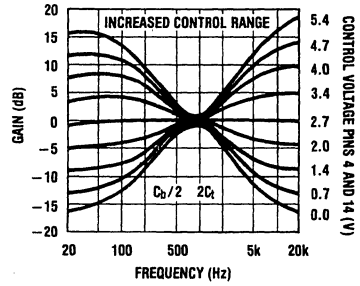

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FIGURE 2. Tone Characteristic (Gain vs Frequency)

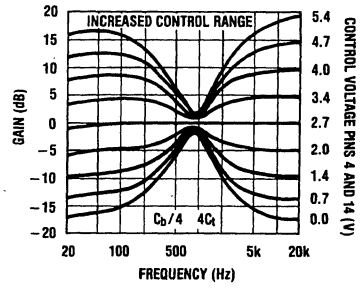

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FIGURE 3. Tone Characteristic (Gain vs Frequency)

Applications Information (Continued)

Figure 4 shows the effect of changing C_t and C_b in the opposite direction to $C_t/2$, $2C_b$ respectively giving reduced control ranges. The various results corresponding to the different C_t and C_b values may be mixed if it is required to give a particular emphasis to, for example, the bass control. The particular case with $C_b/2$, C_t is illustrated in *Figure 5*.

Restriction of Tone Control Action at High or Low Frequencies

It may be desired in some applications to level off the tone responses above or below certain frequencies for example to reduce high frequence noise.

This may be achieved for the treble response by including a resistor in series with C_t. The treble boost and cut will be 3 dB less than the standard circuit when $R = X_C$.

A similar effect may be obtained for the bass response by reducing the value of the AC bypass capacitors on pins 5 (channel 1) and 16 (channel 2). The internal resistance at these pins is 1.3 kΩ and the bass boost/cut will be approximately 3 dB less with X_C at this value. An example of such modified response curves is shown in *Figure 6*. The input coupling capacitors may also modify the low frequency response.

It will be seen from *Figures 2* and *3* that modifying C_t and C_b for greater control range also has the effect of flattening the tone control extremes and this may be utilized, with or without additional modification as outlined above, for the most suitable tone control range and response shape.

Other Advantages of DC Controls

The DC controls make the addition of other features easy to arrange. For example, the negative-going peaks of the output amplifiers may be detected below a certain level, and used to bias back the bass control from a high boost condition, to prevent overloading the speaker with low frequency components.

LOUDNESS CONTROL

The loudness control is achieved through control of the tone sections by the voltage applied to pin 7; therefore, the tone and loudness functions are not independent. There is normally 1 dB more bass than treble boost (40 Hz–16 kHz) with loudness control in the standard circuit. If a greater difference is desired, it is necessary to introduce an offset by means of C_t or C_b or by changing the nominal control voltage ranges.

Figure 7 shows the typical loudness curves obtained in the standard application circuit at various volume levels ($C_b = 0.39\ \mu F$).

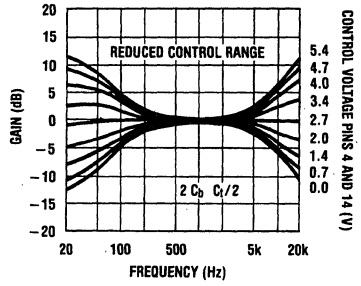

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FIGURE 4. Tone Characteristic (Gain vs Frequency)

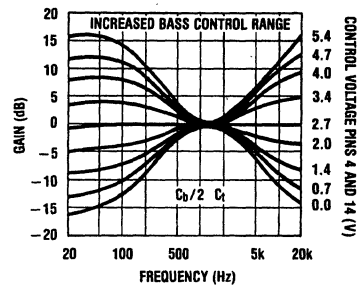

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FIGURE 5. Tone Characteristic (Gain vs Frequency)

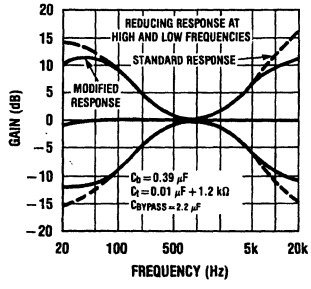

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FIGURE 6. Tone Characteristic (Gain vs Frequency)

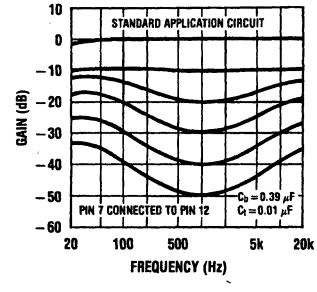

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FIGURE 7. Loudness Compensated Volume Characteristic

Applications Information (Continued)

Figures 8 and *9* illustrate the loudness characteristics obtained with C_b changed to $C_b/2$ and $C_b/4$ respectively, C_t being kept at the nominal 0.01 μF. These values naturally modify the bass tone response as in *Figures 2* and *3*.

With pins 7 (loudness) and 12 (volume) directly connected, loudness control starts at typically −8 dB volume, with most of the control action complete by −30 dB.

Figures 10 and *11* show the effect of resistively offsetting the voltage applied to pin 7 towards the control reference voltage (pin 17). Because the control inputs are high impedance, this is easily done and high value resistors may be used for minimal additional loading. It is possible to reduce the rate of onset of control to extend the active range to −50 dB volume control and below.

The control on pin 7 may also be divided down towards ground bringing the control action on earlier. This is illustrated in *Figure 12*, With a suitable level shifting network between pins 12 and 7, the onset of loudness control and its rate of change may be readily modified.

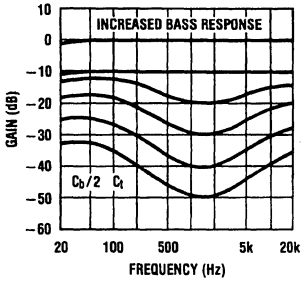

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FIGURE 8. Loudness Compensated Volume Characteristic

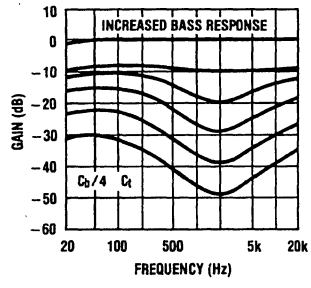

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FIGURE 9. Loudness Compensated Volume Characteristic

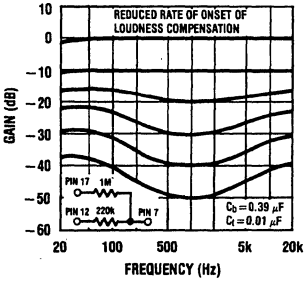

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FIGURE 10. Loudness Compensated Volume Characteristic

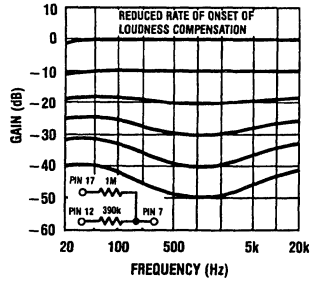

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FIGURE 11. Loudness Compensated Volume Characteristic

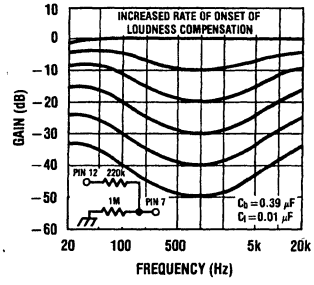

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FIGURE 12. Loudness Compensated Volume Characteristic

Applications Information (Continued)

When adjusted for maximum boost in the usual application circuit, the LM1036 cannot give additional boost from the loudness control with reducing gain. If it is required, some additional boost can be obtained by restricting the tone control range and modifying C_t, C_b, to compensate. A circuit illustrating this for the case of bass boost is shown in *Figure 13*. The resulting responses are given in *Figure 14* showing the continuing loudness control action possible with bass boost previously applied.

USE OF THE LM1036 ABOVE AUDIO FREQUENCIES

The LM1036 has a basic response typically 1 dB down at 250 kHz (tone controls flat) and therefore by scaling C_b and C_t, it is possible to arrange for operation over a wide frequency range for possible use in wide band equalization applications. As an example *Figure 15* shows the responses obtained centered on 10 kHz with $C_b = 0.039\ \mu F$ and $C_t = 0.001\ \mu F$.

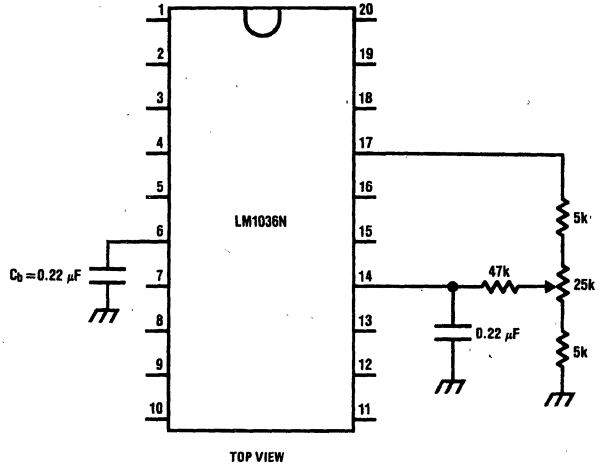

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FIGURE 13. Modified Application Circuit for Additional Bass Boost with Loudness Control

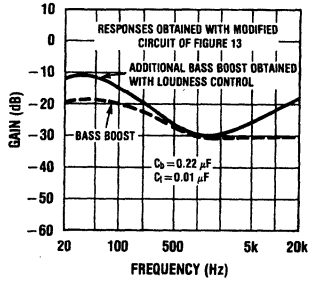

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FIGURE 14. Loudness Compensated Volume Characteristic

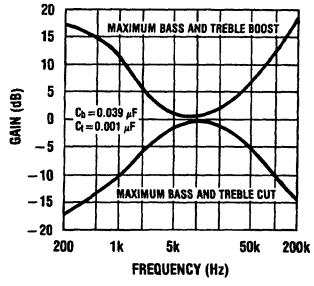

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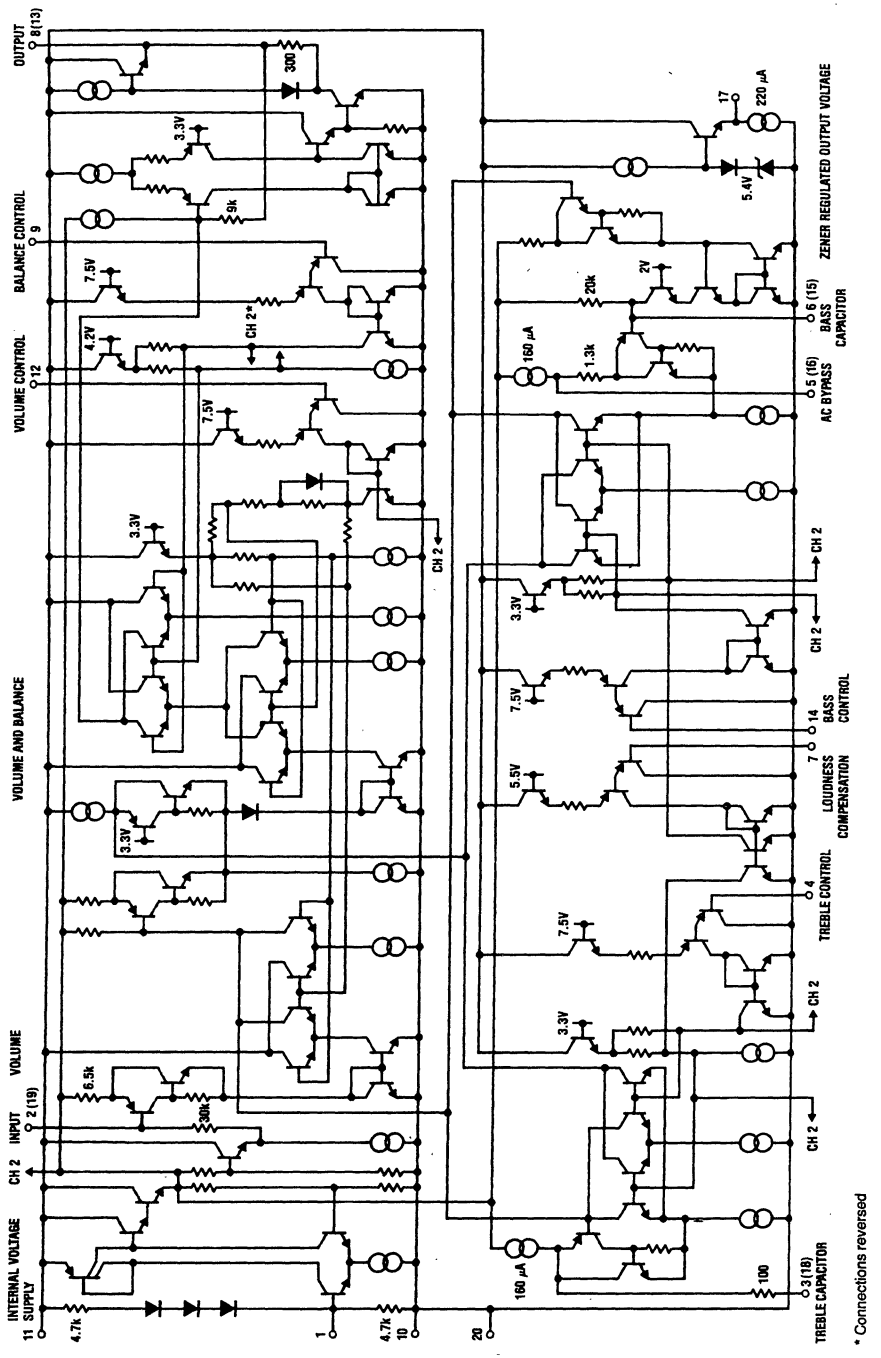
FIGURE 15. Tone Characteristic (Gain vs Frequency)

Simplified Schematic Diagram (One Channel)



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National Semiconductor

PRELIMINARY

LM1040 Dual DC Operated Tone/Volume/Balance Circuit with Stereo Enhancement Facility

General Description

The LM1040 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. A stereo enhancement facility is included whereby the apparent stereo separation of systems requiring closely spaced speakers may be improved. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

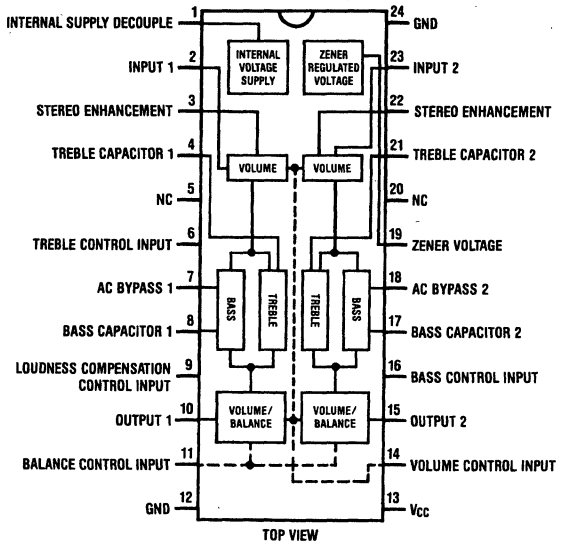
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 9V to 16V
- Large volume control range, 75 dB typical
- Tone control, ±15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 0.3 Vrms
- High signal to noise, 80 dB typical for an input level of 0.3 Vrms
- Few external components required

Block and Connection Diagrams

Dual-in-Line Package



TOP VIEW

TL/H/5147–1

Order Number LM1040N
See NS Package Number N24A

Absolute Maximum Ratings

Supply Voltage	16V	Storage Temperature Range	−65°C to + 150°C
Control Pin Voltage (Pins 6, 9, 11, 14, 16)	V_{CC}	Power Dissipation	1.5W
Operating Temperature Range	0°C to + 70°C	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics $V_{CC}=12V$, $T_A=25°C$ (unless otherwise stated)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range	Pin 13	9		16	V
Supply Current			35	45	mA
Zener Regulated Output Voltage Current	Pin 19		 5.4	 5	 V mA
Maximum Output Voltage	Pins 10, 15; f = 1 kHz $V_{CC}=9V$, Maximum Gain $V_{CC}=12V$		 0.8 1.0		 Vrms Vrms
Maximum Input Voltage (Note 1)	Pins 2, 23; f = 1 kHz, $V_{CC}=9V$ Flat Response, $V_{CC}=12V$ Gain = −10 dB	 1.3	1.1 1.6		Vrms Vrms
Input Resistance	Pins 2, 23; f = 1 kHz	20	30		kΩ
Output Resistance	Pins 10, 15; f = 1 kHz		20		Ω
Maximum Gain	V(Pin 14) = V(Pin 19); f = 1 kHz	−2	0	2	dB
Volume Control Range	f = 1 kHz	70	75		dB
Gain Tracking Channel 1-Channel 2	f = 1 kHz 0 dB through −40 dB −40 dB through −60 dB		 1 2	 3	 dB dB
Balance Control Range	Pins 10, 15; f = 1 kHz		1 −26	 −20	dB dB
Bass Control Range (Note 2)	f = 40 Hz, $C_b=0.39\ \mu F$ V(Pin 16) = V(Pin 19) V(Pin 16) = 0V	 12 −12	 15 −15	 18 −18	 dB dB
Treble Control Range (Note 2)	f = 16 kHz, $C_t=0.01\ \mu F$ V(Pin 6) = V(Pin 19) V(Pin 6) = 0V	 12 −12	 15 −15	 18 −18	 dB dB
Total Harmonic Distortion	f = 1 kHz, $V_{IN}=0.3$ Vrms Gain = 0 dB Gain = −30 dB		 0.06 0.03	 0.3	 % %
Channel Separation	f = 1 kHz, Maximum Gain	60	75		dB
Signal/Noise Ratio	Unweighted 100 Hz-20 kHz Maximum Gain, 0 dB = 0.3 Vrms CCIR/ARM (Note 3) Gain = 0 dB, $V_{IN}=0.3$ Vrms Gain = −20 dB, $V_{IN}=1.0$ Vrms	 76	80 79 72	 	dB dB dB
Output Noise Voltage at Minimum Gain	CCIR/ARM (Note 3)		10	16	μV
Supply Ripple Rejection	200 mVrms, 1 kHz Ripple	35	−50		dB
Control Input Currents	Pins 6, 9, 11, 14, 16 (V = 0V)		−0.6	−2.5	μA
Frequency Response	−1 dB (Flat Response 20 Hz−16 kHz)		250		kHz

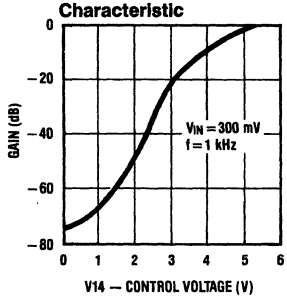
Note 1: The maximum permissible input level is dependent on tone and volume settings. See Application Notes.

Note 2: The tone control range is defined by capacitors C_b and C_t. See Application Notes.

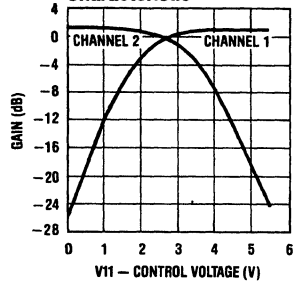
Note 3: Measured with a CCIR filter with a 0 dB level at 2 kHz and an average responding meter.

Typical Performance Characteristics

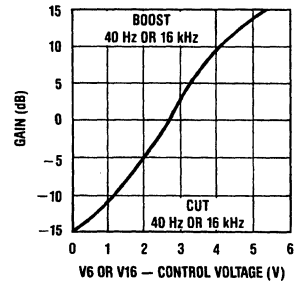
Volume Control Characteristic



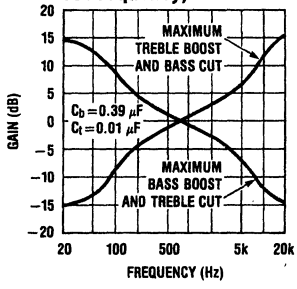
Balance Control Characteristic



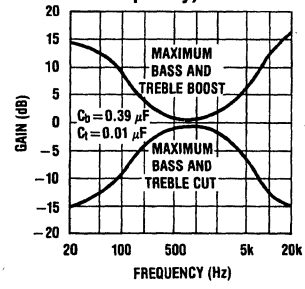
Tone Control Characteristic



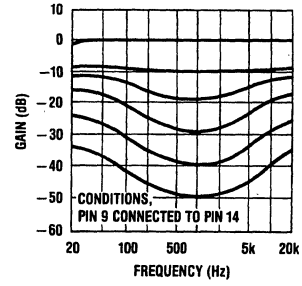
Tone Characteristic (Gain vs Frequency)



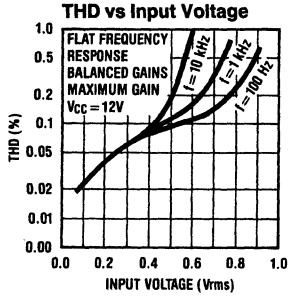
Tone Characteristic (Gain vs Frequency)



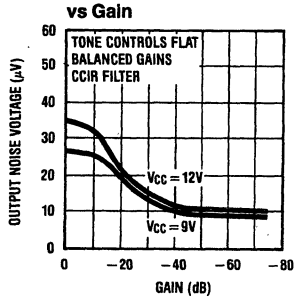
Loudness Compensated Volume Characteristic



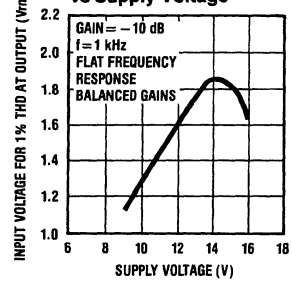
THD vs Input Voltage



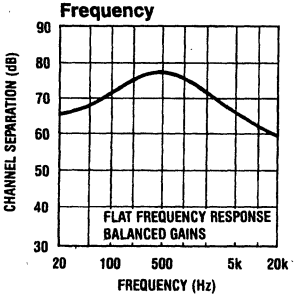
Output Noise Voltage vs Gain



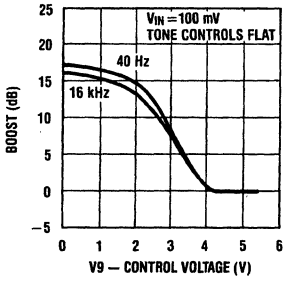
Input Signal Handling vs Supply Voltage



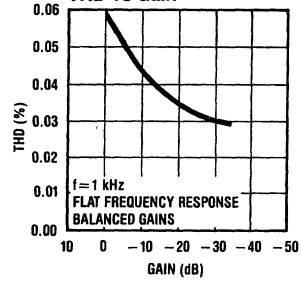
Channel Separation vs Frequency



Loudness Control Characteristic



THD vs Gain



TL/H/5147–2

Application Notes

TONE RESPONSE

The maximum boost and cut can be optimized for individual applications by selection of the appropriate values of C_t (treble) and C_b (bass).

The tone responses are defined by the relationships:

$$\text{Bass Response} = \frac{1 + \dfrac{0.00065(1 - a_b)}{j\omega C_b}}{1 + \dfrac{0.00065a_b}{j\omega C_b}}$$

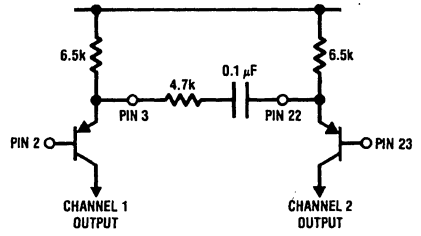
$$\text{Treble Response} = \frac{1 + j\omega 5500(1 - a_t)C_t}{1 + j\omega 5500a_tC_t}$$

Where $a_b = a_t = 0$ for maximum bass and treble boost respectively and $a_b = a_t = 1$ for maximum cut.

For the values of C_b and C_t of 0.39 μF and 0.01 μF as shown in the Application Circuit, 15 dB of boost or cut is obtained at 40 Hz and 16 kHz.

STEREO ENHANCEMENT

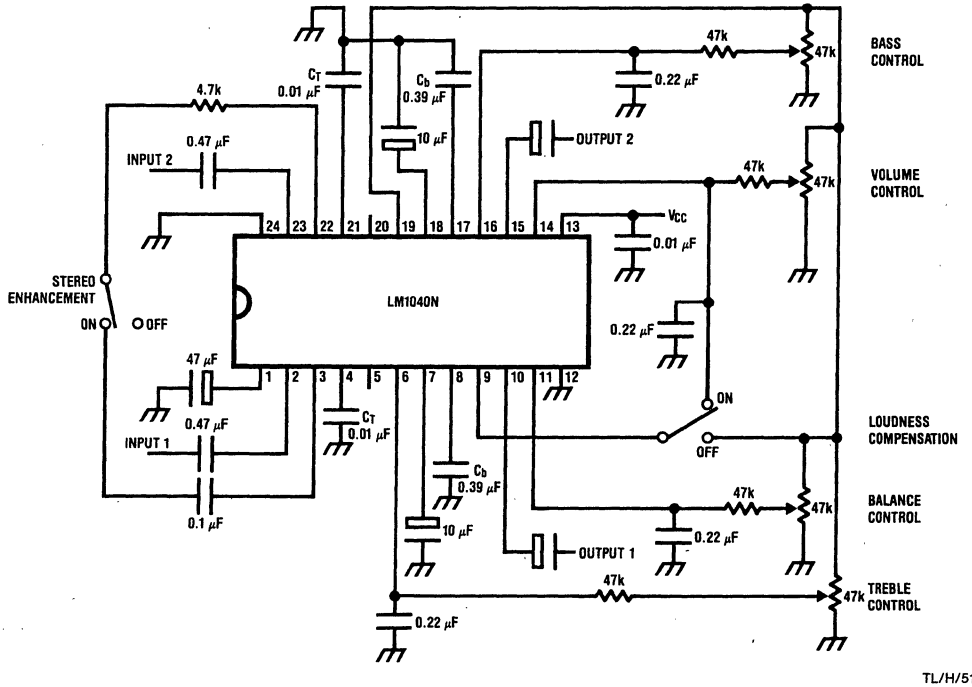
When stereo system speakers need to be closer than optimum because of equipment/cabinet limitations, an improved stereo effect can be obtained using a modest amount of phase—reversed interchannel cross-coupling. In the LM1040 the input stage transistor emitters are brought out to facilitate this. The arrangement is shown below in basic form.



TL/H/5147–3

With a monophonic source, the emitters have the same signal and the resistor and capacitor connected between them have no effect. With a stereo signal each transistor works in the grounded base mode for stereo components, generating an in-phase signal from the opposite channel. As the normal signals are inverted at this point, the appropriate phase-reversed cross-coupling is achieved. An effective level of coupling of 60% can be obtained using 4.7k in conjunction with the internal 6.5k emitter resistors. At low frequencies, speakers become less directional and it becomes desirable to reduce the enhancement effect. With a 0.1 μF coupling capacitor, as shown, roll-off occurs below 330 Hz. The coupling components may be varied for alternative responses.

Application Circuit



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Application Notes (Continued)

ZENER VOLTAGE

A zener voltage (pin 19 = 5.4V) is provided which may be used to bias the control potentiometers. Setting a DC level of one half of the zener voltage on the control inputs, pins 6, 11, and 16, results in the balanced gain and flat response condition. Typical spread on the zener voltage is ±100 mV and this must be taken into account if control signals are used which are not referenced to the zener voltage. If this is the case, then they will need to be derived with similar accuracy.

LOUDNESS COMPENSATION

A simple loudness compensation may be effected by applying a DC control voltage to pin 9. This operates on the tone control stages to produce an additional boost limited by the maximum boost defined by C_b and C_t. There is no loudness compensation when pin 9 is connected to pin 19. Pin 9 can be connected to pin 14 to give the loudness compensated volume characteristic as illustrated without the addition of further external components. (Tone settings are for flat response, C_b and C_t as given in Application Circuit.) Modification to the loudness characteristic is possible by changing the capacitors C_b and C_t for a different basic response or, by a resistor network between pins 9 and 14 for a different threshold and slope.

SIGNAL HANDLING

The volume control function of the LM1040 is carried out in two stages, controlled by the DC voltage on pin 14, to improve signal handling capability and provide a reduction of output noise level at reduced gain. The first stage is before the tone control processing and provides an initial 15 dB of gain reduction, so ensuring that the tone sections are not overdriven by large input levels when operating with a low volume setting. Any combination of tone and volume settings may be used provided the output level does not exceed 1 Vrms, V_{CC} = 12V(0.7 Vrms, V_{CC} = 9V). At reduced gain (< −6 dB) the input stage will overload if the input level exceeds 1.6 Vrms, V_{CC} = 12V (1.1 Vrms, V_{CC} = 9V). As there is volume control on the input stages, the inputs may be operated with a lower overload margin than would otherwise be acceptable, allowing a possible improvement in signal to noise ratio.

Applications Information

OBTAINING MODIFIED RESPONSE CURVES

The LM1040 is a dual DC controlled bass, treble, balance and volume integrated circuit ideal for stereo audio systems.

In the various applications where the LM1040 can be used, there may be requirements for responses different to those of the standard application circuit given in the data sheet. This application section details some of the simple variations possible on the standard responses, to assist the choice of optimum characteristics for particular applications.

TONE CONTROLS

Summarizing the relationship given in the data sheet, basically for an increase in the treble control range C_t must be increased, and for increased bass range C_b must be reduced.

Figure 1 shows the typical tone response obtained in the standard application circuit. (C_t = 0.01 µF, C_b = 0.39 µF). Response curves are given for various amounts of boost and cut.

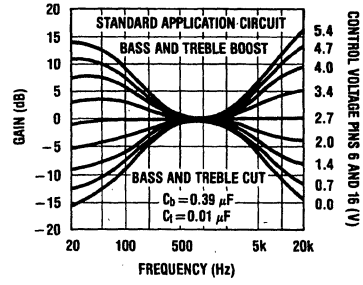

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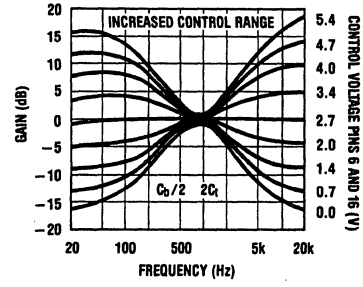
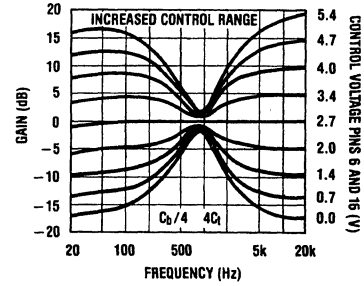
FIGURE 1. Tone Characteristic (Gain vs Frequency)

Figures 2 and *3* show the effect of changing the response defining capacitors C_t and C_b to 2Ct, $C_b/2$ and $4C_t$, $C_b/4$ respectively, giving increased tone control ranges. The values of the bypass capacitors may become significant and affect the lower frequencies in the bass response curves.



TL/H/5147–6

FIGURE 2: Tone Characteristic (Gain vs Frequency)



TL/H/5147–7

FIGURE 3: Tone Characteristic (Gain vs Frequency)

Applications Information (Continued)

Figure 4 shows the effect of changing C_t and C_b in the opposite direction to $C_t/2$, $2C_b$ respectively giving reduced control ranges. The various results corresponding to the different C_t and C_b values may be mixed if it is required to give a particular emphasis to, for example, the bass control. The particular case with $C_b/2$, C_t is illustrated in *Figure 5*.

RESTRICTION OF TONE CONTROL ACTION AT HIGH OR LOW FREQUENCIES

It may be desired in some applications to level off the tone responses above or below certain frequencies for example to reduce high frequency noise.

This may be achieved for the treble response by including a resistor in series with C_t. The treble boost and cut will be 3 dB less than the standard circuit when $R = X_C$.

A similar effect may be obtained for the bass response by reducing the value of the AC bypass capacitors on pins 7 (channel 1) and 18 (channel 2). The internal resistance at these pins is 1.3 kΩ and the bass boost/cut will be approximately 3 dB less with X_C at this value. An example of such modified response curves is shown in *Figure 6*. The input coupling capacitors may also modify the low frequency response.

It will be seen from *Figures 2* and *3* that modifying C_t and C_b for greater control range also has the effect of flattening the tone control extremes and this may be utilized, with or without additional modification as outlined above, for the most suitable tone control range and response shape.

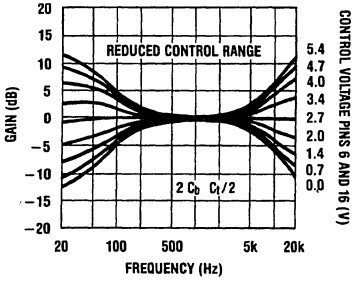
OTHER ADVANTAGES OF DC CONTROLS

The DC controls make the addition of other features easy to arrange. For example, the negative-going peaks of the output amplifiers may be detected below a certain level, and used to bias back the bass control from a high boost condition; to prevent overloading the speaker with low frequency components.

LOUDNESS CONTROL

The loudness control is achieved through control of the tone sections by the voltage applied to pin 9; therefore, the tone and loudness functions are not independent. There is normally 1 dB more bass than treble boost (40 Hz−16 kHz) with loudness control in the standard circuit. If a greater difference is desired, it is necessary to introduce an offset by means of C_t or C_b or by changing the nominal control voltage ranges.

Figure 7 shows the typical loudness curves obtained in the standard application circuit at various volume levels ($C_b = 0.39\ \mu F$).



TL/H/5147–8

FIGURE 4. Tone Characteristic (Gain vs Frequency)

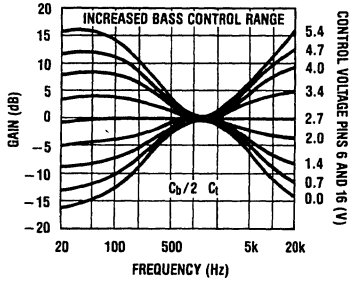


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FIGURE 5. Tone Characteristic (Gain vs Frequency)

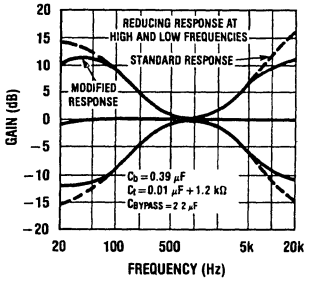

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FIGURE 6. Tone Characteristic (Gain vs Frequency)

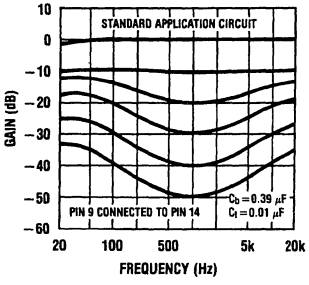

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FIGURE 7. Loudness Compensated Volume Characteristic

Applications Information (Continued)

Figures 8 and *9* illustrate the loudness characteristics obtained with C_b changed to $C_b/2$ and $C_b/4$ respectively, C_t being kept at the nominal 0.01 μF. These values naturally modify the bass tone response as in *Figures 2* and *3.*

With pins 9 (loudness) and 14 (volume) directly connected, loudness control starts at typically −8 dB volume, with most of the control action complete by −30 dB.

Figures 10 and *11* show the effect of resistively offsetting the voltage applied to pin 9 towards the control reference voltage (pin 19). Because the control inputs are high impedance, this is easily done and high value resistors may be used for minimal additional loading. It is possible to reduce the rate of onset of control to extend the active range to −50 dB volume control and below.

The control on pin 9 may also be divided down towards ground bringing the control action on earlier. This is illustrated in *Figure 12.* With a suitable level shifting network between pins 14 and 9, the onset of loudness control and its rate of change may be readily modified.

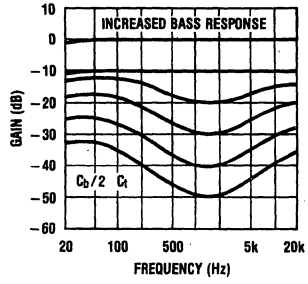

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FIGURE 8. Loudness Compensated Volume Characteristic

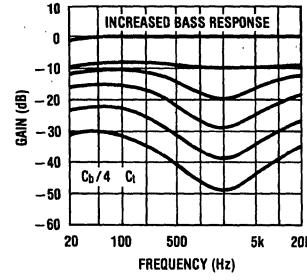

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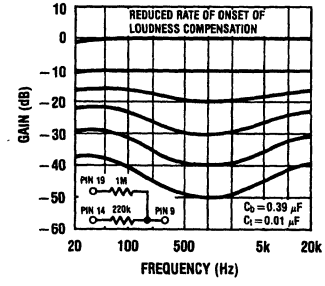
FIGURE 9. Loudness Compensated Volume Characteristic



TL/H/5147–14

FIGURE 10. Loudness Compensated Volume Characteristic

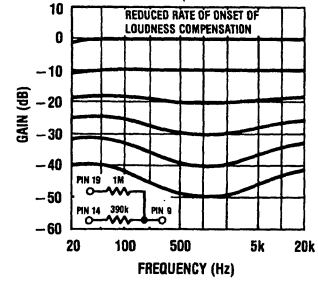


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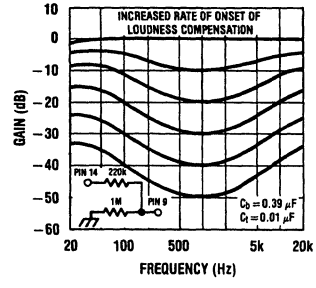
FIGURE 11. Loudness Compensated Volume Characteristic



TL/H/5147–16

FIGURE 12. Loudness Compensated Volume Characteristic

Applications Information (Continued)

When adjusted for maximum boost in the usual application circuit, the LM-1040 cannot give additional boost from the loudness control with reducing gain. If it is required, some additional boost can be obtained by restricting the tone control range and modifying C_t, C_b, to compensate. A circuit illustrating this for the case of bass boost is shown in *Figure 13*. The resulting responses are given in *Figure 14* showing the continuing loudness control action possible with bass boost previously applied.

USE OF THE LM1040 ABOVE AUDIO FREQUENCIES

The LM1040 has a basic response typically 1 dB down at 250 kHz (tone controls flat) and therefore by scaling C_b and C_t, it is possible to arrange for operation over a wide frequency range for possible use in wide band equalization applications. As an example *Figure 15* shows the responses obtained centered on 10 kHz with $C_b = 0.039\ \mu F$ and $C_t = 0.001\ \mu F$.

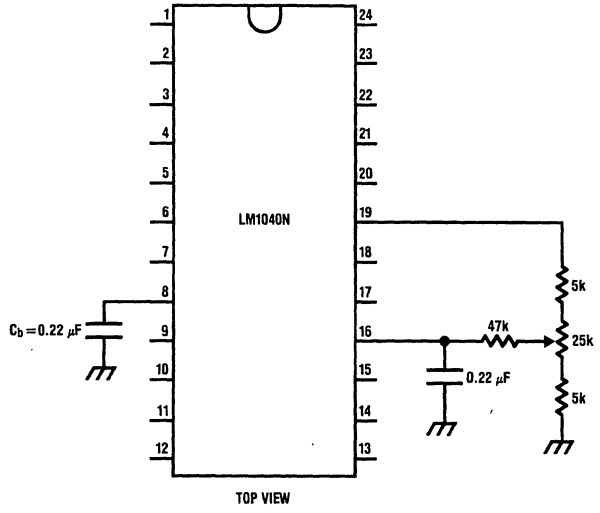


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FIGURE 13. Modified Application Circuit for Additional Bass Boost with Loudness Control

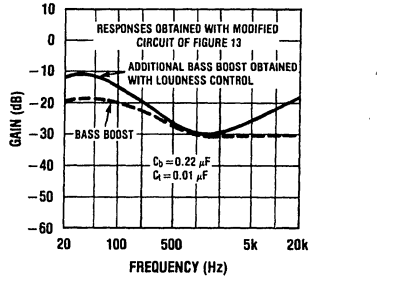

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FIGURE 14. Loudness Compensated Volume Characteristic

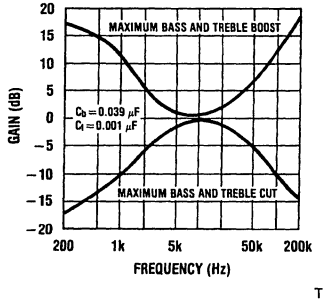

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FIGURE 15. Tone Characteristic (Gain vs Frequency)

S 12

Applications Information (Continued)

DC CONTROL OF STEREO ENHANCEMENT AND LOUDNESS CONTROL

Figure 16 shows a possible circuit if electronic control of these functions is required. the typical DC level at pins 3 and 22 is 7.5V (V_{CC} = 12V), with the input signal superimposed, and this can be used to bias a FET switch as shown to save components. For switching with a 0V−5V signal a low-threshhold FET is required when using a 12V supply. With larger switching levels this is less critical.

The high impedance PNP base input of the loudness control pin 9 is readily switched with a general purpose NPN transistor.

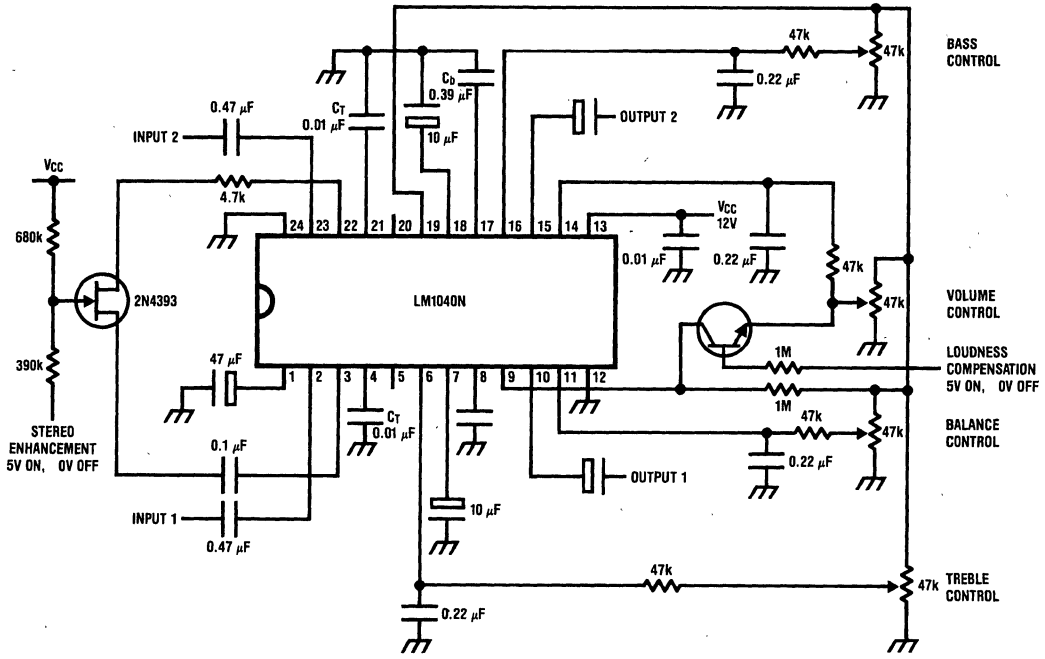

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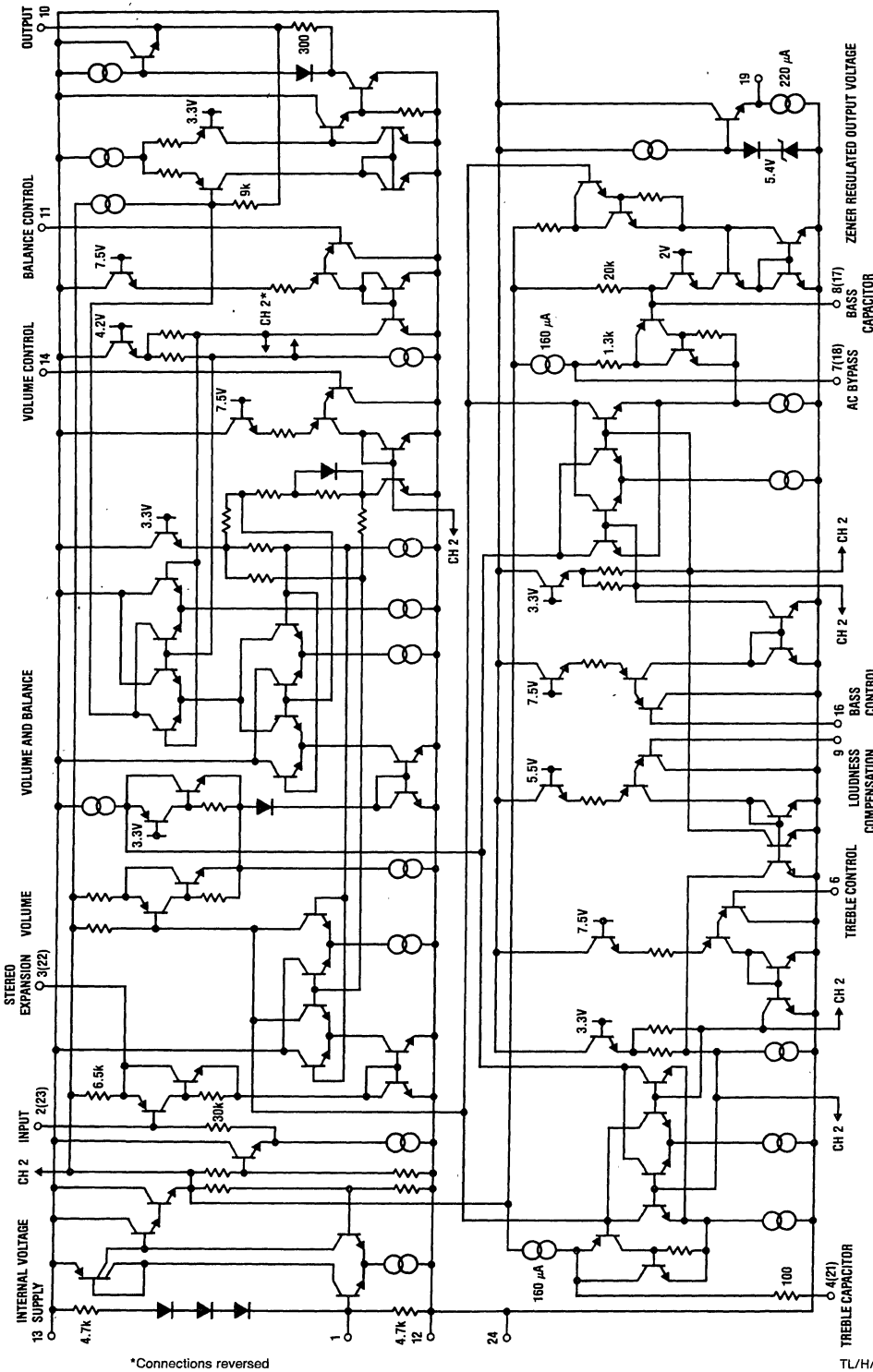
FIGURE 16. Application Circuit with Electronic Switching

Simplified Schematic Diagram (One Channel)



National Semiconductor

PRELIMINARY

LM1121A/LM1121B/LM1121C Dolby B-Type Noise Reduction Processor with DC Switching

General Description

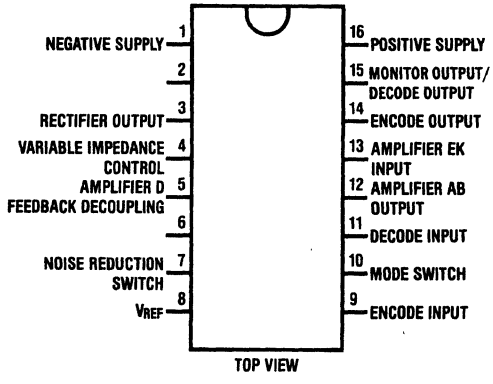
The LM1121 is a monolithic integrated circuit designed to realize the Dolby B-type noise reduction system. It features two separate inputs and outputs for encode and decode signal paths. Both the mode selection and noise reduction switches are internal and controlled by external DC voltage levels.

Features

- DC switching of both encode/decode and noise reduction ON/OFF
- Separate inputs and outputs for encode and decode
- Full-wave detector circuit
- Very close matching to standard Dolby characteristics
- Very high signal/noise ratio—75 dB encode (CCIR/ARM), 83 dB decode
- Very high signal handling capability, >20 dB (V_S=20V)
- Encode output may be used for meter drive in all modes

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5160–1

Order Number LM1121AN, LM1121BN or LM1121CN
See NS Package Number N16E

Available to licensees of Dolby Laboratories Licensing Corporation, San Francisco, CA, from whom licensing and applications information must be obtained.

Absolute Maximum Ratings

Supply Voltage	21V	Storage Temperature Range	−60°C to +150°C
Operating Temperature Range	−20°C to +70°C	Lead Temp. (Soldering, 10 seconds)	300°C

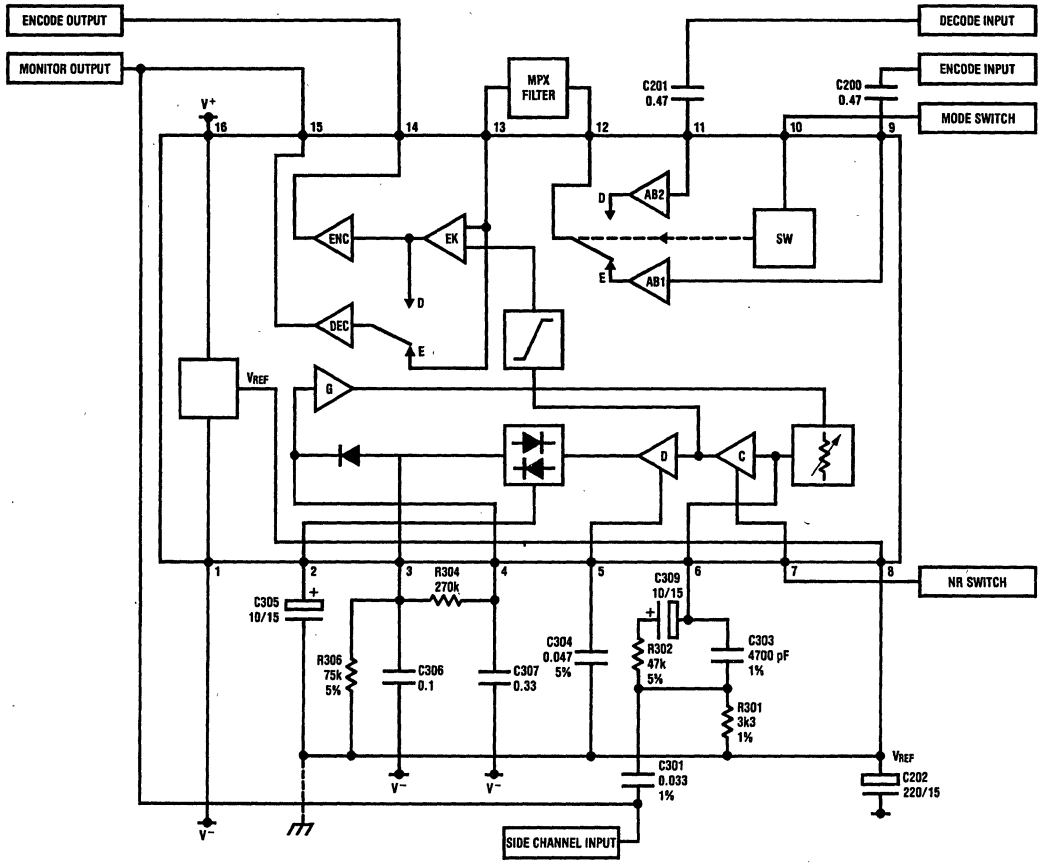
Electrical Characteristics

(V_S = 12V, T_A = 25°C unless otherwise specified) N.B. 0 dB refers to Dolby level and is 580 mVrms measured at TP1.

Parameter	Conditions	LM1121A			LM1121B			LM1121C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		7		20	7		20	7		20	V
Supply Current			17	24		17	24		17	24	mA
Voltage Gain Pins 9–14 and 11–15	1 kHz, Noise Reduction OFF	25.2	25.7	26.2	24.7	25.7	26.7	24.2	25.7	27.2	dB
Voltage Gain Pin 9 or 11–12	1 kHz, Pin 12 Open		19.7			19.7			19.7		dB
Signal/Noise Ratio	CCIR/Arm Filter										
Encode	Pin 14, R_S = 10k	71.5			71			69			dB
	R_S = 1k		75			75			75		dB
Decode	Pin 15, R_S = 10k		83			83			83		dB
NR OFF	Pins 14 and 15										
	R_S = 10k		83			83			83		dB
	R_S = 1k		85			85			85		dB
Encode Characteristics	10 kHz, 0 dB	0	0.5	1.0	−0.2	0.5	1.2	−0.5	0.5	1.5	dB
	1.3 kHz, −20 dB	−16.2	−15.7	−15.2	−16.7	−15.7	−14.7	−17.2	−15.7	−14.2	dB
	5 kHz, −20 dB	−17.3	−16.8	−16.3	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	3 kHz, −30 dB	−21.7	−21.2	−20.7	−22.2	−21.2	−20.2	−22.7	−21.2	−19.7	dB
	5 kHz, −30 dB	−22.3	−21.8	−21.3	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	10 kHz, −30 dB	−24.0	−23.5	−23.0	−24.5	−23.5	−22.5	−25.0	−23.5	−22.0	dB
	10 kHz, −40 dB	−30.1	−29.6	−29.1	−30.3	−29.6	−28.9	−30.6	−29.6	−28.6	dB
Variation in Encode Characteristics with Temperature	0°C−70°C		< ±0.5			< ±0.5			< ±0.5		dB
Distortion	1 kHz, 0 dB		0.03	0.1		0.03	0.1		0.03	0.2	%
	10 kHz, 8 dB		0.2			0.2			0.2		%
Signal Handling	1 kHz, Dist = 0.3%										
	V_S = 7.5V	10	11.2		10	11.2		10	11.2		dB
	V_S = 12V		16.0			16.0			16.0		dB
	V_S = 20V		21.0			21.0			21.0		dB
Switching Transients Measured at Pin 14 or 15 Encode/ Decode/Encode	See *Figure 1*		20			20			20		mV
NR OFF/ON/OFF			20			20			20		mV
Input Resistance	Pins 9 and 11	45	65	80	45	65	80	45	65	80	kΩ
	Pin 13	4.3	5.6	6.9	4.3	5.6	6.9	4.3	5.6	6.9	kΩ
Output Resistance	Pin 12	1.8	2.4	3.0	1.8	2.4	3.0	1.8	2.4	3.0	kΩ
	Pins 14 and 15		30	55		30	55		30	55	Ω
Control Levels (Pin 7)	V_S = 7V−20V										
NR OFF		3.4		V_S	3.4		V_S	3.4		V_S	V
NR OFF			Open			Open			Open		
NR ON		−0.2		1.2	−0.2		1.2	−0.2		1.2	V
Control Levels (Pin 10)	V_S = 7V−20V										
Encode		3.4		V_S	3.4		V_S	3.4		V_S	V
Decode			Open			Open			Open		
Decode		−0.2		1.2	−0.2		1.2	−0.2		1.2	V
Input Resistance	Pins 7 and 10		21			21			21		kΩ

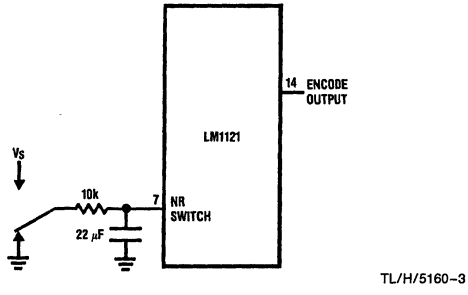
S 12

Schematic Diagram



TL/H/5160–2

Circuit Diagram



TL/H/5160–3

FIGURE 1. Measurement—Switching Transients

National Semiconductor

PRELIMINARY

LM1819 Air-Core Meter Driver

General Description

The LM1819 is a function generator/driver for air-core (moving-magnet) meter movements. A Norton amplifier and an NPN transistor are included on chip for signal conditioning as required. Driver outputs are self-centering and develop ±4.5V swing at 20 mA. Better than 2% linearity is guaranteed over a full 305-degree operating range.

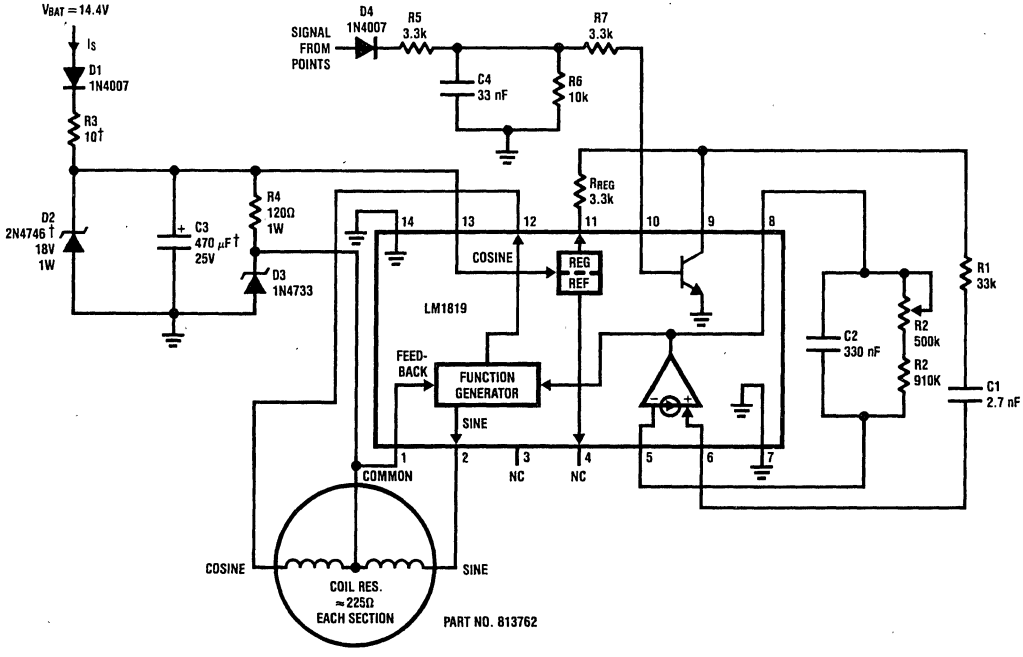
Features

- Self-centering 20 mA outputs
- 12V operation
- Norton amplifier
- Function generator

Applications

- Air-core meter driver
- Tachometers
- Ruggedized instruments

Typical Application



TL/H/5263–1

FIGURE 1. Automotive Tachometer Application. Circuit shown operates with 4 cylinder engine and deflects meter pointer (270°) at 6000 RPM.

Order Number LM1819N
See NS Package Number N14A

Absolute Maximum Ratings

Supply Voltage, V^+ (pin 13)	20V	Storage Temperature	−65°C to −150°C
Power Dissipation (note 1)	700 mW	Lead Temp. (Soldering, 10 seconds)	300°C
Operating Temperature	−40°C to 85°C	BV_{CEO}	$20V_{MIN}$

Electrical Characteristics V_S = 13.1V T_A = 25°C unless otherwise specified

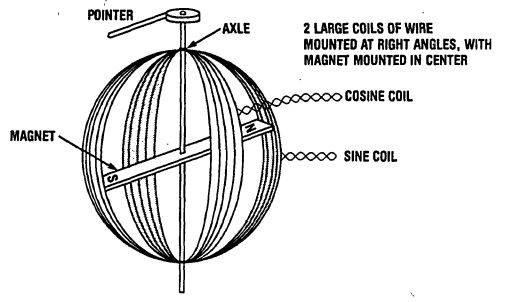
Parameter	Pin(s)	Conditions	Min	Typ	Max	Symbol	Units
Supply Current	13	Zero Input Frequency (See *Figure 1*)			65	I_S	mA
Regulator Voltage	11	I_{REG} = 0 mA	8.1	8.5	8.9	V_{REG}	V
Regulator Output Resistance	11	I_{REG} = 0 to 3 mA		13.5			Ω
Reference Voltage	4	I_{REF} = 0 mA	1.9	2.1	2.3	V_{REF}	V
Reference Output Resistance	4	I_{REF} = 0 to 50 μA		5.3			kΩ
Norton Amplifier Mirror Gain	5, 6	$I_{BIAS} \cong$ 20 μA	.9	1.0	1.1		
NPN Transistor DC Gain	9, 10			125		h_{FE}	
Function Generator Feedback Bias Current	1	V_1 = 5.1V		1.0			mA
Drive Voltage Extremes, Sine and Cosine	2, 12	I_{LOAD} = 20 mA	±4	±4.5			V
Sine Output Voltage with Zero Input	2	$V_8 = V_{REF}$	−350	0	+350		mV
Function Generator Linearity		FSD = 305°			±1.7		%FSD
Function Generator Gain		Meter Deflection/ ΔV_8	50.75	53.75	56.75	k	Degrees/ Volt

Note 1: For operation above 25°C, the LM1819 must be derated based upon a 125°C maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed circuit board and operating in a still-air ambient.

Application Hints

AIR-CORE METER MOVEMENTS

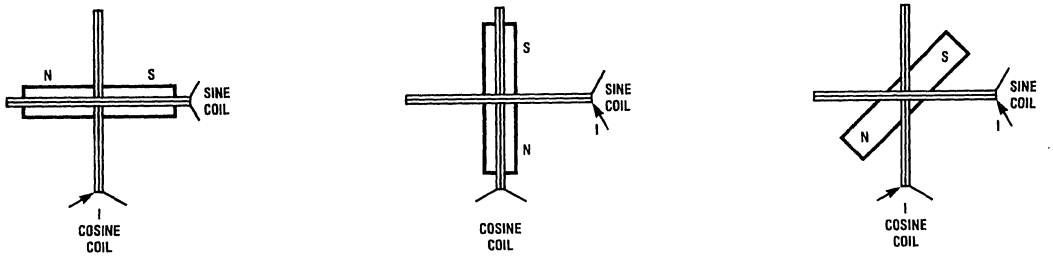
Air-core meters are often favored over other movements as a result of their mechanical ruggedness and their independence of calibration with age. A simplified diagram of an air-core meter is shown in *Figure 2*. There are three basic pieces: a magnet and pointer attached to a freely rotating axle, and two coils, each oriented at a right angle with respect to the other. The only moving part in this meter is the axle assembly. The magnet will tend to align itself with the vector sum of **H** fields of each coil, where **H** is the magnetic field strength vector. If, for instance, a current passes through the cosine coil (the reason for this nomenclature will become apparent later) as shown in *Figure 3(a)*, the magnet will align its magnetic axis with the coil's **H** field. Similarly, a current in the sine coil (*Figure 3(b)*) causes the magnet to align itself with the sine **H** field. If currents are applied simultaneously to both sine and cosine coils, the magnet will turn to the direction of the vector sum of the two **H** fields (*Figure 3(c)*). **H** is proportional to the voltage applied to a coil. Therefore, by varying both the polarity and magnitude of the coil voltages the axle assembly can be made to rotate a full 360°. The LM1819 is designed to drive the meter through a minimum of 305°.



TL/H/5263–2

FIGURE 2. Simplified Diagram of an Air Core Meter.

Application Hints (Continued)



TL/H/5263–3

(a) (b) (c)

FIGURE 3. Magnet and pointer position are controlled by the B field generated by the two drive coils.

In an air-core meter the axle assembly is supported by two nylon bushings. The torque exerted on the pointer is much greater than that found in a typical d'Arsonval movement. In contrast to a d'Arsonval movement, where calibration is a function of spring and magnet characteristics, air-core meter calibration is only affected by the mechanical alignment of the drive coils. Mechanical calibration, once set at manufacture, can not change.

Making pointer position a linear function of some input is a matter of properly ratioing the drive to each coil. The **H** field contributed by each coil is a function of the applied current, and the current is a function of the coil voltage. Our desired result is to have θ (pointer deflection, measured in degrees) proportional to an input voltage:

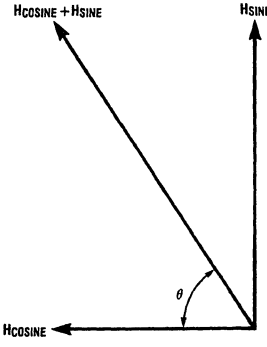
$$\theta = kV_{IN} \qquad [1]$$

where k is a constant of proportionality, with units of degrees/volt. The vector sum of each coils' **H** field must follow the deflection angle θ. We know that the axle assembly always points in the direction of the vector sum of H_{SINE} and H_{COSINE}. This direction (see *Figure 4*) is found from the formula:

$$(\theta) = \arctan \{ | H_{SINE} | / | H_{COSINE} | \} \qquad [2]$$

Recalling some basic trigonometry,

$$(\theta) = \arctan(\sin(\theta) / \cos(\theta)) \qquad [3]$$



TL/H/5263–4

FIGURE 4. The vector sum of H_{COSINE} and H_{SINE} points in a direction θ measured in a clockwise direction from H_{COSINE}.

Comparing [3] to [2] we see that if we allow H_{SINE} to vary as the sine of θ, and H_{COSINE} to vary as the cosine of θ, we will generate a net **H** field whose direction is the same as θ. And since the axle assembly aligns itself with the net **H** field, the pointer will always point in the direction of θ.

THE LM1819

Included in the LM1819 is a function generator whose two outputs are designed to vary approximately as the sine and cosine of an input. A minimum drive of ±20 mA at ±4V is available at pins 2 (sine) and 12 (cosine). The common side of each coil is returned to a 5.1V zener diode reference and fed back to pin 1.

For the LM1819, k≅54°/V (from equation 1). The function generator input (pin 8) is internally connected to the Norton amplifier's output. V_{IN} as considered in equation [1] is actually the difference of the voltages at pins 8 (Norton output/function generator input) and 4. Typically the reference voltage at pin 4 is 2.1V. Therefore,

$$\theta = 54(V_8 - 2.1) \qquad [4]$$

As V_8 varies from 2.1V to 7.75V, the function generator will drive the meter through the chip's rated 305° range.

Air-core meters are mechanically zeroed during manufacture such that when only the cosine coil is driven, the pointer indicates zero degrees deflection. However, in some applications a slight trim or offset may be required. This is accomplished by sourcing or sinking a DC current of a few microamperes at pin 4.

A Norton amplifier is available for conditioning various input signals and driving the function generator. A Norton amplifier was chosen since it makes a simple frequency to voltage converter. While the non-inverting input (pin 6) bias is at one diode drop above ground, the inverting input (5) rides on a 2.1V level, equal to the pin 4 reference. Mirror gain remains essentially flat to $I_{MIRROR} = 5$ mA. The Norton amplifier's output (8) is designed to source current into its load. To bypass the Norton amplifier simply ground the non-inverting input, tie the inverting input to the reference, and drive pin 8 (Norton output/function generator input) directly.

An NPN transistor is included on chip for buffering and squaring input signals. Its usefulness is exemplified in *Figures 1 & 5* where an ignition pulse is converted to a rectangular wave form by an RC network and the transistor. The emitter is internally connected to ground. It is important not to allow the base to drop below $-5V_{dc}$, as damage may occur to the device. The 2.1V reference previously described is derived from an 8.5V regulator at pin 11. Pin 11 is used as a stable supply for collector loads, and currents of up to 5 mA are easily accommodated.

Application Hints (Continued)

TACHOMETER APPLICATION

A measure of the operating level of any motor or engine is the rotational velocity of its output shaft. In the case of an automotive engine the crankshaft speed is measured using the units "revolutions per minute" (RPM). It is possible to indirectly measure the speed of the crankshaft by using the signal present on the engine's ignition coil. The fundamental frequency of this signal is a function of engine speed and the number of cylinders and is calculated (for a four-stroke engine) from the formula:

$$f = n\omega/120 \quad \text{(Hz)} \quad (5)$$

where n = number of cylinders, and ω = rotational velocity of the crankshaft in RPM. From this formula the maximum frequency normally expected (for an 8 cylinder engine turning 4500RPM) is 300 Hz. In certain specialized ignition systems (motorcycles and some automobiles) where the coil waveform is operated at twice this frequency ($f = n\omega/60$). These systems are identified by the fact that multiple coils are used in lieu of a single coil and distributor. Also, the coils have two outputs instead of one.

A typical automotive tachometer application is shown in *Figure 1*. The coil waveform is filtered, squared and limited by the RC network and NPN transistor. The frequency of the pulse train at pin 9 is converted to a proportional voltage by the Norton amplifier's charge pump configuration. The ignition circuit shown in *Figure 5* is typical of automotive systems. The switching element "S" is opened and closed in synchronism with engine rotation. When "S" is closed, energy is stored in Lp. When opened, the current in Lp diverts from "S" into C. The high voltage produced in Ls when "S" is opened is responsible for the arcing at the spark plug. The coil voltage (see *Figure 6*) can be used as an input to the LM1819 tachometer circuit. This waveform is essentially constant *duty cycle*. D4 rectifies this waveform thereby preventing negative voltages from reaching the chip. C4 and R5 form a low pass filter which attenuates the high frequency ringing, and R7 limits the input current to about 2.5mA. R6 acts as a base bleed to shut the transistor OFF when "S" is closed. The collector is pulled up to the internal regulator by R_{REG}. The output at pin 9 is a clean rectangular pulse.

Many ignition systems use magnetic, hall effect or optical sensors to trigger a solid state switching element at "S." These systems (see the LM1815) typically generate pulses of constant *width* and amplitude suitable for driving the charge pump directly.

The charge pump circuit in *Figure 7* can be operated in two modes: constant input pulse width (C1 acts as a coupling capacitor) and constant input duty cycle (C1 acts as a differentiating capacitor). The transfer functions for these two modes are quite diverse. However, deflection is always directly proportional to R2 and ripple is proportional to C2.

The following variables are used in the calculation of meter deflection:

symbol	description
n	number of cylinders
ω, ω_{IDLE}	engine speed at redline and idle, RPM
θ	pointer deflection at redline, degrees
δ	charge pump input pulse width, seconds
V_{IN}	peak to peak input voltages, volts
$\Delta\theta$	maximum desired ripple, degrees
k	function generator gain, degees/volt
f, f_{IDLE}	input frequency at redline and idle, Hz

Where the NPN transistor and regulator are used to create a pulse $V_{IN} = 8.5V$. Acceptable ripple ranges from 3 to 10 degrees (a typical pointer is about 3 degrees wide) depending on meter damping and the input frequency.

The constant pulse width circuit is designed using the following equations:

(1) $100\ \mu A < \frac{V_{IN}}{R1} < 3\ mA$

(2) $C_1 \geq \frac{10\delta}{R_1}$

(3) $R_2 = \frac{R_1\theta}{V_{IN}\delta k f_1} = \frac{120R_1\theta}{V_{IN}\eta\omega\delta k_1}$

(4) $C_2 = \frac{}{R_2\Delta\theta f_{IDLE}} = \frac{}{R_2\Delta\theta\eta\omega_{IDLE}}$

The constant duty cycle equations are as follows:

$R_{REG} \geq 3\ k\Omega$

$R_1 \leq V_{IN} x 10^4 - R_{REG}$

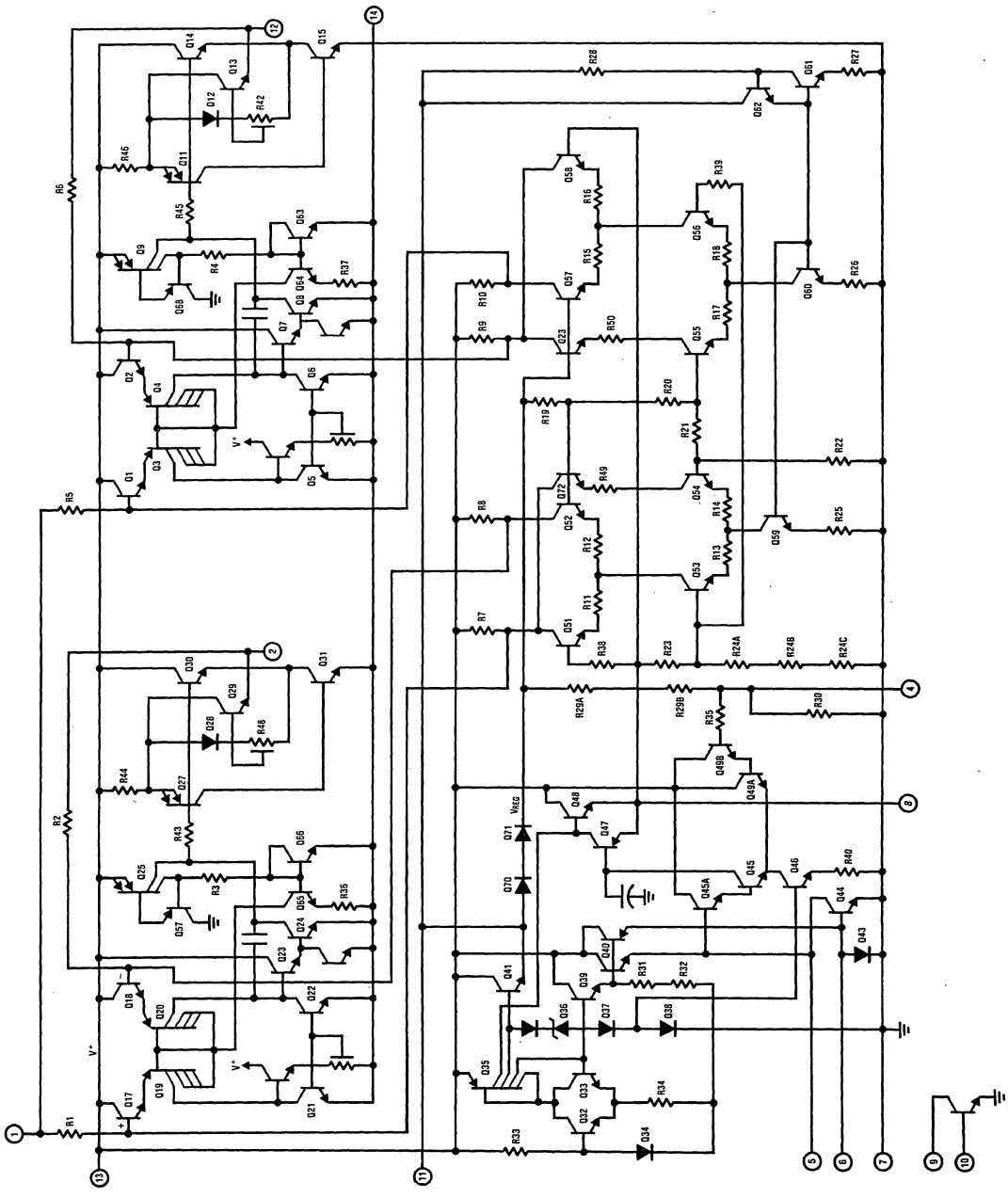
$C_1 \leq \delta/10(R_{REG} + R_1)$

$R_Z = \theta/3.54n\omega C_1 = \theta/425 f C_1$

$C_2 = 425C_1/\Delta\theta$

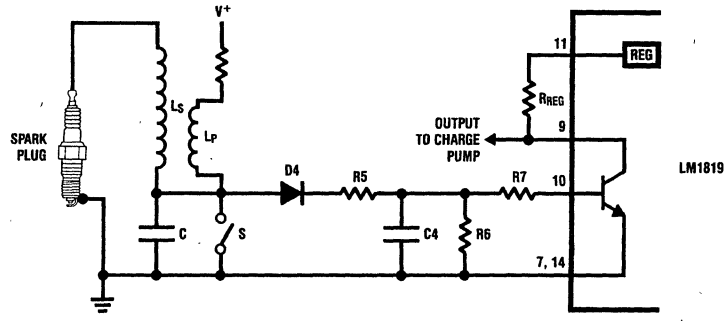
The values in *Figure 1* were calculated with n = 4, ω = 6000RPM, θ = 270 degrees, δ = 1 ms, $V_{IN} = V_{REG} = 8.5V$ and $\Delta\theta = 3$ degrees in the constant duty cycle mode. For distributorless ignitions these same equations will apply if $n\omega/60$ is substituted for F.

Equivalent Schematic



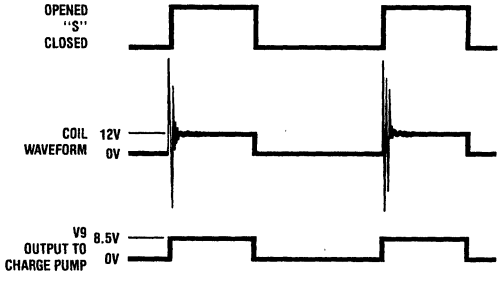
TL/H/5263–12

Typical Applications



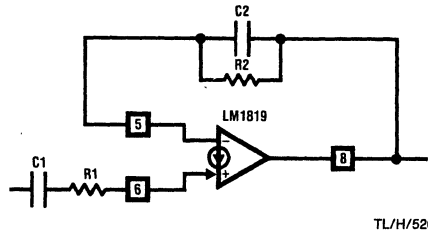
TL/H/5263–9

FIGURE 5. Typical Pulse-Squaring Circuit for Automotive Tachometers.



TL/H/5263–10

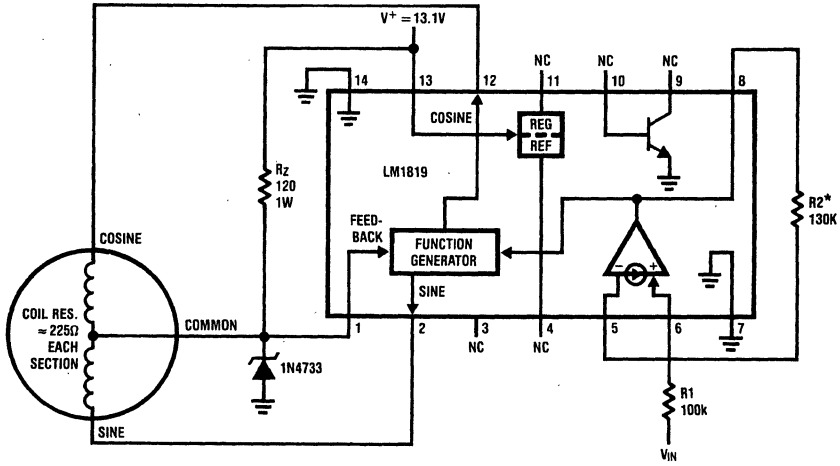
FIGURE 6. Waveforms Encountered in Automotive Tachometer Circuit.



TL/H/5263–11

FIGURE 7. Tachometer Charge Pump.

Voltage Driven Meter with Norton Amplifier Buffer



TL/H/5263–5

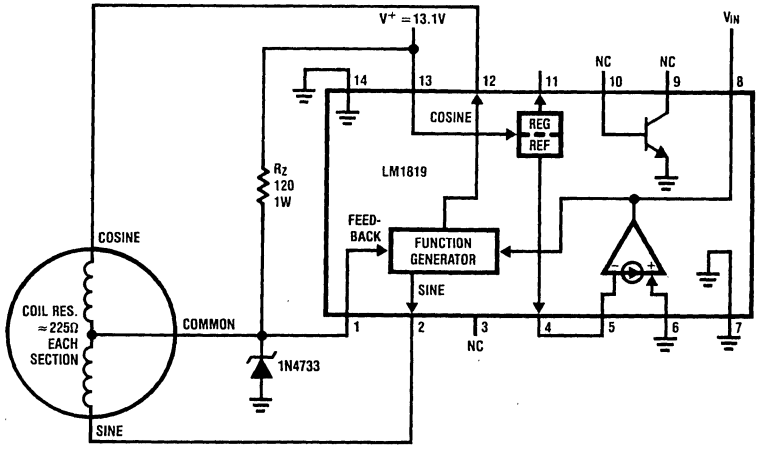
Deflection = 54 $(V_{IN} - .7)R_2/R_1$ (degrees)

0 to 305° deflection is obtained with .7 to 5V input.

*Full scale deflection is adjusted by trimming R_2.

Typical Applications (Continued)

Unbuffered Voltage Driven Meter



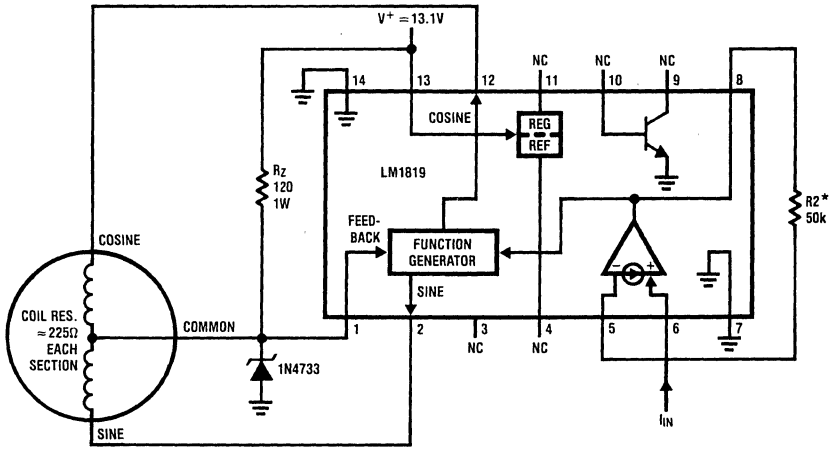
TL/H/5263–6

Deflection = $54(V_{IN} - 2.1)$ (degrees)

0 to 305° deflection is obtained for inputs of 2.1 to 7.75V.

Full scale deflection is adjusted by trimming the input voltage.

Current Driven Meter



TL/H/5263–7

Deflection = $54R_2I_{IN}$ (degrees)

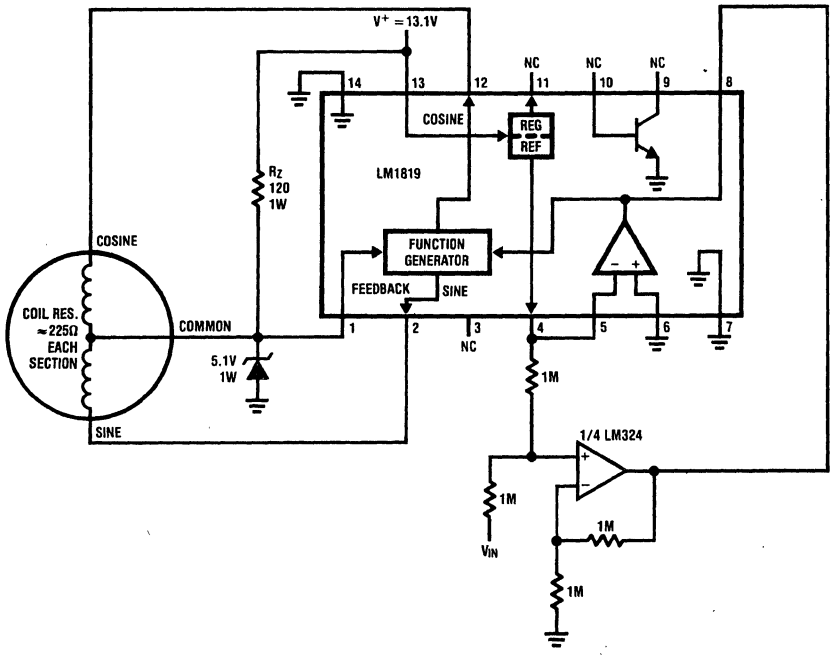
Inputs of 0 to 100 μA deflect the meter 0 to 270°.

*Full scale deflection is adjusted by trimming R_2.

S 12

Typical Applications (Continued)

Level Shifted Voltage Driven Meter



TL/H/5263–8

Deflection = $54V_{IN}$ (degrees)

Inputs of 0 to 5.65V deflect the meter through a range of 0 to 305°.

Full scale deflection is adjusted by trimming the input voltage.

National Semiconductor

LM1823 Video IF Amplifier/PLL Detector System

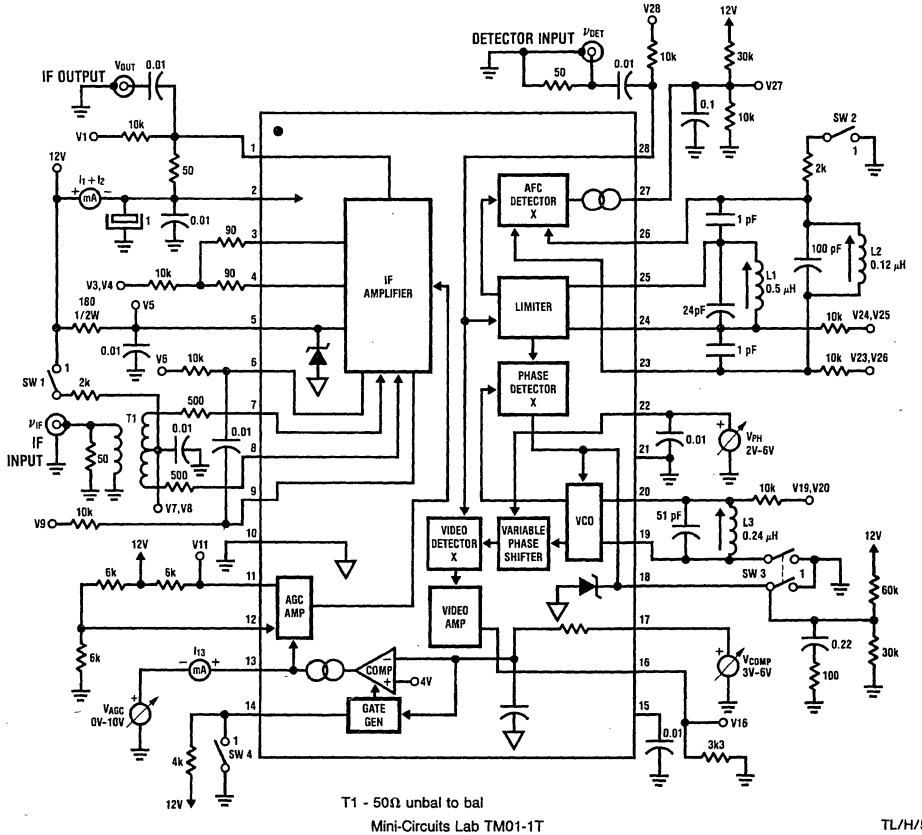
General Description

The LM1823 is a complete video IF signal processing system on a chip. It contains a 5-stage gain-controlled IF amplifier, a PLL synchronous amplitude detector, self-contained gated AGC, and a switchable AFC detector. The increased flexibility of the LM1823 makes it suitable for a wide variety of television applications where high quality video or sound carrier recovery is required. These include home receiver video IFs, cable and subscription TV decoders, and parallel sound IF/intercarrier detector systems. Typical operating frequencies are 38.9 MHz, 45.75 MHz, 58.75 MHz, and 61.25 MHz.

Features

- Low differential gain and phase
- IF and detector pin compatible with LM1822
- Common-base IF inputs for SAW filters
- True synchronous video detector using PLL
- Excellent stability at high system gains
- Noise-averaged gated AGC system
- Uncommitted AGC comparator input
- Internal AGC gate generator
- Superior small-signal detector linearity
- AFC detector with adjustable output bias
- 9 MHz video bandwidth
- Reverse tuner AGC output

Test Circuit Measure parameters at indicated test points



T1 - 50Ω unbal to bal
Mini-Circuits Lab TM01-1T

L1 - 9½T, L2 - 4½T, L3 - 6½T } #22 wire on 3/16" form with HF core, shielded

All caps in µF unless noted

TL/H/5222–1

Order Number LM1823N
See NS Package N28B

Absolute Maximum Ratings

Power Supply Voltage, V2	15V	Power Dissipation	2W
IF Supply Current, I_5	60mA	Thermal Resistance, θ_{JA}	50° C/W
AGC Gate Voltage, V14	±5V	Junction Temperature	125°C
Video Output Current, I_{16}	10 mA	Operating Temperature Range	0°C to 70°C
PLL Filter Current, I_{18}	5 mA	Storage Temperature Range	−65°C to +150°C
Detector Input Signal, ν_{DET}	1 Vrms	Lead Temp. (Soldering, 10 seconds)	265°C

DC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

$T_A = 25°C$, Test Circuit, $\nu_{IF} = \nu_{DET} = 0$, $V_{PH} = 4V$, $V_{COMP} = 4V$, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
12V Supply Current, $I_1 + I_2$	$V_{AGC} = 6.7V$. $V_{COMP} = 6V$	35	60	80	mA
IF Regulator Voltage, V5	$V_{AGC} = 6.7V$, SW4 Position 1	5.8	6.4	7.0	V
IF Input Voltage, V7, V8	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	3.2	3.7	4.1	V
IF Decouple Offset, V6–V9	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1		0	±30	mV
IF Peaker Voltage (Max Gain), V3, V4	$V_{AGC} = 2V$, SW 2, 3, 4 Position 1	2.3	3.0	3.6	V
IF Output Current, I1	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1, Measure V1, $I_1 = (12 - V1)/50$	3.1	5.5	7.8	mA
IF Peaker Voltage (Min Gain), V3, V4	$V_{AGC} = 9V$, SW 2, 3, 4 Position 1	5.5	6.2		V
Detector Input Voltage, V28	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
Limiter Tank Voltage, V24, V25	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	6.4	7.0	7.6	V
AFC Tank Voltage, V23, V26	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.3	4.9	5.5	V
VCO Tank Voltage, V19, V20	$V_{AGC} = 6.7V$, SW 1, 4 Position 1	4.7	5.2	5.7	V
AGC Sync Threshold, V17	SW 1, 2 Position 1, Adjust V_{COMP} for $I_{13} = 0$	3.8	4.0	4.2	V
AGC Filter Leakage Current, I_{13}	SW 1, 2, 4 Position 1		0	±5	μA
AGC Filter Charge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 3.5V$	1.6	2.2	2.8	mA
AGC Filter Discharge Current, I_{13}	SW 1, 2 Position 1, $V_{COMP} = 4.5V$	−0.45	−0.70	−0.90	mA
RF AGC Leakage current, I_{11}	$V_{AGC} = 2V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$		0	20	μA
RF AGC Output Current, I_{11}	$V_{AGC} = 10V$, All Switches Position 1, Measure V11, $I_{11} = (12 - V11)/6000$	1.5	1.8		mA

Detector AC Set-Up Procedure SW 1, 4 position 1, V_{AGC} = 0V

1. Apply v_{DET} = 10 mVrms, 45.75 MHz CW at the detector input. Tune L1 for maximum AC signal at pin 25, measured with a 10x FET probe or through a 1 pF capacitor to prevent loading of the limiter tank.
2. Increase v_{DET} to 60 mVrms. Adjust L3 until the PLL locks, as indicated by a DC voltage at the video output pin 16.
3. With the detector locked, adjust L3 for 4.0V at pin 18.
4. Adjust V_{PH} for maximum detector efficiency by monitoring pin 16 for a minimum DC voltage.
5. Adjust L2 for 3.0V at pin 27 (on sensitive slope of AFC curve).

AC Electrical Characteristics PARAMETERS GUARANTEED BY ELECTRICAL TESTING

T_A = 25°C, Test Circuit, detector set-up as above, f = 45.75 MHz, V_{AGC} = 6.7V, V_{COMP} = 4V, and all switches in position 0 (open) unless noted.

Parameter	Conditions	Min	Typ	Max	Units
IF Amplifier Gain, v_{OUT}/v_{IF} (Note 1)	V_{AGC} = 2V, SW 2, 3, 4 Position 1, v_{IF} = 500 μVrms	25	35		dB
V_{AGC} for 15 dB Gain Reduction	SW 2, 3, 4 Position 1, v_{IF} = 2.8 mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	4.2	4.6	5.0	V
V_{AGC} for 45 dB Gain Reduction	SW 2, 3, 4 Position 1, v_{IF} = 89 mVrms, Adjust V_{AGC} for Same v_{OUT} as Gain Test	5.1	5.5	6.1	V
Zero Carrier Level, V16	SW 1, 2, 4 Position 1, v_{DET} = 0	6.8	7.6	8.4	V
Detected Output Level, ΔV16	SW 1, 2, 4 Position 1, v_{DET} = 60 m/Vrms, Measure Change in V16 from Zero Carrier Test	2	3	4	V
Overload Output Voltage, V16	SW 1, 2, 4 Position 1, v_{DET} = 600 mVrms		2	3	V
AFC Output Voltage (OFF), V27	SW 1, 2, 4 Position 1, v_{DET} = 0	2.8	3.0	3.2	V
AFC Minimum Output Voltage, V27	SW 1, 4 Position 1, v_{DET} = 60 mVrms, 46.75 MHz		0.5	1.0	V
AFC Maximum Output Voltage, V27	SW 1, 4 Position 1, v_{DET} = 60 mVrms, 44.75 MHz	9	10		V
PLL Pull-In Range, Δf	SW 1, 4 Position 1, v_{DET} = 60 mVrms, Vary Frequency and Measure the Difference between Lock Points	2	3		MHz

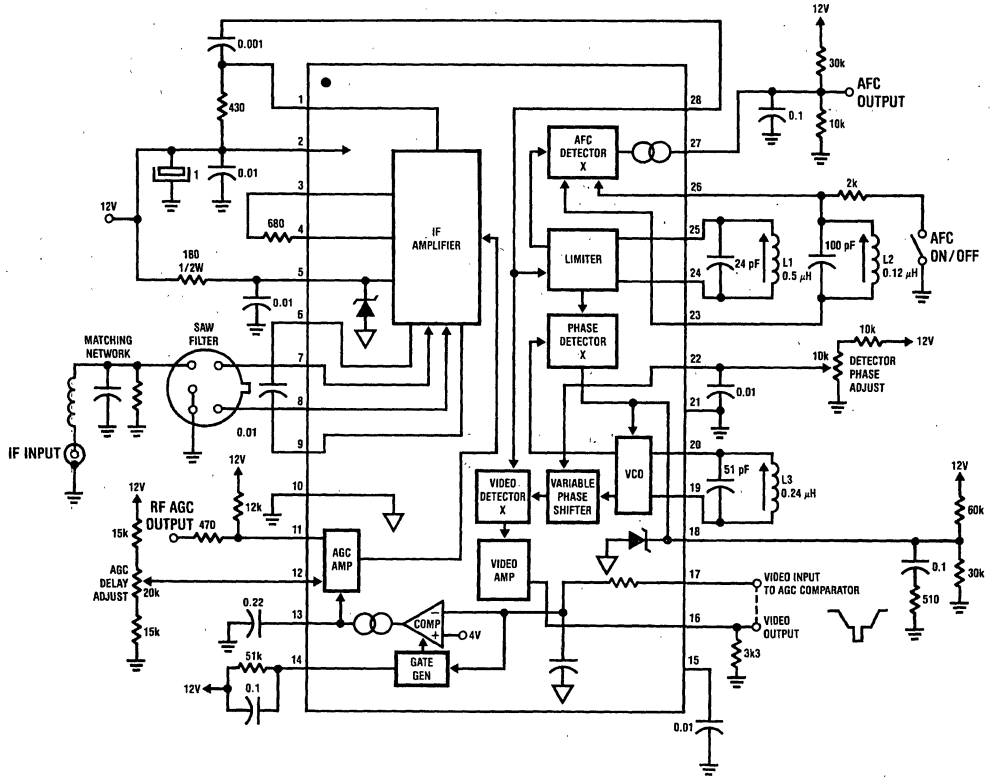
Note 1: The IF amplifier gain is specified with the IF output connected to a 50Ω measurement system which results in a 25Ω loaded impedance. The gain in an actual application will typically be 26 dB higher.

Design Parameters NOT TESTED OR GUARANTEED Typical Application Circuit

Parameter	Typ	Units
Maximum System Operating Frequency	70	MHz
IF Input Impedance (Differential Pin 7–8), 45 MHz	60	Ω
IF Output Impedance, 45 MHz	10	kΩ
IF Gain Control Range	55	dB
Detector Input Impedance, 45 MHz	3	kΩ
Detector Output Bandwidth, −3 dB	9	MHz
Detector Differential Gain (Note 2)	2	%
Detector Differential Phase (Note 2)	1	deg
Detector Output Harmonic Levels below 3 Vp-p Video	−40	dB
VCO Temperature Coefficient	−150	ppm/°C

Note: 2: Differential gain and phase measured with the limiter tank adjusted for minimum differential phase.

Typical Application 45.75 MHz (see Application Notes)



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SAW Filter - MuRata SAF45MC/MA

L1 - 9½T
L2 - 4½T
L3 - 6½T
} #22 wire on 3.16" form with HF core, shielded

All caps in µF unless noted

Application Notes Refer to Typical Application Circuit

COMMENTS ON RF Coupling

The LM1823 is a high gain RF system which is critically dependent on the ground plane and positioning of the external components. For this reason, it is suggested that the printed circuit layout shown in *Figure 3* be strictly adhered to.

The most sensitive points in the system to unwanted RF coupling are the IF input pins 6–9. There are two different signals which can cause different problems when coupling into the IF inputs. If the IF output is coupling to the input, it can cause bandpass tilting, peaking, and in extreme cases, oscillation. The other signal which can couple to the IF inputs is the PLL detector VCO. This VCO coupling can cause AFC skewing, non-symmetrical detector pull-in, and failure of the detector to acquire lock at weak signal levels. These input coupling problems will be most acute at maximum gain and will decrease as the IF is gain reduced by AGC action.

The differential IF inputs offer a large amount of inherent rejection to unwanted RF coupling. Therefore, A FULLY BALANCED INPUT SOURCE IS MANDATORY. The input leads must be routed together and socketless operation is recommended above 50 MHz. However, residual coupling may still dictate the maximum IF amplifier gain which can be taken (see Pin Descriptions).

PIN DESCRIPTIONS

Pin 1-IF Amplifier Output: Pin 1 is connected to an open-collector NPN device. The load on pin 1 must be returned to the 12V supply as close as possible to pin 2. The IF output load may be either resistive as shown in the Typical Application, or an LC tank. The tank need only be used if a tunable bandpass characteristic is desired, or in conjunction with a sound trap.

Pin 2–12V Supply: The LM1823 requires a nominal 12V supply but can accept a ±10% variation. Pin 2 must be RF decoupled to a good ground as close as possible to the IC.

Pins 3, 4-IF Gain Adjustment: Pins 3 and 4 are connected to the two emitters of the 4th IF differential amplifier such that the gain of the stage is set by the impedance between the pins. There is an internal 1360Ω resistor to set the minimum gain when the pins are left open. Adding an external resistor increases the gain by the ratio of the parallel impedance to the original 1360Ω. The pin 3 to 4 external resistor primarily affects the maximum IF gain; the relative gain increase goes away over the first 20 dB of AGC.

Pin 5-IF Supply: The IF supply employs an internal 6.4V shunt regulator which is fed by an external dropping resistor from pin 2 to pin 5. RF decoupling from pin 5 to the pin 10 ground plane is critical.

Pins 6–9-IF Input and Decouple Pins: The LM1823 uses a common-base differential input stage as shown in *Figure 1*. Pins 7 and 8 connect directly to the emitters of the input devices, while pins 6 and 9 decouple the DC feedback loop at the bases.

The gain of a common-base amplifier depends inversely on the source impedance. The LM1823 is designed to operate from differential impedances in the 500Ω to 2000Ω range, which is typical for surface acoustic wave (SAW) filters. Alternatively, the IF may be used with a transformer input configuration similar to that shown in the Test Circuit, as long as the required source impedance is maintained. In all cases a balanced source must be used.

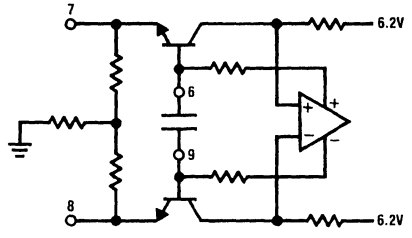

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FIGURE 1. IF Input Stage

Both the input network to pins 7 and 8 and decoupling capacitor between pin 6 and pin 9 must be as close to the device as is physically possible to minimize RF coupling.

Pin 10-IF Ground: Pin 10 grounds the IF and AGC circuits in the LM1823. It is separate from the detector and chip substrate grounds to prevent internal coupling.

Pin 11-RF AGC Output: Pin 11 is connected to an open-collector NPN device. It begins to conduct current when the voltage on the AGC filter capacitor at pin 13 exceeds the voltage set at the takeover pin 12 by approximately 0.6V. When connected to a resistor to 12V, this produces a falling voltage at pin 11 suitable for reverse tuner AGC inputs.

Pin 12-RF AGC Takeover Adjust: The voltage preset at pin 12 determines when the IF stops gain reducing and the tuner begins gain reducing as the pin 13 AGC filter capacitor voltage increases with signal level. A higher voltage at pin 12 delays the RF AGC takeover until more IF gain reduction has been taken (higher signal levels), while a lower voltage limits the IF gain reduction before RF takeover.

When the LM1823 is being used without a tuner, pin 12 may be connected to supply.

Pin 13-AGC Filter: Pin 13 is a push-pull current source output from the AGC comparator. The comparator compares the negative sync tips of noise-averaged pin 17 video with an internal 4V reference. Increases in signal produce a current out of pin 13 which charges the filter capacitor, while decreases discharge the capacitor. The resulting change in voltage at pin 13 controls the IF and tuner gains to maintain the pin 17 sync tip level at 4V. An optional capacitor between pin 13 and the takeover pin 12 couples the ripple produced by a rapidly varying signal into the takeover pin to enhance the AGC loop response.

Pin 14-AGC Gate Generator Time Constant: The AGC comparator is gated on during sync time by a pulse from an internal gate generator. The gate pulse which activates the comparator is derived from the sync pulse in the same video which feeds the comparator input (see pin 17 description). An RC time constant on pin 14 determines the slice level on the leading edge of the sync pulse at which the comparator is gated on. This level is approximately $V_{SLICE} = 1/(2RC)$ in millivolts above the sync tip, and should be set at ≤25% of the sync amplitude. Note that V_{SLICE} only determines when the AGC comparator turns on, and is unrelated to the comparator reference.

In the Typical Application, $V_{SLICE} = 100$ mV, or 10% of a 1V sync pulse. Increasing V_{SLICE} improves the AGC recovery from step changes in signal level but increases the risk of video interaction. When modifying the time constant, change the capacitor value only.

Application Notes (Continued) Refer to Typical Application Circuit

Pin 15-Supply Decouple: Pin 15 is an additional connection to the 12V supply to allow RF decoupling on the detector side of the chip.

Pin 16-Video Output: Pin 16 is a Darlington NPN emitter-follower output supplying negative sync video. With no detector input signal the pin 16 voltage sits at the zero carrier level, representing peak white. As the input signal level increases, the pin 16 voltage decreases towards black. The sync pulses are normally the most negative portion of the recovered video.

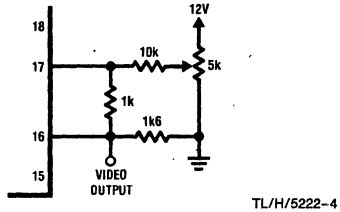

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FIGURE 2. Adjustable Recovered Video Level

Pin 17-AGC Comparator Input: External negative sync video is fed to the AGC comparator and gate generator via pin 17. An internal low pass filter removes high frequency noise and transients. The peak-to-peak video level with the AGC loop active is determined by the difference between the zero carrier level at pin 17 and the 4V sync tip level being held by the AGC comparator (see pin 13 description).

When the LM1823 is being used to recover normal video, pin 17 may simply be returned to pin 16. This results in a nominal 3 Vp-p video level, but which is subject to variations in the pin 16 zero carrier level. The network shown in *Figure 2* can be used to change the zero carrier at pin 17, thus providing an adjustable recovered video level. The pin 16 video level should be maintained at between 1 Vp-p minimum and 4 Vp-p maximum.

In suppressed sync systems, the recovered video at pin 16 may require processing to restore normal sync amplitude before being fed to pin 17. In this case, it is mandatory that a DC path be maintained for the zero carrier level through any external circuitry. Any DC level shift between pins 16 and 17 will have the effect of changing the video level as previously described.

Pin 18-PLL Filter: Pin 18 is connected to both the output of the phase detector and the control input of the VCO. The polarity of the VCO control characteristic is such that increasing the pin 18 voltage increases the VCO frequency. An external resistive divider at pin 18 serves two functions. The divider parallel impedance sets the gain of the phase detector, while the divider ratio places the quiescent voltage at the center of the VCO control characteristic. The 20 kΩ impedance, ⅓ supply divider shown in the Typical Application has been chosen to provide optimum performance. The series capacitor and resistor to ground complete the PLL filter.

An internal zener clamp to ground at pin 18 prevents the phase detector output from pulling the VCO control input over 5.6V. For this reason, external voltages should not be forced at pin 18 to avoid damaging the clamp.

Pins 19, 20-VCO Tank: A parallel LC tank between pins 19 and 20 sets the VCO center frequency. The tank Q is RpL/Xc, where RpL is the coil Rp loaded by an internal 1500Ω resistor. Increasing the Q (larger C) improves stability but reduces the VCO control range. The tank shown in the Typical Application will yield a loaded Q of around 15, providing stable operation with a control range in excess of 2 MHz.

Pin 21-Substrate Ground: Pin 21 grounds the chip substrate along with all of the AFC and PLL detector grounds.

Pin 22-Detector Phase Adjust: The video detector requires a reference signal in phase with the input signal carrier for maximum detection efficiency. However, the action of the PLL inherently sets the VCO phase in quadrature (at 90 degrees) with the limiter output. Therefore a variable phase shift network, controlled by pin 22, is used internally between the VCO and video detector to insure proper phasing. Pin 22 requires an adjustment voltage centered at ⅓ supply with ±2V of control range.

The pin 22 adjustment procedure described in the Detector AC Set-Up Procedure is an open loop approach where the voltage is adjusted for maximum detected output with a fixed detector input signal. In the Typical Application, with the detector input being fed from the IF amplifier and the AGC loop active, the pin 22 adjustment is made by maximizing the AGC filter voltage at pin 13. In all cases the detector phase adjustment must be performed after the limiter is tuned.

Pins 23, 26-AFC Tank: A parallel LC tank between pins 23 and 26 sets the center of the AFC characteristic. The internal resistance is typically 20 kΩ, so that Q will be dominated by the coil Rp. The L/C ratio shown in the Typical Application maximizes Q to provide a steep AFC output slope.

A quadrature input signal is required at the AFC tank to operate the AFC detector. This signal is derived by light capacitive coupling from the limiter tank. For applications at 45 MHz and above, the stray printed circuit capacitance from the adjacent limiter tank couples sufficient signal for proper operation. However, at lower IF frequencies, small (1 pF–5 pF) capacitors may be required between the adjacent pins as shown in the Test Circuit.

A second function of pins 23 and 26 allows turning the AFC detector OFF by grounding either side of the AFC tank. Up to 2 kΩ may be placed in series with the switch connection to prevent unbalancing the tank.

Pins 24, 25-Limiter Tank: A parallel LC tank between pins 24 and 25 forms the tuned load for a single stage limiting amplifier which strips amplitude information from the signals feeding the AFC and phase detectors. The amplifier has a small signal gain of approximately 50, with internal Schottky diodes across the tank to limit the output amplitude to 500 mVp-p.

The linearity of the detector video outputs depends directly on limiter tuning. Making the limiter adjustment based on maximum signal level at pins 24, 25 as outlined in the Detector AC Set-Up Procedure results in nearly optimum output linearity. However, to completely null the output differential phase the limiter should be adjusted while monitoring this parameter.

Pin 27-AFC Detector Output: Pin 27 is push-pull current source output from the AFC detector. The polarity is such that pin 27 sources current when the input signal is below the center frequency, and sinks current above the center frequency. An external resistive divider sets both the gain and quiescent output voltage of the AFC. Although the net-

Application Notes (Continued) Refer to Typical Application Circuit

work shown in the Typical Application sets up the output at ¼ supply, it could easily be changed to ½ supply by using equal-valued resistors. When setting up the AFC detector, the tank should always be tuned so the output is at the quiescent divider voltage with the desired center frequency applied.

Pin 28-Detector Input: Pin 28 is internally DC-biased and requires an AC-coupled input signal. The network between pins 1 and 28 should not allow over 1 Vrms at the input during signal transients to prevent overloading the detector. When a tank is being used for the IF output load, a capacitive divider may be used from pin 1 to pin 28 in which the series equivalent capacitance resonates with the coil.

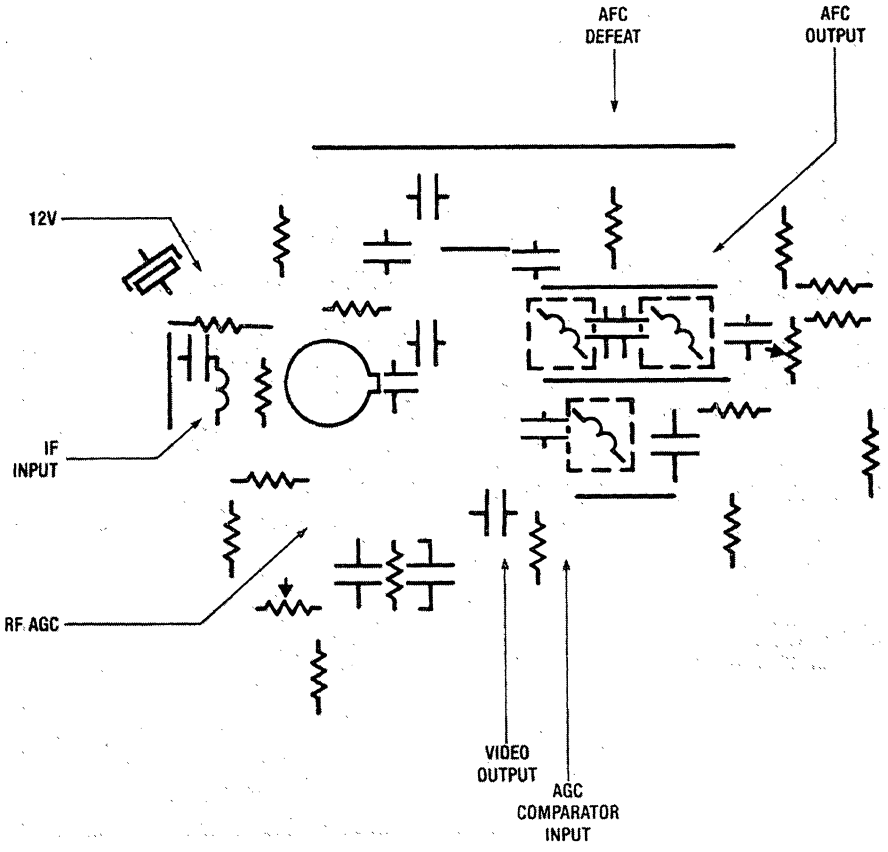

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FIGURE 3. Printed Circuit Layout (Component Side).

National Semiconductor

PRELIMINARY

LM1863 AM Radio System for Electronically Tuned Radios

General Description

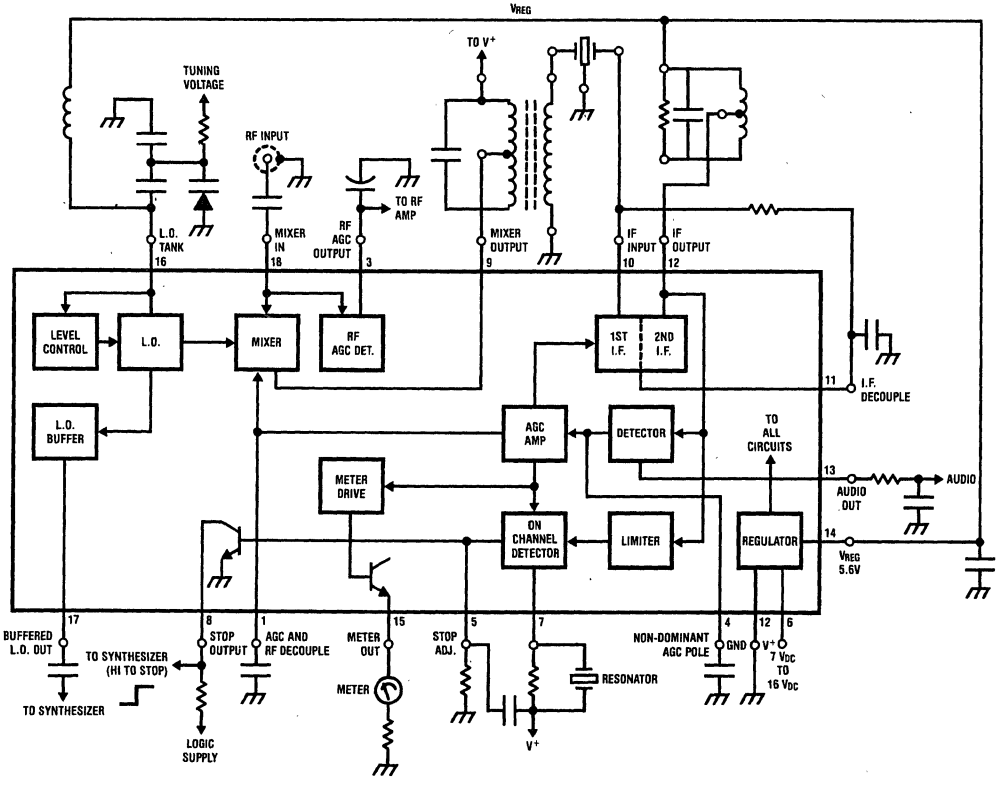
The LM1863 is a high performance AM radio system intended primarily for electronically tuned radios. Important to this application is an on-chip stop detector circuit which allows for a user adjustable signal level threshold and center frequency stop window. The IC uses a low phase noise, level-controlled local oscillator.

Low phase noise is important for AM stereo which detects phase noise as noise in the L-R channel. A buffered output for the local oscillator allows the IC to directly drive a phase locked loop synthesizer. The IC uses a RF AGC detector to gain reduce an external RF stage thereby preventing overload by strong signals. An improved noise floor and lower THD are achieved through gain reduction of the IF stage. Fast AGC settling time, which is important for accurate stop detection, and excellent THD performance are achieved with the use of a two pole AGC system. Low tweet radiation and sufficient gain are provided to allow the IC to also be used in conjunction with a loopstick antenna.

Features

- Low supply current
- Level-controlled, low phase noise local oscillator
- Buffered local oscillator output
- Stop circuitry with adjustable stop threshold and adjustable stop window
- Open collector stop output
- Excellent THD and stop time performance
- Large amount of recovered audio
- RF AGC with open collector output
- Meter output
- Compatible with AM stereo

Block Diagram



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Order Number LM1863N
See NS Package Number N18A

Absolute Maximum Ratings

Supply Voltage	16V	Operating Temperature Range	0°C to +70°C
Package Dissipation (Note 1)	1.89W	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−55°C to +150°C		

Electrical Characteristics

(Test Circuit, T_A = 25°C, V+ = 12V, SW1 = Position 1, SW2 = Position 2, unless indicated otherwise)

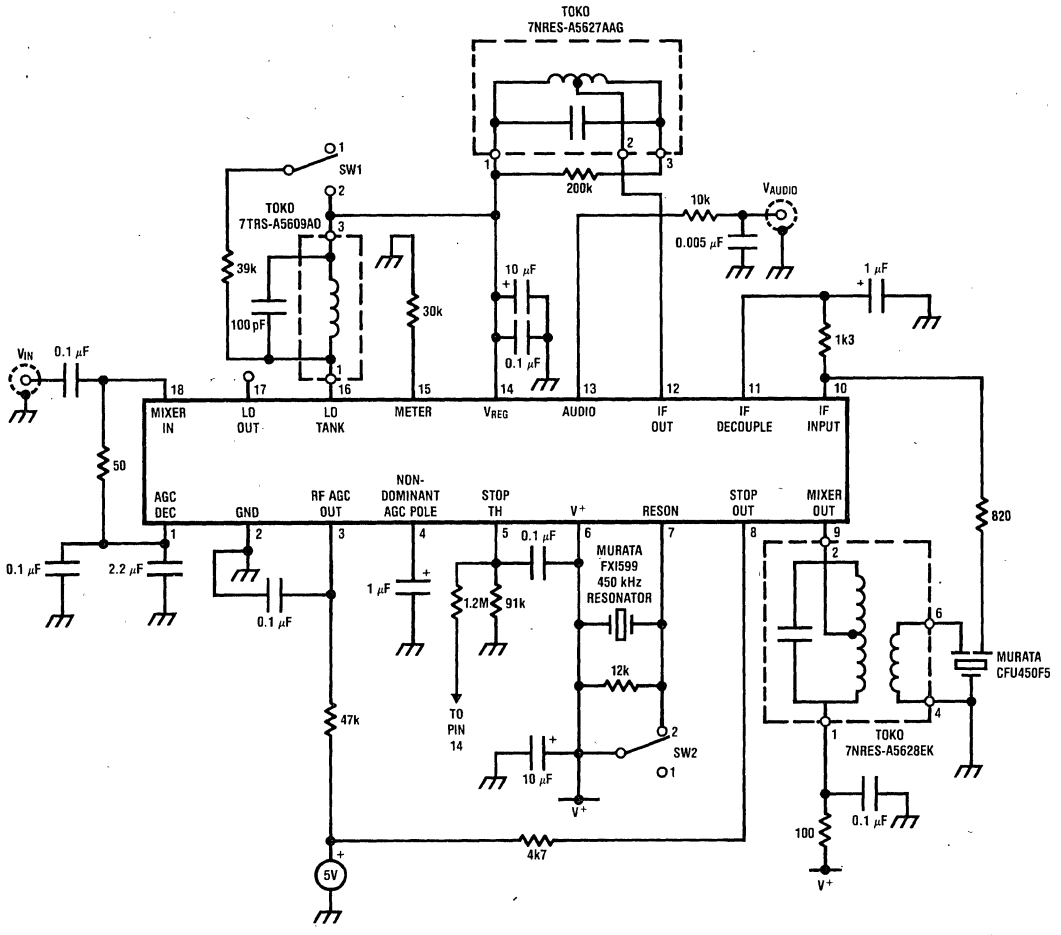
Parameter	Conditions	Min	Typ	Max	Units
STATIC CHARACTERISTICS					
Supply Current	V_{IN} = 0 mV		8.3	10	mA
Pin 14, Regulator Voltage			5.6		V
Operating Voltage Range	(See Note 2)	7		16	V
Pin 3 Leakage Current	V_{IN} = 0 mV		0.1		μA
Pin 8, Low Output Voltage	V_{IN} = 0 mV		.15		V
Pin 15, Output Voltage	V_{IN} = 0 mV		0		V
DYNAMIC CHARACTERISTICS: (f_{MOD} = 1 kHz, f_{IN} = 1 MHz, M = 0.3)					
Maximum Sensitivity	V_{IN} For V_{AUDIO} = 6 mVrms		7.5		μV
20 dB Quieting Sensitivity	V_{IN} for 20 dB S/N in Audio		15	30	μV
Maximum Signal to Noise Ratio	V_{IN} = 10 mV	40	54		dB
Total Harmonic Distortion	V_{IN} = 10 mV		.26		%
Total Harmonic Distortion	V_{IN} = 10 mV, M = 0.8		.63	2	%
Audio Output Level	V_{IN} = 10 mV	80	120	160	mVrms
Overload Distortion	V_{IN} = 50 mV, M = 0.8		7.5		%
Meter Output Voltage	V_{IN} = 100 μV		0.5		V
Meter Output Voltage	V_{IN} = 10 mV		4.6		V
Local Oscillator Output Level on Pin 17	(See Note 3), SW1 = Position 1	100	147		mVrms
Local Oscillator Output Level on Pin 17	(See Note 3), SW1 = Position 2		125		mVrms
Stop Detector Valid Station Frequency Window	V_{IN} = 10 mV, difference between the two frequencies at which Pin 8 < 1V, SW2 = Position 1	2.5	4	5.5	kHz
Stop Detector Valid Station Signal Level Threshold	Find V_{IN} for which Pin 8 > 1V	7	16	40	μVrms
RF AGC Threshold	Find V_{IN} that produces 10 μA of current into Pin 3	3	6	10	mVrms
Pin 3 Low Output Level	V_{IN} = 30 mV		0.1		V
Pin 8 Leakage Current	V_{IN} = 30 mV		0.1		μA
Pin 15 Output Resistance	V_{IN} = 10 mV		825		Ω

Note 1: Above T_A = 25°C derate based on $T_{j\,(MAX)}$ = 150°C and θ_{jA} = 66°C/W.

Note 2: All data sheet specifications are for V+ = 12V and may change slightly with supply.

Note 3: The local oscillator level at Pin 17 is identical to the level at Pin 16 since Pin 17 is an emitter follower off of Pin 16.

Test Circuit



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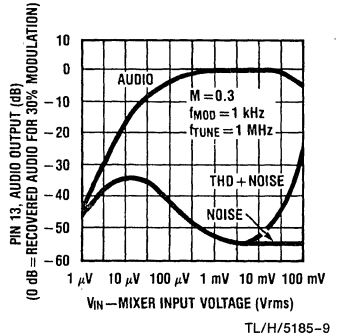
Typical Performance Characteristics (From Test Circuit)



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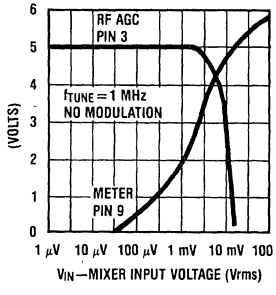

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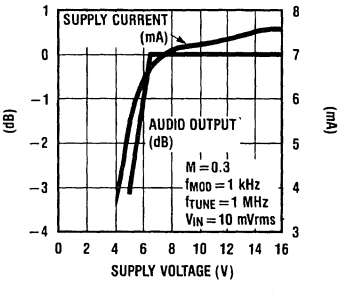
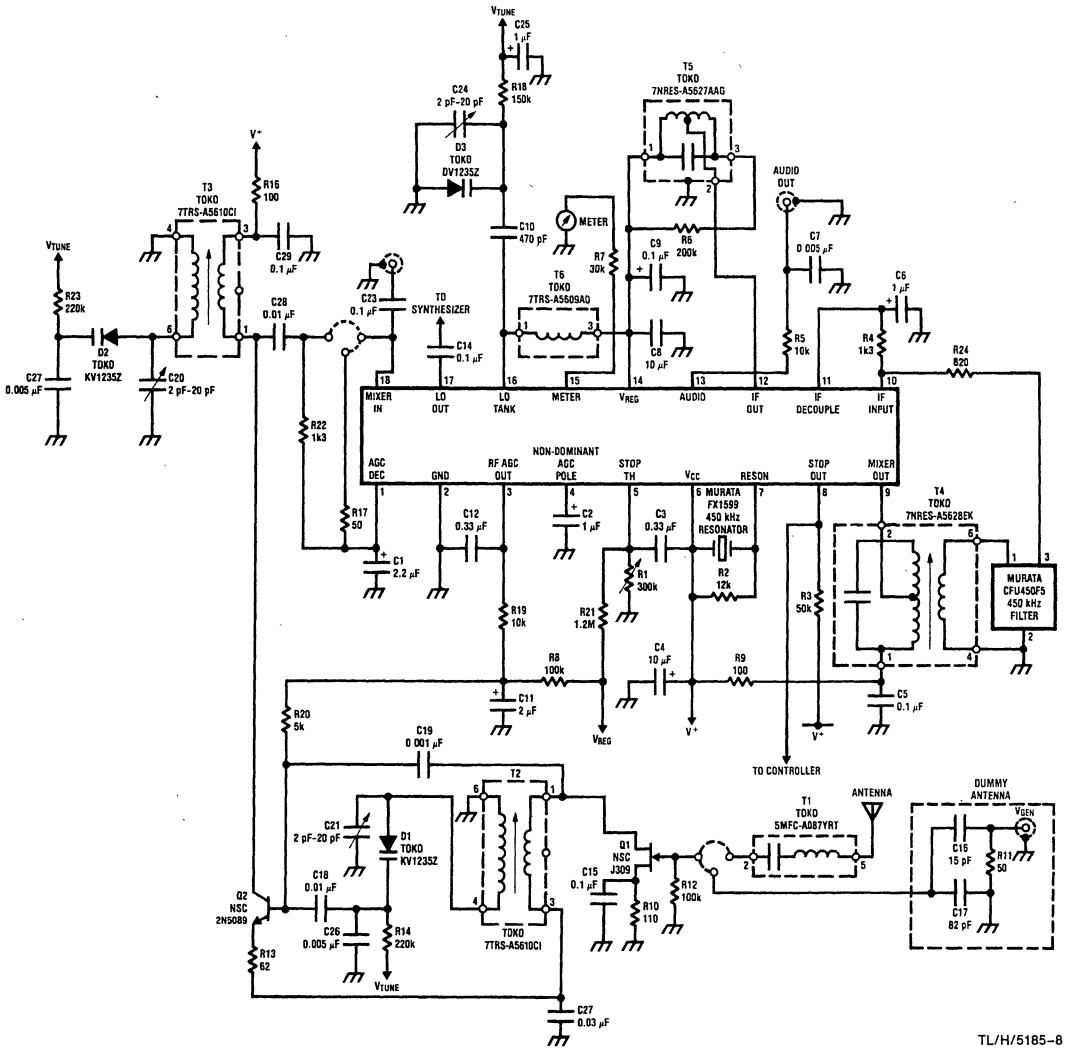


TL/H/5185-11

LM1863: AM ETR Radio



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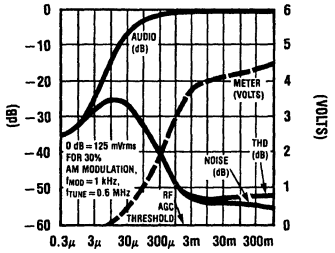
Performance Characteristics of Applications Circuit



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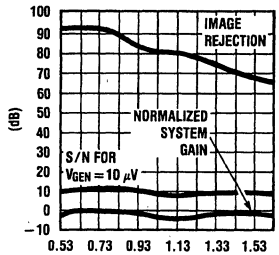

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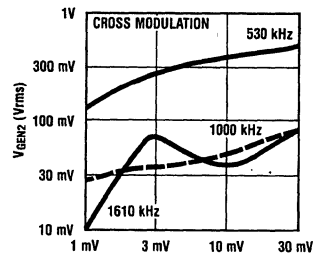
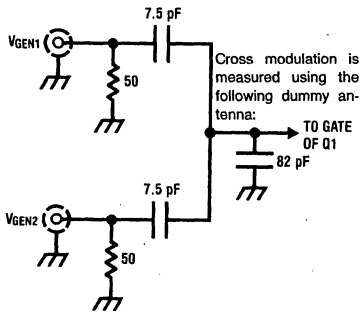


TL/H/5185–14



TL/H/5185–15

The following procedure was used to measure cross modulation:

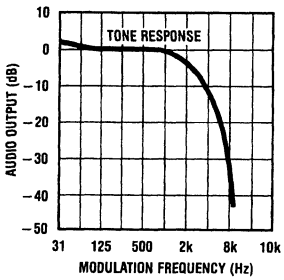
1. Tune the radio to the center frequency of interest and tune V_{GEN}, to this same frequency.

2. Set at 0 dB audio reference with V_{GEN}, = 10 mV RMS and 30% AM mod; f_{MOD} = 1 kHz.

3. Remove the modulation from V_{GEN1} and set the level of V_{GEN1}.

4. Set the modulation level of V_{GEN2} = 80% at f_{MOD} = 1 kHz and tune V_{GEN2} ± 40 kHz away from center frequency.

5. Increase the level of V_{GEN2} until −40 dB of audio is recovered. The level of V_{GEN2} is the cross modulation measurement.



TL/H/5185–16

Additional Performance Information:

* THD for 80% modulation for f_{MOD} = 1 kHZ at:
  V_{GEN} = 1V is 0.5%
  V_{GEN} = 10 mV is 0.4%
* Tweet <2% at all input levels.
* Typical time for valid stop indication < 50 ms.

Note: Tweet is an audio tone produced by the 2nd and 3rd harmonic of the IF beating against the received signal. It is measured as an equivalent modulation level: ie, 30% tweet has the same amplitude at the detector as a desired signal with 30% modulation.

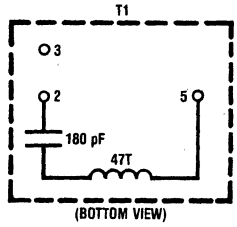
IC External Components (See Application Circuit)

Component	Typical Value	Comments
C1	2.2 μF	Sets dominant AGC pole, affects stop time and THD.
C2	1 μF	Sets non-dominant AGC pole, affects stop time and THD.
C3	0.33 μF	Stop level threshold decoupling, affects stop time and sensitivity of stop detector to large modulation peaks.
C4	10 μF	Supply decoupling, low frequency.
C5	0.1 μF	Supply decoupling, high frequency.
C6	1 μF	IF decouple, affects IF gain.
C7	0.005 μF	Audio output filter, removes IF ripple from detector.
C8	10 μF	Regulator decouple, low frequency.
C9	0.1 μF	Regulator decouple, high frequency.
C10	470 pF	Pad capacitor for varactor, affects tracking.
C11	2 μF	RF AGC decouple, affects stop time and THD.
C12	0.33 μF	RF AGC high frequency decouple.
C14	0.1 μF	Local oscillator output coupling.
C19	0.001 μF	Sets gain at high end of AM band.
C26	0.005 μF	Sets gain at low end of AM band.
C28	0.01 μF	Couples RF stage output to mixer input, keep small to insure proper stop time performance when RF AGC is active.
R1	300k Pot.	Sets level stop threshold.
R2	12k	Sets size of stop window.
R3	50k	Open collector pull up resistor.
R4	1k3	IF filter termination, and gain set.
R5	10k	Sets RC time constant on audio outputs, smaller values may cause distortion of high frequencies.
R6	200k	Sets gain of IF stage, affects noise floor and sensitivity.
R7	Meter Dependent	Sets full-scale deflection of meter.
R8	100k	Sets gain and threshold of RF AGC.
R9	100Ω	Aids mixer output decoupling.
R19	10k	Sets 2'nd pole in RF AGC, affects THD for large input signals.
R21	1.2 MΩ	Biases pin 5 to 0.4 volts which permits shorter stop time.
R24	820Ω	Sets system gain.
D1, D2, D3,	TOKO KV1235Z or Equivalent	Varactor diodes.
Resonator	450 kHz ± 1 kHz Murata*, FX1599	Parallel type resonator.
IF filter	Murata* CFU450F5	Sets selectivity and tone response.

*Murata Corporation of America
1148 Franklin Rd. S. E.
Marietta, GA, 30067, U.S.A.
404-952-9777

Performance Characteristics of Applications Circuit (Continued)

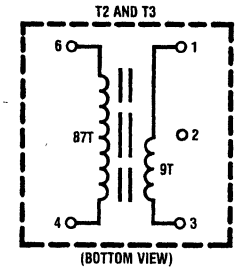
Part No. 5MFC-A087YRT
TOKO Electronics Ltd.*



TL/H/5185-17

Center Frequency = 2 MHz
Qu > 50 at 2 MHz

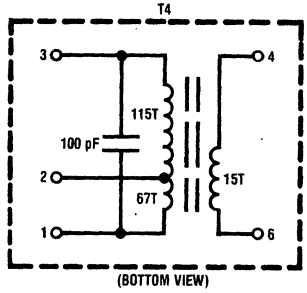
Part No. 7TRS-A5610CI
TOKO Electronics Ltd.



TL/H/5185-18

Qu > 95 at 1 MHz
L_{4-6} = 200 μH

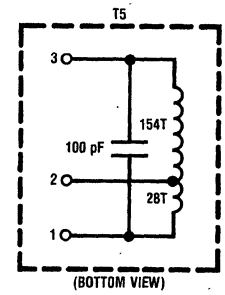
Part No. 7NRES-A5628EK
TOKO Electronics Ltd.



TL/H/5185-19

Center Frequency = 450 kHz
Qu > 100 at 450 kHz

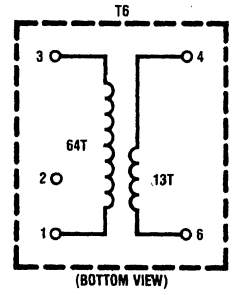
Part No. 7NRES-A5627AAG
TOKO Electronics Ltd.



TL/H/5185-20

Center Frequency = 450 kHz
Qu > 100 at 450 kHz

Part No. 7TRS-A5609A0
TOKO Electronics Ltd.



TL/H/5185-21

Center Frequency = 1 MHz
Qu > 95 at 1 MHz
L_{1-3} = 110 μH

*Toko America Inc.
5520 West Touhy Ave.
Skokie, Illinois, 60077, U.S.A.
312-677-3640

Layout Considerations

Although the pinout of the LM1863 has been chosen to minimize layout problems, some care is required to insure proper performance. If the LM1863 is used with a loopstick antenna, care in the placement of C3 must be observed in order to minimize tweet radiation. Orient C3 parallel to the axis of the loopstick and as far away as possible. Keep C3 close to the IC. The ground on C6 should be located near the ground terminal of the 450 kHz ceramic filter. C11 should be located near Q2 and C12 should be located near the IC. Also, the resonator on Pin 7 and resistor R2 should be located near the IC in order to minimize tweet radiation.

The mixer output, Pin 9 and the IF input, Pin 10, traces should be as short as possible to prevent stray pick up from the resonator.

Applications Information

(See typical application and LM1863 schematic diagram.)

STOP DETECTOR

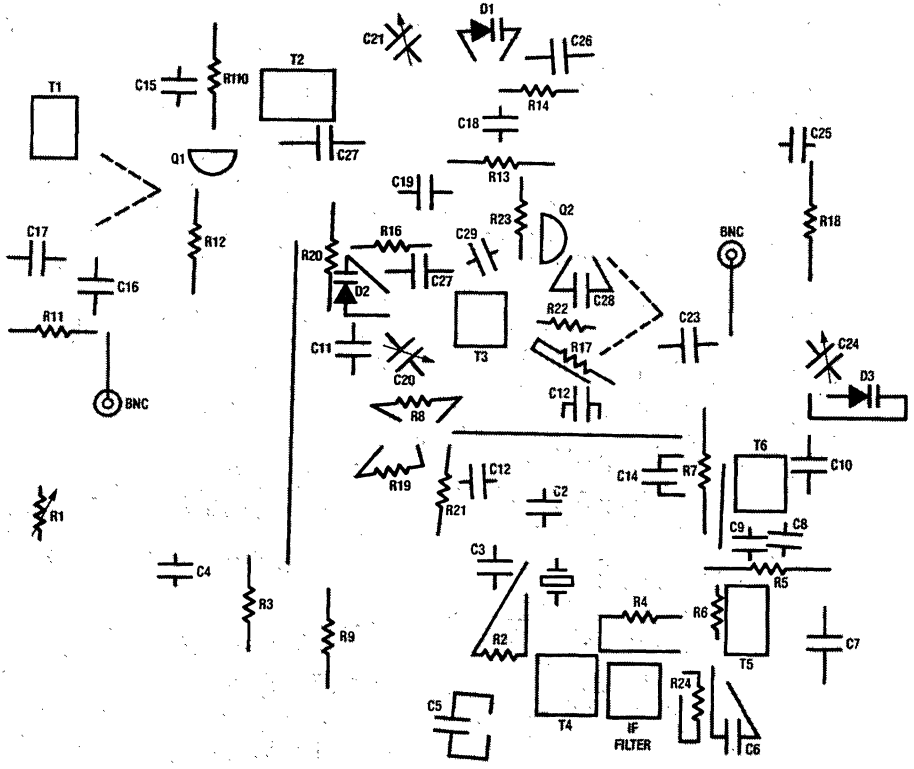
There are two criteria that determine when an electronically tuned radio is tuned to a valid station. The first criterion is that the incoming signal be of sufficient strength to be listenable. The second criterion requires that the radio be tuned to the center frequency of the incoming station. Both the signal strength threshold and the center tune window are externally adjustable.

The signal strength threshold is set by resistor R1. Increasing the value of this resistor will reduce the signal level threshold. There is no difficulty in setting the signal strength threshold, either above or below the AGC threshold.

Resistor R2 sets the center tune window. The incoming station is considered to be center tuned whenever the frequency of the signal at the IF output falls within the center tune window. Increasing the value of R2 will narrow the window, while decreasing R2 will widen the window. Since there is some interaction between R2 and R1, R2 should be chosen before R1. In the United States, stations within the AM band are spaced no closer than 10 kHz apart. Consequently, the controller should be set up to stop every 10 kHz within the AM band when the ETR is in scan mode. A center tune window anywhere less than ±10 kHz is therefore adequate in determining the center tune condition, though a narrower stop window is desirable in order to minimize the chance that side bands from a strong adjacent channel will fall within the stop window.

Because of asymmetry in the resonator amplitude characteristic, the center tune stop window will not be symmetric

PC Layout (Component Side)



TL/H/5185–22

Applications Information (Continued)

about the center frequency of the resonator. This is not a problem as long as the stop window brackets the center frequency of the IF and does not extend into the next channel. However, in order to avoid any problems in this regard it is recommended that the resonator center frequency deviate no more than ±1 kHz from the center frequency of the IF.

The stop output, Pin 8, is an open collector NPN transistor. This output must be taken to a positive voltage through a load resistor, R3. A valid stop condition is indicated by a high output level on Pin 8 (i.e., the NPN is turned off). The voltage on this pin should not exceed 16 volts.

STOP DETECTOR STOP TIME

The amount of time required for the LM1863 to output an accurate stop indication on Pin 8 is defined as the stop time. The stop time determines how quickly the ETR can scan across the AM band. There are several factors that influence the stop time. Since the signal level stop function operates in conjunction with the Automatic Gain Control (AGC), the AGC settling time is a critical factor. This settling time is dominated by the low frequency AGC pole which is set by C1 and internal IC resistances. Decreasing C1 will decrease the AGC settling time but increase total harmonic distortion, THD, of the recovered audio. A good compromise between AGC settling time and THD is very difficult to reach with a single pole AGC system. Consequently, the LM1863 has been designed with a second, higher frequency, AGC pole. This non-dominant pole is externally set by capacitor C2. As a result, C1 can be made much smaller than it otherwise could for an equivalent amount of THD. Reducing C1 will reduce the stop time. The combination of C1 and C2 as shown in the applications circuit results in a stop time of less than 50 ms for most input conditions, while at the same time the circuit achieves .9% THD at 80% modulation with 400 Hz modulation frequency at 10 mV input signal strength. Had C2 not been present the stop time would still be 50 ms but the THD for similar input conditions would be 8%. By decreasing both C1 and C2 (keeping the ratio of C1/C2 constant) the stop time can be reduced at the expense of THD, while the converse is also true.

The addition of a second pole to the AGC response does add some ringing to the AGC voltage following signal transients. The frequency, duration and amount of ringing are dependent on where both AGC poles are placed and to some extent the input signal conditions. The amount of ringing should be kept to a minimum in order to insure proper stop indications. The amount of ringing can be reduced by either reducing C2 (this will increase THD) or by increasing C1 (this will improve THD but increase stop time).

If the ratio of C1/C2 is made too small, an increase in low frequency noise may be noticed resulting from the peaking that a closed loop two pole system exhibits near the unity gain frequency. The extent of this peaking can be observed by examining the amount of recovered audio at various low frequency modulations. In general, the values shown reach a good compromise between THD, stop time, ringing and low frequency noise.

The center tuning detector on the LM1863 passes the signal at the IF output through a limiting amplifier which removes most of the modulation from the IF waveform. The output of this limiter is then applied to the resonator on Pin 7. Unfortunately, large modulation peaks are not completely removed by the limiting amplifier. Without C3, these large modulation peaks would cause glitches on the stop output when the LM1863 was tuned to a valid station. C3 acts to reduce these glitches by filtering the output of the center tune circuit. C3, however, also affects the stop time and cannot be made arbitrarily large. A time constant of about 30 ms on Pin 5 gives the best compromise. R21 biases Pin 5 to about .4 volts, which is below the stop threshold at this point. This biasing results in a shorter stop time.

Extra precaution can be taken within the software of the controller IC to further insure accurate stop detector performance over a wide variety of input signal conditions. A typical controller IC stop algorithm is as follows:

> The controller waits the first 10 ms after the LM1863 is tuned to the next channel. The controller then samples the LM1863 stop output 10 times within the next 40 ms. If no high output is sensed within that time the controller concludes there is no valid station at the frequency and moves to the next channel. If, however, at least one high output is detected within the first 50 ms the controller waits an additional 200 ms and at the end of that time re-samples the stop output in order to make its final stop determination.

RF AGC

The RF AGC detector is designed to control the gain of an external RF amplifier which is placed between the antenna and the mixer input. The RF AGC operates by detecting when the input signal to the mixer reaches 6 mVrms, the RF AGC threshold. When the mixer input signal reaches this level the RF AGC is activated and will hold the mixer input level relatively constant at the level of the RF AGC threshold. The gain of the RF AGC determines how constant the RF AGC can control the RF output. The LM1863 RF AGC is high gain and consequently the RF AGC output, Pin 3, will transition from high to low over a very narrow input range to the mixer when the LM1863 is examined in an OPEN LOOP condition. However, in a radio where the RF AGC controls the RF gain, a CLOSED LOOP negative feedback system is established. In this application the RF AGC output will transition from high to low over a large range of signal levels to the input of the RF stage.

The RF AGC threshold has been carefully chosen to prevent overloading the mixer, which would cause distortion and tweet problems. However, the threshold level is sufficiently large to minimize the possibility of strong adjacent stations de-sensitizing the radio by activating the RF AGC and thereby gain reducing the RF front end.

The RF AGC output, Pin 3, is an open collector NPN transistor. This collector must be tied to a positive voltage through a load resistor, R8. Furthermore, decoupling is required (C11 and C12) in order to insure that the RF AGC does not induce significant distortion in the recovered audio. However, the tradeoff between good THD performance and fast stop time is not too severe for the RF AGC because large changes in the RF AGC level are unlikely when moving between adjacent channels. This is because the selectivity in the RF stage is not great enough to cause abrupt signal level changes at the mixer input as the radio is tuned. Thus, since the RF AGC does not have to follow abrupt signal level changes, the time constant on the AGC output can be relatively long which allows for good THD performance. C12 is required in order to insure good RF decoupling of signals at the RF AGC output, and sets the non-dominant pole.

The RF AGC 10 μA threshold is fixed at 6 mVrms at the mixer input. However, due to the gain of the RF stage and

Applications Information (Continued)

losses through the RF transformers, this level may be different when referenced to the antenna input. For the application circuit shown the RF threshold occurs at 2 mVrms at the dummy antenna input. Thus, the RF AGC threshold can effectively be adjusted by altering the gain of the RF stage.

The value of R8 also has some affect on the RF AGC threshold of the application circuit. Smaller values will tend to increase the threshold while larger values will tend to reduce the threshold.

GAIN DISTRIBUTION

The purpose of this section is to clarify some of the tradeoffs involved in redistributing gain from one portion of the radio to another. An AM radio basically has three gain blocks consisting of the RF stage, the mixer, and the IF stage. The total gain of these three blocks must be sufficiently large as to insure reception of weak stations. Given then a fixed amount of required gain how does distributing this gain among the three blocks affect the radio performance?

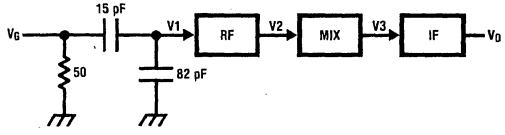
Large amounts of gain in the RF stage will have the effect of decreasing the RF AGC threshold. A decreased RF AGC threshold means that it is more likely that strong adjacent stations can activate the RF AGC and desensitize the radio. Also, a lot of RF gain implies large signals across the RF varactor diodes, which is undesirable for good tracking and can result in overloading these varactors which can cause cross modulation. On the other hand, high RF gain insures good noise performance and improved THD.

High mixer gain implies large signal swings at the mixer output, especially on AGC transients. These large signal swings could cause the mixer ouput transistors to saturate and also could overload the IF stage. On the other hand, redistributing the gain from the IF to the mixer would improve the noise performance of the radio. The gain of the mixer can be controlled moving the tap on the mixer output transformer, T4.

Since the output signal level of the IF is held constant by the AGC, increasing gain in the IF has the effect of reducing the signal level at the IF input. Noise sources at the IF input therefore become a larger percentage of the IF input signal thereby degrading the S/N floor of the radio. For this reason, the LM1863 employs 20 dB of IF AGC. The IF gain of the LM1863 is adjustable by changing the tap across the IF ouput coil, or by changing the ratio of R24 to R4.

The gain distribution for the application circuit is as follows:

Gain Distribution



TL/H/5185–23

V_G = 0 dB (10 μV)
V1 = −16 dB
V2 = +10 dB (Pin 18)
V3 = +33 dB (Pin 10)
V_O = +84 dB (Pin 12)

The IF gain could also be varied by changing the value of R6 across the IF output coil. However, it is a good idea to maintain a high Q IF tank in order to achieve good adjacent channel rejection. In order to prevent distortion due to overloading the IF amplifier, it is important that the impedance Pin 12 sees looking into the IF output tank, T5, does not go below 3K ohms.

The above gain distribution is prior to any AGC action in the radio. This distribution represents a good compromise between the various tradeoffs outlined previously.

LEVEL CONTROLLED LOCAL OSCILLATOR

Tracking of the RF varactors with the local oscillator varactor is a serious consideration in order to insure adequate performance of the ETR radio. Due to non-linear capacitance versus voltage characteristic of the varactor, large signals across these varactors will tend to modulate their capacitance and cause tracking problems. This problem is compounded further if the level of the signals across the varactors change. In an AM radio, the local oscillator frequency changes a ratio of two to one. The Q of the oscillator tank remains fairly constant over this range. Thus, since $Q = R_P/\omega L$ = Constant, this implies that R_P(R_P = unloaded parallel resistance of the tank) must change two to one. The internal level-control loop prevents the two to one change in AC voltage across the tank which the change in the R_P would otherwise cause.

Phase jitter of the local oscillator is very important in regard to AM stereo, where L-R information is contained in the phase of the carrier. Local oscillator jitter has the effect of modulating the L-R channel with phase noise, thus degrading the stereo signal to noise performance. Great care has been taken in the design of the LM1863 local oscillator to insure that phase jitter is a minimum. In fact the dominant source of phase jitter is the high impedance resistor drive to the varactor. The thermal noise of the resistor modulates the varactor voltage, thus causing phase jitter.

VARACTOR TUNED RF STAGE

Electronically tuned car radios require the use of a tuned RF stage prior to the mixer. Many of the performance characteristics of the radio are determined by the design of this stage. Generally speaking it is very difficult to design an integrated RF stage in bipolar, as bipolar transistors do not have good overload characteristics. Thus, the RF stage is usually designed using discrete components. Because of this there is a great deal of concern with minimizing the number of discrete components without severely sacrificing performance. The applications circuit RF stage does just this.

The circuit consists of only two active devices, an N-channel JFET, Q1, which is connected in a cascode type of configuration with an NPN BJT, Q2. Both Q1 and Q2 are varactor tuned gain stages. Q2 also serves to gain reduce Q1 when Q2's base is pulled low by the RF AGC circuit on the LM1863. The gain reduction occurs because Q1 is driven into a low gain resistive region as its drain voltage is reduced. R10 and C15 set the gain of the 1'st RF stage which is kept high (about 19 dB) for good low signal, signal/noise performance. The gain of the front end to the mixer input referenced to the generator output is about +10 dB.

T2 in conjunction with D1, C21 and C26 form the 1'st tuned circuit. C26 does not completely de-couple the RF signal at the cathode of the varactor. In fact, the combination of C26 and C19 act to keep the gain of the whole RF stage constant over the entire AM band. Without special care in this regard the gain variation could be as high as 14 dB.This gain

Applications Information (Continued)

variation would result from the increase in impedance at the secondary's of T2 and T1 as the tuned frequency is increased. The increased impedance results from a constant Q=Rp/(wL) of the tanks over the AM band. With C26 and C19 the gain is held constant to within 6 dB (including the tracking error) over the entire AM band.

C27 de-couples RF signal from the top of T2's primary and allows Q2 to operate properly. C18 is a coupling capacitor which in conjunction with C19 couples the signal from the 1'st RF stage to the 2'nd RF stage. R20 acts to isolate this signal from AC ground at C11. R19 acts in conjunction with C12 to set a high frequency (ie: non-dominant) RF AGC pole which is important for low distortion when the RF AGC is active. The dominant RF AGC pole is set by R8 and C11. Q2 is a high beta transistor allowing for little voltage drop across R20 and R8 due to base current. This keeps the emitter of Q2 sufficiently high (in the absence of RF AGC) to bias Q1 in its square law region.

R13 acts to reduce the 2'nd stage gain and increase Q2's signal handling. R13 must not get too large, however, (ie: R13>100 Ω), or low level signal/noise will be degraded. T3 in conjunction with C20, C27 and D2 form the 2'nd RF tuned circuit. The output of Q2 is capacitively coupled through C28 to the mixer input. The output of Q2 is loaded not only by the reflected secondary impedance but also by R22. R22 is carefully chosen to load the 2'nd stage tuned circuit and broaden its bandwidth. The increased bandwidth of the 2'nd stage greatly improves the cross modulation performance of the front end. In the absence of this increased bandwidth, the relatively large AC signals across varactor D2 result in cross modulation. R22 also reduces the total gain of the 2'nd stage. R22 does slightly degrade (by about 6 dB) the image rejection especially at the high end of the AM band. However, the image rejection of this front end is still excellent and 6 dB is a small price to pay for the greatly increased immunity to cross modulation.

R16 and C29 decouple unwanted signals on V+ from being coupled into the RF stage. This front end also offers superior performance with respect to varactor overload by strong adjacent channels. This results because of the way that gain has been distributed between the 1'st and 2'nd stages.

In summary, this front end offers two stages of RF gain with the 2'nd stage acting to gain reduce the 1'st stage when RF AGC is active. Furthermore, a unique coupling scheme is employed from the output of the 1'st stage to the input of the 2'nd stage. This coupling scheme equalizes the gain from one end of the AM band to the other. Additional care has been taken to insure that excellent cross modulation performance, image rejection, signal to noise performance, overload performance, and low distortion are achieved. Performance characteristics for this front end in conjunction with the LM1863 are shown in the data sheet. Also, information with regard to the bandwidth of the front end versus tuned frequency are given below.

TUNED FREQUENCY	−3 dB BANDWIDTH
530 kHz	6.6 kHz
600 kHz	7.2 kHz
1200 kHz	20.6 kHz
1500 kHz	26.4 kHz
1630 kHz	36 kHz

VARACTOR ALIGNMENT PROCEDURE

The following is a procedure which will allow you to properly align the RF and local oscillator trim capacitors and coils to insure proper tracking across the AM band.

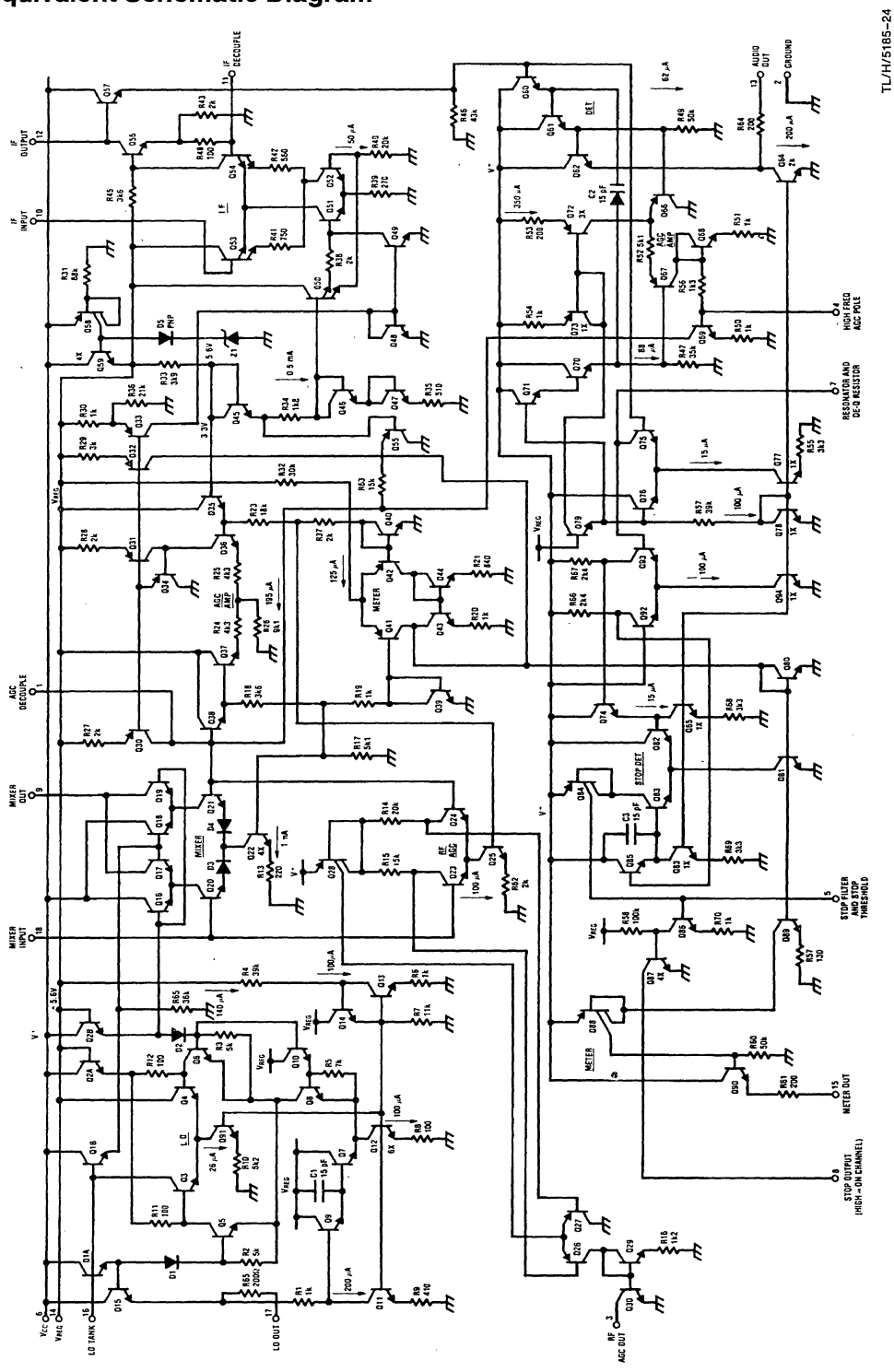
1. Set the voltage across the varactors = 1 volt.
2. Set the trimmers to 50%.
3. Adjust the oscillator coil until the local oscillator is at 980 kHz.
4. Increase the varactor voltage until the local oscillator (LO) is at 2060 kHz and check to see if this voltage is less than 9.5 volts but greater than 7.5 volts. If it is then the LO is aligned. If it is not then adjust the LO coil/trimmer until the varactor voltage falls in this range.
5. Set the RF in to 600 kHz and adjust the tuning voltage until the LO is at 1050 kHz. Peak all RF coils for maximum recovered audio at low input levels.
6. Set RF in to 1500 kHz and adjust the tuning voltage until the LO is at 1950 kHz. Peak all RF trim capacitors for maximum recovered audio at low input levels.
7. Go back to step 5 and iterate for best adjustment.
8. Check the radio gain at 530 kHz and 750 kHz to make sure that the gain is about the same at these two frequencys. If it is not, then slightly adjust the RF coils until it is.

The above procedure will insure perfect tracking at 600 kHz, 950 kHz and 1500 kHz. The amount of gain variation across the AM band using the above procedure should not exceed 6 dB.

ADDITIONAL INFORMATION

R5 and C7 act as a low pass filter to remove most of the residual 450 kHz IF signal from the audio output. Some residual 450 kHz signal is still present, however, and may need to be further removed prior to audio amplification. This need becomes more important when the LM1863 is used in conjunction with a loopstick antenna which might pick up an amplified 450 kHz signal. An additional pole can be added to the audio output after R5 and C7 prior to audio amplification if further reduction of the 450 kHz component is required.

Equivalent Schematic Diagram



National Semiconductor

PRELIMINARY

LM1875 20 Watt Power Audio Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on ±25V supplies. Using an 8Ω load and ±30V supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of advanced circuit techniques and processing to achieve extremely low distortion levels even at high output power levels. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is internally compensated and stable for gains of 10 or greater.

Features

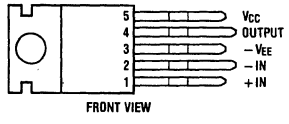
- Up to 30 watts output power
- A_{VO} typically 90 dB
- Low distortion 0.015%, 1 kHz, 20 W
- Wide power bandwidth 70 kHz
- Short circuit protection
- Thermal protection with parole circuit
- High current capability 3A
- Wide supply range 20V-60V
- Internal protection diodes
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Connection Diagram

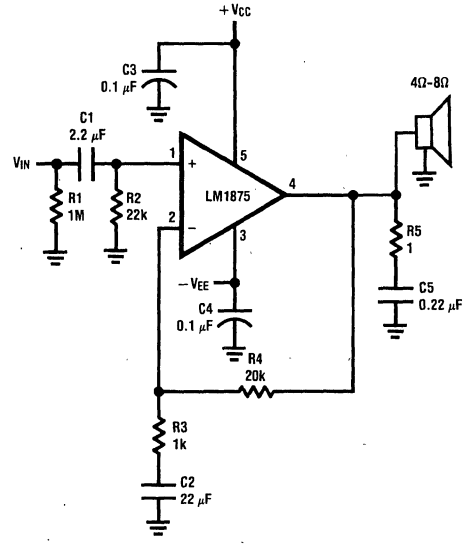
TO-220 Power Package (T)



TL/H/5030–1

Order Number LM1875
See NS Package T05B

Typical Applications



TL/H/5030–2

Absolute Maximum Ratings

Supply Voltage	±30V	Junction Temperature	150°C
Input Voltage	$-V_{EE}$ to V_{CC}	Power Dissipation (Note 1)	30W
Operating Temperature	0°C to + 70°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature	−65°C to + 150°C		

Electrical Characteristics

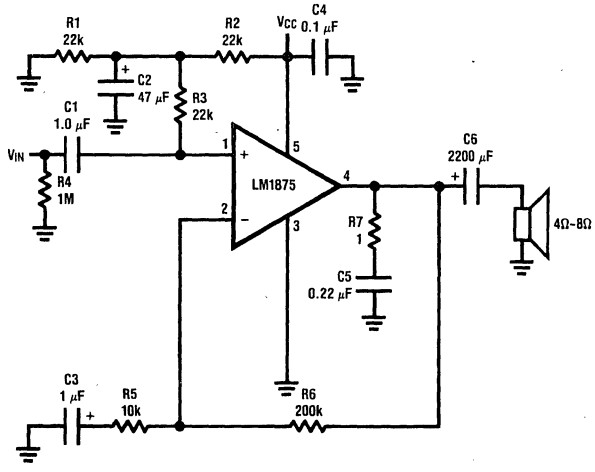
V_{CC} = +25V, $-V_{EE}$ = −25V, T_{TAB} = 25°C, R_L = 8Ω, A_V = 20 (26 dB), f_o = 1 kHz, unless otherwise specified.

Parameter	Conditions	Typical	Tested Limits	Units
Supply Current	P_{OUT} = 0W	70	100	mA
DC Output Level		0		V
Output Power	THD = 1%	25		W
THD	P_{OUT} = 20W, f_o = 1 kHz	0.015		%
	P_{OUT} = 20W, f_o = 20 kHz	0.05	0.4	%
	P_{OUT} = 20W, R_L = 4Ω, f_o = 1 kHz	0.022		%
	P_{OUT} = 20W, R_L = 4Ω, f_o = 20 kHz	0.07	0.6	%
Offset Voltage		±1	±15	mV
Input Bias Current		±0.2	±2	μA
Input Offset Current		0	±0.5	μA
Gain-Bandwidth Product	f_o = 20 kHz	5.5		MHz
Open Loop Gain	DC	90		dB
PSRR	V_{CC}, 1 kHz, 1 Vrms	95	52	dB
	$-V_{EE}$, 1 kHz, 1 Vrms	83	52	dB
Max Slew Rate		8		V/μS
Current Limit		4	3	A
Equivalent Input Noise Voltage	R_S = 600Ω, CCIR	3		μVrms

Note 1: Assumes T_{TAB} equal to 60°C max. For operation at higher tab temperatures and at ambient temperatures greater than 25°C, the LM1875 must be derated based on a maximum 150°C junction temperature. Thermal resistance depends upon device mounting techniques. θ_{JC} is typically 2° C/W. See Application Hints.

Typical Applications (Continued)

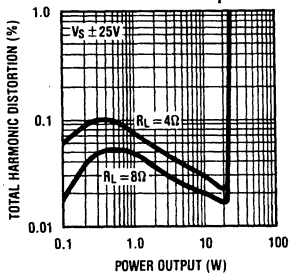
Typical Single Supply Operation



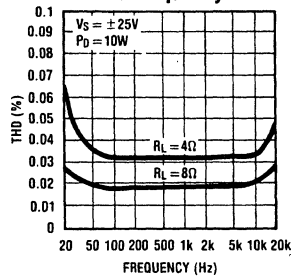
TL/H/5030–3

Typical Performance Characteristics

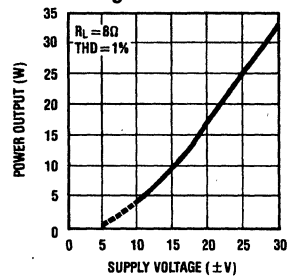
THD vs Power Output



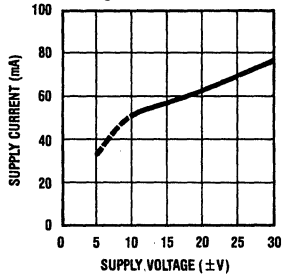
THD vs Frequency



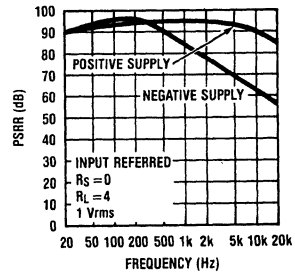
Power Output vs Supply Voltage



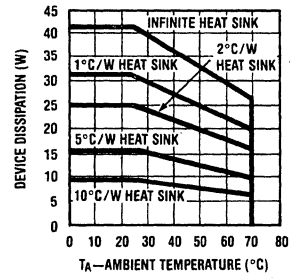
Supply Current vs Supply Voltage



PSRR vs Frequency

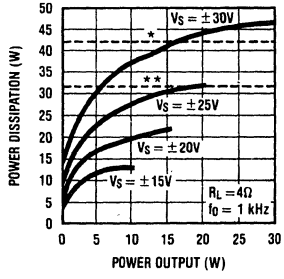


Device Dissipation vs Ambient Temperature†

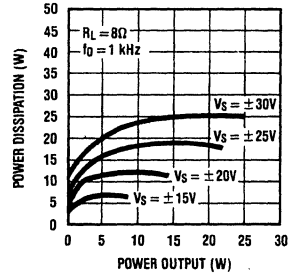


†ϕINTERFACE = 1°C/W.
See Application Hints.

Power Dissipation vs Power Output



Power Dissipation vs Power Output

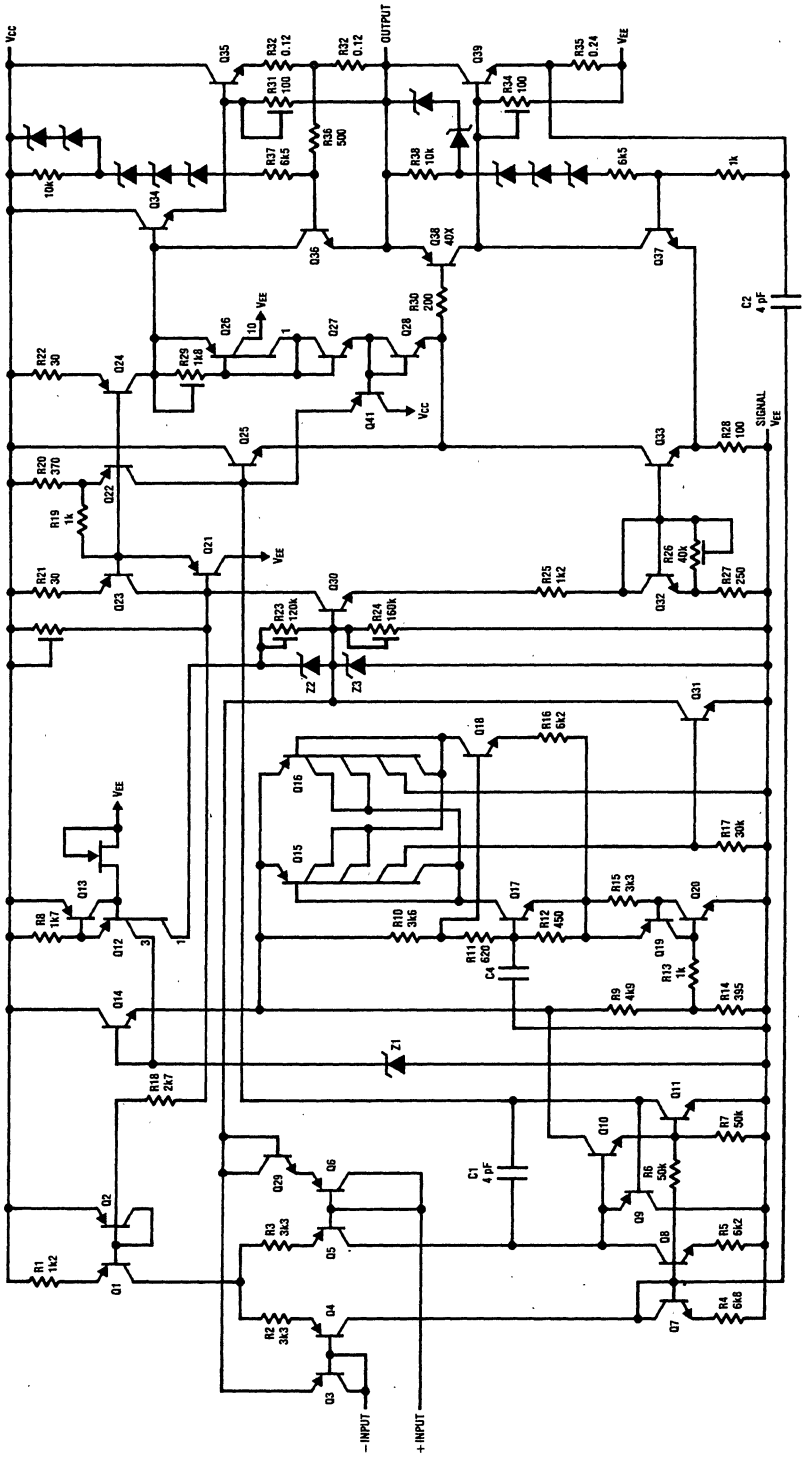


TL/H/5030–4

*Thermal shutdown with infinite heat sink

**Thermal shutdown with 1°C/W heat sink

Schematic Diagram



TL/H/5030–5

Application Hints

STABILITY

The LM1875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM1875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

Proper layout of the printed circuit board is very important. While the LM1875 will be stable when installed in a board similar to the ones shown in this data sheet, it is sometimes necessary to modify the layout somewhat to suit the physical requirements of a particular application. When designing a different layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM1875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM1875 is no exception. If the output of the LM1875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF. The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1Ω) should be placed in series with the output of the LM1875. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a 5 μH inductor.

DISTORTION

The preceding suggestions regarding circuit board grounding techniques will also help to prevent excessive distortion levels in audio applications. For low THD, it is also necessary to keep the power supply traces and wires separated from the traces and wires connected to the inputs of the LM1875. This prevents the power supply currents, which are large and nonlinear, from inductively coupling to the LM1875 inputs. Power supply wires should be twisted together and separated from the circuit board. Where these wires are soldered to the board, they should be perpendicular to the plane of the board at least to a distance of a couple of inches. With a proper physical layout, THD levels at 20 kHz with 10W output to an 8Ω load should be less than 0.05%, and less than 0.02% at 1 kHz.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic audio power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM1875 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM1875, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM1875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM1875 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

POWER DISSIPATION AND HEAT SINKING

The LM1875 must always be operated with a heat sink, even when it is not required to drive a load. The maximum idling current of the device is 100 mA, so that on a 60V power supply an unloaded LM1875 must dissipate 6W of power. The 54°C/W junction-to-ambient thermal resistance of a TO-220 package would cause the die temperature to rise 324°C above ambient, so the thermal protection circuitry will shut the amplifier down if operation without a heat sink is attempted.

Application Hints (Continued)

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM1875 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM1875, R_L is the load resistance, and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. The curves of "Power Dissipation vs Power Output" give a better representation of the behavior of the LM1875 with various power supply voltages and resistive loads. As an example, if the LM1875 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150°C - 70°C}{19W} = 4.2°C/W.$$

Using $\theta_{JA} = 2°C/W$, the sum of the case-to-heat-sink interface thermal resistance and the heat-sink-to-ambient thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry.

If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM1875 and the heat sink. The heat sink thermal resistance must then be less than

4.2°C/W − 2°C/W − 1.6°C/W = 0.6°C/W.

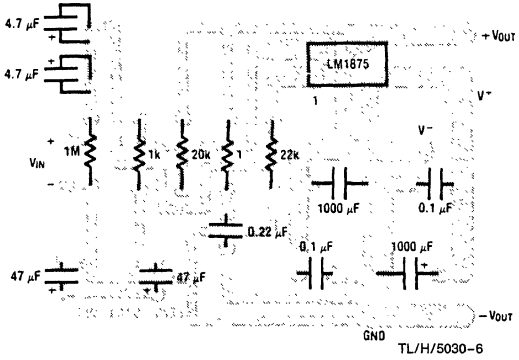
This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be reduced to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

Note: When using a single supply, maximum transfer of heat away from the LM1875 can be achieved by mounting the device directly to the heat sink (tab is at ground potential); this avoids the use of a mica or other type insulator.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load (usually considered to be a worst-case loudspeaker load) will be roughly that of the same amplifier driving the resistive part of that load. For example, a loudspeaker may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Component Layouts

Split Supply



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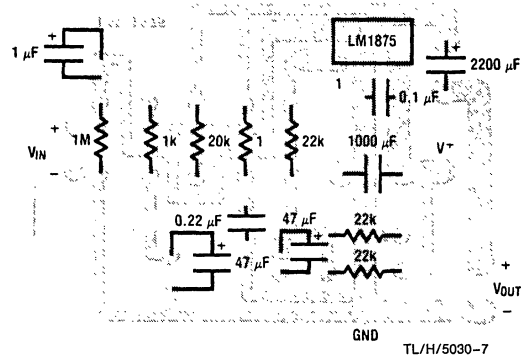
Single Supply



TL/H/5030-7

S 12

National Semiconductor

PRELIMINARY

LM1884 TV Stereo Decoder

General Description

The LM1884 is a decoder designed for television stereo. An L-R output is provided to drive further audio processing.

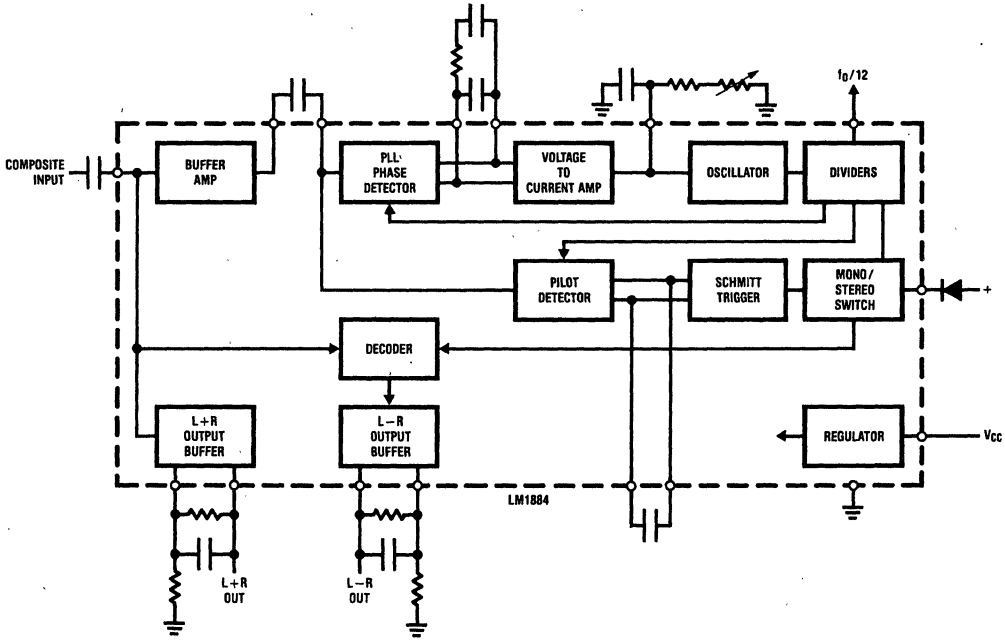
Applications

- Stereo television sets
- Stereo adapters
- Cable television

Features

- Low impedance L+R and L−R outputs
- Mono/Stereo switching and indication
- Low distortion - 0.10% typical

Block Diagram



TL/H/6759–1

Absolute Maximum Ratings $T_A = +25°C$ unless otherwise noted

Power Supply Voltage	16V	Storage Temperature Range	−65°C to +150°C
Power Dissipation (Package Limitation)	1800 mW	Lamp Drive Voltage	
Derate Above $T_A = +25°C$	15 mW/°C	Max Voltage at Pin 7 with Lamp "Off"	16V
Operating Temp. Range (Ambient)	−40°C to +85°C	Lamp Current	100 mA

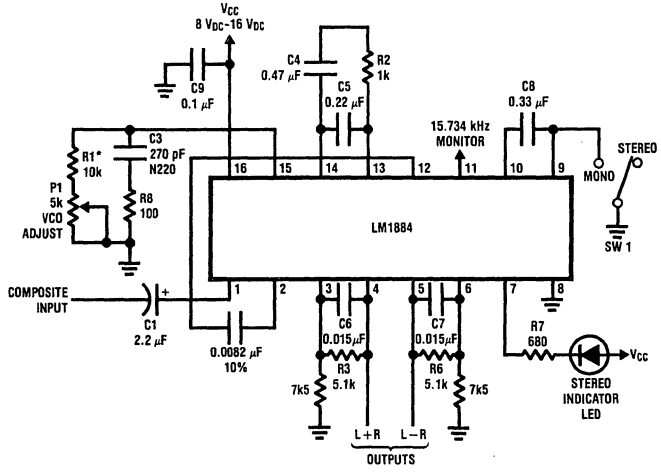
Electrical Characteristics Parameters Guaranteed by Electrical Testing

Test Circuit, $T_A = +25°C$, $V_{CC} = 12V$ unless noted

Parameter	Conditions	Min	Typ	Max	Units
DC	$V_{IN} = 0$				
Supply Current	$V_{CC} = 16V$	15	33	50	mA
Output Voltage	Pin 4	1.7	3.5	5.0	V
Output Voltage	Pin 5	1.7	3.8	5.0	V
Output Impedance	Pins 4, 5		100	300	Ω
Lamp Leakage	Lamp off, pin 7 voltage = 16V			1.0	mA
Lamp Saturation Voltage	Lamp on, pin 7 current = 100 mA			2.0	V
Audio	Composite signal with 38 kHz subcarrier and 10% 19 kHz pilot. Adjust P1 for 19 kHz plus/minus 10 hz. (Note 1)				
L+R Channel Gain	$V_{IN} = 2.5Vpp$ L = R, pilot off, pin 4	0.8	1.0	1.2	
L+R Channel THD	$V_{IN} = 2.5Vpp$ L = R, pilot off, pin 4		0.1	1.0	%
Gain Ratio, L+R Channel to L−R Channel	$V_{IN} = 2.5Vpp$, L only	−2.0	0.0	2.0	db
Supply Rejection	100 mVrms, 1 kHz on supply, $V_{IN} = 0$	30	60		db
DC Output Shift, Mono to Stereo	Pilot off to on, pins 4, 5			±20	mV
Input Impedance	Pin 1	15	50	150	kΩ
PLL					
Pilot Level for Lamp On		12		20	mV
Pilot Level for Lamp Off		3		10	mV
Capture Range	Pilot = 25 mVrms	±0.5			%

Note 1: The LM1884 will be available tested with a 15.734 kHz pilot after product introduction.

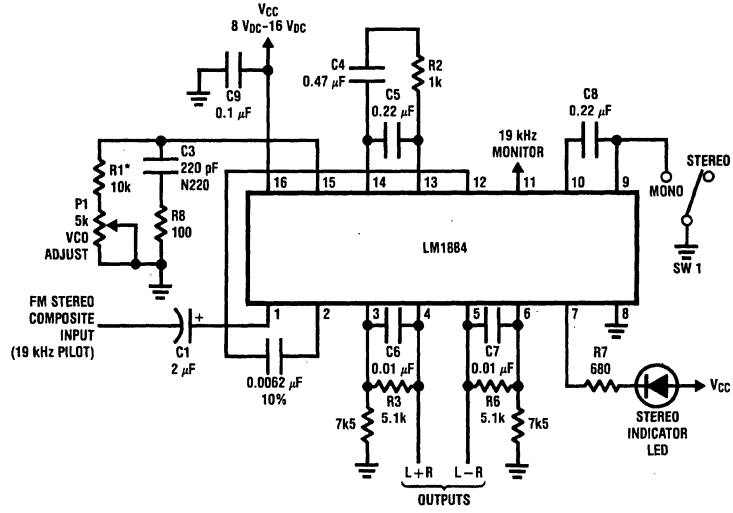
Test Circuit



* Metal film, zero temperature Coefficient resistor recommended

FIGURE 1.

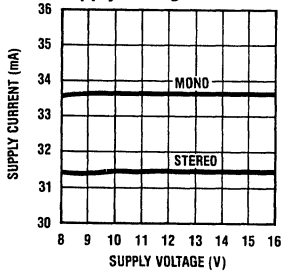
Typical Application



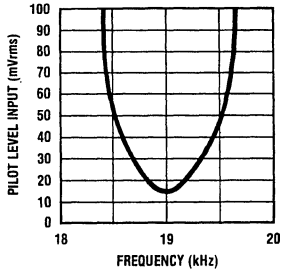
TL/H/6759–3

* Metal film, zero temperature coefficient resistor recommended

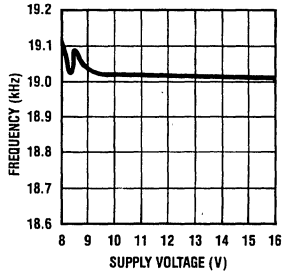
Supply Current vs Supply Voltage



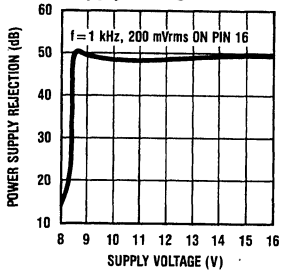
Capture Range vs Pilot Level



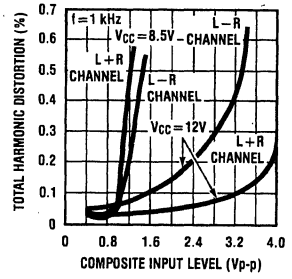
Total Harmonic Distortion vs Composite Input Level



VCO Frequency vs Supply Voltage



Power Supply Rejection vs Supply Voltage



TL/H/6759–4

National Semiconductor

PRELIMINARY

BI-LINE™

LM1893 Carrier-Current Transceiver†

General Description

Carrier-current systems use the power mains to transfer information between remote locations. This bipolar carrier-current chip performs as a power line interface for half-duplex (bi-directional) communication of serial bit streams of virtually any coding. In transmission, a sinusoidal carrier is FSK modulated and impressed on most any power line via a rugged on-chip driver. In reception, a PLL-based demodulator and impulse noise filter combine to give maximum range. A complete system may consist of the LM1893, a COPS™ controller, and discrete components.

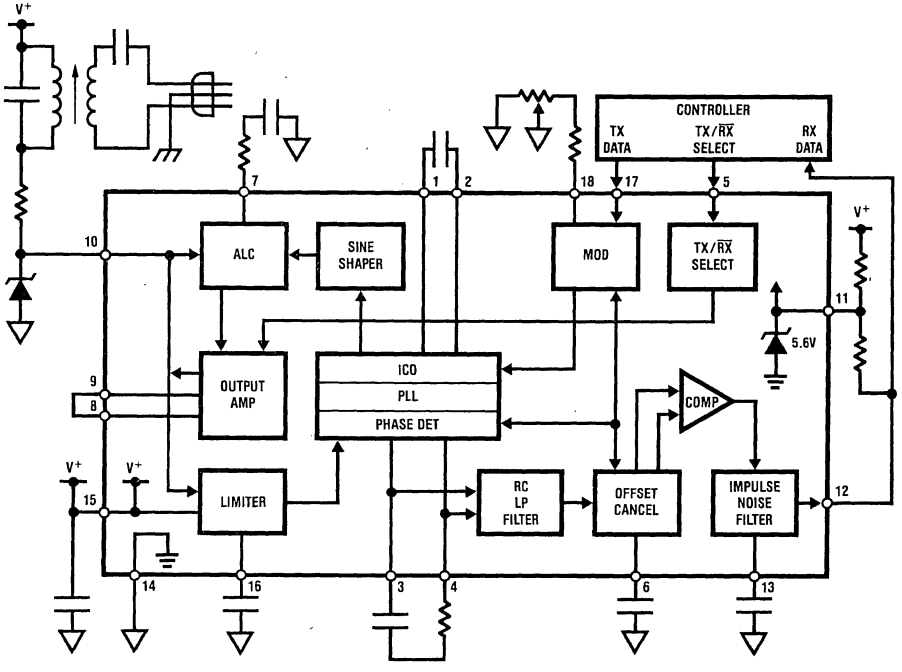
Features

- Noise resistant FSK modulation
- User-selected impulse noise filtering
- Up to 4.8 kBaud data transmission rate
- Strings of 0's or 1's in data allowed
- Sinusoidal line drive for low RFI
- Output power easily boosted 10-fold
- 50 to 300 kHz carrier frequency choice
- TTL and MOS compatible digital levels
- Regulated voltage to power logic
- Drives all conventional power lines

Applications

- Energy management systems
- Home convenience control
- Inter-office communication
- Appliance control
- Fire alarm systems
- Security systems
- Telemetry
- Computer terminal interface

Typical Application



TL/H/6750–1

FIGURE 1. Block diagram of carrier—current chip with a complement of discrete components making a complete transceiver. Use caution with this circuit—dangerous line voltage is present.

†Carrier-Current Transceivers are also called Power Line Carrier (PLC) transceivers.

Absolute Maximum Ratings

Supply voltage	30 V
Voltage on pin 12	55 V
Voltage on pin 10 (Note 1)	41 V
Voltage on pins 5 and 17	40 V
5.6 V DC zener current	100 mA
Junction temperature: transmit mode	150°C
receive mode	125°C
Maximum continuous dissipation, $T_A = 25°C$, (Note 2): plastic DIP N	1.66 W
Operating ambient temp. range	−25 to 85°C
Storage temperature range	−65 to 150°C
Lead temp., soldering, 7 seconds	260°C

General Electrical Characteristics (Note 3). The test conditions are: $V^+ = 18$ V and $F_O = 125$ kHz, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
1	5.6 V Zener voltage, V_Z	Pin 11, $I_Z = 2$ mA	5.6	5.2 5.9		V min. V max.
2	5.6 V Zener resistance, R_Z	Pin 11, $R_Z = (V_Z@10\text{ mA} - V_Z@1\text{ mA})/(10\text{ mA} - 1\text{ mA})$	5			Ω
3	Carrier I/O peak survivable transient voltage, V_{OT}	Pin 10, discharge 1 μF cap. charged to V_{OT}	80	60		V max.
4	Carrier I/O clamp voltage, V_{OC}	Pin 10, $I_{OC} = 10$ mA, RX mode 2N2222 diode pin 8 to 9	44	41 50		V min. V max.
5	Carrier I/O clamp resistance, R_{10}	Pin 10, $I_{OC} = 10$ mA	20			Ω
6	TX/$\overline{RX}$ low input voltage, V_{IL}	Pin 5	1.8	0.8		V max.
7	TX/$\overline{RX}$ high input voltage, V_{IH}	Pin 5 (Note 9)	2.2	2.8		V min.
8	TX/$\overline{RX}$ low input current, I_{IL}	Pin 5 at 0.8 V	−2	−20 1		μA min. μA max.
9	TX/$\overline{RX}$ high input current, I_{IH}	Pin 5 at 40 V	10^{-4}	−1 10		μA min. μA max.
10	RX−TX switch-over time, T_{RT}	Time to develop 63% of full current drive through pin 10	10			μs
11	TX−RX switch-over time, T_{TR}	1 bit time $T_B = 1/(2F_{DATA})$ Time T_{TR} is user controlled with C_M, see Apps. Info.	2			bit
12	ICO initial accuracy of F_O	TX mode, $R_O = 6.65$ kΩ, $C_O = 560$ pF	125	113 137		kHz min. kHz max.
13	ICO temperature coefficient of F_O	TX mode, $(F_{OMAX} - F_{OMIN})/(T_{JMAX} - T_{JMIN})$	(±200)			PPM/°C
14	Temperature drift of F_O	TX mode, $-25 \le T_J \le 150°C$	(±2.0)		(±5.0)	% max.

Transmitter Electrical Characteristics (Note 3). The test conditions are: $V_+ = 18$ V and $F_O = 125$ kHz unless otherwise noted. The transmit center frequency is F_O, FSK low is F_1, and FSK high is F_2.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
15	Supply voltage, V^+, range	Meets test 17 spec. at $T_J = 25°C$ and: $\lvert(F_1[14V] - F_1[18V])/F_1[18V]\rvert < 0.01$ $\lvert(F_1[24V] - F_1[18V])/F_1[18V]\rvert < 0.01$	(13)	14 24	(15) (23)	V min. V max.
16	Total supply current, I_{QT}	Pin 15. Pin 12 high. I_{QT} is I_Q through pin 15 and the average current I_{ODC} of the Carrier I/O through pin 10	42	79		mA max.
17	Carrier I/O output current, I_O	100Ω load on pin 10	70	45		mApp min.
18	Carrier I/O lower swing limit, V_{ALC}	Pin 10. Set internally be ALC 2N2222 diode pin 8 to 9	4.7	4.0 5.7		V min. V max.
19	THD of I_O (Note 6)	Q of 10 tank driving 10Ω line 100Ω load, no tank	0.6 5.5		(2.0) 9	% max. % max.
20	FSK deviation, $F_2 - F_1$	$(F_2 - F_1)/([F_2 + F_1]/2)$	4.4	3.7 5.2		% min. % max.
21	Data In. low input voltage, V_{IL}	Pin 17	1.7	0.8		V max.
22	Data In. high input voltage, V_{IH}	Pin 17 (Note 9)	2.1	2.8		V min.
23	Data In. low input current, I_{IL}	Pin 17 at 0.8 V	−1	−10 1		μA min. μA max.
24	Data In. high input current, I_{IH}	Pin 17 at 40 V	10^{-4}	−1 10		μA min. μA max.

Note 1: Transients may reach above 60 V; see the transient peak voltage characteristic curve.

Note 2: The maximum power dissipation rating should be derated for device operation above 25°C to insure that the junction temperature remains below the maximum rating. Use a θ_{JA} of 75°C/W for the N package using a socket in still air. Consult the Application Information section for more detail.

Receiver Electrical Characteristics (Note 3). The test conditions are: $V^+ = 18$ V, $F_O = 125$ kHz, ±2.2% deviation FSK, $F_{DATA} = 2.4$ kHz, $V_{IN} = 100$ mVpp, in the receive mode, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
25	Supply voltage, V^+, range	Functional receiver (Note 7)	(12)	13 30	(13.5) (28)	V min. V max.
26	Supply current, I_{QT}	I_{QT} is pin 15 (V_+) plus pin 10 (Carrier I/O) current. 2.4 kΩ Pin 13 to GND.	11	5 14		mA min. mA max.
27	Carrier I/O input resistance, R_{10}	Pin 10	19.5	15 30		kΩ min. kΩ max.
28	Max. data rate, F_{MD}	Functional receiver (Note 7) square-wave data, 2.4 kHz = 4.8 kBaud	10	4.8	(2.4)	kBaud
29	PLL capture range, F_C	$C_F = 100$ pF, $R_F = 0$ Ω	±40	±20		% min.
30	PLL lock range, F_L	$C_F = 100$ pF, $R_F = 0$ Ω	±45	±20		% min.
31	Receiver input sensitivity, S_{IN}	For a functional receiver (Note 8) Referred to chip side (pin 10) of the line-coupling XFMR: $F_O = 50$ kHz $F_O = 300$ kHz Referred to line side of XFMR: (assuming a 7.07:1 XFMR) $F_O = 50$ kHz $F_O = 300$ kHz	 1.8 2.0 1.4 0.26 0.29 0.20	 10	 (12)	 mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS} mV_{RMS}
32	Tolerable input dc voltage offset range, V_{INDC}	Pin 10 lower than pin	2	0.1		V max.
33	Data Out. breakdown voltage	Pin 12, leakage I ≤ 20 μA	70	55		V min.
34	Data Out. low output, V_{OL}	Pin 12, sat. voltage at $I_{OL} = 2$ mA	0.15	0.4		V max.
35	Impulse noise filter current, I_I	Pin 13 charge and discharge current	±50	±45 ±85		μA min. μA max.
36	Offset hold cap. bias voltage, V_{CM}	Pin 6	2.0	1.3 3.5		V min. V max.
37	Offset hold capacitor max. drive current, I_{MCM}	Pin 6. V(pin 3) − V(pin 4) = ±250 mV	±48	±25 ±80		μA min. μA max.
38	Offset hold bias current, I_{OHB}	Pin 6, TX mode. Bias pin 6 as it self-biased during test 32.	−0.5	−20	(−40) (40)	nA min. nA max.
39	Phase comparator current, I_{PC}	Bias pins 3 and 4 at 8.5 V I_{PC} = I(pin 3) + I(pin 4), TX mode	100	50 200		μA min. μA max.
40	Phase detector output resistance, R_{PD}	Pins 3 and 4. $R_{PD} = (V@100\mu A - V@50\mu A)/(50\mu A)$	10	6 18		kΩ min. kΩ max.
41	Phase detector demodulated output voltage, V_{PD}	Pin 3 to 4, measured after filtering out the $2F_O$ component	100	60 180		mVpp min. mVpp max.
42	Fast offset cancel voltage "window" -to-V_{PD} ratio, V_W/V_{PD}	$V_{PIN3} - V_{PIN4} = \pm V_{WINDOW}$ + DC offset Drive for ±1 μA pin 6 current	0.95	0.70 1.20		V/V min. V/V max.
43	Power supply rejection, PSRR	$C_L = 0.1$ μF. PSRR = CMRR. 120 Hz	80			dB min.

Note 3: The values inside parenthesis ( ) apply over the full operating temperature range after warmup for the specified supply voltage range. All other numbers apply at $T_A = T_J = 25°C$.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed (but not 100% production tested) over the temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Total harmonic distortion is measured using THD = [I_{RMS} (all components at or above $2F_O$)]/[I_{RMS} (fundamental)].

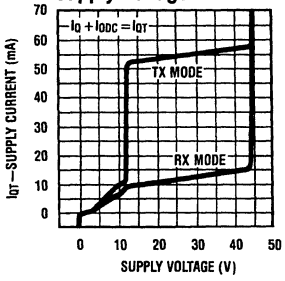
Note 7: Receiver function is defined as the error-free passage of 1 cycle of 50% duty-cycle 2.4 kHz square-wave data (2 sequential 208 μS bits), with the first bit being a "1." All of the data transitions (edges) must fall within ±10% (±20.8 μs) of their noise-free positions. RX time delay is minimized by using no impulse noise filter cap. C_I for this test.

Note 8: During the sensitivity check, note 7 requirements are followed with these exceptions: (1) data rate $F_{DATA} = 1.2$ kHz, (2) all of the data transitions must fall within ±20% (±41.6 μs) of their noise-free positions, and (3), a time-domain filter capacitor (C_I) is used. The time delay of C_I is ½ bit, or 208 μs. (C_I is approximately 6200 pF).

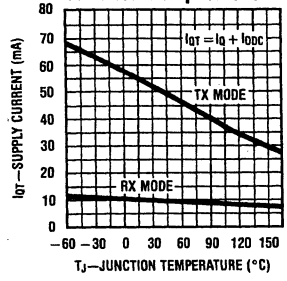
Note 9: For TTL compatibility use a pull-up resistor to increase min. V_{OH} to above 2.8 V.

Typical Performance Characteristics (V^+ = 18V, F_O = 125 kHz, circuit of *Figure 1*)

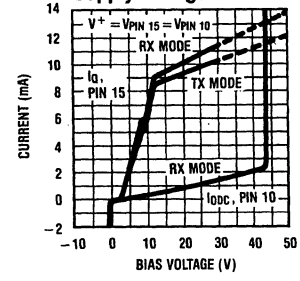
Supply Current vs. Supply Voltage



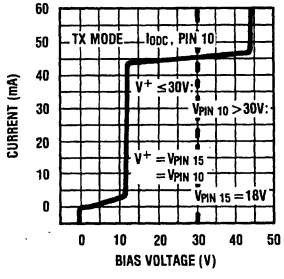
Supply Current vs. Junction Temperature



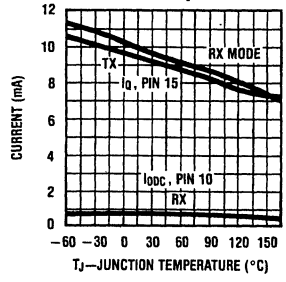
Bias Currents vs. Supply Voltage



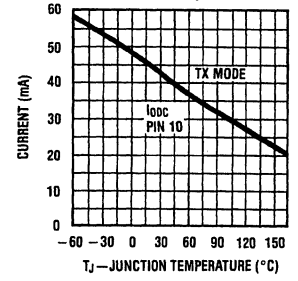
Pin 10 Current vs. Supply Voltage



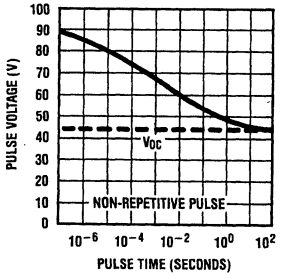
Bias Currents vs. Junction Temperature



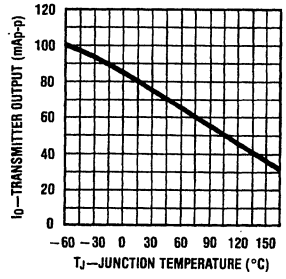
Pin 10 Current vs. Junction Temperature



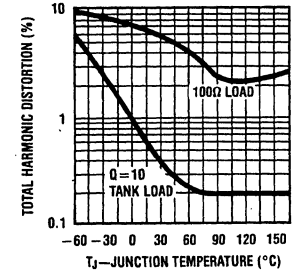
Transient Voltage Survival vs. Pulse Time



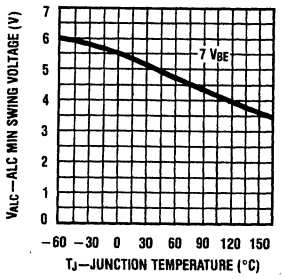
Transmitter Output Current vs. Junction Temperature



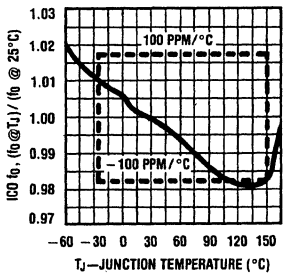
Transmitter Sinusoid THD vs. Junction Temperature



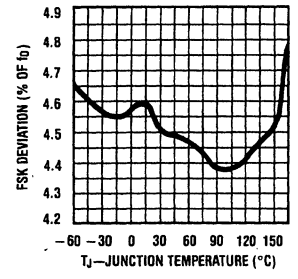
ALC Voltage vs. Junction Temperature



ICO Frequency vs. Junction Temperature



Transmitter FSK Deviation vs. Junction Temperature



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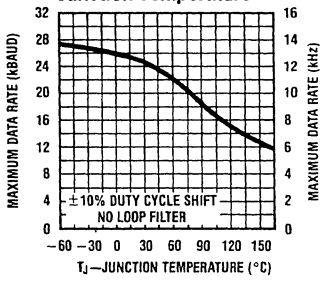
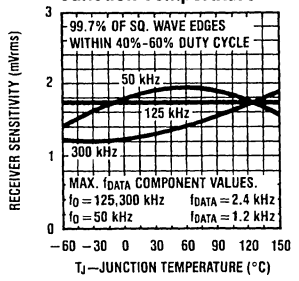
Typical Performance Characteristics ($V^+ = 18V$, $F_O = 125$ kHz, circuit of *Figure 1*) (Continued)

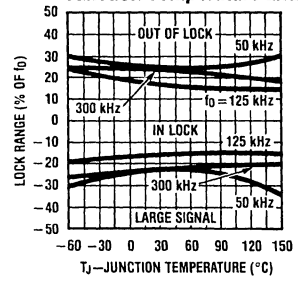
Maximum Data Rate vs. Junction Temperature



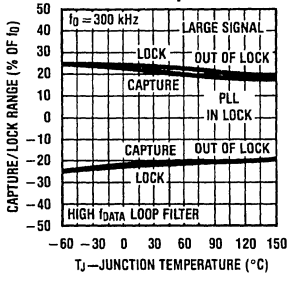
Receiver Sensitivity vs. Junction Temperature



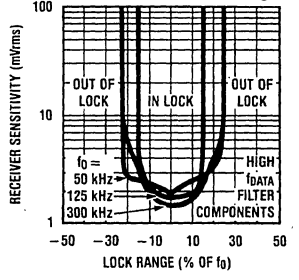
PLL Lock Range vs. Junction Temperature and F_O



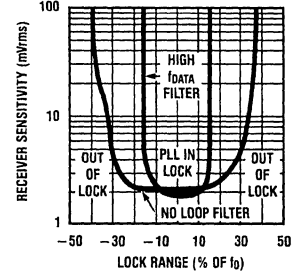
PLL Capture & Lock Range vs. Junction Temperature



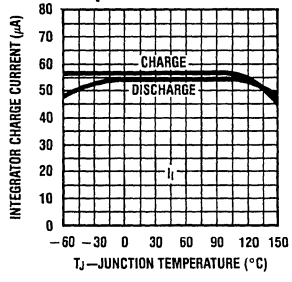
Receiver Sensitivity vs. PLL Lock Range and F_O



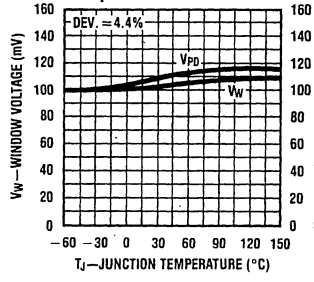
Receiver Sensitivity vs. PLL Lock Range and Loop Filter



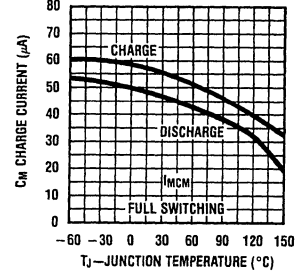
Impulse Noise Filter Current vs. Junction Temperature



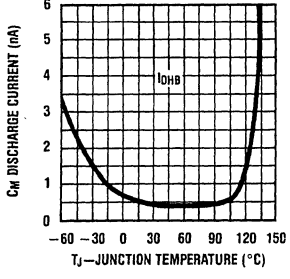
Phase Detector Output Voltage vs. Junction Temperature



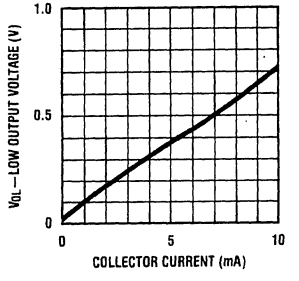
Offset Hold Cap. Charge Currents vs. Junction Temperature



Offset Hold Cap. Bias Current vs. Junction Temperature



Data Out. Low Voltage vs. Pull Down Current



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Application Information

THE DATA PATH

The BI-LINE™ chip serves as a power line interface in the carrier-current transceiver (CCT) system of *Figure 3*. *Figure 4* shows the interface circuit now discussed. The controller may select either the transmit (TX) or receive (RX) mode. Serial data from the controller is used to generate a FSK-modulated 50 to 300 kHz carrier on the line in the TX mode. In the RX mode line signal passes through the coupling transformer into the PLL-based receiver. The recreated serial bit stream drives the controller.

With the IC in the TX mode (pin 5 a logic high), baseband data to 5 kHz drive the modulator's Data In pin to generate a switched 0.987I/1.022I control current to drive the low TC, triangle-wave, current-controlled oscillator to ±2.2% deviation. The tri-wave passes through a differential attenuator and sine shaper which deliver a current sinusoid through an automatic level control (ALC) circuit to the gain of 200 current output amplifier. Drive current from the Carrier I/O develops a voltage swing on T_1's (*Figure 4*) resonant tank proportional to line impedance then passes through the step-down transformer and coupling capacitor C_C onto the line. Progressively smaller line impedances cause reduced signal swing, but never clipping-thus avoiding potential radio frequency interference. When large line impedances threaten to allow excessive output swing on pin 10, the ALC shunts current away from the output amplifier, holding the voltage swing constant and within the amp's compliance limit. The amplifier is stable with a load of any magnitude or phase.

In the RX mode (pin 5 a logic low), the TX sections on the chip are disabled. Carrier signal, broad-band noise, transient spikes, and power line component impinge of the receiver's input highpass filter, made up of C_C and T_1, and the tank bandpass filter. In-band carrier signal, band-limited noise, heavily attenuated line frequency component, and attenuated transient energy pass through to produce voltage swing on the tank, swinging about the positive supply to drive the carrier I/O receiver input. The balanced Norton-input limiter amplifier removes DC offsets, attenuates line frequency, performs as a bandpass filter, and limits the signal to drive the PLL phase detector differentially. The differential demodulated output signal from the phase detector, containing AC and DC data signal, noise, system DC offsets, and a large twice-the-carrier frequency component, passes through a 3-stage RC lowpass filter to drive the offset cancel circuit differentially. The offset cancelling circuit works by insuring that the (fixed) ±50 mV signal delivered to the data squaring ("slicing") comparator is centered around the 0 mV comparator switch point. Whenever the comparator signal plus DC offset and noise moves outside the carefully matched ±50 mV voltage "window" of the offset cancel circuit, it adjusts its DC correction voltage in series with the differential signal to force the signal back into the window. While the signal is within the ±50 mV window, the DC offset is stored on capacitor C_M. By grace of the highly non-linear offset hold capacitor charging during offset cancelling, the DC cancellation is done much more quickly than with an AC coupling capacitor normally used in place of the offset cancel circuit. Since impulse noise spikes normally ring the signal symmetrically around 0 V, the fully bilateral offset cancel topology affords excellent noise rejection. The switched current output of the comparator drives the impulse noise filter integrator capacitor that rejects all data pulses of less than the integrator charge time. False bits and noise may appear as duty-cycle jitter errors at the open collector serial data output.

Dual-In-Line Package

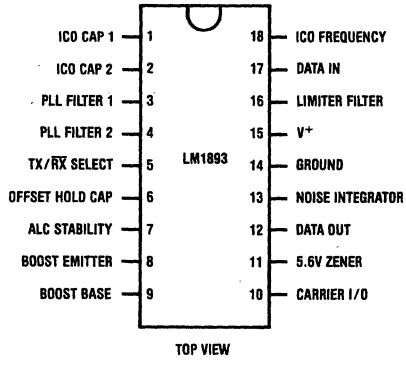

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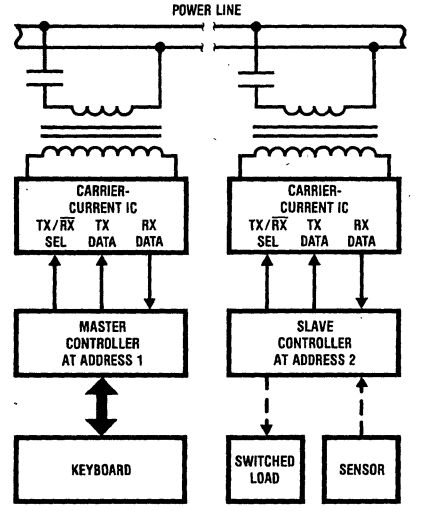
FIGURE 2. Connection Diagram

See NS Package Number N18A
Order Part LM1893N



TL/H/6750–3

FIGURE 3. The block diagram of a carrier-current system using the Bi-Line chip to interface digital controllers via the power line

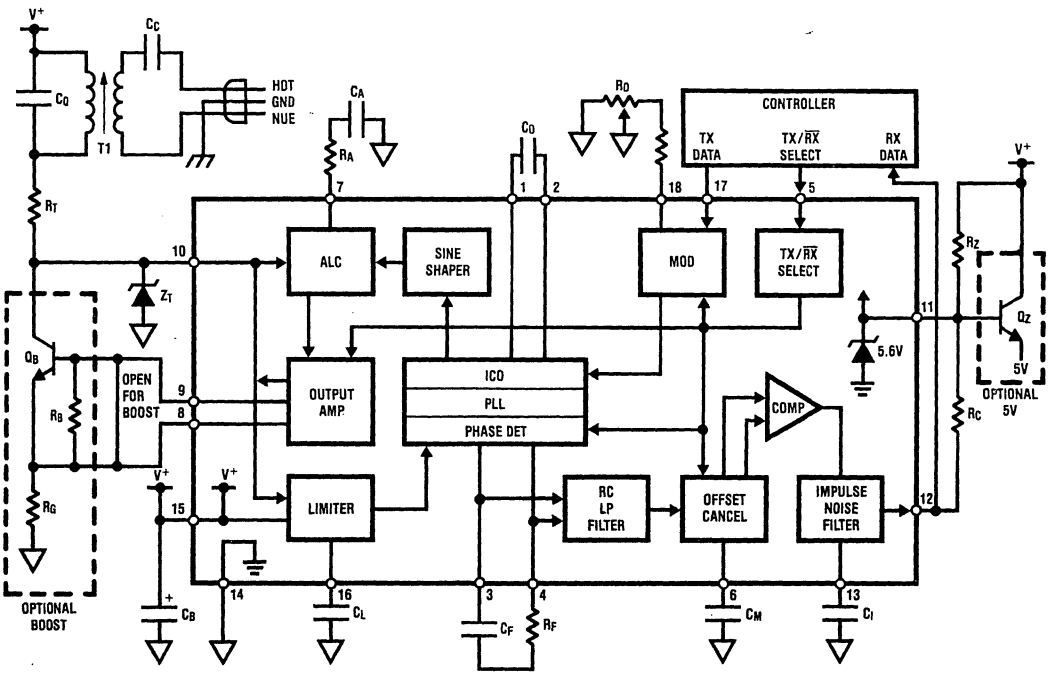


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FIGURE 4. Block diagram of a CCT system with the boost and 5V supply options shown in dashed boxes

Application Information (Continued)

#	Recommended Value	Purpose	Effect of making the component value: Smaller	Effect of making the component value: Larger	Notes
C_O	560 pF	Together, C_O and R_O	Increases F_O	Decreases F_O	±5% NPO ceramic. Use low TC
R_O	6.2 kΩ	set ICO F_O.	Increases F_O <5.6 k not recommended.	Decreases F_O >7.6 k not recommended.	2 k pot and 5.6 k fixed R. Poor F_O TC with <5.6 k R_O.
C_F	0.047 μF	PLL loop filter pole	Less noise immune, higher F_{DATA}, more PLL stability.	More noise immune, lower F_{DATA}, less PLL stability.	Depending on R_F value and F_O, PLL unstable with large
R_F	3.3 kΩ	PLL loop filter zero	PLL less stable, allows less C_F. Less ringing.	PLL more stable, allows more C_F. More ringing.	C_F. See Apps. Info. C_F and R_F values not critical.
C_C	0.22 μF	Couple F_O to line, C_C and T_1 low-pass attenuates 60 Hz.	Low TX line amplitude. Less 60 Hz T_1 current. Less stored charge.	Drives lower line Z. More 60 Hz T_1 current. More stored charge.	≥250 V non-polar. Use $2C_C$ on hot and neutral for max. line isolation, safety.
C_Q	0.033 μF	Tank matches line Z, bandpass filters,	Tank F_O up or increase L of T_1 for constant F_O.	Tank F_O down or decrease L of T_1 for constant F_O.	100 V nonpolar, low TC, ±10% High large-signal Q needed.
T_1	Use recommended XFMR	isolates from line, and attenuates transients.	Smaller L: higher F_O or increase C_C; decreased F_O line pull.	Larger L: lower F_O or decrease C_C; increased F_O line pull.	Optimize for low F_O line pull with control of F_O TC and Q.
C_A	0.1 μF	ALC pole	Noise spikes turn ALC off.	Slower ALC response.	R_A optional. ALC stable
R_A	10 kΩ	ALC zero	Less stable ALC.	More stable ALC.	for $C_A \geq 100$ pF.
C_L	0.047 μF	Limiter 50 kHz pole, 60 Hz rejection.	Higher pole F, more 60 Hz reject. F_O attenuation?	Lower pole F, less 60 Hz reject, more noise BW.	Any reasonably low TC cap. 300 pF guarantees stability.
C_M	0.47 μF	Holds RX path V_{OS}	Less noise immune, shorter V_{OS} hold, faster V_{OS} acquisition, shorter preamble.	More noise immune, longer V_{OS} hold, slower V_{OS} acquisition, longer preamble.	Low leakage ±20% cap. Scale with F_{DATA}.
C_I	0.047 μF	Rejects short pulses like impulse noise.	Less impulse reject, delay, more pulse jitter.	More impulse reject, delay, less pulse jitter.	C_I charge time ½ bit nom. Must be <1 bit worst-case.
R_C	10 kΩ	Open-col. pull-up	Less available sink I.	Less available source I.	$R_C \geq 1.5$ kΩ on 5.6 V
R_Z	12 kΩ	5.6 V Zener bias	Larger shunt current, more chip dissipation.	Smaller shunt current, less V+ current draw.	$1 < I_Z < 30$ mA recommended. (Chip power-up needs 5.6 V)
Z_T	≥44 V BV <60 V peak	Transient clamp	Higher R_Z-excess peak V, Zener and chip damage.	Lower R_Z gives enhanced transient clamp. Costly.	Recommend Zener rated for ≥500 W for 1 ms
R_T	4.7 Ω	Transient I limit	Damage Z_T, pull up V_+.	Excessive TX attenuation.	Carbon comp. recommended
R_B	180 Ω	Base bleed	Faster, lower THD I_O.	Inadequate turn-off speed.	Boost optional. Q_B F(−3 dB)
Q_B	Power NPN	Boost gain device	Excessive T_J and V_{SAT}.	More rugged, but costly.	of >200 MHz. R_B > 24 Ohm.
R_G	1.1 Ω	Current setting R	More I_O, need higher h_{fe}.	Less I_O, lower min. h_{fe}.	$I_O = 700[(10 + R_G)/10R_G]$ mApp.
C_B	≥47 μF	Supply bypass	Transients destroy chip.	Less supply spike.	V_+ never over abs. max.

FIGURE 5. A quick explanation of the external component function using the circuit of *Figure 4*. Values given are for $V_+ = 18$ V, $F_O = 125$ kHz, $F_{DATA} = 360$ Baud (180 Hz), using a 115 V 60 Hz power line

Component Selection

Assuming the circuit of *Figure 4* is used with something other than the nominal 125 kHz carrier frequency, 180 Hz data rate, 18V supply voltage, etcetera, the component values listed in *Figure 5* will need changing. This section will help direct the CCT designer in finding the required component values with emphasis placed on look-up tables and charts instead of circuit theory. It is assumed that the designer has selected values for carrier center frequency, F_O; data rate, F_{DATA}; supply voltage, V_+; and power line voltage, V_L, and frequency, F_L. If one or more of those parameters is not defined, one may read the data sheet and make an educated guess - or just pick a nominal value and try the circuit.

Maxims to keep in mind, based on CCT electrical performance considerations only, are: 1) the higher the F_O the better, 2) the lower the maximum data rate the better, and 3) the more time and frequency filtering the better.

Use *Figure 5* as a quick reference to the external component function.

The Transmitter

C_O

Central to chip operation is the low TC of F_O emitter-coupled oscillator. With proper C_O, the F_O of the $2V_{BE}$ amplitude triangle-wave oscillator output may vary from near DC to above 300 kHz. While C_O may have any value, C_O should

The Transmitter (Continued)

be made above 10 pF so that parasitic capacitance is not dominant. Excessive or unbalanced common-mode-to-ground capacitance should be avoided. A low temperature coefficient (TC) of capacitance (<100 PPM/°C), such as a monolithic NPO ceramic multilayer type, preserves low TC of F_O. *Figure 6* finds a C_O value given F_O.

R_O

Resistor R_O is used by the IC to generate a V_{BE}/R related current that is multiplied by 2 to produce the 200 μA ICO control current that sets F_O. The control current TC "bucks" the V_{BE} related tri-wave amplitude across C_O to effect a low TC of F_O. Vary R_O to trim F_O, within limits. Raising F_O more than 20% above its untrimmed value by means of decreasing R_O more than 20% is not recommended. Low R_O, and so high control current, risks ICO saturation and poor TC under worst-case conditions. Raising R_O reduces the demodulated signal amplitude from the phase detector; raising R_O by more than a factor of 2 (1 octave) is not recommended.

Since lower TC pots are relatively costly, it is recommended that R_O be made up of a 5.6 k fixed (<100 PPM/°C) resistor with a 2 kΩ (<250 PPM/°C) series pot.

C_A and R_A

Components C_A and R_A control the dynamic characteristics of the transmitter output envelope. Their values are not critical. Use the values given in *Figure 5*. C_A and R_A are functions of loaded T_1 tank Q, R_O, F_{DATA}, and line impulse noise. Any changes made in C_A and R_A should be made based on empirical measurements of a CCT on the line. Roughly, C_A acts as an ALC pole and R_A an ALC zero.

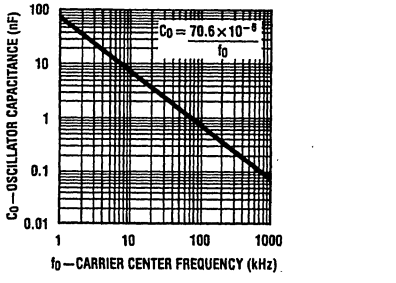
T_1

At this point, the CCT system designer may choose to use one of the recommended transformers or to design T_1 oneself. Consult "The Coupling Transformer" section to help with the design of T_1 if a new or boost-capable transformer is needed. The recommended 125 kHz transformer functions with an I_O of up to 600 mApp.

It is recommended that CCT systems use the recommended transformers, described in *Figure 7*, for T_1. The 3 transformers are optimized for use in the ranges of 50–100 kHz, 100–200 kHz, and 200–400 kHz with unloaded Q's (Q_U) of about 35, and loaded Q's (Q_L) of about 12. Three secondary taps are supplied with nominal 7.07, 10, and 14.1 turns ratios (N) to drive industrial and residential power line impedances of 3.5, 7, and 14Ω respectively. All are inexpensive, all have the same pin-outs for easy exchange in a PC board, and all are small - on the order of 10 mm diameter at the base.

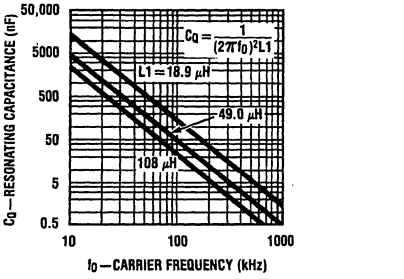
C_Q

Tank resonant frequency F_Q must be correct to allow passage of transmitter signal to the line. Use *Figure 8* to find C_Q's value. Trimming F_Q to equal F_O is done with T_1's trimming slug. The inductance of T_1 has a TC of +150 PPM/°C which may be cancelled by using a −150 PPM/°C cap such as polystyrene. Since circulating current in the tank is ¼ A_{RMS}, C_Q should have a low series resistance (a 1 Ω series resistance is too much). Polypropelene caps are excellent, "orange drop" mylars are adequate, while many other mylars are inadequate. A 100V rating is needed for transient protection.



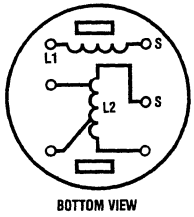
TL/H/6750-5

FIGURE 6. Find C_O's value knowing F_O

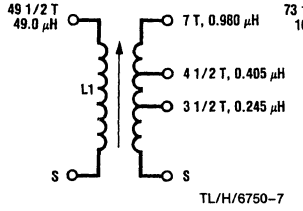


TL/H/6750-10

FIGURE 8. Find C_O's value given F_O

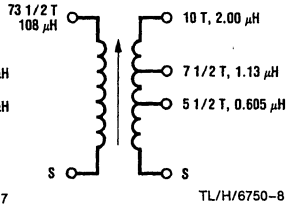


TL/H/6750-6



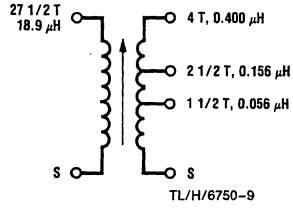
TL/H/6750-7

125 kHz
C^2 10UL-001
Toko 707VX-A042YUK



TL/H/6750-8

50 kHz
C^2 10UL-002
Toko 707VX-A043YUK



TL/H/6750-9

300 kHz
C^2 10UL-003
Toko 161XN-A207YUK

FIGURE 7. The recommended T_1 transformers. All are available through:
1) C^2 Electronics, 1787 Vets Highway, Central Islip, N.Y., 11722 (516) 348-6839 or,
2) Toko America, 5520 W. Touhy Ave., Skokie, IL, 60077, (312) 677-3640.

The Transmitter (Continued)

C_C

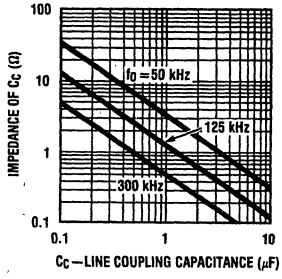
Capacitor C_C's primary function is to block the power line voltage from T_1's line-side winding. Also, C_C and T_1's line-side winding comprise a LC highpass filter. The self-inductance of T_1 is far too low to support a direct line connection. C_C must have a low enough impedance at F_O to allow T_1 to drive transmitted energy onto the line. To drive a 14 Ω power line, the impedance of C_C should be below 14 Ω.

Use *Figures 9* and *10* to find the reactive impedance of C_C to check that it is less than the line impedance. Then check to see that the power line current is small enough to keep T_1 well out of saturation; the recommended transformers can withstand a 10 Amp-turn magnetizing force (1 Amp through the worst-case 10 turn line-side winding).

Caution is required when choosing C_C to avoid series resonance of the series combination of C_C, the transformer inductance, and the reflected tank impedance. The low resistance of the network under series resonance will load the line, possibly decreasing range. For your particular line coupling circuit, measure for series resonance using some expected line impedance load.

R_B

This base-bleed resistor turns Q_B off quickly - important since the amplifier output swing is about 200 V/μs. An R_B below about 24 Ω will conduct excessive current and overload the chip amplifier and is not recommended.



TL/H/6750–11

FIGURE 9. C_C's impedance should be, as a rule-of-thumb, smaller than the lowest expected line impedance

R_G

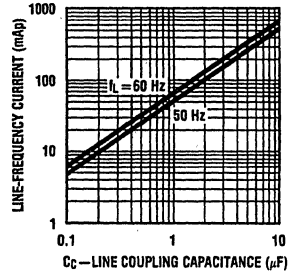
This resistor, in parallel with the internal 10 Ω resistor, fixes the current gain of the output amplifier, and so the output current amplitude. *Figure 11* gives output current and minimum AC current gain h_{fe} for Q_B when R_G is used to boost output current.

Q_B

The boost gain transistor Q_B must be fast. Double-diffused devices with 50 MHz F_T's work, slower transistors (epi-base types) do not preserve a sinusoidal waveform when F_O is high or oscillate. Q_B must have a certan minimum h_{fe} for given boost levels, as shown in *Figure 11*. *Figure 12* shows the power Q_B must dissipate continuously operating with a shorted output. BV_{CER} (R = R_B) must be 60 V or greater and Q_B must have adequate SOA for transient survival.

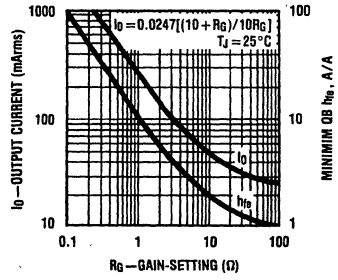
Z_T

Unfortunately, potentially damaging transient energy passes through transformer T_1 onto the Carrier I/O pin (instantaneous power of greater than 1 KW has been measured using the recommended transformers). For self protection, the Carrier I/O has an internal 44 V voltage clamp with a 20 Ω series resistance. A parallel low impedance 44 V external transient suppression diode will then conduct the lion's share of any current when transients force the Carrier I/O to a high voltage.



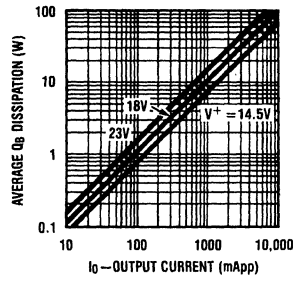
TL/H/6750–12

FIGURE 10. A graph showing the AC line-induced current passed by C_C



TL/H/6750–13

FIGURE 11. Output amplifier current and required min. Q_B h_{fe} versus gain-setting resistor R_G



TL/H/6750–14

FIGURE 12. Boost transistor power dissipation versus amplifier output current

Z_T must be used unless some precaution is taken to protect the Carrier I/O pin from line transients or transients caused when stored line energy in C_C is discharged by the random phase of power line connection and disconnection. Worst case, C_C may discharge a full peak-to-peak line voltage into the tuned circuit. Another way to reduce the need for Z_T is by placing another magnetic circuit in the signal path that relies on a high, but easily saturated, permeability to couple a primary and secondary winding - a toroidal transformer for example. Toroids cost more than Z_T.

Use an avalanche diode designed specifically for transient suppression — they have orders of magnitude higher pulse power capability than standard avalanche diodes rated for

The Transmitter (Continued)

Breakdown Voltage	44–49V @ 1 mA
Maximum Leakage	1 μA @ 40V
Capacitance	300 pF @ BV
Maximum Clamp Voltage	64.5V @ 7.8A
Peak Non-Repetitive Pulse Power (REA Standard Exponential Pulse)	10 kW for 1 μs
Surge Current	70A for 1/120s

FIGURE 13. Key specifications for a recommended transient suppressor Z_T available from General Semiconductor, 2001 West Tenth Place, Tempe, AZ 85281, 602-968-3101, part no. SA40A

equal DC dissipation. Metal oxide varistors have not proven useful because of their inferior clamping coefficient. Specifications for an example minimum diode are given in *Figure 13.*

The Receiver

The receiver and transmitter share components C_C, T_1, C_Q, R_T, Z_T, C_O, R_O, and peripheral supply and bias components that are not in need of change for RX mode operation. Values for the balance of the components are now found.

Line-Frequency Rejection

To use the ultimate sensitivity of the device, fully 110 dB of 115 V, 60 Hz attenuation is required between the line and the limiter amplifier output. Using the circuit topology of *Figure 4*, the combined attenuation of the C_C/T_1 highpass, the tuned transformer, and the bandpass filter attenuation of the limiter amplifier give far more line rejection than the above-stated minimum. However, if some other CCT line coupling circuit is used, line rejection will become important to the system designer.

Receiver input power supply rejection (PSRR) and common-mode rejection (CMRR) are one-in-the-same using the supply-referenced signal input of *Figure 4*. Ripple swings both differential inputs of the Norton amp. equally, while the single-ended input signal swings only the positive input. Overall PSRR consists of the input CMRR (set by the input stage component matching) and the ripple-frequency attenuation of the input amplifier bandpass response that passes carrier frequency but stops low frequencies. A typical 1% resistor and 1 mV n-p-n mirror offsets give 26 dB of attenuation, the bandpass gives 54 dB 120 Hz attenuation, for an overall 80 dB PSRR to allow tens of volts of ripple before impacting ultimate sensitivity.

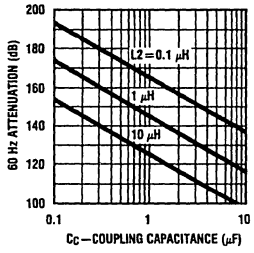
C_C

A value was chosen earlier. Knowing T_1's secondary inductance allows a check of LC line attenuation using *Figure 14.*

C_L

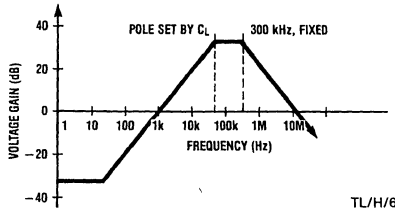
The Norton input limiter amplifier has a bandpass filter for enhanced receiver selectivity, noise immunity, and line frequency rejection. The nominal response curve for F_O = 50 kHz is shown in *Figure 15.* The 300 kHz pole is fixed. The 50 kHz pole is set by C_L's value. After C_L is found, the resulting line frequency attenuation is found for the bandpass filter.

Use *Figure 15* to find a C_L value given for F_O. The approximate line frequency attenuation of the bandpass filter may then be found in *Figure 16. Figure 15* returns a value for C_L 33% larger than nominal, giving a low frequency pole 33% low to allow for component tolerances.

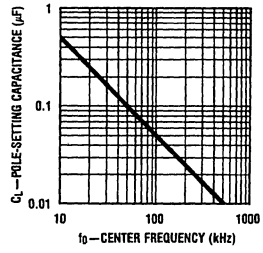


TL/H/6750–15

FIGURE 14. The 60 Hz line rejection of the highpass filter made up of C_C and T_1's line-side winding (neglecting capacitive coupling)



TL/H/6750–16

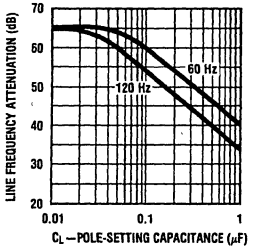


TL/H/6750–17

FIGURE 15. Given F_O, C_L is found. Also shown is the input amplifier's small signal amplitude response

C_F and R_F

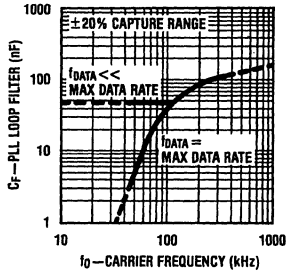
These phase-locked loop (PLL) loop filter components remove some of the noise and most of the $2F_O$ components present in the demodulated differential output voltage signal from the phase detector. They affect the PLL capture range, loop bandwidth, loop overshoot, damping, and capture time. Because the PLL has an inherent loop pole due to the integrator action of the ICO (via C_O), the loop pole set by C_F and the zero set by R_F gives the loop filter a classical 2nd-



TL/H/6750–18

FIGURE 16. The Norton-input limiter amplifier bandpass filter line-frequency signal attenuation given C_L

The Transmitter (Continued)



TL/H/6750–19

FIGURE 17. Find C_F given F_O. *Figure 19* gives the maximum data rate

order response. Zero C_F and R_F give the most stable PLL with the fastest response. Large C_F's with a too-small R_F cause PLL loop instability leading to poor capture range and step response or oscillation.

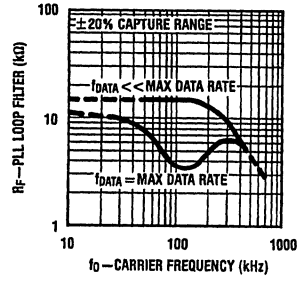
Calculation of C_F and R_F is quite difficult, involving not only the 2nd-order loop step response, but also the PLL non-dominant poles, the tuned transformer stepped-frequency response, and the RC lowpass step response (for data rates approaching 1 kHz). C_F and R_F values are best found empirically. Tolerance is not critical. Component values are selected to give the best possible impulse noise rejection while preserving a ±20% capture range and wide stability margin. *Figures 17* and *18* give C_F and R_F values versus F_O.

Note that C_F and R_F are a function of data rate only for high data rates and are not plotted against data rate - as one might expect. The reason for this is important to understand if the CCT system designer wishes to find C_F and R_F empirically. Data signal is, loosely speaking, passed through the PLL loop and is therefore potentially attenuated if the loop bandwidth is on the order of the 3rd harmonic of the data rate, or less. Overall loop bandwidth is held as low as possible for maximum noise rejection while passing the data. Loop bandwidth is roughly proportional to the geometric mean of the unfiltered loop bandwidth and the filter pole set by C_F. Therefore, C_F is related to data rate. Unfortunately, the loop capture range falls to critically low values when large enough values of C_F are used to reduce loop bandwidth down to the 100's of Hz range, for low data rates. The obvious way out is to then reduce the unfiltered loop bandwidth. That bandwidth is approximately proportional to the value of C_O. For a fixed F_O, unfiltered loop bandwidth reduction requires a larger C_O and larger control current. With this chip, changing the control current is not allowed. So one is forced to choose a C_F/R_F combination with some minimum capture range, say ±20%, that is within some guardband from the point of loop instability. Happily, impulse noise tends to last only fractions of a millisecond so that the lack of low bandwidth loop response with low data rates is not a heavy penalty. As long as there is adequate capture range, the impulse noise filter performs admirably. Note that reducing F_O will reduce the no-filter loop bandwidth, and indeed the maximum data rate falls below the limit set by the RC lowpass filter as F_O falls below 100 kHz.

The tuned transformer characteristics will affect the demodulated data waveform more than C_F and R_F at low data rates. Tank Q and off-tuning will affect overshoot during the FSK frequency steps. This is a property of tuned circuits.

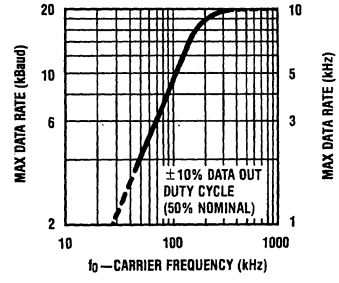
C_M

Capacitor C_M stores a voltage corresponding to a correction factor required to cancel the phase detector differential output DC offsets. The stored voltage is 5/6 of the DC offset plus some bias level of about 2.2 V. A large C_M value increases the time required to bias-up the receive path at the beginning of transmission. A large C_M does filter well and store its bias voltage long. Because of the initial random charge of C_M, the receiver must be given both a positive-going and a negative-going data transition to charge to the proper bias voltage. Therefore, reducing C_M's value to one that may be charged in less than 1 bit time will not save biasing time and is not recommended.



TL/H/6750–20

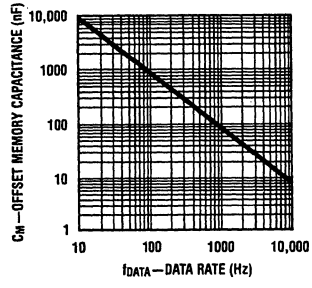
FIGURE 18. Find R_F given F_O with F_{DATA} a parameter



TL/H/6750–21

FIGURE 19. The maximum data rate versus F_O using loop filter components optimized for max. noise performance while retaining a min. ±20% capture range (large signal)

Use *Figure 20* to find C_M's value knowing F_{DATA}, assuming the standard 2 bit receive charge time is desired. The cap. value and TC are not critical, but the capacitor should have low leakage.



TL/H/6750–22

FIGURE 20. Size C_M assuming a 2 bit-time receive bias time

The Transmitter (Continued)

C_I

The impulse noise filter integrator capacitor C_I is used to disallow the passage of any pulse shorter than the integrator charge time. That charge time, set to a nominal ½ bit time, is the time required for a ±50 μA charge current to swing C_I over a 2 V_{BE} range. Charge time under worst case conditions must never be greater than a bit time since no signal could then pass. Using a ±10% capacitor, full junction temperature range, and full specified current range, a maximum nominal charge time of ½ bit is recommended. *Figure 21* gives C_I versus data rate under those conditions.

R_C

The collector pull-up resistor is sized to supply adequate pull-up current drive and speed while preserving adequate output low current drive.

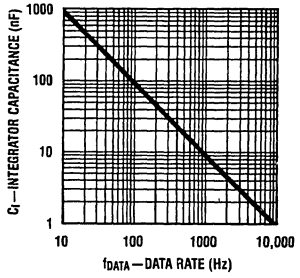


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FIGURE 21. Impulse noise filter cap. C_I versus F_{DATA} where the charge time is ½ bit time

Breadboarding Tips

During CCT system evaluation, some techniques listed below will simplify certain measurements.

— Use caution when working on this circuit - dangerous line voltages may be present.

— When evaluating PLL operation, offset cancel circuit operation, and loop filter values, use the filter of *Figure 22* to view the demodulated signal minus the $2F_O$ and noise components. This filter models the RC lowpass filter on chip.

— When evaluating CCT system noise performance on a real power line, it is desirable to vary the signal amplitude to the receiver. This is not easy. An in-line lineproof L-pad is fine except that the line impedance is unknown and variable and so the L-pad will rarely match. Instead, the power output of a chip transmitter may be controlled using the circuit of *Figure 23*. This circuit controls the ALC.

— Monitoring charge current in C_M is sometimes important to analyze the offset cancel circuit. Measuring the current by dropping more than a few mV in a series resistor affects operation and is not recommended. A workable method is to make C_M small so that it may follow any data signal. Any change in pin 6 voltage shows that the data signal reaching the offset cancel circuit is larger than its nominal ±50 mV voltage window. A C_M on the order of 500 pF with a 1 μA pull-down allows pin 6 to follow the internal signal (with a gain of about 5.6).

— It is sometimes desirable to place impulse noise on the line. A simple light dimmer with a 100 W light bulb load produces representative impulse noise.

— Do not allow peak currents of over 1 A through the 5.6 V Zener. In other words, don't short charged capacitors into this low-impedance device. Take care not to momentarily short pins 10 and 11 - damaging the IC.

— *Figure 24* shows some typical signals beginning with serial data transmitted to received signal.

Tuning Procedure

First, trim F_O by putting the chip in the TX mode, setting a logical high data input, and measuring the TX high frequency, 1.022 F_O, on the Carrier I/O using these steps:

1. Take pin 17 to a logic low.
2. Take pin 5 to a logic high.
3. Place a counter on pin 10.
4. Adjust R_O on pin 18 for F = 1.022F_O.

Second, the line transformer is tuned. The chip is placed in the TX mode, a resistive line load is connected to disable the ALC by reducing tank voltage swing below its limit. FSK data is then passed through the tank so that the tank envelope may be adjusted for equal amplitude for high and low data.

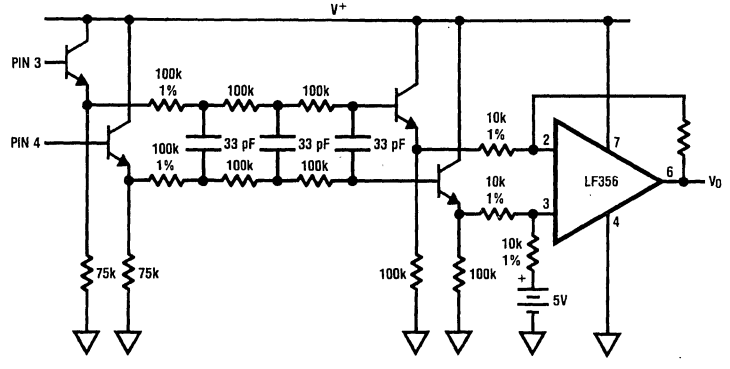

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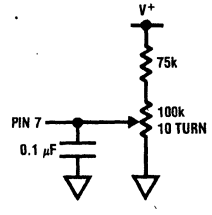
FIGURE 22. Circuit to view the differential demodulated data signal, minus the noise and $2F_O$ components, conveniently with a single-ended gain-of-ten output

The Transmitter (Continued)

1. Take pin 5 to a logic high.
2. Place a logic-level square wave at or below the receiver's maximum data rate on pin 17.
3. Temporarily place a 330 Ω resistor across the tank.
4. Place a scope on pin 10.
5. Adjust the transformer slug for the lowest envelope modulation.

In lieu of the 330 Ω resistive load, T_1 may be coupled to the power line to better simulate actual load and tank pull conditions during tank tuning. Alternatively, a passive network representing an average line impedance may be connected to the line side of T_1. The circuit of *Figure 23* should then be used to defeat the leveling effect of the ALC.



TL/H/6750–26

FIGURE 23. A means of transmitter output amplitude control is shown

Thermal Considerations

It is desirable to place the largest possible signal on the power line for maximum range, limited only by the chip power dissipation and maximum junction temperature T_J. The falling output power at elevated T_J allows a more optimal power output - high power at low T_J and lower power at high T_J for chip self-protection. However, it is still possible to exceed the maximum T_J within the specified ambient temperature limit (T_A = 85°C) under worst case conditions of 100% TX duty cyle, high supply, shorted load, poor PC board layout (with small copper foil area), and an above nominal current part. Under those conditions, a part may dissipate 2140 mW, reaching a T_J = 170°C worst-case (admittedly a rare occurrence). Proper system design includes the measurement or calculation of T_J max. to guarantee function under worst-case operation. Like all devices with failure modes modeled by the Arrhenius model, the high chip reliability is further enhanced by keeping the die temperature mercifully below the absolute maximum rating.

A direct method of measuring operating junction temperature is to measure the V_{BE} voltage on pin 18, which is always available under all operating modes. The graph of *Figure 25* may be used to find T_J, knowing V_{BE} at the operating point in question and V_{BE} at $T_A = T_J$ = 25°C. V_{BE} is found by powering up a chip (in RX mode) that has been dissipating zero power at some T_A for some time and measuring V_{BE} in under 1 s (for better than 5°C accuracy).

Alternately, T_J may be calculated using:

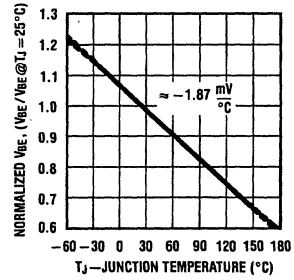
$$T_J = T_A + \theta_{JA}P_D \quad (1)$$

where θ_{JA} is 75°C/W for the plastic (N) package using a socket. That θ_{JA} value is for a high confidence level; nominal θ_{JA} for an N package is 60°C/W, lower with good PC board layout. Since P_D is a relatively strong function of T_J, an iterative solution process starting with an initial guess for T_J is used. With the estimated T_J, find the total supply current found in the typical performance characteristics.

Transmit-To- Receive Switch-Over Time

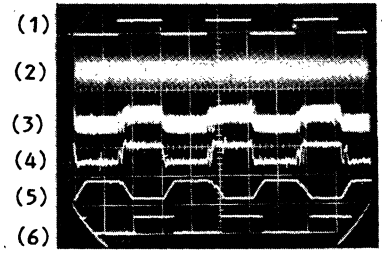
An important figure-of-merit for a half-duplex CCT link, affecting effective data rate, is the TX-to-RX switch time T_{TR}. Using the recommended component values gives this part a nominal 2 bit-time (1 bit time = $1/[2F_{DATA}]$) over a wide range of operating conditions, where the receiver requires 1 positive-going and 1 negative-going data transition. T_{TR} cannot be decreased significantly but does increase as noise filtering, especially via C_M, is increased. Impulse noise at switch, signals near the limiting sensitivity, poor F_O match between receiver and transmitter because of poor trim or worst-case conditions, and the statistical nature of PLL locking may all contribute to increase T_{TR} to possibly 4 bit-times.

T_{TR} is lower when a pair of LM1893's handshake rapidly. The receiver was designed to "remember" the RX-mode DC operating points on C_M and C_F while in the TX mode.



TL/H/6750–27

FIGURE 25. T_J may be found by using the temperature coefficient of pin 18 V_{BE} if V_{BE} is known at 25°C



TL/H/6750–23

FIGURE 24. Oscillogram revealing signals at several important nodes under weak signal (0.5 mV_{RMS}) conditions with SCR spikes on an otherwise quiet 115 V, 60 Hz power line. The signals are: 1) transmitted data, 2) RX carrier on the tuned transformer, 3) demodulated signal from the PLL, 4) signal after RC lowpass, 5) data at impulse noise filter integrator, and 6) received data. Horizontal scale is 10 ms per div.

The Transmitter (Continued)

Under noisey worst case conditions, C_M will discharge to the point of false operation after 35 bit-times in the TX mode (1400 bit times with no noise and a nominal part, F_{DATA} = 180 Hz). T_{TR} is about 0.8 ms (proportional to the selected F_O) plus ½ bit-time.

The major components of T_{TR} are described below for a nominal 125 kHz F_O, 180 Hz F_{DATA}, lightly-loaded tank with a Q of 20, and the circuit of *Figure 4*. The remote CCT has been operating in the TX mode with a 26.6 V_{PP} tank swing and is now selected as a receiver. An incoming signal requiring the ultimate receiver sensitivity immediately is placed on the line.

First, the tank stored energy at the transmit frequency must decay to a level below the 2.8 mV_{PP} swing caused by the 0.14 mV_{RMS} incoming line signal containing the information to be received.

$$\text{decay time} = \frac{Q}{\pi F_O} \ln\left(\frac{V_1}{V_O}\right) =$$

$$\frac{20}{\pi \times 125\,000} \ln\left(\frac{26.6}{0.0028}\right) = 0.466 \text{ ms} \qquad (2)$$

That is 0.47 ms of delay (proportional to $1/F_O$ and Q).

Second, the PLL must acquire the signal, it must lock and settle. Acquisition time is statistical and may take any length of time, but average acquisition time depends on the loop filter components C_F and R_F and the difference in center frequencies, ΔF_O, of the TX/RX pair. Using the recommended C_F and R_F (47 nF and 6.2 kΩ) with a ±4.4% ΔF_O (a ± 100 mV DC offset on C_F and R_F), lock was measured to take less than 50 cycles of F_O. That is a 0.40 ms delay (proportional to $1/F_O$).

Acquisition is incomplete until the second order PLL loop settles. For the above-mentioned C_F and R_F, the loop natural frequency F_N and damping factor are found to be (reference 1) 2.3 kHz and 1.0 respectively. Settling to within ±25 mV of the ±100 mV DC offset change requires 2.7 periods of F_N, or 1.2 ms (a function of C_F and R_F).

Third, the RC lowpass filter introduces a 0.12 ms delay.

Fourth, C_M must charge up to ±(5%)100 = 83 mV depending on the polarity of F_O. Borderline data squaring with zero noise immunity is possible with only ±(5%) 50 mV of charging. C_M charge current is a linear and asymptotic function approximated by assuming a 50 μA charge current and a full 83 mV charge voltage. C_M charge time is then 1.7 ms (proportional to $1/F_{DATA}$).

Fifth, the impulse noise filter adds a ½ bit-time delay

Total T_{TR} is 3.9 ms plus ½ bit-time for a total of 1.9 bit-times at 360 Baud.

Receive-To-Transmit Switch-Over Time

Assume the chip has been in the RX mode and the TX mode is now selected. In less than 10 μs, full output current is exponentially building tank swing. 50% of full swing is achieved in less than 10 cycles - or under 80 μs at 125 kHz. In the same 10 μs that the output amp went on, the phase detector and loop filter are disconnected and the modulator input is enabled. FSK modulation is produced in 10 μs after switching to TX mode.

Power Line Impedance

Irrespective of how wide the limits on power line impedance Z_L are placed, there are no guarantees. However, since the CCT design requires an estimate of the lowest expected line impedance Z_{LN} encountered for the most efficient transmitter-to-line coupling, line impedance should be measured and Z_L limits fixed to a given confidence level. Resonable values for T_1 turns ratio, loaded Q, and tank resonant frequency pull F_Q may be found to enable a CCT system design that functions with the overwhelming majority of power lines.

A limited sampling of Z_L was made during the LM1893 design of residential and commercial 115 V 60 Hz power line. Data was also drawn from the research of Nicholson and Malack (reference 2), among others, to produce *Figures 26* and *27*. All measured impedances are contained within the shaded portions of *Figure 27*. A nominal 3.5, 7.0 and 14 Ω Z_{LN} is used throughout the application information with a nominal 45° phase (0° is sometimes used for simplicity).

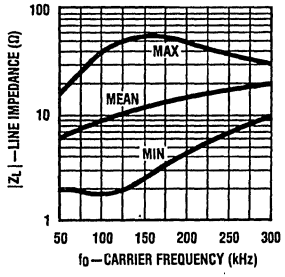


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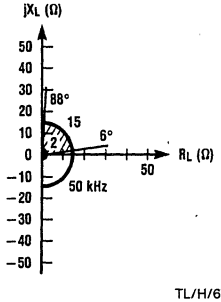
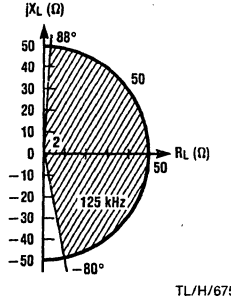
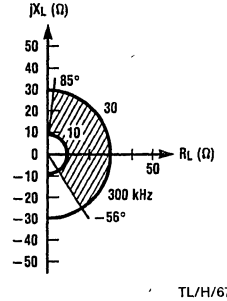
FIGURE 26. Measured line impedance range for residential and commercial 115V, 60 Hz lines



TL/H/6750-29



TL/H/6750-30



TL/H/6750-31

FIGURE 27. Complex-plane plots of measured 115V, 60 Hz line impedance where $Z_L = R_L + jX_L$

S 12

The Transmitter (Continued)

Power Line Attenuation

The wiring in most US buildings is a flat 3 conductor cable called Amerflex, BX, or Romex. All referenced line impedances refer to hot-to-neutral impedances with a grounded center conductor. The cable has a 100 Ω characteristic impedance, a 125 kHz quarter-wavelength of 600 m (250 m at 300 kHz), and a measured 7 dB attenuation for a 50 m run with a 10 Ω termination. Generally, line loads may be treated as lumped impedances. Instrument line cords exhibit about 0.7 μH and 30 pF per meter.

Limited tests of CCT link range using this chip show extensive coverage while remaining on one phase of a distribution transformer (100's of m) with link failure across transformer phases or through transformers unless coupling networks are utilized. Total line attenuation allowed from full signal to limiting sensitivity is more than 70 dB. Typically, signal is coupled across transformer phases by parasitic winding capacitance, typically giving 40 dB attenuation between phased 115 V windings. Coupling capacitors must be installed for link operation across phases. Power factor correcting capacitor banks on industrial lines or filter capacitors across the power lines of some electronic gear short carrier signal and should be isolated with inductors. Increasing range is sometimes accomplished by electing to install the isolating inductors and coupling capacitors, as well as by electing to use the boost option and by building repeaters.

The Coupling Transformer

The design arrived at for T_1 is the result of an unhappy compromise - but a workable one. The goals of 1) building T_1 with a stable resonant frequency, F_Q, that is little affected by the de-tuning effect of the line impedance Z_L, and of 2) building a tightly line-coupled transformer for transmitted carrier with loose coupling for transients, are somewhat mutually exclusive. The tradeoffs are exposed in the following pedagogue for the CCT designer attempting a new boost-capable or different core transformer design.

The compromises might be eliminated by separating the TX output and RX input. An untuned TX coupling transformer with only core coupling (not air-coupled solenoid windings) would employ a high permeability, high magnetic field, low loss, square saturating, toroidal core. The resonant RX path would be isolated from line-pull problems by a unilateral amplifier that operates at line voltages with much more than 110 dB of dynamic range. The solution is prohibitively complex and expensive, and is not used.

First, choose the turns ratio N based on an estimated lowest Z_L likely encountered, Z_{LN}. *Figure 28* shows graphically how N affects line signal. N should be as large as possible to drive Z_{LN} with full signal. If T_1 has an unloaded Q, Q_U, of well less than 35, a guess of N somewhat high should be used and later checked for accuracy. The recommended transformers have secondary taps giving a choice of N=7.07, 10, and 14.1 (nominally) for driving Z_{LN}'s of 14, 7.0, and 3.5 Ω respectively (at T_J = 25°C, V+ = 18V, and Q_U = 35).

The resonating inductance of the tuned primary, L_1, is sought. Note that, while standard transformer design gives a transformer self-inductance with an impedance at operating frequency well above load impedance, the tuned transformer requires a low L_1 for adequate Q_U and minimum line pull. Result: relatively poor mutual coupling.

$$L_1 = \frac{R}{2\pi F_O Q} \tag{3}$$

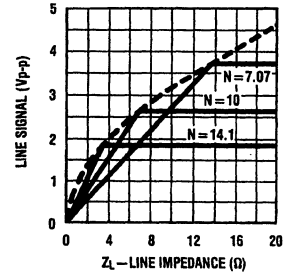


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FIGURE 28. Impressed line voltage for a given Z_L for each of the 3 taps available on the recommended transformers

It is known that resonant frequency $F_Q = F_O$ and some minimum bandwidth, or maximum Q, will be required to pass signal under full load conditions.

$$L_1 = \frac{R_Q \parallel |Z_{LN}|'}{2\pi F_O Q_L} \tag{4}$$

$|Z_{LN}|'$ is the reflected Z_{LN}, Q_L is the loaded Q, and parallel resistance R_Q models all transformer losses and sets Q_O.

$R_Q \parallel |Z_{LN}|'$ is found knowing that it absorbs full rated power.

$$P_O = I_O V_O = \frac{I_{OPP}}{2\sqrt{2}}\left[\frac{2(-V_{ALC}+V_+)}{2\sqrt{2}}\right] = \frac{(-4.7+V_+)I_O}{4} \tag{5}$$

where I_O is in App. at an elevated T_J

$$P_O = \frac{(18 - 4.7)\,0.06}{4} = 0.200\ \text{W} \tag{6}$$

$$R_Q \parallel |Z_{LN}|' = \frac{V_O^2}{P_O} = \frac{(-V_{ALC} + V_+)\sqrt{2}}{I_O} = 442\ \Omega \tag{7}$$

R_Q is found using Z_{LN} and the value for N found when assuming Q_U = 35.

$$|Z_{LN}|' = N^2 Z_{LN} = (7.07)^2\,13.9 = 695\ \Omega \tag{8}$$

$$R_Q = \frac{1}{\frac{1}{R_Q \parallel |Z_{LN}|'} - \frac{1}{|Z_{LN}|'}} = \frac{1}{\frac{1}{442} - \frac{1}{695}} = 1210\ \Omega \tag{9}$$

$$R_{QS} = \frac{R_Q}{1 + Q_U^2} = \frac{1210}{1 + 35^2} = 1\ \Omega \tag{10}$$

Only Q_L remains to be found to calculate L_1. Q_L is related to the −3 dB (half-power) bandwidth by

$$Q_L = \frac{1}{\text{BW (\% of } F_O)} \tag{11}$$

An iterative solution is forced where line pull, ΔF_Q, must be guessed to find Q_L and L_1. L_1 is then used to check the line pull guess; a large error requires a new guess. Try a BW of 8.7% - that is 4.4% for deviation, 1% for TC of F_O, and 3.3% for F_Q - giving Q_L = 11.5.

$$L_1 = \frac{442}{2\pi \times 125\,000 \times 11.5} = 49.0\ \mu\text{H}$$

Knowing the core inductance per turn, L, and L_1, the number of turns is found.

$$T_1 = \sqrt{\frac{L_1}{L}} = 49.0 = 49\ ½\ \text{turns} \tag{14}$$

T is normally an integer, but these transformers require so few turns that half-turns are specified, remembering that the remaining ½ turn is completed on the P.C. board and is loosely coupled. The secondary turns are calculated

The Transmitter (Continued)

$$T_2 = \frac{T_1}{N} = \frac{49.5}{7.07} = 7.00 = 7 \text{ turns} \quad (15)$$

giving an L_2 of 0.98 μH. Note that the recommended 125 kHz transformer mirrors these specifications. The resonating capacitor is

$$C_Q = \frac{1}{(2\pi F_Q)^2 L_1} = 33.1 \times 10^{-9} = 33 \text{ nF} \quad (16)$$

Line pull ΔF_Q was calculated (reference 5) for a Z_L magnitude of 14Ω and up with any phase angle from $-90°$ to 90°. ΔF_Q was 6.4% - well above the 3.3% estimate. Referring to (11), an 11.8% bandwidth is required, forcing L_1 to be reduced to reduce Q. That fix was not implemented; some signal attenuation under worst-case drift and ΔF_Q is allowed. L_1 is already so small that the 31 gauge winding conducts a ¼ A_{RMS} circulating current.

Line Carrier Detection

While the addition of a carrier detection circuit (for a mute or squelch function) will only decrease receiver ultimate sensitivity, there is sometimes good reason to employ it to free the controller from watching for RX signal when no carrier is incoming, or to employ it to reduce the probability of line collisions (when multiple transmitters operate simultaneously to cause one or more transmissions to fail). Unless the detector is heavily filtered or uses a high carrier amplitude threshold, there will be false outputs that force the controller to have Data Out data checking capability just as is required when using no carrier detector. If false triggering is minimized, the probability of line collisions is increased due to the inability to sense low carrier amplitudes and because of sense delay. The property of the LM1893 to change output state infrequently (although the polarity is undefined) when in the RX mode, even with no incoming carrier, reduces the desire to implement carrier detection and preserves the full ultimate sensitivity. Also, many impulse-noise insensitive transmission schemes, like handshaking, are easily modified to recover from line collisions.

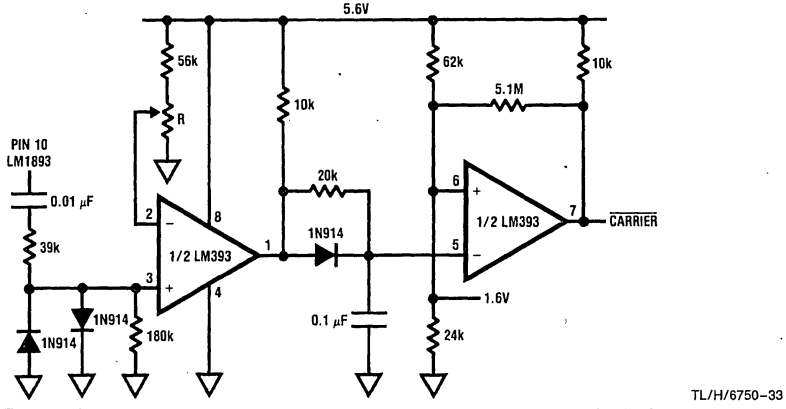


FIGURE 29. A simple carrier amplitude detector with output low when carrier is detected

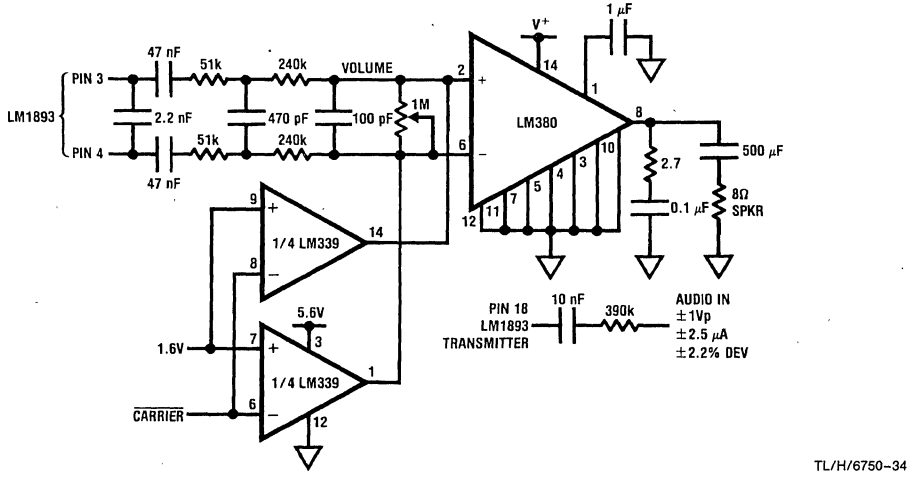


FIGURE 30. A simple linear analog audio transmitter and receiver are shown. The carrier and 1.6V inputs are derived from the carrier detector of *Figure 29*. The remaining 2 LM339 comparators may be used to build the carrier detector circuit.

Line Carrier Detection (Continued)

Figure 29 shows a low cost carrier amplitude detection circuit. Pot. R gives a variable threshold; R may be replaced by a fixed resister when the threshold has been chosen. A 150Ω R gives a 10 mV_{RMS} threshold. The circuit exhibits a 1 ms delay and a 2 ms off delay. Minimize the capacitance of the node including pin 3, especially for operation a high carrier frequencies.

Audio Transmission

The LM1893 is designed to allow analog data transmission and reception. Base-band audio-bandwidth signals FM modulate the carrier passing through the tuned transformer (placing a limit on the usable percent modulation) onto the power line to be linearly demodulated by the receiver PLL. Because the receiver data path beyond the phase detector will pass only digital signal, external audio filtering and amplification is required. *Figure 30* shows a very simple audio transmitter and receiver circuit utilizing a carrier detection mute circuit. A single LM339 quad. comparator may be used to build the carrier detect and mute. Filter bandwidth is held to a minimum to minimize noise, especially line-related correlated noise.

Data Encoding

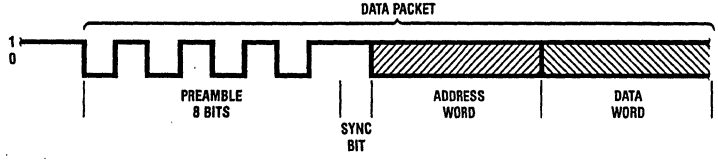
At the beginning of a received transmission, the first 0 to 2 bits may be lost while the chip's receiver settles to the DC bias point required for the given transmitter/receiver pair carrier frequency offset. With proper data encoding, dropped start bits can be tolerated and correct communication can take place. One recommended data encoding scheme is now discussed.

Generally, a CCT system consists of many transceivers that normally listen to the line at all times (or during predetermined time windows), waiting for a transmission that directs one or more of the receivers to operate. If any receiver finds its address in the transmitted data packet, further action such as handshaking with the transmitter is initiated. The receiver might tell the transmitter, via retransmission, that it received this data, waiting for acknowledgement before acting on the received command. Error detecting and correcting codes may be employed throughout. The transmitter must have the capability to retransmit after a time if no response from the receiver is heard - under the assumption that the receiver didn't detect its address because of noise, or that the response was missed because of noise or a line collision. (A line collision happens when more than 1 transmitter operates at one time - causing one or more of the communications to fail). After many re-transmissions the transmitter might choose to give up. Collision recovery is achieved by waiting some variable amount of time before retransmission, using a random number of bits delay or a delay based on each transmitter's address, since each transceiver has a unique address.

An example recommended transmission data packet is shown in *Figure 31*. The 8 bit 50% duty-cycle preamble is long enough to allow receiver biasing with enough bits left over to allow the receiver controller to detect the square-wave that signals the start of a transmission. If there had been no transmission for some time, the receiver would simply need to note that a data transition had occurred and begin its watch for a square-wave. If the receive controller detected the alternating-polarity data square-wave it would then use the sync. bit to signal that the address and data were immediately following. The address data would then be loaded, assuming the fixed format, and tested against its own. If the address was correct, the receiver would then load and store the data. If the address was not correct, either the transmission was not meant for this receiver or noise has fooled the receiver. In the former case, when the transmission was not meant for the receiver, the controller should immediately return to watching the incoming data for its address. If the later case were true, then the receive controller would continue to detect edges, tieing itself up by loading false data and being forced to handshake. The square-wave detection and address load and check routines should be fast to minimize the time spent in loops after being false-triggered by noise. If the controller detects an error (a received data packet that does not conform to the pre-defined encoding format) it should immediately resume watching the LM1893's Data Out for transmissions. Best receiver operation is obtained when the receive controller has the ability to store all incoming data in a shift register the length of a data packet. The controller would then check the whole packet for proper format. If the test failed, the next bit would be shifted in and the process repeated. Every possible incoming bit sequence would then be checked and dead time reduced.

A line-synchronous CCT system passing 3 bits per half-cycle may replace the long 8 bit preamble and sync pulse with a 2 bit start-of-transmission bias preamble. The receive controller might then assume that preamble always starts after bit 1 (the first bit after zero-crossing) so that any data transition at a zero crossing must be the start of the address bits and is tested as such. The line synchronous receiver operates with a simpler controller than an asynchronous system.

Discussion has assumed that the controller has always known when the Data Out is high or low. The controller must sample at the proper time to check the Data Out state. Since noise shows itself as pulse width jitter, symmetrically placed about the no-noise switch-points, optimum Data Out sampling is done in the center of the received data pulse. The receive data path has a time delay that, at low data rates, is dominated by the impulse noise filter integrator and is nominally ½ bit (¼ to 1 bit over tolerance and temperature). At a 2 kHz data rate, an additional delay of approximately $\frac{1}{10}$ bit is added because of the cumulative delay of

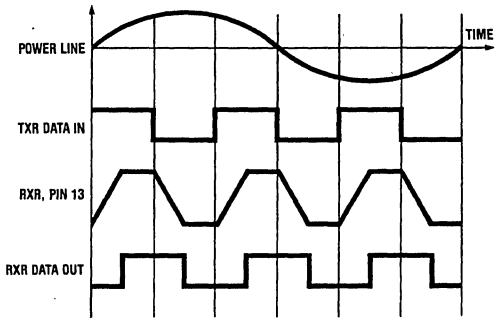


TL/H/6750–35

FIGURE 31. A recommended encoded data packet, generated by the transmit controller is shown. The horizontal axis is time where 1 bit time is $1/(2F_{DATA})$

Audio Transmission (Continued)

the remainder of the receiver. *Figure 32* shows that Data Out sampling occurs conveniently at the transmitted data edges for the line synchronous data transmission scheme mentioned in the previous paragraph. With the asynchronous system suggested, the receive controller must sample the Data Out pin often to determine, with several bits of



TL/H/6750–36

FIGURE 32. Operating waveforms of a line-synchronized transceiver pair are shown. The diagram shows how the transmitted data transitions may be used as received data sampling points

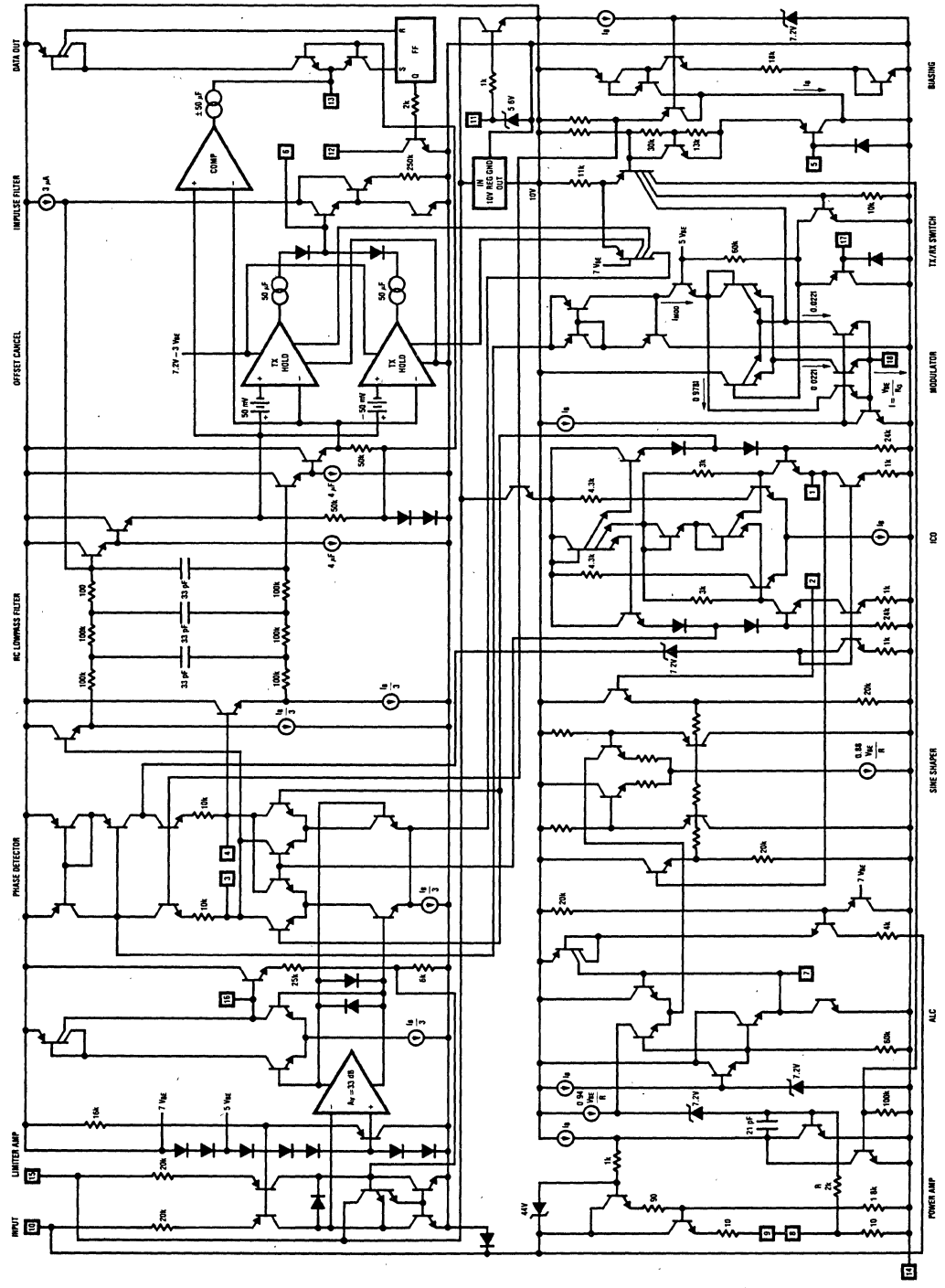
accuracy, where the square-wave data transitions take place, average their positions assuming a known data rate, and calculate where the center of the data bits are and will continue to be as the address and data are read. A long preamble is helpful. Software that continuously updates the center-of-bit time estimate, as address and data are received, works even better. Alternatively, a coding scheme employing an embedded clock can be used.

A line-synchronous system using the LM1893 and COPS™ controller that transmits data packets with a start-of-transmission signal, address word, and data word has been built. Handshaking routines are employed that have proven to be very effective - no false operation or AC lines has ever been observed. Covered range, while operating in residential environs, is excellent. Operation in commercial and, especially, industrial buildings may be limited because of low line impedance and high noise levels unless the boost option, inductive isolation of capacitors, and capacitive transformer bridging are resorted too.

References:

1. Gray, Paul R. and Robert G. Meyer; "Analysis and Design of Integrated Circuits;" John Wiley and Sons; 1977; pp. 575–593; (Phase-Locked Loop tutorial)
2. Nicholson, J.R. and J.A. Malack; "RF Impedance of Power Lines and Line Impedance Stabilization Network in Conducted Interference Measurements;" IEEE Transactions on Electromagnetic Compatibility; May 1973; (line impedance data)
3. Southwick, R.A.; "Impedance Characteristics of Single-Phase Power Lines;" Conference Rec.; 1973 IEEE Int. Symp. on Electromagnetic Compatibility; (line impedance data)
4. Hayt, William H. Jr. and Jack E. Kemmerly; "Engineering Circuit Analysis;" McGraw-Hill Books; 1971; pp. 447–453; (linear transformer reflected impedance)
5. FCC, "Notice of Proposed Rule Making," Docket 20780, adopted Apr. 14, 1976, (Proposed regulation)
6. Monticelli, Dennis M. and Michael E. Wright; "A Carrier Current Transceiver IC for Data Transmission Over the AC Power Lines;" IEEE J. Solid-State Circuits; vol. SC-17; Dec. 1982; pp. 1158-1165; (LM1893 circuit description)
7. Lee, Mitchell; "A New Carrier Current Transceiver IC;" IEEE Trans. on Consumer Electronics; vol. CE-28; Aug. 1982; pp. 409–414; (Application of LM1893)

Simplified Schematic



National Semiconductor

LM1949 Injector Drive Controller

General Description

The LM1949 linear integrated circuit serves as an excellent control of fuel injector drive circuitry in modern automotive systems. The IC is designed to control an external power NPN Darlington transistor that drives the high current injector solenoid. The current required to open a solenoid is several times greater than the current necessary to merely hold it open; therefore, the LM1949, by directly sensing the actual solenoid current, initially saturates the driver until the "peak" injector current is four times that of the idle or "holding" current (*Figure 3-Figure 7*). This guarantees opening of the injector. The current is then automatically reduced to the sufficient holding level for the duration of the input pulse. In this way, the total power consumed by the system is dramatically reduced. Also, a higher degree of correlation of fuel to the input voltage pulse (or duty cycle) is achieved, since opening and closing delays of the solenoid will be reduced.

Normally powered from a 5-volt ±10% supply, the IC is typically operable over the entire temperature range (−55°C to +125°C ambient) with supplies as low as 3 volts. This is particularly useful under "cold crank" conditions when the battery voltage may drop low enough to deregulate the 5-volt power supply.

The LM1949 is available in the plastic miniDIP, (contact factory for other package options).

Features

- Low voltage supply (3V-5.5V)
- 22 mA output drive current
- No RFI radiation
- Adaptable to all injector current levels
- Highly accurate operation
- TTL/CMOS compatible input logic levels
- Short circuit protection
- High impedance input
- Externally set holding current, I_H
- Internally set peak current ($4 \times I_H$)
- Externally set time-out
- Can be modified for full switching operation
- Available in plastic 8-pin miniDIP

Applications

- Fuel injection
- Throttle body injection
- Solenoid controls
- Air and fluid valves
- DC motor drives

Typical Application Circuit

Order Number LM1949N
NS Package Number N08B

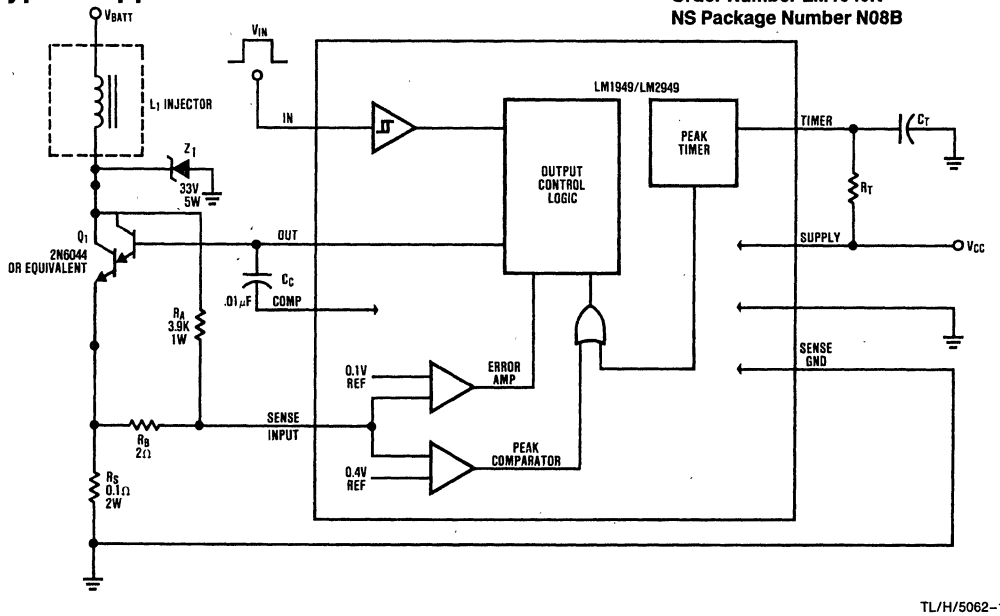


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FIGURE 1. Typical Application and Test Circuit

Absolute Maximum Ratings

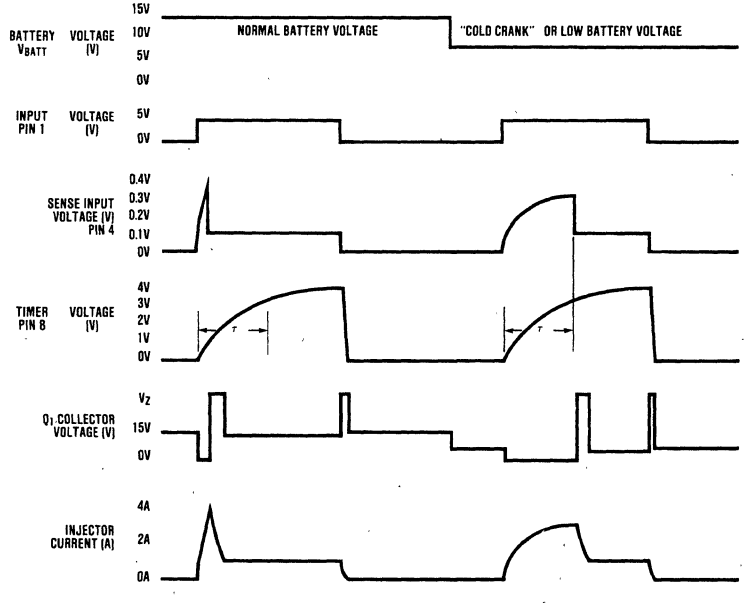
Supply Voltage	8V	Storage Temperature Range	−65°C to +150°C
Power Dissipation (Note 1)	360 mW	Junction Temperature	150°C
Input Voltage Range	−0.3V to V_{CC}	Lead Temp. (Soldering 10 Seconds)	300°C
Operating Temperature Range	−40°C to +125°C		

Electrical Characteristics (V_{CC} = 5.5V, V_{IN} = 2.4V, T_j = 25°C, *Figure 1*, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current					
	Off	V_{IN} = 0V		11	23	mA
	Peak	Pin 8 = 0V		28	54	mA
	Hold	Pin 8 Open		16	26	mA
V_{OH}	Input On Level	V_{CC} = 5.5V		1.4	2.4	V
		V_{CC} = 3.0V		1.2	1.6	V
V_{OL}	Input Off Level	V_{CC} = 5.5V	1.0	1.35		V
		V_{CC} = 3.0V	0.7	1.15		V
I_B	Input Current		−25	3	+25	μA
I_{OP}	Output Current					
	Peak	Pin 8 = 0V	−10	−22		mA
	Hold	Pin 8 Open	−1.5	−5		mA
V_S	Output Saturation Voltage	10 mA, V_{IN} = 0V		0.2	0.4	V
	Sense Input					
V_p	Peak Threshold	V_{CC} = 4.75V	350	386	415	mV
V_H	Hold Reference		88	94	102	mV
t	Time-out, t	$t \div R_T C_T$	90	100	110	%

NOTE 1: Thermal resistance from junction to ambient is typically 110°C/W for the N-package.

Typical Circuit Waveforms



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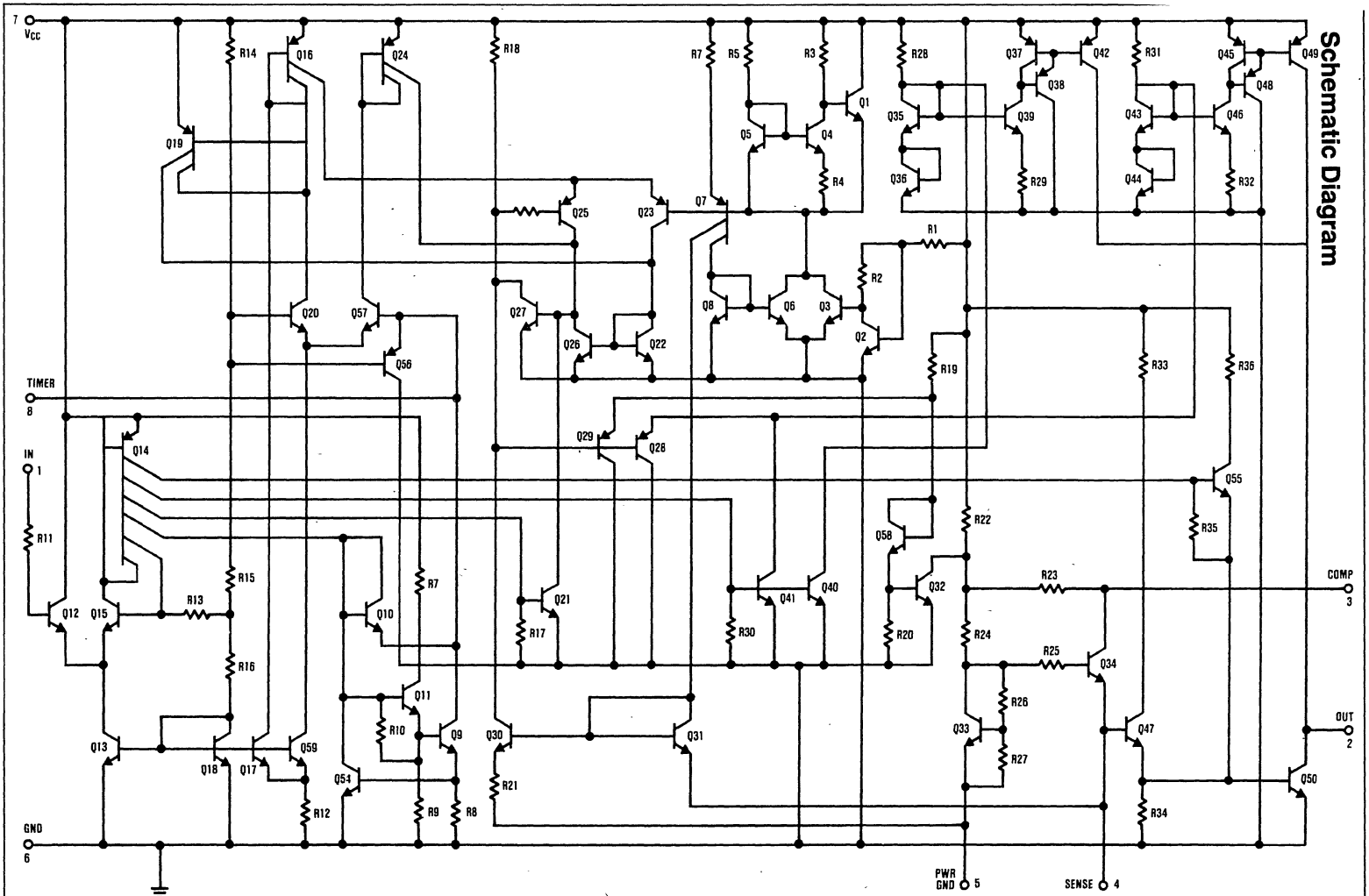

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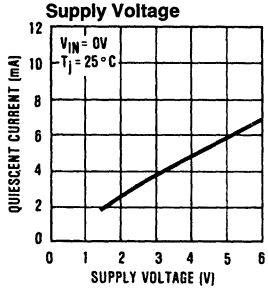
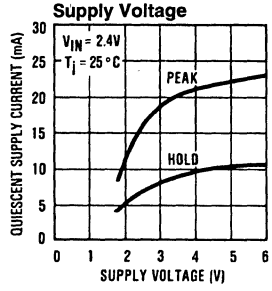
FIGURE 2. LM1949 Circuit

Typical Performance Characteristics

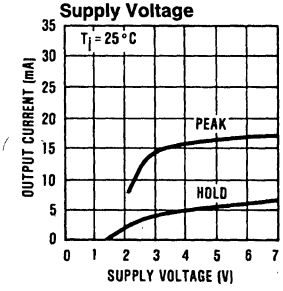
Quiescent Current vs Supply Voltage



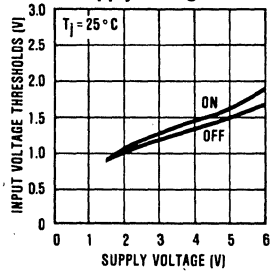
Supply Current vs Supply Voltage



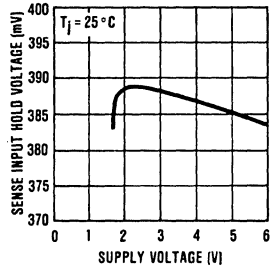
Output Current vs Supply Voltage



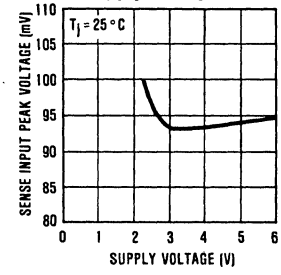
Input Voltage Thresholds vs Supply Voltage



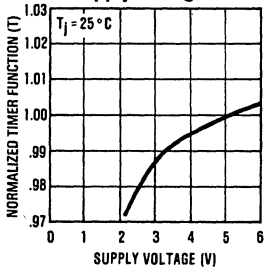
Sense Input Peak Voltage vs Supply Voltage



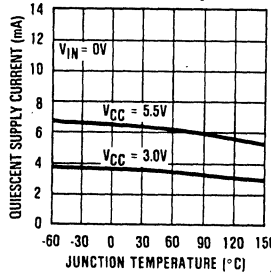
Sense Input Hold Voltage vs Supply Voltage



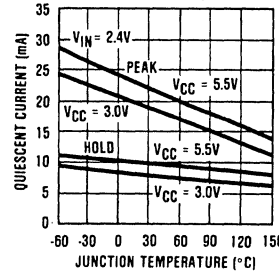
Normalized Timer Function vs Supply Voltage



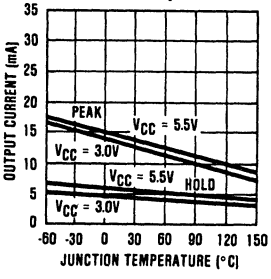
Quiescent Supply Current vs Junction Temperature



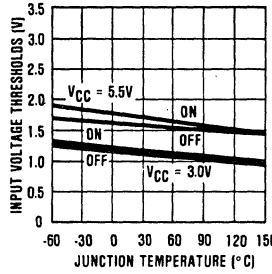
Quiescent Supply Current vs Junction Temperature



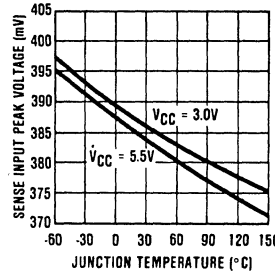
Output Current vs Junction Temperature



Input Voltage Thresholds vs Junction Temperature



Sense Input Peak Voltage vs Junction Temperature



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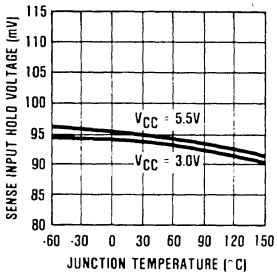
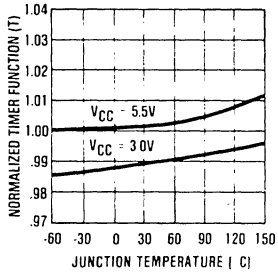
Typical Performance Characteristics (Continued)

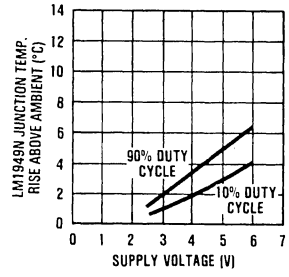
Sense Input Hold Voltage vs Junction Temperature



Normalized Timer Function vs Junction Temperature



LM1949N Junction Temperature Rise Above Ambient vs Supply Voltage



TL/H/5062–5

Application Hints

The injector driver integrated circuits were designed to be used in conjunction with an external controller. The LM1949 derives its input signal from either a control oriented processor (COPS™), microprocessor, or some other system. This input signal, in the form of a square wave with a variable duty cycle and/or variable frequency, is applied to Pin 1. In a typical system, input frequency is proportional to engine RPM. Duty cycle is proportional to the engine load. The circuits discussed are suitable for use in either open or closed loop systems. In closed loop systems, the engine exhaust is monitored and the air-to-fuel mixture is varied (via the duty cycle) to maintain a perfect, or stochiometric, ratio.

INJECTORS

Injectors and solenoids are available in a vast array of sizes and characteristics. Therefore, it is necessary to be able to design a drive system to suit each type of solenoid. The purpose of this section is to enable any system designer to use and modify the LM1949 and associated circuitry to meet his/her system specifications.

Fuel injectors can usually be modeled by a simple RL circuit. *Figure 3* shows such a model for a typical fuel injector. In actual operation, the value of L_1 will depend upon the status of the solenoid. In other words, L_1 will change depending

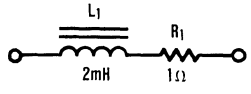


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FIGURE 3. Model of a Typical Fuel Injector

upon whether the solenoid is open or closed. This effect, if pronounced enough, can be a valuable aid in determining the current necessary to open a particular type of injector. The change in inductance manifests itself as a breakpoint in the initial rise of solenoid current. The waveforms on Page 2 at the sense input show this occurring at approximately 130 mV. Thus, the current necessary to overcome the constrictive forces of that particular injector is 1.3 amperes.

PEAK AND HOLD CURRENTS

The peak and hold currents are determined by the value of the sense resistor R_S. The driver IC, when initiated by a logic 1 signal at Pin 1, initially drives Darlington transistor Q_1 into saturation. The injector current will rise exponentially from zero at a rate dependent upon L_1, R_1, the battery voltage and the saturation voltage of Q_1. The drop across the sense resistor is created by the solenoid current, and when this drop reaches the peak threshold level, typically 385 mV, the IC is tripped from the peak state into the hold state. The IC now behaves more as an op amp and drives Q_1 within a closed loop system to maintain the hold reference voltage, typically 94 mV, across R_S. Once the injector current drops from the peak level to the hold level, it remains there for the duration of the input signal at Pin 1. This mode of operation is preferable when working with solenoids, since the current required to overcome kinetic and constriction forces is often a factor of four or more times the current necessary to hold the injector open. By holding the injector current at one fourth of the peak current, power dissipation in the solenoids and Q_1 is reduced by at least the same factor.

In the circuit of *Figure 1*, it was known that the type of injector shown opens when the current exceeds 1.3 amps and closes when the current then falls below 0.3 amps. In order to guarantee injector operation over the life and temperature range of the system, a peak current of approximately 4 amps was chosen. This led to a value of R_S of 0.1Ω. Dividing the peak and hold thresholds by this factor gives peak and hold currents through the solenoid of 3.85 amps and 0.94 amps respectively.

Different types of solenoids may require different values of current. The sense resistor R_S may be changed accordingly. An 8-amp peak injector would use R_S equal to .05Ω, etc. Note that for large currents above one amp, IR drops within the component leads or printed circuit board may create substantial errors unless appropriate care is taken. The sense input and sense ground leads (Pins 4 and 5 respectively), should be Kelvin connected to R_S. High current should not be allowed to flow through any part of these traces or connections. An easy solution to this problem on double-sided PC boards (without plated-through holes) is to have the high current trace and sense trace attach to the R_S lead from opposite sides of the board.

TIMER FUNCTION

The purpose of the timer function is to limit the power dissipated by the injector or solenoid under certain conditions. Specifically, when the battery voltage is low due to engine cranking, or just undercharged, there may not be sufficient voltage available for the injector to achieve the peak current. In the *Figure 2* waveforms under the low battery condition, the injector current can be seen to be leveling out at 3

Timer Function (Continued)

amps, or 1 amp below the normal threshold. Since continuous operation at 3 amps may overheat the injectors, the timer function on the IC will force the transition into the hold state after one time constant (the time constant is equal to R_TC_T). The timer is reset at the end of each input pulse. For systems where the timer function is not needed, it can be disabled by grounding Pin 8. For systems where the initial peak state is not required, (i.e., where the solenoid current rises immediately to the hold level), the timer can be used to disable the peak function. This is done by setting the time constant equal to zero, (i.e., $C_T = 0$). Leaving R_T in place is recommended. The timer will then complete its time-out and disable the peak condition before the solenoid current has had a chance to rise above the hold level.

The actual range of the timer in injection systems will probably never vary much from the 3.9 milliseconds shown in *Figure 1*. However, the actual useful range of the timer extends from microseconds to seconds, depending on the component values chosen. The useful range of R_T is approximately 1k to 240k. The capacitor C_T is limited only by stray capacitances for low values and by leakages for large values.

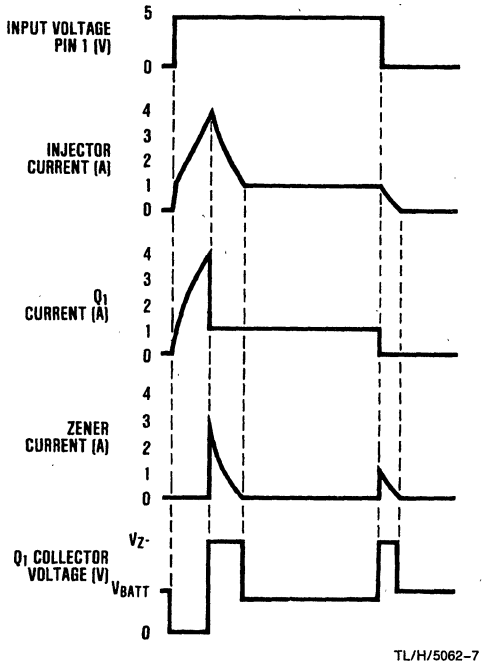
The capacitor reset time at the end of each controller pulse is determined by the supply voltage and the capacitor value. The IC resets the capacitor to an initial voltage (V_{BE}) by discharging it with a current of approximately 15 mA. Thus, a 0.1 μF cap is reset in approximately 25 μs.

COMPENSATION

Compensation of the error amplifier provides stability for the circuit during the hold state. External compensation (from Pin 2 to Pin 3) allows each design to be tailored for the characteristics of the system and/or type of Darlington power device used. In the vast majority of designs, the value or type of the compensation capacitor is not critical. Values of 100 pF to 0.1 μF work well with the circuit of *Figure 1*. The value shown of .01 μF (disc) provides a close optimum in choice between economy, speed, and noise immunity. In some systems, increased phase and gain margin may be acquired by bypassing the collector of Q_1 to ground with an appropriately rated 0.1 μF capacitor. This is, however, rarely necessary.

FLYBACK ZENER

The purpose of zener Z_1 is twofold. Since the load is inductive, a voltage spike is produced at the collector of Q_1 anytime the injector current is reduced. This occurs at the peak-to-hold transition, (when the current is reduced to one fourth of its peak value), and also at the end of each input pulse, (when the current is reduced to zero). The zener provides a current path for the inductive kickback, limiting the voltage spike to the zener value and preventing Q_1 from damaging voltage levels. Thus, the rated zener voltage at the system peak current must be less than the guaranteed minimum breakdown of Q_1. Also, even while Z_1 is conducting the majority of the injector current during the peak-to-hold transition (see *Figure 4*), Q_1 is operating at the hold current level. This fact is easily overlooked and, as described in the following text, can be corrected if necessary. Since the error amplifier in the IC demands 94 mV across R_S, Q_1 will be biased to provide exactly that. Thus, the safe operating area (SOA) of Q_1 must include the hold current with a V_{CE} of Z_1 volts. For systems where this is not desired, the zener anode may be reconnected to the top of R_S as shown in *Figure 5*. Since the voltage across the sense resistor now accurately portrays the injector current at all times, the error

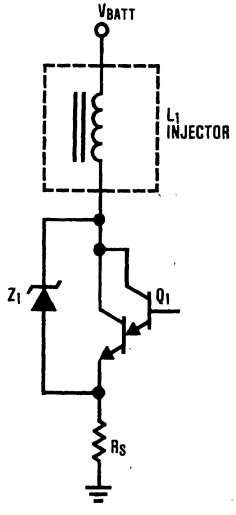


TL/H/5062–7

FIGURE 4. Circuit Waveforms

amplifier keeps Q_1 off until the injector current has decayed to the proper value. The disadvantage of this particular configuration is that the ungrounded zener is more difficult to heat sink if that becomes necessary.

The second purpose of Z_1 is to provide system transient protection. Automotive systems are susceptible to a vast array of voltage transients on the battery line. Though their duration is usually only milliseconds long, Q_1 could suffer permanent damage unless buffered by the injector and Z_1. This is one reason why a zener is preferred over a clamp diode back to the battery line, the other reason being long decay times.



TL/H/5062–8

FIGURE 5. Alternate Configuration for Zener Z_1

POWER DISSIPATION

The power dissipation of the system shown in *Figure 1* is dependent upon several external factors, including the frequency and duty cycle of the input waveform to Pin 1. Calculations are made more difficult since there are many discontinuities and breakpoints in the power waveforms of the various components, most notably at the peak-to-hold transition. Some generalizations can be made for normal operation. For example, in a typical cycle of operation, the majority of dissipation occurs during the hold state. The hold state is usually much longer than the peak state, and in the peak state nearly all power is stored as energy in the magnetic field of the injector, later to be dumped mostly through the zener. While this assumption is less accurate in the case of low battery voltage, it nevertheless gives an unexpectedly accurate set of approximations for general operation.

The following nomenclature refers to *Figure 1*. Typical values are given in parentheses:

R_S = Sense Resistor (0.1Ω)
V_H = Sense Input Hold Voltage (.094V)
V_p = Sense Input Peak Voltage (.385V)
V_Z = Z_1 Zener Breakdown Voltage (33V)
V_{BATT} = Battery Voltage (14V)
L_1 = Injector Inductance (.002H)
R_1 = Injector Resistance (1Ω)
n = Duty Cycle of Input Voltage of Pin 1 (0 to 1)
f = Frequency of Input (10Hz to 200Hz)

Q_1 Power Dissipation:

$$P_Q \approx n \bullet V_{BATT} \bullet \frac{V_H}{R_S} \text{ Watts}$$

Zener Dissipation:

$$P_Z \approx V_Z \bullet L_1 \bullet f \bullet \frac{(V_P^2 + V_H^2)}{((V_Z - V_{BATT}) \bullet R_S^2)} \text{ Watts}$$

Injector Dissipation:

$$P_I \approx n \bullet R_1 \bullet \frac{V_H^2}{R_S^2} \text{ Watts}$$

Sense Resistor:

$$P_R \approx n \frac{V_H^2}{R_S^2} \text{ Watts}$$

$$P_R \text{ (worst case)} \approx n \frac{V_P^2}{R_S^2} \text{ Watts}$$

SWITCHING INJECTOR DRIVER CIRCUIT

The power dissipation of the system, and especially of Q_1, can be reduced by employing a switching injector driver circuit. Since the injector load is mainly inductive, transistor Q_1 can be rapidly switched on and off in a manner similar to switching regulators. The solenoid inductance will naturally integrate the voltage to produce the required injector current, while the power consumed by Q_1 will be reduced. A note of caution: The large amplitude switching voltages that are present on the injector can and do generate a tremendous amount of radio frequency interference (RFI). Because of this, switching circuits are not recommended. The extra cost of shielding can easily exceed the savings of reduced power. In systems where switching circuits are mandatory, extensive field testing is required to guarantee that RFI cannot create problems with engine control or entertainment equipment within the vicinity.

The LM1949 can be easily modified to function as switchers. Accomplished with the circuit of *Figures 6* and *7*, the only additional components required are two external resistors, R_A and R_B. Additionally, the zener needs to be reconnected, as shown, to R_S. The amount of ripple on the hold current is easily controlled by the resistor ratio of R_A to R_B. R_B is kept small so that sense input bias current (typically 0.3 mA) has negligible effect on V_H. Duty cycle and frequency of oscillation during the hold state are dependent on the injector characteristics, R_A, R_B, and the zener voltage as shown in the following equations.

$$\text{Hold Current} \approx \frac{V_H}{R_S}$$

$$\text{Minimum Hold Current} \approx \frac{\left(V_H - \frac{R_B}{R_A} \bullet V_Z\right)}{R_S}$$

$$\text{Ripple or } \Delta I \text{ Hold} \approx \frac{R_B}{R_A} \bullet V_Z \bullet \frac{1}{R_S}$$

$$f_o \approx \frac{R_S}{L_1} \bullet \frac{R_A}{R_B} \bullet \frac{V_{BATT}}{V_Z} \bullet \left(1 - \frac{V_{BATT}}{V_Z}\right)$$

f_o = Hold State Oscillation Frequency

$$\text{Duty Cycle of } f_o \approx \frac{V_{BATT}}{V_Z}$$

Component Power Dissipation

$$P_Q \approx n \bullet \left(1 - \frac{V_{BATT}}{V_Z}\right) \bullet \frac{V_{SAT}}{R_S} \bullet V_H$$

V_{SAT} = Q_1 Saturation Volt @ ~ 1 Amp (1.5V)

$$P_Z \approx n \bullet \frac{V_{BATT} \bullet V_H}{R_S}$$

$$P_{RA} \approx \frac{V_B \bullet V_Z}{R_1}$$

As shown, the power dissipation by Q_1 in this manner is substantially reduced. Measurements made with a thermocouple on the bench indicated better than a fourfold reduction in power in Q_1. However, the power dissipation of the zener (which is independent of the zener voltage chosen) is increased over the circuit of *Figure 1*.

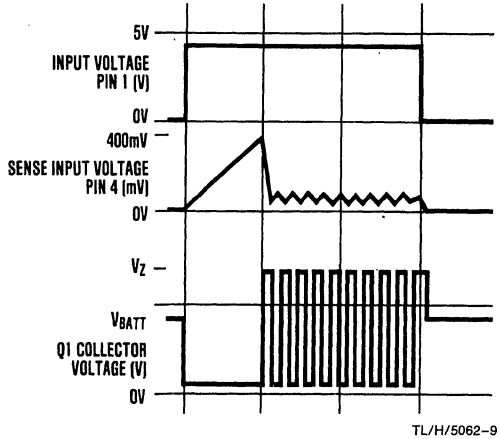


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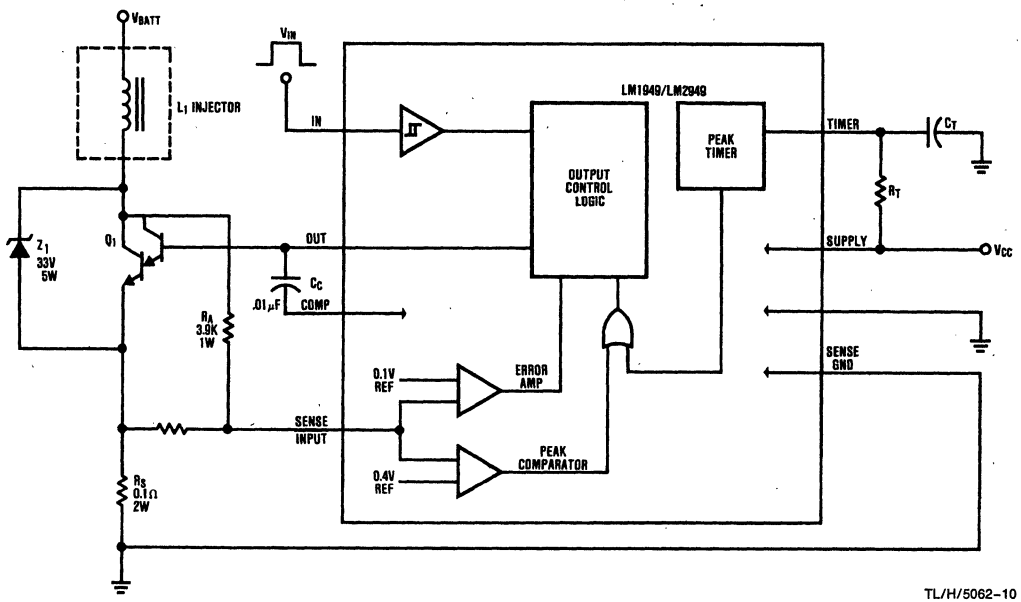
FIGURE 7. Switching Waveforms



TL/H/5062–10

FIGURE 6. Switching Application Circuit

National Semiconductor

PRELIMINARY

LM1964 Sensor Interface Amplifier

General Description

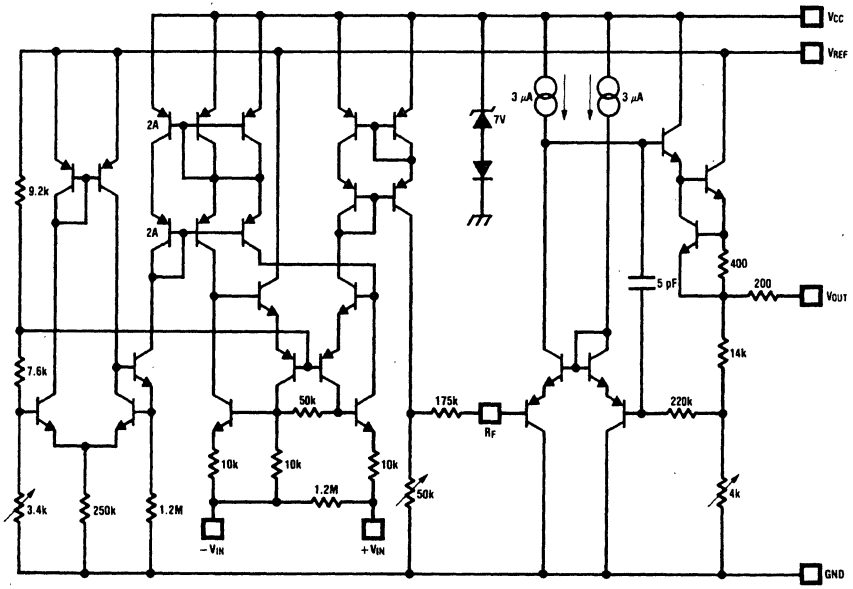
The LM1964 is a precision differential amplifier specifically designed for operation in the automotive environment. Gain accuracy is guaranteed over the entire automotive temperature range (−40°C to +125°C) and is factory trimmed prior to package assembly. The input circuitry has been specifically designed to reject common-mode signals as much as 3V below ground on a single positive power supply. This facilitates the use of sensors which are grounded at the engine block while the LM1964 itself is grounded at chassis potential. An external capacitor sets the maximum operating frequency of the amplifier, thereby filtering high frequency transients. Both inputs are protected against accidental shorting to the battery and against load dump transients. The input impedance is typically 1 MΩ

The output op amp is capable of driving capacitive loads and is fully protected. Also, internal circuitry has been provided to detect open circuit conditions on either or both inputs and force the output to a "home" position (a ratio of the external reference voltage).

Features

- Normal circuit operation guaranteed with inputs up to 3V below ground on a single supply
- Gain factory trimmed and guaranteed over temperature (±3% of full-scale from −40°C to +125°C)
- Low power consumption (typically 1 mA)
- Fully protected inputs
- Input open circuit detection
- Operation guaranteed over the entire automotive temperature range (−40°C to +125°C)
- Single supply operation

Schematic and Connection Diagrams



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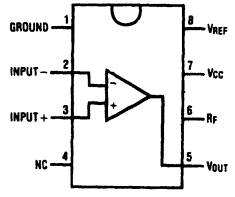
Dual-In-Line Package



TL/H/6744–2

Top View

Order Number LM1964N
NS Package Number N08E

Absolute Maximum Ratings

V_{CC} Supply Voltage (RV_{CC} = 15 kΩ)	±60V	Output Short Circuit Duration	Indefinite
V_{REF} Supply Voltage	−0.3V to +6V	Operating Temperature Range	−40°C to +125°C
DC Input Voltage (Either Input)	−3V to +16V	Storage Temperature Range	−65°C to +150°C
Input Transients (Note 1)	±60V	Lead Temperature (Soldering, 10 Seconds)	+280°C

Electrical Characteristics V_{CC} = 12V, V_{REF} = 5V, T_A = 25°C unless otherwise noted

Parameter	Conditions	(Note 2)			(Note 3)			Units
		Min	Typ	Max	Min	Typ	Max	
Differential Voltage Gain	V_{DIF}=0.5V −1V≤V_{CM}≤+1V	4.41	4.50	4.59				V/V
	V_{DIF}=0.5V, −40°C≤T_A≤125°C −3V≤V_{CM}≤+1V				4.36	4.50	4.64	V/V
Gain Error (Note 5)	0≤V_{DIF}≤1V −1V≤V_{CM}≤+1V	−2	0	2				%/FS
	0≤V_{DIF}≤1V −3V≤V_{CM}≤+1V −40°C≤T_A≤+125°C				−3	0	3	%/FS
Differential Input Resistance	o≤V_{DIF}≤1V −1V≤V_{CM}≤+1V	1.00	1.20					MΩ
	0≤V_{DIF}≤1V −3V≤V_{CM}≤+1V −40°C≤T_A+125°C				0.70	1.20		MΩ
Non-Inverting Input Bias Current	0≤V_{DIF}≤1V −1V≤V_{CM}≤+1V		0.3	1.0				μA
	0≤V_{DIF}≤1V −3V≤V_{CM}≤+1V −40°C≤T_A≤+125°C					0.3	1.5	μA
Inverting Input Bias Current	0≤V_{DIF}≤1V −1V≤V_{CM}≤+1V		45	100				μA
	0V≤V_{DIF}≤1V −3V≤V_{CM}≤+1V −40°C≤T_A≤+125°C					45	150	μA
V_{CC} Supply Current	V_{CC}=12V, RV_{CC}=15k		300	500				μA
V_{REF} Supply Current	4.75V≤V_{REF}≤5.5V		0.5	1.0				mA
Common-Mode Voltage Range (Note 4)	−40°C≤T_A≤+125°C	−1		1	−3		1	V
DC Common-Mode Rejection Ratio	Input Referred −1V≤V_{CM}≤+1V V_{DIF}=0.5V	50	60					dB
Open Circuit Output Voltage	One or Both Inputs Open, −1V≤V_{CM}≤+1V	0.371	0.397	0.423				XV_{REF}
	−3V≤V_{CM}≤+1V −40°C≤T_A≤+125°C				0.365	0.397	0.429	XV_{REF}
Short Circuit Output Current	Output Grounded	1.0	2.7	5.0				mA
V_{CC} Power Supply Rejection Ratio	V_{CC}=12V, RV_{CC}=15K V_{DIF}=0.5V	50	65					dB
V_{REF} Power Supply Rejection Ratio	V_{REF}=5 V_{DC} V_{DIF}=0.5V	60	74					dB

Note 1: This test is performed with a 1000Ω source impedance.

Note 2: These parameters are guaranteed and 100% production tested.

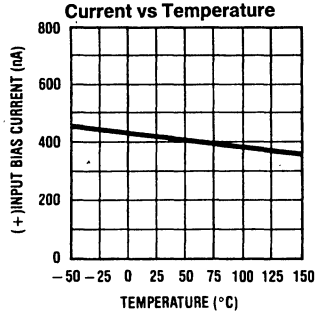
Note 3: These parameters will be guaranteed but not 100% production tested.

Note 4: The LM1964 has been designed to common-mode to −3V, but production testing is only performed at ±1V.

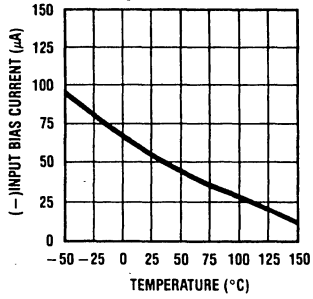
Note 5: Gain error is given as a percent of full-scale. Full-scale is defined as 1V at the input and 4.5V at the output.

Typical Performance Characteristics

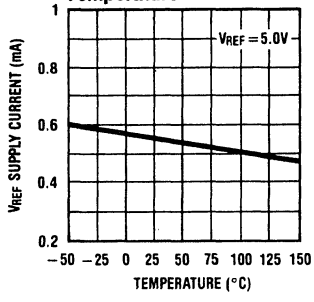
Non-Inverting Input Bias Current vs Temperature



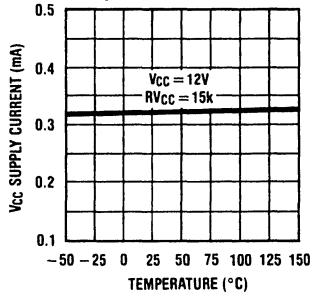
Inverting Input Bias Current vs Temperature



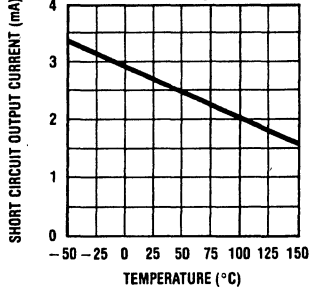
V_{REF} Supply Current vs Temperature



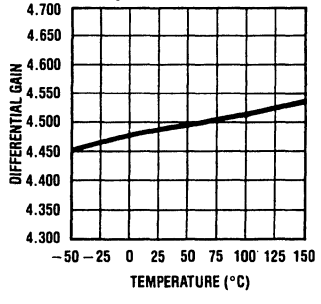
V_{CC} Supply Current vs Temperature



Short Circuit Output Current vs Temperature



Differential Gain vs Temperature



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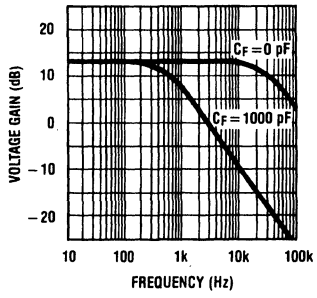
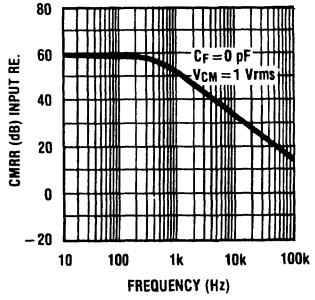
Typical Performance Characteristics (Continued)

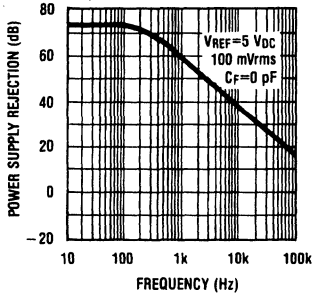
Voltage Gain vs Frequency



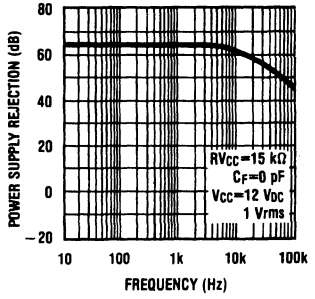
CMRR vs Frequency



V_{REF} Power Supply Rejection



V_{CC} Power Supply Rejection



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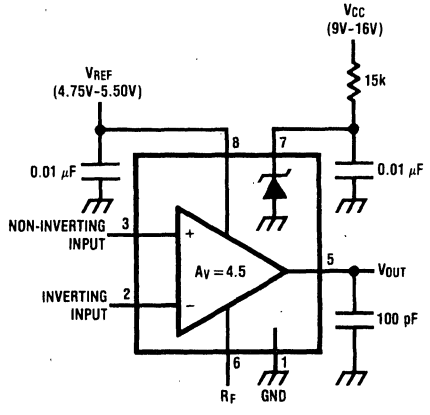
Test Circuit



TL/H/6744–5

National Semiconductor

PRELIMINARY

LM2005 20-Watt Automotive Power Amplifier

General Description

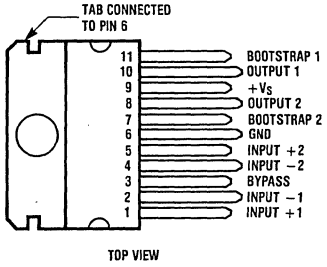
The LM2005 is a dual high power amplifier, designed to deliver optimum performance and reliability for automotive applications. High current capability (3.5A) enables the device to deliver 10W/channel into 2Ω (LM2005S), or 20W bridged monaural (LM2005M) into 4Ω, with low distortion.

Features

- Wide supply range (8V–18V)
- Externally programmable gain
- With or without bootstrap
- Low distortion
- Low noise
- High peak current capability
- P_O = 20W bridge
- High voltage protection
- AC and DC output short circuit protection to ground or across load
- Thermal protection
- Inductive load protection
- Accidental open ground protection
- Immunity to 40V power supply transients
- 3°C/W device dissipation
- Pin for pin compatible with TDA2005

Connection Diagram

Plastic Package



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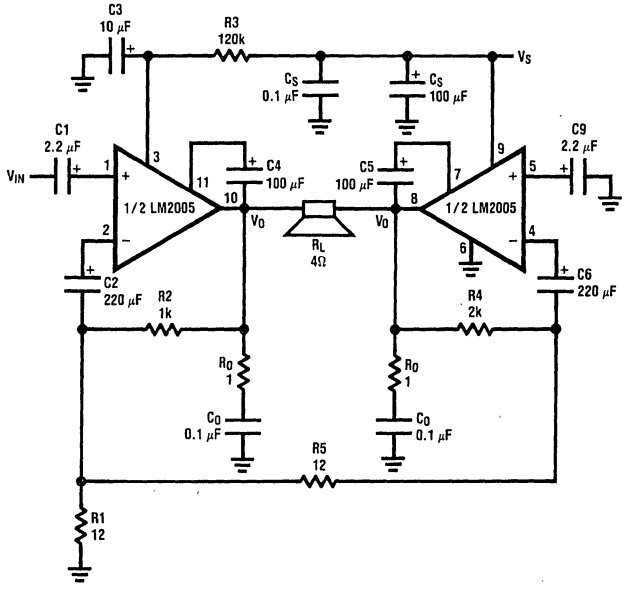
Order Number LM2005T
See NS Package T11A

Typical Application



TL/H/5129–2

FIGURE 1. 20W Bridge Amplifier Application and Test Circuit

S 12

Absolute Maximum Ratings

Operating Supply Voltage	18V
DC Supply Voltage (Note 1)	28V
Peak Supply Voltage (50 ms)	40V
Output Current	
Repetitive (Note 2)	3.5A
Non-Repetitive	4.5A
Power Dissipation	30W
Operating Temperature	−40°C to +85°C
Storage Temperature	−60°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Electrical Characteristics

$V_S = 14.4V$, $R_L = 2\Omega$ dual, $R_L = 4\Omega$ bridge, $T_{TAB} = 25°C$, frequency = 1 kHz unless otherwise specified

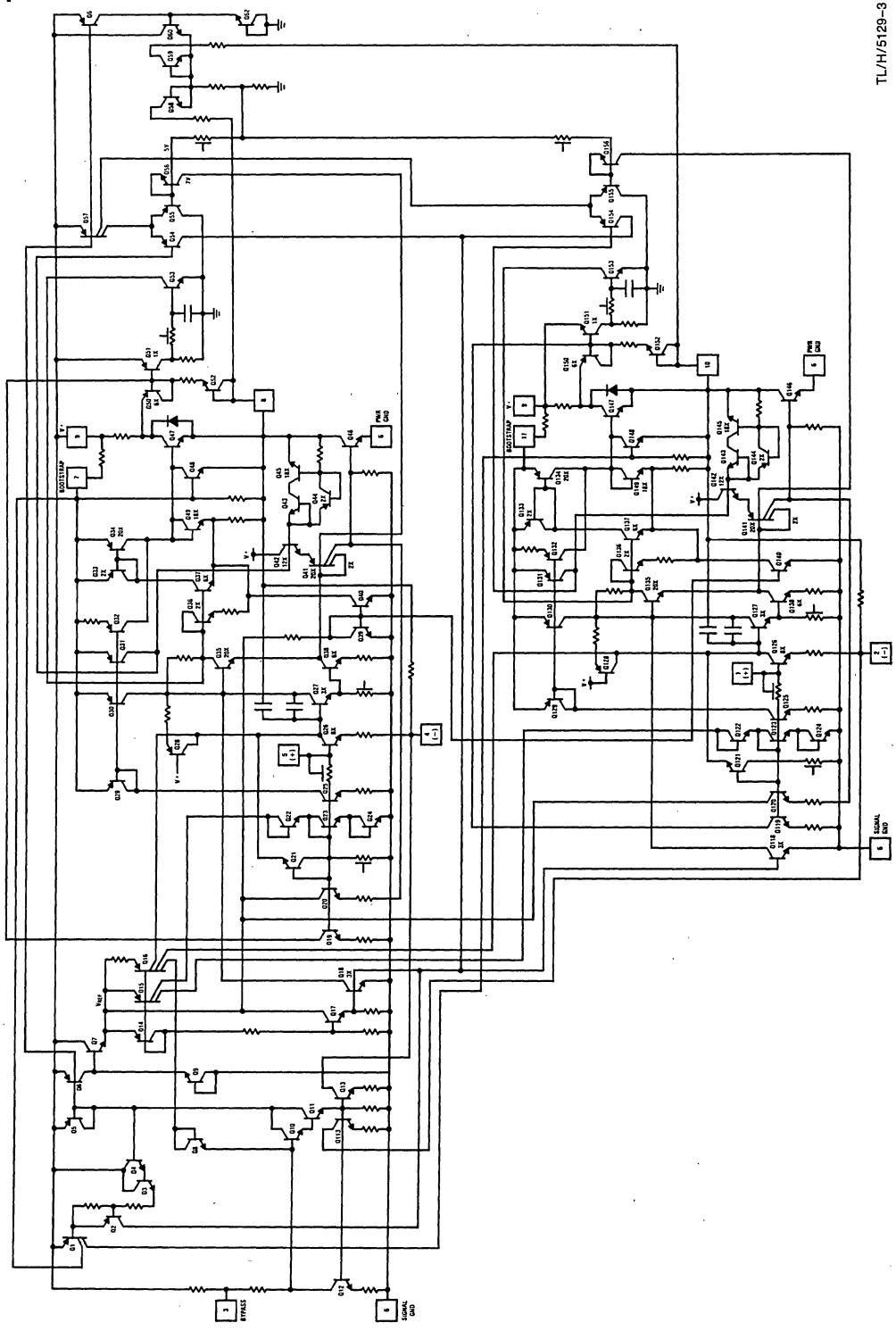
Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range		8		18	V
Quiescent Supply Current	$P_O = 0W$, Dual Mode		70	120	mA
DC Output Level (Pins 8 and 10)		6.6	7.2	7.8	V
Output V_{OS} (Between Pins 8 and 10)	LM2005M only			150	mV
Output Power	THD = 10%				
	$R_L = 4\Omega$ Dual	6	6.5		W/Ch
	2Ω Dual	9	10		W/Ch
	4Ω Bridge	18	20		W
	1.6Ω Dual	10	11		W/Ch
	3.2Ω Bridge	20	22		W
Distortion	$R_L = 4\Omega$, $P_O = 2W$ Dual		0.2	1	%
	$R_L = 4\Omega$, $P_O = 4W$ Bridge		0.3	1	%
	$R_L = 1.6\Omega$, $P_O = 4W$ Dual		0.3	1	%
	$R_L = 3.2\Omega$, $P_O = 8W$ Bridge		0.3	1	%
Power Supply Rejection Ratio (Output Referred)	$R_S = 0\Omega$, f = 100 Hz				
	Dual	35	45		dB
	Bridge	45	55		dB
Noise (Note 3)	Equivalent Input Noise				
	$R_S = 0\Omega$, BW = 20-20 kHz		1.5	5	μV
Channel Separation	Output Referred		60		dB
	$V_O = 4$ Vrms, LM2005S only				
Input Impedance	Pins 5 and 1 (Non-Inverting)	70	200		kΩ
Voltage Gain (Open Loop)			90		dB
Voltage Gain (Closed Loop)		48	50	51	dB
Low Frequency Roll Off	−3 dB				
	Dual			50	Hz
	Bridge			40	Hz
High Frequency Roll Off	−3 dB				
	Dual	15			kHz
	Bridge	20			kHz

Note 1: Internal voltage limit.

Note 2: Internal current limit.

Note 3: Not production tested. Not used to calculate AQL.

Equivalent Schematic

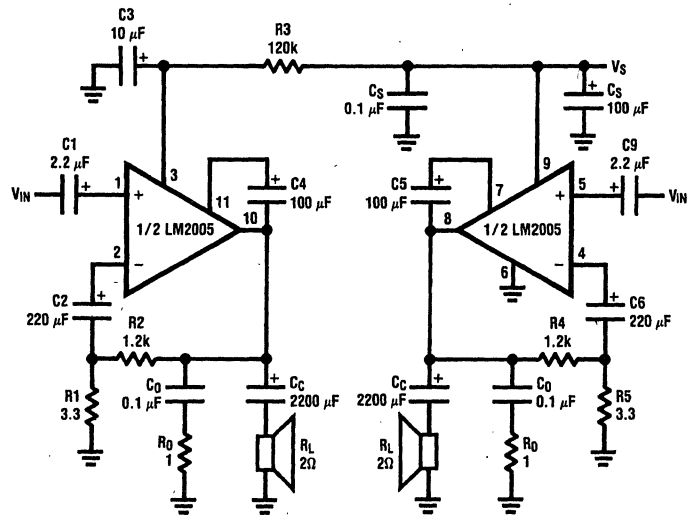


TL/H/5129–3

External Components *(Figure 2)*

Components	Comments
1. R1, R2 R5, R4	Sets voltage gain, $A_V \cong 1+\frac{R'}{R1}$ for one channel, $A_V = 1+\frac{R'}{R5}$ for the other. Where R' is the equivalent resistance of R2 in parallel with an internal 10k resistor: $R' = \frac{10k \bullet R2}{R2+10k}$. If $R2 << 10k$, then $A_V \cong 1+\frac{R2}{R1}$.
2. R3	Adjusts output symmetry for maximum power output.
3. R_O, C_O	Works to stabilize internal output stage. Necessary for stability. C_O should be ceramic disc or equivalently good high frequency capacitor.
4. C1, C9	Input coupling capacitor. Low frequency pole set by $F_L1 = \frac{1}{2\pi Z\,(\text{non-inverting})\,C1}$. Decreasing capacitor value will also increase noise.
5. C4, C5	Bootstrap capacitors, used to increase drive to output stage.
6. C3	Improves power supply rejection. Increasing C3 increases turn-on delay (approximately 2 ms per μF).
7. C2, C6	Inverting input DC decouple. Low frequency pole: $F_L2 = \frac{1}{2\pi Z(\text{inverting})C2}$. Z (inverting) $\approx$ 10 kΩ.
8. C_C	Output coupling capacitor. Isolates pins 10 and 8 from load. Low frequency pole; $F_L3 = \frac{1}{2\pi R_L C_C}$.
9. C_S	Power supply filtering.

Typical Applications (Continued)

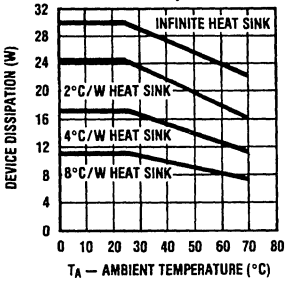


TL/H/5129–4

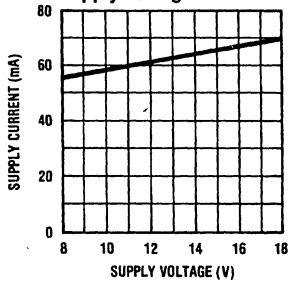
FIGURE 2. 10W/Channel Stereo Amplifier Application and Test Circuit

Typical Performance Characteristics

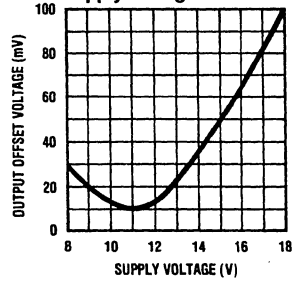
Device Dissipation vs Ambient Temperature



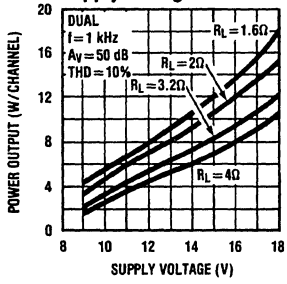
Supply Current vs Supply Voltage



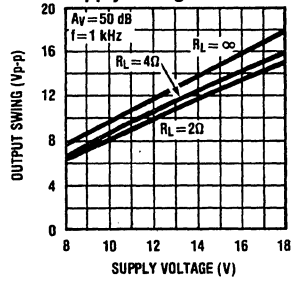
Output Offset Voltage vs Supply Voltage



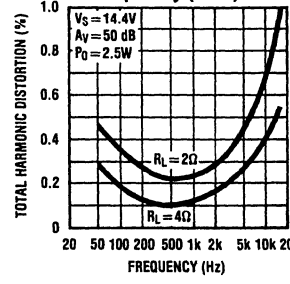
Power Output vs Supply Voltage



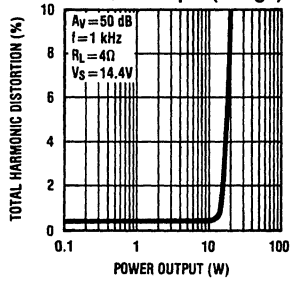
Output Swing vs Supply Voltage



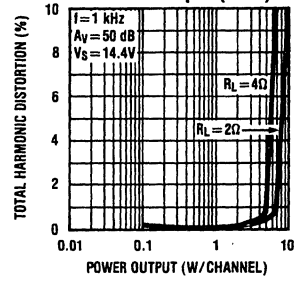
Total Harmonic Distortion vs Frequency (Dual)



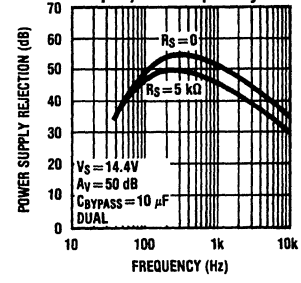
Total Harmonic Distortion vs Power Output (Bridge)



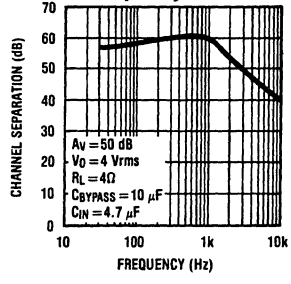
Total Harmonic Distortion vs Power Output (Dual)



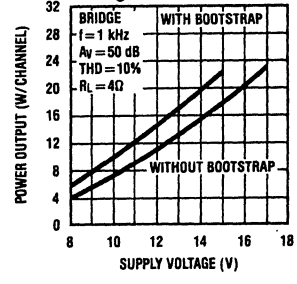
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



Channel Separation (Referred to the Output) vs Frequency



Power Output vs Supply Voltage



TL/H/5129–5

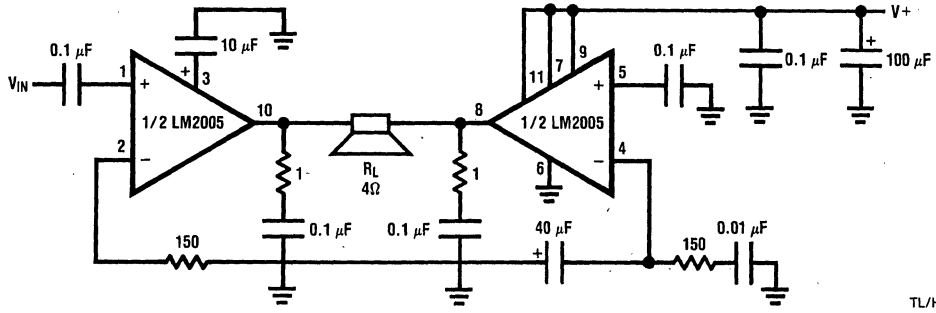
Application Hints

The high current capability of the LM2005 allows it to continuously endure either AC or DC short circuit to the output with a maximum supply voltage of 16V. This will protect the loudspeaker in a bridge mode, when a DC short to the output occurs to one side of the speaker. The device will prevent the speaker from destruction by reducing the DC across the load (bridge mode) to typically less than 2 V_{DC}(V_S = 14.4V, R_L = 4Ω), by an internal current pullback method.

The LM2005 can withstand a constant 28 V_{DC} on the supply with no damage (maximum operating voltage is 18V). The device is also protected from load dump or dangerous transients up to 40V for 50 ms (every 1000 ms) on the supply with no damage.

Protection diodes protect the device driving inductive loads, during which the load can generate voltages greater than supply or less than ground levels. The protection diodes will clamp these transients to a safe V_{BE} above and below the rail.

The bridge configuration in *Figure 3* is designed for applications requiring minimal printed circuit board area and maximum cost effectiveness. The circuit will function with the elimination of bootstrap components R3, C4 and C5 (refer to *Figure 1*). This will result in less output power by decreasing output voltage swing to the load. By using internal feedback resistors (typically 10 kΩ), feedback components R2, R3 and C2 (*Figure 1*) may be omitted where closed loop voltage gain accuracy is not critical. The net result is a stable, cost effective circuit that will satisfy many application needs.

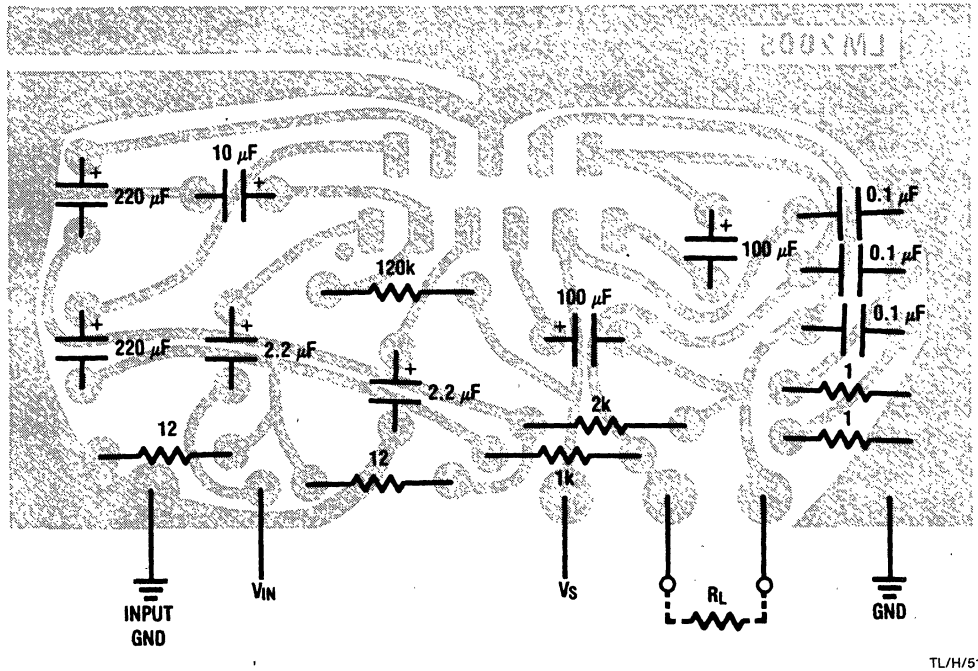


TL/H/5129–6

A_V = 41.5 dB @ 1 kHz

FIGURE 3. Minimal Component Application Circuit

Component Side (Scale 2:1)



TL/H/5129–7

FIGURE 4. Printed Circuit Board Layout for LM2005

National Semiconductor

PRELIMINARY

LM2879 Dual 9-Watt Audio Amplifier

General Description

The LM2879 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, AM-FM stereo receivers, etc.

The LM2879 will deliver 9W/channel to an 8Ω load. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown. The LM2879 is an LM379 in an improved power package. For more information, see AN-125.

Features

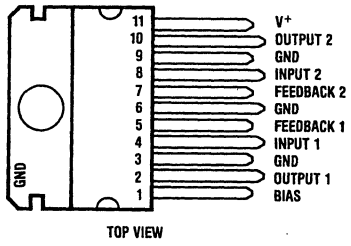
- A_{VO} typical 90 dB
- 9W per channel (typical)
- 70 dB ripple rejection
- 70 dB channel separation
- Internal stabilization
- Self centered biasing
- 3 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Applications

- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Connection Diagram

Plastic Package



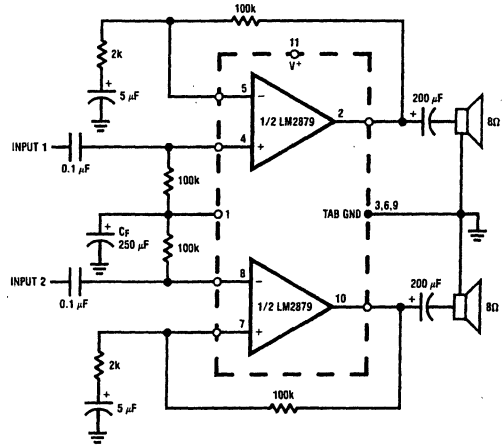
TOP VIEW

TL/H/5291–1

Order Number LM2879
See NS Package T11A

Test Circuit

Stereo Amplifier



TL/H/5291–2

Absolute Maximum Ratings

Supply Voltage	35V	Storage Temperature	−65°C to + 150°C
Input Voltage	0V − V_{SUPPLY}	Junction Temperature	150°C
Operating Temperature (Note 1)	0°C to + 70°C	Lead Temp. (Soldering, 10 seconds)	300°C

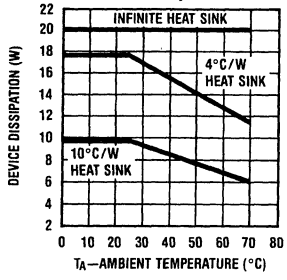
Electrical Characteristics $V_S = 28V$, $T_{TAB} 25°C$, Test Circuit of *Figure 1*, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Total Supply Current	$P_{OUT} = 0W$ $P_{OUT} = 2W$/Channel		12 460	65	mA mA
DC Output Level			14		V
Supply Voltage		10		34	V
Output Power	THD = 5% THD = 10%	 8	8 9		W W
THD	$P_{OUT} = 1W$/Channel, f = 1 kHz $P_{OUT} = 4W$/Channel, f = 1 kHz		0.05 0.04	1	% %
Input Offset Voltage			±15		mV
Input Bias Current			100		nA
Input Impedance		3			MΩ
Open Loop Gain	$R_S = 0Ω$		90		dB
Channel Separation	f = 1 kHZ	50	70		dB
Ripple Rejection	f = 120 Hz, $C_F = 250\ \mu F$		70		dB
Current Limit			1.5		A
Slew Rate			1.4		V/μs
Equivalent Input Noise Voltage	$R_S = 600Ω$, 100 Hz–10 kHz		3		μVrms

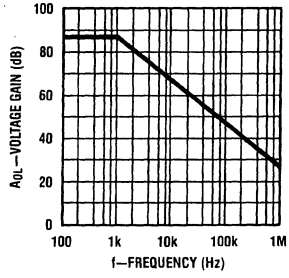
Note 1: For operation at ambient temperatures greater than 25°C the LM2879 must be derated based on a maximum 150°C junction temperature. Thermal resistance, junction to case, is 3°C/W. Thermal resistance, case to ambient, is 40°C/W.

Typical Performance Characteristics

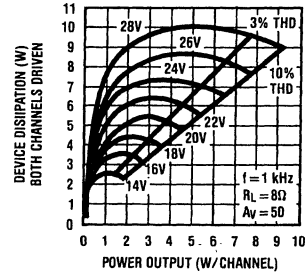
Device Dissipation vs Ambient Temperature



Open Loop Gain



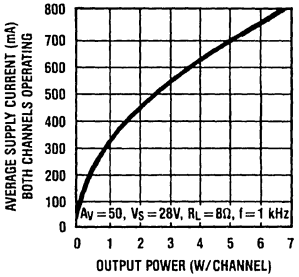
Power Dissipation vs Power Output



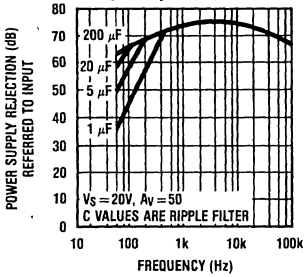
TL/H/5291–3

Typical Performance Characteristics (Continued)

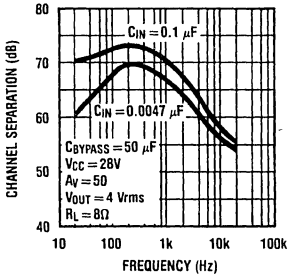
Supply Current vs Output Power



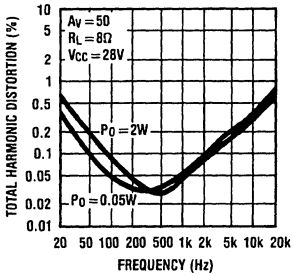
Supply Rejection vs Frequency



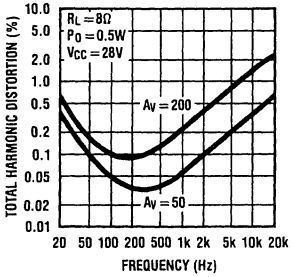
Channel Separation (Referred to the Output) Frequency



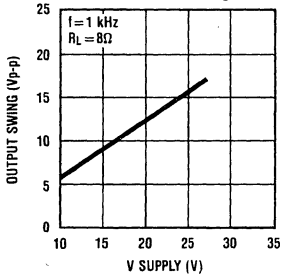
Total Harmonic Distortion vs Frequency



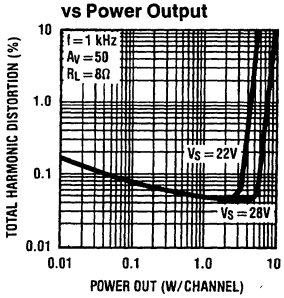
Total Harmonic Distortion vs Frequency



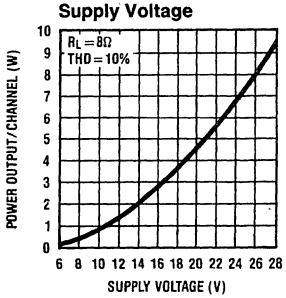
Output Swing vs V_S



Total Harmonic Distortion vs Power Output

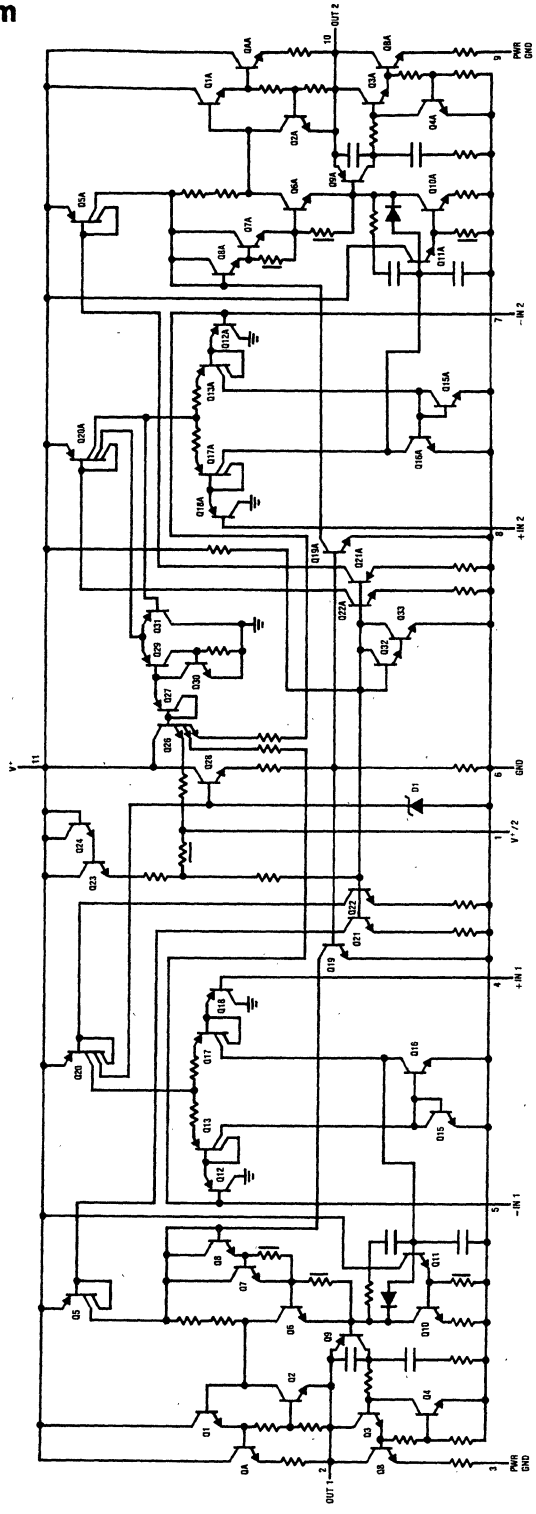


Power Output/Channel vs Supply Voltage



TL/H/5291–4

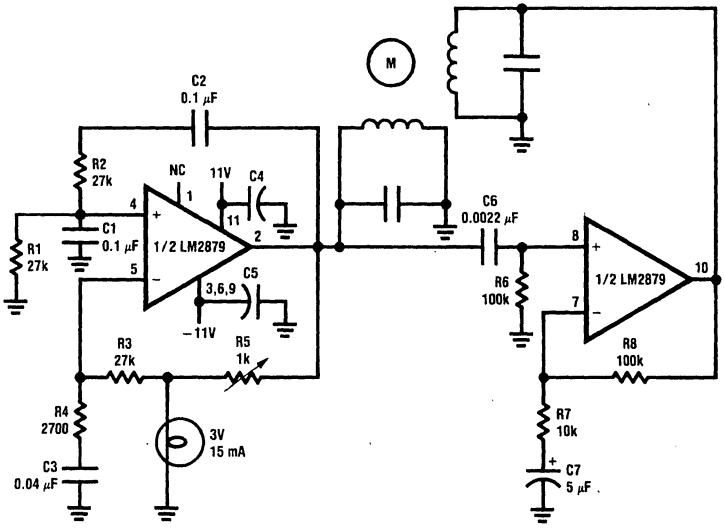
Schematic Diagram



TL/H/5291–5

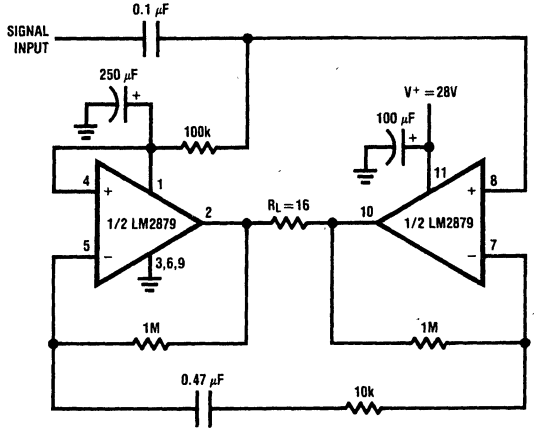
Typical Applications

Two-Phase Motor Drive



TL/H/5291–6

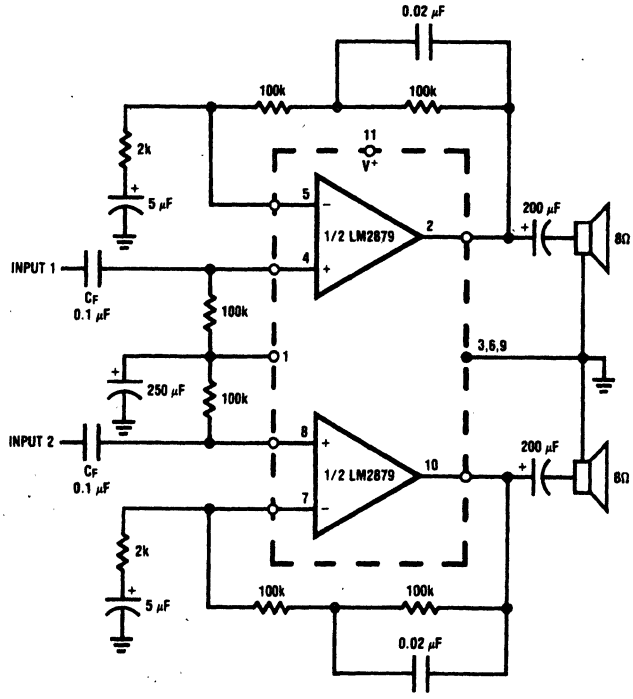
12W Bridge Amplifier



TL/H/5291–7

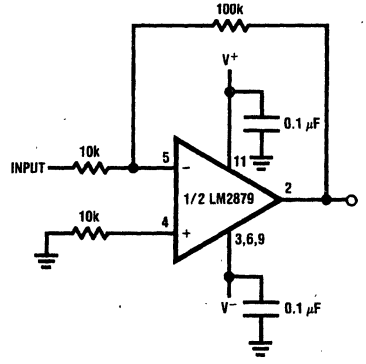
Typical Applications (Continued)

Simple Stereo Amplifier with Bass Boost



TL/H/5291–8

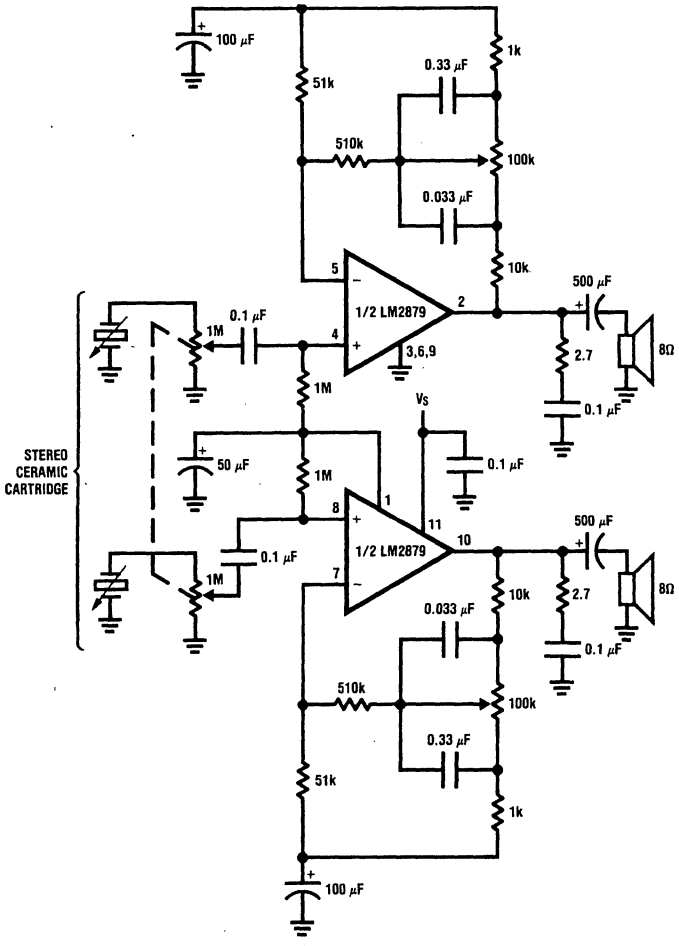
Power Op Amp (Using Split Supplies)



TL/H/5291–9

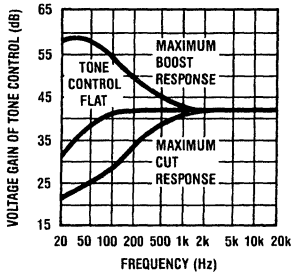
Typical Applications (Continued)

Stereo Phonograph Amplifier with Bass Tone Control



TL/H/5291–10

Frequency Response of Bass Tone Control



TL/H/5291–11

National Semiconductor

PRELIMINARY

LM2889 TV Video Modulator

General Description

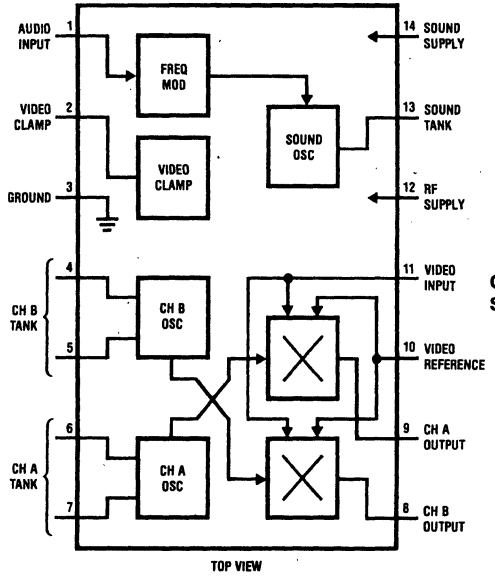
The LM2889 is designed to interface audio and video signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator and FM modulator, video clamp, and RF oscillators and modulators for two low-VHF channels.

The LM2889 allows video information from VTRs, video disk systems, games, test equipment, or similar sources to be displayed on black and white or color TV receivers.

Features

- Pin for pin compatible with LM1889 RF section
- Low distortion FM sound modulator (less than 1% THD)
- Video clamp for AC-coupled video
- Low sound oscillator harmonic levels
- 10V to 16V supply operation
- DC channel switching
- Excellent oscillator stability
- Low intermodulation products

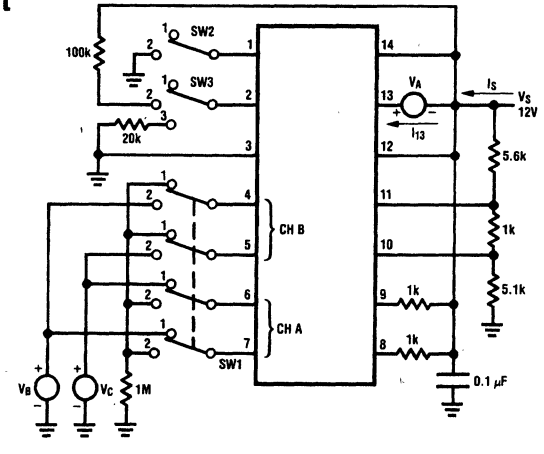
Block and Connection Diagrams (Dual-In-Line Package)



TOP VIEW

Order Number LM2889N
See NS Package Number N14A

DC Test Circuit



TL/H/5079–1

Absolute Maximum Ratings

Supply Voltage	$18V_{DC}$	(V14–V13) Max	$\pm 5V_{DC}$
Power Dissipation Package (Note 1)	700 mW	(V12-V8) Max	$7V_{DC}$
Operating Temperature Range	0°C to 70°C	(V12-V9) Max	$7V_{DC}$
Storage Temperature Range	−55°C to + 150°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

(DC test circuit, all switches normally pos. 1, $V_S = 12V$, $V_A = 2V$, $V_B = V_C = 10V$)

Parameter	Conditions	Min	Typ	Max	Units
Supply Current I_S		10	16	25	mA
Sound Oscillator Current ΔI_{13}	Change V_A from −2V to +2V	0.2	0.35	0.6	mA
Sound Oscillator Zener Current I_{13}			0.85		mA
Sound Modulator Audio Current ΔI_{13}	Change SW2 from Pos. 1 to Pos. 2		0.9		mA
Video Clamp Voltage V2 Unloaded Loaded	 SW3 Pos. 3	 5.0	 5.25 5.1	 5.45	 V_{DC} V_{DC}
Video Clamp Capacitor Discharge Current $(V_S-V2)/10^5$	SW3 Pos. 2		20		μA
Ch. A Oscillator OFF Voltage, V6, V7	SW1 Pos. 2		2		mV_{DC}
Ch. A Oscillator Current Level I_7	$V_B = 10V$, $V_C = 11V$	2.5	3.5	5.0	mA
Ch. B Oscillator OFF Voltage V4, V5			2		mV_{DC}
Ch. B Oscillator Current Level I_4	SW1 Pos. 2, $V_B = 10V$, $V_C = 11V$	2.5	3.5	5.0	mA
Ch. A Modulator Conversion Ratio $\Delta V9/(V11-V10)$	Measure ΔV9 by Changing from $V_B = 10V$, $V_C = 11V$, to $V_B = 11V$, $V_C = 10V$; Divide by V11–V10	0.3	0.50	0.75	V/V
Ch. B Modulator Conversion Ratio $\Delta V8/(V11-V10)$	SW1 Pos. 2, Measure ΔV8 by Changing from $V_B = 10V$, $V_C = 11V$, to $V_B = 11V$, $V_C = 10V$; Divide by V11–V10	0.3	0.50	0.75	V/V

AC Electrical Characteristics (AC test circuit, $V_S = 12V$)

Parameter	Conditions	Min	Typ	Max	Units
Sound Carrier Oscillator Level (V13)			3.4		Vp-p
Sound Modulator Deviation	$\Delta f/\Delta V_{IN}$, SW1 Pos. 2, Change V_{IN} from 1.4V to 1.0V, Measure Δf at Pin 13, Divide as Shown		250		Hz/mV
Ch. 3 RF Oscillator Level $\nu 6$, $\nu 7$	Ch. Sw. Pos. 3, f = 61.25 MHz, Use FET Probe		550		mVp-p
Ch. 4 RF Oscillator Level, $\nu 4$, $\nu 5$,	Ch. Sw. Pos. 4, f = 67.25 MHz, Use FET Probe		550		mVp-p
RF Modulator Conversion Gain $\nu_{OUT}/(V10-V11)$	Ch. Sw. Pos. 3, f = 61.25 MHz. (Note 2)		10		mVrms/V

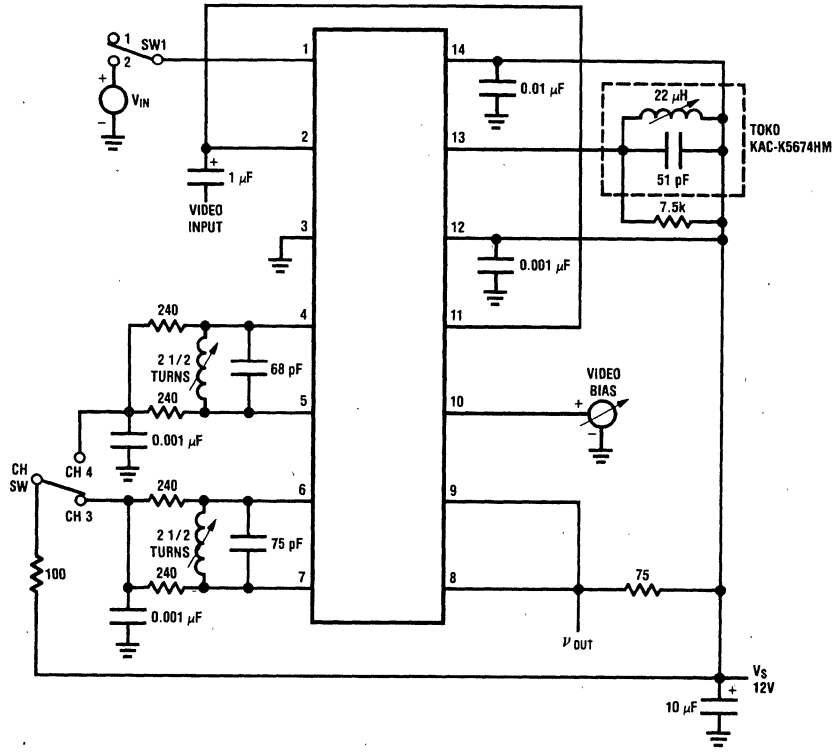
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 80°C/W junction to ambient.

Note 2: Conversion gain shown is measured with 75Ω input RF meter which makes the AC RF output load 37.5Ω.

Design Characteristics (AC test circuit, $V_S = 12V$)

Parameter	Typ	Units
Sound Modulator Audio THD at ±25 kHz Deviation, V_{IN} must be 1 kHz Source, Demodulate as Shown in *Figure 1*	0.8	%
Sound Modulator Input Impedance (Pin 1)	1.5	kΩ
Sound Modulator Bandwidth	100	kHz
Oscillator Supply Dependence, Sound Carrier, RF	See Curves	
Oscillator Temperature Dependence (IC Only)		
Sound Carrier	−15	ppm/°C
RF	−50	ppm/°C
RF Oscillator Maximum Operating Frequency (Temperature Stability Degraded)	100	MHz
RF Modulator		
Carrier Suppression (Adjust Video Bias for Minimum RF Carrier at v_{OUT} and Reference to v_{OUT} with 3V Offset at Pins 10 and 11, See Applications Information, RF Modulation Section)	30	dB
3.58 MHz Differential Gain	5	%
Differential Phase	3	degrees
2.5V Vp-p Video, 87.5% Mod		
Output Harmonics below RF Carrier		
2nd, 3rd	−12	dB
4th and Above	−20	dB
Input Impedance, Pin 10, Pin 11	1 MΩ//2 pF	

AC Test Circuit



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Test Circuit

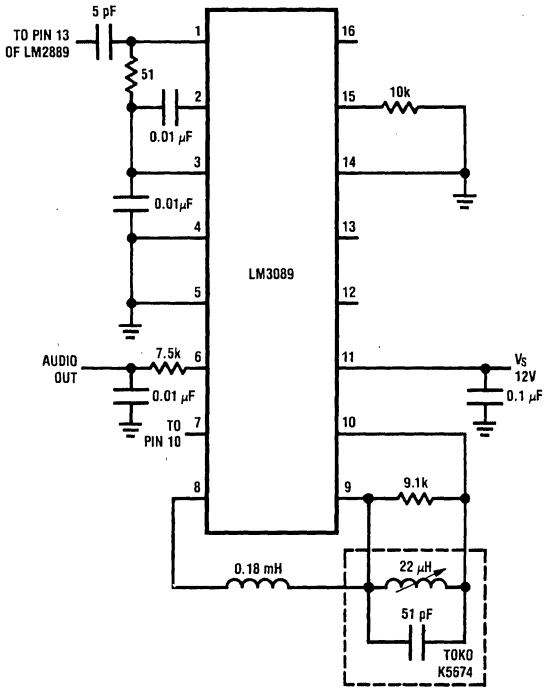

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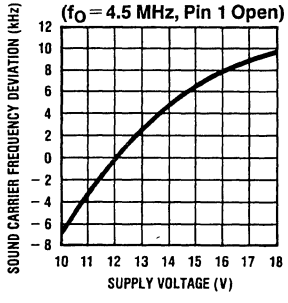
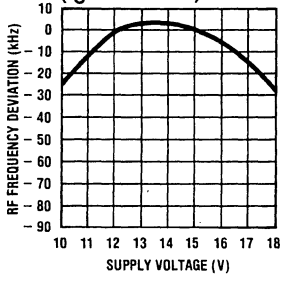
FIGURE 1. 4.5 MHz Sound FM Demodulator

Typical Performance Characteristics (Refer to AC test circuit unless noted)

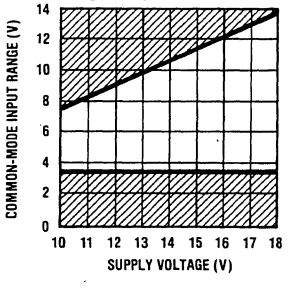
Sound Carrier Oscillator Supply Dependence (f_O = 4.5 MHz, Pin 1 Open)



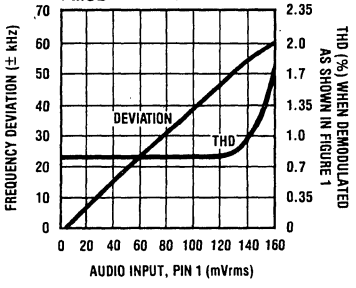
RF Oscillator Frequency Supply Dependence (f_O = 67.25 MHz)



RF Modulator Common-Mode Input Range Pins 10, 11 (Circuit Diagrams)



FM Sound Modulator Dynamic Characteristics (f_{MOD} = 1 kHz)



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Circuit Description (Refer to Circuit Diagrams)

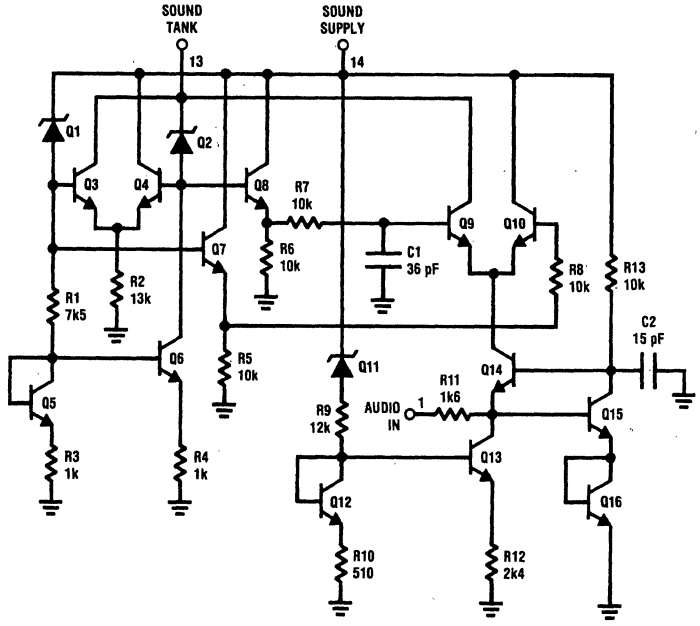
The sound carrier oscillator is formed by differential amplifier Q3, Q4 operated with positive feedback from the pin 13 tank to the base of Q4. Frequency modulation is obtained by varying the 90 degree phase shifted current of Q9. Q14's emitter is a virtual ground, so the voltage at pin 1 determines the current R11, which ultimately modulates the collector current of Q9.

The video clamp is comprised of devices Q58-Q60. The clamp voltage is set by resistors R40, R41, R49, and R50. The $\Delta V_{BE}/R42$ current sets the capacitor discharge current. Q59 and the above mentioned resistor string help maintain a temperature stable clamp voltage.

The channel B oscillator consists of devices Q24 and Q25 cross-coupled through level-shift zener diodes Q22 and Q23. A current regulator consisting of devices Q17–Q21 is used to achieve good RF stability over temperature and supply. The channel B modulator consists of multiplier devices Q28–Q31, Q34 and Q35. The top quad is coupled to the channel B tank through isolating devices Q26 and Q27. A DC potential between pins 10 and 11 offsets the lower pair to produce an output RF carrier at pin 8. That carrier is then modulated by both the sound subcarrier at pin 10 and the composite video signal at pin 11. The channel A modulator shares pin 10 and 11 buffers, Q32 and Q33, with channel B and operates in an identical manner.

The current flowing through channel B oscillator diodes Q22, Q23 is turned around in Q36–Q38 to source current for the channel B RF modulator. In the same manner, the channel A oscillator Q54–Q57 uses turn-around Q49–Q51 to source the channel A modulator. One oscillator at a time may be activated by its current turn-around, and the other oscillator/modulator combination remains off.

Circuit Diagrams



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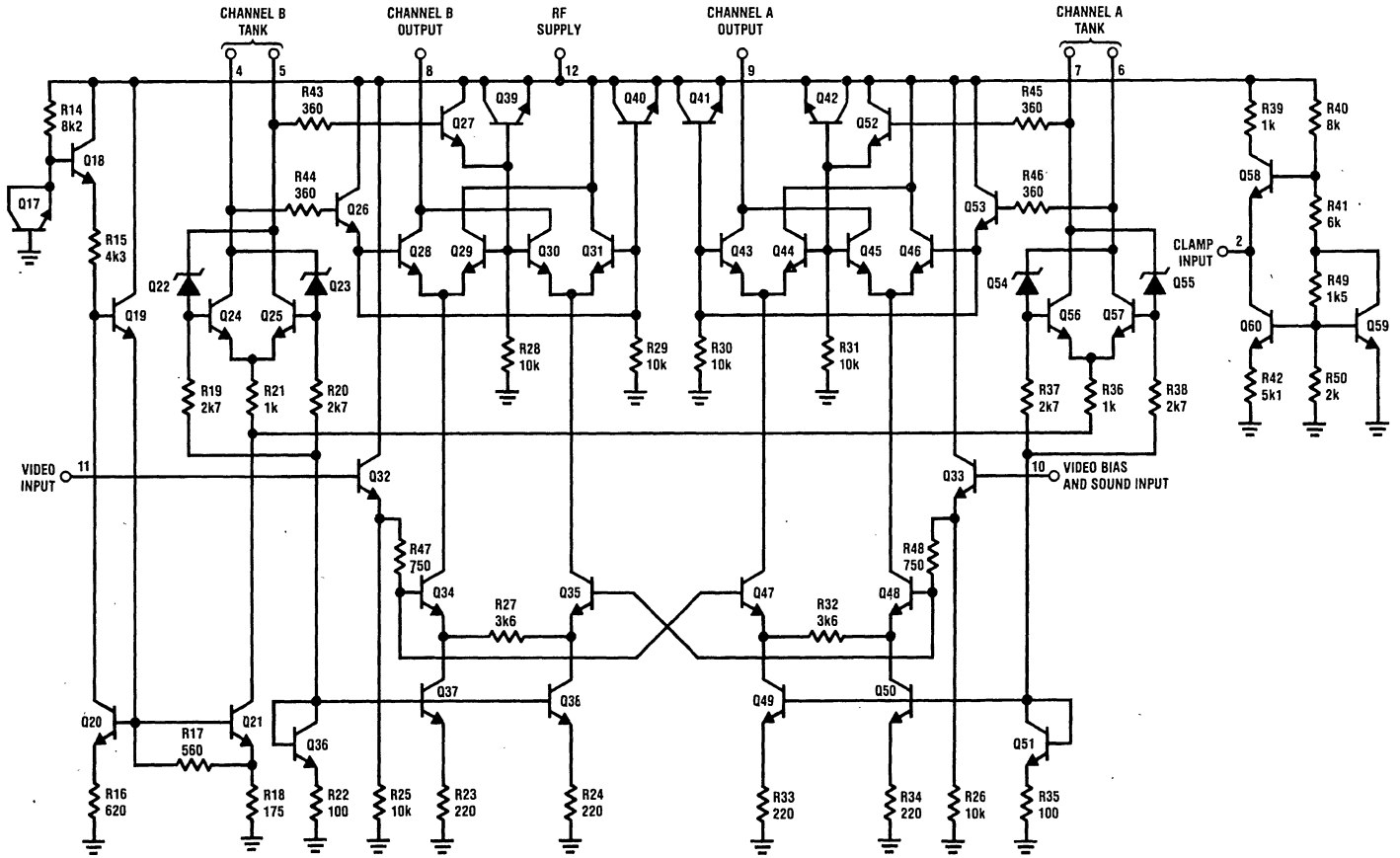
CHANNEL B TANK
CHANNEL B OUTPUT
RF SUPPLY
CHANNEL A OUTPUT
CHANNEL A TANK
4
5
8
12
9
7
6
R14 8k2
Q18
Q17
R15 4k3
R43 360
R44 360
Q26
Q27
Q39
Q40
Q41
Q42
Q52
R45 360
R46 360
Q53
R39 1k
R40 8k
Q58
R41 6k
CLAMP INPUT
2
R49 1k5
Q60
Q59
R42 5k1
R50 2k
Q22
Q23
Q19
Q24
Q25
Q28
Q29
Q30
Q31
Q43
Q44
Q45
Q46
Q54
Q55
Q56
Q57
R28 10k
R29 10k
R30 10k
R31 10k
R19 2k7
R21 1k
R20 2k7
R37 2k7
R36 1k
R38 2k7
VIDEO INPUT
11
Q32
Q33
10
VIDEO BIAS AND SOUND INPUT
R47 750
R48 750
Q34
Q35
Q47
Q48
R27 3k6
R32 3k6
Q37
Q36
Q49
Q50
Q20
Q21
R17 560
Q36
Q51
R16 620
R18 175
R22 100
R25 10k
R23 220
R24 220
R33 220
R34 220
R26 10k
R35 100

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Applications Information

SOUND FM MODULATOR

Frequency deviation is determined by the Q of the tank circuit at pin 13 and the current entering the audio input, pin 1. This current is set by the input voltage V_{IN}, the device input impedance (1.5 kΩ), and any impedance network connected externally. A signal of 60 mVrms at pin 1 will yield about ±25 kHz deviation when configured as shown in *Figure 2*.

VIDEO CLAMP

When video is not available at DC levels within the RF modulator common-mode range, or if the DC level of the video is not temperature stable, then it should be AC-coupled as shown in the typical applications circuit (*Figure 2*). The clamp holds the horizontal sync pulses at 5.2V for $V_S = 12V$. The clamp coupling capacitor is charged during every sync pulse and discharged when video information is present. The discharge current is approximately 20 μA. This current and the amount of acceptable tilt over a line of video determines the value of the coupling capacitor C1. For most applications 1 μF is sufficient.

RF MODULATION

Two RF channels are available, with carrier frequencies up to 100 MHz being determined by L-C tank circuits at pins 4/5 and 6/7. The signal inputs (pins 10 and 11) are common to both modulators, but removing the power supply from an RF oscillator will also disable that modulator.

The offset between the two signal pins determines the level of the RF carrier output. To preserve the DC content of the video signal, amplitude modulation of the RF carrier is done in one direction only, with increasing video (toward peak white) decreasing the carrier level. This means the active composite video signal at pin 11 must be offset with respect to pin 10 and the sync pulse should produce the largest offset.

The largest video signal (peak white) should not be able to suppress the carrier completely, particularly if sound transmission is needed. This requires that pin 10 be biased above the largest expected video signal. Because peak white level is often difficult to define, a good rule to follow is to bias pin 10 at a level which is four times the sync amplitude above the sync tip level at pin 11. For example, the DC bias at pin 10 with 0.5V sync clamped to 5.2V on pin 11, should be $5.2 + (4 \times 0.5) = 7.2V$.

Typical Application

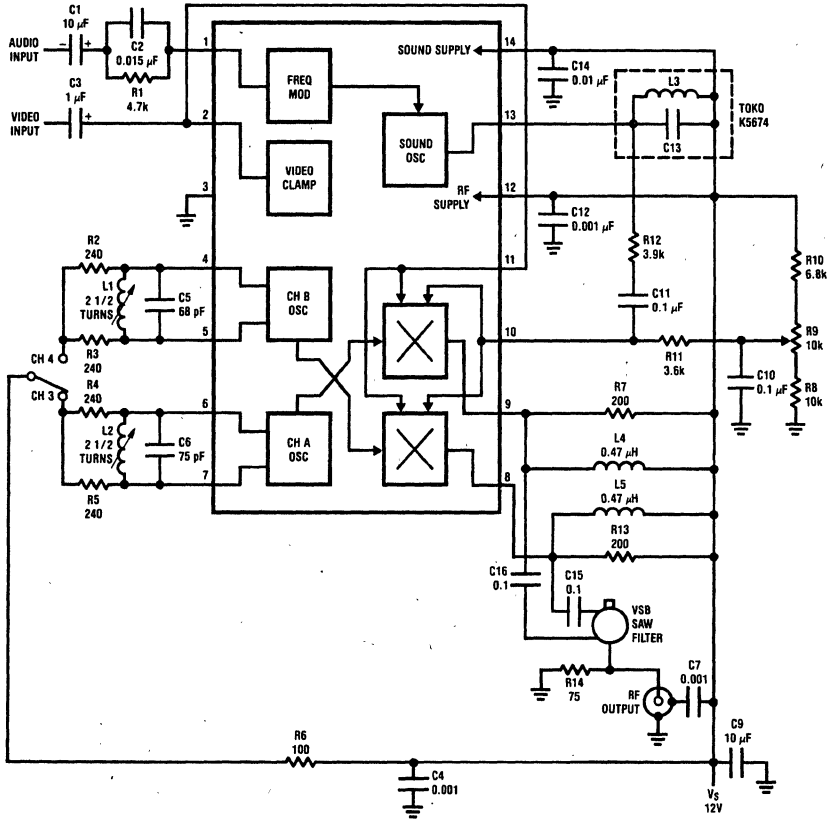

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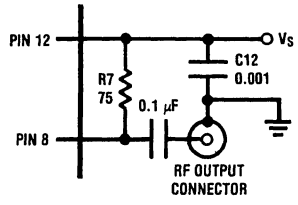
FIGURE 2. Two Channel Video Modulator with FM Sound

Applications Information (Continued)

When the signal inputs are exactly balanced, ideally there is no RF carrier at the output. Circuit board layout is critical to this measurement. For optimum performance, the output and supply decoupling circuitry should be configured as shown in *Figure 3*.



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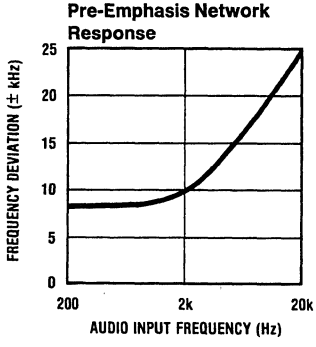
RF decouple supply directly to output ground.

FIGURE 3. Correct RF Supply Decoupling

The video clamp level is derived from a resistive divider connected to supply (V_S). To maintain good supply rejection, pin 10, which is biased externally, should also be referenced to supply (see *Figure 2*).

Pin Description (Refer to *Figure 2*)

Pin 1—Audio Input: Pin 1 is the audio input to the sound FM generator. Frequency deviation is proportional to the signal at this pin. A pre-emphasis network comprised of R1, C2, and the device input impedance yields the following response with an 80 mVrms audio input.



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Increasing R1 lowers the boost frequency, and decreases deviation below the boost frequency. Increasing C2 only lowers the boost frequency. C1 is a coupling capacitor, and must be a low impedance compared to the sum of R1 and the device input impedance (1.5 kΩ).

Pin 2—Video Clamp: The video clamp restores the DC component to AC-coupled video. The video is AC-coupled to the clamp via C3. Decreasing C3 will cause a larger tilt between vertical sync pulses in the clamped video waveform.

Pin 3—Ground: Although separate on the chip level, all ground terminate at pin 3.

Pins 4/5—Channel 4 Oscillator: Pins 4 and 5 are the collector outputs of the channel 4 oscillator. L1 and C5 set the oscillator frequency defined by $f_O = 0.159/\sqrt{L1C5}$. Increasing L1 will decrease the oscillator frequency while decreasing L1 will increase the oscillator frequency. Decreasing C5 will increase the oscillator frequency and lower the tank Q causing possible drift problems. R2 and R3 are the oscillator loads which determine the oscillator amplitude and the tank Q. Increasing these resistors increases the Q and the oscillator amplitude, possibly overdriving the RF modulator, which will increase output RF harmonics. Decreasing R2 and R3 reduces the tank Q and may cause increased drift. C4 is an RF decoupling capacitor. Increasing C4 may result in less effective decoupling at RF. Decreasing C4 may introduce RF to supply coupling.

Pins 6/7—Channel 3 Oscillator; Pins 6 and 7 are the channel 3 oscillator outputs. Every component at these pins has the same purpose and effect as those at pins 4 and 5.

Pin 8—Channel 4 RF Output: Pin 8 is the channel 4 RF output and R13 is the load resistor. The RF signal is AC coupled via C15 to the output filter which is a two channel VSB filter. L5 is parallel resonant with the filter input capacitance minimizing loss in the output network. R14 terminated the filter output.

Pin 9—Channel 3 RF Output: Pin 9 is the channel 3 RF output with all components performing the same functions as those in the pin 8 description.

Pin 10—RF Modulator Sound Subcarrier Input: Pin 10 is one of the RF modulator inputs and may be used for video or sound. It is used as a sound subcarrier input in *Figure 2*. R8, R9, and R10 set the DC bias on this pin which determines the modulation depth of the RF output (see Application Notes). R12 and C11 AC-couple the sound subcarrier from the sound modulator to the RF modulator. R12 and R11 form a resistive divider that determines the level of sound at pin 10, which in turn sets the picture carrier to sound subcarrier ratio. Increasing the ratio of R11/R12 will increase the sound subcarrier at the output. C10 forms an AC ground, preventing R8, R9, and R10 from having any effects on the circuit other than setting the DC potential at pin 10. R11 and R12 also effect the FM sound modulator (see pin 13 description).

Pin Description (Continued)

Pin 11—Video Input: Pin 11, when configured as shown, is the RF modulator video input. In this application, video is coupled directly from the video clamp. Alternatively, video could be DC-coupled directly to pin 11 if it is already within the DC common-mode input range of the RF modulator (see curves). In any case, the video sync tip at pin 11 must have a constant DC level independent of video content. Because of circuit symmetry, pins 10 and 11 may be interchanged.

Pin 12—RF Supply: Pin 12 is the RF supply, with C12 and C7 serving as RF decouple capacitors. Increasing C12 or C7 may result in less effective RF decoupling, while decreasing them may cause supply interaction. It is important that C7 be grounded at the RF output ground.

Pin 13—Sound Tank: Pin 13 is the collector output of the sound oscillator. L3 and C13 determine the oscillating frequency by the relationship $f_O = 0.159/\sqrt{L3C13}$. Increasing L3 or C13 will lower the operating frequency, while decreasing them will raise the frequency. L3 and C13 also help define the Q of the tank, on which FM modulator deviation level depends. As C13 increases, Q increases, and frequency deviation decreases. Likewise, decreasing C13 increases deviation. The other factor concerning Q is the external resistance across the tank. The series combination R11 + R12 usually dominates the tank Q. Decreasing this resistive network will decrease Q and increase deviation. It should be noted that because the level of phase modulation of the 4.5 MHz signal remains constant, variation in Q will not effect distortion of the frequency modulation process if the audio at pin 1 is left constant. The amplitude of the sound subcarrier is directly proportional to Q, so increasing the unloaded Q or either of the resistors mentioned above will increase the sound subcarrier amplitude. For proper operation of the frequency modulator, the sound subcarrier amplitude should be greater than 2 Vp-p.

Pin 14—Sound Supply: Pin 14 is the sound supply and C14 is an RF decouple capacitor. Decreasing C14 may result in increased supply interaction.

Printed Circuit Layout

Printed circuit board layout is critical in preventing RF feedthrough. The location of RF bypass capacitors on supply is very important. *Figure 4* shows an example of a properly layed out circuit board. It is recommended that this layout be used.

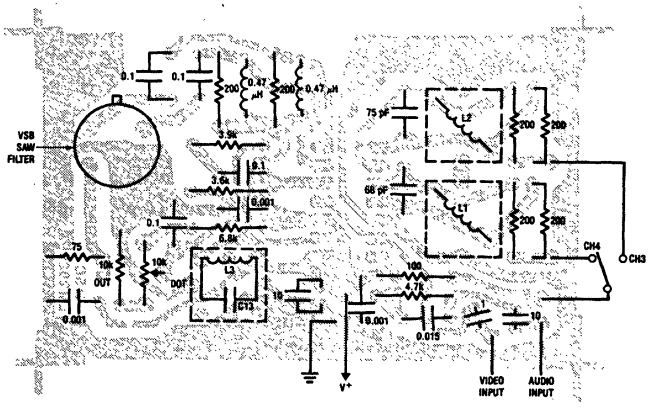

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FIGURE 4. Printed Circuit Board and Component Diagram (Component Side 1X)

National Semiconductor

PRELIMINARY

LM3361A Low Voltage/Power Narrow Band FM IF System

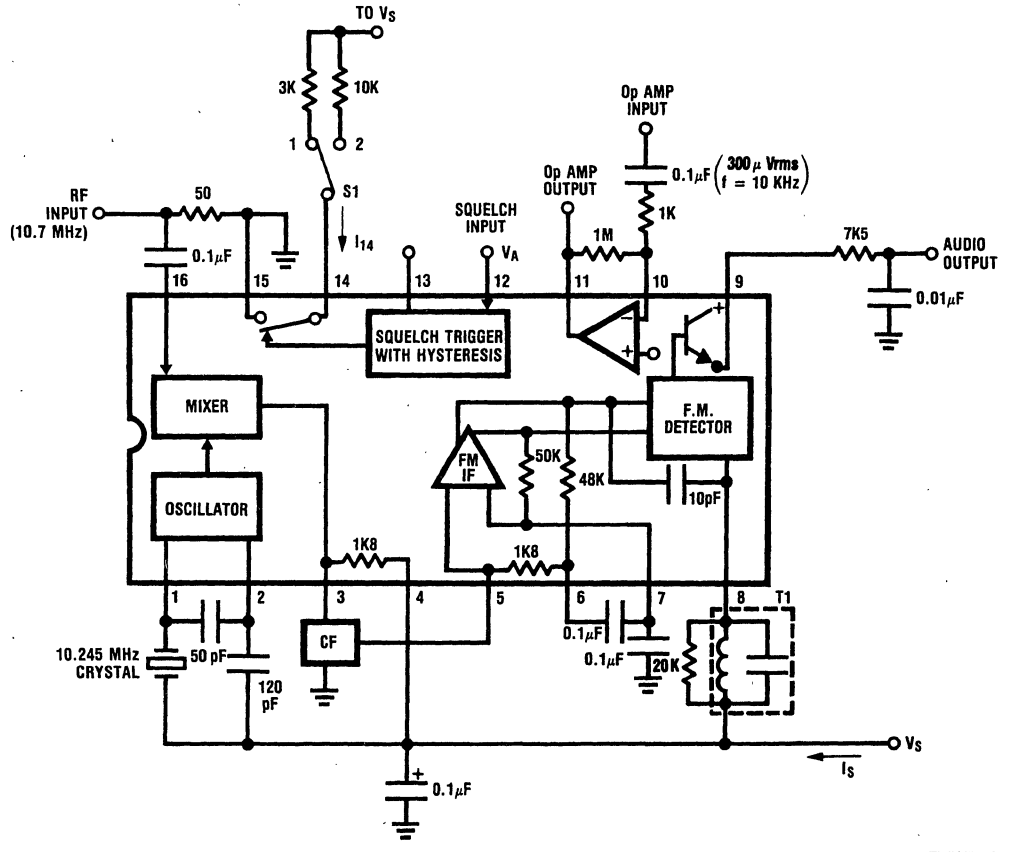
General Description

The LM3361A contains a complete narrow band FM demodulation system operable to less than 2V supply voltage. Blocks within the device include an oscillator, mixer, FM IF limiting amplifier, FM demodulator, op amp, scan control, and mute switch. The LM3361A is similar to the MC3361 with the following improvements: the LM3361A has higher voltage swing both at the op amp and audio outputs. It also has lower nominal drain current and a squelch circuit that draws significantly less current than the MC3361. Device pinout functions are identical with some slightly different operating characteristics.

Features

- Functions at low supply voltage (less than 2V)
- Highly sensitive (−3 dB limiting at 2.0 μV input typical)
- High audio output (increased 6 dB over MC3361)
- Low drain current (2.8 mA typ., V_{CC} = 3.6V)
- Minimal drain current increase when squelched
- Low external parts count

Block Diagram And Test Circuit



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Order Number LM3361AN
See NS Package N16E

T1-TOKO RMC-2A6597HM
CF-MURATA CFU 455E

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Absolute Maximum Ratings

Package dissipation (Note 1)	1500 mW	Operating ambient temperature range	0° to 70°C
Power supply voltage (V_S)	12 V	Storage temperature range	−55° to +150°C
RF input voltage (V_S>3.6V)	1 Vrms	Lead temp. (Soldering 10 seconds)	300°C
Mute function (pin 14)	−.7 to 5 Vp		

Parameters Guaranteed By Electrical Testing

(Test ckt., T_A=25°C, V_S=3.6V, f_O=10.7 MHz, Δf= ±3 KHz, f_{MOD}=1 KHz, 50Ω source)

Parameter	Measure	Min	Typ	Max	Units
Supply Voltage Range	V_S	2.0	3.6	9.0	V
Supply Current					
Squelch Off	I_S		2.8	5.0	mA
Squelch On	I_S		3.6	6.0	mA
RF Input for −3 dB Limiting	RF Input		2.0	6.0	μV
Recovered Audio at Audio Output	Audio Output	200	350		mV_{RMS}
Audio Out DC	V_9	1.2	1.5	1.8	V_{DC}
Op Amp Gain	v_{11}/v_{IN}	40	55		dB
Op amp Output DC	V_{10}	0.4	0.7		V_{DC}
Op Amp Input Bias Current	$(V_{10}-V_{11})/1M\Omega$		20	75	nA
Scan voltage					
Pin 12 high (2V)	V_{13}		0	0.5	V_{DC}
Pin 12 Low (0V)	V_{13}	3.0	3.4		V_{DC}
Mute Switch Impedance, Pin 12 0V Switch S1 from pos.1 to pos.2	$\Delta V_{14}/\Delta I_{14}$		15	30	ohms

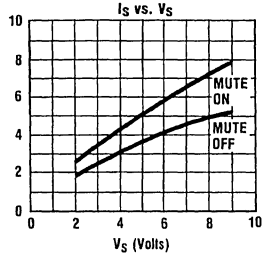
Design Parameters Not Tested or Guaranteed

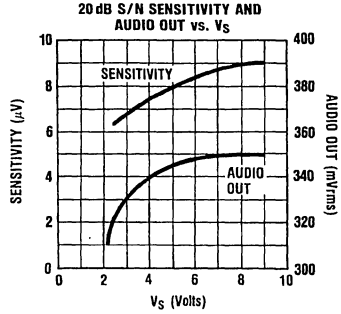
	Typ	
Mixer Conversion Gain (Note 2.)	46	V/V
Mixer Input Resistance	3.6	Kohm
Mixer Input Capacitance	2.2	pF
Detector output impedance	500	ohm
Trigger Hysterisis	100	mV
Mute off impedance (measure pin 14 with pin 12 @ 2V)	10	Mohm
Squelch threshold	.65	V_{DC}
Detector center frequency slope	0.15	V/KHz

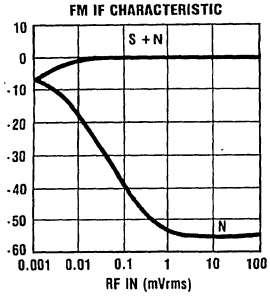
Note 1. For operation above 25°C ambient temperature, the device must be derated based on 150°C maximum junction temperature and a thermal resistance θ_{JA} of 80°C/W.

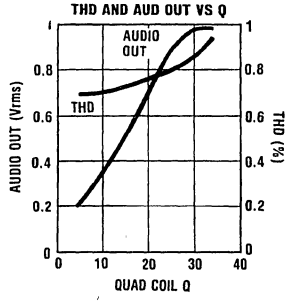
Note 2. Mixer gain is supply dependent and effects overall sensitivity accordingly (See Typical Performance Characteristics).

Typical Performance Characteristics (Test Circuits)









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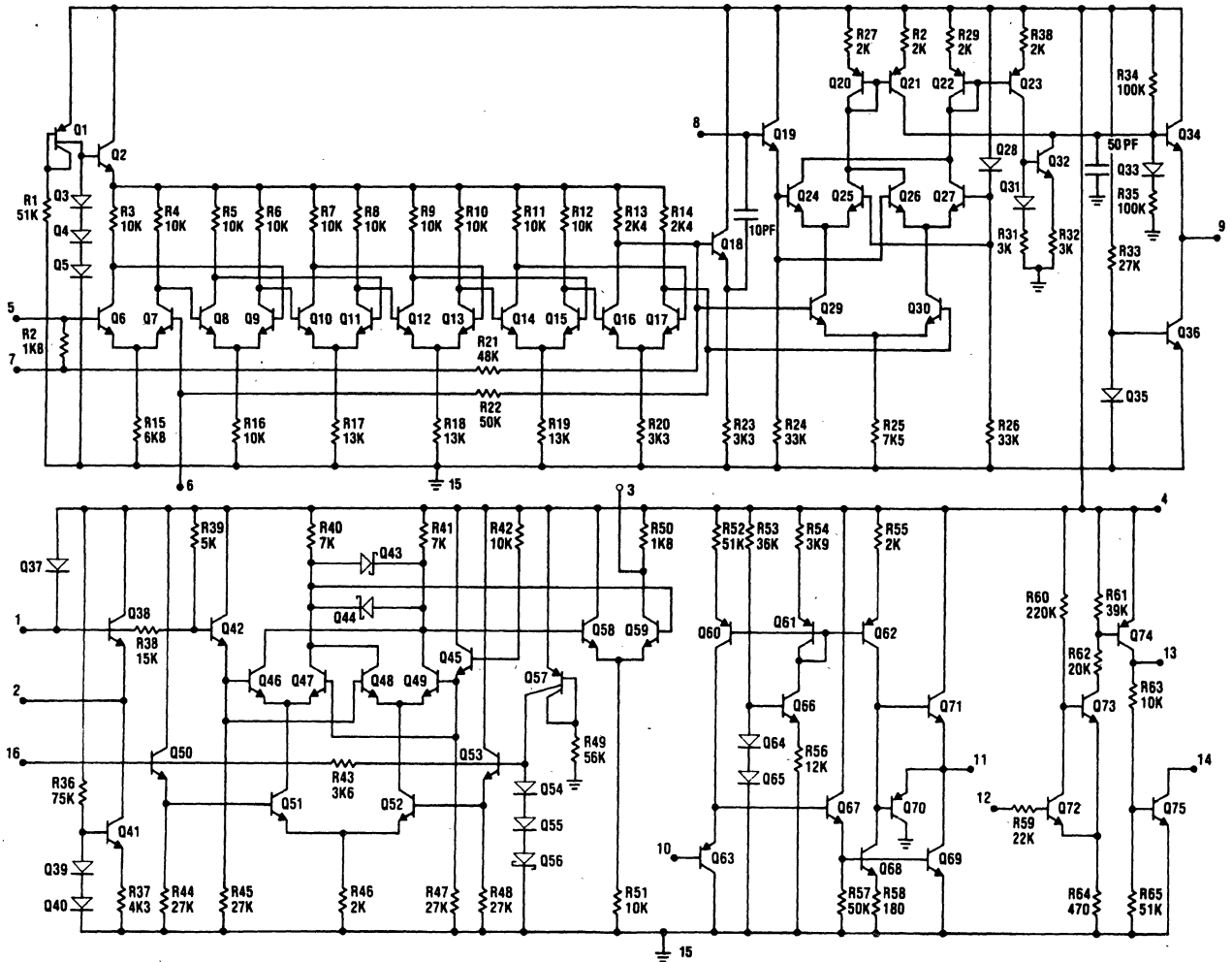
Internal Schematic



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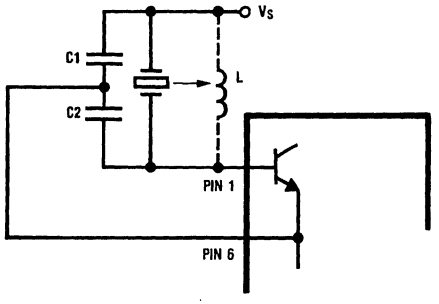
Applications Information (See Internal Schematic)

OSCILLATOR

The Colpitts type oscillator is internally biased with a regulated current source which assures proper operation over a wide supply range. The collector, base, and emitter terminals are at pins 4, 1, and 2 respectively. The crystal, which is used in the parallel resonant mode, may be replaced with an appropriate inductor if the application does not require the stability of a crystal oscillator. In this case, the resonant frequency will be determined by the inductor in parallel with the series combination of C1 and C2.



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so $Ct = (C1)(C2)/(C1+C2)$

and $f_O = .159/\sqrt{L(Ct)}$

MIXER

The mixer is double balanced to reduce spurious responses. The upper pairs are switched by the oscillator while the RF input is applied to the lower pair (pin 16). R43 sets the mixer input impedance at 3.6 kΩ. The mixer output impedance of 1.8 kΩ will properly match the input impedance of a ceramic filter which is used as a bandpass filter coupling the mixer output to the IF limiting amplifier.

IF LIMITER

The IF amplifier consists of six differential gain stages, with the input impedance set by R2 at 1.8 kΩ to properly terminate the ceramic filter driving the IF. The IF alone (without mixer) has a −3 dB limiting sensitivity of approximately 50 μV. The system bandwidth is limited to about 5 MHz due to high impedances in the IF which are necessary to meet low power requirements. The IF output is connected to the external quad coil at pin 8 via an internal 10 pF capacitor.

FM DEMOD AUDIO OUT

A conventional quadrature detector is used to demodulate the FM signal. The Q of the quad coil, which is determined by the external resistor placed across it, has multiple affects on the audio output. Increasing the Q increases output level but because of nonlinearities in the tank phase characteristic, also increases distortion (see Typical Performance Characteristics). For proper operation, the voltage swing on pin 8 should be adequate to drive the upper rank of the multiplier into switching (about 100 mVrms). This voltage level is dependent on the internal 10 pF capacitor and the tank R_p voltage divider network. After detection and de-emphasis, the audio output at pin 9 is buffered by an emitter follower.

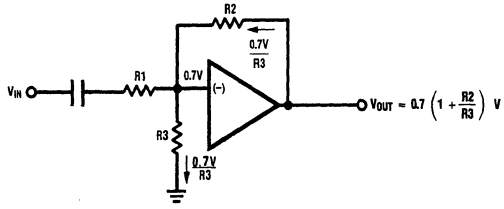
OP AMP

The op amp inverting input (pin 10) which is internally referenced to .7V, receives dc bias from the output at pin 11 through the external feedback network. Because of the low D.C. bias, maximum swing on the op amp output with 10% distortion is 500mVrms. This can be increased when operating on supplies over 2.3V by adding a resistor from the op amp input to ground which raises the quiescent D.C. at the output allowing more swing (see figure below for selection of added resistor). The op amp is normally utilized as either a bandpass filter to extract a specific frequency from the audio output, such as a ring or dial tone, or as a high pass filter to detect noise due to no input at the mixer. The latter condition will generate a signal at the op amp oput, which when applied to pin 12 can mute the external audio amp.

for max swing: $V_{OUT} = (V_S - V_{BE})/2$ (from internal circuit)

$$\text{so } (V_S - V_{BE})/2 = .7\left(1 + \frac{R2}{R3}\right)$$

$$\text{and } * \frac{R2}{R3} = \left(\frac{V_S - V_{BE}}{1.4}\right) - 1$$



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Increasing OP Amp Swing

SQUELCH TRIGGER CIRCUIT

The squelch trigger circuit is configured such that a low bias on the input (pin 12) will force pin 13 high (200 mV below supply), where it can support at least a 1 mA load, and pin 14 to be a low impedance, typically 15Ω to ground. Connecting pin 14 to a high impedance ground reference point in the audio path between pin 9 and the audio amp will mute the audio output. Pulling pin 12 above mute threshold (.65V) will force pin 13 to an impedance of about 60 kΩ to ground and pin 14 will be an open circuit. There is 100 mV of hysterisis at pin 12 which effectively prevents jitter.

National Semiconductor

PRELIMINARY

LMC835 Digital Controlled Graphic Equalizer

General Description

The LMC835 is a monolithic, digitally-controlled graphic equalizer CMOS LSI for Hi-Fi audio. The LMC835 consists of a Logic section and a Signal Path section made of analog switches and thin-film silicon-chromium resistor networks. The LMC835 is used with external resonator circuits to make a stereo equalizer with seven bands, ±12 dB or ±6 dB gain range and 25 steps each. Only three digital inputs are needed to control the equalization. The LMC835 makes it easy to build a μP-controlled equalizer.

The signal path is designed for very low noise and distortion, resulting in very high performance, compatible with PCM audio.

Features

- No volume controls required
- Three-wire interface
- 14 bands, 25 steps each
- ±12 dB or ±6 dB gain ranges
- Low noise and distortion
- TTL, CMOS logic compatible

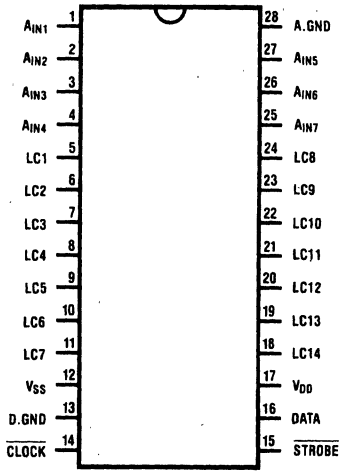
Applications

- Hi-Fi equalizer
- Receiver
- Car stereo
- Musical instrument
- Tape equalization
- Mixer
- Volume controller

Connection Diagram

Order Number LMC835N
See NS Package N28B

Dual-In-Line Package



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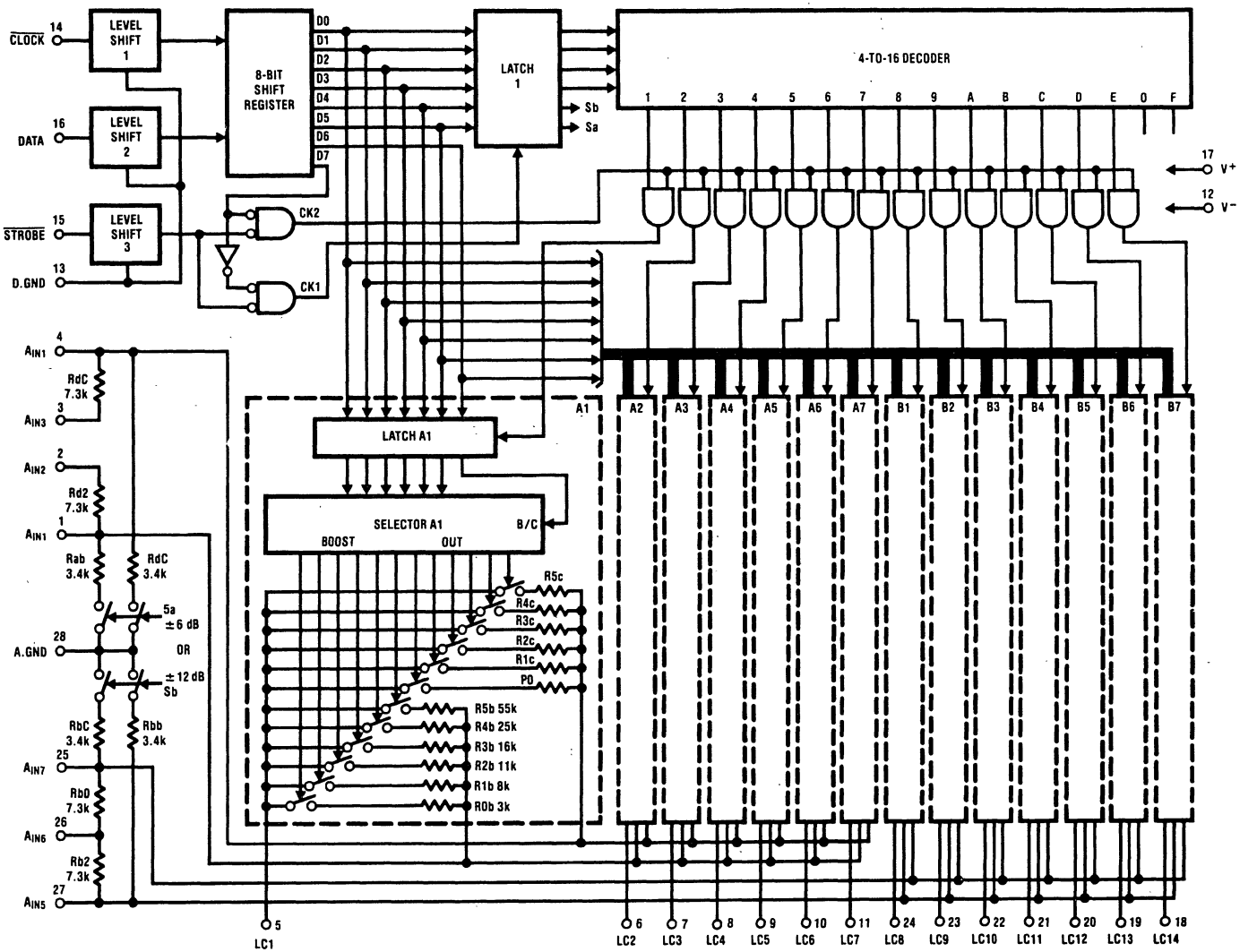
Top View

Block Diagram



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LMC835

Absolute Maximum Ratings

Supply Voltage, $V_{DD}-V_{SS}$	18V
Allowable Input Voltage (Note 1)	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Storage Temperature, T_{stg}	$-60°C$ to $+150°C$
Lead Temperature (Soldering, 10 sec), T_L	$+300°C$

Operating Ratings

Supply Voltage, $V_{DD}-V_{SS}$	5V to 16V
Digital Ground (Pin 13)	V_{SS} to V_{DD}
Digital Input (Pins 14, 15, 16)	V_{SS} to V_{DD}
Analog Input (Pins 1, 2, 3, 4, 25, 26, 27) (Note 1)	V_{SS} to V_{DD}
Operating Temperature, T_{ope}	$-40°C$ to $+85°C$

Electrical Characteristics (Note 2) $V_{DD}=7.5V$, $V_{SS}=-7.5V$, A.GND = 0V

LOGIC SECTION

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
I_{DDL}	Supply Current	Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{SSL}		Pins 14, 15, 16 are 0V	0.01	0.5	**0.5**	mA (Max)
I_{DDH}		Pins 14, 15, 16 are 5V	1.3	5	**5**	mA (Max)
I_{SSH}		Pins 14, 15, 16 are 5V	0.9	5	**5**	mA (Max)
V_{IH}	High-Level Input Voltage	@Pins 14, 15, 16	1.8	2.3	**2.5**	V (Min)
V_{IL}	Low-Level Input Voltage	@Pins 14, 15, 16	0.9	0.6	**0.4**	V (Max)
f_o	Clock Frequency	@Pin 14	2000	500	**500**	kHz (Max)
$t_{w(\overline{STB})}$	Width of $\overline{STB}$ Input	See *Figure 1*	0.25	1	**1**	μS (Min)
t_{setup}	Data Setup Time	See *Figure 1*	0.25	1	**1**	μS (Min)
t_{hold}	Data Hold Time	See *Figure 1*	0.25	1	**1**	μS (Min)
t_{cs}	Delay from Rising Edge of $\overline{CLOCK}$ to $\overline{STB}$	See *Figure 1*	0.25	1	**1**	μS (Min)
I_{IN}	Input Current	@Pins 14, 15, 16 $0V<V_{IN}<5V$	±0.01	±1		μA (Max)
C_{IN}	Input Capacitance	@Pins 14, 15, 16 f = 1 MHz	5			pF

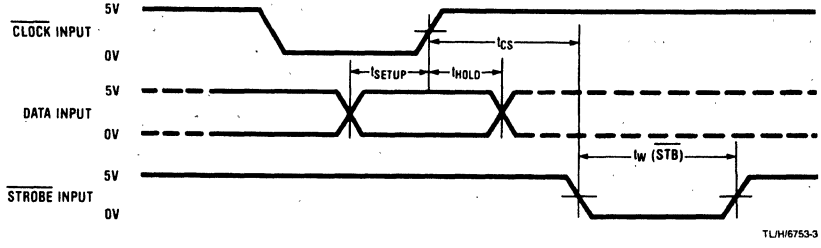
Note 1: Pins 2, 3 and 26 have a maximum input voltage range of ±22V for the typical application shown in *Figure 7*.

Note 2: Bold numbers apply at temperature extremes. All other numbers apply at $T_A=25°C$, $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND = A.GND = 0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagram



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Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 1

Electrical Characteristics (Note 2) $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND=A.GND=0V

SIGNAL PATH SECTION

Symbol	Parameter	Test Conditions	Typ	Tested Limit (Note 3)	Design Limit (Note 4)	Unit (Limit)
AA_V	Gain Error	$A_V=0$ dB @ ± 12 dB Range	0.1	0.5	**0.5**	dB (Max)
		$A_V=0$ dB @ ± 6 dB Range	0.1	1	**1**	dB (Max)
		$A_V=\pm1$ dB @ ± dB Range (R_{b5} or R_{c5} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm2$ dB @ ± 12 dB Range (R_{b4} or R_{c4} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm3$ dB @ ± 12 dB Range (R_{b3} or R_{c3} is ON)	0.1	0.5	**0.6**	dB (Max)
		$A_V=\pm4$ dB @ ± 12 dB Range (R_{b2} or R_{c2} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V=\pm5$ dB @ ± 12 dB Range (R_{b1} or R_{c1} is ON)	0.1	0.5	**0.7**	dB (Max)
		$A_V=\pm9$ dB @ ± 12 dB Range (R_{b0} or R_{c0} is ON)	0.2	1	**1.3**	dB (Max)
THD	Total Harmonic	$A_V=0$ dB @ ± 12 dB Range $V_{IN}=4V_{rms}$, f=1 kHz	0.0015			%
		$A_V=12$ dB @ ± 12 dB Range				
		$V_{IN}=1V_{rms}$, f=1 kHz	0.01	0.1		% (Max)
		$V_{IN}=1V_{rms}$, f=20 kHz	0.1	0.5		% (Max)
		$A_V=-12$ dB @ ± 12 dB Range				
		$V_{IN}=4V_{rms}$, f=1 kHz	0.01	0.1		% (Max)
		$V_{IN}=4V_{rms}$, f=20 kHz	0.1	0.5		% (Max)
$V_{O\ Max}$	Maximum Output Voltage	$A_V=0$ dB @ ± 12 dB Range THD <1%, f=1 kHz	5.5	5.1	**5**	V_{rms} (Min)
S/N	Signal to Noise	$A_V=0$ dB @ ± 12 dB Range $V_{ref}=1\ V_{rms}$	114			dB
		$A_V=12$ dB @ ± 12 dB Range $V_{ref}=1V_{rms}$	106			dB
		$A_V=-12$ dB @ ± 12 dB Range $V_{ref}=1V_{rms}$	116			dB
I_{LEAK}	Leakage Current	$A_V=0$ dB @ ± 12 dB Range (All internal switches are OFF)				
		Pin 2+3, Pin 26		500		nA (Max)
		Pin 5 ~ Pin 11, Pin 18 ~ Pin 24		50		nA (Max)

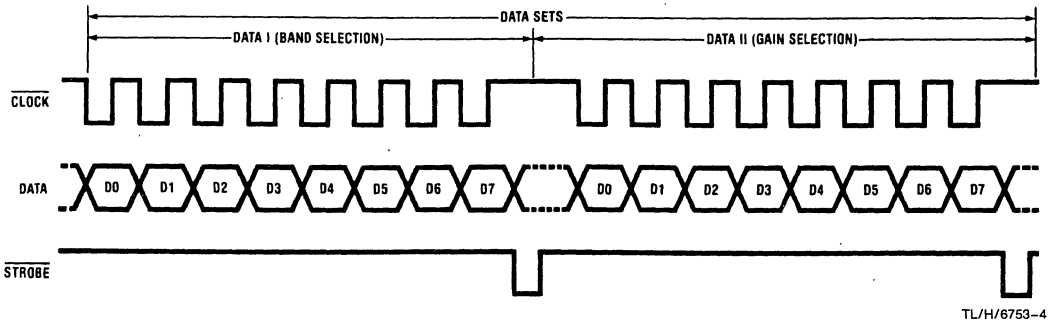
Note 1: Pins 2, 3 and 26 have a maximum input voltage range of ±22V for the typical application shown in *Figure 7*.

Note 2; Boldface numbers apply at temperature extremes. All other numbers apply at $T_A=25°C$, $V_{DD}=7.5V$, $V_{SS}=-7.5V$, D.GND=A.GND=0V as shown in the test circuit, *Figures 3* and *4*.

Note 3: Guaranteed and 100% production tested.

Note 4: Guaranteed (but not 100% production tested) over the operating temperature range. These limits are not used to calculate outgoing quality levels.

Timing Diagrams



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Note: To change the gain of the presently selected band, it is not necessary to send DATA 1 (Band Selection) each time.

FIGURE 2

Truth Tables

DATA I (Band Selection)

D7	D6	D5	D4	D3	D2	D1	D0	
H	X	L	L	L	L	L	L	(Ch A: Band 1 ~ 7, Ch B: Band 8 ~ 14)
H	X	L	L	L	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	L	L	L	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 1
H	X	L	L	L	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 2
H	X	L	L	L	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 3
H	X	L	L	L	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 4
H	X	L	L	L	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 5
H	X	L	L	L	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 6
H	X	L	L	H	L	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 7
H	X	L	L	H	L	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 8
H	X	L	L	H	L	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 9
H	X	L	L	H	L	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 10
H	X	L	L	H	H	L	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 11
H	X	L	L	H	H	L	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 12
H	X	L	L	H	H	H	L	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 13
H	X	L	L	H	H	H	H	Ch A ± 12 dB Range, Ch B ± 12 dB Range, Band 14
H	X	L	H	Valid Binary Input				Ch A ± 12 dB Range, Ch B ± 12 dB Range, No Band Selection
H	X	H	L	Valid Binary Input				Ch A ± 12 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14
H	X	H	H	Valid Binary Input				Ch A ± 6 dB Range, Ch B ± 12 dB Range, Band 1 ~ 14
↑ ①	↑ ②	↑ ③	↑ ④	← Band Code →				Ch A ± 6 dB Range, Ch B ± 6 dB Range, Band 1 ~ 14

① DATA 1
② Don't Care
③ Ch A ±6 dB/±12 dB Range
④ Ch B ±6 dB/±12 dB Range

This is the gain if the ±12 dB range is selected by DATA I. If the ±6 dB range is selected, then the values shown must be approximately halved. See the characteristics curves for more exact data.

DATA II (Gain Selection)

	D7	D6	D5	D4	D3	D2	D1	D0
Flat	L	X	L	L	L	L	L	L
1 dB Boost	L	H	H	L	L	L	L	L
2 dB Boost	L	H	L	H	L	L	L	L
3 dB Boost	L	H	L	L	H	L	L	L
4 dB Boost	L	H	L	L	L	H	L	L
5 dB Boost	L	H	L	L	L	L	H	L
6 dB Boost	L	H	L	H	L	L	H	L
7 dB Boost	L	H	H	L	H	L	H	L
8 dB Boost	L	H	L	H	L	H	H	L
9 dB Boost	L	H	L	L	L	L	L	H
10 dB Boost	L	H	H	L	H	L	L	H
11 dB Boost	L	H	H	L	H	H	L	H
12 dB Boost	L	H	H	L	H	H	H	H
1 dB ~ 12 dB Cut	L	L	Valid Above Input					
	↑ ⑤	↑ ⑥	← Gain Code →					

⑤ DATA II
⑥ Boost/Cut

Test Circuits

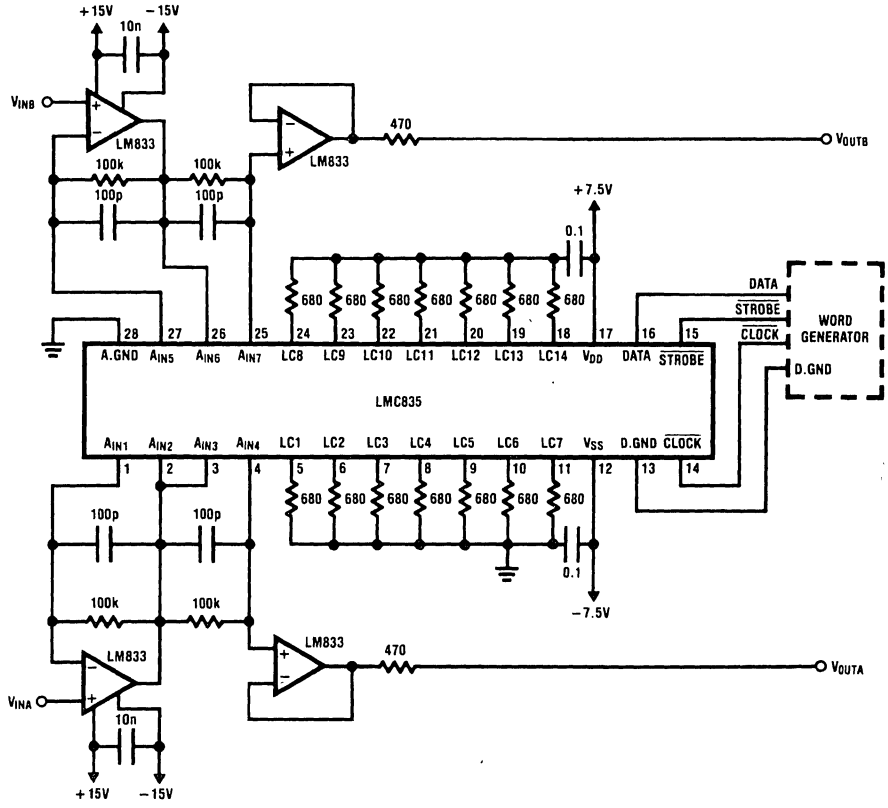

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FIGURE 3. Test Circuit for AC Measurement

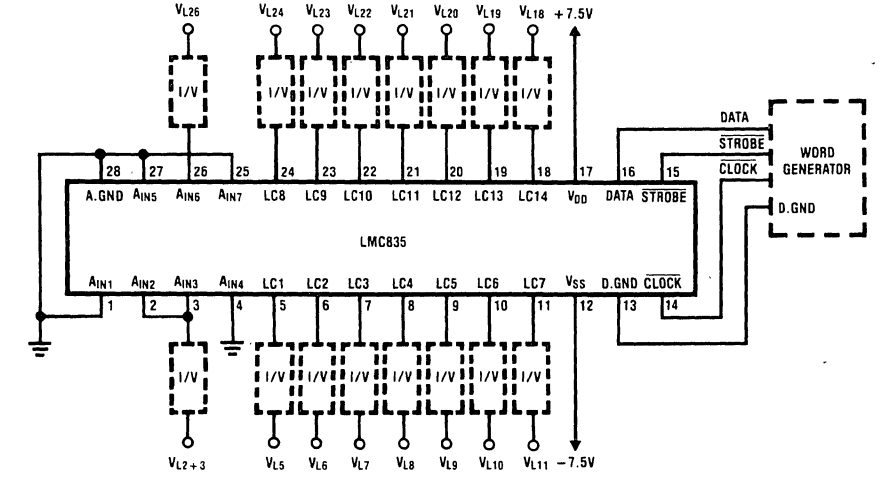

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FIGURE 4. Test Circuit for Leakage Current Measurement

Test Circuits (Continued)

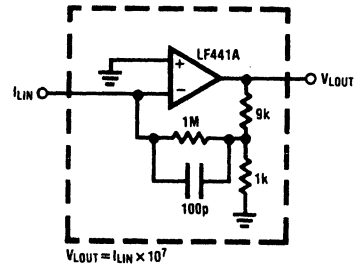

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FIGURE 5. I to V Converter

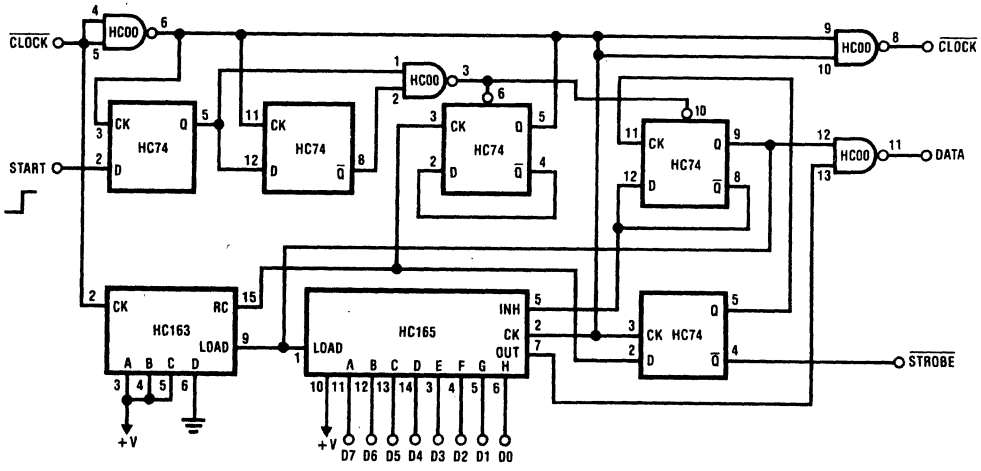

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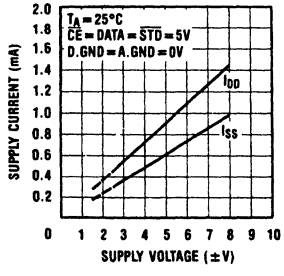
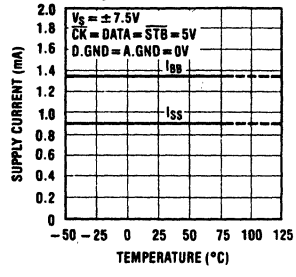
FIGURE 6. Simple Word Generator

Typical Performance Characteristics

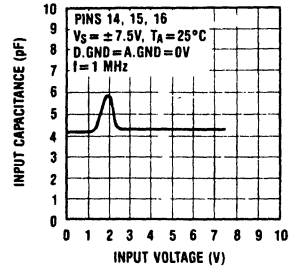
Supply Current vs Supply Voltage



Supply Current vs Temperature



Input Capacitance vs Input Voltage



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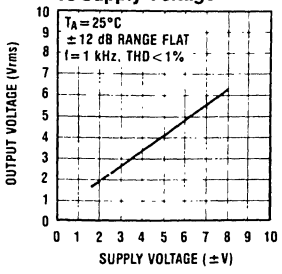
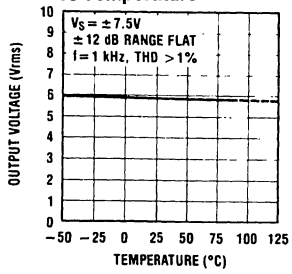
Typical Performance Characteristics (Continued)

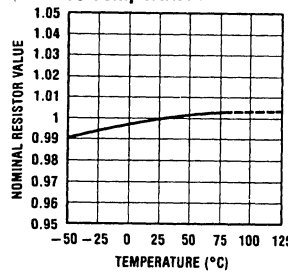
Maximum Output Voltage vs Supply Voltage



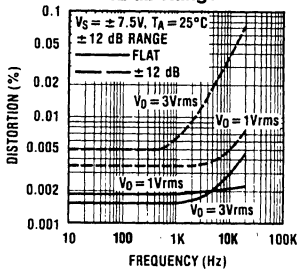
Maximum Output Voltage vs Temperature



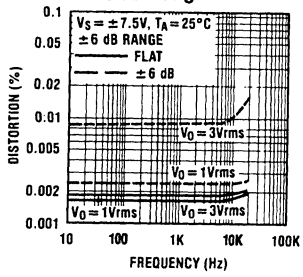
Nominal Resistor vs Temperature



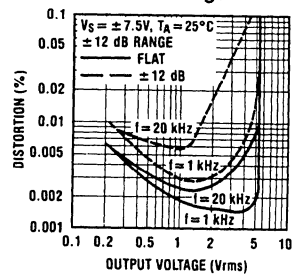
Distortion vs Frequency @ ± 12 dB Range



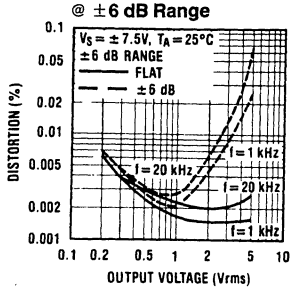
Distortion vs Frequency @ ±6 dB Range



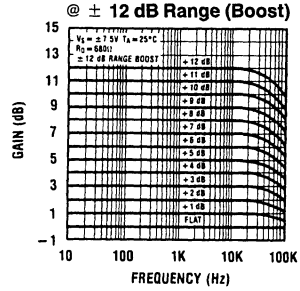
Distortion vs Output Voltage @ ± 12 dB Range



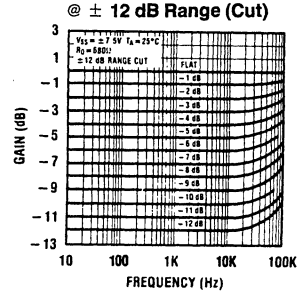
Distortion vs Output Voltage @ ±6 dB Range



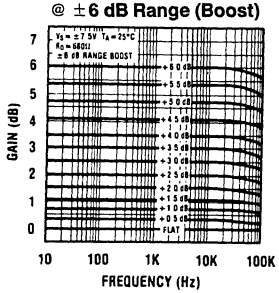
Gain vs Frequency @ ± 12 dB Range (Boost)



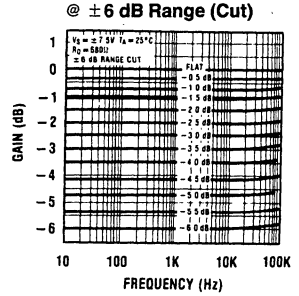
Gain vs Frequency @ ± 12 dB Range (Cut)



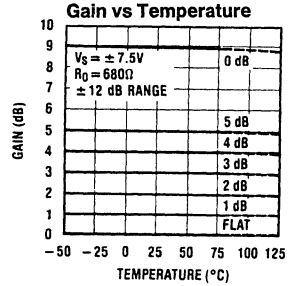
Gain vs Frequency @ ±6 dB Range (Boost)



Gain vs Frequency @ ±6 dB Range (Cut)



Gain vs Temperature



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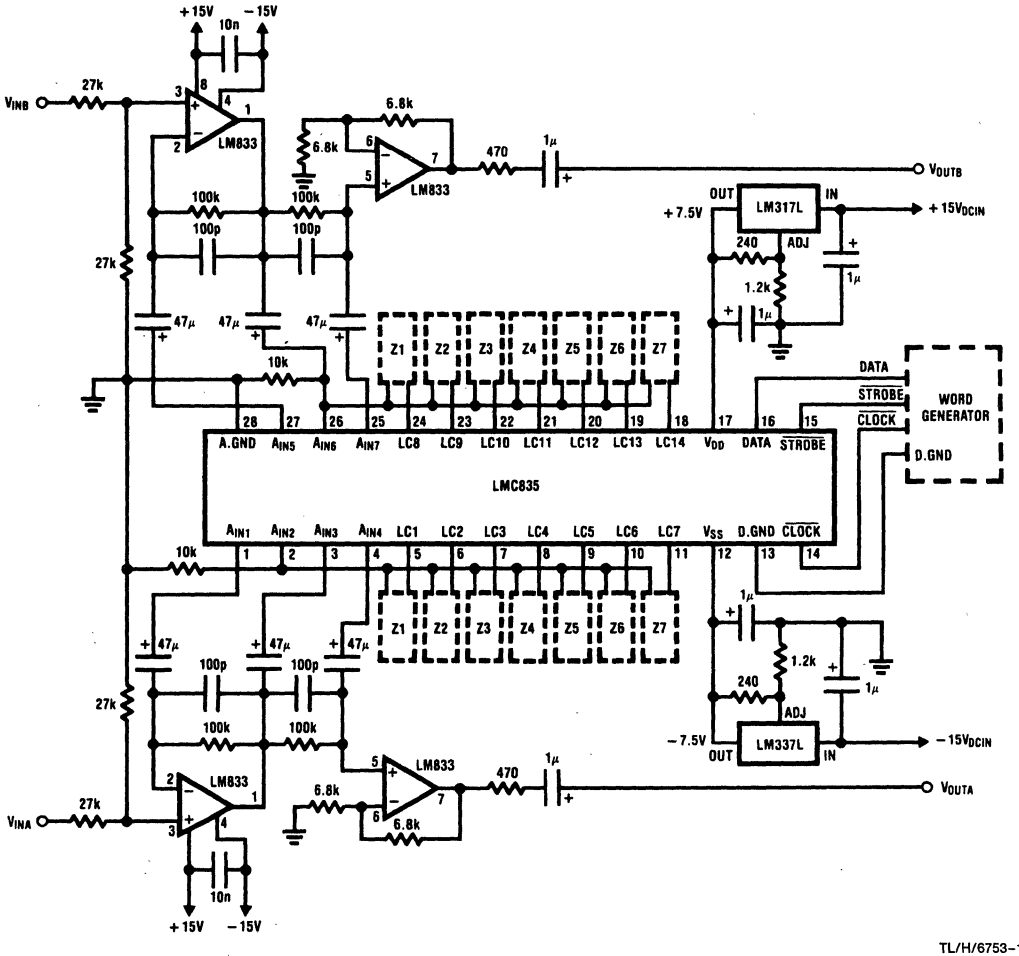
Typical Applications

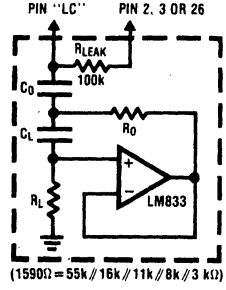


TL/H/6753–11

FIGURE 7. Stereo 7-Band Equalizer

TABLE I: Tuned Circuit Elements

$Q_0 = 3.5$, $Q_{12dB} = 1.05$					
Z1	**f_o (Hz)**	**C_O (F)**	**C_L (F)**	**R_L (Ω)**	**R_O (Ω)**
Z1	63	1µ	0.1µ	100k	680
Z2	160	0.47µ	0.033µ	100k	680
Z3	400	0.15µ	0.015µ	100k	680
Z4	1k	0.068µ	0.0068µ	82k	680
Z5	2.5k	0.022µ	0.0033µ	82k	680
Z6	6.3k	0.01µ	0.0015µ	62k	680
Z7	16k	0.0047µ	680p	47k	680



$$L_O = C_L R_L R_O$$

$$f_O = \frac{1}{2\pi\sqrt{L_O C_O}}$$

$$Q_O = \sqrt{\frac{L_O}{C_O R_O^2}}$$

$$Q_{12\,dB} = \frac{R_O Q_O}{R_O + 1590}$$

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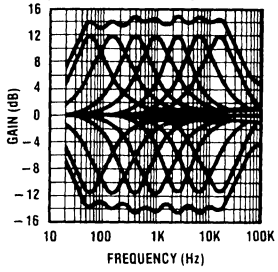
FIGURE 8. Tuned Circuit for Stereo 7-Band Equalizer (*Figure 7*)

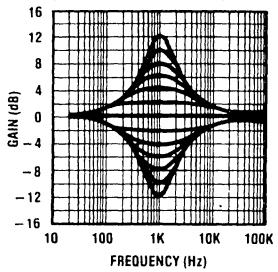
Typical Applications (Continued)

Performance Characteristics (Circuit of *Figure 7*)

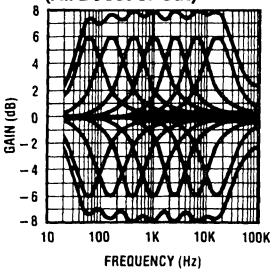
LM835 Gain vs Frequency @ ± 12 dB Range (All Boost or Cut)



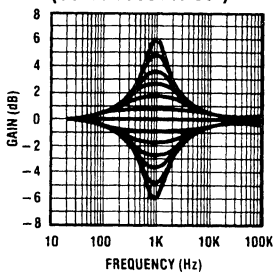
LM835 Gain vs Frequency @ ± 12 dB Range (1 kHz Boost or Cut)



LM835 Gain vs Frequency @ ±6 dB Range (All Boost or Cut)



LM835 Gain vs Frequency @ ±6 dB Range (1 kHz Boost or Cut)



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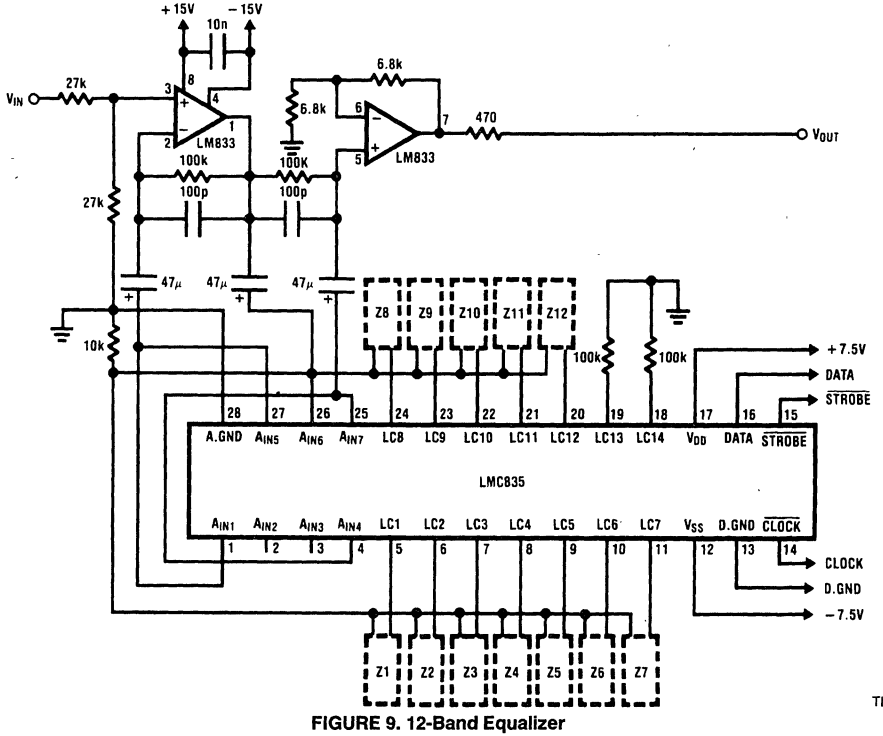

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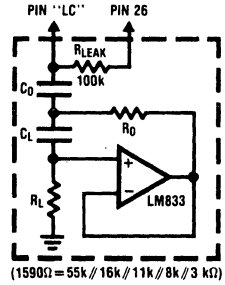
FIGURE 9. 12-Band Equalizer

Typical Applications (Continued)

TABLE II. Tuned Circuit Elements

$Q_0 = 4.7$, $Q_{12\,dB} = 1.4$					
	f_0 (Hz)	C_0 (F)	C_L (F)	R_L (Ω)	R_0 (Ω)
Z1	16	3.3μ	0.47μ	100k	680
Z2	31.5	15μ	0.22μ	110k	680
Z3	63	1μ	0.1μ	100k	680
Z4	125	0.39μ	0.068μ	91k	680
Z5	250	0.22μ	0.033μ	82k	680
Z6	500	0.1μ	0.015μ	100k	680
Z7	1k	0.047μ	0.01μ	82k	680
Z8	2k	0.022μ	0.0047μ	91k	680
Z9	4k	0.01μ	0.0022μ	110k	680
Z10	8k	0.0068μ	0.001μ	82k	680
Z11	16k	0.0033μ	680p	62k	680
Z12	32k	0.0015μ	470p	68k	510



$$L_0 = C_L R_L R_0$$

$$f_0 = \frac{1}{2\pi\sqrt{L_0 C_0}}$$

$$Q_0 = \sqrt{\frac{L_0}{C_0 R_0^2}}$$

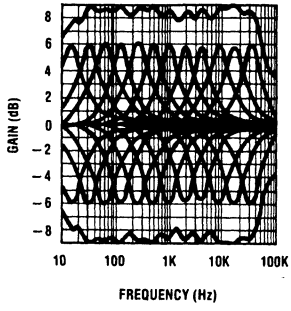
$$Q_{12\,dB} = \frac{R_0 Q_0}{R_0 + 1590}$$

TL/H/6753–15

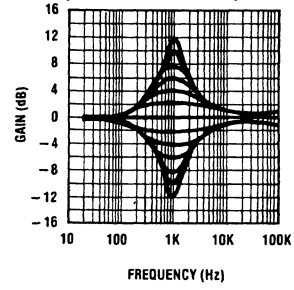
FIGURE 10. Tuned Circuit for 12-Band Equalizer (*Figure 9*)

Performance Characteristics (Circuit of Figure 9)

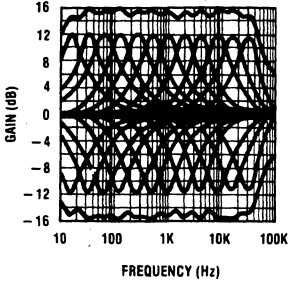
12 Band Equalizer Application
LM835 Gain vs Frequency
@ ±6 dB Range
(All Boost or Cut)



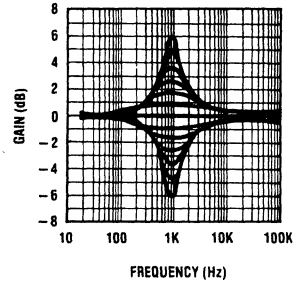
LM835 12 Band E.Q. Application
Gain vs Frequency
@ ±12 dB Range
(1 kHz Boost or Cut)



12 Band Equalizer Application
LM835 Gain vs Frequency
@ ± 12 dB Range
(All Boost or Cut)



LM835 12 Band E.Q. Application
Gain vs Frequency
@ ±6dB Range
(1 kHz Boost or Cut)



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Typical Applications (Continued)

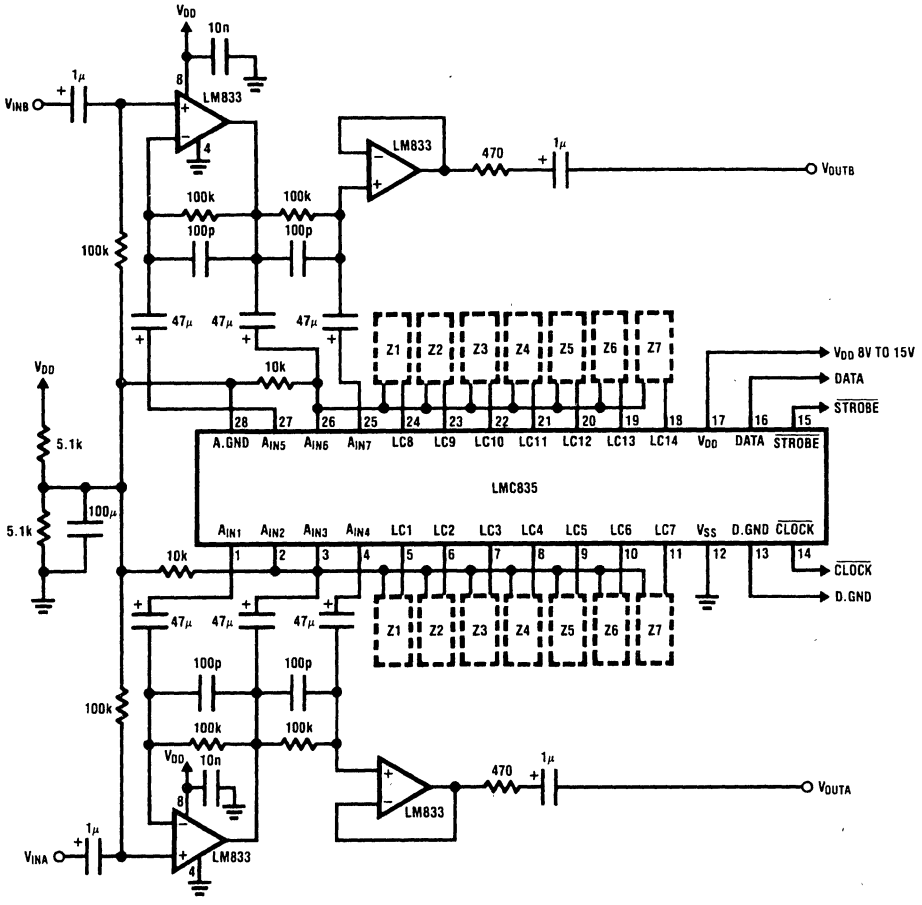

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FIGURE 11. Single Supply Stereo Equalizer

Typical Applications (Continued)

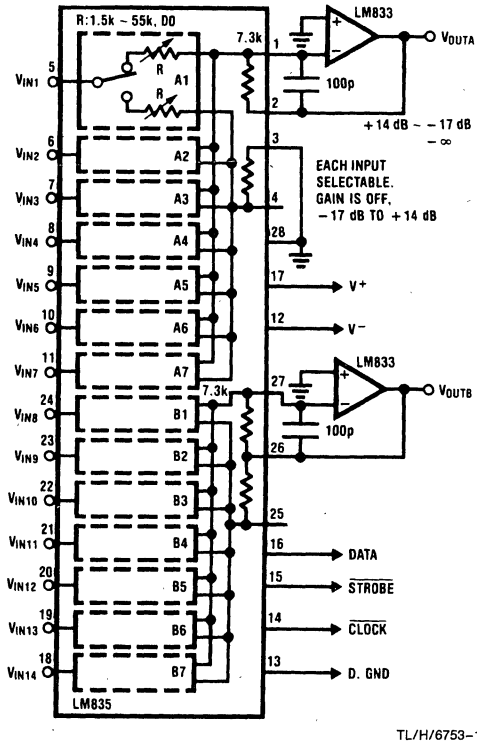

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FIGURE 12. Stereo 7-Input/1-Output Mixers (THD is not as low as equalizer circuit)

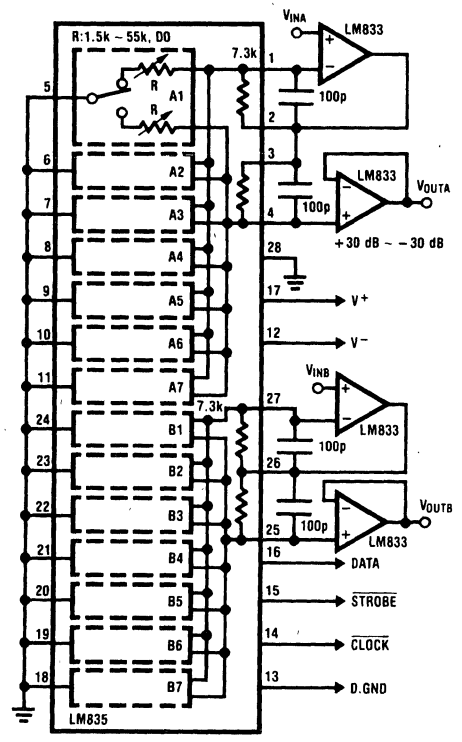

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FIGURE 13. Stereo Volume Control, Very Low THD

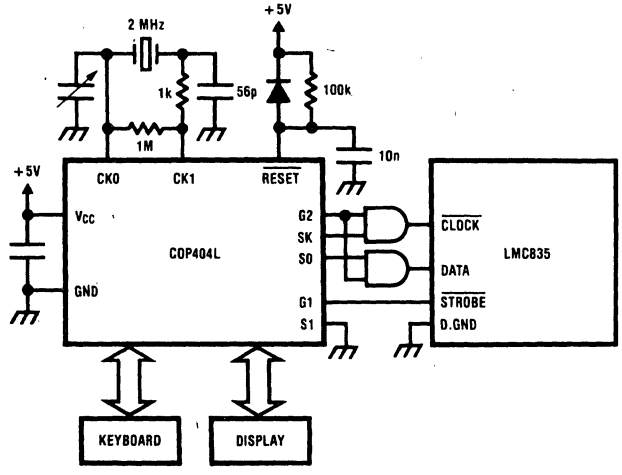

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FIGURE 14. LMC835-COP404L CPU Interface

Typical Applications (Continued)

Sample Subroutine Program for *Figure 14*, LMC835-COP404L CPU Interface

```
HEX
CODE      LABEL      MNEMONICS                    COMMENTS
3F        LMC835:    LBI      3F      ;POINT TO RAMADDRESS 3F
05        SEND       LD               ;RAMDATA TO A
22                   SC               ; SET CARRY
335F                 OGI              ;SET PORT G= 1111, OPEN THE AND GATES
4F                   XAS              ;SWAP A AND SIO, CLOCK START
05                   LD               ;RAMDATA TO A, MAKE SURE A = DATA
07                   XDS              ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
05                   LD               ;RAMDATA TO A
4F                   XAS              ;SWAP A AND SIO
05                   LD               ;RAMDATA TO A, MAKE SURE A=NEWDATA
07                   XDS              ;SWAP A AND RAMDATA, RAMADDRESS=RAMADDRESS-1
32                   RC               ;RESET CARRY
4F                   XAS              ;SWAP A AND SIO, CLOCK STOP
335D                 OGJ      13      ;SET PORT G=1101, MAKE STROBE LOW
335B                 OGI      11      ;SET PORT G=1011, MAKE STROBE HIGH, CLOSE THE
                                                                    GATES
4E                   CBA              ;BD TO A
43                   AISC     3       ;RAMADDRESS<3C THEN RETURN
48                   RET
80                   JP       SEND
```

```
      RAM
   ADDRESS          COMMENTS
3C      DATA    ;GAIN DATA D4-D7
3D      DATA    ;GAIN DATA D0-D3
3E      DATA    ;BAND DATA D4-D7
3F      DATA    ;BAND DATA D0-D3
```

Application Hints

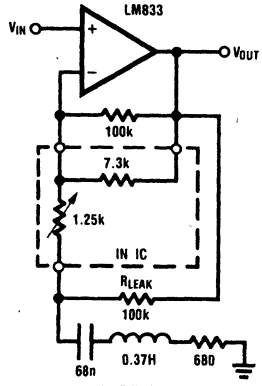
SWITCHING NOISE

The LMC835 uses CMOS analog switches that have small leakages (less than 50 nA). When a band is selected for flat gain, all the switches in that band are open and the resonator circuit is not connected to the LMC835 resistor network. It is only in the flat mode that the small leakage currents can cause problems. The input to the resonator circuit is usually a capacitor and the leakage currents will slowly charge up this capacitor to a large voltage if there is no resistive path to limit it. When the band is set to any value other than flat, the charge on the capacitor will be discharged by the resistor network and there will be a transient at the output. To limit the size of this transient, R_{LEAK} is necessary.

HOW TO AVOID SWITCHING NOISE DUE TO LEAKAGE CURRENT (Refer to *Figures 7* and *8*)

To avoid switching noise due to leakage currents when changing the gain, it is recommended to put R_{LEAK} = 100 KΩ between Pin 3 and Pin 5—11 each, Pin 26 and Pin 12—24 each. The resistor limits the voltage that the capacitor can charge to, with minimal effects on the equalization. The frequency response change due to R_{LEAK} are shown in *Figure 15*. The gain error is only 0.2 dB and Q error is only 5% at 12 dB boost or cut.

Application Hints (Continued)



MODEL

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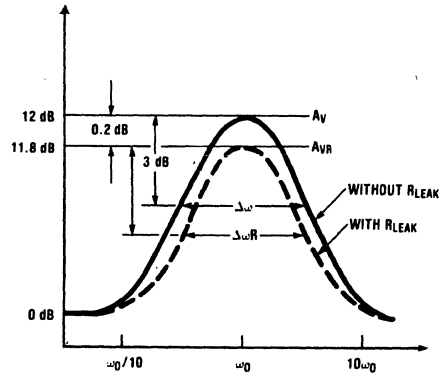


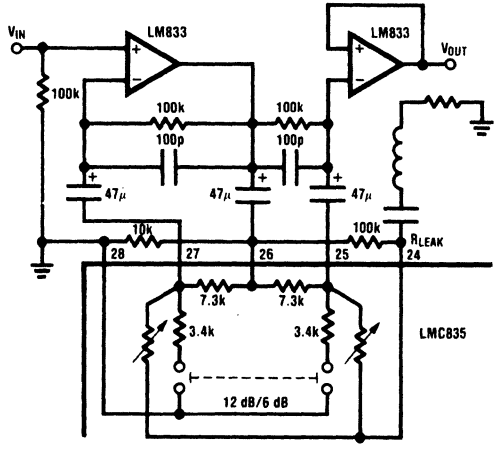
RESULT

TL/H/6753-22

FIGURE 15. Effect of R_{LEAK}

REDUCING EXTERNAL COMPONENTS

The typical application shown in *Figure 7* is switching noise free. The DC-coupled circuit in *Figure 16* is also switching noise free, except at 12 dB/6 dB switch turn ON/OFF. This switching noise is caused by the I_{bias} and V_{offset} of the op amps. Selecting a low I_{bias} and V_{offset} op amp can minimize the switching noise due to the 12 dB/6 dB switch. The DC-coupled application can also eliminate the R_F = 100k resistors with only a 0.5 dB gain error at 12 dB boost or cut.



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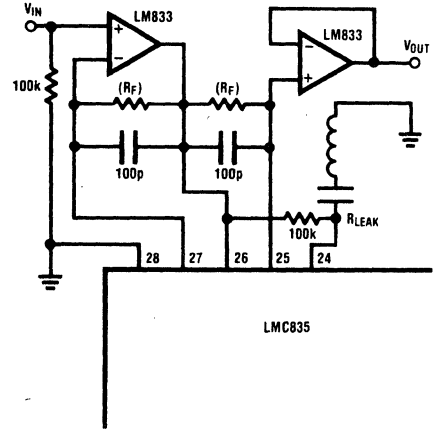
AC COUPLING



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DC COUPLING

FIGURE 16. Reducing External Components

Section 13

Telecommunications Circuits

Section Contents

National Semiconductor

microCMOS

TP3020/TP3020-1/TP3021/TP3021-1 Monolithic CODECs

General Description

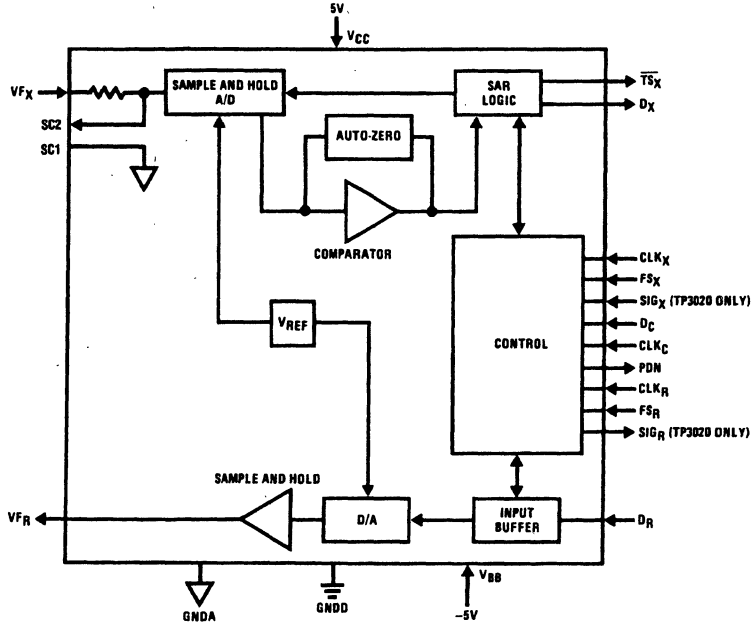
The TP3020 and TP3021 are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP3020 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The TP3021 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the TP3020/TP3021 may be operated in a fixed time slot mode. Both devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- Low operation power—45 mW typical
- Low standby power—1 mW typical
- ±5V operation
- TTL compatible digital interface
- Time slot assignment or alternate fixed time slot modes
- Internal precision reference
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP3020—μ-law coding with signaling capabilities
- TP3021—A-law coding
- Synchronous or asynchronous operation

Simplified Block Diagram



TL/H/5538–1

S 13

Absolute Maximum Ratings

Operating Temperature	−25°C to + 125°C	Voltage at Any Analog Input or Output	V_{BB} −0.3V to V_{CC} + 0.3V
Storage Temperature	−65°C to + 150°C	Voltage at Any Digital Input or Output	GNDD −0.3V to V_{CC} + 0.3V
V_{CC} with Respect to GNDD	7V	Lead Temperature (Soldering, 10 seconds)	300°C
V_{BB} with Respect to GNDD	−7V		

DC Electrical Characteristics

Unless otherwise noted $T_A = 0°C$ to 70°C, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$. Typical characteristics are specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$ and $T_A = 25°C$. All digital signals are referenced to GNDD. All analog signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0 < V_{IN} < V_{CC}$	−10		10	μA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, $I_{OL} = 4.0$ mA SIG_R, $I_{OL} = 0.5$ mA $\overline{TS}_X$, $I_{OL} = 3.2$ mA, Open Drain PDN, $I_{OL} = 1.6$ mA			0.4 0.4 0.4 0.4	V V V V
V_{OH}	Output High Voltage	D_X, $I_{OH} = 6$ mA SIG_R, $I_{OH} = 0.6$ mA	2.4 2.4			V V
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2.0			kΩ
Z_O	Output Impedance at VF_R	$-3.1V < VF_R < 3.1V$		10	20	Ω
V_{OS}	Output Offset Voltage at VF_R	D_R = PCM Zero Code (TP3020) or Alternating ± 1 Code (TP3021)	−25		25	mV
I_{IN}	Analog Input Bias Current	$V_{IN} = 0V$	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				160	kΩ
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}			0.1	0.4	mA
I_{BB0}	Standby Current, V_{BB}			0.03	0.1	mA
I_{CC1}	Operating Current, V_{CC}			4.5	8.0	mA
I_{BB1}	Operating Current, V_{BB}			4.5	8.0	mA

Note: TP3020-1 specifications are the same as those for TP3020 except where noted. Similarly, TP3021-1 specifications are the same as TP3021 except where noted.

AC Electrical Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP3020 and TP3021 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the TP3020/TP3021 are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute TP3020, TP3021 TP3020-1, TP3021-1	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	 −0.125 −0.175		 0.125 0.175	 dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%	−0.07		0.07	dB
G_{XA}	Transmit Gain, Absolute TP3020, TP3021 TP3020-1, TP3021-1	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	 −0.325 −0.375		 −0.075 −0.025	 dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%	−0.07		0.07	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 −0.3 −0.2 −0.4 −1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 −0.3 −0.2 −0.4 −1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB
S/D_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 35 29 25			 dBc dBc dBc
S/D_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 35 29 25			 dBc dBc dBc
N_R	Receive Idle Channel Noise	D_R = Steady State PCM Code			6	dBrnc0
N_X	Transmit Idle Channel Noise	TP3020, VF_X = 0V (No Signaling) TP3021, VF_X = 0V			13 −66*	dBrnc0 dBn0p
HD_R	Receive Harmonic Distortion	2nd or 3rd Harmonic			−47	dB
HD_X	Transmit Harmonic Distortion	2nd or 3rd Harmonic			−47	dB

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AC Electrical Characteristics (Continued) Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

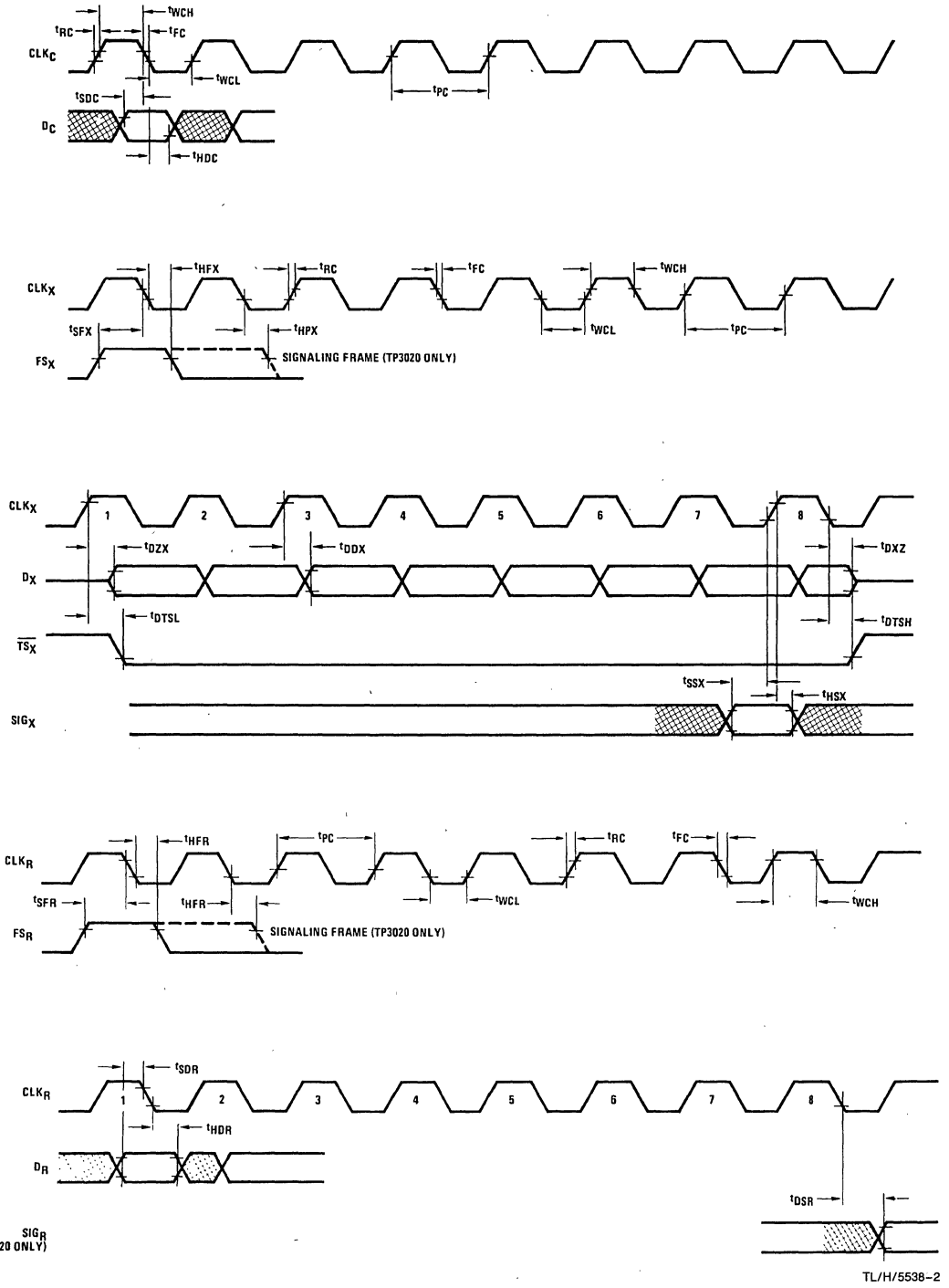
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, V_{CC} = 5.0 V_{DC} + 200 mVrms, f = 1.02 kHz	50			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{CC} = 5.0 V_{DC} + 200 mVrms, F = 1.02 kHz	40			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, V_{BB} = −5.0 V_{DC} + 200 mVrms, f = 1.02 kHz	50			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{BB} = −5.0 V_{DC} + 200 mVrms, f = = 1.02 kHz	45			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			−75	dB
CT_{RX}	Receive to Transmit Crosstalk	Transmit Input Level = 0V TP3020 TP3021			 −70 −65*	 dB dB

*Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Timing Specification Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0 ± 5%, V_{BB} = −5.0 ± 5%. All digital signals are referenced to GNDD and measured at V_{IL} and V_{IH} levels as indicated in the Timing Waveforms.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PC}	Period of Clock	CLK_C, CLK_R, CLK_X	485			ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	CLK_C, CLK_R, CLK_X			30	ns
t_{WCH}	Width of Clock High	CLK_C, CLK_R, CLK_X	165			ns
t_{WCL}	Width of Clock Low	CLK_C, CLK_R, CLK_X	165			ns
$t_{A/D}$	A/D Conversion Time	From End of Encoder Time Slot to Completion of Conversion			16	Time Slots
$t_{D/A}$	D/A Conversion Time	From End of Decoder Time Slot to Transition of VF_R			2	Time Slots
t_{SDC}	Set-Up Time, D_C to CLK_C		100			ns
t_{HDC}	Hold Time, CLK_C to DC		100			ns
t_{SFC}	Set-Up Time, FS_X or CLK_X		100			ns
t_{HFX}	Hold Time, CLK_X to FS_X		100			ns
t_{DZX}	Delay Time to Enable D_X on TS Entry	C_L = 150 pF	25		125	ns
t_{DDX}	Delay Time, CLK_X to D_X	C_L = 150 pF			125	ns
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	C_L = 0 pF	50		165	ns
t_{DTSL}	Delay to $\overline{TS}_X$ Low	0 ≤ C_L ≤ 150 pF	30		185	ns
t_{DTSH}	Delay to $\overline{TS}_X$ Off	C_L = 0 pF	30		185	ns
t_{SSX}	Set-Up Time, SIG_X to CLK_X		100			ns
t_{HSX}	Hold Time, CLK_X to SIG_X		100			ns
t_{SFR}	Set-Up Time, FS_R to CLK_R		100			ns
t_{HFR}	Hold Time, CLK_R to FS_R		100			ns
t_{SDR}	Set-Up Time, D_R to CLK_R		40			ns
t_{HDR}	Hold Time, CLK_R to D_R		30			ns
t_{DSR}	Delay Time, CLK_R to SIG_R	C_L = 100 pF			300	ns

Timing Waveforms



TL/H/5538–2

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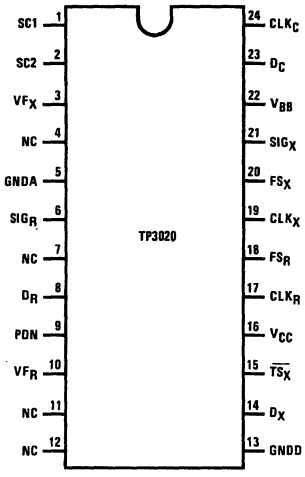
Connection Diagrams

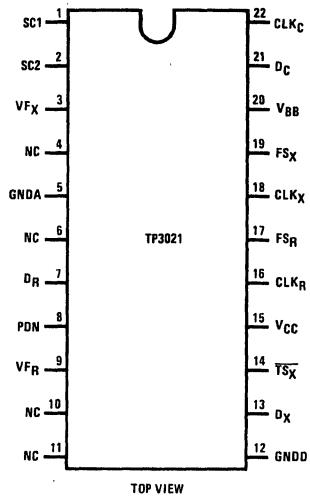
Dual-In-Line Package



Order Number
TP3020J, TP3020J-1
See NS Package J24A

TL/H/5538–3

Dual-In-Line Package



Order Number
TP3021J, TP3021J-1
See NS Package J22A

TL/H/5538–4

Description of Pin Functions

TP3020

Pin No.	Name	Function
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatibility.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output—SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
7	NC	Unused
8	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
9	PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.

TP3020 (Continued)

Pin No.	Name	Function
10	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μS after the end of the decode time slot.
11	NC	Unused
12	NC	Unused
13	GNDD	Digital ground. All digital levels are referenced to this pin.
14	D_X	Serial CM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
15	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
16	V_{CC}	5V (±5%) input.
17	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MH_Z, 1.544 MH_Z or 2048 MHz. May be asynchronous with CLK_X or CLK_C.
18	FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.

Description of Pin Functions (Continued)

TP3020 (Continued)

Pin No.	Name	Function
19	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
20	FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.
21	SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
22	V_{BB}	−5V (±5%) input.
23	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
24	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3020/TP3021 into the fixed time slot mode.

TP3021

Pin No.	Name	Function
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatibility.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	NC	Unused
7	D_R	Serial PCM data input to the encoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
8	PDN	Open drain output which turns off when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.

TP3021 (Continued)

Pin No.	Name	Function
9	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μS after the end of the decode time slot.
10	NC	Unused
11	NC	Unused
12	GNDD	Digital ground. All digital levels are referenced to this pin.
13	D_X	Serial PCM TRI-STATE output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
14	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
15	V_{CC}	(5V ±5%) input.
16	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_X or CLK_C.
17	FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide.
18	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz 1.544 MHz, or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
19	FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide.
20	V_{BB}	−5V (±5%) input.
21	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
22	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3020/TP3021 into the fixed time slot mode.

Functional Description

POWER-UP

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or −5V is required. In the power-down mode, all non-essential circuits are deactivated, the TRI-STATE PCM data output D_X is placed in the high impedance state and the receive signaling output of the TP3020, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the TP3020/TP3021 depends on the chosen mode of operation, time slot assignment or fixed time slot.

TIME SLOT ASSIGNMENT MODE

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μS or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequent control bits B3−B8 are to specify the time slot for the encoder (B1=0), the decoder (B2=0) or both (B1 and B2=0) or if the CODEC is to be placed into the power-down mode (B1 and B2=1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputted during the previously assigned time slot which may now be assigned to another CODEC.

FIXED TIME SLOT MODE

There are several ways in which the TP3020/TP3021 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_c prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

SERIAL CONTROL PORT

When the TP3020/TP3021 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	Action
0	0	Assign time slot to encoder and decoder
0	1	Assign time slot to encoder
1	0	Assign time slot to decoder
1	1	Power-down CODEC

B3	B4	B5	B6	B7	B8	Time Slot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

SIGNALING

The TP3020 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "½" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

Functional Description (Continued)

ENCODING DELAY

The encoding process begins immediately at the end of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μS later, resulting in an encoding delay of 125 μS. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz clock, the FS rate could be increased to 15 kHz reducing the delay from 125 μS to 67 μS.

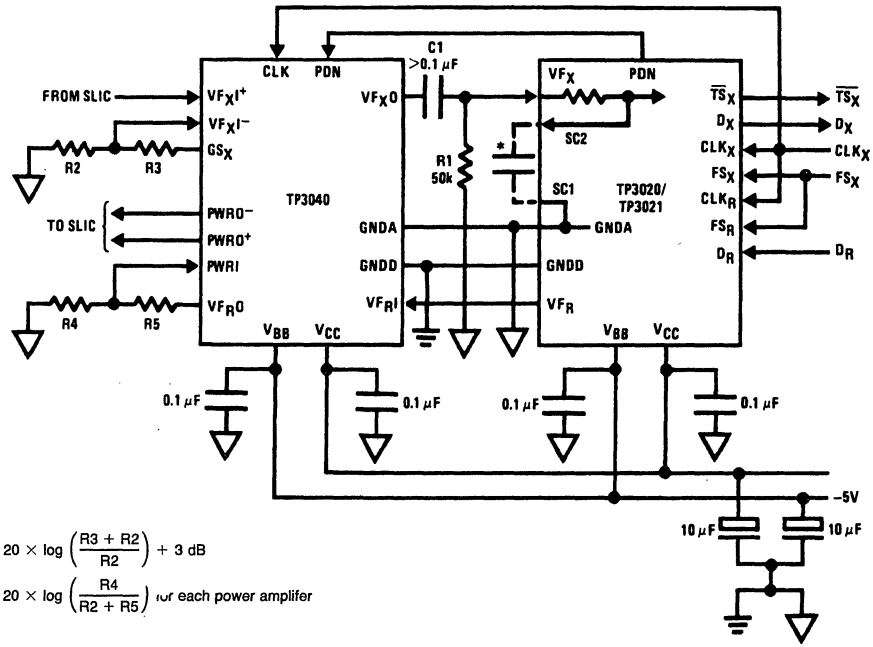
DECODING DELAY

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81 μS for a 1.544 MHz system with an 8 kHz frame rate or 76 μS for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

TYPICAL APPLICATION

A typical application of the TP3020/TP3021 used in conjunction with the TP3040 PCM filter is shown. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should not exceed 160 kΩ, and the product R1 × C1 should exceed 4 rms.

Typical Application



$$\text{XMT gain} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\ \text{dB}$$

$$\text{RCV gain} = 20 \times \log\left(\frac{R4}{R2 + R5}\right) \text{ for each power amplifer}$$

TL/H/5538–5

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of the TP3020/TP3021/TP3040, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

*The external sample/hold capacitor required for use with pin-compatible NMOS CODECs introduces attenuation due to the capacitive divider formed with C1. The SC pin connects VF_X to this sample/hold capacitor (via a 300Ω resistor) to ensure gain compatibility. The TP3020/TP3021 itself does not require an external sample/hold capacitor.

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National Semiconductor

PRELIMINARY

TP5700/TP5700-1/TP5710 Telephone Speech Circuits

General Description

The TP5700 is a linear bipolar device which includes all the functions required to build the speech circuit of a telephone. It replaces the hybrid transformer, compensation circuit and sidetone network used in traditional designs. When used with an electret microphone (with integral FET buffer) and dynamic receiver, superior audio linearity, distortion and noise performance are obtained. Loop attenuation compensation is also included.

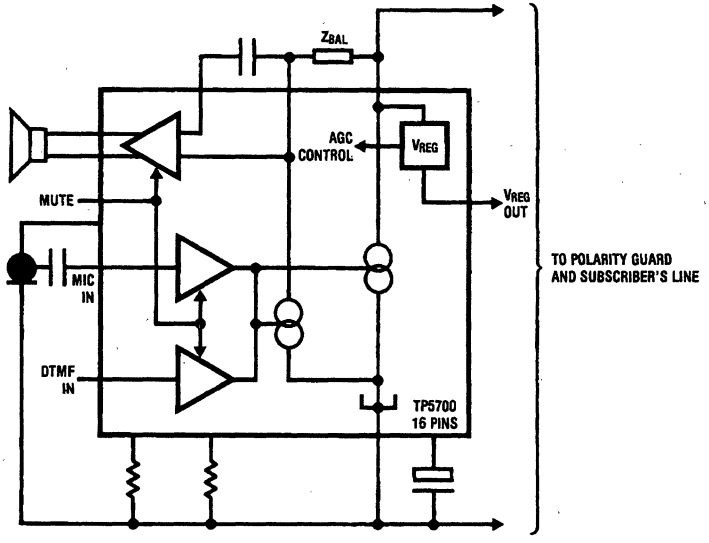
The TP5710 provides additional gain and differential inputs for use with a dynamic microphone.

The low voltage design enables the circuit to work over a wide range of operating conditions, including long loops, extension telephones and subscriber carrier applications. Operating power is derived from the telephone line.

Features

- 5 mA–120 mA loop operation
- Voltage swing down to 1.0V
- Transmit amplifier for electret microphone — TP5700, -1
- Transmit amplifier for dynamic microphone — TP5710
- Receive amplifier with push-pull outputs
- Automatic gain compensation for loop length
- Sidetone impedance independent of input impedance
- DTMF interface with muting
- Voltage regulator outputs for DTMF generator etc.
- Works in parallel with a standard phone on 20 mA loop

Simplified Block Diagram



TL/H/5201–1

Absolute Maximum Ratings

V^+ with Respect to V^-	20V	Storage Temperature, T_S	−65°C to +150°C
Voltage at Any Other Pin	$V^+ + 0.3V$ to $V^- - 0.3V$	Junction Temperature	150°C
Operating Temperature, T_A	−25°C to +70°C	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	1W		

DC Electrical Characteristics

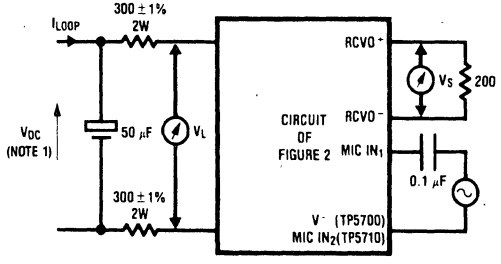
Unless otherwise specified, all tests based on the test circuits shown in *Figure 1*, all limits apply for T_A = 0°C to 60°C, typical values apply at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{T-R}	Tip-Ring Voltage including nominal 1.4V polarity guard (See *Figure 1*)	I_{LOOP} = 5 mA		2.8		V
		= 20 mA, TP5700			4	
		= 20 mA, TP5700-1			5	V
		= 20 mA, TP5710		4.7		V
		= 50 mA		7		V
		= 80 mA		10.5		V
		= 120 mA		15		V
V_I	Minimum Instantaneous Voltage Swing	V^+ to V^-, I_{LOOP} = 5mA		1.0		V
TRANSMIT AMPLIFIER TP5700, TP5700-1						
R_{XIN}	Input Resistance	From Pin 7 to V^-	15	30	50	kΩ
G_{XA}	Gain at 1 kHz, T_A = 25°C	R_{AGC} = 0Ω to V^-, I_{LOOP} = 20 mA, TP5700	33	35	37	dB
		TP5700-1	32		38	dB
G_{XT}	Gain Variation v. T_A	T_A = 0°C to 60°C		±1		dB
G_{XI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
N_X	Transmit Noise	MIC IN_1 = 0V		12	18	dBrnC
TP5710						
R_{XIN}	Differential Input Resistance	From Pin 7 to Pin 11		1.2		kΩ
G_{XA}	Gain at 1 kHz, T_A = 25°C	R_{AGC} = 0Ω to V^-, I_{LOOP} = 20 mA, T_A = 25°C		57		dB
G_{XT}	Gain Variation v. T_A	T_A = 0°C to 60°C		±1		dB
G_{XI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
N_X	Transmit Noise	MIC IN_1 = MIC IN_2 = OV		18		dBrnC
ALL DEVICES						
S/D_X	Signal/Total Harmonic Distortion	$I_{LOOP} \geq$ 20 mA, V_L = 800 mVrms		2	10	%
G_{XM}	Gain Change when MUTED	MUTE IN ≥ V_{MON}		−55		dB
DTMF AMPLIFIER						
R_{DIN}	Input Resistance	From Pin 8 to V^-		20		kΩ
G_{XD}	Gain at 1 kHz	R_{AGC} = 0Ω to V^-, I_{LOOP} = 20 mA, T_A = 25°C		6		dB
G_{XDT}	Gain Variation v. T_A	T_A = 0°C to 60°C		±1		dB
G_{XDI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
MUTE INPUT						
I_{MIN}	Input Current	Pin 9 = 1.5V		40		μA
V_{MOFF}	MUTE OFF Input Voltage				0.5	V
V_{MON}	MUTE ON Input Voltage		1.5			V

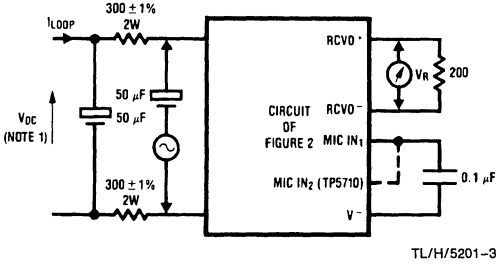
DC Electrical Characteristics (Continued)

Unless otherwise specified, all tests based on the test circuits shown in *Figure 1*, all limits apply for T_A = 0°C to 60°C, typical values apply at T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE AMPLIFIER						
R_{RIN}	Input Resistance	From Pin 12 to V−	20	35	55	kΩ
G_{RA}	Gain at 1 kHz, T_A = 25°C	R_{AGC} = 0Ω, MUTE IN ≤ V_{MOFF} I_{LOOP} = 20 mA	−5.5	−4	−2.5	dB
G_{RT}	Gain Variation v. T_A	T_A = 0°C to 60°C		±0.5		dB
G_{RI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
G_{RM}	Gain Change when MUTED	MUTE IN ≥ V_{MON}	−15	−20	−23	dB
N_R	Receive Noise	V_{RCVIN} = 0V		0	10	dBrnC
S/D_R	Signal/Total Harmonic Distortion	V_R = 400 mVrms I_{LOOP} ≥ 20 mA		2	10	%
V_RC	Output Clipping Level		1.2	2		Vp-p
V_{ROS}	Output Offset Voltage				100	mV
SIDETONE CHARACTERISTICS						
STC	Sidetone Cancellation at 1kHz	20 mA ≤ I_{LOOP} ≤ 100 mA, Note 2		15		dB
VOLTAGE REGULATOR OUTPUTS						
V_{REG1}	Output Voltage, Pin 10	I_{LOOP} ≥ 20 mA MUTE IN ≤ V_{MOFF} MUTE IN ≥ V_{MON}	2	 3		V V
I_{REG1}	Maximum Output Current, Pin 10	MUTE IN ≤ V_{MOFF} MUTE IN ≥ V_{MON}		200 2.7		μA mA
V_{REG2}	Output Voltage, Pin 11	I_{LOOP} ≥ 20 mA	1.1	1.2		V
I_{REG2}	Maximum Output Current, Pin 11	I_{LOOP} ≥ 20 mA	300	500		μA



1a. Test Circuit for Transmit and Sidetone



1b. Test Circuit for Receive

FIGURE 1. Test Circuits for Electrical Characteristics

Note 1. Adjust V_{DC} to set specified I_{LOOP} current.

Note 2. To measure Sidetone Cancellation, set oscillator in *Fig. 1a* for V_L = 100 mVrms; measure V_S. Then in *Fig. 1b* set oscillator = 100 mVrms; measure V_R. STC = 20log V_R/V_S.

Functional Description

The TP5700, TP5710 Telephone Speech Circuits are powered from the telephone Tip and Ring terminals via a full-wave rectifier bridge to protect against loop polarity reversals. The devices provide the following functions:

LINE REGULATOR

A DC regulator sinks current from the loop in order to maintain a DC slope resistance similar to that of a standard phone.

R_{DC} provides an adjustment for the slope resistance.

MICROPHONE AMPLIFIER

A single-ended input amplifier on the TP5700 enables a low cost electret microphone to be used. This provides superior distortion, linearity and noise performance compared to a traditional carbon microphone. The electret should be capacitively coupled to the amplifier input. The acoustic sensitivity of the microphone is intended to be in the range of −60 to −70 dBV/μBar.

Loss can be inserted if required by adding a resistive potentiometer either at MIC IN_1 or the connection between the pre-amp output and driver stage input. The driver stage provides automatic gain compensation to reduce the gain as loop length decreases. The AGC range can be adjusted by means of R_{AGC} to limit the maximum loss on a short loop from 0 to 6 dB.

Functional Description (Continued)

The TP5710 provides additional gain and balanced differential inputs for use with a dynamic microphone.

RECEIVE AMPLIFIER

This buffer amplifier provides the necessary gain or loss for the receive signal. RCV IN should be AC coupled to SIDETONE (pin 4). Automatic gain control is built into the amplifier to reduce the gain as loop length decreases. The AGC range is adjusted in common with the transmit AGC range with a range of adjustment for maximum loss from 0 to 6 dB. Push-pull complementary outputs provide balanced direct drive to a dynamic transducer, which may have an impedance as low as 100Ω. The effective receive gain can be reduced by adding a resistor in series with the transducer. The receive gain is automatically reduced by 20 dB when the MUTE input is pulled high.

SIDETONE CIRCUIT

The level of Sidetone cancellation may be adjusted by connecting an external balance impedance to SIDETONE (pin 4) and coupling this point to V^+. For good sidetone cancellation the balance impedance should be approximately 10 times the subscriber line input impedance. Some typical component values to match a precise 600Ω termination for test purposes are shown in *Figure 2.* Use the component values shown in the Applications Section for better results over a wide range of telephone line impedances.

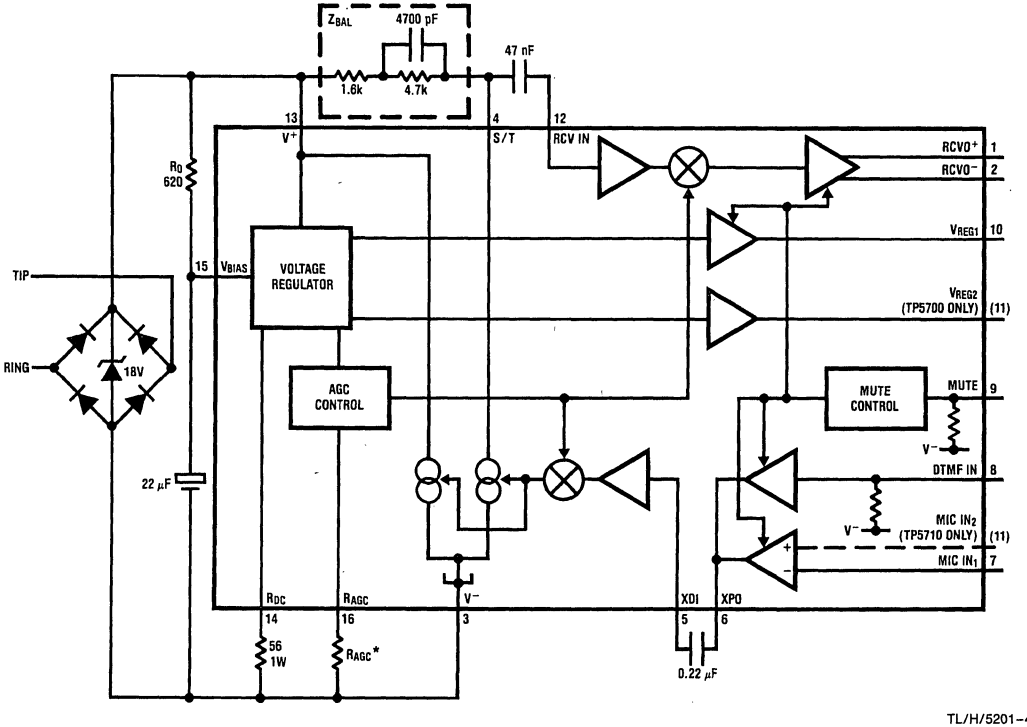
DTMF AMPLIFIER

An additional transmit amplifier is included to enable the open-emitter output of a conventional DTMF generator to be connected to the line via the transmit output stage. This path includes the transmit AGC section. When the MUTE input is pulled high, the DTMF input is enabled and the MIC input disabled. When MUTE IN is open-circuit or pulled to V^- the DTMF input is switched off and the MIC input is enabled.

VOLTAGE REGULATOR OUTPUTS

A precision band-gap voltage reference on the TP5700 and TP5710 controls a regulator to provide bias for internal circuits. Two auxiliary outputs are also available (one on the TP5710). V_{REG1} is provided specifically for powering a low voltage pulse dialer or DTMF generator. In order to protect this output in low voltage situations where the instantaneous voltage across the Speech Circuit may swing below the V_{REG1} output voltage, an internal switch controls the maximum available output current. In speech mode, MUTE IN is low, V_{REG1} output will track approximately ½ the Tip-Ring voltage and the available output current is limited to 200 μA. This is adequate to power a DTMF generator in standby mode. When MUTE IN is pulled high to switch the Speech Circuit to the DTMF dialing mode, V_{REG1} is switched to a 3V regulated output and up to 2 mA may be drawn from it to power the active DTMF generator.

On the TP5700 only, a 1.2V regulated output is also provided at V_{REG2} to power a low voltage 2-wire electret microphone such as the Primo EM80-PMI$_2$.



TL/H/5201–4

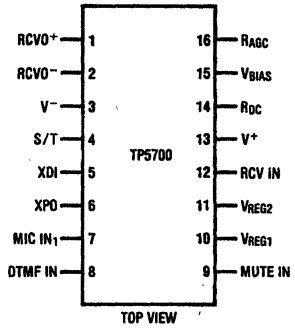
* See Figure 3

Note: Z_{BAL} circuit shown is for test purposes with a resistive line termination. See Applications Information for suggested component values for normal reactive line applications.

FIGURE 2. TP5700, TP5710 Telephone Speech Circuits

Connection Diagrams

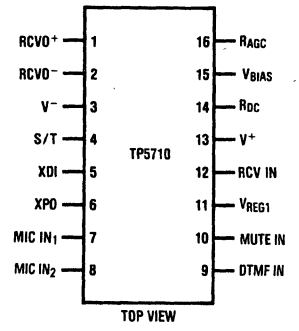
Dual-In-Line Package



TL/H/5201–5

Order Number TP5700, TP5710
See NS Package N16A

Dual-In-Line Package



TL/H/5201–6

Pin Descriptions

Pins 1, 2 RCVO+ and RCVO−

The push-pull complementary outputs of the receive amplifier. Dynamic transducers with a minimum impedance of 100 Ω can be directly driven by these outputs.

Pin 3 V−

This is the negative supply input to the device and should be connected to the negative output of the polarity guard. All other voltages on the device are referred to this pin.

Pin 4 S/T

This is the output of the Sidetone cancellation signal, which requires a balance impedance of approximately 10 times the subscriber's line impedance to be connected from this pin to V+ (pin 13).

Pin 5 XDI

The input to the line output driver amplifier. Transmit AGC is applied in this stage.

Pin 6 XPO

This is the transmit pre-amp output which is normally capacitively coupled to pin 5.

Pin 7 MIC IN_1

This is the inverting input to the transmit pre-amplifier and is intended to be capacitively coupled to an FET-buffered electret microphone (TP5700).

Pin 8 DTMF IN

The DTMF input which has an internal resistor to V− to provide the emitter load resistor for a CMOS DTMF generator. This input is only active when MUTE IN (pin 9) is pulled high.

Pin 9 MUTE IN

The MUTE Input, which must be pulled at least 1.5V higher than V− to mute MIC IN and enable DTMF IN.

Pin 10 V_{REG1}

The regulated output for biasing a pulse dialer or DTMF generator. A 4.7 μF decoupling capacitor to V− should be fitted if this output is used.

Pin 11 V_{REG2} (TP5700, TP5700-1 only)

A 1.2V regulated output suitable for powering a low-voltage electret microphone. A 1μF decoupling capacitor to V− should be fitted if this output is used.

Pin 11 MIC IN_2 (TP5710 only).

The non-inverting input to the transmit pre-amplifier for dynamic microphones.

Pin 12 RCV IN

The receive AGC amplifier input.

Pin 13 V+

This is the positive supply input to the device and should be connected to the positive output of the polarity guard. The current through this pin is modulated by the transmit signal.

Pin 14 R_{DC}

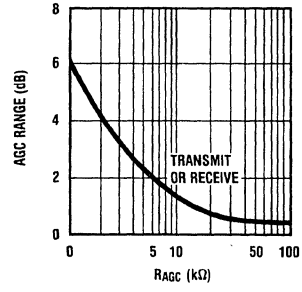
An external 1W resistor is required from this pin to V− to control the DC input impedance of the circuit. The nominal value is 56Ω for low voltage operation. Values up to 82Ω may be used to increase the available transmit output voltage swing at the expense of low voltage operation.

Pin 15 V_{BIAS}

This internal voltage bias line must be connected to V+ via an external resistor, R_o, and decoupled to V− with a 22 μF capacitor. R_o dominates the AC input impedance of the circuit and should be 620Ω for a 600Ω input impedance or 910Ω for a 900Ω input impedance.

Pin 16 R_{AGC}

The range of transmit and receive gain variations between short and long loops may be adjusted by connecting a resistor from this pin to V− (pin 3). *Figure 3* shows the relationship between the resistor value and the AGC range. This pin may be left open-circuit to defeat AGC action.



TL/H/5201–7

FIGURE 3.

Applications Information

The TP5700 and TP5710 are flexible circuits designed with several user adjustments to enable the performance to be optimized for different applications. The choice of transducer types and the cavities in which they are mounted will also greatly influence the acoustic performance of the telephone. Some of the consequences of circuit adjustments are as follows:

R_{DC} ADJUSTMENT

56Ω is the recommended value for R_{DC} if it is required to meet a maximum Tip-Ring voltage of 4V on a 20 mA loop (assuming no more than 1.4V is dropped across the polarity guard). If a higher Tip-Ring voltage is acceptable, R_{DC} may be increased, which will provide a small increase in the available transmit output voltage swing before clipping occurs. R_{DC} should be less than 82Ω to avoid exceeding the maximum rated voltage on a short loop.

R_{AGC} ADJUSTMENT

The available AGC range is more than adequate to compensate for the loss of most loops. R_{AGC} should be chosen only to partly compensate for the anticipated maximum loop loss, as over-compensation may tend to exaggerate the variations of sidetone with loop length.

SIDETONE ADJUSTMENT

The component values used for Z_{BAL} should be selected to provide a clear sidetone sound without excessive "hollowness." The capacitor value and ratio of the two resistors will fix the pole location. To avoid reducing the low voltage performance of the circuit the sum of the two resistors should not exceed 10 kΩ.

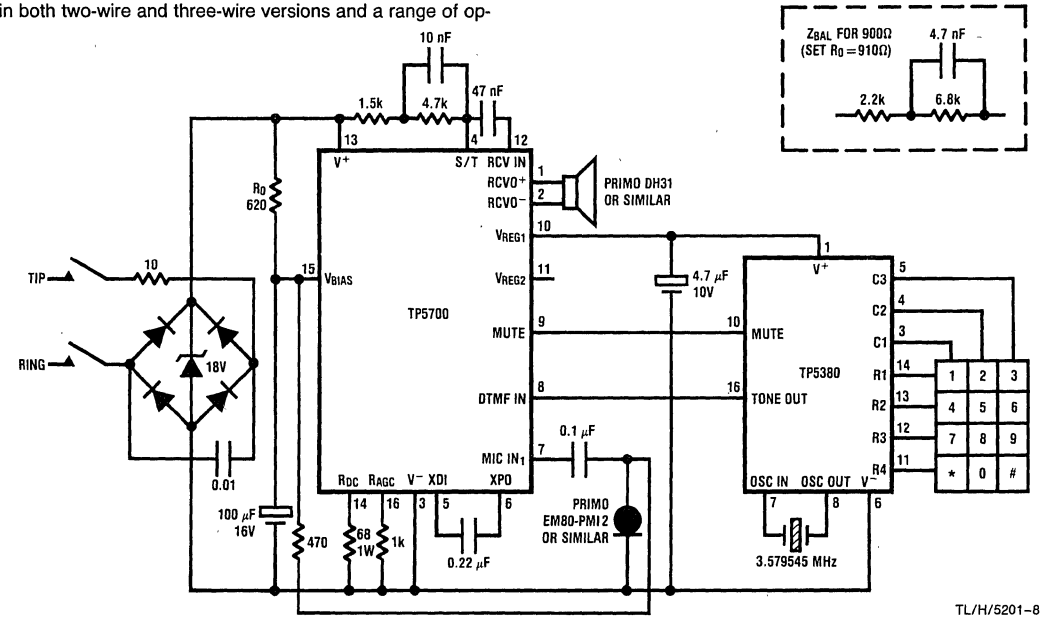
POWERING ELECTRET MICROPHONES (TP5700 only)

Electret microphones with integral FET buffers are available in both two-wire and three-wire versions and a range of operating voltage ranges. There are four methods of powering the microphone.

1. The 1.2V V_{REG2} output provides the lowest voltage method for microphones rated down to 1V. V_{REG2} must be decoupled with a 1 μF capacitor to ground.
2. If V_{REG1} is not required for DTMF generator operation, it may be used to provide up to 200 μA for microphone power.
3. V_{BIAS} (pin 15) may be used as a decoupled, but unregulated, supply for electrets requiring a higher operating voltage than V_{REG1} or V_{REG2}. The additional current drawn through R_0 will, however, raise the minimum operating voltage of the Speech Circuit. If this method is used the decoupling capacitor must be increased to at least 100 μF to maintain good low frequency return loss.
4. An electret type with a good power supply rejection ratio can be powered from V^+, or a regulated and decoupled supply dropped from V^+.

TONE DIALING TELEPHONE

Figure 4 shows the TP5700 directly interfacing to a low voltage DTMF generator. V_{REG1} supplies the necessary 2V minimum bias to enable the TP5380 to sense key closures and pull its MUTE output high. V_{REG1} then switches to a 3V regulated output to sustain the Tone Dialer during tone generation. The TP5700 DTMF input incorporates the necessary load resistor to V^- and provides gain plus AGC action to compensate for loop length. A muted tone level is heard in the receiver. For DTMF generators with a higher output level than the TP5380, a resistive potentiometer should be added to reduce the level at the speech circuit DTMF Input.



TL/H/5201–8

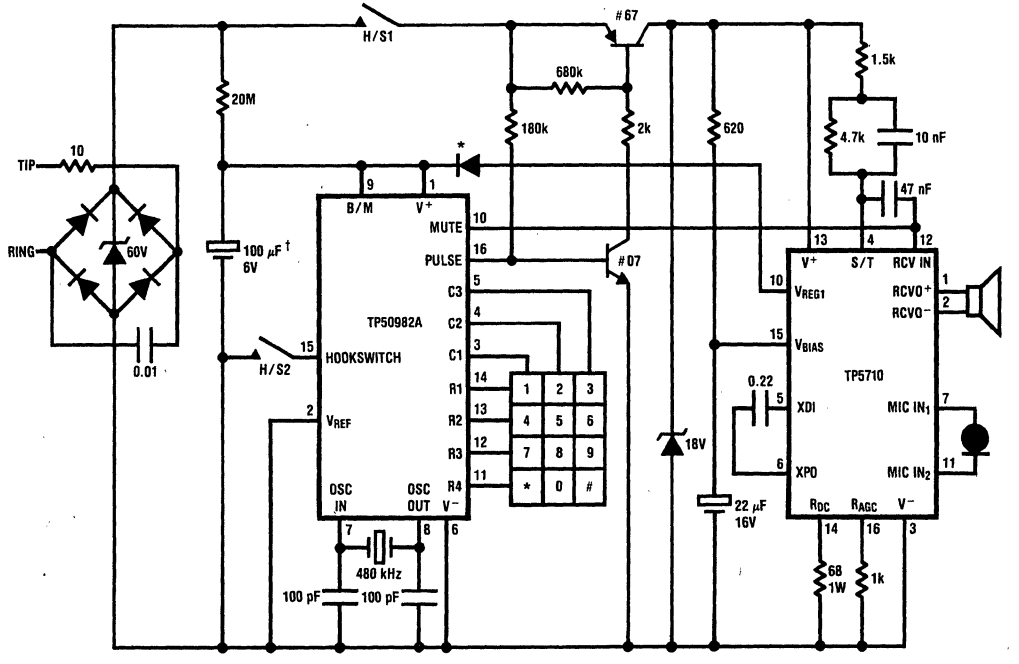
FIGURE 4. Typical Tone Dialing Telephone

Applications Information (Continued)

PULSE DIALING TELEPHONE

The TP5700 or TP5710 can reduce the number of components required to build a pulse dialing telephone, as shown in *Figure 5*. The usual current source can be eliminated by using the V_{REG1} output to power a TP50982A low-voltage (1.7V) pulse dialer via a blocking diode. A low forward-voltage drop diode such as a Schottky type is necessary because V_{REG1} is used in its non-regulated mode and its output voltage may fall to 2V on a 20 mA loop. A 100 μF decoupling capacitor is required to hold up the pulse dialer supply voltage during dialing. This capacitor will take about one second to charge up when the telephone is first connected to the line, but thereafter the 20 MΩ resistor required to retain the last-number dialed memory will keep this capacitor charged. Partial muting is obtained by directly connecting the N-channel open-drain MUTE output of the pulse dialer to the RCV IN pin on the Speech Circuit.

A fully muted pulse dialer design requires the use of a shunt-mode dialer such as the TP50981A or TP50985A. Suitable interface circuits are shown in the TP50981A data sheet.



TL/H/5201–9

* Select as necessary to suit mic sensitivity

† Low leakage type

FIGURE 5. Typical Pulse Dialing Telephone

National Semiconductor

TP53190 Push-Button Pulse Dialer

General Description

The TP53190 is a low threshold voltage, ion implanted, metal-gate CMOS integrated circuit that provides all the logic required to convert a push-button input into a series of pulses suitable for simulating a telephone rotary dial. The circuit works with both calculator type keypad (single-contact) or standard 2-of-7 type keypad. An inexpensive ceramic resonator is used as a frequency reference. When not actually outpulsing, or if there are no keypad entries, the TP53190 consumes only microamperes of current and does not allow any internal oscillators to run.

The TP53190 contains a 16-digit first-in—first-out memory that allows the user to enter digits faster than they are outpulsed. Numbers up to 16 digits may be dialed. After 16 digits have been entered, no more entries will be accepted. The outpulsing rate can be externally selected as either 10 pps or 20 pps. An interdigit pause of 4, 6, 8 or 10 times the dial pulse period is also externally selectable. The break/make ratio (ratio of the time the line is broken to the time the line is looped during outpulsing) is externally selectable to 1/1, 1.5/1, 1.6/1 or 2/1. A mute output is provided to mute receiver noise during outpulsing. No muting occurs during the inter-digit pause, thereby allowing the user to hear any busy or invalid condition arising during the call. The TP53190 provides a pacifier tone of 632 Hz every time a key is depressed. The last number entered may be redialed by use of the # key.

Features

- Powered directly from the telephone line
- Uses standard calculator type keypad or 2-of-7 type keypad
- Uses inexpensive ceramic resonator for a frequency reference
- Pin-selectable outpulsing rate
- Pin-selectable interdigit pause
- Pin-selectable break/make ratio
- 632 Hz pacifier tone
- Redial of last number
- 2 digit overwrite for PABX access

Block and Connection Diagrams

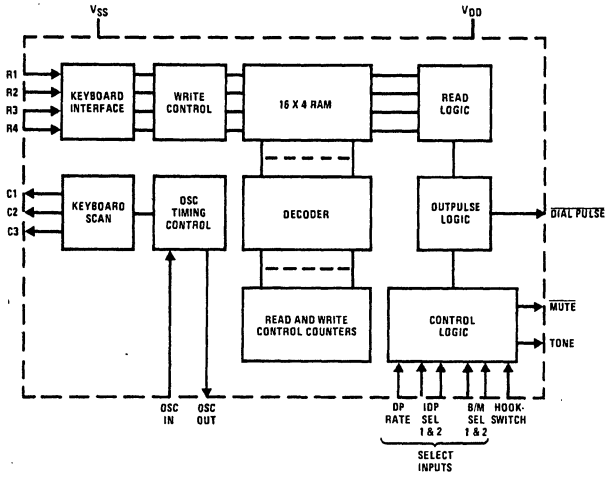


FIGURE 1.

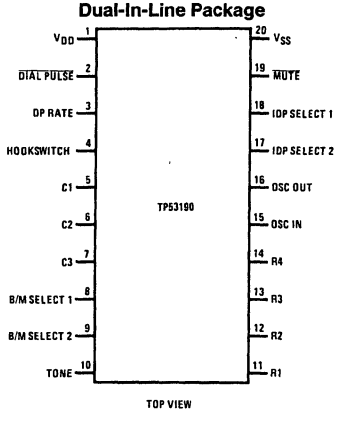


FIGURE 2. TL/H/5130–1

Order Number TP53190
See NS Package N20A

Absolute Maximum Ratings

Voltage at Any Pin	$V_{SS}-0.3$ to $V_{DD}+0.3V$
Current into $\overline{DP}$	
for Voltages Exceeding V_{DD}	$\leq 500\ \mu A$
Operating Temperature Range	$-30°C$ to $+70°C$
Storage Temperature Range	$-40°C$ to $+70°C$
V_{DD}—V_{SS}	6.5V
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Voltage Range

V_{SS} = GND, V_{DD} = 2.5V min, 5.5V max

Electrical Characteristics

V_{SS} = GND, $2.5V \leq V_{DD} \leq 5.5V$, $-30°C \leq T_A \leq +70°C$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage					
Logical "1"		$V_{DD}-0.25$		V_{DD}	V
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Output Current Levels:					
$\overline{\text{Dial Pulse}}$					
Logical "0", Sink	$V_{DD}=3V$, $V_{OUT}=0.7V$	500			μA
$\overline{\text{Mute}}$					
Logical "0", Sink	$V_{DD}=3V$, $V_{OUT}=0.7V$	500			μA
Tone					
Logical "1"	$V_{DD}=3V$, $V_{OUT}=2.75V$	4			μA
Logical "0"	$V_{DD}=3V$, $V_{OUT}=0.25V$	4			μA
C1—C3					
Logical "1"	$V_{DD}=3V$, $V_{OUT}=2.75V$	1			μA
Logical "0"	$V_{DD}=3V$, $V_{OUT}=0.25V$	18			μA
Keypad Resistance				1	kΩ
Operating Current	$V_{DD}=3V$				
	Quiescent			1	μA
	Oscillating			300	μA
Outpulsing Frequency	Osc = 488 kHz	9.5		10.5	Hz
Input Leakages:					
Pins 3, 8, 9, 17, 18	$V_{DD}=5.5V$, $V_{IN}=V_{SS}$			5	μA
Pins 11, 12, 13, 14	$V_{DD}=5.5V$, $V_{IN}=V_{SS}$			30	μA
Pin 4 (Hookswitch)	$V_{DD}=5.5V$, $V_{IN}=V_{SS}$			1	μA
Pins 3, 8, 9, 17, 18	$V_{DD}=5.5V$, $V_{IN}=V_{DD}$			1	μA
Pins 11, 12, 13, 14	$V_{DD}=5.5V$, $V_{IN}=V_{DD}$			1	μA
Pin 4 (Hookswitch)	$V_{DD}=5.5V$, $V_{IN}=V_{DD}$			5	μA

Functional Description

A block diagram of the TP53190 integrated circuit is shown in *Figure 1* and a package connection diagram is shown in *Figure 2*.

Oscillator (Pins 15 and 16): The precision time base of the TP53190 pulse dialer is provided by an internal oscillator circuit which utilizes an inexpensive ceramic resonator as a frequency reference. Two external capacitors, as shown in *Figure 3*, are needed to load the resonator to operate in the anti-resonant mode. A 455 kHz series resonance ceramic resonator will result in a frequency of oscillation of 480 kHz. Ceramic resonators are available from Vernitron Corporation, Murata Corporation, and Radio Materials Company. Frequency stability of ±5% can be maintained for all devices over the voltage and temperature ranges. When the circuit is not outpulsing, or no keys are depressed, the oscillator will be shut down to eliminate noise and minimize dissipation.

Keypad (Pins 5–7 and 11–14): Three column scan output pins and four row input pins are provided to utilize a standard single-contact keypad or 2-of-7 type keypad (*Figure 4*). A valid key closure is recorded when a single row (R_X input) is connected to a single column (C_X output) or when a single row and a single column are brought to V_{SS}. Key closures are protected from contact bounce for 6 ms. Roll-over keyboard inputs will be considered valid.

Functional Description (Continued)

Dial Pulse Output (Pin 2): The Dial Pulse output drives an external bipolar transistor that sequentially opens (breaks) the telephone loop a number of times equal to the input digit selected. For example, key 5 will generate 5 loop current breaks. The Dial Pulse output is an open drain transistor that sinks current only during a break.

Break/Make Select (Pins 8–9): The break/make ratio of the TP53190 can be externally selected by the 2 break/make select pins to be 1/1, 1.5/1, 1.6/1 or 2/1. This allows applications in a wide variety of telephone systems (Table I).

DP Rate Select (Pin 3): The dial pulse rate select input is used to select an outpulsing rate of either 10 pps or 20 pps (Table II).

IDP Select (Pins 17 and 18): The IDP select inputs are used to select an interdigit separation of 400 ms, 600 ms, 800 ms or 1000 ms when the outpulsing rate is 10 pps; and 200 ms, 300 ms, 400 ms, or 500 ms when the outpulsing rate is 20 pps (Table III)

Mute (Pin 19): The Mute output is used to drive an external bipolar transistor that is used to mute the receiver during the outpulse period. The Mute output is an open drain transistor that only sinks current while muting. System timing between key closure, mute and dial pulse are shown in the timing diagram in *Figure 5*. For initial key entries, and subsequent key entries made 1 IDP period after the last digit has been outpulsed, mute will occur 1 IDP period before outpulsing begins.

For key entries made during outpulsing, or during an IDP, there will be a pre-dial mute of 100 ms when the outpulsing rate is 10 pps, and a pre-dial mute of 50 ms when the outpulsing rate is 20 pps. The post-dial mute is 50 ms when the outpulsing rate is 10 pps and 25 ms when the outpulsing rate is 20 pps.

Tone (Pin 10): The TP53190 provides a pacifier tone output to provide audio feedback to the user that a key has been depressed. The output is a 632 Hz tone that can be capacitively coupled in to the telephone receiver.

Redial: This feature allows the user to automatically dial the last number that was dialed. This is accomplished by pushing the # key on the next dial attempt. The number to be redialed may be 3 to 16 digits long. If an access code is required, as in a PBX system, up to 2 digits may be entered before the dial tone is established and the redial key is pushed to automatically dial the remainder of the number. To maintain memory information, power must be present to the part while in the ON-HOOK condition. To detect the ON-HOOK condition, the hookswitch input (pin 4) must be left floating. Hookswitch is used to reset the internal control circuitry and memory pointers. To detect the OFF-hook condition, hookswitch must be at a logical "1". An example of the redial operation is shown below.

	Key Inputs	Outpulses	Memory
First Try	85P4087375000	854087375000	854087375000
Second Try	85P#	854087375000	854087375000
Third Try	85P#	854087375000	854087375000

Note: P indicates a user pause

TABLE I

Break/Make Ratio		
B/M	**Select 1**	**Select 2**
1.5/1	0	0
2/1	0	1
1/1	1	0
1.6/1	1	1

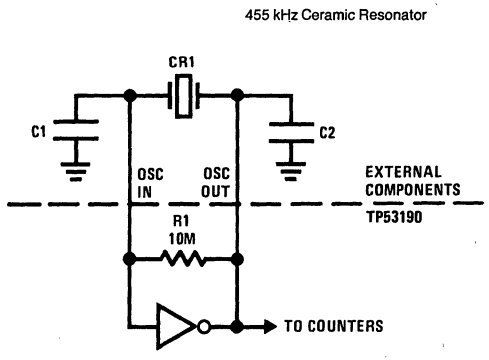
TABLE II

Dial Pulse Rate	
pps	**SELECT**
10	0
20	1

TABLE III

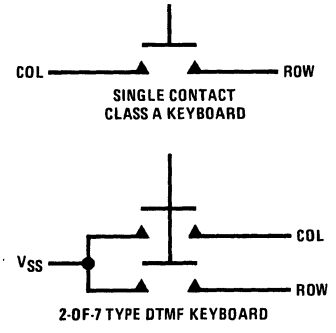
Interdigital Pause			
IDP Length	**Dial Pulse Rate**	**Select 1**	**Select 2**
800 ms	10 pps	0	0
400 ms	20 pps	0	0
1000 ms	10 pps	0	1
500 ms	20 pps	0	1
400 ms	10 pps	1	0
200 ms	20 pps	1	0
600 ms	10 pps	1	1
300 ms	20 pps	1	1

Functional Description (Continued)



C1 = C2 = 80 pF

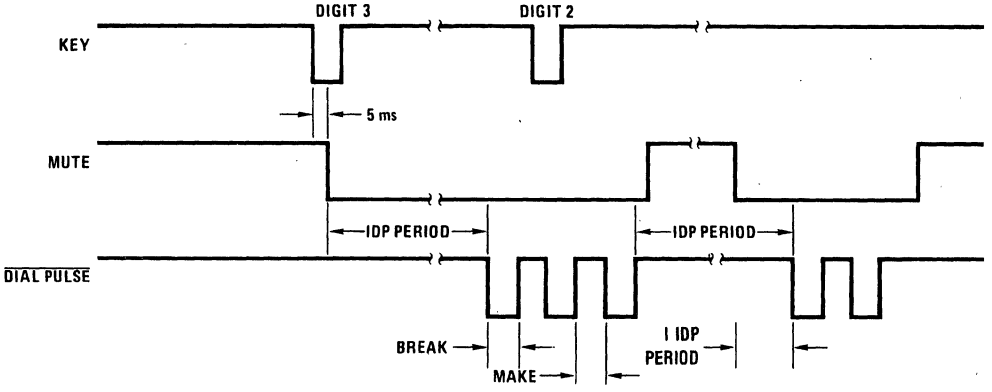
FIGURE 3.



TL/H5130–2

FIGURE 4.

Output Timing Waveforms

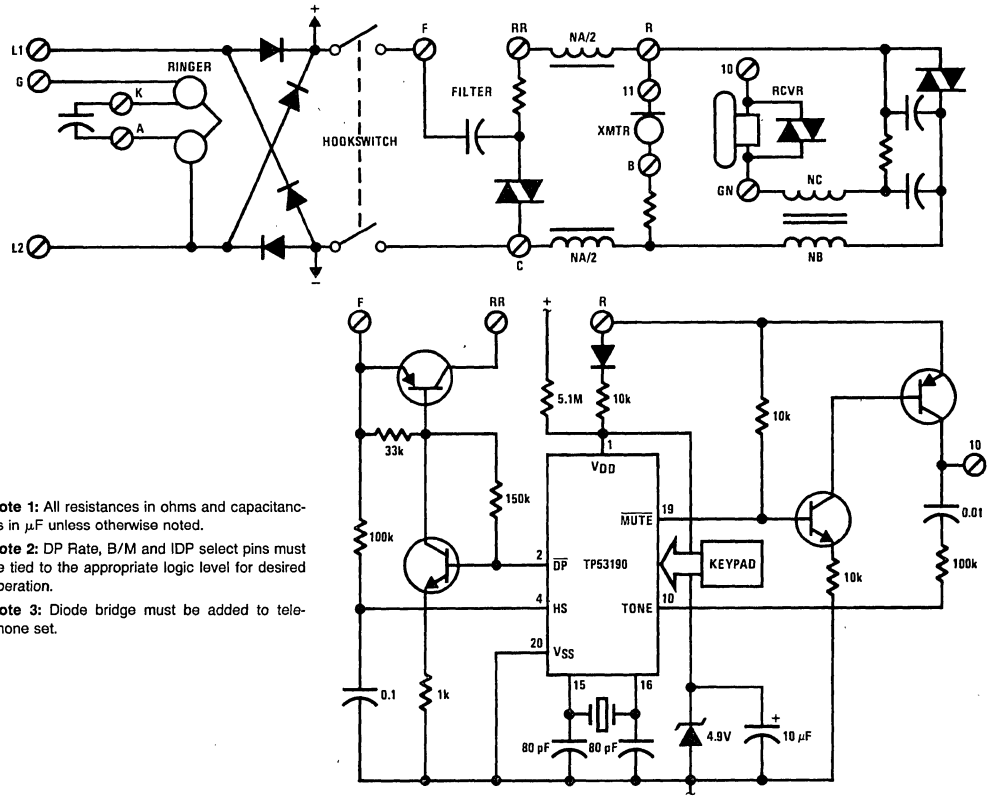


TL/H/5130–3

IDP = Interdigit Pause

FIGURE 5. $\overline{\text{Mute}}$ Not Active Between Digits

Functional Description (Continued)



TL/H/5130–4

Note 1: All resistances in ohms and capacitances in µF unless otherwise noted.

Note 2: DP Rate, B/M and IDP select pins must be tied to the appropriate logic level for desired operation.

Note 3: Diode bridge must be added to telephone set.

FIGURE 6. Using the TP53190 Pulse Dialer with Redial Option

Section 14

Speech

Section Contents

DIGITALKER Speech Synthesis

National Semiconductor

DTSW-500 DIGITALKER® Vocabulary Selection System (DVSS)

Product Description

The DIGITALKER Vocabulary Development System (DVSS) is a CP/M™ software package which provides 500 highly intelligible English words in a male speaking voice. These words are intended for users of National Semiconductor's DIGITALKER MM54104 Speech Processor Chip. The package provides a complete software environment that allows users to create speech PROMs containing a vocabulary of words, phrases, or sentences put together from the 500 words supplied.

The DVSS package consists of 2 floppy disks and a user's manual. The first disk contains the speech data archive and the second contains the system software. Both floppy disks are standard 8" single-sided, single density disks written in CP/M format.

In a typical application, a user would start by developing a vocabulary for his envisioned talking product. This vocabulary could be composed of a list of single words, phrases, or sentences. A standard CP/M text file is created containing the vocabulary list using any CP/M based text editor or the editor provided with the DVSS. This vocabulary list is checked to assure that all words on the list are contained in the current archive. Missing or misspelled words are flagged and the user must then return to the text editor to make corrections.

The DVSS software creates what is called a work file for the vocabulary from an error-free vocabulary list. This work file can then be submitted to the ROM image building routine. The output is a ROM image file in binary format. This file in turn can be used to program PROMs.

In order to use the DVSS software, a user needs a computer system that runs CP/M-80 and that has two 8" single density floppy disk drives. Also necessary is a CRT terminal with both upper and lower case capability. (Note that this configuration can actually be thought of as a model of the computer system on which DVSS will operate. There are however computer systems which don't exactly match this model that will run DVSS.)

The DVSS programs are easy to use. A complete instruction manual and tutorial examples ensure that even a person unfamiliar with speech or programming will have little difficulty in producing vocabulary lists and speech PROMs.

The speech ROM images produced by the DVSS system will be nearly as memory efficient as speech ROMs produced at the National Semiconductor Speech Lab. The data rate for ROMs containing more than 50 words will be approximately 1200 bits per word. (Smaller speech ROMs result in a slightly higher data rates.)

Features

- Create your own speech EPROMs
- Choose words from a large database
  - — 500 words to start
  - — Future library expansion
- Build sentences and phrases
- No previous knowledge of synthetic speech required
- Runs on most CP/M machines
- Supports MM54104 Digitalker Speech Processor Chip

Functional Description

THE SPEECH DATA ARCHIVE

The speech data disk supplied with the system contains 500 words. (Consult Table 1 for a listing of these words.) Each word stored on the floppy is a self-contained, stand-alone, playable entity. Adding further standard vocabulary or even custom words to the archive is a simple operation which is discussed in the software section below.

THE SOFTWARE

The DVSS software is a CP/M 2.2 applications program written in BDS C which will execute on most CP/M 2.2 compatible computers. The software requires the service of a CRT terminal.

OPERATING ON SPEECH DATA ARCHIVES

The speech data archive is the basic unit on which all the software operates. The system, as it is shipped from the factory, consists of a single speech data archive containing 500 words. The archive architecture, however, makes it very easy to add to or create new archives from existing ones. This capability is useful in a number of situations. For instance, as more standard words are released by National Semiconductor, a user may wish to make a new archive that contains the entire standard word library. Or, if the full speech data archive has become too cumbersome or too large for storage on a single floppy, a subset of the full archive can be selected to create a new more manageable archive.

The word archival software allows the user to obtain a variety of information about the contents of any archive. For example, the user can generate an alphabetical listing of all words in the archive. All of the lists generated by the DVSS can be output to any of the standard CP/M devices such as CON:, the system console, LST:, the system printer, or a file residing on any system supported disk.

PREPARING VOCABULARY LISTS

The central purpose of the DVSS system is building speech ROM images which (after conversion to some physical media such as EPROM or RAM) can be played by the MM54104. The first step in building a ROM image is to list the messages, i.e. the words and phrases, that are to be contained in the image. In order to create, and if necessary, correct, such a message list, any CP/M text editor (for example, WORDSTAR™ in "non-document" mode) may be used to create a file of the proper format (format specified in detail in the manual). The DVSS package includes a simple but powerful text editor that may be used in lieu of other CP/M editors.

COMPILING VOCABULARY LISTS

After a vocabulary list has been entered into a file, it must be compiled. The compiler checks for existence of words in the archive and prepares a workfile for the image builder. Any missing words are pointed out for the user.

BUILD SPEECH DATA ROM IMAGES

Once the user has successfully compiled the vocabulary list, a ROM image can be made of these words and/or phrases by using the ROM image builder. This function retrieves the raw speech data for each word in the vocabulary list, finds all redundancies; eliminates them; and packs the remaining data into a playable image.

PROGRAM SPEECH DATA EPROMS

When the user has built a speech ROM image, he can program a physical PROM (or set of PROMs) to contain this image. The DVSS will directly support PROM programming on the local PROM programmer in STARPLEX™ systems. Speech ROM images are nothing more than CP/M files in binary format. They may easily be converted (with user supplied software) to other formats for use with other user supplied PROM programming hardware (for example, with a remote programmer connected to a serial port).

AUDITIONING SUPPORT

Customers who are using the DVSS to experiment with DIGITALKER speech, can easily obtain a speech system in which to play their EPROMs. National sells a simple board (DT 1058) and a software upgrade (DT 1060) that enables the original DIGITALKER demonstration board (DT 1000) to play up to eight 16k EPROMs (or 4 32k EPROMs) (see the DT data sheets for more information on these products.) There are also vendors who build DIGITALKER based add-ons to various computers which can accept speech EPROMs. These boards allow a user to play speech EPROMs under computer control (users of these boards might also want to use the DT 1058 PROM board). A list of such vendors is available on request from National.

DTSW- 500 Word List

0	add	blocking	converter
1	address	blue	cool
2	adjust	brake	copy
3	after	budget	correct
4	again	building	cost
5	air	buoy	count
6	aisle	busy	cross
7	alarm	button	customer
8	alert	by	cut
9	all	c	d
10	alternate (adjective)	call	d. c.
11	amp	cancel	danger
12	ampere	capacitance	data
13	an	car	date
14	and	case	day
15	announcement	caution	december
16	answer	cease	decrease
17	april	celsius	default
18	arrival	cent	degree
19	ask	centi- (prefix)	delay
20	assistance	centigrade	demonstration
30	astern	centimeter	deposit
40	at	change	depth
50	attention	channel	dial
60	august	check	did
70	authorize	circuit	disable
80	auto	clear	divide
90	available	close	dollar
100	average	code	door
1000	away	cold	down
a	b	comma	e
a. c.	back	command	east
a. m.	barometric	common	ed (suffix)
able	basement	communication	electric
abort	bath	complete	electricity
accumulate	battery	condition	else
acknowledge	been	configuration	emergency
activate	before	connect	enable
active	between	continue	end
activity	black	control	enter

entry
equal
er (suffix)
error
evacuate
examine
exit
extreme
f
fail
failure
far
farad
fast
february
feet
fifth
fight
fire
first
floor
flow
forward
friday
from
frontal
fuel
fuse
g
gallon
gas
get
going
good
gram
gray
great
green
group
h
half
have
hello
help
here
hertz
high
hit
hold
home
hour
house
hurt
i
if
in
inactive
inches
incorporated
incorrect
increase
ing (suffix)
insert
interface
intruder
invalid (not valid)
is
it
j
january
july
june
just
k
key
keypad
kilo-
l
leave
left
less
level
lie
light
lime
limit
line
link
listen
load
lock
loop
low
m
march
mark
may
meg- (prefix)
mega- (prefix)
message
meter
micro
mile
milli- (prefix)
millimeter
million
minus
minute
miss
model
modem
module
monday
monitor
more
move
my
n
nano- (prefix)
near
need
next
night
no
normal
north
not
notice
november
number
o
o'clock
october
of
off
ohm
okay
on
onward
open
operator
optical
or
other
out
over
over-range
p
p. m.
pair
pan
parent
pass
past
per
percent
phone
phone number
pico
place
play
please
plus
point
pound
power
program
present
press
pressure
pull
pulse
push
put
q
quarter
r
rain
range
rate
re- (prefix)
reach
ready
receive
receiver
record
red
remove
repair
repeat
replace
reset
resistance
response
restore
return
reverse
right
ring
room
route
run
s
safe
saturday
second
secure
security
select
send
sensor
september
sequence
service
set
short
should
side
sight
sink
slow
smile
smoke
sound
south
space
span
spare
speed
spell
squad
ss (suffix)
stair
star
start
station
status
steam
stern
stop
store
storm
stream
street
sub
subscriber
sunday
supervisory
switch
system
t
tank
tape
target
tear
teen
temperature
temporary
terminate
test
th (suffix)
than
thank
thank-you
that
the
thee
then
there
therm
thermal
third
this
thursday
tide
time
tip
today
tone
total

touch
tracking
traffic
transfer
trip
true
trunk
try
tuesday
turn
type
u
un- (prefix)
unable
unattended
unit
unknown
unlock
up
use
uth (suffix)
utility
v
voice
volt
voltage
vote
w
wait
wake
wake up
warm
warning
was
water
watt
wave
wear
wednesday
week
welcome
west
what
will
wind (short i)
wind (long i)
wish
with
within
word
work
x
y
yellow
yes
you
your
z
zone

National Semiconductor

MM54104 DIGITALKER® Speech Synthesis System

General Description

The DIGITALKER is a speech synthesis system consisting of multiple N-channel MOS integrated circuits. It contains an MM54104 speech processor chip (SPC) and speech ROM and when used with external filter, amplifier, and speaker, produces a system which generates high quality speech including the natural inflection and emphasis of the original speech. Male, female, and children's voices can be synthesized.

The SPC communicates with the speech ROM, which contains the compressed speech data as well as the frequency and amplitude data required for speech output. Up to 128k bits of speech data can be directly accessed. This can be expanded with minimal external logic.

With the addition of an external resistor, on-chip debounce is provided for use with a switch interface.

An interrupt is generated at the end of each speech sequence so that several sequences or words can be cascaded to form different speech expressions.

Encoding (digitizing) of custom word or phrase lists must be done by National Semiconductor. Customers submit to the factory high quality recorded magnetic reel to reel tapes containing the words or phrases to be encoded. National Semiconductor will sell kits consisting of the SPC and ROM(s) containing the digitized word or phrases.

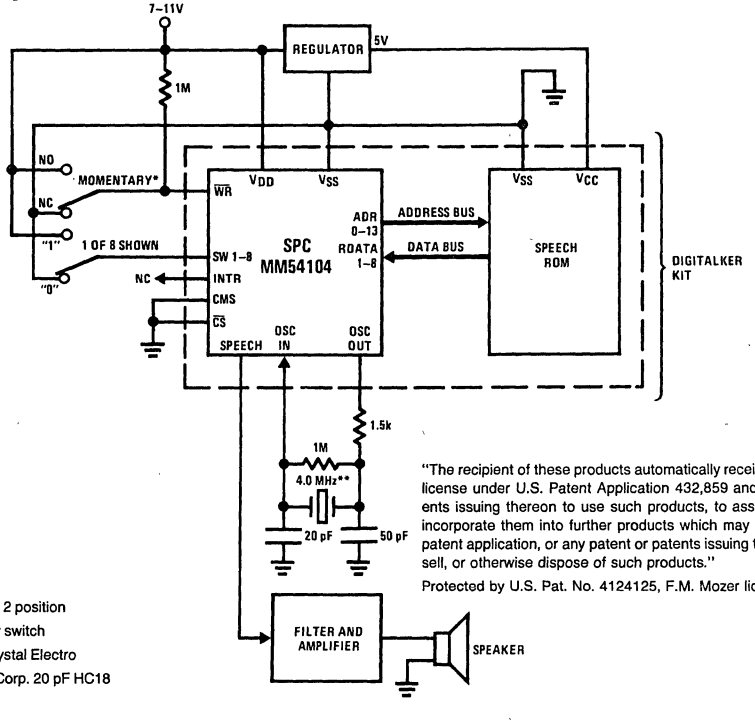
Features

- Designed to be easily interfaced to most popular microprocessors
- 256 possible addressable expressions
- Male, female, and children's voices
- Any language
- Natural inflection and emphasis of original speech
- Addresses 128k of ROM directly
- TTL compatible
- MICROBUS™ and COPS™ compatible
- On-chip switch debounce for interfacing to manual switches independent of a microprocessor
- Easily expandable to greater than 128k ROM
- Interrupt capability for cascading words or phrases
- Crystal controlled or externally driven oscillator
- Ability to store silence durations for timing sequences
- Standard vocabulary sets available

Applications

- Telecommunications
- Appliance
- Automotive
- Teaching aids
- Consumer products
- Clocks
- Language translation
- Annunciators

Typical Applications Minimum Configuration Using Switch Interface



*Single pole 2 position momentary switch

**4.0 MHz crystal Electro Dynamics Corp. 20 pF HC18

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TL/B/5611–1

S 14

Absolute Maximum Ratings

Storage Temperature Range	−65°C to +150°C	Voltage Any Pin	12V
Operating Temperature Range	−40°C to 85°C	Operating Voltage Range, $V_{DD}-V_{SS}$	7V to 11V
$V_{DD}-V_{SS}$	12V	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

$T_A=0°C$ to 70°C, $V_{DD}=7V$-11V, $V_{SS}=0V$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		−0.3		0.8	V
V_{IL}	Input Low Voltage	$T_A=-40°C$ to 85°C	−0.3		0.6	V
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{IH}	Input High Voltage	$T_A=-40°C$ to 85°C	2.2		V_{DD}	V
V_{OL}	Output Low Voltage	$I_{OL}=1.6$ mA			0.4	V
V_{OH}	Output High Voltage	$I_{OH}=-100$ μA	2.4		5.0	V
V_{ILX}	Clock Input Low Voltage		−0.3		1.2	V
V_{IHX}	Clock Input High Voltage		5.5		V_{DD}	V
V_{OLX}	Clock Output Low Voltage	Typical Crystal Configuration and 10M Load on Pin 2			1.2	V
V_{OHX}	Clock Output High Voltage	Typical Crystal Configuration and 10M Load on Pin 2	5.5		V_{DD}	V
I_{DD}	Power Supply Current				45	mA
I_{DD}	Power Supply Current	$T_A=-40°C$ to 85°C			50	mA
I_{IL}	Input Leakage				±10	μA
I_{ILX}	Clock Input Leakage				±10	μA
V_S	Silence Voltage			0.45 V_{DD}		V
V_{OUT}	Peak to Peak Speech Output	$V_{DD}=11V$		2.0		V
R_{EXT}	External Load on Speech Output	R_{EXT} Connected Between Speech Output and V_{SS}	50			kΩ

AC Electrical Characteristics

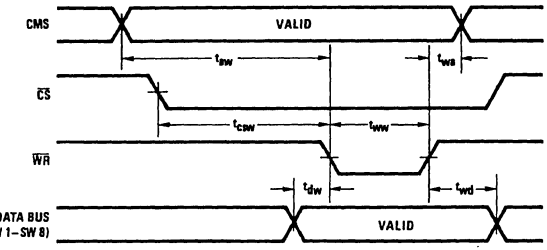
$T_A=0°C$ to 70°C, $V_{DD}=7V-11V$, $V_{SS}=0V$, unless otherwise specified.

Symbol	Parameter	Min	Max	Units
t_{aw}	CMS Valid to Write Strobe	350		ns
t_{csw}	Chip Select ON to Write Strobe	310		ns
t_{dw}	Data Bus Valid to Write Strobe	50		ns
t_{wa}	CMS Hold Time after Write Strobe	50		ns
t_{wd}	Data Bus Hold Time after Write Strobe	100		ns
t_{ww}	Write Strobe Width (50% Point)	430		ns
t_{red}	$\overline{\text{ROMEN}}$ ON to Valid ROM Data		2	μs
t_{wss}	Write Strobe to Speech Output Delay		410	μs
f_t	External Clock Frequency	3.92	4.08	MHz

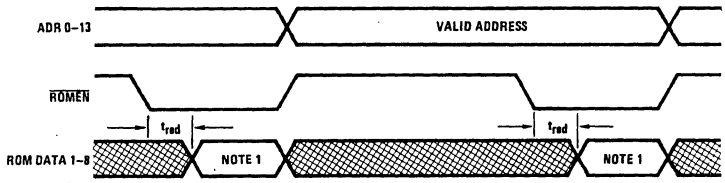
Note: Rise and fall times (10% to 90%) of MICROBUS signals should be 50 ns maximum.

Timing Waveforms

Command Sequence



ROM Data Timing

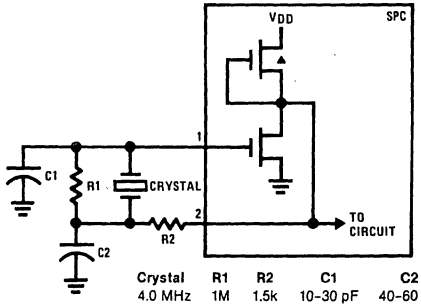


Note 1: ROM data 1-8 can go valid any time after ADR 0-13 changes, however it must be valid within the t_{red} specifications and remain valid until $\overline{ROMEN}$ goes high.

TL/B/5611–2

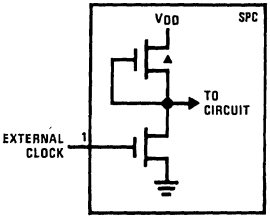
Crystal Circuit Information

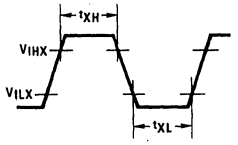
Typical Crystal Oscillator Network



Crystal	R1	R2	C1	C2
4.0 MHz	1M	1.5k	10-30 pF	40-60 pF

External Clock Input (4.0 MHz)



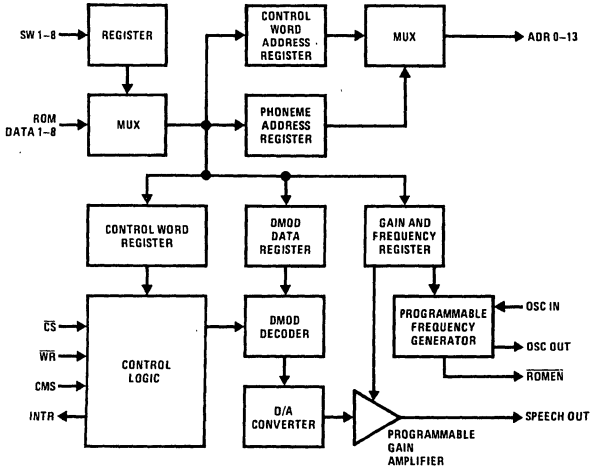


Timing	Min	Units
t_{XH}	100	ns
t_{XL}	100	ns

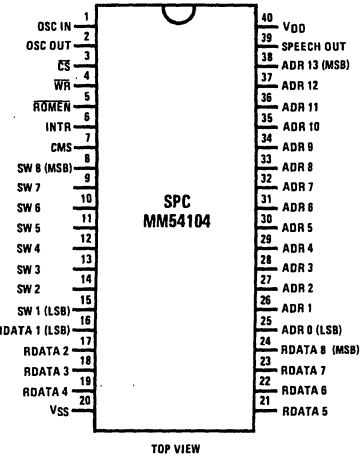
TL/B/5611–3

Order Number MM54104D
See NS Package D40C
Order Number MM54104N
See NS Package N40A

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

TL/B/5611–4

Functional Description

The following describes the function of all SPC input and output pins.

Note: In the following descriptions, a low represents a logic 0 (0.4V nominal), and a high represents a logic 1 (2.4V nominal).

INPUT SIGNALS

Chip Select ($\overline{CS}$): The SPC is selected when $\overline{CS}$ is low. It is only necessary to have $\overline{CS}$ low during a command to the SPC. It is not necessary to hold $\overline{CS}$ low for the duration of the speech data.

Data Bus (SW 1–8): This is an 8-bit parallel data bus which contains the starting address of the speech data. Unused inputs must be tied to V_{SS}.

Command Select (CMS): This line specifies the two commands to the SPC.

CMS	Function
0	Reset interrupt and start speech sequence
1	Reset interrupt only.

Write Strobe ($\overline{WR}$): This line latches the starting address (SW1–SW8) into a register. On the rising edge of the $\overline{WR}$, the SPC starts execution of the command specified by CMS. The command sequence is shown in the timing waveform section. If a command to start a new speech sequence is issued during a speech sequence, the new speech sequence will be started immediately. When connecting $\overline{WR}$ to a switch it must be a single pole 2 position switch as shown on page 1.

ROM Data (RDATA 1–8): This is an 8-bit parallel data bus which contains the speech data from the speech ROM.

OUTPUT SIGNALS

Interrupt (INTR): This signal goes high at the completion of any speech sequence. It is reset by the next valid command. It is also reset at power up.

ROM Address (ADR 0-ADR 13): This is a 14-bit parallel bus that supplies the address of the speech data to the speech ROM.

ROM Enable ($\overline{ROMEN}$): For low power applications, this line can be used to drive a transistor that switches the supply for static speech ROMs. See ROM data timing.

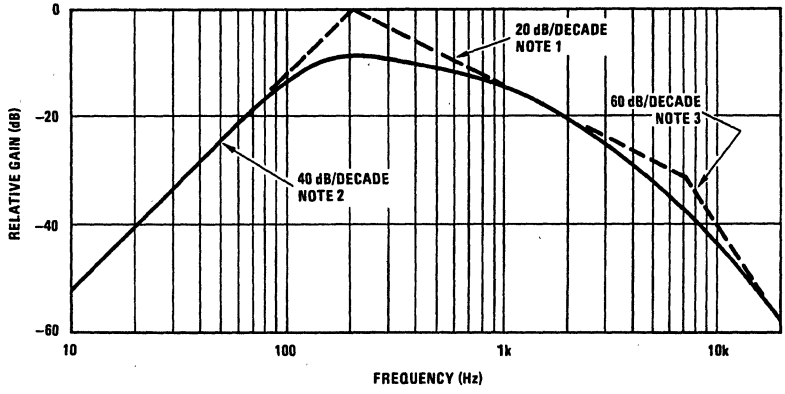
Speech Output (Speech Out): This is the analog output that represents the speech data. See frequency response section.

INPUT/OUTPUT SIGNALS

Clock Input/Output (OSC IN, OSC OUT): These two pins connect the main timing reference (crystal) to the SPC.

Applications Information

Frequency Response of Combined Amplifier and Speaker



TL/B/5611–6

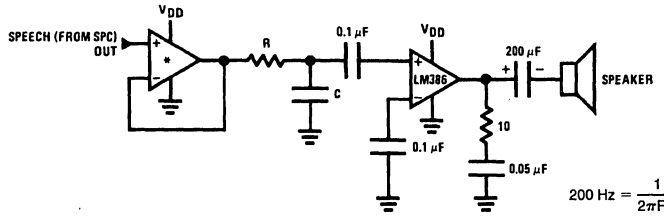
Note 1: This curve is the desired response of the entire audio system including speaker. Minimum response is a low pass filter with a cutoff frequency of 200 Hz. For an audio system with a natural cutoff frequency around 200 Hz, this filter can be eliminated. This cutoff frequency may be tuned for the particular voice being synthesized. For a low pitched male voice it may be 100 Hz, while for a high pitched female or child's voice it might be 300 Hz.

Note 2: This is optional filtering that can be eliminated by proper selection of the speaker. If this 2 pole response is electronically produced, it should be adjusted as described in Note 1.

Note 3: This is optional filtering that can be eliminated for simpler systems. The acceptable range for this cutoff frequency is 6000 Hz–8000 Hz.

Typical Applications (Continued)

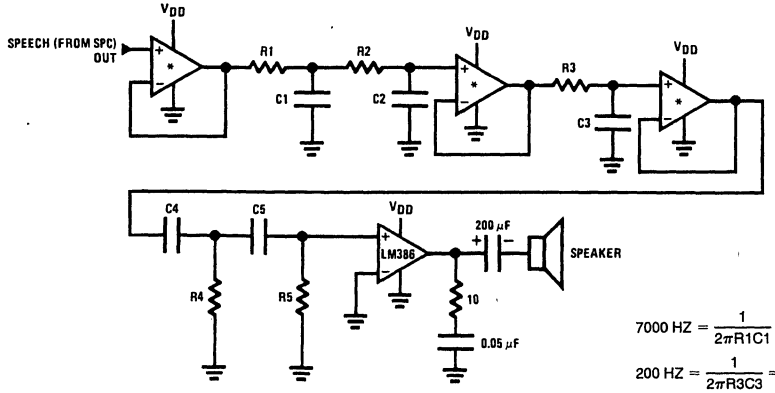
Minimum Filter Circuit



$$200\ \text{Hz} = \frac{1}{2\pi RC}$$

*LM346 or equivalent

Filter Circuit to Produce Maximum Frequency Response

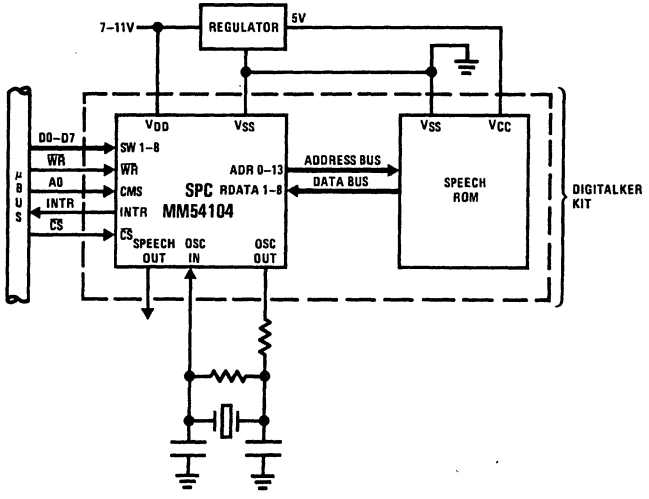


$$7000\ \text{HZ} = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

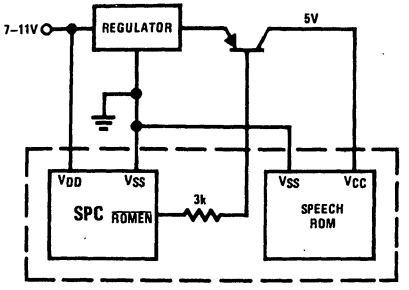
$$200\ \text{HZ} = \frac{1}{2\pi R3C3} = \frac{1}{2\pi R4C4} = \frac{1}{2\pi R5C5}$$

*LM346 or equivalent

DIGITALKER System Utilizing MICROBUS Interface



Low Power Configuration Using Static ROM



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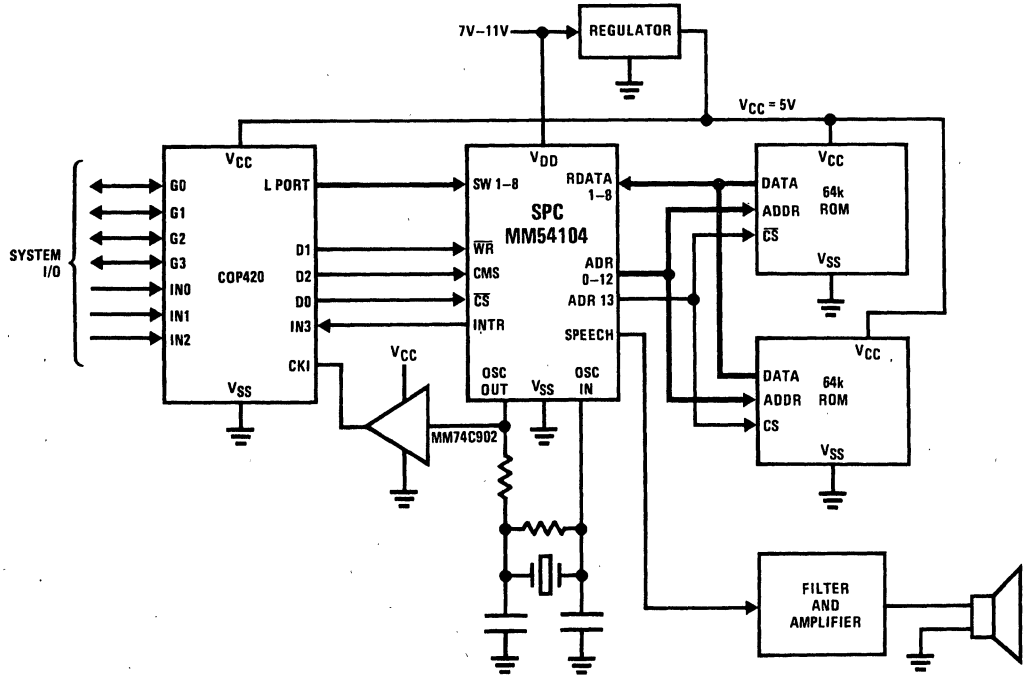
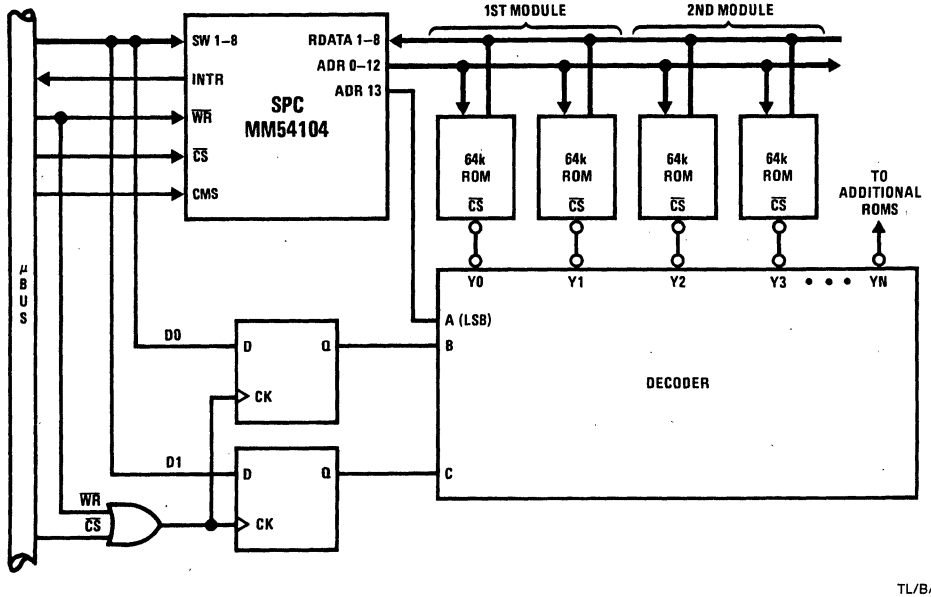
Typical Applications (Continued)

DIGITALKER System Using COP420 Interface



Speech ROM Expansion for Requirements Greater Than 128k Bits



TL/B/5611–8

Implementation of a Speech Synthesizer

National Semiconductor
Technical Paper 18
Fred M. Wickersham
September 1982

The marriage of extensive speech research and large scale integration has made possible substantial end product enhancement with the implementation of low cost speech synthesis integrated circuits. Although driven by a very large and obvious telecommunications market, present day voice synthesizer solutions produce qualities of stored solid state speech at prices attractive to a myriad of consumer, industrial, and military products. It is reasonable to believe that low cost speech synthesizer circuits, such as the National Semiconductor DIGITALKER® system could provide significant product enhancement to many low, medium and high end appliance products.

The typical integrated circuit speech synthesis system utilizes raw speech that has been highly compressed and digitized. This digitized, or synthetic speech is stored in low cost read only memory (ROM). This ROM data is controlled by and fed into a speech processor chip (SPC) which also performs the digital-to-analog conversion and consequent reconstructed speed output. Most synthesizers require only simple filtering and amplification to output intelligible and natural human speech.

The selection of the appropriate phrase or word to be spoken from the synthesizer is generally controlled by an external microprocessor. This microprocessor is typically programmed to monitor various sensing devices, and addresses the appropriate message for a given situation. Some synthesizers, however, will operate without the control of a microprocessor, depending on switch closures or simple logic activation. *Figure 1* shows a typical speech synthesis integrated circuit analysis.

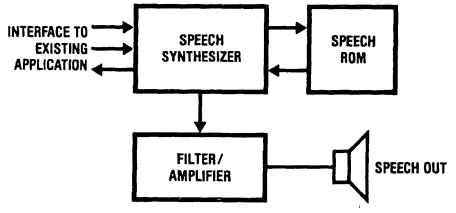


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FIGURE 1. Typical Speech Synthesis System

FACTORS DETERMINING SPEECH SYNTHESIS QUALITY

Synthesis Technique

With the specific goal of generating speech, using low data rates to be attractive to consumer products, several approaches to solving the problem have been tried. Perhaps the most obvious approach was the straightforward analog-to-digital conversion of the raw human speech waveforms. This approach is satisfactory for storing very high quality speech, but the memory requirements are not cost effective for any consumer products. (However, products such as mainframe computers, where large quantities of mass memory are available, could conceivably utilize this approach.) Initial research into the compressing of the raw speech prior to digitizing revealed that the quality is degraded substantially, with only minor compressions and reductions in data rate.

A second approach stemmed from thoughts and strong beliefs that speech could be artificially created, using noise sources and filters. Experiments with this theory proved its feasibility and, in fact, low cost circuitry produced reasonably intelligible but inhuman speech at very low data rates. Further research in this technology evolved and provided human vocal tract models, relying on parametric data extracted from raw human speech waveforms, but highly analyzed by extensive computer software algorithms. The final set of digitized and compressed speech data, under microprocessor or computer control, stimulates noise and impulse sources and creates speech by channeling the noise and impulses through time varying filters. The data rates experienced by the vocal tract model approach proved very promising for consumer product applications, but voice quality still left something to be desired. Typically, the vocal tract model algorithms could be optimized for a single voice, but the difficulty arose in developing a universal algorithm which did a good job in analyzing and reconstructing any voice submitted for synthesis.

The quality of the speech produced by an optimized voice model, however, is typically good, for the most part sounding like natural human speech and is largely intelligible.

During this period of heavy research in the vocal tract model approach, there remained a small community of researchers who continued to believe that raw human speech waveforms could be highly compressed prior to analog-to-digital conversion, without seriously degrading the quality and naturalness of the speech. One particular inventor, Dr. Forrest Mozer, made significant progress in this area, and consequently made possible the DIGITALKER speech synthesis system. This technology again takes raw human speech initially, but then, through a series of processes, compresses the original speech by a factor of 100. Thus it is affordable, and lends itself very nicely to a myriad of consumer products, including appliances.

Unlike the vocal tract model approach, the Mozer technology is capable of reproducing any voice with high quality because it compresses only the raw speech waveform. No attempt at modeling the human vocal tract is made with this process.

The raw human speech waveforms contain all speech data such as pitch, amplitude, inflections, articulation, plus all of the resonances and other features which tend to make a voice unique. By nature of the Mozer process, which is merely, but uniquely, tracking and compressing the original waveform, all of these qualities are retained, thus producing highly intelligible and natural stored speech.

Understanding the synthesis process may not be crucial in determining the appropriate synthesizer for an application, but certainly a thorough listening test is. Extreme care ought to be exercised in evaluating intelligibility, naturalness, clarity, crispness, different voices and foreign languages, in that order.

Certainly for a speech product to be successful in the marketplace, intelligibility of the speech is of prime importance. The testing of intelligibility should be performed by a large set of listeners in the natural environment in which the proposed end product will be utilized. For example, if the synthesizer is to perform a paging function in a department store, the intelligibility ought to be measured in the environment with the usual amounts of background noise of people, commotion, music, cash registers ringing and so on.

Crispness and clarity are important factors governing the degree of intelligibility and, in particular, control the intelligibility within relative distances from the output transducer or loudspeaker. Naturalness is a feature which can enhance a product by adding personality to the product, as opposed to a computerlike voice which can be monotonous, unrealistic, and even offensive.

The idea of different voices for different products is interesting: celebrity voices, "name brand" or even "trademark" voices could segregate competing products. The ability to easily synthesize different voices could protect a Ford from sounding like a Chevy and vice versa. It is expected that manufacturers of competing talking products will take care that the devices will not speak in the same voice. In fact, each manufacturer can select his favorite voice and submit it for synthesis and feel confident his competitor will do the same, therefore alleviating the possibility that both products will sound the same.

Many foreign languages contain complex combinations of sounds which some speech synthesizers have difficulty in reproducing. Samples of the desired language ought to be obtained prior to expending large amounts of money for encoding custom vocabularies. Once again, by nature of the process, the Mozer technology reproduces foreign language waveforms without difficulty.

Single Words vs Complete Phrases

Having decided on the synthesis process desired, ample thought should be given to the accessing approach to the vocabulary which will ultimately be spoken from the end product.

Synthesizer ICs are designed with the capability of accessing address locations. The contents of an address location can be either single words, phrases, or complete sentences.

A potential user's first conclusion is, that since a vocabulary of phrases or sentences is made up of individual words, that it should be necessary to synthesize only each new and different word in the vocabulary, as opposed to all words in the vocabulary.

Each different word could be located at a single address location for concatenation by the microprocessor program, or, each word could be concatenated into phrases or sentences as a part of the speech ROM program. In the latter case, each constructed phrase or sentence would be assigned a single address location. This approach is feasible and can feature tremendous flexibility, in that libraries of singly addressed, synthesized words could provide unlimited phrases or sentences for an end product.

The disadvantage to the single word approach is the poor quality of the actual phrases or sentences constructed. (To appreciate the effect using this approach, think about slicing words from recorded messages on a tape, then placing these clipped words into different phrases or sentences. Words in the context of a sentence have cast intonations and inflections which would be improper in other sentences.)

As a solution to this problem, and not having the ability to arbitrarily blend single words together naturally, it is necessary to speak, record and synthesize each single word in a monotone, or some other consistent intonation so that, when the words are concatenated, there is at least some consistency to the words.

As we humans speak phrases or sentences, we automatically contour the words together with smooth transitions. In fact, we carefully slur words together to provide smooth and flowing speech. The effect that this has to the synthesis process is that it produces an unbroken waveform, from beginning to end. While we speak phrases or sentences, we also add energy to express our state of mind. This energy is also evident in the waveform of the spoken phrase. It should be obvious that waveforms of single words do not look like those waveforms of the same words when spoken in complete sentences.

If natural flowing sentences would be a feature in the end product, the proper approach is to synthesize complete sentences. The result can be compared to playing back a recorded message from a tape recorder. The entire message of the speaking person can be obtained completely, even to retain his state of mind which might be denoting sadness, happiness, urgency, or whatever the relevant situation might require.

Since sentences are, in fact, no more than groups of words slurred together consequently producing a single continuous waveform, the Mozer synthesizing process merely

tracks and compresses the same waveform, thus producing high quality natural stored phrases. Memory requirements in the stored phrase approach may be somewhat larger than the single word approach, but not extensively so. The increase in quality more than outweighs any increase in memory.

It is always advisable to synthesize and store complete and natural phrases and sentences to produce the highest quality of synthesized speech and possibly insure the success of the end product.

It is, however, possible to synthesize a combination of complete phrases and individual words for applications such as a talking clock where "the time is" is a complete phrase and single numbers properly sequenced speak the appropriate time of day.

There are some special cases where a single synthesized word can appropriately fit as a part of many phrases. These are words that are typically used in the same place in each phrase and have the same intonation each time such as "check oven time" and "check oven temperature" and "check turn off time."

Voice Qualities

The typical process of any synthesizer relies initially on a selected human speaking the actual phrases to be spoken from the end product. Usually, a high quality tape recording is made of the favorite person speaking the required messages. The tape is then submitted to the synthesizer manufacturer for analysis, compression, and digitizing.

Even though some synthesizers reproduce any voice quite nicely, there are still suggestions and guidelines to be observed in selecting a desired voice which would probably apply to any manufacturer's speech synthesizer.

The best voice in either male or female is a solid, non-breathy, crisp, clear, medium pitched voice. Some products might suggest a "sexy" connotation but sexiness in a voice is usually associated with extensive breathiness. Breathiness tends to expand memory requirements quickly and significantly, and usually does not duplicate or synthesize with good quality. Deep pitched male voices tend to get raspy, as sub-100 Hz frequencies are approached, or else become exceedingly breathy, and can, in fact, excede the lower frequency limits of synthesizers.

Because women's voices are higher in frequency, they usually require more memory for synthesis and storage. Similarly to the male voice, a high pitched female or child's voice can excede upper frequency limits of the synthesizer circuit. In these cases, the synthesizing process clamps or flattens the frequency to its upper and/or lower frequency limit, which tends to make the synthesized speech not totally representative of the original person.

Once again, a medium pitched clear, crisp, non-breathy voice will yield the most pleasing results.

Filters, Baffles, and Speakers

The reader of this paper should begin to appreciate how each part of the synthesis process depends on the next. Having gone through great effort to understand the synthesizer circuit which will provide the best quality, having chosen the best voice for the job, and having produced the tape recording for synthesis, one should understand that no less effort should be put into filtering, baffling and choosing the appropriate output transducer or speaker which, in the end, "speaks" the synthesized messages.

The typical speech synthesizer requires only a simple filter, but care and some experimentation should be performed to understand appropriate frequency cutoffs. These cutoffs are high or lowpass filters or combinations of high and lowpass filters which contour the output speech waveform. Suggestions for proper filter cutoff frequencies are given, but, by and large, these frequencies can be determined by varying the filter values while actually listening to the speech output. In this way, the filter values are decided by what sounds most pleasant to the ear.

Baffles, or the speaker enclosures are also a pertinent part of the entire system. The output transducer or speaker stand alone, without any sort of enclosure, although perfectly capable of outputting audio, actually depends on some type of enclosure to faithfully reproduce the original required sounds. Speakers without baffles or enclosures tend to sound empty and generally lose the majority of the low frequency components of the audio. For this reason, most quality audio product manufacturers have paid ample attention to the design of the enclosure which houses the output speaker.

A speech synthesizer is no different than any other product requiring a quality audio output, in that the quality of speech output is very much dependent on having and designing an appropriate baffle.

The final section of the speech synthesis audio system is the output transducer itself. Speakers come in thousands of varieties to include wattage values, frequency response, physical size, and price. Unfortunately, for most consumer products the tendency is to choose a speaker based on price and physical size only. *Again, not unlike any other quality audio system, the speaker used in the speech synthesis system ought to be chosen in such a way as to complement and/or enhance the actual synthesized vocabulary.*

In particular, to reproduce the human voice frequency response, one needs to choose a speaker which has a bandwidth from 60 Hz to about 7000 Hz. Although most ordinary speakers feature this range, physical size (speaker diameter) can impact quality severely. Extremely small speakers in the 1.5 inch to 5 inch diameter range tend to lack bass response that is critical when reproducing a male voice. True, the small speakers will respond to the male frequencies but fullness and robustness is not included. On the other hand, large speakers, unless compensated, do not enhance high frequencies typical in a female voice. Large uncompensated speakers tend to have a muffled effect on higher frequency female or children's voices. This is not to indicate that a small speaker would be perfect for a female voice because, as in the male voice, it depends on a certain amount of low frequency response to maintain fullness and robustness.

The recommendation is that the product designer actually test different sizes of baffled speakers with the speech synthesizers and make decisions based on the combination most pleasing to the ear.

Having selected an appropriate speaker, and having an understanding of baffling effects, the synthesizer ought to be "tuned" to the actual speaker and baffle to be used in the actual production prototype by once again performing listening tests with a variable filter bank between the synthesizer and speaker. In this way, filter cutoff values can be determined based on the combination most pleasing to the ear.

APPROACHES TO INTERFACING TO MECHANICAL AND ELECTRONIC SYSTEMS

Before discussing the interfacing of a speech synthesizer into a specific application, it is necessary to have an understanding of all input and output functions of the particular synthesizer desired.

The particular synthesizer of interest in this paper looks like a typical peripheral on an 8-bit microprocessor bus. The SPC relies on a chip select to activate the entire circuit logic, an 8-bit code which corresponds to some word or phrase applied to the SW1–SW8 address lines, and a write strobe to begin the selected speech output. At the end of any address speech output, an interrupt is provided to the bus to indicate that the previously selected message is completed.

While the variety of synthetic speech applications are numerous, the actual implementation in any single application is usually limited to one of the following three techniques:

(a) single channel, hardware control logic

(b) single channel, software control logic

(c) multichannel, hardware or software control logic.

Each of these circuit approaches for the SPC will be discussed in this section.

Certain applications require a relatively small number of sentences or announcements with very little similarity between the different sentences. An example of this application might be a talking elevator controller where the messages are brief and non-redundant, such as "going up", "first floor", "second floor", etc. In this application, certain words are used repeatedly but the number of messages is short. This application and others just like it do not require the assembly of short phrases into complete sentences, nor do they require a dynamic message structure as would be required with an automatic bank teller speaking "your change is ten dollars", where a monetary amount may change from message to message. This fixed message application, therefore may require only the minimum control circuit as shown in *Figure 2*.

In *Figure 2*, the SPC receives a separate coded input for each complete sentence or word that is synthesized. This input code is received by the SPC through the SW1–SW8 ports. The circuit shown in *Figure 2* uses a mechanical switch group to interface to the SPC. These mechanical switches could be toggle switch banks, relays, microswitches, or even rotating thumbwheel switches that put out coded outputs. In the simplest of applications, and if the application only requires up to eight discrete messages, the speech ROM could be coded such that a positive voltage on any one of the SW lines would cause any one of the 8 messages to be spoken.

After the proper message address is established on the SW ports, a momentary pulse must be applied to the $\overline{WR}$ line. If this signal is applied with a momentary action switch, as shown in *Figure 2*, then an external pull-up resistor should be used to pull the $\overline{WR}$ line up to logic high and complete the on-chip debounce circuitry. The $\overline{WR}$ input signal will latch the coded message address into the SPC on the rising edge of $\overline{WR}$ and initiate the speech message. Since each complete message uses a unique address code of the SW ports, no further control action is required after this point. The SPC will speak the requested message and return to the idle state. If a new input command signal is received, either during or after a message is spoken, the SPC will immediately abort the current message and begin the new message. This is a priority override, if you will, to allow superseding the present speech output with a more important message.

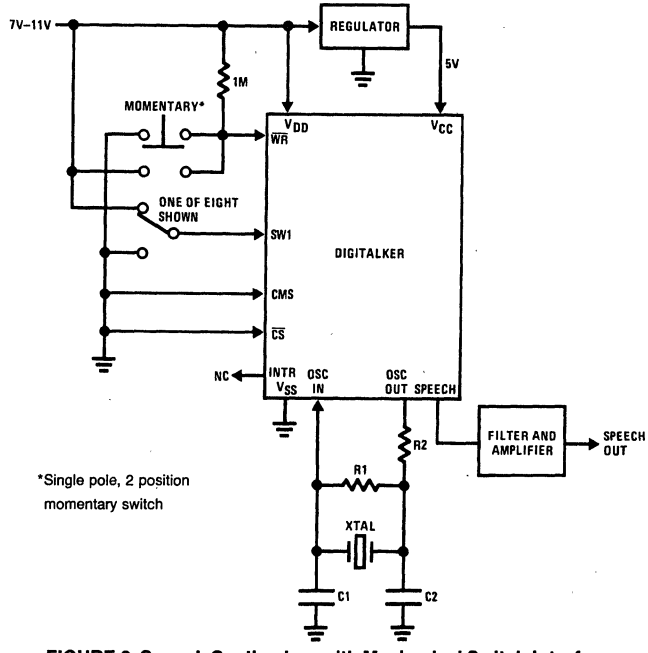

FIGURE 2. Speech Synthesizer with Mechanical Switch Interface

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In *Figure 3,* a message is initiated whenever a valid address code is detected by the combinational logic decoder and timed to insure that all transitions have died. Once the valid code is timed, a set/reset latch is set and a $\overline{WR}$ rising edge is generated to start the SPC. The circuit in *Figure 3* shows a lockout circuit to prevent the aborting of a current message, so that all messages must be completed before a new message can be initiated. Once the message has ended, the SPC will set the INTR line to the high state and a reset pulse will be generated to reset the lockout latch. A new speech message can now be started by momentarily applying an idle address code for the next message of interest, followed by a valid code on the SW input ports.

While the simple control schemes discussed so far can be used in many applications, a far more important group of applications will take advantage of the SPC's ability to construct sentences from cast phrases and groups of words. This type of application uses an intelligent controller or a microprocessor to string together a group of synthesized phrases, or combinations of phrases and individual words. The electronic bank teller previously mentioned is a good example of this application. The microprocessor controls the stringing of SPC address codes and applies them, one at a time, to the SW address ports of the SPC. Handshake timing between the microprocessor and the SPC is provided with the interrupt line. This microprocessor interface arrangement is shown in *Figure 4.*

The use of a microprocessor controller expands the versatility of the SPC significantly. Messages that are composed of numerical responses or fixed phrases in random sequence can easily be constructed from a library speech memory. In addition, various tones or warnings can be synthesized and added before, during, or after an announcement to identify the urgency of each message. For example, an automobile message may state that "oil pressure is low". Alone, that message may mean only that pressure has dropped but no immediate hazard exists. If, however, pressure has dropped below a critical value, the message could be compounded to say "warning—oil pressure is low, pull over and stop the engine". In this latter case, phrases of high urgency are added to the initial message to increase its level of importance. Of course, the second message is not completely separate from the first but is, instead, an expansion of the first. This technique allows fewer input address codes to initiate a larger number of messages without assigning a separate address code for each message and for each of its derivatives. This would be particularly important to an electronic bank teller, since a large number of monetary amounts must be synthesized for a relatively small number of finished sentences.

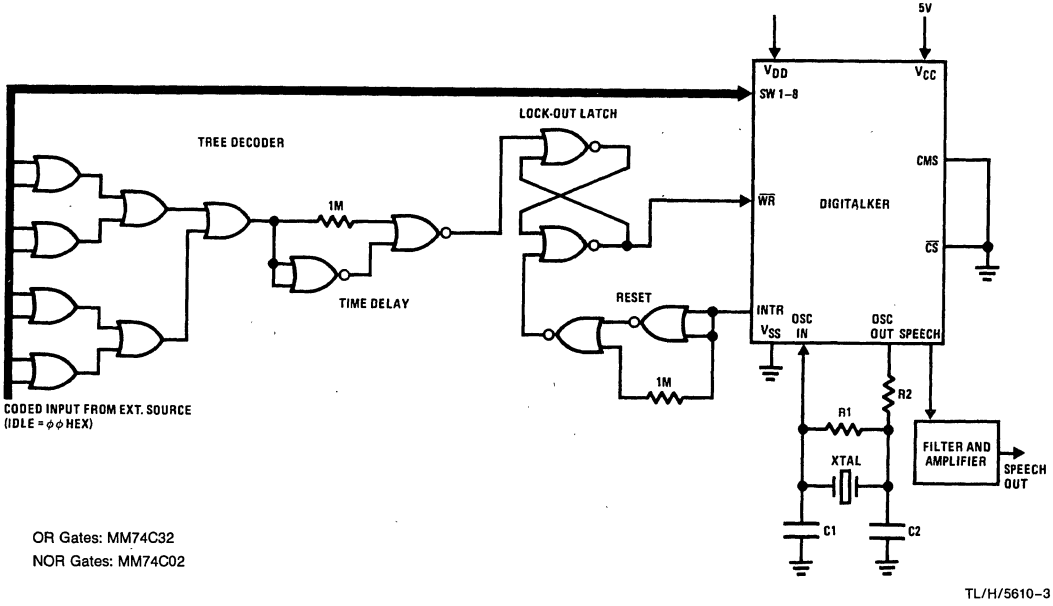

FIGURE 3. Speech Synthesizer with Logic Control Interface

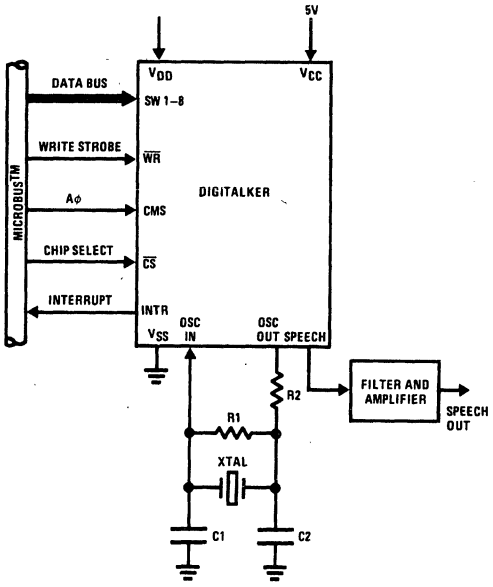

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FIGURE 4. Typical Microprocessor Interface

Although the SPC works typically in an 8-bit microprocessor system, it will work equally as well in a 4-bit microprocessor system. 4-bit systems are usually very low cost solutions for lower end consumer and industrial products. *Figure 5* shows a typical interface approach to a common low cost 4-bit microprocessor.

The final application technique to be covered is the multi-channel configuration. The previous arrangements used an SPC and dedicated speech ROMs to provide a single channel of synthetic speech. Appliances, autos, toys, terminals, etc., would probably use a single channel SPC arrangement. But an entirely different group of products could take advantage of a multiple channel approach to reduce the ROM requirements. This group of products includes multiple elevator controllers, electronic bank tellers, multiple pupil learning centers, voice response telephone answering centers, etc. In this application, each channel would use a separate SPC and amplifier circuit, but several channels would share a common speech library ROM. A typical configuration is shown in *Figure 6.*

The library ROM of *Figure 6* is shared over eight SPC channels. Through a series of octal buffers and registers it is possible to interface up to 8 SPC devices to a common speech ROM. The hardware and timing requirements in this application are rather uncomplicated and straightforward as shown in the diagram. The system can be further expanded to as many as 16 lines with the addition of a 4-to-16 line decoder. The entire application hardware and wiring can then be even further simplified by multiplexing address and data over the same parallel bus. This system is demonstrated by *Figure 7.*

This approach is particularly attractive when each SPC channel is located on an individual circuit card. A telephone central office or PABX announcement system is a typical example of a single channel per card per channel arrangement, but the idea is certainly not limited to just that application.

REFERENCES

Smith, Jim and Weinrich, David W., AN-252 Speech Synthesis, National Semiconductor Corporation, December 1980.

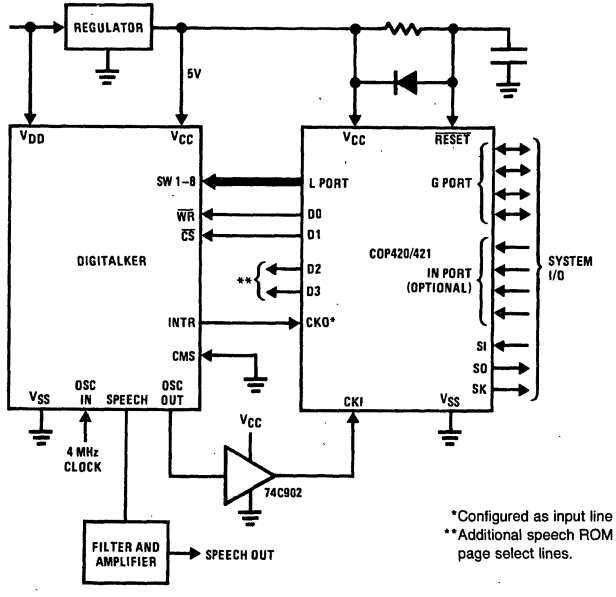

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FIGURE 5. Interface to 4-Bit Microprocessor

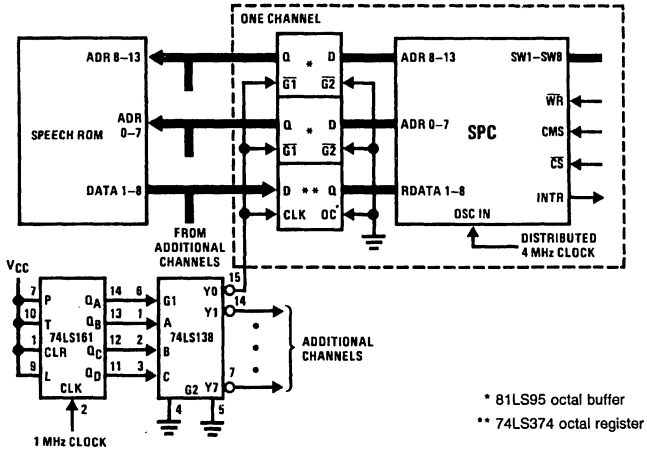

FIGURE 6. Multichannel Speech Synthesizer

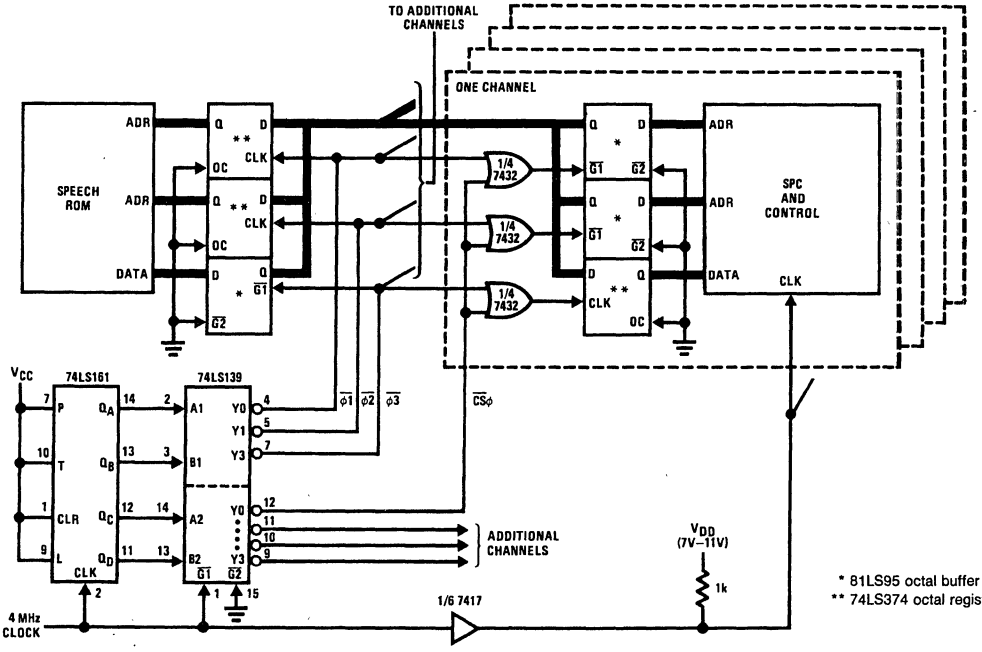

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FIGURE 7. Multichannel Synthesizer with Unified Bus

Section 15

Special Analog Functions

Special Analog Function

Section Contents

National Semiconductor

PRELIMINARY

LP395 Ultra Reliable Power Transistor

General Description

The LP395 is a fast monolithic transistor with complete overload protection. This very high gain transistor has included on the chip, current limiting, power limiting, and thermal overload protection, making it difficult to destroy from almost any type of overload. Available in an epoxy TO-92 transistor package this device is guaranteed to deliver 100 mA.

Thermal limiting at the chip level, a feature not available in discrete designs, provides comprehensive protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive die temperature.

The LP395 offers a significant increase in reliability while simplifying protection circuitry. It is especially attractive as a small incandescent lamp or solenoid driver because of its low drive requirements and blowout-proof design.

The LP395 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LP395 as with any transistor. When the device is used as an emitter follower with a low source impedance, it is necessary to insert a 4.7 KΩ resistor in series with the base lead to prevent possible emitter follower oscillations. Also since it has good high frequency response, supply bypassing is recommended.

Areas where the LP395 differs from a standard NPN transistor are in saturation voltage, leakage (quiescent) current and in base current. Since the internal protection circuitry requires voltage and current to function, the minimum voltage across the device in the on condition (saturated) is typically 1.6 Volts, while in the off condition the quiescent (leakage) current is typically 200 μA. Base current in this device flows out of the base lead, rather than into the base as is the case with conventional NPN transistors. Also the base can be driven positive up to 36 Volts without damage, but will draw current if driven negative more than 0.6 Volts. Additionally, if the base lead is left open, the LP395 will turn on.

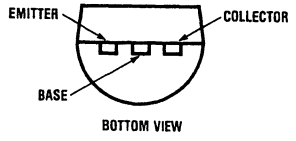
The LP395 is rated for operation over a −40°C to +125°C range.

Features

- Internal thermal limiting
- Internal current and power limiting
- Guaranteed 100 mA output current
- 0.5 μA typical base current
- Directly interfaces with TTL or CMOS
- +36 Volts on base causes no damage
- 2 μs switching time

Connection Diagram

TO-92 Package



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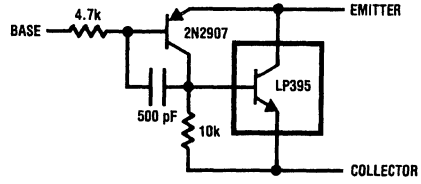
Order Number LP395Z
See NS Package Z03A

Typical Applications

Composite PNP



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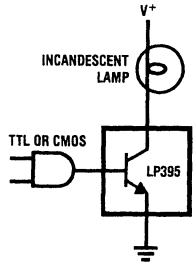
Fully Protected Lamp Driver



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Absolute Maximum Ratings

Collector to Emitter Voltage	36V	Collector Current Limit	Internally Limited
Collector to Base Voltage	36V	Power Dissipation	Internally Limited
Base To Emitter Voltage (Forward)	36V	Operating Temperature Range	−40°C to +125°C
Base to Emitter Voltage (Reverse)	10V	Storage Temperature Range	−65°C to +150°C
Base to Emitter Current (Reverse)	20 mA	Lead Temperature (Soldering, 10 seconds)	260°C

Electrical Characteristics

Symbol	Parameter	Conditions	Typical	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limit)
V_{CE}	Collector to Emitter Operating Voltage	$0.5\ mA \le I_C \le 100\ mA$		36	**36** (Note 1)	V(Max)
I_{CL}	Collector Current Limit (Note 4)	$V_{BE} = 2V, V_{CE} = 36V$ $V_{BE} = 2V, V_{CE} = 15V$ $V_{BE} = 2V, 2V \le V_{CE} \le 6V$	45 90 130	25 60 100	**20** **50** **100**	mA(Min) mA(Min) mA(Min)
I_B	Base Current	$0 \le I_C \le 100\ mA$	−0.3	−2.0	**−2.5**	μA(Max)
I_Q	Quiescent Current	$V_{BE} = 0V, 0 \le V_{CE} \le 36V$	0.24	0.50	**0.60**	mA(Max)
$V_{CE(SAT)}$	Saturation Voltage	$V_{BE} = 2V, I_C = 100\ mA$	1.82	2.00	**2.10**	V(Max)
BV_{BE}	Base to Emitter Breakdown Voltage (Note 4)	$0 \le V_{CE} \le 36V, I_B = 2\ \mu A$		36	**36**	V(Min)
V_{BE}	Base to Emitter Voltage (Note 5)	$I_C = 5\ mA$	0.69	0.79	**0.90**	V(Max)
		$I_C = 100\ mA$ (Note 4)	1.02		**1.40**	V (Max)
t_S	Switching Time	$V_{CE} = 20V, R_L = 200\Omega$ $V_{BE} = 0V, +2V, 0V$	2			μsec
θ_{JA}	Thermal Resistance Junction to Ambient	0.4″ leads soldered to printed circuit board	150		**180**	°C/W (Max)
		0.125″ leads soldered to printed circuit board	130		**160**	°C/W (Max)

Note 1: Parameters identified with **boldface type** apply at temp. extremes. All other numbers, unless noted apply at +25°C.

Note 2: Guaranteed and 100% production tested.

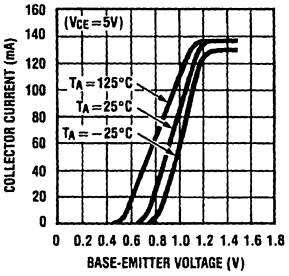
Note 3: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: These numbers apply for pulse testing with a low duty cycle.

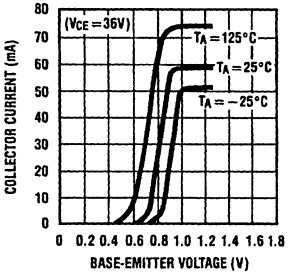
Note 5: Base positive with respect to emitter.

Typical Performance Characteristics

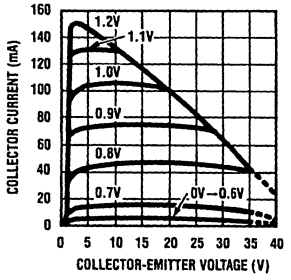
5 Volt Transfer Function



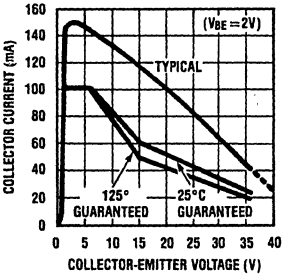
36 Volt Transfer Function



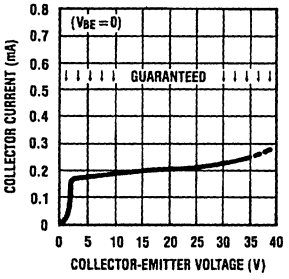
Collector Characteristics



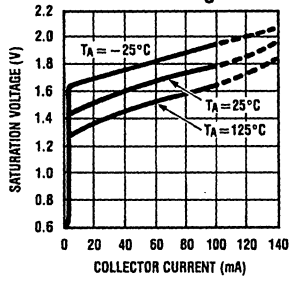
Available Collector Current



Quiescent Collector Current



Saturation Voltage



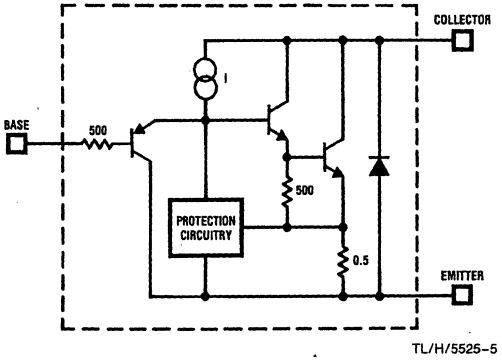
TL/H/5525–4

Typical Applications

Note:

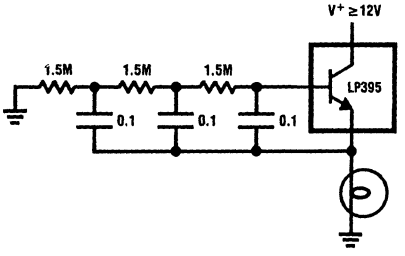
One failure mode incandescent lamps may experience is one in which the filament resistance drops to a very low value before it actually blows out. This is especially rough on most solid-state lamp drivers and in most cases a lamp failure of this type will also cause the lamp driver to fail. Because of its high gain and blowout-proof design, the LP395 is an ideal candidate for reliably driving small incandescent lamps. Additionally, the current limiting characteristics of the LP395 are advantageous as it serves to limit the cold filament inrush current, thus increasing lamp life.

LP395 Simplified Circuit



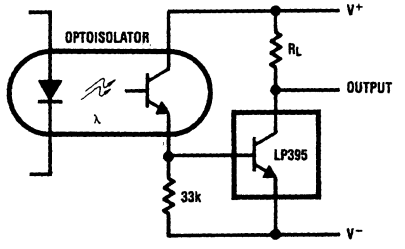
TL/H/5525–5

Lamp Flasher (Short Circuit Proof)



TL/H/5525–6

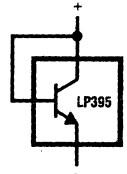
Optically Isolated Switch



TL/H/5525–7

Typical Applications (Continued)

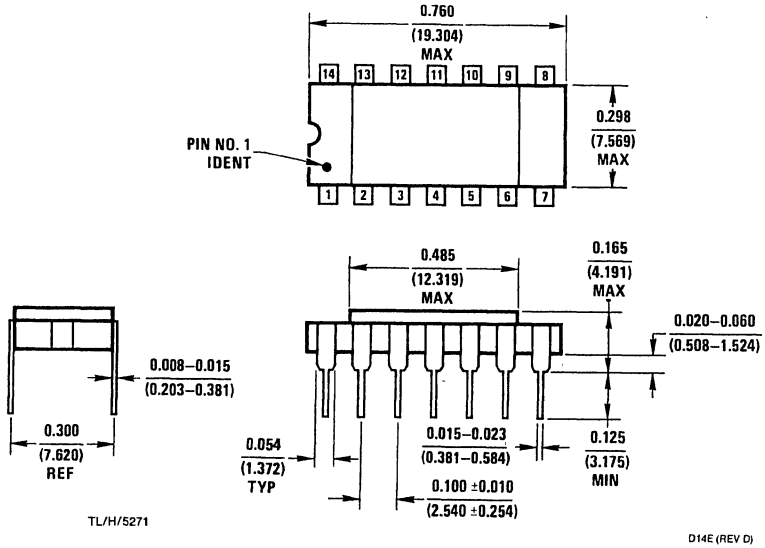
Two Terminal Current Limiter



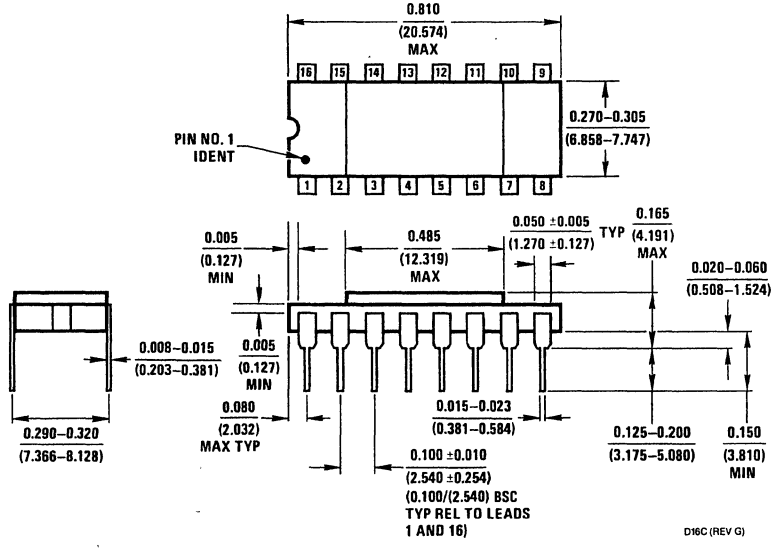
TL/H/5525–08

Section 16

Physical Dimensions

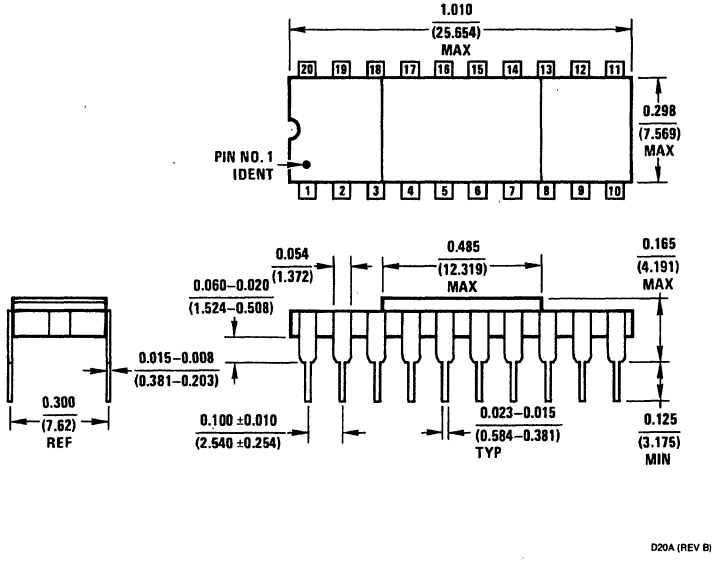


NS Package D14E



NS Package D16C

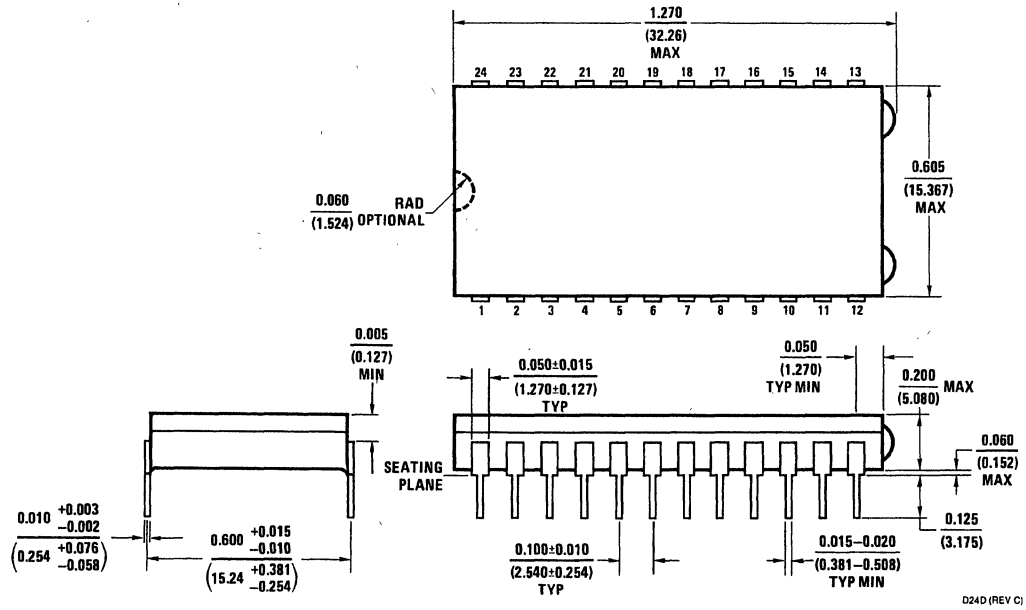
S 16



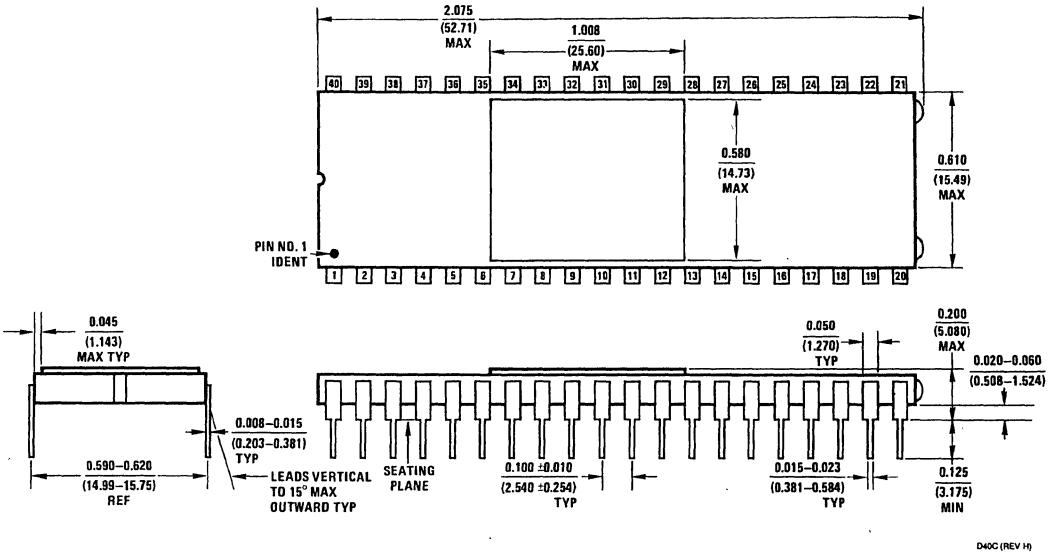
NS Package D20A

NS Package D22A has been replaced by NS Package J22A.

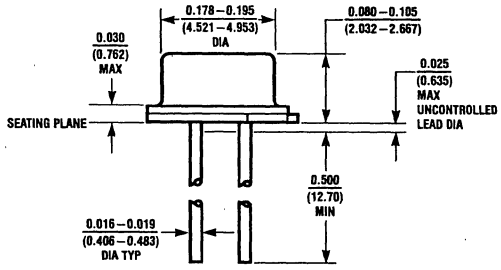
NS Package D24A has been replaced by NS Package J24A.

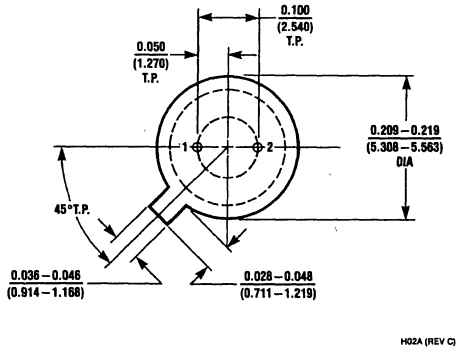


NS Package D24D



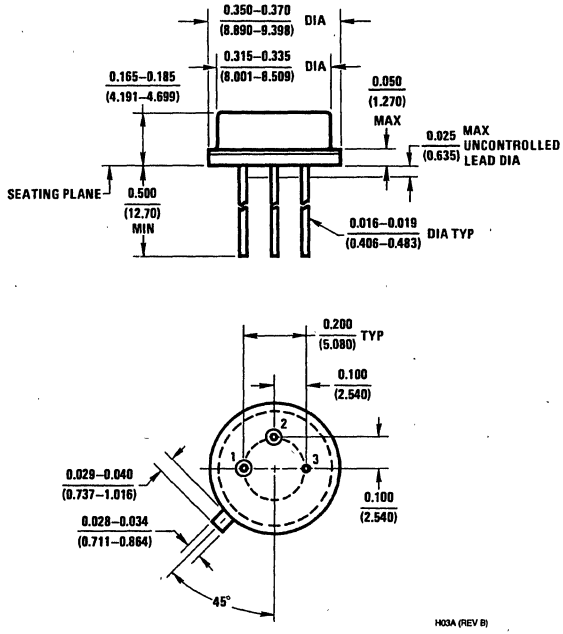
NS Package D40C



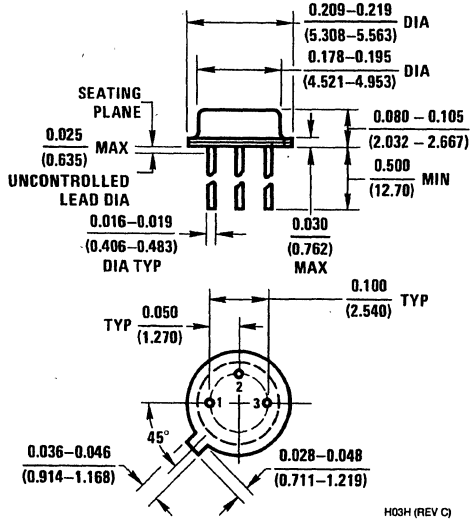


NS Package H02A

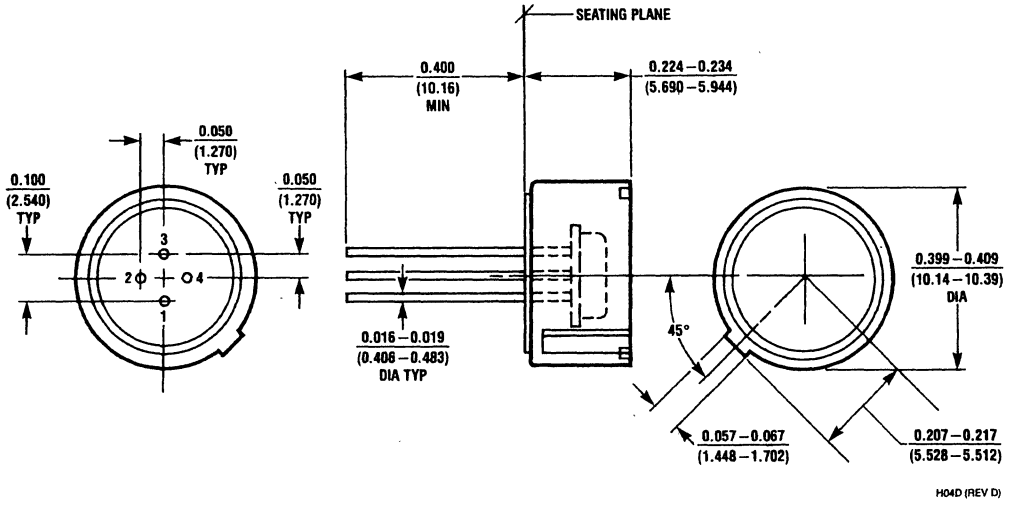
S
16



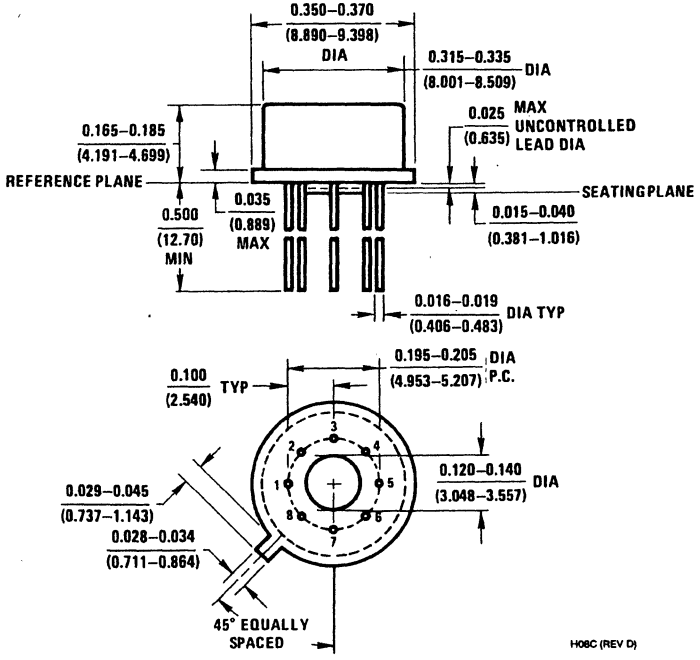
NS Package H03A



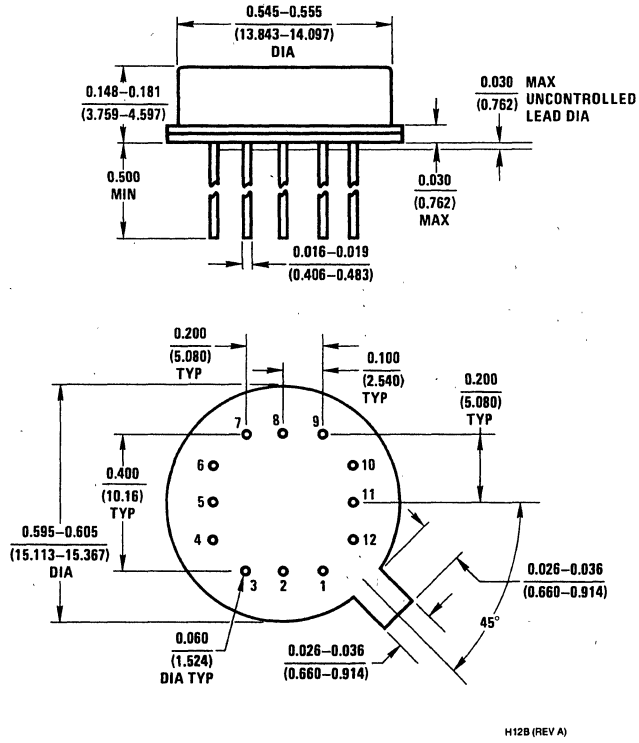
NS Package H03H



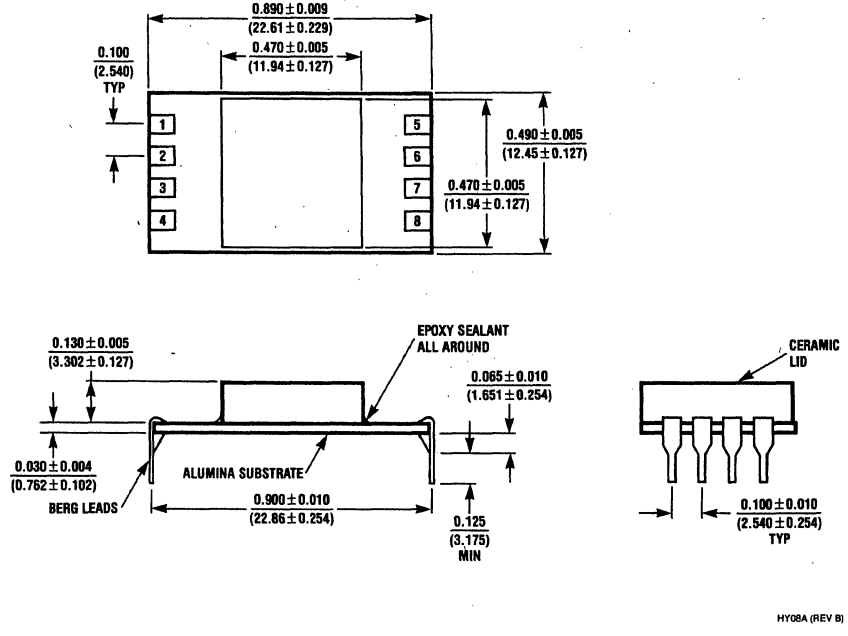
NS Package H04D



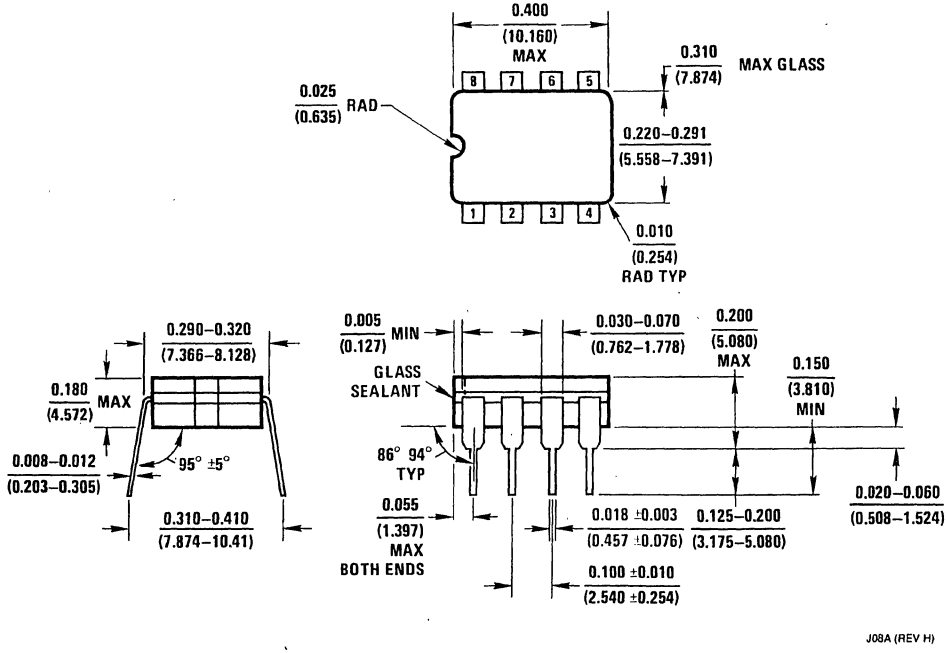
NS Package H08C



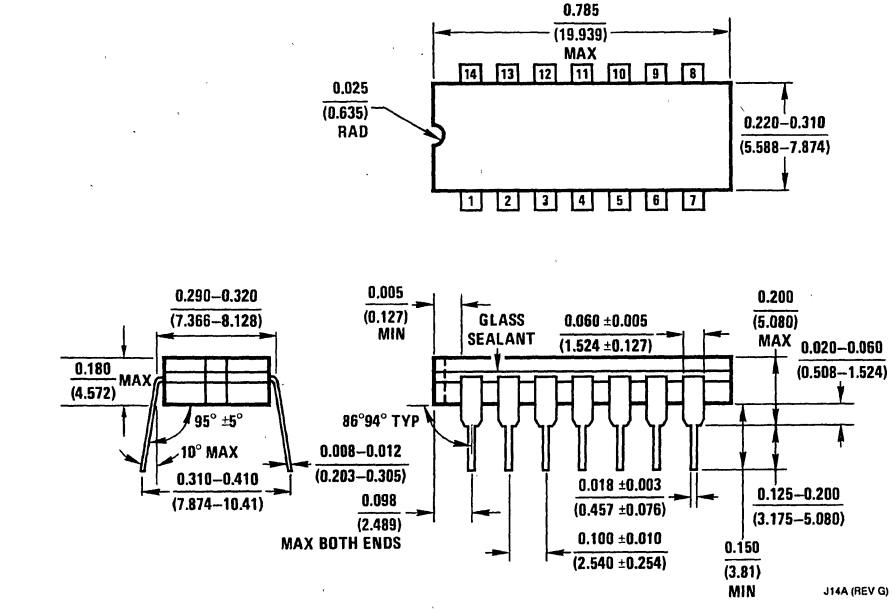
NS Package H12B



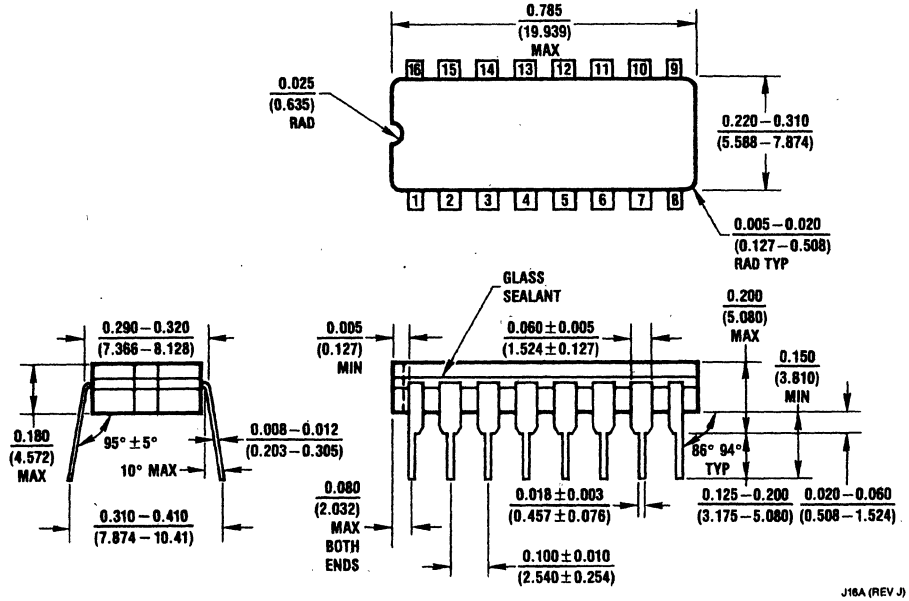
NS Package HY08A



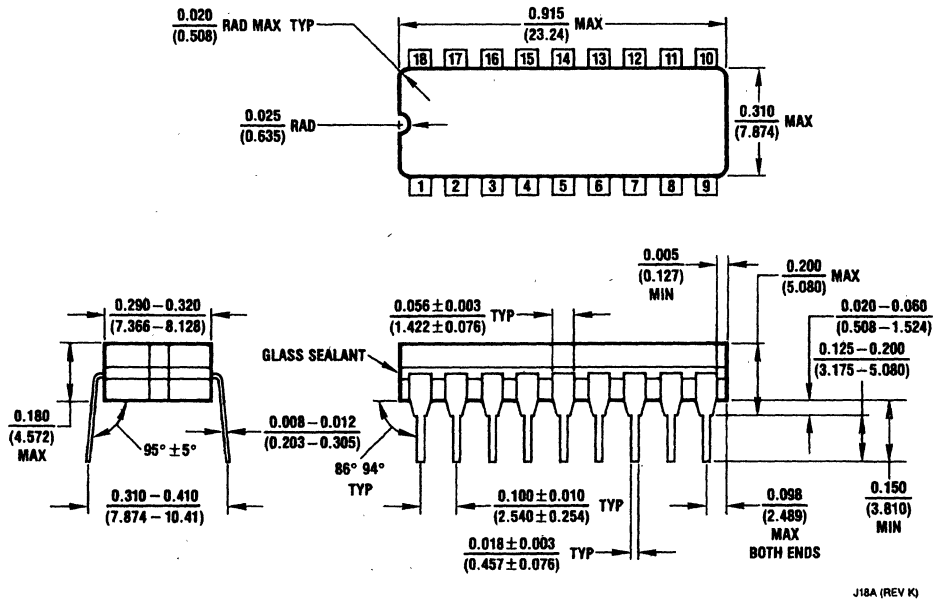
NS Package J08A



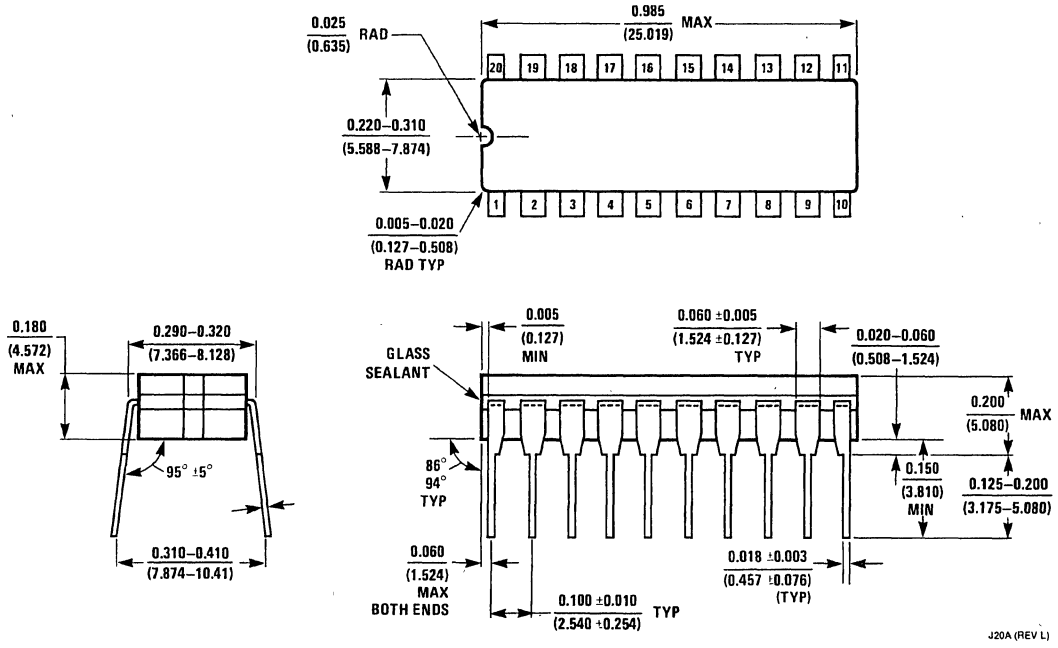
NS Package J14A



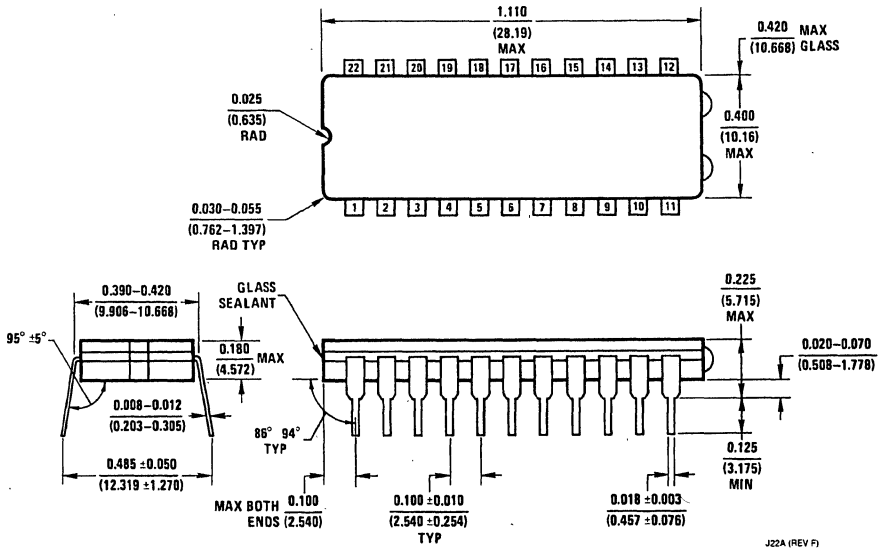
NS Package J16A



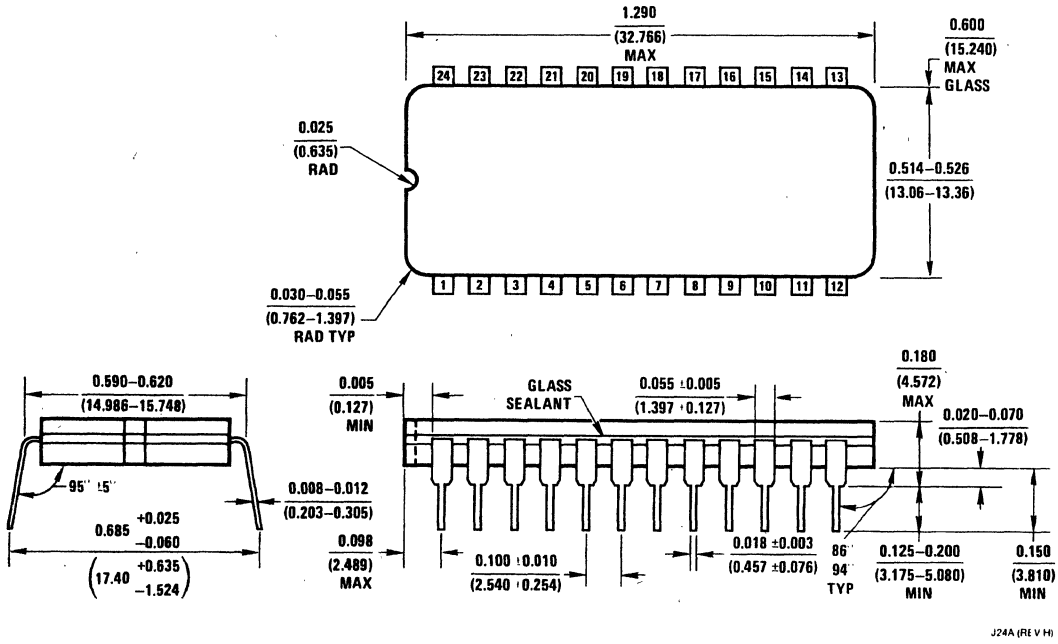
NS Package J18A



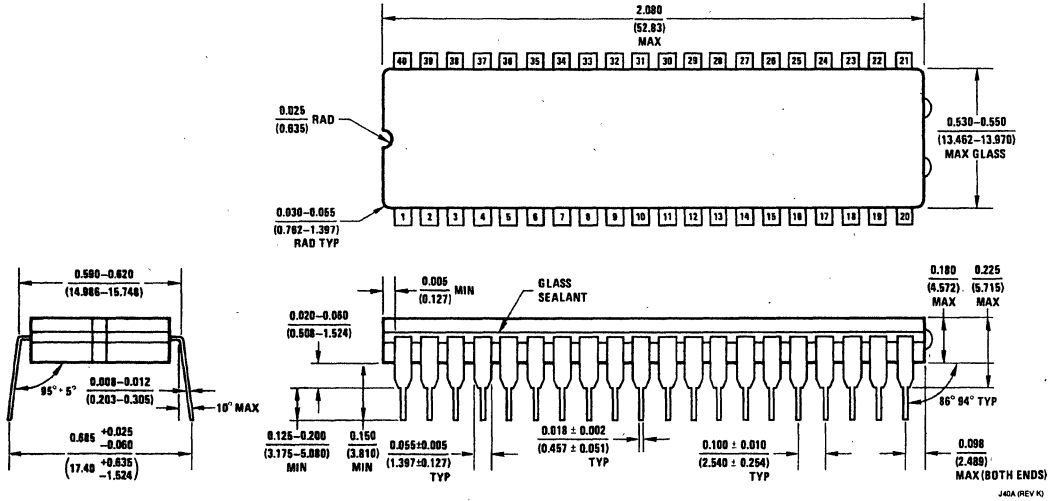
NS Package J20A



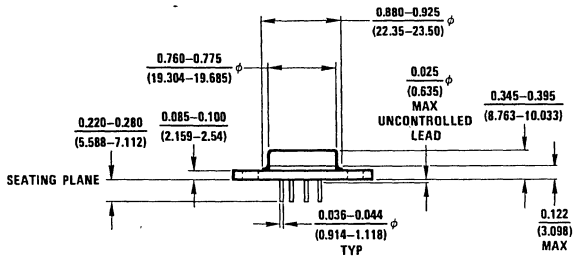
NS Package J22A

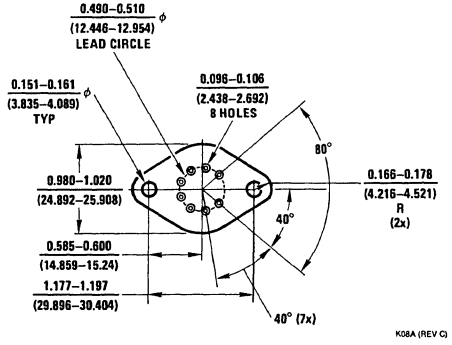


NS Package J24A

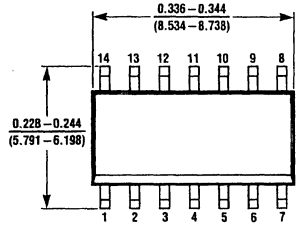


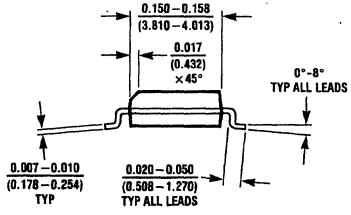
NS Package J40A

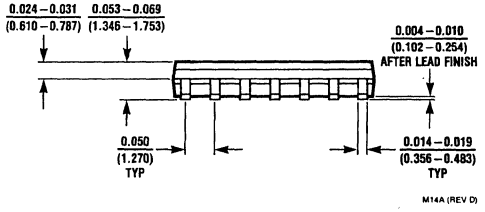




NS Package K08A



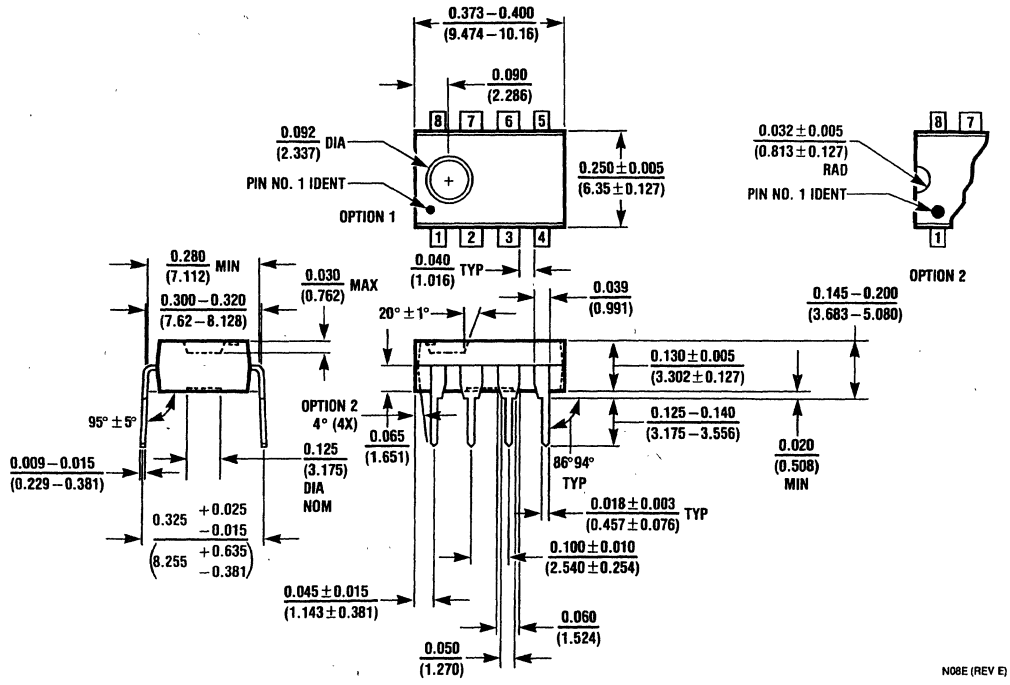




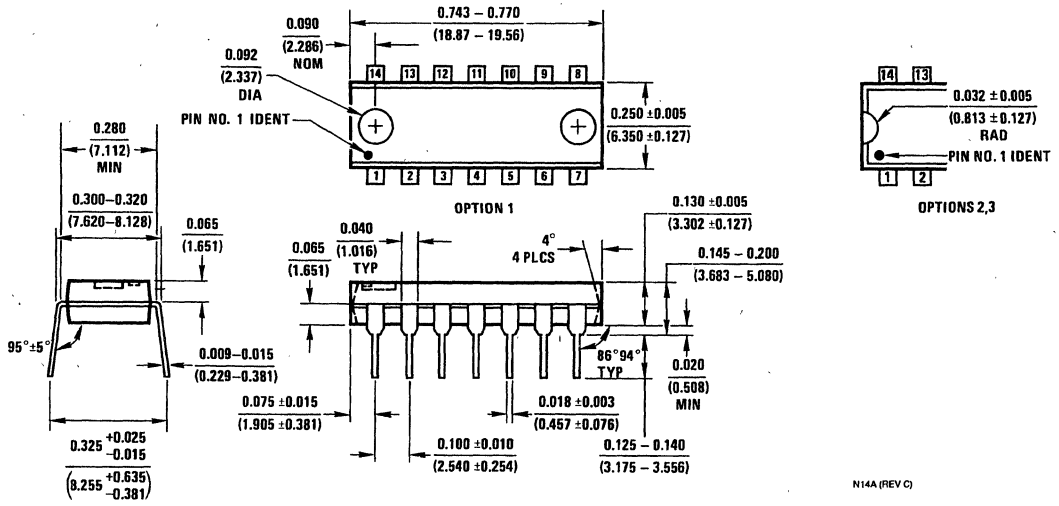
NS Package M14A

S 16

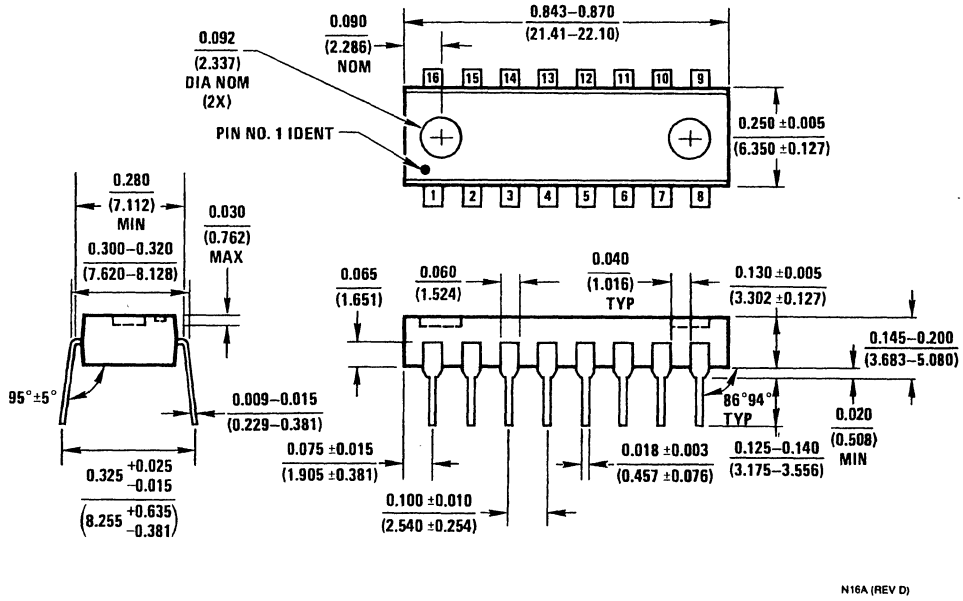
NS Packages N08A and N08B have been replaced by NS Package N08E.



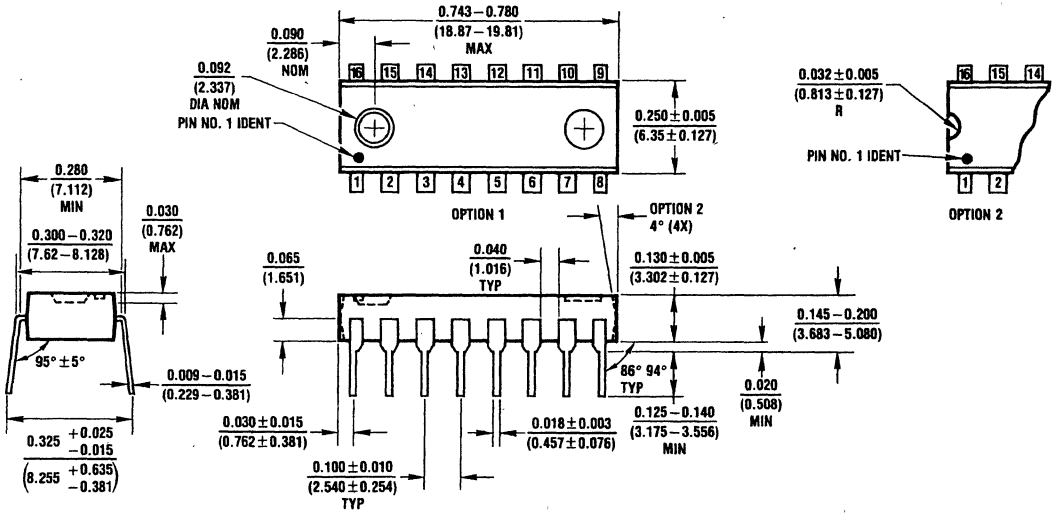
NS Package N08E



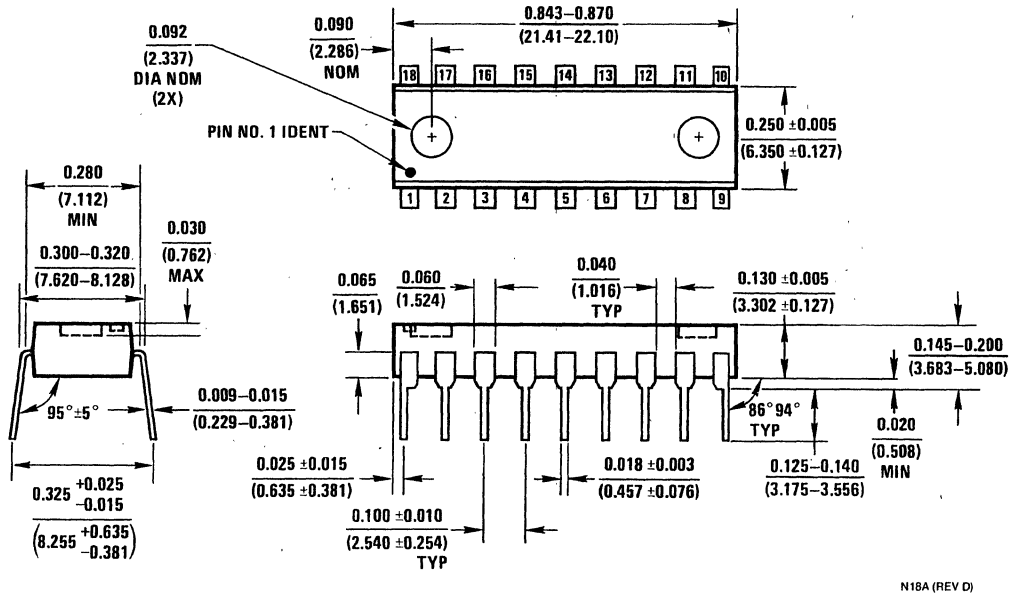
NS Package N14A



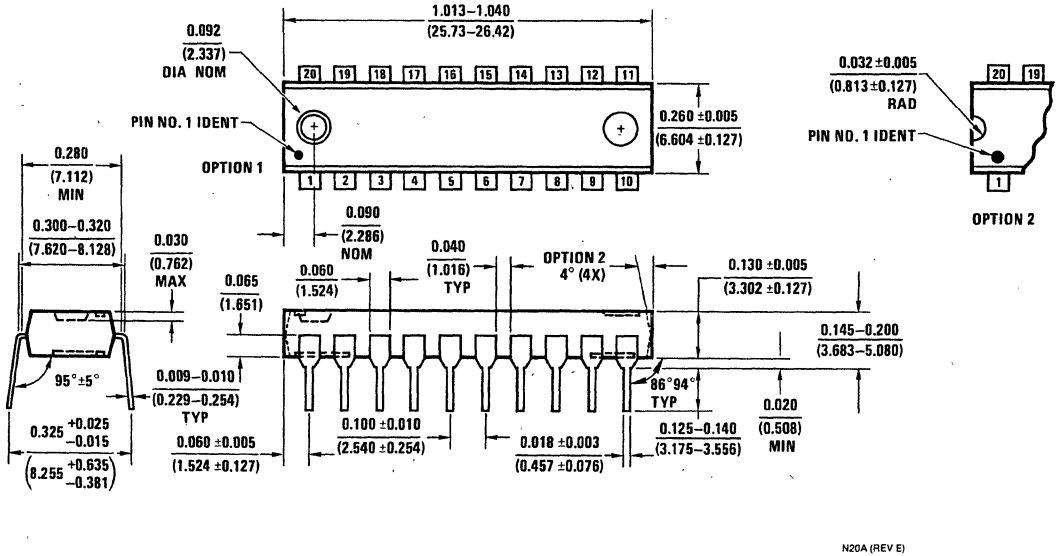
NS Package N16A



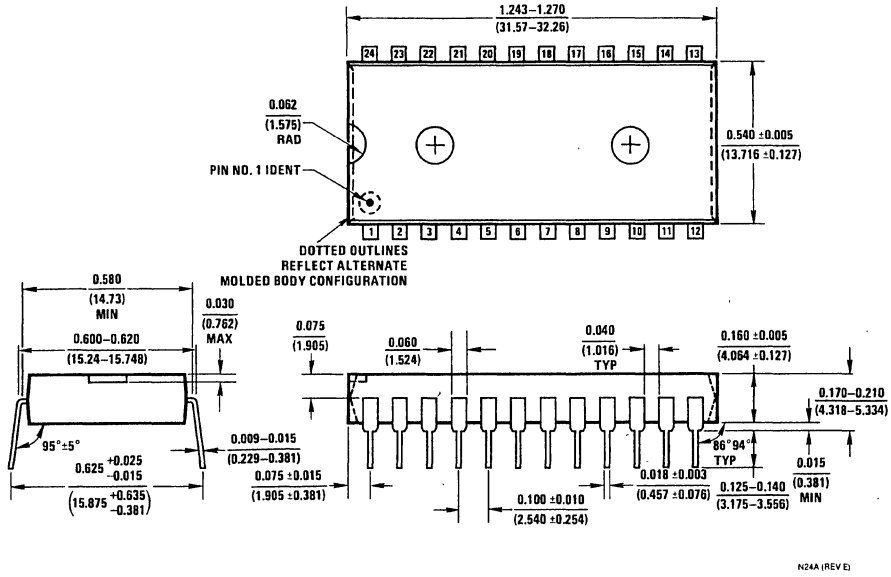
NS Package N16E



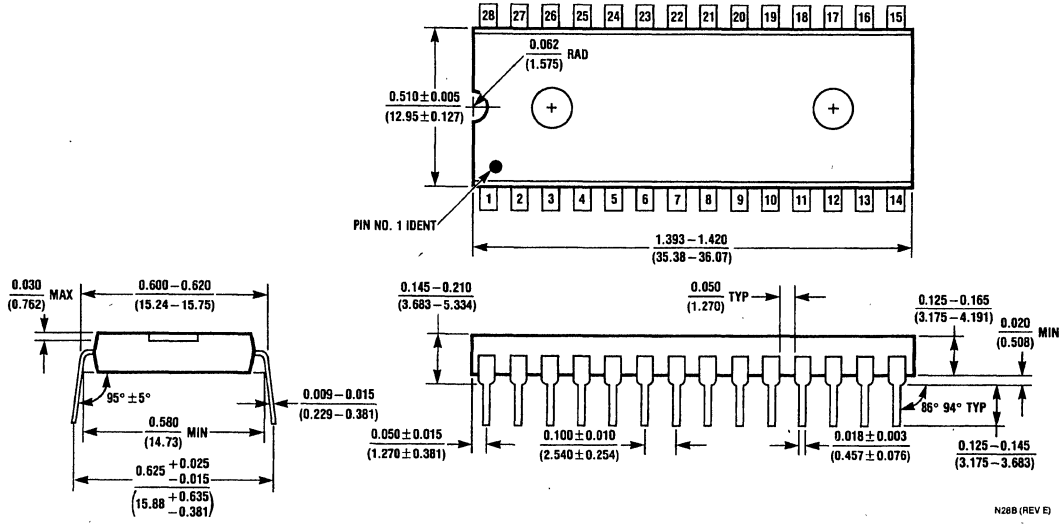
NS Package N18A



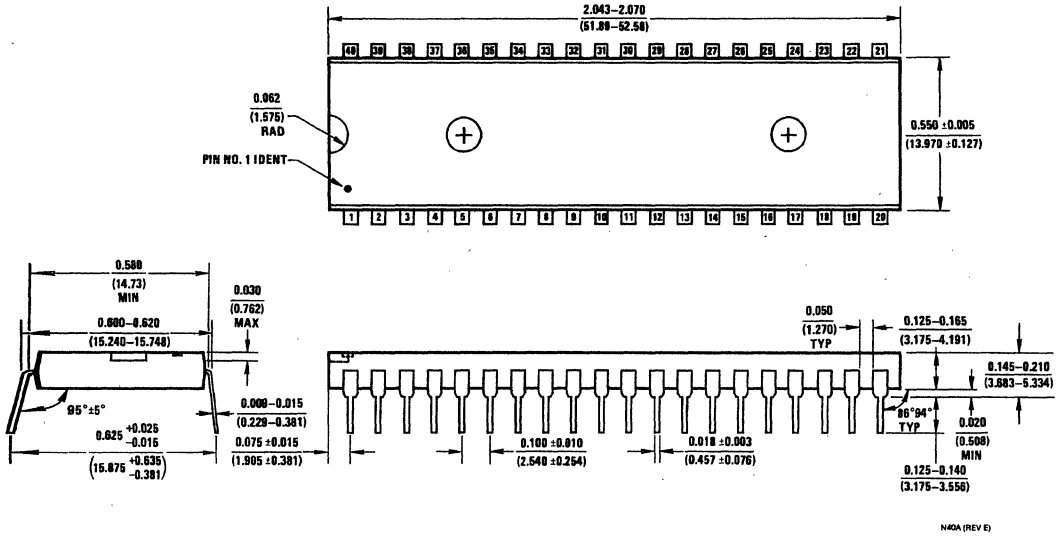
NS Package N20A



NS Package N24A



NS Package N28B



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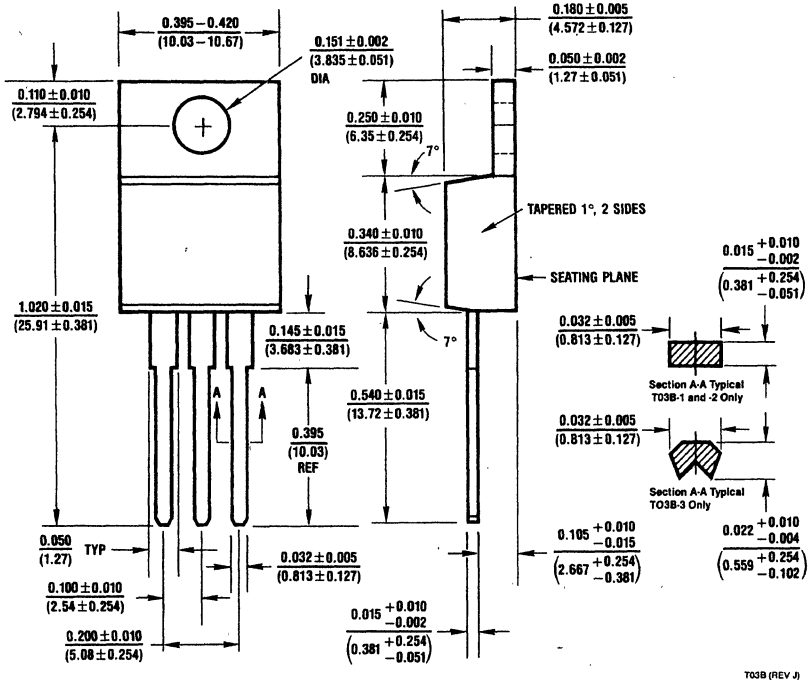

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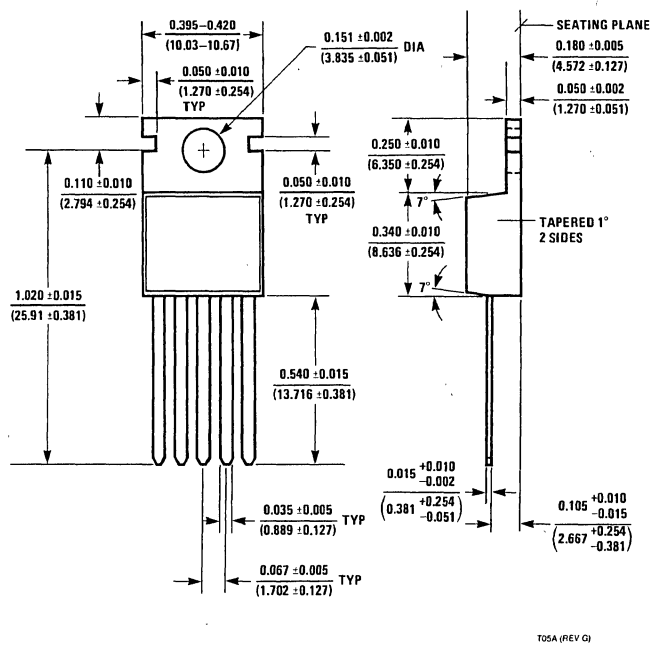

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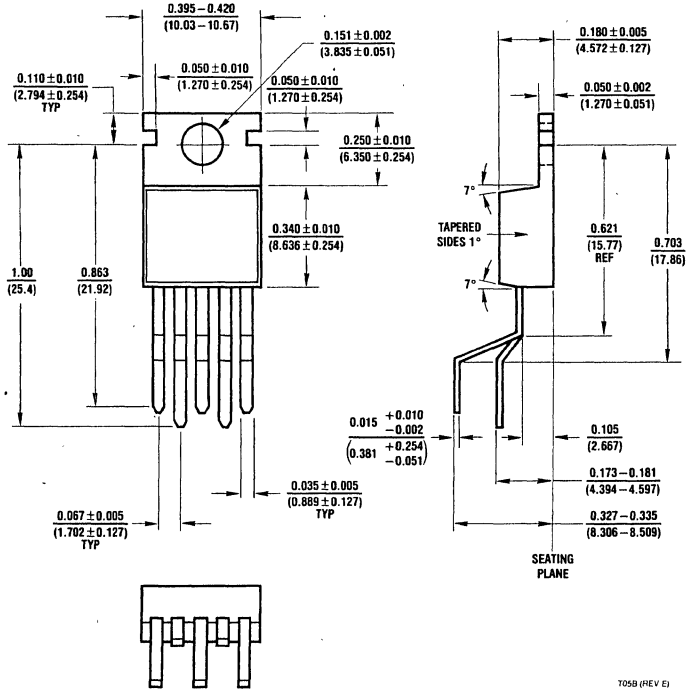

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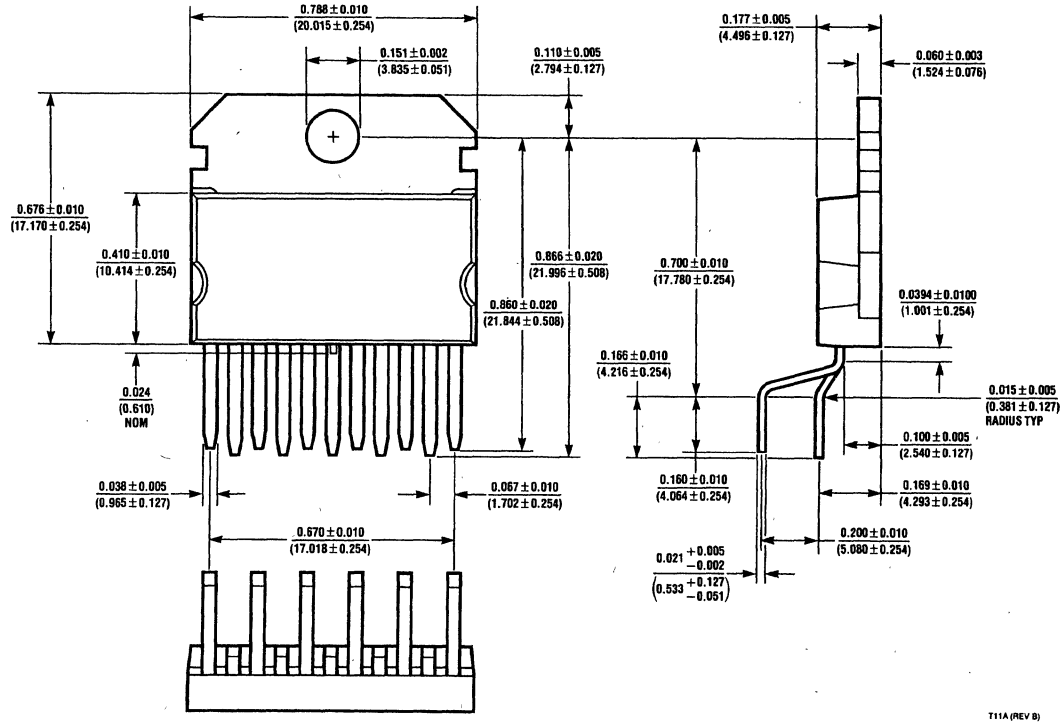

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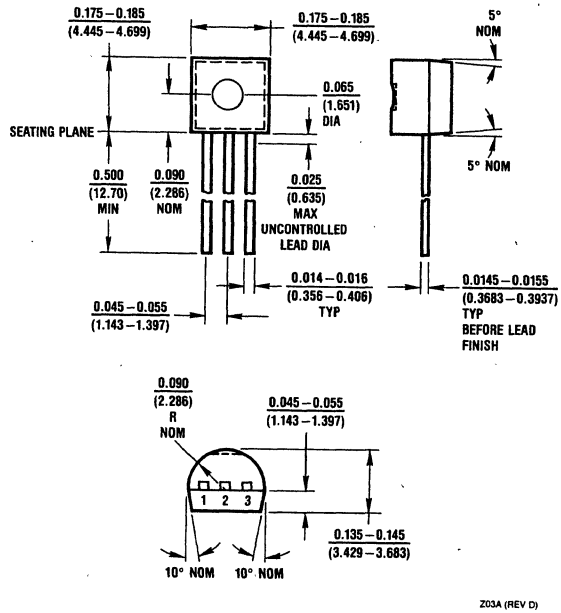

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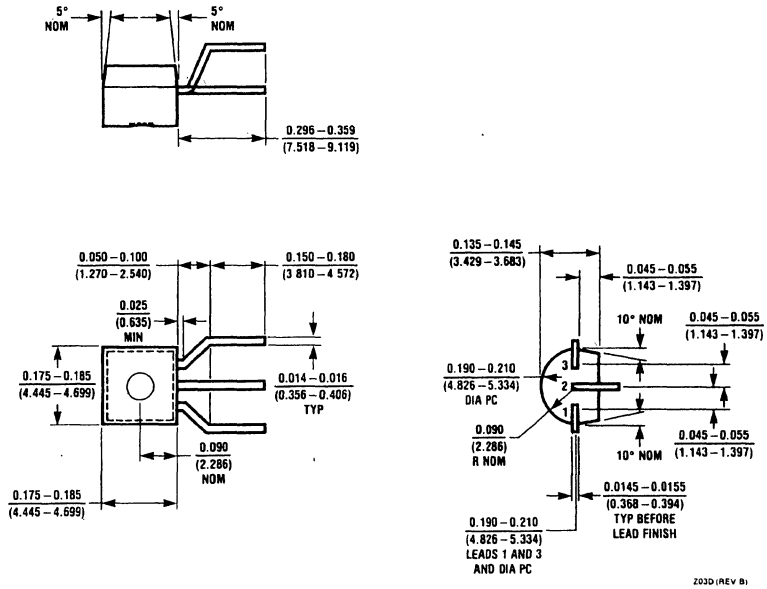

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