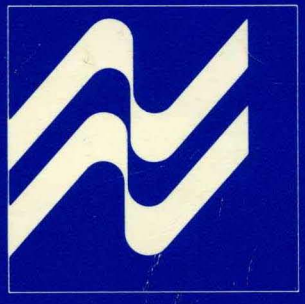
MM54HC/74HC HIGH SPEED microCMOS™ LOGIC FAMILY DATABOOK

NATIONAL SEMICONDUCTOR CORPORATION



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MM54HC/74HC HIGH-SPEED CMOS FAMILY DATABOOK

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Introduction

This comprehensive databook provides information on National Semiconductor's MM54HC/MM74HC high speed CMOS family of SSI/MSI/LSI logic components. The family utilizes microCMOS™ Technology* to achieve the input and power supply characteristics of CD4000B CMOS with the high speed and large output drive of 54LS/74LS logic. This combination enables the construction of very high thru-put low power systems.

The MM54HC/MM74HC family has the same pin-out as equivalent 54LS/74LS functions, in addition, many popular CD4000 series logic functions are offered where no equivalent TTL function exists. Also, this high speed logic family incorporates a growing number of new functions not previously implemented in either a CMOS or TTL logic family.

The MM54HCT/MM74HCT are a subfamily of MM54HC/MM74HC offering TTL compatible inputs. These MM54HCT/MM74HCT devices offer convenient TTL level translation to CMOS for those interface points where only TTL levels are provided, i.e. NMOS microprocessor bus, 54S/74S, 54ALS/74ALS, etc.

The broad line of MM54HC/MM74HC functions greatly simplifies the task of designing complete high speed systems in CMOS.

*** National's microCMOS™ Technology consists of N & P well, oxide-isolated processes with 1, 2 or 3 layers of metal and 1, 2 or 3 layers of polysilicon using either 2, 2.5, 3 or 3.5 micron features—leading to 1 micron and sub-micron in the future.**

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MM54HC113/MM74HC113 Dual J-K Flip-Flop with Preset 4-79
MM54HC173/MM74HC173 Tri-State D Quad Flip-Flop 4-139
MM54HC174/MM74HC174 Hex D Flip-Flop with Clear 4-143
MM54HC175/MM74HC175 Quad D Flip-Flop with Clear 4-146
MM54HC273/MM74HC273 Octal D Flip-Flop with Clear 4-224
MM54HC374/MM74HC374 Octal Tri-State D Flip-Flop 4-266
MM54HCT374/MM74HCT374 Octal Tri-State D Flip-Flop (TTL Input) 5-35
MM54HC534/MM74HC534 Octal Tri-State D Flip-Flop with Inverting Outputs 4-282
MM54HC564/MM74HC564 Octal Tri-State D Flip-Flop with Inverting Outputs 4-291
MM54HC574/MM74HC574 Octal Tri-State D Flip-Flop 4-297

Latches

MM54HC75/MM74HC75 4-Bit Bistable Latch with Q and Q 4-54
MM54HC259/MM74HC259 8-Bit Addressable Latch 4-217
MM54HC373/MM74HC373 Octal Tri-State D Latch 4-263
MM54HCT373/MM74HCT373 Octal Tri-State D Latch (TTL Input) 5-35
MM54HC533/MM74HC533 Octal Tri-State D Latch with Inverting Outputs 4-279
MM54HC563/MM74HC563 Octal Tri-State D Latch with Inverting Outputs 4-288
MM54HC573/MM74HC573 Octal Tri-State D Latch 4-294

Counters

MM54HC160/MM74HC160 4-Bit Synchronous Decade Counter 4-127
MM54HC161/MM74HC161 4-Bit Synchronous Binary Counter 4-127
MM54HC162/MM74HC162 4-Bit Synchronous Decade Counter 4-127
MM54HC163/MM74HC163 4-Bit Synchronous Binary Counter 4-127
MM54HC190/MM74HC190 4-Bit Synchronous Decade Up/Down Counter 4-161
MM54HC191/MM74HC191 4-Bit Synchronous Binary Up/Down Counter 4-161
MM54HC192/MM74HC192 4-Bit Synchronous Decade Up/Down Counter 4-167
MM54HC193/MM74HC193 4-Bit Synchronous Binary Up/Down Counter 4-167
MM54HC292/MM74HC292 31-Bit Programmable Frequency Divider 4-234
MM54HC294/MM74HC294 15-Bit Programmable Frequency Divider 4-234
MM54HC390/MM74HC390 Dual 4-Bit Decade Counter 4-269
MM54HC393/MM74HC393 Dual 4-Bit Binary Counter 4-269
MM54HC4017/MM74HC4017 Decade Counter Divider with 10 Decoded Outputs 4-348
MM54HC4020/MM74HC4020 14 Stage Binary Counter 4-352
MM54HC4024/MM74HC4024 7 Stage Binary Counter 4-352
MM54HC4040/MM74HC4040 12 Stage Binary Counter 4-352
MM54HC4060/MM74HC4060 14 Stage Binary Counter 4-367

High Speed CMOS Product Guide (Continued)

Shift Registers

MM54HC164/MM74HC164 8-Bit Serial-In Parallel-Out Shift Register 4-132
MM54HC165/MM74HC165 8-Bit Parallel-In Serial-Out Shift Register 4-135
MM54HC194/MM74HC194 4-Bit Bidirectional Shift Register 4-173
MM54HC195/MM74HC195 4-Bit Parallel-In Shift Register 4-177
MM54HC299/MM74HC299 8-Bit Universal Shift Register 4-244
MM54HC589/MM74HC589 8-Bit Tri-State Parallel-In Serial-Out Shift Register with Latches 4-300
MM54HC595/MM74HC595 8-Bit Tri-State Serial-In Parallel-Out Shift Register with Latches 4-305
MM54HC597/MM74HC597 8-Bit Tri-State Serial-In Parallel-Out Shift Register with Latches 4-310

Modems

MM74HC942 300 Baud Modem (+5, −5 Volt Supply) 4-328
MM74HC943 300 Baud Modem (5 Volt Supply) 4-334

High Speed CMOS Product Availability Guide

Device	Function	Production Availability
MM54HC/74HC00	Quad 2-Input NAND Gate	Now
MM54HC/74HC02	Quad 2-Input NOR Gate	Now
MM54HC/74HC03	2-Input NAND Gate (Open Drain)	3Q '83
MM54HC/74HC04	Hex Inverter	Now
MM54HC/74HCU04	Hex Inverter (Unbuffered)	Now
MM54HC/74HC08	Quad 2-Input AND Gate	Now
MM54HC/74HC10	Triple 3-Input NAND Gate	Now
MM54HC/74HC11	Triple 3-Input AND Gate	Now
MM54HC/74HC14	Hex Inverting Schmitt Trigger	Now
MM54HC/74HC20	Dual 4-Input NAND Gate	Now
MM54HC/74HC27	Triple 3-Input NOR Gate	Now
MM54HC/74HC30	8-Input NAND Gate	Now
MM54HC/74HC32	Quad 2-Input OR Gate	Now
MM54HC/74HC42	BCD-to Decimal Decoder	Now
MM54HC/74HC51	Dual 2-Input AND-OR-Inverting Gates	3Q '83
MM54HC/74HC58	Dual AND/OR Gate	3Q '83
MM54HC/74HC73	Dual J-K Flip-Flop w/Clear	Now
MM54HC/74HC74	Dual D Flip-Flop w/Preset & Clear	Now
MM54HC/74HC75	4-Bit Bistable Latch w/Q & Q Output	Now
MM54HC/74HC76	Dual J-K Flip-Flop w/Preset & Clear	Now
MM54HC/74HC85	4-Bit Magnitude Comparator	Now
MM54HC/74HC86	Quad 2-Input Exclusive OR (XOR) Gate	Now
MM54HC/74HC107	Dual J-K Flip-Flop w/Clear	Now
MM54HC/74HC109	Dual J-K Flip-Flop w/Preset & Clear	Now
MM54HC/74HC112	Dual J-K Flip-Flop w/Preset & Clear	Now
MM54HC/74HC113	Dual J-K Flip-Flops w/Preset	Now
MM54HC/74HC123	Dual Retrigger Monostable Multivibrator	Now
MM54HC/74HC125	Quad TRI-STATE Buffer (Low Enable)	Now
MM54HC/74HC126	Quad TRI-STATE Buffer (High Enable)	Now
MM54HC/74HC132	Quad 2-Input NAND Schmitt Trigger	Now
MM54HC/74HC133	13-Input NAND Gate	Now
MM54HC/74HC137	1 to 8 w/Latch Decoder (Inverting Output)	3Q '83
MM54HC/74HC138	3–8 Line Decoder	Now
MM54HC/74HC139	Dual 2-to-4 Line Decoder	Now
MM54HC/74HC147	10-to-4 Line Priority Encoder	Now
MM54HC/74HC149	8-Line to 8-Line Priority Encoder	4Q '83
MM54HC/74HC151	8-Channel Digital Multiplexer	Now
MM54HC/74HC153	Dual 4-Input Multiplexer	Now
MM54HC/74HC154	4–16 Line Decoder	Now
MM54HC/74HC157	Quad 2-Input Multiplexer	Now
MM54HC/74HC158	Quad 2-Input Multiplexer (Inverting Output)	Now
MM54HC/74HC160	Synchronous Decade Counter	Now
MM54HC/74HC161	Synchronous Binary Counter	Now
MM54HC/74HC162	Synchronous Decade Counter	Now
MM54HC/74HC163	Synchronous Binary Counter	Now
MM54HC/74HC164	8-Bit Serial-in/ Parallel-out Shift Register	Now
MM54HC/74HC165	8-Bit Parallel-in/ Serial-out Shift Register	Now
MM54HC/74HC173	TRI-STATE Quad D Flip-Flop	4Q '83

High Speed CMOS Product Availability Guide (Continued)

Device	Function	Production Availability
MM54HC/74HC174	Hex D Flip-Flop w/Clear	Now
MM54HC/74HC175	Quad D Type Flip-Flop w/Clear	Now
MM54HC/74HC181	4-Bit Arithmetic Logic Unit	3Q '83
MM54HC/74HC182	Carry Look Ahead Generator	3Q '83
MM54HC/74HC190	Up/Down Decade Counter	4Q '83
MM54HC/74HC191	Up/Down Binary Counter	4Q '83
MM54HC/74HC192	Synchronous Decade Up/Down Counter	Now
MM54HC/74HC193	Synchronous Binary Up/Down Counter	Now
MM54HC/74HC194	4-Bit Bidirectional Universal Shift Register	Now
MM54HC/74HC195	4-Bit Parallel Shift Register	Now
MM54HC/74HC221	Dual Monostable Multivibrator	Now
MM54HC/74HC237	3-to-8 Line Decoder with Address Latches	3Q '83
MM54HC/74HC240	Inverting Octal TRI-STATE Buffer	Now
MM54HC/74HC241	Octal TRI-STATE Buffer (TTL Buffer)	Now
MM54HC/74HC242	Inverting Quad TRI-STATE Transceiver	Now
MM54HC/74HC243	Quad TRI-STATE Transceiver	Now
MM54HC/74HC244	Octal TRI-STATE Buffer	Now
MM54HC/74HC245	Octal TRI-STATE Transceiver	Now
MM54HC/74HC251	8-Channel TRI-STATE Multiplexer	Now
MM54HC/74HC253	Dual 4-Channel TRI-STATE Multiplexer	Now
MM54HC/74HC257	Quad 2-Channel TRI-STATE Multiplexer	Now
MM54HC/74HC259	8-Bit Addressable Latch 3-to-8 Line Decoder	Now
MM54HC/74HC266	Quad 2-Input Exclusive-NOR (XNOR) Gate	Now
MM54HC/74HC273	Octal D Flip-Flop	Now
MM54HC/74HC280	9-Bit Odd/Even Parity Generator/Checker	Now
MM54HC/74HC283	4-Bit Binary Full Adder	4Q '83
MM54HC/74HC292	Programmable 31/15 Bit Dividers/Timers	3Q '83
MM54HC/74HC294	Programmable 31/15 Bit Dividers/Timers	3Q '83
MM54HC/74HC298	Quad 2-Channel w/Storage Multiplexer	4Q '83
MM54HC/74HC299	8-Bit TRI-STATE Universal Shift Register	Now
MM54HC/74HC354	8-Channel TRI-STATE Latched Multiplexer	Now
MM54HC/74HC356	8-Channel TRI-STATE Latched Multiplexer	Now
MM54HC/74HC365	Hex TRI-STATE Buffer	Now
MM54HC/74HC366	Inverting Hex TRI-STATE Buffer	Now
MM54HC/74HC367	Hex TRI-STATE Buffer	Now
MM54HC/74HC368	Inverting Hex TRI-STATE Buffer	Now
MM54HC/74HC373	TRI-STATE Octal D Type Latch	Now
MM54HC/74HC374	TRI-STATE Octal D Type Flip-Flop	Now
MM54HC/74HC390	Dual 4-Bit Decade Counter	Now
MM54HC/74HC393	Dual 4-Bit Binary Counter	Now
MM54HC/74HC423	Dual Non-Retriggerable 1-Shot Multivibrator	Now
MM54HC/74HC533	TRI-STATE Octal D Type Latch w/Inverting Output	Now
MM54HC/74HC534	TRI-STATE Octal D Type Flip-Flop	Now
MM54HC/74HC540	Octal TRI-STATE Driver/Buffer	3Q '83
MM54HC/74HC541	Octal TRI-STATE Driver/Buffer	3Q '83

High Speed CMOS Product Availability Guide (Continued)

Device	Function	Production Availability
MM54HC/74HC563	TRI-STATE Octal D (Type Latch (Inverting Output)	Now
MM54HC/74HC564	TRI-STATE Octal D Type Flip-Flop w/Inverting Output	Now
MM54HC/74HC573	TRI-STATE Octal D Type Latch	Now
MM54HC/74HC574	TRI-STATE Octal D Type Flip-Flop	Now
MM54HC/74HC589	8-Bit Parallel-to-Serial Shift Register	4Q '83
MM54HC/74HC595	8-Bit Parallel-to-Serial Shift Register	3Q '83
MM54HC/74HC597	8-Bit Parallel-to-Serial Shift Register	4Q '83
MM54HC/74HC640	Inverting Octal TRI-STATE Transceiver	Now
MM54HC/74HC643	Octal TRI-STATE Transceiver	Now
MM54HC/74HC646	Non-Inverting Octal Bus Transceiver/ Register	3Q '83
MM54HC/74HC648	Inverting Octal Bus Transceiver/Register	3Q '83
MM54HC/74HC688	8-Bit Magnitude Comparator (Equality Detector)	Now
MM74HC942	300 Baud Modem	Now
MM74HC943	300 Baud Modem	Now
MM54HC/74HC4002	Dual 4-Input NOR Gate	Now
MM54HC/74HC4016	Quad Bilateral Analog Switch	4Q '83
MM54HC/74HC4017	Decade Counter/ Divider w/10 Decoded Outputs	3Q '83
MM54HC/74HC4020	14-Stage Binary Counter	Now
MM54HC/74HC4024	7-Stage Ripple Counter	3Q '83
MM54HC/74HC4040	12-Stage Binary Counter	Now
MM54HC/74HC4046	Phase-Locked Loop	4Q '83
MM54HC/74HC4049	Hex Inverting Logic Level Down Converter	Now
MM54HC/74HC4050	Hex Logic Level Down Converter	Now
MM54HC/74HC4051	Single 8-Channel w/Storage Multiplexer	4Q '83
MM54HC/74HC4052	Dual 4-Channel w/Storage Multiplexer	4Q '83
MM54HC/74HC4053	Triple 2-Channel w/Storage Multiplexer	4Q '83
MM54HC/74HC4060	14-Stage Binary Counter	Now
MM54HC/74HC4066	Quad Bilateral Analog Switch	4Q '83
MM54HC/74HC4075	Triple 3-Input OR Gate	Now
MM54HC/74HC4078	8-Input NOR Gate	Now
MM54HC/74HC4316	Quad Bilateral Analog Switch	4Q '83
MM54HC/74HC4351	8-Channel Analog Multiplexer Demultiplexer w/Latch	4Q '83
MM54HC/74HC4352	Dual 4-Channel Multiplexer Demultiplexer w/Latch	4Q '83
MM54HC/74HC4353	Triple 2-Channel Multiplexer Demultiplexer w/Latch	4Q '83
MM54HC/74HC4511	BCD-to-7 Segment Latch/Decoder Driver	TBA
MM54HC/74HC4538	Dual Retriggerable Monostable Multivibrator	Now
MM54HC/74HC4543	BCD-to-7 Segment Latch/Decoder for Liquid Crystal Display	Now
MM54HC/74HC4560	NBCD Adder	4Q '83
MM54HCT/74HCT00	Quad 2-Input NAND Gate (TTL Input)	3Q '83
MM54HCT/74HCT04	Hex Inverter (TTL Input)	3Q '83
MM54HCT/74HCT05	Hex Inverter Open Collector (TTL Input)	3Q '83
MM54HCT/74HCT34	Hex Buffer (TTL Input)	3Q '83
MM54HCT/74HCT74	Dual D Flip-Flop w/Preset & Clear (TTL Input)	4Q '83
MM54HCT/74HCT109	Dual J-K Flip-Flop w/Preset & Clear (TTL Input)	4Q '83
MM54HCT/74HCT138	1 of 8 Decoder (TTL Input)	3Q '83

High Speed CMOS Product Availability Guide (Continued)

Device	Function	Production Availability
MM54HCT/74HCT139	Dual 2-to-4 Line Decoder (TTL Input)	4Q '83
MM54HCT/74HCT149	8-Line to 8-Line Priority Encoder (TTL Input)	4Q '83
MM54HCT/74HCT240	Inverting Octal TRI-STATE Buffer (TTL Input)	Now
MM54HCT/74HCT241	Octal Buffer TRI-STATE (TTL Input)	Now
MM54HCT/74HCT244	Inverting Octal TRI-STATE Buffer (TTL Input)	Now
MM54HCT/74HCT245	Octal Transceiver TRI-STATE (TTL Input)	Now
MM54HCT/74HCT373	Octal D Type TRI-STATE Latch (TTL Input)	3Q '83
MM54HCT/74HCT374	Octal D Type TRI-STATE Flip-Flop (TTL Input)	3Q '83
MM54HCT/74HCT640	Inverting Octal TRI-STATE Transceiver (TTL Input)	Now
MM54HCT/74HCT643	Octal TRI-STATE Transceiver (TTL Input)	Now
MM54HCT/74HCT688	8-Bit Magnitude Comparator (TTL Input)	4Q '83

Section 1

AC Switching Waveforms and Test Circuits

AC Parameter Definitions

f_{MAX} Operating frequency. This is the fastest speed that a circuit can be toggled.

t_{PHL} Propagation delay from input to output going low.

t_{PLH} Propagation delay from input to output going high.

t_{PZH} Enable propagation delay time. This is measured from the input to the output going to an active high level from TRI-STATE®.

t_{PZL} Enable propagation delay time. This is measured from the input to the output going to an active low level from TRI-STATE.

t_{PHZ} Disable propagation delay time to the output going from an active high level to TRI-STATE.

t_{PLZ} Disable propagation delay time to the output going from an active low level to TRI-STATE.

t_W Input signal pulse width.

t_S Input setup time. This is the time that data must be present prior to clocking input transitioning.

t_H Input hold time. This is the time that data must remain after clocking input has transitioned.

t_{REM} Clock removal time. This is the time that an active clear or enable signal must be removed before the clock input transitions.

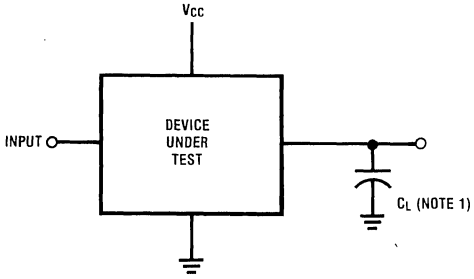
t_r Input signal rise time.

t_f Input signal fall time.

t_{TLH} Output Rise time (transition time low to high)

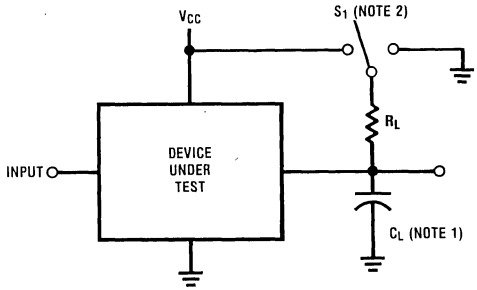
t_{THL} Output Fall time (transition time high to low)

MM54HC/MM74HC AC Switching Test Circuits and Timing Waveforms



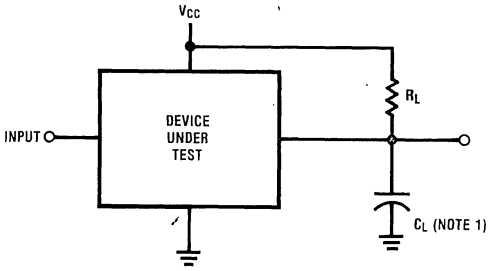
TL/F/5376–1

Test Circuit for Push Pull Outputs



TL/F/5376–2

Test Circuit for TRI-STATE Output Tests

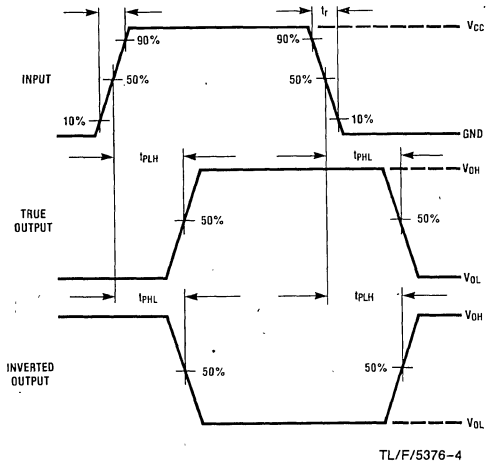


TL/F/5376–3

Test Circuit for Open Drain Outputs

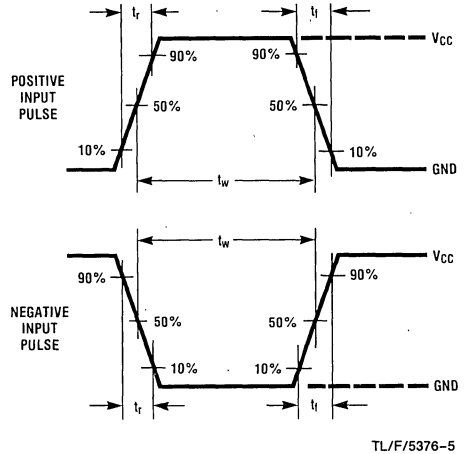
Note 1: C_L includes load and test jig capacitance.

Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = Gnd for t_{PZH}, and t_{PHZ} measurements.



TL/F/5376–4

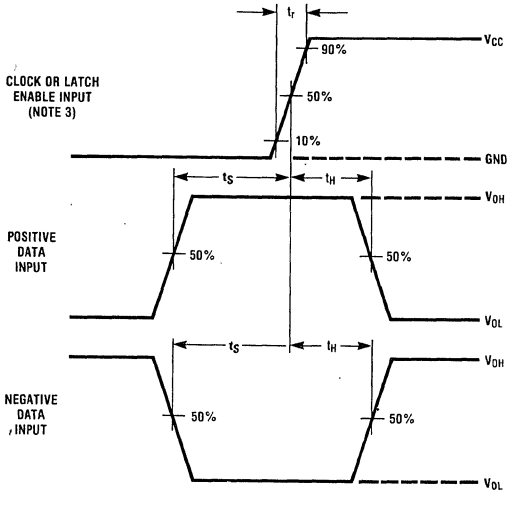
Propagation Delay Waveforms



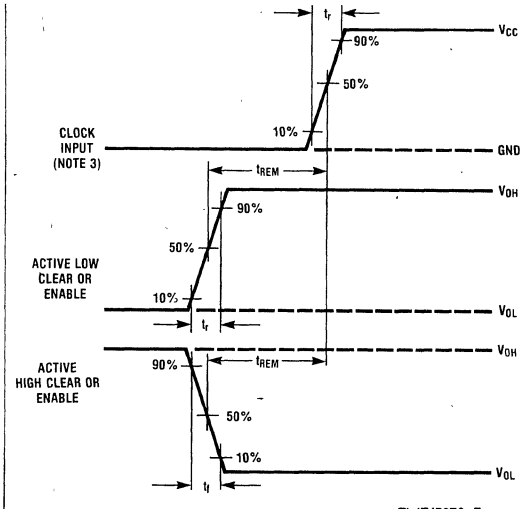
TL/F/5376–5

Input Pulse Width Waveforms

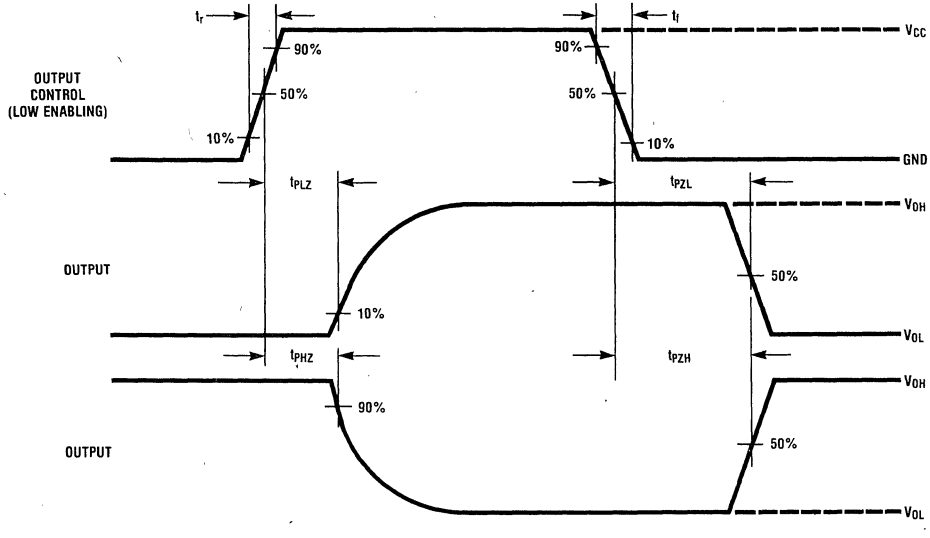
MM54HC/MM74HC AC Switching Test Circuits and Timing Waveforms (Continued)



Setup and Hold Time Waveforms



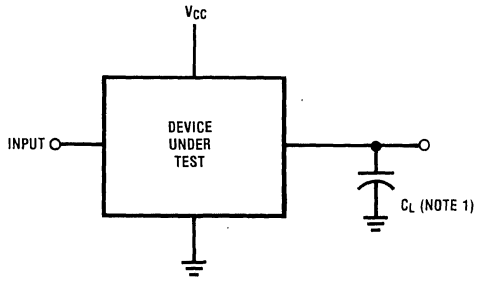
Removal Time Waveforms



TRI-STATE Output Enable and Disable Waveforms

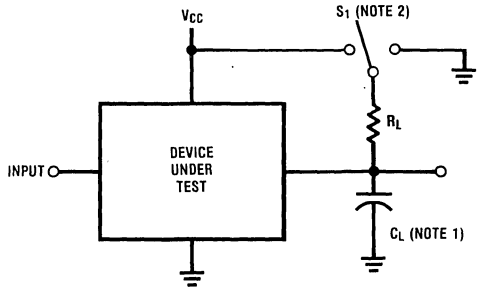
Note 3: Waveform for negative edge sensitive circuits will be inverted

MM54HCT/MM74HCT AC Switching Test Circuits and Timing Waveforms



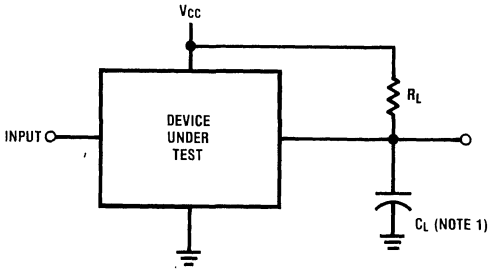
TL/F/5376–1

Test Circuit for Push Pull Outputs



TL/F/5376–2

Test Circuit for TRI-STATE Output Tests

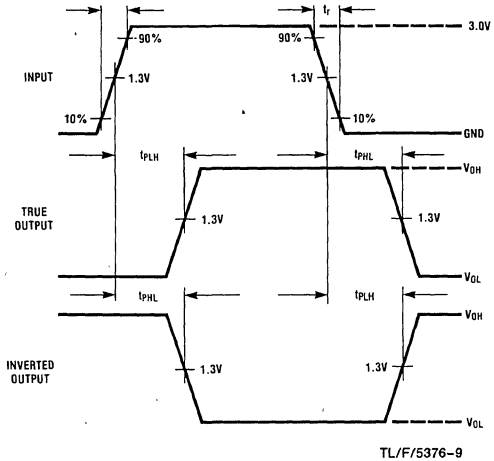


TL/F/5376–3

Test Circuit for Open Drain Outputs

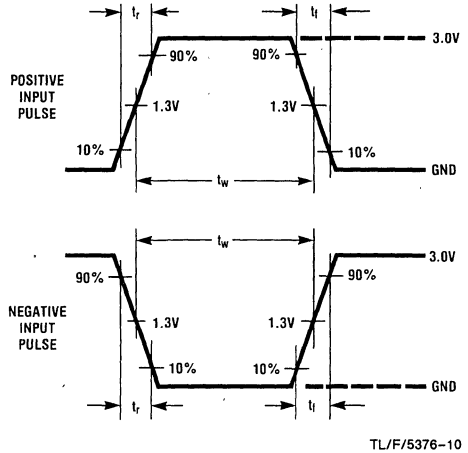
Note 1: C_L includes load and test jig capacitance.

Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = Gnd for t_{PZH}, and t_{PHZ} measurements.



TL/F/5376–9

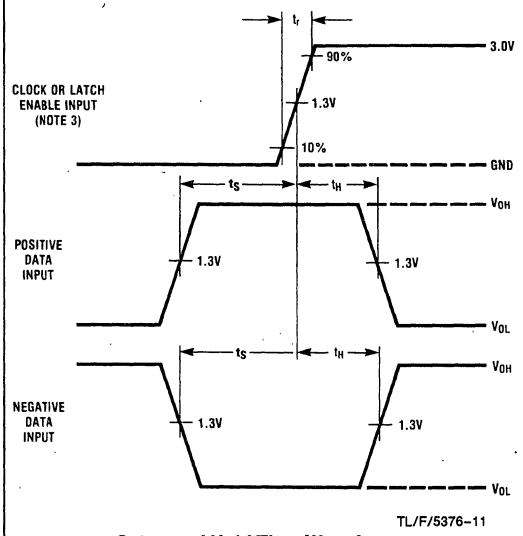
Propagation Delay Waveforms



TL/F/5376–10

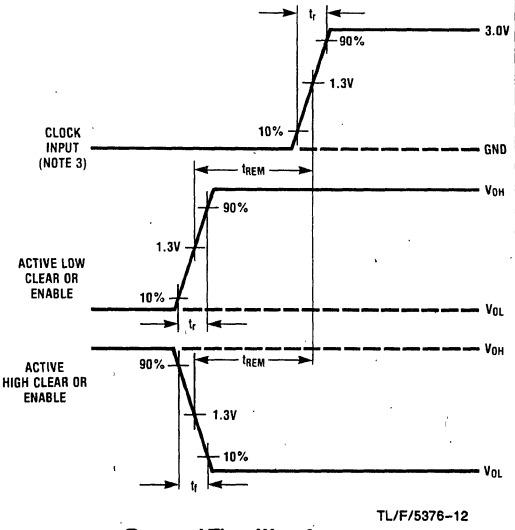
Input Pulse Width Waveforms

MM54HCT/MM74HCT AC Switching Test Circuits and Timing Waveforms (Continued)



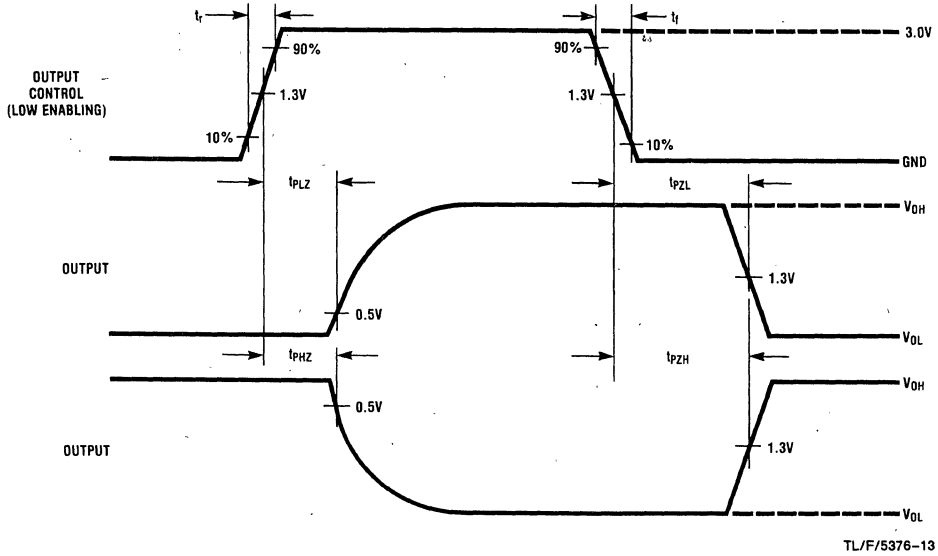
TL/F/5376–11

Setup and Hold Time Waveforms



TL/F/5376–12

Removal Time Waveforms



TL/F/5376–13

TRI-STATE Output Enable and Disable Waveforms

Note 3: Waveform for negative edge sensitive circuits will be inverted

Section 2

Application Notes

HC-CMOS Power Dissipation

National Semiconductor
Application Note 303
Kenneth Karakotsios
June 1983

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, high-speed CMOS draws five to seven orders of magnitude less power than the equivalent LSTTL function. When switching, the amount of power dissipated by both metal gate and high-speed silicon gate CMOS is directly proportional to the operating frequency of the device. This is because the higher the operating frequency, the more often the device is being switched. Since each transition requires power, power consumption increases with frequency.

First, one will find a description of the causes of power consumption in HC-CMOS and LSTTL applications. Next will follow a comparison of MM54HC/MM74HC to LSTTL power dissipation. Finally, the maximum ratings for power dissipation imposed by the device package will be discussed.

Quiescent Power Consumption

Ideally, when a CMOS integrated circuit is not switching, there should be no DC current paths from V_{CC} to ground, and the device should not draw any supply current at all. However, due to the inherent nature of semiconductors, a small amount of leakage current flows across all reverse-biased diode junctions on the integrated circuit. These leakages are caused by thermally-generated charge carriers in the diode area. As the temperature of the diode increases, so do the number of these unwanted charge carriers, hence leakage current increases.

Leakage current is specified for all CMOS devices as I_{CC}. This is the DC current that flows from V_{CC} to ground when all inputs are held at either V_{CC} or ground, and all outputs are open. This is known as the quiescent state.

For the MM54HC/MM74HC family, I_{CC} is specified at ambient temperatures (T_A) of 25°C, 85°C, and 125°C. There are three different specifications at each temperature, depending on the complexity of the device. The number of diode junctions grows with circuit complexity, thereby increasing the leakage current. The worst case I_{CC} specifications for the MM54HC/MM74HC family are summarized in Table 1. In addition, it should be noted that the maximum I_{CC} current will decrease as the temperature goes below 25°C.

TABLE 1. Supply Current (I_{CC}) for MM54HC/MM74HC Specified at $V_{CC}=6V$

T_A	Gate	Buffer	MSI	Unit
25°C	2.0	4.0	8.0	μA
85°C	20	40	80	μA
125°C	40	80	160	μA

To obtain the quiescent power consumption for any CMOS device, simply multiply I_{CC} by the supply voltage:

$$P_{DC}=I_{CC}V_{CC}$$

Sample calculations show that at room temperature the maximum power dissipation of gate, buffer, and MSI circuits at $V_{CC}=6V$ are 10 μW, 20 μW, and 40 μW, respectively.

Dynamic Power Consumption

Dynamic power consumption is basically the result of charging and discharging capacitances. It can be broken down into three fundamental components, which are:

1. Load capacitance transient dissipation
2. Internal capacitance transient dissipation
3. Current spiking during switching.

Load Capacitance Transient Dissipation

The first contributor to power consumption is the charging and discharging of external load capacitances. *Figure 1* is a schematic diagram of a simple CMOS inverter driving a capacitive load. A simple expression for power dissipation as a function of load capacitance can be derived starting with:

$$Q_L=C_LV_{CC}$$

where C_L is the load capacitance, and Q_L is the charge on the capacitor. If both sides of the equation are divided by the time required to charge and discharge the capacitor (one period, T, of the input signal), we obtain:

$$\frac{Q_L}{T}=C_LV_{CC}\left(\frac{1}{T}\right)$$

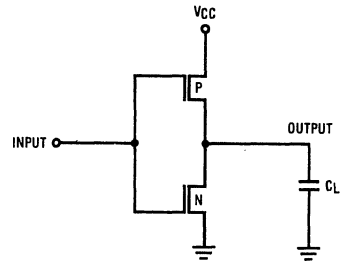


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FIGURE 1. Simple CMOS Inverter Driving a Capacitive External Load

Since charge per unit time is current ($Q_L/T=I$) and the inverse of the period of a waveform is frequency ($1/T=f$):

$$I_L=C_LV_{CC}f$$

To find the power dissipation, both sides of the equation must be multiplied by the supply voltage ($P=VI$), yielding:

$$P_L=C_L\,V_{CC}{}^2f$$

One note of caution is in order. If all the outputs of a device are not switching at the same frequency, then the power consumption must be calculated at the proper frequency for each output:

$$P_L = V_{CC}^2(C_{L1}f_1 + C_{L2}f_2 + \ldots + C_{Ln}f_n)$$

Examples of devices for which this may apply are: counters, dual flip-flops with independent clocks, and other integrated circuits containing dual, triple, etc., independent circuits.

Internal Capacitance Transient Dissipation

Internal capacitance transient dissipation is similar to load capacitance dissipation, except that the internal parasitic "on-chip" capacitance is being charged and discharged. *Figure 2* is a diagram of the parasitic nodal capacitances associated with two CMOS inverters.

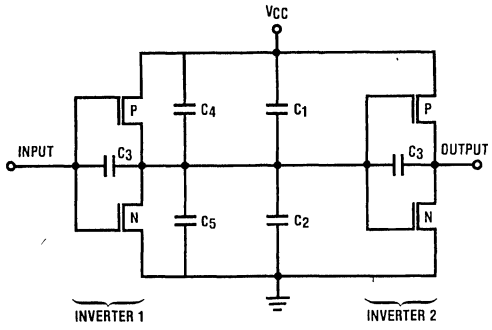

FIGURE 2. Parasitic Internal Capacitances Associated with Two Inverters

C_1 and C_2 are capacitances associated with the overlap of the gate area and the source and channel regions of the P- and N-channel transistors, respectively. C_3 is due to the overlap of the gate and source (output), and is known as the Miller capacitance. C_4 and C_5 are capacitances of the parasitic diodes from the output to V_{CC} and ground, respectively. Thus the total internal capacitance seen by inverter 1 driving inverter 2 is:

$$C_I = C_1 + C_2 + 2C_3 + C_4 + C_5$$

Since an internal capacitance may be treated identically to an external load capacitor for power consumption calculations, the same equation may be used:

$$P_I = C_I V_{CC}^2 f$$

At this point, it may be assumed that different parts of the internal circuitry are operating at different frequencies. Although this is true, each part of the circuit has a fixed frequency relationship between it and the rest of the device. Thus, one value of an effective C_I can be used to compute the internal power dissipation at any frequency. More will be said about this shortly.

Current Spiking During Switching

The final contributor to power consumption is current spiking during switching. While the input to a gate is making a transition between logic levels, both the P- and N-channel transistors are turned partially on. This creates a low impedance path for supply current to flow from V_{CC} to ground, as illustrated in *Figure 3*.

For fast input rise and fall times (shorter than 50 ns for the MM54HC/MM74HC family), the resulting power consumption is frequency dependent. This is due to the fact that the more often a device is switched, the more often the input is situated between logic levels, causing both transistors to be partially turned on. Since this power consumption is proportional to input frequency and specific to a given device in any application, as is C_I, it can be combined with C_I. The resulting term is called "C_{PD}," the no-load power dissipation capacitance. It is specified for every MM54HC/MM74HC device in the AC Electrical Characteristic section of each data sheet.

It should be noted that as input rise and fall times become longer, the switching current power dissipation becomes more dependent on the amount of time that both the P- and N-channel transistors are turned on, and less related to C_{PD} as specified in the data sheets. *Figure 4* is a representation of the effective value of C_{PD} as input rise and fall times increase for the MM54HC/MM74HC08, MM54HC/MM74HC139, and MM54HC/MM74HC390. To get a fair comparison between the three curves, each is divided by the value of C_{PD} for the particular device with fast input rise and fall times. This is represented by "C_{PD0}," the value of C_{PD} specified in the data sheets for each part. This comparison appears in *Figure 5*. C_{PD} remains constant for input rise and fall times up to about 20 ns, after which it rises, approaching a linear slope of 1. The graphs do not all reach a slope of 1 at the same time because of necessary differences in circuit design for each part. The MM54HC/MM74HC08 exhibits the greatest change in C_{PD}, while the MM54HC/MM74HC139 shows less of an increase in C_{PD} at any

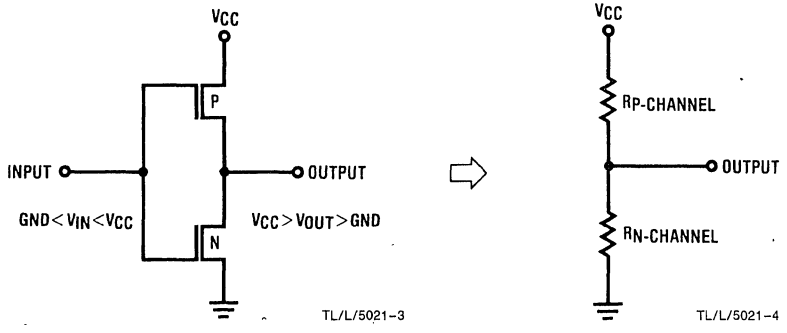

FIGURE 3. Equivalent schematic of a CMOS inverter whose input is between logic levels

given frequency. Thus, the power dissipation for most of the parts in the MM54HC/MM74HC family will fall within these two curves. One notable exception is the MM54HC/MM74HCU04.

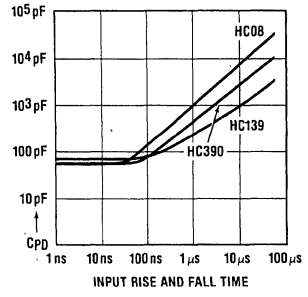

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FIGURE 4. Comparison of Typical C_{PD} for MM54HC/MM74HC08, MM54HC/MM74HC139 MM54HC/MM74HC390 as a Function of Input Rise and Fall Time. $t_{rise} = t_{fall}$, $V_{CC} = 5V$, $T_A = 25°C$

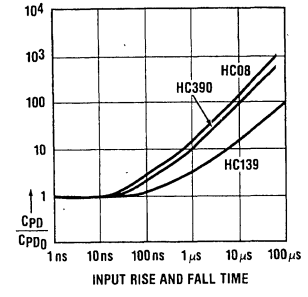

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FIGURE 5. Normalized Effective C_{PD} (Typical) for Slow Input Rise and Fall Times. $t_{rise} = t_{fall}$, $V_{CC} = 5V$, $T_A = 25°C$

Inputs that do not pull all the way to V_{CC} or ground can also cause an increase in power consumption, for the same reason given for slow rise and fall times. If the input voltage is between the minimum input high voltage and V_{CC}, then the input N-channel transistor will have a low impedance (i.e., be "turned on") as expected, but the P-channel transistor will not be completely turned off. Similarly, if the input is between ground and the maximum input low voltage, the P-channel transistor will be fully on and the N-channel transistor will be partially on. In either case, a resistive path from V_{CC} to ground will occur, resulting in an increase in power consumption.

Combining all the derived equations, we arrive at the following:

$$P_{TOTAL} = (C_L + C_{PD})V_{CC}^2 f + I_{CC}V_{CC}$$

This equation can be used to compute the total power consumption of any MM54HC/MM74HC device, as well as any other CMOS device, at any operating frequency. It includes both DC and AC contributions to power usage. C_{PD} and I_{CC} are supplied in each data sheet for the particular device, and V_{CC} and f are determined by the particular application.

Comparing HC-CMOS to LSTTL

Although power consumption is somewhat dependent on frequency in LSTTL devices, the majority of power dissipated below 1 MHz is due to quiescent supply current. LSTTL contains many resistive paths from V_{CC} to ground, and even when it is not switching, it draws several orders of magnitude greater supply current than HC-CMOS. *Figure 6* is a bar graph comparison of quiescent power requirements (V_{CC})×(I_{CC}) between LSTTL and HC-CMOS devices.

The reduction in CMOS power consumption as compared to LSTTL devices is illustrated in *Figures 7* and *8*. These graphs are comparisons of the typical supply current (I_{CC}) required for equivalent functions in MM54HC/MM74HC, MM54HC/MM74C, CD4000, and 54LS/74LS logic families. The currents were measured at room temperature (25°C) with a supply voltage of 5V.

Figure 7 represents the supply current required for a quad NAND gate with one gate in the package switching. The MM54HC/MM74HC family draws slightly more supply current than the 54C/74C and CD4000 series. This is mainly due to the large size of the output buffers necessary to source and sink currents characteristic of the LSTTL family. Other reasons include processing differences and the larger internal circuitry required to drive the output buffers at high frequencies. The frequency at which the CMOS device draws as much power as the LSTTL device, known as the power cross-over-frequency, is about 20 MHz.

In *Figure 8*, which is a comparison of equivalent flip-flops (174) and shift registers (164) from the different logic families, the power cross-over frequency again occurs at about 20 MHz.

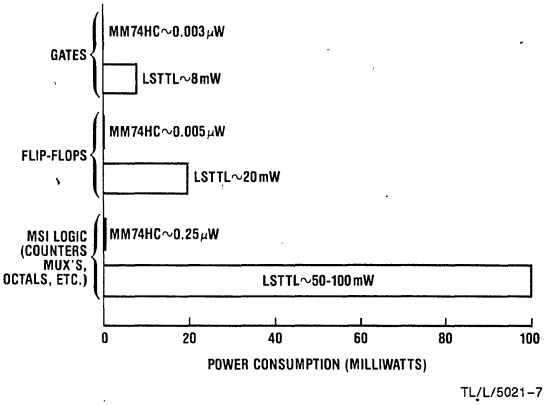

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FIGURE 6. High Speed CMOS (HC-CMOS) vs. LSTTL Quiescent Power Consumption

The power cross-over frequency increases as circuit complexity increases. There are two major reasons for this. First, having more devices on an LSTTL integrated circuit means that more resistive paths between V_{CC} and ground will occur, and more quiescent current will be required. In a CMOS integrated circuit, although the supply leakage current will increase, it is of such a small magnitude (nanoAmps per device) that there will be very little increase in total power consumption.

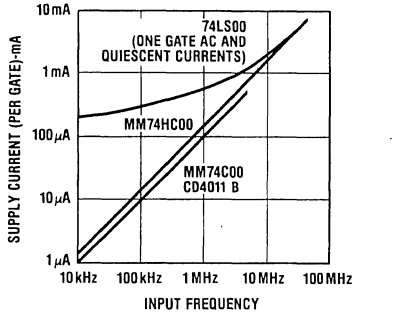

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FIGURE 7. Supply Current vs. Input Frequency for Equivalent NAND Gates

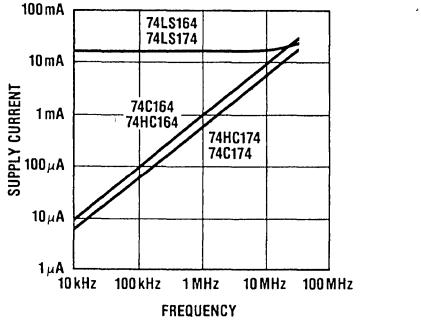

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FIGURE 8. Supply Current vs. Frequency

Secondly, as system complexity increases, the precentage of the total system operating at the maximum frequency tends to decrease. *Figure 9* shows block diagrams of a CMOS and an equivalent LSTTL system. In this abstract system, there is a block of parts operating at the maximum frequency (F_{max}), a block operating at half F_{max}, a block operating at one quarter F_{max}, and so on. Let us call the power consumed in the first section P1. In a CMOS system, since power consumption is directly proportional to the operating frequency, the amount of power consumed by the second block will be (P1)/2, and the amount used in the third section will be (P1)/4. If the power consumed over a large number of blocks is summed up, we obtain:

$$P_{TOTAL} = P1 + (P1)/2 + (P1)/4 + \ldots + (P1)/(2^{n-1})$$

and $P_{TOTAL} \leq 2(P1)$

Now consider the LSTTL system. Again, the power consumed in the first block is P1. The amount of power dissipated in the second block is something less than P1, but greater than (P1)/2. For simplicity, we can assume the best case, that P2 = (P1)/2. The power consumption for all system blocks operating at frequencies $F_{max}/2$ and below will be dominated by quiescent current, which will not change with frequency. The power used by blocks 3 through n will be approximately equal to the power dissipated by block 2, (P1)/2. The total power consumed in the LSTTL system is:

$$P_{TOTAL} = (P1 + (P1)/2 + (P1)/2 + \ldots + (P1)/2$$

$$P_{TOTAL} = P1 + (N-1)(P1)/2$$

and for $n > 2$, $P_{TOTAL} > 2(P1)$

Thus, an LSTTL system will draw more power than an equivalent HC-CMOS system.

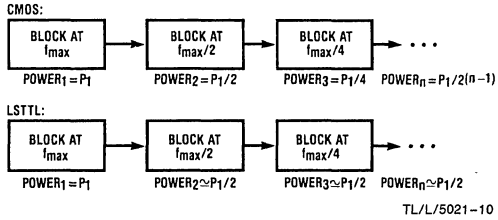

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FIGURE 9. Comparison of Equivalent CMOS and LSTTL Systems

This effect is further illustrated in *Figure 10*. An arbitrary system is composed of 200 gates, 150 counters, and 150 full adders, with 50 pF loads on all of the outputs. The supply voltage is 5V, and the system is at room temperature. For this system, the worst case power consumption for CMOS is about an order of magnitude lower than the typical LSTTL power requirements. Thus, as system complexity increases, CMOS will save more power.

Maximum Power Dissipation Limits

It is important to take into consideration the maximum power dissipation limits imposed on a device by the package when designing with high-speed CMOS. Both the plastic and ceramic packages can dissipate up to 500 mW. Although this limit will rarely be reached in typical high-speed applications, the MM54HC/MM74HC family has such large output current source and sink capabilities that driving a resistive load could possibly take a device to the 500 mW limit. This maximum power dissipation rating should be derated by −12 mW/°C, starting at 65°C for the plastic package and 100°C for the ceramic package. This is illustrated in *Figures 11* and *12*. Thus, if a device in a plastic package is operating at 70°C, then the maximum power dissipation rating would be 500 mW — (70°C—65°C) (12 mW/°C) = 44 mW. Note that the maximum ambient temperature is 85°C for plastic packages and 125°C for ceramic packages.

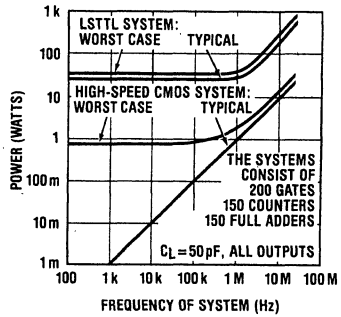

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FIGURE 10. System Power vs. Frequency MMHC74HC vs. LSTTL

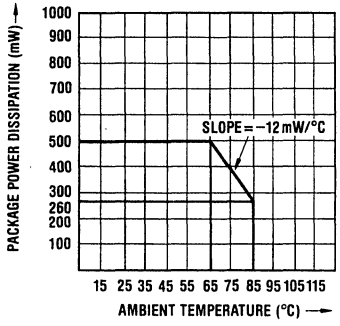

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FIGURE 11. Plastic Package (MM74HC) High Temperature Power Derating for MM54HC/MM74HC Family

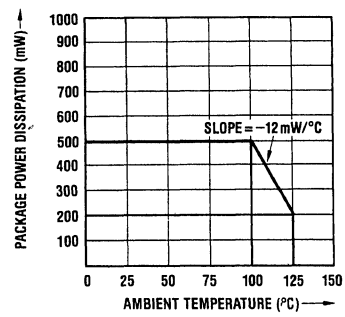

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FIGURE 12. Ceramic Package (MM54HC) High Temperature Power Derating for MM54HC/MM74HC Family

Summary

The MM54HC/MM74HC high-speed silicon gate CMOS family has quiescent (standby) power consumption five to seven orders of magnitude lower than the equivalent LSTTL function. At high frequencies (30 MHz and above), both families consume a similar amount of power for very simple systems. However, as system complexity increases, HC-CMOS uses much less power than LSTTL. To keep power consumption low, input rise and fall times should be fast (less than 50 to 100 ns) and inputs should swing all the way to V_{CC} and ground.

There is an easy-to-use equation to compute the power consumption of any HC-CMOS device in any application:

$$P_{TOTAL} = (C_L + C_{PD})V_{CC}^2 f + I_{CC}V_{CC}$$

The maximum power dissipation rating is 500 mW per package at room temperature, and must be derated as temperature increases.

High-Speed CMOS (MM54HC/MM74HC) Processing

National Semiconductor
Application Note 310
Kenneth Karakotsios
June 1983

The MM54HC/MM74HC logic family achieves its high speed by utilizing microCMOS™ Technology. This is a 3.5 silicon gate P-well CMOS process single layer poly, single layer metal, P-well process with oxide-isolated transistors. Why do silicon-gate transistors (polycrystalline) switch faster than metal-gate transistors? The reason is related both to the parasitic capacitances inherent in integrated circuits and the gain of the transistors. The speed at which an MOS transistor can switch depends on how fast its internal parasitic capacitance, as well as its external load capacitance, can be charged and discharged. Capacitance takes time to be charged and discharged, and hence degrades a transistor's performance. The gain of a transistor is a measure of how well a transistor can charge and discharge a capacitor. Therefore, to increase speed, it is desirable to both decrease parasitic capacitance and increase transistor gain. These advantages are achieved with National's silicon-gate CMOS process. To understand exactly how these improvements occur in silicon-gate CMOS, it is helpful to compare the process to the metal-gate CMOS process.

Metal-Gate CMOS Processing

Figure 1 through *12* are cross sections of a metal-gate CMOS pair of P- and N-channel transistors with associated guard rings. Guard rings are necessary in metal-gate processing to prevent leakage currents between the sources and drains of separate transistors. The starting material is an N− type silicon substrate covered by a thin layer of thermally grown silicon dioxide (SiO_2) (*Figure 1*). Silicon dioxide, also called oxide acts as both a mask for certain processing steps and a dielectric insulator. *Figure 2* shows the addition of a lightly doped P− well in which the N-channel transistors and P+ guard rings will later be located. The P− well is ion implanted into the substrate. A thin layer of oxide allows ions to be implanted through it, while a thicker oxide will block ion implantation.

Next, the oxide over the P− well is stripped, and a new layer of oxide is grown. Following this, holes are etched into the oxide where the P+ source, drain, and guard ring diffusions shall occur. The P+ regions are diffused, and then additional oxide is grown to fill the holes created for diffusion (*Figures 3, 4,* and *5*). The following step is to cut holes in the oxide to diffuse the N-channel sources, drains and guard bands. Then oxide is again thermally grown (*Figures 6* and *7*).

In the following step, the composite mask is created by again cutting holes in the oxide. This defines the areas where contacts and transistor gates will occur (*Figure 8*). A thin layer of gate oxide is grown over these regions (*Figure 9*), and alignment of this to the source and drain regions is a critical step. If the gate oxide overlaps the source or drain, this will cause additional parasitic capacitance.

Contacts to transistor sources and drains are cut into the thin oxide where appropriate (*Figure 10*), and then the interconnect metal is deposited (*Figure 11*). Depositing the metal over the gate areas is also a critical step, for a misalignment will cause extra unwanted overlap capacitance. *Figure 12* illustrates the final step in processing, which is to deposit an insulating layer of silicon dioxide over the entire surface of the integrated circuit.

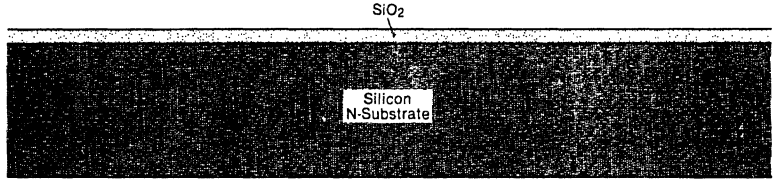

FIGURE 1. Initial Oxidation, Thermally Grown Silicon Dioxide Layer on Silicon Substrate Surface

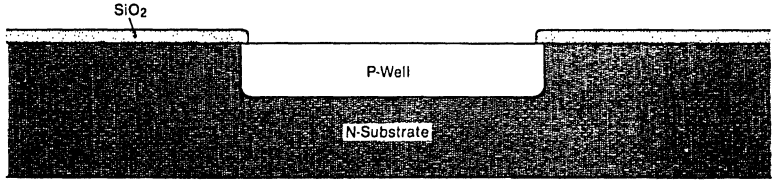

FIGURE 2. P− Mask and Formation of P− Well Tub in Which N-Channel Devices Will Be Located

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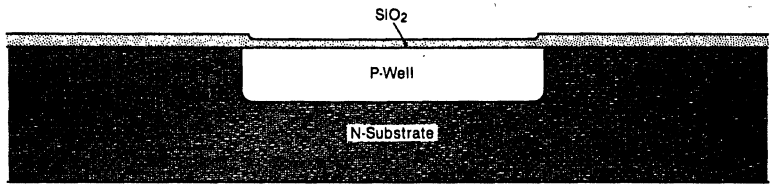

FIGURE 3. P− Well Oxidation, Thermally Grown Silicon Dioxide Layer Over P− Well Area

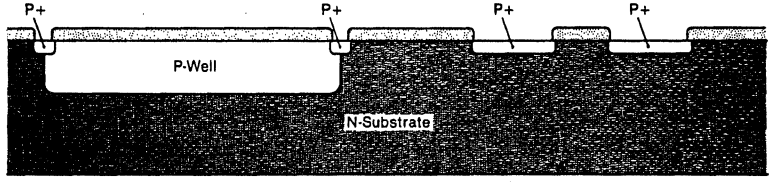

FIGURE 4. P + Mask and Formation of Low Resistance P + Type Pockets in P− Well and N-Substrate

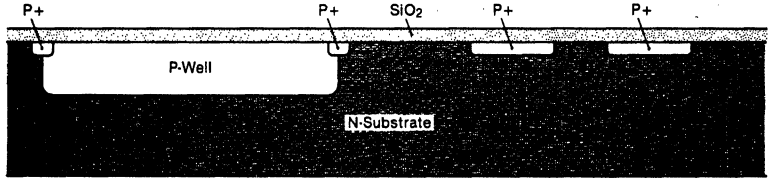

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FIGURE 5. P + Oxidation, Thermally Grown Silicon Dioxide Layer Over P+ Type Pockets

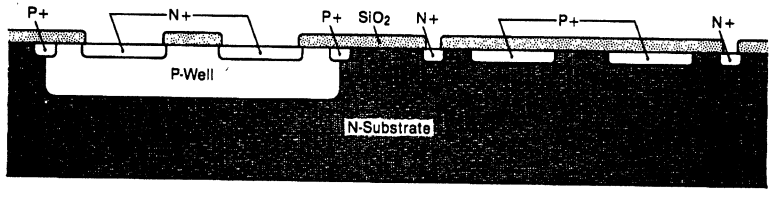

FIGURE 6. N + Mask and Formation of Low Resistance N + Type Pockets in P− Well and N-Substrate

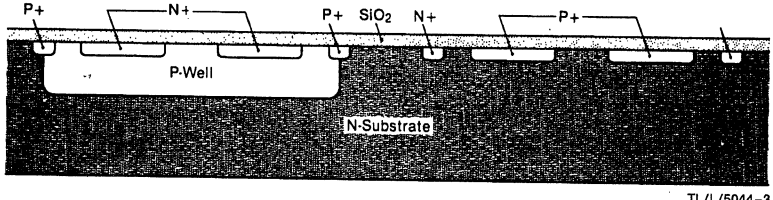

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FIGURE 7. N + Oxidation, Thermally Grown Silicon Dioxide Layer Over N + Type Pockets

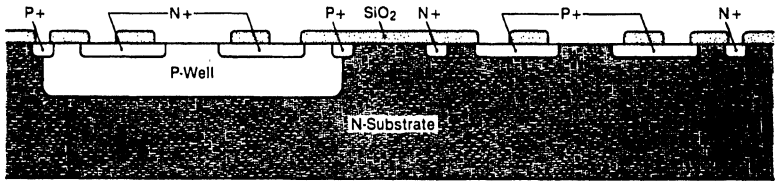

FIGURE 8. Composite Mask and Openings to N- and P-Channel Devices

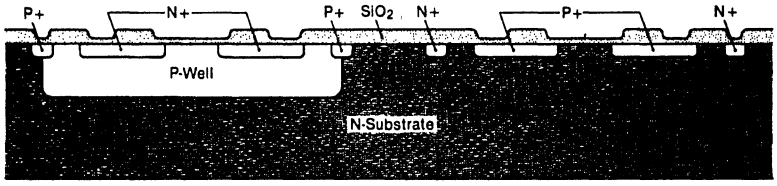

FIGURE 9. Gate Oxidation, Thermally Grown Silicon Dioxide Layer Over N- and P-Channel Devices

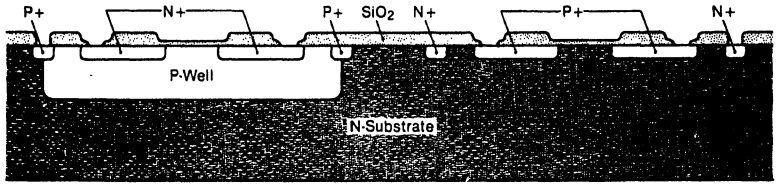

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FIGURE 10. Contact Mask and Openings to N- and P-Channel Devices

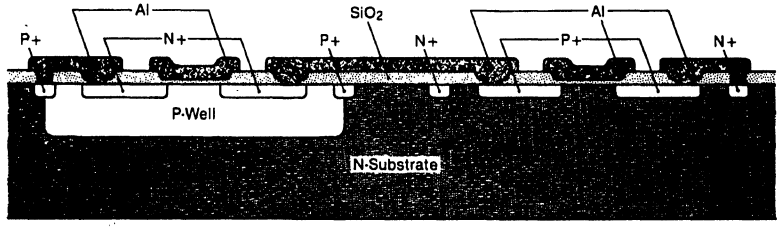

FIGURE 11. Metallization, Metal Mask, Resulting in Gate Metal and Metal Interconnects

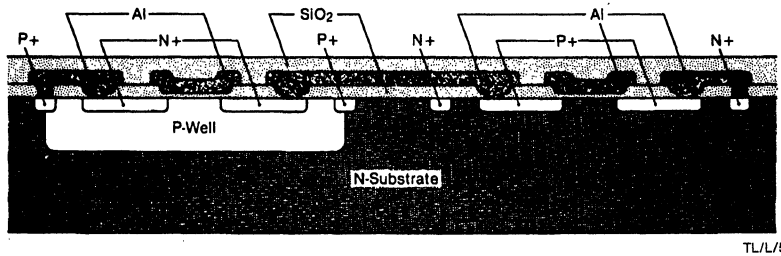

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FIGURE 12. Passivation Oxide, Deposited Silicon Dioxide Over Entire Die Surface

Silicon-Gate CMOS Processing

The silicon-gate CMOS process starts with the same two steps as the metal-gate process, yielding an N− substrate with an ion-implanted P− well (*Figures 13* and *14*). That, however, is where the similarity ends. Next, the initial oxide is stripped, and another layer of oxide, called pad oxide, is thermally grown. Also, a layer of silicon nitride is deposited across the surface of the wafer (*Figure 15*). The nitride prevents oxide growth on the areas it covers. Thus, in *Figure 16*, the nitride is etched away wherever field oxide is to be grown. The field oxide is a very thick layer of oxide, and it is grown everywhere except in the transistor regions (*Figure 17*). As an oxide grows in silicon, it consumes the silicon substrate beneath it and combines it with ambient oxygen to produce silicon dioxide. Growth of this very thick oxide causes the oxide to be recessed below the surface of the silicon substrate by a significant amount. A recessed field oxide eliminates the need for guard ring diffusions, because current cannot flow through the field oxide, which completely isolates each transistor from every other transistor.

The next step is to deposit a layer of polycrystalline silicon, also called poly, which will form both the gate areas and a second layer of interconnect (*Figure 18*). The poly is then etched, and any poly remaining becomes a gate if it is over gate oxide, and interconnect if it is over field oxide. A new layer of oxide is grown over the poly, which will act as an insulator between the poly and the metal interconnect (*Figure 19*). The poly over the transistor areas is not as wide as the gate oxide. This allows the source and drain diffusions to be ion implanted through the gate oxide. The poly gate itself, along with the field oxide, is used as a mask for implantation. Therefore, the source and drain implants will automatically be aligned to the gate poly, which is what makes this process a self-aligned gate process (*Figure 20*).

Figure 21 illustrates the steps of cutting contacts into the insulating layer of oxide, so the metal may be connected to gate and field poly, as well as to source and drain implants. A layer of metal is deposited across the entire wafer, and is etched to produce the desired interconnection. Finally, as in metal-gate processing, an insulating layer of oxide is deposited onto the wafer (*Figure 22*).

Advantages of Silicon-Gate Processing

There are three major ways in which silicon-gate processing reduces parasitic capacitance: recessed field oxide, lower gate overlap capacitance, and shallower junction depths. *Figures 23* and *24* are cross sections of metal gate and silicon gate CMOS circuits, respectively. These figures show the parasitic on-chip capacitances (C_1 through C_4) for each type of process.

The N+ and P+ source and drain regions, as well as guard ring regions, in the metal-gate process, have two capacitances associated with them: periphery and area capacitances (C_2 and C_1). These capacitances are associated with the diode junctions between the P+ regions and the N− substrate, as well as the N+ regions and P− well. The finer line widths of silicon-gate CMOS, coupled with the shallower junction depths, act to decrease the size of these parasitic diodes. Capacitance is proportional to diode area, hence the diode area reduction results in a significantly reduced parasitic capacitance in silicon-gate CMOS.

Another origin of unwanted capacitance is the area where the gate overlaps the source and drain regions (C_4). The overlap is much larger in metal-gate processing than in silicon-gate CMOS. This is due to the fact that the metal-gate must be made wider than the channel width to allow for alignment tolerances. In silicon-gate processing, since the gate acts as the mask for the ion implantation of the source and drain regions, there is no alignment error, which results in greatly reduced overlap.

How does the use of polysilicon gates increase the gain of a MOSFET? Polysilicon may be etched to finer line widths than metal, permitting the fabrication of transistors with shorter gate lengths. The equation that describes the gain of a MOSFET is shown below:

$$I = \frac{(\text{Beta})(\text{Width})}{2(\text{Length})}[(\text{Gate Voltage}) - (\text{Threshold Voltage})]^2$$

Thus, a decrease in gate length will cause an increase in current drive capability. This, in turn, will allow the transistor to charge a capacitance more rapidly, therefore increasing the gain of the transistor. Also, the gate oxide is thinner for the silicon-gate CMOS process. A thinner gate oxide increases the Beta term in the equation, which further increases gain. Finally, although it is not apparent from the processing cross sections, the transistor threshold (turn on) voltage is lower. This is accomplished by the use of ion implants to adjust the threshold.

There is one more advantage of silicon-gate processing that should be noted: the polysilicon provides for an additional layer of interconnect. This allows three levels of interconnect, which are metal, polysilicon, and the N+ and P+ ion-implanted regions. Having these three levels helps to keep the die area down, since much die area is usually taken up by interconnection.

When all these advantages are summed up, the result is a CMOS technology that produces devices as fast as the equivalent LSTTL device. *Figure 25* illustrates a comparison between the MM74HC00 buffered NAND gate and the MM74C00, CD4011B, and DM74LS00 NAND gates. The MM74HC00 is about an order of magnitude faster than the CD4011B buffered NAND gate, and about 5 times faster than the unbuffered MM74C00, at 15 pF. As load capacitance increases, the speed differential between metal-gate and silicon-gate CMOS increases, with the MM74HC00 operating as fast as the DM74S00 at any load capacitance.

Summary

Polycrystalline silicon-gate CMOS has many advantages over metal-gate CMOS. It is faster because on-chip parasitic capacitances are reduced and transistor gains are increased. This is due mainly to a recessed field oxide and a self-aligned gate process. Transistor gains are increased by decreasing transistor lengths and threshold voltages, and increasing beta. Polysilicon also allows for an extra layer of interconnect, which helps to keep die area down.

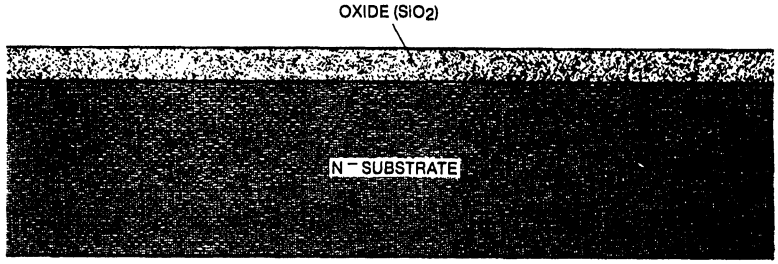

FIGURE 13. Initial Oxidation, Thermally Grown Silicon Dioxide on N− Silicon Substrate

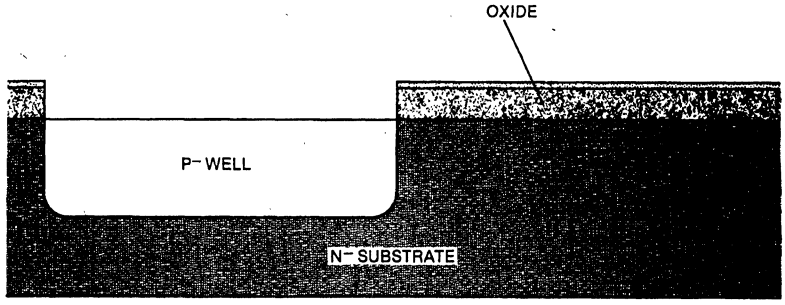

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FIGURE 14. Ion-Implanted P− Tub in Which N-Channel Devices Will Be Located

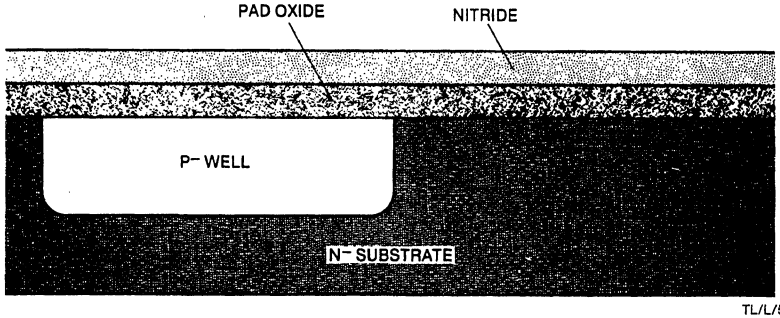

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FIGURE 15. Initial Oxide Is Stripped, Pad Oxide Is Thermally Grown, and a Layer of Silicon Nitride Is Deposited Across the Surface of the Wafer

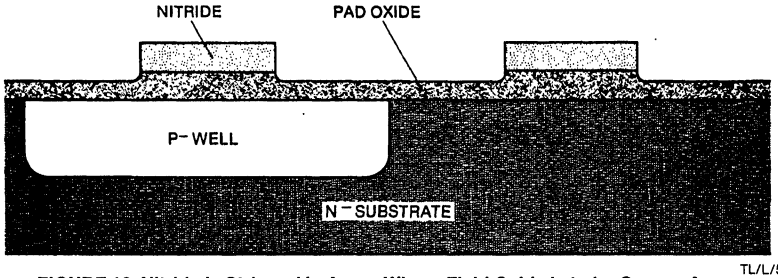

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FIGURE 16. Nitride Is Stripped in Areas Where Field Oxide is to be Grown. Areas Covered by Nitride Will Become Transistor Area

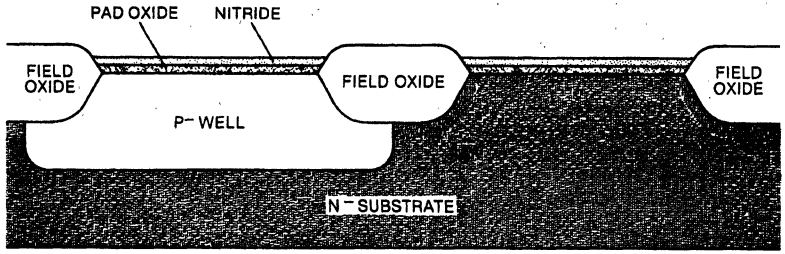

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FIGURE 17. Field Oxide Is Thermally Grown. The Nitride Acts as a Barrier to Oxide Growth

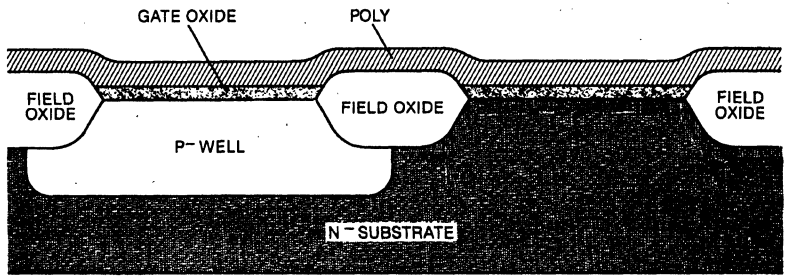

FIGURE 18. Nitride is Stripped, Pad Oxide Is Stripped Over Transistor Areas and a Thin Gate Oxide Is Grown Polycrystalline Silicon Is Deposited

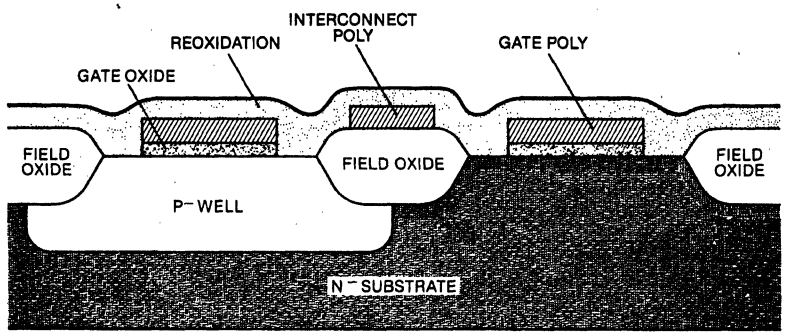

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FIGURE 19. Polysilicon Layer Is Etched to Provide Gate and Interconnect Poly Areas. New Layer of Oxidation is Grown

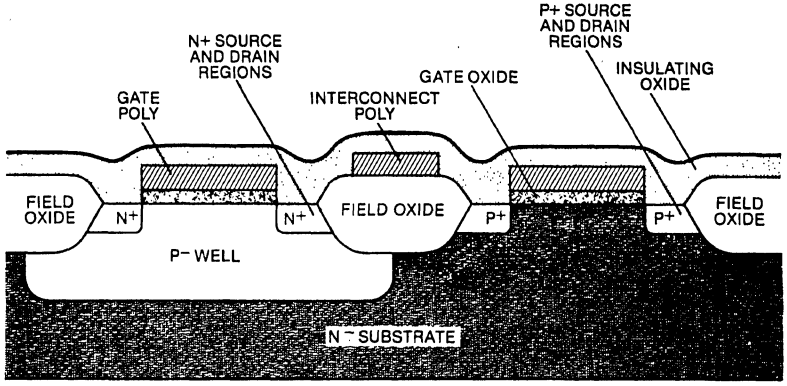

FIGURE 20. N+ and P+ Source and Drain Regions Are Ion Implanted, and the Reoxidation Is Grown Thicker to Form an Insulating Layer

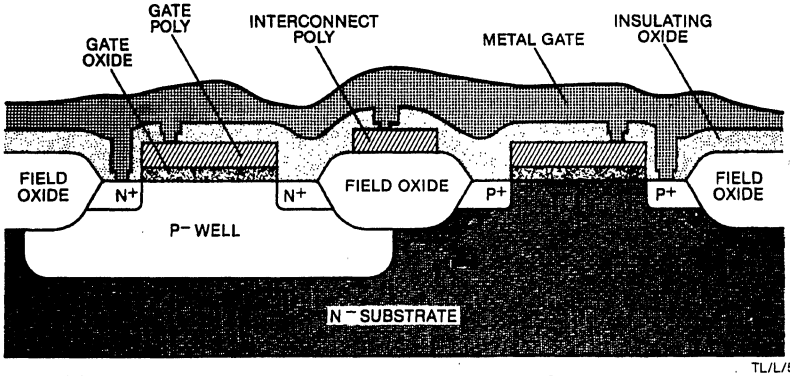

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FIGURE 21. Contact Openings Are Cut in the Insulating Oxide, and a Layer of Metalization Is Deposited Across the Entire Wafer

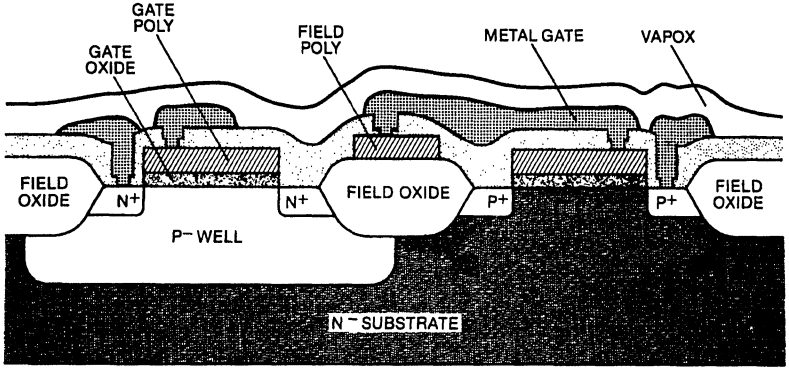

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FIGURE 22. Metal Mask Is Etched to Provide Interconnect. Vapox (SiO_2) Is Deposited Over Entire Surface of Wafer

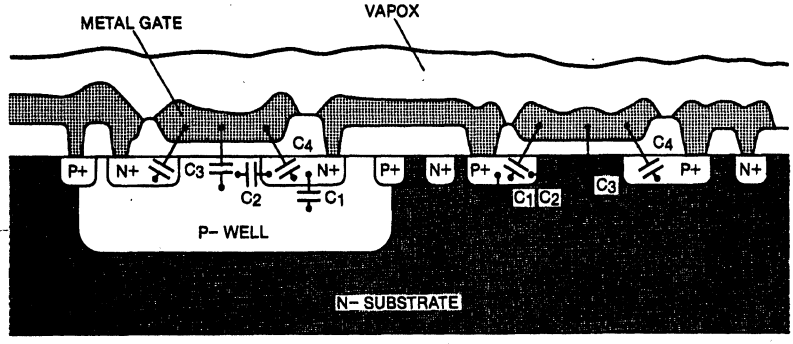

FIGURE 23. Cross Section of Metal Gate CMOS Process Showing Parasitic On-Chip Capacitances

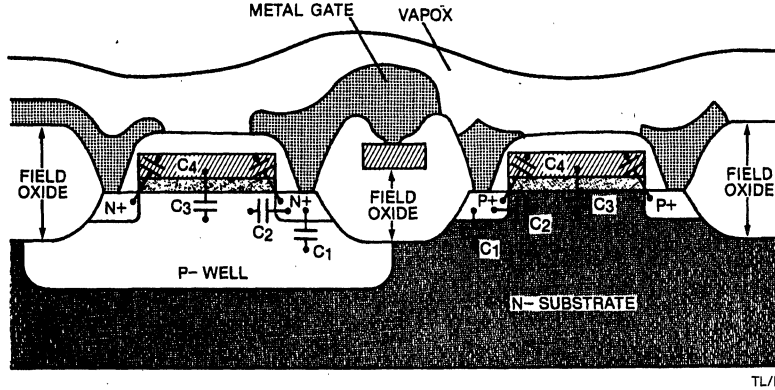

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FIGURE 24. Cross Section of Silicon Gate CMOS Process Showing Parasitic On-Chip Capacitances

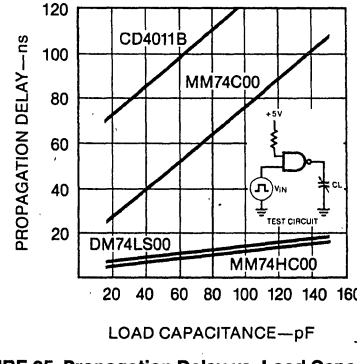

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FIGURE 25. Propagation Delay vs. Load Capacitance for 2-Input NAND Gate

DC Electrical Characteristics of MM54HC/MM74HC High-Speed CMOS Logic

National Semiconductor
Application Note 313
Larry Wakeman
June 1983

The input and output characteristics of the MM54HC/MM74HC high-speed CMOS logic family were conceived to meet several basic goals. These goals are to provide input current and voltage requirements, noise immunity and quiescent power dissipation similar to CD4000 and MM54C/MM74C metal-gate CMOS logic and output current drives similar to low power Schottky TTL. In addition, to enable merging of TTL and HC-CMOS designs, the MM54HCT/MM74HCT sub family differs only in their input voltage requirements, which are the same as TTL, to ease interfacing between logic families.

In order to familiarize the user with the MM54HC/MM74HC logic family, its input and output characteristics are discussed in this application note, as well as how these characteristics are affected by various parameters such as power supply voltage and temperature. Also, for those users who have been designing with metal-gate CMOS and TTL logic, notable differences and features of high-speed CMOS are compared to those logic families.

A Buffered CMOS Logic Family

The MM54HC/MM74HC is a "buffered" logic family like the CD4000B series CMOS. Buffering CMOS logic merely denotes designing the IC so that the output is taken from an inverting buffer stage. For example, the internal circuit implementation of a NAND gate would be a simple NAND followed by two inverting stages. An unbuffered gate would be implemented as a single stage. Both are shown in *Figure 1*. Most MSI logic devices are inherently buffered because they are inherently multi-stage circuits. Gates and similar small circuits yield the greatest improvement in performance by buffering.

There are several advantages to buffering this high-speed CMOS family. By using a standardized buffer, the output characteristics for all devices are more easily made identical. Multi-stage gates will have better noise immunity due to the higher gain caused by having several stages from input to output. Also, the output impedance of an unbuffered gate may change with input logic level voltage and input logic combination, whereas buffered outputs are unaffected by input conditions.

Finally, single stage gates implemented in MM54HC/MM74HC CMOS would require large transistors due to the large output drive requirements. These large devices would have a large input capacitance associated with them. This would affect the speed of circuits driving into an unbuffered gate, especially when driving large fanouts. Buffered gates have small input transistors and correspondingly small input capacitance.

One may think that a major disadvantage of buffered circuits would be speed loss. It would seem that a two or three stage gate would be two to three times slower than a buffered one. However, internal stages are much faster than the output stage and the speed lost by buffering is relatively small.

The one exception to buffering is the MM54HCU04/MM74HCU04 hex inverter which is unbuffered to enable its use in various linear and crystal oscillator applications.

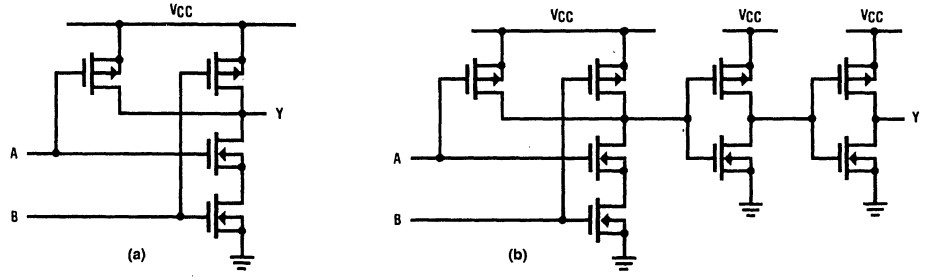

FIGURE 1. Schematic Diagrams of (a) Unbuffered and (b) Buffered NAND Gate

CMOS Input Voltage Characteristics

As mentioned before, MM54HC/MM74HC standard input levels are similar to metal-gate CMOS. This enables the high-speed logic family to enjoy the same wide noise margin of CD4000 and MM54C/MM74C logic. With $V_{CC}=5V$ these input levels are 3.5V for minimum logic "1" (V_{IH}) and 1.0V for a logic "0" (V_{IL}). The output levels when operated at $V_{CC}=5V\pm10\%$ and worst case input levels, are specified to be $V_{CC}-0.1$ or 0.1V. The output levels will actually be within a few millivolts of either V_{CC} or ground.

When operated over the entire supply voltage range, the input logic levels are: $V_{IH}=0.7V_{CC}$ and $V_{IL}=0.2V_{CC}$. *Figure 2* illustrates the input voltage levels and the noise margin of these circuits over the power supply range. The shaded area indicates the noise margin which is the difference between the input and output logic levels. The logic "1" noise margin is 29% of V_{CC} and the logic "0" noise margin is 19% of V_{CC}. Also shown for comparison are the 54LS/74LS input levels and noise margins over their supply range.

These input levels are specified on individual data sheets at $V_{CC}=2.0V$, 4.5V, 6.0V. At 2.0V the input levels are not quite $0.7(V_{CC})$ and $0.2(V_{CC})$ as at low voltages transistor turn on thresholds become significant. This is shown in *Figure 2*.

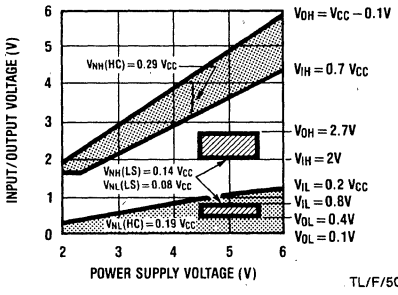

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FIGURE 2. Worst Case Input and Output Voltages Over Operating Supply Range for "HC" and "LS" Logic

The input and output logic voltages and their behavior with temperature variation is determined by the input to output transfer function of the logic circuit. *Figure 3a* shows the transfer function of the MM54HC00/MM74HC00 NAND gate. As can be seen, the NAND gate has V_{CC} and ground output levels and a very sharp transition at about 2.25V. Thus, good noise immunity is achieved, since input noise of a volt or two will not appear on the output. The transition point is also very stable with temperature, drifting typically 50 or so millivolts over the entire temperature range. As a comparison, the transfer function for a 54LS00/74LS00 is plotted in *Figure 3b*. LSTTL output transitions at about 1.1V and the transition region varies several hundred millivolts over the temperature range. Also, since the transition region is closer to the low logic level, less ground noise can be tolerated on the input.

In typical systems, noise can be capacitively coupled to the signal lines. The amount of voltage coupled by capacitively induced currents is dependent on the impedance of the output driving the signal line. Thus, the lower the output impedance the lower the induced voltage. High-speed CMOS offers improved noise immunity over CD4000 in this respect because its output impedance is one tenth that of CD4000 and so it is about 7 times less susceptible to capacitively induced current noise.

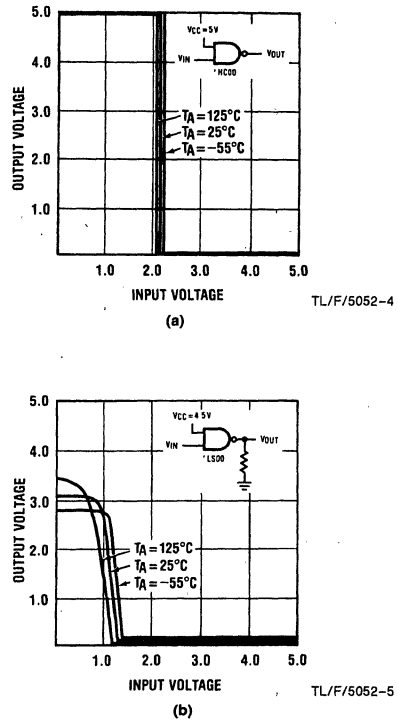

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FIGURE 3. Input/Output Transfer Characteristics for (a) 'HC00 and (b) 'LS00 Nand Gate

The MM54HCT/MM74HCT sub-family of MM54HC/MM74HC logic provides TTL compatible input logic voltage levels. This will enable TTL outputs to be guaranteed to correctly drive CMOS inputs. An incompatibility results because TTL outputs are only guaranteed to pull to a 2.7V logic high level, which is not high enough to guarantee a valid CMOS logic high input. To design the entire family to be TTL compatible would compromise speed, input noise immunity and circuit size. This sub-family can be used to interface sub-systems implemented using TTL logic to CMOS sub-systems. The input level specifications of MM54HCT/MM74HCT circuits are the same as LSTTL. Minimum input high level is 2.0V and the maximum low level is 0.8V using a $5V\pm10\%$ supply.

A fairly simple alternative to interfacing from LSTTL is to tie a pull-up resistor from the TTL output to V_{CC}, usually 4–10 kΩ. This resistor will ensure that TTL will pull up to V_{CC}. (See Interfacing MM54HC/MM74HC High-Speed CMOS Logic application note.)

High-Speed CMOS Input Current and Capacitance

Both standard "HC" and TTL compatible "HCT" circuits maintain the ultra low input currents inherent in CMOS circuits when CMOS levels are applied. This current is typically less than a nanoamp and is due to reverse leakages of the input protection diodes. Input currents are so small that they can usually be neglected. Since CMOS inputs present essentially no load, their fanout is nearly infinite.

Each CMOS input has some capacitance associated with it, as do TTL inputs. This capacitance is typically 3–5 pF for MM54HC/MM74HC, and is due to package, input protection diode, and transistor gate capacitances. Capacitance information is given in the data sheets and is measured with all pins grounded except the test pin. This method is used because it yields a fairly conservative result and avoids capacitance meter and power supply ground loops and decoupling problems. *Figure 4* plots typical input capacitance versus input voltage for HC-CMOS logic with the device powered on. The small peaking at 2.2V is due to internal Miller feedback capacitance effects.

When comparing MM54HC/MM74HC input currents to TTL logic, 54LS/74LS does need significantly more input current. LSTTL requires 400 μA of current when a logic low is applied and 40 μA in the high state which is significantly more than the worst case 1 μA leakage that MM54HC/MM74HC has.

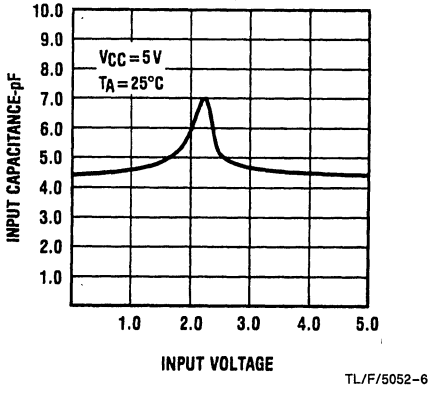

FIGURE 4. Input Capacitance vs. Input Voltage for a Typical Device

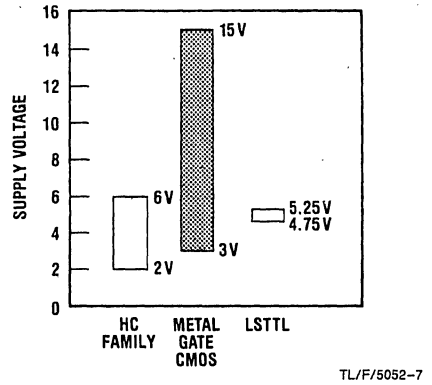

FIGURE 5. Comparison of Supply Range for "HC", "LS" and Metal-Gate

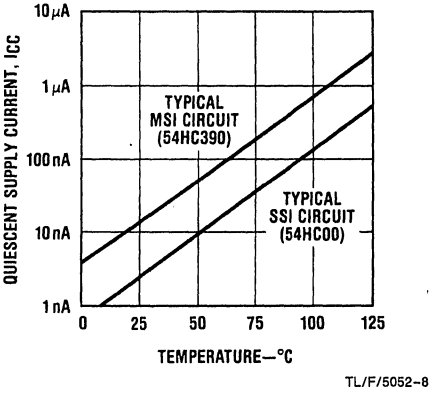

FIGURE 6. Typical Quiescent Supply Current Variation with Temperature

MM54HC/MM74HC Power Supply Voltage and Quiescent Current

Figure 5 compares the operating power supply range of high-speed CMOS to TTL and metal-gate CMOS. As can be seen, MM54HC/MM74HC can operate at power supply voltages from 2–6V. This range is narrower than the 3–15V range of CD4000 and MM54C/MM74C CMOS. The narrower range is due to the silicon-gate CMOS process employed which has been optimized to attain high operating frequencies at V_{CC} = 5V. The 2–6V range is however much wider than the 4.5V to 5.5V range specified for TTL circuits, and guaranteeing operation down to 2V is useful when operating CMOS off batteries in portable or battery backup applications.

The quiescent power supply current of the high-speed CMOS family is very similar to CD4000 and MM54C/MM74C CMOS. When CMOS circuits are not switching there is no current path between V_{CC} and ground, except for leakage currents which are typically much less than 1 μA. These are due to diode and transistor leakages.

Figure 6 illustrates how this leakage increases with temperature by plotting typical leakage current versus temperature for an MSI and SSI device. As a result of this temperature dependence, there is a set of standardized I_{CC} specifications which specify higher current at elevated temperatures. A summary of these specifications are shown in Table 1.

TABLE 1. Standardized I_{CC} Specifications for MM54HC/MM74HC Logic at 25°C, 85°C and 125°C at V_{CC} = 6.0V

Temperature	Gates	Flip-Flops	MSI
25°C	2 μA	4 μA	8 μA
85°C	20 μA	40 μA	80 μA
125°C	40 μA	80 μA	160 μA

Output Characteristics

One of the prime advantages of MM54HC/MM74HC over metal-gate CMOS (besides speed) is the output drive current, which is about ten times CD4000 or MM54C/MM74C logic. The larger output current enables high-speed CMOS to directly drive large fanouts of 54LS/74LS devices, and also enables HC-CMOS to more easily drive large capacitive loads. This improvement in output drive is due to a variety of enhancements provided by the silicon-gate process used. The basic current equation for a MOSFET is:

$$I = (\text{Beta})(\text{Width/Length})((V_g - V_t)V_d - 0.5(V_d^2))$$

Where V_g is the transistor gate voltage, V_t is the transistor threshold voltage, and V_d is the transistor drain voltage which is equivalent to the circuit output voltage. This CMOS process, when compared to metal-gate CMOS, has increased transistor gains, Beta, and lower threshold voltages, V_t. Also, improved photolithography has reduced the transistor lengths, and wider transistors are also possible because of tighter geometries.

Figure 7 compares the output high and low current specifications of MM74HC, 74LS and metal-gate CMOS for standard device outputs. High-speed CMOS has worst case output low current of 4 mA which is similar to low power Schottky TTL circuits, and offers symmetrical logic high and low currents as well. In addition, CMOS circuits whose functions make them ideal for use driving large capacitive loads have a larger output current of 6 mA. For example, these bus driver outputs are used on the octal flip-flops, latches, buffers, and bidirectional circuits.

Table 2 summarizes the various output current specifications for MM54HC/MM74HC CMOS along with their equivalent LSTTL fanouts. As Table 2 shows, the output currents of the MM54HC/MM74HC devices are derated from the MM74HC devices. The derating is caused by the decrease in current drive of the output transistors as temperature is increased. To show this, *Figure 8* plots typical output source and sink currents against temperature for both standard and bus driver circuits. This variation is similar to that found in metal-gate CMOS, and so the same −0.3% per °C derating that is used to approximate temperature derating of CD4000 and MM54C/MM74C can be applied to 54HC/74HC. As an example, the approximate worst case 25°C current drive one would expect by using the 4 mA 85°C data sheet number would be about 4 mA at $V_{OUT} = 0.26V$, and this is what is specified in the device data sheets.

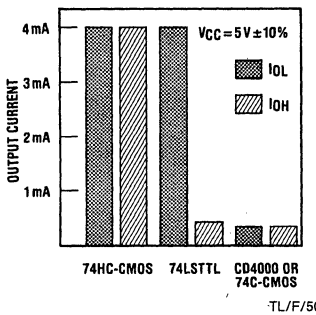

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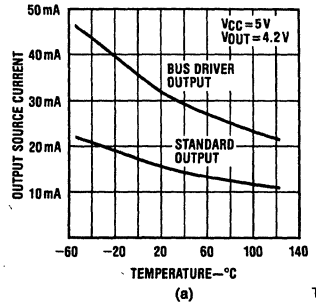
FIGURE 7. Comparison of 74HC, 74LS and CD4000/ 74C Output Drive Currents, I_{OH} and I_{OL}



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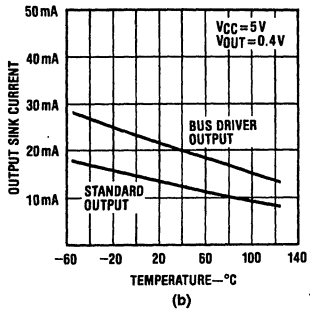

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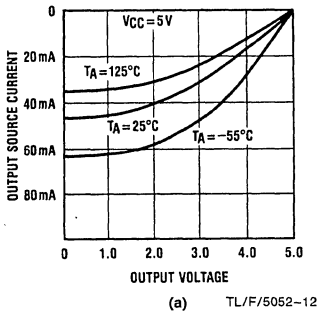
FIGURE 8. Typical Output (a) Source and (b) Sink Current Temperature for Standard and Bus Outputs

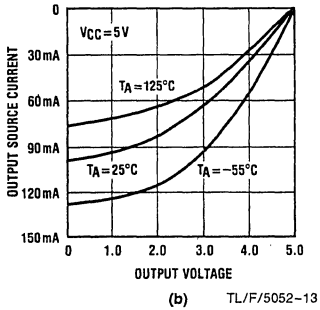
TABLE 2. Data Sheet Output Current Specifications for MM54HC/MM74HC Logic

Device $V_{CC} = 4.5V$	Output High Current	Output Low Current	LSTTL Fanout
Standard 54HC	4.0 mA ($V_{OUT} = 3.7V$)	4.0 mA ($V_{OUT} = 0.4V$)	10
Bus Driver 54HC	6.0 mA ($V_{OUT} = 3.7V$)	6.0 mA ($V_{OUT} = 0.4V$)	15
Standard 74HC	4.0 mA ($V_{OUT} = 3.94$)	4.0 mA ($V_{OUT} = 0.33V$)	10
Bus 74HC	6.0 mA ($V_{OUT} = 3.94$)	6.0 mA ($V_{OUT} = 0.33V$)	15

The data sheet specifications for output current are measured at only one output voltage for either source or sink current for each of three temperature ranges, room, commercial, and military. The outputs can supply much larger currents if larger output voltages are allowed. This is shown in *Figures 9* and *10*, which plot output current versus output voltage for both N-channel sink current and P-channel source current. Both standard and bus driver outputs are shown. For example, a standard output would typically sink 20 mA with $V_{OL}=1V$, and typically capable of a short circuit current of 50 mA.



(a) TL/F/5052–12



(b) TL/F/5052–13

FIGURE 9. Typical P-Channel Output Source Current vs. Output Voltage for (a) Standard and (b) Bus Outputs

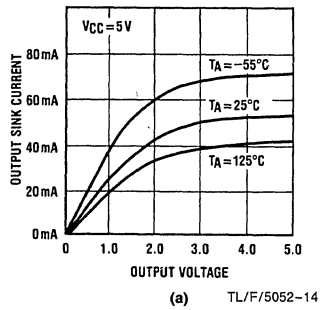
The output current and voltage characteristics of a logic circuit determine how well that circuit will switch its output when driving capacitive loads and transmission lines. The more current available, the faster the load can be switched. In order for HC-CMOS to achieve LSTTL performance, the outputs should have characteristics similar to LSTTL. This similarity is illustrated in *Figure 11* by plotted typical LSTTL and HC-CMOS output characteristics together.

As the supply voltage is decreased, the output currents will decrease. *Figure 12a* plots the output sink current versus power supply voltage with a 0.4V output voltage, and *Figure 12b* plots output source current against power supply with an output voltage of $V_{CC}-0.8V$. It is interesting to note that MM54HC/MM74HC powered at $V_{CC}=3V$, typically, will still drive 10 LSTTL inputs ($T=25°C$).

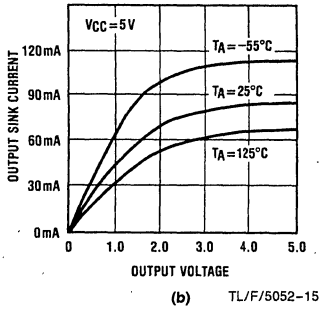
Absolute Maximum Ratings

Absolute maximum ratings are a set of guidelines that define the limits of operation for the MM54HC/MM74HC logic devices. To exceed these ratings could cause a device to malfunction and permanently damage itself. These limits are tabulated in Table 3, and their reasons for existing are discussed below.

The largest power supply voltage that should be applied to a device is 7V. If larger voltages are applied, the transistors will breakdown, or "punch through". The smallest voltage that should be applied to a MM54HC/MM74HC circuit is −0.5V. If more negative voltages are applied, a substrate diode would become forward biased. In both cases large currents could flow, damaging the device.

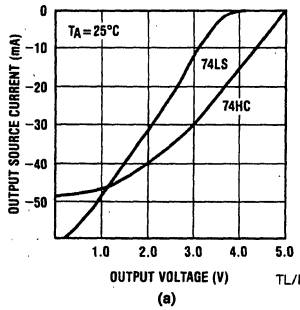


(a) TL/F/5052–14



(b) TL/F/5052–15

FIGURE 10. Typical N-Channel Output Sink Current vs. Output Voltage for (a) Standard and (b) Bus Outputs



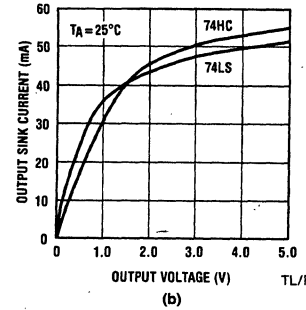
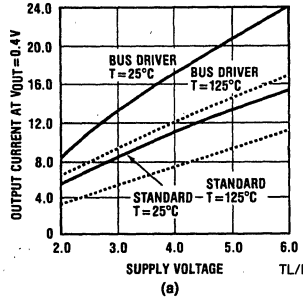


FIGURE 11. Comparison of Standard LSTTL and HC-CMOS Output (a) Source and (b) Sink Currents



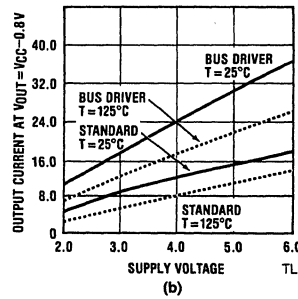


FIGURE 12. Output (a) Sink and (b) Source Current Variation with Power Supply

High-speed CMOS inputs should not have DC voltages applied to them that exceed V_{CC} or go below ground by more than 1.5V. To do so would forward bias input protection diodes excessive currents which may damage them. In actuality the diodes are specified to withstand 20 mA current. Thus the input voltage can exceed 1.5V if the designer limits his input current to less than 20 mA. The output voltages should be restricted to no less than −0.5V and no greater than $V_{CC}+0.5V$, or the current must be limited to 20 mA. The same limitations on the input diodes apply to the outputs as well. This includes both standard and TRI-STATE outputs. These are DC current restrictions. In normal high speed systems, line ringing and power supply spiking unavoidably cause the inputs or outputs to glitch above these limits. This will not damage these diodes or internal circuitry. The diodes have been specifically designed to withstand momentary transient currents that would normally occur in high speed systems.

Additionally, there is a maximum rating on the DC output or supply currents as shown in Table 3. This is a restriction dictated by the current capability of the integrated circuit metal traces. Again this is a DC specification and it is expected that during switching transients the output and supply currents could exceed these specifications by several times these numbers.

For most CD4000 and MM54C/MM74C CMOS operating at $V_{CC}=5V$, the designer does not need to worry about excessive output currents, since the output transistors usually cannot source or sink enough current to stress the metal or dissipate excessive amounts of power. The high-speed CMOS devices do have much improved output characteristics, so care should be exercised to ensure that they do not draw excessive currents for long durations, i.e., greater than 0.1 seconds. It is also important to ensure that internal dissipation of a circuit does not exceed the package power dissipation. This will usually only occur when driving large currents into small resistive loads.

TABLE 3. Absolute Maximum Ratings for MM54HC/MM74HC CMOS Logic

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to 7.0	V
V_{IN}	DC Input Voltage		−1.5 to $V_{CC}+1.5$	V
V_{OUT}	DC Output Voltage		−0.5 to $V_{CC}+0.5$	V
I_{OUT}	DC Current, Per Output Pin	Standard	±25	mA
		Bus Driver	±35	mA
I_{CC}	DC V_{CC} or Ground Current	Standard	±50	mA
		Bus Driver	±70	mA
I_{IK}, I_{OK}	Input or Output Diode Current		±20	mA

MM54HC/MM74HC Input Protection

As with any circuits designed with MOS transistors "HC" logic must be protected against damage due to excessive electrostatic discharges, which can sometimes occur during handling and assembly procedures. If no protection were provided, large static voltages appearing across any two pins of a MOS IC could cause damage. However, the new input protection which takes full advantage of the "HC" silicon-gate process has been carefully designed to reduce the susceptibility of these high-speed CMOS circuits to oxide rupture due to large static voltages. In conjunction with the input protection, the output parasitic diodes also protect the circuit from large static voltages occuring between any input, output, or supply pin.

Figure 13 shows a schematic of the input protection network employed. The network consists of three elements: a polysilicon resistor, a diode connected to V_{CC}, and a distributed diode-resistor connected to ground. This high-speed process utilizes the poly resistor to more effectively isolate the input diodes than the diode-resistor used in metal-gate CMOS. This resistor will slow down incoming transients and dissipate some of their energy. Connected to the resistor are the two diodes which clamp the input spike and prevent large voltages from appearing across the transistor. These diodes are larger than those used in metal-gate CMOS to enable greater current shunting and make them less susceptable to damage. The input network is ringed by V_{CC} and ground diffusions, which prevent substrate currents caused by these transients from affecting other circuitry.

The parasitic output diodes (*Figure 13*) that isolate the output transistor drains from the substrate are also important in preventing damage. They clamp large voltages that appear across the output pins. These diodes are also ringed by V_{CC} and ground diffusions to again shunt substrate currents, preventing damage to other parts of the circuit.

Summary

The MM54HC/MM74HC, because of many process enhancements, does provide a combination of features from 54LS/74LS and metal-gate CMOS logic families. High-speed CMOS gives the designer increased flexibility in power supply range over LSTTL, much larger output drive than CMOS has previously had, wider noise immunity than 54LS/74LS, and low CMOS power consumption.

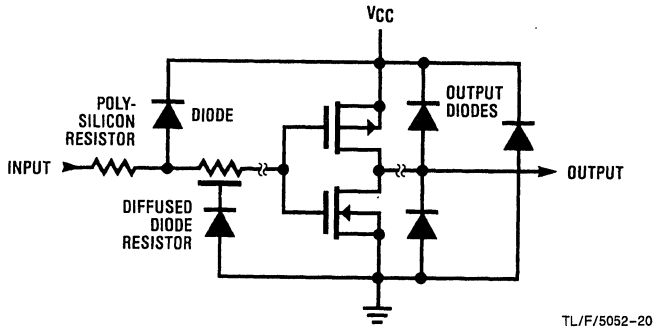


FIGURE 13. Schematic Diagram of Input and Output Protection Structures

Interfacing to MM54HC/ MM74HC High-Speed CMOS Logic

National Semiconductor
Application Note 314
Larry Wakeman
June 1983

On many occasions it might be necessary to interface MM54HC/MM74HC logic to other types of logic or to some other control circuitry. HC-CMOS can easily be interfaced to any other logic family including 54LS/74LS TTL, MM54C/MM74C, CD4000 CMOS and 10,000 ECL logic. Logic interfacing can be sub-divided into two basic categories: interfacing circuitry operating at the same supply voltage and interfacing to circuitry operating on a different voltage. In the latter case, some logic level translation is usually required, but many easily available circuits simplify this task. Usually, both instances require little or no external circuitry.

Interfacing Between TTL and MM54HC/MM74HC Logic

This high-speed CMOS family can operate from 2–6V, however, in most applications which interface to TTL, both logic families will probably operate off the same 5V TTL supply. The interconnection can be broken down into two categories: TTL outputs driving CMOS inputs, and CMOS outputs driving TTL inputs. In both cases the interface is very simple.

In the first case, TTL driving HC, there are some minor differences in TTL specifications for totem-pole outputs and high-speed CMOS input specifications. The TTL output low level is completely compatible with the MM54HC/MM74HC input low, but TTL outputs are specified to have an output high level of 2.4V (2.7V for LSTTL). High-speed CMOS's logic "1" input level is 3.5V (V_{CC} = 5.0V), so TTL is not guaranteed to pull a valid CMOS logic "1" level. If the TTL circuit is only driving CMOS, its output voltage is usually about 3.5V. HC-CMOS typically recognizes levels greater than 3V as a logic high, so in most instances TTL can drive MM74HC/MM54HC.

To see why TTL does not pull up further, *Figure 1a* shows a typical standard TTL gate's output schematic. As the output pulls up, it can go no higher than two diode voltage drops below V_{CC} due to Q2 and D2. So when operating with a 5V supply, the TTL output cannot go much higher than about 3.5V. *Figure 1b* shows an LSTTL gate, which has an output structure formed by Q2 and Q4. As the LSTTL output goes high, these two transistors cannot pull higher than two base-emitter voltage drops below V_{CC}, and, as above, the output cannot go much higher than 3.5V. If the output of either the LSTTL or TTL gate is loaded or the off sink transistor has some collector leakages, the output voltage will be lower.

Many LSTTL and ALSTTL circuits take R2 of *Figure 2b* and instead of connecting it to ground, it is connected to the output. This enables the TTL output to go to 4.3V (V_{CC} = 5.0V) which is more than adequate to drive CMOS. A simple measurement of open circuit V_{OH} can verify this circuit configuration.

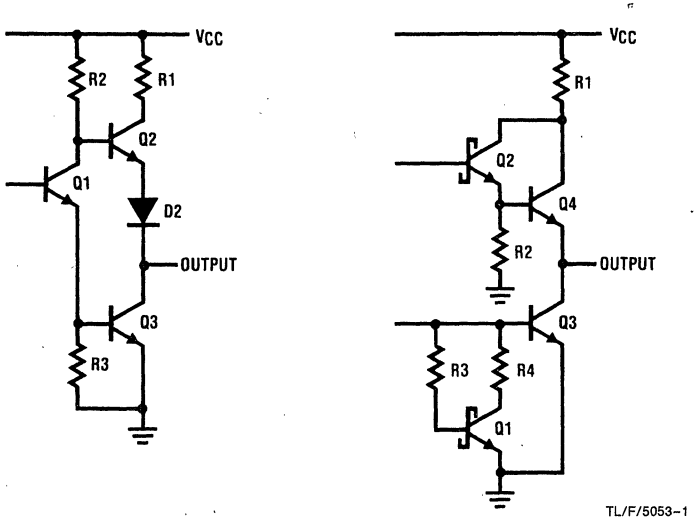


FIGURE 1. Schematic Diagrams for Typical (a) Standard and (b) Low Power Schottky TTL Outputs

Since LSTTL specifications guarantee a 2.7V output high level instead of a 3.5V output high, when designing to the worst case characteristics greater compatibility is sometimes desired. One solution to increase compatibility is to raise the output high level on the TTL output by placing a pull-up resistor from the TTL output to V_{CC}, as shown in *Figure 2*. When the output pulls up, the resistor pulls the voltage very close to V_{CC}. The value of the resistor should be chosen based on the LSTTL and CMOS fanout of the LS gate. *Figure 3* shows the range of pull-up resistors values versus LS fanout that can be used. For example, if an LSTTL device is driving only CMOS circuits, the resistor value is chosen from the left axis which corresponds to a zero LSTTL fanout.

A second solution is to use one of the many MM54HCT/MM74HCT TTL input compatible devices. These circuits have a specially designed input circuit that is compatible with TTL logic levels. Their input high level is specified at 2.0V and their input low is 0.8V with $V_{CC} = 5.0V \pm 10\%$. Thus LS can be directly connected to HC logic and the extra pull-up resistors can be eliminated. The direct interconnection of the TTL to CMOS translators is shown in *Figure 4*.

If TTL open collector outputs with a pull-up resistor are driving MM54HC/MM74HC logic, there is no interface circuitry needed as the external pull-up will pull the output to a high level very close to V_{CC}. The value of this pull-up for LS gates has the same constraints as the totem-pole outputs and its value can be chosen from *Figure 2* as well. The special TTL to CMOS buffers may also be used in this case, but they are not necessary.

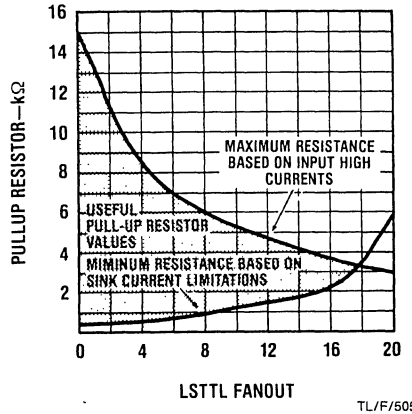


FIGURE 3. Range of Pull-Up Resistors for Low Power Schottkey TTL to CMOS Interface

When MM54HC/MM74HC outputs are driving TTL inputs, as shown in *Figure 5*, there is no incompatibility. Both the high and low output voltages are compatible with TTL. The only restriction in high-speed CMOS driving TTL is the same fanout restrictions that apply when TTL is driving TTL.

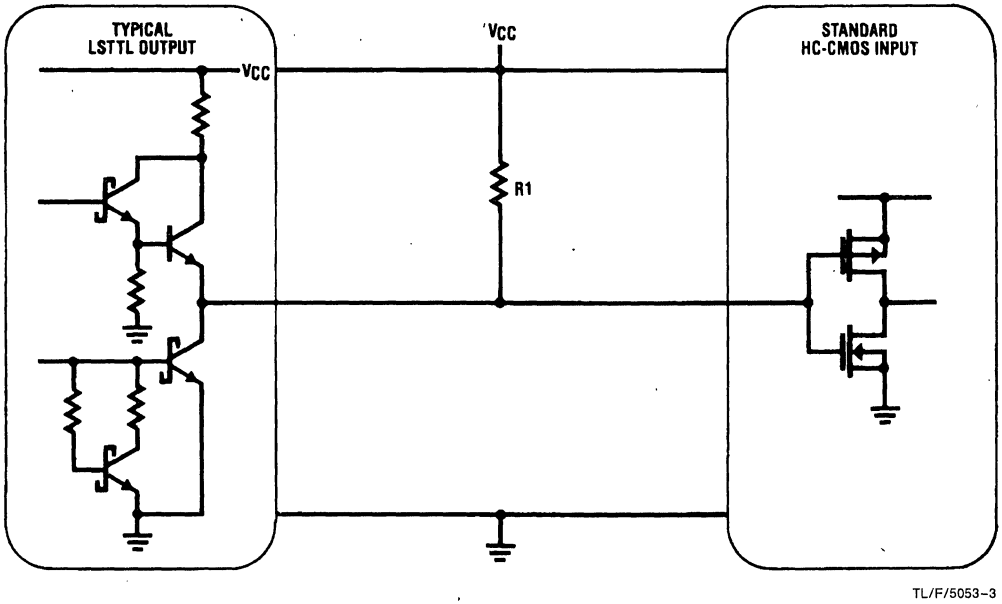


FIGURE 2. Interfacing LSTTL Outputs to Standard CMOS Inputs Using a Pull-Up Resistor

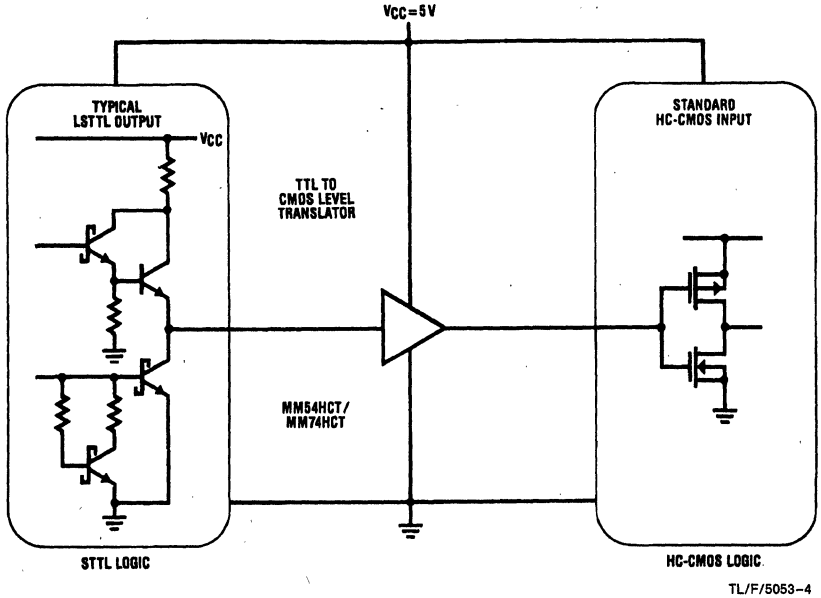


FIGURE 4. LSTTL Outputs Directly Drives MM54HCT/MM74HCT Logic Directly Which Can Interface to MM54HC/MM74HC

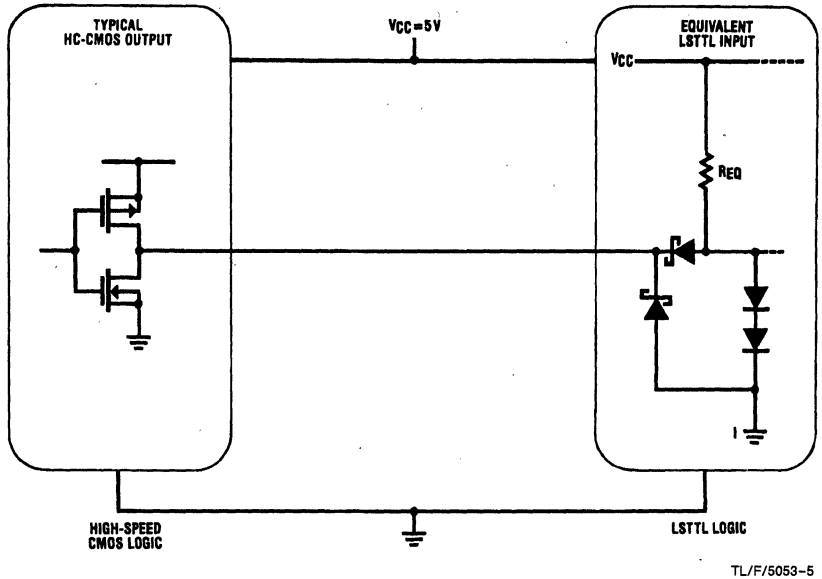


FIGURE 5. High-Speed CMOS Can Directly Connect Up to LSTTL Within its Fanout Restrictions

High-speed CMOS has much improved output drive compared to CD4000 and MM54C/MM74C metal-gate CMOS logic. *Figure 6* tabulates the fanout capabilities for this family. MM54HC/MM74HC standard outputs have a fanout capability of driving 10 LSTTL equivalent load and MM74HC bus driver outputs can drive up to 15 LSTTL inputs. It is unlikely that greater fanouts will be necessary, but several gates can be paralleled to increase output drive.

MM54HC/MM74HC and NMOS/HMOS Interconnection

With the introduction of CMOS circuits that are speed-equivalent to LSTTL, these fast CMOS devices will replace much of the bipolar support logic for many NMOS and HMOS microprocessor and LSI circuits. As a group, there is no real standard set of input and output specifications, but most NMOS circuits conform to TTL logic input and output logic level specifications.

NMOS outputs will typically pull close to V_{CC}. As with LSTTL, standard MM54HC/MM74HC CMOS inputs will typically accept NMOS outputs directly. However, to improve compatibility the MM54HCT/MM74HCT series of TTL compatible circuits may be used. These devices are particularly useful in microprocessor systems, since many of the octal devices are bus oriented and have pin-outs with inputs and outputs on opposite sides of the package. As with LSTTL, a second solution is to add a pull-up resistor between the NMOS output and V_{CC}. Both methods are shown in *Figure 7*.

MM54HC/MM74HC outputs can directly drive NMOS inputs. In fact, this situation is the same as if high-speed CMOS was driving itself. NMOS circuits have near zero input current and usually have input voltage levels that are TTL compatible. Thus MM54HC/MM74HC needs no additional circuitry to drive NMOS and there is also virtually no DC fanout restriction.

Interfacing High-Speed CMOS to MM54C/MM74C, CD4000 and CMOS-LSI

MM54HC/MM74HC CMOS and metal-gate CMOS logic interconnection is trivial. When both families are operated for the same power supply, no interface circuitry is needed. MM54HC/MM74HC, CD4000 and MM54C/MM74C logic families are completely input and output logic level compatible. Since both families have very low input currents, there is essentially no fanout limitations for either family.

The same input and output compatibility of the HC-CMOS makes it also ideal for use interfacing to CMOS-LSI circuits. For example, MM54HC/MM74HC can be directly connected to the NSC800, and 80C48 microprocessors and other P²CMOS products, as well as CMOS telecommunications products.

MM54HC/MM74HC to ECL Interconnection

There may be some instances where an ECL logic system must be connected to high-speed CMOS logic. There are several possible methods to interconnect these families. *Figure 8* shows one method which uses the 10125/10525 ECL to TTL interface circuit to go from ECL to HC-CMOS logic and the 10124/10524 to connect CMOS outputs to ECL inputs. These devices allow the CMOS to operate with $V_{CC} = 5V$ while the ECL circuitry uses a $-5.2V$ supply.

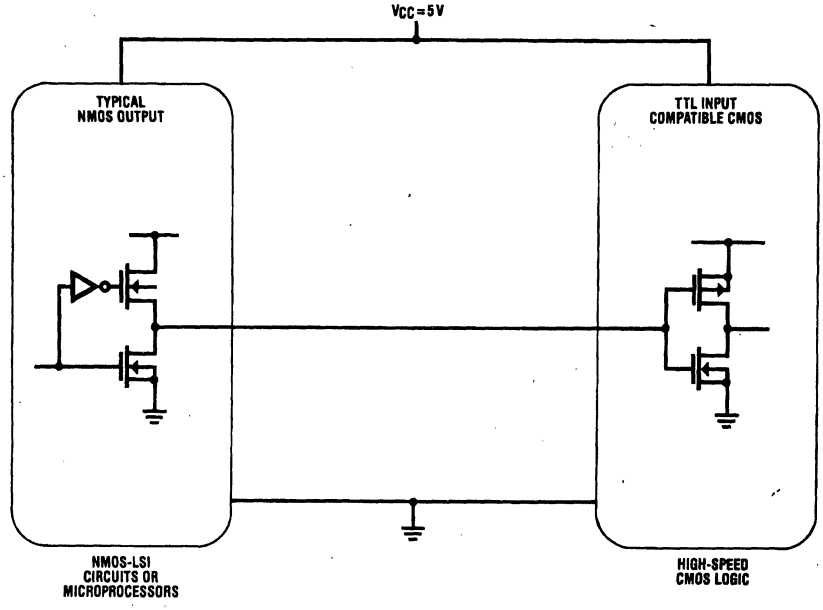
An alternate approach would be to operate the CMOS from the $-5.2V$ ECL supply as shown in *Figure 9*. Thus CMOS outputs could be directly connected to ECL inputs.

Logic Interfaces Requiring Level Translation

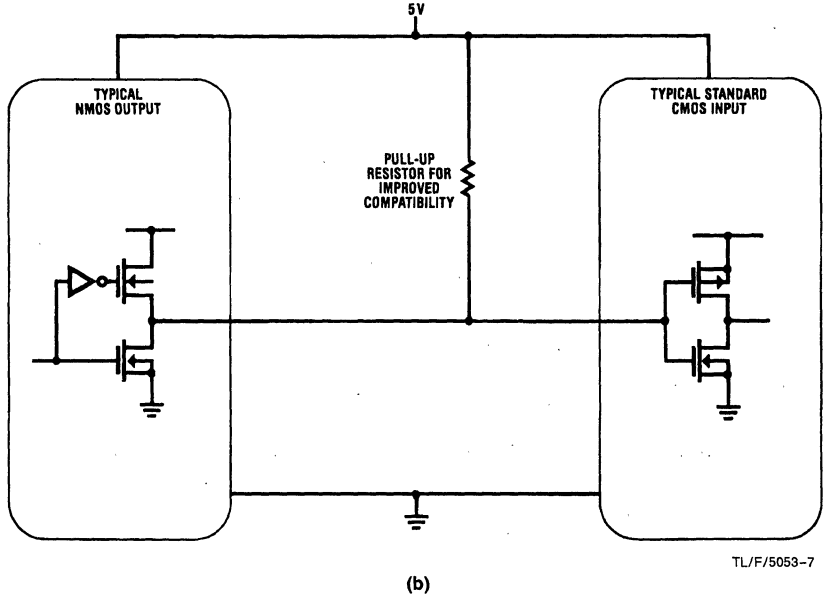
There are many instances when interfacing from one logic family to another that the other logic family will be operating from a different power supply voltage. If this is the case, a level translation must be accomplished. There are many different permutations of up and down level conversions that may be required. A few of the more likely ones are discussed here.

HC-CMOS Equivalent Fanouts	LSTTL		TTL		S-TTL		ALS-TTL	
	Min	Typ	Min	Typ	Min	Typ	Min	Typ
Standard Output MM54HC/MM74HC	10	20	2	4	2	4	20	40
Bus Driver Output MM54HC/MM74HC	15	30	4	8	3	6	30	60

FIGURE 6. Equivalent Fanout Capabilities of High-Speed CMOS Logic

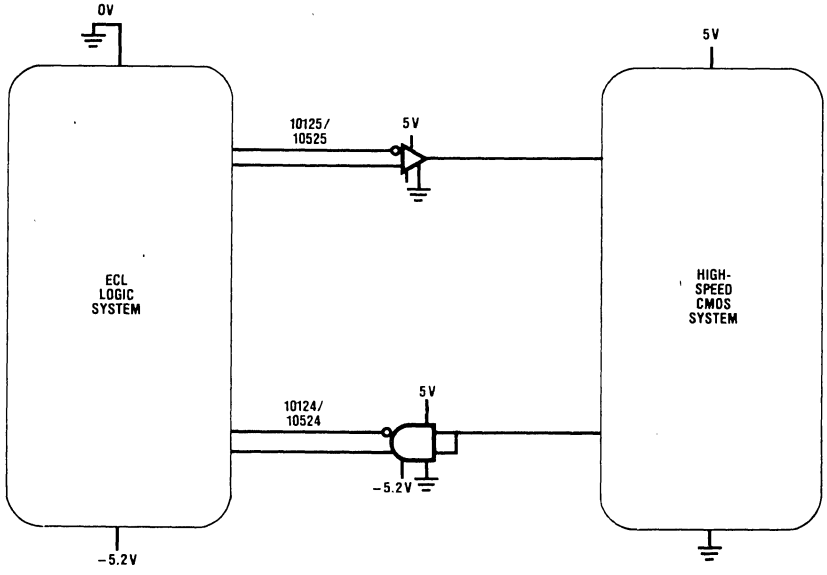


(a)



(b)

FIGURE 7. Improved Compatibility NMOS to CMOS Connection Using (a) TTL Input Compatible Devices or (b) External Pull-Up Resistors



TL/F/5053–8

FIGURE 8. MM54HC/MM74HC to ECL and ECL to HC-CMOS Interface

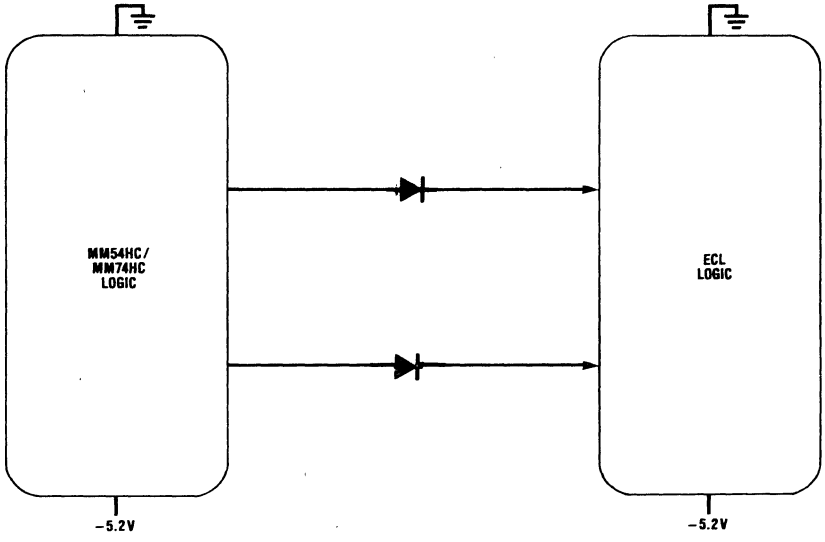


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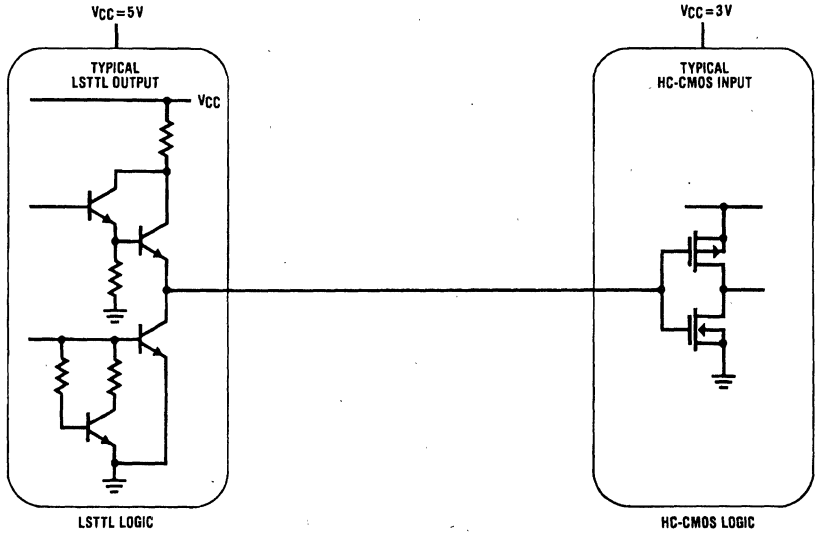
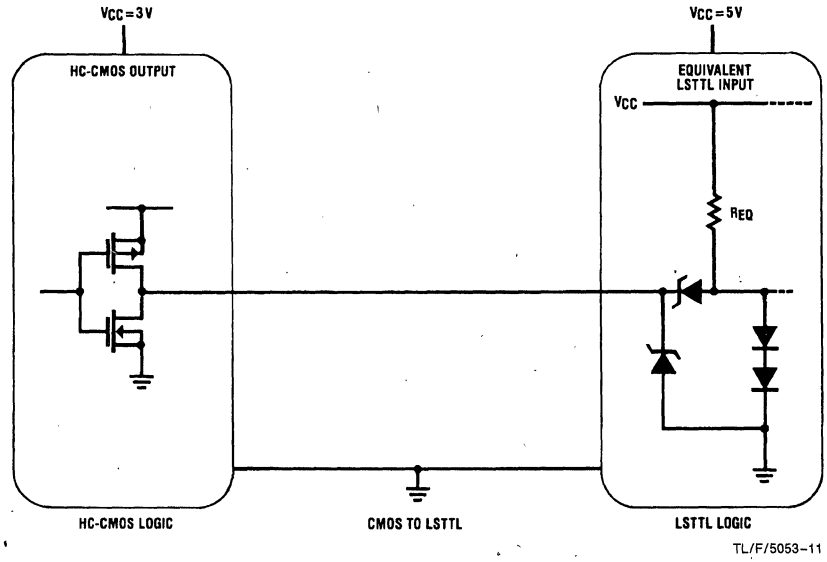
FIGURE 9. HC-CMOS Driving ECL Logic from Same Power Supply

If MM54HC/MM74HC is operated in a battery back up application for a TTL system, high-speed CMOS may be operated at $V_{CC} = 2-3V$ and can be connected to 5V TTL. CMOS operating at 3V can be directly connected to TTL since its input and output levels are compatible with TTL, and the TTL output levels are compatible with CMOS inputs, as shown in *Figure 10*. When high-speed CMOS is operated at 2V, the TTL outputs will exceed the CMOS power supply and the CMOS outputs will just barely pull high enough to drive TTL, so some level translation will be necessary.



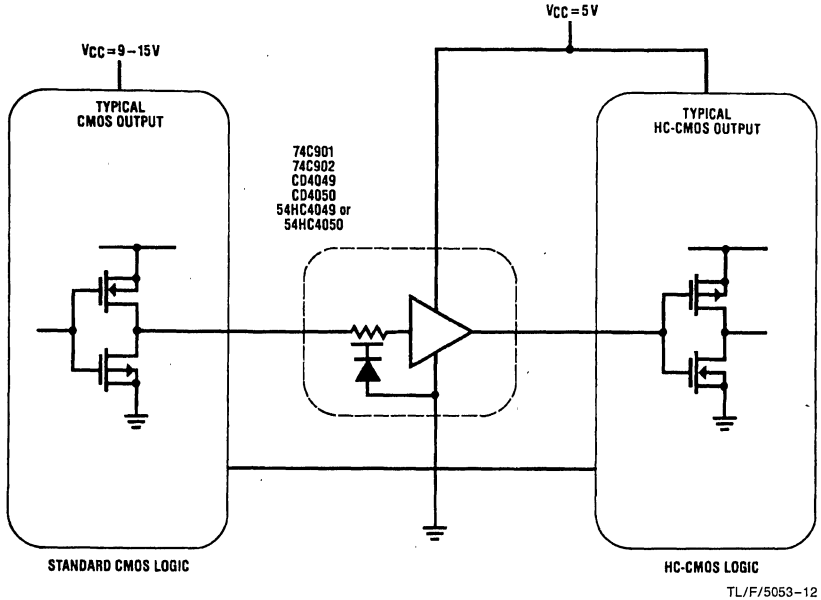
(a)



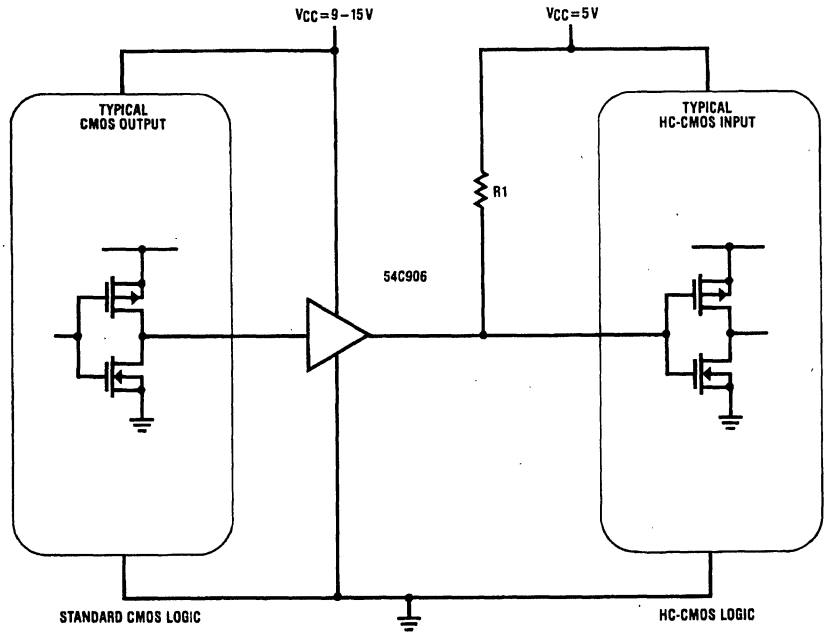
(b)

FIGURE 10. When HC-CMOS Is Operating At $V_{CC} = 3V$ No Logic Level Conversion Circuitry Is Needed

CD4000 and MM54C/MM74C metal-gate CMOS logic can be operated over a wider supply range that MM54HC/MM74HC, and because of this there will be instances when metal-gate CMOS and HC-CMOS will be operated off different supply voltages. Usually 9V to 15V CD4000 logic levels will have to be down converted to 5V high-speed CMOS levels. *Figure 11* shows several possible down conversion techniques using either a CD4049, CD4050, MM54HC4049, MM54HC4050, or MM54C906.



(a)

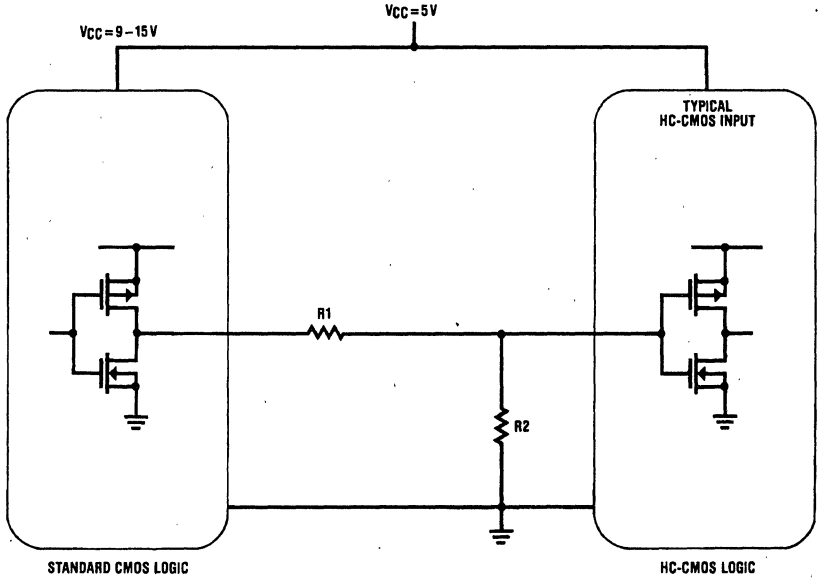


(b)

FIGURE 11. CD4000 or 74C Series CMOS to HC-CMOS Connection with Logic Level Conversion Using (a) Special Down Converters or (b) Open Drain CMOS

Since CMOS has a high input impedance, another possibility is to use a resistor voltage divider for down level conversion as shown in *Figure 12*. Voltage dividers will, however, dissipate some power.

Up conversion from MM54HC/MM74HC to metal-gate CMOS can be accomplished as shown in *Figure 13*. Here an MM54C906 open drain buffer with a pull-up resistor tied to the larger power supply is used.



TL/F/5053–14

FIGURE 12. CMOS to "HC" CMOS Logic Level Translation Using Resistor Divider

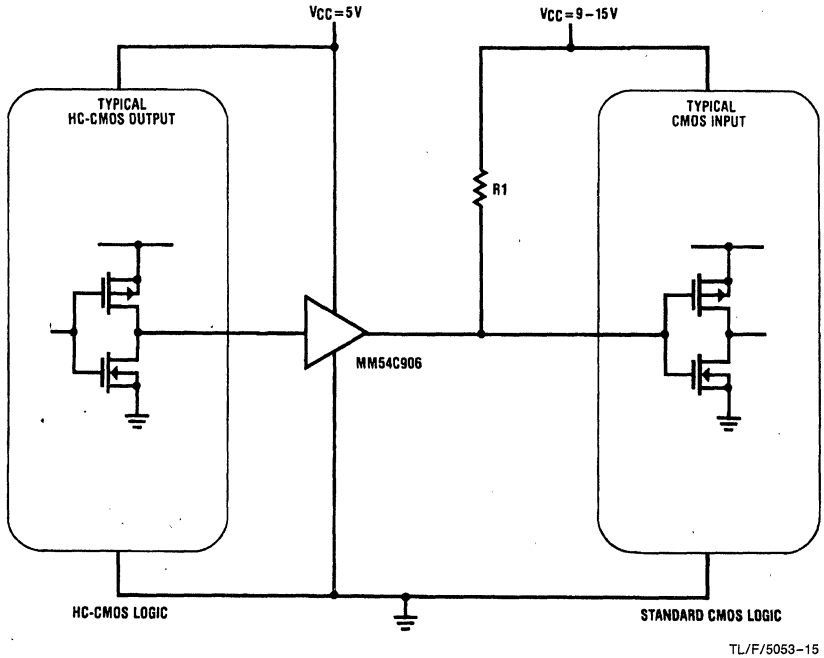


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FIGURE 13. HC-CMOS to CD4000 or 74C Series CMOS Connection with Logic Level Conversion Using an Open Drain CMOS Circuit

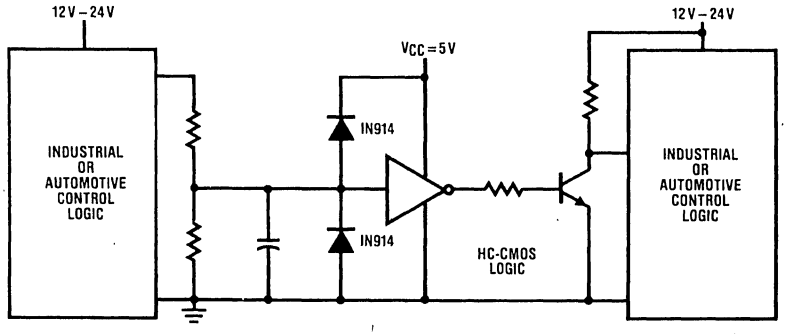


FIGURE 14. Interfacing Between HC-CMOS and High Voltage Control Logic

High Voltage and Industrial Control Interfaces

On occasion, interfacing to industrial and automotive control systems may be necessary. If these systems operate within the metal-gate CMOS supply range, interfacing MM54HC/MM74HC to them is similar to interfacing to CD4000 operating at a higher supply. In rugged industrial environments, care may be required to ensure that large transients do not harm the CMOS logic. *Figure 14* shows a typical connection to a high voltage system using diode clamps for input and output protection.

The higher drive of HC-CMOS can enable direct connection to relay circuits, but additional isolation is recommended. Clamp diodes should again be used to prevent spikes generated by the relay from harming the CMOS device. For higher current drive an external transistor may be used to interface to high-speed CMOS. Both of these are shown in *Figure 15*. Also, the higher drive enables easy connection to SCR's and other power control semiconductors as shown in *Figure 16*.

Conclusion

Interfacing between different logic families is not at all difficult. In most instances, when no logic level translation between is done, no external circuitry is needed to interconnect logic families. Even though the wide supply range of MM54C/MM74C and CD4000 creates many possible logic level conversion interface situations, most are easily handled by employing a minimum of extra circuitry. Additionally, several special interface devices also simplify logic level conversion.

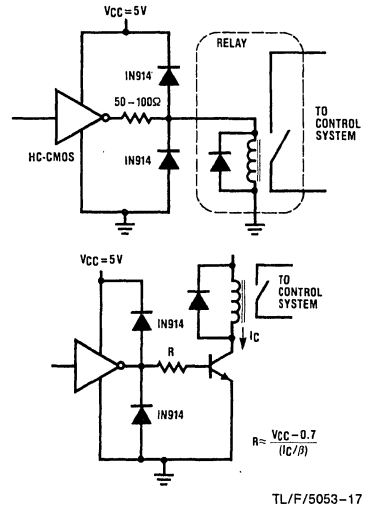


FIGURE 15. Interfacing MM54HC/MM74HC to Relays

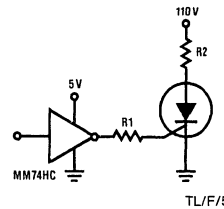


FIGURE 16. MM54HC/MM74HC Driving an SCR

AC Characteristics of MM54HC/MM74HC High-Speed CMOS

National Semiconductor
Application Note 317
Larry Wakeman
June 1983

When deciding what circuits to use for a design, speed is most often a very important criteria. MM54HC/MM74HC is intended to offer the same basic speed performance as low power Schottky TTL while giving the designer the low power and high noise immunity characteristics of CMOS. In other words, HC-CMOS is about ten times faster than CD4000 and MM54C/MM74C metal-gate CMOS logic. Even though HC-CMOS logic does have speeds similar to LSTTL, there are some differences in how this family's speeds are specified, and how various parameters affect circuit performance.

To give the designer an idea of the expected performance, this discussion will include how the AC characteristics of high-speed CMOS are specified. This logic family has been specified so that in the majority of applications, the specifications can be directly applied to the design. Since it is impossible to specify a device under all possible situations, performance variations with power supply, loading and temperature are discussed, and several easy methods for determining propagation delays in nearly any situation are also described. Finally, it is useful to compare the performance of HC-CMOS to 54LS/74LS and to CD4000.

Data Sheet Specifications

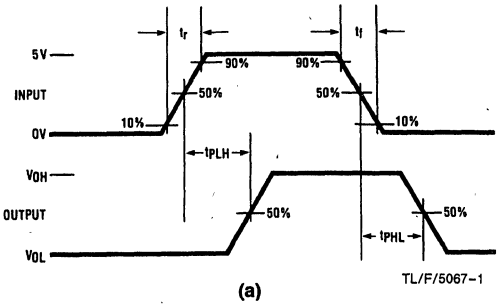
Even though the speeds achieved by this high-speed CMOS family are similar to LSTTL, the input, output and power supply characteristics are very similar to metal-gate CMOS. Because of this, the actual measurements for various timing parameters are not done the same way as TTL. The MM54HCT/MM74HCT TTL input compatible circuits are an exception.

Standard HC-CMOS AC specifications are measured at V_{CC} = 2.0V, 4.5V, 6.0V for room, military and commercial temperature ranges. Also HC is specified with LS equivalent supply (5.0V) and load conditions to enable proper comparison to low power Schottkey TTL. Input signal levels are ground to V_{CC} with rise and fall times of 6 ns (10% to 90%). Since standard CMOS logic has a logic trip point at about mid-supply, and the outputs will transition from ground to V_{CC}, timing measurements are made from the 50% points on input and output waveforms. This is shown in *Figure 1*. Using the mid-supply point gives a more accurate representation of how high-speed CMOS will perform in a CMOS system. This is different from the 1.3V measurement point and ground to 3V input waveforms that are used to measure TTL timing.

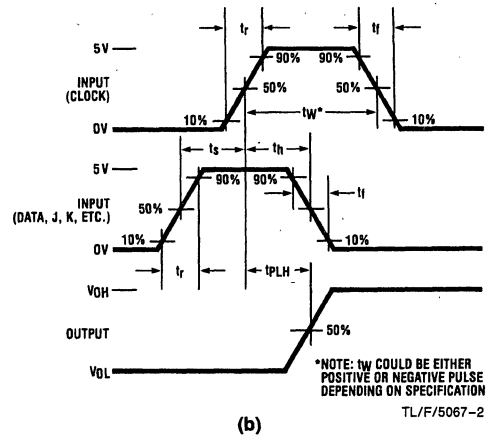
This output loading used for data sheet specifications fall into two categories, depending on the output drive capability of the specific device. The output drive categories are standard outputs (I_{OL} = 4 mA) and bus driver outputs (I_{OL} = 6 mA). Timing measurements for standard outputs are made using a 50 pF load. Bus driver circuits are measured using both a 50 pF and 150 pF load. In all AC tests, the test load capacitance includes all stray and test jig capacitances.

TRI-STATE® measurements where the outputs go from an active output level to a high impedance state, are made using the same input waveforms described above, but the timing is measured to the 10% or 90% points on the output waveforms. The test circuit load is composed of a 50 pF capacitor and a 1 kΩ resistor. To test t_{PHZ}, the resistor is swiched to ground, and for t_{PLZ} it is switched to V_{CC}. The TRI-STATE test circuit and typical timing waveforms are shown in *Figure 2*.

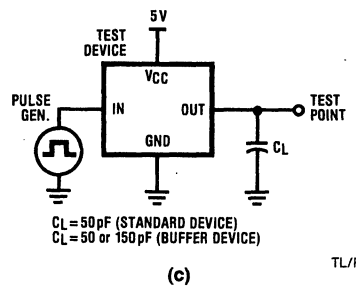
Measurements, where the output goes from the high impedance state to active output, are the same except that measurements are made to the 50% points and for bus driver devices both 50 pF and 150 pF capacitors are used.



(a)



(b)



(c)

FIGURE 1. Typical Timing Waveform for (a) Propagation Delays, and (b) Clocked Delays. Also Test Circuit (c) for These Waveforms ($t_r = t_f$ = 6 ns)

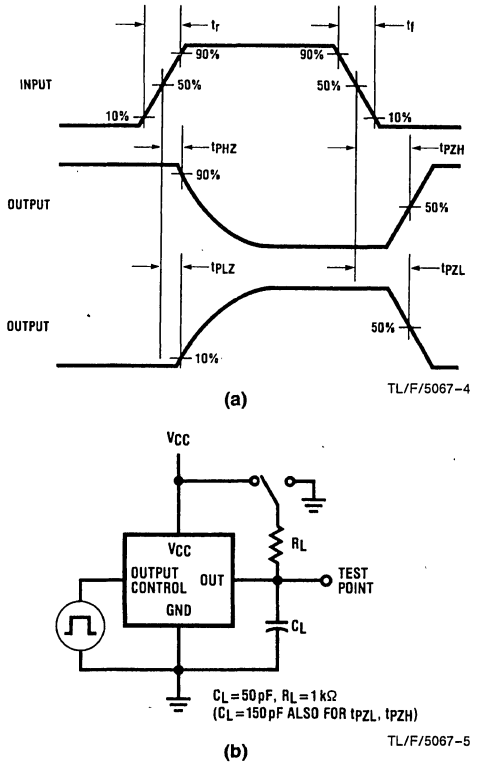


FIGURE 2. Typical TRI-STATE (a) Timing Waveforms and (b) Test Circuit

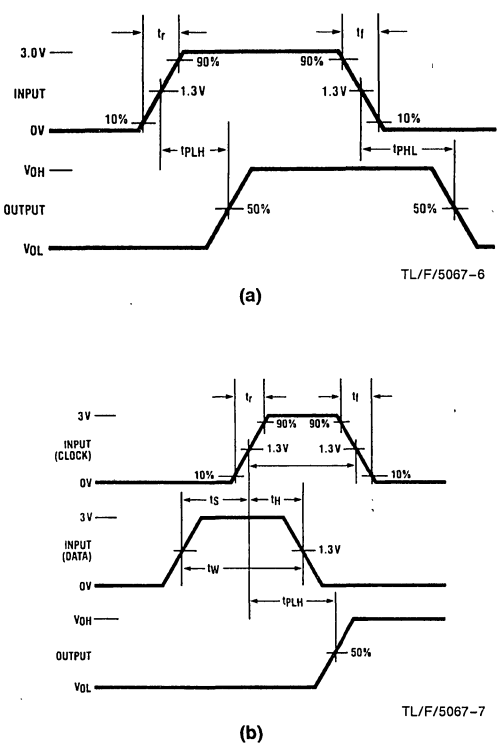


FIGURE 3. Typical Timing Waveforms for (a) Propagation Delays, and (b) Clocked Delays for 54HCT/74HCT Devices ($t_r = t_f = 6$ ns)

Note: Some early data sheets used a different test circuit. This has been changed or will be changed.

The MM54HCT/MM74HCT TTL input compatible devices are intended to operate with TTL devices, and so it makes sense to specify them the same way as TTL. Thus, as shown in *Figure 3*, typical timing input waveforms use 0–3V levels and timing measurements are made from the 1.3V levels on these signals. The test circuits used are the same as standard HC input circuits. This is shown in *Figure 3*. These measurements are compatible with TTL type specified devices.

Specifying standard MM54HC/MM74HC speeds using 2.5V input measurement levels does represent a specification incompatibility between TTL and most RAM/ROM and microprocessor speed specifications. It should not, however, present a design problem. The timing difference that results from using different measurement points is the time it takes for an output to make the extra excursion from 1.3V to 2.5V. Thus, for a standard high-speed CMOS output, the extra transition time should result, worst case, in less than a 2 ns increase in the circuit delay measurement for a 50 pF load. Thus in speed critical designs adding 1–2 ns safely enables proper design of HC into the TTL level systems.

Power Supply Affect on AC Performance

The overall power supply range of MM54HC/MM74HC logic is not as wide as CD4000 series CMOS due to performance optimization for 5V operation; however, this family can operate over a 2–6V range which does enable some versatility, especially when battery operated. Like metal-gate CMOS, lowering the power supply voltage will result in increased circuit delays. Some typical delays are shown in *Figure 4*. As the supply voltage is decreased from 5V to 2V, propagation delays increase by about two to three times, and when the voltage is increased to 6V, the delays decrease by 10–15%.

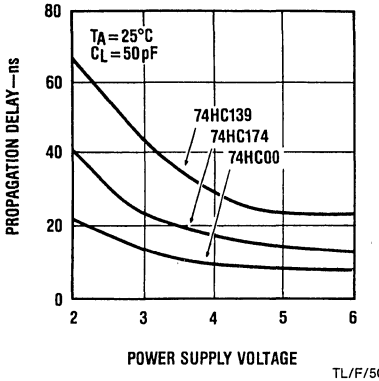


FIGURE 4. Typical Propagation Delay Variations of 74HC00, 74HC139, 74HC174 with Power Supply

In some designs it may be important to calculate the expected propagation delays for a specific situation not covered in the data sheet. This can easily be accomplished by using the normalized curve of *Figure 5* which plots propagation delay variation constant, t(V), versus power supply voltage normalized to 4.5V and 5V operation. This constant, when used with the following equation and the data sheet 5.0V specifications, yields the required delay at any power supply.

$$t_{PD}(V) = [t(V)]\,[t_{PD}(5V)] \qquad 1.0$$

Where $t_{PD}(5V)$ is the data sheet delay and $t_{PD}(V)$ is the resultant delay at the desired supply voltage. This curve can also be used for the $V_{CC} = 4.5V$ specifications.

For example, to calculate the typical delay of the 74HC00 at $V_{CC} = 6V$, the data sheet typical of 9 ns (15 pF load) is used. From *Figure 5* t(V) is 0.9, so the 6V delay would be 8 ns.

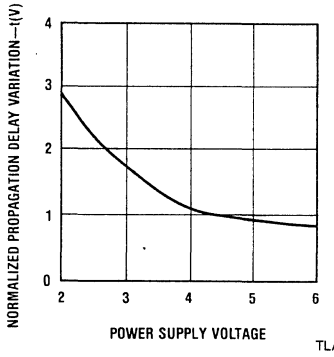


FIGURE 5. MM54HCMM74HC Propagation Delay Variation Vs. Power Supply Normalized to $V_{CC} = 4.5V$, and $V_{CC} = 5.0V$

Speed Variation with Capacitive Loading

When high-speed CMOS is designed into a CMOS system, the load on a given output is essentially capacitive, and is the sum of the individual input capacitances, TRI-STATE output capacitances, and parasitic wiring capacitances. As the load is increased, the propagation delay increases. The rate of increase in delay for a particular device is due to the increased charge/discharge time of the output and the load. The rate at which the delay changes is dependent on the output impedance of the MM54HC/MM74HC circuit. As mentioned, for high-speed CMOS, there are two output structures: bus driver and standard.

Figure 6 plots some typical propagation delay variations against load capacitance. To calculate under a particular load condition what the propagation delay of a circuit is, one need only know what the rate of change of the propagation delay with the load capacitance and use this number to extrapolate the delay from the data sheet vaue to the desired value. *Figure 7* plots this constant, t(C), against power supply voltage variation. Thus, by expanding on equation 1.0, the propagation delay at any load and power supply can be calculated using:

$$t_{PD}(C,V) = [t(C)(C_L - 15\text{ pF})] + [t_{PD}(5V)\,t(V)] \qquad 1.1$$

Where t(V) is the propagation delay variation with power supply constant, $t_{PD}(5V)$ is the data sheet 4.5V (use (C_L − = 50 pF) in equation) or 5V delay, C_L is the load capacitance and $t_{PD}(C,V)$ is the resultant propagation delay at the desired load and supply. This equation's first term is the difference in propagation delay from the desired load and the data sheet specification load. The second term is essentially equation 1.0. If the delay is to be calculated at $V_{CC} = 5V$, then t(V) = 1 and t(C) = 0.042 ns/pF (standard output), 0.028 ns/pF (bus output).

Using the previous 74HC00 example, the delay at $V_{CC} = 6V$ and a 100 pF load is:

$$t_{PD}(100\text{ pF},6V) = (0.042)(100—15) + (0.9 \times 9) = 11\text{ ns}$$

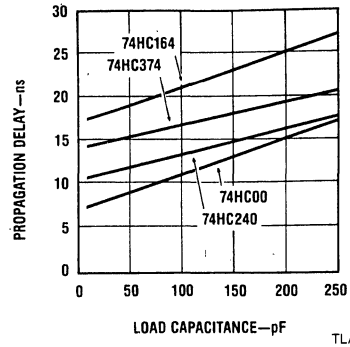


FIGURE 6. Typical Propagation Delay Variation With Load Capacitance for 74HC04, 74HC164, 74HC240, 74HC374

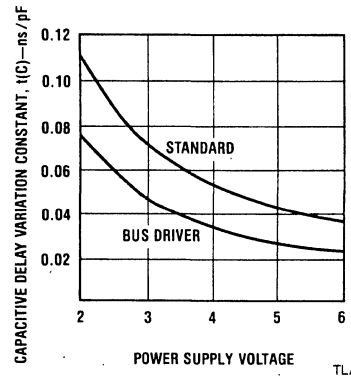


FIGURE 7. Propagation Delay Capacitance Variation Constant Vs. Power Supply

Speed Variations with Change in Temperature

Changes in temperature will cause some change in speed. As with CD4000 and other metal-gate CMOS logic parts, MM54HC/MM74HC operates slightly slower at elevated temperatures, and somewhat faster at lower temperatures. The mechanism which causes this variation is the same as that which causes variations in metal-gate CMOS. This

factor is carrier mobility, which decreases with increase in temperature, and this causes a decrease in overall transistor gain which has a corresponding affect on speed.

Figure 8 shows some typical temperature-delay variations for some high-speed CMOS circuits. As can be seen, speeds derate fairly linearly from 25°C at about −0.3%/C. Thus, 125°C propagation delays will be increased about 30% from 25°C. 54HC/74HC speeds are specified at room temperature, −40 to 85°C (commercial temperature range), and −55 to 125°C (military range). In virtually all cases the numbers given are for the highest temperature.

To calculate the expected device speeds at any temperature, not specified in the device data sheet, the following equation can be used:

$$t_{PD}(T) = [1 + ((T-25)(0.003))][t_{PD}(25)] \quad 1.2$$

Where $t_{PD}(T)$ is the delay at the desired temperature, and $t_{PD}(25)$ is the room temperature delay. Using the 74HC00 example from the previous section, the expected increase in propagation delay when operated at $V_{CC}=5V$ and 85°C is $[1+(85-25)(0.003)](10\ ns)]=12$ ns. The expected delay at some other supply can also be calculated by calculating the room temperature delay then calculating the delay at the desired temperature.

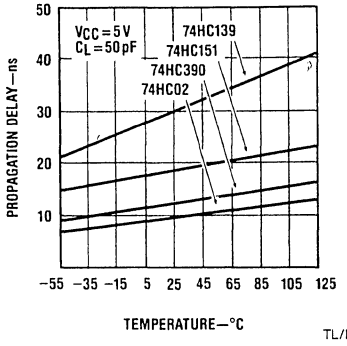


FIGURE 8. Typical Propagation Delay Variation With Temperature for 54HC02, 54HC390, 54HC139, 54HC151

Output Rise and Fall, Setup and Hold Times and Pulse Width Performance Variations

So far, the previous discussion has been restricted to propagation delay variations, and in most instances, this is the most important parameter to know. Output rise and fall times may also be important. Unlike TTL type logic families HC specifies these in the data sheet. High-speed CMOS outputs were designed to have typically symmetrical rise and fall times. Output rise and fall time variations track very closely the propagation delay variations over temperature and supply. *Figure 9* plots rise and fall time against output load at $V_{CC}=5V$ and at room temperature. Load variation of the transition time is twice the delay variation because delays are measured at halfway points on the waveform transition.

Setup times and pulse width performance under different conditions may be necessary when using clocked logic circuits. These parameters are indirect measurements of internal propagation delays. Thus they exhibit the similar temperature and supply dependence as propagation delays. They are, however, independent of output load conditions.

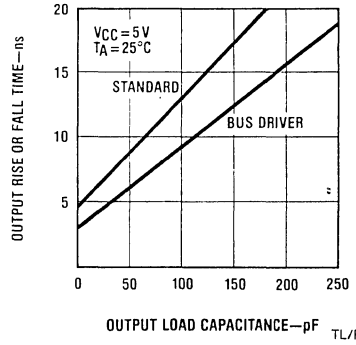


FIGURE 9. Typical Output Rise or Fall Time Vs. Load For Standard and Bus Driver Outputs

Input Rise and Fall Times

Another speed consideration, though not directly related to propagation delays, is input rise and fall time. As with other high-speed logic families and also CD4000B and 54C/74C CMOS, slow input rise and fall times on input signals can cause logic problems.

Typically, small signal gains for a MM54HC/MM74HC gate is greater than 1000 and, if input signals spend appreciable time between logic states, noise on the input or power supply will cause the output to oscillate during this transition. This oscillation could cause logic errors in the user's circuit as well as dissipate extra power unnecessarily. For this reason MM54HC/MM74HC data sheets recommend that input rise and fall times be shorter than 500 ns at $V_{CC}=4.5V$.

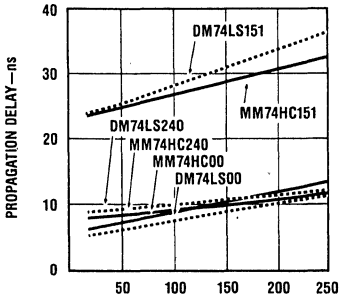
Flip-flops and other clocked circuits also should have their input rise and fall times faster than 500 ns at $V_{CC}=4.5V$. If clock input rise and fall times become too long, system noise can generate internal oscillations, causing the internal flip-flops to toggle on the wrong external clock edge. Even if no noise were present, internal clock skew caused by slow rise times could cause the logic to malfunction.

If long rise and fall times are unavoidable, Schmitt triggers ('HC14/'HC132) or other special devices that employ Schmitt trigger circuits should be used to speed up these input signals.

Logic Family Performance Comparison

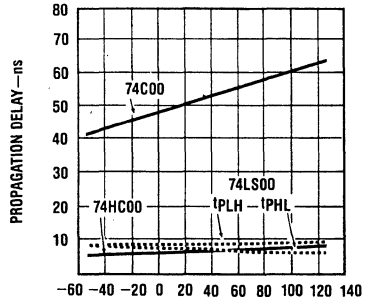
To obtain a better feeling of how high-speed CMOS compares to bipolar and other CMOS logic families, *Figure 10* plots MM54HC/MM74HC, 54LS/74LS and CD4000B logic device speeds versus output loading. HC-CMOS propagation delay and delay variation with load is nearly the same as LSTTL and about ten times faster than metal-gate CMOS. Utilizing a silicon-gate process enables achievement of LSTTL speeds, and the large output drive of this family enables the variation with loading to be nearly the same as LSTTL as well.

When comparing to CD4000 operating at 5V, HC-CMOS is typically ten times faster, and about three times faster than CD4000 logic operating at 15V. This is shown in *Figure 11.*



TL/F/5067–14

FIGURE 10. Comparison of LSTTL and High-Speed CMOS Delays



TL/F/5067–16

FIGURE 12. Comparison of HC-CMOS, Metal-Gate CMOS, and LSTTL Propagation Delay Vs. Temperature

At 5V CD4000 has about a tenth the output drive of MM54HC/MM74HC and as seen in *Figure 10*, the capacitive delay variation is much larger.

As shown in *Figure 12*, the temperature variation of HC-CMOS is similar to CD4000. This is due to the same physical phenomenon in both families. The 54LS/74LS logic family has a very different temperature variation, which is due to different circuit parameter variations. One advantage to CMOS is that its temperature variation is predictable, but with LSTTL, sometimes the speed increases and other times speed decreases with temperature.

The inherent symmetry of MM54HC/MM74HC's logic levels and rise and fall times tends to make high to low and low to high propagation delay very similar, thus making these parts easy to use.

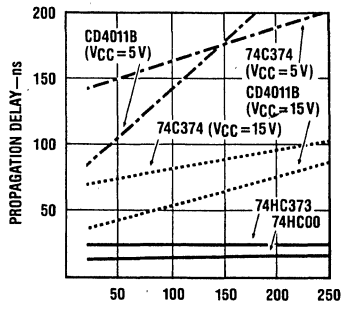


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FIGURE 11. Comparison of Metal-Gate CMOS and High-Speed CMOS Delays

Conclusion

High-speed CMOS circuits are speed compatible with 54LS/74LS circuits, not only on the data sheets, but even driving different loads. In general, HC-CMOS provides a large improvement in performance over older metal-gate CMOS.

By using some of the equations and curves detailed here, along with data sheet specifications, the designer can very closely estimate the performance of any MM54HC/MM74HC device. Even though the above examples illustrate typical performance calculations, a more conservative design can be implemented by more conservatively estimating various constants and using worst case data sheet limits. It is also possible to estimate the fastest propagation delays by using speeds about 0.4–0.7 times the data sheet typicals and aggressively estimating the various constants.

Comparison of MM54HC/MM74HC to 54LS/74LS, 54S/74S and 54ALS/74ALS Logic

National Semiconductor
Application Note 319
Larry Wakeman
June 1983

The MM54HC/MM74HC family of high speed logic components provides a combination of speed and power characteristics that is not duplicated by bipolar logic families or any other CMOS family. This CMOS family has operating speeds similar to low power Schottky (54LS/74LS) technology. MM54HC/MM74HC is approximately half as fast (delays are twice as long) as the 54ALS/74ALS and 54S/74S logic. Compared to CD4000 and 54C/74C, this is an order of magnitude improvement in speed, which is achieved by utilizing an advanced 3.5 micron silicon gate-recessed oxide CMOS process. The MM54HC/MM74HC components are designed to retain all the advantages of older metal gate CMOS, plus provide the speeds required by today's high speed systems.

Another key advantage of the MM54HC/MM74HC family is that it provides the functions and pin outs of the popular 54LS/74LS series logic components. Many functions which are unique to the CD4000 metal gate CMOS family have also been implemented in this high speed technology. In addition, the MM54HC/MM74HC family contains several special functions not previously implemented in CD4000 or 54LS/74LS.

Although the functions and the speeds are the same as 54LS/74LS, some of the electrical characteristics are different from either LS-TTL, S-TTL or ALS-TTL. The following discusses these differences and highlights the advantages and disadvantages of high speed CMOS.

AC PERFORMANCE

As mentioned previously, the MM54HC/MM74HC logic family has been designed to have speeds equivalent to LS-TTL, and to be 8–10 times faster than CD4000B and MM54C/MM74C logic. Table I compares high speed CMOS to the bipolar logic families. HC-CMOS gate delays are typically the same as LS-TTL, and ALS-TTL is two to three times faster. S-TTL is also about twice as fast as HC-CMOS. Flip-flop and counter speeds also follow the same pattern.

Also, HC logic's propagation delay variation due to changes in capacitive loading is very similar to LS-TTL. *Figure 1* illustrates this by plotting delay versus loading for the various bipolar logic families and MM54HC/MM74HC. HC-CMOS has virtually the same speed and load-delay variation as

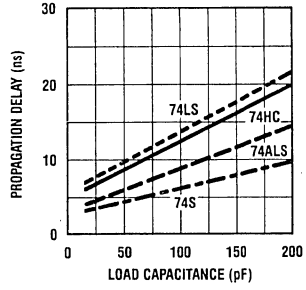

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FIGURE 1. HC, LS, ALS, S Comparison of Propagation Delay vs Load for a NAND Gate

TABLE I. COMPARISON OF TYPICAL AC PERFORMANCE OF LS-TTL, S-TTL, ALS-TTL AND HC-CMOS

Gates		LS-TTL	ALS-TTL	HC-CMOS	S-TTL	Units
74XX00	Propagation Delay	8	5	8	4	ns
74XX04	Propagation Delay	8	4	8	3	ns
Combinational MSI						
74XX139	Propagation Delay					
	Select	25	8	25	8	ns
	Enable	21	8	20	7	ns
74XX151	Propagation Delay					
	Address	27	8	26	12	ns
	Strobe	26	7	17	12	ns
74XX240	Propagation Delay	12	3	10	5	ns
	Enable/Disable Time	20	7	17	10	ns
Clocked MSI						
74XX174	Propagation Delay	20	7	18	13	ns
	Operating Frequency	40	50	50	100	MHz
74XX374	Propagation Delay	19	7	16	11	ns
	Enable/Disable Time	21	9	17	11	ns
	Operating Frequency	50	50	50	100	MHz

LS-TTL and, as is expected, is slower than ALS and S-TTL logic. The slopes of these lines indicate the amount of variation in speed with loading, and are dependent on the output impedance of the particular logic gate. The delay variation of LS-TTL and HC-CMOS is similar whereas ALS-TTL and S-TTL have slightly less variation.

POWER DISSIPATION

CD4000B and MM54C/MM74C CMOS devices are well known for extremely low quiescent power dissipation, and high speed CMOS retains this feature. Table II compares typical HC static power consumption with LS, ALS and S-TTL. Even CMOS MSI dissipation is well below 1 μW while LS-TTL dissipation is many milliwatts. This makes MM54HC/MM74HC ideal for battery operated or ultra-low power systems where the system may be put to "sleep" by shutting off the system clock.

TABLE II. COMPARISON OF TYPICAL QUIESCENT SUPPLY CURRENT FOR VARIOUS LOGIC FAMILIES

	HC-CMOS	LS-TTL	ALS-TTL	S-TTL
SSI	0.0025 μW	5.0 mW	2.0 mW	75 mW
Flip-Flop	0.005 μW	20.0 mW	10 mW	150 mW
MSI	0.25 μW	90 mW	40 mW	470 mW

CMOS dissipation increases proportionately with operating frequency. Doubling the operating frequency doubles the current consumption. This is due to currents generated by charging internal and load capacitances. *Figure 2* shows power dissipation versus frequency for a completely unloaded NAND gate, flip-flop and counter implemented in all 4 technologies.

The LS, S and ALS curves are essentially flat because the quiescent currents mask out capacitive effects, except at very high frequencies. Capacitive effects are slightly lower for the TTL families, so that, at high frequencies, CMOS dissipation may actually be more than ALS and LS. However, the power crossover frequency is usually well above the maximum operating frequency of MM54HC/MM74HC.

The previously mentioned curves plot unloaded circuits. When considering typical system power consumption, capacitive loading should also be considered. Table III lists components to implement all the support logic for a small microprocessor based system. By assuming a typical load capacitance of 50 pF, the power dissipation for these devices can be calculated at various average system clock frequencies. *Figure 3* plots power consumption for 74HC, 74LS, 74ALS and 74S logic implementations. Above 1 MHz, capacitive currents now also tend to dominate bipolar power dissipation as well.

TABLE III. HYPOTHETICAL "GLUE" LOGIC FOR A TYPICAL MICROPROCESSOR SYSTEM

System Components	# of ICs
Address Decoders ('138)	10
Address Comparators ('688)	5
Address/Data Buffers ('240/4)	10
Address/Data Latches ('373/4)	20
MSI Control/Gating ('00, '10)	30
Misc. Counter/Shift Reg ('161, '164)	20
Flip-Flops ('73/4)	10

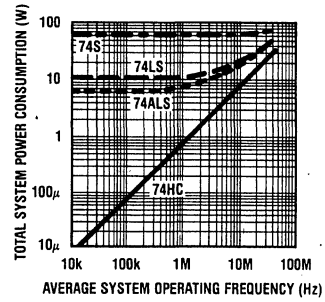

FIGURE 3. Power Consumption for Hypothetical Microprocessor System Support Logic

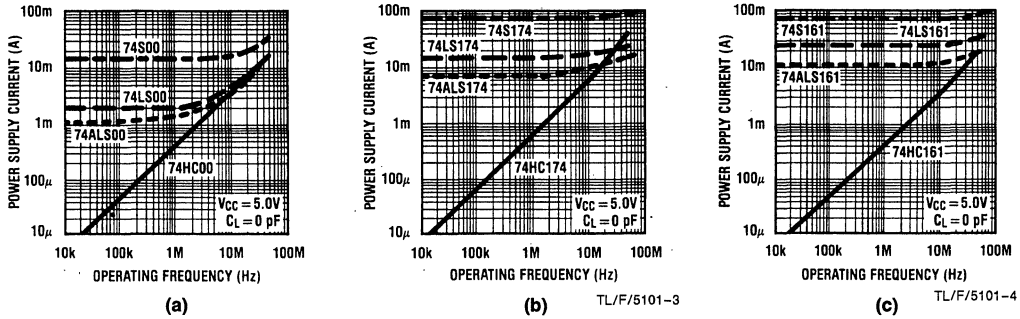

FIGURE 2. Supply Current Consumption Comparison for (a) 74XX00 (b) 74XX714 (c) 74XX161 Circuits

Since, in a typical system, some sections will operate at a high frequency and other parts at lower frequencies, the average system clock frequency is a simplification. For example, a 10 MHz microprocessor will have a bus cycle frequency of 2 to 5 MHz. Most system and memory components will be accessed a small amount of the time, resulting in effective clock frequencies on the order of 100 kHz for these sections. Thus, the average system clock frequency would be around 1 to 2 MHz, and an 8 to 1 power savings would be realized by using CMOS.

Another simplification was made to calculate system power. CMOS circuits will dissipate much less power when TRI-STATE®, which would save much power since, in a given bus cycle, only a few buffers will be enabled. LS, ALS and S, however, actually dissipate more power when their outputs are disabled.

Several interesting conclusions can be drawn from *Figure 3*. First, notice that, at higher frequencies, the bipolar logic families start to dissipate more power. This is a result of current consumption due to switching the load. As the operating frequency approaches infinity, this will be the dominant effect. So, for extremely fast low power systems, minimizing load capacitance and overall operating frequency becomes more important. As lower power TTL logic is introduced, system power will be increasingly dependent on capacitive load effects similar to CMOS.

Second, TTL logic has a slightly smaller logic voltage swing than CMOS. Thus, for a given load, TTL will actually have a lower average load current. So, similar to the unloaded example, at very high frequencies, CMOS could consume more power than TTL. As *Figure 5* indicates, these frequencies are usually far above the 30 MHz limit of HC-CMOS or LS-TTL.

INPUT VOLTAGE CHARACTERISTICS AND NOISE IMMUNITY

To maintain the advantage CMOS has in noise immunity, the input logic levels are defined to be similar to metal gate CMOS. At $V_{CC}=5V$, MM54HC/MM74HC is designed to have input voltages of $V_{IH}=3.5V$ and $V_{IL}=1.0V$. Additionally, input voltage over the operating supply voltage range is: $V_{IH}=0.7V_{CC}$ and $V_{IL}=0.2V_{CC}$. This compares to $V_{IH}=2.0V$ and $V_{IL}=0.8V$ specified for LS-TTL over its supply range. *Figure 4* illustrates the input voltage differences, and the greater noise immunity HC logic has over its supply range. Maintaining wide noise immunity gives HC-CMOS an advantage in many industrial, automotive, and computer applications where high noise levels exist.

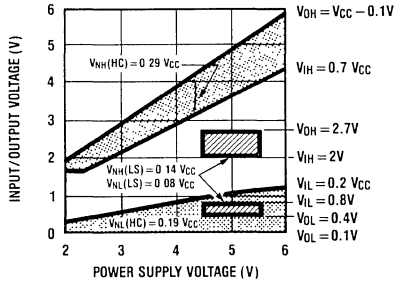

FIGURE 4. Worst-Case Input and Output Voltages Over Operating Supply Range for HC and LS Logic

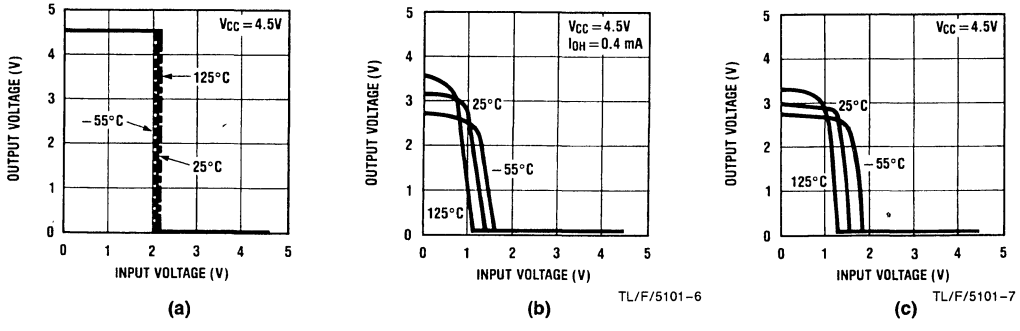

FIGURE 5. Input-Output Transfer Characteristics for 74XX00 NAND Gate Implemented in (a) HC-CMOS (b) LS-TTL (c) ALS-TTL

Another indication of DC noise immunity is the typical transfer characteristics for the logic families. *Figure 5* shows the transfer function of the 74XX00 NAND gate for HC-CMOS, LS-TTL and ALS-TTL. High speed CMOS has a very sharp transition typically at 2.25V, and this transition point is very stable over temperature. The bipolar logic transfer functions are not as sharp and vary several hundred millivolts over temperature. This sharp transition is due to the large circuit gains provided by triple buffering the HC-CMOS gate compared to the single bipolar gain stage. *Figure 6* compares the transfer function of the 'HC08 and the 'ALS08, both of which are double buffered. The 'ALS08 has a sharper transition, but the CMOS gate still has less temperature variation and a more centered trip point. However, the TTL trip point is not dependent on V_{CC} variation as CMOS is.

The high speed CMOS input levels are not totally compatible with TTL output voltage specifications. To make them compatible would compromise noise immunity, die size, and significant speed. The designer may improve compatibility by adding a pull-up resistor to the TTL output. He may also utilize a series of TTL-to-CMOS level converters which are being provided to ease design of mixed HC/LS/ALS/S systems. These buffers have 0.8V and 2.0V TTL input voltage specifications, and provide CMOS compatible outputs. When mixing logic, the noise immunity at the TTL to CMOS interface is no better than LS-TTL, but a substantial savings in power will occur when using MM54HC/MM74HC logic.

INPUT CURRENT

The HC family maintains the ultra-low input currents typical of CMOS circuits. This current is less than 1 μA and is caused by input protection diode leakages. This compares to the much larger LS-TTL input currents of 0.4 mA for a low input and 40 μA for a high input. ALS-TTL input currents are 0.2 mA and 20 μA and S-TTL input currents are 3.2 mA and 100 μA. *Figure 7* tabulates these values. The near zero input current of CMOS eases designing, since a typical input can be viewed as an open circuit. This eliminates the need for fanout restrictions which are necessary in TTL logic designs.

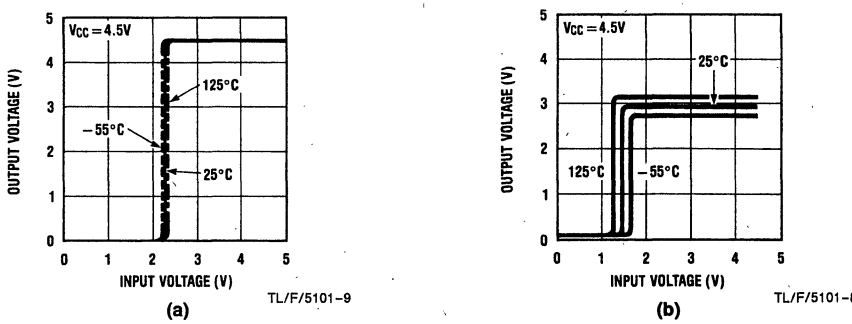

FIGURE 6. Input-Output Transfer Characteristics for 74XX08 AND Gate Implemented in (a) HC-CMOS (b) ALS-TTL

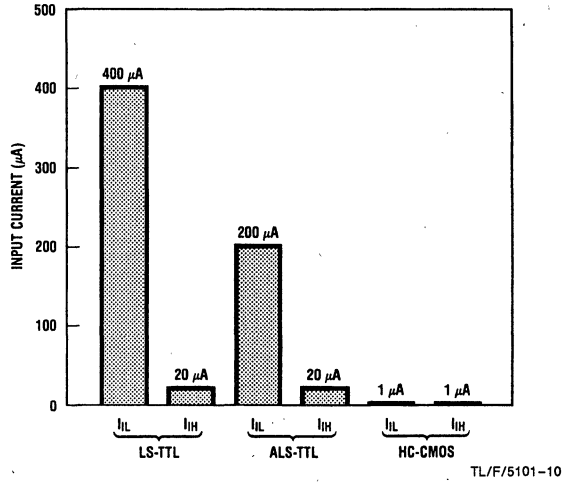

FIGURE 7. Comparison of Input Current Specifications for Various Logic Families

POWER SUPPLY RANGE

Figure 4 also compares the supply range of MM54HC/MM74HC logic and LS-TTL. The high speed CMOS family is specified to operate at voltages from 2V to 6V. 54LS, 54S and 54ALS logic is specified to operate from 4.5V to 5.5V, and 74LS and 74S will operate from 4.75V to 5.25V. 74ALS is specified over a 4.5V to 5.5V supply range. This wider operating range for the HC family eases power supply design by eliminating costly regulators and enhances battery operation capabilities.

OUTPUT DRIVE

Since there was no speed, noise immunity, or power tradeoff, standard HC-CMOS was designed to have similar high current output drive that is characteristic of LS-TTL and ALS-TTL. Schottky TTL has about 5 times the output drive of MM54HC/MM74HC. Thus HC-CMOS has an output low current specification of 4 mA at an output voltage of 0.4V. In keeping with CD4000B series and 54C/74C series logic, the source and sink currents are symmetrical. Thus HC logic can source 4 mA as well. This large increase in output current for high speed CMOS over CD4000B also has the added advantage of reducing signal line crosstalk which can be of greater concern in high speed systems. *Figure 8* compares HC, LS, and ALS specified output currents.

Since TTL logic families do have significant input currents they have a limited fanout capability. Table IV illustrates the limitations of these families, based on their input and output currents. High speed CMOS is also included. MM54HC/MM74HC has the same CMOS-to-CMOS fanout characteristics as CD4000B, virtually infinite.

TABLE IV. FANOUT OF HC-CMOS, LS-TTL, ALS-TTL, S-TTL

From, To	74HC	74LS	74ALS	74S
74HC	4000	10	20	2
74LS	*	20	40	4
74ALS	*	20	40	4
74S	*	50	100	10

As another indication of the similarity of HC-CMOS to LS-TTL, *Figure 9* plots typical output currents versus output voltage for LS and HC. The output sink current curves are very similar, but LS source current is somewhat different, due to its emitter-follower output circuitry.

MM54HC/MM74HC bus driving circuits, namely the TRI-STATE buffers and latches, have half again as much output current drive as standard outputs. These components have a 6 mA output drive. The 6 mA was chosen based on a trade-off of die size and speed-load variations. This current is less than the 12 mA or more specified for LS and ALS bus driver circuits, because the bus fanout limitations of these families do not apply in CMOS systems. S-TTL bus output sink current is 48 mA.

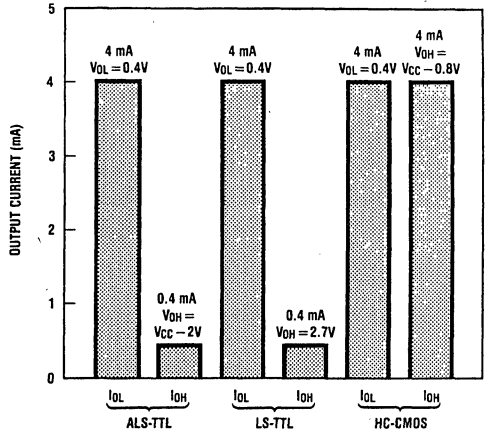

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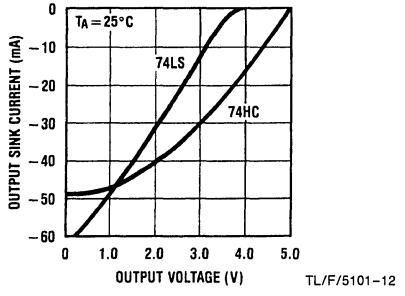
FIGURE 8. Output Current Specifications for ALS-TTL, S-TTL and HC-CMOS



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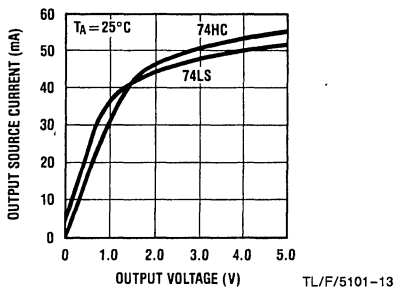
(a)



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(b)

FIGURE 9. Comparison of Standard LS-TTL and HC-CMOS Output (a) Source (b) Sink Currents

OPERATING TEMPERATURE RANGE

The operating temperature range and temperature effects on various HC-CMOS operating parameters differ from bipolar logic. The recommended temperature range for 74LS, 74S, and 74ALS is 0°C to 70°C, compared to −40°C to 85°C for the 74HC family. 54 series logic is specified from −55°C to 125°C for all four families.

Temperature variation of operating parameters for the MM54HC/MM74HC family behaves very predictably and is due to the gain decreasing of MOSFET transistors as temperature is increased. Thus the output currents decrease and propagation delays increase at about 0.3% per degree centigrade.

Figure 10 shows typical propagation delays for the 74XX00 over the −55°C to +125°C temperature range. The 'HC00's speed increases almost linearly with temperature, whereas the LS and ALS behave differently.

A WORD ABOUT PLUG-IN REPLACEMENT OF TTL

MM54HC/MM74HC logic implements TTL equivalent functions with the same pin outs as TTL. HC is not designed to be directly plug-in replaceable, but, with some care, some TTL systems can be converted to MM54HC/MM74HC with little or no modification. The replaceability of HC is determined by several factors.

One factor is the difference in input levels. In systems where all TTL is not being replaced and TTL outputs feed CMOS inputs, the input high voltages, as specified, are not totally compatible. Although TTL outputs will typically drive HC inputs correctly, an external pull-up resistor should be added to the TTL outputs, or an MM54HCT/MM74HCT TTL compatible circuit should be used. This incompatibility tends to limit the designer's ability to intermingle TTL and HC-CMOS. Note, though, that HC outputs are completely compatible with the various TTL family's input specifications; therefore, there is no problem when HC is driving TTL.

Another source of possible problems can occur when the LS design floats device inputs. This practice is not recommended when using LS-TTL, but it is sometimes done. Usually, TTL inputs float high; however, CMOS inputs may float either high or low depending on the static charge on the input. It is therefore important to always tie unused CMOS inputs to either V_{CC} or ground to avoid incorrect logic functioning.

A third factor to consider when replacing any TTL logic is AC performance. The logic functions provided by 54HC/74HC are equivalent to LS-TTL, and the propagation delay, set-up and hold times are similar to LS. However, there are some differences in the way CMOS circuits are implemented which will cause differences in speed. For the most part, these differences are minor, but it is important to verify that they do not affect the design.

CONCLUSION

The MM54HC/MM74HC family represents a major step forward in CMOS performance. It is a full line family capable of being designed into virtually any application which now uses LS-TTL with substantial improvement in power consumption. ALS and S-TTL primarily offer faster speeds than HC-CMOS, but still do not have the input and output advantages or the lower power consumption of CMOS. Because of its high input impedance and large output drive, HC logic is actually easier to use. This, coupled with continued expansion of the 54HC/74HC, will make it an increasingly popular logic family.

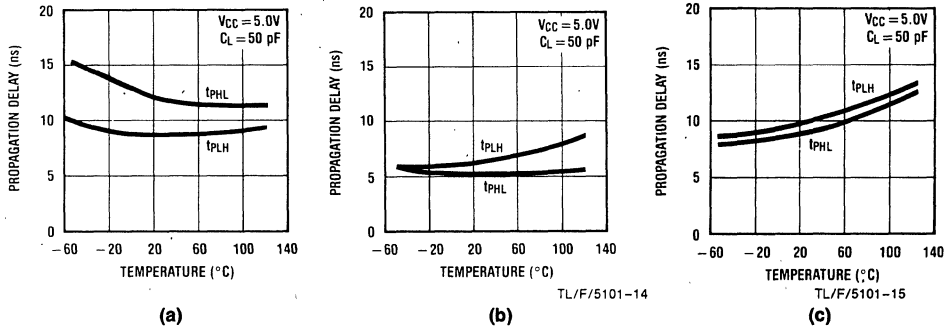


FIGURE 10. Propagation Delay Variation Across Temperature for (a) 74LS00 (b) 74ALS00 and (c) 74HC00

National's Process Enhancements Eliminate the CMOS SCR Latch-Up Problem In 54HC/74HC Logic

National Semiconductor
Application Note 339
Larry Wakeman

INTRODUCTION

SCR latch-up is a parasitic phenomena that has existed in circuits fabricated using bulk silicon CMOS technologies. The latch-up mechanism, once triggered, turns on a parasitic SCR internal to CMOS circuits which essentially shorts V_{CC} to ground. This generally destroys the CMOS IC or at the very least causes the system to malfunction. In order to make MM54HC/MM74HC high speed CMOS logic easy to use and reliable it is very important to eliminate latch-up. This has been accomplished through several layout and process enhancements. It is primarily several proprietary innovations in CMOS processing that eliminates the SCR.

First, what is "SCR latch-up?" It is a phenomena common to most monolithic CMOS processes, which involves "turning on" a four layer thyristor structure (P-N-P-N) that appears from V_{CC} to ground. This structure is formed by the parasitic substrate interconnections of various circuit diffusions. It most commonly can be turned on by applying a voltage greater than V_{CC} or less than ground any input or output, which forward biases the input or output protection diodes. *Figure 1* schematically illustrates these diodes found in the MM54HC/MM74HC family. Standard CD4000 and MM54C/MM74C logic also has a very similar structure. These diodes can act as the gate to the parasitic SCR, and if enough current flows the SCR will trigger. A second method of turning on the SCR is to apply a very large supply voltage across the device. This will breakdown internal diodes causing enough current to flow to trigger latch up. In HC logic the typical V_{CC} breakdown voltage is above 10V so this method is more uncommon. In either case, once the SCR is turned on a large current will flow from V_{CC} to ground, causing the CMOS circuit to malfunction and possibly damage itself.

CMOS SCR problems can be minimized by proper system design techniques or added external protection circuits, but obviously the reduction or elimination of latch up in the IC itself would ease CMOS system design, increase system reliability and eliminate additional circuitry. For this reason it was important to eliminate this phenomena in National's high speed CMOS logic family.

Characterization of this proprietary high speed CMOS process for latch up has verified the elimination of this parasitic mechanism. In tests conducted under worst case conditions (V_{CC}=8V and T_A=125°C) it has been impossible to latch-up these devices on the inputs or on the outputs.

In testing for latch up, caution must be exercised when trying to force large currents into an IC. As with any integrated circuit there are maximum limitations to the current handling capabilities of the internal metalization, and diodes, and thus they can be damaged by excessive currents. This is discussed later in the test section.

To enable the user to understand what latch up is and how it has been eliminated, it is useful to review the operating of a simple discrete SCR, and then apply this to the CMOS SCR. Since most latch up problems historically have been caused by extraneous noise and system transients, the AC characteristics of CMOS latch are presented. Also various methods of external and internal protection against latch up is discussed as well as example test methods for determining the latch up susceptibility of CMOS IC's.

SIMPLE DISCRETE SCR OPERATION

To understand the behavior of the SCR structure parasitic to CMOS IC's, it is first useful to review the basic static operation of the discrete SCR, and then apply it to the CMOS SCR. There are two basic trigger methods for this SCR. One is turning on the SCR by forcing current into its gate, and the second is by placing a large voltage across its anode and cathode. *Figure 2* shows the basic four layer structure biased into its forward blocking state. The SCR action can be more easily understood if this device is modeled as a cross coupled PNP and NPN transistor as shown in *Figure 3*.

In the case of latch up caused by forward biasing a diode, if current is injected into the base of Q2, this transistor turns on, and a collector current beta times its base current flows into the base of Q1. Q1 in turn amplifies this current by beta and feeds it back into the base of Q2, where the current is again amplified. If the product of the two transistors' Beta becomes greater than one, B(NPN)xB(PNP)>1, this current multiplication continues until the transistors saturate, and the SCR is triggered. Once the regenerative action occurs a large anode current flows, and the SCR will remain on even after the gate current is removed, if enough anode current flows to sustain latch up. However, if the transistor current gains are small no self sustaining positive feedback will occur, and when the base current is removed the collector current will stop. In a similar manner the SCR can be triggered by drawing current by forward biasing the base of Q1.

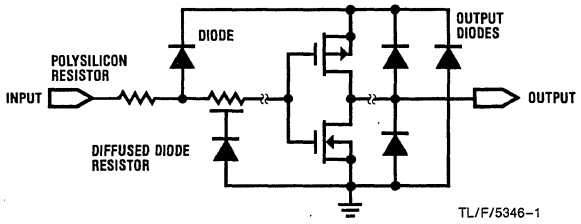


FIGURE 1. Schematic Diagram of Input and Output Protection Structures

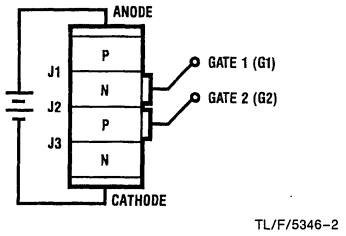
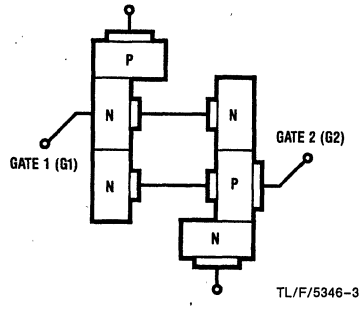


FIGURE 2. Simplified SCR Structure



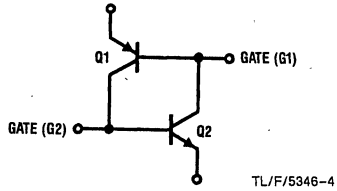


FIGURE 3. Cross-Coupled Transistor Model of SCR

The second case, the SCR may also be triggered without injecting any gate current. In the forward blocking state the small leakage current that is present does not trigger the SCR, but if the voltage is increased to a point where significant leakage currents start conducting, these currents could also trigger the SCR, again forming a low impedance path through the device. The same requirement that the Beta product of the PNP and NPN be greater than one in order for the SCR to trigger applies here as well. This leakage current trigger is characteristic of Schottkey diode operation.

THE CMOS SCR: STATIC DC OPERATION

For discussion purposes CMOS SCR latch up characteristics can be divided into two areas. One is the basic operation of the SCR when static DC voltages are applied, and the second is the behavior when transients or pulses are applied.

First looking at the device statically, the parasitic SCR in CMOS integrated circuits is much more complex and its triggering is somewhat different than the simple SCR already discussed. However, the regenerative feedback effect is basically the same. *Figure 4a* shows a simplified P− well CMOS structure illustrating only the diffusions and the resultant parasitic transistors. The NPN transistor is a vertical device whose emitter is formed by n+ diffusions. The P− well forms the base and the N− substrate forms the collector of the NPN. The PNP transistor is a lateral device. Its emitter is formed by p+ diffusions, its base is the N− substrate, and its collector is the P− well.

Figure 4b illustrates a cross section of a simplified N− well process and its corresponding parasitic bipolar transistors. In this process the NPN is a lateral device and the PNP is vertical. Essentially the description of the P− well SCR is the same as the N− well version except the NPN is a low gain lateral device and the PNP is a high gain vertical transistor. Thus the following discussion for the P− well also applies to the N− well with this exception.

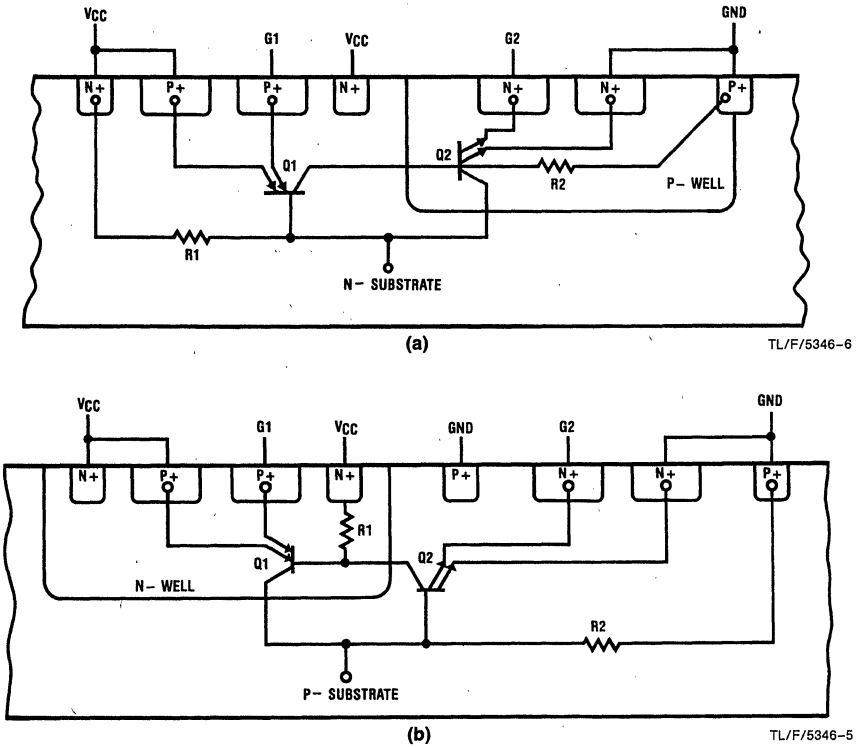


FIGURE 4. Simplified Cross Section of CMOS Processes a) P− well and b) N− well

The transistors for the P− well CMOS process are drawn schematically in *Figure 5*, so that their cross coupled interconnection is more easily seen. The SCR structure in *Figure 5* differs from that of *Figure 3* in two ways. First, the transistors of *Figure 5* have multiple emitters, due to the many diffusions on a typical die. One emitter of each transistor could function as the trigger input to the SCR. Secondly, R1 and R2 have been added and are due to P− and N− substrate resistances between the base of each transistor and the substrate power supply contacts.

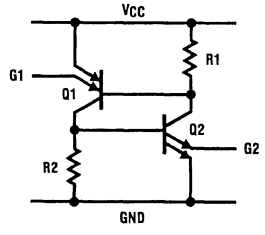


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FIGURE 5. Schematic of Simple SCR Model

Like the discrete SCR there are two basic methods of turning the CMOS SCR on. The first method is however slightly different. In the CMOS parasitic SCR current cannot be directly injected into the base of one of its transistors. Instead either node G1 must be raised above V_{CC} enough to turn on Q1, or node G2 must be lowered below ground enough to turn on Q2. If G1 is brought above V_{CC}, current is injected from the emitter of Q1 and is swept to the collector of Q1. The collector of Q1 feeds the base of Q2 and also R2. R2 has the effect of stealing current from the base of Q2, but as current flows through R2 a voltage will appear at the base of Q2. Once this voltage reaches 0.6 volts Q2 will turn on and feed current from its collector back into R1 and into Q1. If 0.6 volts is generated across R1, Q1 then turns on even more.

Again, if the two transistors have enough gain and enough anode current flows to sustain the SCR, it will turn on, and remain on even after G1 is returned to V_{CC}. The actual requirements for latch up are altered by the two resistors, R1 and R2. Since the resistors shunt some current away from the base of both transistors, the resistors essentially reduce the effective gains of the transistors. Thus the transistors must actually have much higher gains in order to achieve an overall SCR loop gain greater than one, and hence enable the SCR to trigger. The actual equations to show quantitatively how the resistors effect the SCR's behavior could be derived, but it is sufficient to notice that as R1 and R2 become smaller the SCR becomes harder to turn on. IC designers utilize this to reduce latch up.

The second method of turning on the SCR mentioned earlier also applies here. If the supply voltage is raised to a large value, and internal substrate diodes start breaking down excessive leakage currents will flow possibly triggering the SCR. The resistors also affect this trigger method as well, since they steal some of the leakage currents from Q1 and Q2, and hence it takes more current to trigger the SCR. In high speed CMOS the process enhancements reduce the transistor betas and hence eliminate latch up by this mechanism as well.

While useful, the SCR model of *Figures 4 and 5* is very simplified, since in actuality the CMOS SCR is a structure with many transistors interconnected by many resistances. Although still somewhat simiplified, *Figure 6* attempts to illustrate how the parasitics on a chip connect. It is important to remember that any transistor or diode diffusion can parasitically form part of the SCR. In the figure transistor Q1 and Q2 are single emitter transistors formed by the input protection diodes. Internal P and N channel transistors have no external connection and are represented by Q3 and Q4. Q5 and Q6 represent output transistor diffusions, and the second emitter corresponds to the output. All of these transistors are connected together by the N− substrate and P− well resistances, which are illustrated by the resistor mesh.

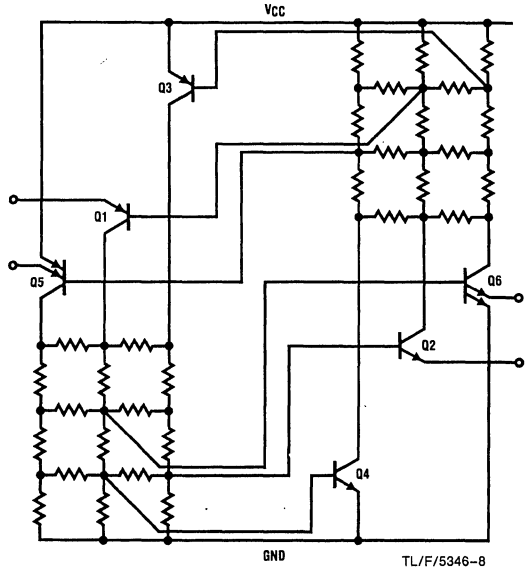

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FIGURE 6. Distributed Model of CMOS SCR

If any of the emitters associated with the trigger inputs G1–G4 become forward biased the SCR may be triggered. Also due to the intertwined nature of this structure, part of the SCR may be initially latched up. In this case only a limited amount of current may flow, but this limited latch up may spread and cause other parts to be triggered until eventually the whole chip is involved.

In general the trigger to the SCR has been conceptualized as a current, since ideally the CMOS input looks into the base of the SCR transistors. However this may not be quite true. There may be some resistance in series with each base, due to substrate or input protection resistances. In newer silicon gate CMOS processes, MM54HC/MM74HC for example, a poly-silicon resistor is used for electrostatic protection, and this enables larger voltages to be applied to the circuit pins without causing latchup. This is because the poly resistor actually forms a current limit resistor in series with the diodes. In most applications the designer is more concerned with accidental application of a large voltage, and the use of the poly resistor internally enables good voltage resistance to latch up. CMOS outputs are directly connected to parasitic output diodes since no poly resistor can be placed on an output without degrading output current drive. Thus the output latch up mechanism is usually thought of as a current.

Temperature variations will affect the amount of current required to trigger the SCR. This is readily understandable since temperature effects the bipolar transistor's gain and the resistance of the base-emitter resistors. Generally, as the temperature is increased less current is needed to cause latch-up. This is because as temperature increases the bipolar transistor's base-emitter voltage decreases and the base-emitter resistor value increases. *Figure 7* plots trigger current versus temperature for a sensitive CMOS input. This data was taken on a CMOS device without any layout or process enhancements to eliminate latch up. Increasing temperature from room to 125°C will reduce the trigger current by about a factor of three. Once the circuit is latched up, heating of the device die caused by SCR currents will actually increase the susceptibility to repeated latch up.

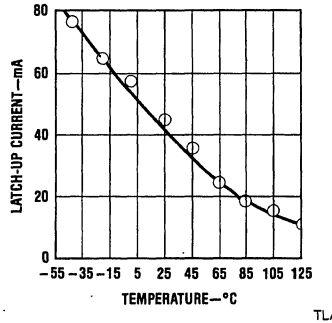

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FIGURE 7. Temperature versus SCR Trigger Current for Special CMOS Test Structure

OTHER LATCH UP TRIGGER METHODS

There are some other methods of latching up CMOS circuits, they are not as circuit design related and shall only be briefly mentioned. The first is latch up due to radiation bombardment. In hostile environments energetic atomic particals can bombard a CMOS die freeing carriers in the substrate. These carriers then can cause the SCR to trigger. This can be of concern in high radiation environments which call for some sort of radiation hardened CMOS logic.

Another latch up mechanism is the application of a fast rise or fall spike to the supply inputs of a CMOS device. Even if insufficient current is injected into the circuit the fast voltage change could trigger latch up. This occurs because the voltage change across the part changes the junction depletion capacitances, and this change in capacitance theoretically could cause a current that would trigger the SCR latch. In actual practice this is very difficult to do because the response time of the SCR (discussed shortly) is very poor. This is hardly a problem since power supplies must be adequately decoupled anyway.

A third latch up cause which is completely internal to the IC itself and is out of the control of the system designer is internally triggered latch up. Any internal switching node connects to a diode diffusion, and as these diffusions switch the junction depletion capacitance associated with these nodes changes causing a current to be generated. This current could trigger the SCR. The poor frequency response of the SCR tends to make this difficult, but as chip geometries are shrunk packing densities will increase and the gain of the lateral PNP transistor increase. This may increase the latch up susceptibility. It is up to the IC designer to ensure that this doesn't happen, and care in the layout and circuit design of 54HC/74HC logic has ensured that this will be avoided.

THE CMOS SCR: TRANSIENT BEHAVIOR

With the introduction of fast CMOS logic the transient nature of the CMOS SCR phenomena becomes more important because signal line ringing and power supply transients are more prevalent in these systems. Older metal gate CMOS (CD4000 & 74HC) circuits have slow rise and fall times which do not cause a large amount of line ringing. Power supply spiking is also somewhat less, again due to slow switching times associated with these circuits.

The previous discussion assumed that the trigger to the CMOS SCR was essentially static and was a fixed current. Under these conditions a certain value current will cause the SCR to trigger, but if the trigger is a short pulse the peak value of the pulse current that will trigger the SCR can be much larger than the static DC trigger current. This is due to the poor frequency characteristics of the SCR.

For short noise pulses, $<1\ \mu s$, the peak current required to latch up a device is dependent on the duty cycle of the pulses. At these speeds it is the average current that causes latch-up. For example, if a 1 MHz 50% duty cycle over voltage pulse train is applied to a device that latched with 20 mA DC current, then typically the peak current required will be about 40 mA. For a 25% duty cycle the peak current would be 80 mA. An example of this is shown in *Figure 8* which plots latch up current against over-voltage pulse width at 1 MHz.

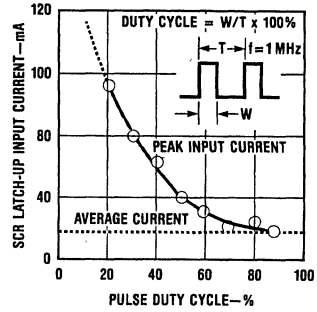

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FIGURE 8. Trigger Current of SCR of Input Overvoltage Pulses at High Repetition Rate on Special Test Unit

If the pulse widths become long, many microseconds, the latch up current will approach the DC value even for low duty cycles. This is shown in *Figure 9* which plots peak trigger current vs pulse width for the same test device used in *Figure 8*. The repetition rate in this case is a slow 2.5 kHz (period = 400 μs). These long pulse widths approach the trigger time of the SCR, and thus pulses lasting several microseconds are long enough to appear as DC voltages to the SCR. This indirectly indicates the trigger speed of the SCR to be on the order of ten to fifteen microseconds. This is however dependent on the way the IC was designed and the processing used.

In normal high speed systems noise spikes will typically be only a few nanoseconds in duration, and the average duty cycle will be small. So even a device that is not designed to

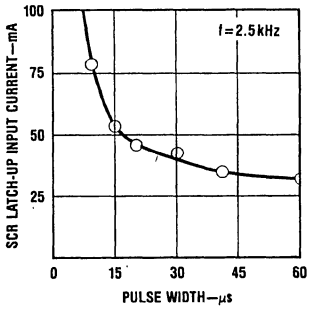

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FIGURE 9. Trigger Current of Pulse on Special Test Unit SCR for Single Transient Overvoltage

be latch up resistant, will probably not latch up even with significant line ringing on its inputs or outputs (Then again . . .) However, in some systems where inductive or other loads are used transients of several microseconds can be easily generated. For example, some possible applications are automotive and relay drivers. In other CMOS logic families spikes of this nature are much more likely to cause the SCR to trigger, but here again MM54HC/MM74HC high speed CMOS is immune.

PREVENTING SCR LATCH UP: USER SYSTEM DESIGN SOLUTIONS

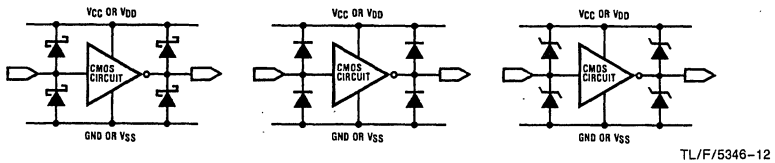
SCR latch-up can be prevented either on the system level or on the IC level. Since National's MM54HC/MM74HC series will not latch up, this eliminates the need for the system designer to worry about preventing latch up at the system level. This not only eases the design, but negates the need to add external diodes and resistors to protect the CMOS circuit, and hence additional cost. (Note however that even though the devices don't latch up, diode currents should be limited to their Absolute Maximum Ratings listed in the Data Sheets).

If one is using a CMOS device that may latch up, older CD4000 CMOS or another vendors HC for example, and its input or output voltages may forward bias the input or output diodes then some external circuitry may need to be added to eliminate possible SCR triggering. As with the previous discussions of latch-up preventing SCR latch-up falls into two categories: the static case, and the transient condition. Each is related but has some unique solutions.

In the static condition to ensure SCR latch up does not occur, the simplest solution is to design CMOS systems so that their input/output diodes don't become forward biased. To ease this requirement some special circuits that have some of their input protection diodes removed are provided, and this enables input voltages to exceed the supply range. These devices are MM54HC4049/50, CD4049/50, and MM54C901/2/3/4.

If standard logic is used and input voltages will exceed the supply range, an external network should be added that protects the device by either clamping the input voltage or by limiting the currents which flow through the internal diodes. *Figure 10* illustrates various input and output diode clamping circuits that shunt the diode currents when excessive input voltages are applied. Usually either an additional input or output diode is required, rarely both, and if the voltages only exceed one supply then only one diode is necessary. If an external silicon diode is used the current shunt is only partially effective since this diode is in parallel with the internal silicon protection diode, and both diodes clamp to about 0.7V.

A second method, limiting input current, is very effective in preventing latch-up, and several designs are shown in *Figure 11*. The simplest approach is a series input resistor. It is recommended that this resistor should be as large as possible without causing excessive speed degradation yet ensure the input current is limited to a safe value. If speed is critical, it is better to use a combination diode-resistor network as shown in *Figures 11b* and *11c*. These input networks effectively limit input currents while using lower input resistors. The series resistor may not be an ideal solution for protecting outputs because it will reduce the effective drive of the output. In most cases this is only a problem when the output must drive a lot of current or must switch large capacitances quickly.



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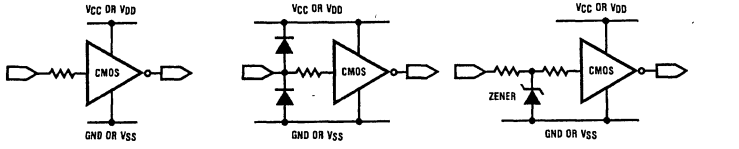
Schottkey Diodes (a) **Germainium Diodes (b)** **Zener Diodes (c)**

FIGURE 10. External Input and Output Protection Diodes Circuits for Eliminating SCR Latch-up



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(a) **(b)** **(c)**

FIGURE 11. Input Resistor and Resistor-Diode Protection Circuits for Eliminating Latch-up

A third approach is instead of placing resistors in series with the inputs to place them in series with the power supply lines as shown in *Figure 12.* The resistors must be bypassed by capacitors so that momentary switching currents don't produce large voltage transients across R1 and R2. These resistors can limit input currents but primarily they should be chosen to ensure that the supply current that can flow is less than the holding current of the SCR. Thus even though the input current can cause latch up it cannot be sustained and the IC will not be damaged.

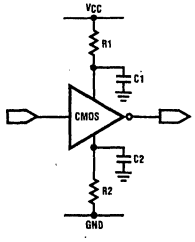

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FIGURE 12. Supply Resistor-Capacitor Circuits for Eliminating Latch-up.

This last solution has the advantage of fewer added components, but also has some disadvantages. This method may not prevent latch up unless the resistors are fairly large, but this will greatly degrade the output current drive and switching characteristics of the device. Secondly, this circuit protects the IC from damage but if diodes currents are applied causing large supply currents, the circuits will logically malfunction where as with other schemes logic malfunction can be prevented as well.

PREVENTING LATCH UP: IC DESIGN SOLUTIONS

The previous latch up solutions involve adding extra components and hence extra cost and board space. One can imagine that in a microprocessor bus system if for some reason the designer had to protect each output of several CMOS devices that are driving a 16-bit address bus that up to 32 diodes and possibly 16 resistors may need to be added. Thus for the system designer the preferable solution is to use logic that won't latch up.

Most methods previously employed to eliminate latch up are either not effective, increase the die size significantly, and/or degrade MOS transistor performance. The process enhancements employed on 54HC/74HC logic circumvent these problems. Primarily it is effective without degrading MOS performance.

When designing CMOS integrated circuits, there are many ways that the SCR action of these circuits can be reduced. One of the several methods of eliminating the SCR is to reduce the effective gain of at least one of the transistors, thus eliminating the regenerative feedback. This can be accomplished either by modifying the process and/or by inserting other parasitic structures to shunt the transistor action. Also the substrate resistances modeled as R1 and R2 in *Figures 4* and *5* can be reduced. As these resistances approach zero more and more current is required to develop enough voltage across them to turn on the transistors.

As mentioned, the current gains of the NPN and PNP parasitic transistors directly affect the current required to trigger the latch. Thus some layout and process enhancements can be implemented to reduce the NPN and PNP Betas. In a P–well process the gain of the vertical NPN is determined by the specific CMOS process, and is dependent on junction depths and doping concentrations. These parameters also control the performance of the N-MOS transistors as well and so process modification must be done without degrading CMOS performance. To reduce the gain of the vertical PNP the doping levels of the P–well can be increased. This will decrease minority carrier lifetimes. It will also reduce the subtrate resistance lowering the NPN base-emitter resistance. However this will increase parasitic junction capacitances, and may affect NMOS threshold voltages and carrier mobility. The depth of the well may be increased as well. This will reduce layout density due to increased lateral diffusion, and increase processing time as it will take longer to drive the well deeper into the substrate.

The lateral PNP's gain is determined by the spacing of input and output diode diffusions to active circuitry and minority carrier life times in the N–substrate. The carrier life times are a function of process doping levels as well, and care must be exercised to ensure no MOS transistor performance degradation. Again the doping levels of the substrate can be increased, but this will increase parasitic junction capacitances, and may alter the PMOS threshold characteristics. The spacing between input/output diodes and other

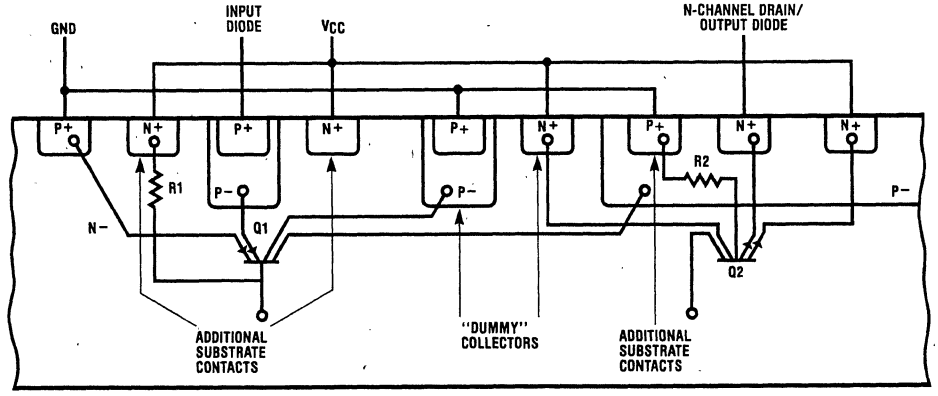

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FIGURE 13. Simplified CMOS Cross Section Showing Added Latch-up Reduction Structures

diffusions can be increased. This will increase the PNP's base width, lowering its beta. This may be done only a limited amount without significantly impacting die size and cost.

Another method for enhancing the latch-up immunity of MM54HC/MM74HC is to short out the SCR by creating additional parasitic transistors and reducing the effective substrate resistances. These techniques employ the use of ringing structures (termed guard rings) to surround inputs and outputs with diffusions that are shorted to V_{CC} or ground. These diffusions act to lower the substrate resistances, making it harder to turn on the bipolar transistors. They also act "dummy" collectors that shunt transistor action by collecting charges directly to either V_{CC} or ground, rather than through active circuitry. *Figure 13* shows a cross section of how this might look and *Figure 14* schematically illustrates how these techniques ideally modify the SCR structure.

Ideally, in *Figure 14* if the inputs are forward biased any transistor action is immediately shunted to V_{CC} or ground through the "dummy" collectors. Any current not collected will flow through the resistors, which are now much lower in value and will not allow the opposite transistor to turn on.

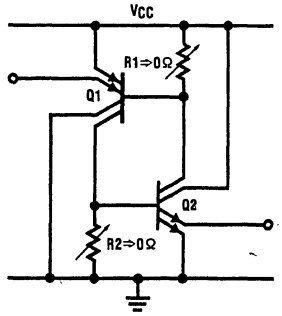

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FIGURE 14. Schematic Representation of SCR with Improvements to Reduce Turn On.

Unfortunately in order to reduce latch up these techniques add quite significantly to the die size, and still may not be completely effective.

The ineffectiveness of the ringing structures at completely eliminating latch up is for one because the collectors are only surface devices and carriers can be injected very deep into the N− substrate. Thus they can very easily go under the fairly small "dummy" collectors and be collected by the relatively large active P− well. A possible solution might be to make the collector diffusions much deeper. This suffers from the same drawbacks as making the well deeper, as well as requiring additional mask steps increasing process complexity. Secondly, the base emitter resistances can be reduced only so much, but again only the surface resistances are reduced. Some transistor action can occur under the P− well and deep in the N− bulk where these surface shorts are only partially effective.

The above discussion described modifications to a P− well process. For an N− well process the descriptions are the same except that instead of a P− well an N− well is used resulting in a vertical PNP instead of an NPN and a lateral NPN instead of a PNP.

These methods are employed in 54HC/74HC CMOS logic, but in addition processing enhancements were made that effectively eliminate the PNP transistor. The primary enhancement is a modification to the doping profile of the N− substrate (P− well process). This lowers the conductivity of the substrate material while maintaining a lightly dope surface concentration. This allows optimum performance NMOS and PMOS transistors while dramatically reducing the gain of the PNP and its base-emitter resistance. The gain of the PNP is reduced because the minority carrier lifetimes are reduced. This modification also increases the effectiveness of the "dummy" collectors by maintaining carriers closer to the surface. This then eliminates the SCR latch up mechanism.

5.0 TESTING SCR LATCH UP

There are several methods and test circuits that can be employed to test for latch up. The one primarily used to characterize the 54HC/74HC logic family is shown in *Figure 15*. This circuit utilizes several supplies and various meters to either force current into the V_{CC} diodes or force current out of the ground diodes. By controlling the input supply a current is forced into or out of an input or output of the test device. As the input supply voltage is increased the current into the diode increases. Internal transistor action may cause some supply current to flow, but this should not be considered latch up. When latch up occurs the power supply current will jump, and if the input supply is reduced to zero the power supply current should remain. The input trigger current is the input current seen just prior to the supply current jumping. Testing latch-up is a destructive test, but in order to test 54HC/74HC devices without causing immediate damage, test limits for the amount of input or output currents and supply voltages should be observed. Even though immediate damage is avoided, SCR latch-up test is a destructive test and the IC performance may be degraded when testing to these limits. Therefore parts tested to these limits should not be used for design or production purposes. In the case of National's high speed CMOS logic the definition of "latch-up proof" requires the following test limits when using the standard DC power supply test as is shown in *Figure 15*.

1. Inputs: When testing latch-up on CMOS inputs the current into these inputs should be limited to less than 70 mA. Application of currents greater than this may damage the input protection poly resistor or input metalization, and prevent further testing of the IC.
2. Outputs: When testing outputs there is a limit to the metalization's current capacity. Output test currents should be limited to 200 mA. This limitation is due again to metalization short term current capabilities, similar to inputs. Application of currents greater than this may blow out the output.
3. Supply: The power supply voltage is recommended to be 7.0V which is at the absolute maximum limit specified in 54HC/74HC and is the worst case voltage for testing latch-up. If a device latches up it will short out the power supply and self destruct. (Another Vendors HC may latch-up for example.) It is recommended that to prevent immediate destruction of other vendors parts that the power supply be current limited to less than 300 mA.

It should be remembered that testing SCR latch up is essentially a destructive test even though precautions are taken

to limit the currents. In almost all instances at high temperature, if it is going to occur, latch-up will occur at current values between 0–50 mA.

There are a few special considerations when trying to measure worst case latch up current. Measuring input latch up current is straight forward, just force the inputs above or below the power supply, but to measure an output it must first be set to a high level when forcing it above V_{CC}, or to a low level when forcing it below ground. When measuring Tri-State outputs, the outputs should be disabled, and when measuring analog switches they should be either left open or turned off.

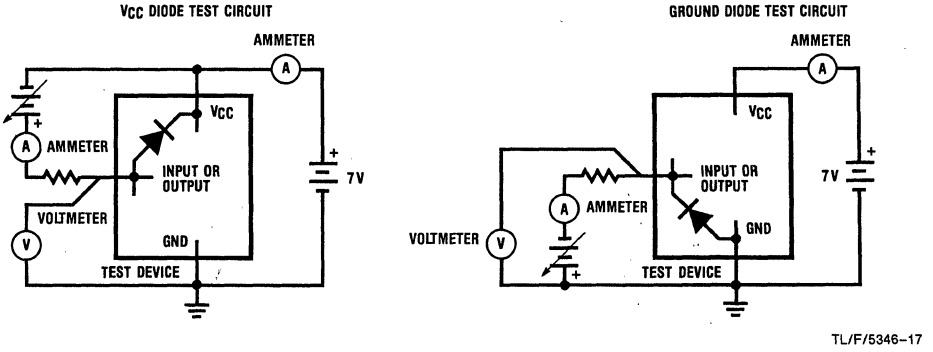
To measure the transient behavior of the test device or to reduce IC heating effects a pulse generator can be used in place of the input supply and an oscilloscope with a current probe should then replace the current meter. Care should be exercised to avoid ground loops in the test hardware as this may short out the supplies.

Although there are several methods of testing latch up, this method is very simple and easy to understand. It also yields conservative data since manually controlling the supplies is a slow process which causes localized heating on the chip prior to latch up, and lowers the latch up current.

6.0 CONCLUSION

SCR latch-up in CMOS circuits is a phenomena which when understood can be effectively controlled both from the integrated circuit and system level. National's proprietary CMOS process and layout considerations have eliminated CMOS latch up in the MM54HC/MM74HC family. This will increase the ease of use and design of this family by negating the need for extra SCR protection circuitry as well as very favorable impact system integrity and reliability.

Testing SCR Latch-Up of HCMOS



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$T_A = 125°C$

FIGURE 15. Bench Test Setup for Measuring Latch-up

HCMOS Crystal Oscillators

National Semiconductor
Application Note 340
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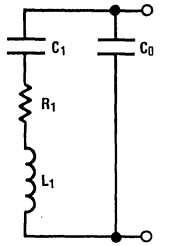
With the advent of high speed HCMOS circuits, it is possible to build systems with clock rates of greater than 30 MHz. The familiar gate oscillator circuits used at low frequencies work well at higher frequencies and either L–C or crystal resonators maybe used depending on the stability required. Above 20 MHz, it becomes expensive to fabricate fundamental mode crystals, so overtone modes are used.



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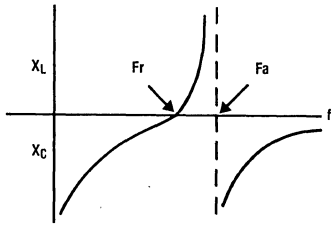
Crystal Equivalent Circuit



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Reactance of Crystal Resonator
FIGURE 1.

Basic Oscillator Theory

The equivalent circuit of a quartz crystal, and its reactance characteristics with frequency are shown in *Figure 1*. F_R is called the resonant frequency and is where L_1 and C_1 are in series resonance and the crystal looks like a small resistor R1. The frequency F_A is the antiresonant frequency and is the point where L_1–C_1 look inductive and resonate with C_O to form the parallel resonant frequency F_A, F_R and F_A are usually less than 0.1% apart. In specifying crystals, the frequency F_R is the oscillation frequency to the crystal in a series mode circuit, and F_R is the parallel resonant frequency. In a parallel mode circuit, the oscillation frequency will be slightly below F_A where the inductive component of the L_1 – C_1 arm resonates with C_O and the external circuit capacitance. The exact frequency is often corrected by the crystal manufacture to a specified load capacitance, usually 20 or 32 picofarads.

TABLE I Typical Crystal Parameters

Parameter	32 kHz fundamental	200 kHz fundamental	2 MHz fundamental	30 MHz overtone
R_1	200 kΩ	2 kΩ	100 Ω	20 Ω
L_1	7000H	27H	529 mH	11 mH
C_1	.003 pF	0.024 pF	0.012 pF	0.0026 pF
C_0	1.7 pF	9 pF	4 pF	6 pF
Q	100k	18k	54k	100k

The Pierce oscillator is one of the more popular circuits, and is the foundation for almost all single gate oscillators in use today. In this circuit, *Figure 2*, the signal from the input to the output of the amplifier is phase shifted 180 degrees. The crystal appears as a large inductor since it is operating in the parallel mode, and in conjunction with C_A and C_B, forms a pi network that provides an additional 180 degrees of phase shift from output to the input. C_A in series with C_B

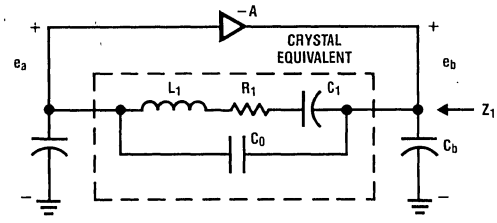

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FIGURE 2. Pierce Oscillator

plus any additional stray capacitance form the load capacitance for the crystal. In this circuit, C_A is usually made about the same value as C_B, and the total value of both capacitors in series is the load capacitance of the crystal which is generally chosen to be 32 pF, making the value of each capacitor 64 pF. The approximation equations of the load impedance, Z_1, presented to the output of the crystal oscillator's amplifier by the crystal network is:

$$Z_L = \frac{X_C^2}{R_L}$$

Where $X_C = -j/\omega C_B$ and R_L is the series resistance of the crystal as shown in Table I. Also $\omega = 2\pi f$ where f is the frequency of oscillation.

The ratio of the crystal network's input voltage to it's output voltage is given by:

$$\frac{e_A}{e_B} = \frac{\omega C_B}{\omega C_A} = \frac{C_B}{C_A}$$

C_A and C_B are chosen such that their series combintion capacitance equals the load capacitance specified by the manufacturer, ie 20 pF or 32 pF as mentioned. In order to oscillate the phase shift at the desired frequency around the oscillator loop must be 360° and the gain of the oscillator loop must be greater or equal to one, or:

$$(A_A)(A_F) \geq 1$$

Where A_A is amplifier gain and A_F is crystal network voltage gain of the crystal π network: e_A/e_B. Thus not only should the series combination of C_B and C_A be chosen. The ratio of the two can be set to adjust the loop gain of the oscillator.

For example if a 2 MHz oscillator is required. Then $R_L = 100\Omega$ (Table I). If $e_A/e_B = 1$ and the crystal requires a 32 pF load so $C_B = 64$ pF and then C_A becomes 64 pF also. The load presented by the crystal network is $Z_L = (1/2\pi\ (2$ MHz) (64 pF)$^2)/100 = 16$ kΩ

The CMOS Gate Oscillator

A CMOS gate sufficiently approaches the ideal amplifier shown above that it can be used in almost the same circuit. A review of manufacturers data sheets will reveal there are two types of inverting CMOS gates:

a) Unbuffered: gates composed of a single inverting stage. Voltage gain in the hundreds.

b) Buffered: gates composed of three inverting stages in series. Voltage gains are greater than ten thousand.

CMOS gates must be designed to drive relatively large loads and must supply a fairly large amount of current. In a single gate structure that is biased in its linear region so both devices are on, supply current will be high. Buffered gates are designed with the first and second gates to be much smaller than the output gate and will dissipate little power. Since the gain is so high, even a small signal will drive the output high or low and little power is dissipated. In this manner, unbuffered gates will dissipate more power than buffered gates.

Both buffered and unbuffered gates maybe used as crystal oscillators, with only slight design changes in the circuits.

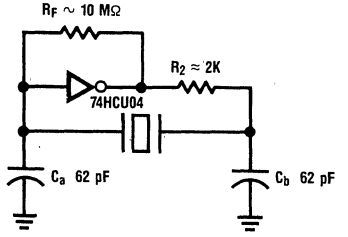

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FIGURE 3. Typical Gate Oscillator

In this circuit, R_F serves to bias the gate in its linear region, insuring oscillation, while R_2 provides an impedance to add some additional phase shift in conjunction with C_B. It also serves to prevent spurious high frequency oscillations and isolates the output of the gate from the crystal network so a clean square wave can be obtained from the output of the gate. Its value is chosen to be roughly equal to the capacitive reactance of C_B at the frequency of oscillation, or the value of load impedance Z_L calculated above. In this case, there will be a two to one loss in voltage from the output of the gate to the input of the crystal network due to the voltage divider effect of R_2 and Z_L. If C_A and C_B are chosen equal, the voltage at the input to the gate will be the same as that at the input to the crystal network or one half of the voltage at the output of the gate. In this case, the gate must have a voltage gain of 2 or greater to oscillate. Except at very high frequencies, all CMOS gates have voltage gains well in excess of 10 and satisfactory operation should result.

Theory and experiment show that unbuffered gates are more stable as oscillators by as much as 5 to 1. However, unbuffered gates draw more operating power if used in the same circuit as a buffered gate. Power consumption can be minimized by increasing feedback which forces the gate to operate for less time in it's linear region.

When designing with buffered gates, the value of R_2 or C_B may be increased by a factor of 10 or more. This will increase the voltage loss around the feedback loop which is desirable since the gain of the gate is considerably higher than that of an unbuffered gate.

C_A and C_B form the load capacitance for the crystal. Many crystals are cut for either 20 to 32 picofarad load capacitance. This is the capacitance that will cause the crystal to oscillate at its nominal frequency. Varying this capacitance will vary the frequency of oscillation. Generally designers work with crystal manufacturers to select the best value of load capacitance for their application, unless an off the shelf crystal is selected.

High Frequency Effects

The phase shift thru the gate may be estimated by considering it's delay time:

Phase Shift = Frequency X Time delay X 360°

The "typical gate oscillator" works well at lower frequencies where phase shift thru the gate is not excessive. However, above 4 MHz, where 10 nsec of time delay represents 14.4° of excess phase shift, R_2 should be changed to a small capacitor to avoid the additional phase shift of R_2. The value of this capacitor is approximately $1/\omega C$ where $\omega = 2\pi f$, but not less than about 20 pF.

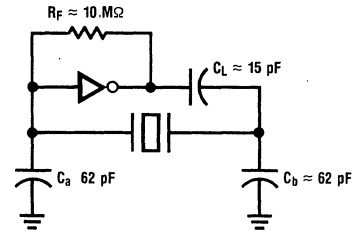

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FIGURE 4. Gate Oscillator for Higher Frequencies

Improving Oscillator Stability

The CMOS gate makes a mediocre oscillator when compared to a transistor or FET: It draws more power and is generally less stable. However, extra gates are often available and are often pressed into service as oscillators. If improved stability is required, especially from buffered gate oscillators, an approach shown in *Figure 5* can be used.

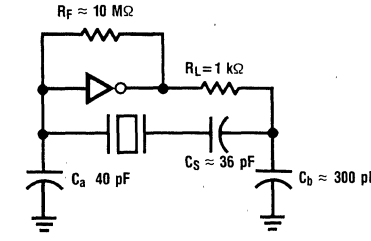

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FIGURE 5. Gate oscillator with improved stability

In this circuit, C_A and C_B are made large to swamp out the effects of temperature and supply voltage change on the gate input and output impedances. A small capacitor in series with the crystal acts as the crystal load and further isolates the crystal from the rest of the circuit.

Overtone Crystal Oscillators

At frequencies above 20 MHz, it becomes increasingly difficult to cut or work with crystal blanks and so generally a crystal is used in it's overtone mode. Also, fundamental mode crystals above this frequency have less stability and greater aging rates. All crystals will exhibit the same reactance vs. frequency characteristics at odd overtone frequencies that they do at the fundamental frequency. However, the overtone resonances are not exact multiples of the fundamental, so an overtone crystal must be specified as such.

In the design of an overtone crystal oscillator, it is very important to suppress the fundamental mode, or the circuit will try to oscillate there, or worse, at both the fundamental and the overtone with little predictability as to which. Basically, this requires that the crystal feedback network have more gain at the overtone frequency than the fundamental. This is usually done with a frequency selective network such as a tuned circuit.

The circuit in *Figure 6* operates in the parallel mode just as the Pierce oscillator above. The resonant circuit L_A—C_B is an effective short at the fundamental frequency, and is tuned somewhat below the deferred crystal overtone frequency. Also, C_L is chosen to suppress operation in the fundamental mode.

The coil L_A may be tuned to produce maximum output and will affect the oscillation frequency slightly. The crystal should be specified so that proper frequency is obtained at maximum output level from the gate.

Some Practical Design Tips

In the above circuits, some generalizations can be made regarding the selection of component values.

R_F: Sets the bias point, should be as large as practical.

R1: Isolates the crystal network from the gate output and provides excess phaseshift decreasing the probability of spurious oscillation at high frequencies. Value should be approximately equal to input impedance of the crystal network or reactance of C_B at the oscillator frequency. Increasing value will decrease the amount of feedback and improve stability.

C_B: Part of load for crystal network. Often chosen to be twice the value of the crystal load capacitance. Increasing value will increase feedback.

C_A: Part of crystal load network. Often chosen to be twice the value of the crystal load capacitance. Increasing value will increase feedback.

C_L: Used in place of R1 in high frequency applications. Reactance should be approximately equal to crystal network input impedance.

Oscillator design is an imperfect art at best. Combinations of theoretical and experimental design techniques should be used.

A. Do not design for an excessive amount of gain around the feedback loop. Excessive gain will lead to instability and may result in the oscillator not being crystal controlled.

B. Be sure to worst case the design. A resistor may be added in series with the crystal to simulate worst case crystals. The circuit should not oscillate on any frequency with the crystal out of the circuit.

C. A quick check of oscillator peformance is to measure the frequency stability with supply voltage variations. For HCMOS gates, a change of supply voltage from 2.5 to 6 volts should result in less than 10 PPM change in frequency. Circuit value changes should be evaluated for improvements in stability.

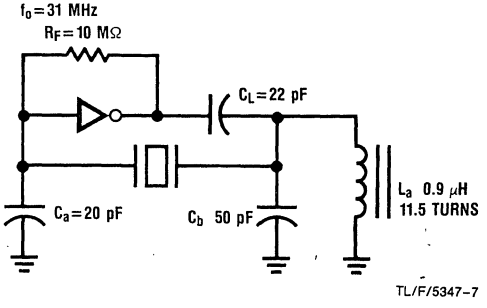


FIGURE 6. Parallel Mode Overtone Circuit

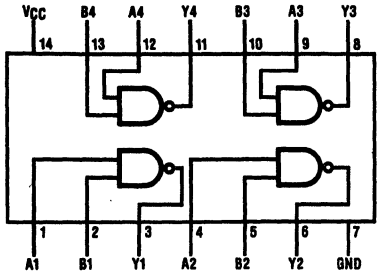
Section 3

Connection Diagrams

National Semiconductor

MM54HC/MM74HC Logic Connection Diagrams and Truth Tables

00 Quad 2-Input NAND



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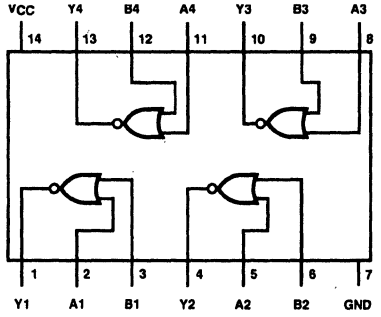
02 Quad 2-Input NOR



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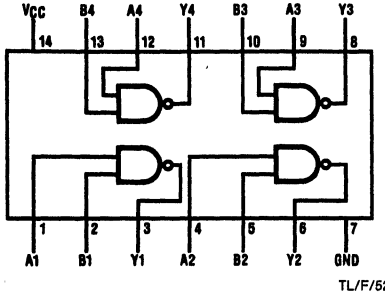
03 Quad 2-Input Open Drain NAND



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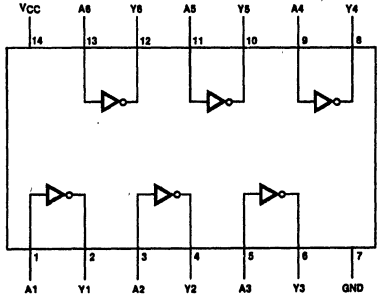
04 Hex Inverter



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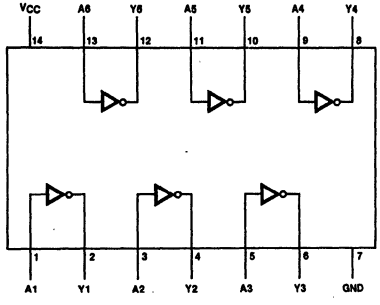
05 Hex Inverter (Open Drain)



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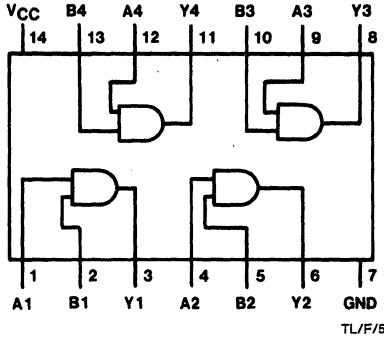
08 Quad 2-Input AND Gate



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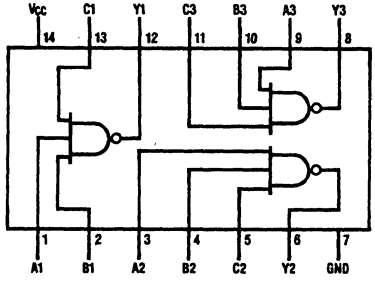
10 Triple 3-Input NAND Gate



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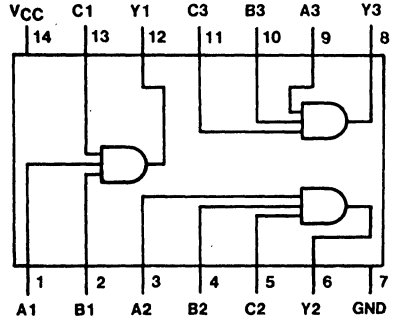
11 Triple 3-Input AND Gate



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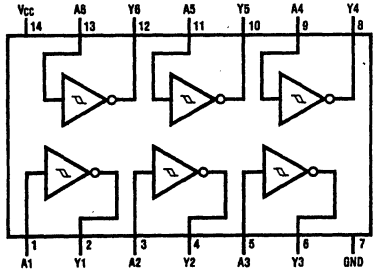
14 Hex Schmitt Trigger



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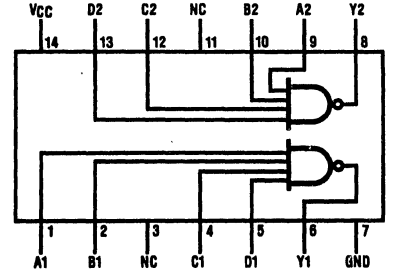
20 Dual 4-Input NAND Gate



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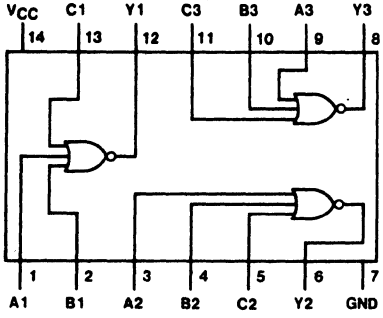
27 Triple 3-Input NOR



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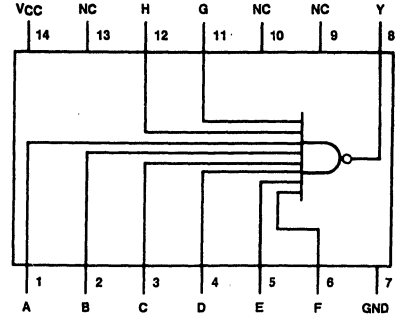
30 8-Input NAND Gate



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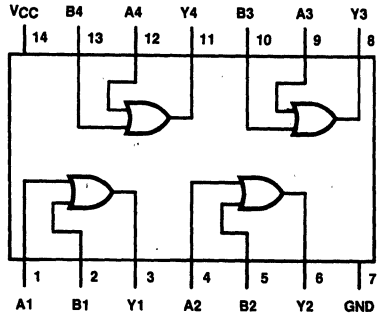
3

32 Quad 2-Input OR Gate



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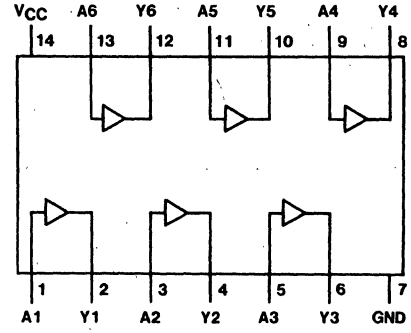
34 Hex Non-Inverting Gate



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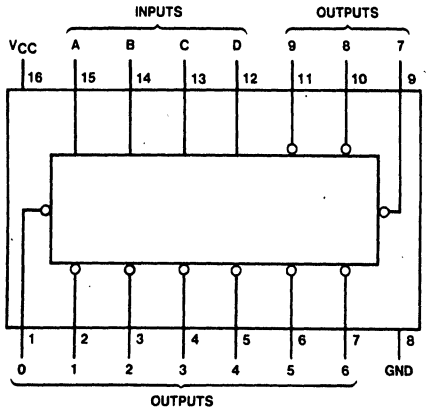
42 BCD-to-Decimal Decoder



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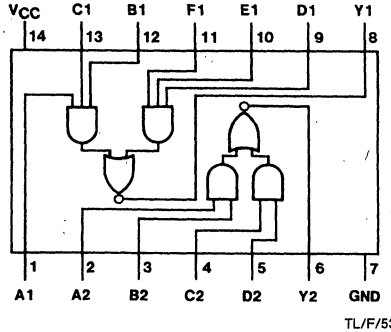
Truth Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level

51 Dual AND-OR-Invert Gate



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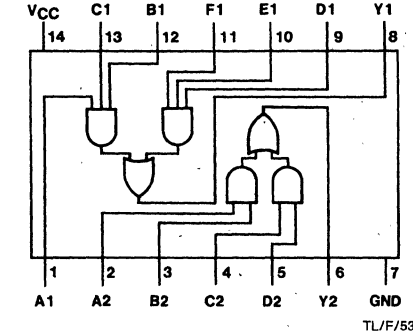
58 Dual AND-OR Gate



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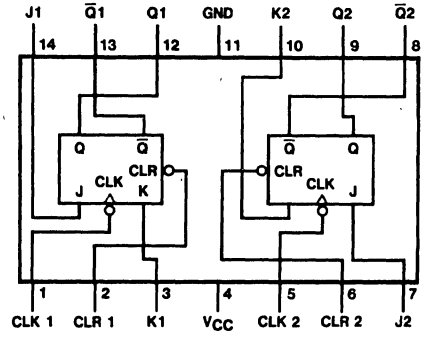
73 Dual J-K Flip-Flop with Clear



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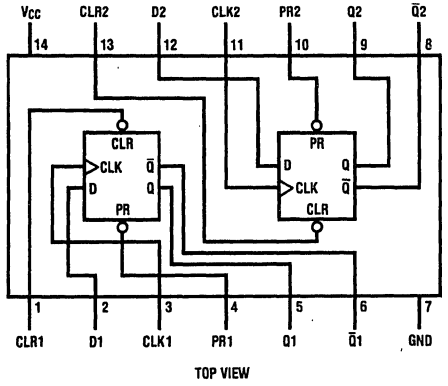
Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

74 Dual D Flip-Flop with Preset and Clear



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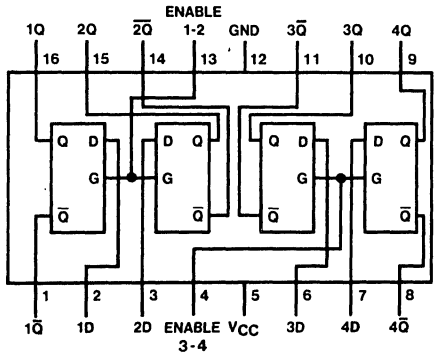
Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

75 Quad D Latch with Q and $\overline{Q}$



TL/F/5303–1

Truth Table

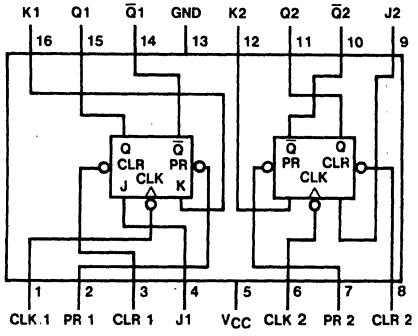
Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level; L = Low Level

X = Don't Care:

Q_0 = The level of Q before the transition of G

76 Dual J-K Flip-Flop with Preset and Clear



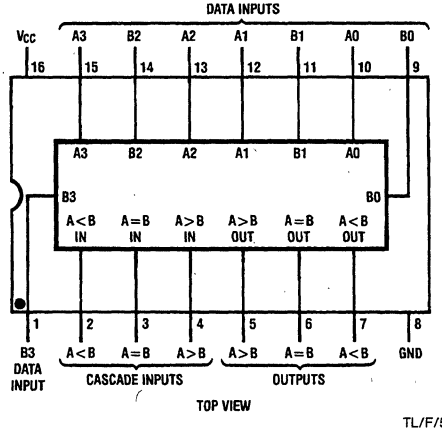
TL/F/5074–1

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed

85 4-Bit Magnitude Comparator

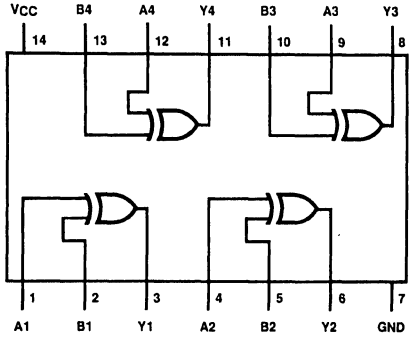


TL/F/5205–1

Truth Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

86 Quad 2-Input XOR



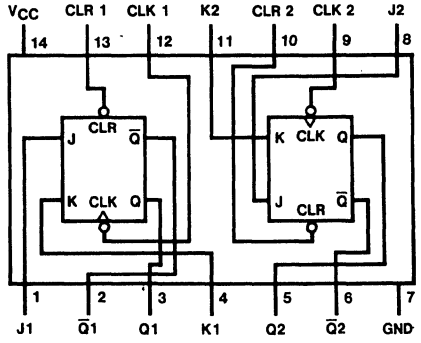
TL/F/5305–1

Truth Table

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

107 Dual J-K Flip-Flop with Clear

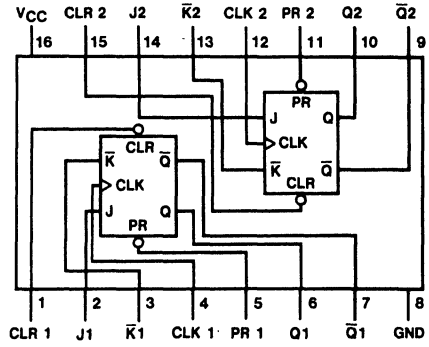


TL/F/5304–1

Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

109 Dual J-$\overline{K}$ Flip-Flop with Preset and Clear



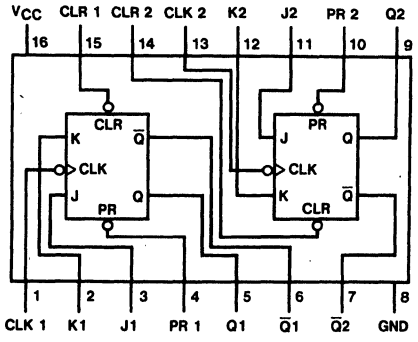
TL/F/5306–1

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

3

112 Dual J-K Flip-Flop with Preset and Clear



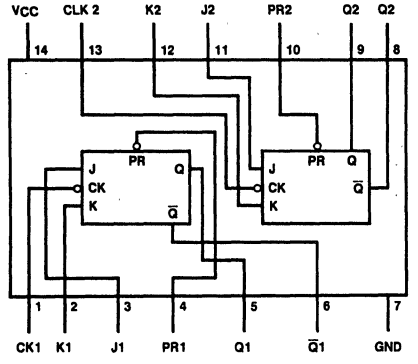
TL/F/5307–1

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed

113 Dual J-K Flip-Flop with Preset

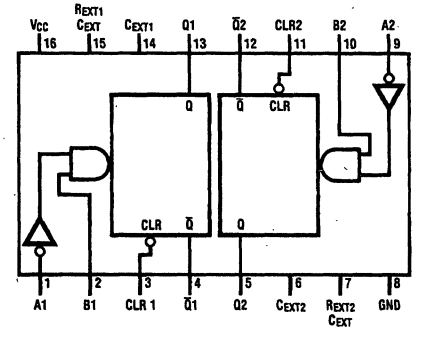


TL/F/5073–1

Truth Table

Inputs				Outputs	
PR	CLK	J	K	O	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

123 Dual Retriggerable Monostable Multivibrator



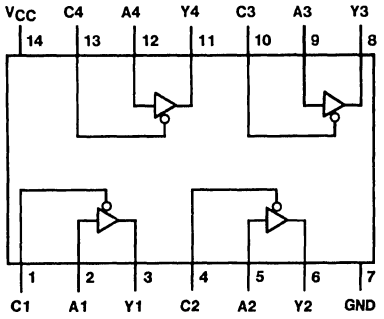
TL/F/5206–1

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎍ = One Low Level Pulse
X = Irrelevant

125 TRISTATE® Quad Buffer

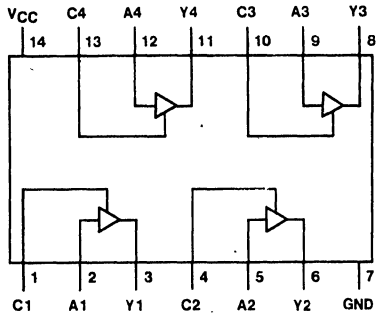


TL/F/5308–1

Truth Table

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Z

126 TRISTATE® Quad Buffer

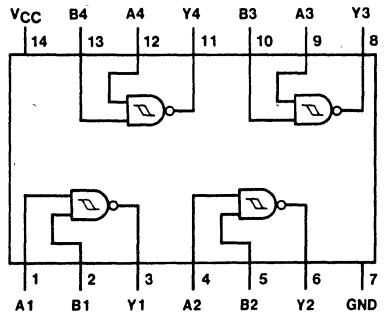


TL/F/5308–2

Truth Table

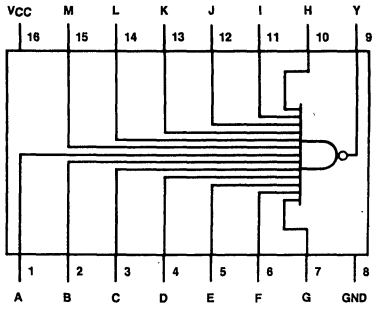
Inputs		Output
A	C	Y
H	H	H
L	H	L
X	L	Z

132 Quad 2-Input NAND Schmitt Trigger



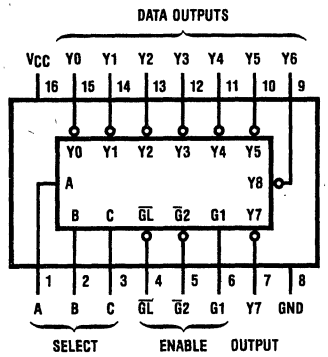
TL/F/5309–1

133 13-Input NAND



TL/F/5134–1

137 3-to-8 Line Decoder With Address Latches



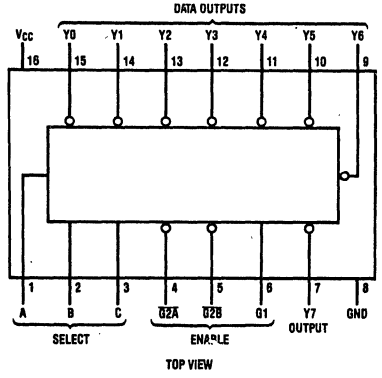
TL/F/5310–1

Truth Table

Inputs						Outputs							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address L; all others, H							

H = high level, L = low level, X = irrelevant

138 3-to-8 Line Decoder



TL/F/5120–1

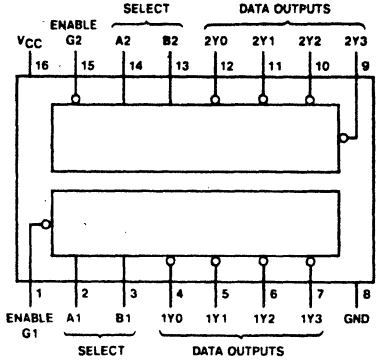
Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2}$ = G2A + G2B

H = high level, L = low level, X = don't care

139 Dual 2-to-4 Line Decoder



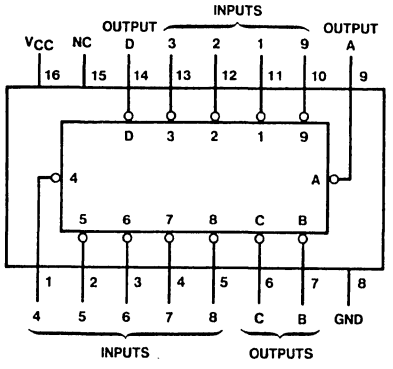
TL/F/5311–1

Truth Table

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

147 10-to-4 Line Priority Encoder



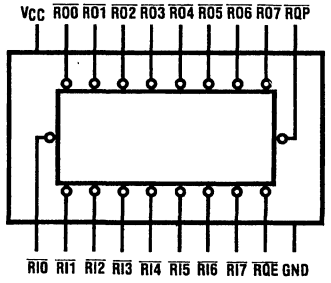
TL/F/5007–1

Truth Table

Inputs									Outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Logic Level, L = Low Logic Level, X = Irrelevant

149 8 Line to 8 Line Priority Encoder

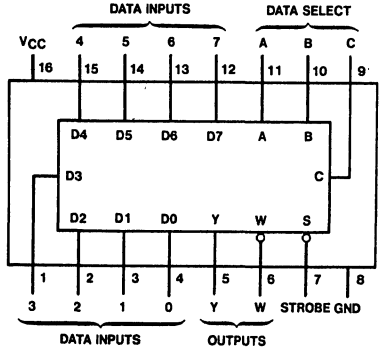


TL/F/5312–1

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

151 8 Channel Multiplexer



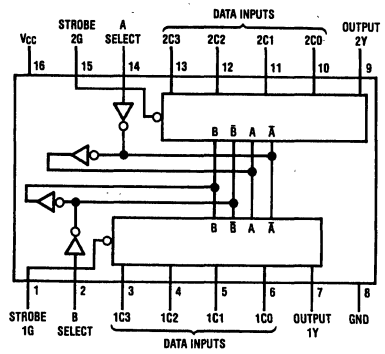
TL/F/5313–1

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0, D1...D7 = the level of the respective D input

153 Dual 4 Channel Multiplexer



TL/F/5107–1

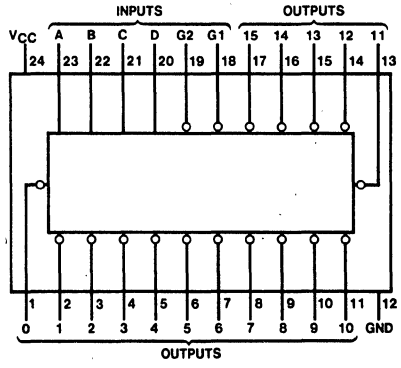
Truth Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = don't care.

154 4-to-16 Line Decoder



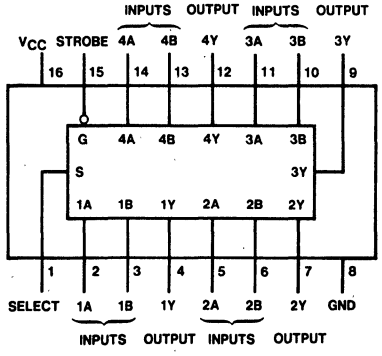
TL/F/5122–1

Truth Table

Inputs						Low Output*
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
L	L	L	H	L	L	4
L	L	L	H	L	H	5
L	L	L	H	H	L	6
L	L	L	H	H	H	7
L	L	H	L	L	L	8
L	L	H	L	L	H	9
L	L	H	L	H	L	10
L	L	H	L	H	H	11
L	L	H	H	L	L	12
L	L	H	H	L	H	13
L	L	H	H	H	L	14
L	L	H	H	H	H	15
L	H	X	X	X	X	—
H	L	X	X	X	X	—
H	H	X	X	X	X	—

*All others high

157 Quad 2-Input Multiplexer



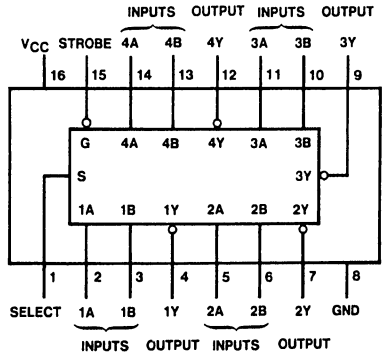
TL/F/5314–1

Truth Table

Inputs				Output Y
Strobe	Select	A	B	HC157
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Irrelevant

158 Quad 2-Input Multiplexer (Inverted Outputs)



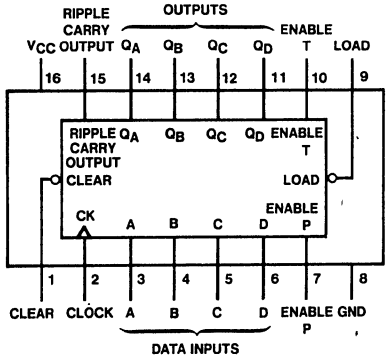
TL/F/5314–2

Function Table

Inputs				Output Y
Strobe	Select	A	B	HC158
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High Level, L = Low Level, X = Irrelevant

160, 161, 162, 163 4-Bit Synchronous Counter



TL/F/5008–1

Truth Tables

'HC160/HC161

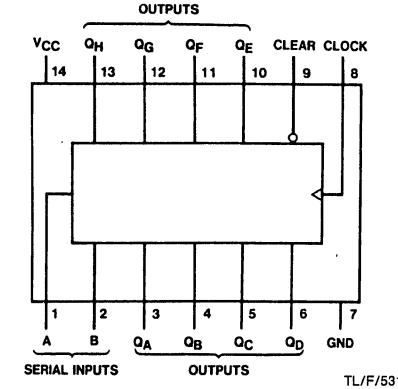
CLK	CLR	ENP	ENT	Load	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care, ↑ = low to high transition

'HC162/HC163

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

164 8-Bit Serial-In Parallel-Out Shift Register



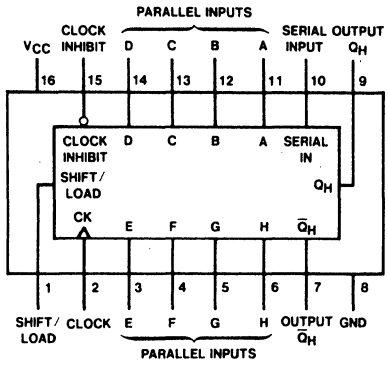
TL/F/5315–1

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from low to high level.
Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

165 8-Bit Parallel-In Serial-Out Shift Register



TL/F/5316–1

Function Table

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

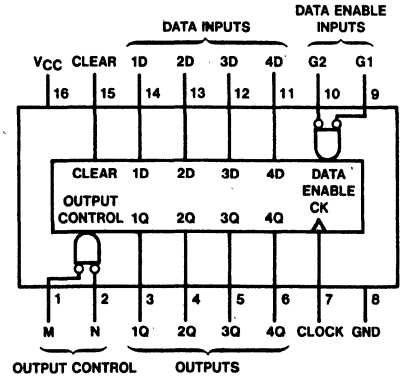
X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{AN}, Q_{GN} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

173 TRI-STATE® Quad D Flip-Flop



TL/F/5317–1

Truth Table

Inputs					Output
Clear	Clock	Data Enable G1	Data Enable G2	Data D	Q
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state: however, sequential operation of the flip-flops is not affected.

H = high level (steady state)

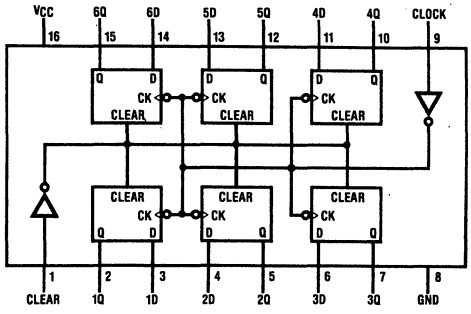
L = low level (steady state)

↑ = low-to-high level transition

X = don't care (any input including transitions)

Q_0 = the level of Q before the indicated steady state input conditions were established

174 Hex D Flip-Flop With Clear



TL/F/5318–1

Truth Table (Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level (steady state)

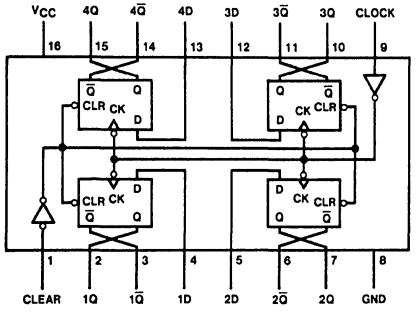
L = Low level (steady state)

X = Don't Care

↑ = Transition from low to high level

Q_0 = The level of Q before the indicated steady-state input conditions were established.

175 Quad D Flip-Flop With Clear



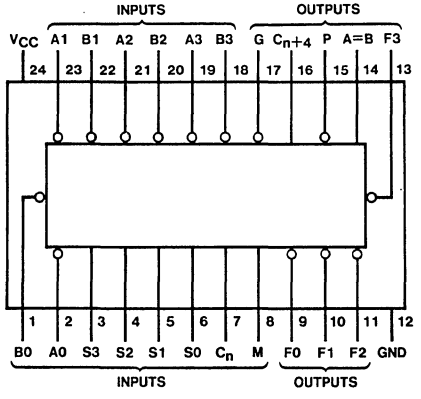
TL/F/5319–1

Truth Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

181 4-Bit Arithmetic/Logic Unit

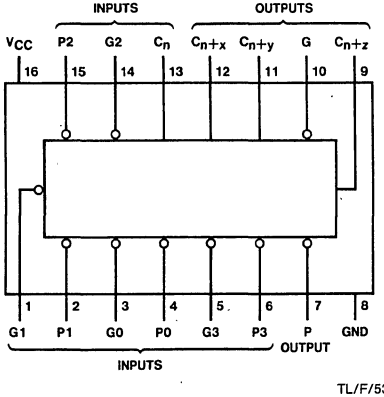


TL/F/5320–1

Pin Designations

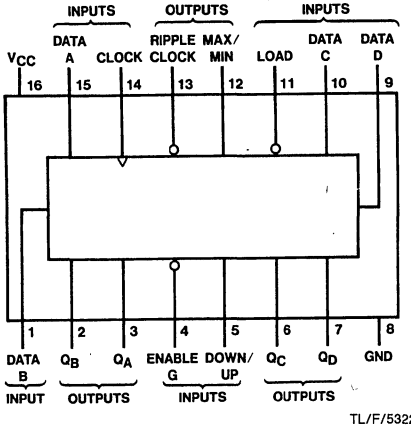
Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Outputs
P	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

182 4-Bit Look Ahead Carry Generator



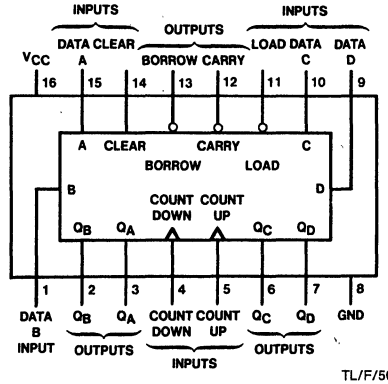
TL/F/5321–1

190, 191 4-Bit Synchronous Up/Down Counter



TL/F/5322–1

192, 193 4-Bit Synchronous Up/Down Counter



TL/F/5011–1

Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

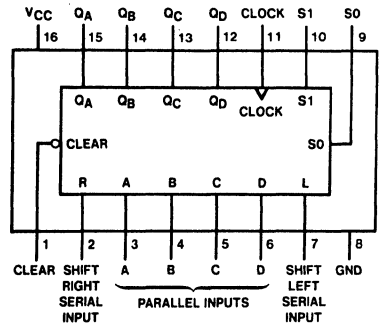
H = High level

L = Low level

↑ = Transition from low-to-high

X = Don't care

194 4-Bit Bidirectional Shift Register



TL/F/5323–1

Function Table

Inputs									Outputs			
Clear	Mode S1	Mode S2	Clock	Serial Left	Serial Right	Parallel A	Parallel B	Parallel C	Parallel D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

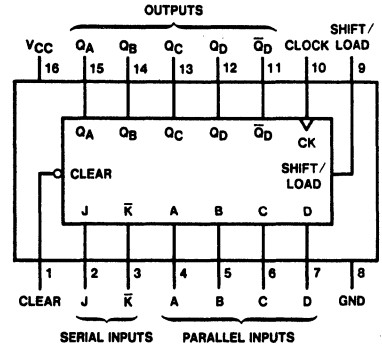
↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

195 4-Bit Parallel Shift Register



TL/F/5324–1

Function Table

Inputs										Outputs				
Clear	Shift/ Load	Clock	Serial J	Serial $\overline{K}$	Parallel A	Parallel B	Parallel C	Parallel D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

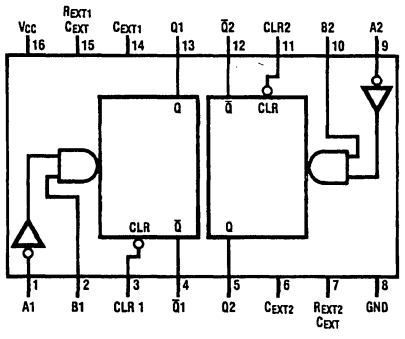
↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = the level of $Q_{A,\ QB}$, Q_C, respectively, before the most-recent transition of the clock.

221 Dual Monostable Multivibrator



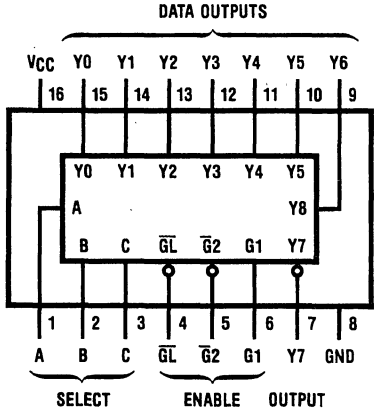
TL/F/5206–1

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

237 3-to-8 Line Decoder With Address Latches



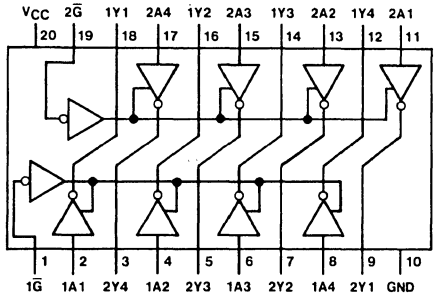
TL/F/5326–1

Truth Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant

240 Inverting Octal TRI-STATE® Buffer



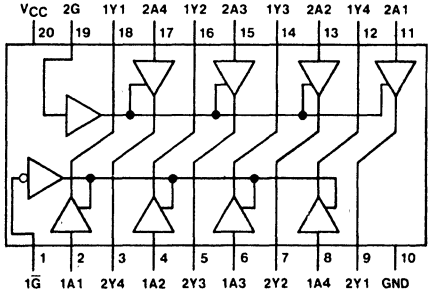
TL/L/5020–1

Truth Tables

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H=high level, L=low level, Z=high impedance

241 Octal TRI-STATE® Buffer

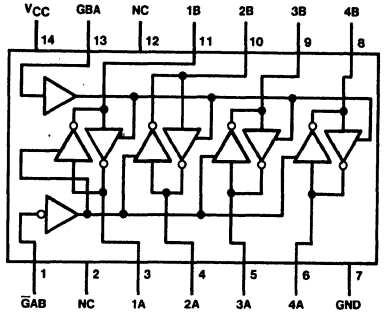


TL/L/5020–2

Truth Tables

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

242 Inverting Quad Bidirectional Transceiver

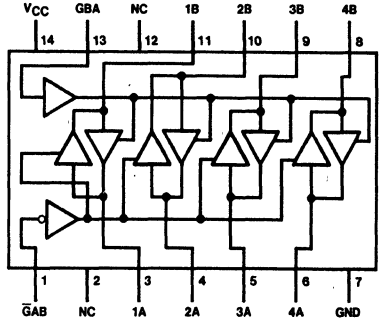


TL/L/5019–1

Truth Table

Control Inputs		Data Port Status	
$\overline{GAB}$	GBA	A	B
H	H	$\overline{OUTPUT}$	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	$\overline{OUTPUT}$

243 Quad Bidirectional Transceiver

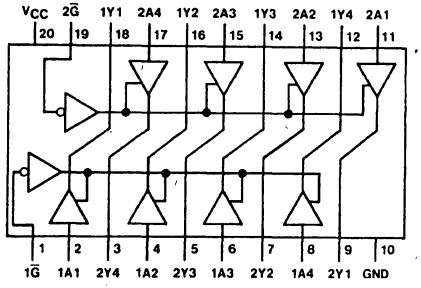


TL/L/5019–2

Truth Table

Control Inputs		Data Port Status	
$\overline{GAB}$	GBA	A	B
H	H	OUTPUT	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	OUTPUT

244 Octal TRI-STATE® Buffer



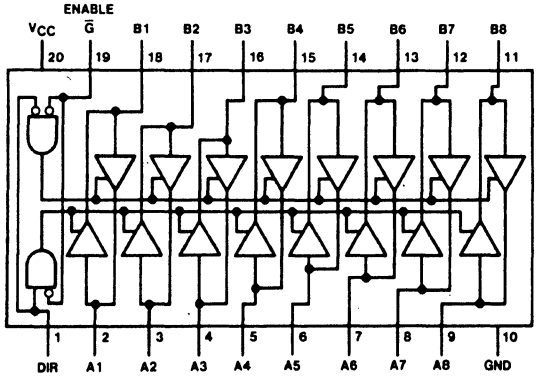
TL/F/5327–1

Truth Table

1$\overline{G}$	1A	1Y	2$\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

245 Octal Bidirectional Transceiver



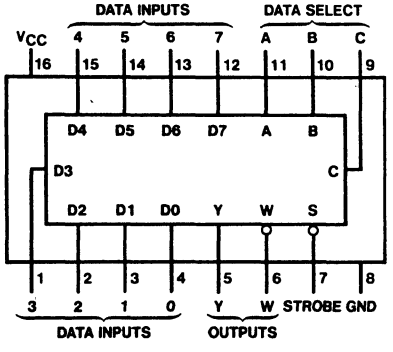
TL/F/5165–1

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

251 8-Channel TRI-STATE® Multiplexer



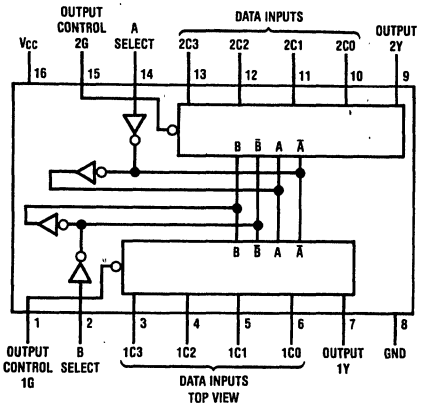
TL/F/5328–1

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

253 Dual 4-Channel TRI-STATE® Multiplexer



TL/F/5108–1

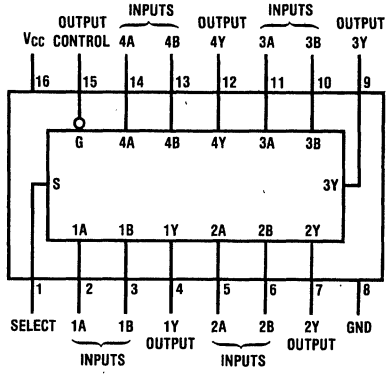
Truth Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off).

257 Quad 2-Channel TRI-STATE® Multiplexer



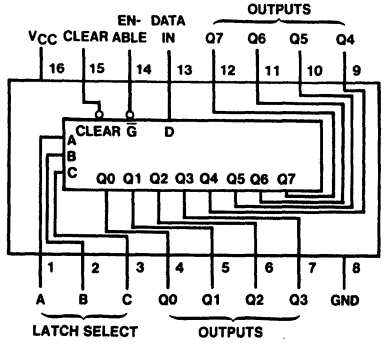
TL/F/5329–1

Truth Table

Inputs				Output Y
Output Control	Select	A	B	
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

259 8-Bit Addressable Latch

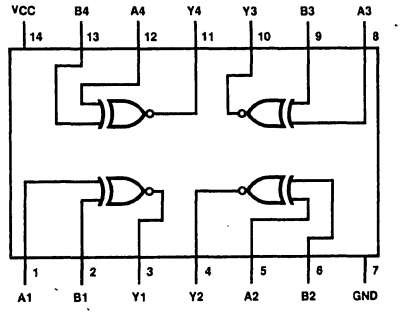


TL/F/5006–1

Truth Table

Inputs		Outputs of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Decoder
L	H	L	L	Clear

266 Quad 2-Input XNOR Gate



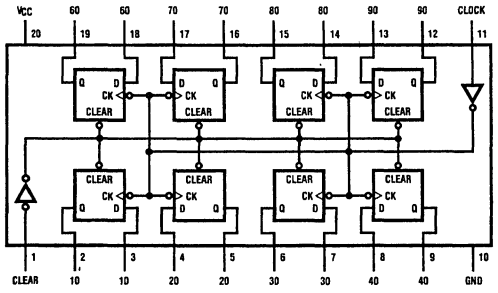
TL/F/5330–1

Truth Table

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

$Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

273 Octal D Flip-Flop With Clear



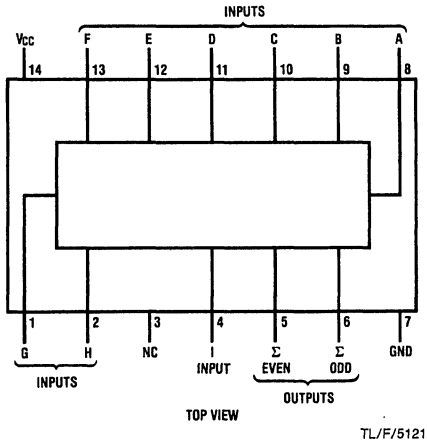
TL/F/5331–1

Truth Table
(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level (steady state)
L = Low level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established

280 9-Bit Odd/Even Parity Generator/Checker



TL/F/5121–1

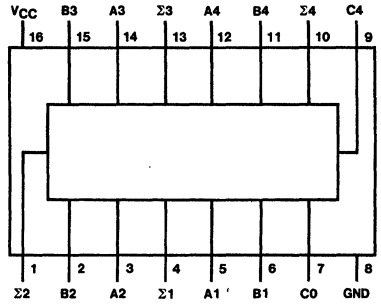
Function Table

Numbers of Inputs A thru 1 that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

3

283 4-Bit Binary Adder



TL/F/5332–1

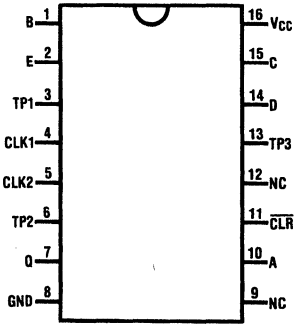
Truth Table

Input								Output									
								When C0 = L						When C0 = H			
												When C2 = L					When C2 = H
A1	A3	B1	B3	A2	A4	B2	B4	Σ1	Σ3	Σ2	Σ4	C2	C4	Σ1	Σ3	Σ2	Σ4	C2	C4
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	L	L
H	H	L	L	L	L	L	L	L	H	L	L	L	L	H	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L	L	H	H	L	L	L	L
H	L	H	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L	H	L
L	H	H	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L	H	L
H	H	H	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	H	H	L	L	L	L
H	L	L	H	L	L	L	L	H	H	L	L	L	L	L	L	L	L	H	L
L	H	L	H	L	L	L	L	H	H	L	L	L	L	L	L	L	L	H	L
H	H	L	H	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H	L
H	L	H	H	L	L	L	L	H	L	H	L	L	L	L	H	L	L	H	L
L	H	H	H	L	L	L	L	H	L	H	L	L	L	L	H	L	L	H	L
H	H	H	H	L	L	L	L	L	H	H	L	L	L	H	H	L	L	H	L
L	L	L	L	H	L	L	L	L	L	L	H	L	L	H	L	H	L	L	H
H	L	L	L	H	L	L	L	H	L	L	H	L	L	L	H	H	L	L	H
L	H	L	L	H	L	L	L	H	L	L	H	L	L	L	H	H	L	L	H
H	H	L	L	H	L	L	L	L	H	L	H	L	L	H	H	H	L	L	H
L	L	H	L	H	L	L	L	L	L	H	H	L	L	H	L	H	L	L	H
H	L	H	L	H	L	L	L	H	L	H	H	L	L	L	H	H	L	L	H
L	H	H	L	H	L	L	L	H	L	H	H	L	L	L	H	H	L	L	H
H	H	H	L	H	L	L	L	L	H	H	H	L	L	H	H	H	L	L	H
L	L	L	H	H	L	L	L	L	L	L	L	H	L	H	L	L	H	H	L
H	L	L	H	H	L	L	L	H	L	L	L	H	L	L	H	L	H	H	L
L	H	L	H	H	L	L	L	H	L	L	L	H	L	L	H	L	H	H	L
H	H	L	H	H	L	L	L	L	H	L	L	H	L	H	H	L	H	H	L
L	L	H	H	H	L	L	L	L	L	H	L	H	L	H	L	H	H	H	L
H	L	H	H	H	L	L	L	H	L	H	L	H	L	L	H	H	H	H	L
L	H	H	H	H	L	L	L	H	L	H	L	H	L	L	H	H	H	H	L
H	H	H	H	H	L	L	L	L	H	H	L	H	L	H	H	H	H	H	L
L	L	L	L	L	H	L	L	L	L	L	H	L	H	H	L	L	H	L	H
H	L	L	L	L	H	L	L	H	L	L	H	L	H	L	H	L	H	L	H
L	H	L	L	L	H	L	L	H	L	L	H	L	H	L	H	L	H	L	H
H	H	L	L	L	H	L	L	L	H	L	H	L	H	H	H	L	H	L	H
L	L	H	L	L	H	L	L	L	L	H	H	L	H	H	L	H	H	L	H
H	L	H	L	L	H	L	L	H	L	H	H	L	H	L	H	H	H	L	H
L	H	H	L	L	H	L	L	H	L	H	H	L	H	L	H	H	H	L	H
H	H	H	L	L	H	L	L	L	H	H	H	L	H	H	H	H	H	L	H
L	L	L	H	L	H	L	L	L	L	L	H	H	H	H	L	L	H	H	H
H	L	L	H	L	H	L	L	H	L	L	H	H	H	L	H	L	H	H	H
L	H	L	H	L	H	L	L	H	L	L	H	H	H	L	H	L	H	H	H
H	H	L	H	L	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	L	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	H	L	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H
L	H	H	H	L	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	H	H	H	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	L	L	L	L	L	H	H	H	H	L	L	H	H	H
H	L	L	L	H	H	L	L	H	L	L	H	H	H	L	H	L	H	H	H
L	H	L	L	H	H	L	L	H	L	L	H	H	H	L	H	L	H	H	H
H	H	L	L	H	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	L	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	H	H	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	L	L	L	L	L	H	H	H	H	L	L	H	H	H
H	L	L	H	H	H	L	L	H	L	L	H	H	H	L	H	L	H	H	H
L	H	L	H	H	H	L	L	H	L	L	H	H	H	L	H	L	H	H	H
H	H	L	H	H	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	L	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H
L	H	H	H	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level

Note Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4

292 Programmable Frequency Dividers/Digital Timer

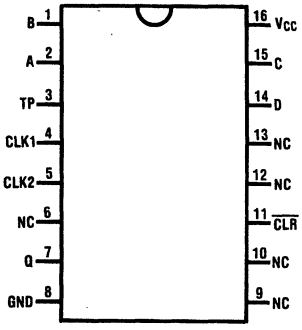


TL/F/5333–1

Truth Table

CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↑	L	Count
H	L	↑	Count
H	H	X	Inhibit
H	X	H	Inhibit

294 Programmable Frequency Dividers/Digital Timer

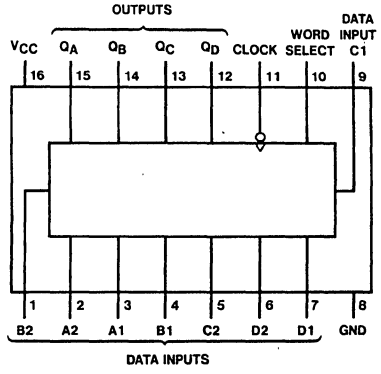


TL/F/5333–2

Truth Table

CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↑	L	Count
H	L	↑	Count
H	H	X	Inhibit
H	X	H	Inhibit

298 Quad 2 Channel Multiplexer With Latches



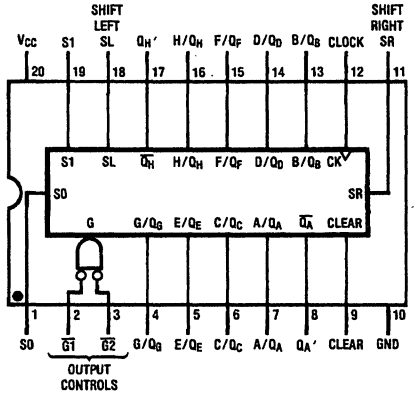
TL/F/5334–2

Truth Table

Inputs		Outputs			
Word Select	Clock	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↓ = Transition from high to low level
a1, a2, etc. = The level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = The level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.

299 8-Bit Universal Shift Register



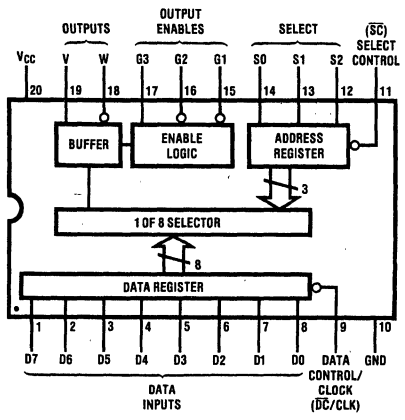
TL/F/5207–1

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L or H	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{GN}
	H	L	H	L	L	↑	X	H	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{GN}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

354, 356 8-Channel TRI-STATE® Multiplexer with Latches



TOP VIEW TL/F/5208–1

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
Z = high-impedance state (off state)
↑ = transition from low to high level

Function Table

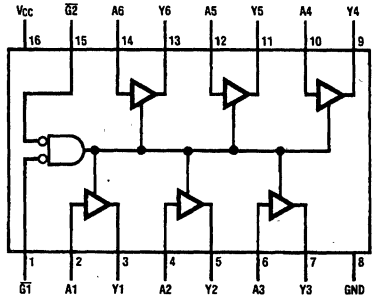
Inputs								Outputs	
Select†			Data Control 'HC354	Clock 'HC356	Output Enables				
S1	S2	S0	$\overline{DC}$	CLK	$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H	H or L	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

D0 . . . D7 = the level steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of 'HC356

$D0_n$ . . . $D7_n$ = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock.

†This column shows the input address set-up with $\overline{SC}$ low.

365 Hex TRI-STATE® Buffer

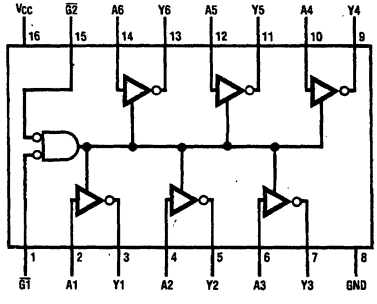


TL/F/5209–1

Truth Table

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

366 Inverting Hex TRI-STATE® Buffer

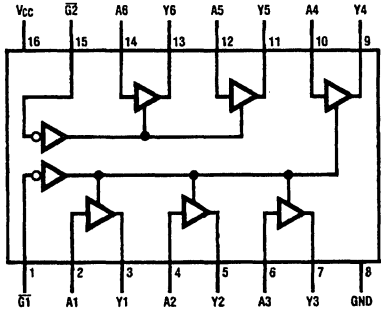


TL/F/5209–2

Truth Table

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

367 Hex TRI-STATE® Buffer

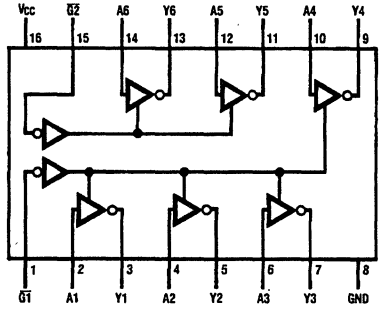


TL/F/5209–3

Truth Table

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

368 Inverting Hex TRI-STATE® Buffer

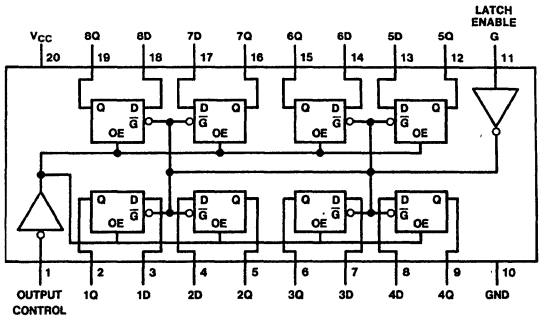


TL/F/5209–4

Truth Table

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

373 Octal TRI-STATE® Latch



TL/F/5335–1

Truth Table

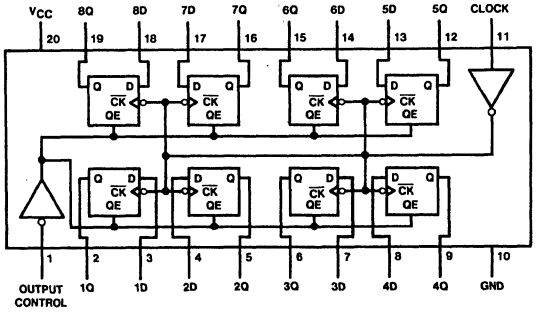
Output Control	Latch Enable G	Data	373 Output
L	H	H	H
L	H	L	H
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

374 Octal TRI-STATE® Flip-Flop



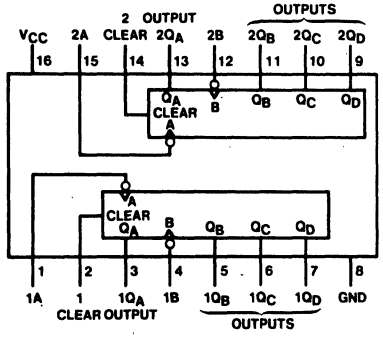
TL/F/5336–1

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

390 Dual 4-Bit Decade Counter

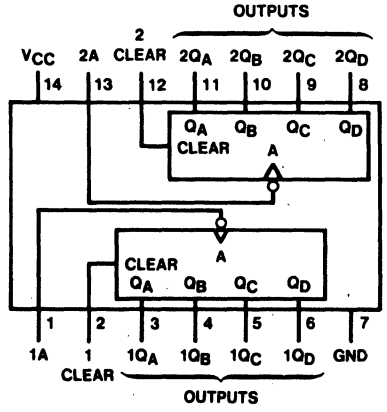


TL/F/5337–1

Truth Table

Inputs		Function
Clock	Clear	
↓	L	Increment
X	H	Clear

393 Dual 4-Bit Binary Counter

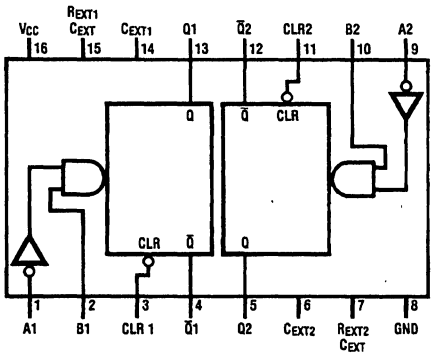


TL/F/5337–2

Truth Table

Input		Function
Clock	Clear	
↓	L	Increment
X	H	Clear

423 Dual Retriggerable Monostable Multivibrator



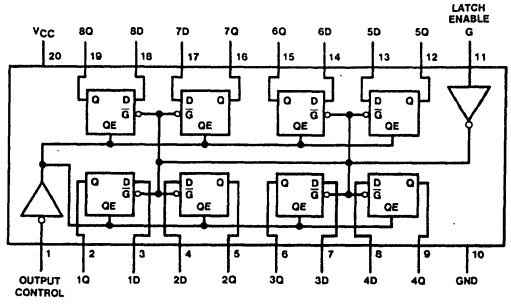
TL/F/5206–1

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

533 Octal TRI-STATE® Latch with Inverted Outputs



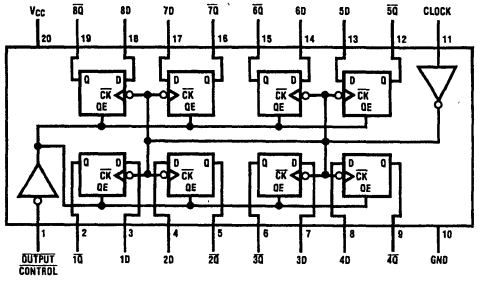
TL/F/5339–1

Truth Table

Output Control	Latch Enable G	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance

534 Octal TRI-STATE® Flip-Flops with Inverted Outputs



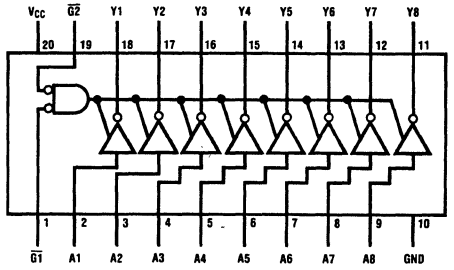
TL/F/5340–1

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

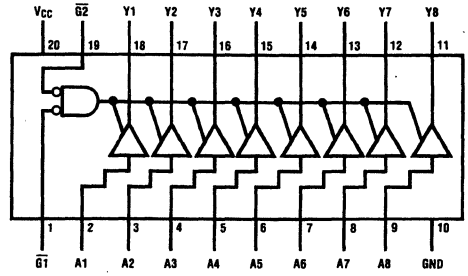
H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
$\overline{Q}_0$ = The level of the output before steady state input conditions were established

540 Inverting Octal TRI-STATE® Buffer



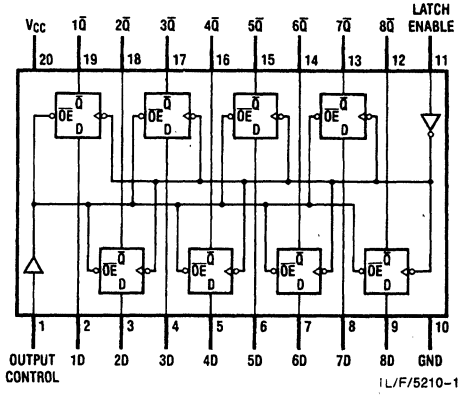
TL/F/5341–1

541 Octal TRI-STATE® Buffer



TL/F/5341–2

563 Octal TRI-STATE® Octal Latch with Inverted Outputs



TL/F/5210–1

TOP VIEW

Truth Table

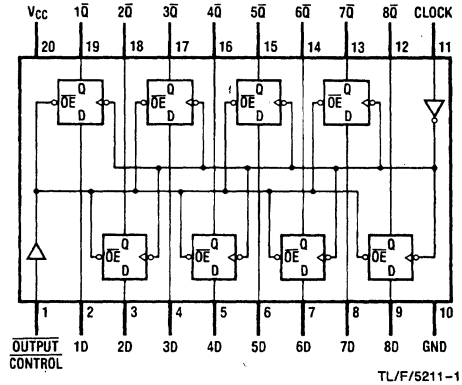
Output Control	Latch Enable	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established

Z = high impedance

564 Octal TRI-STATE® Flip-Flop with Inverted Outputs



TL/F/5211–1

TOP VIEW

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level

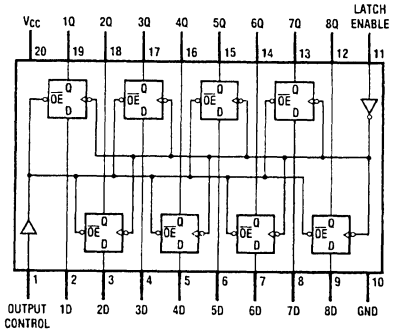
X = Don't Care

↑ = Transition from low-to-high

Z = High Impedance State

Q_0 = The level of the output before steady state Input conditions were established

573 Octal TRI-STATE® Latch



TOP VIEW

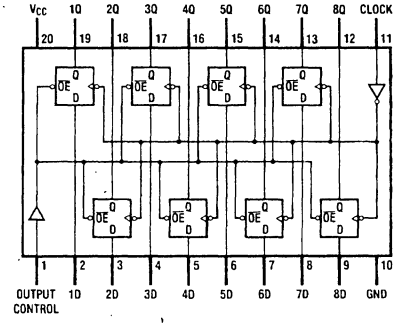
TL/F/5212–1

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance
X = Don't care

574 Octal TRI-STATE® Flip-Flop



TOP VIEW

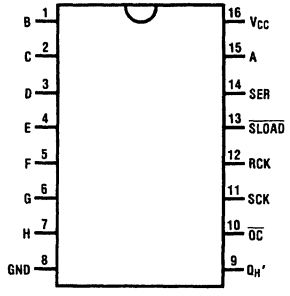
TL/F/5213–1

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

589 8-Bit Shift Registers with Input Latches

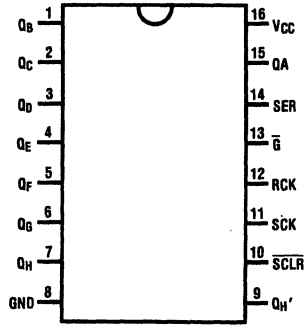


TL/F/5368–1

Truth Table

RCK	SCK	$\overline{SLOAD}$	$\overline{OC}$	Function
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	X	L	Serial output in high impedance state
X	↑	H	H	Shift register clocked $Q_M = Q_{n-1}$, Q_O = SER

595 8-Bit Serial-In Parallel-Out Shift Register with Latches

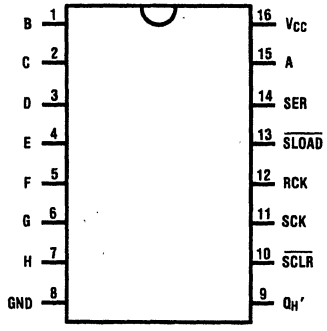


TL/F/5342–1

Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{G}$	Function
X	X	X	1	Q_A thru Q_H = Tri-State
X	X	L	X	Shift Register cleared $Q_{H'} = 0$
X	↑	H	X	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER
↑	X	H	X	Contents of Shift Register transferred to output latches

597 8-Bit Parallel to Serial Shift Register

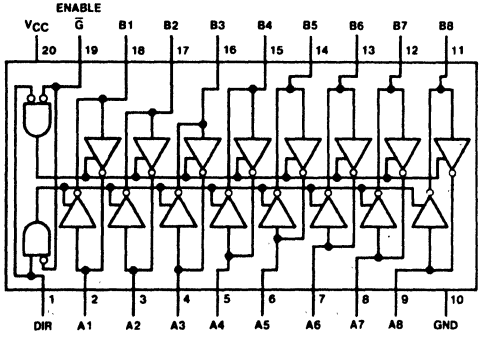


TL/F/5343–1

Truth Table

RCK	SCK	$\overline{SLOAD}$	$\overline{SCLR}$	Function
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked $Q_n = Q_{n-1}$, Q_0 = SER

640 Inverting Octal Bidirectional Transceiver



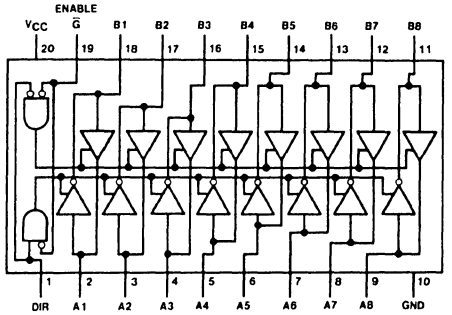
TL/F/5344–1

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	640
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

643 True/Inverting Octal Bidirectional Transceiver



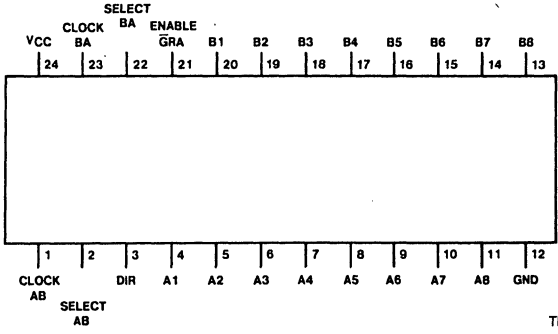
TL/F/5344–2

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	643
L	L	B data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

646, 648 Octal Bidirectional Transceiver with Latches



TL/F/5345–2

Truth Table

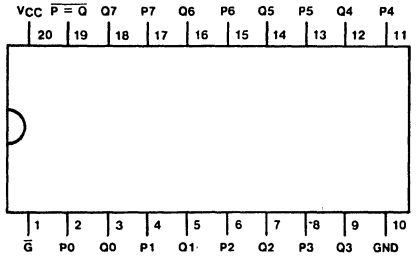
Inputs						Data I/O		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	646	648
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Input	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

H = High Level L = Low Level X = Irrelevant ↑ = low-to-high level transition

The data output functions i.e., data at the bus pins may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled.

The data output functions i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

688 8-Bit Magnitude Comparator

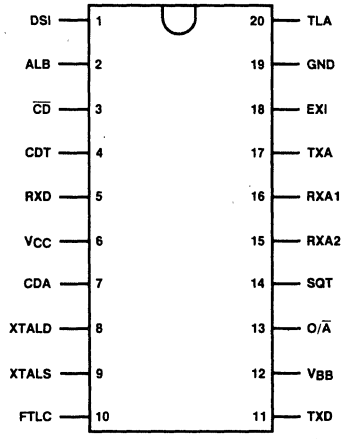


TL/F/5018–1

Truth Table

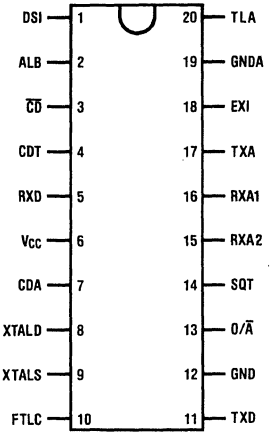
Inputs		
Data P,Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

942 300 Baud Modem



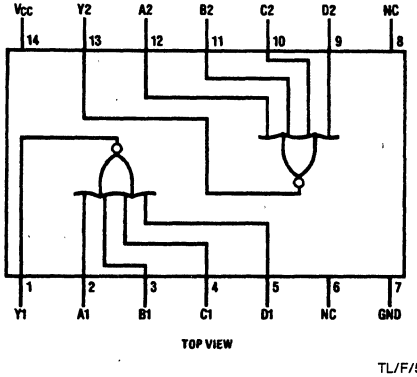
TL/F/5348–1

943 300 Baud Modem (Single Power Supply)



TL/F/5349–1

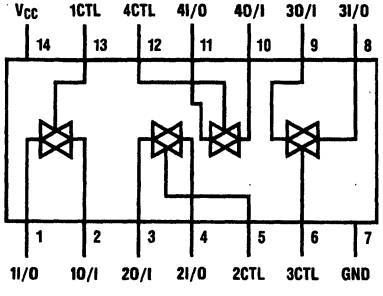
4002 Dual 4-Input NOR Gate



TOP VIEW

TL/F/5154–1

4016 Quad Bilateral Analog Switch

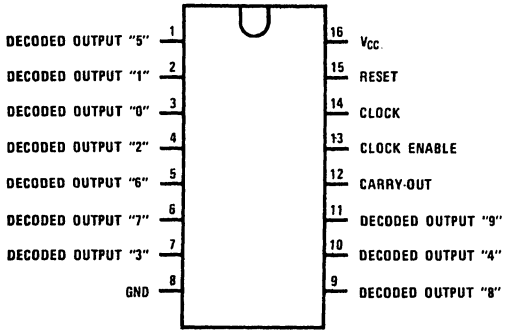


TL/F/5350–1

Truth Table

Input	Switch
CTL	I/O-O/I
L	"OFF"
H	"ON"

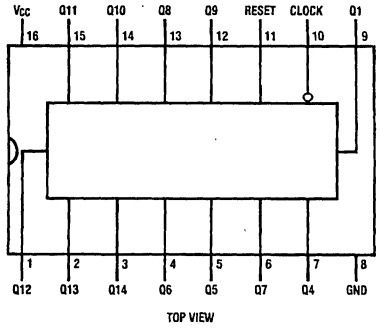
4017 Decade Counter Divider with 10 Decoded Outputs



TOP VIEW

TL/F/5351–1

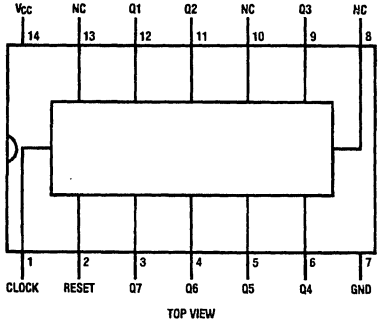
4020 14 Stage Binary Counter



TOP VIEW

TL/F/5216–1

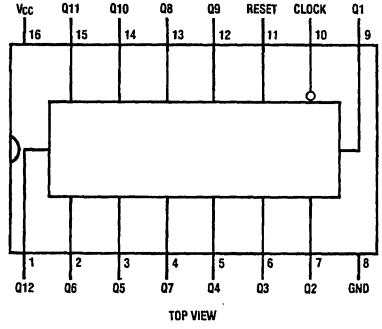
4024 7 Stage Ripple Counter



TOP VIEW

TL/F/5216–2

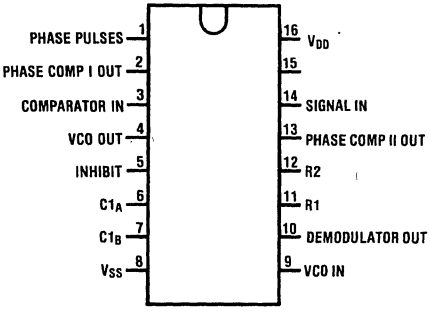
4040 12 Stage Binary Counter



TOP VIEW

TL/F/5216–3

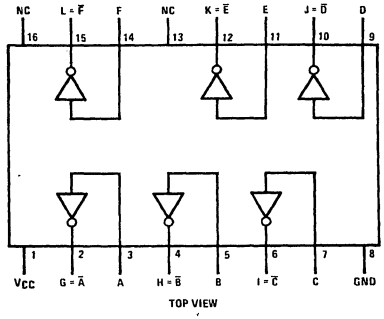
4046 Phase Lock Loop



TOP VIEW

TL/F/5352–2

4049 Hex Inverting Logic Level Down Converter

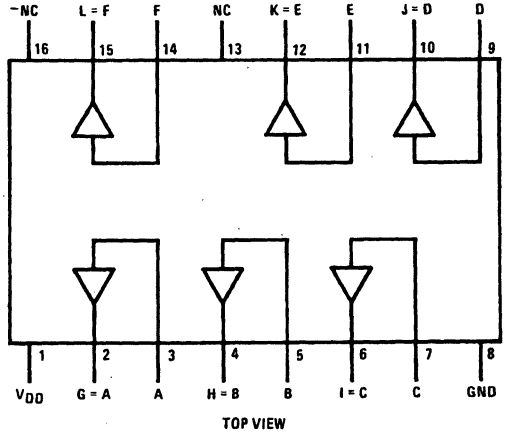


TOP VIEW

TL/F/5214–1

3

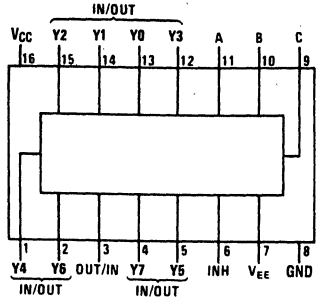
4050 Hex Logic Level Down Converter



TOP VIEW

TL/F/5214–2

4051 8 Channel Analog Multiplexer

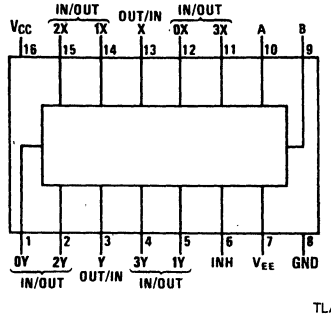


TL/F/5353–1

Truth Tables

Input				"ON" Channel
Inh	C	B	A	
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

4052 Dual 4-Channel Analog Multiplexer

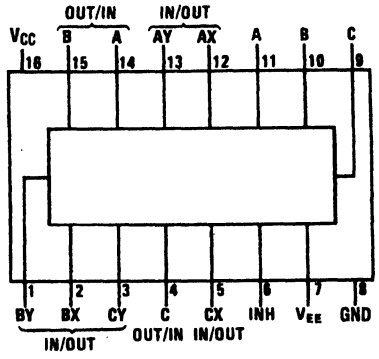


TL/F/5353–2

Truth Tables

Inputs			"ON" Channels	
Inh	B	A	X	Y
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

4053 Triple 2 Channel Analog Multiplexer

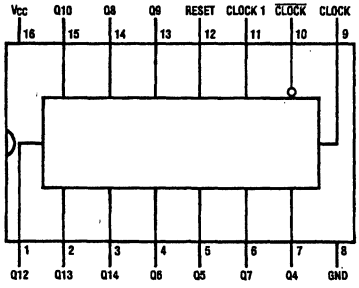


TL/F/5353–3

Truth Tables

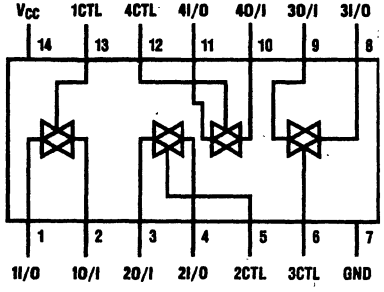
Input				"ON" Channels		
Inh	C	B	A	C	b	a
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AY
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AY
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AY
L	H	H	H	CY	BY	AY

4060 14 Stage Binary Counter



TL/F/5216–4

4066 Quad Analog Switch

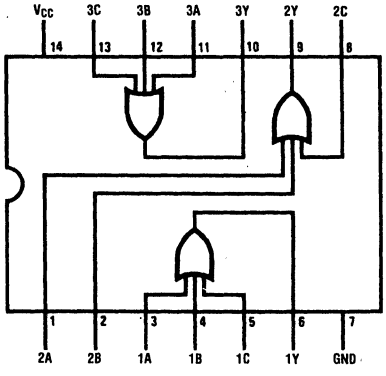


TL/F/5350–1

Truth Table

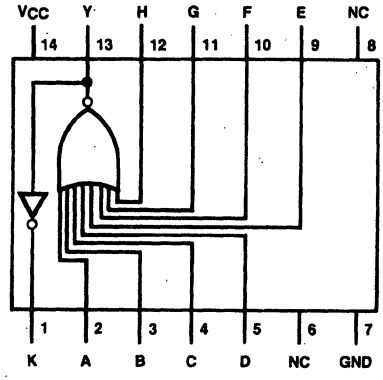
Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

4075 Triple 3-Input OR Gate



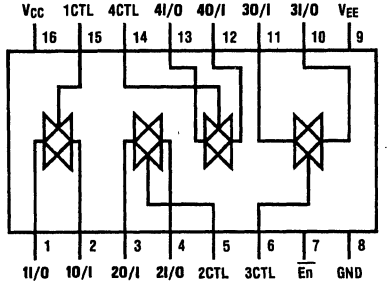
TL/F/5155–1

4078 8-Input OR/NOR Gate



TL/F/5135–1

4316 Quad Analog Switch with Level Translator

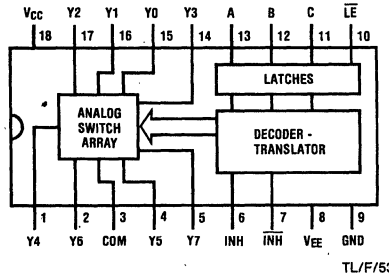


TL/F/5369–1

Truth Table

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

4351 8 Channel Analog Multiplexer with Latches

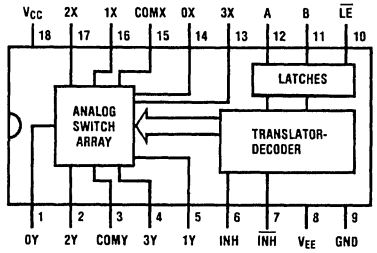


TL/F/5372–1

Truth Table

Inh	$\overline{Inh}$	$\overline{LE}$	C	B	A	"On" Channel
H	X	X	X	X	X	None
X	L	X	X	X	X	None
L	H	H	L	L	L	Y0
L	H	H	L	L	H	Y1
L	H	H	L	H	L	Y2
L	H	H	L	H	H	Y3
L	H	H	H	L	L	Y4
L	H	H	H	L	H	Y5
L	H	H	H	H	L	Y6
L	H	H	H	H	H	Y7
L	H	L	X	X	X	Last Selected Channel "On"
X	X	↓	X	X	X	Selected Channel Latched

4352 Dual 4 Channel Analog Multiplexer with Latches

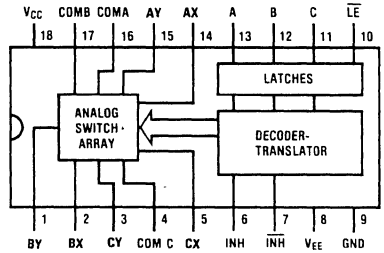


TL/F/5372-2

Truth Table

Inh	$\overline{Inh}$	$\overline{LE}$	B	A	"On" Channels X	"On" Channels Y
H	X	X	X	X	None	
X	L	X	X	X	None	
L	H	H	0	0	0X	0Y
L	H	H	0	1	1Y	1Y
L	H	H	1	0	2Y	2Y
L	H	H	1	1	3Y	3Y
L	H	L	X	X	Last Selected Channels "On"	
X	X	↓	X	X	Selected Channels Latched	

4353 Triple 2 Channel Analog Multiplexer with Latches

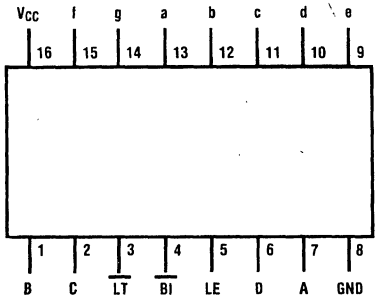


TL/F/5372-3

Truth Table

Inh	$\overline{Inh}$	$\overline{LE}$	C	B	A	"On" Channels C	"On" Channels B	"On" Channels A
H	X	X	X	X	X	None		
X	L	X	X	X	X	None		
L	H	H	L	L	L	CX	BX	AX
L	H	H	L	L	H	CX	BX	AY
L	H	H	L	H	L	CX	BY	AX
L	H	H	L	H	H	CX	BY	AY
L	H	H	H	L	L	CY	BX	AX
L	H	H	H	L	H	CY	BX	AY
L	H	H	H	H	L	CY	BY	AX
L	H	H	H	H	H	CY	BY	AY
L	H	L	X	X	X	Last Selected Channels "On"		
X	X	↓	X	X	X	Selected Channels Latched		

4511 BCD-to-7 Segment Latch/Decoder Driver



TL/F/5373-1

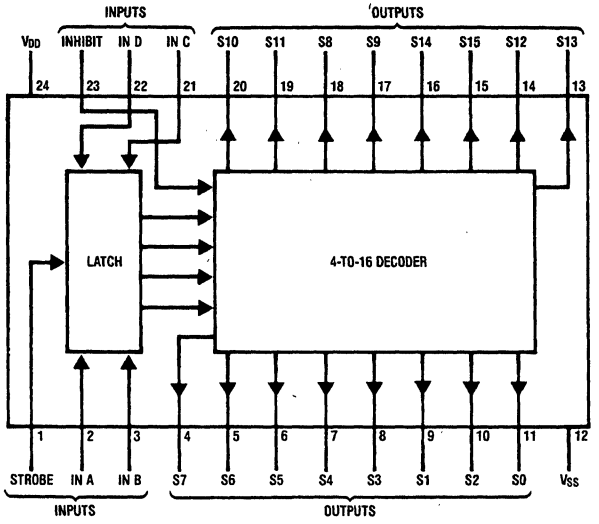
Truth Table

INPUTS LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	OUTPUTS a	b	c	d	e	f	g	DISPLAY
x	x	0	x	x	x	x	1	1	1	1	1	1	1	8
x	0	1	x	x	x	x	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	x	x	x	x				*				*

x = Don't care

* = Depends upon the BCD code applied during the 0 to 1 transition of LE.

4514 4-to-16 Line Decoder with Address Latch

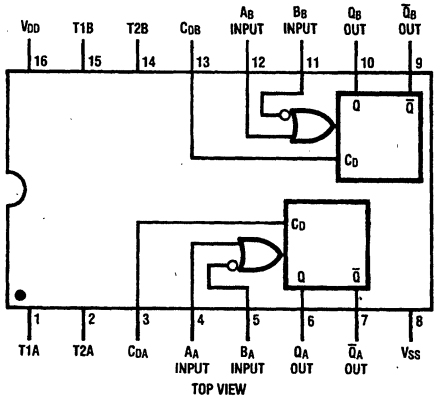


TL/F/5215–1

Truth Table

LE	Inhibit	Data Inputs D	C	B	A	Selected Output High
H	L	L	L	L	L	S0
H	L	L	L	L	H	S1
H	L	L	L	H	L	S2
H	L	L	L	H	H	S3
H	L	L	H	L	L	S4
H	L	L	H	L	H	S5
H	L	L	H	H	L	S6
H	L	L	H	H	H	S7
H	L	H	L	L	L	S8
H	L	H	L	L	H	S9
H	L	H	L	H	L	S10
H	L	H	L	H	H	S11
H	L	H	H	L	L	S12
H	L	H	H	L	H	S13
H	L	H	H	H	L	S14
H	L	H	H	H	H	S15
X	H	X	X	X	X	All Outputs = 0
L	L	X	X	X	X	Latched Data

4538 Dual Retriggerable Monostable Multivibrator



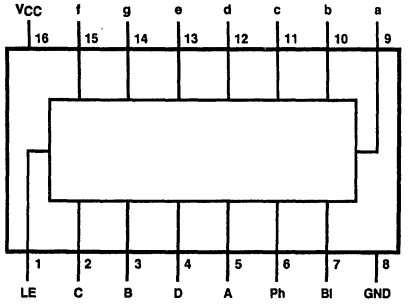
TL/F/5217–1

Truth Table

Inputs Clear	A	B	Outputs Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transistion from Low to High
↓ = Transistion from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

4543 BCD-to-7 Segment Latch/Decoder/Driver for Liquid Crystal Displays



TL/F/5128–1

Truth Table

Inputs							Outputs							
LE	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	**							**
†	†	H	†				Inverse of Output Combinations Above							Display as above

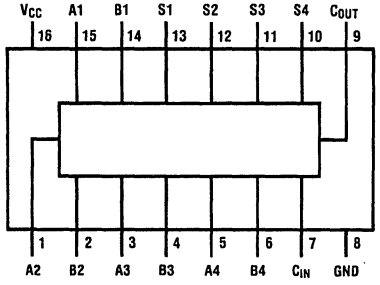
X—Don't care

†=Same as above combinations

*=For liquid crystal readouts, apply a square wave to Ph.

**=Depends upon the BCD code previously applied when LE—H

4560 4-Bit NBCD Adder



TL/F/5374–1

Truth Table*

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{IN}	C_{OUT}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	1	1	1	0	0	1	1	1	1	0	0	1

*Partial truth table to show logic operation for representative input values

Section 4

MM54HC/MM74HC Data Sheets

National Semiconductor

MM54HC00/MM74HC00 Quad 2-Input NAND Gate

General Description

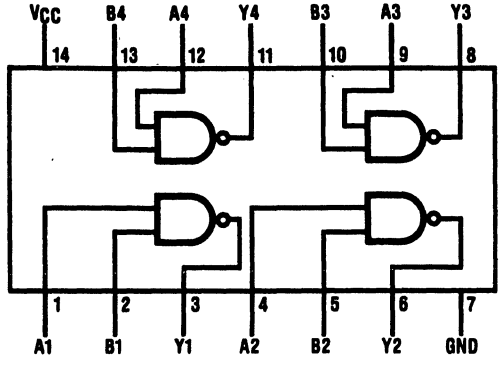
These NAND gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LSTTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5295–1

MM54HC00/MM74HC00

54HC00 (J) 74HC00 (J,N)

Logic Diagram

TL/F/5292–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC02/MM74HC02 Quad 2-Input NOR Gate

General Description

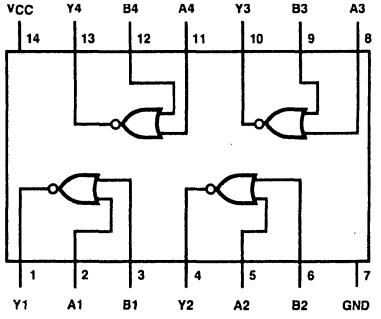
These NOR gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent supply current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- High output current: 4 mA minimum

Connection Diagram

Dual-In-Line Package

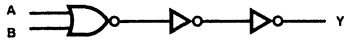


TL/F/5294–1

MM54HC02/MM74HC02

54HC02 (J) 74HC02 (J,N)

Logic Diagram



TL/F/5294–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC03/MM74HC03 Quad 2-Input Open Drain NAND Gate

General Description

These NAND gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LSTTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

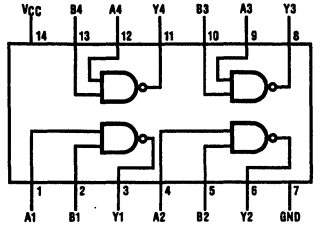
As with standard 54HC/74HC push-pull outputs there are diodes to both V_{CC} and ground. Therefore the output should not be pulled above V_{CC} as it would be clamped to one diode voltage above V_{CC}. This diode is added to enhance electrostatic protection.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

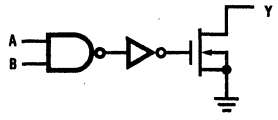


TL/F/5295–1

MM54HC03/MM74HC03

54HC03 (J) 74HC03 (J,N)

Logic Diagram



TL/F/5295–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage(V_{CC})	−0.5 to +7.0V
DC Input Voltage(V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage(V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current(I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
		R_L=1 kΩ	4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
V_{OL}	Minimum Low Level Output Voltage	V_{IN}=V_{IH}						
		$\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
		R_L=∞	4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH}						
		$\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{LKG}	Minimum High Level Output Leakage Current	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}	6.0V		0.5	5	10	μA
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$R_L=1$ KΩ	10	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$R_L=1$ KΩ	2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{THL}	Maximum Output Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$. The power dissipated by R_L is not included.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HCU04/MM74HCU04 Hex Inverter

General Description

These inverters utilize microCMOS™ Technology, 3.5 micro silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

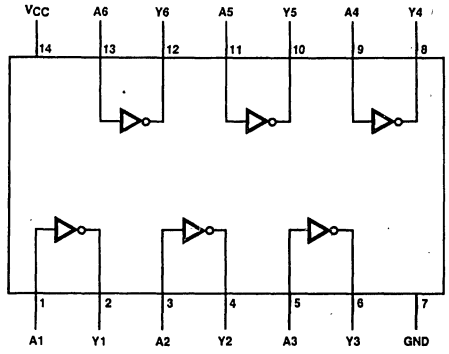
The MM54HCU04/MM74HCU04 is an unbuffered inverter. It has high noise immunity and the ability to drive 15 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns
- Fan out of 15 LS-TTL loads
- Quiescent power consumption: 10 μA maximum at room temperature
- Typical input current: 10^{-5} μA

Connection Diagram

Dual-In-Line Package

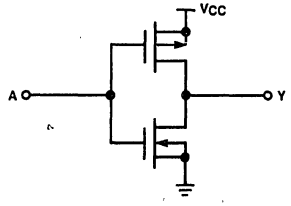


TL/F/5296–1

MM54HCU04/MM74HCU04

54HCU04 (J) 74HCU04 (J,N)

Schematic Diagram



TL/F/5296–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.7	1.7	1.7	V
			4.5V		3.6	3.6	3.6	V
			6.0V		4.8	4.8	4.8	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.8	0.8	0.8	V
			6.0V		1.1	1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.8	1.8	1.8	V
			4.5V	4.5	4.0	4.0	4.0	V
			6.0V	6.0	5.5	5.5	5.5	V
		V_{IN}=GND $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $|I_{OUT}|\leq$20 μA	2.0V	0	0.2	0.2	0.2	V
			4.5V	0	0.5	0.5	0.5	V
			6.0V	0	0.5	0.5	0.5	V
		V_{IN}=V_{CC} $|I_{OUT}|\leq$6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		7	13	ns

AC Electrical Characteristics

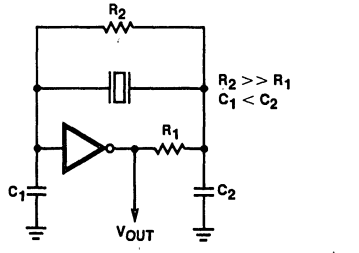
$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	49	82	103	120	ns
			4.5V	9.9	16	21	24	ns
			6.0V	8.4	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		90				pF
C_{IN}	Maximum Input Capacitance			8	15	15	15	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

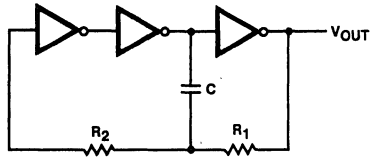
Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Typical Applications



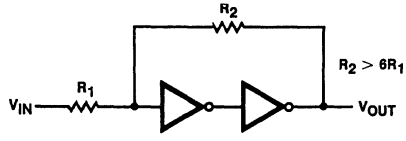
TL/F/5296–3

FIGURE 1: Crystal Oscillator



TL/F/5296–4

FIGURE 2: Stable RC Oscillator



TL/F/5296–5

FIGURE 3: Schmitt Trigger

4

National Semiconductor

MM54HC04/MM74HC04 Hex Inverter

General Description

These Inverters utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

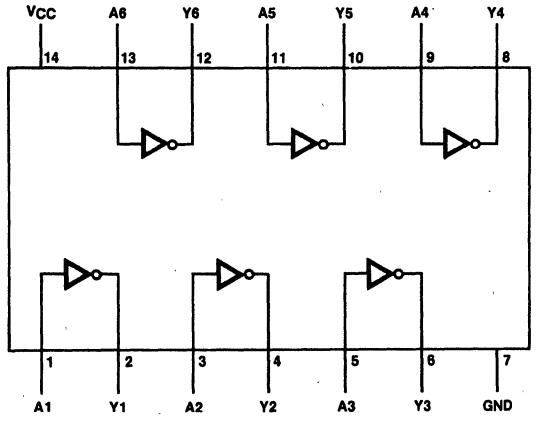
The MM54HC04/MM74HC04 is a triple buffered inverter. It has high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Fan out of 10 LS-TTL loads
- Quiescent power consumption: 10 μW maximum at room temperature
- Typical input current: 10^{-5} μA

Connection Diagram

Dual-In-Line Package



TL/F/5069–1

MM54HC04/MM74HC04

54HC04 (J) 74HC04 (J,N)

Logic Diagram

TL/F/5069–2

1 of 6 Inverters

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	55	86	108	129	ns
			4.5V	11	19	24	29	ns
			6.0V	9	16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC08/MM74HC08 Quad 2-Input AND Gate

General Description

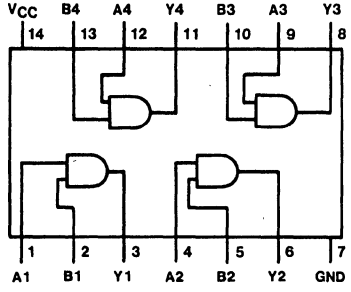
These AND gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. The HC08 has buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns (t_{PHL}), 12 ns (t_{PLH})
- Fanout of 10 LS-TTL loads
- Quiescent power consumption: 2 μA maximum at room temperature
- Typical input current: 10^{-5} μA

Connection Diagram

Dual-In-Line Package



TL/F/5297–1

MM54HC08/MM74HC08

54HC08 (J) 74HC08 (J,N)

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage(V_{CC})	−0.5 to +7.0V
DC Input Voltage(V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage(V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current(I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, Output High to Low		12	20	ns
t_{PLH}	Maximum Propagation Delay, Output Low to High		7	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay Output High to Low		2.0V	77	121	151	175	ns
			4.5V	15	24	30	35	ns
			6.0V	13	20	25	30	ns
t_{PLH}	Maximum Propagation Delay Output Low to High		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		38				pF
C_{IN}	Maximum Input Capacitance			4	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC10/MM74HC10 Triple 3-Input NAND Gate

General Description

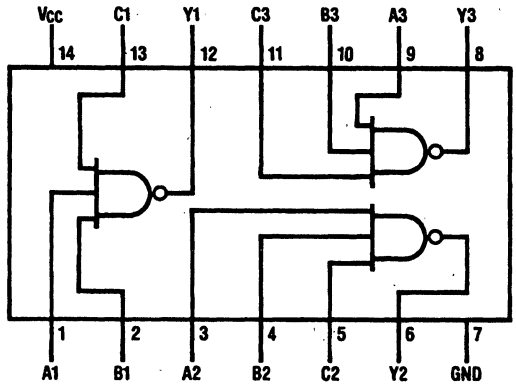
These NAND gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LSTTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

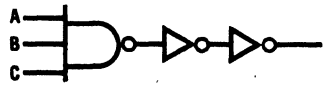


TL/F/5153–1

MM54HC10/MM74HC10

54HC10 (J) 74HC10 (J,N)

Logic Diagram



$Y = \overline{ABC}$

TL/F/5153–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN}=V_{IH}					
		$\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4 V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40 μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

4

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	48	90	113	134	ns
			4.5V	10	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC11/MM74HC11 Triple 3-Input AND Gate

General Description

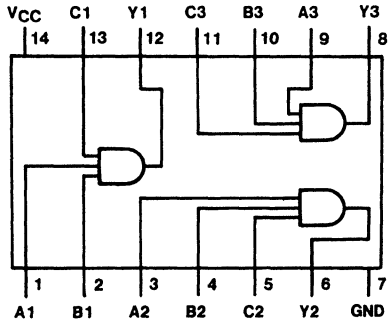
These AND gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

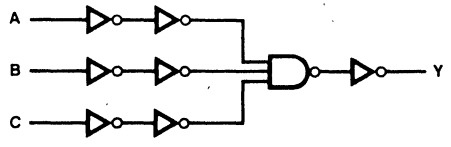


TL/F/5298–1

MM54HC11/MM74HC11

54HC11 (J) 74HC11 (J,N)

Logic Diagram



TL/F/5298–2

(1 OF 3 GATES)

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Output High to Low		2.0V	48	125	156	190	ns
			4.5V	18	25	31	38	ns
			6.0V	15	21	27	31	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		35				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC14/MM74HC14 Hex Inverting Schmitt Trigger

General Description

The MM54HC14/MM74HC14 utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

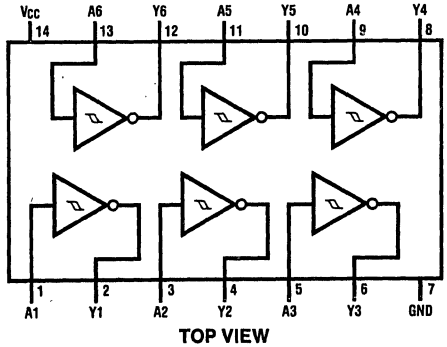
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC}=4.5V

Connection Diagram

Dual-In-Line Package



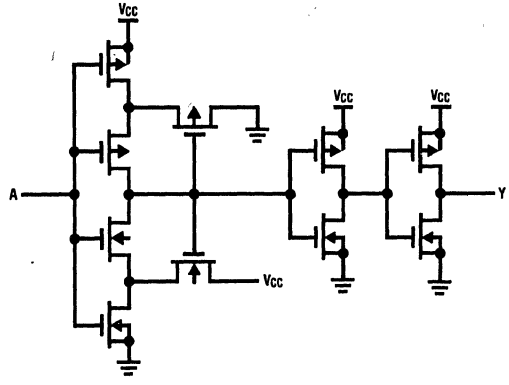
TOP VIEW

TL/F/5105–1

MM54HC14/MM74HC14

54HC14(J) 74HC14(J,N)

Schematic Diagram



TL/F/5105–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_T+	Maximum Positive Going Threshold Voltage		2.0V	1.2	1.5	1.5	1.5	V
			4.5V	2.7	3.15	3.15	3.15	V
			6.0V	3.2	4.2	4.2	4.2	V
V_T−	Minimum Negative Going Threshold Voltage		2.0V	0.7	0.3	0.3	0.3	V
			4.5V	1.8	0.9	0.9	0.9	V
			6.0V	2.2	1.2	1.2	1.2	V
V_H	Hysterisis Voltage	Min	2.0V	0.5	0.2	0.2	0.2	V
			4.5V	0.9	0.4	0.4	0.4	V
			6.0V	1.0	0.6	0.6	0.6	V
		Max	2.0V	0.5	1.2	1.2	1.2	V
			4.5V	0.9	2.25	2.25	2.25	V
			6.0V	1.0	3.0	3.0	3.0	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	22	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

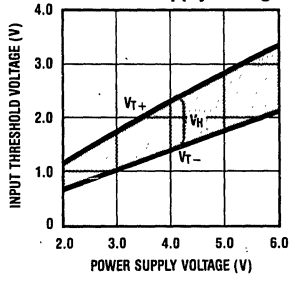
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	11	21	26	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		27				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

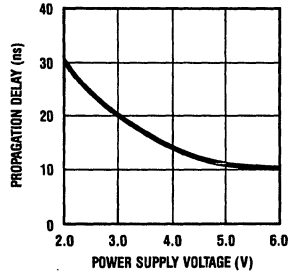
Typical Performance Characteristics

Input Threshold, V_{T+}, V_{T-}, vs Power Supply Voltage



TL/F/5105–3

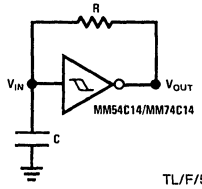
Propagation Delay vs Power Supply



TL/F/5105–4

Typical Applications

Low Power Oscillator



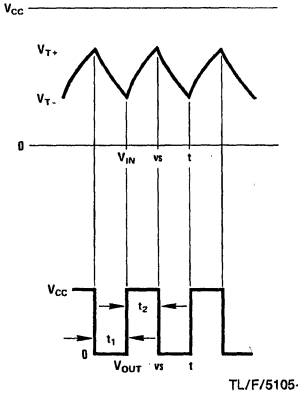
TL/F/5105–5

$$t_1 \approx RC \ln \frac{V_{T+}}{V_{-T}}$$

$$t_2 \approx RC \ln \frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC}-V_{T-})}{V_{T-}(V_{CC}-V_{T+})}}$$

Note: The equations assume $t_1+t_2 \gg t_{pd0}+t_{pd1}$



TL/F/5105–6

National Semiconductor

MM54HC20/MM74HC20 Dual 4-Input NAND Gate

General Description

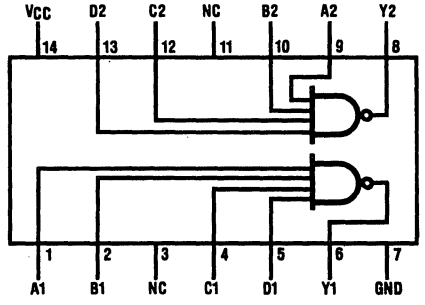
These NAND gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-Well CMOS, to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LSTTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

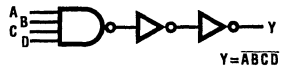


TL/F/5299–1

MM54HC20/MM74HC20

54HC20 (J) 74HC20 (J,N)

Logic Diagram



TL/F/5299–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

4

National Semiconductor

MM54HC27/MM74HC27 Triple 3-Input NOR Gate

General Description

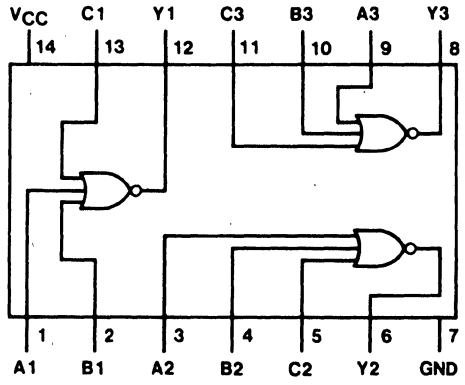
These NOR gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical Propagation Delay: 8 ns
- Wide Operating Supply Voltage Range: 2–6V
- Low Input Current: < 1 μA
- Low Quiescent Supply Current: 40 μA maximum (74HC series)
- Fanout of 10 LS-TTL Loads

Connection Diagram

Dual-In-Line Package



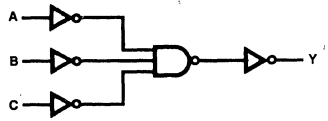
TL/F/5300–1

MM54HC27/MM74HC27

54HC27 (J) 74HC27 (J,N)

Logic Diagram

$$Y = \overline{A + B + C}$$



(1 of 3)

TL/F/5300–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		36				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC30/MM74HC30 8-Input NAND Gate

General Description

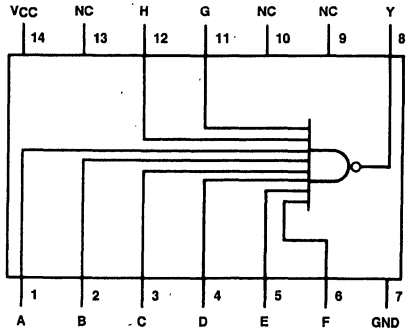
This NAND gate utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. This device has high noise immunity and the ability to drive 10 LSTTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

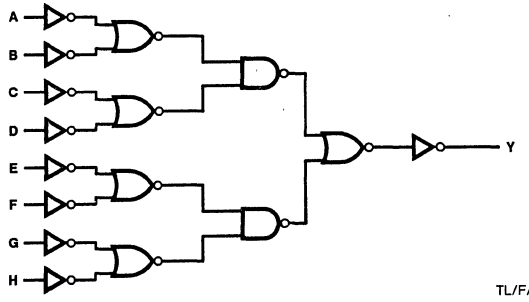


TL/F/5133–1

MM54HC30/MM74HC30

54HC30 (J) 74HC30 (J,N)

Logic Diagram



Y = ABCDEFGH

TL/F/5133–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
DC Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} $\|I_{OUT}\|$≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26		0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		20	30	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	66	160	190	220	ns
			4.5V	23	35	42	49	ns
			6.0V	18	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			34				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC32/MM74HC32 Quad 2-Input OR Gate

General Description

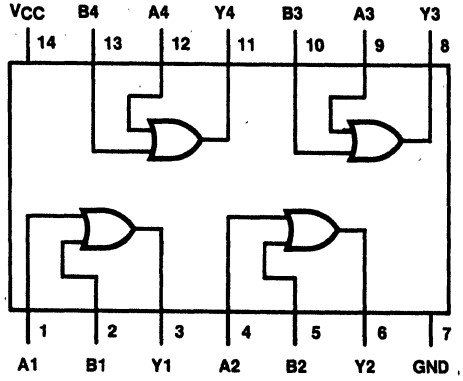
These OR gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

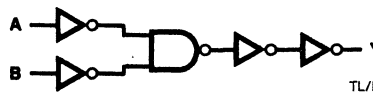


TL/F/5132–1

M54HC32/MM74HC32

54HC32 (J) 74HC32 (J,N)

Logic Diagram



Y = A + B

TL/F/5132–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.7	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	30	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	9	17	21	25	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC42/MM74HC42 BCD-to-Decimal Decoder

General Description

This decoder utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. Data on the four input pins select one of the 10 outputs corresponding to the value of the BCD number on the inputs. An output will go low when selected, otherwise it remains high. If the input data is not a valid BCD number all outputs will remain high. The circuit has high noise immunity and low power consumption usually associated with CMOS circuitry, yet also has speeds comparable to low power Schottky TTL (LS-TTL) circuits, and is capable of driving 10 LS-TTL equivalent loads.

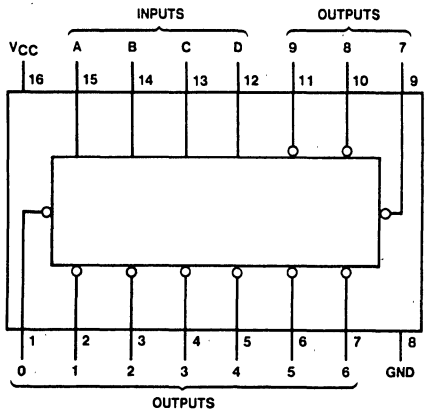
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide supply range: 2V–6V
- Low quiescent current: 80 mA (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-in-line Package



TL/F/5301–1

MM54HC42/MM74HC42

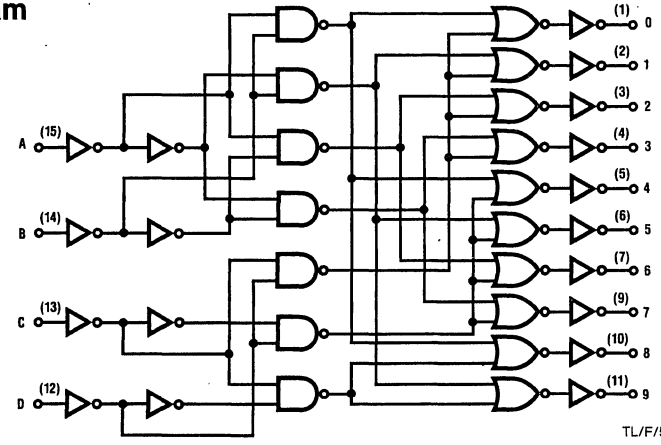
54HC42(J) 74HC42(J,N)

Truth Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level

Logic Diagram



TL/F/5301–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Minimum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		15	25	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	75	150	189	224	ns
			4.5V	17	30	38	45	ns
			6.0V	15	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)						pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HC51/MM74HC51 Dual AND-OR-Invert Gate
MM54HC58/MM74HC58 Dual AND-OR Gate

General Description

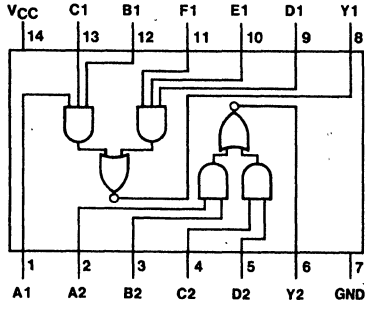
These gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent supply current: 20 μA maximum (74 series)
  74HC
- Low input current: 1 μA maximum
- High output current: 4 mA minimum

Connection Diagram

Dual-In-Line Package

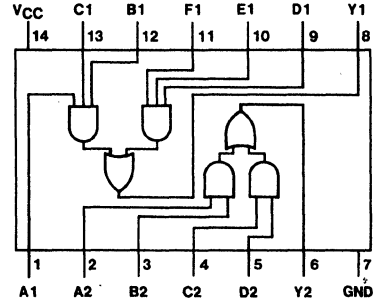


TL/F/5302–1

MM54HC51/MM74HC51

54HC51 (J) 74HC51 (J,N)

Dual-In-Line Package



TL/F/5302–2

MM54HC58/MM74HC58

54HC58 (J) 74HC58 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5 V
			4.5V		3.15	3.15	3.15 V
			6.0V		4.2	4.2	4.2 V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3 V
			4.5V		0.9	0.9	0.9 V
			6.0V		1.2	1.2	1.2 V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9 V
			4.5V	4.5	4.4	4.4	4.4 V
			6.0V	6.0	5.9	5.9	5.9 V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7 V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2 V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1 V
			4.5V	0	0.1	0.1	0.1 V
			6.0V	0	0.1	0.1	0.1 V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4 V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40 μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per AND-OR-Gate)			20			pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC73/MM74HC73 Dual J-K Flip-Flops with Clear

General Description

These J-K Flip-Flops utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent, J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family.

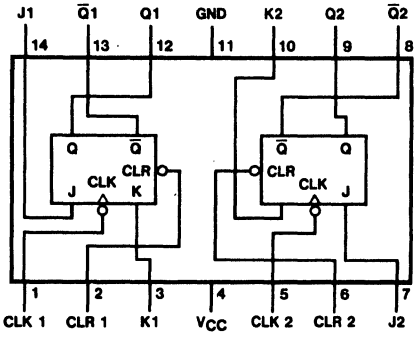
All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5072–1

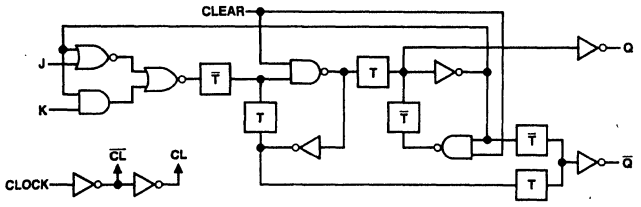
MM54HC73/MM74HC73

54HC73 (J) 74HC73 (J,N)

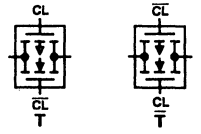
Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

Logic Diagram



TL/F/5304–2



TL/F/5304–3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K to Clock		−3	0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

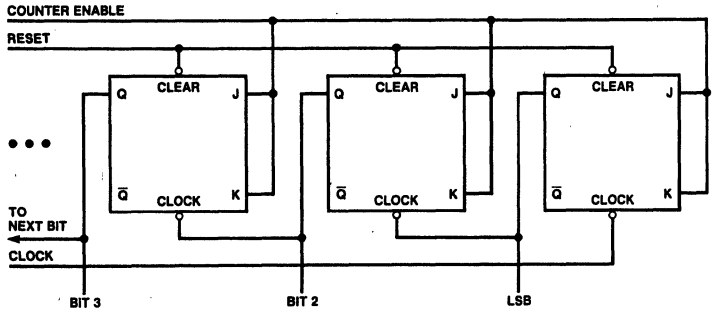
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	100	126	160	185	ns
			4.5V	20	25	32	37	ns
			6.0V	17	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V	126	155	194	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	32	40	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Set Up Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15.4	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

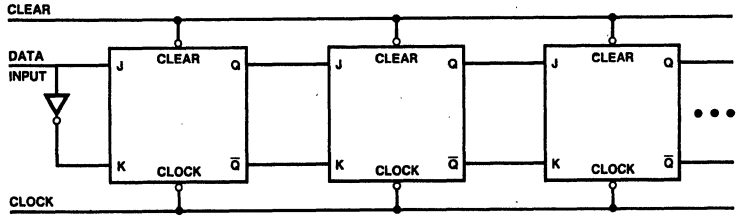
Typical Applications

N Bit binary ripple counter with enable and reset



TL/F/5072–4

N Bit shift register with clear



TL/F/5072–5

National Semiconductor

MM54HC74/MM74HC74
Dual D Flip-Flop with Preset and Clear

General Description

The MM54HC74/MM74HC74 utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

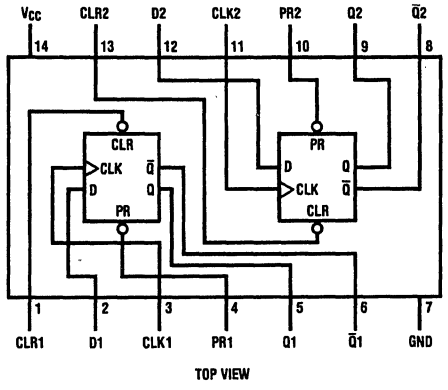
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 40 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5106–1

MM54HC74/MM74HC74

54HC74 (J) 74HC74 (J,N)

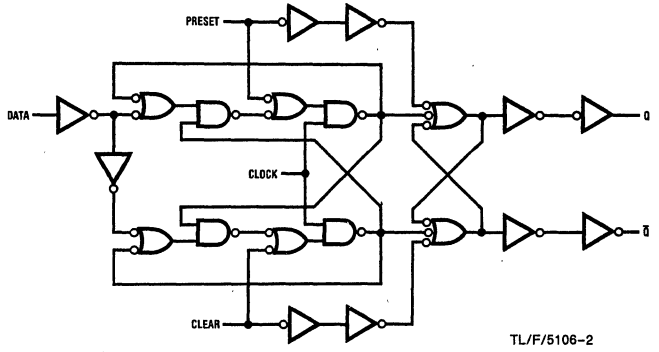
Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Logic Diagram



TL/F/5106–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.3	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear to Q or $\overline{Q}$		25	40	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			5	ns
t_S	Minimum Set Up Time Data to Clock			20	ns
t_H	Minimum Hold Time Clock to Data			0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 32	4 21 25	4 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	88 18 15	175 35 30	221 44 37	261 52 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear To Q or $\overline{Q}$		2.0V 4.5V 6.0V	98 30 28	230 46 39	290 58 49	343 69 58	ns ns ns
t_{REM}	Minimum Removal Time Preset or Clear To Clock		2.0V 4.5V 6.0V		25 5 4	32 6 5	37 7 6	ns ns ns
t_S	Minimum Set Up Time Data to Clock		2.0V 4.5V 6.0V		100 20 17	126 25 21	149 30 25	ns ns ns
t_H	Minimum Hold Time Clock to Data		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum, Pulse Width Clock, Preset or Clear		2.0V 4.5V 6.0V	30 9 8	80 16 14	101 20 17	119 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)						pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

4

National Semiconductor

MM54HC75/MM74HC75
4 Bit Bistable Latch with Q and $\overline{Q}$ Output

General Description

This 4-Bit Latch utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. To achieve the high noise immunity and low power consumption normally associated with standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

This latch is ideally suited for use as temporary storage for binary information processing, input/output, and indicator units. Information present at the data (D) input is transferred to the Q output when the enable (G) is high. The Q output will follow the data input as long as the enable remains high. When the enable goes low, the information that was present at the data input at the time the transition occurred is retained at the Q output until the enable is permitted to go high again.

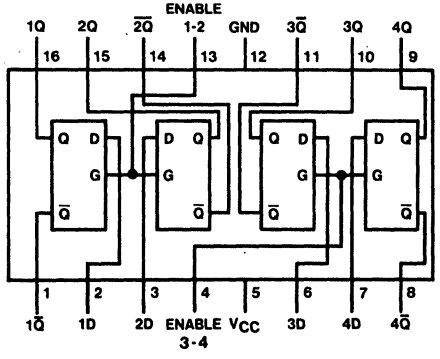
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 12 ns
- Wide operating supply voltage range: 2–6V
- Low input current: < 1 μA
- Low quiescent supply current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5303–1

MM54HC75/MM54HC75

54HC75 (J) 74HC75 (J,N)

Truth Table

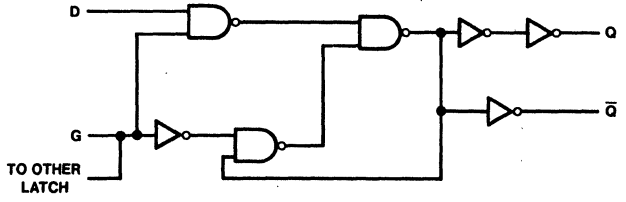
Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level; L = Low Level

X = Don't Care:

Q_0 = The level of Q before the transition of G

Logic Diagram



TL/F/5303–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q		14	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$		10	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Q		16	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$		11	23	ns
t_S	Minimum Set Up Time			20	ns
t_H	Minimum Hold Time		−2	0	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q		2.0V	37	125	156	188	ns
			4.5V	15	25	32	38	ns
			6.0V	14	24	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$		2.0V	29	110	138	165	ns
			4.5V	12	22	28	33	ns
			6.0V	11	19	24	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Q		2.0V	40	145	181	218	ns
			4.5V	18	29	36	44	ns
			6.0V	16	25	31	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$		2.0V	36	125	156	188	ns
			4.5V	15	25	31	38	ns
			6.0V	14	22	28	33	ns
t_S	Minimum Set Up Time Data to Enable		2.0V	40	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	25	ns
t_H	Minimum Hold Time Enable to Data		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_W	Minimum Enable Pulse Width		2.0V	40	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		40				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC76/MM74HC76 Dual J-K Flip-Flops with Preset and Clear

General Description

These high speed (30 MHz minimum) J-K Flip-Flops utilize microCMOS™ Technology, 3.5 micron silicon P-well CMOS, to achieve, the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

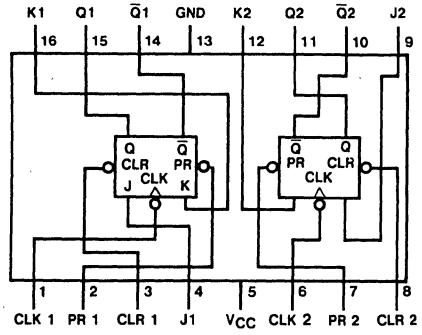
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5074–1

MM54HC76/MM74HC76

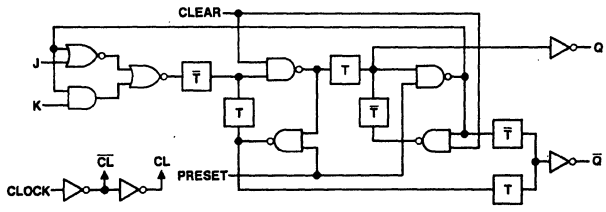
54HC76 (J) 74HC76 (J,N)

Truth Table

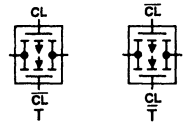
Inputs					Outputs	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed

Logic Diagram



TL/F/5307–2



TL/F/5307–3

MM54HC76/MM74HC76

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		4	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time,		10	20	ns
t_S	Minimum Set Up Time J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K to Clock		−3	0	ns
t_W	Minimum Pulse Width Preset, Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	9 45 53	5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	100 20 17	126 25 21	160 31 27	183 37 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V 4.5V 6.0V	126 25 21	155 31 26	191 39 33	250 47 40	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V 4.5V 6.0V	137 27 23	165 33 28	210 41 35	240 50 40	ns ns ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V 4.5V 6.0V	55 11 9	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Time J or K to Clock		2.0V 4.5V 6.0V	77 15 13	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time J or K from Clock		2.0V 4.5V 6.0V	−3 −3 −3	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum, Pulse Width, Preset, Clear or Clock		2.0V 4.5V 6.0V	55 11 9	80 16 14	100 20 18	120 24 21	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		20.V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

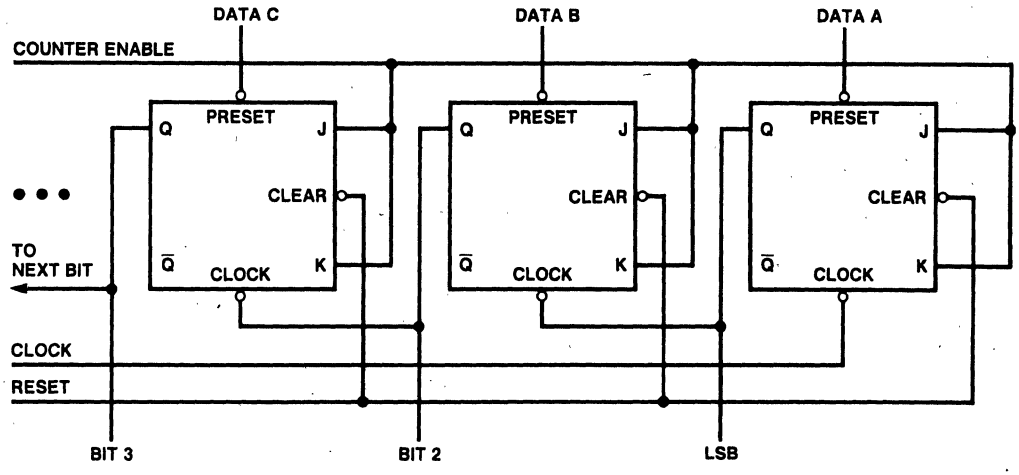
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

4

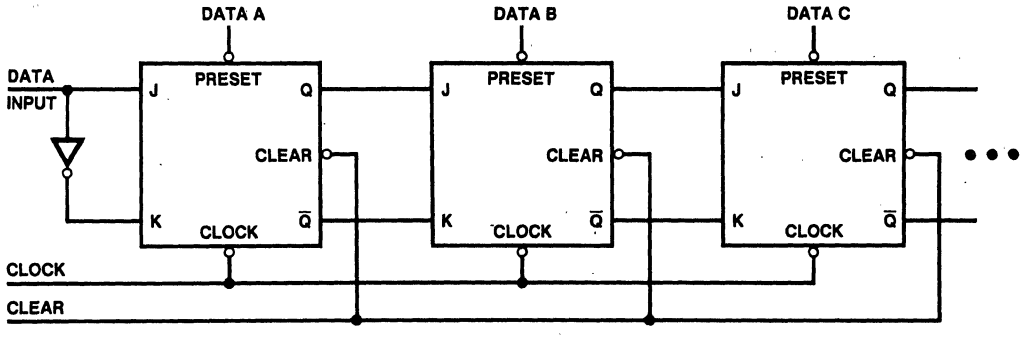
Typical Applications

N Bit presettable ripple counter with enable and reset



TL/F/5074–4

N Bit parallel load/serial load shift register with clear



TL/F/5074–5

National Semiconductor

MM54HC85/MM74HC85 4-Bit Magnitude Comparator

General Description

The MM54HC85/MM74HC85 is a 4-bit magnitude comparator that utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It is designed for high speed comparison of two four bit words. This circuit has eight comparison inputs, 4 for each word; three cascade inputs (A < B, A > B, A = B); and three decision outputs (A < B, A > B, A = B). The result of a comparison is indicated by a high level on one of the decision outputs. Thus it may be determined whether one word is "greater than," "less than," or "equal to" the other word. By connecting the outputs of the least significant stage to the cascade inputs of the next stage, words of greater than four bits can be compared. In addition the least significant stage must have a high level applied to the A = B input, and a low level to the A < B, and A > B inputs.

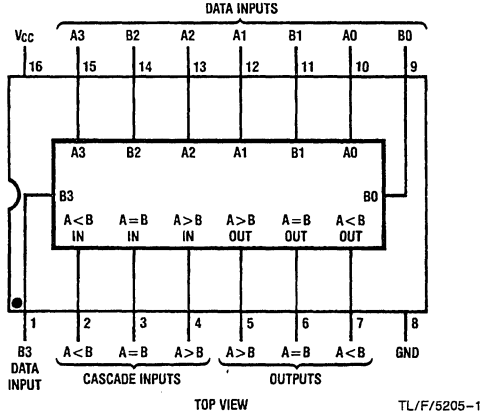
The comparator's outputs can drive 10 low power Schottky TTL (LS-TTL) equivalent loads, and is functionally, and pin equivalent to the 54LS85/74LS85. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 27 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



MM54HC85/MM74HC85

54HC85 (J) 74HC85 (J,N)

Truth Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC Vcc or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A<B or A>B		20	36	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A=B Input to A=B Output		12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cascade Input to Output		13	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A=B		20	30	ns

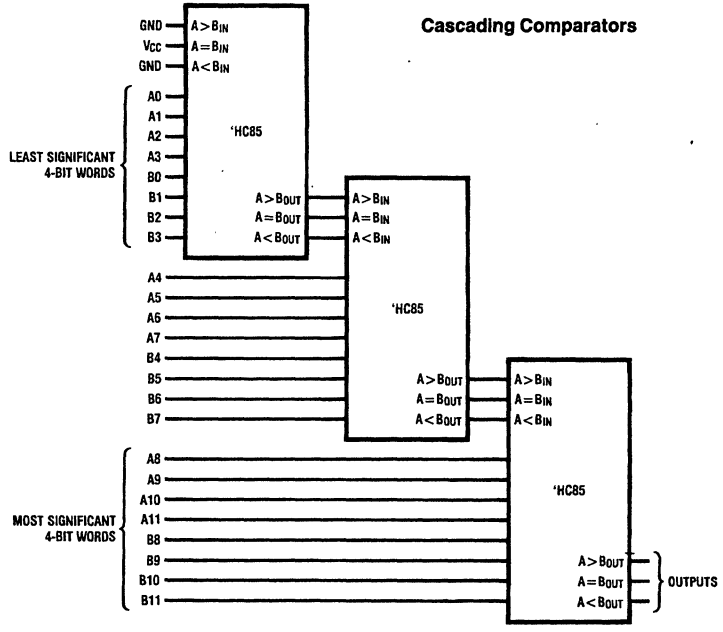
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to Output		2.0V	100	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A=B Output		2.0V	88	175	221	261	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A=B Input to A=B Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cascade Input to Output (except A=B)		2.0V	70	155	195	231	ns
			4.5V	16	31	39	46	ns
			6.0V	13	26	33	39	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

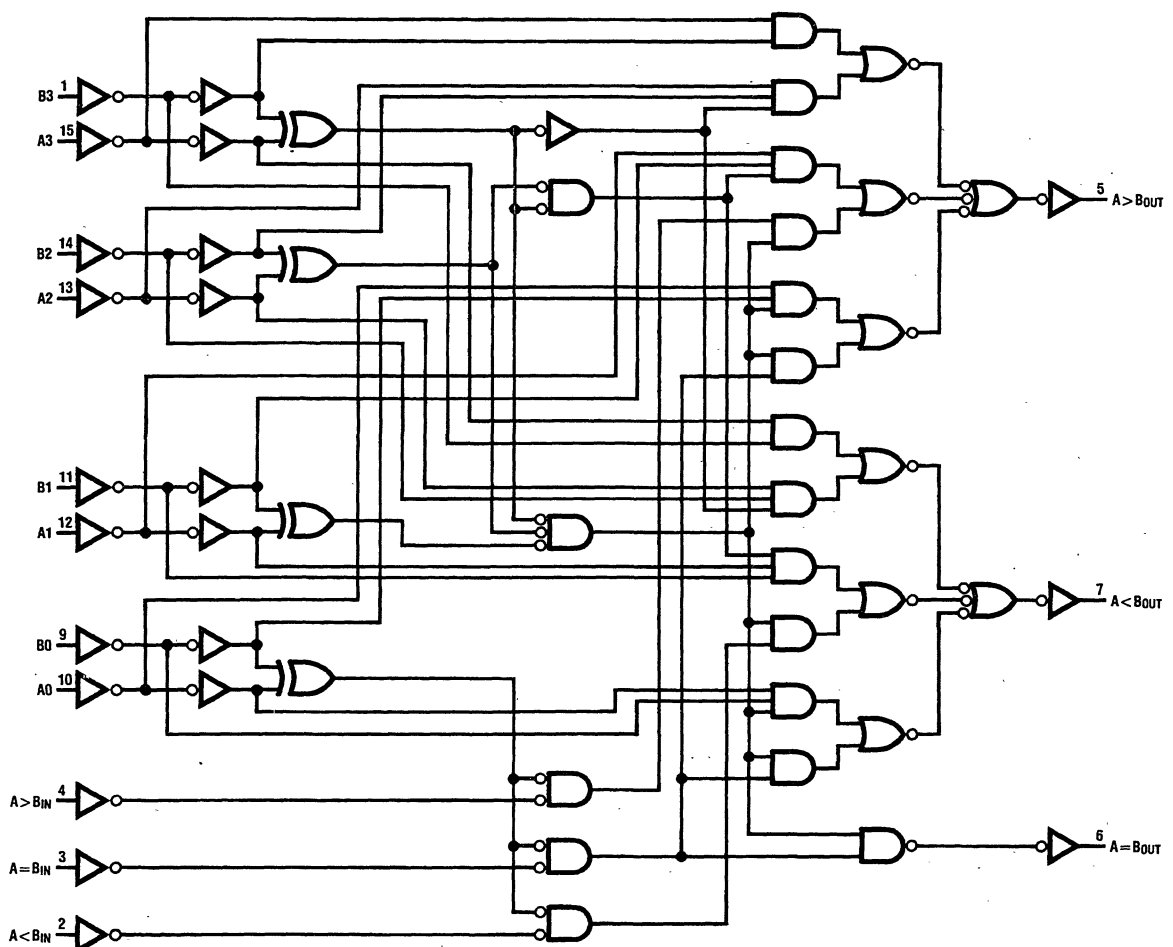
Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Typical Application



TL/F/5205–4

Logic Diagram



TL/F/5205–3

National Semiconductor

MM54HC86/MM74HC86 Quad 2-Input Exclusive OR Gate

General Description

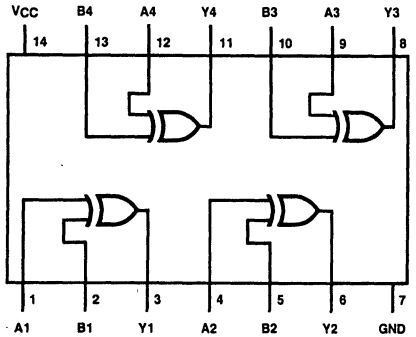
This EXCLUSIVE OR gate utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The MM54HC/74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 9 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 20 μA maximum (74 series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5305–1

MM54HC86/MM54HC86

54HC86 (J) 74HC86 (J,N)

Truth Tables

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC107/MM74HC107
Dual J-K Flip-Flops with Clear

General Description

These J-K Flip-Flops utilize microCMOS™ Technology, 3.5 micron silicon gate P-Well, to achieve the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input.

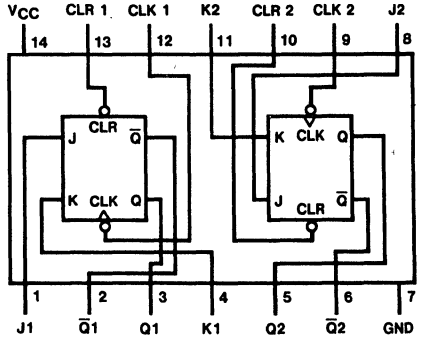
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5304–1

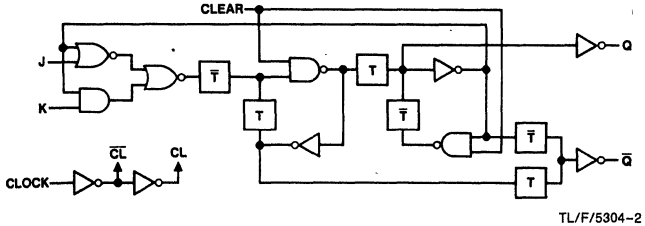
MM54HC107/MM74HC107

54HC107 (J) 74HC107 (J,N)

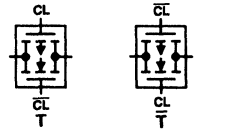
Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

Logic Diagram



TL/F/5304–2



TL/F/5304–3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V		3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

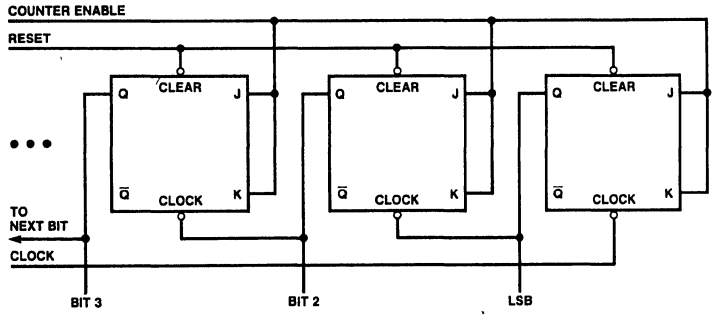
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	100	126	160	185	ns
			4.5V	20	25	32	37	ns
			6.0V	17	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V	126	155	194	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	32	40	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Set Up Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K to Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	10	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Typical Applications

N Bit binary ripple counter with enable and reset



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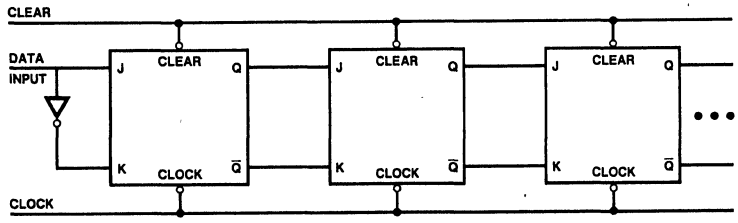
N bit shift register with clear



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Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC109/MM74HC109
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear

General Description

These J-$\overline{K}$ FLIP-FLOPS utilize microCMOS™ Technology, 3.5 micron silicon gate P-Well CMOS to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip flop has independent J, $\overline{K}$ PRESET, CLEAR and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

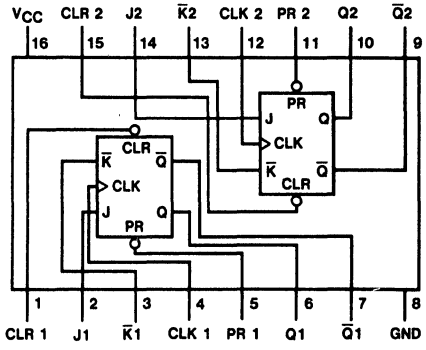
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HC series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5306–1

MM54HC109/MM74HC109

54HC109 (J) 74HC109 (J,N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V		3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V		0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$		21	42	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			5	ns
t_S	Minimum Set Up Time, J or $\overline{K}$ to Clock			20	ns
t_H	Minimum Hold Time, J or $\overline{K}$ to Clock			0	ns
t_W	Minimum Pulse Width: Preset, Clear or Clock		9	16	ns

AC Electrical Characteristics

$C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 31	4 21 24	4 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	88 18 15	175 35 30	221 44 37	261 52 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$		2.0V 4.5V 6.0V	115 23 20	230 46 39	290 58 49	343 69 58	ns ns ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V 4.5V 6.0V	−10 5 3	25 5 4	32 6 5	37 7 6	ns ns ns
t_S	Minimum Set Time J or $\overline{K}$ to Clock		2.0V 4.5V 6.0V		100 20 17	126 25 21	119 30 20	ns ns ns
t_H	Minimum Hold Time Clock to J or K		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Clock, Preset or Clear		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC112/MM74HC112
Dual J-K Flip-Flops with Preset and Clear

General Description

These high speed (30 MHz minimum) J-K Flip-Flops utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

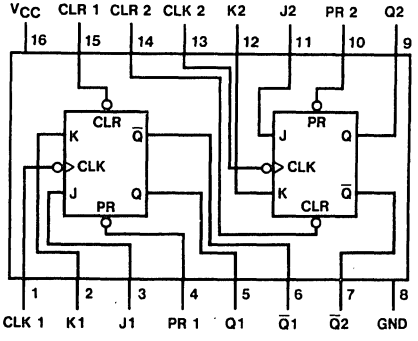
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5307–1

MM54HC112/MM74HC112

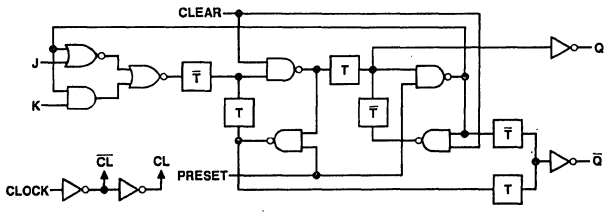
54HC112 (J) 74HC112 (J,N)

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed

Logic Diagrams



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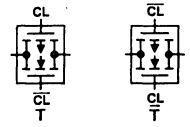
MM54HC112/MM74HC112



TL/F/5307–3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Q or $\overline{Q}$		21	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock		10	20	ns
t_S	Minimum Set Up Time J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width Clock Preset or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

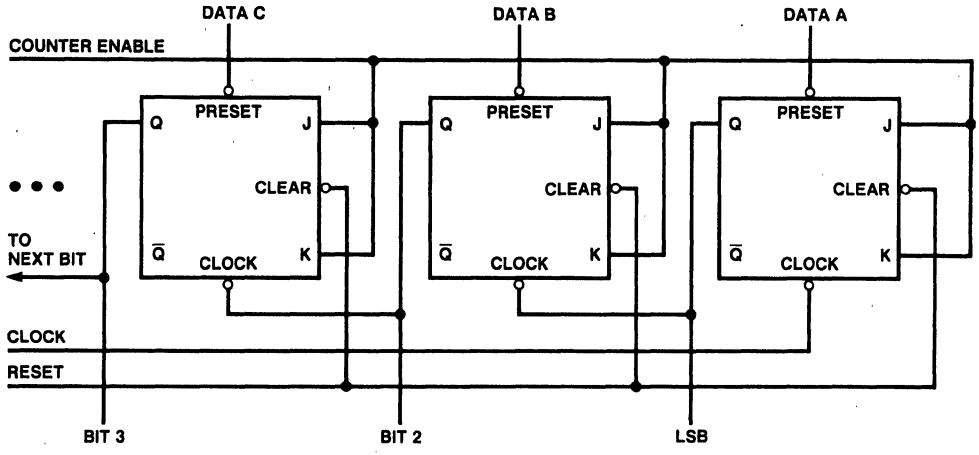
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	9 45 53	5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	100 20 17	126 25 21	160 32 27	183 37 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Q or $\overline{Q}$		2.0V 4.5V 6.0V	126 25 21	155 31 26	191 39 33	250 47 40	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V 4.5V 6.0V	137 27 23	165 33 28	210 41 35	240 50 40	ns ns ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V 4.5V 6.0V	55 11 9.4	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time J or K to Clock		2.0V 4.5V 6.0V	77 15 13	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time J or K from Clock		2.0V 4.5V 6.0V	−3 −3 −3	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Preset, Clear or Clock		2.0V 4.5V 6.0V	55 11 9	80 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

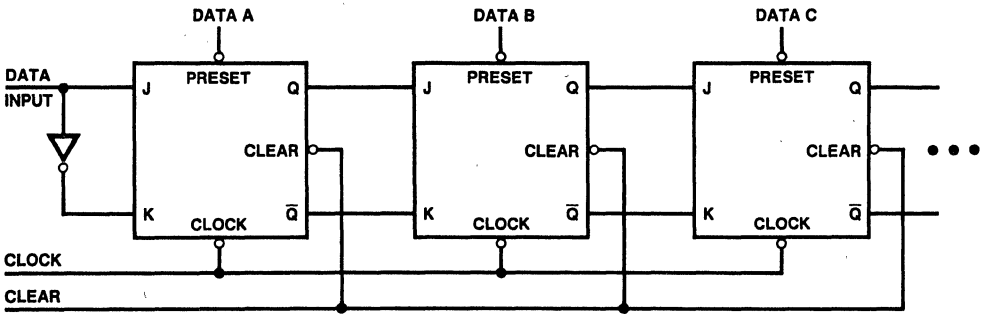
Typical Applications

N Bit presettable ripple counter with enable and reset



TL/F/5074–4

N Bit parallel load/serial load shift register with clear



TL/F/5074–5

National Semiconductor

MM54HC113/MM74HC113
Dual J-K Flip-Flops with Preset

General Description

These high speed J-K Flip-Flops utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and PRESET inputs and Q and $\overline{Q}$ inputs. PRESET is independent of the clock and accomplished by a low level on the input.

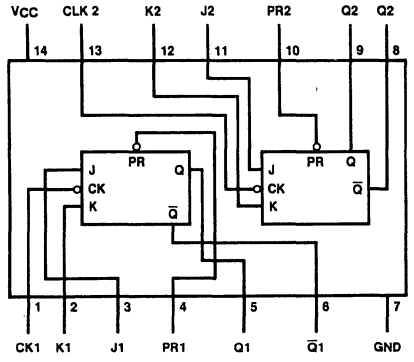
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5073–1

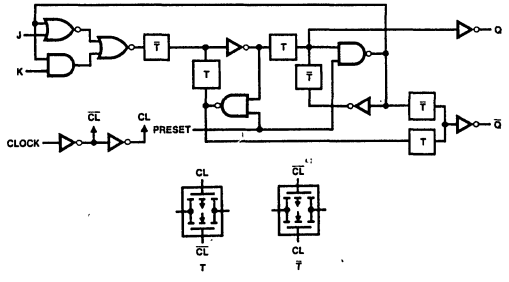
Inputs				Outputs	
PR	CLK	J	K	O	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

MM54HC113/MM74HC113

54HC113 (J) 74HC113 (J,N)

Logic Diagram

MM54HC113/MM74HC113



TL/F/5073–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time, Preset to Clock		10	20	ns
t_S	Minimum Set Up Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time, J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width, Preset, Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

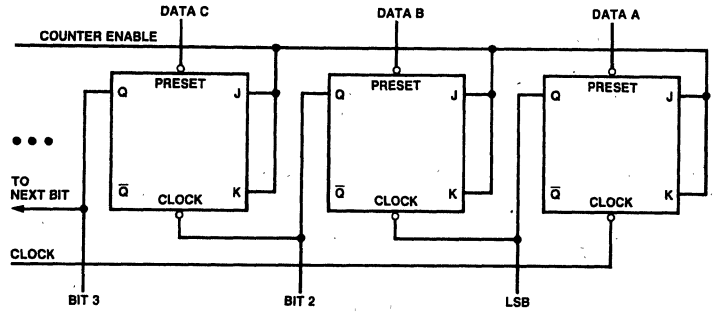
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	100	125	160	183	ns
			4.5V	20	25	32	37	ns
			6.0V	17	33	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V	137	165	206	239	ns
			4.5V	27	33	41	47	ns
			6.0V	23	28	35	40	ns
t_{REM}	Minimum Removal Time Preset to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Set Up Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width, Preset, Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

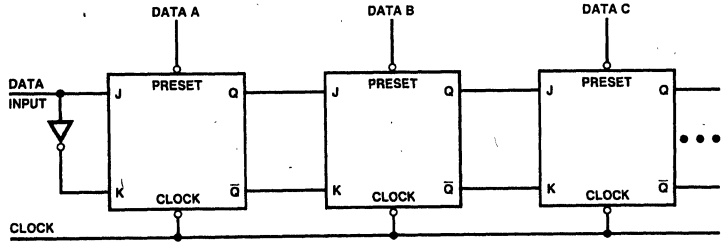
Typical Applications

N Bit presettable binary ripple counter with enable



TL/F/5073–3

N Bit parallel load/serial load shift register



TL/F/5073–4

National Semiconductor

MM54HC123/MM74HC123
Dual Retriggerable Monostable Multivibrator

General Description

The MM54/74HC123 high speed monostable multivibrators (one shots) utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC123 can be triggered on the positive transition of the clear while A is held low and B is held high.

The 'HC123 is retriggerable. That is it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

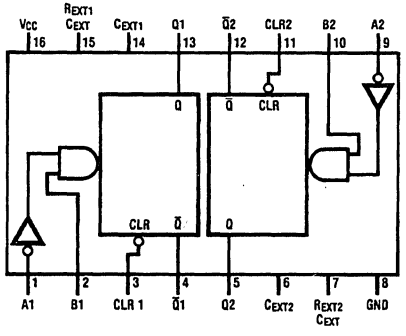
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})(C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs enable infinite signal input rise and fall times.

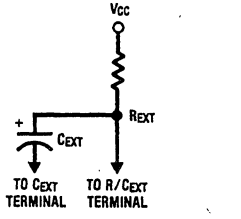
Connection Diagram

Dual-In-Line Package



TL/F/5206–1

Timing Component



TL/F/5206–2

MM54HC123/MM74HC123

54HC123 (J) 74HC123 (J,N)

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (Clear Input) (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤ 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤ 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN}=V_{CC} or GND	6.0V		±0.5	±5.0	±5.0	μA
I_{IN}	Maximum Input Current (All other pins)	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Standby)	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable)	V_{IN}=V_{CC} or GND R/C EXT=0.5V_{CC}	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating:

Plastic "N" Package: −12mW/°C from 65°C to 85°C

Ceramic "J" Package: −12mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

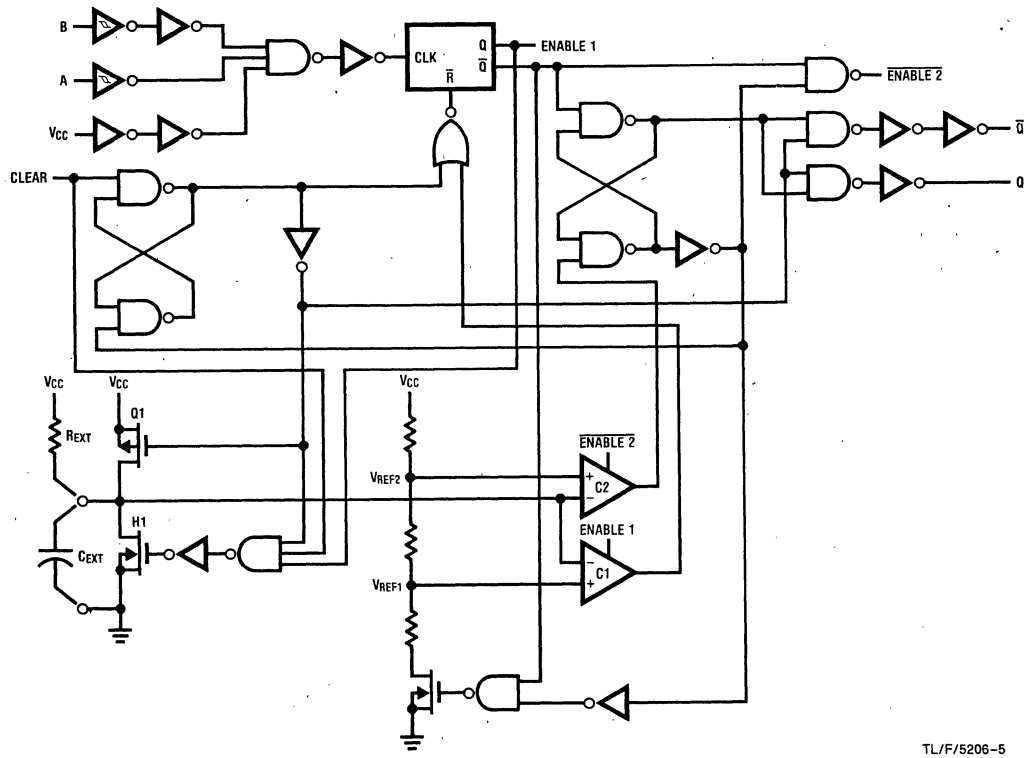
Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		22	33	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C		54HC $T_A=-55$ to 125°C		Units
					Typ	Guaranteed Limits				
t_{PLH}	Maximum Trigger Propagation Delay, A, B or Clear to Q			2.0V	77	169		194	210	ns
				4.5V	26	42		51	57	ns
				6.0V	21	32		39	44	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B or Clear to $\overline{Q}$			2.0V	88	197		229	250	ns
				4.5V	29	48		60	67	ns
				6.0V	24	38		46	51	ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V	54	114		132	143	ns
				4.5V	23	34		41	45	ns
				6.0V	19	28		33	36	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V	56	116		135	147	ns
				4.5V	25	36		42	46	ns
				6.0V	20	29		34	37	ns
t_W	Minimum Pulse Width A, B, Clear			2.0V	57	123		144	157	ns
				4.5V	17	39		37	42	ns
				6.0V	12	21		27	30	ns
t_{REM}	Minimum Clear Removal Time			2.0V		0		0	0	ns
				4.5V		0		0	0	ns
				6.0V		0		0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V		75		95	110	ns
				4.5V		15		19	22	ns
				6.0V		13		16	19	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF		2.0V	1.5					μs
		$R_{EXT}=2$ kΩ		4.5V	450					ns
		$R_{EXT}=6$ kΩ ($V_{CC}=2V$)		6.0V	380					ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	4.5V	1	0.9				ms
			Max	4.5V	1	1.1				ms
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20		20	20	pF
C_{IN}	Maximum Input Capacitance (Other Inputs)				6	10		10	10	pF

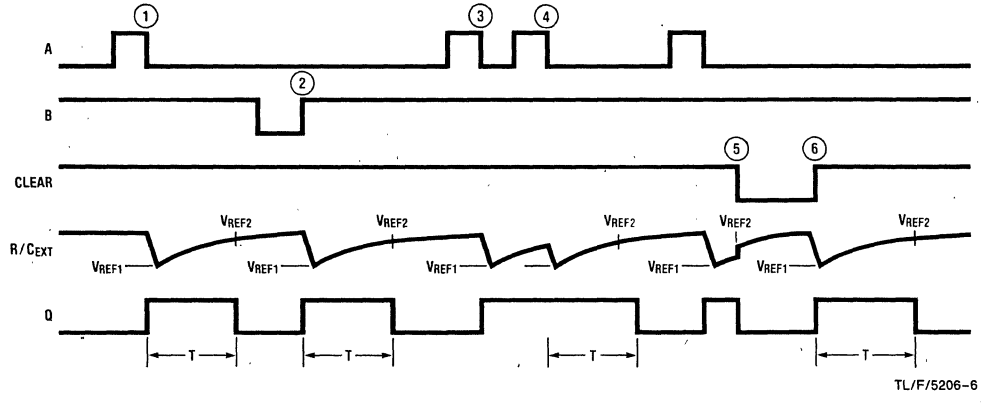
Note 5: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5206–5

Theory of Operation



TL/F/5206–6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
⑤ RESET PULSE SHORTENING
⑥ CLEAR TRIGGER ('HC123, 'HC221 ONLY)

FIGURE 1.

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the one shot is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}②. The 'HC123 can also be triggered when clear goes from GND to V_{CC} (while A is at GND and B is at V_{CC}⑥.)

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC123 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

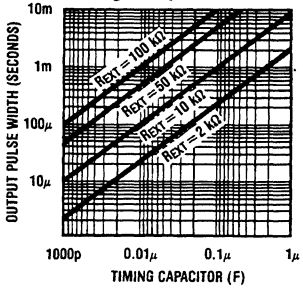
RETRIGGER OPERATION

The 'HC123 is retriggered if a valid trigger occurs ③ followed by another trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin or has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

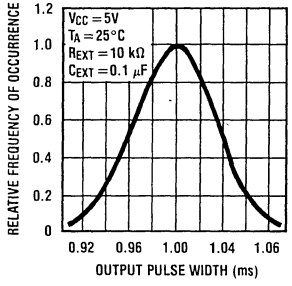
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



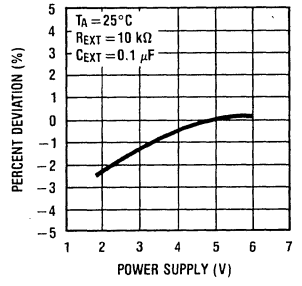
TL/F/5206-7

Typical Distribution of Output Pulse Width, Part to Part



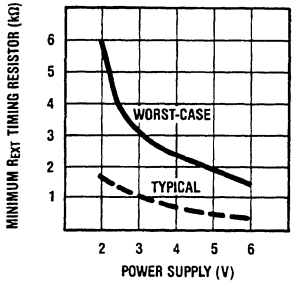
TL/F/5206-8

Typical 1ms Pulse Width Variation vs. Supply



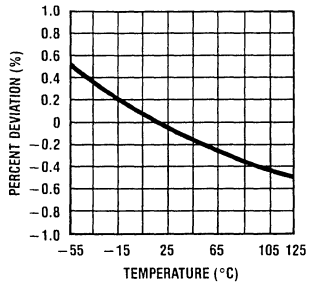
TL/F/5206-9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5206-10

Typical 1ms Pulse Width Variation vs. Temperature



TL/F/5206-11

4

National Semiconductor

MM54HC125/MM74HC125
MM54HC126/MM74HC126 TRISTATE® QUAD BUFFERS

General Description

These are general purpose TRI-STATE high speed non-inverting buffers utilize microCMOS™ technology, 3.5 micron silicon gate P-well CMOS. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The MM54HC125/MM74HC125 require the TRI-STATE control input C to be taken high to put the output into the high impedance condition, whereas the MM54HC126/MM74HC126 requires the control input to be low to put the output into high impedance.

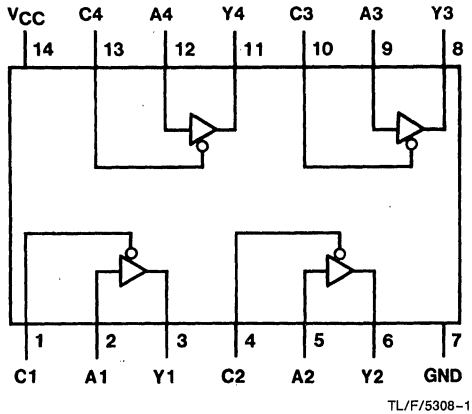
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC)
- Fanout of 15 LS-TTL loads

Connection Diagrams

Dual-In-Line

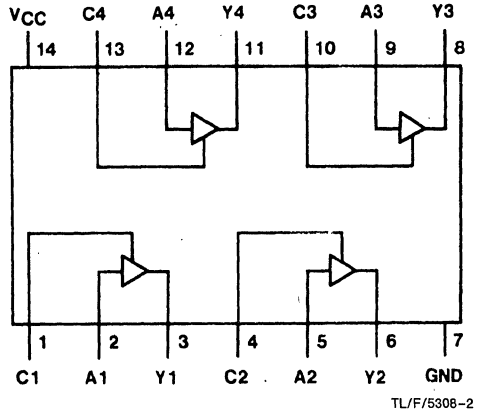


TL/F/5308–1

MM54HC125/MM74HC125

54HC125 (J) **54HC125 (J,N)**

Dual-In-Line



TL/F/5308–2

MM54HC126/MM74HC126

54HC126 (J) **54HC126 (J,N)**

Truth Tables

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Z

Inputs		Output
A	C	Y
H	H	H
L	H	L
X	L	Z

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.74	5.48	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{OZ}	Maximum Tri-State Output Leakage Currrent	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND C_n=Disabled	6.0V		±0.5	±5	±10	μA
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		13	18	ns
t_{PZH}	Maximum Output Enable Time to High Level	$R_L=1$ kΩ	13	25	ns
t_{PHZ}	Maximum Output Disable Time from High Level	$R_L=1$ kΩ $C_L=5$ pF	17	25	ns
t_{PZL}	Maximum Output Enable Time to Low Level	$R_L=1$ kΩ	18	25	ns
t_{PLZ}	Maximum Output Disable Time from Low Level	$R_L=1$ kΩ $C_L=5$ pF	13	25	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	Temperature °C				Units
				54HC/74HC $T_A=25°C$		74HC −40 to 85°C	54HC −55 to 125°C	
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	8	17	21	25	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	$C_L=150$ pF	2.0V	35	130	163	195	ns
			4.5V	14	26	33	39	ns
			6.0V	12	22	28	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=150$ pF $R_L=1$ kΩ	2.0V	35	140	175	210	ns
			4.5V	15	28	35	42	ns
			6.0V	13	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	30	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{OUT}	Output Capacitance Outputs			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) Enabled Disabled		45 6				pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC132/MM74HC132 Quad 2-Input NAND Schmitt Trigger

General Description

The MM54HC132/MM74HC132 utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

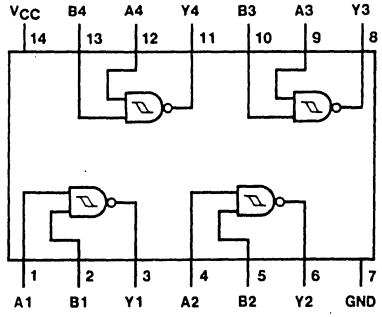
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at $V_{CC}=4.5V$.

Connection Diagram

Dual-In-Line Package

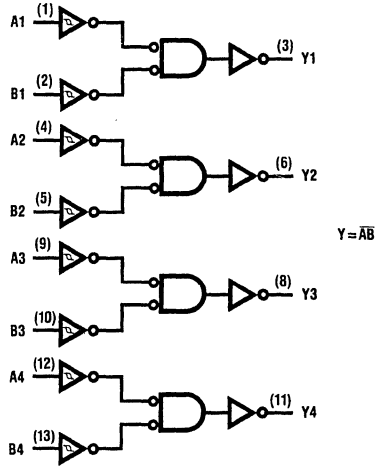


TL/F/5309–1

MM54HC132/MM74HC132

54HC132 (J) 74HC132 (J,N)

Logic Diagram



$Y=\overline{AB}$

TL/F/5309–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits		
V_{T+}	Positive Going Threshold Voltage		Min	2.0V		1.0	0.95	0.95	V
			Max			1.5	1.5	1.5	V
			Min	4.5V		2.30	2.25	2.25	V
			Max			3.15	3.15	3.15	V
			Min	6.0V		3.0	2.95	2.95	V
			Max			4.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage		Min	2.0V		0.3	0.3	0.3	V
			Max			0.8	0.85	0.85	V
			Min	4.5V		0.9	0.9	0.9	V
			Max			2.0	2.05	2.05	V
			Min	6.0V		1.2	1.2	1.2	V
			Max			2.3	2.35	2.35	V
V_H	Hysterisis Voltage		Min	2.0V		0.2	0.2	0.2	V
			Max	2.0V		1.2	1.2	1.2	V
			Min	4.5V		0.4	0.4	0.4	V
			Max	4.5V		2.25	2.25	2.25	V
			Min	6.0V		0.6	0.6	0.6	V
			Max	6.0V		3.0	3.0	3.0	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} |I_{OUT}| ≤ 20 μA		2.0V	2.0	1.9	1.9	1.9	V
				4.5V	4.5	4.4	4.4	4.4	V
				6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} |I_{OUT}| ≤ 4.0 mA		4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}| ≤ 5.2 mA		6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} |I_{OUT}| ≤ 20 μA		2.0V	0	0.1	0.1	0.1	V
				4.5V	0	0.1	0.1	0.1	V
				6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} |I_{OUT}| ≤ 4.0 mA		4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}| ≤ 5.2 mA		6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)						pF
C_{IN}	Maximum Input Capacitance				5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC133/MM74HC133 13-Input NAND Gate

General Description

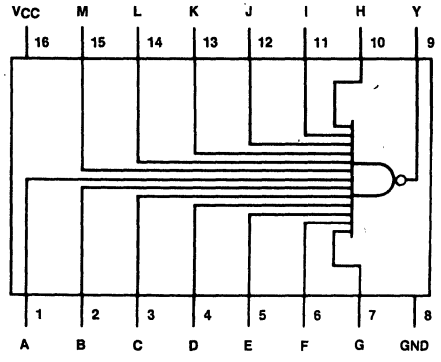
This NAND gate utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LSTTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

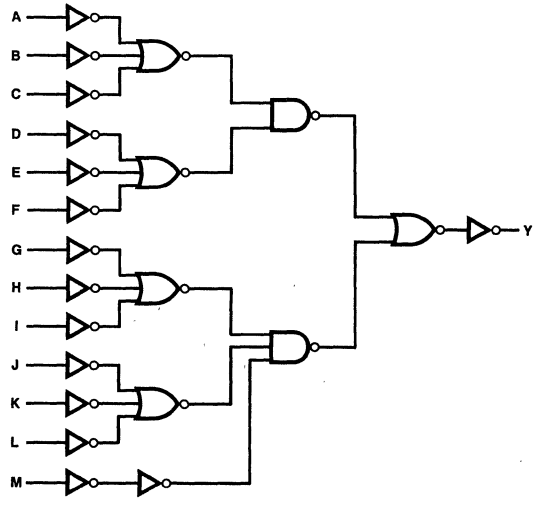
Dual-In-Line Package



TL/F/5134–1

MM54HC133/MM74HC133
54HC133 (J) 74HC133 (J,N)

Logic Diagram



TL/F/5134–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		20	30	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	66	160	190	220	ns
			4.5V	23	35	42	49	ns
			6.0V	18	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			34				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

PRELIMINARY

National Semiconductor

MM54HC137/MM74HC137 3-to-8 Line Decoder With Address Latches (Inverted Output)

General Description

This device utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to implement a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

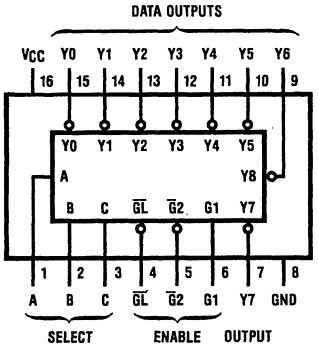
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing.
- Fanout of 10 LS-TTL loads.

Connection Diagram

Dual-In-Line Package

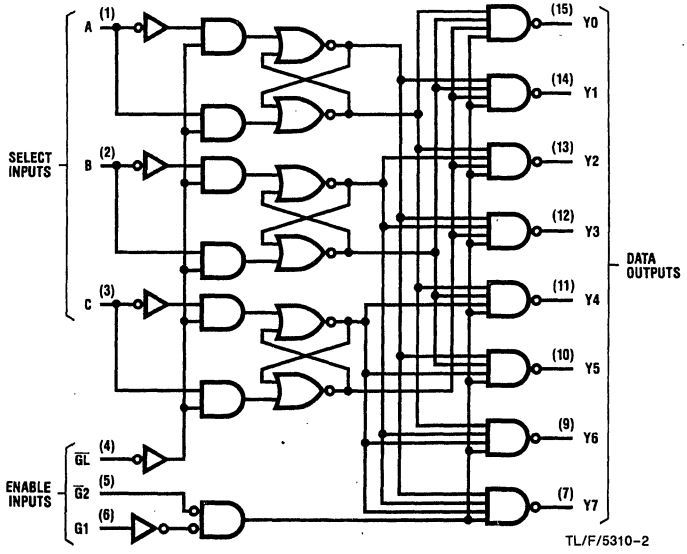


TL/F/5310–1

MM54HC137/MM74HC137

54HC137 (J) 74HC137 (J,N)

Functional Block Diagram



TL/F/5310–2

Truth Table

Inputs						Outputs							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address L; all others, H							

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V		3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V		0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		14	29	ns
t_{PHL}	Maximum Propagation Delay, A, B or C to any Y Output		20	42	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		12	22	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		15	34	ns
t_{PLH}	Maximum Propagation Delay G1 to any Output		13	25	ns
t_{PHL}	Maximum Propagation Delay GL to any Output		17	34	ns
t_{PLH}	Maximum Propagation GL to Output		15	30	ns
t_{PHL}	Maximum Propagation Delay GL to Output		22	34	ns
t_S	Minimum Set Up Time at A, B and C inputs			20	ns
t_H	Minimum Hold Time at A, B and C inputs			0	ns
t_W	Minimum Pulse Width of enabling pulse at $\overline{GL}$			16	ns

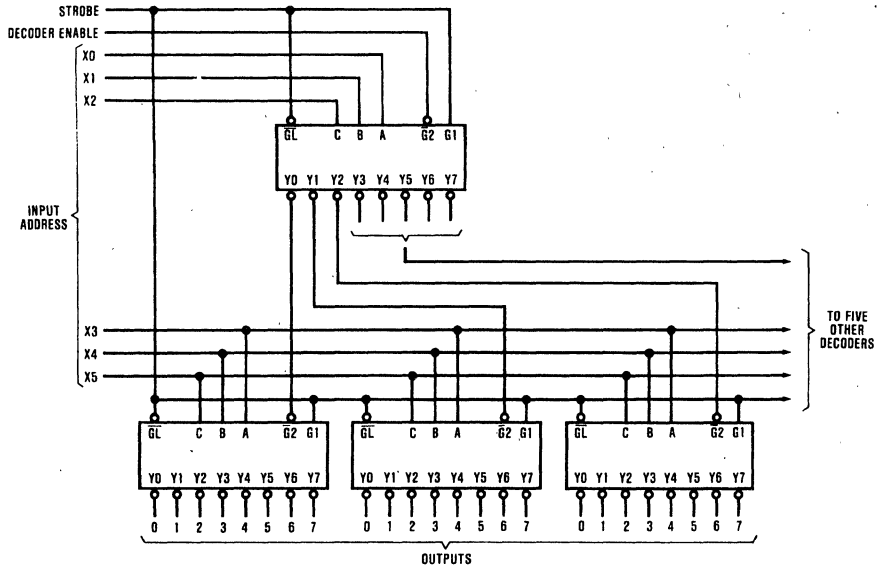
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		2.0V 4.5V 6.0V	85 17 14	170 34 29	214 43 36	253 51 43	ns ns ns
t_{PHL}	Maximum Propagation Delay A, B or C to any Y Output		2.0V 4.5V 6.0V	120 24 20	240 48 41	302 60 51	358 72 61	ns ns ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		2.0V 4.5V 6.0V	65 13 11	130 26 22	164 33 28	194 39 33	ns ns ns
t_{PLH}	Maximum Propagation Delay G1 to Output		2.0V 4.5V 6.0V	75 15 13	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}	Maximum Propagation Delay G1 to Output		2.0V 4.5V 6.0V	98 20 17	195 39 33	246 49 42	291 58 49	ns ns ns
t_{PLH}	Maximum Propagation Delay GL to Output		2.0V 4.5V 6.0V	88 18 15	175 35 30	221 44 37	261 52 44	ns ns ns
t_{PHL}	Maximum Propagation Delay GL to Output		2.0V 4.5V 6.0V	125 25 21	250 50 43	315 63 54	373 75 63	ns ns ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$, to any Y Output		2.0V 4.5V 6.0V	98 20 17	195 39 33	246 49 42	291 58 49	ns ns ns
t_S	Minimum Set Up Time at A, B and C inputs		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time at A, B and C inputs		2.0V 4.5V 6.0V		50 10 8	63 13 11	75 15 13	ns ns ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		2.0V 4.5V 6.0V		80 16 14	100 20 18	120 24 21	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)			75				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Typical Application



TL/F/5310–3

6-Line to 64-Line Decoder with Input Address Storage

National Semiconductor

MM54HC138/MM74HC138 3-to-8 Line Decoder

General Description

This decoder utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and is well suited to memory address decoding or data routing applications. The circuit features high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM54HC138/MM74HC138 has 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, $\overline{G2A}$ and $\overline{G2B}$) are provided to ease the cascading of decoders.

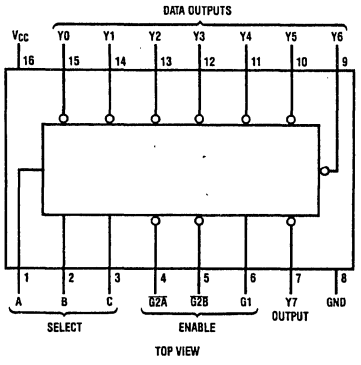
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

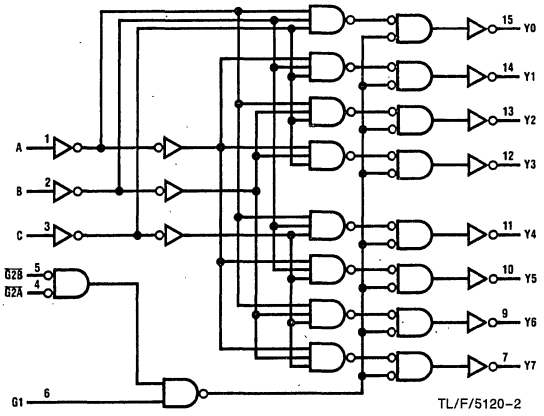


TL/F/5120–1

MM54HC138/MM74HC138

54HC138 (J) 74HC138 (J,N)

Logic Diagram



TL/F/5120–2

Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2} = G2A + G2B$

H = high level, L = low level, X = don't care

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, Binary Select to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay, Binary Select to any Output		28	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, G1 to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		23	30	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		18	25	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay Binary Select to any Output Low to High		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}	Maximum Propagation Delay Binary Select to any Output High to Low		2.0V	100	200	252	298	ns
			4.5V	20	40	40	60	ns
			6.0V	17	34	43	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay G1 to any Output		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	82	175	221	261	ns
			4.5V	28	35	44	52	ns
			6.0V	22	30	37	44	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			3	10	10	10	μF
C_{PD}	Power Dissipation Capacitance	(Note 5)		75				μF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

4

National Semiconductor

MM54HC139/MM74HC139 Dual 2-To-4 Line Decoder

General Description

This decoder utilizes microCMOS™ Technology,, 3.5 micron silicon gate P-well CMOS, and is well suited to memory address decoding or data routing applications. It possesses the high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM54HC139/MM74HC139 contain two independent one-of-four decoders each with a single active low enable input (G1, or G2). Data on the select inputs (A1, and B1 or A2, and B2) cause one of the four normally high outputs to go low.

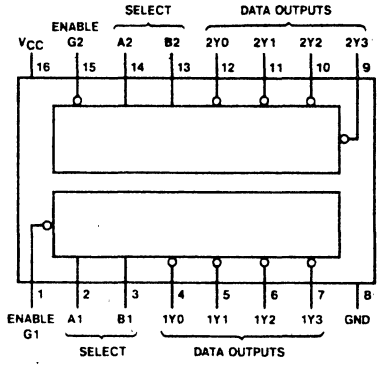
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally as well as pin equivalent to the 54LS139/74LS139. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delays —
  Select to outputs (4 delays): 18 ns
  Select to output (5 delays): 28 ns
  Enable to output: 20 ns
- Low power: 40 μW quiescent supply power
- Fanout of 10 LS-TTL devices
- Input current maximum 1 μA, typical 10 pA

Connection Diagram

Dual-In-Line



TL/F/5311–1

MM54HC139/MM74HC139

54HC139 (J) 74HC139 (J,N)

Truth Table

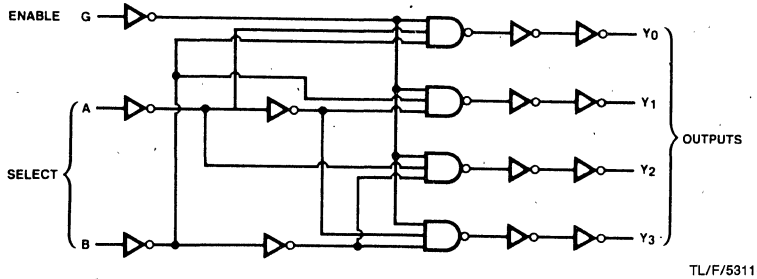
'HC139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

½ MM54HC139/MM74HC139



TL/F/5311–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 4 levels of delay		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 5 levels of delay		28	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to any Output		19	30	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 4 levels of delay		2.0V	110	175	219	254	ns
			4.5V	22	35	44	51	ns
			6.0V	18	30	38	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 5 levels of delay		2.0V	165	220	275	320	ns
			4.5V	33	44	55	64	ns
			6.0V	28	38	47	54	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to any Output		2.0V	115	175	219	254	ns
			4.5V	23	35	44	51	ns
			6.0V	19	30	38	44	ns
t_{TLH}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			3	10	10	10	μF
C_{PD}	Power Dissipation Capacitance (Note 5)	(Note 5)		75				μF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC147/MM74HC147 10-to-4 Line Priority Encoder

General Description

This high speed 10-to-4 Line Priority Encoder utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits. This device is fully buffered, giving it a fanout of 10 LS-TTL loads.

The MM54HC147/MM74HC147 features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at the low logic level.

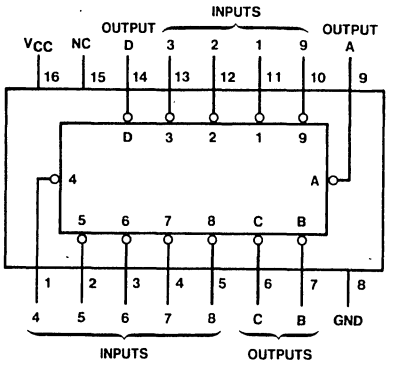
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent power consumption: 40 μW maximum at 25°C
- High speed: 31 ns propagation delay (typical)
- Very low input current: 10^{-5} μA typical
- Wide supply range: 2V to 6V

Connection Diagram

Dual-In-Line Package

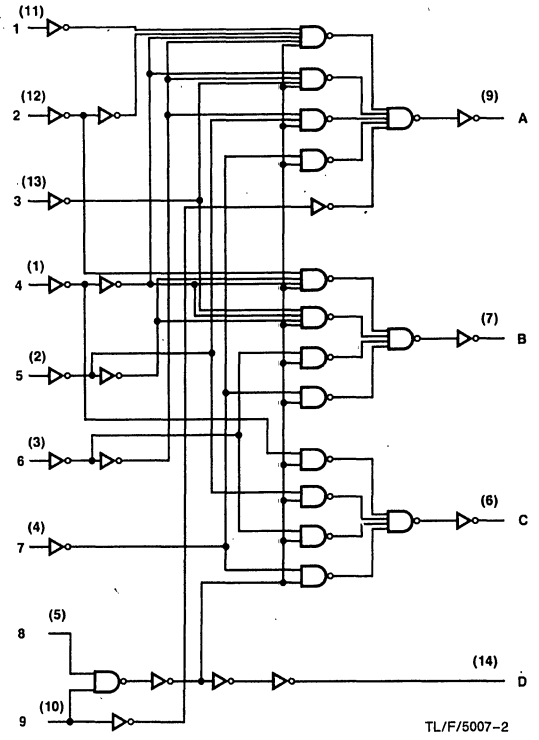


TL/F/5007–1

MM54HC147/MM74HC147

54HC147 (J) 74HC147 (J,N)

Logic Diagram



TL/F/5007–2

Truth Table

Inputs									Outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Logic Level, L = Low Logic Level, X = Irrelevant

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.7	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		31	38	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	181	220	275	319	ns
			4.5V	36	44	55	64	ns
			6.0V	31	37	47	54	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		180				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HC149/MM74HC149
8 Line to 8 Line Priority Encoder

General Description

This priority encoder utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority encoder accepts 8 input request lines, $\overline{RI7}$–$\overline{RI0}$, and outputs 8 lines, $\overline{RO7}$–$\overline{RO0}$. It is the logical combination of a '148 8–3 line priority encoder driving a '138 3–8 line decoder. Only one request output can be low at a time. The output that is low is dependent on the highest priority request that is low. The order of priority is $\overline{RI7}$ highest and $\overline{RI0}$ lowest. Also provided is and enable input, $\overline{RQE}$, which when high forces all outputs high. A request output is also provided, $\overline{RQP}$, which goes low when any $\overline{RQP}$ is active.

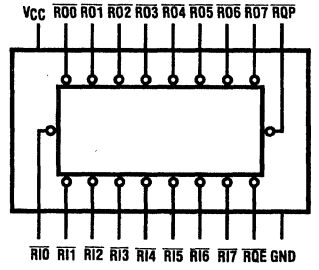
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and Ground.

Features

- Propagation delay: 15 ns typ.
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA max (74HC series)
- Wide input noise immunity

Connection Diagram

Dual-In-Line Package



TL/F/5312–1

MM54HC149/MM74HC149

54HC149 (J) 74HC149 (J,N)

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=15 pF, t_r=t_f=6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay RIn to Any Output		15	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{RQP}$ to Any Output		16	26	ns

AC Electrical Characteristics

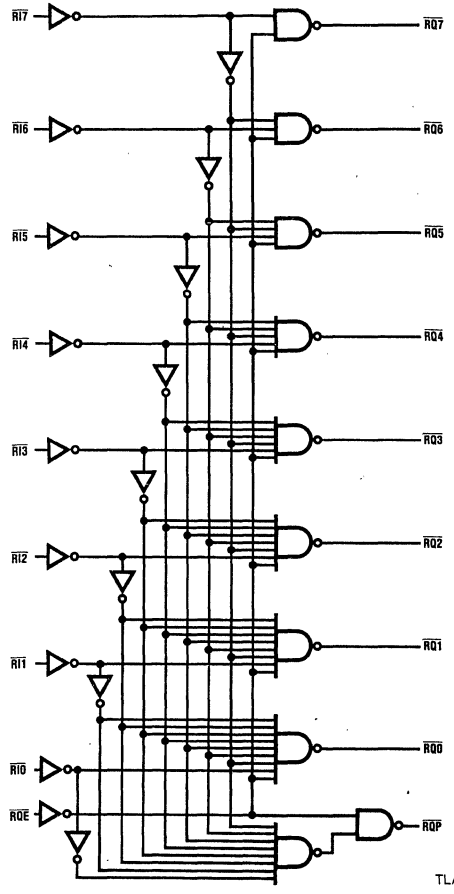
V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay RIn to Any Output		2.0V 4.5V 6.0V	60 19 16	140 28 24	175 36 30	210 42 36	ns ns ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay $\overline{RQP}$ to Any Output		2.0V 4.5V 6.0V	70 22 18	155 31 26	190 39 33	230 46 39	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance Note 5				70			pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Simplified Logic Diagram



TL/F/5312–2

National Semiconductor

MM54HC151/MM74HC151 8-Channel Digital Multiplexer

General Description

This high speed DIGITAL MULTIPLEXER utilizes micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM54HC151/MM74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output high and the Y output low.

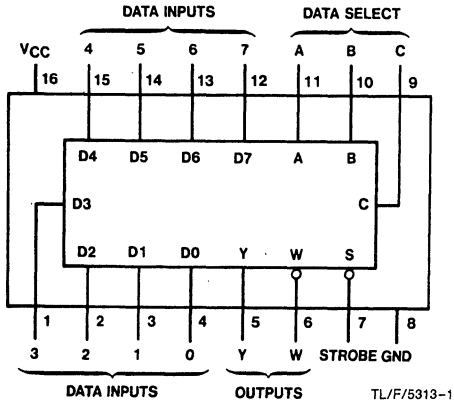
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay data select to output Y: 26 ns
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 4 mA minimum

Connection Diagram

Dual-In-Line



TL/F/5313–1

MM54HC151/MM74HC151

54HC151 (J) 74HC151 (J,N)

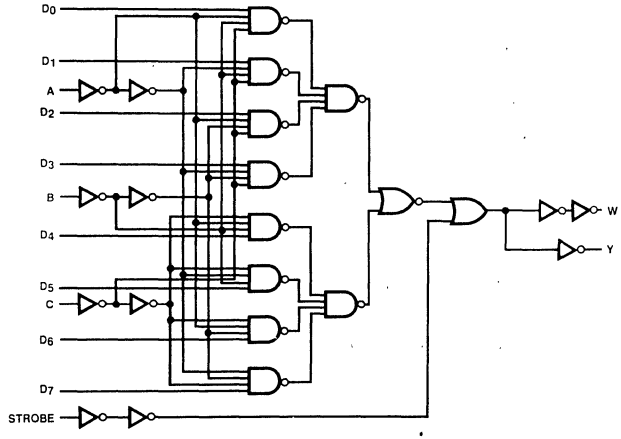
Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

D0, D1...D7 = the level of the respective D input

Logic Diagram



TL/F/5313–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		24	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		17	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		16	21	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V	90	205	256	300	ns
			4.5V	31	41	51	60	ns
			6.0V	26	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		2.0V	95	205	256	300	ns
			4.5V	32	41	51	60	ns
			6.0V	27	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to Y		2.0V	70	195	244	283	ns
			4.5V	27	39	49	57	ns
			6.0V	23	33	41	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		2.0V	75	185	231	268	ns
			4.5V	29	37	46	54	ns
			6.0V	25	32	40	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		2.0V	50	140	175	203	ns
			4.5V	21	28	35	41	ns
			6.0V	18	24	30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		2.0V	45	127	159	185	ns
			4.5V	20	25	32	37	ns
			6.0V	17	22	28	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC153/MM74HC153 Dual 4-Input Multiplexer

General Description

This 4-to-1 line multiplexer utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It has the low power consumption and high noise immunity of standard CMOS integrated circuits. This device is fully buffered, allowing it to drive 10 LS-TTL loads. Information on the data inputs of each multiplexer is selected by the address on the A and B inputs, and is presented on the Y outputs. Each multiplexer possesses a strobe input which enables it when taken to a low logic level. When a high logic level is applied to a strobe input, the output of its associated multiplexer is taken low.

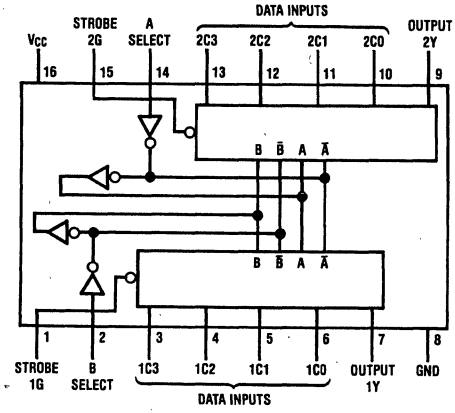
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5107–1

TOP VIEW

MM54HC153/MM74HC153

54HC153 (J) 74HC153 (J,N)

Truth Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = don't care.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.3	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		26	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any Data to Y		20	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y		8	15	ns

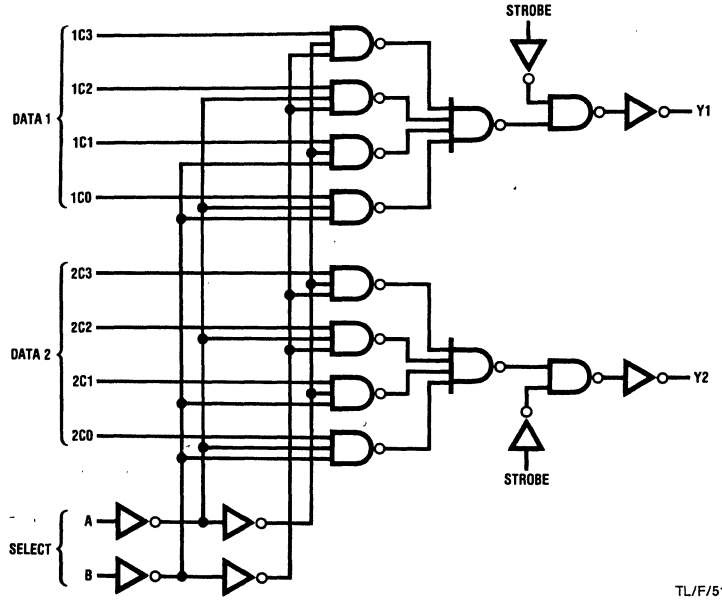
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		2.0V	131	158	198	237	ns
			4.5V	29	35	44	52	ns
			6.0V	25	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any Data to Y		2.0V	99	126	158	189	ns
			4.5V	22	28	35	42	ns
			6.0V	19	23	29	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y		2.0V	50	86	108	129	ns
			4.5V	12	19	24	29	ns
			6.0V	10	16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)(per package) Outputs Enabled		90				pF
		Outputs Disabled		25				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5107–2

National Semiconductor

MM54HC154/MM74HC154 4-to-16 Line Decoder

General Description

This decoder utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and is well suited to memory address decoding or data routing applications. It possesses high noise immunity, and low power consumption of CMOS with speeds similar to low power Schottky TTL circuits.

The MM54HC154/MM74HC154 have 4 binary select inputs (A, B, C, and D). If the device is enabled these inputs determine which one of the 16 normally high outputs will go low. Two active low enables ($\overline{G1}$ and $\overline{G2}$) are provided to ease cascading of decoders with little or no external logic.

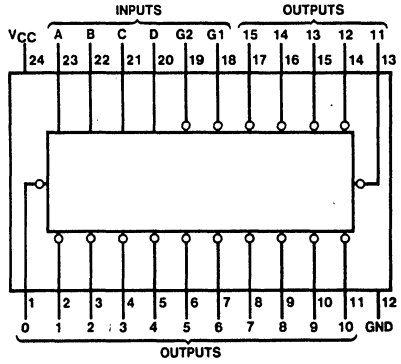
Each output can drive 10 low power Schottky TTL equivalent loads, and is functionally and pin equivalent to the 54LS154/74LS154. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 21 ns
- Power supply quiescent current: 80 μA (74HC)
- Wide power supply voltage range: 2–6V
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5122–1

TOP VIEW
MM54HC154/MM74HC154

54HC154 (J) 74HC154 (J,N)

Truth Table

Inputs						Low Output*
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
L	L	L	H	L	L	4
L	L	L	H	L	H	5
L	L	L	H	H	L	6
L	L	L	H	H	H	7
L	L	H	L	L	L	8
L	L	H	L	L	H	9
L	L	H	L	H	L	10
L	L	H	L	H	H	11
L	L	H	H	L	L	12
L	L	H	H	L	H	13
L	L	H	H	H	L	14
L	L	H	H	H	H	15
L	H	X	X	X	X	—
H	L	X	X	X	X	—
H	H	X	X	X	X	—

*All others high

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, $\overline{G1}$, $\overline{G2}$ or A, B, C, D		21	32	ns

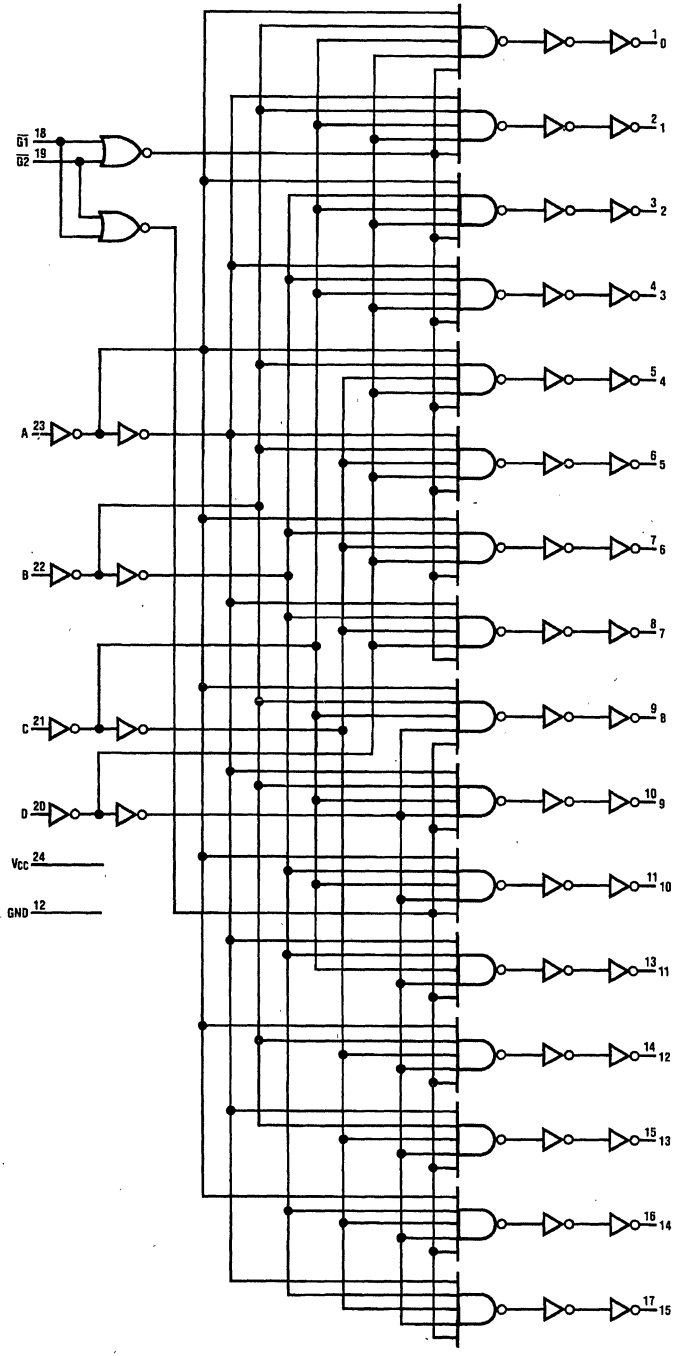
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, $\overline{G1}$ or $\overline{G2}$ or A, B, C, D		2.0V	63	160	190	220	ns
			4.5V	24	36	42	46	ns
			6.0V	20	30	35	39	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5122–2

National Semiconductor

MM54HC157/MM74HC157 Quad 2-Input Multiplexer
MM54HC158/MM74HC158 Quad 2-Input Multiplexer (Inverted Output)

General Description

These high speed QUAD 2-to-1 LINE DATA SELECTOR/MULTIPLEXERS utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These devices each consist of four 2-input digital multiplexers with common select and STROBE inputs. On the MM54HC157/MM74HC157, when the STROBE input is at logical "0" the four outputs assume the values as selected from the inputs. When the STROBE input is at a logical "1" the outputs assume logical "0". The MM54HC158/MM74HC158 operates in the same manner, except that its outputs are inverted. Select decoding is done internally resulting in a single select input only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

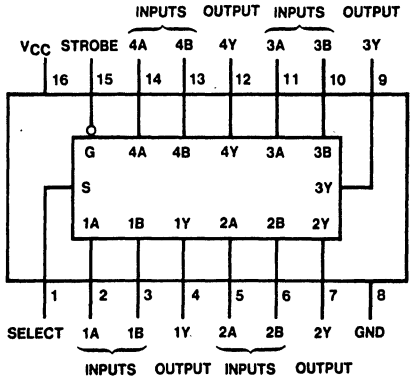
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns data to any output
- Wide power supply range: 2–6V
- Low power supply quiescent current: 80 μA maximum (74HC series)
- Fan-out of 10 LS-TTL loads
- Low input current: 1 μA maximum

Connection Diagrams

Dual-In-Line Package

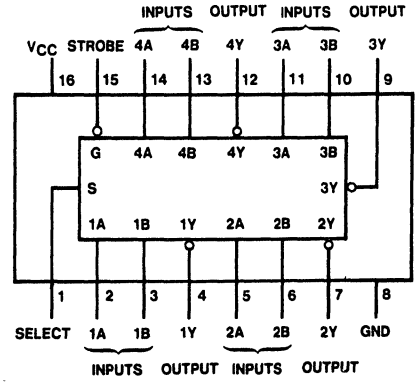


TL/F/5314–1

MM54HC157/MM74HC157

54HC157 (J) **74HC157 (J,N)**

Dual-In-Line Package



TL/F/5314–2

MM54HC158/MM74HC158

54HC158 (J) **74HC158 (J,N)**

Function Table

Inputs				Output Y	
Strobe	Select	A	B	HC157	HC158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		12	18	ns

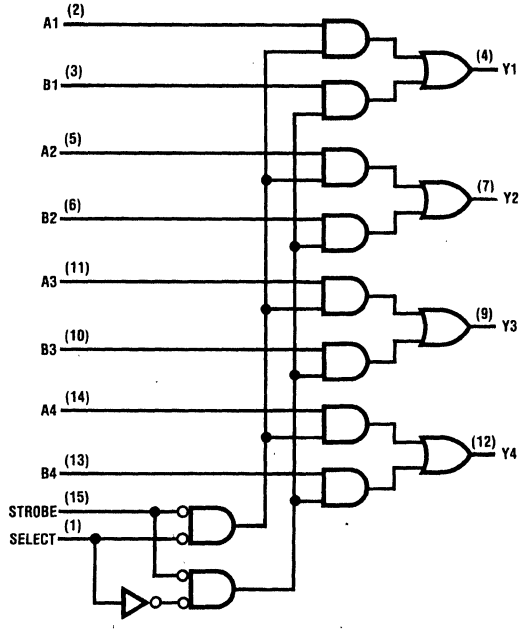
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		2.0V	58	115	145	171	ns
			4.5V	12	23	29	34	ns
			6.0V	10	20	25	29	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)							pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

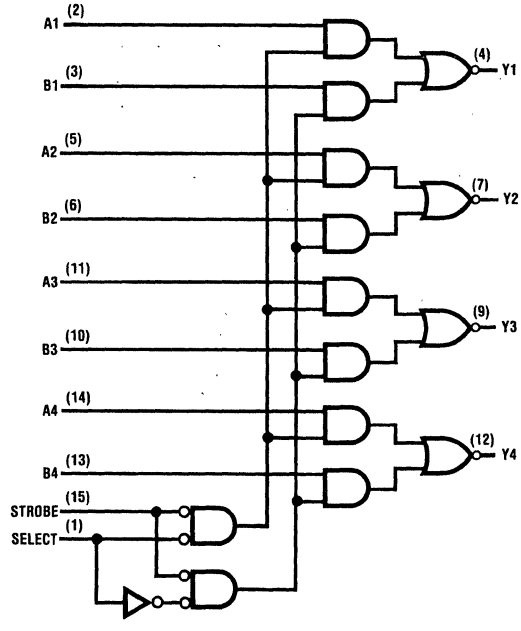
Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagrams



TL/F/5314–3

'HC157



TL/F/5314–4

'HC158

National Semiconductor

MM54HC160/MM74HC160
Synchronous Decade Counter with Asynchronous Clear
MM54HC161/MM74HC161
Synchronous Binary Counter with Asynchronous Clear
MM54HC162/MM74HC162
Synchronous Decade Counter with Synchronous Clear
MM54HC163/MM74HC163
Synchronous Binary Counter with Synchronous Clear

General Description

The MM54HC160/MM74HC160, MM54HC161/MM74HC161, MM54HC162/MM74HC162, and MM54HC163/MM74HC163 synchronous presettable counters utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and internal look-ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. The 'HC160 and the 'HC162 are 4 bit decade counters, and the 'HC161 and the 'HC163 are 4 bit binary counters. All flip-flops are clocked simultaneously on the low to high to transition (positive edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip-flops is synchronous to the rising edge of CLOCK. When LOAD is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken high before the positive edge of CLOCK the count operation will be unaffected.

All of these counters may be cleared by utilizing the CLEAR input. The clear function on the MM54HC162/MM74HC162 and MM54HC163/MM74HC163 counters are synchronous to the clock. That is, the counters are cleared on the positive edge of CLOCK while the clear input is held low.

The MM54HC160/MM74HC160 and MM54HC161/MM74HC161 counters are cleared asynchronously. When the CLEAR is taken low the counter is cleared immediately regardless of the CLOCK.

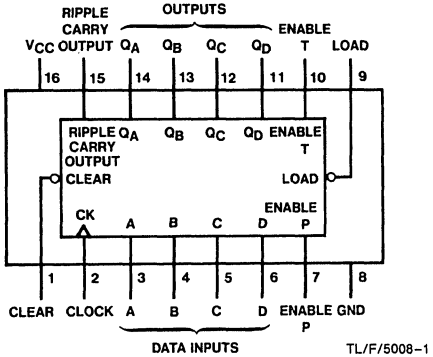
Two active high enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be high to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the Q_A output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 40 MHz
- Typical propagation delay; clock to Q: 18 ns
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Wide power supply range: 2–6V

Connection Diagram



TL/F/5008–1

54HC160 (J) 74HC160 (J,N)
54HC161 (J) 74HC161 (J,N)
54HC162 (J) 74HC162 (J,N)
54HC163 (J) 74HC163 (J,N)

Truth Tables

'HC160/HC161

CLK	CLR	ENP	ENT	Load	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care, ↑ = low to high transition

'HC162/HC163

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		43	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to RC		30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		29	34	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, ENT to RC		18	32	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		27	38	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock			30	ns
t_H	Minimum Hold Time, Data from Clock			5	ns
t_W	Minimum Pulse Width Clock, Clear, or Load			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 40 45	5 27 32	4 21 25	4 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to RC		2.0V 4.5V 6.0V	100 32 28	215 43 37	271 54 46	320 64 54	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V 4.5V 6.0V	95 30 26	205 41 35	258 52 44	305 61 52	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, ENT to RC		2.0V 4.5V 6.0V	90 28 24	195 39 33	246 49 42	291 58 49	ns ns ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		2.0V 4.5V 6.0V	100 32 28	220 44 37	277 55 47	328 66 55	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V		125 25 21	158 32 27	186 37 32	ns ns ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock		2.0V 4.5V 6.0V		150 30 26	190 38 32	225 45 38	ns ns ns
t_H	Minimum Hold Time Data from Clock		2.0V 4.5V 6.0V		50 10 9	63 13 11	75 15 13	ns ns ns
t_W	Minimum Pulse Width Clock, Clear, or Load		2.0V 4.5V 6.0V		80 16 14	100 20 17	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	40 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)			90			pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

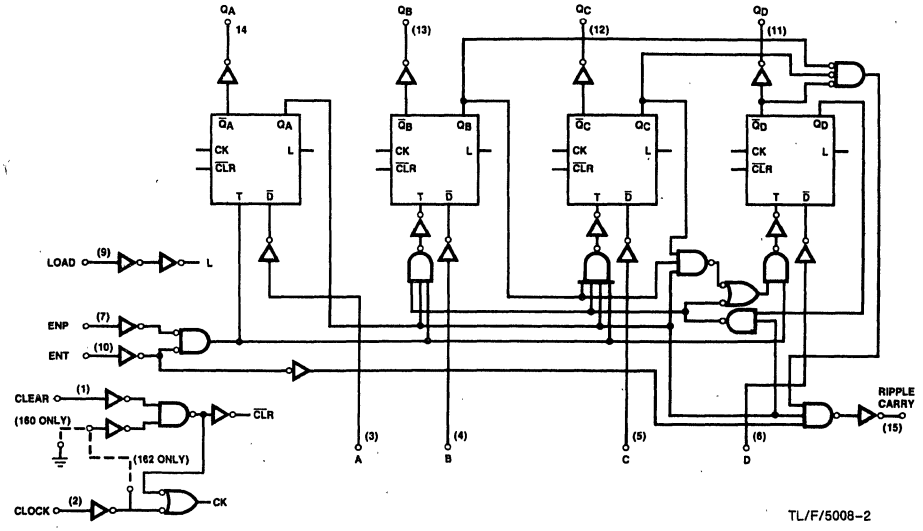
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

4

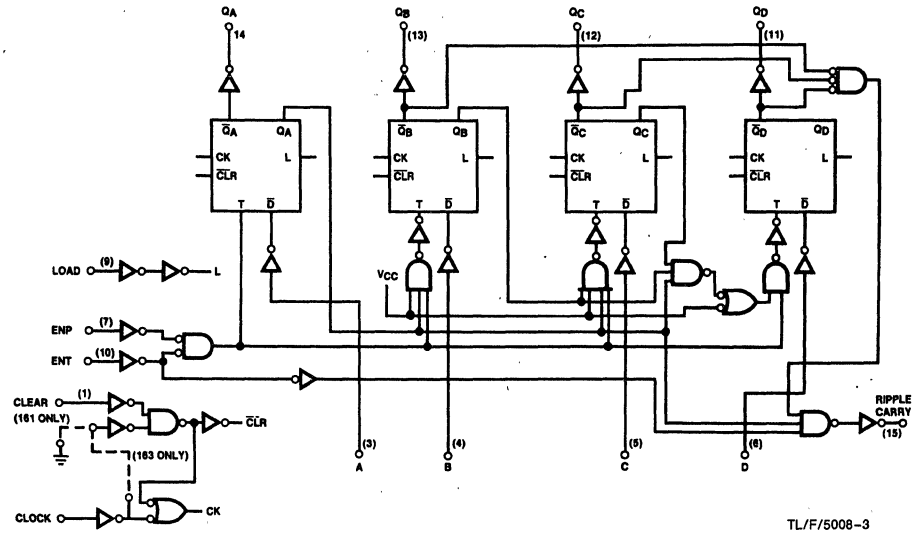
Logic Diagrams

MM54HC160/MM74HC160 or MM54HC162/MM74HC162



TL/F/5008–2

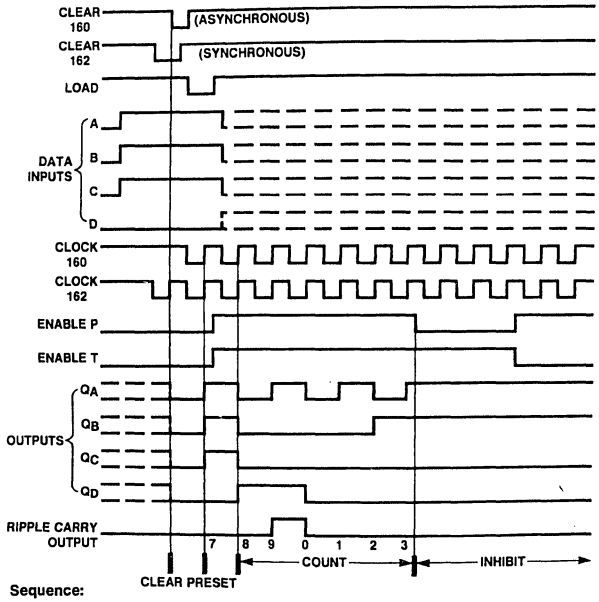
MM54HC161/MM74HC161 or MM54HC163/MM74HC163



TL/F/5008–3

Logic Waveforms

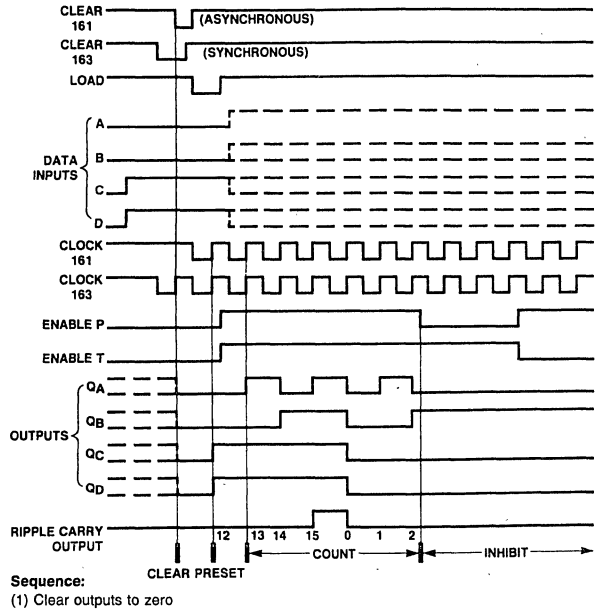
160, 162 Synchronous Decade Counters Typical Clear, Preset, Count and Inhibit Sequences



Sequence:
(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

TL/F/5008-4

161, 163 Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences



Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit

TL/F/5008-5

National Semiconductor

MM54HC164/MM74HC164
8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM54HC164/MM74HC164 utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-BIT SHIFT REGISTER has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-BIT REGISTER during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

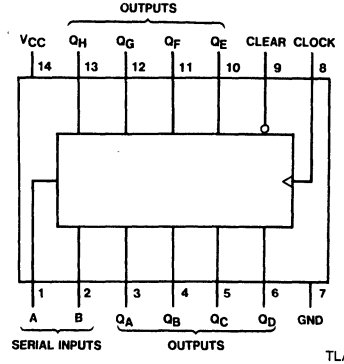
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 19 ns (Clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5315–1

MM54HC164/MM74HC164

54HC164 (J) 74HC164 (J,N)

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

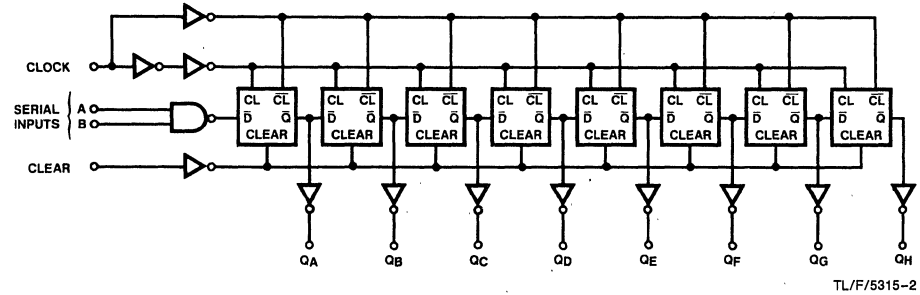
X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

Logic Diagram



TL/F/5315–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		19	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Output		23	35	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	0	ns
t_S	Minimum Set Up Time Data to Clock		12	20	ns
t_H	Minimum Hold Time Clock to Data		1	5	ns
t_W	Minimum Pulse Width Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 31	4 21 24	3 18 20	 MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V 4.5V 6.0V	115 13 20	175 35 30	218 44 38	254 51 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Output		2.0V 4.5V 6.0V	140 28 24	205 41 35	256 51 44	297 59 51	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V	−7 −3 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_S	Minimum Set Up Time Data to Clock		2.0V 4.5V 6.0V	25 14 12	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Clock to Data		2.0V 4.5V 6.0V	−2 0 1	5 5 5	5 5 5	5 5 5	ns ns ns
t_W	Minimum Pulse Width Clear or Clock		2.0V 4.5V 6.0V	22 11 10	80 16 14	100 20 18	120 24 20	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V		75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)	5.0V	150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

PRELIMINARY

National Semiconductor

MM54HC165/MM74HC165
Parallel-in/Serial-out 8-Bit Shift Register

General Description

The MM54HC165/MM74HC165 high speed PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the SHIFT/LOAD input. Also included is a gated CLOCK input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a CLOCK INHIBIT function. Holding either of the CLOCK inputs high inhibits clocking, and holding either CLOCK input low with the SHIFT/LOAD input high enables the other CLOCK input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the SHIFT/LOAD input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

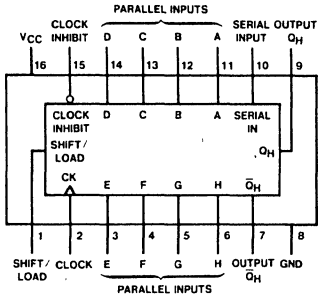
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns (Clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5316–1

MM54HC165/MM74HC165

54HC165 (J) 74HC165 (J,N)

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{AN}, Q_{GN} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND V_{CC}=2–6V	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA V_{CC}=2–6V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		13	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		15	25	ns
t_S	Minimum Set Up Time Serial Input to Clock, Parallel or Data to Shift/Load		10	20	ns
t_S	Minimum Set Up Time Shift/Load to Clock		11	20	ns
t_S	Minimum Set Up Time Clock Inhibit to Clock		10	20	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load			0	ns
t_W	Minimum Pulse Width Clock			16	ns

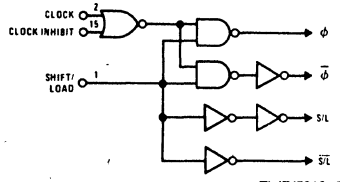
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	5	4	4 MHz
			4.5V	45	27	21	18 MHz
			6.0V	50	32	25	21 MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or Q_H		2.0V	70	150	189	225 ns
			4.5V	21	30	38	45 ns
			6.0V	18	26	33	39 ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/ Parallel Load to Q_H		2.0V	70	150	189	225 ns
			4.5V	21	30	38	45 ns
			6.0V	18	26	33	39 ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		2.0V	70	150	189	225 ns
			4.5V	21	30	38	45 ns
			6.0V	18	26	33	39 ns
t_S	Minimum Set Up Time Serial Input to Clock, or Parallel Data to Shift/Load		2.0V	35	100	125	150 ns
			4.5V	11	20	25	30 ns
			6.0V	9	17	21	25 ns
t_S	Minimum Set Up Time Shift/Load to Clock		2.0V	38	100	125	150 ns
			4.5V	12	20	25	30 ns
			6.0V	9	17	21	25 ns
t_S	Minimum Set Up Time Clock Inhibit to Clock		2.0V	35	100	125	150 ns
			4.5V	11	20	25	30 ns
			6.0V	9	17	21	25 ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load		2.0V		0	0	0 ns
			4.5V		0	0	0 ns
			6.0V		0	0	0 ns
t_W	Minimum Pulse Width, Clock		2.0V	30	80	100	120 ns
			4.5V	9	16	20	24 ns
			6.0V	8	14	18	20 ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110 ns
			4.5V	9	15	19	22 ns
			6.0V	8	13	16	19 ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000 ns
			4.5V		500	500	500 ns
			6.0V		400	400	400 ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100			pF
C_{IN}	Maximum Input Capacitance			5	10	10	10 pF

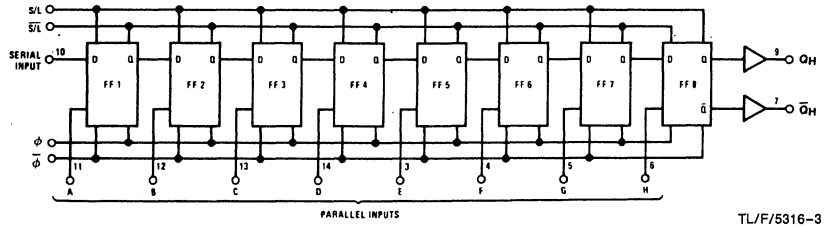
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Block Diagram



TL/F/5316–2



TL/F/5316–3

National Semiconductor

MM54HC173/MM74HC173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54HC173/MM74HC173 is a high speed TRI-STATE QUAD D TYPE FLIP-FLOP that utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It possesses the low power consumption and high noise immunity of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device. The outputs are buffered, allowing this circuit to drive 15 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

The four D TYPE FLIP-FLOPS operate synchronously from a common clock. The TRI-STATE outputs allow the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip flops to remain in the same state. Clearing is enabled by taking the CLEAR input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

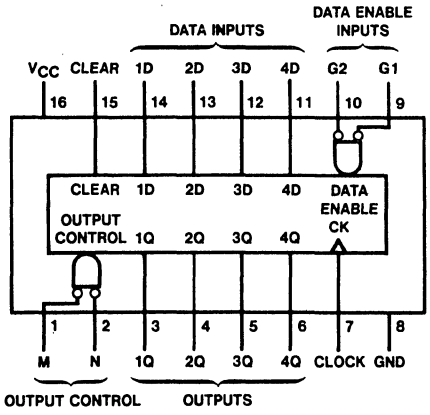
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating supply voltage range: 2–6V
- TRI-STATE outputs
- Low input current: <1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 6 mA minimum

Connection Diagram

Dual-In-Line Package



TL/F/5317–1

MM54HC173/MM74HC173

54HC173 (J) 74HC173 (J,N)

Truth Table

Inputs					Output
Clear	Clock	Data Enable		Data	Q
		G1	G2	D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state: however, sequential operation of the flip-flops is not affected.

H = high level (steady state)

L = low level (steady state)

↑ = low-to-high level transition

X = don't care (any input including transitions)

Q_0 = the level of Q before the indicated steady state input conditions were established

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V		3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V		0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT}=V_{CC} or GND Enable=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay: Clock to Q			31	ns
t_{PHL}	Maximum Propagation Delay: Clear to Q		18	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	16	25	ns
t_S	Minimum Data Set Up Time			20	ns
t_S	Minimum Data Enable Set Up Time			20	ns
t_H	Minimum Data Hold Time			0	ns
t_H	Minimum Data Enable Hold Time			0	ns
t_W	Minimum Clock Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	55	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q	$C_L=50$ pF	2.0V	80	175	220	262	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	23	35	44	53	ns
		$C_L=150$ pF	4.5V	28	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	38	45	ns
		$C_L=150$ pF	6.0V	26	38	48	57	ns
t_{PHL}	Maximum Propagation Delay from Clear to Q	$C_L=50$ pF	2.0V	70	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	20	30	38	45	ns
		$C_L=150$ pF	4.5V	25	40	50	60	ns
		$C_L=50$ pF	6.0V	17	26	32	38	ns
		$C_L=150$ pF	6.0V	22	34	43	51	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ					
		$C_L=50$ pF	2.0V	70	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	20	30	38	45	ns
		$C_L=150$ pF	4.5V	25	40	50	60	ns
		$C_L=50$ pF	6.0V	17	26	32	38	ns
		$C_L=150$ pF	6.0V	22	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	70	150	189	224	ns
			4.5V	20	30	38	45	ns
			6.0V	17	26	32	38	ns
t_S	Minimum Data or Data Enable Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_{REM}	Minimum Removal Time		2.0V		90	112	135	ns
			4.5V		18	22	26	ns
			6.0V		15	19	22	ns
t_H	Minimum Data or Data Enable Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Clear or Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns

AC Electrical Characteristics (Continued)

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	5	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance	(per flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC174/MM74HC174 Hex D Flip-Flops With Clear

General Description

These edge triggered flip-flops utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The CLEAR input when low, sets all outputs to a low state.

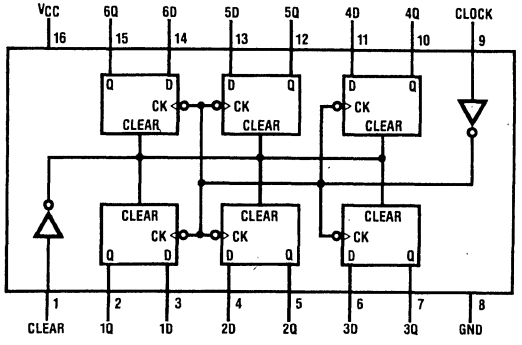
Each output can drive 10 low power Schottky TTL equivalent loads. The MM54HC174/MM74HC174 is functionally as well as pin compatible to the 54LS174/74LS174. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA (74HC series)
- Output drive: 10 LSTTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5318–1

MM54HC174/MM74HC174

54HC174 (J) 74HC174 (J,N)

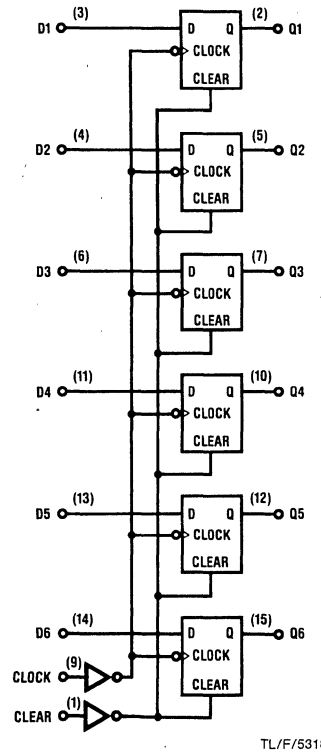
Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level (steady state)
L = Low level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.

Logic Diagram



TL/F/5318–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock or Clear to Output		16	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	5	ns
t_S	Minimum Set Up Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		0	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock or Clear to Output		2.0V	55	165	206	248	ns
			4.5V	18	33	41	49	ns
			6.0V	16	28	35	42	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t_S	Minimum Set Up Time Data to Clock		2.0V	42	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	10	17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	35	80	106	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		136				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

4

National Semiconductor

MM54HC175/MM74HC175
Quad D-Type Flip-Flop With Clear

General Description

This high speed D-TYPE FLIP-FLOP with complementary outputs utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Information at the D inputs of the MM54HC175/MM74HC175 is transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse. Both true and compliment outputs from each flip flop are externally available. All four flip flops are controlled by a common clock and a common CLEAR. Clearing is accomplished by a negative pulse at the CLEAR input. All four Q outputs are cleared to a logical "0" and all four $\overline{Q}$ outputs to a logical "1".

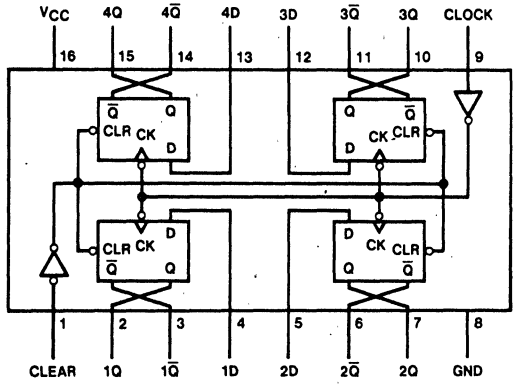
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 4 mA minimum (74HC)

Connection Diagram

Dual-In-Line Package



TL/F/5319–1

MM54HC175/MM74HC175

54HC175 (J) 74HC175 (J,N)

Truth Table

(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		60	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		13	21	ns
t_{REC}	Minimum Removal Time, Clear to Clock			20	ns
t_S	Minimum Set Up Time, Data to Clock			20	ns
t_H	Minimum Hold Time, Data from Clock			0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC Electrical Characteristics

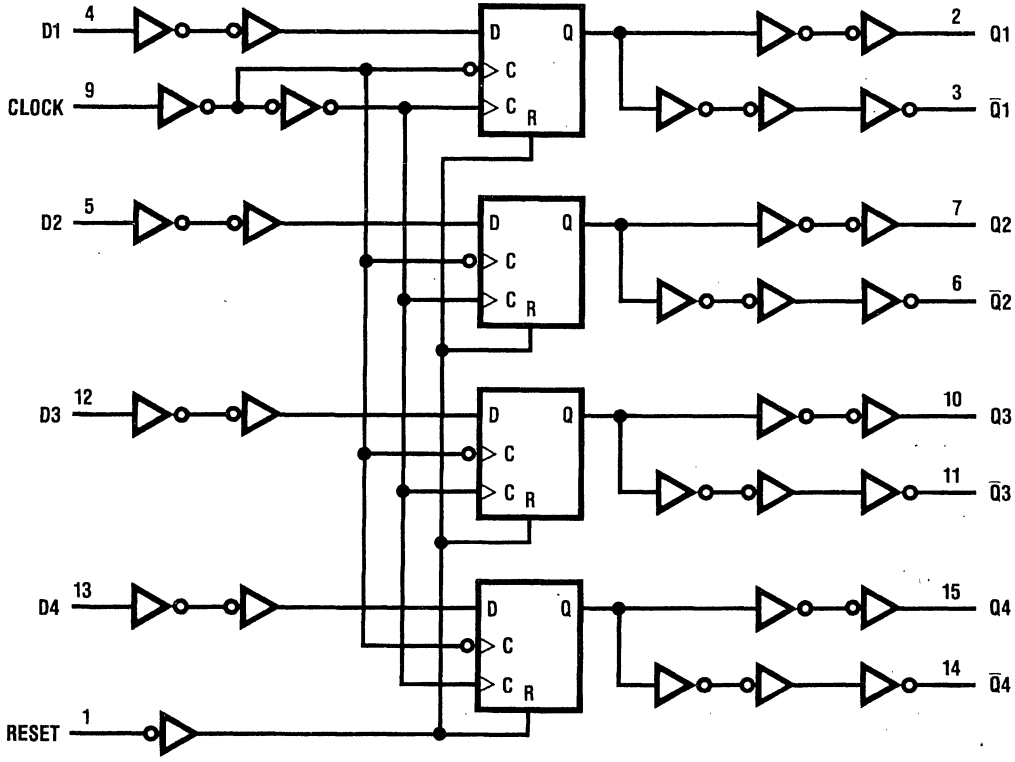
$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	12	6	5	4	MHz
			4.5V	60	30	24	20	MHz
			6.0V	70	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	80	150	190	225	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		2.0V	64	125	158	186	ns
			4.5V	14	25	32	37	ns
			6.0V	12	21	27	32	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Set Up Time Data to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Data from Clock		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	9	15	19	22	ns
			6.0V	8	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)			150			pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5319–2

National Semiconductor

PRELIMINARY

MM54HC181/MM74HC181
Arithmetic Logic Units/Function Generators

General Description

These arithmetic logic units (ALU)/function generators utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The MM54HC181/MM74HC181 are arithmetic logic unit (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the MM54HC182 or MM74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading HC182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the MM54HC182/MM74HC182.

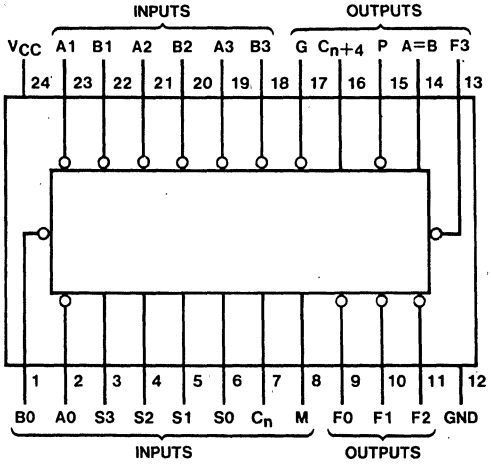
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

Features

- Full look-ahead for high-speed operations on long words
- Arithmetic operating Modes:
  - Addition
  - Substraction
  - Shift operand A one position magnitude comparison
  - Plus Twelve other arithmetic operations
- Logic funtion modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5320–1

TOP VIEW

MM54HC181/MM74HC181

54HC181 (J) 74HC181 (J,N)

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Outputs
P	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

General Description (Continued)

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to produce A—B.

The 181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with C_n=H when performing this comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+_4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control inpu (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The MM54HC181/MM74HC181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table 1; those obtained with the signal designations of *Figure 2* are given in Table 2.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table 1)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-Low Data (Table 1)	$\overline{A}$0	$\overline{B}$0	$\overline{A}$1	$\overline{B}$1	$\overline{A}$2	$\overline{B}$2	$\overline{A}$3	$\overline{B}$3	$\overline{F}$0	$\overline{F}$1	$\overline{F}$2	$\overline{F}$3	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Input C_n	Output C_n+4	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

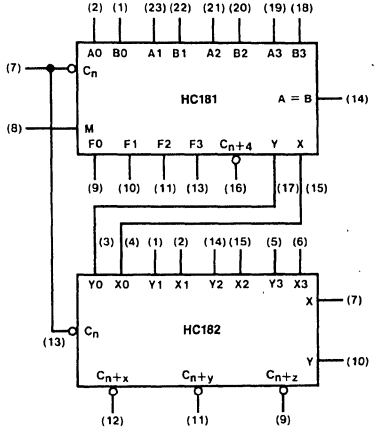


Figure 1

Table 1

Selection				Active High Data		
				M=H	M=L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n=H (no carry)	C_n=L (with carry)
L	L	L	L	F=$\overline{A}$	F=A	F=A Plus 1
L	L	L	H	F=$\overline{A+B}$	F=A + B	F=(A + B) Plus 1
L	L	H	L	F=$\overline{A}$B	F=A + $\overline{B}$	F=(A + $\overline{B}$) Plus 1
L	L	H	H	F=0	F=Minus 1 (2's Compl)	F=Zero
L	H	L	L	F=$\overline{AB}$	F=A Plus A$\overline{B}$	F=A Plus A$\overline{B}$ Plus 1
L	H	L	H	F=$\overline{B}$	F=(A + B) Plus A$\overline{B}$	F=(A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F=A ⊕ B	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ Minus 1	F=A$\overline{B}$
H	L	L	L	F=$\overline{A}$ + B	F=A Plus AB	F=A Plus AB Plus 1
H	L	L	H	F=$\overline{A \oplus B}$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=(A + $\overline{B}$) Plus AB	F=(A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F=AB	F=AB Minus 1	F=AB
H	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	F=A + $\overline{B}$	F=(A + B) Plus A	F=(A + B) Plus A Plus 1
H	H	H	L	F=A + B	F=(A + $\overline{B}$) Plus A	F=(A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F=A	F=A Minus 1	F=A

*Each bit is shifted to the next more significant position.

General Description (Continued)

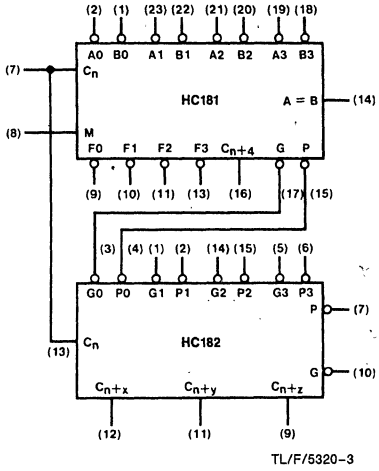


Figure 2

Table 2

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = (A$\overline{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A + B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$ Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A + B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage (any output except A=B)	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
I_{LKG}	Maximum Leakage Open Drain Output Current (A=B Output)	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}	6.0V		0.5	5.0	10	μA
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_n to C_n+4		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to C_N+4	M=0V, S0=S3=V_{CC} S1=S0=0V ($\overline{\text{Sum}}$ mode)	30	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to C_N+4	M=0V,S0=S3=0V S1=S2=V_{CC} ($\overline{\text{Diff.}}$ mode)	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_n to any F	M=0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff.}}$ mode)	13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to G	M=0V, S0= S3=V_{CC} S1=S2=0V ($\overline{\text{Sum}}$ mode)	14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to G	M=0V, S0= S3=0V S1=S2=V_{CC} ($\overline{\text{Diff}}$ mode)	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to P	M=0V, S0= S3=V_{CC} S1=S2=0V ($\overline{\text{Sum}}$ mode)	17	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to P	M=0V, S0= S3=0V S1=S2=V_{CC} ($\overline{\text{Diff}}$ mode)	17	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M=0V, S0= S3=V_{CC} S1=S2=0V ($\overline{\text{Sum}}$ mode)	28	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M=0V, S0= S3=0V S1=S2=V_{CC} ($\overline{\text{Diff}}$ mode)	32	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M=V_{CC} (logic mode)	32	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to A=B	M=0V, S0= S3=0V S1=S2=V_{CC} ($\overline{\text{Diff}}$ mode)	36	50	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_n to C_n+4		2.0V	55	120	160	200	ns
			4.5V	17	24	30	36	ns
			6.0V	14	20	25	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to C_n+4	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	110	250	325	375	ns
			4.5V	35	50	63	75	ns
			6.0V	30	43	53	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to C_n+4	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V	120	280	350	420	ns
			4.5V	40	56	70	84	ns
			6.0V	35	48	60	72	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_n to any F	M = 0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff}}$ mode)	2.0V	55	120	160	200	ns
			4.5V	17	24	30	36	ns
			6.0V	14	20	25	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to G	M = 0V, S0 = S3 = V_{CC}, S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	55	120	160	200	ns
			4.5V	17	24	30	36	ns
			6.0V	14	20	25	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to G	M = 0V, S0 = S3 = 0V S1 = S2 ($\overline{\text{Diff}}$ mode)	2.0V	70	150	189	224	ns
			4.5V	20	30	38	45	ns
			6.0V	17	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to P	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	70	150	189	224	ns
			4.5V	20	30	38	45	ns
			6.0V	17	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to P	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V	70	150	189	224	ns
			4.5V	20	30	38	45	ns
			6.0V	17	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	115	240	300	360	ns
			4.5V	35	48	60	72	ns
			6.0V	30	41	51	61	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V	120	275	344	344	ns
			4.5V	40	55	69	83	ns
			6.0V	34	47	59	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to F_I	M = V_{CC} (logic mode)	2.0V	120	275	344	344	ns
			4.5V	40	55	60	83	ns
			6.0V	34	47	59	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From any A or B to A = B	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V	120	280	350	420	ns
			4.5V	40	56	70	84	ns
			6.0V	35	48	60	72	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = V_{CC}, S0 = S3 = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase

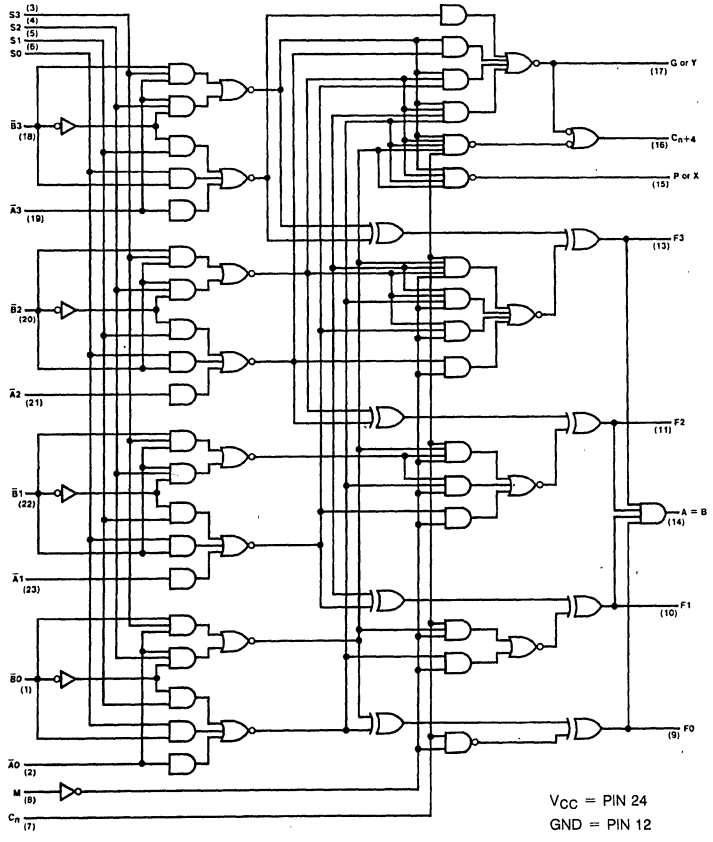
$\overline{SUM}$ Mode Test Table
Function Inputs: S0 = S3 = V_{CC} S1 = S2 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	B_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

$\overline{Diff}$ Mode Test Table
Function Inputs: S1 = S2 = V_{CC}, S0 = S3 = M = 0 V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A and B	None	C_n+4 or any F	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A, B, C_n	C_n+4	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A, B, C_n	C_n+4	In-Phase

Logic Diagram



TL/F/5320–4

National Semiconductor

PRELIMINARY

MM54HC182/MM74HC182 Look-Ahead Carry Generator

General Description

The MM54HC182/MM74HC182 is a high speed LOOK-AHEAD CARRY GENERATOR utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

These circuits are capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the HC181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

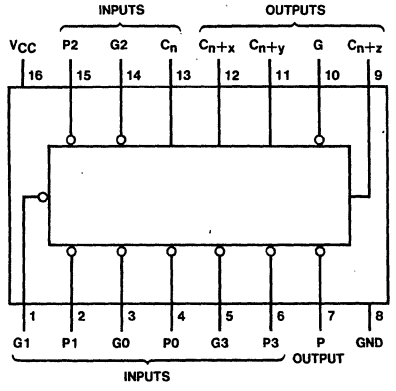
Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator.

Features

- TTL pinout compatible
- Typical propagation delay: 18 ns (Clock to Q)
- Wide Operating Supply Voltage Range: 2–6V
- Low Input Current: < 1 μA
- Low Quiescent Supply Current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL Loads

Connection Diagram

Dual-In-Line Package

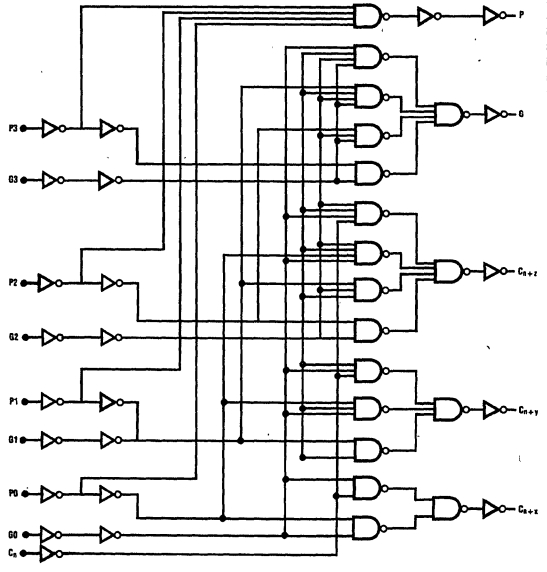


TL/F/5321–1

MM54HC182/MM74HC182

54HC182 (J) 74HC182 (J,N)

Logic Diagram



TL/F/5321–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T=25°C	74HC T=−40 to 85°C	54HC T=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=15 pF, $t_r=t_f$=6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Pn to P		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Cn to any output		18	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Pn or Gn to any output		23	35	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T=25°C	74HC T=−40 to 85°C		54HC T=−55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Pn to P		2.0V	45	112	140	162	ns
			4.5V	18	28	35	40	ns
			6.0V	15	22	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cn to any output		2.0V	50	125	156	182	ns
			4.5V	20	30	37	44	ns
			6.0V	16	24	30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Pn or Gn to any output		2.0V	62	155	194	225	ns
			4.5V	25	37	46	54	ns
			6.0V	22	33	42	48	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance			90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Logic Equations

$C_{n+x}=G0+P0\ C_n$

$C_{n+y}=G1+P1\ G0+P1\ P0\ C_n$

$C_{n+z}=G2+P2\ G1+P2\ P1\ P0\ C_n$

$\overline{G}=\overline{G3+P3\ G2+P3\ P2\ G1+P3\ P2\ P1\ G0}$

$\overline{P}=\overline{P3\ P2\ P1\ P0}$

or

$\overline{C}_{n+x}=\overline{Y0\ (X0+C_n)}$

$\overline{C}_{n+y}=\overline{Y1\ [X1+Y0\ (X0+C_n)]}$

$\overline{C}_{n+z}=\overline{Y2\ \{X2+Y1\ [X1+Y0\ (X0+C_n)]\}}$

$Y=Y3\ (X3+Y2)\ (X3+X2+Y1)\ (X3+X2+X1+Y0)$

$X=X3+X2+X1+X0$

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P3}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

FUNCTION TABLE FOR C_{n+y} OUTPUT

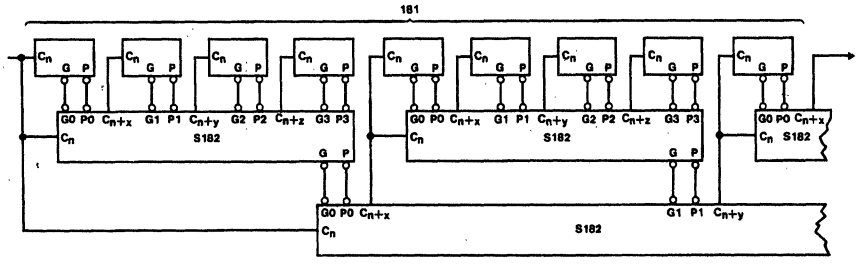
INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

H=high level L=low level X=irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS



A and B inputs, and F outputs of 181 are not shown.

PRELIMINARY

National Semiconductor

MM54HC190/MM74HC190 Synchronous Decade Up/Down Counters with Mode Control MM54HC191/MM74HC191 Synchronous Binary Up/Down Counters with Mode Control

General Description

These high speed synchronous counters utilize micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL.

These circuits are synchronous, reversible, up/down counters. The MM54HC191/MM74HC191 are 4-bit binary counters and the MM54HC190/MM74HC190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

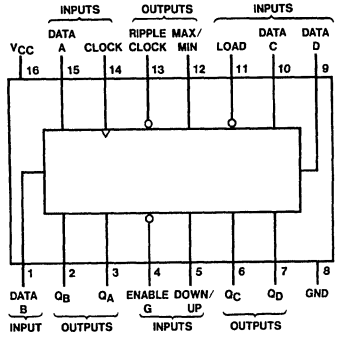
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Typical propagation delay
  Clock to output: 24 ns
- Typical operating frequency: 50 MHz
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5322–1

MM54HC190/MM74HC190, MM54HC191/MM74HC191
54HC190 (J) 74HC190 (J,N)
54HC191 (J) 74HC191 (J,N)

Asynchronous inputs Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency				40	25	MHz
t_{PLH}, t_{PHL}	Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		30	50	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		27	40	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Ripple Clock		16	24	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		24	36	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Max/Min		30	50	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Ripple Clock		29	45	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Max/Min		22	33	ns
t_{PHL}, t_{PLH}	Propagation Delay Time	Enable	Ripple Clock		22	33	ns
$t_{W(CLOCK)}$	Width of Clock, Clear or Load Input Pulse				10	20	ns
t_{SETUP}	Data Setup Time					20	ns
t_{HOLD}	Data Hold Time					0	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
						Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency				2.0V	10	4	3	2	MHz
					4.5V	38	20	15	13	MHz
					6.0V	40	23	18	15	MHz
t_{PLH}, t_{PHL}	Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		2.0V	106	290	360	435	ns
					4.5V	32	58	72	87	ns
					6.0V	29	49	61	73	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		2.0V	93	230	290	345	ns
					4.5V	28	46	57	69	ns
					6.0V	25	39	49	58	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Ripple Clock		2.0V	62	150	190	225	ns
					4.5V	18	30	37	45	ns
					6.0V	16	26	32	37	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		2.0V	90	220	275	330	ns
					4.5V	27	44	55	66	ns
					6.0V	24	37	46	56	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Clock	Max/Min		2.0V	108	290	360	435	ns
					4.5V	33	58	72	87	ns
					6.0V	30	49	61	73	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Ripple Clock		2.0V	98	265	330	398	ns
					4.5V	30	53	66	80	ns
					6.0V	28	45	56	68	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Down/Up	Max/Min		2.0V	85	200	250	300	ns
					4.5V	25	40	50	60	ns
					6.0V	23	54	42	51	ns
t_{PHL}, t_{PLH}	Propagation Delay Time	Enable	Ripple Clock		2.0V	85	200	250	300	ns
					4.5V	25	40	50	60	ns
					6.0V	23	34	42	51	ns
t_W	Width of Clock, Load or Clear Input Pulse				2.0V		100	125	150	ns
					4.5V		20	25	30	ns
					6.0V		17	21	25	ns
t_{SETUP}	Data Setup Time				2.0V	20	100	125	150	ns
					4.5V	10	20	25	30	ns
					6.0V	8	17	21	25	ns

AC Electrical Characteristics V_{CC}=2.0V to 6.0V, C_L=50 pF $t_r=t_f$=6 ns (unless otherwise specified)

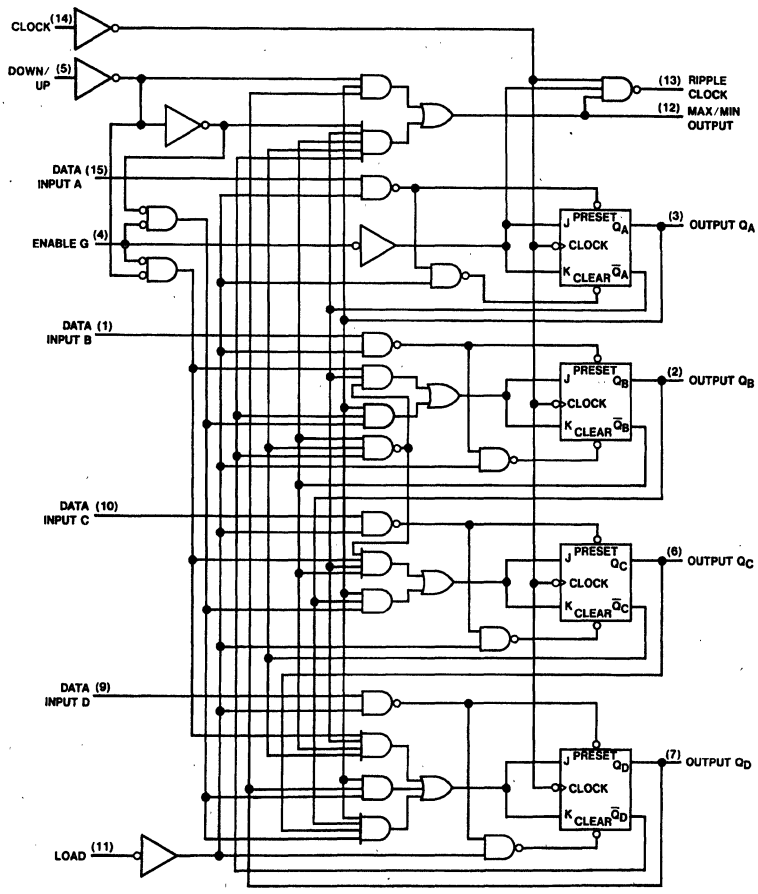
Symbol	Parameter	From (Input)	To (Output)	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
						Typ	Guaranteed Limits		
t_H	Data Hold Time				2.0V		0	0	0	ns
					4.5V		0	0	0	ns
					6.0V		0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time				2.0V		75	95	110	s
					4.5V		15	19	22	ns
					6.0V		13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time				2.0V		1000	1000	1000	ns
					4.5V		500	500	500	ns
					6.0V		400	400	400	ns
C_{IN}	Input Capacitance					5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)					100				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Logic Diagrams

'HC190 Decade Counters

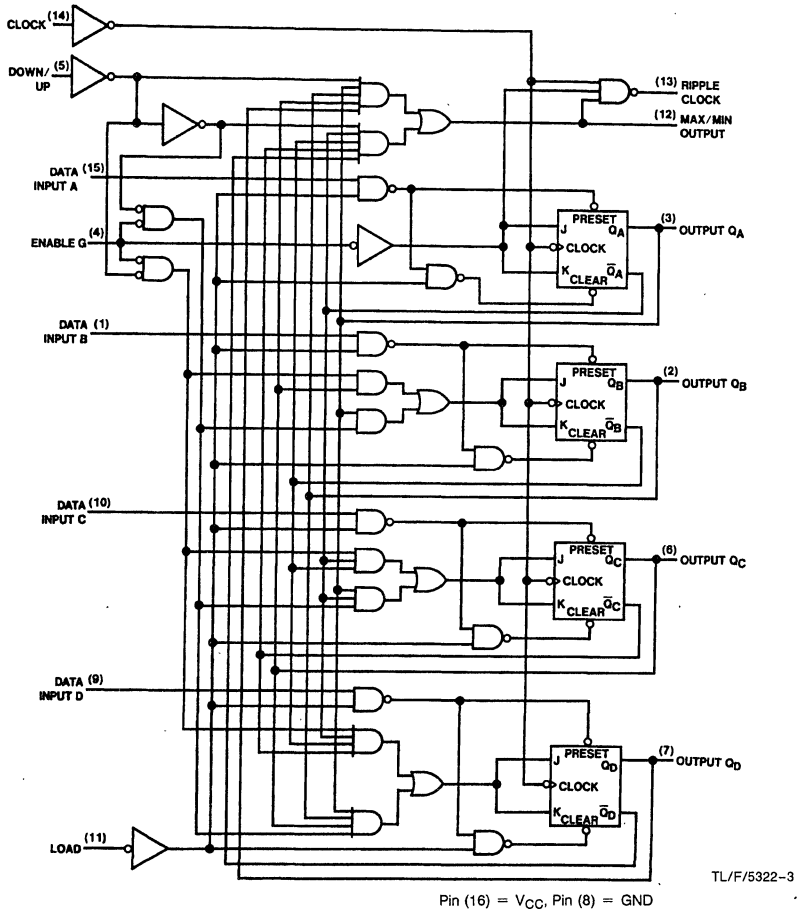


Pin (16) = V_{CC}, Pin (8) = GND

TL/F/5322–2

Logic Diagrams (Continued)

'HC191 Binary Counters

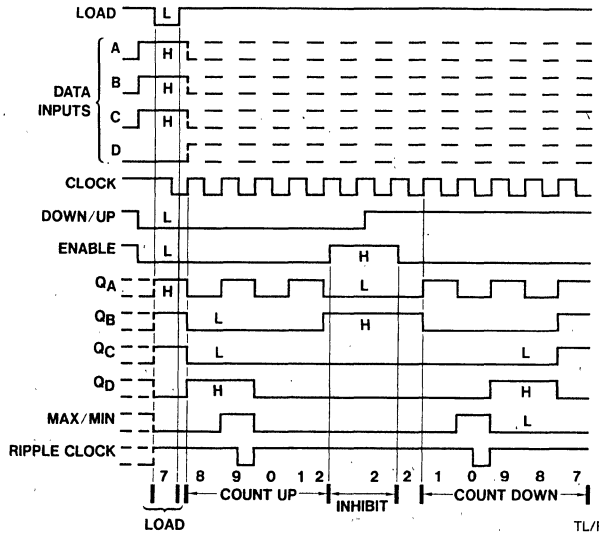


TL/F/5322–3

Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

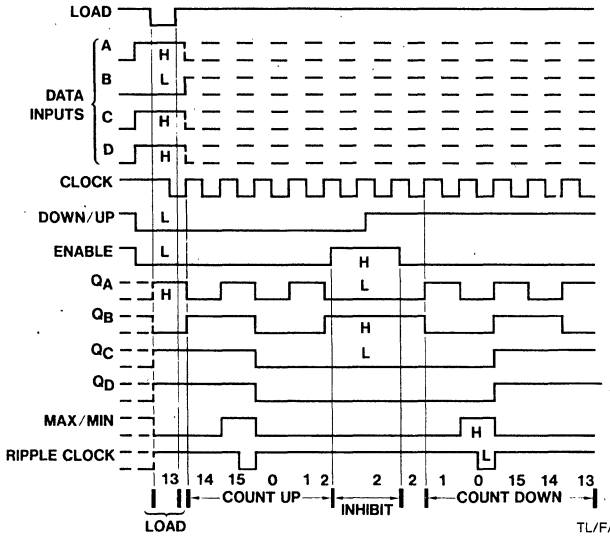
'HC190 Decade Counters
Typical Load, Count, and Inhibit Sequences



TL/F/5322–4

Sequence:
(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one and two
(3) Inhibit
(4) Count down to one, zero, nine, eight, and seven

'HC191 Decode Counters
Typical Load, Count, and Inhibit Sequence



TL/F/5322–5

Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

National Semiconductor

MM54HC192/MM74HC192 Synchronous Decade Up/Down Counters MM54HC193/MM74HC193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters utilize micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HC192/MM74HC192 is a decade counter, and the MM54HC193/MM74HC193 is a binary counter. Both counters have two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

These counters may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

In addition both counters can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counters can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

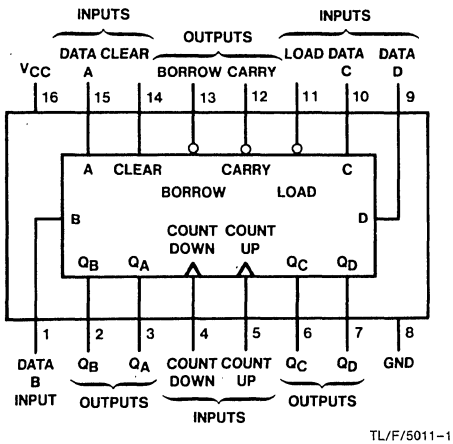
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, Clock to output: 20 ns
- Typical operating frequency: 27 MHz
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum.

Connection Diagram

Dual-In-Line Package



TL/F/5011–1

MM54HC192/MM74HC192
MM54HC193/MM74HC193

54HC192 (J) 74HC192 (J,N)
54HC193 (J) 74HC193 (J,N)

Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = High level
L = Low level
↑ = Transition from low-to-high
X = Don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$T_A = 25°C$, V_{CC} = 5.0V, $t_r = t_f = 6$ ns $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	Conditions		Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency	Count Up		27	20	MHz
		Count Down		31	24	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry		17	26	ns
t_{PHL}	Maximum Propagation Delay High to Low			18	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Down to Borrow		16	24	ns
t_{PHL}	Maximum Propagation Delay High to Low			15	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q		28	40	ns
t_{PHL}	Maximum Propagation Delay High to Low			36	52	ns
t_{PLH}	Maximum Propagation Delay Low to High	Load to Q		30	42	ns
t_{PHL}	Maximum Propagation Delay High to Low			40	55	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q		35	47	ns
t_W	Minimum Pulse Width	Clear	'HC192	40	52	ns
			'HC193	20	26	ns
		Load		10	20	ns
		Count Up/Down		15	22	ns
t_{SD}	Minimum Setup time	Data to Load		10	20	ns
t_{HD}	Minimum Hold Time			−3	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock			10	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency	Count Up	2.0V	5	3	2.5	2	MHz
			4.5V	25	18	14	12	MHz
			6.0V	29	20	16	13	MHz
		Count Down	2.0V	5	4	3	2	MHz
			4.5V	27	20	16	11	MHz
			6.0V	31	23	18	12	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry	2.0V	30	140	175	210	ns
			4.5V	13	28	35	42	ns
			6.0V	11	24	30	36	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	39	130	163	195	ns
			4.5V	16	26	33	39	ns
			6.0V	14	22	28	33	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (Continued)

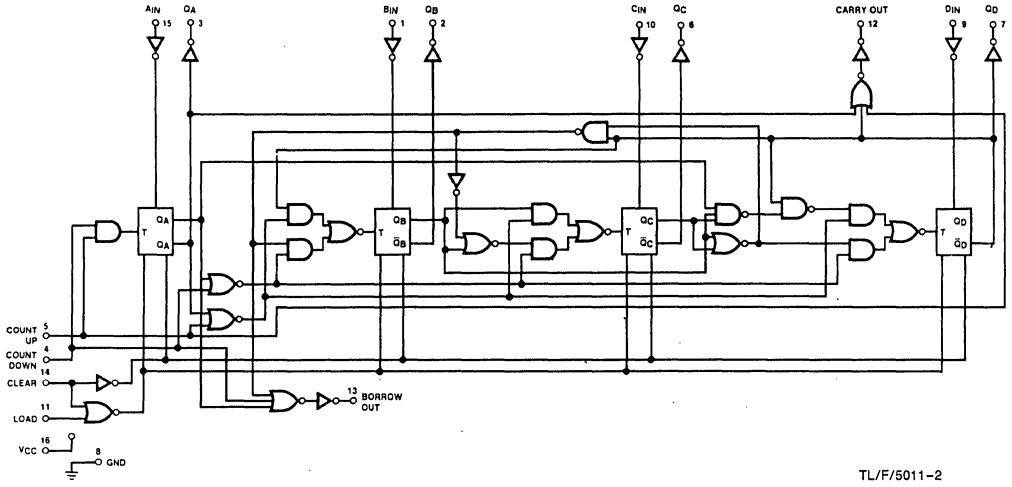
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay	Count Down to Borrow	2.0V	39	130	163	195	ns
			4.5V	16	26	33	39	ns
			6.0V	14	22	28	33	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q	2.0V	77	215	269	323	ns
			4.5V	35	43	54	65	ns
			6.0V	30	37	46	55	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	95	275	344	413	ns
			4.5V	45	55	69	83	ns
			6.0V	38	47	59	71	ns
t_{PLH}	Maximum Propagation Delay Low to High	Load to Q	2.0V	85	230	280	345	ns
			4.5V	37	46	58	69	ns
			6.0V	30	39	49	59	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	102	290	363	435	ns
			4.5V	47	58	73	87	ns
			6.0V	39	49	61	74	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q	2.0V	85	265	331	398	ns
			4.5V	42	53	66	80	ns
			6.0V	38	45	56	68	ns
t_W	Minimum Pulse Width	Clear 'HC192	2.0V	119	260	325	390	ns
			4.5V	42	52	65	78	ns
			6.0V	38	45	56	68	ns
		Load	2.0V	31	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	26	ns
		Count Up/Down	2.0V	43	110	138	165	ns
			4.5V	17	22	28	33	ns
			6.0V	15	19	24	29	ns
		Clear 'HC193	2.0V	70	130	163	195	ns
			4.5V	21	26	33	39	ns
			6.0V	19	22	28	33	ns
t_{SD}	Minimum Setup Time	Data To Load	2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	22	25	ns
t_{HD}	Minimum Hold Time		2.0V	−30	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock	2.0V	−20	10	10	10	ns
			4.5V	−3	10	10	10	ns
			6.0V	−2	10	10	10	ns
t_r, t_f	Maximum Input Rise & Fall Time		2.0V		500	500	500	ns
			4.5V		300	300	300	ns
			6.0V		200	200	200	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

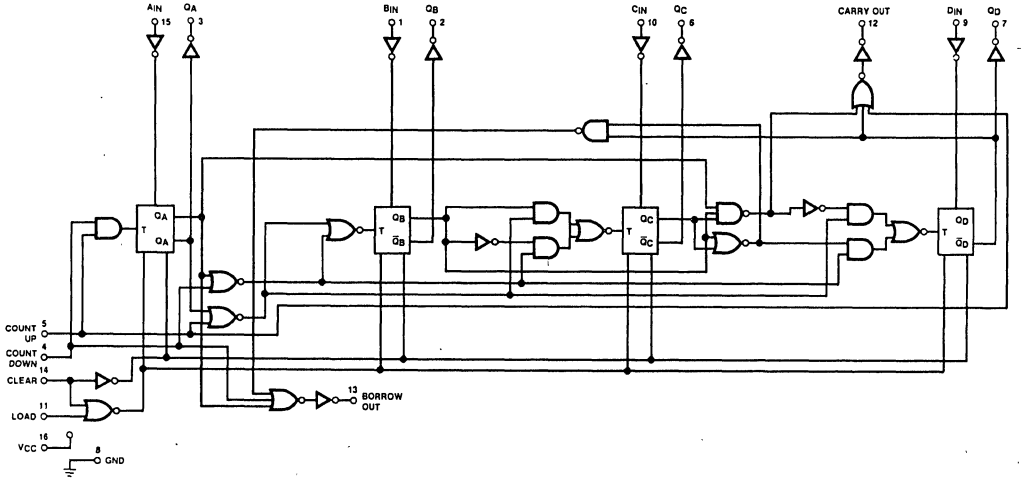
Logic Diagrams

MM54HC192 Synchronous 4-Bit Up/Down Decade Counter



TL/F/5011–2

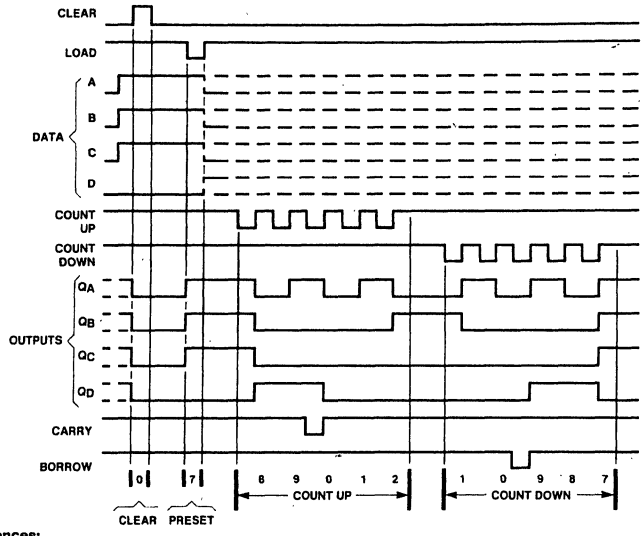
MM54HC193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/5011–3

Logic Waveforms

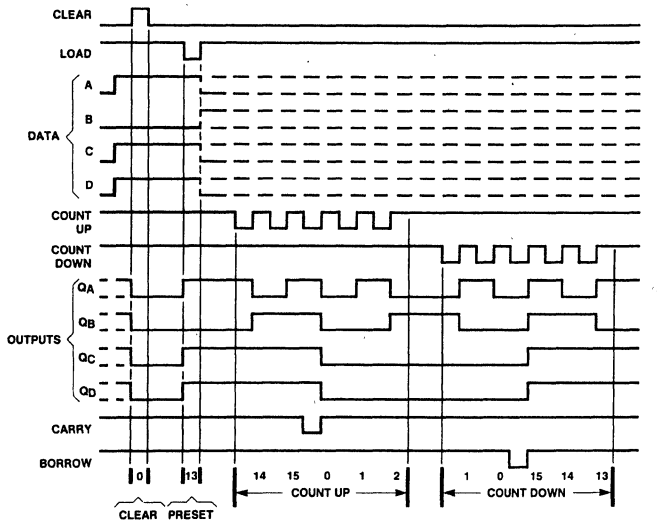
'HC192 Synchronous Decade Counters
Typical Clear, Preset, and Count Sequences



TL/F/5011–4

Sequences:
(1) Clear outputs to zero
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

'HC193 Synchronous Binary Counters
Typical Clear, Load, and Count Sequences



TL/F/5011–5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
Note A: Clear overrides load data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor

MM54HC194/MM74HC194
4-Bit Bidirectional Universal Shift Register

General Description

This 4-bit high speed BIDIRECTIONAL SHIFT REGISTER utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads. This device operates at speeds similar to the equivalent low power Schottky part.

This BIDIRECTIONAL SHIFT REGISTER is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation: PARALLEL (broadside) LOAD; SHIFT RIGHT (in the direction Q_A toward Q_D); SHIFT LEFT; INHIBIT CLOCK (do nothing).

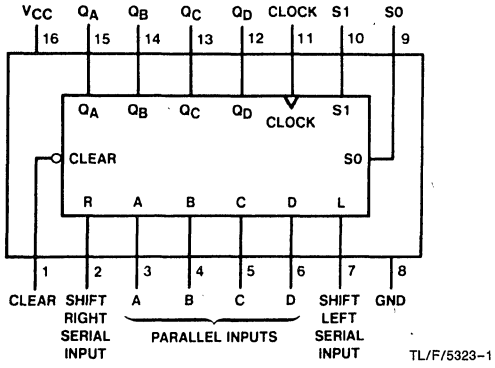
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into their respective flip flops and appear at the outputs after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the SHIFT RIGHT data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the SHIFT LEFT serial input. Clocking of the flip flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the CLOCK input is high.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: ns (Clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 160 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram



TL/F/5323–1

MM54HC194/MM74HC194

54HC194 (J) 74HC194 (J,N)

Function Table

Inputs										Outputs			
Clear	Mode S1	Mode S2	Clock	Serial Left	Serial Right	Parallel A	Parallel B	Parallel C	Parallel D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		17	24	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		19	25	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock			20	ns
t_S	Minimum Set Up Time (A, B, C, D to Clock)			20	ns
t_S	Minimum Set Up Time Mode Controls to Clock			25	ns
t_W	Minimum Pulse Width Clock or Reset		9	16	ns
t_H	Minimum Hold Time Any Input		−3	0	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

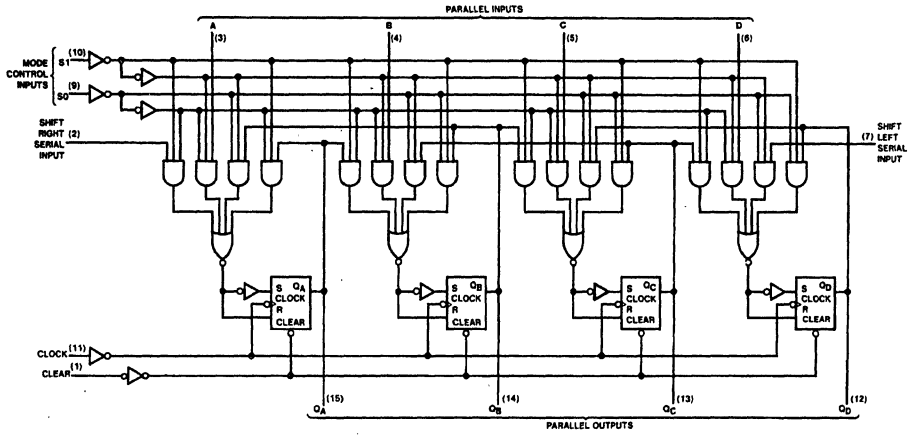
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 45 50	6 30 35	5 24 28	4 20 24	 MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V 4.5V 6.0V	70 15 12	145 29 25	183 37 31	216 45 37	ns ns ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		2.0V 4.5V 6.0V	80 15 12	150 30 26	189 37 31	216 45 37	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_{REM}	Minimum Removal Time Reset Inactive to Clock		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time (A, B, C, or D to Clock)		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Time Mode Controls to Clock		2.0V 4.5V 6.0V		125 25 21	156 31 26	188 38 32	ns ns ns
t_H	Minimum Hold Time Any Input		2.0V 4.5V 6.0V	−10 −3 −3	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Clock or Reset		2.0V 4.5V 6.0V	30 89 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram

MM54HC194/MM74HC194



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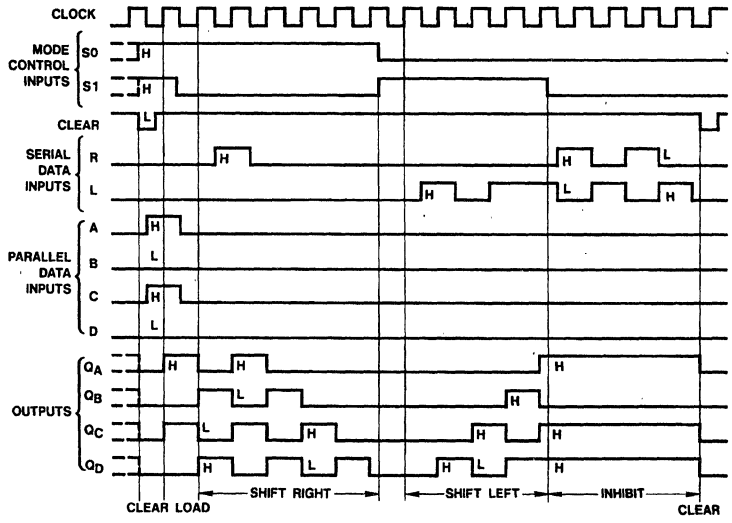
Timing Diagram



TL/F/5323–3

National Semiconductor

MM54HC195/MM74HC195 4-Bit Parallel Shift Register

General Description

The MM54HC195/MM74HC195 is a high speed 4-bit SHIFT REGISTER utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads at LS type speeds.

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, SHIFT/LOAD control input, and a direct overriding CLEAR. This shift register can operate in two modes: Parallel Load; Shift from Q_A towards Q_D.

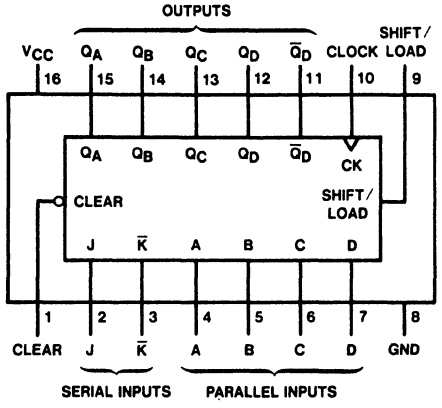
Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/LOAD control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/LOAD control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or TOGGLE flip flop as shown in the truth table.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: 16 ns (Clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagram

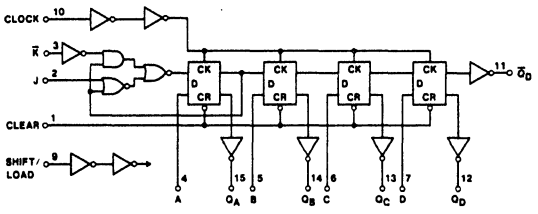


TL/F/5324–1

MM54HC195/MM74HC195

54HC195 (J) 74HC195 (J,N)

Logic Diagram



TL/F/5324–2

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent transition of the clock.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		14	24	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		16	25	ns
t_{REM}	Minimum Removal Time, Shift/Load to Clock			0	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock			20	ns
t_S	Minimum Set Up Time, (A, B, C, D, J, $\overline{K}$ to Clock)			20	ns
t_S	Minimum Set Up Time, Shift/Load to Clock			25	ns
t_W	Minimum Pulse Width Clock or Reset			16	ns
t_H	Minimum Hold Time, any Input except Shift/Load			0	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

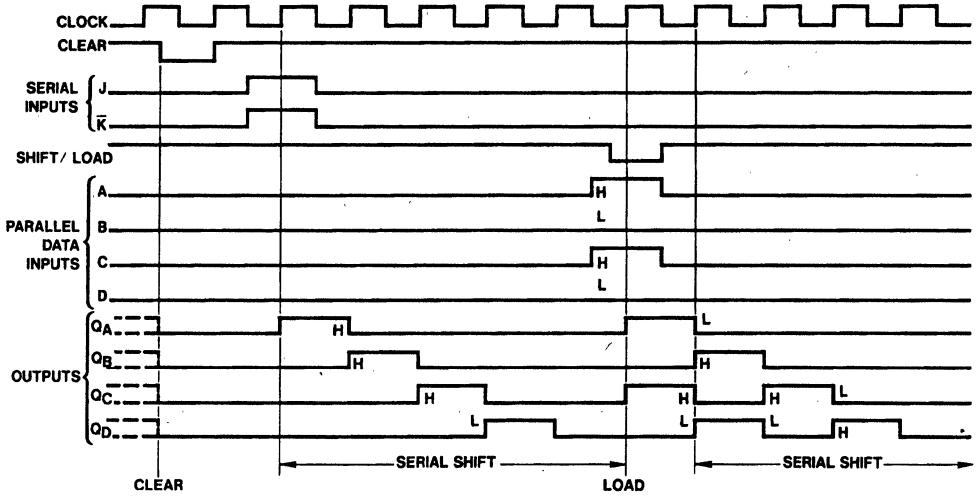
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 45 50	6 30 35	5 24 28	4 20 24	MHz MHz MHz
t_{PHL}	Maximum Propagation Delay, Reset to Q		2.0V 4.5V 6.0V	70 15 12	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V 4.5V 6.0V	70 15 12	145 29 25	183 37 31	216 43 37	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_{REM}	Minimum Removal Time, Shift Load to Clock		2.0V 4.5V 6.0V	−2 −2 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time, (A, B, C, D, J, $\overline{K}$ to Clock)		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Set Up Time, Shift/Load to Clock		2.0V 4.5V 6.0V		125 25 21	156 31 26	188 38 32	ns ns ns
t_H	Minimum Hold Time Any Input except Shift/Load		2.0V 4.5V 6.0V	−10 −2 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width, Clock or Reset		2.0V 4.5V 6.0V	30 10 9	80 16 14	100 20 18	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

4

Timing Diagram



TL/F/5324–3

National Semiconductor

MM54HC221/MM74HC221
Dual Non-Retriggerable Monostable Multivibrator

General Description

The MM54/74HC221 high speed monostable multivibrators (one shots) utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC221 can be triggered on the positive transition of the clear while A is held low and B is held high.

The 'HC221 is a non-retriggerable, and therefore cannot be retriggered until the output pulse times out.

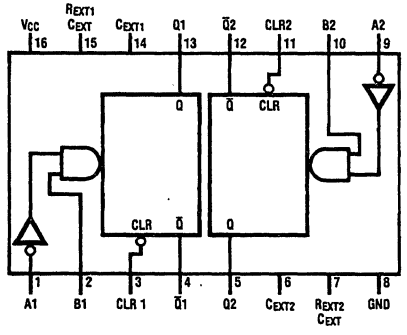
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})\ (C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs enable infinite signal input rise or fall times

Connection Diagram

Dual-In-Line Package

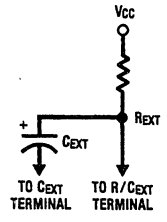


TL/F/5206–1

MM54HC221/MM74HC221

54HC221 (J) 74HC221 (J,N)

Timing Component



TL/F/5206–2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN} = V_{CC} or GND	6.0V		±0.5	±5.0	±5.0	μA
I_{IN}	Maximum Input Current (All other pins)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Standby)	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable	V_{IN} = V_{CC} or GND R/C_{EXT} = 0.5V_{CC}	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

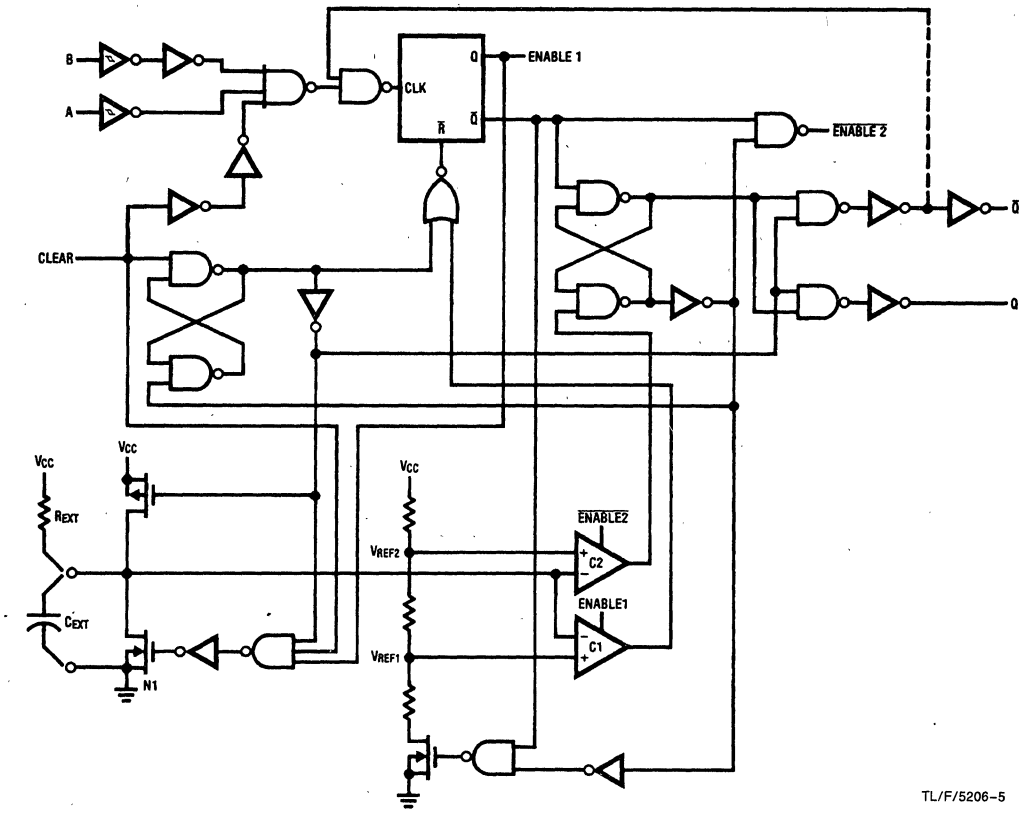
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		22	36	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay Clear to Q		20	31	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns(unless otherwise specified)

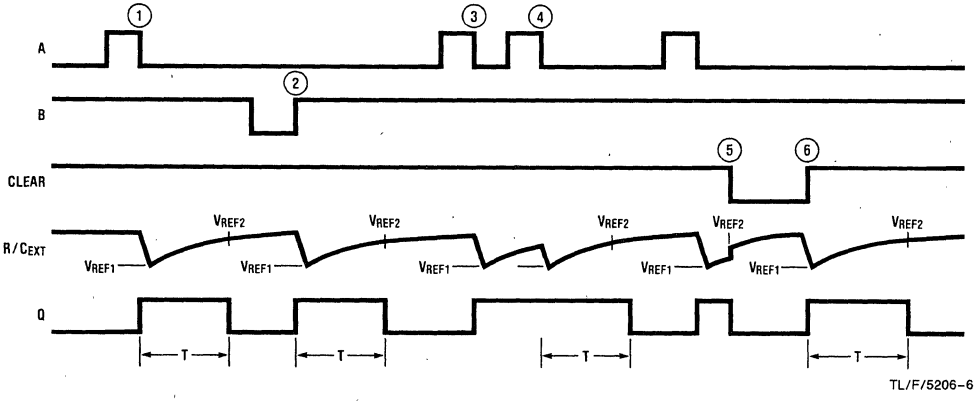
Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C		54HC $T_A=-55$ to 125°C		Units
					Typ	Guaranteed Limits				
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q			2.0V	77	169		194	210	ns
				4.5V	26	42		51	57	ns
				6.0V	21	32		39	44	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$			2.0V	88	197		229	250	ns
				4.5V	29	48		60	67	ns
				6.0V	24	38		46	51	ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V	54	114		132	143	ns
				4.5V	23	34		41	45	ns
				6.0V	19	28		33	36	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V	56	116		135	147	ns
				4.5V	25	36		42	46	ns
				6.0V	20	29		34	37	ns
t_W	Minimum Pulse Width A, B, Clear			2.0V	57	123		144	157	ns
				4.5V	17	30		37	42	ns
				6.0V	12	21		27	30	ns
t_{REM}	Minimum Clear Removal Time			2.0V		0		0	0	ns
				4.5V		0		0	0	ns
				6.0V		0		0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V		75		95	110	ns
				4.5V		15		19	22	ns
				6.0V		13		16	19	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF		2.0V	1.5					μs
		$R_{EXT}=2$ kΩ		4.5V	450					ns
		$R_{EXT}=6$ kΩ ($V_{CC}=2V$)		6.0V	380					ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	4.5V	1	0.9				ms
			Max	4.5	1	1.1				ms
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20		20	20	pF
C_{IN}	Maximum Input Capacitance (Other Inputs)				6	10		10	10	pF

Logic Diagram



TL/F/5206–5

Theory of Operation



TL/F/5206–6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING) 'HC123, 423 ONLY
⑤ RESET PULSE SHORTENING
⑥ CLEAR TRIGGER ('HC123, 'HC221 ONLY)

FIGURE 1.

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}②. The 'HC221 can also be triggered when clear goes from GND to V_{CC} (while A is at Gnd and B is at V_{CC}⑥.)

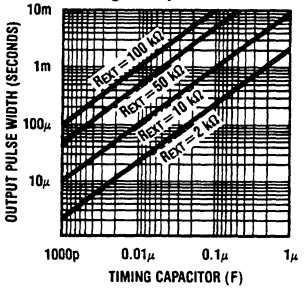
It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC221 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

The 'HC221 is non-retriggerable and will ignore input transitions on A and B until it has timed out ③ and ④.

RESET OPERATION

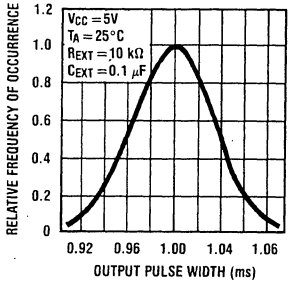
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



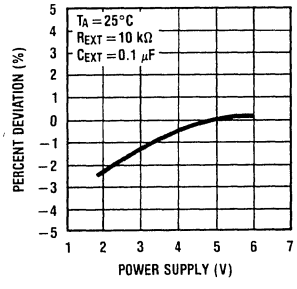
TL/F/5206–7

Typical Distribution of Output Pulse Width, Part to Part



TL/F/5206–8

Typical 1ms Pulse Width Variation vs. Supply



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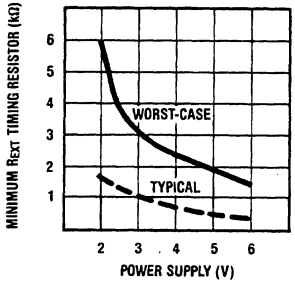
Minimum R_{EXT} vs. Supply Voltage



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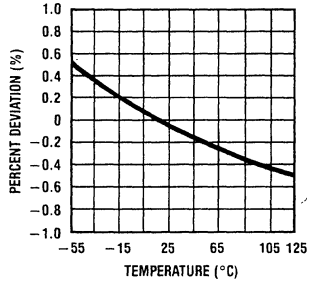
Typical 1 ms Pulse Width Variation vs. Temperature



TL/F/5206–11

National Semiconductor

MM54HC237/MM74HC237
3-to-8 Line Decoder With Address Latches

General Description

These devices utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to implement a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independantly of the select or latch-enable inputs. All of the outputs are low unless G1 is high and $\overline{G2}$ is low. The 'HC237 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

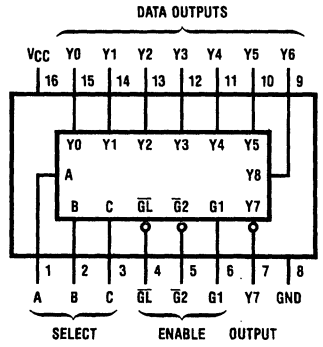
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing.
- Fanout of 10 LS-TTL loads.

Connection Diagram

Dual-In-Line Package

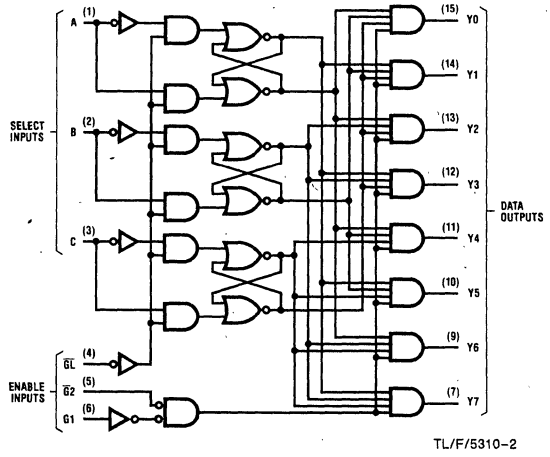


TL/F/5326–1

MM54HC237/MM74HC237

54HC237 (J) 74HC237(J,N)

Functional Block Diagram



TL/F/5310–2

Truth Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		20	41	ns
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		16	32	ns
t_{PLH}	Maximum Propagation $\overline{GL}$ to any Y Output		22	44	ns
t_{PHL}	Maximum Propagation Delay GL to any Y Output		17	33	ns
t_{PLH}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		16	35	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		14	25	ns
t_S	Minimum Set Up Time at A, B and C inputs		10	20	ns
t_H	Minimum Hold Time at A, B and C inputs		−3	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		9	16	ns

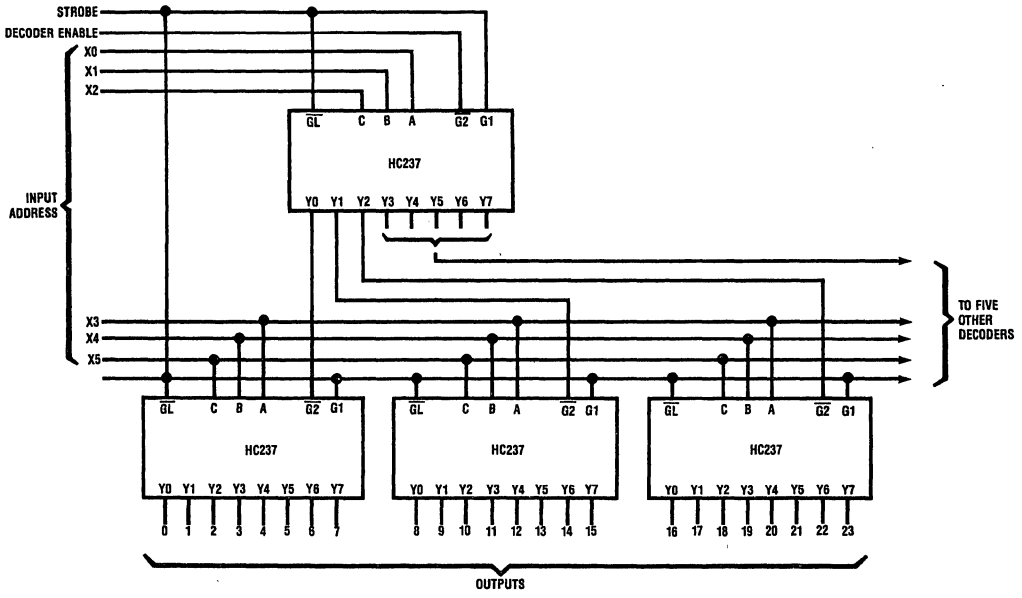
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	100	235	296	350	ns
			4.5V	24	47	59	70	ns
			6.0V	20	40	50	60	ns
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	80	185	233	276	ns
			4.5V	19	37	47	55	ns
			6.0V	17	31	40	47	ns
t_{PLH}	Maximum Propagation $\overline{GL}$ to any Y Output		2.0V	125	250	315	373	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	63	ns
t_{PHL}	Maximum Propagation Delay GL to any Y Output		2.0V	95	190	239	283	ns
			4.5V	19	38	48	75	ns
			6.0V	16	32	41	48	ns
t_{PLH}	Maximum Propagation Delay, G1 or $\overline{G2}$ to Output		2.0V	100	200	252	298	ns
			4.5V	20	40	50	60	ns
			6.0V	17	34	43	51	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		2.0V	73	145	183	216	ns
			4.5V	15	29	37	43	ns
			6.0V	12	25	31	37	ns
t_S	Minimum Set Up Time at A, B and C Inputs		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time at A, B and C Inputs		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			75				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Typical Application



TL/F/5326–3

6-Line to 64-Line Decoder with Input Address Storage

National Semiconductor

MM54HC240/MM74HC240 Inverting Octal TRI-STATE® Buffer MM54HC241/MM74HC241 Octal TRI-STATE Buffer

General Description

These Tri-State buffers utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. Each have a fanout of 15 LS-TTL equivalent inputs.

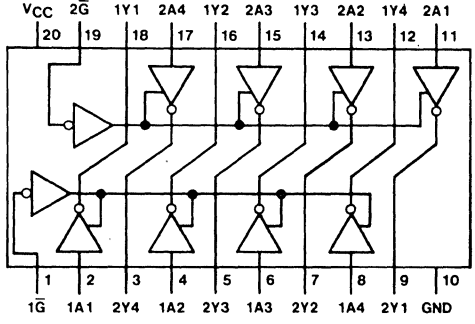
The MM54HC240/MM74HC240 is an inverting buffer and has two active low enables ($1\overline{G}$ and $2\overline{G}$). Each enable independently controls 4 buffers. MM54HC241/MM74HC241 is a non-inverting buffer that has one active low enable and one active high enable, each again controlling 4 buffers. Neither device has Schmitt trigger inputs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74 series)
- Output current: 6 mA

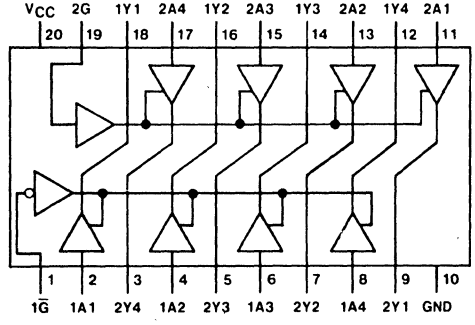
Connection Diagrams Dual-In-Line Packages



TL/L/5020–1

MM54HC240/MM74HC240

54HC240 (J) 74HC240 (J,N)



TL/L/5020–2

MM54HC241/MM74HC241

54HC241 (J) 74HC241 (J,N)

Truth Tables

('HC240)

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

('HC241)

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}, G=V_{IL}	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC240/MM74HC240

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ $C_L=45$ pF	14	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	$R_L=1$ kΩ $C_L=5$ pF	13	25	ns

AC Electrical Characteristics MM54HC240/MM74HC240

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	80	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	28	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	75	150	189	224	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}=V_{IH}$, $G=V_{IL}$		12				pF
		$\overline{G}=V_{IL}$, $G=V_{IH}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

AC Electrical Characteristics MM54HC241/MM74HC241

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions		Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF		13	20	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ	$1\overline{G}$	17	28	ns
		$C_L=45$ pF	2G	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Input	$R_L=1$ kΩ	$1\overline{G}$	15	25	ns
		$C_L=5$ pF	2G	13	25	ns

AC Electrical Characteristics MM54HC241/MM74HC241

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

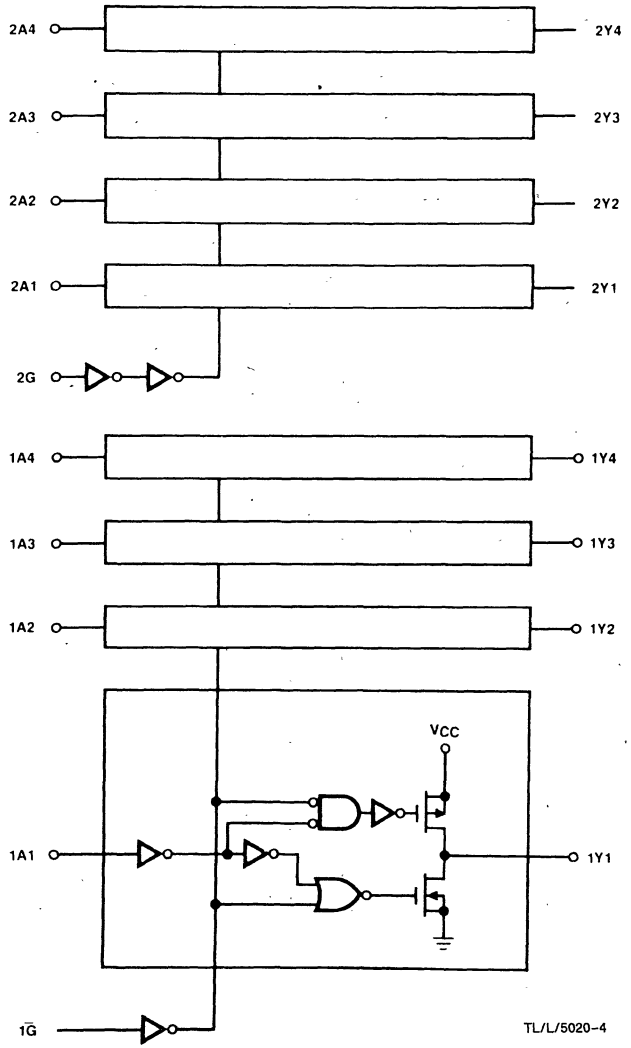
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	83	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	10	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	75	150	189	224	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}=V_{IH}$, $G=V_{IL}$		12				pF
		$\overline{G}=V_{IL}$, $G=V_{IH}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

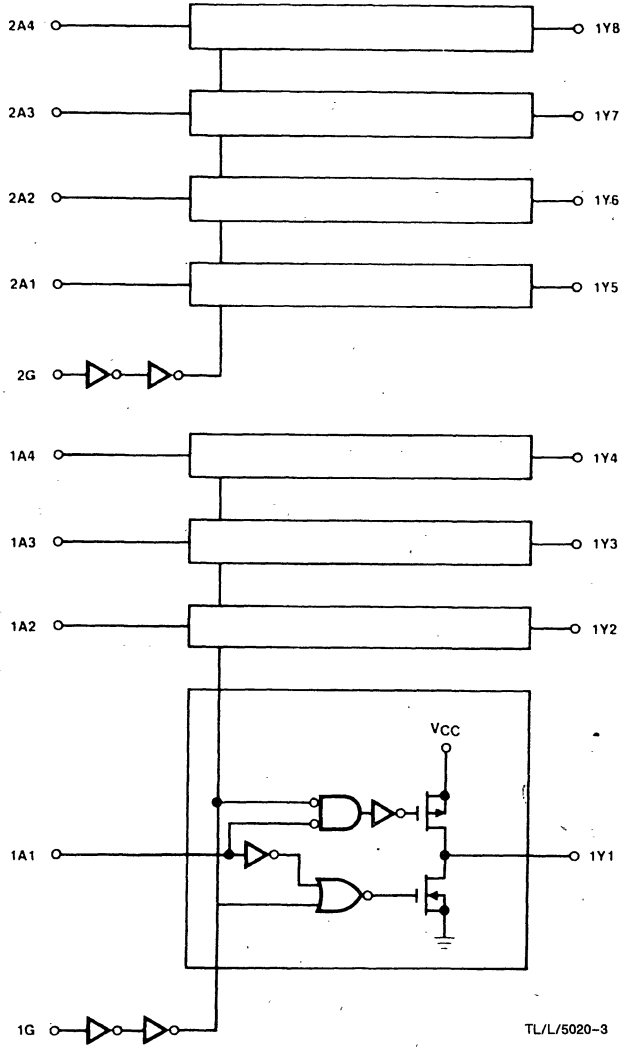
Logic Diagrams

'HC240



TL/L/5020-4

'HC241



TL/L/5020-3

National Semiconductor

MM54HC242/MM74HC242 Inverting Quad TRI-STATE® Transceiver MM54HC243/MM74HC243 Quad TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional inverting and non-inverting buffers utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation when driving large bus capacitances. These circuits possess the low power dissipation and high noise immunity associated with CMOS circuits, but speeds comparable to low power Schottky TTL circuits. They can also drive 15 LS-TTL loads.

The MM54HC242/MM74HC242 is a non-inverting buffer and the MM54HC243/MM74HC243 is an inverting buffer. Each device has one active high enable (GBA), and one active low enable (GAB). GBA enables the A outputs and GAB enables the B outputs. This device does not have Schmitt trigger inputs.

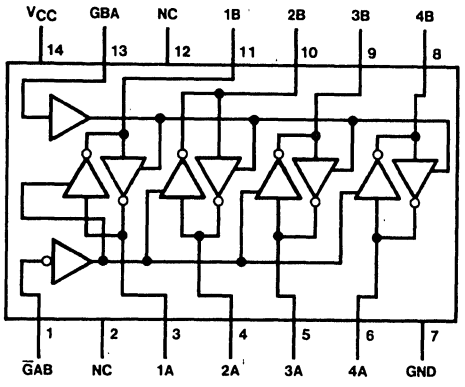
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs
- Two way asynchronous communication
- High output current: 6 mA (74HC)
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74HC)

Connection Diagrams

Dual-In-Line Package



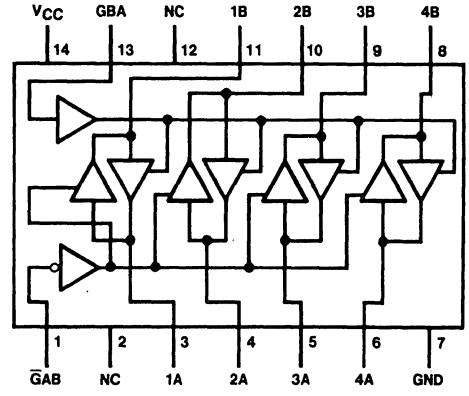
TL/L/5019–1

TOP VIEW

MM54HC242/MM74HC242

54HC242 (J) 74HC242 (J,N)

Dual-In-Line Package



TL/L/5019–2

TOP VIEW

MM54HC243/MM74HC243

54HC243 (J) 74HC243 (J,N)

Truth Tables

Control Inputs		Data Port Status	
$\overline{GAB}$	GBA	A	B
H	H	$\overline{OUTPUT}$	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	$\overline{OUTPUT}$

Control Inputs		Data Port Status	
$\overline{GAB}$	GBA	A	B
H	H	OUTPUT	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	OUTPUT

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	V_{OUT}=V_{CC} or GND $\overline{G}AB$=V_{IH}, GBA=V_{IL} ($\overline{G}AB$ and GBA only)	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2: Unless otherwise specified all voltages are referenced to ground.
Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.
Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics (MM54HC242/MM74HC242)

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PHL}	Maximum Output Disable Time from Active Output	$R_L=$kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics MM54HC242/MM74HC242

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	80	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	18	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from Active Output	$R_L=1$ kΩ	2.0V	75	150	189	224	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}=V_{IH}$, $G=V_{IL}$		12				pF
		$\overline{G}=V_{IL}$, $G=V_{IH}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

AC Electrical Characteristics (MM54HC243/MM74HC243)

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	13	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=k\Omega$ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from Active Output	$R_L=k\Omega$ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics MM54HC243/MM74HC243

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

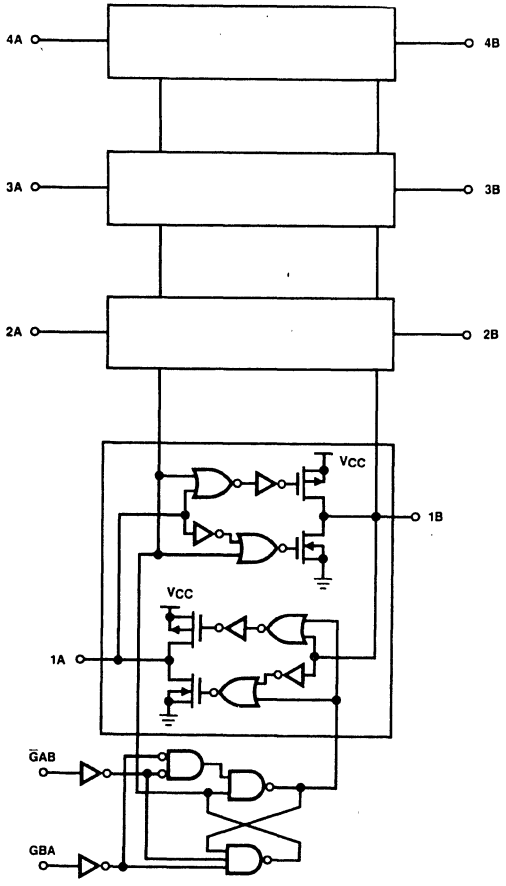
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	88	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	10	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from Active Output	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}=V_{IH}$, $G=V_{IL}$		12				pF
		$\overline{G}=V_{IL}$, $G=V_{IH}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagrams

MM54HC242/MM74HC242



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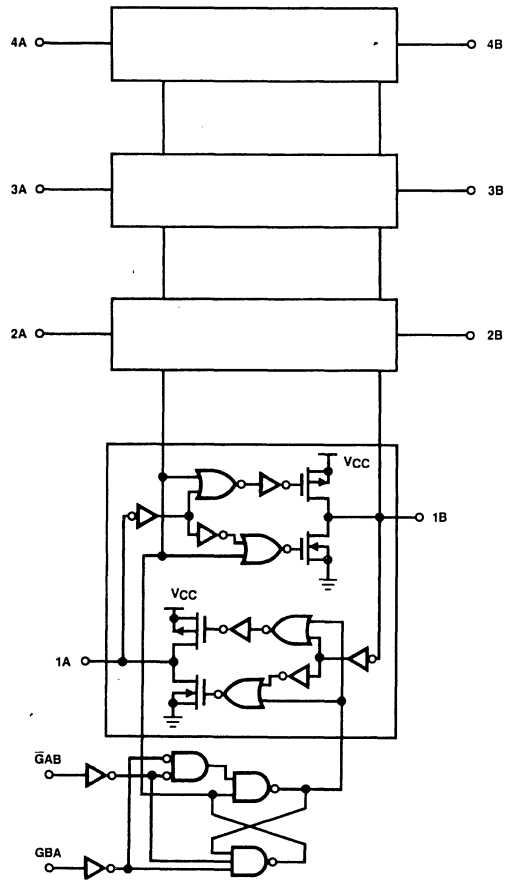
MM54HC243/MM74HC243



TL/L/5019–4

National Semiconductor

MM54HC244/MM74HC244 Octal TRI-STATE® Buffer

General Description

These TRI-STATE buffers utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and are general purpose high speed non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. All three devices have a fanout of 15 LS-TTL equivalent inputs.

The MM54HC244/MM74HC244 is a non-inverting buffer and has two active low enables (1G and 2G). Each enable independently controls 4 buffers. This device does not have Schmitt trigger inputs.

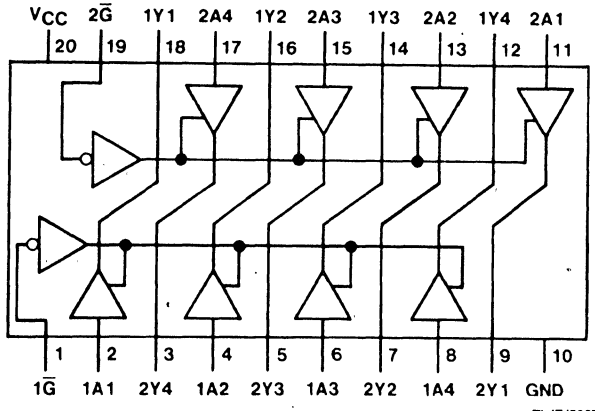
All inputs are protected from damage due to static discharge by diodes to V_{CC} and Ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74 series)
- Output current: 6 mA

Connection Diagram

Dual-In-Line Package



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MM54HC244/MM74HC244

54HC244 (J) 74HC244 (J,N)

Truth Table

('HC244)

1G	1A	1Y	2G	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	V_{IN}=V_{IH}, or V_{IL} V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC244/MM74HC244

V_{CC} = 5V, T_A = 25°C, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	R_L = 1 kΩ C_L = 45 pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay From Active Output	R_L = 1 kΩ C_L = 5 pF	15	25	ns

AC Electrical Characteristics

V_{CC} = 2.0V-6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

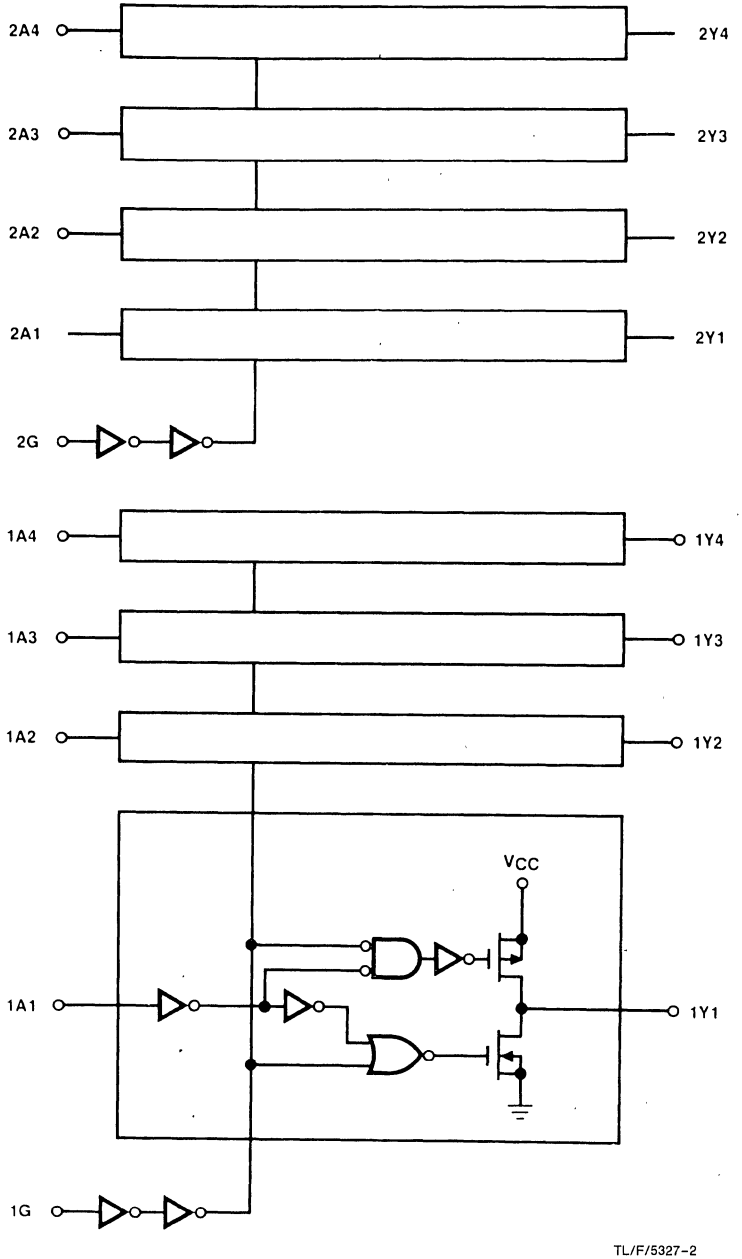
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	2.0V	58	115	145	171	ns
		C_L = 150 pF	2.0V	83	165	208	246	ns
		C_L = 50 pF	4.5V	14	23	29	34	ns
		C_L = 150 pF	4.5V	17	33	42	49	ns
		C_L = 50 pF	6.0V	10	20	25	29	ns
		C_L = 150 pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	75	750	189	224	ns
		C_L = 150 pF	2.0V	100	200	252	298	ns
		C_L = 50 pF	4.5V	15	30	38	45	ns
		C_L = 150 pF	4.5V	30	40	50	60	ns
		C_L = 50 pF	6.0V	13	26	32	38	ns
		C_L = 150 pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G} = V_{IH}$		12				pF
		$\overline{G} = V_{IL}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram

'HC244



TL/F/5327–2

National Semiconductor

MM54HC245/MM74HC245 Octal TRI-STATE® Transceiver

General Description

These TRI-STATE bi-directional buffers utilize micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

Each device has an active low enable input $\overline{G}$ and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC245/MM74HC245 transfers true data from one bus to the other.

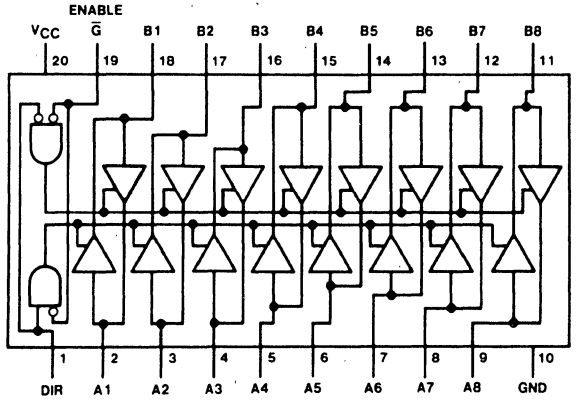
This device can drive up to 15 LS-TTL Loads, and does not have Schmitt trigger inputs. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74 HC)
- Tri-State outputs for connection to bus oriented systems
- High output drive: 6 mA (minimum)

Connection Diagram

Dual-In-Line Package



TL/F/5165–1

MM54HC245/MM74HC245

54HC245 (J) 74HC245 (J,N)

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5 to V_{CC}+1.5V
DC Input/Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	$V_{IN}=V_{CC}$ to GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	MaximumTri-State Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $\overline{G}=V_{IH}$, $V_{IN}=V_{IH}$ or V_{IL}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	13	17	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 45 pF	33	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 5 pF	32	42	ns

AC Electrical Characteristics

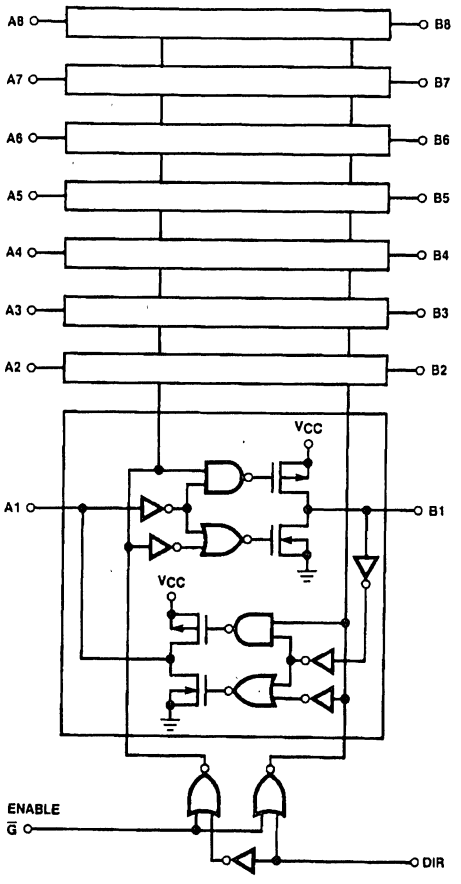
$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	2.0V	29	72	88	96	ns
		C_L = 150 pF	2.0V	38	96	116	128	ns
		C_L = 50 pF	4.5V	14	18	22	24	ns
		C_L = 150 pF	4.5V	18	24	29	32	ns
		C_L = 50 pF	6.0V	14	18	22	24	ns
		C_L = 150 pF	6.0V	18	24	29	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	70	184	224	240	ns
		C_L = 150 pF	2.0V	80	216	260	284	ns
		C_L = 50 pF	4.5V	35	46	56	60	ns
		C_L = 150 pF	4.5V	41	54	65	71	ns
		C_L = 50 pF	6.0V	31	41	50	54	ns
		C_L = 150 pF	6.0V	36	47	57	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0V	47	172	208	224	ns
			4.5V	33	43	52	56	ns
			6.0V	31	41	50	54	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V	20	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G}=V_{IL}$		70				pF
		$\overline{G}=V_{IH}$		12				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5165–2

'HC245

National Semiconductor

MM54HC251/MM74HC251
8-Channel TRI-STATE® Multiplexer

General Description

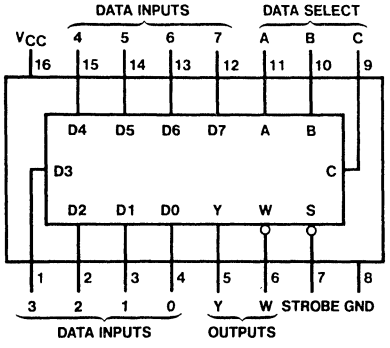
This 8-CHANNEL DIGITAL MULTIPLEXER with TRI-STATE outputs utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and W outputs. The 54HC/74HC logic family is speed, function, as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay
  Data Select to Y: 26 ns
- Wide supply range: 2–6V
- Low power supply quiescent current: 80 μA maximum (74HC)
- TRI-STATE outputs for interface to bus oriented systems

Connection Diagram



TL/F/5328–1

MM54HC251/MM74HC251

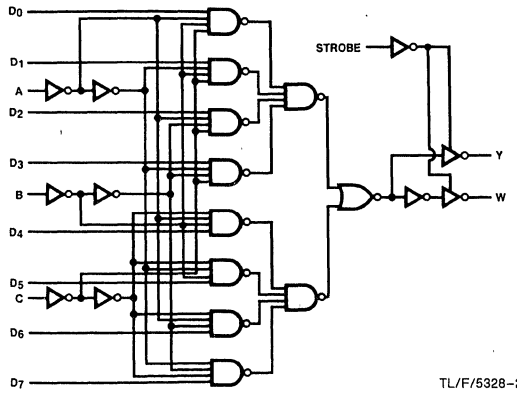
54HC251 (J) 74HC251 (J,N)

Truth Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

Logic Diagram



TL/F/5328–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE® Leakage Current	Strobe=V_{CC} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to W		24	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, W Output	$R_L=1k$ $C_L=50$ pF	19	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, Y Output	$R_L=1k$ $C_L=50$ pF	19	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1k$ $C_L=5$ pF	26	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1k$ $C_L=5$ pF	27	35	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V 4.5V 6.0V	90 31 26	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		2.0V 4.5V 6.0V	95 32 27	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to Y		2.0V 4.5V 6.0V	70 27 23	195 39 33	244 49 41	283 57 48	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to W		2.0V 4.5V 6.0V	75 29 25	185 37 32	231 46 40	268 54 46	ns ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time W Output	$R_L=1k$	2.0V 4.5V 6.0V	45 21 18	150 30 26	188 38 33	218 44 38	ns ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output	$R_L=1k$	2.0V 4.5V 6.0V	45 21 18	145 29 25	181 36 31	210 42 36	ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1k$	2.0V 4.5V 6.0V	60 29 25	220 44 37	275 55 46	319 64 54	ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1k$	2.0V 4.5V 6.0V	60 30 26	195 39 33	244 49 41	283 57 48	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC253/MM74HC253
Dual 4-Channel TRI-STATE® Multiplexer

General Description

The MM54HC253/MM74HC253 utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the capability to drive 10 LS-TTL loads. The large output drive and TRI-STATE features of this device make it ideally suited for interfacing with bus lines in bus organized systems. When the output control input is taken high, the multiplexer outputs are sent into a high impedance state.

When the output control is held low, the associated multiplexer chooses the correct output channel for the given input signals determined by the select A and B inputs.

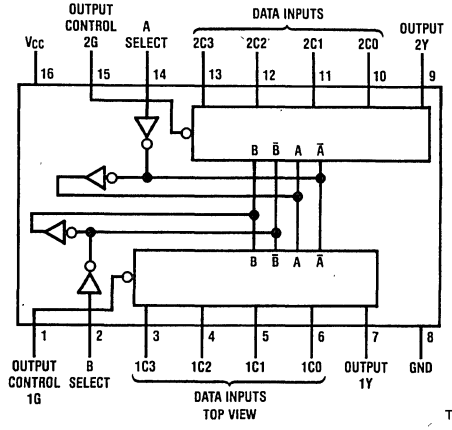
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5108–1

MM54HC253/MM74HC253

54HC253 (J) 74HC253 (J,N)

Truth Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off).

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	Strobe=V_{CC} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns, $C_L=15$ pF

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		24	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		18	23	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output to a Logic Level	$R_L=1k$	13	18	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output to High Impedance State	$R_L=1k$	18	27	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

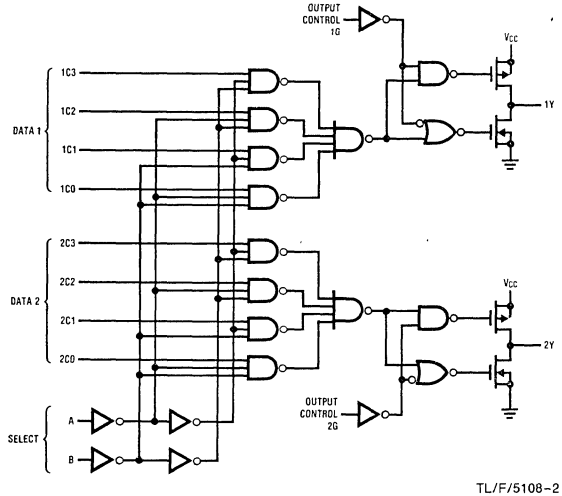
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		2.0V	131	158	198	237	ns
			4.5V	29	35	44	53	ns
			6.0V	24	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		2.0V	99	126	158	189	ns
			4.5V	22	28	35	42	ns
			6.0V	19	23	29	35	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1\ k\Omega$	2.0V	63	90	113	135	ns
			4.5V	14	20	25	30	ns
			6.0V	12	17	21	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1\ k\Omega$	2.0V	90	135	169	203	ns
			4.5V	20	30	38	45	ns
			6.0V	17	25	31	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Outputs Enabled		90				pF
		Outputs Disabled		25				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC-Switching Waveforms and Test Circuits.

Logic Diagram

'HC253



TL/F/5108–2

National Semiconductor

MM54HC257/MM74HC257
Quad 2-Channel TRI-STATE® Multiplexer

General Description

This QUAD 2-TO-1 LINE DATA SELECTOR/MULTIPLEXER utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive LS-TTL loads. The large output drive capability coupled with the TRI-STATE feature make this device ideal for interfacing with bus lines in a bus organized system. When the OUTPUT CONTROL input line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the OUTPUT CONTROL line is low, the SELECT input chooses whether the A or B input is used.

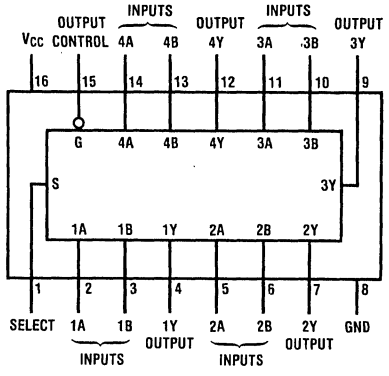
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- TRI-STATE outputs for connection to system buses.

Connection Diagram

Dual-In-Line Package

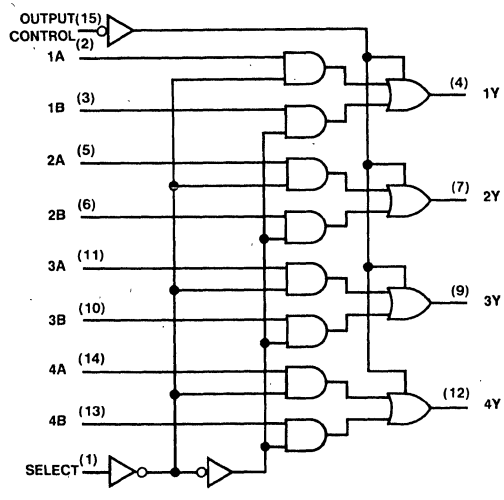


TL/F/5329–1

MM54HC257/MM74HC257

54HC257 (J) 74HC257 (J,N)

Logic Diagram



TL/F/5329–2

MM54HC257/MM74HC257

Truth Table

Inputs				
Output Control	Select	A	B	Output Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage	V_{OUT}=V_{CC} or GND OC=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Y Output	$C_L=45$ pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L=50$ pF	13	21	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L=1$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L=1$ kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Y Output	$C_L=50$ pF	2.0V	50	100	125	150	ns
		$C_L=150$ pF	2.0V	70	150	189	224	ns
		$C_L=50$ pF	4.5V	10	20	25	30	ns
		$C_L=150$ pF	4.5V	15	30	38	45	ns
		$C_L=50$ pF	6.0V	9	17	21	25	ns
		$C_L=150$ pF	6.0V	13	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L=50$ pF	2.0V	50	110	137	165	ns
		$C_L=150$ pF	2.0V	70	160	200	240	ns
		$C_L=50$ pF	4.5V	12	22	28	33	ns
		$C_L=150$ pF	4.5V	20	32	40	48	ns
		$C_L=50$ pF	6.0V	10	19	24	33	ns
		$C_L=150$ pF	6.0V	17	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Any Y Output to a Logic Level	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Inpedance State	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per mux)						
		Enable		30				pF
		Disabled		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC259/MM74HC259
8-Bit Addressable Latch/3-to-8 Line Decoder

General Description

This device utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to implement an 8-bit addressable latch, designed for general purpose storage applications in digital systems.

The MM54HC259/MM74HC259 has a single data input (D), 8 latch outputs (Q1–Q8), 3 address inputs (A, B, and C), a common enable input (E), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addressed output. The data is stored when ENABLE transitions from low to high. All unaddressed latches will remain unaffected. With enable in the high state the device is deselected, and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

If enable is held high and CLEAR is taken low all eight latches are cleared to a low state. If enable is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

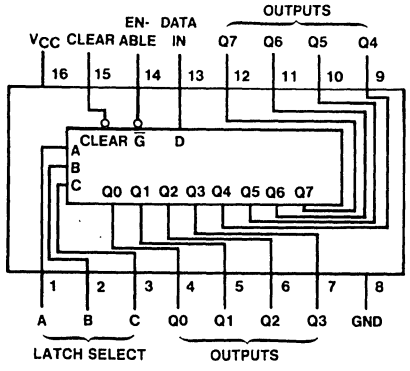
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide supply range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)

Connection Diagram

Dual-In-Line Package



TL/F/5006–1

MM54HC259/MM74HC259

54HC259 (J) 74HC259 (J,N)

Truth Table

Inputs		Outputs of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Decoder
L	H	L	L	Clear

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level.

D = the level at the data input

Q_{i0} the level of Q_i (i = 0, 1 . . . 7, as appropiate) before the indicated steady-state input conditions were established.

4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

(V_{CC} = 5.0V, T_A = 25°C, $t_r = t_f$ = 6 ns, C_L = 15 pF unless otherwise specified.)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		18	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		20	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		20	35	ns
t_{PHL}	Maximum Propagation Delay Clear to Output		17	27	ns
t_W	Minimum Enable Pulse Width		10	16	ns
t_W	Minimum Clear Pulse Width		10	16	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	ns
t_S	Minimum Setup Time Select or Data to Enable		15	20	ns
t_H	Minimum Hold Time Data or Address to Enable		−2	0	ns

AC Electrical Characteristics $t_r = t_f$ = 6 ns, C_L = 50 pF, V_{CC} = 2.0V–6.0V

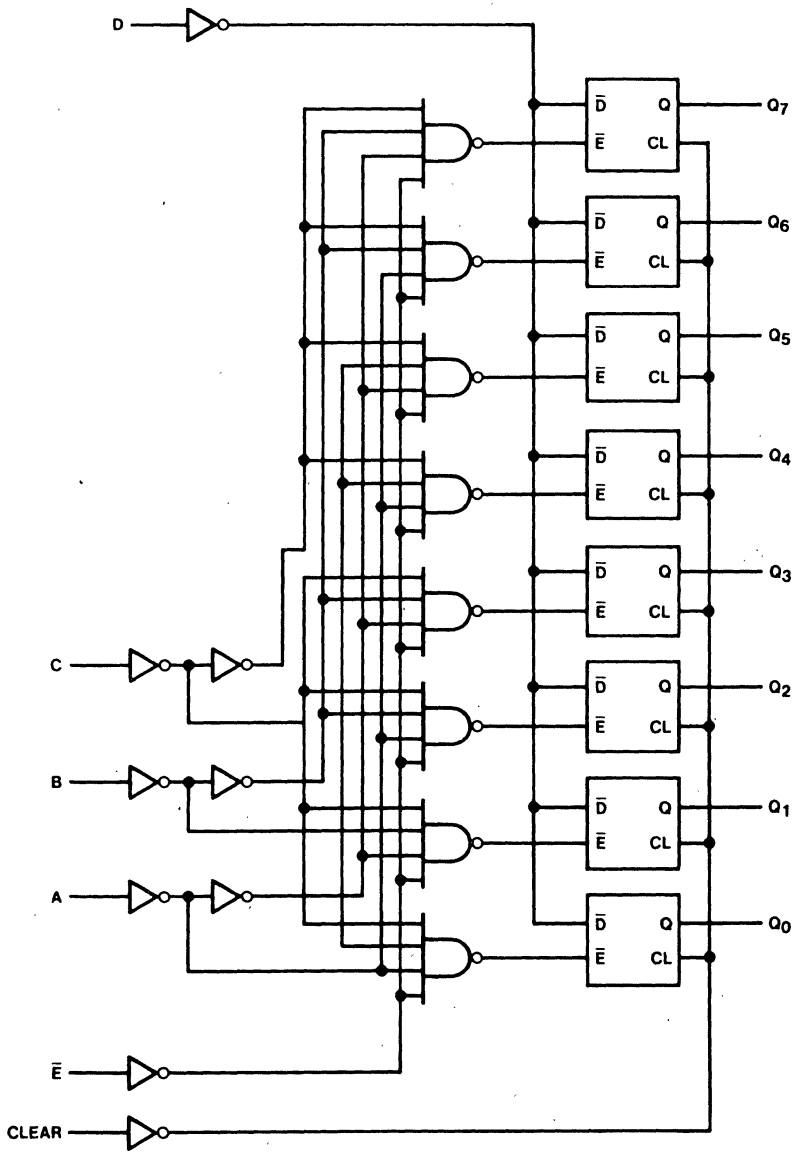
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		2.0V	60	180	225	250	ns
			4.5V	19	37	46	52	ns
			6.0V	17	32	40	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		2.0V	72	220	275	310	ns
			4.5V	21	43	54	60	ns
			6.0V	18	37	46	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		2.0V	65	200	250	280	ns
			4.5V	27	40	50	58	ns
			6.0V	23	35	44	50	ns
t_{PHL}	Maximum Propagation Delay Clear to Output		2.0V	50	150	190	210	ns
			4.5V	18	31	39	44	ns
			6.0V	16	26	32	37	ns
t_W	Minimum Pulse Width Clear or Enable		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_S	Minimum Setup Time Address or Data to Enable		2.0V		100	125	150	ns
			4.5V		20	25	28	ns
			6.0V		15	19	25	ns
t_H	Minimum Hold Time Address or Data to Enable		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram

MM54HC259/MM74HC259



TL/F/5006–2

National Semiconductor

MM54HC266/MM74HC266 Quad 2-Input Exclusive NOR Gate

General Description

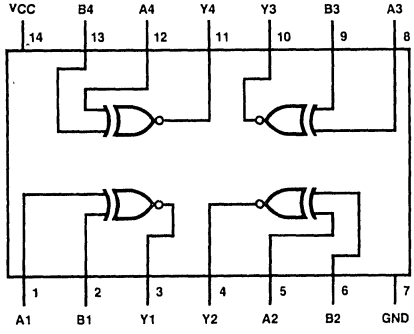
This exclusive NOR gate utilizies microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The MM54HC/MM74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. However, unlike the 'LS266 which is an open collector gate the 'HC266 has standard CMOS push-pull outputs. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 9 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 20 μA maximum (74 series)
- Output drive capability: 10 LS-TTL loads
- Push-pull output

Connection Diagram

Dual-In-Line Package



TL/F/5330–1

MM54HC266/MM74HC266

54HC266 (J) 74HC266 (J,N)

Truth Table

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

$Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HC273/MM74HC273 Octal D Flip-Flops With Clear

General Description

These edge triggered flip-flops utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The CLEAR input when low, sets all outputs to a low state.

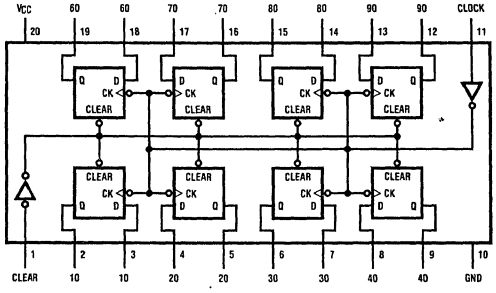
Each output can drive 10 low power Schottky TTL equivalent loads. The MM54HC273/MM74HC273 is functionally as well as pin compatible to the 54LS273/74LS273. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA (74 series)
- Output drive: 10 LSTTL loads

Connection Diagram

Dual-In-Line Package

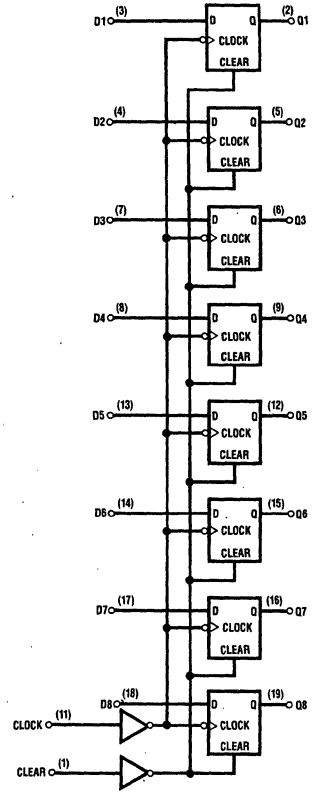


TL/F/5331–1

MM54HC273/MM74HC273

54HC273 (J) 74HC273 (J,N)

Logic Diagram



TL/F/5331–2

Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level (steady state)

L = Low level (steady state)

X = Don't Care

↑ = Transition from low to high level

Q_0 = The level of Q before the indicated steady-state input conditions were established

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		18	27	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		18	27	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		−2	0	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V	50	160	200	240	ns
			4.5V	21	32	40	48	ns
			6.0V	19	27	33	40	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		2.0V	50	160	200	240	ns
			4.5V	21	32	40	48	ns
			6.0V	19	27	33	40	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Set Up Time Data to Clock		2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		175				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC280/MM74HC280
9-Bit Odd/Even Parity Generator/Checker

General Description

The MM54HC280/MM74HC280 utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits. It possesses the ability to drive 10 LS-TTL loads.

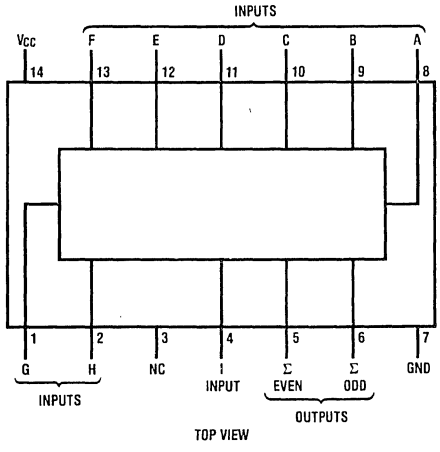
This parity generator/checker features odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading devices. The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 28 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5121–1

MM54HC280/MM74HC280

54HC280 (J) 74HC280 (J,N)

Function Table

Numbers of Inputs A thru I that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Even		28	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Odd		28	35	ns

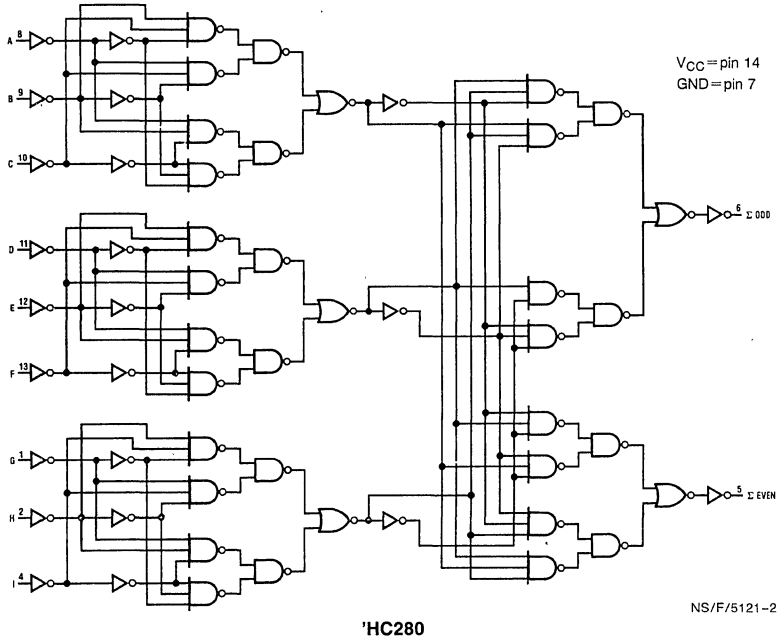
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Even		2.0V	103	205	258	305	ns
			4.5V	21	41	52	61	ns
			6.0V	17	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Odd		2.0V	103	205	258	305	ns
			4.5V	21	41	52	61	ns
			6.0V	17	35	44	52	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



NS/F/5121-2

'HC280

National Semiconductor

PRELIMINARY

MM54HC283/MM74HC283
4-Bit Binary Adder with Fast Carry

General Description

This full adder performs the addition of two 4-bit binary numbers utilizing microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

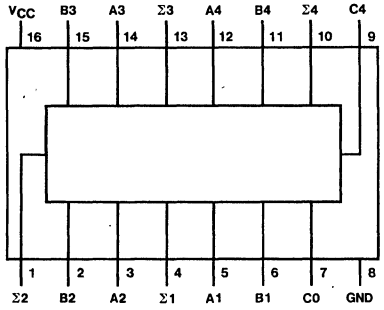
- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Wide supply range: 2V to 6V
- Low quiescent power consumption: 8 μA at 25°C
- Low input current: <1 μA

Typical Add Times

Two 8-Bit Words	Two 16-Bit Words
25 ns	45 ns

Connection Diagram

Dual-In-Line Package



TL/F/5332–1

MM54HC283/MM74HC283

54HC283 (J) 74HC283 (J,N)

Truth Table

Input								Output									
								When C0 = L						When C0 = H			
												When C2 = L					When C2 = H
A1	A3	B1	B3	A2	A4	B2	B4	Σ1	Σ3	Σ2	Σ4	C2	C4	Σ1	Σ3	Σ2	Σ4	C2	C4
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	L	L
H	H	L	L	L	L	L	L	L	H	L	L	L	L	H	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L	L	H	H	L	L	L	L
H	L	H	L	L	L	L	L	H	H	L	L	L	L	L	L	H	H	L	L
L	H	H	L	L	L	L	L	H	H	L	L	L	L	L	L	H	H	L	L
H	H	H	L	L	L	L	L	L	L	H	L	L	L	H	L	H	H	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	H	H	L	L	L	L
H	L	L	H	L	L	L	L	H	H	L	L	L	L	L	L	H	H	L	L
L	H	L	H	L	L	L	L	H	H	L	L	L	L	L	L	H	H	L	L
H	H	L	H	L	L	L	L	L	L	H	L	L	L	H	L	H	H	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L	H	L	H	H	L	L
H	L	H	H	L	L	L	L	H	L	H	L	L	L	L	H	H	H	L	L
L	H	H	H	L	L	L	L	H	L	H	L	L	L	L	H	H	H	L	L
H	H	H	H	L	L	L	L	L	H	H	L	L	L	H	H	H	H	L	L

H = High Level, L = Low Level

Note Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to $\Sigma 1$ or $\Sigma 2$		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to $\Sigma 3$		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to $\Sigma 4$		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to Σ_I		15	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to C4		11	17	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to C4		12	17	ns

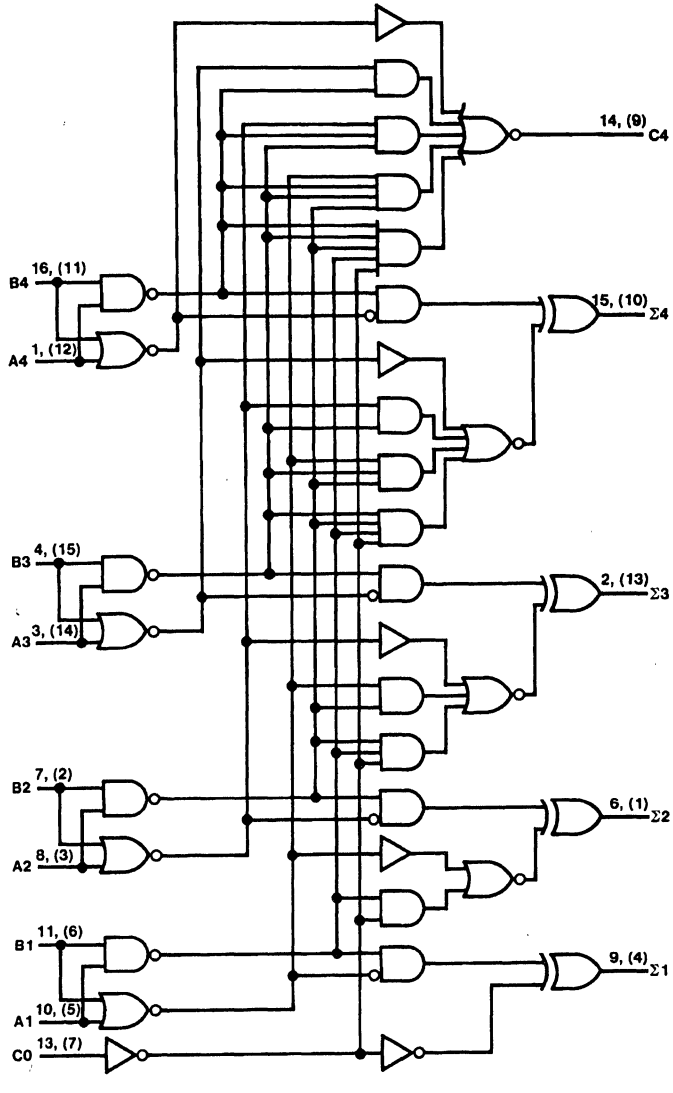
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to $\Sigma 1$ or $\Sigma 2$		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to $\Sigma 3$		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to $\Sigma 4$		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to Σ_I		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to C4		2.0V	52	125	156	188	ns
			4.5V	17	25	31	38	ns
			6.0V	14	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A_I or B_I to C4		2.0V	56	130	162	195	ns
			4.5V	18	26	32	39	ns
			6.0V	14	22	27	33	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	28	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	μF
C_{PD}	Power Dissipation Capacitance (Note 5)							μF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5332–2

'HC283

National Semiconductor

PRELIMINARY

MM54HC292/MM74HC292, MM54HC294/MM74HC294 Programmable Frequency Dividers/Digital Timers

General Description

These high speed dividers/timers utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These programmable frequency dividers/digital timers contain 31 flip-flops ('HC292) or 15 flip-flops ('HC294) plus 30 gates on a single chip. The count modulo is under digital control of the inputs provided.

Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided (TP1, TP2, and TP3 on the 'HC292 and TP on the 'HC294). These test points are not intended to drive system loads. Both types feature two clock inputs; either one may be used for clock gating. (See the truth table below.)

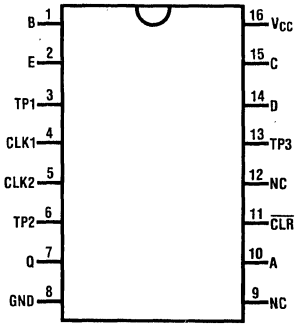
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Count divider chain
- Digitally programmable from 2^2 to 2^n (n = 31 for 'HC292, n = 15 for 'HC294)
- Usable frequency range from DC to 30 MHz
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Easily cascadable
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



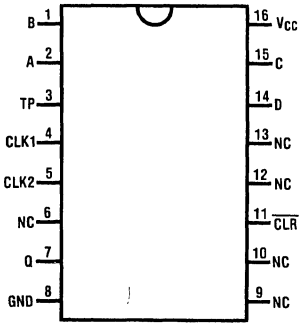
TL/F/5333–1

TOP VIEW

MM54HC292/MM74HC292

54HC292 (J) 74HC292 (J,N)

Dual-In-Line Package



TL/F/5333–2

TOP VIEW

MM54HC294/MM74HC294

54HC294 (J) 74HC294 (J,N)

'HC292, 'HC294 Truth Table

CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↑	L	Count
H	L	↑	Count
H	H	X	Inhibit
H	X	H	Inhibit

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CLK1, CLK2 to Q Output		80	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CLK1, CLK2 to TP Output		80		ns
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to Q Output		80		ns
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to TP Output	$\overline{CLR}$ to TP Output	80		ns
t_{REM}	Minimum Removal Time, $\overline{CLR}$ to CLK1, CLK2	$\overline{CLR}$ to CLK1, CLK2	10	20	ns
t_W	Minimum Pulse Width $\overline{CLR}$ to CLK1, CLK2	CLK1, CLK2	10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 45 50	5 27 32	4 21 25	3 18 21	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CLK1, CLK2 to Q Output		2.0V 4.5V 6.0V	300 80 70	600 120 100	750 150 125	900 180 150	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CLK1, CLK2 to TP Output		2.0V 4.5V 6.0V	380 80 70				ns ns ns
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to Q Output		2.0V 4.5V 6.0V	380 80 70				ns ns ns
t_{PHL}	Maximum Propagation Delay, $\overline{CLR}$ to TP Output		2.0V 4.5V 6.0V	380 80 70				ns ns ns
t_{REM}	Minimum Removal Time $\overline{CLR}$ to CLK1, CLK2		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time (Q Output)		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_W	Minimum Pulse Width $\overline{CLR}$, CLK1, CLK2		2.0V 4.5V 6.0V	30 10 9	80 16 14	100 20 18	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

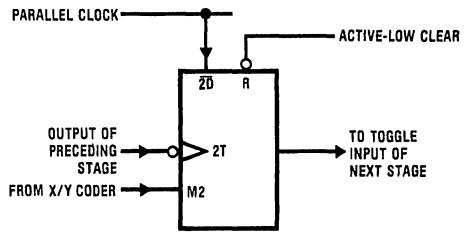
Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Operation

A brief look at the digital timing capabilities will show that with a 1-MHz input frequency, programming for 2^{10} will give a period of 1.024 ms, and 2^{20} will give a period of 1.05s, 2^{26} will give a period of 1.12 min, and 2^{31} will give a period of 35.79 min.

The functional block diagram shows that the count modulo is controlled by an X/Y decoder connected to the mode-control inputs of several flip-flops. These flip flops with mode controls each have a "D" input connected to the parallel clock line and a "T" input driven by the preceding stage. The parallel clock frequency is always the input frequency divided by four.

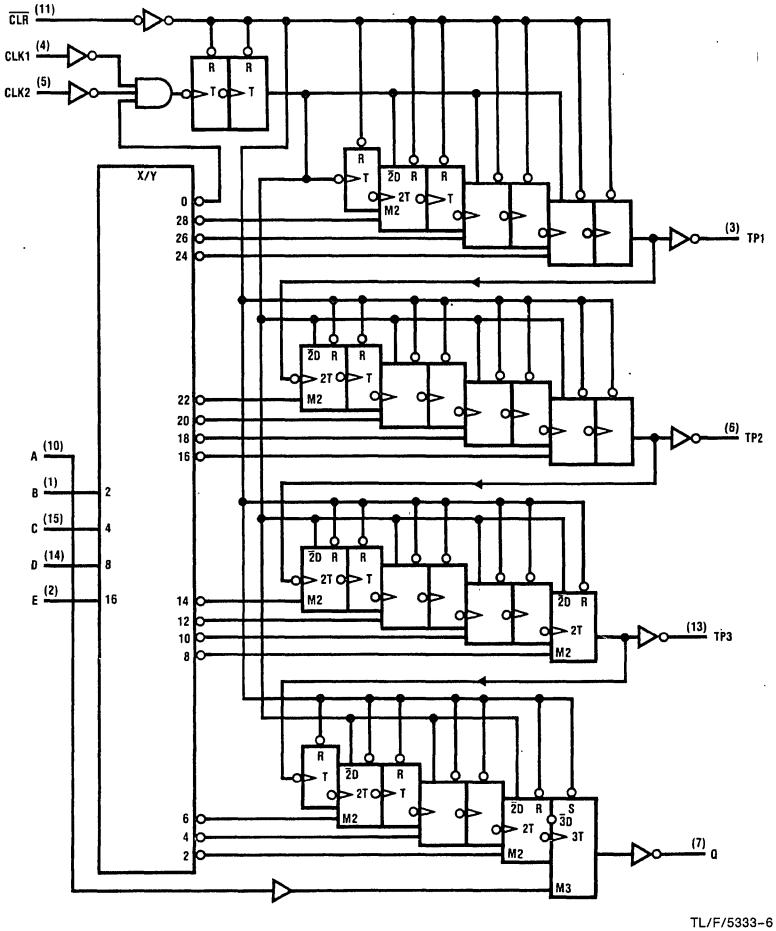
The X/Y decoder output selected by the programming inputs goes low. While a mode control is low, the "D" input of the flip-flop is enabled, and the signal from the parallel clock line ($f_{IN} \div 4$) is passed to the "T" input of the following stage. All the other mode controls are high enabling the "T" inputs and causing each flip-flop in turn to divide by two.



TL/F/5333–3

Functional block diagram (positive logic)

'HC292



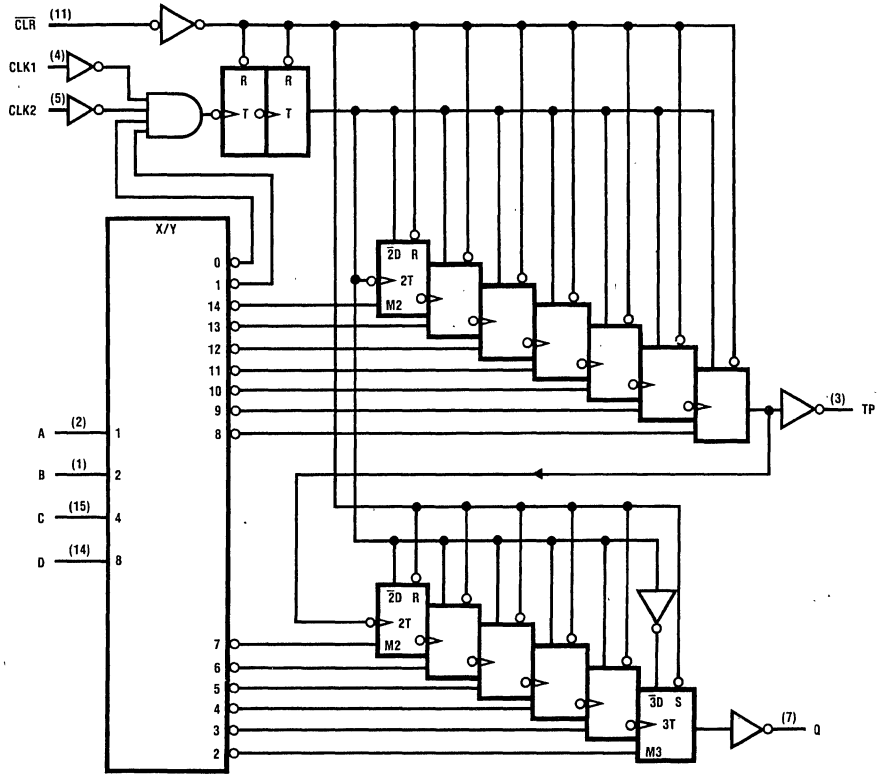
TL/F/5333–6

'HC292 Function Table

Programming Inputs					Frequency Division							
					Q		TP1		TP2		TP3	
E	D	C	B	A	Binary	Decimal	Binary	Decimal	Binary	Decimal	Binary	Decimal
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^4	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

Functional block diagram (positive logic)

'HC294



TL/F/5333–7

'HC294 Function Table

Programming Inputs				Frequency Division			
				Q		TP	
D	C	B	A	Binary	Decimal	Binary	Decimal
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

PRELIMINARY

National Semiconductor

MM54HC298/MM74HC298 Quad 2-Multiplexers With Storage

General Description

These high speed quad two input multiplexers with storage utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. Both circuits feature high noise immunity and low power consumption associated with CMOS circuitry, along with speeds comparable to low power Schottky TTL logic.

These circuits are controlled by the signals WORD SELECT and CLOCK. When the WORD SELECT input is taken low Word 1 (A1, B1, C1 and D1) is presented to the inputs of the flip-flops, and when WORD SELECT is high Word 2 (A2, B2, C2 and D2) is presented to the inputs of the flip-flops. The selected word is clocked to the output terminals on the negative edge of the clock pulse.

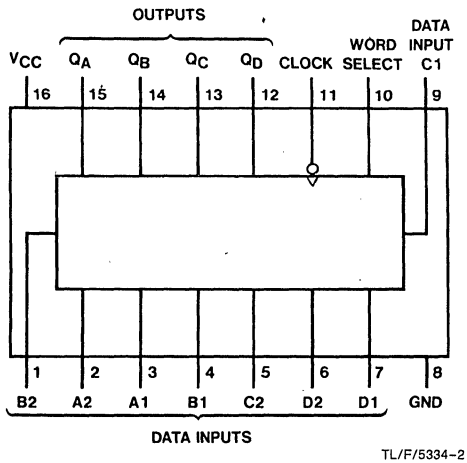
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, Clock to output: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package

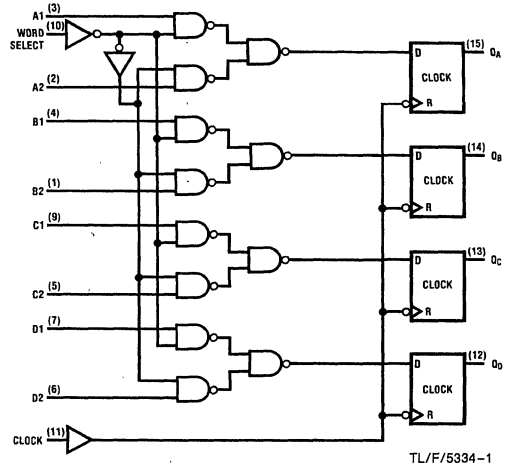


TL/F/5334–2

MM54HC298/MM74HC298

54HC298 (J) 74HC298 (J,N)

Logic Diagram



TL/F/5334–1

Truth Table

Inputs		Outputs			
Word Select	Clock	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↓ = Transition from high to low level
a1, a2, etc. = The level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = The level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Parameter			Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Ouput			21	32	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			15	32	ns
t_W	Width of Clock Pulse, High or Low Level			10	16	ns
t_{SETUP}	Setup Time	Data		5	20	ns
		Word Select		10	20	
t_{HOLD}	Hold Time	Data		−2	0	ns
		Word Select		−2	0	

AC Electrical Characteristics

$C_L=50$ pF, $t_r=t_f=6$ ns

Symbol	Parameter		Conditions	V_{CC}	54HC/74HC $T_A=25°C$ Typ	54HC/74HC $T_A=25°C$ Guaranteed Limits	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
t_{PLH}	Propagation Delay Time Low-to-High Level Output			2.0V	75	185	231	278	ns
				4.5V	25	37	46	56	ns
				6.0V	20	31	39	47	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output			2.0V	75	185	231	278	ns
				4.5V	25	37	46	56	ns
				6.0V	20	31	39	47	ns
t_W	Width of Clock Pulse High or Low Level			2.0V	35	80	100	120	ns
				4.5V	10	16	20	24	ns
				6.0V	9	14	18	21	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			2.0V	90	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
t_{SETUP}	Set-up Time	Data		2.0V	35	100	125	150	ns
				4.5V	5	20	25	30	ns
				6.0V	4	17	21	25	ns
		Word Select		2.0V	40	100	125	150	ns
				4.5V	10	20	25	30	ns
				6.0V	9	17	21	25	ns
t_{HOLD}	Hold Time	Data		2.0V	−10	0	0	0	ns
				4.5V	−3	0	0	0	ns
				6.0V	−2	0	0	0	ns
		Word Select		2.0V	−10	0	0	0	ns
				4.5V	−3	0	0	0	ns
				6.0V	−2	0	0	0	ns

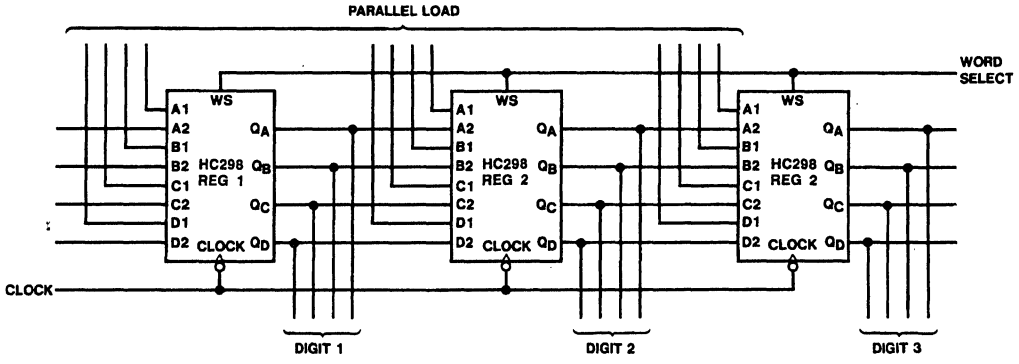
Typical Applications

Figure 1 illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.

When the word select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered into the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

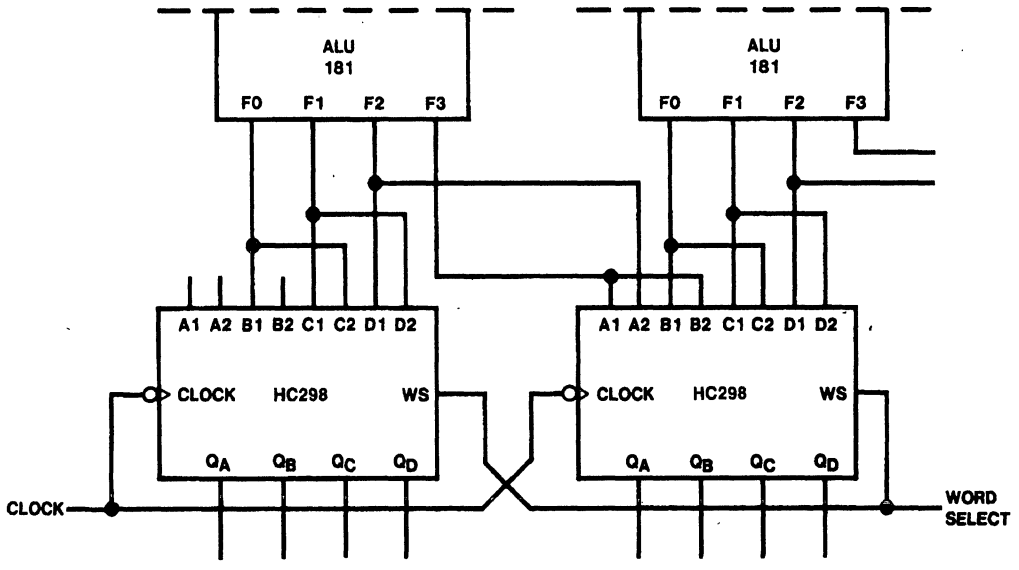
Another function that can be implemented with the MM54HC298/MM74HC298 is a register that can be designed specifically for supporting multiplier or division operations. *Figure 2* is an example of a one place/two place shift register.

When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.



TL/F/5334–3

FIGURE 1



TL/F/5334–4

FIGURE 2

National Semiconductor

MM54HC299/MM74HC299
8-Bit TRI-STATE® Universal Shift Register

General Description

This 8-bit TRI-STATE shift/storage register utilizes micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS. Along with the low power consumption and high noise immunity of standard CMOS integrated circuits, it has the ability to drive 15 LS-TTL loads. This circuit also features operating speeds comparable to the equivalent low power Schottky device.

The MM54HC299/MM74HC299 features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus oriented system.

Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines S0 and S1 high. This places the TRI-STATE outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding CLEAR input is provided to clear the register whether the outputs are enabled or disabled.

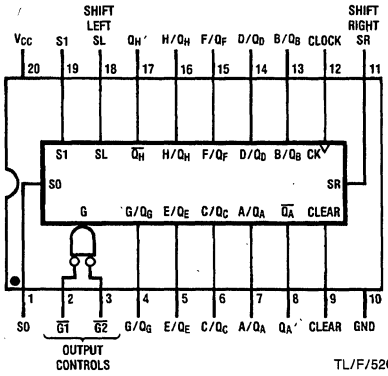
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency 40 MHz
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HC)
- High output drive for bus applications
- Low quiescent current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5207–1

TOP VIEW

MM54HC299/MM74HC299

54HC299 (J) 74HC299 (J,N)

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L or H	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{GN}
	H	L	H	L	L	↑	X	H	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{GN}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA ($Q_{A'}$, $Q_{H'}$)
	±35 mA (others)
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	$Q_{A'}$ & $Q_{H'}$ Outputs	V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
	A/Q_A thru H/Q_H Outputs	V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	$Q_{A'}$ and $Q_{H'}$ Outputs	V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
	A/Q_A thru H/Q_H Outputs	V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\| \leq 6$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Currrent	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}	6.0V		±0.5	±0.5	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns, $C_L=45$ pF

Symbol	Parameter		Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			40	25	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q_A, or Q_H,			25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A, or Q_H,			39	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_A–Q_H		$C_L=45$ pF	25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A–Q_H		$C_L=45$ pF	28	40	ns
t_{PZL}, t_{PZH}	Maximum Enable Time		$C_L=45$ pF $R_L=1$ kΩ	10	35	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time		$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_S	Minimum Set-Up Time	Select			20	ns
		Data			20	
t_H	Minimum Hold Time	Select			0	ns
		Data			0	
t_W	Minimum Pulse Width			12	20	ns
t_{REM}	Clear Removal Time				10	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	5	4	3.5	MHz
			4.5V	25	20	18	MHz
			6.0V	29	23	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_A, orQ_H,		2.0V	15	170	210	240	ns
			4.5V	27	38	48	54	ns
			6.0V	25	35	44	49	ns
t_{PHL}	Maximum Propagation Delay Clear to Q_A, orQ_H,		2.0V	70	200	250	280	ns
			4.5V	30	44	55	62	ns
			6.0V	26	38	46	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_A–Q_H	$C_L=50$ pF	2.0V	65	170	210	240	ns
		$C_L=150$ pF	2.0V	100	206	260	295	ns
		$C_L=50$ pF	4.5V	27	38	48	54	ns
		$C_L=150$ pF	4.5V	34	46	57	66	ns
		$C_L=50$ pF	6.0V	25	35	44	49	ns
		$C_L=150$ pF	6.0V	31	39	49	55	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_A–Q_H	$C_L=50$ pF	2.0V	70	200	250	280	ns
		$C_L=150$ pF	2.0V	110	236	295	325	ns
		$C_L=50$ pF	4.5V	30	44	55	62	ns
		$C_L=150$ pF	4.5V	37	52	65	75	ns
		$C_L=50$ pF	6.0V	26	38	46	52	ns
		$C_L=150$ pF	6.0V	32	46	57	64	ns

AC Electrical Characteristic (Continued)

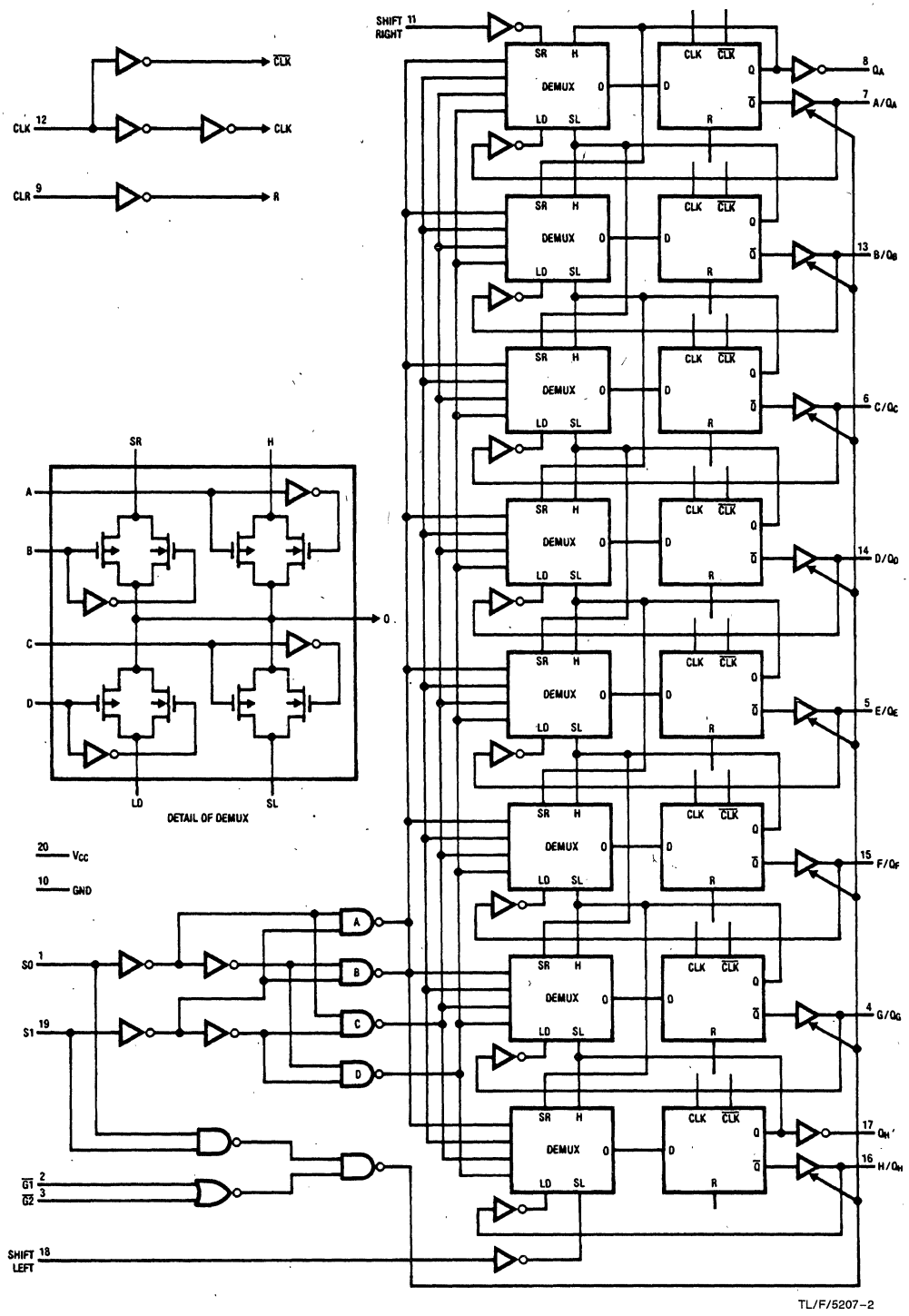
$C_L = 50$ pF ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L = 1\ k\Omega$					
		$C_L = 50$ pF	2.0V	70	160	200	225	ns
		$C_L = 150$ pF	2.0V	90	220	275	310	ns
		$C_L = 50$ pF	4.5V	22	32	40	45	ns
		$C_L = 150$ pF	4.5V	30	44	55	62	ns
		$C_L = 50$ pF	6.0V	19	28	34	38	ns
		$C_L = 150$ pF	6.0V	24	47	47	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1\ k\Omega$	2.0V	70	160	200	225	ns
		$C_L = 50$ pF	4.5V	22	32	40	45	ns
			6.0V	19	28	34	38	ns
t_S	Minimum Set Up Time, Data Select S_L or S_R		2.0V		100	125	140	ns
			4.5V		20	25	28	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Data Select, S_L or S_R		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{REM}	Minimum Clear Removal Time		2.0V		10	10	10	ns
			4.5V		10	10	10	ns
			6.0V		10	10	10	ns
t_W	Minimum Pulse Width, Clock and Clear		2.0V		100	125	140	ns
			4.5V		20	25	28	ns
			6.0V		17	21	25	ns
t_r, t_f	Maximum Input Rise and Fall Time				500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance	Outputs Enabled		240				pF
		Outputs Disabled		110				pF
C_{IN}	Maximum Input Capacitance Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Tri-State Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5207–2

National Semiconductor

MM54HC354/MM74HC354, MM54HC356/MM74HC356 8-Channel TRI-STATE® Multiplexers with Latches

General Description

The MM54HC354/MM74HC354 and MM54HC356/MM74HC356 utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They exhibit the high noise immunity and low power dissipation of standard CMOS integrated circuits, along with the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data select address is stored in transparent latches that are enabled by a low level address on pin 11, $\overline{SC}$. Data on the 8 input lines is stored in a parallel input/output register which in the MM54HC354/MM74HC354 is composed of 8 transparent latches enabled by a low level on pin 9, $\overline{DC}$, and in the MM54HC356/MM74HC356 is composed of 8 edge-triggered flip-flops, clocked by a low to high transition on pin 9, CLK. Both true (Y) and complementary (W) TRI-STATE outputs are available on both devices.

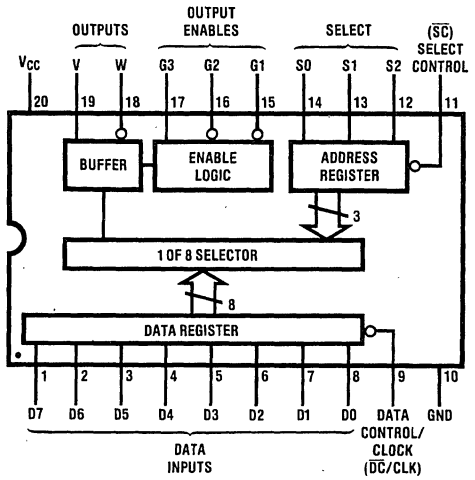
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS-TTL logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Transparent latches on data select inputs
- Choice of data registers:
  Transparent ('354)
  Edge-triggered ('356)
- TRI-STATE complementary outputs with fan-out of 15 LS-TTL loads
- Typical propagation delay:
  Data to output ('354): 32 ns
  Clock to output ('346): 35 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μA maximum
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5208–1

MM54HC354/MM74HC354, MM54HC356/MM74HC356

54HC354 (J) 74HC354 (J,N)
54HC356 (J) 74HC356 (J,N)

Function Table

Inputs								Outputs	
Select†			Data Control 'HC354	Clock 'HC356	Output Enables				
S1	S2	S0	$\overline{DC}$	CLK	$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H	H or L	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

Z = high-impedance state (off state)

↑ = transition from low to high level

D0 . . . D7 = the level steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of 'HC356

$D0_n$ . . . $D7_n$ = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock.

†This column shows the input address set-up with $\overline{SC}$ low.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| < 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{G1}$ = V_{CC}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

MM54HC354/MM74HC354

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0–D7 to either Output	$C_L=45$ pF	32	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{DC}$ to either Output	$C_L=45$ pF	38	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	$C_L=45$ pF	40	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	$C_L=45$ pF	42	58	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	17	24	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	23	32	ns
t_S	Minimum Set-Up Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		3	10	ns
t_H	Minimum Hold Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		0	5	ns
t_W	Minimum Pulse Width, $\overline{SC}$ or $\overline{DC}$		10	15	ns

MM54HC356/MM74HC356

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay CLK to either Output	$C_L=45$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	$C_L=45$ pF	40	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	$C_L=45$ pF	42	58	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	17	24	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	23	32	ns
t_S	Minimum Set-Up Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		3	10	ns
t_H	Minimum Hold Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		0	5	ns
t_W	Minimum Pulse Width, $\overline{SC}$ or CLK		10	15	ns

AC Electrical Characteristics

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

MM54HC354/MM74HC354

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0–D7 to either Output	C_L = 50 pF	2.0V	90	235	294	352	ns
		C_L = 150 pF	2.0V	100	275	344	412	ns
		C_L = 50 pF	4.5V	35	47	59	70	ns
		C_L = 150 pF	4.5V	40	55	68	83	ns
		C_L = 50 pF	6.0V	26	40	50	60	ns
		C_L = 150 pF	6.0V	32	46	58	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{DC}$ to either Output	C_L = 50 pF	2.0V	115	270	337	405	ns
		C_L = 150 pF	2.0V	125	310	387	465	ns
		C_L = 50 pF	4.5V	40	54	68	82	ns
		C_L = 150 pF	4.5V	46	62	78	93	ns
		C_L = 50 pF	6.0V	32	46	58	69	ns
		C_L = 150 pF	6.0V	38	52	66	78	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	C_L = 50 pF	2.0V	120	285	356	427	ns
		C_L = 150 pF	2.0V	130	325	406	488	ns
		C_L = 50 pF	4.5V	42	57	71	86	ns
		C_L = 150 pF	4.5V	50	65	81	97	ns
		C_L = 50 pF	6.0V	34	48	60	72	ns
		C_L = 150 pF	6.0V	40	55	69	82	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	C_L = 50 pF	2.0V	120	300	375	450	ns
		C_L = 150 pF	2.0V	110	340	425	510	ns
		C_L = 50 pF	4.5V	45	60	75	90	ns
		C_L = 150 pF	4.5V	52	68	85	102	ns
		C_L = 50 pF	6.0V	36	51	64	77	ns
		C_L = 150 pF	6.0V	42	58	72	87	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	50	125	156	188	ns
		C_L = 150 pF	2.0V	60	165	206	248	ns
		C_L = 50 pF	4.5V	18	25	31	38	ns
		C_L = 150 pF	4.5V	25	33	41	49	ns
		C_L = 50 pF	6.0V	15	21	26	32	ns
		C_L = 150 pF	6.0V	21	28	35	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ	2.0V	68	165	206	248	ns
		C_L = 50 pF	4.5V	24	33	40	46	ns
			6.0V	20	28	35	42	ns
t_S	Minimum Set-Up Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		2.0V	6	50	60	75	ns
			4.5V	3	10	13	15	ns
			6.0V	3	10	13	15	ns
t_H	Minimum Hold Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		2.0V	0	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	0	5	5	5	ns
t_W	Minimum Pulse Width $\overline{SC}$ or $\overline{DC}$		2.0V	30	80	100	120	ns
			4.5V	10	16	20	27	ns
			6.0V	10	15	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Active		150				pF
		TRI-STATE		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

AC Electrical Characteristics

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

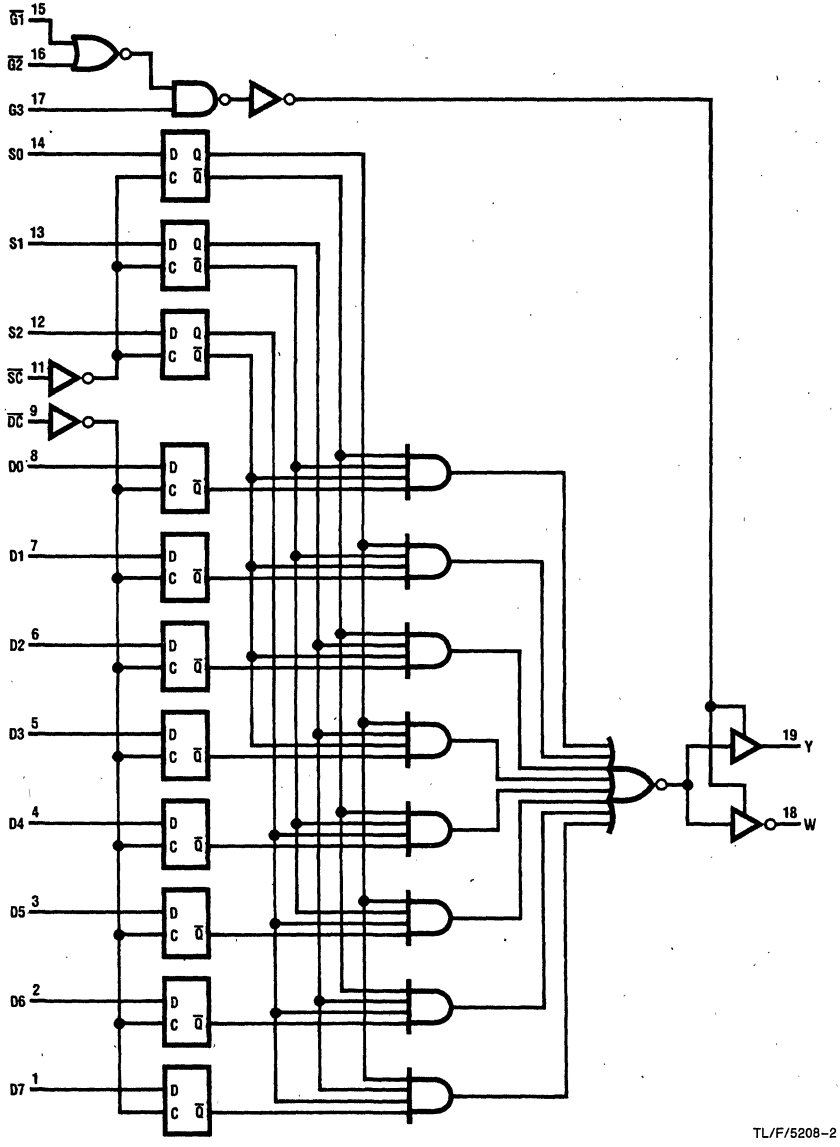
MM54HC356/MM74HC356

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay CLK to either Output	C_L = 50 pF	2.0V	100	225	318	338	ns
		C_L = 150 pF	2.0V	110	295	369	442	ns
		C_L = 50 pF	4.5V	36	51	63	76	ns
		C_L = 150 pF	4.5V	42	59	73	90	ns
		C_L = 50 pF	6.0V	28	43	53	64	ns
		C_L = 150 pF	6.0V	34	50	63	75	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	C_L = 50 pF	2.0V	120	285	356	427	ns
		C_L = 150 pF	2.0V	130	325	406	488	ns
		C_L = 50 pF	4.5V	42	57	71	86	ns
		C_L = 150 pF	4.5V	50	65	81	97	ns
		C_L = 50 pF	6.0V	34	48	60	72	ns
		C_L = 150 pF	6.0V	40	55	69	82	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	C_L = 50 pF	2.0V	120	300	375	450	ns
		C_L = 150 pF	2.0V	110	340	425	510	ns
		C_L = 50 pF	4.5V	45	60	75	90	ns
		C_L = 150 pF	4.5V	52	68	85	102	ns
		C_L = 50 pF	6.0V	36	51	64	77	ns
		C_L = 150 pF	6.0V	42	58	72	87	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	50	125	156	188	ns
		C_L = 150 pF	2.0V	60	165	206	248	ns
		C_L = 50 pF	4.5V	18	25	31	38	ns
		C_L = 150 pF	4.5V	25	33	41	49	ns
		C_L = 50 pF	6.0V	15	21	26	32	ns
		C_L = 150 pF	6.0V	21	28	35	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ	2.0V	68	165	206	248	ns
		C_L = 50 pF	4.5V	24	33	41	49	ns
			6.0V	20	28	35	42	ns
t_S	Minimum Set-Up Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		2.0V	6	50	50	50	ns
			4.5V	3	10	10	10	ns
			6.0V	3	10	10	10	ns
t_H	Minimum Hold Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		2.0V	0	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	0	5	5	5	ns
t_W	Minimum Pulse Width $\overline{SC}$ to CLK		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	10	15	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Active		150				pF
		TRI-STATE		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

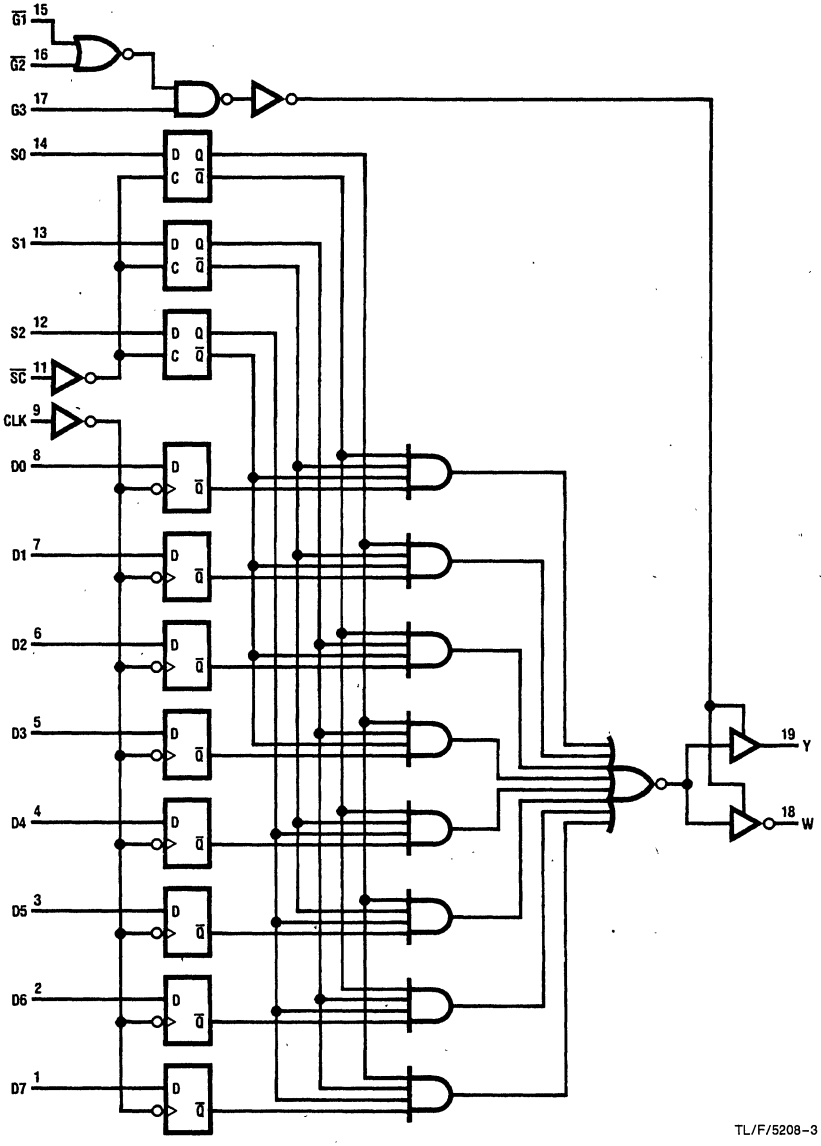
Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

'HC354 Logic Diagram



TL/F/5208–2

'HC356 Logic Diagram



National Semiconductor

MM54HC365/MM74HC365 Hex TRI-STATE® Buffer
MM54HC366/MM74HC366 Inverting Hex TRI-STATE Buffer
MM54HC367/MM74HC367 Hex TRI-STATE Buffer
MM54HC368/MM74HC368 Inverting Hex TRI-STATE Buffer

General Description

These TRI-STATE buffers are general purpose high speed inverting and non-inverting buffers that utilize micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. All 4 circuits are capable of driving up to 15 low power Schottky inputs.

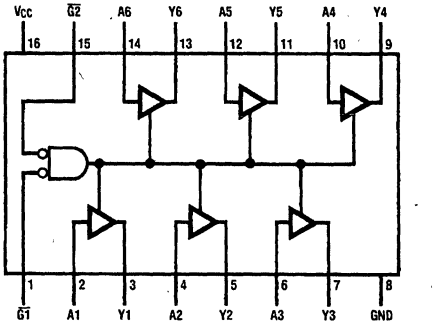
The MM54/74HC366 and the MM54/74HC368 are inverting buffers, where as the MM54/74HC365 and the MM54/74HC367 are non-inverting buffers. The MM54/74HC365 and the MM54/74HC366 have two Tri-State control inputs ($\overline{G1}$ and $\overline{G2}$) which are NORed together to control all six gates. The MM54/74HC367 and the MM54/74HC368 also have two output enables, but one enable ($\overline{G1}$) controls 4 gates and the other ($\overline{G2}$) controls the remaining 2 gates.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 series)
- Output drive capability: 15 LS-TTL loads

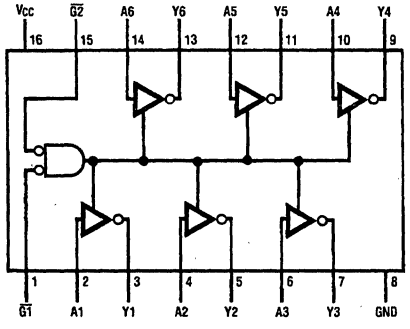
Connection Diagram Dual-In-Line Packages



TL/F/5209–1

MM54HC365/MM74HC365

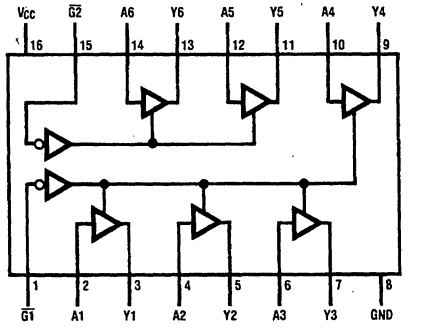
54HC365 (J) 74HC365 (J,N)



TL/F/5209–2

MM54HC366/MM74HC366

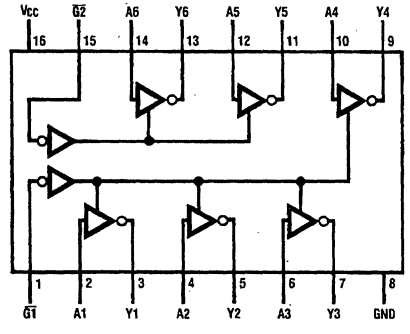
54HC366 (J) 74HC366 (J,N)



TL/F/5209–3

MM54HC367/MM74HC367

54HC367 (J) 74HC367 (J,N)



TL/F/5209–4

MM54HC368/MM74HC368

54HC368 (J) 74HC368 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC365/MM74HC365

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	15	22	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	29	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	25	36	ns

AC Electrical Characteristics MM54HC365/MM74HC365

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	35	105	130	150	ns
		$C_L=150$ pF	2.0V	45	135	168	205	ns
		$C_L=50$ pF	4.5V	14	24	30	36	ns
		$C_L=150$ pF	4.5V	17	29	36	45	ns
		$C_L=50$ pF	6.0V	11	19	24	28	ns
		$C_L=150$ pF	6.0V	15	24	30	36	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	90	230	287	345	ns
		$C_L=150$ pF	2.0V	98	245	306	367	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	38	53	66	80	ns
		$C_L=50$ pF	6.0V	25	35	43	52	ns
		$C_L=150$ pF	6.0V	29	41	51	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	58	175	218	260	ns
		$C_L=50$ pF	4.5V	26	44	55	66	ns
			6.0V	22	37	46	55	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Truth Table

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

AC Electrical Characteristics MM54HC366/MM74HC366

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	29	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	25	36	ns

AC Electrical Characteristics MM54HC366/MM74HC366

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	33	82	102	125	ns
		$C_L=150$ pF	2.0V	43	107	134	160	ns
		$C_L=50$ pF	4.5V	12	19	24	30	ns
		$C_L=150$ pF	4.5V	16	26	32	39	ns
		$C_L=50$ pF	6.0V	10	16	20	24	ns
		$C_L=150$ pF	6.0V	14	22	27	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						ns
		$C_L=50$ pF	2.0V	90	230	287	345	ns
		$C_L=150$ pF	2.0V	98	245	306	367	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	38	53	66	80	ns
		$C_L=50$ pF	6.0V	25	35	43	52	ns
		$C_L=150$ pF	6.0V	29	41	51	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	58	175	218	260	ns
			4.5V	26	44	55	66	ns
			6.0V	22	37	46	55	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Truth Table

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

AC Electrical Characteristics MM54HC367/MM74HC367

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	13	22	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	23	37	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	25	33	ns

AC Electrical Characteristics MM54HC367/MM74HC367

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$		Units
				Typ	Guaranteed Limits				
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	35	105		130	150	ns
		$C_L=150$ pF	2.0V	45	135		168	205	ns
		$C_L=50$ pF	4.5V	14	24		30	36	ns
		$C_L=150$ pF	4.5V	17	29		36	45	ns
		$C_L=50$ pF	6.0V	11	19		24	28	ns
		$C_L=150$ pF	6.0V	15	24		30	36	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ							ns
		$C_L=50$ pF	2.0V	69	172		216	250	ns
		$C_L=150$ pF	2.0V	75	187		233	280	ns
		$C_L=50$ pF	4.5V	24	38		47	57	ns
		$C_L=150$ pF	4.5V	29	46		57	69	ns
		$C_L=50$ pF	6.0V	22	35		43	52	ns
		$C_L=150$ pF	6.0V	26	42		52	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	47	117		146	220	ns
		$C_L=50$ pF	4.5V	22	35		44	52	ns
			6.0V	19	31		39	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60		75	90	ns
			4.5V	7	12		15	18	ns
			6.0V	6	10		13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45					pF
		Any Disabled A Input		8					pF
C_{IN}	Maximum Input Capacitance			5	10		10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20		20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Truth Table

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

AC Electrical Characteristics MM54HC368/MM74HC368

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	11	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	23	37	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	33	ns

AC Electrical Characteristics MM54HC368/MM74HC368

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	33	82	102	125	ns
		$C_L=150$ pF	2.0V	43	107	134	160	ns
		$C_L=50$ pF	4.5V	12	19	24	30	ns
		$C_L=150$ pF	4.5V	16	26	32	39	ns
		$C_L=50$ pF	6.0V	10	16	20	24	ns
		$C_L=150$ pF	6.0V	14	22	27	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						ns
		$C_L=50$ pF	2.0V	69	172	216	250	ns
		$C_L=150$ pF	2.0V	75	187	233	280	ns
		$C_L=50$ pF	4.5V	24	38	47	57	ns
		$C_L=150$ pF	4.5V	29	46	57	69	ns
		$C_L=50$ pF	6.0V	22	35	43	52	ns
		$C_L=150$ pF	6.0V	26	42	52	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	47	117	146	220	ns
			4.5V	22	35	44	52	ns
			6.0V	19	31	39	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Input Capacitance			10	20	20	20	pF

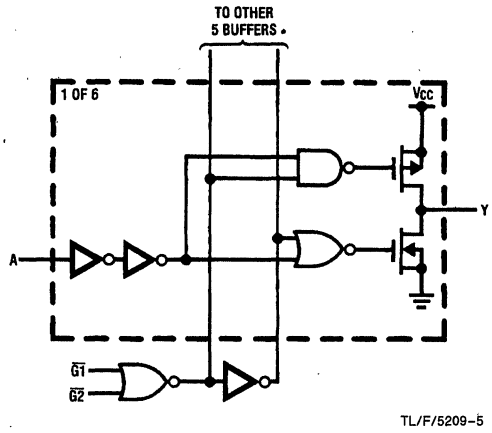
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Truth Table

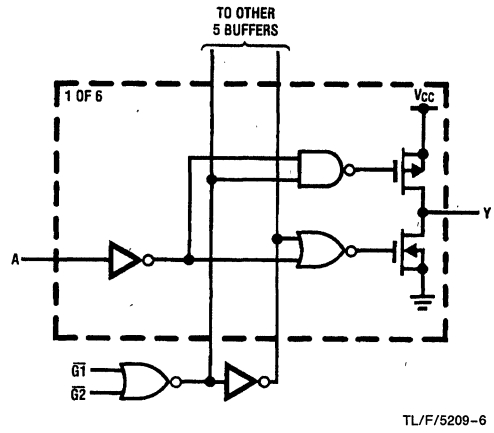
Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

Logic Diagrams



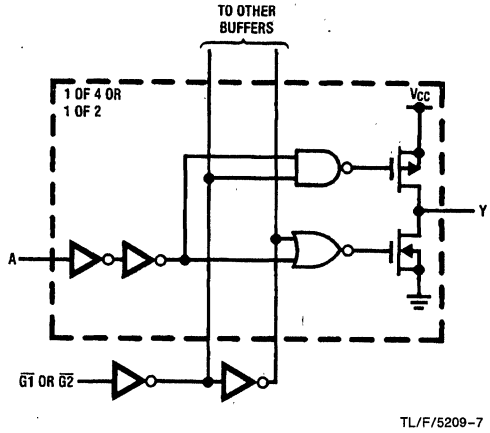
TL/F/5209–5

MM54HC365/MM74HC365



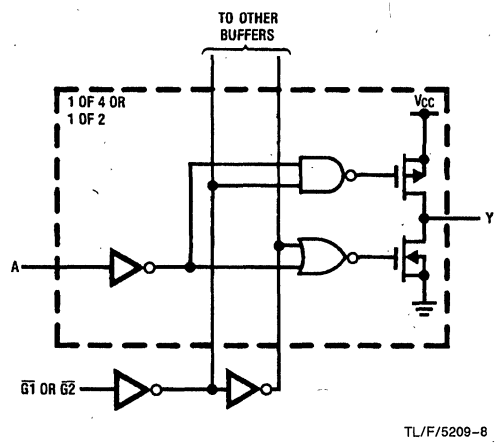
TL/F/5209–6

MM54HC366/MM74HC366



TL/F/5209–7

MM54HC367/MM74HC367



TL/F/5209–8

MM54HC368/MM74HC368

National Semiconductor

MM54HC373/MM74HC373 TRI-STATE® Octal D-Type Latch

General Description

These high speed OCTAL D-TYPE LATCHES utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

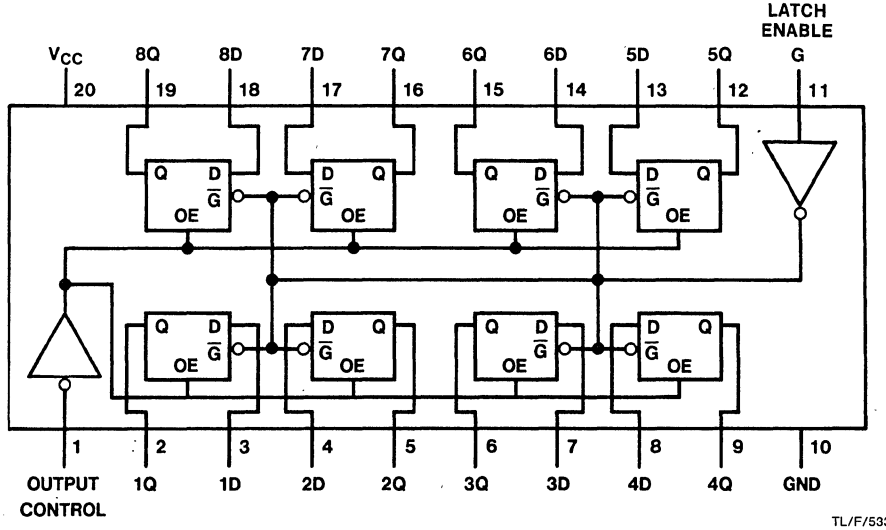
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 series)
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5335–1

MM54HC373/MM74HC373

54HC373 (J) 74HC373 (J,N)

Truth Table

Output Control	Latch Enable G	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	V_{IN}=V_{IH} or V_{IL}, OC=V_{IH} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	22	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	63	175	220	263	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	25	35	44	52	ns
		$C_L=150$ pF	4.5V	35	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	28	39	49	59	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V	5	25	31	38	ns
			4.5V	2	5	6	8	ns
			6.0V	2	5	6	8	ns
t_H	Minimum Hold Time		2.0V	20	50	60	75	ns
			4.5V	6	10	13	20	ns
			6.0V	6	10	13	20	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch)						
		OC = V_{CC}		30				pF
		OC = GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC374/MM74HC374
TRI-STATE® Octal D-Type Flip-Flop

General Description

These high speed Octal D-Type Flip-Flops utilize micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

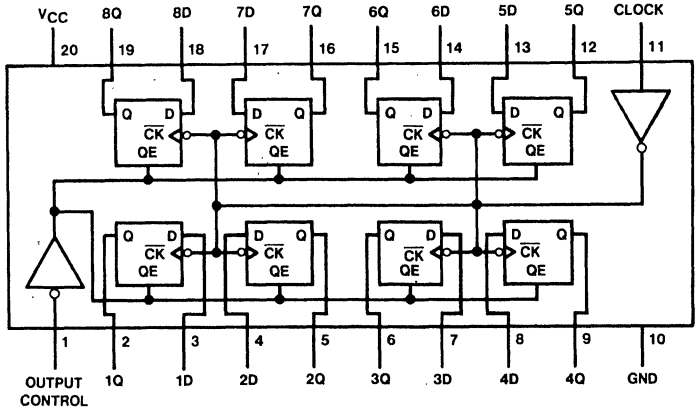
These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram



TL/F/5336–1

MM54HC374/MM74HC374

54HC374 (J) 74HC374 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	V_{IN}=V_{IH}, OC=V_{IH} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=$ kΩ $C_L=45$ pF	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=$ kΩ $C_L=5$ pF	17	25	ns
t_S	Minimum Set Up Time			20	ns
t_H	Minimum Hold Time			5	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	68	180	225	270	ns
		$C_L=150$ pF	2.0V	110	230	288	345	ns
		$C_L=50$ pF	4.5V	22	36	45	48	ns
		$C_L=150$ pF	4.5V	30	46	57	69	ns
		$C_L=50$ pF	6.0V	20	31	39	46	ns
		$C_L=150$ pF	6.0V	28	40	50	60	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	189	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		25	31	38	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop) OC=V_{CC}		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC390/MM74HC390 Dual 4-Bit Decade Counter
MM54HC393/MM74HC393 Dual 4-Bit Binary Counter

General Description

These counter circuits contain independent ripple carry counters and utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. The MM54HC390/MM74HC390 incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual bi-quinary, or various combinations up to a single divide-by-100 counter. The MM54HC393/M74HC393 contain two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each of the two 4-bit counters is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

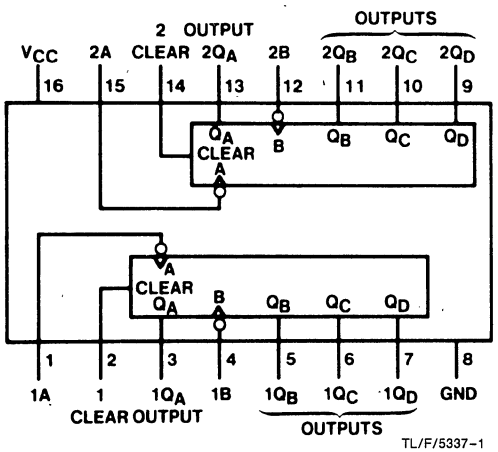
Each of the counters outputs can drive 10 low power Schottky TTL equivalent loads. These counters are functionaly as well as pin equivalent to the 54LS390/74LS390 and the 54LS393/74LS393, respectively. All inputs are protected from damage due to static discharge by diodes to V_C and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 13 ns (Ck to Q_A)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC series)
- Fanout of 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package

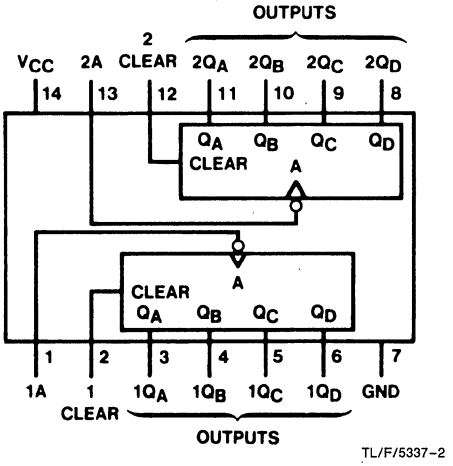


TL/F/5337–1

MM54HC390/MM74HC390

54HC390 (J) 74HC390 (J,N)

Dual-In-Line Package



TL/F/5337–2

MM54HC393/MM74HC393

54HC393 (J) 74HC393 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC390/MM74HC390

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency, Clock A or B		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A Output		12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A connected to Clock B)		32	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_B or Q_D		15	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_C		20	32	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Output		15	28	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	5	ns
t_W	Minimum Pulse Width, Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A		2.0V	45	120	150	180	ns
			4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A connected to Clock B)		2.0V	100	290	360	430	ns
			4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_B or Q_D		2.0V	50	130	160	195	ns
			4.5V	16	26	33	39	ns
			6.0V	13	22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_C		2.0V	60	185	230	280	ns
			4.5V	20	37	46	55	ns
			6.0V	17	32	40	48	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Q		2.0V	55	165	210	250	ns
			4.5V	17	33	41	49	ns
			6.0V	15	28	35	42	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		25	25	25	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per counter)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

AC Electrical Characteristics MM54HC393/MM74HC393

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_B		19	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C		23	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_D		27	50	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Q		15	28	ns
t_{REM}	Minimum Removal Time		−2	5	ns
t_W	Minimum Pulse Width Clear or Clock		10	16	ns

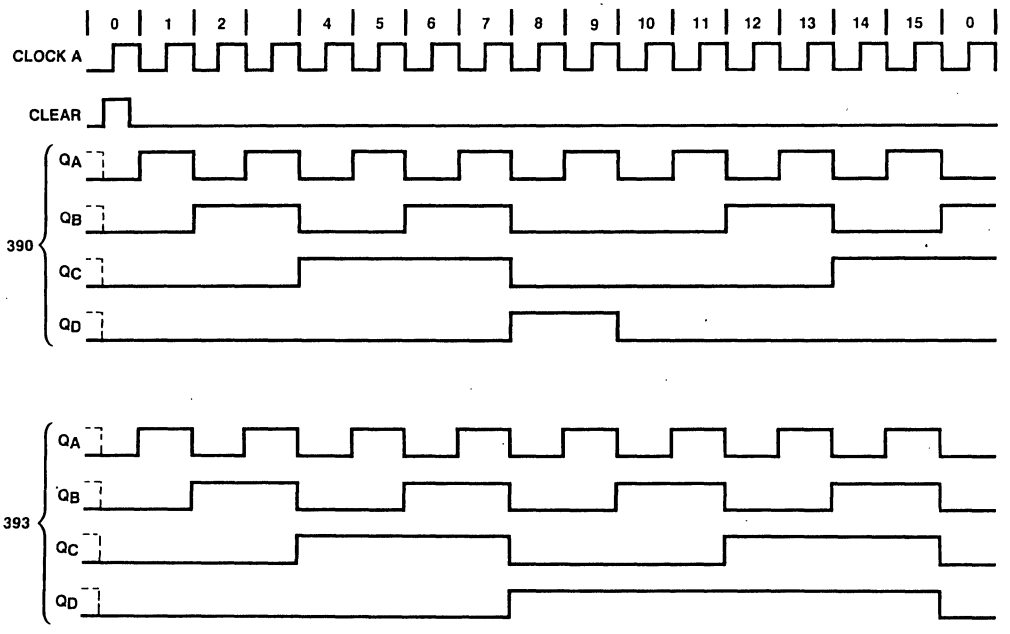
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_A		2.0V	45	120	150	180	ns
			4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_B		2.0V	68	190	240	285	ns
			4.5V	23	38	47	57	ns
			6.0V	20	32	40	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_C		2.0V	90	240	300	360	ns
			4.5V	30	48	60	72	ns
			6.0V	26	41	51	61	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_D		2.0V	100	290	360	430	ns
			4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t_{PHL}	Maximum Propagation Delay Clear to any Q		2.0V	54	165	210	250	ns
			4.5V	18	33	41	49	ns
			6.0V	15	28	35	42	ns
t_{REM}	Minimum Clear Removal Time		2.0V		25	25	25	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per counter)		42				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Timing Waveforms



TL/F/5337–3

National Semiconductor

MM54HC423/MM74HC423
Dual Retriggerable Monostable Multivibrator

General Description

The MM54/74HC423 high speed monostable multivibrators (one shots) utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC423 cannot be triggered from clear.

The 'HC423 is retriggerable. That is they may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

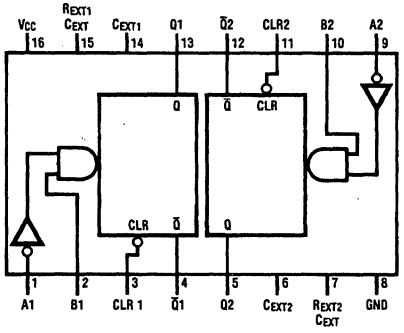
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})(C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs allow infinite rise and fall times on these inputs

Connection Diagram

Dual-In-Line Package

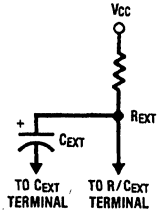


TL/F/5206–1

MM54HC423/MM74HC423

54HC423 (J) 74HC423 (J,N)

Timing Component



TL/F/5206–2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage(V_{CC})	−0.5V to +7.0V
DC Input Voltage(V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage(V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current(I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL}						V
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.96	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.46	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL}						V
		$\|I_{OUT}\| \leq 4$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	$V_{IN}=V_{CC}$ or GND	5.0V		0.5	0.5	0.5	μA
I_{IN}	Maximum Input Current (All other pins)	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (Standby)	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable)	$V_{IN}=V_{CC}$ or GND $R/C_{EXT}=0.5V_{CC}$	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C Ceramic "J" Package: −12mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

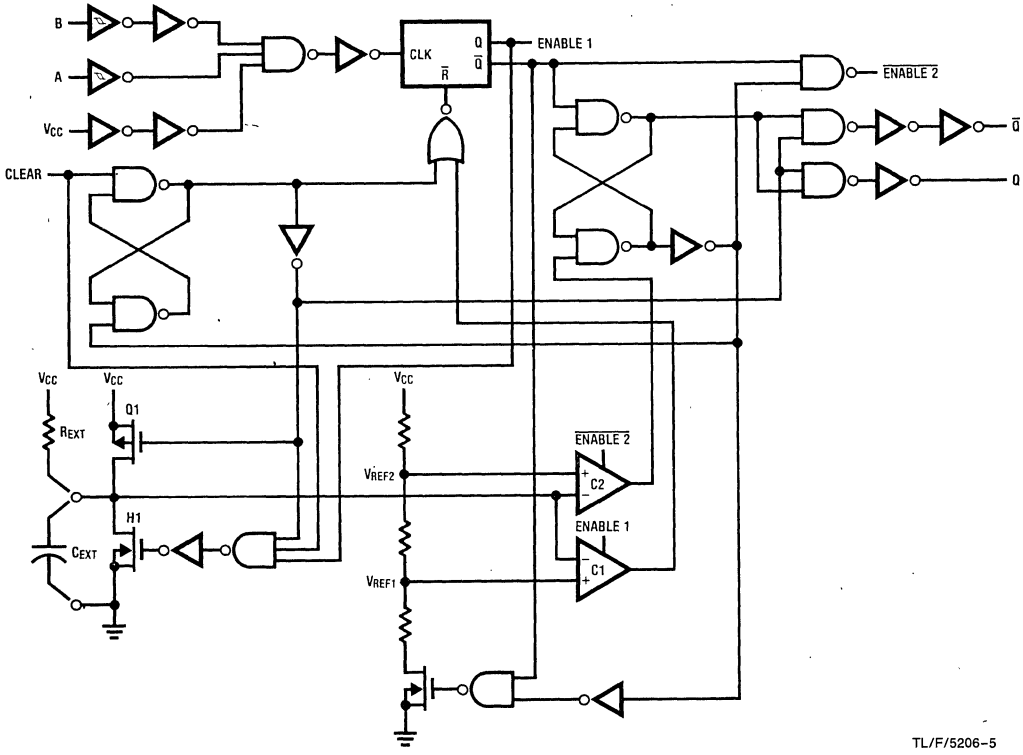
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay, A, B to Q		22	33	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns (Unless otherwise specified)

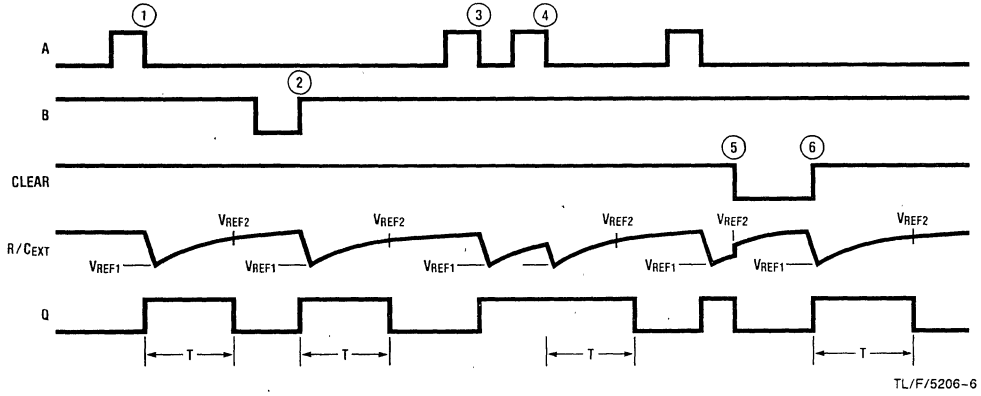
Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ	Guaranteed Limits		
t_{PLH}	Maximum Trigger Propagation Delay, A, B or Clear to Q			2.0V	77	169	194	210	ns
				4.5V	26	42	51	57	ns
				6.0V	21	32	39	44	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B or Clear to $\overline{Q}$			2.0V	88	197	229	250	ns
				4.5V	29	48	60	67	ns
				6.0V	24	38	46	51	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q			2.0V	54	114	132	143	ns
				4.5V	23	34	41	45	ns
				6.0V	19	28	33	36	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$			2.0V	56	116	135	147	ns
				4.5V	25	36	42	46	ns
				6.0V	20	29	34	37	ns
t_W	Minimum Pulse Width, A, B, Clear			2.0V	57	123	144	157	ns
				4.5V	17	30	37	42	ns
				6.0V	12	21	27	30	ns
t_{REM}	Minimum Clear Removal Time			2.0V	0	0	0	0	ns
				4.5V	0	0	0	0	ns
				6.0V	0	0	0	0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF		2.0V	1.5				μs
		$R_{EXT}=2$ kΩ		4.5V	450				ns
		$R_{EXT}=6$ kΩ ($V_{CC}=2V$)		6.0V	380				ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	4.5V	1	0.9			ms
			Max	4.5V	1	1.1			ms
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (Other Inputs)				6	10	10	10	pF

Logic Diagram



TL/F/5206–5

Theory of Operation



TL/F/5206–6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
⑤ RESET PULSE SHORTENING
⑥ CLEAR TRIGGER ('HC123, 'HC221 ONLY)

FIGURE 1.

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the one-shot is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the one-shot in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC}②.)

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC423 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

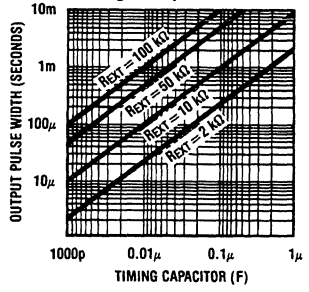
RETRIGGER OPERATION

The 'HC423 is retriggered if a valid trigger occurs ③ followed by another trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin or has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



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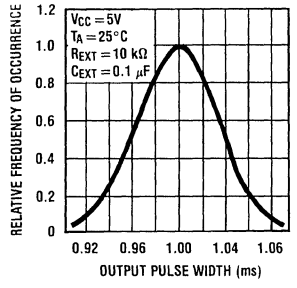
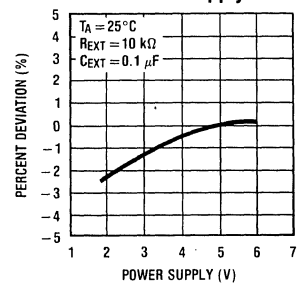
Typical Distribution of Output Pulse Width, Part to Part



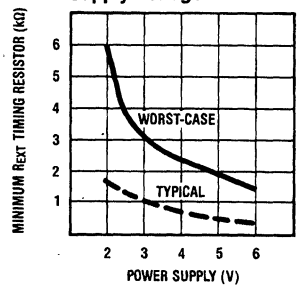
TL/F/5206–8

Typical 1ms Pulse Width Variation vs. Supply



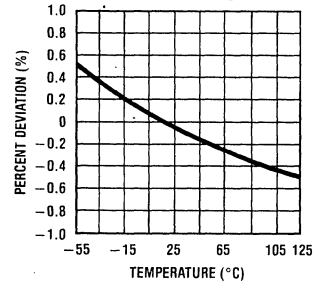
TL/F/5206–9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5206–10

Typical 1ms Pulse Width Variation vs. Temperature



TL/F/5206–11

National Semiconductor

MM54HC533/MM74HC533 TRI-STATE Octal D-Type Latch with Inverted Outputs

General Description

These high speed OCTAL D-TYPE LATCHES utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the inversion of the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

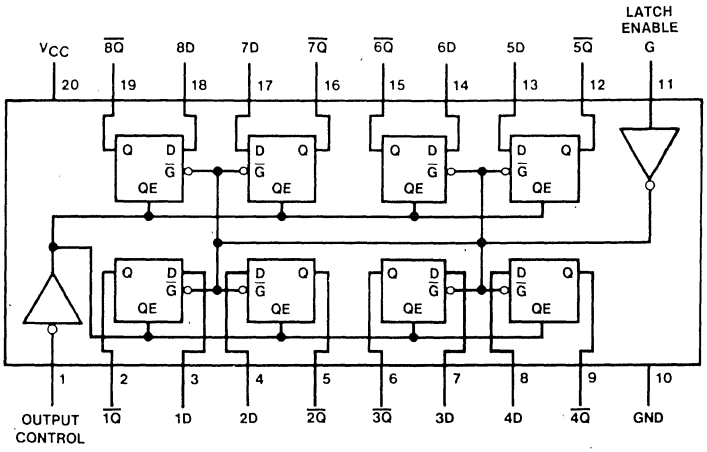
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA, maximum (74HC series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5339–1

MM54HC533/MM74HC533

54HC533 (J) 74HC533 (J,N)

Truth Table

Output Control	Latch Enable G	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	V_{IN}=V_{IH} or V_{IL}, OC=V_{IH} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0V-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	22	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$	$C_L=50$ pF	2.0V	63	175	220	263	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	25	35	44	52	ns
		$C_L=150$ pF	4.5V	35	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	28	39	49	59	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V	5	25	31	38	ns
			4.5V	2	5	6	8	ns
			6.0V	2	5	6	8	ns
t_H	Minimum Hold Time		2.0V	20	50	60	75	ns
			4.5V	6	10	13	20	ns
			6.0V	6	10	13	20	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch)						
		OC = V_{CC}		30				pF
		OC = Gnd		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC534/MM74HC534
TRI-STATE® Octal D-Type Flip-Flop with Inverted Outputs

General Description

These high speed Octal D-Type Flip-Flops utilize micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

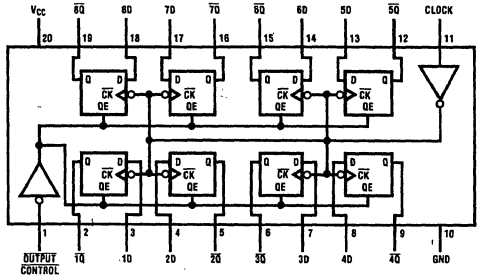
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5340–1

MM54HC534/MM74HC534

54HC534 (J) 74HC534 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level

X = Don't Care

↑ = Transition from low-to-high

Z = High impedance state

$\overline{Q}_0$ = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{IN}=V_{IH}$ or V_{IL}, OC=V_{IH} $V_{OUT}=V_{CC}$ or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to $\overline{Q}$	$C_L=45$ pF	23	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	21	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	25	ns
t_S	Minimum Set Up Time		10	20	ns
t_H	Minimum Hold Time		0	5	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	68	180	225	270	ns
		$C_L=150$ pF	2.0V	110	230	288	345	ns
		$C_L=50$ pF	4.5V	22	36	45	48	ns
		$C_L=150$ pF	4.5V	30	46	57	69	ns
		$C_L=50$ pF	6.0V	20	31	39	46	ns
		$C_L=150$ pF	6.0V	28	40	50	60	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	29	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	25	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	189	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop) OC = V_{CC}		30				pF
		OC = Gnd		50				
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC540/MM74HC540 Inverting Octal TRI-STATE® Buffer MM54HC541/MM74HC541 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. Both devices have a fanout of 15 LS-TTL equivalent inputs.

The MM54HC540/MM74HC540 is an inverting buffer and the MM54HC541/MM74HC541 is a non-inverting buffer. The TRI-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

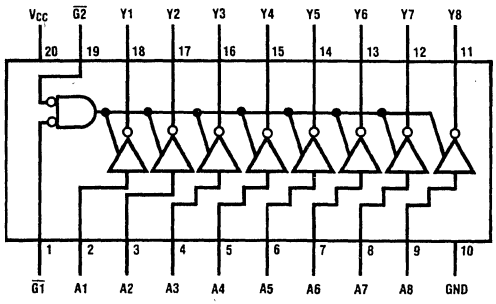
In order to enhance PC board layout, the 'HC540 and 'HC541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74HC series)
- Output current: 6 mA

Connection Diagram

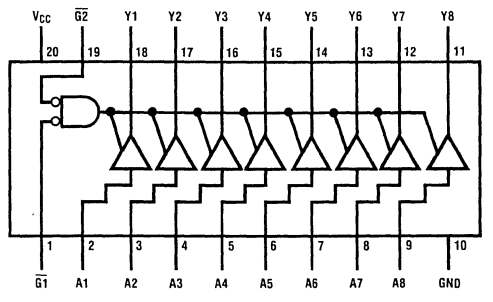
Dual-In-Line Package



TL/F/5341–1

MM54HC540/MM74HC540

54HC540 (J) 74HC540 (J,N)



TL/F/5341–2

MM54HC541/MM74HC541

54HC541 (J) 74HC541 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	V_{IN}=V_{IH} or V_{IL}, $\overline{G}$=V_{IH} V_{OUT}=V_{CC} or GNd	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC}=5V, T_A=25°C, t_r=t_f=6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	C_L=45 pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	C_L=45 pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L= kΩ C_L=45 pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L= kΩ C_L=5 pF	15	25	ns

AC Electrical Characteristics

V_{CC}=2.0V to 6.0V, C_L=50 pF, t_r=t_f=6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	C_L=50 pF	2.0V	55	100	126	149	ns
		C_L=150 pF	2.0V	83	150	190	224	ns
		C_L=50 pF	4.5V	12	20	25	30	ns
		C_L=150 pF	4.5V	22	30	38	45	ns
		C_L=50 pF	6.0V	11	17	21	25	ns
		C_L=150 pF	6.0V	18	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	C_L=50 pF	2.0V	58	115	145	171	ns
		C_L=150 pF	2.0V	83	165	208	246	ns
		C_L=50 pF	4.5V	14	23	29	34	ns
		C_L=150 pF	4.5V	17	33	42	49	ns
		C_L=50 pF	6.0V	11	20	25	29	ns
		C_L=150 pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L=1 kΩ						
		C_L=50 pF	2.0V	75	150	189	224	ns
		C_L=150 pF	2.0V	100	200	252	298	ns
		C_L=50 pF	4.5V	15	30	38	45	ns
		C_L=150 pF	4.5V	30	40	50	60	ns
		C_L=50 pF	6.0V	13	26	32	38	ns
		C_L=150 pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L=1 kΩ C_L=50 pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L=50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	OC=V_{CC}		10				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}, and the no load dynamic current consumption, I_S=C_{PD} V_{CC} f+I_{CC}.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC563/MM74HC563
TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed OCTAL D-TYPE LATCHES utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE (LE) input is high, the Q outputs will follow the inversion of the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

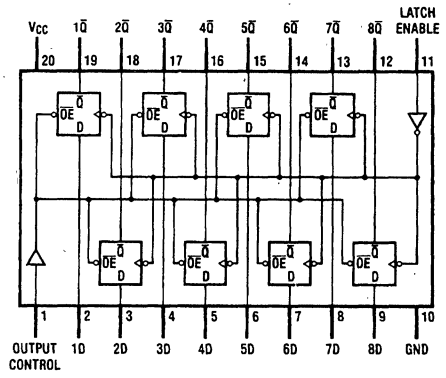
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5210–1

MM54HC563/MM74HC563

54HC563 (J) 74HC563 (J,N)

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CC})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND O_C=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA			8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	12	19	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set Up Time		10	15	ns
t_H	Minimum Hold Time		2	5	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=50$ pF	2.0V	45	110	138	165	ns
		$C_L=150$ pF	2.0V	58	150	188	225	ns
		$C_L=50$ pF	4.5V	14	22	28	33	ns
		$C_L=150$ pF	4.5V	21	30	38	40	ns
		$C_L=50$ pF	6.0V	12	19	24	29	ns
		$C_L=150$ pF	6.0V	19	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF	2.0V	46	115	143	173	ns
		$C_L=150$ pF	2.0V	60	155	194	233	ns
		$C_L=50$ pF	4.5V	14	23	29	35	ns
		$C_L=150$ pF	4.5V	21	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	19	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	55	140	175	210	ns
		$C_L=150$ pF	2.0V	67	180	225	270	ns
		$C_L=50$ pF	4.5V	15	28	35	42	ns
		$C_L=150$ pF	4.5V	24	36	45	54	ns
		$C_L=50$ pF	6.0V	14	24	30	36	ns
		$C_L=150$ pF	6.0V	22	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	40	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	12	21	27	32	ns
t_S	Minimum Set Up Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_H	Minimum Hold Time		2.0V		25	31	38	ns
			4.5V		5	6	7	ns
			6.0V		4	5	6	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Output Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	OE=V_{CC}		30				pF
		OE=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC564/MM74HC564
TRI-STATE® Octal D-Type Flip-Flop with Inverted Outputs

General Description

These octal D-type flip-flops utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

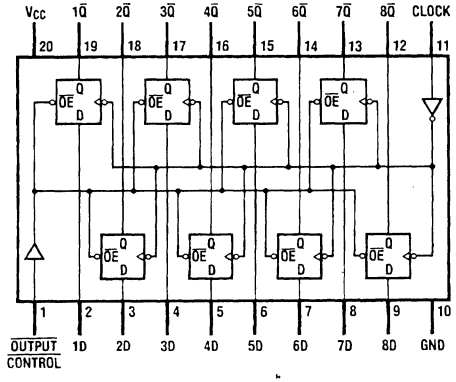
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5211–1

MM54HC564/MM74HC564

54HC564 (J) 74HC564 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High Impedance State
Q_0 = The level of the output before steady state Input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND O_C=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set-Up Time			20	ns
t_H	Minimum Hold Time			0	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF	2.0V	40	115	143	173	ns
		$C_L=150$ pF	2.0V	51	155	194	233	ns
		$C_L=50$ pF	4.5V	13	23	29	35	ns
		$C_L=150$ pF	4.5V	19	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	18	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	45	140	175	210	ns
		$C_L=150$ pF	2.0V	59	180	225	270	ns
		$C_L=50$ pF	4.5V	14	28	35	42	ns
		$C_L=150$ pF	4.5V	20	36	45	54	ns
		$C_L=50$ pF	6.0V	12	24	30	36	ns
		$C_L=150$ pF	6.0V	18	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	35	125	156	188	ns
			4.5V	12	25	31	38	ns
			6.0V	10	21	27	32	ns
t_S	Minimum Set-Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	8	16	20	24	ns
			6.0V◇	7	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	OC=VCC		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC573/MM74HC573
TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE(LE) input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

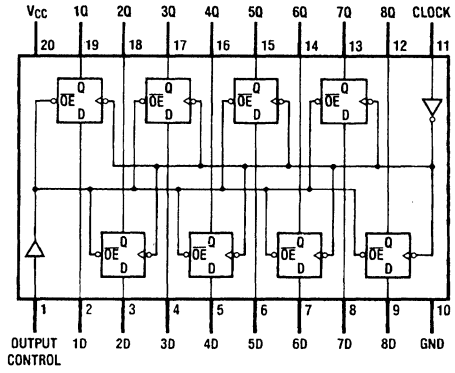
The 54HC/74HC logic family is speed, function and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5212–1

MM54HC573/MM74HC573

54HC573 (J) 74HC573 (J,N)

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

X = Don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND O_C=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	12	19	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set Up Time		10	15	ns
t_H	Minimum Hold Time		2	5	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to $\overline{Q}$	$C_L=50$ pF	2.0V	45	110	138	165	ns
		$C_L=150$ pF	2.0V	58	150	188	225	ns
		$C_L=50$ pF	4.5V	14	22	28	33	ns
		$C_L=150$ pF	4.5V	21	30	38	40	ns
		$C_L=50$ pF	6.0V	12	19	24	29	ns
		$C_L=150$ pF	6.0V	19	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF	2.0V	46	115	143	173	ns
		$C_L=150$ pF	2.0V	60	155	194	233	ns
		$C_L=50$ pF	4.5V	14	23	29	35	ns
		$C_L=150$ pF	4.5V	21	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	19	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	55	140	175	210	ns
		$C_L=150$ pF	2.0V	67	180	225	270	ns
		$C_L=50$ pF	4.5V	15	28	35	42	ns
		$C_L=150$ pF	4.5V	24	36	45	54	ns
		$C_L=50$ pF	6.0V	14	24	30	36	ns
		$C_L=150$ pF	6.0V	22	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	40	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	12	21	27	32	ns
t_S	Minimum Set Up Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_H	Minimum Hold Time		2.0V		25	31	38	ns
			4.5V		5	6	7	ns
			6.0V		4	5	6	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	OE = V_{CC}		30				pF
		OE = GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC574/MM74HC574
TRI-STATE® Octal D-Type Flip-Flop

General Description

These high speed octal D-type flip-flops utilize micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

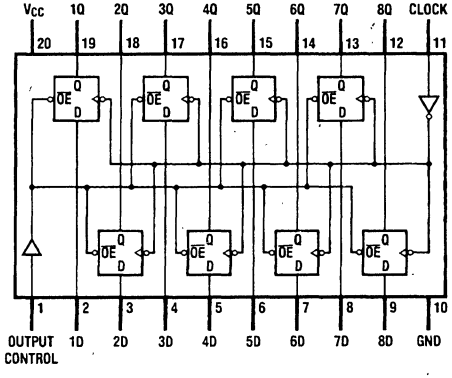
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



TOP VIEW

TL/F/5213–1

MM54HC574/MM74HC574

54HC574 (J) 74HC574 (J,N)

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND O_C=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set-Up Time			20	ns
t_H	Minimum Hold Time			0	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF	2.0V	40	115	143	173	ns
		$C_L=150$ pF	2.0V	51	155	194	233	ns
		$C_L=50$ pF	4.5V	13	23	29	35	ns
		$C_L=150$ pF	4.5V	19	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	18	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	45	140	175	210	ns
		$C_L=150$ pF	2.0V	59	180	225	270	ns
		$C_L=50$ pF	4.5V	14	28	35	42	ns
		$C_L=150$ pF	4.5V	20	36	45	54	ns
		$C_L=50$ pF	6.0V	12	24	30	36	ns
		$C_L=150$ pF	6.0V	18	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	35	125	156	188	ns
			4.5V	12	25	31	38	ns
			6.0V	10	21	27	32	ns
t_S	Minimum Set-Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Output Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	OC=VCC		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HC589/MM74HC589
8-Bit Shift Registers with Input Latches and TRI-STATE® Serial Output

General Description

This high speed shift register utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

The 'HC589 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and a Tri-State output to enable the wire-ORing of multiple devices on a serial bus.

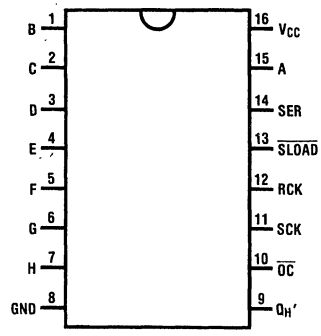
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- 8-Bit parallel storage register inputs
- Wide operating voltage range: 2V–6V
- Shift register has direct overriding load
- Guaranteed shift frequency . . . DC to 30 MHz
- Low quiescent current: 80 μA maximum (74HC Series)
- TRI-STATE output for 'Wire-OR'

Connection Diagram

Dual-In-Line Package



TL/F/5368–1

MM54HC589/MM74HC589

54HC589 (J) 74HC589 (J,N)

Truth Table

RCK	SCK	$\overline{SLOAD}$	$\overline{OC}$	Function
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	X	L	Serial output in high impedance state
X	↑	H	H	Shift register clocked $Q_M = Q_{n-1}$, Q_O = SER

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V		3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V		0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency for SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK to $Q_{H'}$			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From $\overline{SLOAD}$ to $Q_{H'}$			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to $Q_{H'}$	$\overline{SLOAD}$ = logic '0'	25	45	ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L=1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	25	ns
t_S	Minimum Set Up Time From RCK to SCK		10	20	ns
t_S	Minimum Set Up Time From SER to SCK		10	20	ns
t_S	Minimum Set Up Time From Inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		−3	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SLOAD}$		8	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

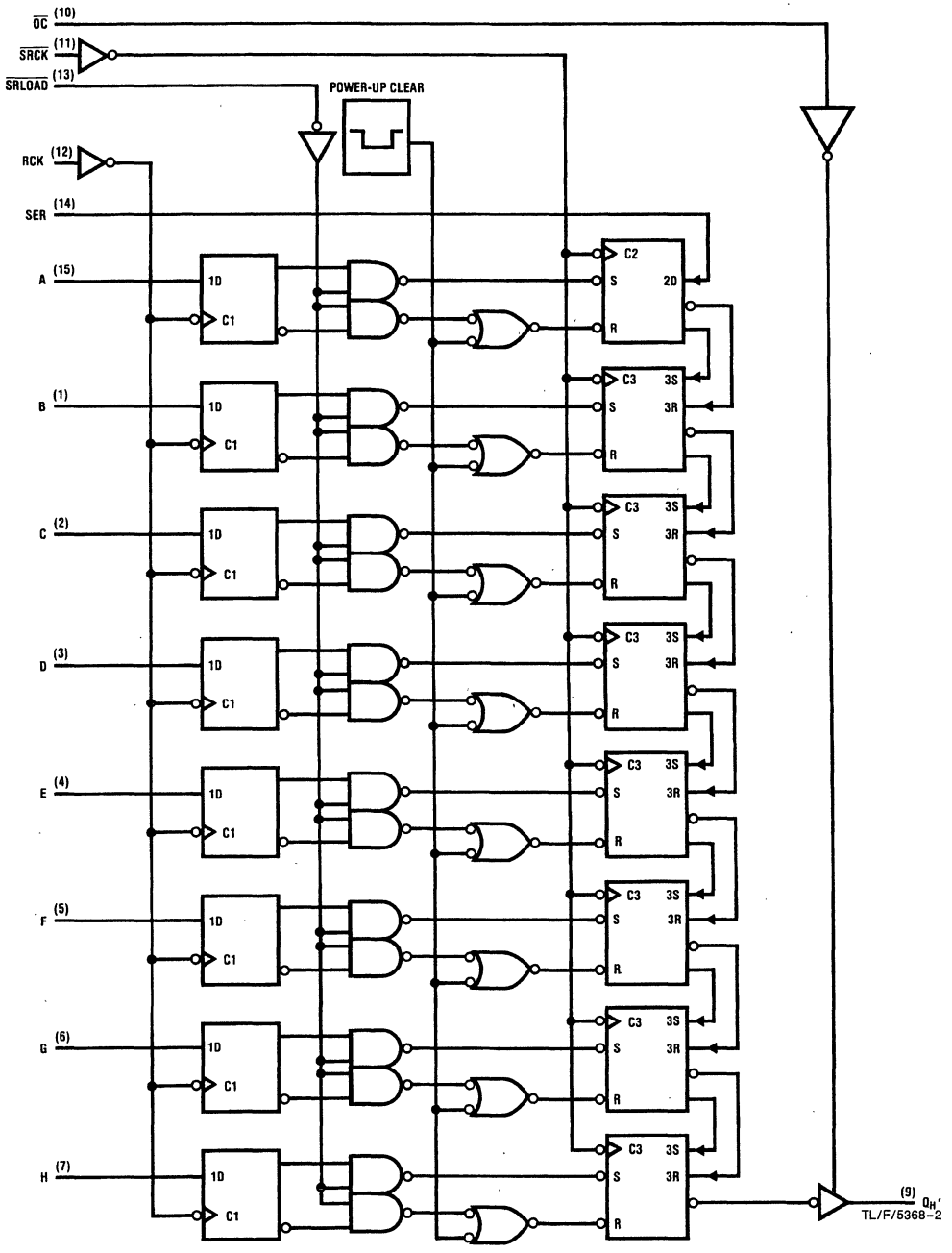
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency for SCK		2.0V		5	4	4	MHz
			4.5V		27	21	18	MHz
			6.0V		32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK to $Q_{H'}$		2.0V	62	175	220	266	ns
			4.5V	20	35	43	52	ns
			6.0V	18	30	37	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From $\overline{SLOAD}$ to $Q_{H'}$		2.0V	62	175	220	266	ns
			4.5V	20	35	43	52	ns
			6.0V	18	30	37	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to $Q_{H'}$	$\overline{SLOAD}$ = logic '0'	2.0V	120	250	312	375	ns
			4.5V	31	50	63	75	ns
			6.0V	28	43	53	65	ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L=1$ kΩ	2.0V	70	150	189	224	ns
			4.5V	22	30	38	45	ns
			6.0V	20	26	32	38	ns
t_{PHZ}, t_{PLZ}	Output Enable Time	$R_L=1$ kΩ	2.0V	70	150	189	224	ns
			4.5V	22	30	38	45	ns
			6.0V	20	26	32	38	ns
t_S	Minimum Set Up Time From RCK to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_S	Minimum Set Up Time From SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_S	Minimum Set Time From Inputs A thru H to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$, $\overline{SLOAD}$		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1500	1500	1500	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	12	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

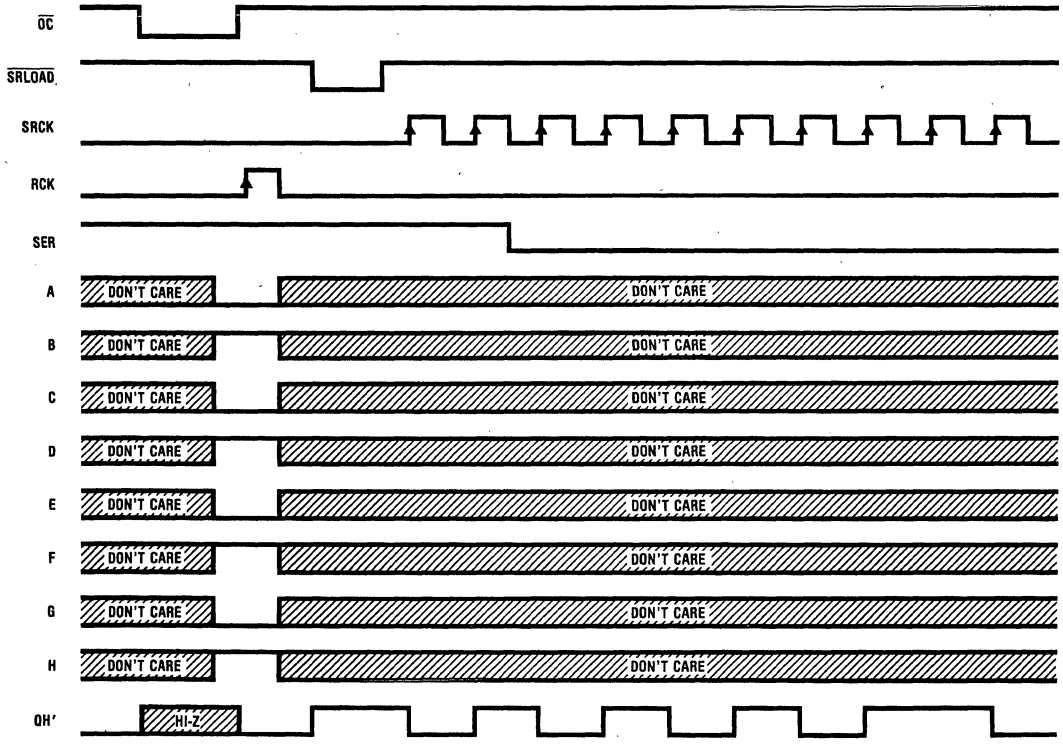
Functional Block Diagram (positive logic)

MM54HC589/MM74HC589



Logic Timing Diagram

MM54HC589/MM74HC589



TL/F/5368–3

National Semiconductor

PRELIMINARY

MM54HC595/MM74HC595
8-Bit Shift Registers with Output Latches

General Description

This high speed shift register utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 TRI-STATE® outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

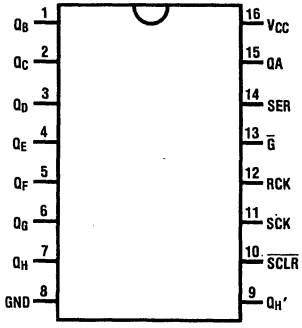
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 8-Bit Serial-In, Parallel-Out Shift Register With Storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift Register Has Direct Clear
- Guaranteed Shift Frequency: DC to 30 MHz

Connection Diagram

Dual-In-Line Package



TL/F/5342–1

MM54HC595/MM74HC595

54HC595 (J) 74HC595 (J,N)

Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{G}$	Function
X	X	X	1	Q_A thru Q_H = Tri-State
X	X	L	X	Shift Register cleared $Q_{H'} = 0$
X	↑	H	X	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER
↑	X	H	X	Contents of Shift Register transferred to output latches

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	$Q_{H'}$	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.2	5.48	5.34	5.2	V
	Q_A thru Q_H	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	$Q_{H'}$	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
	Q_A thru Q_H	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage	V_{OUT}=V_{CC} or GND Enable=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to $Q_{H'}$	$C_L=45$ pF	12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, RCK to Q_A thru Q_H	$C_L=45$ pF	18	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time From $\overline{G}$ to Q_A thru Q_H	$R_L=1$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time From $\overline{G}$ to Q_A thru Q_H	$R_L=$ kΩ $C_L=5$ pF	15	25	ns
t_S	Minimum Set Up Time From SER to SCK			20	ns
t_S	Minimum Set Up Time From $\overline{SCLR}$ to SCK			20	ns
t_S	Minimum Set Up Time From SCK to RCK (See Note 5)			40	ns
t_H	Minimum Hold Time From SER to SCK			0	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

Note 5: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

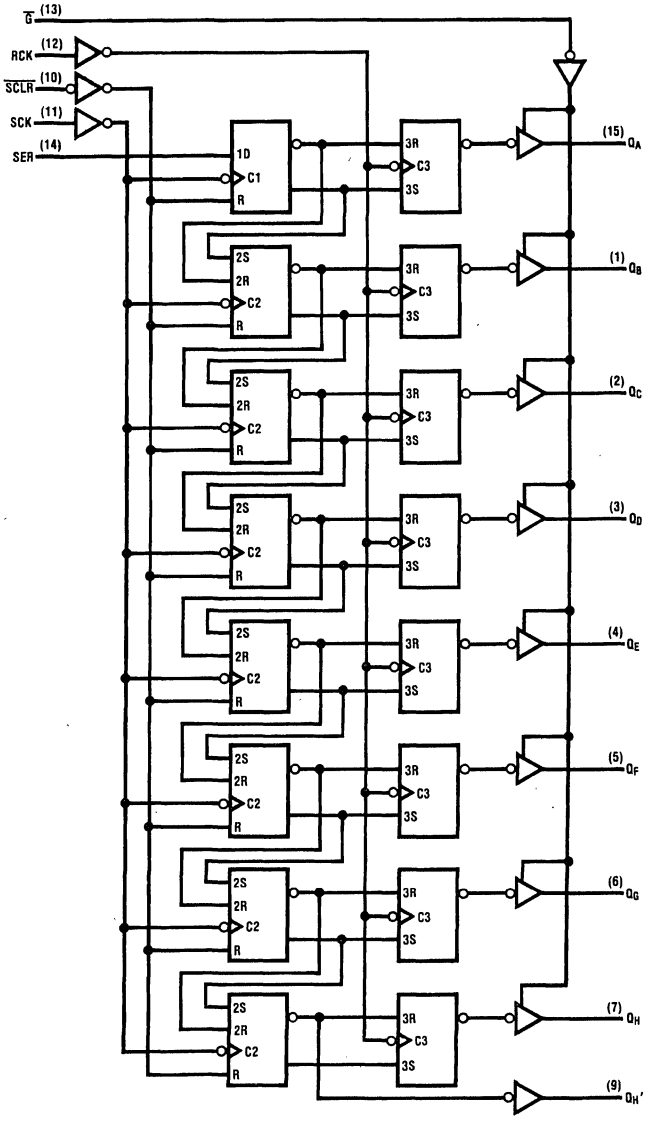
AC Electrical Characteristics V_{CC}=2.0–6.0V, C_L=50 pF, $t_r=t_f$=6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	C_L=50 pF	2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	50	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK to Q_H'	C_L=50 pF	2.0V	58	115	145	171	ns
		C_L=150 pF	2.0V	83	165	208	246	ns
		C_L=50 pF	4.5V	14	23	29	34	ns
		C_L=150 pF	4.5V	17	33	42	49	ns
		C_L=50 pF	6.0V	10	20	25	29	ns
		C_L=150 pF	6.0V	14	28	35	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to Q_A thru Q_H	C_L=50 pF	2.0V	70	150	188	225	ns
		C_L=150 pF	2.0V	105	200	225	250	ns
		C_L=50 pF	4.5V	21	30	38	45	ns
		C_L=150 pF	4.5V	28	40	50	60	ns
		C_L=50 pF	6.0V	18	26	33	39	ns
		C_L=150 pF	6.0V	26	34	43	51	ns
t_{PZH}, t_{PZL}	Maximum Output Enable From $\overline{G}$ to Q_A thru Q_H	R_L=1 kΩ						
		C_L=50 pF	2.0V	75	150	189	224	ns
		C_L=150 pF	2.0V	100	200	252	298	ns
		C_L=50 pF	4.5V	15	30	38	45	ns
		C_L=150 pF	4.5V	20	40	50	60	ns
		C_L=50 pF	6.0V	13	26	32	38	ns
		C_L=150 pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time From $\overline{G}$ to Q_A thru Q_H	R_L=1 kΩ	2.0V	75	150	189	224	ns
		C_L=50 pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_S	Minimum Set Up Time From SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Set Up Time From $\overline{SCLR}$ to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Set Up Time From SCK to RCK		2.0V		200	250	300	ns
			4.5V		40	50	60	ns
			6.0V		34	42	50	ns
t_H	Minimum Hold Time SER to SCK		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of SCK or RCLK		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	22	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 6)	$\overline{G}=V_{CC}$		90				pF
		G=GND		150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 7: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Logic Diagram (positive logic)



TL/F/5342–3

'HC595

PRELIMINARY

National Semiconductor

MM54HC597/MM74HC597
8-Bit Shift Registers with Input Latches

General Description

This high speed shift register utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The 'HC597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs

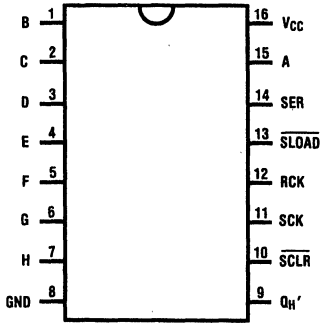
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- 8-Bit Parallel Storage Register Inputs
- Wide operating voltage range: 2V–6V
- Shift Register has Direct Overriding Load and Clear
- Guaranteed Shift Frequency . . . DC to 30 MHz
- Low quiescent current: 80 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5343–1

MM54HC597/MM74HC597

54HC597 (J) 74HC597 (J,N)

Truth Table

RCK	SCK	$\overline{SLOAD}$	$\overline{SCLR}$	Function
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked $Q_n = Q_{n-1}$, Q_0 = SER

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency for SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK to $Q_{H'}$		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From $\overline{SLOAD}$ to $Q_{H'}$		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to $Q_{H'}$	$\overline{SLOAD}$ = logic'0'	25	45	ns
t_{PHL}	Maximum Propagation Delay From $\overline{SCLR}$ to $Q_{H'}$		20	30	ns
t_{REM}	Minimum Removal Time, $\overline{SCLR}$ to SCK		10	20	ns
t_S	Minimum Set Up Time From RCK to SCK		30	40	ns
t_S	Minimum Set Up Time From SER to SCK		10	20	ns
t_S	Minimum Set Up Time From Inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		−2	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$ $\overline{SLOAD}$		10	16	ns

AC Electrical Characteristics

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency for SCK		2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	50	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From SCK to $Q_{H'}$		2.0V	62	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From $\overline{SLOAD}$ to $Q_{H'}$		2.0V	65	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From RCK to $Q_{H'}$	$\overline{SLOAD}$ = Logic '0'	2.0V	120	250	312	375	ns
			4.5V	30	50	65	75	ns
			6.0V	28	43	53	65	ns
t_{PHL}	Maximum Propagation Delay From $\overline{SCLR}$ to $Q_{H'}$		2.0V	66	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{REM}	Minimum Removal Time $\overline{SCLR}$ to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Set Up Time From RCK to SCK		2.0V		200	250	300	ns
			4.5V		40	50	60	ns
			6.0V		34	42	50	ns
t_S	Minimum Set Up Time From SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

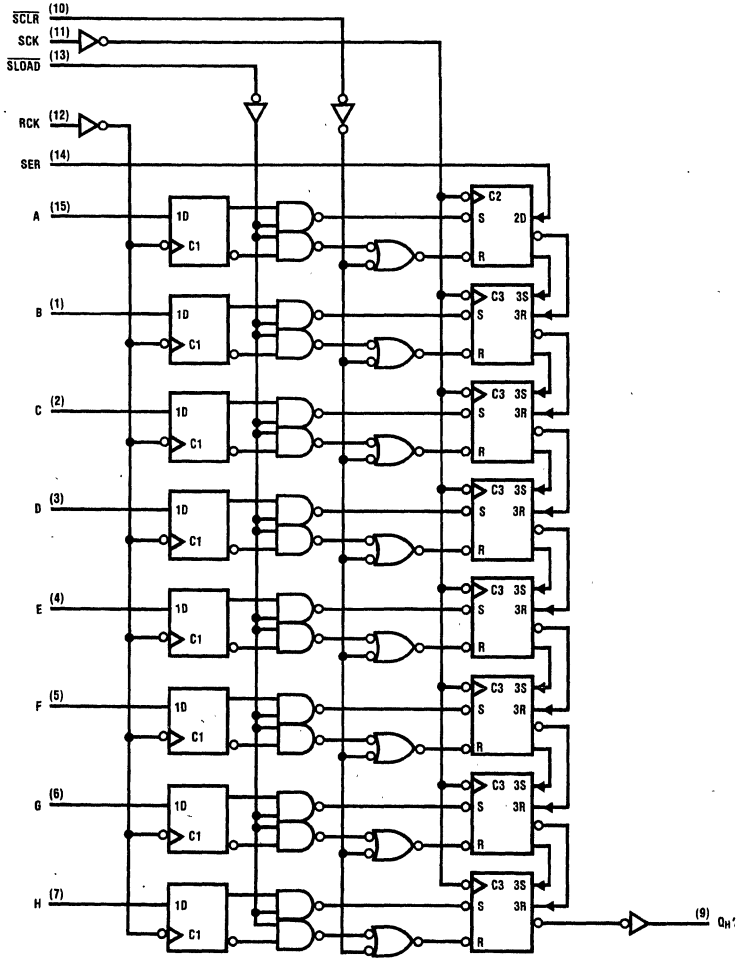
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_S	Minimum Set Up Time From Inputs A thru H to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$, $\overline{SLOAD}$		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	8	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Functional Block Diagram (Positive logic)

'HC597



TL/F/5343–2

National Semiconductor

MM54HC640/MM74HC640 Inverting Octal TRI-STATE® Transceiver MM54HC643/MM74HC643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional buffers utilize micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

Each device has an active enable $\overline{G}$ and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC640/MM74HC640 transfers inverted data from one bus to other and the MM54HC643/MM74HC643 transfers inverted data from the A bus to the B bus and true data from the B bus to the A bus.

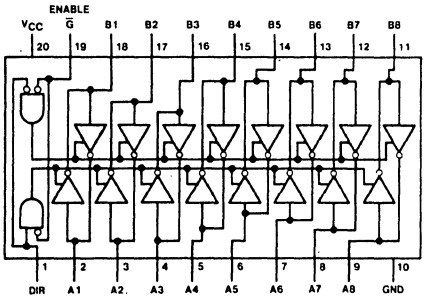
These devices can drive up to 15 LS-TTL Loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74 HC)
- Tri-State outputs for connection to bus oriented systems
- High Output Drive: 6 mA (min)

Connection Diagrams

Dual-In-Line Package

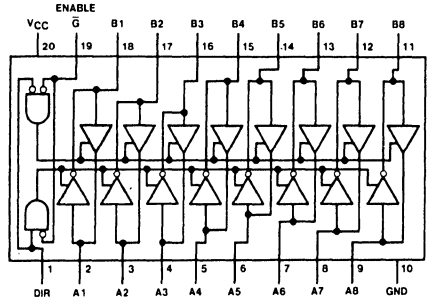


TL/F/5344–1

MM54HC640/MM74HC640

54HC640 (J) 74HC640 (J,N)

Dual-In-Line Package



TL/F/5344–2

MM54HC643/MM74HC643

54HC643 (J) 74HC643 (J,N)

Truth Table

Control Inputs		Operation	
$\overline{G}$	DIR	640	643
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	$V_{OUT}=V_{CC}$ or GND Enable=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	13	17	ns
t_{PHZ}, t_{PLZ}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	33	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	32	42	ns

AC Electrical Characteristics

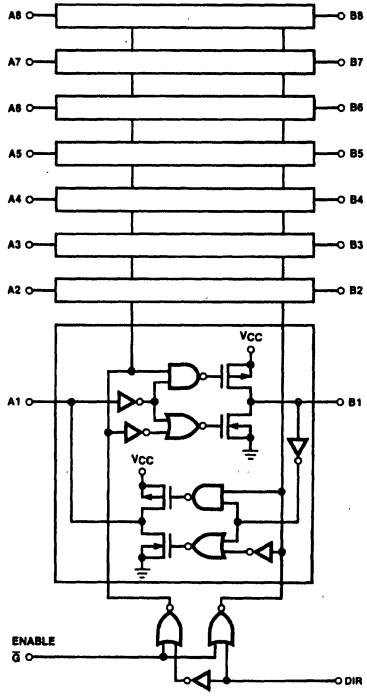
$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	29	72	88	96	ns
		$C_L=150$ pF	2.0V	38	96	116	128	ns
		$C_L=50$ pF	4.5V	14	18	22	24	ns
		$C_L=150$ pF	4.5V	18	24	29	32	ns
		$C_L=50$ pF	6.0V	14	18	22	24	ns
		$C_L=150$ pF	6.0V	18	24	29	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	70	184	224	240	ns
		$C_L=150$ pF	2.0V	80	216	260	284	ns
		$C_L=50$ pF	4.5V	35	46	56	60	ns
		$C_L=150$ pF	4.5V	41	54	65	71	ns
		$C_L=50$ pF	6.0V	31	41	50	54	ns
		$C_L=150$ pF	6.0V	36	47	57	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	47	172	208	224	ns
			4.5V	33	43	52	56	ns
			6.0V	31	41	50	54	ns
t_{THL}, t_{TLH}	Output Rise and Fall Time		2.0V	20	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	643 B-A $\overline{G}=V_{IL}$		100				pF
		640(643 A-B) $\overline{G}=V_{IL}$		120				pF
		643 $\overline{G}=V_{IH}$		12				pF
		640(643 A-B) $\overline{G}=V_{IH}$		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

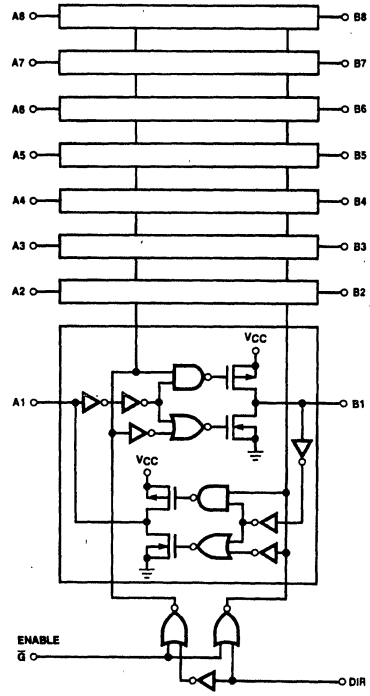
Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagrams



TL/F/5344–3

'HC640



TL/F/5344–4

'HC643

National Semiconductor

MM54HC646/MM74HC646 Non-Inverting Octal Bus Transceiver/Registers MM54HC648/MM74HC648 Inverting Octal Bus Transceiver/Registers

General Description

These transceivers utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and contain two sets of TRI-STATE® outputs, two sets of D-type flip-flops, and control circuitry designed for high speed multiplexed transmission of data.

Six control inputs enable this device to be used as a latched transceiver, unlatched transceiver, or a combination of both. As a latched transceiver, data from one bus is stored for later retrieval by the other bus. Alternately real time bus data (unlatched) may be directly transferred from one bus to another.

Circuit operation is determined by the G, DIR, CAB, CBA, SAB, SBA control inputs. The enable input, G, controls whether any bus outputs are enabled. The direction control, DIR, determines which bus is enabled, and hence the direction data flows: The SAB, SBA inputs control whether the latched data (stored in D type flip flops), or the bus data (from other bus input pins) is transferred. Each set of flip-flops has its own clock CAB, and CBA, for storing data. Data is latched on the rising edge of the clock.

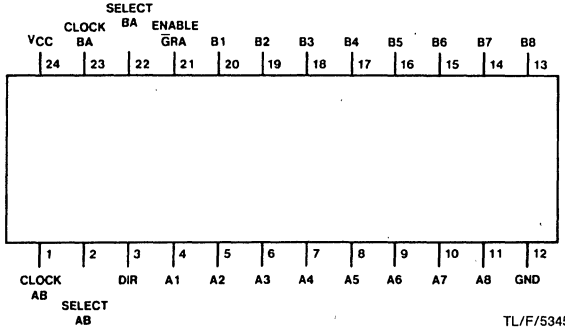
Each output can drive up to 15 low power Schottky TTL loads. These devices are functionally and pin compatible to their LS-TTL counterparts. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

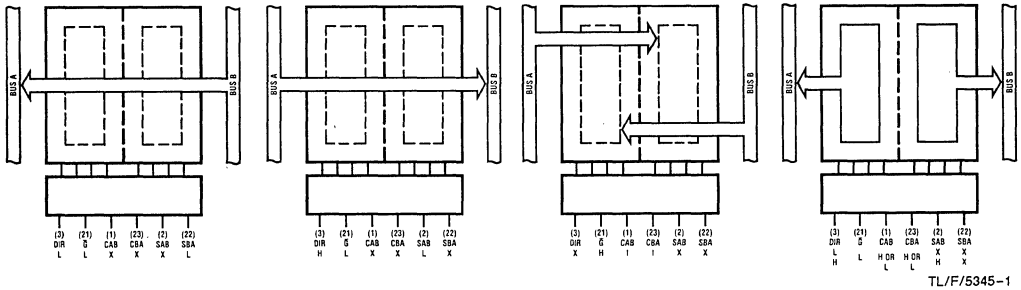
- Typical propagation delay: 14 ns
- TRI-STATE outputs
- Bi-directional communication
- Wide power supply range: 2–6V
- Low quiescent supply current: 160 μA maximum (74HC)
- High output current: 6 mA (74HC)

Connection Diagrams

Dual-In-Line Package



TL/F/5345–2



TL/F/5345–1

Real-Time Transfer Bus B to Bus A | **Real-Time Transfer Bus A to Bus B** | **Storage from A, B, or A and B** | **Transfer Stored Data to A or B**

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.96	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.46	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

Truth Table

Inputs						Data I/O		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	646	648
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Input	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

H = High Level L = Low Level X = Irrelevant ↑ = low-to-high level transition

The data output functions i.e., data at the bus pins may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled.

The data output functions i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

AC Electrical Characteristics MM54HC646/MM74HC646

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=45$ pF	14	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=45$ pF	31	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=45$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	$C_L=45$ pF	35	50	ns
t_{PZH}, t_{PZL}	Maximum Enable Time $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=45$ pF	18	33	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time, $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=5$ pF	17	30	ns

AC Electrical Characteristics MM54HC646/MM74HC646

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=50$ pF	2.0V	60	180	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	18	26	31	39	ns
		$C_L=150$ pF	6.0V	22	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=50$ pF	2.0V	110	220	275	330	ns
		$C_L=150$ pF	2.0V	150	270	338	405	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	40	54	68	81	ns
		$C_L=50$ pF	6.0V	28	38	47	57	ns
		$C_L=150$ pF	6.0V	34	47	59	71	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=50$ pF	2.0V	180	290	363	435	ns
		$C_L=150$ pF	2.0V	210	340	425	510	ns
		$C_L=50$ pF	4.5V	39	58	72	87	ns
		$C_L=150$ pF	4.5V	47	68	85	102	ns
		$C_L=50$ pF	6.0V	34	50	63	75	ns
		$C_L=150$ pF	6.0V	39	58	72	87	ns

AC Electrical Characteristics MM54HC646/MM74HC646 (Continued)

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	C_L = 50 pF	2.0V	180	290	363	435	ns
		C_L = 150 pF	2.0V	210	340	425	510	ns
		C_L = 50 pF	4.5V	39	58	72	87	ns
		C_L = 150 pF	4.5V	47	68	85	102	ns
		C_L = 50 pF	6.0V	34	50	63	75	ns
		C_L = 150 pF	6.0V	39	58	72	87	ns
t_{PZH}, t_{PZH}	Maximum Output Enable Time, $\overline{G}$ Input or DIR to A or B Output	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	80	175	219	263	ns
		C_L = 150 pF	2.0V	120	225	281	338	ns
		C_L = 50 pF	4.5V	23	35	44	53	ns
		C_L = 150 pF	4.5V	31	45	56	68	ns
		C_L = 50 pF	6.0V	21	30	37	45	ns
		C_L = 150 pF	6.0V	27	38	48	57	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, $\overline{G}$ Input to A or B Output	R_L = 1 kΩ	2.0V	85	175	219	263	ns
		C_L = 50 pF	4.5V	23	35	44	53	ns
			6.0V	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Clock		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Input Capacitance			15	20	20	20	pF

AC Electrical Characteristics MM54HC648/MM74HC648

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		44	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=50$ pF	14	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=50$ pF	31	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=50$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	$C_L=50$ pF	35	50	ns
t_{PZH}, t_{PZL}	Maximum Enable Time $\overline{G}$ Input to A or B Output	$R_L=1$ kΩ $C_L=45$ pF	18	33	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time, $\overline{G}$ Input to A or B Output	$R_L=1$ kΩ $C_L=5$ pF	17	30	ns

AC Electrical Characteristics MM54HC648/MM74HC648

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=50$ pF	2.0V	60	180	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	18	26	31	39	ns
		$C_L=150$ pF	6.0V	22	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=50$ pF	2.0V	110	220	275	330	ns
		$C_L=150$ pF	2.0V	150	270	338	405	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	40	54	68	81	ns
		$C_L=50$ pF	6.0V	28	38	47	57	ns
		$C_L=150$ pF	6.0V	34	47	59	71	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=50$ pF	2.0V	180	290	363	435	ns
		$C_L=150$ pF	2.0V	210	340	425	510	ns
		$C_L=50$ pF	4.5V	39	58	72	87	ns
		$C_L=150$ pF	4.5V	47	68	85	102	ns
		$C_L=50$ pF	6.0V	34	50	63	75	ns
		$C_L=150$ pF	6.0V	39	58	72	87	ns

AC Electrical Characteristics MM54HC648/MM74HC648 (Continued)

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	C_L = 50 pF	2.0V	180	290	363	435	ns
		C_L = 150 pF	2.0V	210	340	425	510	ns
		C_L = 50 pF	4.5V	39	58	72	87	ns
		C_L = 150 pF	4.5V	47	68	85	102	ns
		C_L = 50 pF	6.0V	34	50	63	75	ns
		C_L = 150 pF	6.0V	39	58	72	87	ns
t_{PZL}, t_{PZL}	Maximum Output Enable Time, $\overline{G}$ Input or DIR to A or B Output	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	80	175	219	263	ns
		C_L = 150 pF	2.0V	120	225	281	338	ns
		C_L = 50 pF	4.5V	23	35	44	53	ns
		C_L = 150 pF	4.5V	31	45	56	68	ns
		C_L = 50 pF	6.0V	21	30	37	45	ns
		C_L = 150 pF	6.0V	27	38	48	57	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, $\overline{G}$ Input to A or B Output	R_L = 1 kΩ, C_L = 50 pF	2.0V	85	175	219	263	ns
			4.5V	23	35	44	53	ns
			6.0V	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Clock		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC688/MM74HC688
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to compare bit for bit two 8-bit words and indicates whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

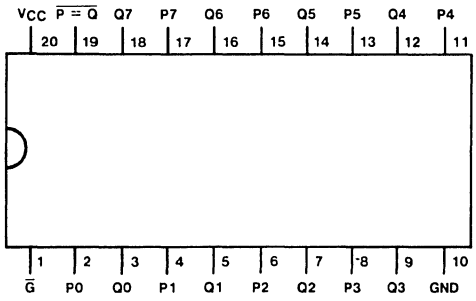
The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 54LS688/74LS688. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA (74 series)
- Large output current: 4 mA (74 series)

Connection and Logic Diagrams

Dual-In-Line Package



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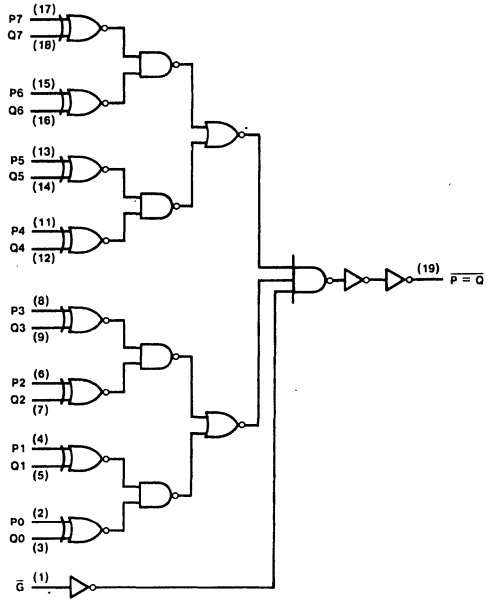
MM54HC688/MM74HC688

54HC688 (J) 74HC688 (J,N)



TL/F/5018–2

Truth Table

Inputs		
Data P,Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

4

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any P or Q to Output		21	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to any Output		14	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	175	220	263	ns
			4.5V	22	35	44	53	ns
			6.0V	19	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	120	150	180	ns
			4.5V	15	24	30	36	ns
			6.0V	13	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			45				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM74HC942 300 Baud Modem

General Description

The MM74HC942 is a full duplex low speed modem. It provides a 300 baud bidirectional series interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC942 utilizes microCMOS™ Technology, 2 layers of polysilicon and 1 layer of metal P-well CMOS. Switched capacitor techniques are used to perform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600 Ω phone line. They can perform two to four wire conversion and drive the line at 0 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

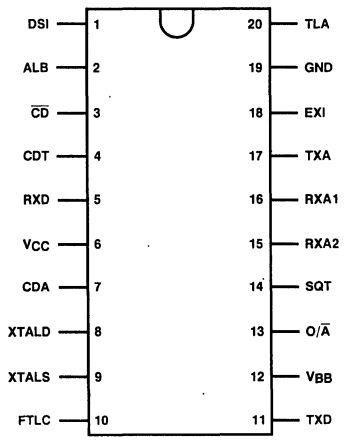
- Drives 600Ω at 0 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- ±5V supplies
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signalling systems
- Remote process control

Connection Diagram

Dual-In-Line Package



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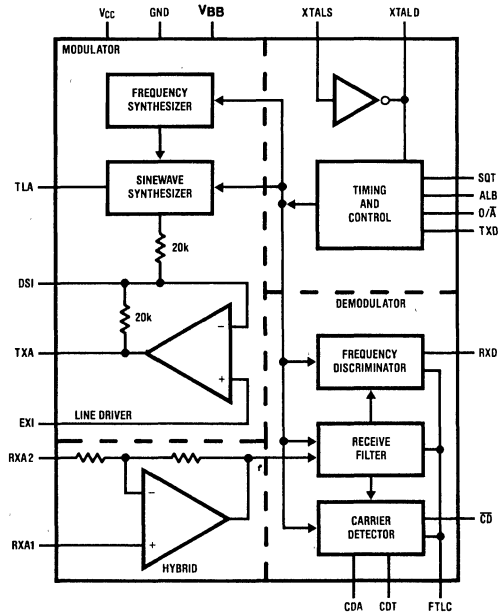
MM74HC942

74HC942 (J,N)

Block Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
Supply Voltage (V_{BB})	+0.5 to −7.0V
DC Input Voltage (V_{IN})	V_{BB} −1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	V_{BB} −0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
Supply Voltage(V_{BB})	−4.5	−5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A) MM74HC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics

Symbol	Parameter	Conditions	T = 25°C	74HC T = −40 to 85°C		Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	V_{CC}	V_{CC} −0.1 3.98	V_{CC} −0.1 3.7	V V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V		0.1 0.26	0.1 0.4	V V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC}, V_{IL} = GND ALB or SQT = GND Transmit Level = −9 dBm	8.0			mA
I_{CC}	Power Down Supply Current	ALB = SQT = V_{CC} V_{IH} = V_{CC}, V_{IL} = GND			250	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

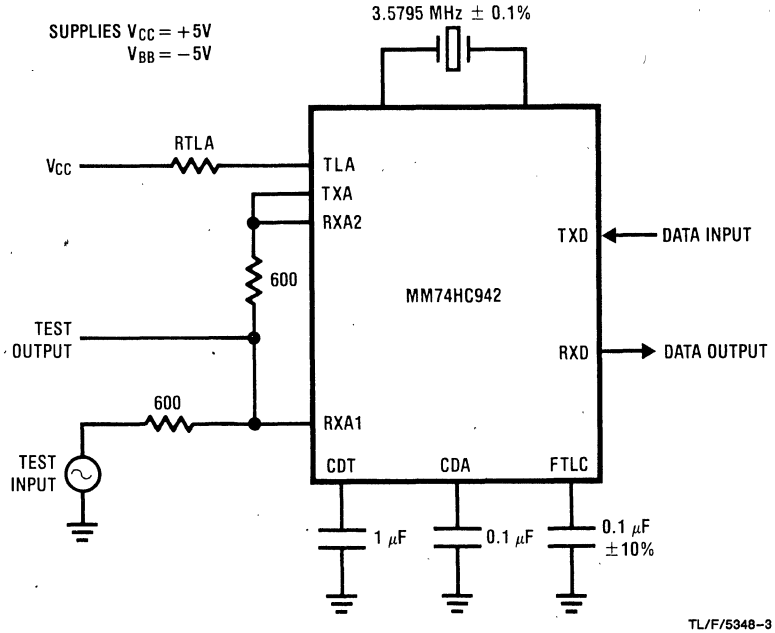
*The demodulator specifications apply to the MM74HC942 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC942 modulator.

AC Electrical Characteristics

Unless otherwise specified all specifications apply to the MM74HC942 over the range −40°C to +85°C using a V_{CC} = +5V ±10%, a V_{BB} = −5V ±10% and a 3.579MHz ±0.1% crystal.*

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMITTER						
F_{CE}	Carrier Frequency Error				4	Hz
	Power Output	V_{CC}=5.0V R_{TLA} = 0 R_L=1.2 kΩ R_{TLA} = ∞		0 −12		dBm dBm
	2nd Harmonic Energy			−56		dBm
RECEIVE FILTER AND HYBRID						
	Hybrid Input Impedance (Pins 15 and 16)		50			kΩ
	FTLC Output Impedance		10		50	kΩ
	Adjacent Channel Rejection	RXA2=GND TXA=GND or V_{CC} Input to RXA1	60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)						
	Carrier Amplitude		−48		−12	dBm
	Dynamic Range			36		dB
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud		100		μS
	Bit Bias			5		%
	Carrier Detect Trip Points	CDA=1.2V Off to On On to Off		−44 −47		dBm dBm

AC Specification Circuit



Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data outpin pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system, XTALD can be driven.
9	XTALS	Crystal Sense: Refer to pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receive filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	V_{BB}	Negative Supply: The recommended supply is −5V.
13	O/$\overline{A}$	Originate/$\overline{Answer}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded.
19	GND	Ground: This defines the chip 0V.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC942 uses frequency shift keying (FSK) of an audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC942 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC942 is capable of transmitting and receiving data simultaneously.

The tone allocation by the MM74HC942 and other Bell 103 compatible modems is shown in Table I. The terms "originate" and "answer" which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

TABLE I BELL 103 ALLOCATION

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switched capacitor nine pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60 Hz, a common noise component.

The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques. The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency produces one of four tones depending on the O/$\overline{A}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter. The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

TRANSMIT LEVEL ADJUSTMENT

The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source impedances.

The transmit level is programmable by placing a resistor from TLA to VCC. With a 5.5k resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the MM74HC942 will interface to most telephones. This arrangement is called the "permissive arrangement". The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

SNR can be maximized by adjusting the transmit level until the level at the exchange reaches −12 dBm. This must be done with the cooperation of the telephone company. The programming resistor used is specific for a given installation and is often included in the telephone jack at the installation. The modem is thus programmable and can be used with any jack correctly wired. This arrangement is called the universal registered jack arrangement and is possible with the MM74HC942. The values of resistors required to program the MM74HC942 follow the most common code in use; the universal service order code. The required resistors are given in Table II.

TABLE II Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ohms)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490
4	−8	3,610
5	−7	2,520
6	−6	1,780
7	−5	1,240
8	−4	866
9	−3	562
10	−2	336
11	−1	150
12	0	0

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used;

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$T_{\overline{CD}L} \cong 6.4 \times C_{CDT}$ for $\overline{CD}$ going low

$T_{\overline{CD}H} \cong 0.54 \times C_{CDT}$ for $\overline{CD}$ going high

Where $T_{\overline{CD}L}$ & $T_{\overline{CD}H}$ are in seconds, and C_{CDT} is in μF.

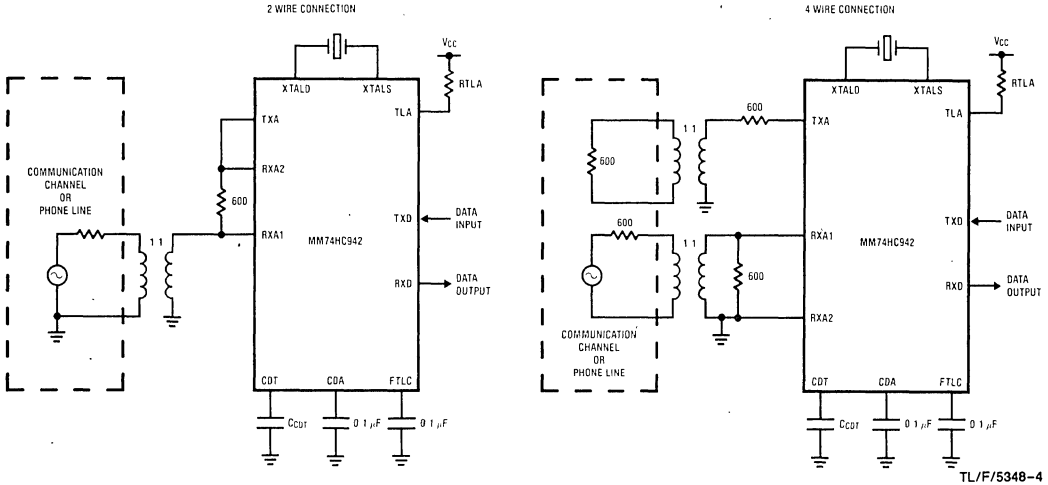
Applications Information (Continued)

DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC942 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

Interface Circuits for MM74HC942 300 Baud Modem



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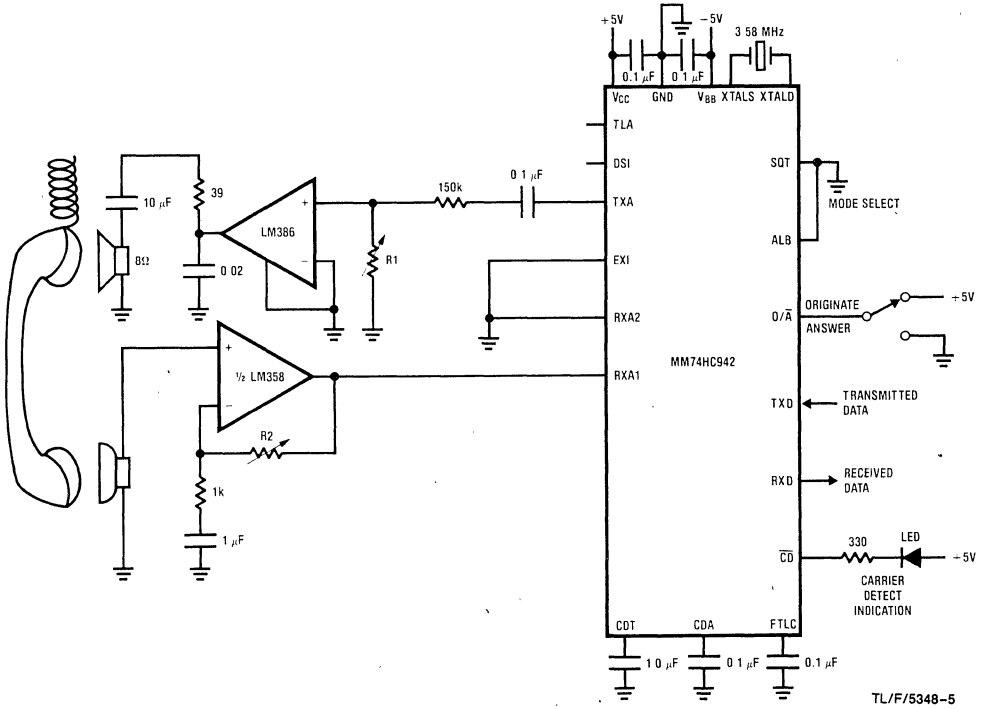
C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.

Complete Acoustically Coupled 300 Baud Modem



TL/F/5348–5

Note: The efficiency of the acoustic coupling will set the valves of R1 and R2.

National Semiconductor

PRELIMINARY

MM74HC943 300 Baud Modem

General Description

The MM74HC943 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC943 utilizes microCMOS™ Technology, 2 layers of polysilicon and 1 layer metal P-well CMOS. Switched capacitor techniques are used to peform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600Ω phone line. They can perform two to four wire conversion and drive the line at −9 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

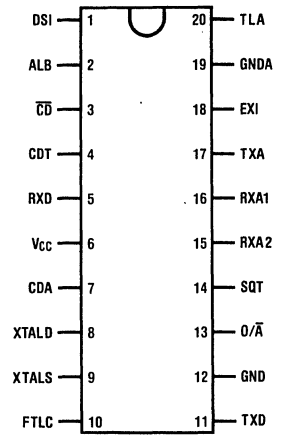
- 5V supply
- Drives 600Ω at −9 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signaling systems
- Remote process control

Connection Diagram

Dual-In-Line Package

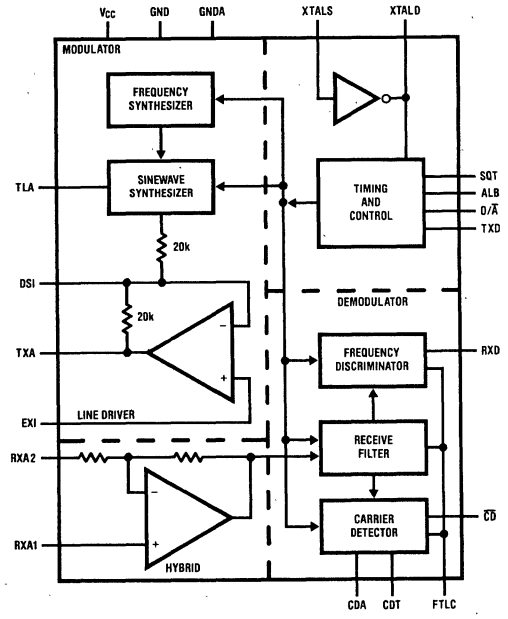


TOP VIEW TL/F/5349–1

MM74HC943

74HC943 (J,N)

Block Diagram



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Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A) MM74HC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HC T_A=−40 to 85°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	V_{CC}	V_{CC}−0.1 3.84	V_{CC}−0.1 3.7	V V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V		0.1 0.33	0.1 0.4	V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IH}=V_{CC}, V_{IL}=GND ALB or SQT=GND Transmit Level=−9 dBm	8.0			mA
I_{CC}	Power Down Supply Current	ALB=SQT=V_{CC} V_{IH}=V_{CC}, V_{IL}=GND			250	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

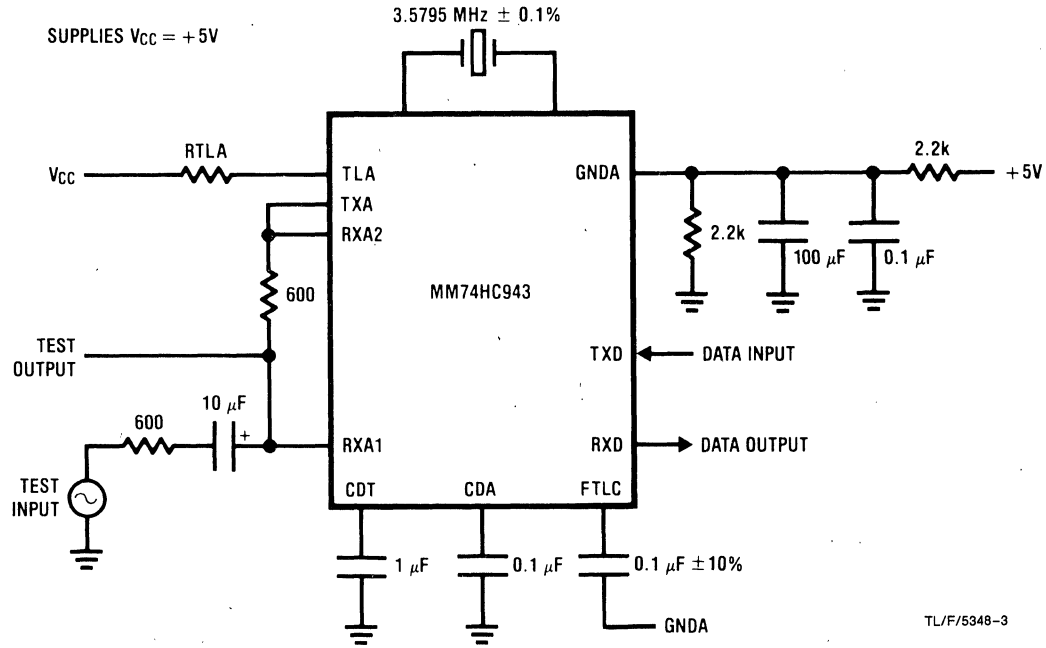
*The demodulator specifications apply to the MM74HC943 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC943 modulator.

AC Electrical Characteristics

Unless otherwise specified all specifications apply to the MM74HC943 over the range −40°C to +85°C using a V_{CC} of +5V ±10%, and a 3.579 MHz ±0.1% crystal.*

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER							
F_{CE}	Carrier Frequency Error				1	4	Hz
	Power Output	V_{CC} = 5.0V R_L = 1.2 kΩ	R_{TLA} = 5490 R_{TLA} = ∞		−9 −12		dBm dBm
	2nd Harmonic Energy				−56		dBm
RECEIVE FILTER AND HYBRID							
	Hybrid Input Impedance (Pins 15 and 16)			50			kΩ
	FTLC Output Impedance			10		50	kΩ
	Adjacent Channel Rejection	RXA2 = GNDA, TXD = GND or V_{CC} Input to RXA1		60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)							
	Carrier Amplitude			−48		−12	dBm
	Dynamic Range				36		dB
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud			100		μS
	Bit Bias				5		%
	Carrier Detect Trip Points	CDA = 1.2V	Off to On On to Off		−44 −47		dBm dBm

AC Specification Circuit



Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This input may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data output pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system. XTALD can be driven.
9	XTALS	Crystal Sense: Refer to pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receiver filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	GND	Ground: This defines the chip 0V.
13	O/$\overline{A}$	Originate/$\overline{Answer}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded.
19	GNDA	Analog Ground: Analog signals within the chip are referred to this pin.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC943 uses frequency shift keying (FSK) of audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC943 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC943 is capable of transmitting and receiving data simultaneously.

The tone allocation used by the MM74HC943 and other Bell 103 compatible modems is shown in Table I. The terms "originate" and "answer" which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

TABLE I. Bell 103 Tone Allocation

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switch capacitor nine pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60Hz, a common noise component.

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The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency synthesizer produces one of four tones depending on the O/$\overline{A}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter.

The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

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The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source inpedances.

The transmit level is programmable by placing a resistor from TLA to V_{CC}. With a 5.5K resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the MM74HC943 will interface to most telephones. This arrangement is called the "permissive arrangement". The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

TABLE II. Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ω)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used;

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$T_{\overline{CDL}} \cong 6.4 \times C_{CDT}$ for $\overline{CD}$ going low

$T_{\overline{CDH}} \cong 0.54 \times C_{CDT}$ for $\overline{CD}$ going high

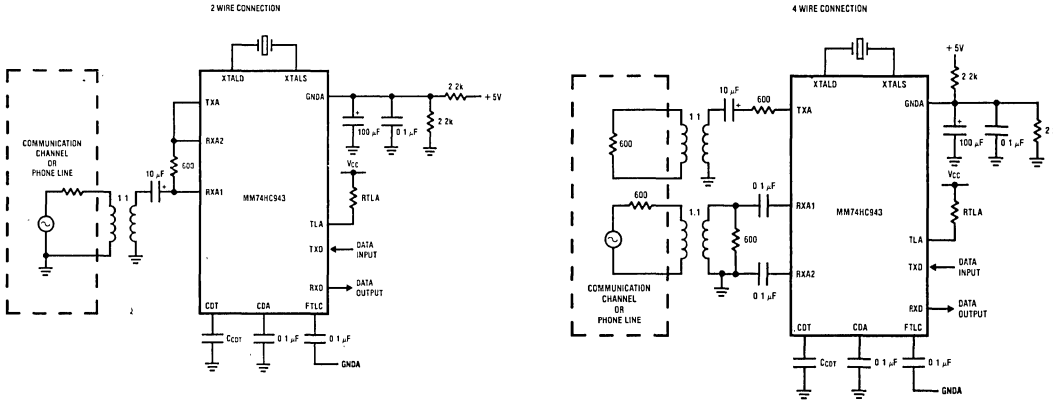
Where $T_{\overline{CDL}}$ & $T_{\overline{CDH}}$ are in seconds, and C_{CDT} is in μF.

DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC943 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout. Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

Applications Information (Continued)

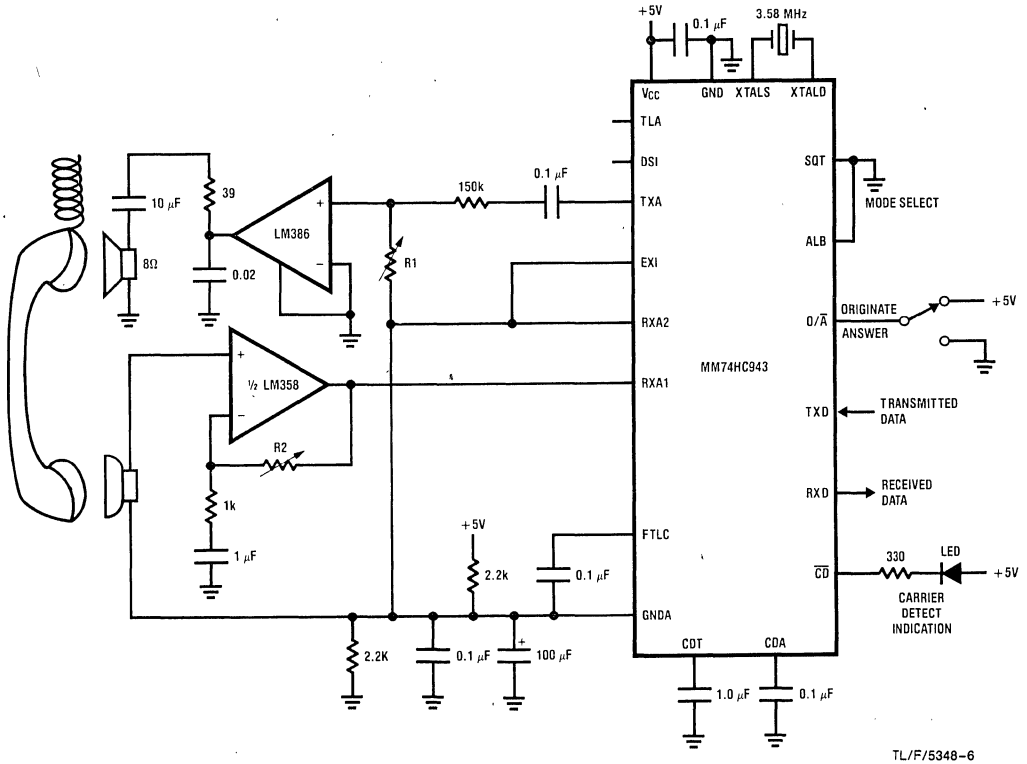
Interface Circuits for MM74HC943 300 Baud Modem



TL/F/5348–4 TL/F/5348–5

C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.

Complete Acoustically Coupled 300 Baud Modem



TL/F/5348–6

Note: The efficiency of the acoustic coupling will set the values of R1 and R2.

National Semiconductor

MM54HC4002/MM74HC4002 Dual 4-Input NOR Gate

General Description

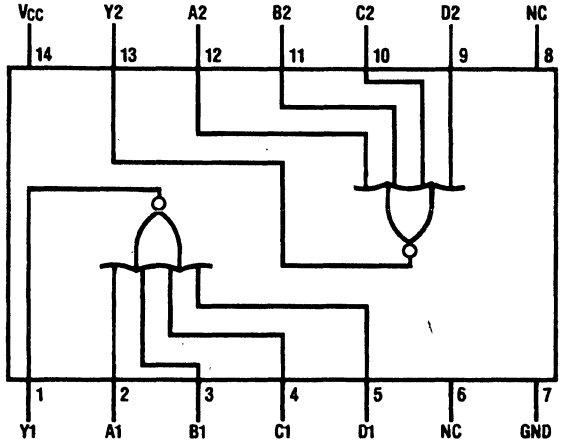
These NOR gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4002/74HC4002 is functionally equivalent and pin-out compatible with the CD4002B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



TOP VIEW

TL/F/5154–1

MM54HC4002/MM74HC4002

54HC4002 (J) 74HC4002 (J,N)

$$Y = \overline{A + B + C + D}$$

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		11	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	40	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

PRELIMINARY

National Semiconductor

MM54HC4016/MM74HC4016 Quad Analog Switch

General Description

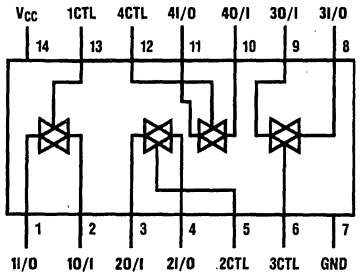
These devices are digitally controlled analog switches implemented in microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. These switches have low 'on' resistance and low 'off' leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. The '4016 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low 'on' resistance: 50Ω typ
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram

Dual-In-Line



TL/F/5350–1

MM54HC4016/MM74HC4016

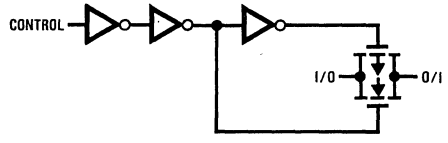
54HC4016 (J) 74HC4016 (J,N)

Truth Table

Input	Switch
CTL	I/O-O/I
L	"OFF"
H	"ON"

Schematic Diagram

MM54HC4016/MM74HC4016



TL/F/5350–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	6.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			9.0V		1.8	1.8	1.8	V
			12.0V		2.4	2.4	2.4	V
R_{ON}	Maximum 'ON' Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=.1 mA V_{IS}=V_{CC} to GND (Figure 1)	4.5V	100			Ω
			9.0V	50			Ω
			12.0V	30			Ω
		V_{CTL}=V_{IH}, I_S=.1 mA V_{IS}=V_{CC} or GND (Figure 1)	2.0V	120			Ω
			4.5V	50			Ω
			9.0V	35			Ω
			12.0V	20			Ω
R_{ON}	Maximum 'ON' Resistance Matching	V_{CTL}=V_{IH} V_{IS}=V_{CC} to GND	4.5V	10			Ω
			9.0V	5			Ω
			12.V	5			Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND V_{CC}=2–6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch 'OFF' Leakage Current	V_{OS}=V_{CC} or GND V_{IS}=GND or V_{CC} V_{CTL}=V_{IL} (Figure 2)	5.5V	10			nA
			9.0V	15			nA
			12.0V	20			nA
I_{IZ}	Maximum Switch 'ON' Leakage Current	V_{OS}=V_{CC} or GND V_{CTL}=V_{IH} (Figure 3)	5.5V	10			nA
			9.0V	15			nA
			12.0V	20			nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	5.5V		2.0	20	40	μA
			9.0V		8.0	80	160	μA
			12.0V		16.0	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so these values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

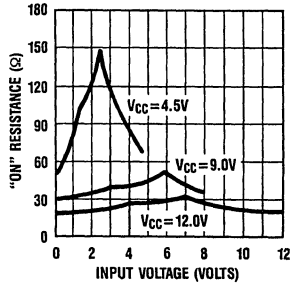
AC Electrical Characteristics

V_{CC}=2.0V–6.0V V_{EE}=0V to 6V, C_L=15 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V 4.5V 9.0V 12.0V	25 5 4 3				ns ns ns ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L=1 kΩ	2.0V 4.5V 9.0V 12.0V	32 8 6 5				ns ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		2.0V 4.5V 9.0V 12.0V	45 15 10 8				ns ns ns ns
f_{MAX}	Maximum Switch Frequency Response 20log(V_I/V_O)=−3 Db		4.5V 9.0V	100 120				MHz MHz
	Cross Talk Control to Switch	(Figure 7)	4.5V	180				mV_{P-P}
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	4.5V					MHz
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CLT}=GND		5				pF

Typical Performance Characteristics

Typical "On" Resistance Versus Input Voltages ('4016)



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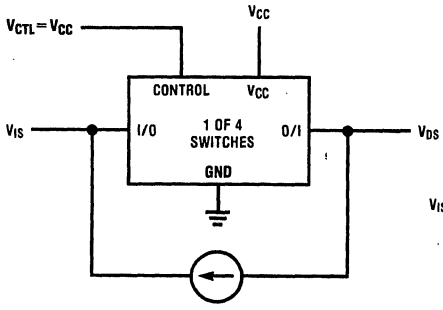
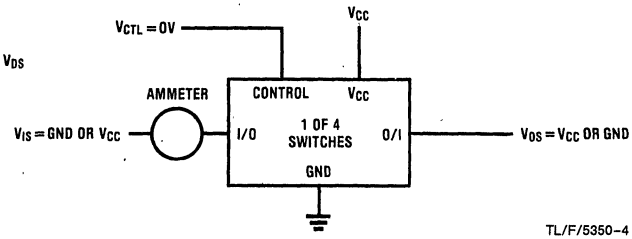
AC Test Circuits and Switching Time Waveforms



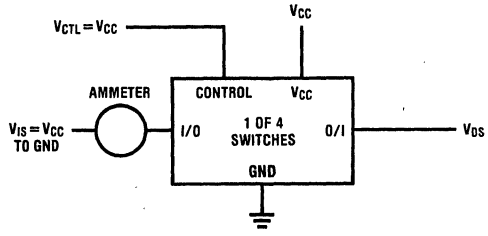
TL/F/5350-3

FIGURE 1. "ON" Resistance



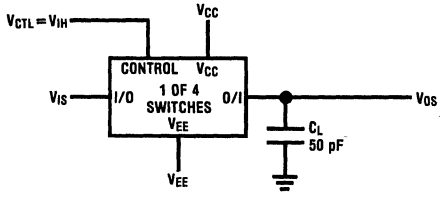
TL/F/5350-4

FIGURE 2. "OFF" Channel Leakage Current



TL/F/5350-5

FIGURE 3. "ON" Channel Leakage Current



TL/F/5350-6

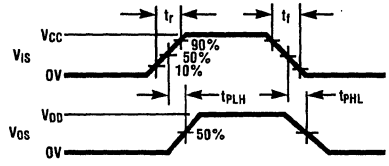


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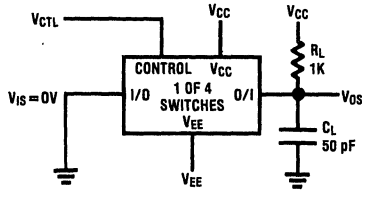
FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



TL/F/5350-8

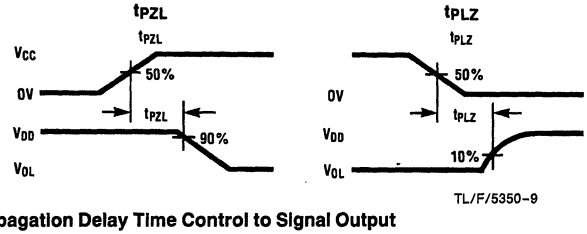


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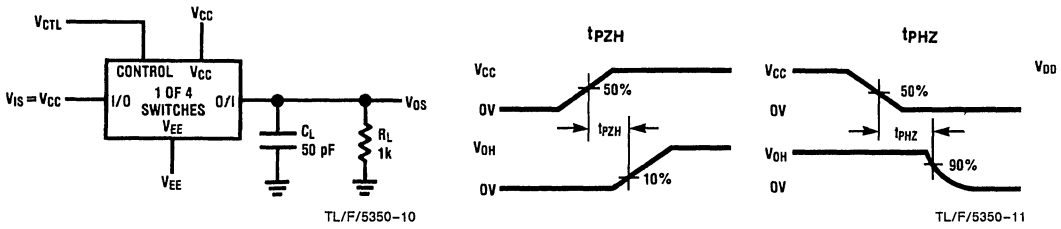
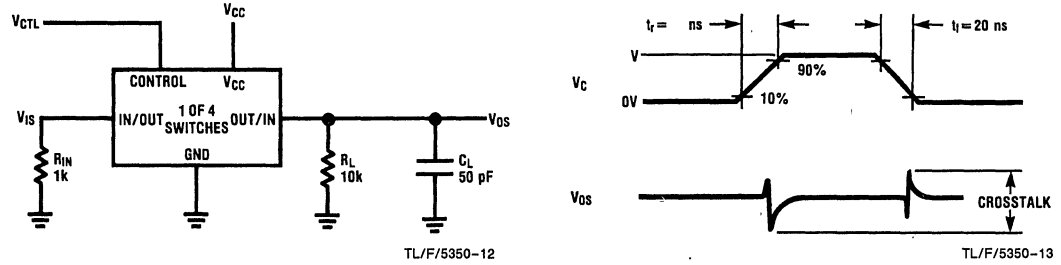
FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



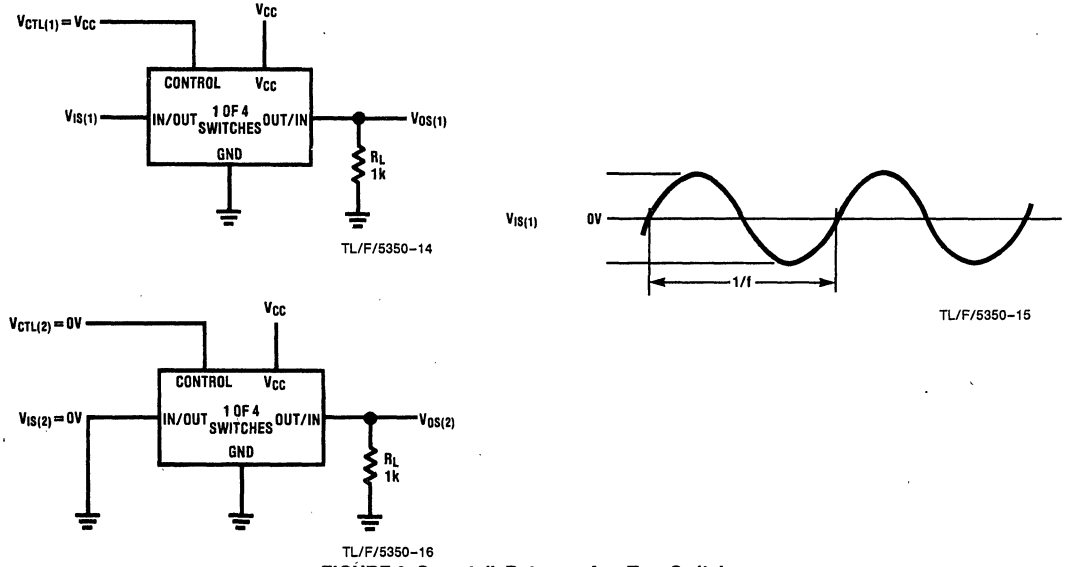
TL/F/5350–10 TL/F/5350–11

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



TL/F/5350–12 TL/F/5350–13

FIGURE 7. Crosstalk: Control Input to Signal Output



TL/F/5350–14 TL/F/5350–15

TL/F/5350–16

FIGURE 8: Crosstalk Between Any Two Switches

National Semiconductor

MM54HC4017/MM74HC4017
Decade Counter/Divider with 10 Decoded Outputs

General Description

The MM54HC4017/MM74HC4017 is a 5-stage Johnson counter with 10 decoded outputs that utilizes micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the clock input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY output transitions low to high after OUTPUT 10 goes low, and can be used in conjuncton with the CLOCK ENABLE to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET input is also provided which when taken high sets all the decoded outputs low.

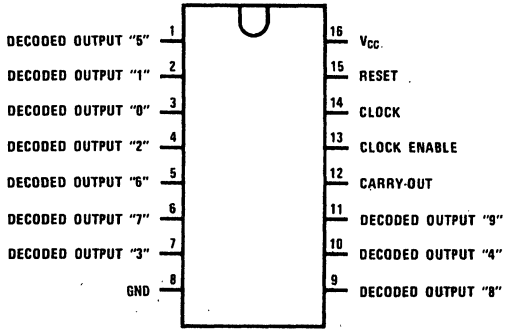
The MM54HC4017/MM74HC4017 is functionally and pinout equivalent to the CD4017BM/CD4017BC. It can drive up to 10 low power Schottky equivalent loads. All inputs are protected from damage due to static discharge by diodes from V_{CC} and ground.

Features

- Wide power supply range: 2–6V
- Typical operating frequency: 30 MHz
- Fanout of 10 LS-TTL loads.
- Low quiescent current: 80 μA (74HC series)
- Low input current: 1.0 μA

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

TL/F/5351–1

MM54HC4017/MM74HC4017

54HC4017 (J) 74HC4017 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency	Measured with respect to carry line	50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Carry-Out Line		26	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable Decode-Out Lines		27	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Decode Out		23	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Carry Out		23	40	ns
t_S	Minimum Clock Inhibit Data Set-Up Time		12	20	ns
t_W	Minimum Clock or Reset Pulse Width		8	16	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, C_L 50 pF $t_r=t_f=6$ ns (unless otherwise specified)

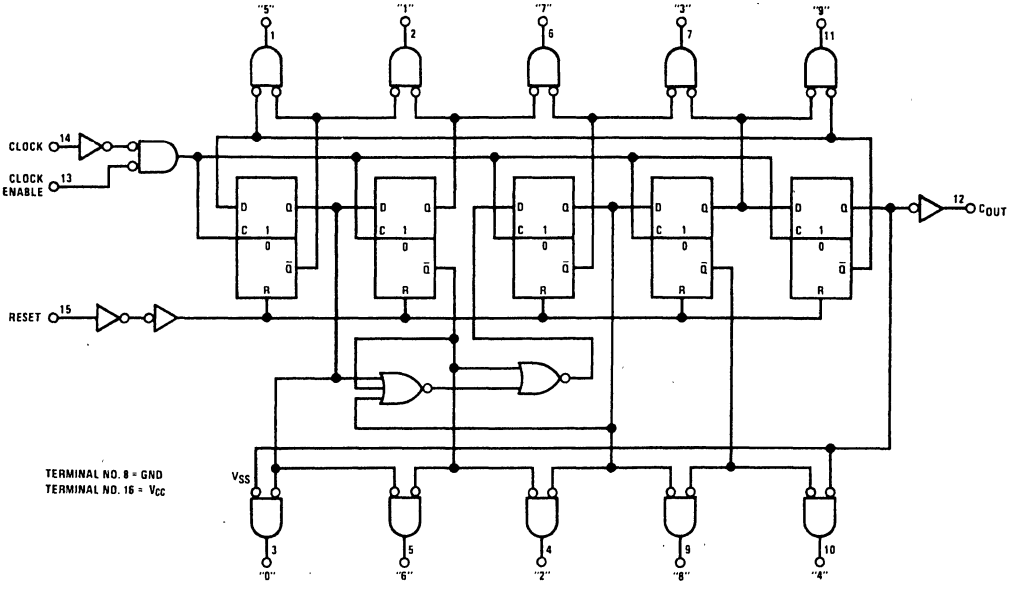
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency	Measured with respect to carry line	2.0V		4	3	3	MHz
			4.5V		20	16	13	MHz
			6.0V		23	18	15	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Carry-Out Line		2.0V	89	250	312	375	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Decode Out Line		2.0V	90	250	312	375	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Decode Out		2.0V	82	230	288	345	ns
			4.5V	22	46	58	69	ns
			6.0V	18	39	49	59	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Carry Out		2.0V	82	230	288	345	ns
			4.5V	22	46	58	69	ns
			6.0V	18	39	49	59	ns
t_W	Minimum Reset or Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	21	ns
t_{REM}	Minimum Reset Removal Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Minimum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)						pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

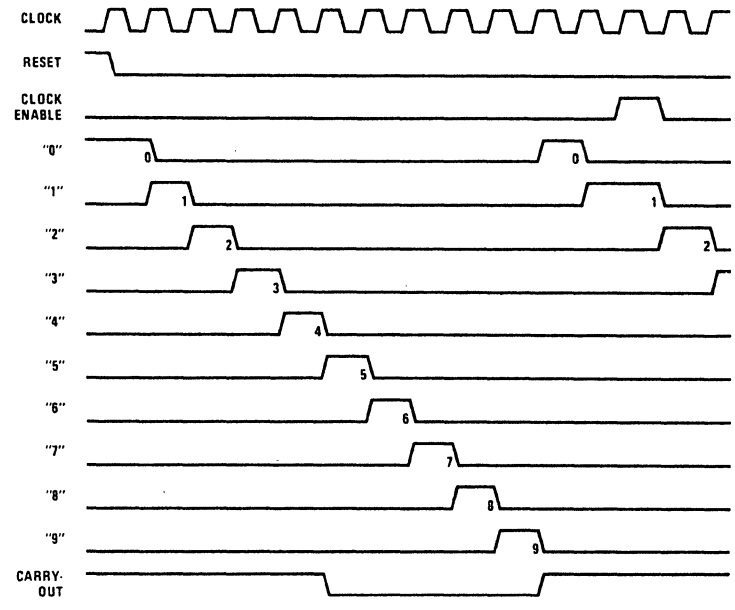
Logic Diagram

MM54HC4017/MM74HC4017



TL/F/5351–2

Timing Diagram



TL/F/5351–3

National Semiconductor

MM54HC4020/MM74HC4020 14 Stage Binary Counter
MM54HC4024/MM74HC4024 7 Stage Binary Counter
MM54HC4040/MM74HC4040 12 Stage Binary Counter

General Description

The MM54HC4020/MM74HC4020, MM54HC4024/MM74HC4024, MM54HC4040/MM74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4020 is a 14 stage counter, the 'HC4040 is a 12 stage counter, and the 'HC4024 is a 7 stage counter. All these devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

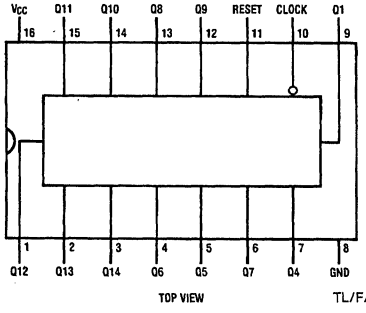
These devices are pin equivalent to the CD4020, CD4024 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC series)
- Output drive capability: 10 LS-TTL loads

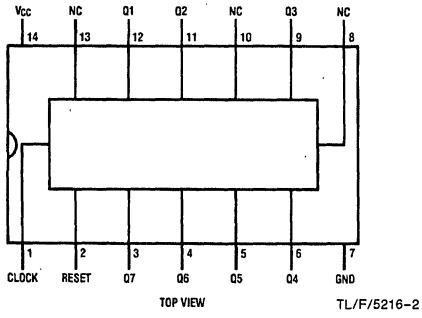
Connection Diagrams

Dual-In-Line Packages



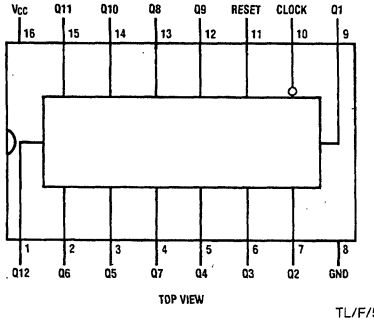
MM54HC4020/MM74HC4020

54HC4020 (J) 74HC4020 (J, N)



MM54HC4024/MM74HC4024

54HC4024 (J) 74HC4024 (J, N)



MM54HC4040/MM74HC4040

54HC4040 (J) 74HC4040 (J, N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	25	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	(Note 5)	17	35	ns
t_{PHL}	Maximum Propagation Delay Reset to Any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency ('4020 and '4040)		2.0V 4.5V 6.0V	10 40 50	4 20 24	3 16 19	3 13 16	MHz MHz MHz
f_{MAX}	Maximum Operating Frequency ('4024)		2.0V 4.5V 6.0V	10 50 60	5 25 29	4 20 23	3 17 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_1		2.0V 4.5V 6.0V	80 21 18	210 42 36	265 53 45	313 63 53	ns ns ns
t_{PHL}	Maximum Propagation Delay Reset to Q ('4024 only)		2.0V 4.5V 6.0V	80 21 18	210 42 36	265 53 45	313 63 53	ns ns ns
t_{PHL}	Maximum Propagation Delay Reset to Any Q ('4020 and '4040)		2.0V 4.5V 6.0V	72 24 20	240 40 41	302 60 51	358 72 61	ns ns ns
t_{REM}	Minimum Reset Removal Time		2.0V 4.5V 6.0V		100 20 16	126 25 21	149 50 25	ns ns ns
t_W	Minimum Pulse Width		2.0V 4.5V 6.0V		90 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 10 9	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time				1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

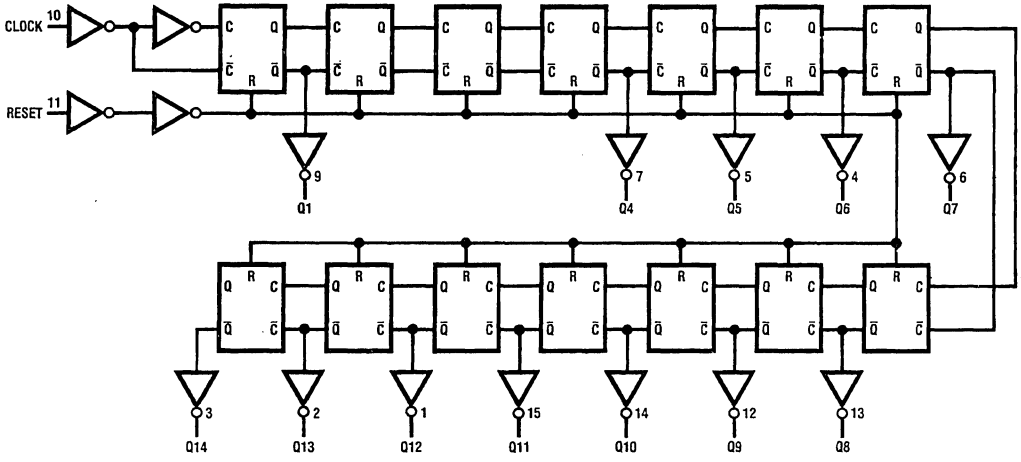
Note 5: Typical Propagation delay time to any output can be calculated using: $t_P=17+12(N-1)$ ns; where N is the number of the output, Q_W, at $V_{CC}=5V$.

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 7: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

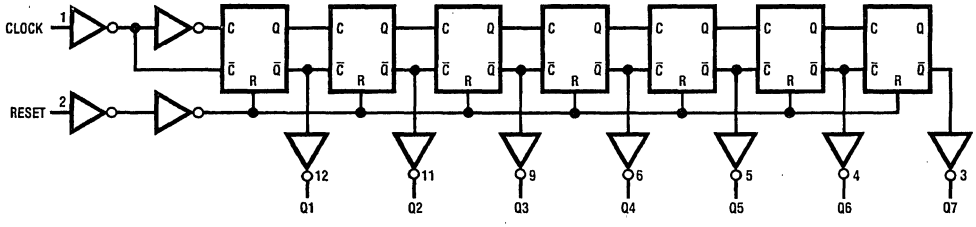
Logic Diagrams

MM54HC4020/MM74HC4020



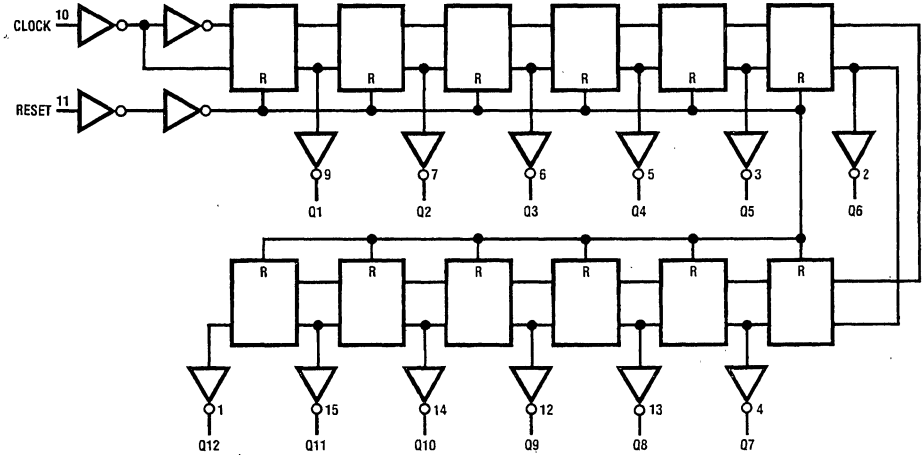
TL/F/5216–5

MM54HC4024/MM74HC4024



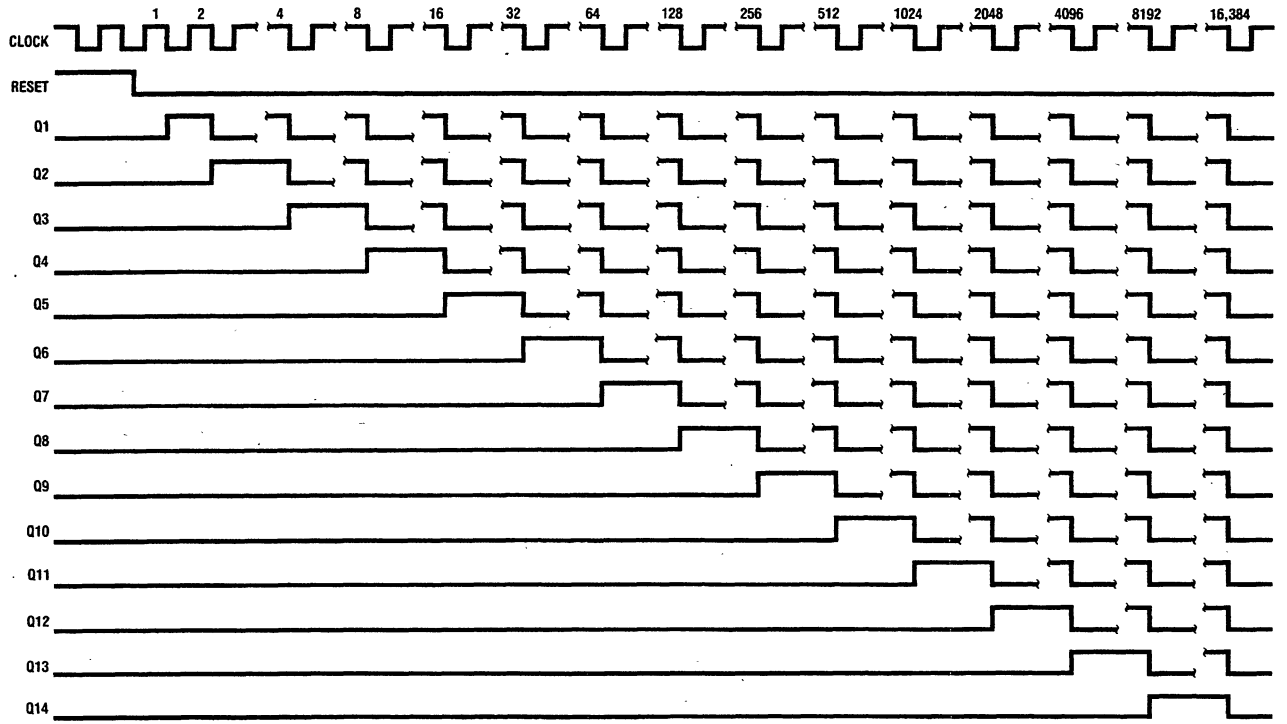
TL/F/5216–6

MM54HC4040/MM74HC4040



TL/F/5216–7

Timing Diagram



TL/F/5216–11

PRELIMINARY

National Semiconductor

MM54HC4046/MM74HC4046 Micropower Phase-Locked Loop

General Description

The HC4046 micropower phase-locked loop (PLL) utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption.

Features

- Wide supply voltage range 2.0V to 6.0V
- Low dynamic power consumption
- VCO frequency
- Low frequency drift with temperature
- High VCO linearity

Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

Block and Connection Diagrams

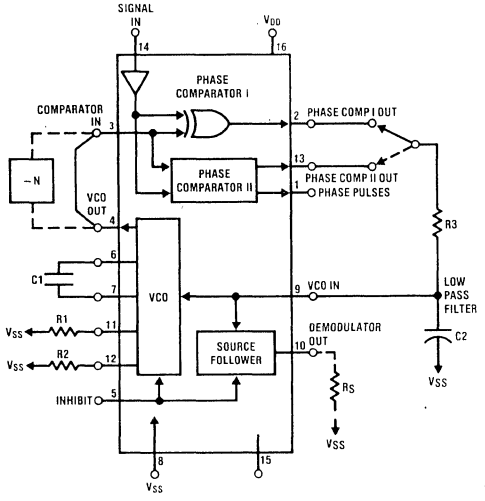
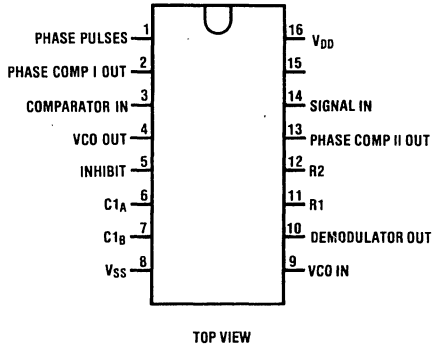


FIGURE 1

TL/F/5352–1

Dual-In-Line Package



TOP VIEW

TL/F/5352–2

MM54HC4046/MM74HC4046

54HC4046 (J) 74HC4046 (J, N)

4

National Semiconductor

MM54HC4049/MM74HC4049 Hex Inverting Logic Level Down Converter
MM54HC4050/MM74HC4050 Hex Logic Level Down Converter

General Description

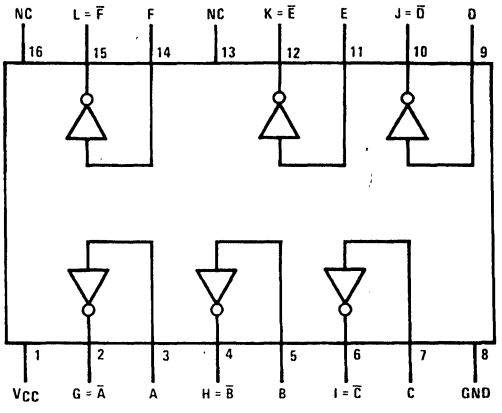
The MM54HC4049/MM74HC4049 and the MM54HC4050/MM74HC4050 utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and have a modified input protection structure that enables these parts to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0–15V CMOS logic can be converted to 0–5V logic when using a 5V supply. The modified input protection has no diode connected to V_{CC} thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition each part can be used as a simple buffer or inverter without level translation. The MM54HC4049/MM74HC4049 is pin and functionally compatible to the CD4049BM/CD4049BC and the MM54HC4050/MM74HC4050 is compatible to the CD4050BM/CD4050BC

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 20 μA maximum (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



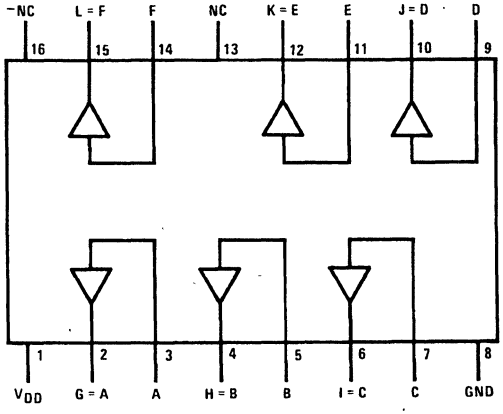
TOP VIEW

TL/F/5214–1

MM54HC4049/MM74HC4049

54HC4049 (J) 74HC4049 (J,N)

Dual-In-Line Package



TOP VIEW

TL/F/5214–2

MM54HC4050/MM74HC4050

54HC4050 (J) 74HC4050 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+18V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{ZK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input Voltage		0	15	V
(V_{IN})			V_{CC}	V
DC Output Voltage		0	V_{CC}	V
(V_{OUT})				
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40°C to 85°C	54HC T_A=−55°C to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4 mA	4.5V	0.2	0.26	0.33	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	V
						0.4	V
						0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	μA
		V_{IN}=15V	6.0V		±0.5	±5	μA
						±1.0	μA
						±5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	μA
						40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40°$ to $85°C$		54HC $T_A=-55°$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	30	76	92	106	ns
			4.5V	10	17	20	26	ns
			6.0V	9	15	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

PRELIMINARY

National Semiconductor

MM54HC4051/MM74HC4051 8 Channel Analog Multiplexer MM54HC4052/MM74HC4052 Dual 4 Channel Analog Multiplexer MM54HC4053/MM74HC4053 Triple 2 Channel Analog Multiplexer

General Description

These multiplexers are digitally controlled analog switches implemented in microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also these switches contain linearization circuitry which lowers the on resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. Three supply pins are provided for V_{CC}, Ground, and V_{EE}. This enables the connection of 0–5V logic signals when $V_{CC}=5V$ and an analog input range of ±5V when $V_{EE}=5V$. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

MM54HC4051/MM74HC4051: This device connects together the outputs of 8 switches, thus achieving an 8 Channel Multiplexer. The binary code placed on the A, B, and C select lines determine which one of the eight switches in "on", and connects one of the eight inputs to the common output.

MM54HC4052/MM74HC4052: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4 channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4 channel differential multiplexer.

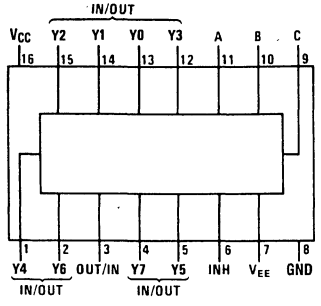
MM54HC4053/MM74HC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configuration. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

Features

- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Logic level translation to enable 5V logic with ±5V analog signals
- Low quiescent current: 80 μA maximum (74HC)
- Matched Switch characteristic

Connection Diagrams

Dual-In-Line Package



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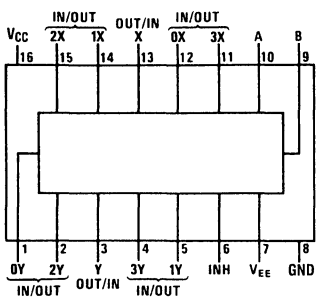
MM54HC4051/MM74HC4051

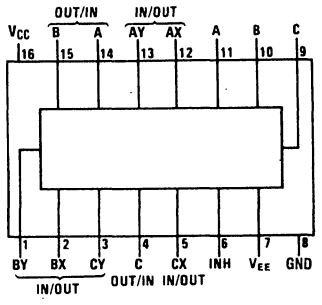
54HC4051 (J) 74HC4051 (J, N)



TL/F/5353-2

MM54HC4052/MM74HC4052

54HC4052 (J) 74HC4052 (J, N)



TL/F/5353-3

MM54HC4053/MM74HC4053

54HC4053 (J) 74HC4053 (J, N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
Output Current, per pin (I_{OUT})	±25 mA
V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
Supply Voltage(V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=0.1 mA	GND	4.5V	40			Ω
		V_{IS}=V_{CC} to GND	−4.5V	4.5V	30			Ω
		(Figure 1)	−6.0V	6.0V	20			Ω
			GND	2.0V	100			Ω
		V_{CTL}=V_{IH}, I_S=0.1 mA	GND	4.5V	40			Ω
		V_{IS}=V_{CC} or GND	−4.5V	4.5V	20			Ω
		(Figure 1)	−6.0V	6.0V	15			Ω
R_{ON}	Maximum "ON"Resistance Matching	V_{CTL}=V_{IH}	GND	4.5V	10			Ω
		V_{IS}=V_{CC} to GND	−4.5V	4.5V	5			Ω
			−6.0V	6.0V	5			Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND				±0.1	±1.0	±1.0	μA
		V_{CC}=2–6V							
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS}=V_{CC} or GND	GND	6.0V	10			nA
		V_{IS}=GND or V_{CC}	−6.0V	6.0V	20			nA
		V_{CTL}=V_{IL} (Figure 2)						
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS}=V_{CC} or GND	GND	6.0V	20			nA
		V_{CTL}=V_{IH}	−6.0V	6.0V	40			nA
		(Figure 3)						
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND	GND	6.0V		8	80	160	μA
		I_{OUT}=0 μA	−6.0V	6.0V		16	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V V_{EE} = 0V–6V, C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C		54HC T_A = −55 to 125°C		Units
					Typ	Guaranteed Limits				
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25					ns
			GND	4.5V	5					ns
			−4.5V	4.5V	4					ns
			−6.0V	6.0V	3					ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	GND	2.0V	92					ns
			GND	4.5V	18					ns
			−4.5V	4.5V	16					ns
			−6.0V	6.0V	15					ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		GND	2.0V	65					ns
			GND	4.5V	28					ns
			−4.5V	4.5V	18					ns
			−6.0V	6.0V	16					ns
f_{MAX}	Minimum Switch Frequency Response $20\log(V_I/V_O) = 3$ dB		GND	4.5V	100					MHz
			−4.5V	4.5V	120					MHz
	Cross Talk Control to Switch	(Figure 7)	−4.5V	4.5V	180					mV_{P-P}
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	−4.5V	4.5V						MHz
C_{IN}	Maximum Control Input Capacitance				5	10	10	10		pF
C_{IN}	Maximum Switch Input Capacitance	Input			15					pF
		4051 Common			90					
		4052 Common			45					
		4053 Common			30					
C_{IN}	Maximum Feedthrough Capacitance				5					pF

Truth Tables

'4051

Input				"ON" Channel
Inh	C	B	A	
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

'4052

Inputs			"ON" Channels	
Inh	B	A	X	Y
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

'4053

Input				"ON" Channels		
Inh	C	B	A	C	b	a
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AY
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AY
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AY
L	H	H	H	CY	BY	AY

AC Test Circuits and Switching Time Waveforms

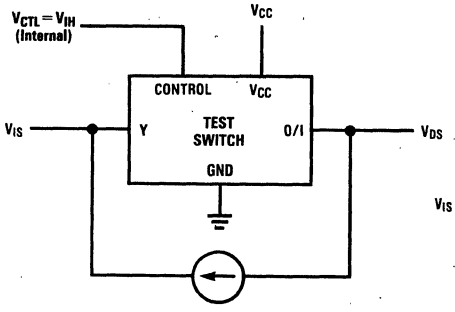


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FIGURE 1. "ON" Resistance

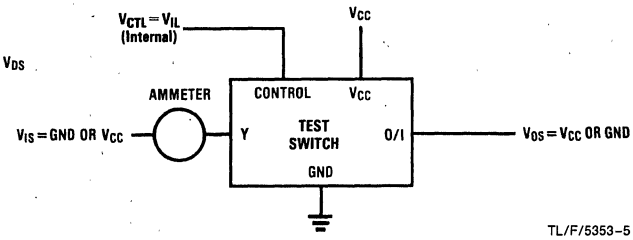

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FIGURE 2. "OFF" Channel Leakage Current

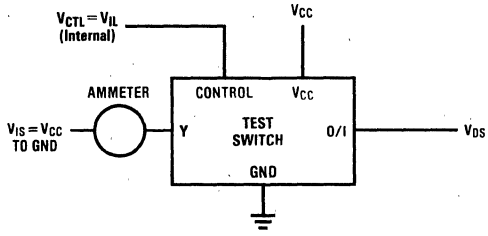

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FIGURE 3. "ON" Channel Leakage Current

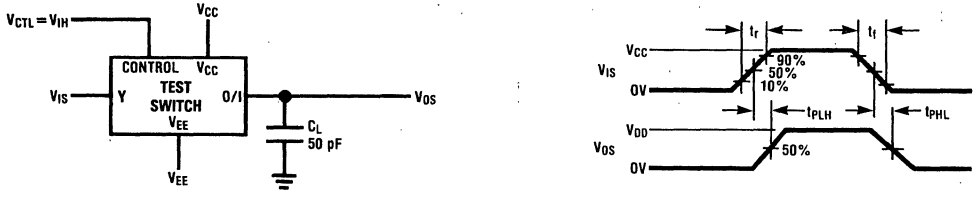

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FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

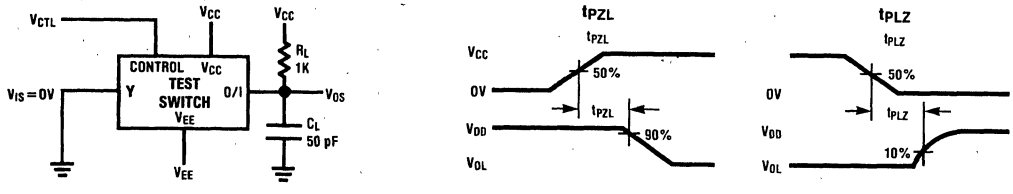

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FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

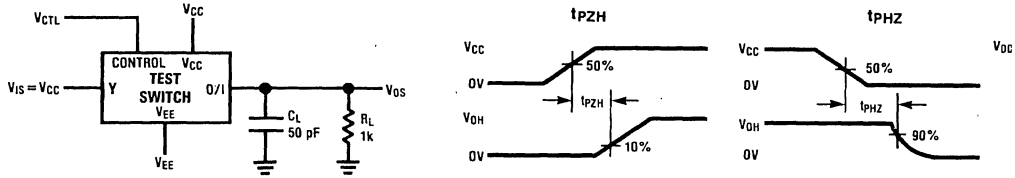


FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

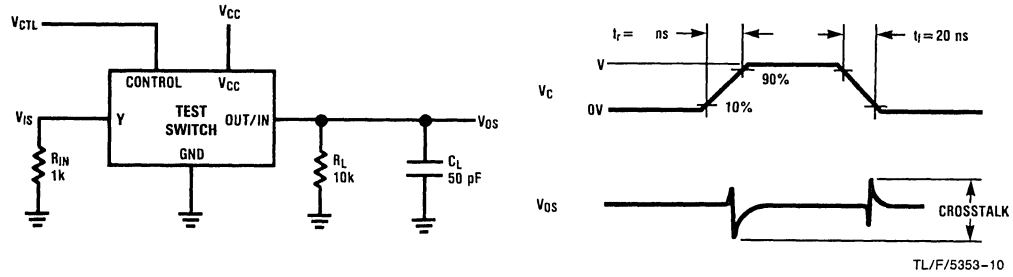


FIGURE 7. Crosstalk: Control Input to Signal Output

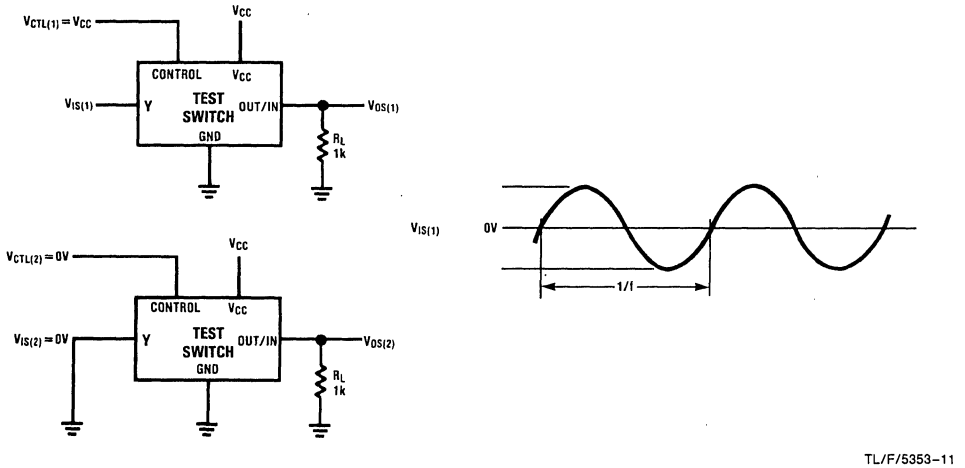
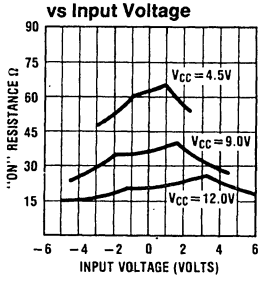


FIGURE 8. Crosstalk Between Any Two Switches

Typical Performance Characteristics

Typical "On" Resistance vs Input Voltage

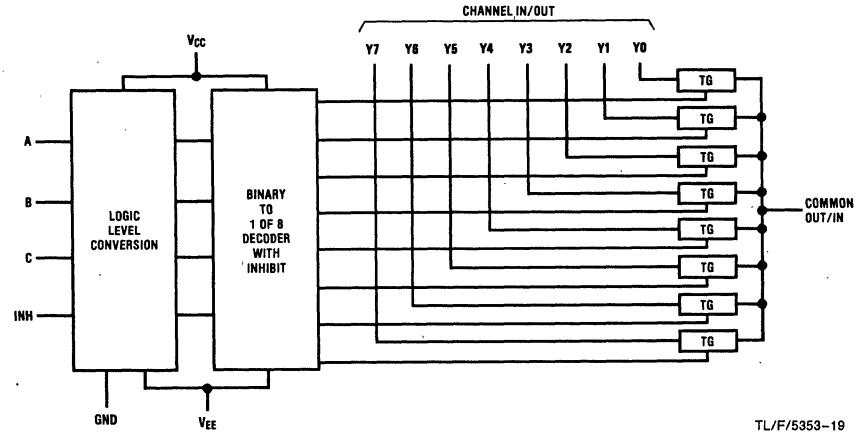


$V_{CC} = -V_{EE}$ TL/F/5353-18

4

Logic Diagrams

MM54HC4051/MM74HC4051



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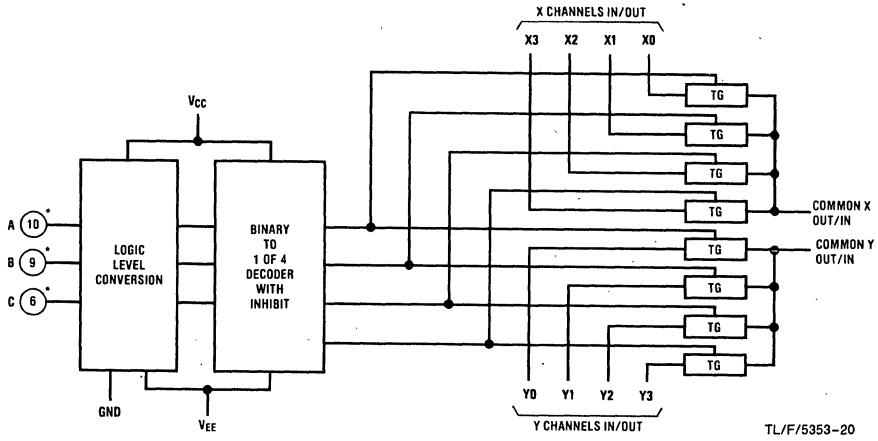
MM54HC4052/MM74HC4052



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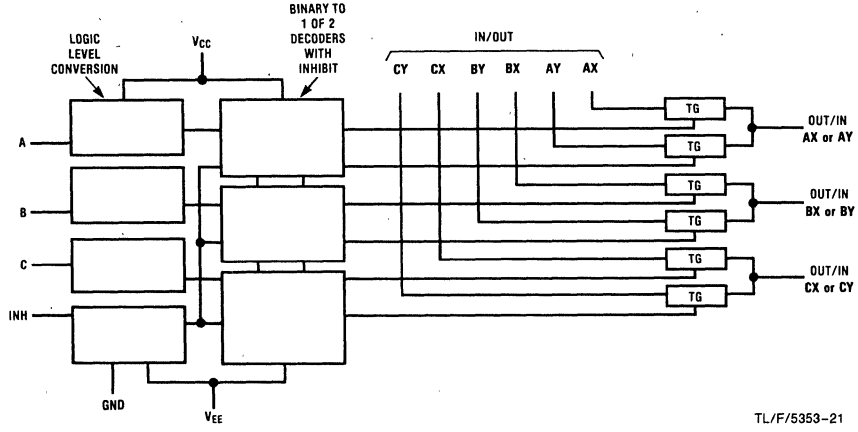
MM54HC4053/MM64HC4053



TL/F/5353–21

National Semiconductor

MM54HC4060/MM74HC4060 14 Stage Binary Counter

General Description

The MM54HC4060/MM74HC4060 is a high speed binary ripple carry counter. These counters are implemented utilizing microCMOS™ technology, 3.5 micron silicon gate P-well CMOS, to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4060 is a 14 stage counter, this device increments on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input. The 'HC4060 also has two additional inputs to enable easy connection of either an RC or crystal oscillator.

This device is pin equivalent to the CD4060. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 series)
- Output drive capability: 10 LS-TTL loads

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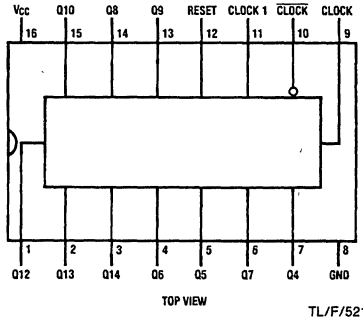
Connection Diagram

Dual-In-Line Package



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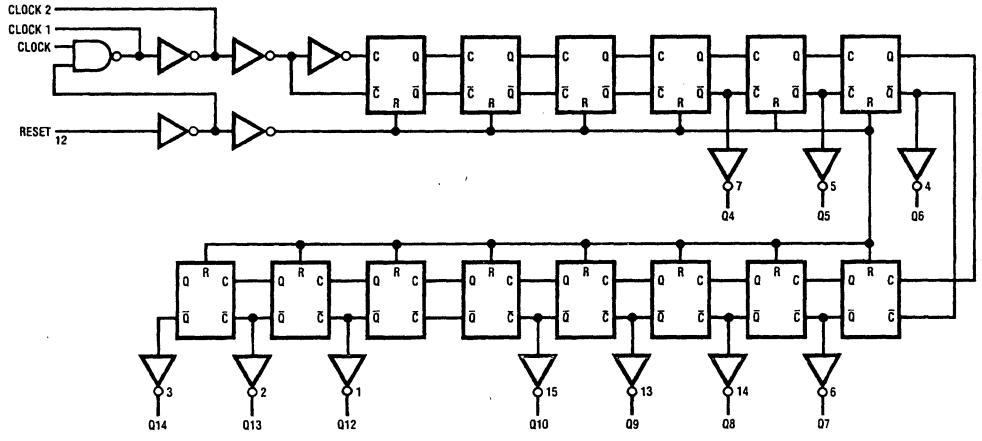
MM54HC4060/MM74HC4060

54HC4060 (J) 74HC4060 (J, N)

Logic Diagram

MM54HC4060/MM74HC4060



TL/F/5216–8

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage(V_{CC})	−0.5 to +7.0V
DC Input Voltage(V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage(V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current(I_{CD})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC Vcc or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤ 4 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating: plastic "N" package: −12 mW/°C from 65°C to 85°C ceramic "J" package: −12 mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		40	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_4	(Note 5)	40	55	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Reset to Any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

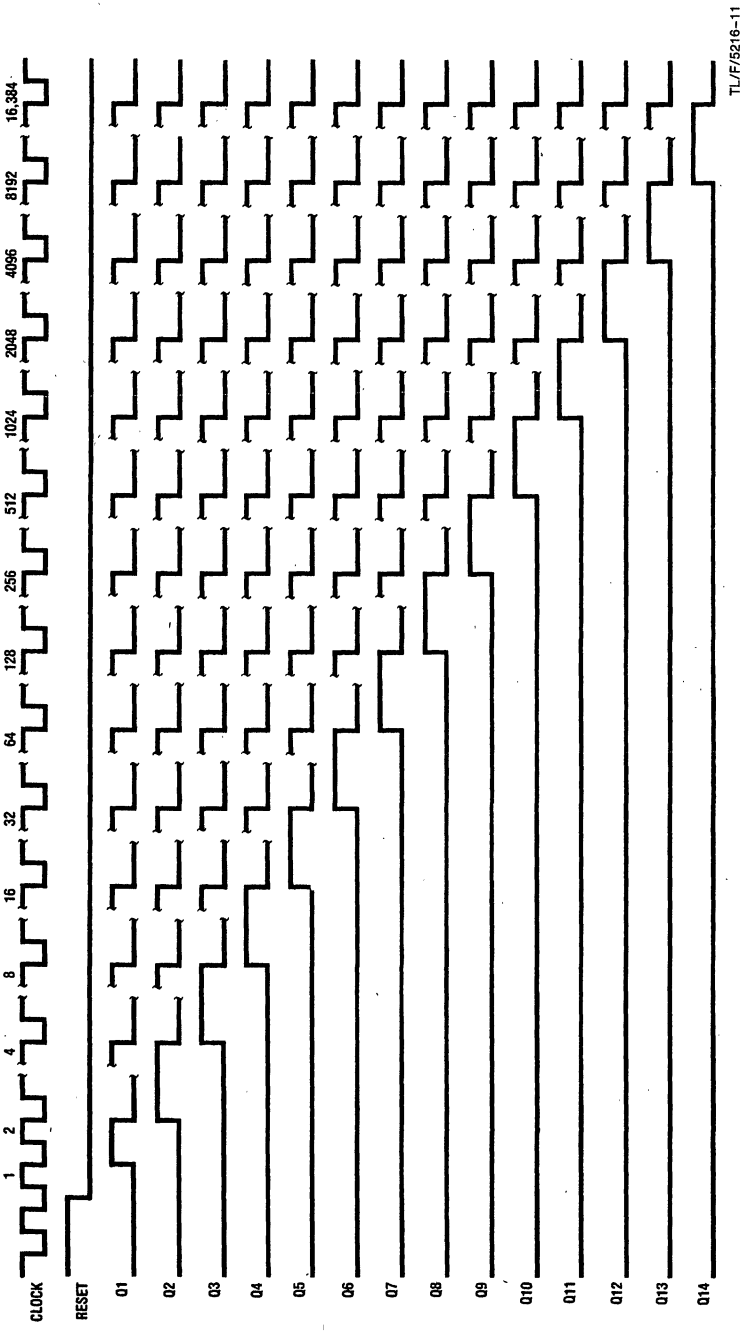
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	T_A74HC $T_A=-40$ to $85°C$	T_A54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	4	3	3	MHz
			4.5V	40	20	16	13	MHz
			6.0V	50	24	19	16	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_4		2.0V	120	300	375	450	ns
			4.5V	42	60	75	90	ns
			6.0V	35	47	59	62	ns
t_{PHL}	Maximum Propagation Delay Reset to Any Q		2.0V	72	240	302	358	ns
			4.5V	24	48	60	72	ns
			6.0V	20	41	51	61	ns
t_{REM}	Minimum Reset Removal Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_W	Minimum Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: Typical Propagation delay time to any output can be calculated using: t_P 17+12(N−1) ns; where N is the number of the output, Q_W, at $V_{CC}=5V$.

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 7: Refer to Section 1 for Typical MM54/74 HC AC Switching Waveforms and Test Circuits.

Timing Diagram



National Semiconductor

PRELIMINARY

MM54HC4066/MM74HC4066 Quad Analog Switch

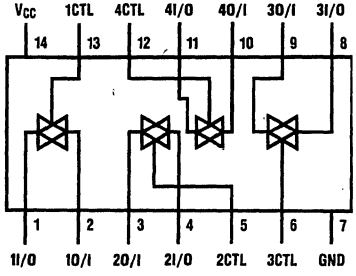
General Description

These devices are digitally controlled analog switches utilizing microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the '4066 switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. The '4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 30 typ. ('4066)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram



TL/F/5350–1

MM54HC4066/MM74HC4066

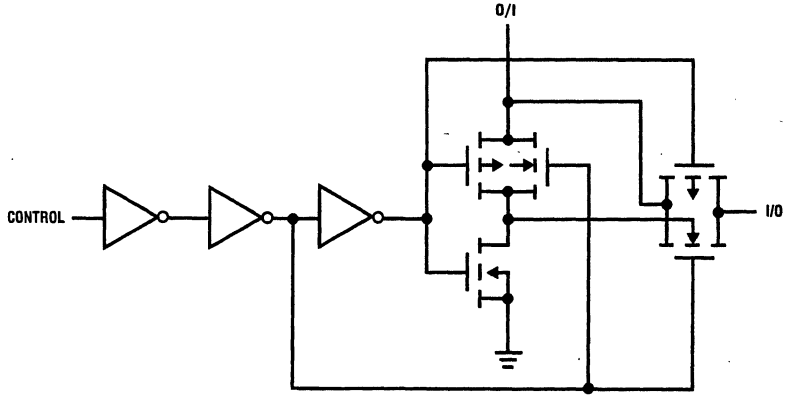
54HC4066 (J) 74HC4066 (J,N)

Truth Table

Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

Schematic Diagram

MM54HC4066/MM74HC4066



TL/F/5355–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=9.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	5.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			9.0V		1.8	1.8	1.8	V
			12.0V		2.4	2.4	2.4	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=.1 mA V_{IS}=V_{CC} to GND (Figure 1)	4.5V	100				Ω
			9.0V	50				Ω
			12.0	30				Ω
		V_{CTL}=V_{IH}, I_S=.1 mA V_{IS}=V_{CC} or GND (Figure 1)	2.0V	120				Ω
			4.5V	50				Ω
			9.0V	35				Ω
			12.0V	20				Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL}=V_{IH} V_{IS}=V_{CC} to GND	4.5V	10				Ω
			9.0V	5				Ω
			12.0V	5				Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND V_{CC}=2–6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS}=V_{CC} or GND V_{IS}=GND or V_{CC} V_{CTL}=V_{IL} (Figure 2)	5.5V	10				nA
			9.0V	15				nA
			12.0V	20				nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS}=V_{CC} or GND V_{CTL}=V_{IH} (Figure 3)	5.5V	10				nA
			9.0V	15				nA
			12.0V	20				nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	5.5V		2.0	20	40	μA
			9.0V		8.0	80	160	μA
			12.0V		16.0	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistance (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

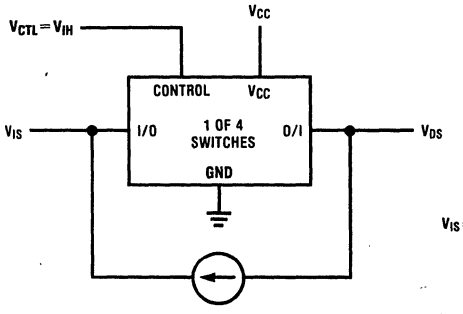
Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC}=2.0V–6.0V V_{EE}=0V–6V, C_L=50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V	25	50		ns
			4.5V	5	10	13	15	ns
			9.0V	4	8	10	12	ns
			12.0V	3	7	9	11	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L=1 kΩ	2.0V	32	80	100	120	ns
			4.5V	8	16	20	24	ns
			9.0V	6	14	18	21	ns
			12.0V	5	12	15	18	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		2.0V	45	150	187	225	ns
			4.5V	15	30	38	45	ns
			9.0V	10	20	25	30	ns
			12.0V	8	16	20	24	
f_{MAX}	Minimum Switch Frequency Response 20log(V_I/V_O)=3 dB		4.5V	100				MHz
			9.0V	120				MHz
	Cross Talk Control to Switch	(Figure 7)	4.5V	180				mV_{P-P}
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	4.5V					MHz
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input		15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL}=GND		5				pF

AC Test Circuits and Switching Time Waveforms



TL/F/5355-3

FIGURE 1. "ON" Resistance

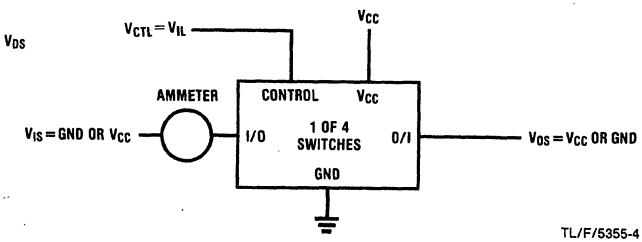


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FIGURE 2. "OFF" Channel Leakage Current

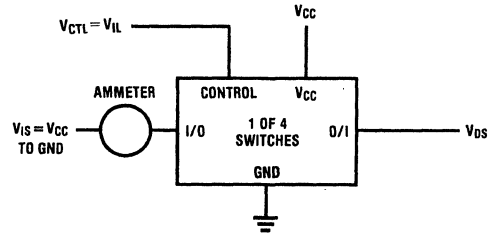

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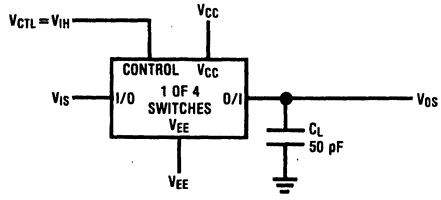
FIGURE 3. "ON" Channel Leakage Current



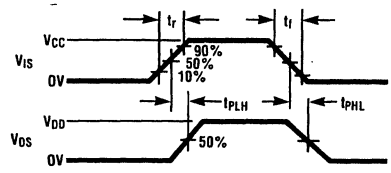


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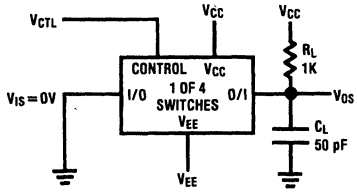
FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



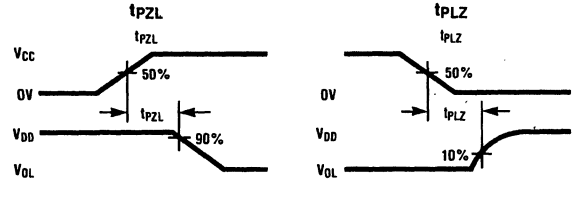


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FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

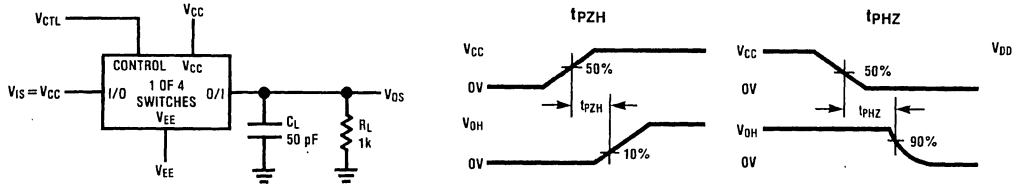

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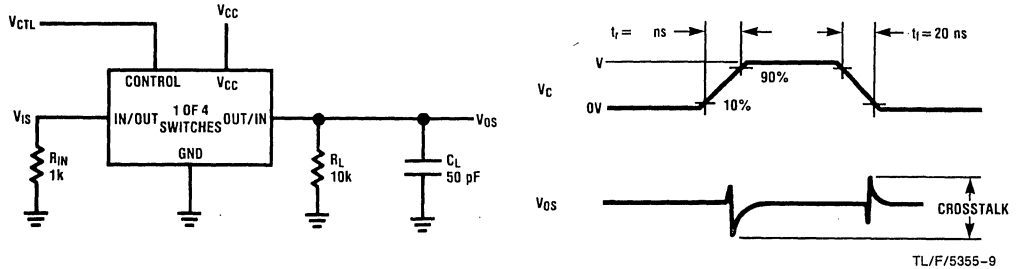
FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



TL/F/5355-9

FIGURE 7. Crosstalk: Control Input to Signal Output

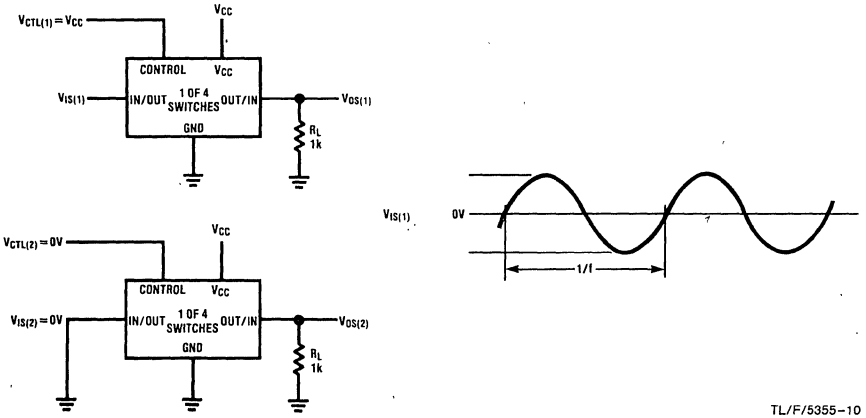


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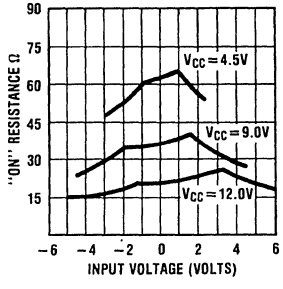
FIGURE 8: Crosstalk Between Any Two Switches

Typical Performance Characteristics

Typical "On" Resistance vs. Input Voltage ('4066)



TL/F/5355-18

National Semiconductor

MM54HC4075/MM74HC4075 Triple 3-Input OR Gate

General Description

These OR gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4075/74HC4075 is functionally equivalent and pin-out compatible with the CD4075B and MC14075B metal gate CMOS devices. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

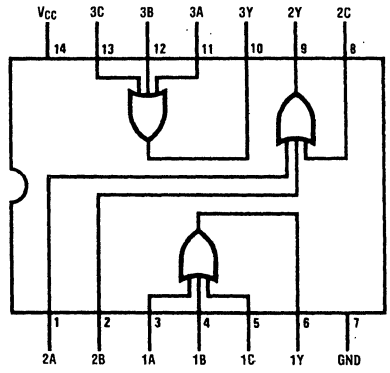
Features

- Typical propagation delay: 11 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

$Y=A+B+C$



TL/F/5155–1

MM54HC4075/MM74HC4075

54HC4075 (J) 74HC4075 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		11	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	40	115	145	171	ns
			4.5V	12	23	29	34	ns
			6.0V	10	20	25	29	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		30				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

MM54HC4078/MM74HC4078 8-Input NOR/OR Gate

General Description

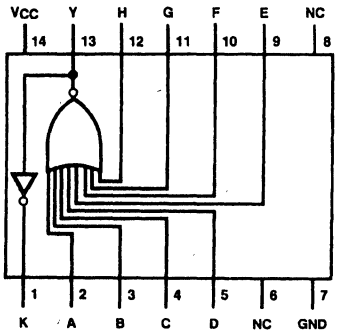
These NOR gates utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. Both outputs are buffered, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC4078/74HC4078 is functionally equivalent and pin-out compatible with the CD4078B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

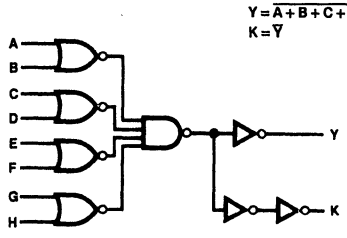


TL/F/5135–1

MM54HC4078/MM74HC4078

54HC4078 (J) 74HC4078 (J,N)

Logic Diagram



TL/F/5135–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC4078///74HC4078

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Y to Output		14	22	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, K to Output		16	24	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Y to Output		2.0V	47	130	160	195	ns
			4.5V	17	26	33	39	ns
			6.0V	14	22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, K to Output		2.0V	50	140	175	210	ns
			4.5V	20	28	35	42	ns
			6.0V	17	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HC4316/MM74HC4316
Quad Analog Switch with Level Translator

General Description

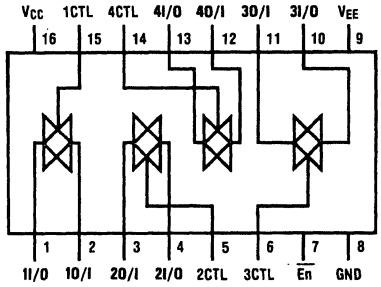
These devices are digitally controlled analog switches implemented in microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the '4316 to implement a level translator which enables this circuit to operate with 0–6V logic levels and up to ±6V analog switch levels. The '4316 also has a common enable input in addition to each switch's control which when low will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 20 ns
- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls plus a common enable

Connection Diagram

Dual-In-Line Package



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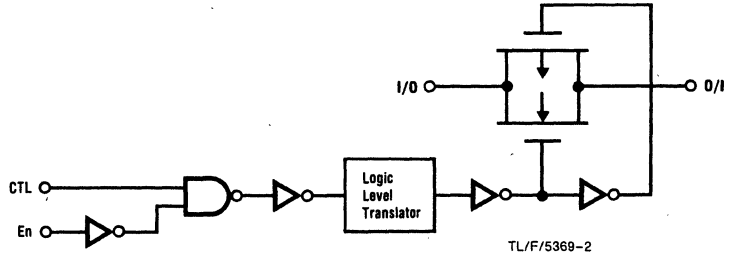
MM54HC4316/MM74HC4316

54HC4316 (J) 74HC4316 (J,N)

Truth Table

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

Logic Diagram



TL/F/5369–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
Supply Voltage(V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
R_{ON}	Minimum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=.1 mA	GND	4.5V	100				Ω
		V_{IS}=V_{CC} to GND	−4.5V	4.5V	40				Ω
		(Figure 1)	−6.0V	6.0V	30				Ω
			GND	2.0V	200				Ω
		V_{CTL}=V_{IH}, I_S=.1 mA	GND	4.5V	50				Ω
		V_{IS}=V_{CC} or GND	−4.5V	4.5V	20				Ω
		(Figure 1)	−6.0V	6.0V	15				Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL}=V_{IH}	GND	4.5V	10				Ω
		V_{IS}=V_{CC} to GND	−4.5V	4.5V	5				Ω
			−6.0V	6.0V	5				Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND			6.0V	±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS}=V_{CC} or GND	GND	5.5V	10				nA
		V_{IS}=GND or V_{CC}	−6.0V	6.0V	10				nA
		V_{CTL}=V_{IL} (Fig 2)							
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS}=V_{CC} or GND	GND	5.5V	15				nA
		V_{CTL}=V_{IH}	−6.0V	6.0V	20				nA
		(Figure 3)							
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND	GND	6.0V		2.0	20	40	μA
		I_{OUT}=0 μA	−6.0V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}−V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V–6V C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25	50	38	75	ns
			GND	4.5V	5	10	13	15	ns
			−4.5V	4.5V	4	8	10	12	ns
			−6.0V	6.0V	3	7	9	10	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	GND	2.0V	32	100	125	150	ns
			GND	4.5V	8	20	25	30	ns
			−4.5V	4.5V	6	15	19	23	ns
			−6.0V	6.0V	5	14	18	21	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		GND	2.0V	45	165	206	250	ns
			GND	4.5V	15	35	43	53	ns
			−4.5V	4.5V	10	30	37	45	ns
			−6.0V	6.0V	8	28	35	42	
f_{MAX}	Minimum Switch Frequency Response $20\log(V_I/V_O) = 3$ dB		GND	4.5V	100				MHz
			−4.5V	4.5V	120				MHz
	Cross Talk Control to Switch	(Figure 7)	−4.5V	4.5V	180				mV_{P-P}
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	−4.5V	4.5V					MHz
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input			15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND			5				pF

AC Test Circuits and Switching Time Waveforms

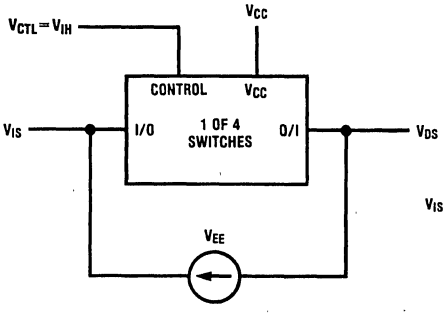


FIGURE 1. "ON" Resistance

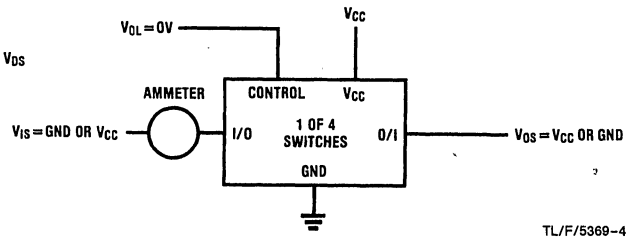


FIGURE 2. "OFF" Channel Leakage Current

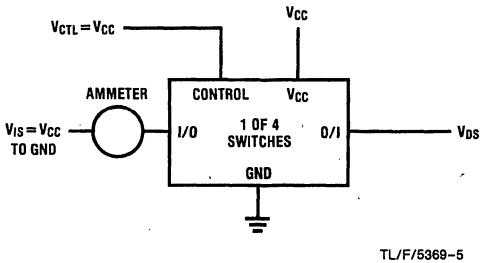


FIGURE 3. "ON" Channel Leakage Current

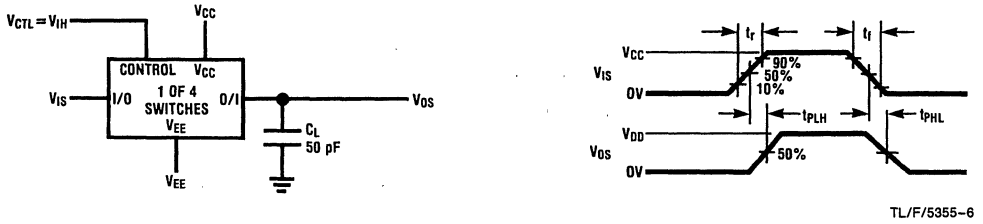


FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

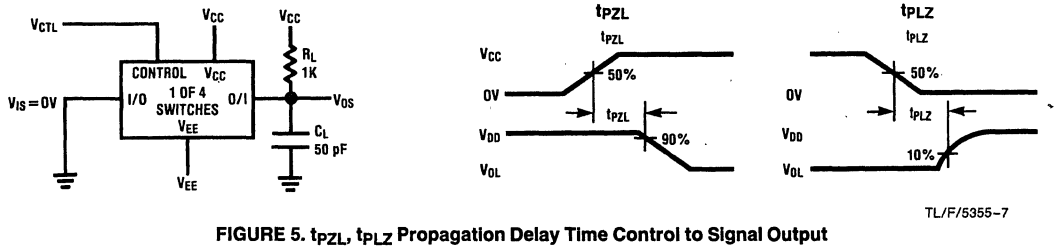


FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

4

AC Test Circuits and Switching Time Waveforms (Continued)

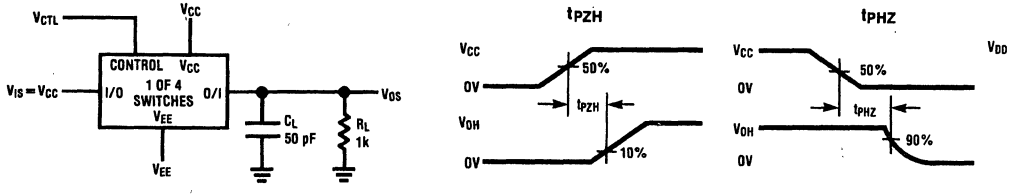


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FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

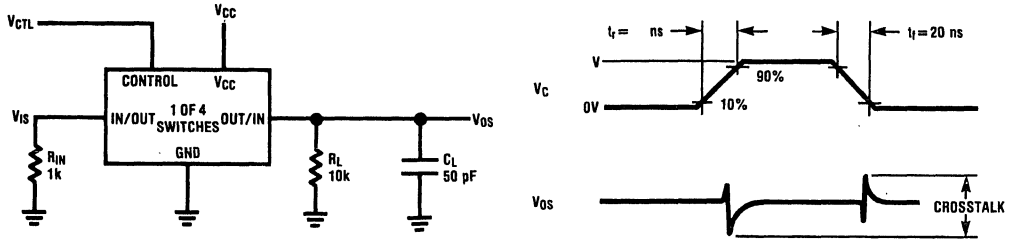

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FIGURE 7. Crosstalk: Control Input to Signal Output

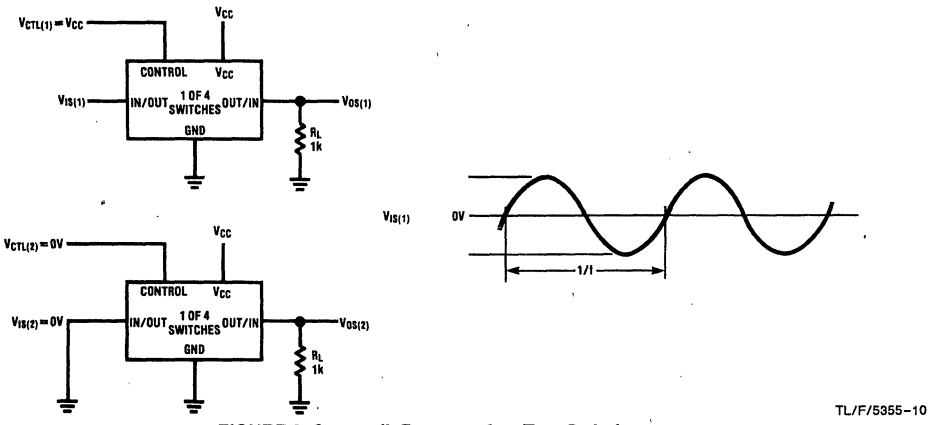

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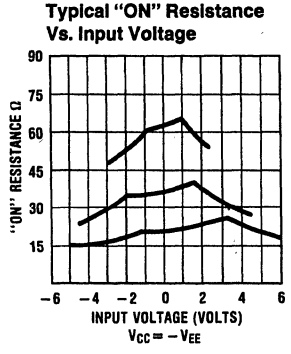
FIGURE 8: Crosstalk Between Any Two Switches

Typical Performance Characteristics



TL/F/5369–17

PRELIMINARY

National Semiconductor

MM54HC4351/MM74HC4351
8 Channel Analog Multiplexer with Latches
MM54HC4352/MM74HC4352
Dual 4 Channel Analog Multiplexer with Latches
MM54HC4353/MM74HC4353
Triple 2 Channel Analog Multiplexer with Latches

General Description

These multiplexers are digitally controlled analog switches implemented in microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. The analog channel select lines are latched to enable storage of the selected channel. This storage register is composed of flow through latches that follow the data when $\overline{LE}$ is high and latch the data when $\overline{LE}$ is taken low.

Three supply pins are provided for V_{CC}, Ground, and V_{EE}. This enables the connection of 0-5V logic signals when $V_{CC}=5V$ and an analog input range of ±5V when $V_{EE}=-5V$. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

MM54HC4351/MMHC4351: This device connects together the outputs of 8 switches, thus acheiving an 8 Channel Multiplexer. The binary code placed on the A, B, and C select lines determine which one of the eight switches in "on", and connects one of the eight inputs to the common output.

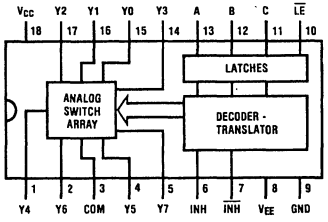
MM54HC4352/MM74HC4352: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4 channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4 channel differential multiplexer.

MM54HC4353/MM74HC4353: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of a single-pole-double throw configuration. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

Features

- Typical Switch Enable Time: 18 ns
- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Logic level translation to enable 5V logic with ±5 analog signals
- Low quiescent current: 80 μA max. (74HC)
- Matched Switch characteristics.
- Latched Select Lines to enable interface to multiplexed data buses.

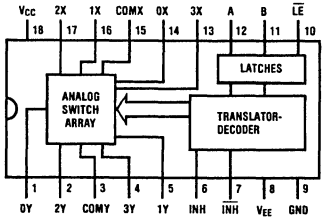
Connection Diagrams



TL/F/5372-1

MM54HC4351/MM74HC4351

54HC4351 (J) 74HC4351 (J,N)



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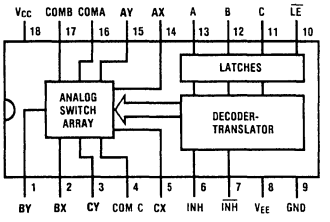
MM54HC4352/MM74HC4352

54HC4352 (J) 74HC4352 (J,N)



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MM54HC4353/MM74HC4353

54HC4353 (J) 74HC4353 (J,N)

4

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
Supply Voltage(V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T=25°C	74HC T=−40 to 85°C	54HC T=−55 to 125°C	Units
					Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=.1 mA V_{IS}=V_{CC} to GND (Figure 1)	GND	4.5V	40				Ω
			−4.5V	4.5V	30				Ω
			−6.0V	6.0	20				Ω
		V_{CTL}=V_{IH}, I_S=.1 mA V_{IS}=V_{CC} or GND (Figure 1)	GND	2.0V	100				Ω
			GND	4.5V	40				Ω
			−4.5V	4.5V	20				Ω
			−6.0V	6.0V	15				Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL}=V_{IH} V_{IS}=V_{CC} to GND	GND	4.5V	10				Ω
			−4.5V	4.5V	5				Ω
			−6.0V	6.0V	5				Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND		6.0V		±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS}=V_{CC} or GND V_{IS}=GND or V_{CC} V_{CTL}=V_{IL} (Fig. 2)	GND	6.0V	15				nA
			−6.0V	6.0V	20				nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS}=V_{CC} or GND V_{CTL}= V_{IH} (Figure 3)	GND	6.0V	15				nA
			−6.0V	6.0V	20				nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	GND	6.0V		8.0	80	160	μA
			−6.0V	6.0V		16	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

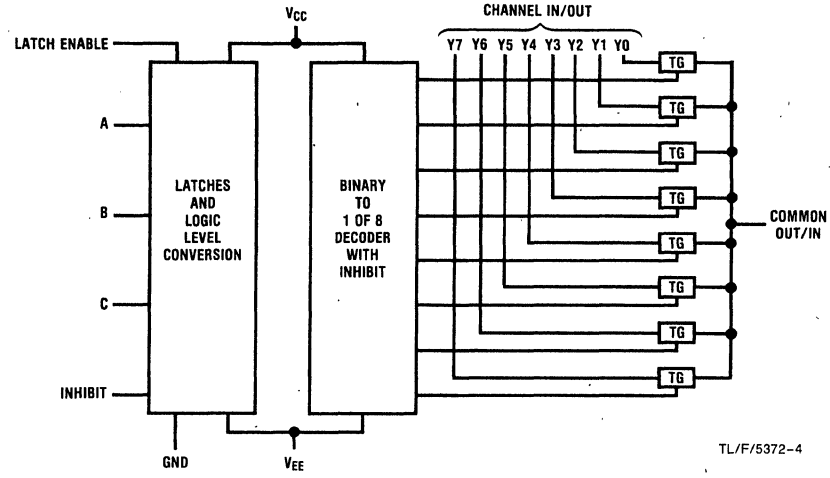
Note 5: At supply voltages (V_{CC}-V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V to −6V, C_L = 50 pF, (unless otherwise specified)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25			ns
			GND	4.5V	5			ns
			−4.5V	4.5V	4			ns
			−6.0V	6.0V	3			ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	GND	2.0V	92			ns
			GND	4.5V	18			ns
			−4.5V	4.5V	16			ns
			−6.0V	6.0V	15			ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		GND	2.0V	65			ns
			GND	4.5V	20			ns
			−4.5V	4.5V	18			ns
			−6.0V	6.0V	16			ns
t_S	Maximum Setup Time, Data to LE			2.0V		100	125	150	ns
				4.5V		20	24	28	ns
				6.0V		17	21	24	ns
t_H	Maximum Hold Time, LE to Data			2.0V		0	0	0	ns
				4.5V		0	0	0	ns
				6.0V		0	0	0	ns
f_{MAX}	Minimum Switch Frequency Response 20log(V_I/V_O) = −3 dB	(Figure 6)	GND	4.5V	100				MHz
			−4.5V	4.5V	120				MHz
	Cross Talk Control to Switch	(Figure 7)	−4.5V	4.5V	180				mV_{PP}
	Cross Talk Between Any Two Switches (Frequency at −50 dB)	(Figure 8)	−4.5V	4.5V					MHz
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input			15				pF
		'4351 Common			90				
		'4352 Common			45				
		'4353 Common			30				
C_{IN}	Maximum Feedthrough Capacitance				5				pF

Logic Diagrams



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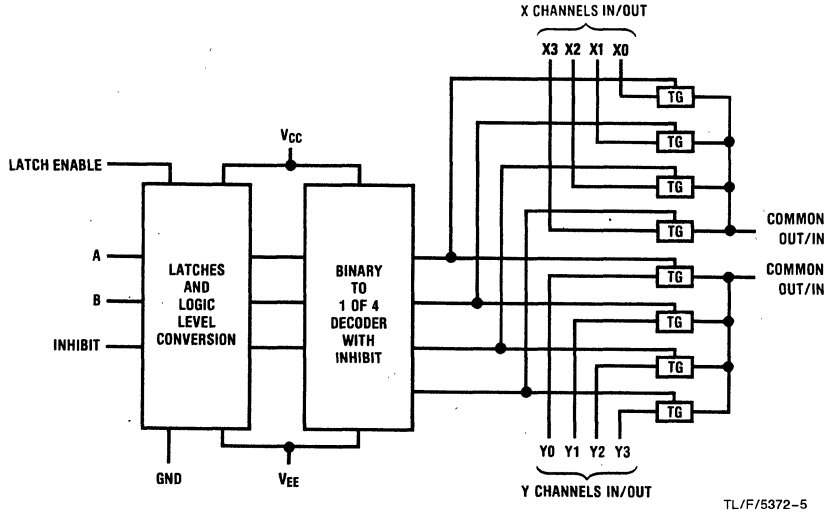

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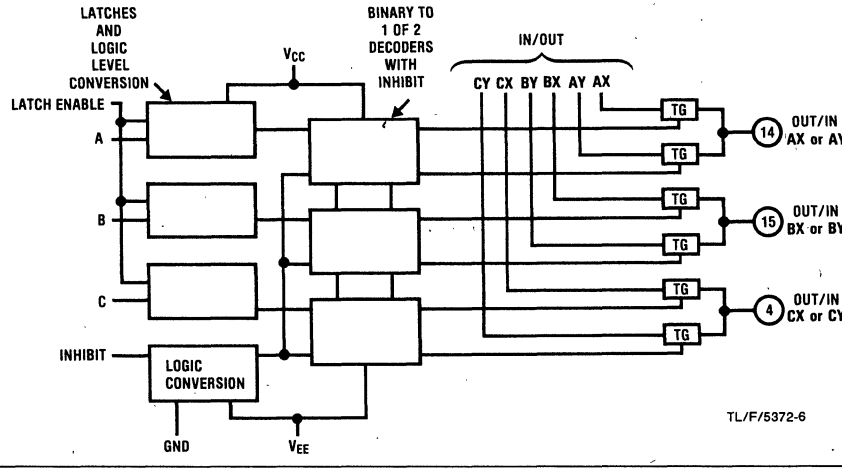

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Logic Diagrams (Continued)

'HC4351

Inh	$\overline{Inh}$	$\overline{LE}$	C	B	A	"On" Channel
H	X	X	X	X	X	None
X	L	X	X	X	X	None
L	H	H	L	L	L	Y0
L	H	H	L	L	H	Y1
L	H	H	L	H	L	Y2
L	H	H	L	H	H	Y3
L	H	H	H	L	L	Y4
L	H	H	H	L	H	Y5
L	H	H	H	H	L	Y6
L	H	H	H	H	H	Y7
L	H	L	X	X	X	Last Selected Channel "On"
X	X	↓	X	X	X	Selected Channel Latched

'HC4352

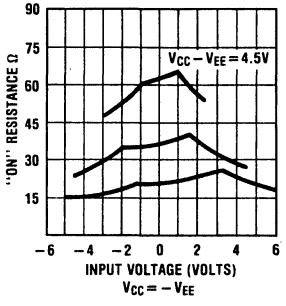
Inh	$\overline{Inh}$	$\overline{LE}$	B	A	"On" Channels	
					X	Y
H	X	X	X	X	None	
X	L	X	X	X	None	
L	H	H	0	0	0X	0Y
L	H	H	0	1	1Y	1Y
L	H	H	1	0	2Y	2Y
L	H	H	1	1	3Y	3Y
L	H	L	X	X	Last Selected Channels "On"	
X	X	↓	X	X	Selected Channels Latched	

'HC4353

Inh	$\overline{Inh}$	$\overline{LE}$	C	B	A	"On" Channels		
						C	B	A
H	X	X	X	X	X	None		
X	L	X	X	X	X	None		
L	H	H	L	L	L	CX	BX	AX
L	H	H	L	L	H	CX	BX	AY
L	H	H	L	H	L	CX	BY	AX
L	H	H	L	H	H	CX	BY	AY
L	H	H	H	L	L	CY	BX	AX
L	H	H	H	L	H	CY	BX	AY
L	H	H	H	H	L	CY	BY	AX
L	H	H	H	H	H	CY	BY	AY
L	H	L	X	X	X	Last Selected Channels "On"		
X	X	↓	X	X	X	Selected Channels Latched		

Typical Performance Characteristics

Typical "On" Resistance vs. Input Voltage



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AC Test Circuits and Switching Time Waveforms

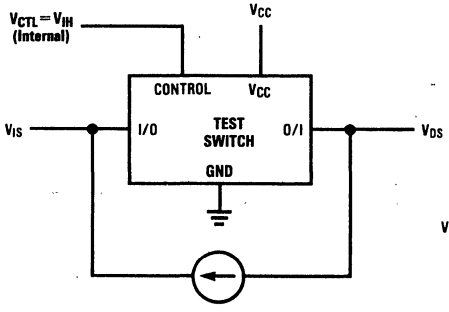

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FIGURE 1. "ON" Resistance

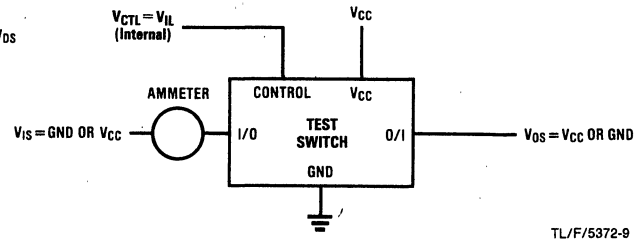

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FIGURE 2. "OFF" Channel Leakage Current

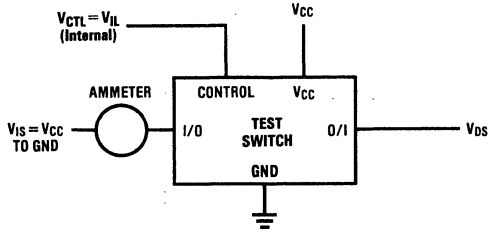

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FIGURE 3. "ON" Channel Leakage Current

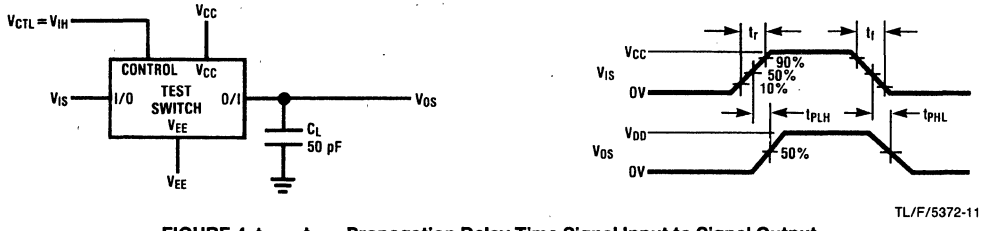

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FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

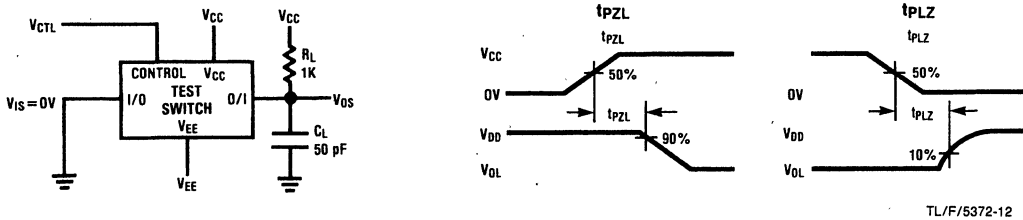

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FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

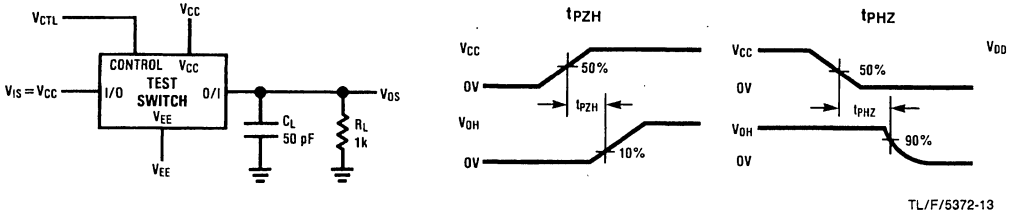


FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

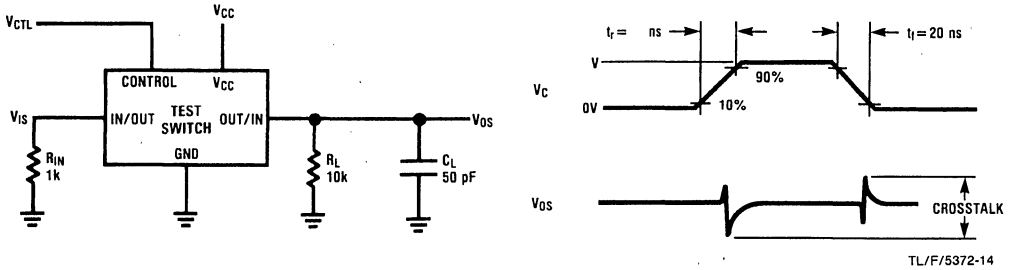


FIGURE 7. Crosstalk: Control Input to Signal Output

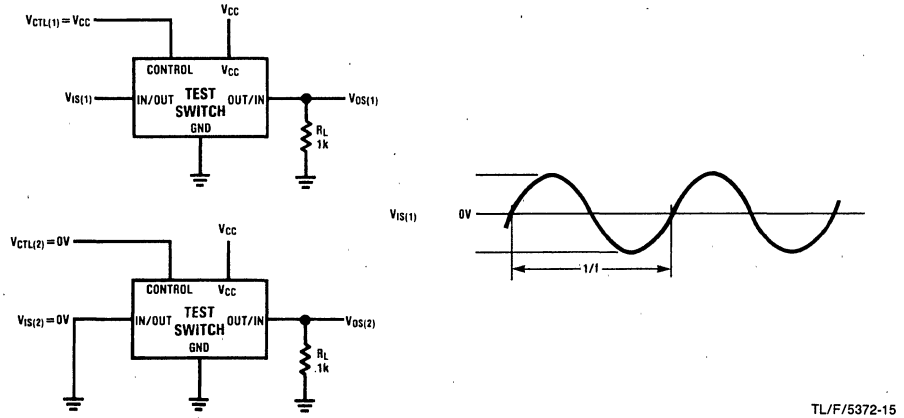


FIGURE 8: Crosstalk Between Any Two Switches

National Semiconductor

PRELIMINARY

MM54HC4511/MM74HC4511
BCD-to-Seven Segment Latch/Decoder/Driver

General Description

This high speed latch/decoder/driver utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

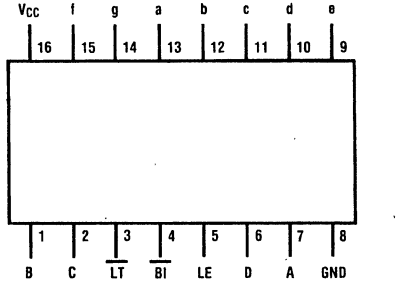
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Latch Storage of Input Data
- Blanking Input
- Lamp Test Input
- Low Power Consumption Characteristics of CMOS Devices
- Wide Operating Voltage Range: 2 to 6 Volts
- Low Input Current: 1 μA Maximum
- Low Quiescent Current: 80 μA Maximum Over Full Temperature Range (74 series)

Connection Diagram

Dual-In-Line Package



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MM54HC4511/MM74HC4511

54HC4511 (J) 74HC4511 (J,N)

Truth Table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
x	x	0	x	x	x	x	1	1	1	1	1	1	1	8
x	0	1	x	x	x	x	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	x	x	x	x				*				*

x = Don't care

* = Depends upon the BCD code applied during the 0 to 1 transition of LE.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 7.5$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 9.75$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Inputs A thru D to any Output		60	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From $\overline{BI}$ to any Output		60	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From $\overline{LT}$ to any Output		60	120	ns
t_S	Minimum Set Up Time Inputs A thru D to LE		10	20	ns
t_H	Minimum Hold Time Inputs A thru D to LE		−3	0	ns
t_W	Minimum Pulse Width for LE			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Inputs A thru D to any Output	LE=0V, $\overline{LT}=V_{CC}$, $\overline{BI}=V_{CC}$	2.0V	300	600	756	894	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{BI}$ to any Output	$\overline{LT}=V_{CC}$	2.0V	300	600	756	894	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{LT}$ to any Output	$\overline{BI}=0V$	2.0V	300	600	756	894	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
t_S	Minimum Set Up Time Inputs A thru D to LE		2.0V		100	126	149	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Inputs A thru D to LE		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width for LE		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

INPUTS

A, B, C, D (Pins 7, 1, 2, 6)—BCD data inputs. A (pin 7) is the least-significant data bit and D (pin 6) is the most significant bit. Hexadecimal data A–F at these inputs will cause the outputs to assume a logic low, offering an alternate method of blanking the display.

OUTPUTS

a–g—Decoded, buffered outputs. These outputs, unlike the 4511, have CMOS drivers, which will produce typical CMOS output voltage levels.

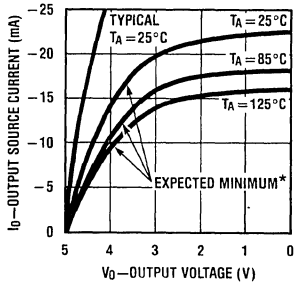
CONTROLS

$\overline{BI}$ (Pin 4)—Active-low display blanking input. A logic low on this input will cause all outputs to be held at a logic low, thereby blanking the display. LT is the only input that will override the BI input.

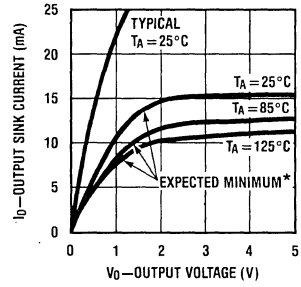
$\overline{LT}$ (Pin 3)—Active-low lamp test. A low logic level on this input causes all outputs to assume a logic high. This input allows the user to test all segments of a display, with a single control input. This input is independent of all other inputs.

LE (Pin 5)—Latch enable input. This input controls the 4-bit transparent latch. A logic high on this input latches the data present at the A, B, C and D inputs; a logic low allows the data to be transmitted through the latch to the decoder.

Output Characteristics ($V_{CC}=5V$)



TL/F/5373–2



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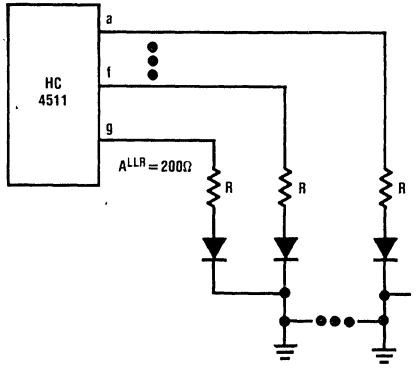
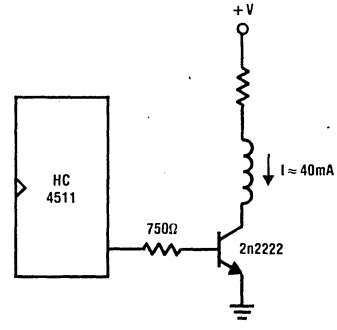
*The expected minimum curves are not guarantees, but are design aids.

Typical Applications



TL/F/5373–4

Typical Common Cathode LED Connection

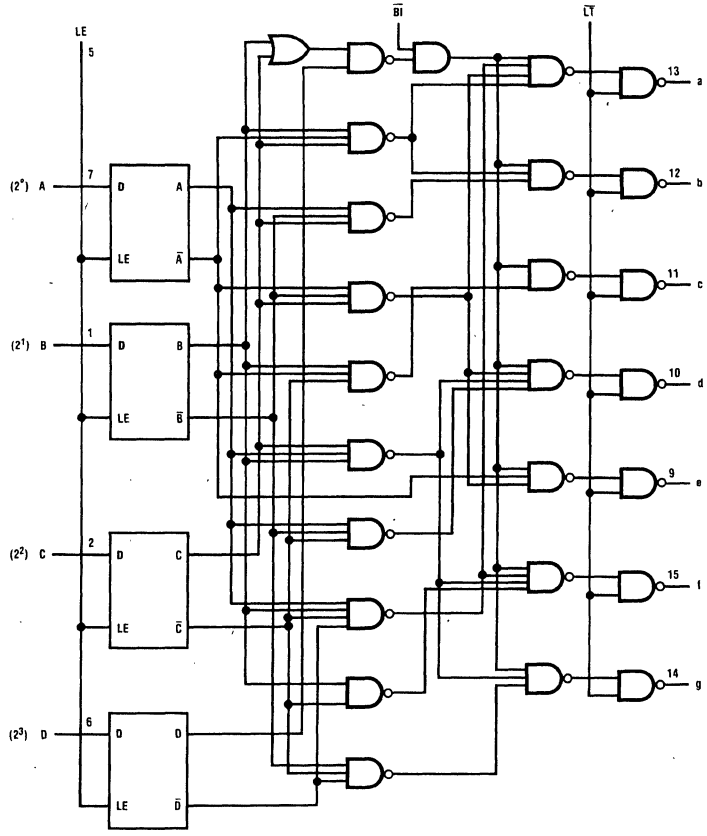


TL/F/5373–5

Incandescent Bulb Driving Circuit

Logic Diagram

'HC4511



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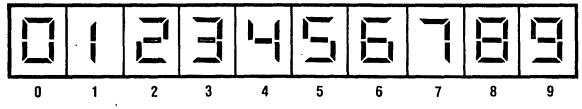
Display



TL/F/5373–7

Segment Identification

TL/F/5373–8

National Semiconductor

PRELIMINARY

MM54HC4514/MM74HC4514
4-to-16 Line Decoder with Latch

General Description

This utilizes microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS decoder, which is well suited to memory address decoding or data routing application. It possesses high noise immunity and low power dissipation usually associated with CMOS circuitry, yet speeds comparable to low power Schottky TTL circuits. It can drive up to 10 LS-TTL loads.

The MM54HC4514/MM74HC4514 contain a 4-to-16 line decoder and a 4-bit latch. The latch can store the data on the select inputs, thus allowing a selected output to remain high even though the select data has changed. When the LATCH ENABLE input to the latches is high the outputs will change with the inputs. When LATCH ENABLE goes low the data on the select inputs is stored in the latches. The four select inputs determine which output will go high provided the INHIBIT input is low. If the INHIBIT input is high all outputs are held low thus disabling the decoder.

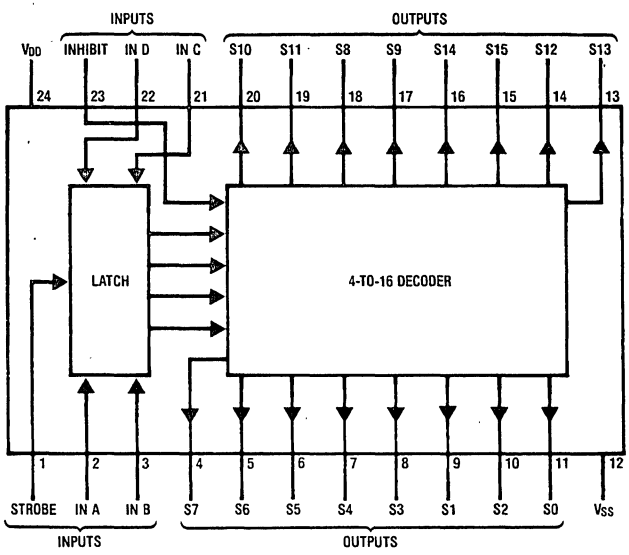
The MM54HC4514/MM74HC4514 is functionally and pinout equivalent to the CD4514BM/CD4514BC and the MC1451BA/MC1451BC. All inputs are protected against damage due to static discharge diodes from V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Low quiescent power: 80 μA maximum (74HC series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC series)

Connection Diagram

Dual-In-Line Package



TL/F/5215–1

MM54HC4514/MM74HC4514

54HC4514 (J) 74HC4514 (J,N)

Truth Table

LE	Inhibit	Data Inputs D	C	B	A	Selected Output High
H	L	L	L	L	L	S0
H	L	L	L	L	H	S1
H	L	L	L	H	L	S2
H	L	L	L	H	H	S3
H	L	L	H	L	L	S4
H	L	L	H	L	H	S5
H	L	L	H	H	L	S6
H	L	L	H	H	H	S7
H	L	H	L	L	L	S8
H	L	H	L	L	H	S9
H	L	H	L	H	L	S10
H	L	H	L	H	H	S11
H	L	H	H	L	L	S12
H	L	H	H	L	H	S13
H	L	H	H	H	L	S14
H	L	H	H	H	H	S15
X	H	X	X	X	X	All Outputs = 0
L	L	X	X	X	X	Latched Data

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay Data to Output		18	30	ns
t_{PLH}	Maximum Propagation Delay Data to Output		24	45	ns
t_{PHL}	Maximum Propagation Delay LE to Output		18	30	ns
t_{PLH}	Maximum Propagation Delay LE to Output		24	45	ns
t_{PHL}	Maximum Propagation Delay Inhibit to Output		16	30	ns
t_{PLH}	Maximum Propagation Delay Inhibit to Output		18	30	ns
t_S	Minimum Set Up Time, Date to LE			20	ns
t_H	Minimum Hold Time, LE to Data			0	ns
t_H	Minimum Pulse Width, Latch Enable			16	ns

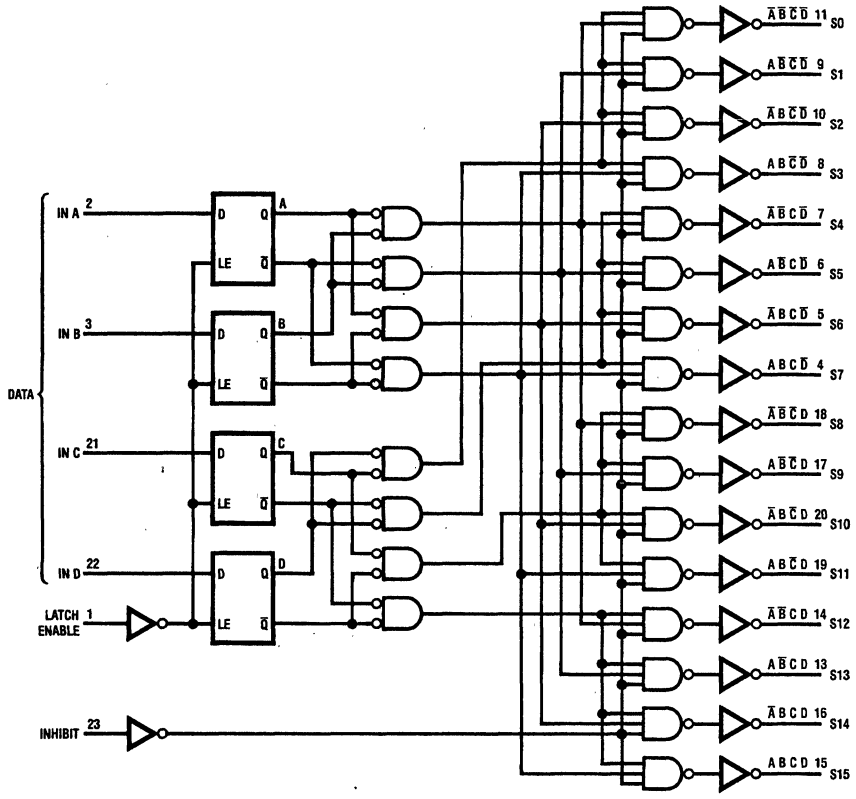
AC Electrical Characteristics $V_{CC}=2.0V-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$		Units
				Typ	Guaranteed Limits				
t_{PHL}	Maximum Propagation Delay Data to Output		2.0V	80	175		220	263	ns
			4.5V	18	35		44	53	ns
			6.0V	16	30		38	45	ns
t_{PLH}	Maximum Propagation Delay Data to Output		2.0V	120	250		312	375	ns
			4.5V	27	50		65	75	ns
			6.0V	22	43		53	65	ns
t_{PHL}	Maximum Propagation Delay LE to Output		2.0V	80	175		220	263	ns
			4.5V	19	35		44	53	ns
			6.0V	17	30		38	45	ns
t_{PLH}	Maximum Propagation Delay LE to Output		2.0V	120	250		312	375	ns
			4.5V	27	50		65	75	ns
			6.0V	22	43		53	65	ns
t_{PHL}	Maximum Propagation Delay Inhibit to Output		2.0V	70	175		220	263	ns
			4.5V	18	35		44	53	ns
			6.0V	16	30		38	45	ns
t_{PLH}	Maximum Propagation Delay Inhibit to Output		2.0V	80	175		220	263	ns
			4.5V	19	35		44	53	ns
			6.0V	17	30		38	45	ns
t_S	Minimum Set Up Time, Data to LE		2.0V		100		125	150	ns
			4.5V		20		25	30	ns
			6.0V		17		21	25	ns
t_H	Minimum Hold Time, LE to Data		2.0V		0		0	0	ns
			4.5V		0		0	0	ns
			6.0V		0		0	0	ns
t_W	Minimum Pulse Width, Latch Enable		2.0V		80		100	120	ns
			4.5V		16		20	24	ns
			6.0V		14		17	20	ns
C_{PD}	Power Dissipation Capacitance								pF
C_{IN}	Maximum Input Capacitance			5	10		10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5215–2

National Semiconductor

MM54HC4538/MM74HC4538 Dual Retriggerable Monostable Multivibrator

General Description

The MM54HC4538/MM74HC4538 high speed monostable multivibrators (one shots) are implemented in micro-CMOS™ Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

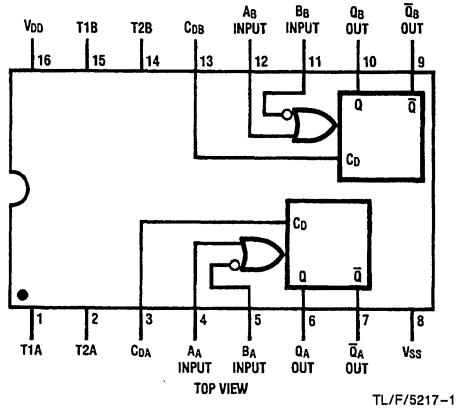
Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC4538 is retriggerable. That is, it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: PW = 0.7(R)(C) where PW is in seconds, R is in Ohms, and C is in Farads. This device is pin compatible with the CD4528, and the CD4538 one shots. All inputs are protected from damage due to static discharge by diodes to Vcc and ground.

Features

- Schmitt trigger on A and B inputs
- Wide power supply range: 2–6V
- Typical Trigger Propagation Delay: 32 ns
- Fanout of 10 LS-TTL loads (74HC)
- Low Input current: 1 μA max

Connection Diagram



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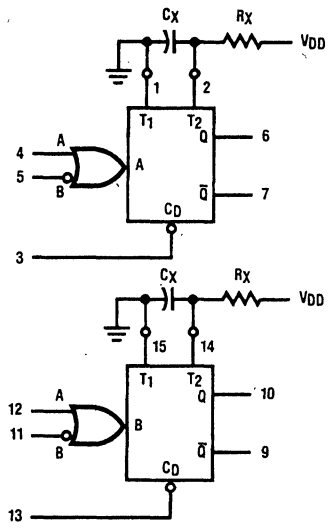
MM54HC4538/MM74HC4538

54HC4538 (J) 74HC4538 (J,N)

Block Diagram



RX AND CX ARE EXTERNAL COMPONENTS

TL/F/5217–2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transistion from Low to High
↓ = Transistion from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage(V_{CC})	−0.5 to +7.0V
DC Input Voltage(V_{IN})	−1.5 to Vcc+1.5V
DC Output Voltage(V_{OUT})	−0.5 to Vcc+0.5V
Clamp Diode Current(I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin(I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin(I_{CC})	±50 mA
Storage Temperature Range(T_{STG})	−65°C to +150°C
Power Dissipation(P_D) (Note 3)	500 mW
Lead Temperature(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (Reset only)			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V		3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤ 4 mA	4.5V		0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 2, 14)	V_{IN}=V_{CC} or GND	6.0V		±0.5	±5.0	±10	μA
I_{IN}	Maximum Input Current (All other pins)	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA Pins 2 and 14=0.5V_{CC}	6.0V	100	150	250	400	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C Ceramic "J" Package: −12mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°$ C, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Propagation Delay A, or B to Q		23	45	ns
t_{PHL}	Maximum Propagation Delay A, or B to $\overline{Q}$		26	50	ns
t_{PHL}	Maximum Propagation Delay Clear to Q		23	45	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		26	45	ns
t_W	Minimum Pluse Width A, B or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns (Unless otherwise specified)

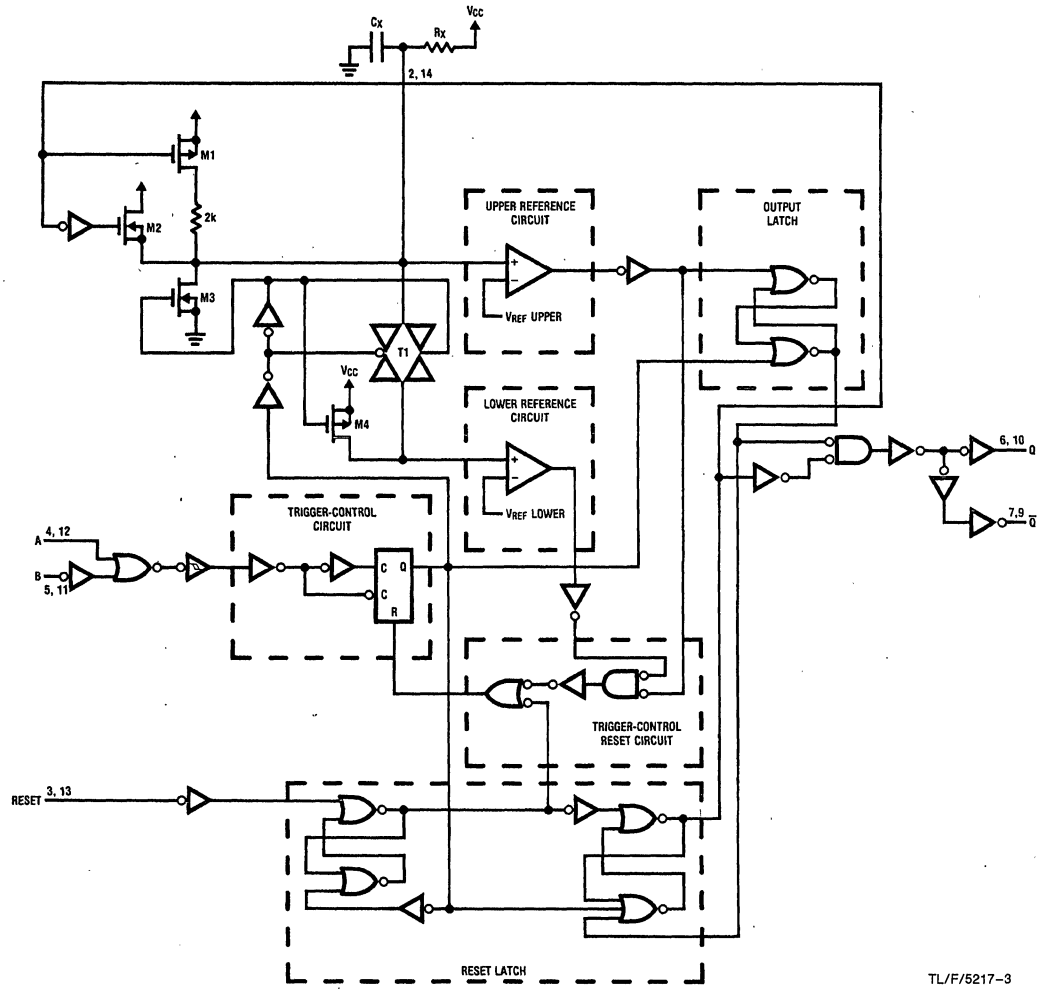
Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay A, or B to Q			2.0V 4.5V 6.0V	100 25 21	250 50 43	315 63 54	373 75 63	ns ns ns
t_{PHL}	Maximum Propagation Delay A, or B to $\overline{Q}$			2.0V 4.5V 6.0V	110 28 23	275 55 47	347 69 59	410 82 70	ns ns ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V 4.5V 6.0V	100 25 21	250 50 43	315 63 54	373 75 63	ns ns ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V 4.5V 6.0V	110 28 23	275 55 47	347 69 59	410 82 70	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V 4.5V 6.0V	30 10 8	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time (Reset only)			2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
t_W	Minimum Pluse Width A, B, Clear			2.0V 4.5V 6.0V		80 16 14	101 20 17	119 24 20	ns ns ns
t_{WQ}	Output Pulse Width	Cx=12 pF Rx=1 kΩ	Min	3.0V 5.0V	283 147	190 120			ns ns
			Max	3.0V 5.0V	283 147	400 185			ns ns
t_{WQ}	Output Pulse Width	Cx=100 pF Rx=10 kΩ	Min	3.0V 5.0V	1.2 1.0				μs μs
			Max	3.0V 5.0V	1.2 1.0				μs μs
t_{WQ}	Output Pulse Width	Cx=1000 pF Rx=10 kΩ	Min	3.0V 5.0V	10.5 10.0	9.4 9.3			μs μs
			Max	3.0V 5.0V	10.5 10.0	11.6 11.7			μs μs
C_{IN}	Maximum Input Capacitance (Pins 2 & 14)				25				pF
C_{IN}	Maximum Input Capacitance (Other Inputs)				5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per one shot)			150				pF
Δt_{WQ}	Pulse Width Match Between Circuits in Same Package				±1				%

Note 5: C_{PD} determines the no load dynamic consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = V_{CC} f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

4

Logic Diagram



Circuit Operation

The 'HC4538 operates as follows (refer to logic diagram). In the quiescent state, the external timing capacitor, C_X, is charged to V_{CC}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{REF} Lower = ⅓ V_{CC}). C_X then charges, through R_X, back up to the upper reference voltage (V_{REF} Upper = ⅔ V_{CC}), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic diagram and the timing diagram.

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in logic diagram).

Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, timing diagram).

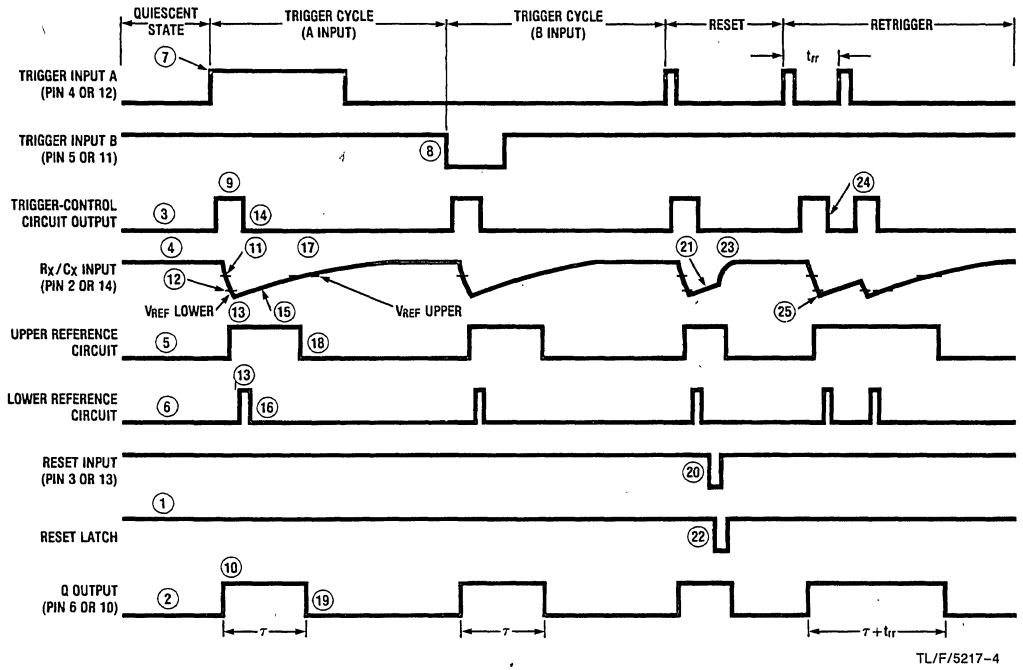
The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{CC} (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has V_{CC} at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The 'HC4538 is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Function Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

Timing Diagram



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The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the 'HC4538 to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator). Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{CC}, with a time constant $t = R_X C_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the 'HC4538 to a low state (#19), and completing the time-out cycle.

RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the 'HC4538 to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{CC} (#23) to await the next trigger signal.

RETRIGGER OPERATION

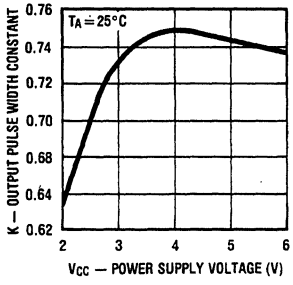
In the retriggerable mode, the 'HC4538 may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

$$t_{rr}(ns) \cong 72 + \frac{V_{CC}(volts) \bullet C_X(pF)}{30.5}, \text{ at room temperature}$$

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the HC4538 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \bullet C_X/(30\ mA)$. For example, if $V_{CC} = 5V$ and $C_X = 15\ \mu F$, the V_{CC} supply must turn off no faster than $t = (15V) \bullet (15\ \mu F)/30\ mA = 2.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{CC} to zero volts occurs, the HC4538 may sustain damage. To avoid this possibility, use an external clamping diode, D_X, connected from V_{CC} to the C_X pin.



TL/F/5217–5

National Semiconductor

MM54HC4543/MM74HC4543 BCD-to-7 Segment Latch/ Decoder/Driver for Liquid Crystal Displays

General Description

The MM54HC4543/MM74HC4543 BCD-to-7 segment latch/decoder/driver utilize microCMOS™ Technology, 3.5 micron silicon gate P-well CMOS, and can be used either as a high speed decoder or as a display driver. This circuit contains a 4-bit latch, BCD-to-7 segment decoder, and 7 output drivers. Data on the input pins flow through to the output when the LATCH ENABLE (LE) is high and is latched on the high to low transition of the LE input. The PHASE input (PH) controls the polarity of the 7 segment outputs. When PH is low the outputs are true 7 segment, and when PH is high the outputs are inverted 7 segment. When the PHASE input is driven by a liquid crystal display (LCD) backplane waveform the segment pins output the correct segment waveform for proper LCD AC drive voltages.

In addition a BLANKING INPUT (BI) is provided, which will blank the display.

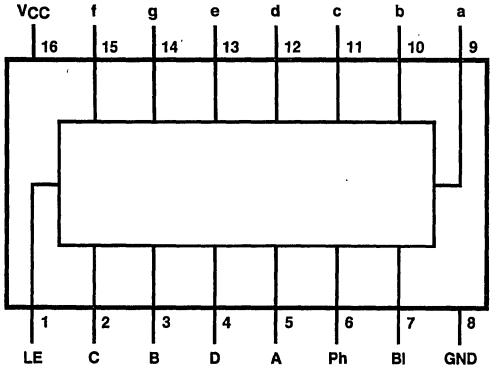
The MM54HC4543/MM74HC4543 are functionally and pinout equivalent to the CD4543BC/CD4543BM and the MC14543BA/MC14543BC. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 60 ns
- Supply voltage range: 2–6V
- Maximum input current: 1 μA
- Maximum quiescent supply current: 80 μA (74HC)
- Display blanking
- Low dynamic power consumption

Connection Diagram

Dual-In-Line Package



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MM54HC4543/MM74HC4543

54HC4543 (J) 74HC4543 (J,N)

Truth Table

Inputs							Outputs							
LE	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	**							**
†	†	H	†				Inverse of Output Combinations Above							Display as above

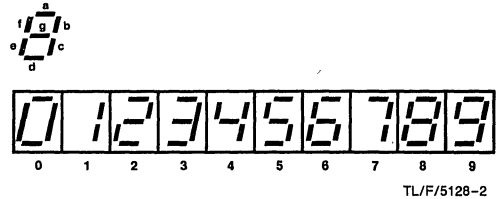
X—Don't care

† = Same as above combinations

* = For liquid crystal readouts, apply a square wave to Ph.

** = Depends upon the BCD code previously applied when LE—H

Display Format



TL/F/5128–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤0.4 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤0.52 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤0.4 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤0.52 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, BI, Ph to Output		60	100	ns
t_S	Minimum Set Up Time LE to Data			20	ns
t_H	Minimum Hold Time Data to LE			10	ns
t_W	Minimum LE Pulse Width			16	ns

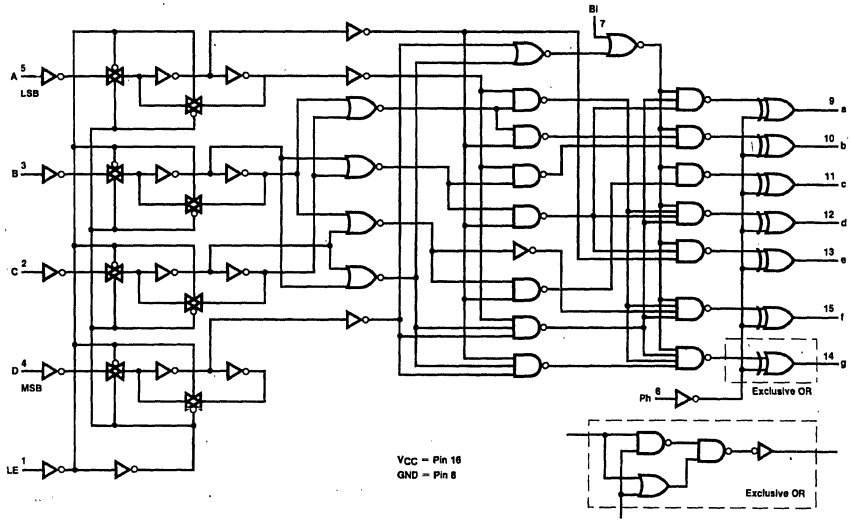
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, Ph, BI to Output		2.0V	300	600	760	895	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
t_S	Minimum Set Up Time LE to Data		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Data to LE		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_W	Minimum LE Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

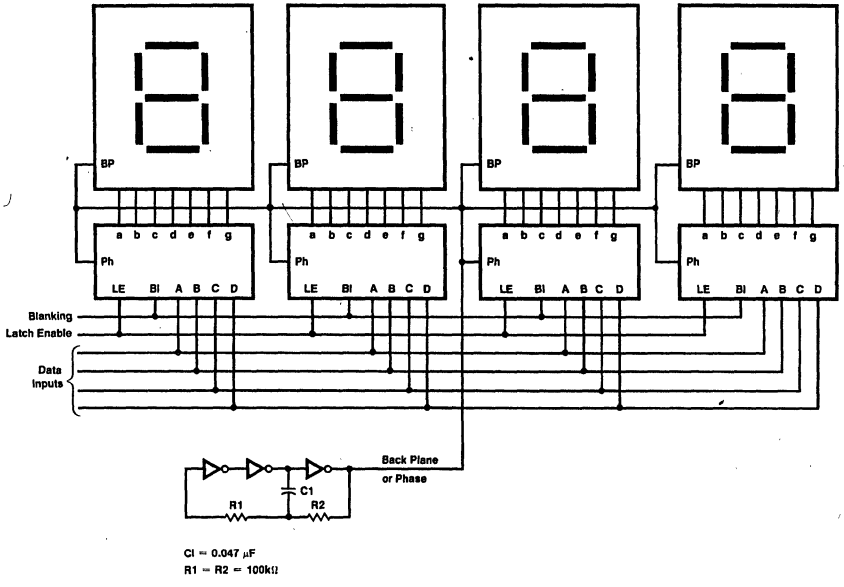
Logic Diagram



TL/F/5128–3

Typical Applications

4 Digit LCD Display



TL/F/5128–4

National Semiconductor

PRELIMINARY

MM54HC4560/MM74HC4560 4 Bit BCD Adder

General Description

This silicon gate CMOS adder performs the addition at LS-TTL speeds of two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

This device can also subtract when one set of inputs is 9's Complemented

All inputs and outputs are active high. The carry input for the least significant digit is connected to GND for no carry in.

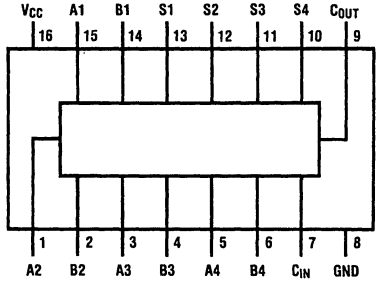
All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Wide supply range: 2V to 6V
- Low quiescent consumption: 8 μA at 25°C
- Low input current: <1 μA
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5374–1

MM54HC4560/MM74HC4560

54HC4560 (J) 74HC4560 (J,N)

Truth Table*

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{IN}	C_{OUT}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	1	1	1	0	0	1	1	1	1	0	0	1

*Partial truth table to show logic operation for representative input values

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	300°C

Operating Conditions

		Min	Max	Units
Supply Voltage(V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temperature Range(T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A or B to Sn			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A or B to C_{OUT}			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_{IN} to C_{OUT}			25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_{IN} to Sn			25	ns

AC Electrical Characteristics

$C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C		54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A or B to Sn		2.0V	75	175	219	262	ns
			4.5V	21	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A or B to C_{OUT}		2.0V	73	175	219	262	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_{IN} to C_{OUT}		2.0V	63	150	189	225	ns
			4.5V	18	30	38	45	ns
			6.0V	16	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_{IN} to Sn		2.0V	63	150	189	225	ns
			4.5V	18	30	38	45	ns
			6.0V	16	26	32	39	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	μF
C_{PD}	Power Dissipation Capacitance	(Note 5)						μF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

4

Section 5

MM54HCT/MM74HCT
Data Sheets

National Semiconductor

PRELIMINARY

MM54HCT00/MM74HCT00 Quad 2 Input NAND Gate

General Description

The MM54HCT00/MM74HCT00 are logic functions fabricated using microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pinout compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

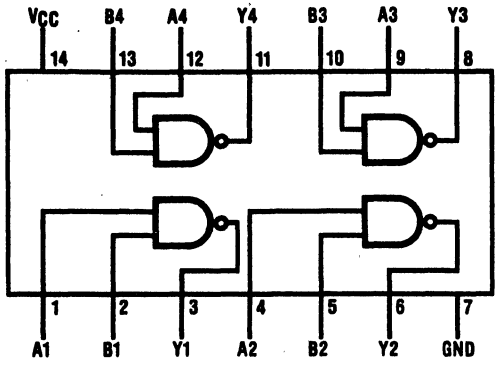
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 8 ns (typ)
- Low power: 10 μW at DC, 2.5 mW at > 5 MHz
- High fan-out, 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5295–1

MM54HCT00/MM74HCT00

54HCT00 (J) 74HCT00 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$, (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	15	ns

AC Electrical Characteristics $V_{CC}=5.0V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF, (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	18	24	27	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HCT04/74HCT04 Hex Inverter

General Description

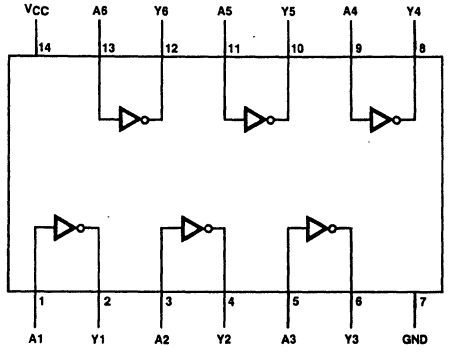
The MM54HCT04/74HCT04 are logic functions fabricated using microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS - low quiescent power and wide power supply range, but are input and output characteristic as well as pin-out compatible with standard DM54LS/74LS devices. The MM54HCT04/MM74HCT04, triple buffered, inverting hex inverters, feature low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: T_{PLH}, T_{PHL} = 8 ns (typ)
- Low power: 10 μW at DC, 2.5 mW at 5 MHz
- High fan-out: ≥ 10 LS loads
- Inverting, triple buffered

Connection Diagram



TL/F/5296–1

MM54HCT04/MM74HCT04

54HCT04 (J) 74HCT04 (J,N)

5

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note: 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics

$V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$, (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	15	ns

AC Electrical Characteristics

$V_{CC}=5.0V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF, (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C		54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	18	24	27	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power comsumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

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National Semiconductor

PRELIMINARY

MM54HCT05/MM74HCT05 Hex Inverter (Open Drain)

General Description

The MM54HCT05/MM74HCT05 are logic functions fabricated using microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are also input-output characteristically and pin-out compatible with standard DM54LS/DM74LS logic families. The MM54HCT05/MM74HCT05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

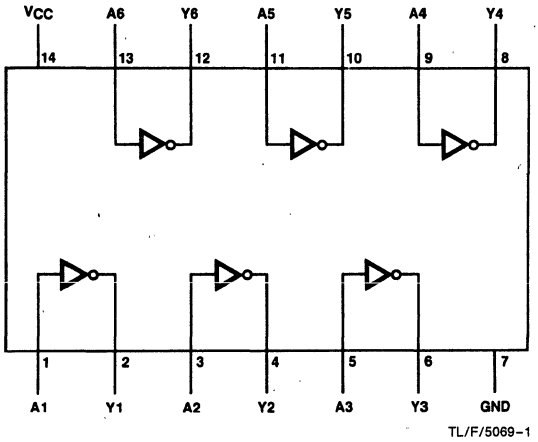
All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Open drain for wire-NOR function
- LS-TTL pinout and threshold compatible
- Fan-out of 10 LS-TTL loads
- Typical propagation delays:
  - t_{PLH} (with 1 kΩ resistor) 10 ns
  - t_{PHL} (with 1 kΩ resistor) 8 ns

Connection Diagram

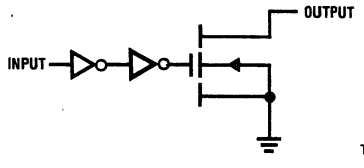


TL/F/5069–1

MM54HCT05/MM74HCT05

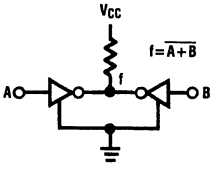
54HCT05 (J) 74HCT05 (J,N)

Logic Diagram



TL/F/5358–2

Typical Application



TL/F/5358–3

MM54HCT05/MM74HCT05

Note: Can be extended to more than 2 inputs.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC}=5V ±10%, unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}, R_L=1 kμ $\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC} 0.1	V_{CC} 0.1	V_{CC} 0.1	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V $\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{LKG}	Minimum High Level Output Leakage Current	V_{IN}=V_{IH} or VIL, V_{OUT}=V_{CC}		0.5	5.0	10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0vA		2.0	20	40	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=15 pF, t_r=t_f=6 ns unless otherwise noted.

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay	R_L=1 kΩ	8	15	ns
t_{PLH}	Maximum Propagation Delay	R_L=1 kΩ	9	16	ns

AC Electrical Characteristics V_{CC}=5V ±10%, C_L=50 pF, t_r=t_f=6 ns unless otherwise specified

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay	R_L=1 kΩ	10	18	24	27	ns
t_{PLH}	Maximum Propagation Delay	R_L=1 kΩ	12	20	25	30	ns
t_{THL}	Maximum Output Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) R_L=∞		20			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}, and the no load dynamic current consumption, I_S=C_{PD} V_{CC} f+I_{CC}.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns unless otherwise noted.

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay	$R_L=1\ k\Omega$	8	15	ns
t_{PLH}	Maximum Propagation Delay	$R_L=1\ k\Omega$	9	16	ns

AC Electrical Characteristics

$V_{CC}=5V\ \pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$		Units
			Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay	$R_L=1\ k\Omega$	10	18	24	27	ns
t_{PLH}	Maximum Propagation Delay	$R_L=1\ k\Omega$	12	20	25	30	ns
t_{THL}	Maximum Output Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) $R_L=\infty$		20			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

5

AC Electrical Characteristics $V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$, (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	15	ns

AC Electrical Characteristics $V_{CC}=5.0V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF, (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	17	21	24	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

PRELIMINARY

National Semiconductor

MM54HCT74/MM74HCT74
Dual D Flip-Flop with Preset and Clear

General Description

The MM54HCT74/MM74HCT74 utilizes microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS, to achieve operation speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 54HCT/74HCT logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

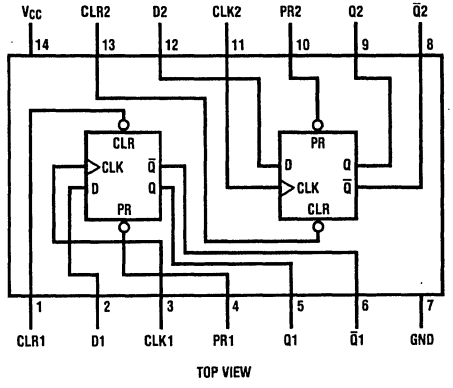
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5106–1

MM54HCT74/MM74HCT74

54HCT74 (J) **74HCT74 (J,N)**

Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

5

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND					
		I_{OUT}=0 μA		4.0	40	80	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per pin. All other inputs are held at V_{CC} Ground.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operatin Frequency From Clock to Q or $\overline{Q}$		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set Up Time Data to Clock			20	ns
t_H	Minimum Hold Time Clock to Data		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics

$V_{CC}=5.0V\pm10\%$ $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Clock to Q or $\overline{Q}$		21	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Preset or Clear to Q or $\overline{Q}$		21	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Set Up Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		9	16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HCT109/MM74HCT109
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear

General Description

These high speed J-$\overline{K}$ FLIP-FLOPS utilize microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS. They possess the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip flop has independent J, $\overline{K}$, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static dischage by internal diode clamps to V_{CC} and ground.

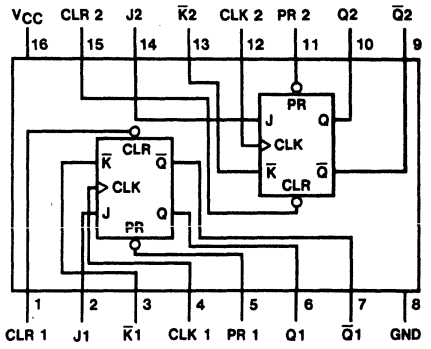
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HCT series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5306–1

MM54HCT109/MM74HCT109

54HCT109 (J) 74HCT109 (J,N)

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA F-F		4.0	40	80	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set Up Time J or $\overline{K}$ Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics

$V_{CC}=5.0V$ ±10% $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Clock to Q or $\overline{Q}$		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From Preset or Clear to Q or $\overline{Q}$		22	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Set Up Time J or $\overline{K}$ to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

PRELIMINARY

National Semiconductor

MM54HCT138/MM74HCT138 3-to-8 Line Decoder

General Description

This decoder utilizes microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS, and are well suited to memory address decoding or data routing applications. Both circuits feature high noise immunity and low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

The MM54HCT138/MM74HCT138 have 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, G2A and G2B) are provided to ease the cascading decoders.

The decoders' output can drive 10 low power Schottky TTL equivalent loads and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

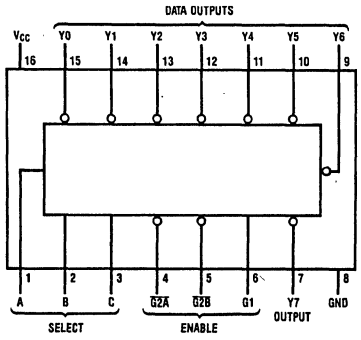
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL Input Compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

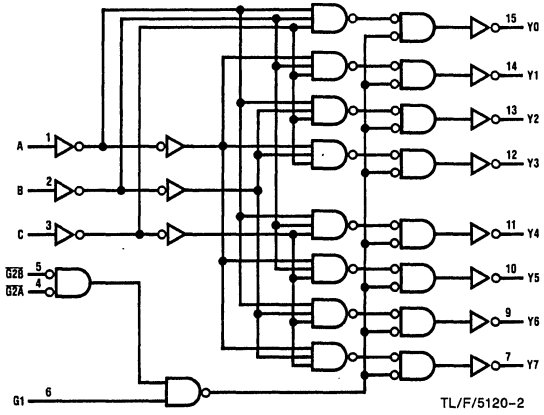


TL/F/5120–1

MM54HCT138/MM74HCT138

54HCT138 (J) 74HCT138 (J,N)

Logic Diagram



TL/F/5120–2

Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

H = high level L = low level X = dont't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input pin. All other inputs are held at V_{CC} or ground.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, A, B, or C to Output		20	35	ns
t_{PLH}	Maximum Propagation Delay, A, B, or C to Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, G1 to Y Output		14	25	ns
t_{PLH}	Maximum Propagation Delay, G1 to Y Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		17	30	ns
t_{PLH}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		13	25	ns

AC Electrical Characteristics

$V_{CC} = 5V \pm 10\%$ $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25°C$	74HCT $T_A = -40$ to $85°C$	54HCT $T = -55$ to $125°C$	Units
			Typ	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay A, B, or C to Output		24	40	50	60	ns
t_{PLH}	Maximum Propagation Delay A, B, or C to Output		18	30	38	45	ns
t_{PHL}	Maximum Propagation Delay G1 to Y Output		17	30	38	45	ns
t_{PLH}	Maximum Propagation Delay G1 to Y Output		20	30	38	45	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		23	35	43	52	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		18	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{IN}	Input Capacitance			5	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)					pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HCT139/MM74HCT139 Dual 2-To-4 Line Decoder

General Description

This decoder utilizes microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS, and is well suited to memory address decoding or data routing applications. It possesses the high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

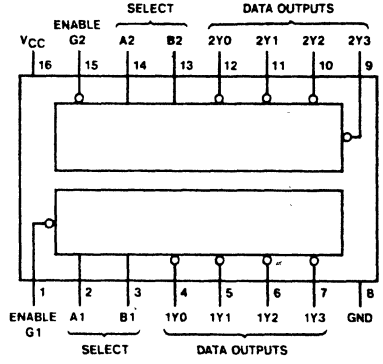
The MM54HCT139/MM74HCT139 contains two independent one-of-four decoders each with a single active low enable input (G1, or G2). Data on the select inputs (A1 and B1, or A2 and B2) cause one of the four normally high outputs to go low.

These devices are input and output characteristic and pinout compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground. MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- LS-TTL pin-out and threshold compatibility
- Typical propagation delays:
  Select to output (4 delays): 19 ns
  Select to output (5 delays): 24 ns
  Enable to output: 20 ns
- Fanout of 10 LS-TTL loads

Connection Diagram



TL/F/5311–1

MM54HCT139/MM74HCT139

54HCT139 (J) 74HCT139 (J,N)

Truth Table

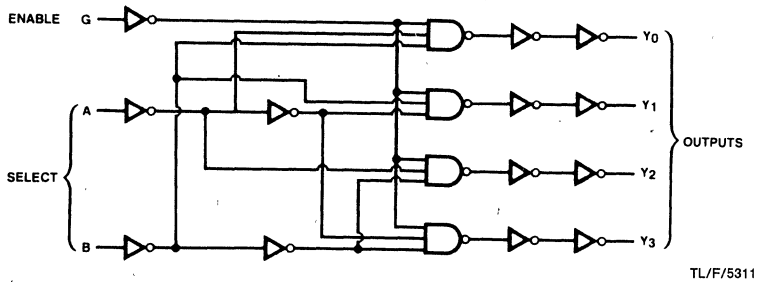
'HCT139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

½ MM54HCT139/MM74HCT139



TL/F/5311–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (Note 4)

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.96	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.96	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State® Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} and GND.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns (unless otherwise noted.)

Symbol	Parameter	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to Any Output 4 levels of delay	19	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to Any Output 5 levels of delay	24	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to any Output	20	30	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pf (unless otherwise noted.)

Symbol	Parameter	$T_A=25°C$	74HCT $T_A=-40°C$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
		Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to Any Output, 4 levels of delay	21	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to Any Output, 5 levels of delay	26	44	55	66	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Any Output	21	35	44	53	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	9	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)					pF
C_{IN}	Maximum Input Capacitance	5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HCT149/MM74HCT149
8 Line to 8 Line Priority Encoder

General Description

This priority encoder is implemented in microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority, encoder accepts 8 input request lines, $\overline{RI7}$–$\overline{RI0}$, and outputs 8 lines, $\overline{RO7}$–$\overline{RO0}$. It is the logical combination of a '148 8–3 line priority encoder driving a '138 3–8 line decoder. Only one request output can be low at a time. The output that is low is dependent on the highest priority request input that is low. The order of priority is $\overline{RI7}$ highest and $\overline{RI0}$ lowest. Also provided is and enable input, $\overline{RQE}$, which when high forces all outputs high. A request output is also provided, $\overline{RQP}$, which goes low when any $\overline{RI}$ is active.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and Ground.

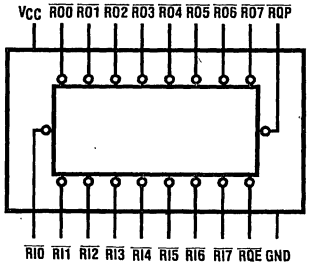
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Internal switched pull up resistors provided to reduce power consumption

Connection Diagram

Dual-In-Line Package



TL/F/5312–1

MM54HCT149/MM74HCT149

54HCT149 (J) 74HCT149 (J,N)

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay RQE to any Output		16	20	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay R_{IN} to R_{ON} (same Output)		17	22	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay R_{IN} to a different Output		18	23	ns

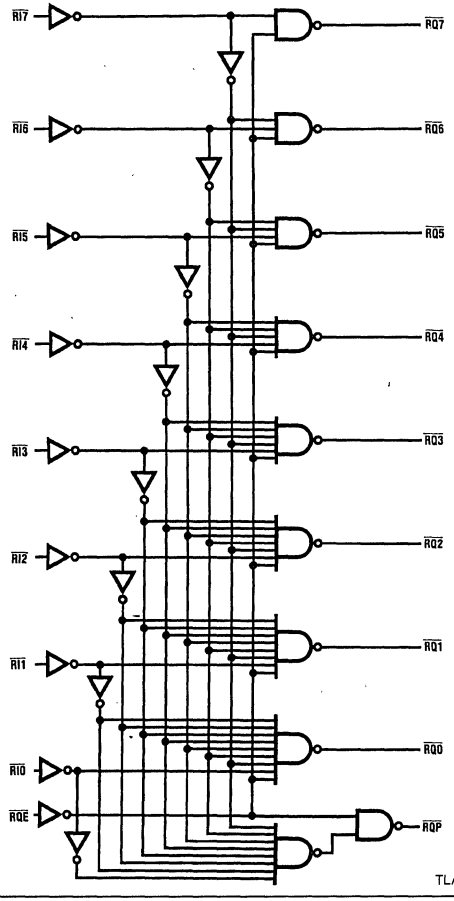
AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pf $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$		54HCT $T_A=-55$ to $125°C$		Units
			Typ	Guaranteed Limits				
t_{PHL}, t_{PLH}	Maximum Propagation Delay RQE to any Output		17	23		29	35	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay R_{IN} to R_{ON} (same Output)		18	25		31	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay R_{IN} to a different Output		20	26		33	39	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		10	15		19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)		50				pF
C_{IN}	Maximum Input Capacitance		5	10		10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

Simplified Logic Diagram



TL/F/5312–2

PRELIMINARY

National Semiconductor

MM54HCT240/MM74HCT240 Inverting Octal TRI-STATE® Buffer
MM54HCT241/MM74HCT241 Octal TRI-STATE Buffer
MM54HCT244/MM74HCT244 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS, and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. All three devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM54HCT240/MM74HCT240 is an inverting buffer and the MM54HCT244/MM74HCT244 is non-inverting buffer. Each device has two active low enables (1G and 2G), and each enable independently controls 4 buffers. MM54HCT241/MM74HCT241 is also a non-inverting buffer like the 244 except that the 241 has one active high enable, each again controlling 4 buffers.

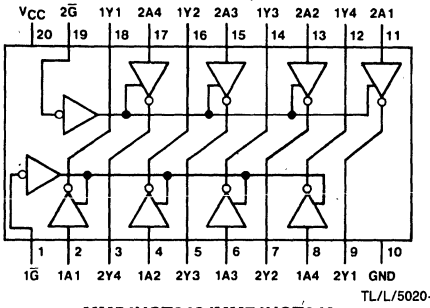
All inputs are protected from damage due to static discharge by diodes to V_{CC} and Ground.

Features

- TTL input compatible
- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Low quiescent current: 80 μA
- Output current: 6 mA

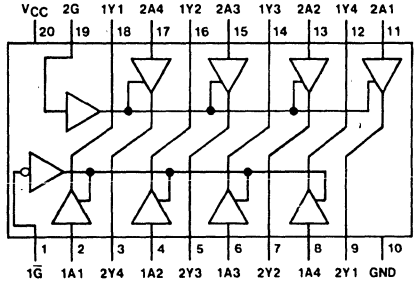
Connection Diagrams

Dual-In-Line Packages



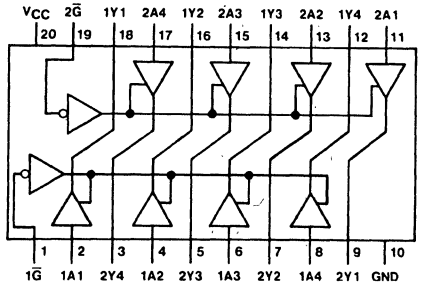
TL/L/5020-1

MM54HCT240/MM74HCT240
54HCT240 (J) 74HCT240 (J,N)



TL/L/5020-2

MM54HCT241/MM74HCT241
54HCT241 (J) 74HCT241 (J,N)



TL/F/5327-1

MM54HCT244/MM74HCT244
54HCT244 (J) 74HCT244 (J,N)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0,33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH} G=GND		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or GND.

Truth Tables

'HC240

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

'HC241

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

'HC244

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H=high level, L=low level, Z=high impedance

AC Electrical Characteristics MM54HCT240/MM74HCT240

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=45$ pF $R_L=1$ kΩ	14	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L=5$ pF $R_L=1$ kΩ	13	25	ns

AC Electrical Characteristics MM54HCT240/MM74HCT240

$V_{CC}=5.0V$ ±10%, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=50$ pF		12	20	25	30	ns
		$C_L=150$ pF		22	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	$C_L=50$ pF	15	30	38	45	ns
			$C_L=150$ pF	20	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF		15	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}=V_{CC}$ $\overline{G}=GND$	12 50				pF pF

AC Electrical Characteristics MM54HCT241/MM74HCT241, MM54HCT244/MM74HCT244

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L=45$ pF	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=45$ pF $R_L=1$ kΩ	17	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L=5$ pF $R_L=1$ kΩ	15	25	ns

AC Electrical Characteristics MM54HCT241/MM74HCT241, MM54HCT244/MM74HCT244

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

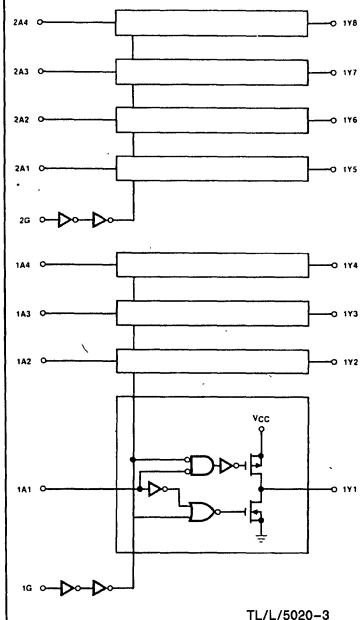
Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		14	23	29	34	ns
		C_L = 150 pF		17	33	42	49	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ	C_L = 50 pF	17	30	38	45	ns
			C_L = 150 pF	22	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF		17	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}$ = V_{CC}	12				pF
			$\overline{G}$ = GND	45				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

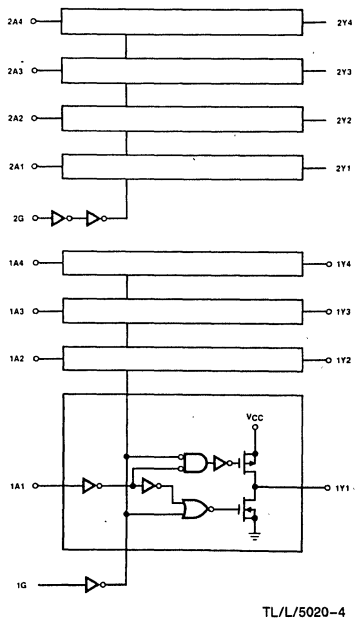
Logic Diagrams

'HCT240



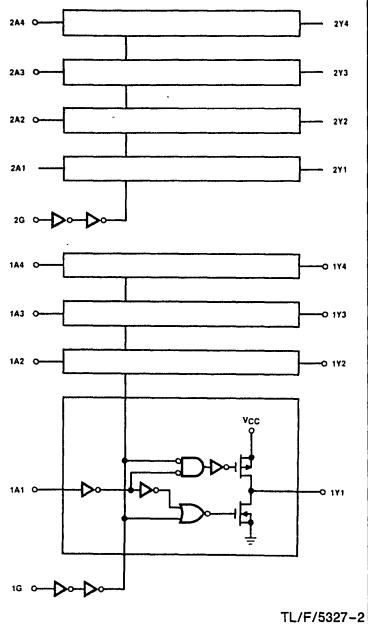
TL/L/5020-3

'HCT241



TL/L/5020-4

'HCT244



TL/F/5327-2

National Semiconductor

PRELIMINARY

MM54HCT245/MM74HCT245 Octal TRI-STATE® Transceiver

General Description

This TRI-STATE bi-directional buffer utilizes microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

All three devices are TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

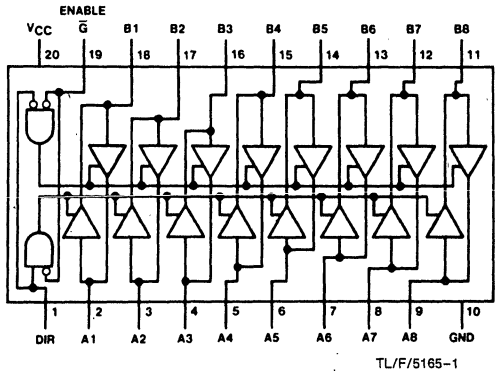
MM54HCT245/MM74HCT245 has one active low enable input ($\overline{G}$), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A.

MM54HCT/74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL Input Compatible
- Octal TRI-STATE outputs for μp bus applications: 6 mA, typ.
- High speed: 12 ns typical propagation delay
- Low Power: 80 μA (74 Series)

Connection Diagram



TL/F/5165–1

MM54HCT245/MM74HCT245

54HCT245 (J) 74HCT245 (J,N)

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	245
L	L	B data to A bus
L	H	A data to B bus
H	X	isolation

H = high level L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max.	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

(V_{CC}=5V±10%, unless otherwise specified.)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or ground.

5

AC Electrical Characteristics MM54HCT245/MM74HCT245

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	15	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kΩ	18	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	16	25	ns

AC Electrical Characteristics MM54HCT245/74HCT245

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		14	23	29	34	ns
		C_L = 150 pF		17	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ	C_L = 50 pF	17	30	38	45	ns
			C_L = 150 pF	20	35	43	52	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ		18	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		8	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance	(Note 5) $\overline{G}$ = V_{CC} $\overline{G}$ = GND						pF

Note 5: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

National Semiconductor

PRELIMINARY

MM54HCT373/MM74HCT373 TRI-STATE® Octal D-Type Latch MM54HCT374/MM74HCT374 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54HCT373/MM74HCT373 Octal D-TYPE LATCHES and MM54HCT374/MM74HCT374 Octal D-TYPE FLIP FLOPS utilize microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pinout compatible. The TRI-STATE outputs are capable of driving 15 LS TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM54HCT373/MM74HCT373 LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54HCT374/MM74HCT374 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

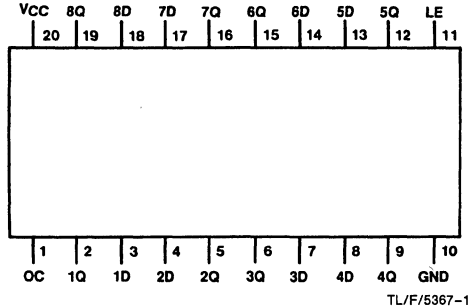
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 15 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package

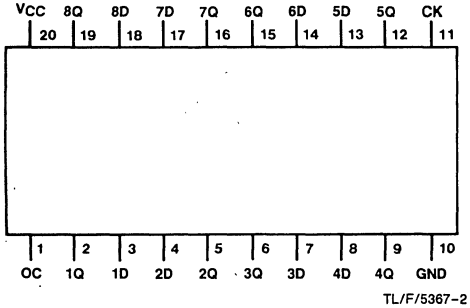


TL/F/5367–1

MM54HCT373/MM74HCT373

54HCT373 (J) 74HCT373 (J,N)

Dual-In-Line Package



TL/F/5367–2

MM54HCT374/MM74HCT374

54HCT374 (J) 74HCT374 (J,N)

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Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT373/MM74HCT373

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical Characteristics MM54HCT373/MM74HCT373

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=50$ pF $C_L=150$ pF	22 30	30 40	37 50	45 60	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=50$ pF $C_L=150$ pF	25 32	35 45	44 56	53 68	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			5	6	8	ns
t_H	Minimum Hold Time Clock to Data			10	13	20	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	G=V_{CC} G=GND					pF pF

Truth Tables

'373

Output Control	Enable G	Data	373 Output	573 Output
L	H	H	H	L
L	H	L	L	H
L	L	X	Q_0	$\overline{Q0}$
H	X	X	Z	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

'374

Output Control	Clock	Data	Output (374)	Output (534)
L	↑	H	H	L
L	↑	L	L	H
L	L	X	Q_0	$\overline{Q_0}$
H	X	X	Z	Z

H = High Level, L = Low Level

X = Don't Care

↑ = Transition from low-to-high

Z = High impedance state

Q_0 = The level of the output before steady state input conditions were established.

AC Electrical Characteristics MM54HCT374/MM74HCT374

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

AC Electrical Characteristics MM54HCT374/MM74HCT374

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

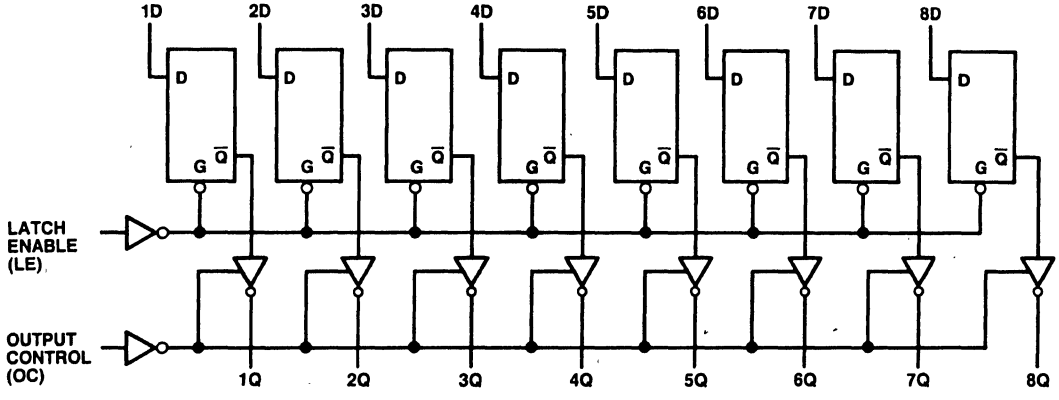
Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency			30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=50$ pF $C_L=150$ pF	22 30	36 46	45 57	48 69	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data			5	5	5	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	$G=V_{CC}$ $G=GND$					pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

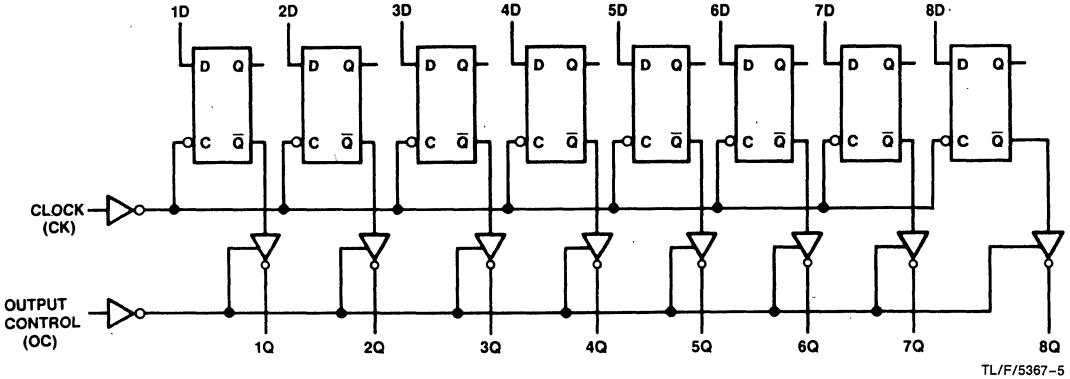
Logic Diagrams

MM54HCT373/MM74HCT373



TL/F/5367–4

MM54HCT374/MM74HCT374



TL/F/5367–5

5

National Semiconductor

PRELIMINARY

MM54HCT640/MM74HCT640 Inverting Octal TRI-STATE® Transceiver MM54HCT643/MM74HCT643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional buffers utilize micro-CMOS™ Technology, 3.0 micron silicon gate N-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

All devices are TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

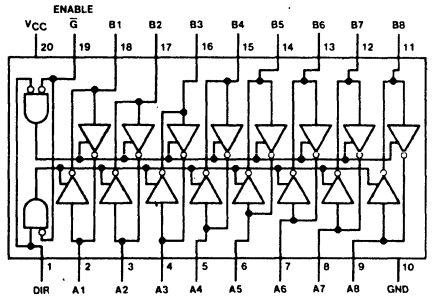
Both the MM54HCT640/MM74HCT640 and the MM54HCT643/MM74HCT643 have one active-low enable input (G), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The MM54HCT640/MM54HCT640 transfers inverted data from one bus to the other. The MM54HCT643/MM54HCT643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL Input Compatible
- Octal TRI-STATE outputs for μP bus applications: 6 mA, typical.
- High Speed: 12 ns typical propagation delay
- Low power: 80 μA maximum (74HCT)

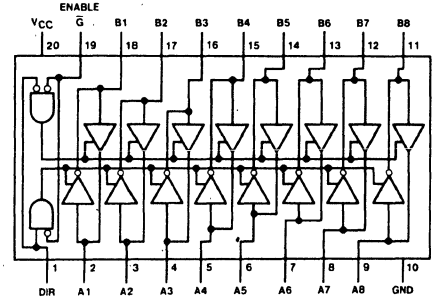
Connection Diagrams



TL/F/5344–1

MM54HCT640/MM74HCT640

54HCT640 (J) 74HCT640 (J,N)



TL/F/5344–2

MM54HCT643/MM74HCT643

54HCT643 (J) 74HCT643 (J,N)

Truth Table

Control Inputs		Operation	
$\overline{G}$	DIR	640	643
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC}=5V ±10%, unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC} 0.1	V_{CC} 0.1	V_{CC} 0.1	V
		$\|I_{OUT}\|$=6.0mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Tri-State Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH} or V_{IL}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0vA		8	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics MM54HCT640/MM74HCT640

V_{CC}=5.0V, t_r=t_f=6 ns, T_A=25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L=45 pF R_L=1 kΩ	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time		17	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L=5 pF R_L=1 kΩ	16	25	ns

AC Electrical Characteristics MM54HCT640/MM74HCT640

V_{CC} = 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		14	23	29	34	ns
		C_L = 150 pF		17	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1kΩ	C_L = 50 pF	17	30	38	45	ns
			C_L = 150 pF	20	35	43	52	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1kΩ C_L = 50 pF		18	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G} = V_{CC}$ $\overline{G}$ = GND					pF pF

AC Electrical Characteristics MM54HCT643/MM74HCT643

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF R_L = 1 kΩ	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time		17	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	16	25	ns

AC Electrical Characteristics MM54HCT643/MM74HCT643

V_{CC} = 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		14	23	29	34	ns
		C_L = 150 pF		17	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1kΩ	C_L = 50 pF	17	30	38	45	ns
			C_L = 150 pF	20	35	43	52	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = kΩ C_L = 50 pF		18	30	38	45	ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G} = V_{CC}$ $\overline{G}$ = GND					pF pF

Note 5: C_{PD} determines the no load power consumption. $P_D = C_{PD}V_{CC}{}^2f + I_{CC}V_{CC}$. The no load dynamic current consumption, $I_S = C_{PD}V_{CC} + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

PRELIMINARY

National Semiconductor

MM54HCT688/MM74HCT688
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS™ Technology, 3.0 micron silicon gate N-well CMOS to compare bit for bit two 8-bit words and indicate whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

The comparator combines the low power consumption of CMOS, but inputs are compatible with TTL logic levels, and the output can drive 10 low power Schottky equivalent loads.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

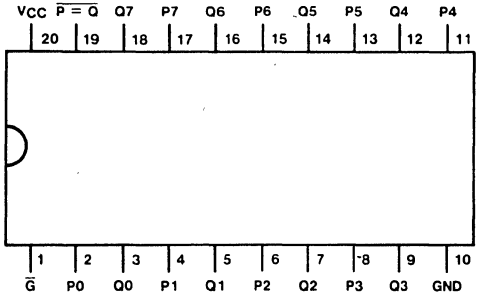
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL Input Compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Large output current: 4 mA

Connection and Logic Diagrams

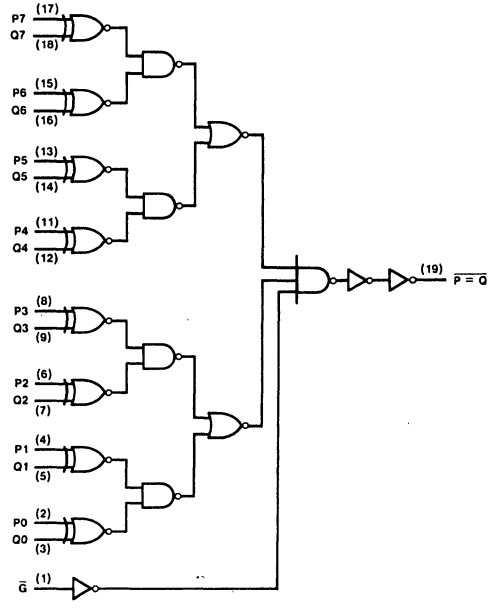
Dual-In-Line Package



TL/F/5018–1

MM54HCT688/MM74HCT688

54HCT688 (J) 74HCT688 (J,N)



TL/F/5018–2

Truth Table

Inputs		
Data P, Q	Enable $\overline{G}$	$\overline{P=Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HCT688	−40	+85	°C
MM54HCT688	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

(V_{CC}=5V ±10% unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=0.8V or 2.0V					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−.1	V_{CC}−.1	V_{CC}−.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V0.8V or 2.0V					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay - P or Q to output		19	30	ns
t_{PHL}	Maximum Propagation Delay - Enable to output		13	20	ns
t_{PHL}	Maximum Propagation Delay - Enable to output		10	18	ns

AC Electrical Characteristics

$V_{CC}=5V \pm 10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$		54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay - P or Q to output		22	34	42	51	ns
t_{PHL}	Maximum Propagation Delay - Enable to output		16	23	29	35	ns
t_{PLH}	Maximum Propagation Delay - Enable to output		13	21	26	32	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			60			pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switching Waveforms and Test Circuits.

5

Section 6

Enhancement Programs

National's A+ Program

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who cannot perform incoming inspection of ICs or do not wish to do so, yet need significantly better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the repair and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quailty are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the precentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National has combined the successful B+ program with the Military/Aerospace processing specifications and provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM
Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts
At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

National's A+ Program (Continued)

High Temperature (100°C) Functional Electrical Test
A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C–15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing
Every device is tested at 25°C for functional and DC parameters.

Burn-in Test
Each device is burned-in for 160 hours at a minimum junction temperature of +125°C or under equivalent conditions of time and temperature, as established by a time-temperature regression curve based on 0.96eV activation energy. All burn-in done under steady-state conditions unless otherwise specified.

DC Functional and Parametric Tests
These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor
Samples from each package type are selected at random each week and submitted to cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-than-normal QC Inspection Plans
Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

National's B+ Program

B+ Program: a comprehensive program that assures high quality *and* high reliability of molded integrated circuits.

The B+ program improves both the quality *and* the reliability of National's digital, linear, and CMOS Epoxy B integrated circuit products. It is intended for the manufacturing user who cannot perform incoming inspection of ICs, or does not wish to do so, yet needs significantly-better-than-usual incoming quality and reliability levels for standard ICs.

Integrated circuit users who specify B+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.

Reliability Saves You Money

With the increases population of integrated circuits in modern electronic systems has come an increased concern with IC failures in such systems.

And rightly so, for at last two reasons.

First of all, the effect of component reliability on system reliability can be quite dramatic. For example, suppose that you, as a system manufacturer, were to choose an IC that is 99 percent reliable. You would find that if your system used only 70 such ICs, the overall reliability of the system's IC portion would be only 50 percent. In other words, only one out of two of your systems would operate. The result? A system very costly to produce and probably very difficult to sell.

Secondly, whether the system is large or small you cannot afford to be hounded by the spectre of unnecessary maintenance costs. Not only because labor, repair, and rework costs have risen—and promise to continue to rise—but also because field replacement may be prohibitively expensive. If you ship a system that contains a marginally-performing IC, an IC that later fails in the field, the cost of replacement may be—literally—hundreds of times more than the cost of the failed IC itself.

Improving The Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Now, it's true that reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement, which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate most marginal, short-life parts.

In any test for reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time to failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

Quality Improvement

When an IC vendor specifies 100 percent final testing of its parts then, in theory, every shipped part should be a good part. However, in any population of mass-produced items there does exist some small percentage of defective parts.

One of the best ways to reduce the number of such faulty parts is, simply, to retest the parts prior to shipment. Thus, if there is a one percent chance that a bad part will escape detection initially, retesting the parts reduces that probability to only 0.01 percent. (A comparable tightening of the QC group's sampled-test plan ensures the maintenance of the improved quality level.)

National's B+ Program Gets It All Together

We've stated that the B+ program improves both the quality *and* the reliability of National's molded integrated circuits, and pointed out the difference between those two concepts. Now, how do we bring them together? The answer is in the B+ program processing, which is a continuum of stress and double testing. With the exception of the final QC inspection, which is sampled, all steps of the B+ process are performed on 100 percent of the program parts. The following flow chart shows how we do it, step by step.

SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

High Temperature (100°C) Functional Electrical Test

A high temperature test such as this with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C–

National's B+ Program (Continued)

15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient. (Even though Epoxy B processing has virtually eliminated thermal intermittents, we perform this test to ensure against even the remote possibility of such a problem. Remember, the emphasis in the B+ program is on the elimination of those marginally-performing devices that would otherwise lower field reliability of the parts.)

DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to 100 cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-than-normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the B+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with two 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sampling plans used in our B+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

MM54HC/883
A High Speed CMOS Family for High Reliability Systems

At National Semiconductor, there has historically been a close relationship between our growth in CMOS technology and our growth in the Mil/Aero portion of the integrated circuit marketplace. National began manufacturing CMOS devices in 1971 and was one of the first companies to qualify CMOS logic devices to MIL-M-38510. Today, National is the acknowledged leader in advanced CMOS technology and is one of the leading supplier's of Military/Aerospace ICs. These two aspects of leadership come together to provide the industry's premier Mil/Aero logic family—54HC/883B and 54HC/883S high speed CMOS.

National's 54HC screening utilizes the Class B and Class S requirements of MIL-STD-883 and MIL-M-38510. National's 883B/RETS™ 54HC devices are processed through the most compliant Class B screening flow offered off-the-shelf by any semiconductor manufacturer. Prior to its release to production, each device must pass the full Group A, B, C, and D qualification defined in Method 5005 of MIL-STD-883. Production screening is performed in accordance with Method 5004 of MIL-STD-883, with quality conformance testing in accordance with Method 5005. The quality conformance test frequency is as defined in MIL-M-38510. The production lines utilized operate with the same level of control as the MIL-M-38510 line, and use the same specifications for calibration, rework, resubmission, and operator certification as JAN products.

The manufacturing system is tailored to MIL-M-38510 because we feel that MIL-M-38510 provides clear and unequivocal procedures. JAN parts have clearly defined electrical test and burn-in requirements. National provides this same level of definition and standardization through the RETS (which is explained in detail in National's *Reliability Handbook*), a simplified, but comprehensive description of the actual electrical testing performed on each device type.

At the time of this book's printing, we are preparing RET's for the entire 54HC/883B high speed CMOS family.

National has also looked toward the needs of the space vehicle manufacturers, and has developed a program for Class S devices, 883S/RETS™. This program provides material screened to the Class S requirements of Method 5004 of MIL-STD-883, with quality conformance testing in accordance with the Class S requirements of Method 5005. All 883S/RETS devices are manufactured entirely in the U.S.

The screening flows for 883B/RETS and 883S/RETS are shown in *Figures 1* and *2* respectively.

The military specifications employed in the National screening flows are dynamic documents. They are subject to continual review and revision by the government. As changes are made to these key documents, National will continue to incorporate those changes into the 883B/RETS and 883S/RETS programs in order to ensure that the parts provided will enable systems manufacturers to maximize the reliability and performance of their equipment.

Military screened 54HC high speed CMOS devices, both Class B and Class S, will provide the military systems manufacturer with the best combination of performance, reliability, and power consumption available in the marketplace.

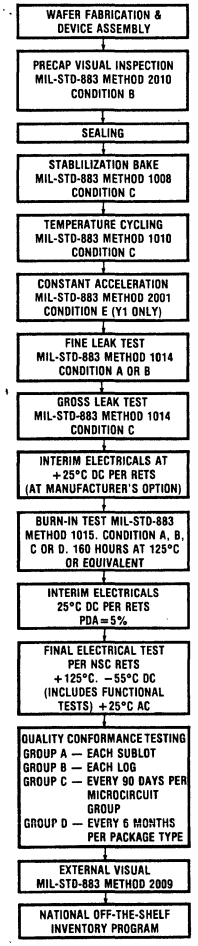


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FIGURE 1: National's 883B/RETS™ Class B screening flow

NOTES:
1. ALL METHODS REFERENCED ARE MIL-STD-883 TEST METHODS.
2. THESE TESTS ARE PERFORMED ON A SAMPLE BASIS. ALL OTHER TESTS ARE PERFORMED 100%.
3. ACCEPTANCE CRITERIA SHALL BE IN ACCORDANCE WITH MIL-M-38510.
4. THE PDA FOR STATIC I AND STATIC II BURN-IN SHALL BE 5% TOTAL.
5. THE PDA INCLUDES Δ FAILURES.
6. GROUP A AND BOND PULL AND DIE SHEAR TESTING OF GROUP B MAY BE PERFORMED ON-LINE.
7. ALL ELECTRICAL TESTING SHALL BE IN ACCORDANCE WITH THE APPLICABLE RETS OR THE APPLICABLE MIL-S-38510 DETAIL SPECIFICATION.

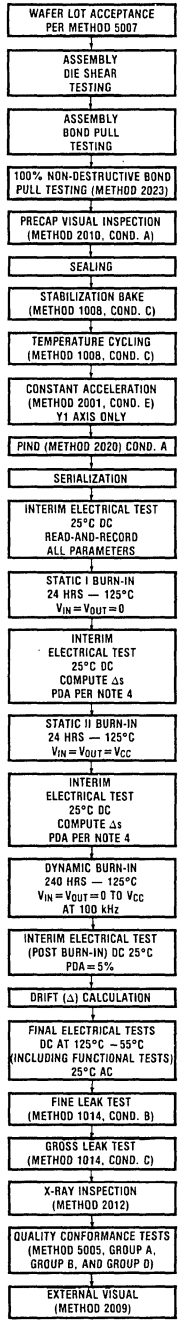

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FIGURE 2: National's 883S/RETS™ Class S CMOS screening flow

Section 7

Reliability Report

RELIABILITY REPORT

Reliability of

High Speed CMOS Logic

National

Semiconductor

RELIABILITY REPORT

INTRODUCTION

Until recently, the primary reasons for the popularity of CMOS logic circuits have been low power dissipation, tolerance to wider variations in power supply voltage, and the flexibility of using a broader range of power supplies. Although the acceptance of CMOS in logic applications has been increasing over the past decade, its growth has been limited by its inherently slower speed compared with its bipolar counterparts.

The metal gate technology, from which all of the popular CMOS families were built, typically yielded a 90 ns propagation delay for a buffered gate, and a guaranteed maximum more than double that, whereas, the bipolar equivalents in the popular low power Schottky family provided typical delay of 8 ns with maximums of 15. Under real-world demands of increasingly faster computer processing times, many systems simply could not use CMOS and at the same time meet system specifications.

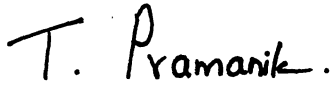
The arrival of the silicon gate process allowed CMOS to make its largest technological improvement since its inception. By employing this process, National Semiconductor has been able to increase CMOS speeds to the point where they are now equal to LS speeds, while still maintaining the earlier power dissipation and supply voltage attractiveness.

Series 54HC/74HC High Speed CMOS was announced in the summer of 1981 and will include, when fully developed, nearly 200 logic devices. Many of these devices will be equivalents to those functions popular today in both "LS" and "4000" families.

Prepared by

Dave Tovar
Manager, CMOS Product Engineering

Approved by



Tapan Pramanik
Manager, CMOS Reliability Engineering

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KEY FEATURES OF THE SERIES 54HC/74HC FAMILY

- LS speeds at CMOS power
- Operation over a 2V to 6V power supply range
- Output sink and source capability of 4 mA
- AC guarantees across the applicable temperature range

HIGH SPEED (HC) CMOS DEVICE FABRICATION

High Speed CMOS wafer fabrication is designed to produce reliable, high performance devices which require minimum handling restrictions. At National Semiconductor, these objectives are achieved through the use of advanced materials, process innovations, and rigorous controls.

This high speed logic family represents an advanced 3.5 micron, single metal, polysilicon gate, oxide-isolated CMOS process. This process makes use of advanced technologies, including extensive use of ion implantations to tightly control substrate profiles.

National's HC processing permits the fabrication of MOS transistors with threshold voltages on the order of one-half that of the more conventional metal gate process. Coupled with thinner gate oxides and self-aligning gates, these lower threshold voltages allow higher speed circuit operation with lower supply voltages. In addition, the threshold voltage distribution from run to run is much tighter, so that long term uniformity of device characteristics is assured.

Figure 1 represents the cross section of the HC process employed at National.

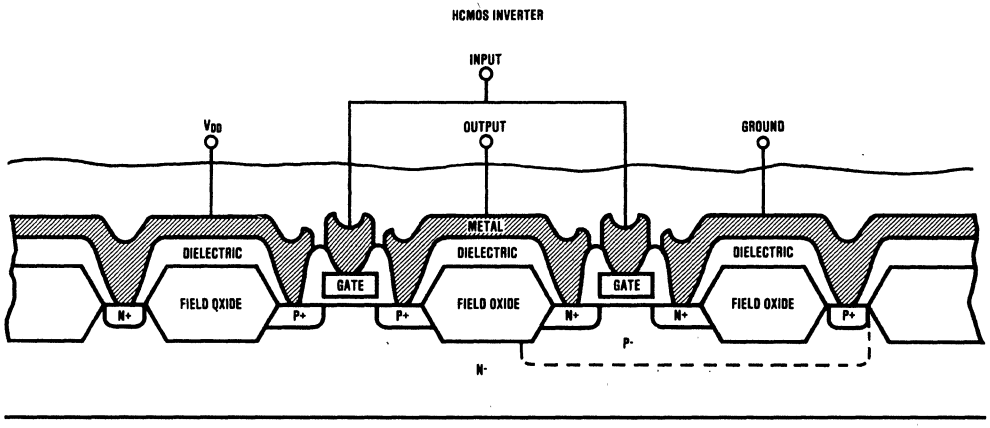

FIGURE 1. HCMOS Cross Section

RELIABILITY REPORT

ACCELERATED LIFE TEST

Accelerated life testing at elevated temperatures is a principal method of simulating long-term operation within a short period of time. This method is particularly useful because it provides a means of accelerating time-to-failure of temperature sensitive failure mechanisms. As a result, data is gathered for failure rate predictions at any operating field ambient.

The following tests have been conducted at an ambient temperature of 125°C with devices biased at a maximum voltage of 5.5 volts. Complete functional and parametric testing to data sheet specifications is performed at reported data points.

HIGH TEMPERATURE BIAS RELIABILITY TEST RESULTS
125°C OPERATION AT 5.5 VOLTS

CERDIP, GLASS SEALED HERMETIC DIP, J

Device	Rel Lot #	SS	168 Hours	500 Hours	1000 Hours
MM54HC04J	RBC71305	51	1 (1)	0	0
MM54HC04J	RBC72012	360	1 (2)	0	0
MM54HC139J	RBC72177	200	0	0	Stopped
MM54HC164J	RBC72178	192	0	0	Stopped
MM54HC00J	RBC72196	256	0	0	0
MM54HC390J	RBC72223	189	0	0	0
MM54HC393J	RBC72224	127	0	0	0
MM54HC04J	RBC72346	324	0	0	0
MM54HC174J	RBC72348	255	0	0	0

Actual Failure Rate = 2/1,757,664 device-hours
= 0.11% per 1000 hrs at 125°C.

Notes: (1) Parametric Failure
(2) Gate Oxide Rupture

M DIP EPOXY MOLDED, N

Device	Rel Lot #	SS	168 Hours	500 Hours	1000 Hours
MM54HC04N	72011	358	0	0	0
MM54HC04N	72064	384	0	0	0
MM54HC04N	72065	384	0	0	0
MM54HC00N	72084	120	0	0	0
MM54HC164N	72142	256	0	0	0
MM54HC688N	72320	122	0	0	0
MM54HC393N	72339	104	1 (1)	0	0
MM54HC390N	72347	64	0	0	0
MM54HC349N	72349	108	0	0	0

Actual Failure Rate = 1/1,900,000 device-hours
= 0.05% per 1000 hrs at 125°C.

Notes: (1) Parametric Failure

Quiescent current leakages were measured on molded pieces of two lots subjected to both HTOpL and T&H. Measurements were conducted before and after testing. Results are listed in Table 1.

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TABLE 1
Average I_{CC} Shifts for Lots
MM54HC04A RBC72064 and RBC72065
(Units In Nanoamps)

Test	Leg	SS	Average At 0 Hours	Average At 1000 Hours
HTOpL	A	48	4	3
	B	48	21	25
	C	48	0	2
	D	48	0	0
T&H	A	48	2	19
	B	48	17	12
	C	48	16	14
	D	48	18	18
HTOpL	A	48	0	0
	B	48	0	0
	C	48	0	0
T&H	A	48	0	0
	B	48	0	0
	C	48	0	0

Threshold voltage measurements were also read before and after on one lot of cerdip and two lots of molded DIPs. Results are listed in Table 2.

TABLE 2
V_T Shifts After 1000 Hours Burn-In
(Units In Volts)

			Pre		Post	
Lot	Leg	SS	Avg. V_{TN}	Avg. V_{TP}	Avg. V_{TN}	Avg. V_{TP}
72012,J	A	48	.387	.579	.390	.580
	B	48	.347	.570	.402	.580
	C	48	.394	.570	.440	.580
	D	48	.350	.567	.336	.580
72064,N	A	48	.470	.580	.472	.570
	B	48	.530	.580	.499	.571
	C	48	.400	.527	.467	.570
	D	48	.471	.519	.518	.575
72065,N	A	48	.428	.580	.423	.572
	B	48	.453	.579	.448	.570
	C	48	.380	.529	.412	.570
	D	48	.402	.526	.453	.572

RESULTS

HC high temperature bias failure rates are calculated and derated at 85°C and 45°C operating environments for molded dual-in-line packages. The Arrhenius relationship is employed to compute the equivalent derated failure rate using an activation energy of 1.0eV. An average confidence limit of 60% is reported for these derated figures as seen in Table 3.

Table 3
High Temperature Operating Life Test
$T_A = 125°C$, $V_{CC} = 5.5V$ Static
60% Confidence Level

Device	Lots	Qty	Dev. Hours	# Fail	λ @ 125°C	λ @ 85°C	λ @ 45°C
Various	9	1,900	1,900,000	1	0.1032	0.0039	6.7100×10^{-5}

λ = Failure Rate; %/1000 Hours at Temperature.

(This data can be further extrapolated to lower temperatures using a 1.0eV activation energy as illustrated in the failure rate versus temperature plot of *Figure 2.*)

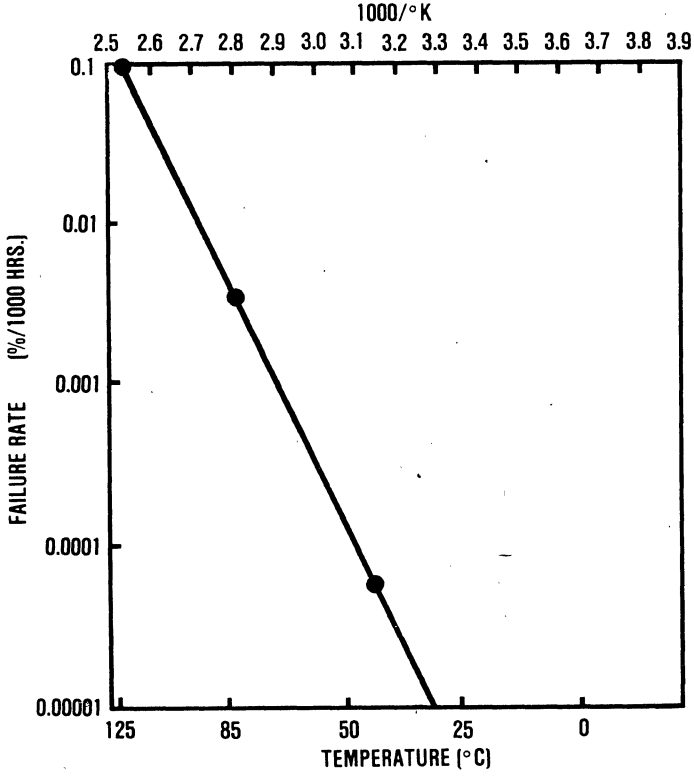

FIGURE 2. Failure Rate vs Temperature

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TEMPERATURE HUMIDITY BIAS TEST (THB)

The steady state humidity test at 85°C and 85% relative humidity is the most common temperature/humidity test in use today. This is an accelerated test; that is, it involves stress levels considerably in excess of the field-use levels encountered by a device. The test is intended to trigger moisture-related failure mechanisms occurring over a period of months or years in the field. Results are seen below.

Device	Rel Lot #	SS	168 Hours	500 Hours	1000 Hours
MM54HC04N	RBC72011	340	0	0	0
MM54HC04N	RBC72064	192	0	0	0
MM54HC04N	RBC72065	192	1 (1)	0	1 (1)
MM54HC00N	RBC72084	96	0	1 (1)	0
MM54HC393N	RBC72339	95	2 (1, 2)	0	1 (3)
MM54HC04N	RBC73025	225	0	0	0
MM54HC390N	RBC72347	48	0	0	0

Cumulative Percent Failures at 1000 Hrs = 6/1188 = 0.51%

Note: 1. Parametric Failures
2. Continuity Failures
3. Functional Failure

BIASED PRESSURE POT TEST

Another commonly used test is the "pressure cooker" test. This test is usually performed with devices in an operating mode while being exposed to saturated steam (100% RH). The most common condition is 115°C. At saturation, this temperature corresponds to a water vapor pressure of 1489mm Hg (28.8 psia). Due to its severity, this test is destructive to virtually all plastic packages. It creates failure mechanisms which would never be triggered at temperature and humidity extremes found in even the most severe application. For this reason, the test is limited to a relative few number of hours, and results are interpreted on a purely qualitative, comparative basis.

Biased Pressure Pot Test Results
$T_A = 115°C$, $V_{CC} = 5.5V$

Device	Rel Lot #	SS	96 Hours	192 Hours
MM54HC04N	RBC72064	75	0	0
MM54HC04N	RBC72065	75	0	0
MM54HC00N	RBC72084	75	0	0
MM54HC04N	RBC73025	148	0	0
MM54HC174N	RBC73024	54	0	1

IMPROVED INPUT PROTECTION

The single most prevalent cause of "infant mortality" field failures in CMOS microcircuits is generally gate oxide damage. This can result from any transient voltage condition, such as electrostatic discharge (ESD), inductive spikes, etc. An improved input protection circuitry which takes full advantage of the HC silicon gate process has been carefully designed to reduce the susceptibility of these HC circuits to oxide ruptures due to large static voltages.

In conjunction with the input protection, the output parasitic diodes also protect the circuit from large static voltages occurring between any input, output, or supply pin.

Figure 3 shows a schematic of the input protection network employed. The network consists of three elements: a polysilicon resistor, a diode connected to V_{CC}, and a distributed diode resistor connected to ground. This HC process utilizes the polyresistor to more effectively isolate the input diodes than the diode resistor used in metal gate CMOS. This resistor will slow down incoming transients and also helps to dissipate some of the energy. Connected to the resistor are the two diodes which clamp the input spike and prevent large voltages from appearing across the transistor. These diodes are larger than those used in metal gate CMOS, to enable greater current shunting and make them less susceptible to damage. The input network is ringed by V_{CC} and ground diffusions, which prevent the substrate currents caused by these transients from affecting other circuitry.

The parasitic output diodes that isolate the output transistor drains from the substrate are also important in preventing damage. They clamp large voltages that appear across the output pins. These diodes are also ringed by V_{CC} and ground diffusions to again shunt substrate currents, thus preventing damage to other parts of the circuit.

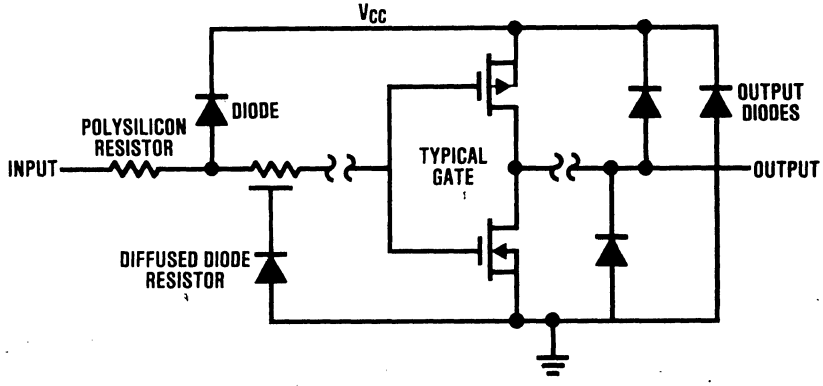
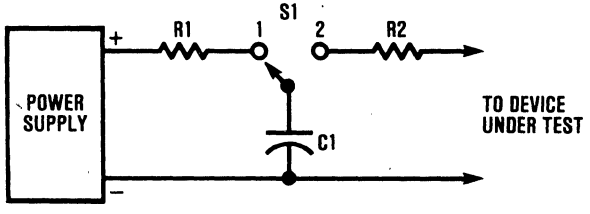


FIGURE 3. Input Protection Network

HIGH SPEED LOGIC INPUT PROTECTION ZAP TEST

Input gates of twenty MM54HC00N were subjected to a high voltage (V_{ZAP}) burst in order to test input protection circuits. The inputs under test were subjected to a voltage pulse from a 100 pF source charged to 1000V and 2000V respectively, according to the test circuit shown in *Figure 4*.



R1 = current limiting resistor; R2 = 1.5k

R1 = current limiting resistor; R2 = 1.5k

FIGURE 4. High Speed Logic Input Protection V_{ZAP} Test

Each input under test was subjected to a sequential V_{ZAP} accordingly:

Positive	Negative
(1) V_{DD}	Input
(2) Input	V_{DD}
(3) Input	V_{SS}
(4) V_{SS}	Input
(5) Output	Input
(6) Input	Output

V_{ZAP} six times (6×) for each condition.
ZAP results appear in Table 4.

TABLE 4
V_{ZAP} Test Results

	Condition 1	Condition 2
Voltage	1000V	2000V
Capacitance	100 pF	100 pF
Energy Discharged	50 μJ	200 μJ
Result	0/20*	0/20*

*Input leakages equal to or less than 4 nA.

HIGH SPEED LOGIC HTOPL BUY-OFF

In addition to ongoing long-term reliability studies and audits, National does an initial 168 hours high temperature bias design buy-off on every single HC product type before it is released into production. The primary reason behind this program is to assure the capture of any design-related reliability problem which might pass through all electrical tests. Accelerated conditions are the same as previously mentioned, i.e., $T_A = 125°C$, $V_{CC} = 5.5$ volts, burn-in time is 168 hours.

Device	SS	Results at 168 Hours
MM74HC00N	45	0
MM74HC02N	50	0
MM74HC04N	50	0
MM74HCU04N	50	0
MM74HC08N	49	0
MM74HC10J	50	0
MM74HC11J	50	0
MM74HC14N	48	0
MM74HC73J	50	0
MM74HC76J	50	0
MM74HC86J	50	0
MM74HC107J	50	0
MM74HC112J	40	0
MM74HC113J	50	0
MM74HC139N	45	0
MM74HC147N	50	0
MM74HC151N	50	0
MM74HC160J	50	0
MM74HC161J	50	0
MM74HC164N	45	0
MM74HC174N	45	0
MM74HC192N	50	0
MM74HC193N	49	0
MM74HC242N	50	0
MM74HC251J	50	0
MM74HC253N	50	0
MM74HC259N	50	0
MM74HC266J	50	0
MM74HC390N	49	0
MM74HC393N	50	0
MM74HC688N	50	0

HANDLING AND TEST GUIDE

Introduction

All CMOS low threshold devices are susceptible to damage by the electrostatic discharge (ESD) of energy through the devices. Although all CMOS devices have input protection networks which are effective in a large number of device-handling situations, they are not effective in 100% of the cases (please refer to specific devices in National's CMOS Databook).

In order to be totally safe, proper handling procedures must be used to eliminate damage and subsequent yield loss caused by static electrical charges. It is the purpose of this application guide to outline proper handling procedures for CMOS devices.

General Handling Procedures

1. The leads of CMOS devices must be in contact with conductive material to avoid build-up of static charge. Containers used for transporting or storing CMOS components should be made of such material or lined with antistatic protection. Rails for handling and shipping MOS devices must be made of electrically conductive material or be made static-free by an appropriate surface coating. In no case will CMOS devices be inserted into polystyrene foam or other high dielectric materials. Any surface coating which is not at ground potential must not come in direct contact with device pins.
2. Devices must be packed in conductive containers, rails or envelopes for storing. In addition, devices must be kept at ground potential and should never come in contact with nonconductive plastics.
3. All electrical equipment must be hard-wired to ground. Soldering iron tips, metal parts of fixtures and tools, and all handling systems must be grounded.

Cleaning

1. Devices should be cleaned by a solvent which will assure complete removal of foreign matter, flux, residual matter, etc., from the exterior of the package.
2. A static neutralizing ion blower should be used when manually cleaning devices or subassemblies with brushes.
3. All automatic cleaning should be grounded.
4. All cleaning baskets should be grounded.

Assembly

1. Subassembly modules and printed circuit boards should be manufactured and handled using the same procedures as those described above for individual CMOS devices.
2. CMOS parts should be the last to be inserted into printed circuit boards or systems so as to avoid overhandling.
3. Circuit boards containing CMOS devices which are being transported between work stations and test areas should be contained in antistatic material or have all board terminals shorted together using a conductive shorting bar. Only handling trays of conductive material should be used.
4. All automatic insertion equipment, solder machines, metallic parts of conveyor systems, and soldering irons should be grounded.

Note: These precautions should be taken until the subassembly is inserted into the complete system in which the proper voltages are applied. Subassemblies should never be constructed, fixtured, stored, or transported in polystyrene or any other high dielectric materials.

General Operating Procedures

The National CMOS product line is comprised of many different device types for a variety of applications. The following operating procedures apply in a general sense to all CMOS devices, but reference to device specification sheets is still necessary to assure correct operating values.

A. Before making any physical connections or applying any external signal sources, be sure that all power supplies are off. Be sure, also, to observe proper static ground conditions.

B. Power supplies should be turned up slowly to the necessary voltages so as to avoid rapid supply changes.

C. After power supplies have been turned on, apply external input signals.

Note: Failure to perform the power-on procedure in this order can result in damage to CMOS circuitry.

D. To power down, remove input signals, then turn power supplies off slowly.

E. If CMOS devices are operated at an elevated environmental temperature, allow devices to reach room temperature before they are powered down.

F. Do not leave inputs to any CMOS device unused. For NAND gates, the unused inputs should be tied to V_{DD}; unused inputs to NOR gates should be tied to ground.

Testing

1. Use grounded metallic fixtures where possible. Any surface that is not at ground potential should not come into direct contact with device pins.
2. Use a static-neutralizing ion air blower when running automatic handlers. Use conductive handling trays when transferring devices.
3. Do not insert devices or boards with power turned on.
4. Ensure that AC signals do not cause excessive current leakage.

Electrical Failure Modes Caused by Improper Handling

If proper handling techniques are not followed, the generation of static electrical discharges may damage the CMOS devices, resulting in inoperable or degraded parts. Typical failure modes are:

a. Shorted or open gates

b. Shorted input protection diodes

c. Open metal paths in the device input circuitry

d. Degraded device characteristics

The presence of these failure modes can be detected easily using a transistor curve tracer.

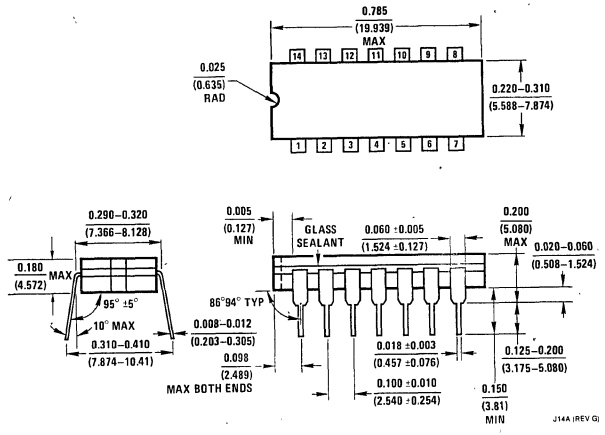
Section 8

Ordering and Package Information

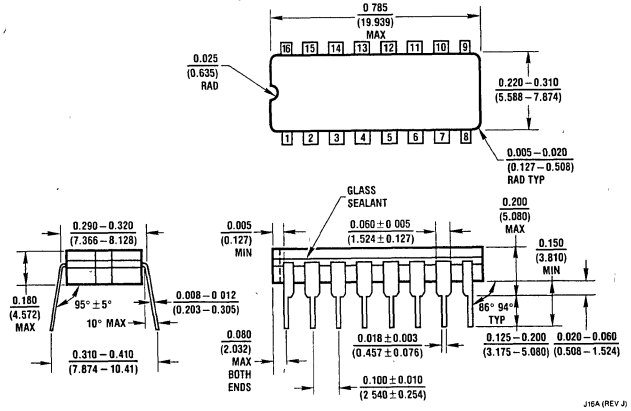
National Semiconductor

Physical Dimensions

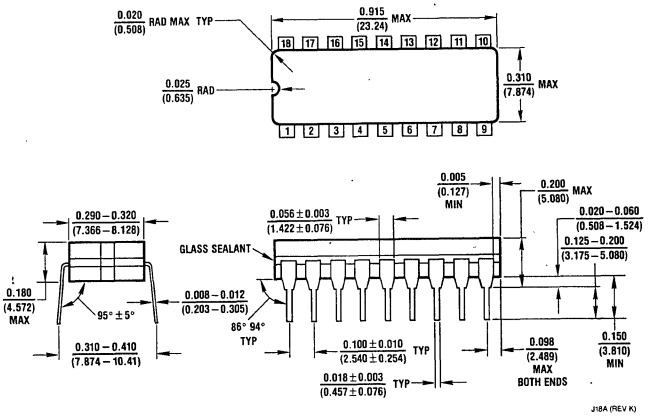
All dimensions in inches (millimeters)



NS Package J14A



NS Package J16A



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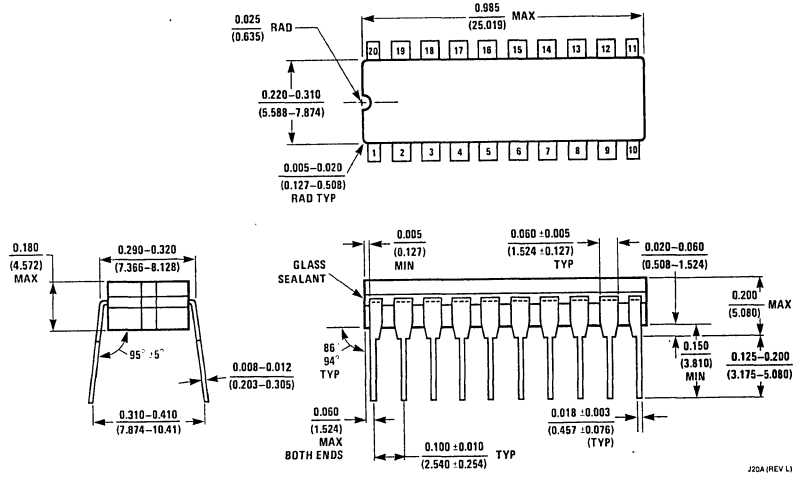
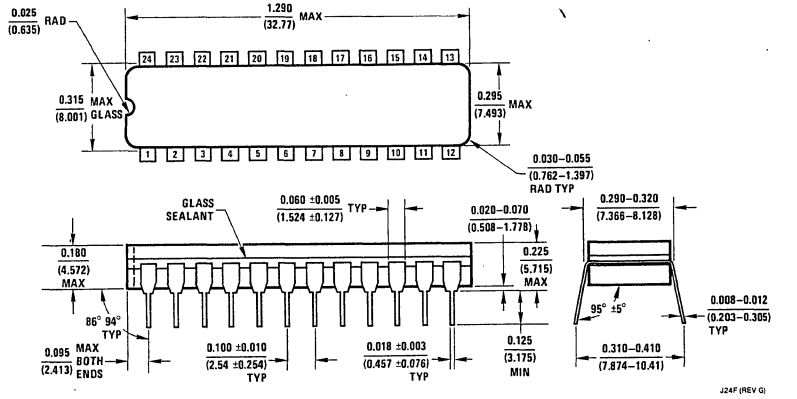
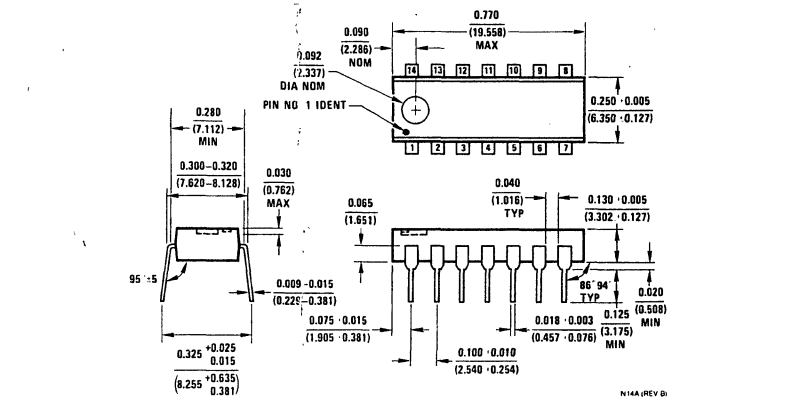


NS Package J20A



NS Package J24F



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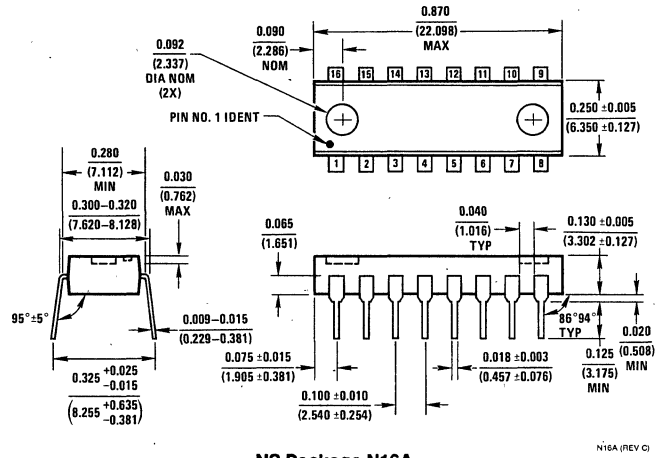

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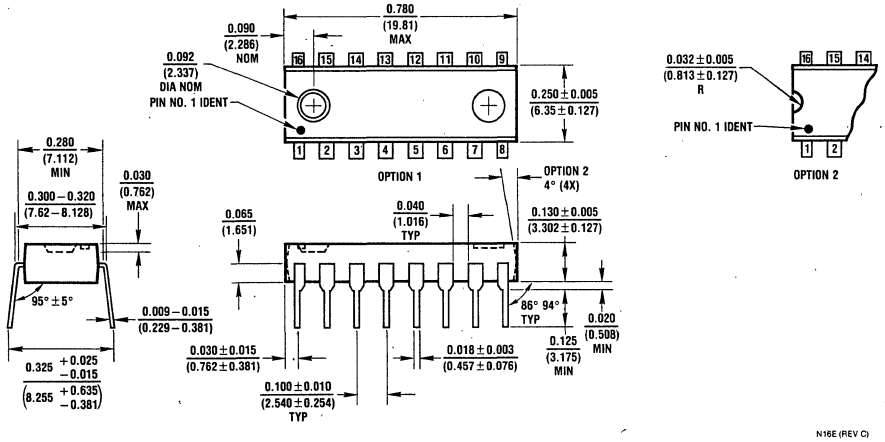

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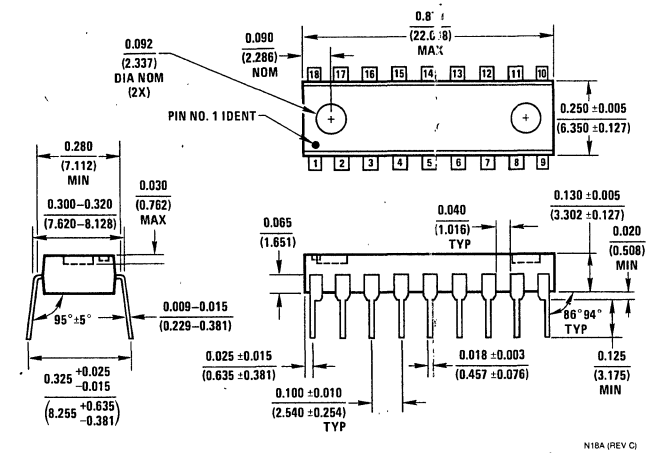

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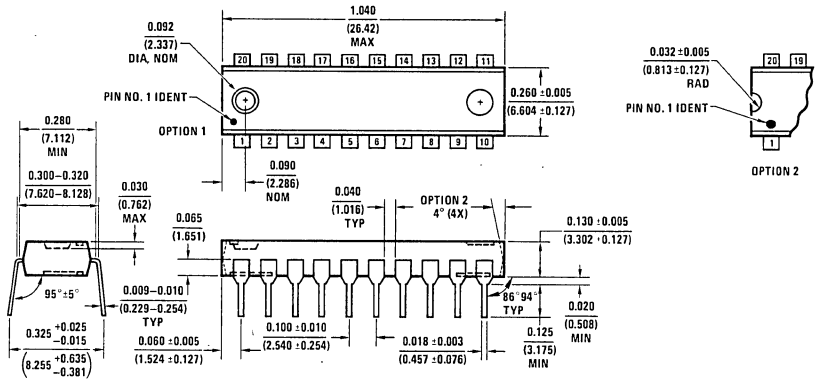
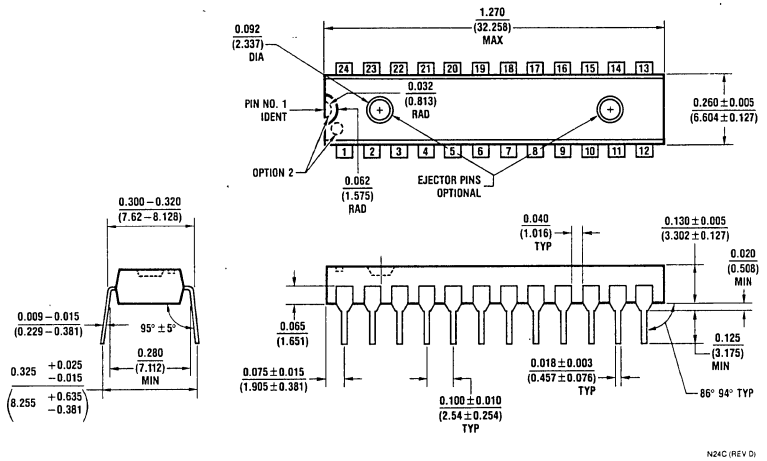


NS Package N20A

N20A (REV D)



N24C (REV D)

NS Package N24C

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